12-2018

Stability Analysis of a High-Power Microgrid

David Manuel Carballo Rojas
University of Arkansas, Fayetteville

Stability Analysis of a High-Power Microgrid

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

by

David Carballo Rojas
University of Arkansas
Bachelor of Science in Electrical Engineering, 2016

December 2018
University of Arkansas

This thesis is approved for recommendation to the Graduate Council

_____
Juan Carlos Balda, Ph.D.
Thesis Director

_____
Roy A. McCann, Ph.D.
Committee Member

_____
Simon Ang, Ph.D.
Committee Member

ABSTRACT

The objective of this thesis is to perform the modeling and stability analysis of a high-power microgrid with multiple parallel-and grid connected voltage source converters using the system parameters from the high-power microgrid testbed at the National Center for Reliable Electric Power Transmission (NCREPT) at the University of Arkansas in order to identify, minimize, if not eliminate, the potential instabilities that can affect the proper operation of the microgrid testbed. To achieve this objective, the mathematical modeling of the high-power microgrid considering the adverse effects of resonances due to interactions among the converter LCL output filters is presented and analyzed. Moreover, the stability range of the high-power microgrid under different conditions is examined using the root locus analysis technique and the theoretical analysis is validated through MATLAB/Simulink™ simulations. The results from this analysis are then used to develop general guidelines to avoid resonance and stability issues when connecting power converters into a microgrid.

In addition, a scaled-down prototype of the high-power microgrid testbed at NCREPT, the so-called "mini-NCREPT", is designed and constructed to reproduce some of the issues already encounter in the high-power tested and to developed countermeasures in a laboratory environment without the safety restrictions typical of high-power applications. Furthermore, this scaled-down prototype can be used in future applications to test advanced microgrid control algorithms before deploying them at the high-power microgrid testbed. Finally, an in-depth analysis of the experimental results of the scaled-down prototype is presented and solutions to improve the power quality of the system are suggested.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my Ph.D. advisor Dr. Juan Carlos Balda for giving me the opportunity to work on this project and for all his support and guidance. I want to extend my gratitude and thankfulness to my committee members Dr. Roy a. McCann and Dr. Simon Ang for all their support. Moreover, I would especially like to thank Vinson Jones for his patience, guidance, and motivation. Vinson was not only the best lab mate I could have asked for but also an amazing friend, and I wish him a future full of happiness and success.

Finally, I would also like to thank my friends and fellow students: Edgar Escala, Rafael Franceschi, Luciano García, Obaid Aldosari, Daniel Schwartz, Jeremy Lingo, Haider Mhiesan, Tyler Adamson, Waleed Alhosaini, Hazzaz Mahmud, Shuang Zhao……

DEDICATION

To my beloved parents, Manuel Carballo and Berta Rojas, and all my friends who were always there for me and provided unconditional love and support.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF PUBLISHED PAPERS

CHAPTER TWO

[1] D. Carballo, E. Escala and J. C. Balda, "Stability Analysis of Multiple Grid-Connected Inverters Using Different Feedback Currents," *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Charlotte, NC, 2018, pp. 1-7.

CHAPTER THREE

[2] D. Carballo, E. Escala and J. C. Balda, "Modeling and Stability Analysis of Grid-connected Inverters with Different LCL Filter Parameters," *2018 IEEE Electronic Power Grid (eGrid)*, Charleston, SC, 2018.

CHAPTER 1

INTRODUCTION

1.1 Motivation for this Research Work

Modern society has become heavily reliant on a constant and secure supply of electric energy to the point where access to electricity is deemed as a right and a fundamental necessity [1]. For about one hundred years, the electrical infrastructure has been responsible for this constant delivery of energy. During that time, this infrastructure has remained mainly unchanged. Despite the aging of the electrical grid, the demand for electricity has steadily increased with the growth of the world population. The current electrical infrastructure, however, is not suited for these growing needs and demands, including resiliency in the face of natural and man-made disasters [2].

The existing electric grid has a centralized power generation with a unidirectional power flow where the electricity is generated far away from the load and is distributed through transmission and distribution lines. One of the deficiencies of the current grid is that it suffers from domino-effect failure because of this hierarchical and unidirectional design [3]. This has been seen in the Northeast blackout of 2003 where an overload of the transmission lines cascaded into the collapse of the electric grid for up to two days [4]. Another issue is that the system is somewhat inefficient with 8 percent of the generated energy being lost on the transmission lines and about 20 percent of the generated capacity being only available for peak demand (i.e., being operated only during a small percentage of the time). In addition, the electricity industry has been a contributing cause of greenhouse gas emissions due to the disproportionate use of fossil fuels [3]. Subsequently, innovative solutions, technologies and grid architectures are needed to address these issues and challenges.

In the last decades, the concept of microgrids was developed due to advancements in power electronics as well as innovations in small-scaled distributed power generation [5]. Microgrids offer solutions to the issues affecting the current electrical infrastructure through the integration of distributed energy resources (DERs). These DERs include distributed generation (DG) units with renewable sources like photovoltaic (PV) modules, wind turbines, micro-turbines, combined cooling, heat and power (CCHP), as well as distributed storage (DS) units such as flywheels, energy capacitors and batteries [1]. The integration of these DERs allows the reduction of carbon emissions due to the use of renewable energy sources instead of fossil fuels, thus, allowing countries to meet their goal of reducing greenhouse gas emission in compliance with the Kyoto protocol [6]. Moreover, since it is generated at the distribution level, the power does not have to "travel" through long transmission lines to reach the final users. Consequently, the system becomes more efficient due to the reduction of transmission losses. Other benefits include: increase of power quality and reliability by supporting and reducing dips in voltage, increase of resiliency, and a potentially decrease on the cost of energy supply [6].

Fig. 1.1 illustrates a typical microgrid structure which comprises a portion of the electric power distribution system and includes various DG, DS, and loads. As seen in the figure, different renewable energy sources and energy storages are connected at the distribution level at the point of common coupling (PCC) to provide power to nearby loads. One of the most promising features of the microgrid is the ability to operate in either grid-connected or islanded mode and to be able to switch between those two modes [7]. In the grid-connected mode, the connection at the PCC is closed; thus, the main grid can provide the deficit power that the microgrid needs for the local loads while the microgrid can trade the excess power generated by the local sources to the main grid [7]. In the islanded mode, the connection at the PCC is

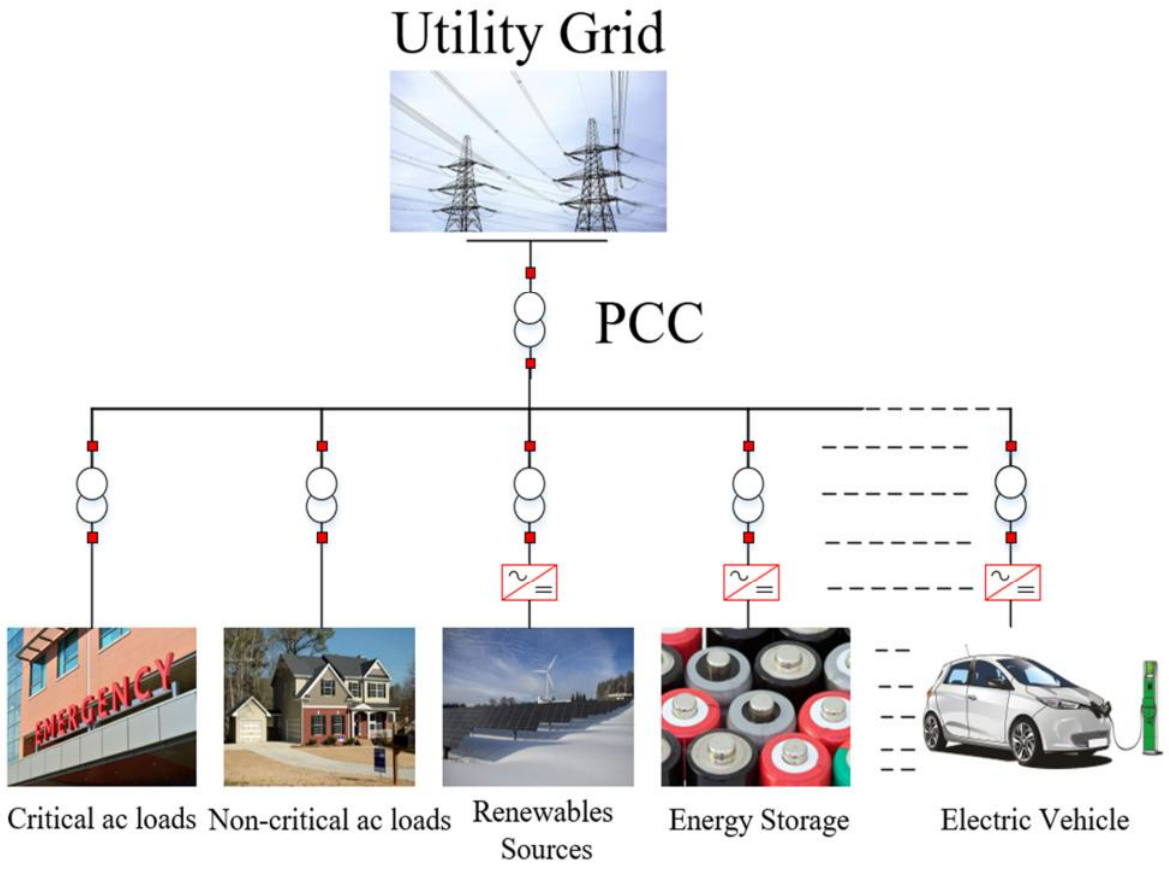


Fig. 1.1: A typical microgrid structure with DG, DS and loads.

opened; thus, the microgrid needs to have enough generating and storing capacities to balance the active and reactive powers demanded by the local loads after being disconnected from the utility system at the PCC [7], [8]. Because of the limited amount of available power in islanded mode, the microgrid might need to apply load shedding schemes to disconnect non-critical loads when an islanded event has been detected. This feature of being able to function autonomously from the macrogrid greatly increases the resiliency of the system since the microgrid can provide power to the local loads regardless of issues on the main grid.

Power electronics converters, as represented by the red boxes in Fig. 1.1, are normally used for the DERs to interface with the microgrid in order to achieve power flow regulation and

power factor correction [9]. The most common topology for these power electronic converters are based on pulse-width-modulation (PWM) voltage-source converters (VSC) [10]. The use of these power electronic converters allows for a better control and flexibility on the operation of the energy sources with respect to conventional rotational machines [5]. However, the output of these VSCs produces high-frequency pulse-width-modulation (PWM) harmonics that are injected into the grid and may damage sensible load and equipment [11]. For this reason, those harmonic components need to be reduced to achieve good power quality at the grid and comply with IEEE standards (IEEE 1547-2018) [12].

An output filter interface is usually placed between the power electronic converter and the point of connection to the microgrid in order to effectively eliminate these switching frequency harmonics [13]. The inductive-capacitive-inductive (LCL) filter has become the most popular choice in grid-connected applications due to a higher attenuation of the PWM switching harmonics, with an overall reduction on the weight and size of the filter when compared with the conventional L- and LC-filters [9]–[11], [13], [14]. However, the integration of this LCL filter increases the control complexity of the DERs because of the introduction of a resonance frequency that can cause instabilities in the microgrid [9], [14]. A detailed analysis and guidelines to avoid the instability caused by the LCL filters of the power converters are proposed in later chapters.

Although the concept of microgrid addresses many of the issues with the current electrical infrastructure, it also brings many challenges. One of the concerns is related to the physical inertia of a microgrid. Unlike bulk power systems, microgrids show an almost negligible physical inertia which could make the system more susceptible to oscillations due to network disturbances [5], [7]. Other challenges are related to the overall control and management

of the microgrid in terms of power sharing, stability, power quality, environmental influence and economic issues [15], [16].

Despite these challenges, microgrids have gained a lot of attention worldwide due to their promising benefits. In fact, many research facilities have begun building microgrid testbeds to demonstrate these benefits, to address some of the existing challenges in control and management of the DERs, and to identify other rising issues and challenges. Usually, these microgrid testbeds are rated in the kVA range and are comprised of different energy sources and storages, variable loads and protecting devices [17]–[19].

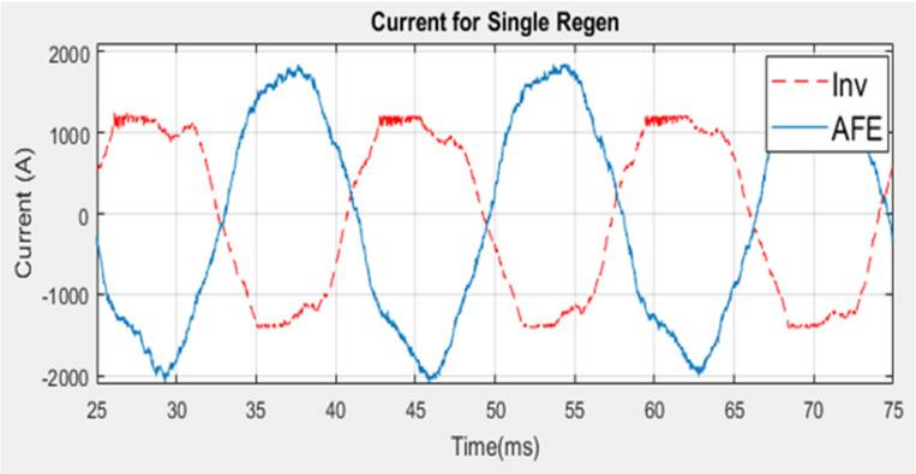
In addition, a growing interest is being presented on building and developing high-power microgrids in the MVA range [20]–[22]. These microgrids could have renewable sources with VSC with power ratings ranging from hundreds of kVA to some MVA. However, considering switching losses, heat management and fundamental voltage drops, the control and design of these VSCs as well as their LCL filter poses more restrictions and challenges than their lower-power counterpart [13]. For instance, their switching frequency is limited to a few kHz which usually places the resonance frequency of the LCL filter close to the switching/sampling frequency of the converters [10], [13]. This can place the operation and control of the VSC near an unstable region [14]. Another issue is that coupling between DERs in the grid-connected mode due to the grid impedance can worsen the resonance issues and stability of the system [23]. At lower power, this coupling might be ignored since the parameters of the LCL filter are larger than grid impedance. Nevertheless, this coupling plays a significant role in the stability of the system at higher power since the filter parameters might be on the same order of magnitude as the grid impedance [24].

Considering the growing interest on high-power microgrids and how different factors and restrictions can affect the stability of the system, there is a need for a stability analysis that determines how these different factors and conditions might affect the stable operation of a high-power microgrid. Ultimately, this stability analysis will allow the development of guidelines that can guarantee the stability of a microgrid and can reduce the engineering required to implement these high-power microgrids around the world.

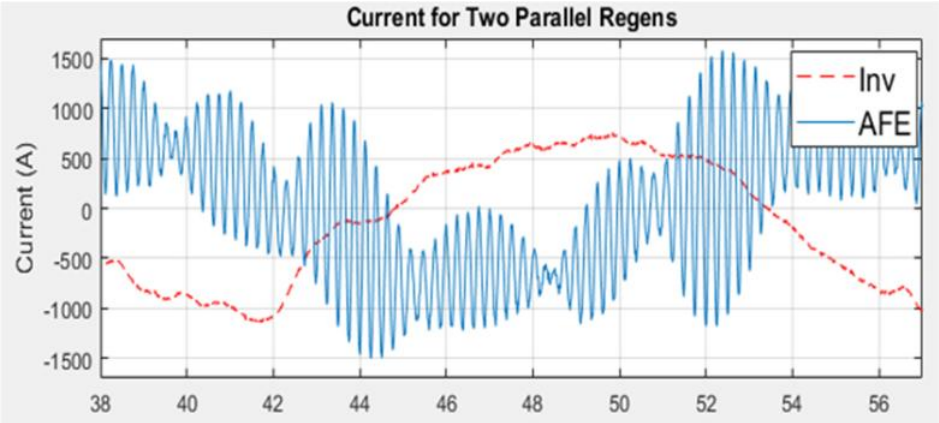
In this thesis, a stability analysis will be performed on the high-power microgrid testbed at the National Center for Reliable Electric Power Transmission (NCREPT) at the University of Arkansas. This high-power testbed allows the parallel operation of three identical 2 MVA rated back-to-back VSC, called regen benches, with the ultimate objective of emulating a microgrid with different grid-connected DERs. A more in-depth description of this high-power microgrid testbed is presented in [25].

One of the main motivations of performing the stability analysis of the high-power microgrid at NCREPT is that the current control approach of the regen benches causes the system to operate in a near unstable region when multiple VSCs (regen benches) are connected in parallel to the grid. This near unstable operation affects the power quality of the system when the multiple regens inject/extract power into/from the grid. Fig. 1-2 illustrated the operation of a single and multiple regen benches. Fig. 1-2(a) shows that when only one of the regen benches is recirculating power, the current waveforms show acceptable results with mainly low-frequency harmonics. However, the current waveforms become more distorted with high-frequency harmonics when two regen benches are recirculating power at the same time, as illustrated in Fig. 1-2(b). The reason for this instability is that the controller of the regen benches was initially developed following the design guidelines for motor drives. However, the emerging research in

microgrids has shown that these conventional guidelines do not account for the coupling and interactions between VSCs in the microgrid, thus, causing the system to deviate from its expected behavior and causing potential stability issues [23], [26].



(a)



(b)

Fig. 1.2: Experimental current waveforms for NCREPT in the grid-connected mode for (a) a single regen bench, and (b) two parallel regen benches.

1.2 Objectives of Thesis

The main objective of this thesis is to perform a stability analysis of a high-power microgrid with multiple parallel- and grid-connected VSCs using the system parameters from the microgrid testbed at NCREPT in order to identify, minimize, if not eliminate, the potential instabilities that can affect the proper operation of the microgrid testbed. To accomplish this goal, the modeling of the high-power microgrid with multiple parallel VSCs whose dynamics are coupled due to the grid inductance is revised and analyzed. Then, the stability regions of the microgrid is determined by analyzing the closed-loop transfer function of the system. Next, changes in the VSCs controller are implemented to improve the range of these regions of stability. Finally, the theoretical analysis is validated through MATLAB/Simulink™ simulations.

Another important objective of this thesis is to develop a scaled-down prototype of the high-power microgrid at NCREPT; the so-called "mini-NCREPT". Using this scaled-down prototype will enable to reproduce issues already encountered in the high-power testbed and to develop countermeasures in an environment where a catastrophic failure will not result in expensive damaged components. Moreover, different advanced control algorithms for power sharing, compensation for deviations in voltage and frequency, and economic concerns in the optimal operation of the microgrid can be tested in the scaled-down prototype before deploying them at the high-power microgrid.

1.3 Organization of Thesis

This thesis is organized as follows: Chapter 2 will develop the mathematical modeling and stability analysis of identical multiple grid-connected VSCs having the same system parameters as the microgrid testbed at NCREPT. Chapter 3 will also develop a similar modeling and stability analysis but with high-power grid-connected VSCs that have different LCL filters

parameters. The design of the scaled-down prototype is documented in Chapter 4 and the implementation of the control algorithm in a microcontroller is presented in Chapter 5. The experimental results of the scaled-down prototype are given in Chapter 6. Finally, conclusions and recommendations for future work are given in Chapter 7.

1.4 References

[1] A. Oudalov, T. Degner, F. van Overbeeke, and J. M. Yarza, “Microgrid: Architectures and Control - Chapter 2,” *Microgrids Architecture and Control*, pp. 1–24, 2003.

[2] V. C. Gungor *et al*., "Smart Grid Technologies: Communication Technologies and Standards," in *IEEE Transactions on Industrial Informatics*, vol. 7, no. 4, pp. 529-539, Nov. 2011.

[3] H. Farhangi, "The path of the smart grid," in *IEEE Power and Energy Magazine*, vol. 8, no. 1, pp. 18-28, January-February 2010.

[4] G. Andersson *et al*., "Causes of the 2003 major grid blackouts in North America and Europe, and recommended means to improve system dynamic performance," in *IEEE Transactions on Power Systems*, vol. 20, no. 4, pp. 1922-1928, Nov. 2005.

[5] N. Pogaku, M. Prodanovic and T. C. Green, "Modeling, Analysis and Testing of Autonomous Operation of an Inverter-Based Microgrid," in *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 613-625, March 2007.

[6] N. Hatziargyriou, H. Asano, R. Iravani and C. Marnay, "Microgrids," in *IEEE Power and Energy Magazine*, vol. 5, no. 4, pp. 78-94, July-Aug. 2007.

[7] D. E. Olivares *et al*., "Trends in Microgrid Control," in *IEEE Transactions on Smart Grid*, vol. 5, no. 4, pp. 1905-1919, July 2014.

[8] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna and M. Castilla, "Hierarchical Control of Droop-Controlled AC and DC Microgrids—A General Approach Toward Standardization," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 158-

[9] Erika Twining and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," in *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 888-895, May 2003.

[10] E. Kantar and A. M. Hava, "LCL-filter design for low-voltage high-power grid-tied voltage-source converter considering various damping methods," *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Trondheim, 2016, pp. 1-8.

[11] D. Yoon, H. Jeong and K. Lee, "The design of an LCL-filter for the three-parallel operation of a power converter in a wind turbine," *2010 IEEE Energy Conversion Congress and Exposition*, Atlanta, GA, 2010, pp. 1537-1544.

[12] IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources with Associated Electric Power Systems Interfaces," in *IEEE Std 1547-2018 (Revision of IEEE Std 1547-2003)*, vol., no., pp.1-138, 6 April 2018

[13] Z. Qiu and G. Chen, "Study and Design of Grid Connected Inverter for 2 MW Wind Turbine," *2007 IEEE Industry Applications Annual Meeting*, New Orleans, LA, 2007, pp. 165-170.

[14] S. G. Parker, B. P. McGrath and D. G. Holmes, "Regions of Active Damping Control for LCL Filters," in *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 424-432, Jan.-Feb. 2014.

[15] L. Meng, M. Savaghebi, F. Andrade, J. C. Vasquez, J. M. Guerrero and M. Graells, "Microgrid central controller development and hierarchical control implementation in the intelligent microgrid lab of Aalborg University," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 2585-2592.

[16] F. Farzan, S. Lahiri, M. Kleinberg, K. Gharieh, F. Farzan and M. Jafari, "Microgrids for Fun and Profit: The Economics of Installation Investments and Operations," in *IEEE Power and Energy Magazine*, vol. 11, no. 4, pp. 52-58, July-Aug. 2013.

[17] R. H. Lasseter *et al*., "CERTS Microgrid Laboratory Test Bed," in *IEEE Transactions on Power Delivery*, vol. 26, no. 1, pp. 325-332, Jan. 2011.

[18] M. Liu, Z. Ding, F. L. Quilumba, W. Lee and D. A. Wetz, "Using a Microgrid test bed to evaluate the strategies for seamless renewable energy integration," *2014 IEEE/IAS 50th Industrial & Commercial Power Systems Technical Conference*, Fort Worth, TX, 2014, pp. 1-9.

[19] J. Eto *et al*., "Overview of the CERTS Microgrid laboratory Test Bed," *2009 CIGRE/IEEE PES Joint Symposium Integration of Wide-Scale Renewable Resources Into the Power Delivery System*, Calgary, AB, 2009, pp. 1-1.

[20] H. Xie, S. Zheng and M. Ni, "Microgrid Development in China: A method for renewable energy and energy storage capacity configuration in a megawatt-level isolated microgrid.," in *IEEE Electrification Magazine*, vol. 5, no. 2, pp. 28-35, June 2017.

[21] C. Marnay, N. DeForest and J. Lai, "A green prison: The Santa Rita Jail campus microgrid," *2012 IEEE Power and Energy Society General Meeting*, San Diego, CA, 2012, pp. 1-2.

[22] M. C. Such and G. Y. Masada, "BESS control on an microgrid with significant wind generation," *2017 IEEE Power & Energy Society General Meeting*, Chicago, IL, 2017, pp. 1-5.

[23] M. Lu, X. Wang, P. C. Loh and F. Blaabjerg, "Resonance Interaction of Multiparallel Grid-Connected Inverters With LCL Filter," in *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 894-899, Feb. 2017.

[24] Y. Liu, C. Farnell, H. A. Mantooth, J. C. Balda, R. A. McCann and C. Deng, "Resonance propagation modeling and analysis of AC filters in a large-scale microgrid," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 143-149.

[25] Y. Liu, C. Farnell, J. C. Balda and H. A. Mantooth, "A 13.8-kV 4.75-MVA microgrid laboratory test bed," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 697-702.

[26] J. L. Agorreta, M. Borrega, J. López and L. Marroyo, "Modeling and Control ofN-Paralleled Grid-Connected Inverters With LCL Filter Coupled Due to Grid Impedance in PV Plants," in *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 770-785, March 2011.

CHAPTER 2

STABILITY ANALYSIS OF MULTIPLE GRID-CONNECTED INVERTERS USING DIFFERENT FEEDBACK CURRENTS

D. Carballo, E. Escala and J. C. Balda, "Stability Analysis of Multiple Grid-Connected Inverters Using Different Feedback Currents," *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Charlotte, NC, 2018, pp. 1-7.

Abstract

Distributed generation is gaining greater penetration levels in distribution grids due to government incentives for integrating distributed energy resources (DERs) and DER cost reductions. The frequency response of a grid-connected single inverter changes as other inverters are connected in parallel due to the couplings among grid inductance and/or inverter output filters. The selection of the inverter- or grid-side currents as feedback control signals is then not trivial because each one has tradeoffs. This paper analyses the system stability for multiple parallel- and grid-connected inverters using the inverter- or grid-side currents as feedback signals. Modeling of both feedback signals is performed using the current separation technique. Moreover, the stability range for different conditions including active damping is analyzed through the root locus technique. The grid-side current has a wider range of stability, but the inverter-side current allows for higher values of the proportional gain near the critical frequency and no extra sensors are needed since measurement of the inverter current is needed for protection in high-power applications.

2.1 Introduction

Microgrids have several advantages like effective integration of distributed energy resources (DERs) into distribution networks to allow for bidirectional power flows, and reduced transmission and distribution losses. Interfaces between DERs and microgrids are often based on power converters (inverters) with LCL filters that provide a higher damping capability (-60 dB/dec) in comparison with a simple L filter (-20 dB/dec) [1]. However, LCL filters introduce resonance issues that can cause current-controller instability and that can become more severe as more power electronics devices are connected to the grid [2]. The scenario becomes more challenging when DER converters of higher power ratings are used while the voltage levels remain in the low-voltage range (208 V ~ 480 V). This results in a much smaller base impedance value on a per-unit (p.u.) basis, making the filter inductor values on the same order as the grid impedance and, thus, increasing the possibility of any instability issue caused by coupling between inverter and grid impedances [1]. Therefore, a stability analysis of the potential interactions between several parallel LCL filters and their effects on current controllers is crucial for satisfactory system performance.

Either the grid- or inverter-side currents can be selected for feedback in a DER current controller. While grid-side currents are usually selected because of direct control of the grid-injected currents, using the inverter-side currents may present some advantages like faster fault current interruption and an inherent damping term in the transfer function [3-4]. The authors of [5] performed a comparison that demonstrated tradeoffs when using these two current-control approaches for only a single inverter. Although the authors of [6-7] presented an analysis on the range of the proportional gain of the current controller for multiple grid-connected inverters, they only considered the grid-side currents for feedback purposes. The work presented here expands

upon the stability analysis in [4-8] to evaluate the stability regions for multiple grid-connected inverters when using the inverter-side currents for feedback with the main goal of determining tradeoffs between these two current-feedback approaches.

This paper is organized as follows: Section 2.2 presents an overview of the modeling of the inverter- and grid-side currents, Section 2.3 evaluates the system stability with and without the use of active damping, Section 2.4 analyzes simulation results, and Section 2.5 provides the main conclusions.

2.2 Modeling of the Parallel Inverters

2.2.1 Inverter-Side Current- Mathematical Modeling

Multiple paralleled grid-connected inverters are illustrated in Fig. 2.1, where Z_1 and Z_2 are the s-domain impedances of the inverter- and grid-side filter inductances, Z_3 is the filter capacitive impedance, Z_g is the grid impedance, and the second subscript refers to the inverter number. Using the principle of superposition to remove the influence of the grid and the other inverter voltages, and assuming that the inverters are equal (i.e., same LCL filter parameters), the inverter-side currents i_{1j} (j=1, 2,..n) with respect to the inverter voltages can be written as:

$$\begin{pmatrix} i_{11} \\ i_{12} \\ \dots \\ i_{1n} \end{pmatrix} = \begin{pmatrix} G_{11} & G_{12} & \dots & G_{12} \\ G_{12} & G_{11} & \dots & G_{12} \\ \dots & \dots & \dots & \dots \\ G_{12} & G_{12} & \dots & G_{11} \end{pmatrix} \cdot \begin{pmatrix} v_{01} \\ v_{02} \\ \dots \\ v_{0n} \end{pmatrix}. \quad (1)$$

where G11 and G12 are calculated as follows [6]:

$$G_{11} = \frac{n-1}{n} G_{inv} + \frac{1}{n} G_{coupling_{inv}}, \quad (2)$$

$$G_{12} = -\frac{1}{n} G_{inv} + \frac{1}{n} G_{coupling_{inv}}, \quad (3)$$

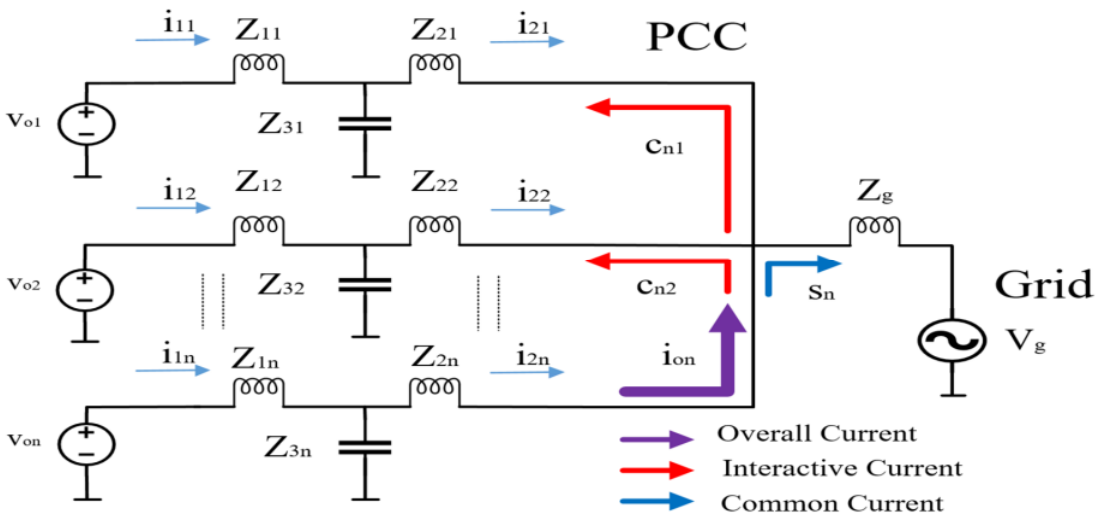


Fig. 2.1: Schematic of multiple paralleled grid-connected inverters.

with G_{inv} the transfer function of the LCL filter and $G_{coupling_{inv}}$ the transfer function including the effects of the grid impedance. Both are presented below:

$$G_{inv} = \frac{(Z_3 + Z_2)}{Z_1Z_2 + Z_1Z_3 + Z_2Z_3} = \frac{s^2 + \omega_0^2}{L_1 s(s^2 + \omega_{res}^2)} \tag{4}$$

$$G_{coupling_{inv}} = \frac{(Z_3 + Z_2 + nZ_g)}{Z_1Z_2 + Z_1Z_3 + Z_2Z_3 + nZ_g(Z_3 + Z_1)} = \frac{s^2 + \omega_{01}^2}{L_1 s(s^2 + \omega_{res1}^2)} \tag{5}$$

where ω_{res} and ω_o are the LCL filter resonance and antiresonance frequencies, and $\omega_{res1}$and ω_{o1} are the resonance and antiresonance frequencies taking into account the coupling with the grid inductance with n paralleled inverters (all in rad/s):

$$\begin{cases} \omega_{res} = 2\pi f_{res} = \sqrt{(L_1 + L_2)/(L_1 L_2 C_f)}, \\ \omega_o = 2\pi f_o = \sqrt{1/(L_2 C_f)}, \\ \omega_{res1} = 2\pi f_{res1} = \sqrt{(L_1 + L_2 + nL_g)/(L_1(L_2 + nL_g)C_f)}, \\ \omega_{o1} = 2\pi f_{o1} = \sqrt{1/((L_2 + nL_g)C_f)}. \end{cases} \tag{6}$$

From (1), the first-inverter-side currents are given by

$$i_{11} = \frac{1}{n} G_{inv}(v_{01} - v_{02}) + \cdots + \frac{1}{n} G_{inv}(v_{01} - v_{0n}) + \frac{1}{n} G_{coupling_{inv}} (v_{01} + \cdots + v_{0n}). \quad (7)$$

From (7) the inverter-side currents i_{11} have two components: the interactive one which circulates between two inverters and the common one that is injected into the grid, as illustrated in Fig. 2.1 [6-7].

2.2.2 Grid-Side Current- Mathematical Modeling

Following the same process as in the previous section and presented in [6], the grid-side currents i_{2j} $(j = 1,2,..n)$ with respect to the inverter voltages can be written like (1)-(3) but with different transfer functions for the LCL filter and the coupling term:

$$G_{11} = \frac{n-1}{n} G_{grid} + \frac{1}{n} G_{coupling_{grid}} \quad (8)$$

$$G_{12} = -\frac{1}{n} G_{grid} + \frac{1}{n} G_{coupling_{grid}} \quad (9)$$

$$G_{grid} = \frac{Z_3}{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3} = \frac{1}{L_1 L_2 C_f s(s^2 + \omega_{res}^2)} \quad (10)$$

$$G_{coupling_{grid}} = \frac{Z_3}{Z_1 Z_2 + Z_1 Z_3 + Z_2 Z_3 + nZ_g(Z_3 + Z_1)} = \frac{1}{sL_1 C_f (L_2 + nL_g)(s^2 + \omega_{res1}^2)} \quad (11)$$

Like (7), the first-grid-side currents can be expressed as:

$$i_{21} = \frac{1}{n} G_{grid}(v_{01} - v_{02}) + \cdots + \frac{1}{n} G_{grid}(v_{01} - v_{0n}) + \frac{1}{n} G_{coupling_{grid}} (v_{01} + \cdots + v_{0n}) \quad (12)$$

comprising interactive and common currents shown in Fig. 2.1.

2.3 Stability Analysis and Active Damping

2.3.1 Control Strategy

The block diagram of a single current-control loop for the inverter-side current feedback in the s-domain is presented in Fig. 2.2 (a). In the figure, i_1^* represents the reference current commanded to the controller, G_{d-DSP} the DSP computational delay, K_{pwm} the linear response of the inverter with gain of $K_{pwm} = V_{dc}/\sqrt{3}$ for a space vector modulation implementation, and G_{PI} the PI controller chosen in this paper:

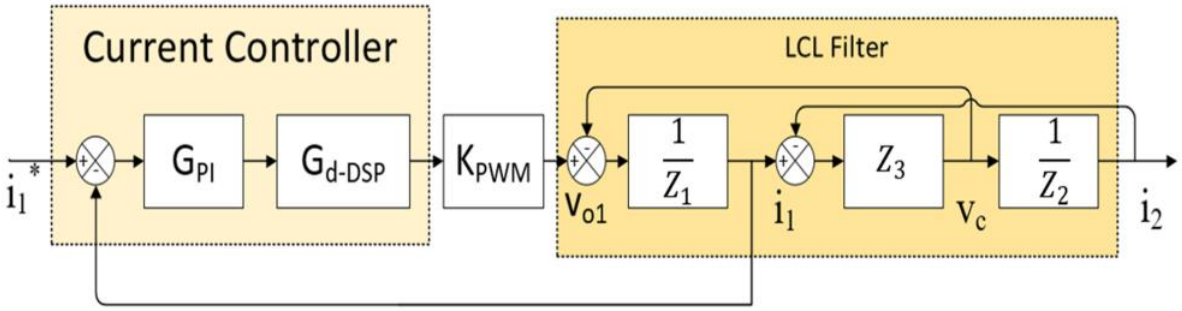
$$G_{PI}(s) = K_P + \frac{K_i}{s} \tag{13}$$

The current controller in Fig. 2.2(a) as modeled in the z-domain is in Fig. 2.2(b) since the DSP is a discrete system. In the figure, the PI controller in (13) is discretized by applying a Tustin transform with prewarping while a zero-order-hold (ZOH) transform is applied to the transfer function of the LCL filter [2]. Moreover, a sample delay z^{-1} accounts for the delay of the DSP. Although both figures are shown using the inverter-side current as reference, the same control diagram can be implemented for the grid-side current just by changing the respective current feedback and reference.

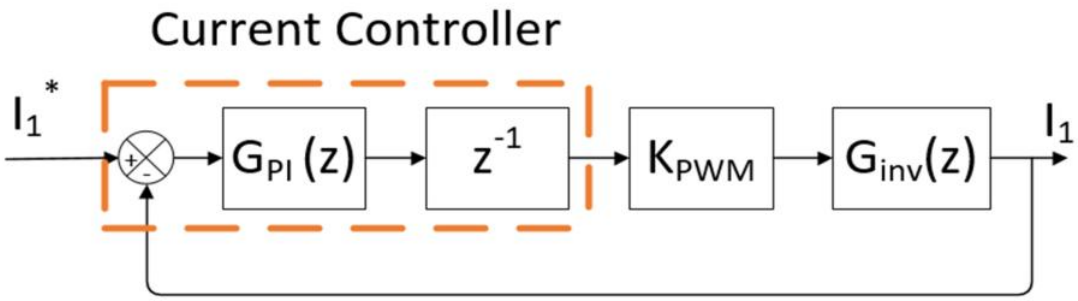
Considering the current controller from Fig. 2.2(b) and the result from (7), the closed-loop transfer function for the interactive and common currents are respectively given by:

$$C_{ij} = \frac{1}{n}\frac{G_{inv}(z)H}{(1+G_{inv}(z)H)}(i_{1i}^* - i_{1j}^*) \tag{14}$$

$$S_i = \frac{1}{n}\frac{G_{coupling\,inv}(z)H}{(1+G_{coupling\,inv}(z)H)}(i_{1i}^* - i_{1j}^*) \tag{15}$$



(a)



(b)

Fig. 2.2: Current control model (a) s-domain (b) z-domain.

where

$$H = G_{PI}(z)z^{-1}K_{pwm}. \tag{16}$$

2.3.2 Stability Analysis for the Inverter-Side Current Case

The system stability is determined by applying the root locus analysis to the open-loop forward path of (14) and (15). A system with multiple grid-connected inverters is only stable when the proportional gains of the current controllers are selected such that all values of the transfer functions for the interactive and common currents are inside the unit circle [6-7].

Furthermore, [2] showed that there is relation between a critical frequency of one sixth of the sampling frequency f_s and the LCL filter resonance f_{res} (or f_{res1}) that will determine whether the system can be stable for a single-loop feedback control. For the inverter-side current control,

the system will only be stable if the resonance frequency is less than the critical frequency (i.e., $f_{res} < f_s/6$ and $f_{res1} < f_s/6$).

Fig. 2.3 shows the root loci of the interactive and common currents for the inverter-side feedback for different number of inverters using the parameters from the high-power microgrid testbed described in [9] and presented in Table 2.1 for convenience. The resonance frequency ω_{res} for the interactive current stability is calculated from (6) and the parameters in Table 2.1. The LCL filter resonance frequency (1.52 kHz) is higher than the critical frequency (1.33 kHz), so the system is interactively unstable for the inverter-side current control. Fig. 2.3 corroborates this since the poles of the LCL filter are placed outside the unit circle for all values of the proportional gain for the interactive current.

However, there is a range where the system is stable for the common current due to a shift in the frequency of the poles and zeroes of the filter resonance and antiresonance frequencies. This stability range for selected number of inverters is given by:

$$K_p Range = \begin{Bmatrix} 0 < K_p < 0.0709, n = 3 \\ 0 < K_p < 0.0822, n = 15 \\ 0 < K_p < 0.0844, n = 50 \end{Bmatrix}. \quad (17)$$

From (17), the stable range of the proportional gain increases as the number of inverters increases but converging towards a maximum value. Nonetheless, the entire system will always be unstable since the system is interactively unstable requiring additional damping when using the inverter-side currents.

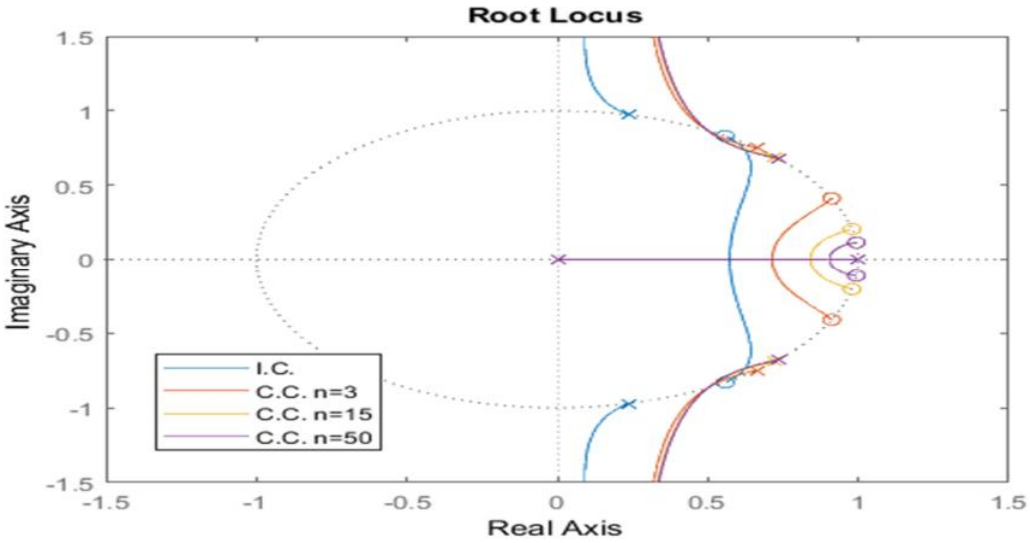


Fig. 2.3: Root loci of the inverter-side current for interactive (I.C) and common currents (C.C).

TABLE 2.1: SYSTEM PARAMETERS

Circuit Parameter	Formula	Nominal Value
Power Rating	S_b	2.0 MVA
Voltage Rating	V_b	480 V
Inverter-Side Inductor	L_1	20 µH
Grid-Side Inductor	L_2	12.2 µH
Filter Capacitor	C_f	Δ3x 480 µH
Resonance Frequency	f_r	1.52 kHz
Sampling Frequency	f_s	8 kHz
Critical Frequency	$f_s/6$	1.33 kHz

Similarly, the LCL resonance frequency ω_{res1} for the common current stability can be calculated from (6). This equation shows that as the number of inverters increase, the resonance frequency decreases. For this reason, increasing the number of inverters could reduce the resonance frequency to a value lower than the critical frequency, making the system commonly stable for the inverter-side current.

Active Damping Control

A system using inverter-side current feedback with the critical frequency near the resonance frequency would require that the controller provides damping to move the poles of the resonance inside the unit circle. Proposed solutions for adding damping can be broadly classified in passive and active algorithms. The ESRs of the various components are normally small so they might not be able to make the system stable in high-power applications. Adding a passive resistor to damp the resonances introduces high power losses. Thus, the best solution is to use active damping algorithms which will reduce the resonances without introducing power losses [2, 10].

In this paper, the capacitor-voltage feedforward active damping algorithm is implemented [10-12]. The main reason for selecting this scheme is that no additional sensors are needed since the capacitor voltage is usually measured to synchronize the inverters with the grid through the phase-locked loop (PLL) algorithm. Moreover, reduction of large inrush currents during startup and suppression of the grid disturbances can be achieved using this active damping algorithm [11].

The block diagram of the dual-loop control system for the inverter-side current feedback with capacitor-voltage active damping is illustrated in Fig. 2.4. In this figure, K_{ff} is the gain of the feedforward control path, and $G_{cv}(z)$ is the transfer function of the capacitor voltage with respect to the inverter voltage, given by:

$$G_{cv}(s) = \frac{v_c(s)}{v_o(s)} = \frac{1}{L_1 C_f (s^2 + \omega_{res}^2)},$$

$$G_{cv}(z) = ZOH(G_{cv}(s)). \tag{18}$$

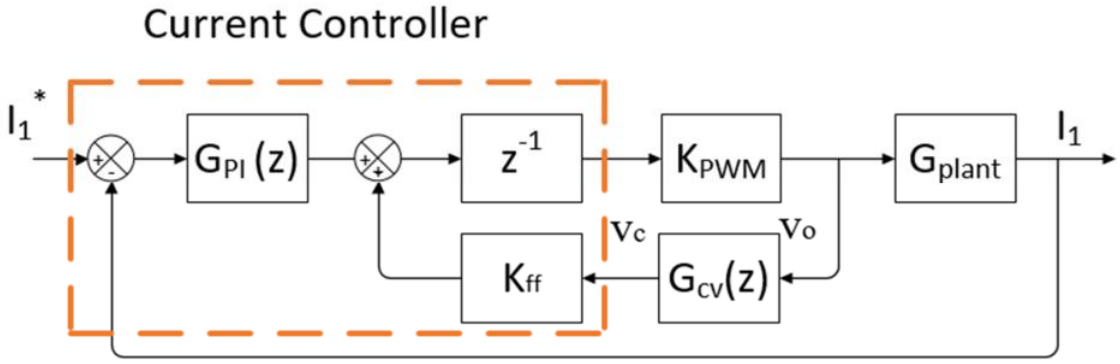


Fig. 2.4: Current control model in z-domain with capacitor-voltage feedforward active damping.

Considering the current controller with this active damping algorithm and the result from (7), the new closed-loop transfer functions for the interactive and common currents are the same ones as (14) and (15) but with a new transfer function for (16), given by:

$$H = \frac{G_{PI}(Z) z^{-1} K_{PWM}}{1 - z^{-1} K_{PWM} K_{ff} G_{cv}(z)} \ . \tag{19}$$

Using this equation, Fig. 2.5 shows the root loci of the interactive and common currents for the inverter-side current feedback using unit capacitor-voltage feedforward gain (i.e., $K_{ff} = 1$).

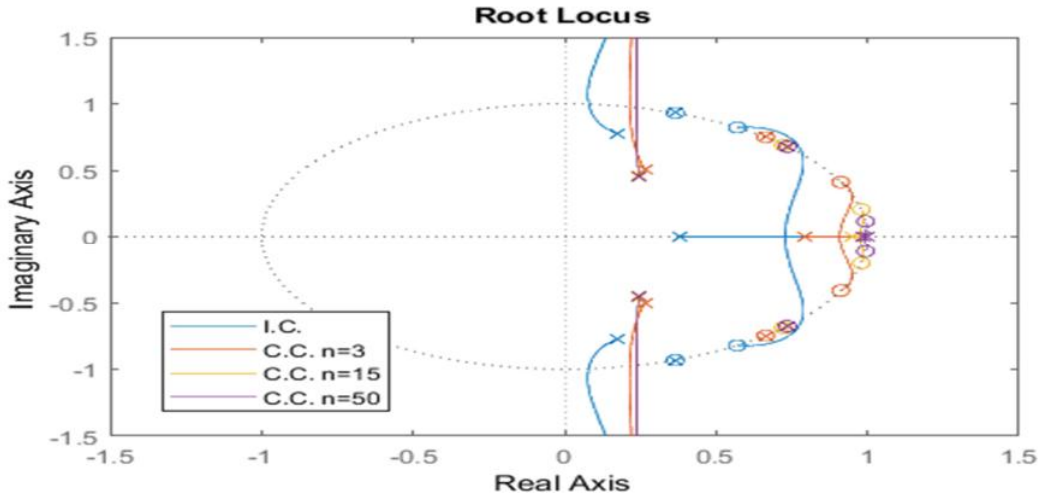


Fig. 2.5: Root loci of the interactive and common currents for inverter-side feedback with capacitor-voltage feedforward algorithm.

Unlike the previous case, the poles of the system are now inside the unit circle for the interactive current. Thus, the system is interactively stable as long as the proportional gain is properly selected from 0 to 0.111. Similarly, the system will continue to have common current stability with a higher range of stability from K_p varying from 0 to 0.131. Applying this feedforward technique extends the limit of the resonance frequency up to one third of the sampling frequency (i.e., $f_r < f_s/3$) provided that:

$$\cos(\omega_{res1} T_s) > -\frac{L_1}{2L_1 + 3(L_2 + nL_g)} \text{ [11].} \tag{20}$$

2.3.3 Stability Analysis for the Grid-Side Current Case

A system with grid-side feedback will only be stable if the resonance frequencies of both the interactive and common currents are greater than the critical frequency (i.e., $f_{res} > f_s/6$ and $f_{res1} > f_s/6$) [2]. Following the same analysis as the case for the inverter-side feedback, it is expected that the system be interactively stable for the grid-side current since the resonance frequency is greater than the critical frequency. Moreover, it is expected that the system be commonly unstable because increasing the number of inverters decreases the resonance frequency f_{res1} to values lower than the critical frequency. In this case, the system will be unstable when only two inverters are added since the resonance frequency of the LCL filter is initially close to the critical frequency.

Fig. 2.6 shows the root loci analysis when using the grid-side current as feedback. In this case, the values that can be selected for the proportional gain to make the system interactively stable are within:

$$K_p Range = \{0 < K_p < 0.0653\}. \tag{21}$$

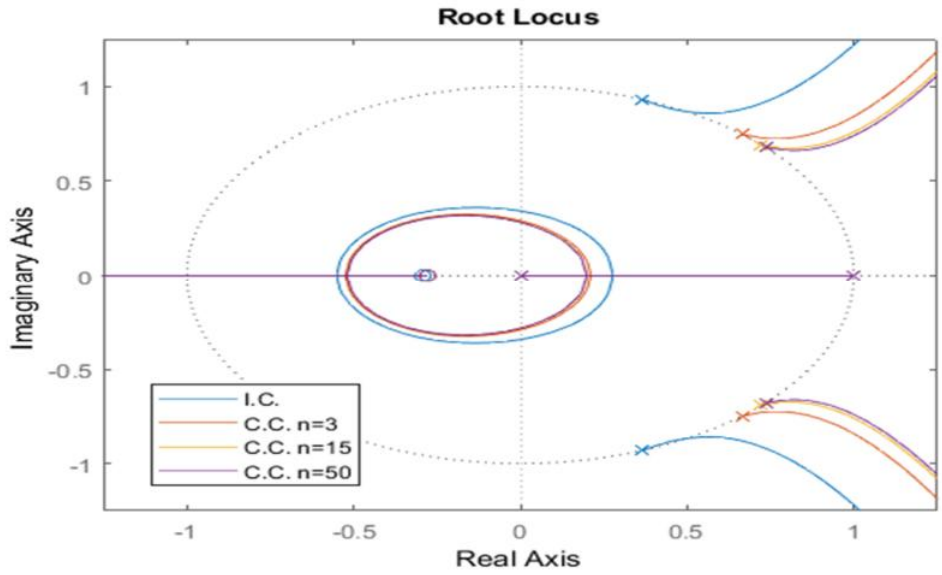


Fig. 2.6: Root loci of the grid-side current for interactive and common currents.

However, the system will be commonly unstable since the poles of the common current are located outside the unit circle regardless of the value of the proportional gain or the number of inverters. Therefore, the entire system is always unstable requiring additional damping. This shows that an inverter employing grid-side-current feedback is in risk of becoming unstable due to the movement of the resonance poles as more inverters are added to grid. Further examination of ω_{res1} shows that the resonance frequency will converge to a defined value. As the number of inverters increases, $nL_g >> L_2$ and $nL_g >> (L_1 + L_2)$. Thus, ω_{res1} will converge to:

$$\omega_{\min res1} = 2\pi f_{\min res1} = \sqrt{\frac{1}{L_1 C_f}}. \tag{22}$$

This means that if the minimum resonance frequency in (22) is greater than the critical frequency (i.e., $f_{min_{res1}} > f_s/6$), the system with grid-side current feedback will no longer be at risk of becoming commonly unstable regardless of the number of inverters in the grid.

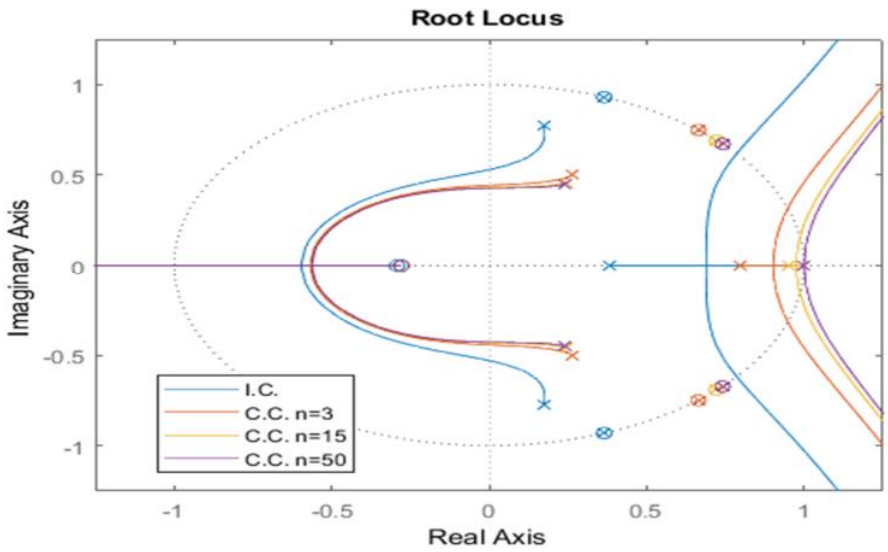


Fig. 2.7: Root loci of the interactive and common currents for grid-side feedback with capacitor-voltage feedforward algorithm.

Active Damping Control

Active damping will be applied to bring the poles of the system inside the unit circle since the system is unstable. Fig. 2.7 shows the root loci of the interactive and common currents for the grid-side-current feedback using the capacitor-voltage feedforward active damping shown in Fig. 2.4.

In this case, the system will continue to have interactive current stability with a higher range of stability from K_p varying from 0 to 0.101. Similarly, the poles for the common current are now inside the unit circle with a range of stability of:

$$K_p Range = \left\{ \begin{array}{l} 0 < K_p < 0.087, n = 3 \\ 0 < K_p < 0.0832, n = 15 \\ 0 < K_p < 0.081, n = 50 \end{array} \right\}. \quad (23)$$

Applying this feedforward technique changes the system stability range. As was the case with stability of the inverter-side current, the system will now be stable only if the resonance

frequency is less than up to one third of the sampling frequency (i.e., $f_r < f_s/3$) and will become unstable if this limit is exceeded [12]. This means that unlike before, the system is no longer in risk of becoming unstable as more inverters are added to the grid since the maximum resonance frequency (1.52 kHz) is less than one third of the sampling frequency (2.67 kHz).

2.3.4 Filter Design Considerations on the System Stability

The previous sections have shown that the stability of the system will highly depend on the LCL filter resonance frequency. A LCL filter is usually designed to attenuate the overall ripple current amplitude, and the resonance frequency is selected to be less than half of the switching frequency f_{sw} and ten times greater than the fundamental frequency f_g (i.e., $10f_g < f_{res} (or\ f_{res1}) < 0.5f_{sw}$) [13]. This relation prevents the filter from amplifying switching noises and low order harmonics.

Fig. 2.8 illustrates the different ranges of stability of the system for the inverter- and grid-side current feedback considering the constrain imposed on the resonance frequency by the design guidelines of the LCL filter. Fig. 2.8(a) and Fig. 2.8(b) show the stability regions when the sampling frequency is equal to the switching frequency (i.e., $f_s = f_{sw}$) for a system with and without the capacitor-feedforward algorithm. In this case, the grid-side current feedback will have a wider range of stability since it can be stable over the critical frequency with a single-loop controller and under twice the critical frequency with the implementation of the capacitor-voltage feedforward active damping.

Similarly, Fig. 2.8 (c) and Fig. 2.8 (d) show the stability regions when the sampling frequency is twice the switching frequency (i.e., $f_s = 2f_{sw}$) for a system with and without the capacitor-feedforward algorithm. In the system with the single-loop controller from Fig. 2.8 (c),

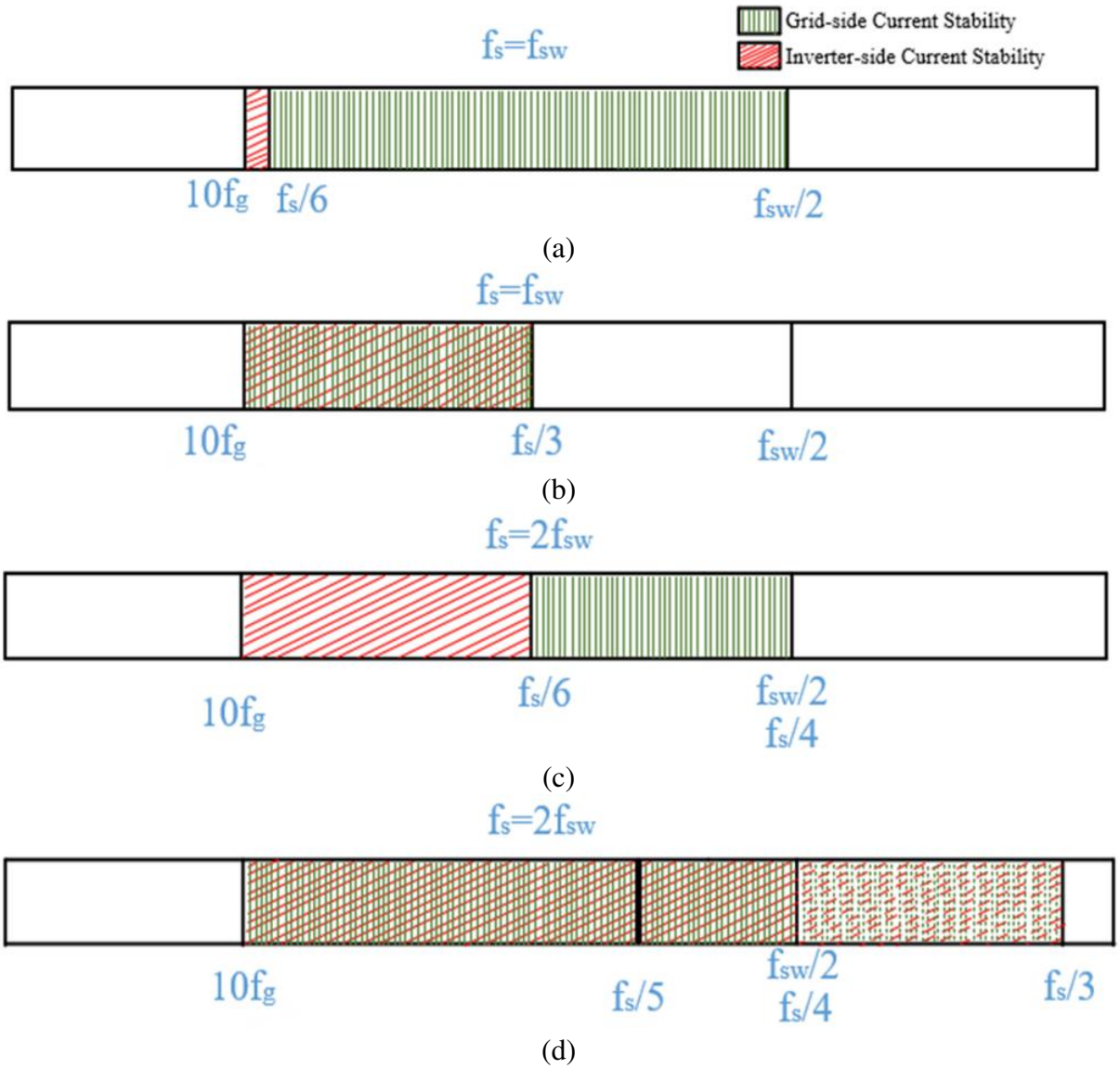


Fig. 2.8: Stability range for inverter- and grid-side current feedback for different cases: (a) fs =fsw without active damping (b) fs =fsw with active damping (c) fs =2fsw without active damping (d) fs =2fsw with active damping.

the regions of stability are evenly distributed between the two feedback currents and the selection of the best feedback method will depend on the value of the filter resonance frequency.

However, the system will always be stable when the capacitor-feedforward algorithm is implemented in Fig 2.8 (d) for both the inverter- and grid-side current feedback provided that the LCL filter had been properly designed.

Despite both feedback currents being stable in this situation, selecting the inverter-side current feedback is overall a better choice than the grid-side current. The main advantage being that no extra sensors are needed since the inverter-side current needs to be measured for switching device protection in high-power applications [1]. In addition, the previous analysis illustrated that the inverter-side current allows for higher values of the proportional gain near the critical frequency for both the interactive and common currents, which translates to a higher bandwidth and faster dynamics for the current controller. By iteratively changing the resonance frequency and examining the root loci, it was found that the inverter-side current feedback have a higher value for the proportional gain when the resonance frequency is lower than about one fifth of the sampling frequency (i.e., $10f_g < f_{res} < f_s/5$). This means that as the sampling frequency increases, this range increases, as well. Conversely, the grid-side current feedback will always have a fixed range of $f_s/5 < f_{res} < f_s/4$. Thus, the inverter-side current will have a wider range where the value of proportional gain can be selected higher than the value of gain for the grid-side current.

2.4 Simulation Results

In order to validate the effects of the active damping algorithm based on feedforward-unity capacitor voltage with both the inverter- and grid-side currents as feedback, MATLAB/SIMULINK™ is used to model a system consisting of three 2-MVA grid-connected parallel inverters feeding the power grid. All three inverters are set to inject 800 kW to the grid. The capacitor voltage feedforward technique is initially used in both cases and is turned off for all inverters at t = 0.3 s.

Fig. 2.9(a) shows that using the inverter-side current as feedback, the system becomes unstable as the capacitor voltage feedforward term is turned off because the interactive current is

unstable. Similarly, Fig. 2.9(b) reveals that using the grid-side current as feedback, the system becomes unstable as the capacitor voltage feedforward term is turned off because the common current is unstable. As mentioned before, the LCL filter resonance frequency utilized in these cases is very close to the critical frequency and therefore, both cases are unstable without active damping.

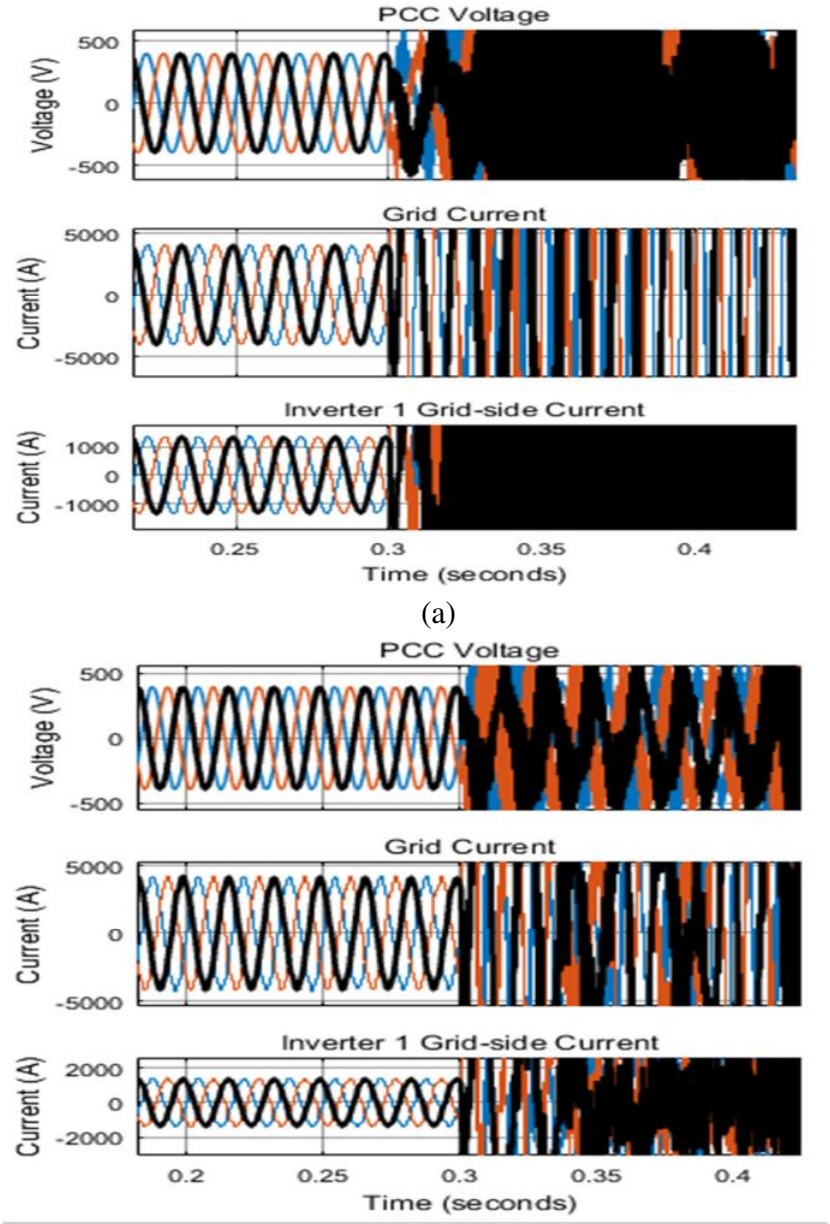


Fig. 2.9: Current waveforms for (a) inverter-side current feedback (b) grid-side current feedback.

2.5 Conclusions

This paper performed a stability analysis considering the proportional gain of the current controller for multiple parallel- and grid-connected inverters using the inverter- and grid-side currents as feedback signals. Modeling of the inverter- and grid-side current feedback using the current separation method was performed. Moreover, the system stability range for both feedback-current approaches with and without active damping based on capacitor-voltage feedforward was examined using the root locus analysis, and those ranges of stability were examined considering the limitations given by the LCL filter design procedure. Overall, the analysis revealed that grid-side current feedback is a better choice when the the sampling frequency is the same as the switching frequency because of its wider range of stability. However, the inverter-side current is better when the sampling frequency is twice the switching frequency due to mainly no needing additional sensors. Finally, the theoretical analysis was validated through simulations.

2.6 Acknowledgments

The authors are grateful to the financial support from the NSF I/UCRC Grid-Connected Advanced Power Electronic Systems (GRAPES) under grant IIP-1439700.

2.7 References

[1] Y. Liu, C. Farnell, V. Jones, K. George, H. A. Mantooth and J. C. Balda, "Resonance propagation of ac filters in a large-scale microgrid," 2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Aachen, 2015, pp. 1-6. doi: 10.1109/PEDG.2015.7223078

[2] S. G. Parker, B. P. McGrath and D. G. Holmes, "Regions of Active Damping Control for LCL Filters," in IEEE Transactions on Industry Applications, vol. 50, no. 1, pp. 424-432, Jan.-Feb. 2014. doi: 10.1109/TIA.2013.2266892

[3] Y. Tang, P. C. Loh, P. Wang, F. H. Choo, F. Gao, "Exploring Inherent Damping Characteristic of LCL-Filters for Three-Phase Grid-Connected Voltage Source Inverters," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1433-1443, Mar. 2012.

[4] Y. Liu, C. Farnell, H. A. Mantooth, J. C. Balda, R. A. McCann and C. Deng, "Resonance propagation modeling and analysis of AC filters in a large-scale microgrid," 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 143-149. doi: 10.1109/APEC.2016.7467865

[5] J. Dannehl, C. Wessels and F. W. Fuchs, "Limitations of Voltage-Oriented PI Current Control of Grid-Connected PWM Rectifiers With LCL Filters," in IEEE Transactions on Industrial Electronics, vol. 56, no. 2, pp. 380-388, Feb. 2009. doi: 10.1109/TIE.2008.2008774

[6] M. Lu, X. Wang, P. C. Loh and F. Blaabjerg, "Resonance Interaction of Multiparallel Grid-Connected Inverters With LCL Filter," in IEEE Transactions on Power Electronics, vol. 32, no. 2, pp. 894-899, Feb. 2017. doi: 10.1109/TPEL.2016.2585547

[7] M. Lu, X. Wang, P. C. Loh and F. Blaabjerg, "Interaction and aggregated modeling of multiple paralleled inverters with LCL filter," 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 1954-1959. doi: 10.1109/ECCE.2015.7309936

[8] J. L. Agorreta, M. Borrega, J. López and L. Marroyo, "Modeling and Control of N -Paralleled Grid-Connected Inverters With LCL Filter Coupled Due to Grid Impedance in PV Plants," in IEEE Transactions on Power Electronics, vol. 26, no. 3, pp. 770-785, March 2011. doi: 10.1109/TPEL.2010.2095429

[9] Y. Liu, C. Farnell, J. C. Balda and H. A. Mantooth, "A 13.8-kV 4.75-MVA microgrid laboratory test bed," 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, 2015, pp. 697-702. doi: 10.1109/APEC.2015.7104426

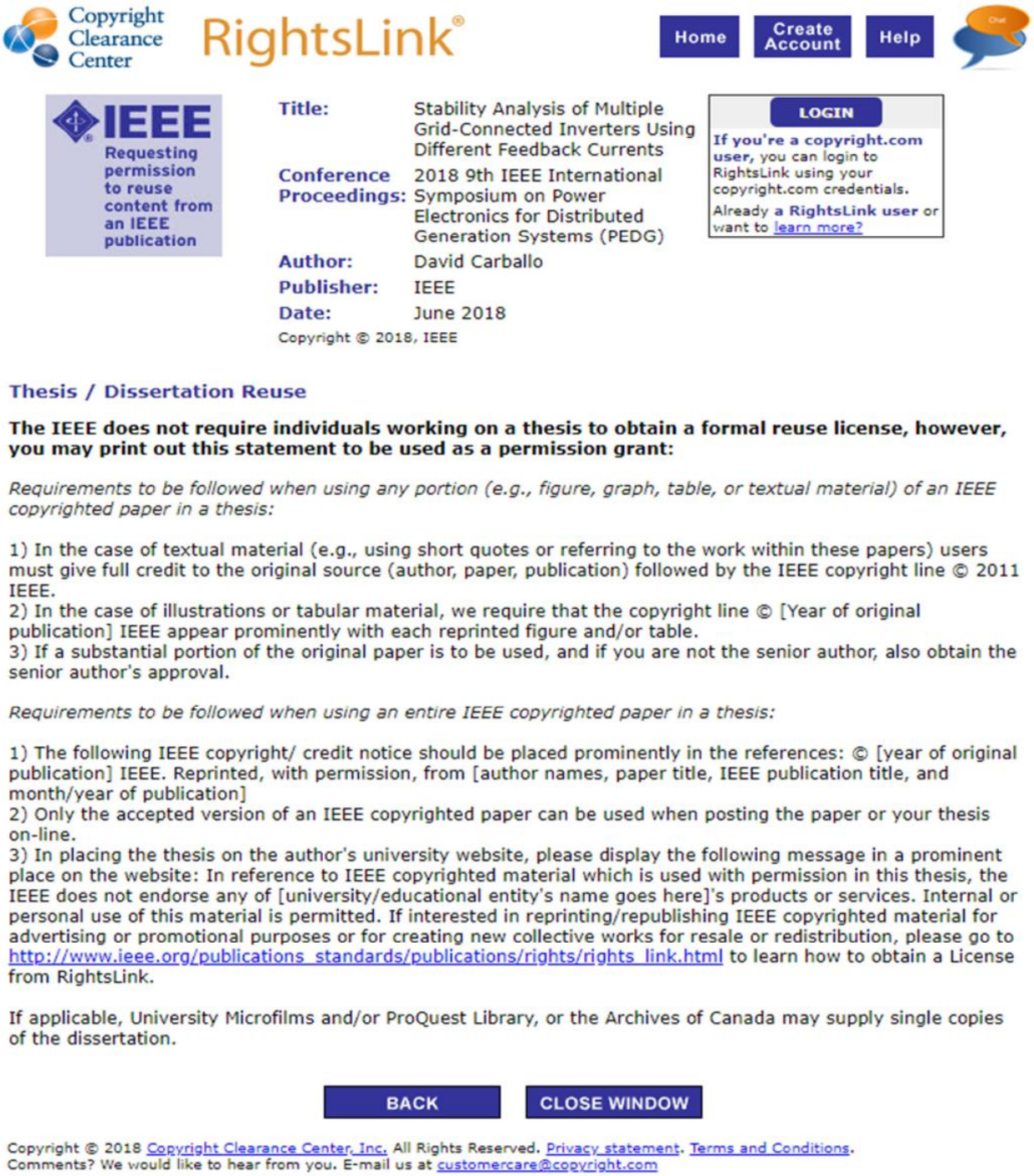
[10] M. Lu, Z. Xin, X. Wang, R. N. Beres and F. Blaabjerg, "Extended stable boundary of LCL-filtered grid-connected inverter based on an improved grid-voltage feedforward control," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-7. doi: 10.1109/ECCE.2016.7855103

[11] X. Li, J. Fang, Y. Tang, X. Wu and Y. Geng, "Capacitor-Voltage Feedforward With Full Delay Compensation to Improve Weak Grids Adaptability of LCL-Filtered Grid-Connected Converters for Distributed Generation Systems," in IEEE Transactions on Power Electronics, vol. 33, no. 1, pp. 749-764, Jan. 2018. doi: 10.1109/TPEL.2017.2665483

[12] M. Lu and F. Blaabjerg, "Stability identification for grid-connected inverters with LCL filters considering grid-voltage feedforward regulator," 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL), Stanford, CA, 2017, pp. 1-5. doi: 10.1109/COMPEL.2017.8013342

[13] A. Reznik, M. G. Simões, A. Al-Durra and S. M. Muyeen, "LCL Filter Design and Performance Analysis for Grid-Interconnected Systems," in IEEE Transactions on Industry Applications, vol. 50, no. 2, pp. 1225-1232, March-April 2014. doi: 10.1109/TIA.2013.2274612

2.8 Permissions



Copyright Clearance Center RightsLink®

Home | Create Account | Help

IEEE Requesting permission to reuse content from an IEEE publication

Title: Stability Analysis of Multiple Grid-Connected Inverters Using Different Feedback Currents

Conference Proceedings: 2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)

Author: David Carballo

Publisher: IEEE

Date: June 2018

Copyright © 2018, IEEE

LOGIN

If you're a copyright.com user, you can login to RightsLink using your copyright.com credentials.

Already a RightsLink user or want to learn more?

Thesis / Dissertation Reuse

The IEEE does not require individuals working on a thesis to obtain a formal reuse license, however, you may print out this statement to be used as a permission grant:

Requirements to be followed when using any portion (e.g., figure, graph, table, or textual material) of an IEEE copyrighted paper in a thesis:

1) In the case of textual material (e.g., using short quotes or referring to the work within these papers) users must give full credit to the original source (author, paper, publication) followed by the IEEE copyright line © 2011 IEEE.
2) In the case of illustrations or tabular material, we require that the copyright line © [Year of original publication] IEEE appear prominently with each reprinted figure and/or table.
3) If a substantial portion of the original paper is to be used, and if you are not the senior author, also obtain the senior author's approval.

Requirements to be followed when using an entire IEEE copyrighted paper in a thesis:

1) The following IEEE copyright/ credit notice should be placed prominently in the references: © [year of original publication] IEEE. Reprinted, with permission, from [author names, paper title, IEEE publication title, and month/year of publication]
2) Only the accepted version of an IEEE copyrighted paper can be used when posting the paper or your thesis on-line.
3) In placing the thesis on the author's university website, please display the following message in a prominent place on the website: In reference to IEEE copyrighted material which is used with permission in this thesis, the IEEE does not endorse any of [university/educational entity's name goes here]'s products or services. Internal or personal use of this material is permitted. If interested in reprinting/republishing IEEE copyrighted material for advertising or promotional purposes or for creating new collective works for resale or redistribution, please go to http://www.ieee.org/publications_standards/publications/rights/rights_link.html to learn how to obtain a License from RightsLink.

If applicable, University Microfilms and/or ProQuest Library, or the Archives of Canada may supply single copies of the dissertation.

BACK | CLOSE WINDOW

Copyright © 2018 Copyright Clearance Center, Inc. All Rights Reserved. Privacy statement. Terms and Conditions.
Comments? We would like to hear from you. E-mail us at customercare@copyright.com

Certification of First Author

I hereby certify that David Carballo Rojas is the first author of the article this chapter is based on and has completed at least 51% of the work described in the article.

Juan Carlos Balda

Signature _____

Date _____

CHAPTER 3

MODELING AND STABILITY ANALYSIS OF GRID-CONNECTED INVERTERS WITH DIFFERENT LCL FILTER PARAMETERS

D. Carballo, E. Escala and J. C. Balda, "Modeling and Stability Analysis of Grid-connected Inverters with Different LCL Filter Parameters," *2018 IEEE Electronic Power Grid (eGrid)*, Charleston, SC, 2018.

Abstract

Microgrid are gaining popularity due to several advantages like potential for fuel savings and resiliency in case of grid catastrophic failures. In a microgrid, many energy sources like wind and solar farms are connected to the grid through inverters with different power ratings and LCL filter parameters. The inverters incorporated in these systems might have a different frequency response and stability ranges than those inverters with identical LCL filter values. This paper establishes the model and analyzes the stability of a system with multiple paralleled- and grid-connected inverters with different LCL filter parameters using the grid-side currents as feedback signals. The analysis results showed that a method similar to the interactive and common current analysis technique used on inverters with identical LCL filters can be implemented on a system with different LCL filers to calculate the maximum values of the inverters' current controller gains without having to derive the complicated equations of the MIMO system.

3.1 Introduction

The growing demand for renewable energy sources, such as solar energy, wind energy, and even energy storage has led to higher penetration of distributed energy resources (DERs) into power systems during the past years. As a result, the design of controllers for grid-connected inverters interfacing DERs and the electric grid has become a crucial task. In renewable power plants, hundreds of inverters operate in parallel to expand the total generation capacity [1]. These paralleled inverters are usually connected to the grid through LCL filters which tend to aggravate the system resonance and instability issues due to coupling produced by the grid impedance and converter's current controller dynamic interactions [2].

These instabilities problems due to the coupling of the inverters LCL filters have been studied thoroughly in the literature. Usually in these studies, the inverters are assumed to have identical LCL filter parameters in order to reduce the complexity of the analysis [3-5]. However, a wide variety of energy sources are incorporated in a microgrid; thus, LCL filters with different parameters and power ratings are connected to the point of common coupling (PCC). Consequently, these inverters have different system responses than those inverters with identical LCL filter values. The authors of [6] presented an analysis on the relationship between the resonant frequency and the different numbers of parallel inverters, the LCL filter parameters as well as the inverter's composition ratios. However, an analysis of the system regarding the stability ranges for the current controllers' proportional gain was not performed. The work presented in this paper aims to model and analyze multiple grid-connected inverters with different LCL filter parameters with the ultimate goal of simplifying the stability analysis to determine the proportional gain stability ranges of the inverters.

This paper is organized as follows: Section 3.2 addresses an overview of the mathematical modeling of the grid-side currents, Section 3.3 evaluates the system stability, Section 3.4 illustrates a method to reduce the complexity of the system's stability analysis, Section 3.5 analyzes simulation results, and Section 3.6 provides the main conclusions.

3.2 Modeling of the Parallel Inverters

3.2.1 Grid-Side Current- Mathematical Modeling

Two grid-connected inverters with different LCL filters are initially considered to decrease the complexity of the analyzed system. The parallel operation of these inverters is illustrated in Fig. 3.1, where Z_{11}, Z_{21} and Z_{31} are the s-domain impedances of the LCL filter for the first inverter, Z_{12}, Z_{22} and Z_{32} are the LCL filter impedances of the second inverter, and Z_g is the grid impedance. In this paper, the equivalent series resistance (ESR) of the components is neglected in order to consider the worst-case stability scenario where the LCL filter resonance is completely undamped. The dynamics of the system from Fig. 3.1 can be described using multivariable control theory as:

$$\mathbf{i_{on}} = \mathbf{G(s)} \cdot \mathbf{v_{on}} \Leftrightarrow \begin{bmatrix} i_{o1} \\ i_{o2} \end{bmatrix},$$

$$= \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} . \begin{bmatrix} v_{o1} \\ v_{o2} \end{bmatrix}, \tag{1}$$

where $\mathbf{i_{on}}$ is the output vector of the grid-side current, $\boldsymbol{v}_{\mathbf{on}}$ the input vector of the inverters voltages and **G(s)** the transfer function matrix that provides the relationship between the grid-side current with respect to the inverter voltages. The diagonal terms of **G(s)** are the influence of an inverter

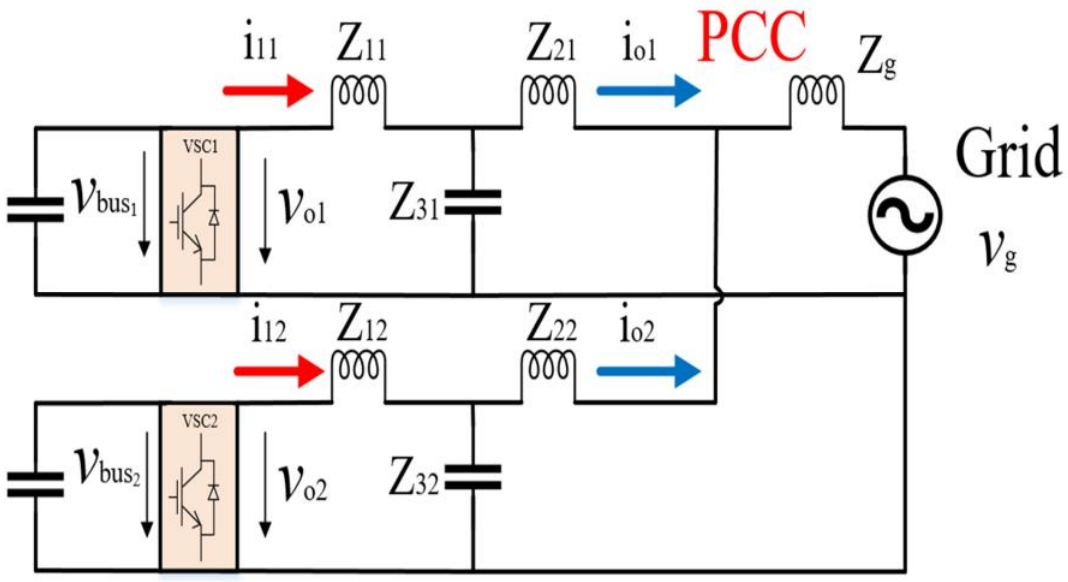
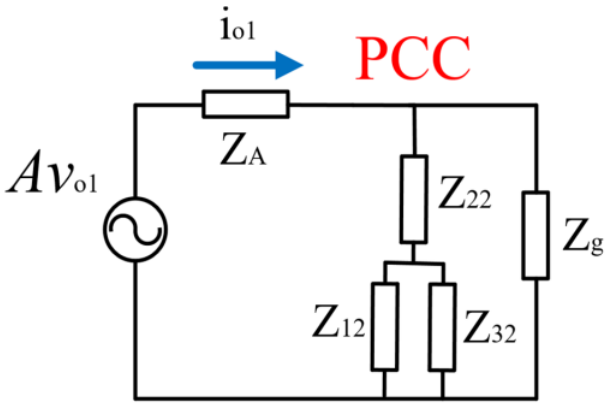


Fig. 3.1:Schematic of multiple grid-connected inverters with different LCL filter parameters.

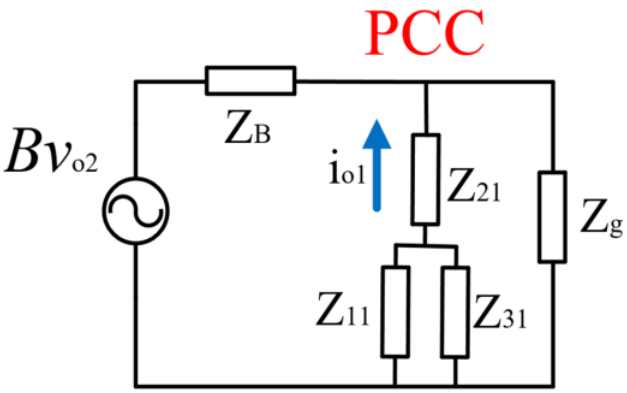
current (e.g., i_{o1}) due to its own inverter voltage (e.g., v_{o1}), and the non-diagonal terms are the influence of an inverter current (e.g., i_{o1}) due to another inverter voltage (e.g., v_{o2}).

Similar to the case with identical LCL filters, the grid inductance causes coupling between the two inverters and, thus, the non-diagonal terms in the **G(s)** matrix are non-zero. Moreover, unlike identical LCL filters, each term in the **G(s)** matrix differ from one another, which increases the complexity when analyzing the system.

Using the principle of superposition to remove the influence of the grid and the other inverter voltages, each element in the **G(s)** matrix can be obtained. For instance, the diagonal element G_{11} is derived by removing all voltage sources except v_{o1} while the non-diagonal element G_{12} is obtained by removing all voltage sources except v_{o2}. Using source transformation, the auxiliary circuits of Figs. 3.2(a) and 3.2(b) are derived from Fig. 3.1 where the equivalent impedances and coefficient for the voltage sources can be written as:



(a)



(b)

Fig. 3.2: Auxiliary circuit of two parallel inverters with different LCL filters parameters provided that (a) all voltage sources except vo1 are zero, (b) all voltage sources except vo2 are zero.

$$A=\frac{Z_{31}}{Z_{11}+Z_{31}}, \qquad B=\frac{Z_{32}}{Z_{12}+Z_{32}}, \tag{2}$$

$$Z_A=\frac{Z_{11}Z_{21}+Z_{11}Z_{31}+Z_{21}Z_{31}}{Z_{11}+Z_{31}}, \qquad Z_B=\frac{Z_{12}Z_{22}+Z_{12}Z_{32}+Z_{22}Z_{32}}{Z_{12}+Z_{32}} \tag{3}$$

From the auxiliary circuit in Fig. 3.2(a), G_{11} is obtained as:

$$G_{11}=\frac{i_{o1}}{v_{o1}}=\frac{Z_{31}}{(Z_{11}+Z_{31})(Z_A+\frac{Z_gZ_B}{(Z_g+Z_B)})}. \tag{4}$$

Likewise, G_{12} is derived from Fig. 3.2(b) as:

$$G_{12} = \frac{i_{o1}}{v_{o2}} = -\frac{Z_{32}Z_g}{(Z_{12}+Z_{32})(Z_A + \frac{Z_g Z_B}{(Z_g+Z_B)})(Z_g+Z_B)}. \quad (5)$$

The remaining elements of the **G(s)** matrix are derived in a similar manner and their expressions are given in the Appendix.

3.2.2 Selection of the LCL Filter Parameters

The authors of [7] presented a systematic design methodology for selecting the parameters of an LCL filter for grid-connected applications. The inverter-side inductance, for example, is given by:

$$L_1 = \frac{V_{DC}V_{ph}}{0.2 f_{sw} P_n \sqrt{2}}. \quad (6)$$

where V_{DC} is the DC link voltage of the inverter, V_{ph} the phase voltage, f_{sw} the switching frequency, and P_n the nominal power.

Expression (6) shows that the value of the inductor is inversely proportional to the nominal power of the inverter. Thus, any change to the nominal power of the inverter if the other inverter parameters remain the same will be inversely reflected to the value of the inverter-side inductance. The equation for the grid-side inductor shows the same inversely proportional relation to the nominal power [7]. However, the filter capacitor is determined as a 5 percent of its base impedance given by:

$$C_f = 0.05\frac{P_n}{\omega_g E_n^2} \quad (7)$$

where ω_g is the grid frequency, and E_n the base voltage. Thus, unlike the inductors, the filter capacitor is proportional to the nominal power of the inverter [7].

In this paper, the LCL filter of the first two inverters are designed considering that one inverter has a 30 percent higher rated power than the other while keeping all other parameters the same. It is important to mention that while the LCL filter parameters were selected using this method, the analytical framework developed in Section III is still valid for any values of the LCL filter parameters.

3.2.3 Multiple Resonance Peaks

Similar to the case with identical LCL filters, the addition of parallel inverters changes the frequency response of the system [8-9]. Fig. 3.3 illustrates the positions of the resonance peaks with two grid-connected inverters with LCL filters values given by Table 3.1.

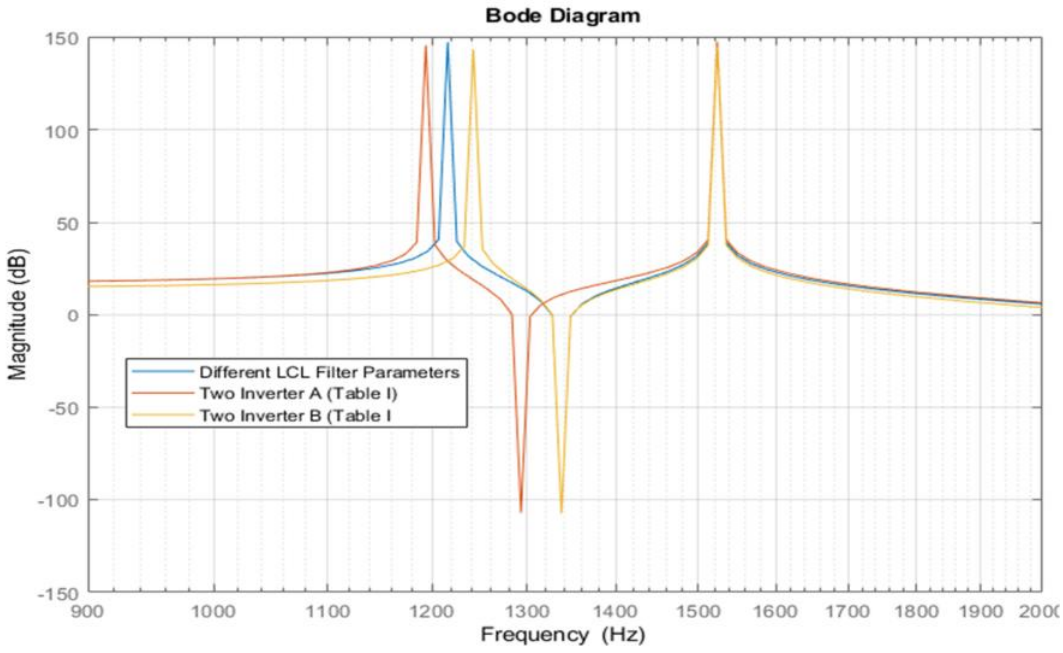


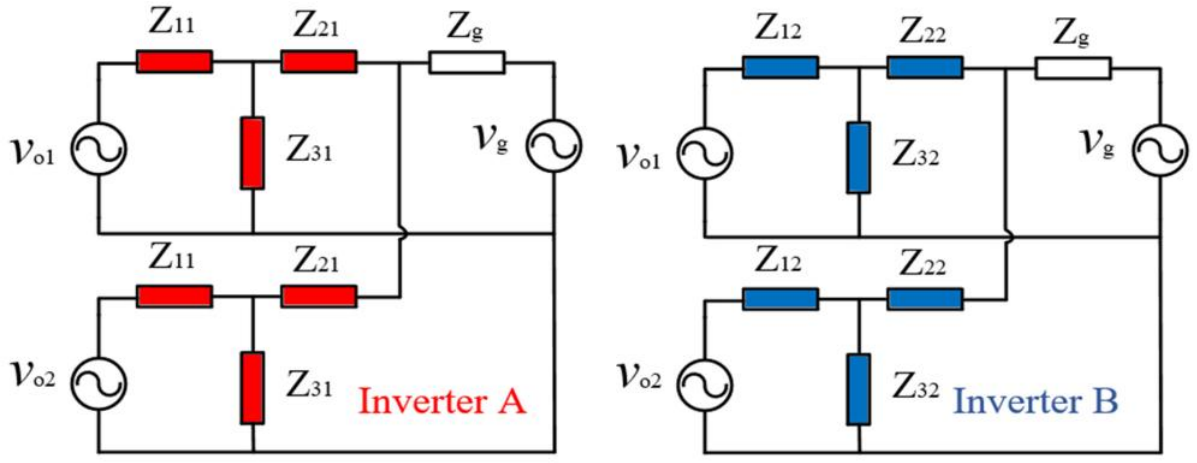
Fig. 3.3: Resonance peaks of the paralleled grid-connected inverters.

Table 3.1: System Parameters

Inverter Parameters		
	Inverter A	Inverter B
Power rating	P_{n1}=2 MVA	P_{n2}=1.4 MVA
Voltage rating	480 V	480 V
Inverter-side inductance	L_{11}=20 µH	L_{12}=28 µH
Grid-side indutance	L_{21}=12.2 µH	L_{22}=17.1 µH
Filter capacitor	C_{f11}=Δ3x480 µF	C_{f12}=Δ3x343 µF
Proportional gain	0.125	0.155
Sampling frequency	4 kHz	4 kHz
Switching frequency	4 kHz	4 kHz
Grid Inductance	L_g=10 µH	

To compare with the case of identical inverters, Fig. 3.3 also shows the resonance peaks of two more cases: one with two identical inverters with the parameters of inverter A (Fig. 3.4(a)), and another one with the parameters of inverter B (Fig. 3.4(b)). For the three cases, the position of the LCL filter main resonance remains the same at

$$\omega_{res} = \sqrt{(L_{11} + L_{21}) / (L_{11} L_{21} C_{f1})} \,. \tag{8}$$



(a) (b)

Fig. 3.4: Schematic of two paralleled grid-connected inverters with the LCL parameters of (a) inverter A, (b) inverter B.

For the case of two different LCL filters, however, the frequency of the second resonance is given by:

$$\omega_{res2} = \sqrt{\frac{(L_{11} + (L_{21} + (1+n')L_g)}{(L_{11}(L_{21} + (1+n')L_g)C_{f1})}}, \tag{9}$$

$$= \sqrt{\frac{(L_{12} + (L_{22} + (1+(1/n'))L_g)}{(L_{12}(L_{22} + (1+(1/n'))L_g)C_{f2})}}, \tag{10}$$

where n' is a gain given by the ratio of the power ratings of the inverters; that is,

$$n' = P_{n2} / P_{n1}. \tag{11}$$

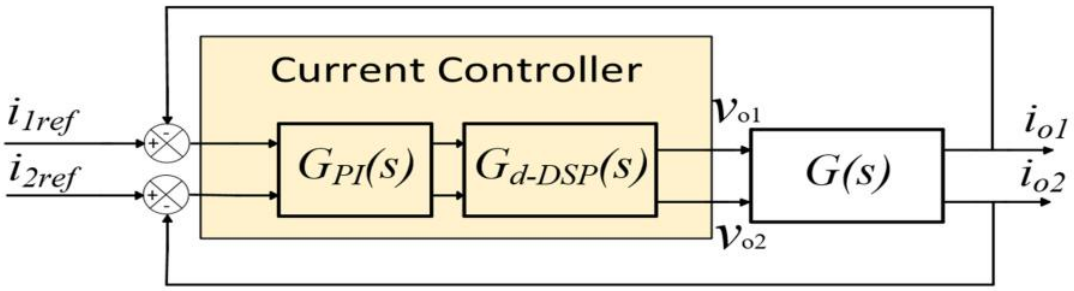
3.3 Stability Analysis of the Parallel Inverters

3.3.1 Control Strategy

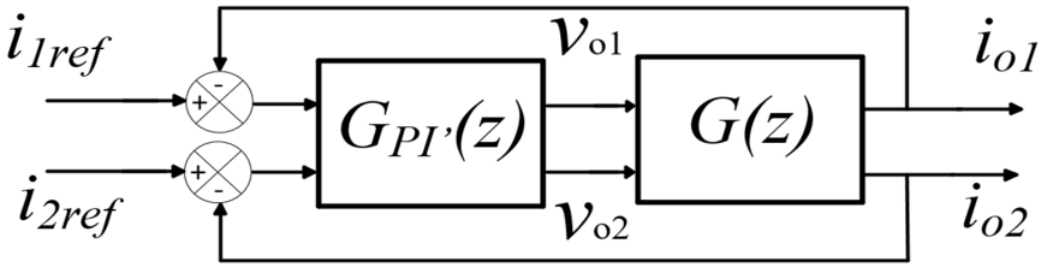
The block diagram of the multiple input, multiple output (MIMO) current-control loop in the s-domain for the two paralleled grid-connected inverter from Fig. 3.1 is presented in Fig. 3.5(a). In the figure, $\mathbf{i_{nref}}$ is the reference commands for the grid-side current given to the controllers, $\mathbf{G_{d\_DSP}(s)}$ the diagonal transfer function which accounts for the delays of the system and $\mathbf{G_{PI}(s)}$ is a diagonal matrix that contains the controller of each inverter which is chosen in this paper as follows:

$$\mathbf{G_{PI}(s)} = \begin{bmatrix} PI_1 & 0 \\ 0 & PI_2 \end{bmatrix}, \qquad PI_{1,2}(s) = K_P + \frac{K_i}{s}. \tag{12}$$

Although the system can be analyzed in the s-domain as in [10], the z-domain modeling of the system will be considered in this paper since the inverters are usually digitally controlled with a microcontroller. Thus, the discrete representation of the controller from Fig. 3.5(a) is presented



(a)



(b)

Fig. 3.5: Multiple current-control loop for the grid-side currents in (a) s-domain, (b) z-domain.

in Fig. 3.5(b), where the PI controller and the transfer function matrix were discretized by using a Tustin and zero-order-hold (ZOH) transform, respectively [11]. Moreover, $\mathbf{G_{PI}'(z)}$ now contains both the PI controllers of the inverters as well as the system delays.

3.3.2 Stability Analysis for Grid-Side Current

The stability of the system can be analyzed by examining the poles of the multivariable system [8]. From Fig. 3.5(b), the closed-loop transfer function of the multivariable system can be derived as follows:

$$\begin{bmatrix} i_{o1} \\ i_{o2} \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \cdot \begin{bmatrix} i_{1ref} \\ i_{2ref} \end{bmatrix}, \tag{13}$$

$$\mathbf{T(z)} = [\mathbf{I} + \mathbf{G(z)PI'(z)}]^{-1} \cdot [\mathbf{G(z)PI'(z)}]. \tag{14}$$

where **I** represents the identity matrix. From (14), the diagonal element $T_{11,}$ and the non-diagonal element T_{12} are derived as follows:

$$T_{11} = \frac{i_{o1}}{i_{1ref}} = \frac{G_{11}PI_1^{'} + (PI_1^{'}PI_2^{'})(G_{11}G_{22} - G_{12}G_{21})}{(1+G_{11}PI_1^{'})(1+G_{22}PI_2^{'}) - (G_{12}PI_2^{'})(G_{21}PI_1^{'})} \tag{15}$$

$$T_{12} = \frac{i_{o1}}{i_{2ref}} = \frac{G_{12}PI_2^{'}}{(1+G_{11}PI_1^{'})(1+G_{22}PI_2^{'}) - (G_{12}PI_2^{'})(G_{21}PI_1^{'})} \tag{16}$$

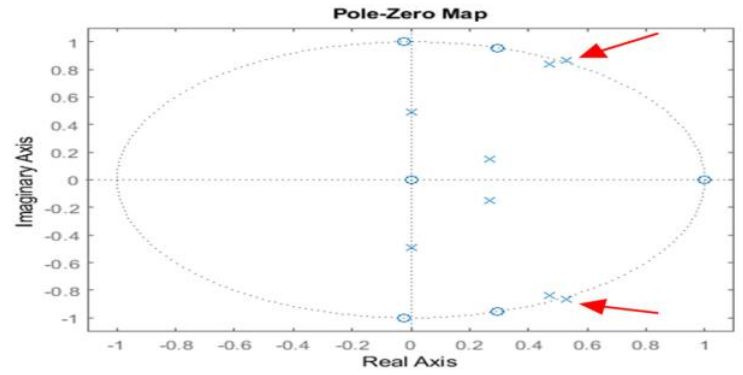
The other elements of the **T(z)** matrix are given in the Appendix. Expressions (15)-(16) show that the denominators of the system are identical since the poles of a multivariable system have to the same [10]. Thus, the characteristic equation of the system is:

$$(1+G_{11}PI_1^{'})(1+G_{22}PI_2^{'}) - (G_{12}PI_2^{'})(G_{21}PI_1^{'}) = 0. \tag{17}$$

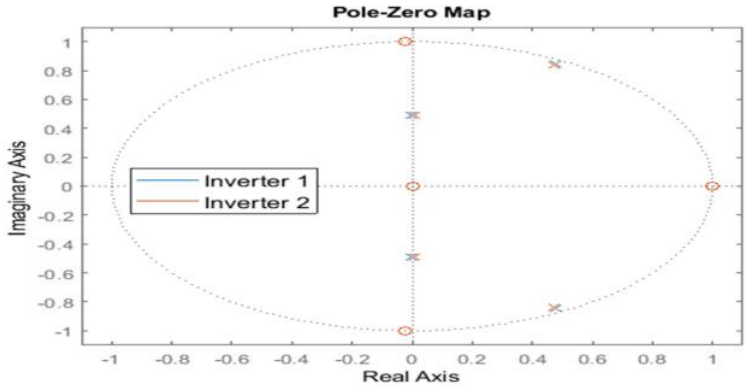
From (17), it is clear that the system stability depends on both controllers as well as the four elements of the transfer function matrix **G(z)**. Then, if and only if all the poles from (14) are inside of the unit circle, the system will be stable.

Therefore, proper selection of the proportional gains of the current controllers will determine the stability of the system.

The poles of the system are plotted in Fig. 3.6(a) using the parameters from Table 3.1 and (17). However, the system will be unstable since some of the poles are outside of the unit circle. The significance of this result is that the proportional gains were selected without considering the coupling of the inverters, such that the inverters were stable when they were individually connected to the grid, as seen in Fig. 3.6(b). Thus, despite the inverters being stable individually with these gains, they become unstable once they are connected to the grid due to mutual



(a)



(b)

Fig. 3.6: Poles of the (a) paralleled inverter system with Kp from Table 3.1, (b) individual inverter system.

coupling. This means that conventional current controller design for individual inverters might not be sufficient to guarantee the stability of multiple grid-connected inverters with different LCL filters.

3.4 Comparison with the Stability Analysis of Identical LCL Filters

3.4.1 Motivation for Comparison

While the previous analysis allows one to accurately determine the stability of the system, the downside is that the analysis becomes more complicated once more inverters are added to microgrid. This section will show that the regions of stability of the inverters with

different LCL filter parameters have some similarities and differences with the case when all paralleled inverters have the same LCL filter values. Understanding these similarities will allow the simplification of the stability analysis of a system with different LCL filters.

For multiple grid-connected inverters with the same LCL filter, [8] showed that the grid-side current is comprised of a current that circulates between two inverters (i.e., interactive current) and one that is injected into the grid ((i.e., common current). Then, the stability of the system can be determined by performing single-input, single-output (SISO) analysis techniques (e.g., root locus) to the open-loop forward path of the closed-loop transfer function of the interactive and common currents [8]. Then, the overall system will only be stable if it has interactive- and common-current stability [8-9].

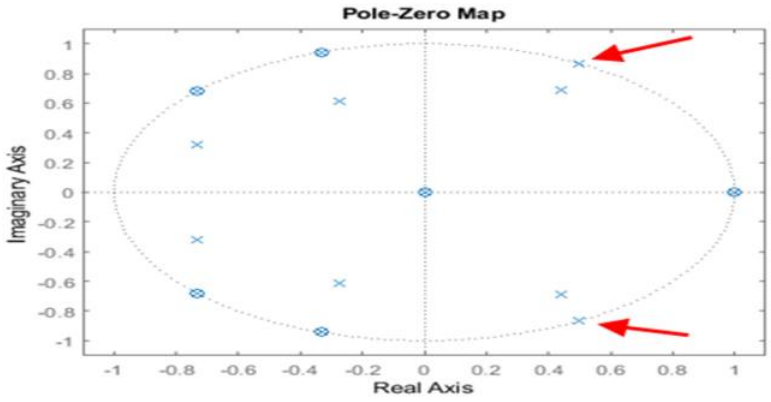
The analysis method described in [8] will be applied to the circuit in Fig. 3.1 to calculate the stability range of Kp for the common and interactive currents. To do so, the circuit in Fig. 3.1 will be reconfigured as the two circuits from Fig. 3.4. Fig. 3.4(a) shows the equivalent model of the system that only has two inverters A connected to the grid while Fig. 3.4(b) has two inverters B connected. Then, the stability analysis in [8] will be implemented to the independent circuits to obtain their values of Kp for the interactive- and common-current stability. The stability ranges of the two inverters are calculated and presented in Table 3.2. Now the values of Kp in Table 3.2 can be tested in the characteristic equation of (17) to determine similarities and differences between the analysis of identical and different LCL filters.

Table 3.2: Stability Range

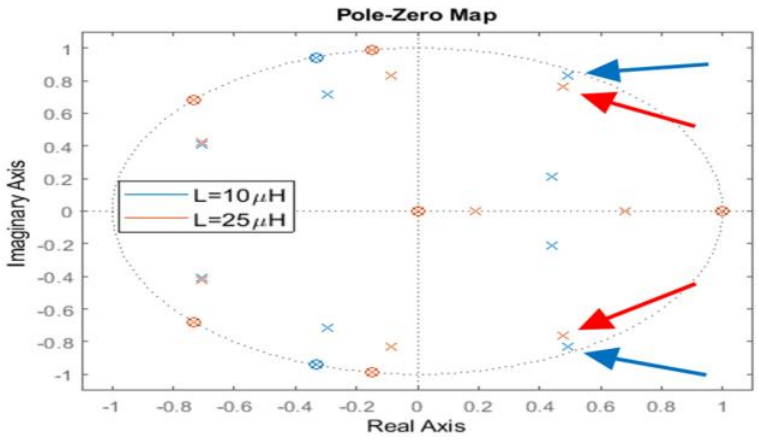
Stability Range for Proportional Gain K_P		
Inverters	Inverter A	Inverter B
Interactive Stability	$0< K_P<0.116$	$0<K_P <0.162$
Common Stability	$0<K_P <0.158$	$0< K_P<0.205$

3.4.2 Interactive-Current Stability

The maximum values of Kp for the interactive-current stability of both inverters play an important role in the system stability with different LCL filter parameters. In this case, selecting the maximum values of Kp for the interactive-current stability of both inverters result in the poles of the system being exactly on the edge of the unit circle as shown in Fig. 3.7(a). Moreover, the positions of these poles with these values of Kp do not change significantly with changes in the grid inductance which is similar to the behavior of the interactive-current stability in [8].



(a)



(b)

Fig. 3.7: Poles of the system for (a) maximum value of Kp for the interative stability, (b) inversely changing the value of Kp for the two inverters.

However, this behavior occurs mainly when the proportional gain of both inverters are selected close to maximum Kp for the interactive-current stability. If one of the inverters is selected with a proportional gain lower than its maximum interactive-current stability gain, the other inverter can increase its proportional gain Kp higher than its maximum value for the interactive-current stability. This is presented in Fig. 3.7(b) where although the value of Kp for the first inverter was selected higher than its interactive-current stability range at 0.125, the poles of the system remain inside of the unit circle due to reducing the gain of the second inverter to 0.07. However, changes to the grid inductance with these values of Kp, will change the position of the poles of the system, as seen in Fig 3.7(b).

3.4.3 Common-Current Stability

Similarly, the maximum value of Kp for the common currents of the inverters will also play an important role in the stability of the system with different LCL filters. To calculate the range of stability of the common currents, the N-equivalent model of the inverters will be used as in [8,10]. In this model, an inverter "perceives" the grid inductance N times bigger, as illustrated in Fig. 3.8 [10]. It is important to mention that this model is only valid for the analysis when inverter A and inverter B have a 1:1 ratio. Using this model, the common-current stability for the system in Fig. 3.4(a) and Fig. 3.4(b) is calculated and presented in Table 3.2. However, since the values of Kp for the common-current stability are larger than the values of the interactive-current stability, the common stability cannot be tested using the parameters from Table 3.1. That is, if the inverters are commonly unstable, they will also be interactively unstable.

Thus, the filter values of inverters A and B are replaced by the values of inverters C and D from Table 3.3 to verify the effect of the common-current stability for inverters with different LCL filters. Using these filter parameters allows the system to have a stability case where the

Table 3.3: System Parameters to Test Common Stability

Inverter Parameters		
	Inverter C	Inverter D
Power rating	P_{n1}=0.75 MVA	P_{n2}=0.54 MVA
Inverter-side inductance	L_{11}=110 µH	L_{12}=154 µH
Grid-side indutance	L_{21}=12.2 µH	L_{22}=17.1 µH
Filter capacitor	C_{f11}=Δ3x600 µF	C_{f12}=Δ3x428 µF
Interactive Stability	$0<K_P<0.352$	$0<K_P<0.492$
Common Stability	$0<K_P<0.132$	$0<K_P<0.274$
Grid Inductance	L_g=10 µH	

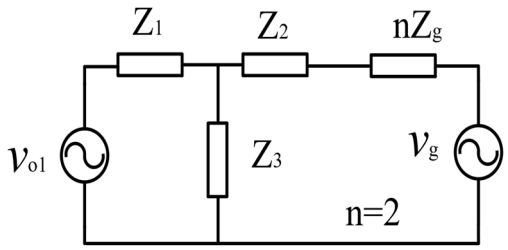


Fig. 3.8: Equivalent N-inverter model to measure the common-current stability gains.

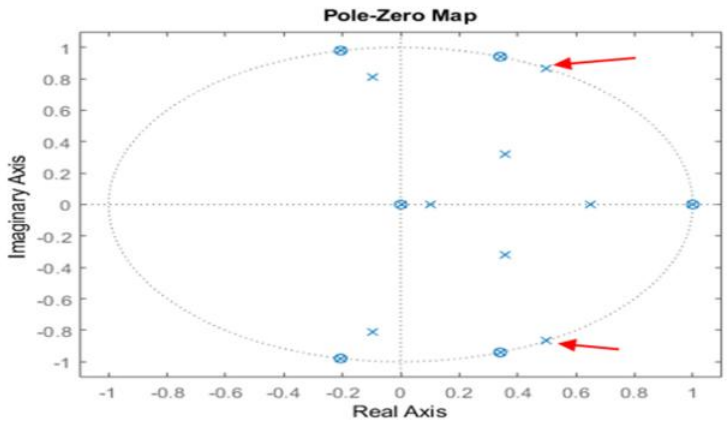


Fig. 3.9: Poles of the system for maximum values of Kp for the common-current stability in Table 3.3.

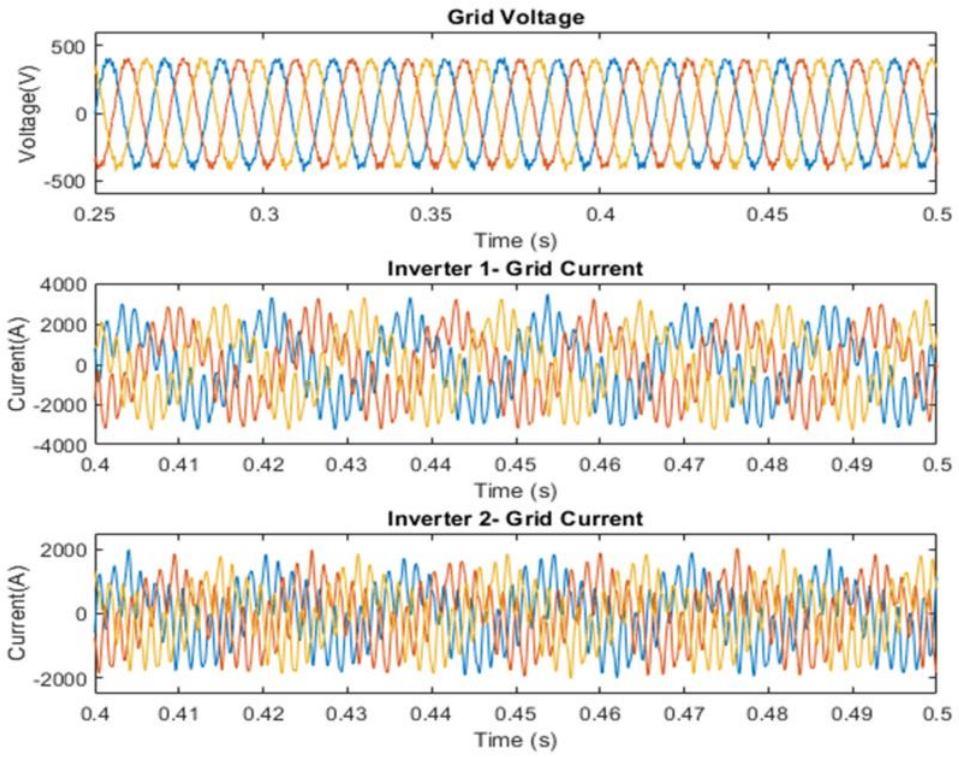
inverters can be commonly unstable but interactively stable. Then, following the same methods as before, the ranges of Kp for the interactive- and common-current stability are calculated and presented in Table 3.3. In this case, selecting the maximum values of Kp for the common-current stability using the N-equivalent model results in the poles of the system being exactly on the edge of the unit circle, as shown in Fig. 3.9.

The results from this section show that the interactive and common stability analysis techniques implemented in [8] can be used to determine the stability ranges of the proportional gain of inverters with different LCL filters that have some variations in their power ratings. The main modification that needs to be made is that the system with different inverters needs to be converted into multiple systems with identical LCL filters as presented in Fig. 3.4.

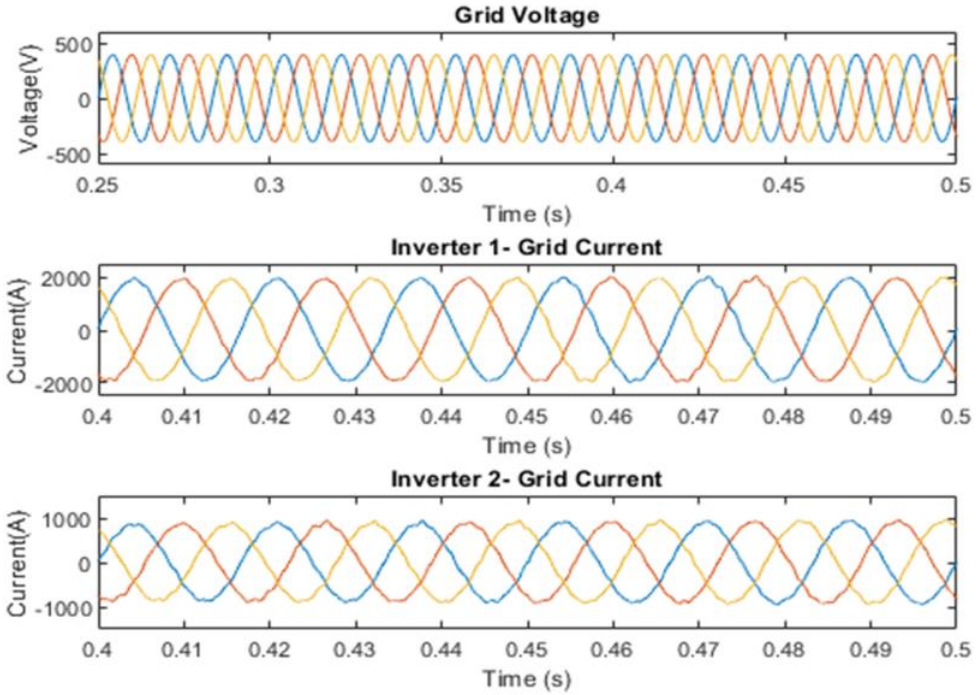
Then, the method in [8] can be applied to each of those equivalent circuits to obtain the maximum value of the proportional gains for the interactive- and common-current stability. Finally, the value of Kp of each inverter needs to be lower than the maximum interactive- and common-current stability gains.

3.5 Simulation Results

In order to validate the theoretical analysis from the previous section, MATLAB/SIMULINK™ is used to model a system consisting of two grid-connected inverters with the parameters from Table 3.1. Inverter A and inverter B are given a reference current of 2 kA and 1 kA, respectively, that needs to be tracked with the current controllers. Fig. 3.10(a) shows that the current controller of the inverters does not track the reference currents and produces harmonics and distortion on the grid current and voltage. This occurs since the poles of the system were outside of the unit circle as shown in Fig. 3.6(a), making the system unstable. Similarly, Fig. 3.10(b) shows that when only one of the inverters is connected to the grid at a time, the current controller can properly track its reference current without great distortion. This is the result of the poles of the system being inside of the unit circle in Fig. 3.6(b), making the system stable.



(a)



(b)

Fig. 3.10: Simulation results of (a) multiple paralleled- (b) individual grid-connected inverters with the values from Table 3.1.

3.6 Conclusions

The modeling and stability analysis for two paralleled grid-connected inverters with different LCL filters using the grid-side current as feedback was performed. The importance of properly selecting the proportional gains of the current controllers using this model was shown since individually stable inverters can become unstable when connected in parallel because of the effect of the grid inductance. The results from this paper indicated that a method similar to the interactive- and common-current analysis technique used to determine the stability ranges of inverters with identical LCL filers can be implemented on a system with different LCL filer parameters to get a good approximation on the maximum values of the inverters' current controller gains without having to derive the equations of the MIMO system. However, the MIMO model for the plant could be derived if a more accurate result is needed using the method described in this paper to guarantee the stability of the system. Finally, the theoretical analysis was validated through simulations.

3.7 Appendix

$$G_{22} = \frac{i_{o2}}{v_{o2}} = \frac{Z_{31}}{(Z_{12} + Z_{32})(Z_B + \frac{Z_g Z_A}{(Z_g + Z_A)})}$$

$$G_{21} = \frac{i_{o2}}{v_{o1}} = \frac{Z_{31} Z_g}{(Z_{11} + Z_{31})(Z_B + \frac{Z_g Z_A}{(Z_g + Z_A)})(Z_g + Z_A)}$$

$$T_{22} = \frac{i_{o2}}{i_{2ref}} = \frac{G_{22} PI_2^{'} + (PI_1^{'} PI_2^{'})(G_{11} G_{22} - G_{12} G_{21})}{(1 + G_{11} PI_1^{'})(1 + G_{22} PI_2^{'}) - (G_{12} PI_2^{'})(G_{21} PI_1^{'})}$$

$$T_{21} = \frac{i_{o2}}{i_{1ref}} = \frac{G_{21} PI_1^{'}}{(1 + G_{11} PI_1^{'})(1 + G_{22} PI_2^{'}) - (G_{12} PI_2^{'})(G_{21} PI_1^{'})}$$

3.8 Acknowledgments

The authors are grateful to the financial support from the NSF I/UCRC Grid-Connected Advanced Power Electronic Systems (GRAPES) under grant IIP-1439700.

3.9 References

[1] M. Lu, X. Wang, F. Blaabjerg and P. C. Loh, "An analysis method for harmonic resonance and stability of multi-paralleled LCL-filtered inverters," *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Aachen, 2015, pp. 1-6, doi: 10.1109/PEDG.2015.7223086.

[2] J. H. R. Enslin and P. J. M. Heskes, "Harmonic interaction between a large number of distributed power inverters and the distribution network," *IEEE 34th Annual Conference on Power Electronics Specialist, 2003. PESC '03*, Acapulco, Mexico, 2003, pp. 1742-1747 vol. 4, doi: 10.1109/PESC.2003.1217719.

[3] M. Lu, X. Wang, P. C. Loh and F. Blaabjerg, "Resonance Interaction of Multiparallel Grid-Connected Inverters With LCL Filter," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 894-899, Feb. 2017, doi: 10.1109/TPEL.2016.2585547.

[4] J. He, Y. W. Li, D. Bosnjak and B. Harris, "Investigation and Active Damping of Multiple Resonances in a Parallel-Inverter-Based Microgrid," *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 234-246, Jan. 2013,doi: 10.1109/TPEL.2012.2195032.

[5] F. Cavazzana, P. Mattavelli, M. Corradin and I. Toigo, "On the stability analysis of multiple parallel inverters using the impedance multiplication effect," *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, Glasgow, 2016, pp. 1-6, doi: 10.1049/cp.2016.0213.

[6] H. Wei, S. Jianjun, M. Qian, Y. Chenxu, L. Fei and Z. Xiaoming, "Modeling and resonant characteristics analysis of multiple paralleled grid-connected inverters with LCL filter," *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, Pittsburgh, PA, 2014, pp. 3371-3377, doi: 10.1109/ECCE.2014.6953858.

[7] A. Reznik, M. G. Simões, A. Al-Durra and S. M. Muyeen, "LCL Filter Design and Performance Analysis for Grid-Interconnected Systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 2, pp. 1225-1232, March-April 2014, doi: 10.1109/TIA.2013.2274612.

[8] M. Lu, X. Wang, P. C. Loh and F. Blaabjerg, "Resonance Interaction of Multiparallel Grid-Connected Inverters With LCL Filter," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 894-899, Feb. 2017, doi: 10.1109/TPEL.2016.2585547.

[9] M. Lu, X. Wang, P. C. Loh and F. Blaabjerg, "Interaction and aggregated modeling of multiple paralleled inverters with LCL filter," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 1954-1959, doi: 10.1109/ECCE.2015.7309936.

[10] J. L. Agorreta, M. Borrega, J. López and L. Marroyo, "Modeling and Control of N -Paralleled Grid-Connected Inverters With LCL Filter Coupled Due to Grid Impedance in PV Plants," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 770-785, March 2011, doi: 10.1109/TPEL.2010.2095429.

[11] S. G. Parker, B. P. McGrath and D. G. Holmes, "Regions of Active Damping Control for LCL Filters," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 424-432, Jan.-Feb. 2014, doi: 10.1109/TIA.2013.2266892.

3.10 Permissions

Certification of First Author

I hereby certify that David Carballo Rojas is the first author of the article this chapter is based on and has completed at least 51% of the work described in the article.

Juan Carlos Balda

Signature _____

Date _____

CHAPTER 4

DESIGN OF THE SCALED-DOWN REGEN BENCH PROTOTYPE

4.1 Introduction

While the stability analysis of a high-power microgrid with the system parameters of NCREPT regen benches was discussed in the previous chapters, the following chapters will focus on the development and analysis of the scaled-down prototype of a NCREPT regen bench. To accomplish these objectives, the power electronic evaluation (PE-EVAL) board developed by Chris Farnell was used as a starting point and was modified to achieve the following goals:

- A reduction of the size, and thus, cost of the boards.
- A modular printed circuit board (PCB) such that a single design can be used for the active front-end (AFE) rectifier or the inverter of the regen benches, and 3VF.
- A similar system response as the high-power testbed at NCREPT.

The main objective of this chapter is, then, to explain the process for designing and constructing the scaled-down prototype of the high-power microgrid at NCREPT. First, the procedure used for scaling down the 2 MVA back-to-back converters at NCREPT will be explained. Then, the component selection of the power and measurement conditioning stages will be discussed. Finally, the design of the PCB will be presented.

4.2 Design of the Prototype Power Stage

4.2.1 Scaling-Down the Case Study

In order to reduce the power ratings of the 2 MVA back-to-back converters to levels that can be easily tested in a laboratory environment without those safety restrictions typical of high-power application, a per-unit scaling of the high-power microgrid parameters is implemented. A

Table 4.1: Parameters of the High-Power and Scaled-Down Microgrid Testbed

Parameter	NCREPT	Scaled-Down
Rated Power	2 MVA	200 VA
Rated Voltage	480 V	25 V
Rated Current	2.5 kA	4.6 A
DC-Bus Voltage	750 V	42 V
Inverter-Side Inductor	20 µH (0.065 p.u.)	560 µH (0.068 p.u.)
Filter Capacitor	480 µF (0.0208 p.u.)	16.4 µF (0.0193 p.u.)
Grid-side Inductor	12.2 µH (0.04 p.u.)	330 µH (0.04 p.u.)
DC link Capacitor	46.2 mF (2.01 p.u.)	1.8 mF (2.12 p.u.)
Switching Frequency	4 kHz	4 kHz

base power of $S_{base} = 2\ MVA$ and a base voltage of $V_{base} = 480\ V$ are used to obtain the per-unit equivalents of the parameters of the high-power converters. Then, the base power was scaled down to $S_{base,scaled} = 200\ VA$ while the base voltage was scaled to $V_{base,scaled} = 25\ V$. These values were chosen because the power and voltage ratings of the three-phase transformers that were available in the lab were 250 VA, and 25Δ/50Y V, respectively. Then, the per-unit parameters of the high-power microgrid using these base values can be converted into the real system parameters of the scaled-down prototype. A summary of these system parameters and per-unit values of the high-power and scaled-down prototype converters is given in Table 4.1.

Another reason for implementing this per-unit scaling was to obtain a similar open-loop response between the high-power and the scaled-down testbeds. By having a similar response, solutions to improve the system stability in grid-connected mode as well as more advanced control algorithms can be tested first in the scaled-down prototype and then in the high power microgrid at NCREPT. Using the parameters from Table 4.1, the open-loop responses of both systems are plotted and illustrated in Fig. 4.1.

By selecting the same per-unit values for the LCL filters, both systems have about the same resonance frequency which, as discussed in Chapter 2, is one of the main factors in determining the stability of the system in grid-connected mode.

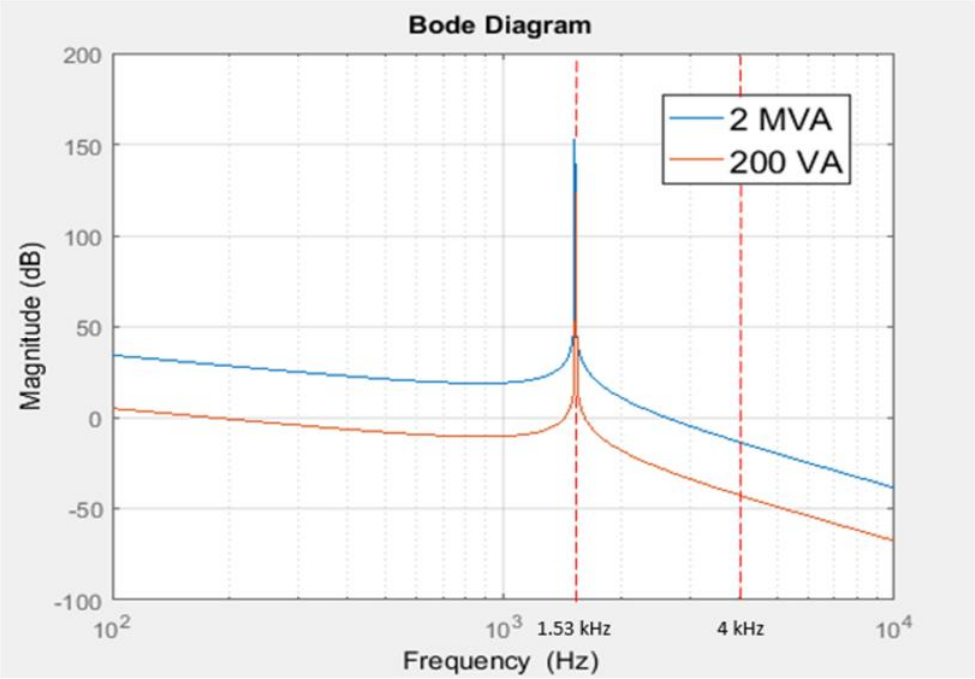


Fig. 4.1: LCL filter open-loop response of the parameters of Table 4.1.

4.2.2 Design of the Gate Driving Circuit

The scaled-down prototype MOSFETs are the SUP70060E from Vishay Intertechnology whose main parameters are listed in Table 4.2. Each of the six MOSFETs in the prototype is driven with a unipolar power supply of $V_{CC} = +15\ V$. This voltage was selected to provide a conservative margin from the maximum voltage ratings of the gate oxide in the MOSFET (± 20 V), as exceeding this voltage can damage the device.

Conventionally, four isolated DC-DC converters are needed to drive the MOSFETs of the VSCs. Using four DC-DC converters, however, is expensive and takes a lot of space in the

Table 4.2: Parameters of Scaled-Down Prototype MOSFETs

Property	Value
Drain-Source Breakdown Voltage	100 V
Gate-Source Voltage	± 20 V
Rated Drain Current @ 25 C	131 A
Maximum Power Dissipation @ 25 C	200 W
Operating Temperature	-55°C to +175°C

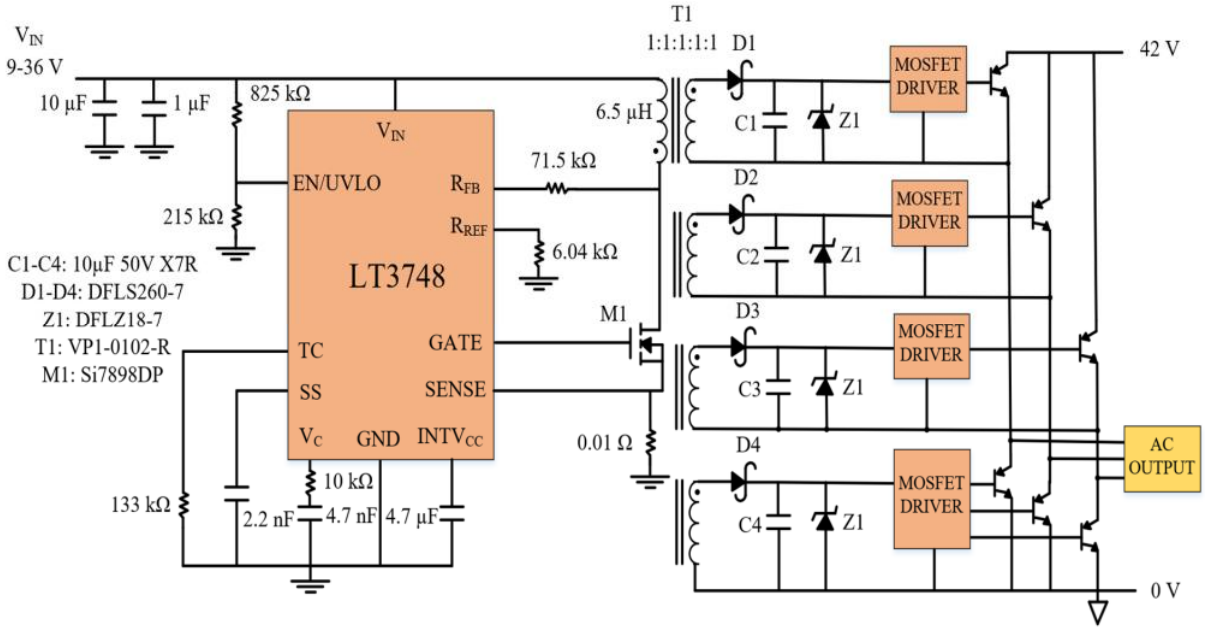


Fig. 4.2: Schematic of the flyback converter configuration.

board. In this prototype, a flyback converter is designed and implemented to provide the required voltages to the MOSFETs. The main advantage of this flyback converter is that it supports multiple isolated output voltages for all the MOSFETs in the board at a cheaper price.

The flyback converter needs an analog switching regulator controller to properly control the output voltage and to guarantee good load regulation. In this prototype, the LT3748 controller from Linear Technology is used. Following the datasheet of the controller, the flyback converter was designed and the schematic with its components is illustrated in Fig. 4.2. This flyback converter has a wide input voltage range from 9V to 36 V and its output voltage can be easily changed by replacing R_{FB} as follows:

$$V_{OUT} = \frac{R_{FB}}{R_{REF}} V_{BG} \tag{1}$$

where V_{BG} is an internal bandgap reference of 1.223 V, and R_{REF} is a fixed resistor of 6.04 kΩ

[1]. Moreover, Zener diodes with a breakdown voltage of 18 V are placed at each of the outputs of the flyback to help with no-load voltage regulation, when the MOSFETs are not switching, and to provide over-voltage protection.

In addition, each MOSFET in the prototype uses the HCPL-3120 isolated gate driver from Broadcom Inc. The main reason to use an isolated gate driver is to reduce the number of components as only one IC is needed to drive the MOSFETs while proving isolation between the low-voltage devices (i.e., the DSP) and the high-voltage components. One important feature of this isolated gate driver is that it provides a maximum low-level output voltage of 0.5 V which, coupled with the fact that the MOSFETs have a gate threshold voltage between 2 V and 4 V, eliminates the need for negative gate drive [2].

This gate driver IC can source up to 2.5 A and sink up to 2.0 A. From this information, the minimum gate driver resistor can be calculated as:

$$R_{G\_\min} \geq \frac{V_{CC}}{I_{peak,source}} = 6\ \Omega \tag{2}$$

A gate resistor closed to this minimum value will have fast switching characteristics at turn-on and turn-off with the downside of an increase of the drain current ringing as well as conducted and radiated EMI noises [3]. From this information, the gate resistor for both turn-on and turn-off was selected as $R_G = 10\ \Omega$, as a compromise between those characteristics. Finally, a capacitor rated 50V and 4.7 µF was placed as close as possible to the input pins of the power stage of the gate driver (i.e., at the positive and negative terminals) in order to smooth low-frequency variations of voltage. Similarly, another capacitor rated 50V and 0.1 µF was placed in parallel with the 4.7 µF capacitor to compensate for the high-frequency oscillations due to the switching of the MOSFETs.

4.2.3 LCL Filter Interface

In this scaled-down design, the LCL filter components are connected externally through terminal blocks instead of being directly mounted on the board. One of the reasons for doing this is to reduce the size and cost of the prototype board, as the LCL filter components would have taken a lot of space in the board. In addition, using those terminal blocks enables a more modular design where the LCL filter components can be easily changed. This allows the use of a single board design for the AFE rectifier or the inverter of the regen benches, and 3VF. Moreover, using this modular design allows one to set-up and analyze different case studies, such as the effect of having grid-connected distributed generators with different filter parameters running in parallel with the regen benches, as presented in Chapter 3.

4.3 Sensors and Measurement Conditioning

4.3.1 Current Sensing Circuit

Isolated hall-effect sensors are used in order to measure the currents needed for the grid-connected operation of the scaled-down prototype. The ACS714 isolated current sensors from Allegro MicroSystems were selected to measure the currents of interest, as opposed to conventional LEM current sensors, due to a cheaper price and smaller form factor. Although each VSC at NCREPT only uses three current sensors to measure the inverter-side currents, the scaled-down prototype has six sensors to measure both the inverter- and grid-side currents. Since one of the goals of the scaled-down prototype is to test more advanced control algorithms before implementing them at NCREPT, these sensors are added to give future students the possibility of testing different control schemes such as drop-controller, observer-based sensorless grid synchronization algorithms, and others [4], [5].

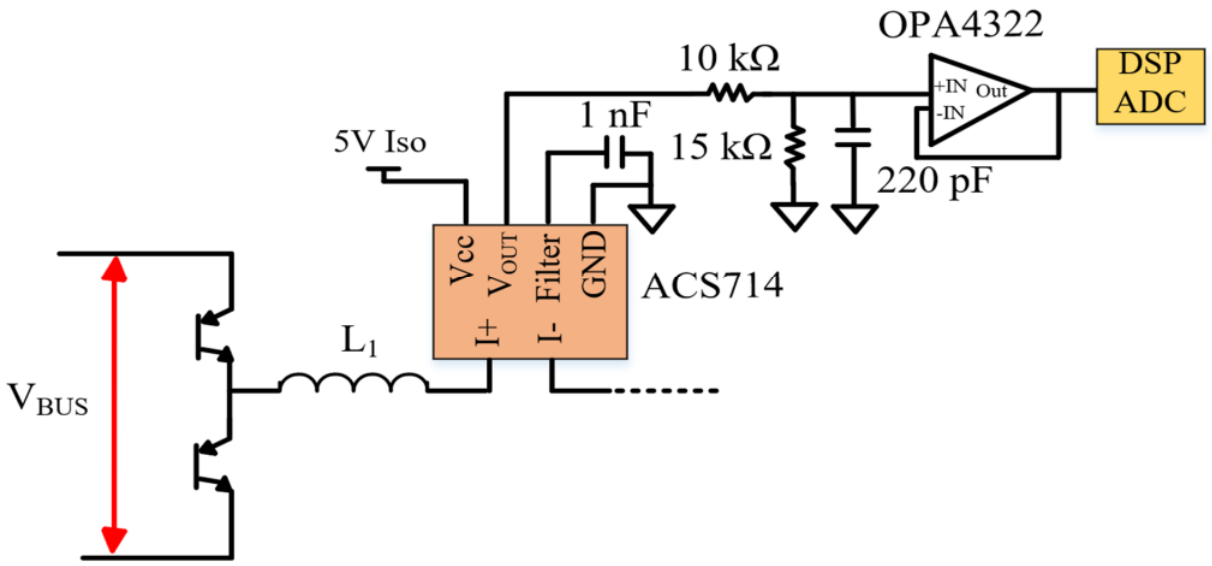


Fig. 4.3: Schematic of ACS714 current sensor configuration.

The schematic of the isolated current sensors used in this scaled-down prototype is presented in Fig. 4.3, where although only one of the sensors is shown, the configuration remains the same for the other sensors. From the figure, the EC4SAW-24S05N isolated DC/DC converter from Cincon is used to supply 5V to all the sensors. A 1 nF capacitor is placed close to the filter pin of the sensor to set the bandwidth and improve the signal-to-noise ratio of the sensor, as recommended by the datasheet. Finally, the output of the sensors goes to the input of an OPA4322 operational amplifier (op-amp) from Texas Instruments to adjust the voltage to one suitable for the voltage levels of the DSP. In this case, the current sensor has an output voltage of 2.5 V with no-load, and thus, a voltage divider is used to scale the signal to 1.5 V, which is half of the maximum voltage that the analog-to-digital converter (ADC) of the DSP can process.

4.3.2 Voltage Sensing Circuit

Similarly, the voltages of interest are measured using the ACPL-C87B isolated operational amplifier from Broadcom Inc. In this case, four isolated voltage sensors are used to

measure the DC-bus voltage, and the phase voltages of the filter capacitors. The schematic of the isolated voltage sensors used in this scaled-down prototype is presented in Fig. 4.4. The maximum input voltage of the sensors is 2 V and, thus, the voltages of interest need to be scaled accordingly by using a voltage divider to avoid exceeding this value. In this case, the resistors of the voltage divider were selected such that a voltage of 66 V is scaled to the maximum input voltage of 2 V. Since the maximum voltage measured by the sensors should be around 42 V, this scaling factor should provide enough margin in case of voltage spikes.

One of the features of this voltage sensor is that it senses a single-ended input voltage and produces a proportional differential output voltage, which helps reduce common-mode noises. An op-amp can, then, be used to convert the differential outputs to single-ended signals to feed to the ADC of the DSP, as illustrated in Fig. 4.4.

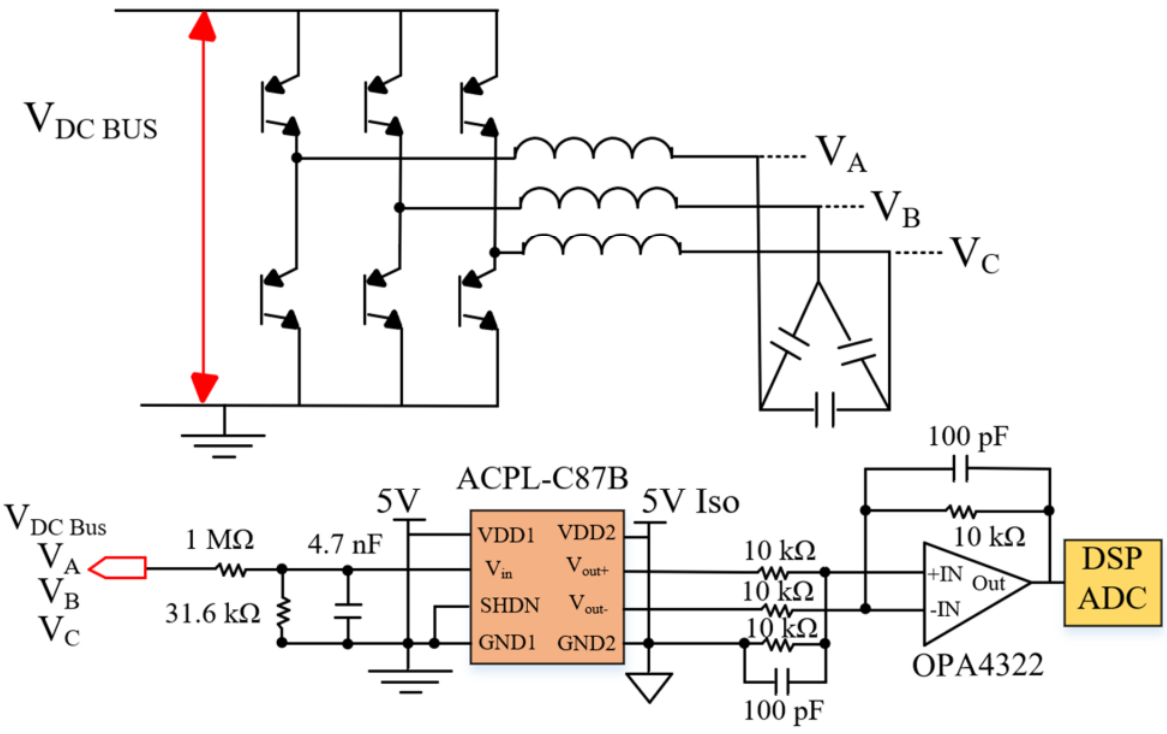


Fig. 4.4: Schematic of ACPL-C87B voltage sensor configuration.

An important detail to take into account is that the single-ended voltages fed to the voltage sensor (i.e., $V_{A,}$ $V_{B,}$ $V_{C,}$ $V_{DC\ BUS}$) are referred to the ground of the DC bus. As such, the voltage measured at the filter capacitors is neither a line-to-line or a line-to-neutral voltage. To obtain a line-to-line voltage, these measured voltages need to be subtracted from one another in the DSP. Finally, the sensor is fed by two 5V power supplies, one relative to the ground of the DC bus (GND1), and another to the logic ground of the DSP (GND2). Thus, the same DC/DC converter used for the current sensors can be used for the outputs of the voltage sensors, but another one is needed for the inputs.

4.4 Design of the Printed Circuit Board

In order to easily integrate the power stage as well as the sensors and measurement conditioning circuit in the same board, a four-layer PCB was designed. Moreover, to reduce the cost of manufacturing, this PCB board was designed with maximum dimensions of 100x150 mm, an area reduction of 20 percent compared to the original board.

Cadence® Allegro® PCB Designer version 17.2 was used to design the layout and routing of the PCB board and to create the positive photoplots of the PCB layers, which are presented in Fig. 4.5 and Fig. 4.6. From the figures, there is a clear division between the power stage of the board (right side) and the sensors and measurement conditioning stage (left side). The main reason for placing them far from one another was to minimize the effect of EMI on the sensitive analog circuitry.

The top and bottom layers of the PCB are illustrated in Fig. 4.5. These layers mainly comprise the traces for the power stage of the board, consisting of the DC bus, the MOSFET outputs, and LCL filter interface. These traces were made as wide and as short as possible in order to increase current capability and decrease stray parasitic inductances. Similarly, the

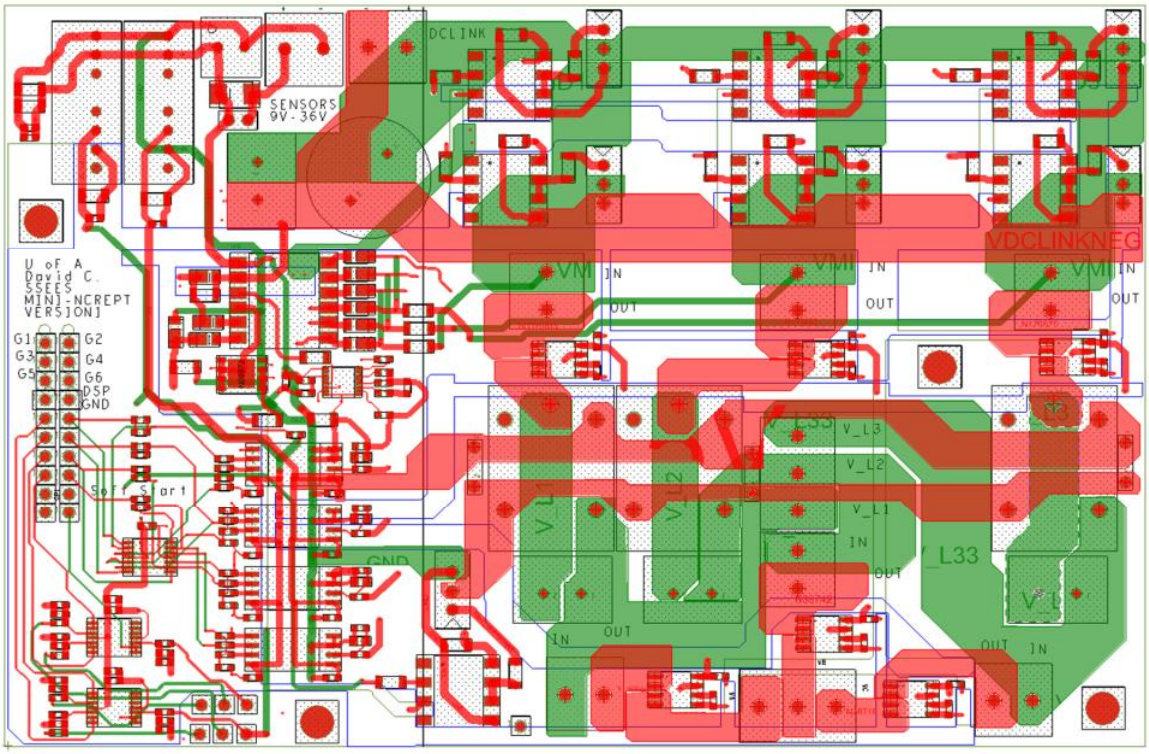


Fig. 4.5: Top (Red), and bottom (Green) layers of PCB board.

isolated gate driver ICs were placed as close as possible to the gate of the MOSFETs to use short traces to decrease gate parasitic inductances. Due to the size restriction of the PCB, the DC-bus capacitor had to be placed horizontally from the MOSFETs. The main downside of this design is that it increases the parasitic inductances of the MOSFETs that are further away from the DC-bus capacitor. To decrease the effect of these parasitics, a bypass film capacitor, rated 250 V and 3.3 µF, is placed between the drain of the top MOSFETs and the source of the bottom MOSFETs. Special care was placed on reducing the parasitic inductances of the power stage, as decreasing these parasitics helps reduce overshoot, and parasitic ringing from the voltage and current switching waveforms [6].

Similarly, the second and third layers of the PCB are illustrated in Fig. 4.6. The second layer mainly comprises the traces for the logic ground of the DSP, which is used by the isolated

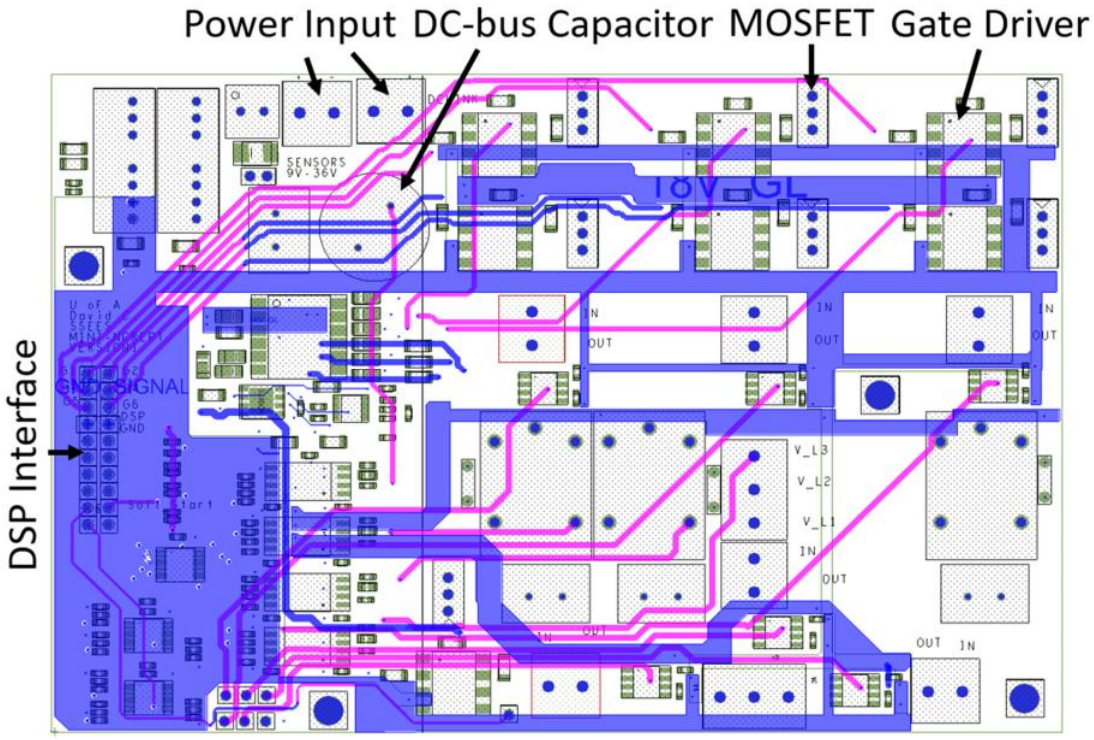


Fig. 4.6: Layer 2 (Blue), and layer 3 (Pink) of PCB board.

current and voltage sensors, and the isolated gate driver ICs. Finally, the third layer consists of the traces for the signals coming from the DSP to control the operation of the MOSFETs, and some traces for interconnections between components. Due to the position of the input interface for the DSP relative to the gate drivers, long traces must be used to connect the two of them, as shown in the figure. These long traces will introduce parasitic inductances that could affect the logic input signals received by the gate drivers. To minimize the effect of these parasitics, a 4.7 nF capacitor was placed at the input of the gate driver ICs to provide a low impedance path to ground for the high-frequency noises.

4.5 Conclusions

The process for designing the scaled-down prototype of the high-power microgrid at NCREPT was addressed in this chapter. This included the per-unit procedure for scaling down

the 2 MVA back-to-back converters at NCREPT to a 200 VA system, which also guaranteed a similar open-loop response between the high- and low-scaled prototype. Furthermore, the process for selecting the components of the power and logic stages of the board as well as for designing the PCB board to minimize the effect of parasitic inductances was presented in this chapter.

After having designed the scaled-down prototype, the next step is to develop and implement the control algorithms for the grid-connected operation of the AFE rectifier and inverter of the system. These algorithms will allow the proper regulation of the power injected/extracted into/from the grid. Thus, the implementation of these control algorithms in a microcontroller is addressed in the next chapter.

4.6 References

[1] Linear Technology, "100V Isolated Flyback Controller," LT3748 datasheet, Feb. 2015.

[2] Broadcom Inc., "2.5 Amp Output Current IGBT Gate Drive Optocoupler," HCPL-3120 datasheet, March 2018.

[3] S. Yin, K. J. Tseng, P. Tu, R. Simanjorang and A. K. Gupta, "Design considerations and comparison of high-speed gate drivers for Si IGBT and SiC MOSFET modules," *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-8.

[4] L. Meng, M. Savaghebi, F. Andrade, J. C. Vasquez, J. M. Guerrero and M. Graells, "Microgrid central controller development and hierarchical control implementation in the intelligent microgrid lab of Aalborg University," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 2585-2592.

[5] J. Kukkola and M. Hinkkanen, "State Observer for Grid-Voltage Sensorless Control of a Converter Under Unbalanced Conditions," in *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 286-297, Jan.-Feb. 2018.

[6] Z. Chen, D. Boroyevich and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," *The 2010 International Power Electronics Conference - ECCE ASIA -*, Sapporo, 2010, pp. 164-169.

CHAPTER 5

IMPLEMENTATION OF THE SYSTEM CONTROL ALGORITHM IN A DSP

5.1 Introduction

Different control algorithms must be developed and implemented in a microcontroller or a digital signal processor (DSP) in order to operate the voltage source converters (VSCs) of the scaled-down prototype as a grid-connected active front-end (AFE) rectifier or inverter. An in-depth explanation of the design and implementation of the control algorithms needed to drive the VSCs into these different operation modes was presented in [1]. As such, the main objective of this chapter is to present the methods used to implement the controller developed in [1] in the Texas Instruments TMS320F28335 DSP, which is a 32-bit floating-point DSP. To accomplish this goal, some of the discrete functions used for the controller will be derived. Then, the initialization of the main DSP modules will be presented. Finally, the process of operation of the controller in the DSP will be explained.

5.2 Derivation of Discrete Functions on the DSP

Some of the main control functions needed for the proper grid-connected operation of the VSCs include the direct-quadrature-zero (DQ0) synchronous frame transformation, the phase-locked loop (PLL) algorithm, and the space vector pulse-width modulation (SVPWM) algorithm. Since the derivation, design, and implementation of these functions in the continuous- and discrete-time domains were performed and thoroughly discussed in [1], they will not be included in this thesis. Also, additional information regarding these functions can be found in [2]-[4]. The objective of this section is to explain some of the functions used for the implementation of the controller in the DSP that were not included in [1].

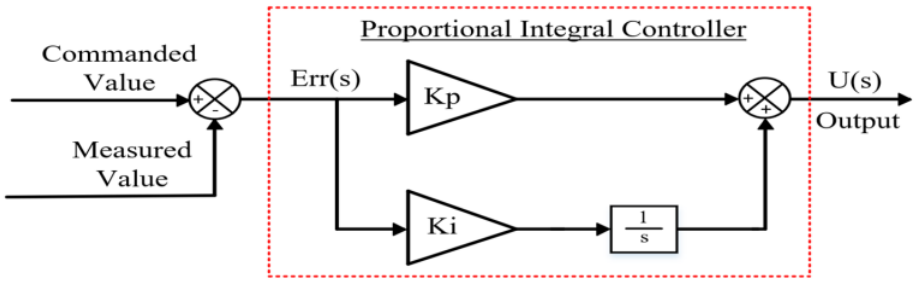


Fig. 5.1: Block diagram for a PI controller.

5.2.1 Proportional Integral (PI) Controller

A PI compensator is a linear controller that calculates the error between a commanded value and its measured value in order to apply a correction based on the controller proportional and integral gains. The block diagram for the PI controller is shown in Fig. 5.1. In this case, the PI controller will be used to control the magnitude and phase angle of the current injected into the grid under the inverter mode of operation, and to control the DC bus voltage and current extracted from the grid for the rectifier mode of operation. The control of these signals, using a conventional PI controller, is made possible due to the transformation of the sinusoidal three-phase variables of the VSCs into DC variables in the synchronous frame [1].

From the figure, the output of the controller in the continuous-time domain can be written as:

$$U(s) = (K_P + \frac{K_I}{s}) \cdot Err(s) \tag{1}$$

where K_P is the proportional gain that sets the bandwidth and "speed" of the controller, and K_I is the integral gain that reduces the steady-state error [5]. The continuous-time expression of (1) must be converted to the discrete-time domain in order to be implemented in the DSP. To accomplish this goal, (1) is first converted to the z domain by using the forward-Euler approximation method, which is defined as:

$$s = \frac{z-1}{T_s} \tag{2}$$

where T_s is the sampling time of the controller. Then, applying the forward-Euler method to (1) and re-arranging the terms yields:

$$U(z) = K_P Err(z) + (K_I T_s - K_P)(Err(z))z^{-1} + (U(z))z^{-1} \tag{3}$$

Finally, the inverse z-transform is used to obtain the discrete function of the PI controller, which is given as:

$$U[k] = K_P Err[k] + (K_I T_s - K_P)(Err[k-1]) + (U[k-1]) \tag{4}$$

The result is a discrete expression for the PI controller that can be easily implemented in the DSP. This is performed by initializing the values of the proportional and integral terms and then calculating (4) at each sampling period.

5.2.2 Second-Order Generalized Integrator (SOGI) Filter

One of the most important factors to consider when implementing the control algorithms is whether the measured signals processed by the DSP are correct. This step is particularly important because if the controller was fed with incorrect measurements the result would be expected to be incorrect as well. Due to the use of long wires to connect the scaled-down prototype board to the DSP development board, the measured signals sampled by the DSP analog-to-digital converter (ADC) may have high-frequency noises and small DC offsets. In order to reduce the effects of these noises, a SOGI filter is implemented in the DSP. However, this filter will be only applied to the voltage signals since applying it to the current measurements will introduce delays that can affect the system dynamic response [6].

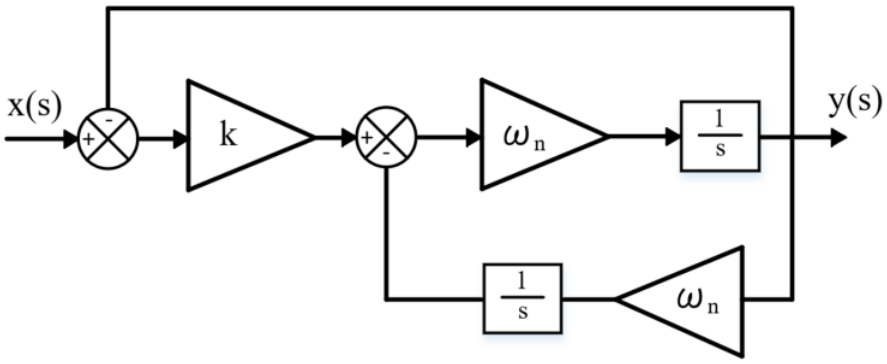


Fig. 5.2: Block diagram of the SOGI filter.

The block diagram of the SOGI filter is illustrated in Fig. 5.2. The transfer function of the SOGI filter in the continuous-time domain can be written as [7]:

$$H_{SOGI}(s) = \frac{y(s)}{x(s)} = \frac{k\omega_n s}{s^2 + k\omega_n s + \omega_n^2} \tag{5}$$

where ω_n is the fundament frequency of the signal (i.e., 60 Hz) and k is a damping coefficient. In order to get a better understanding of the SOGI filter, the Bode plot of the transfer function in (5) is plotted in Fig. 5.3 using different values of k. It becomes clear that the SOGI filter is acting as a band-pass filter that provides unity gain to the signals near the fundamental frequency ω_n while damping those signals outside this "center" frequency. Moreover, the gain k determines the bandwidth of the filter. Thus, this filter should dampen high-frequency noises as well as eliminate any DC offset in the signal.

Similar to the PI controller, the continuous-time transfer function (5) must be converted to the discrete-time domain to be implemented in the DSP. As such, the transfer function will be converted to the z domain by using the trapezoidal approximation, which is given as [2]:

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \tag{6}$$

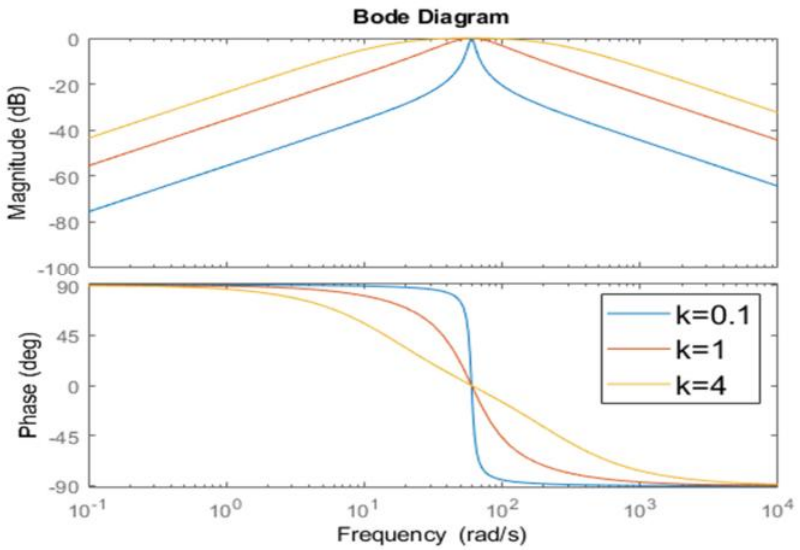


Fig. 5.3: Bode plot of the SOGI filter transfer function with different values of k.

In this case, the trapezoidal approximation was used because it yields better results than the forward-Euler approximation independently of the sampling time [3]. Then, applying the trapezoidal approximation method to (6) and re-arranging the terms yields :

$$H_{SOGI}(z)=\frac{y(z)}{x(z)}=\frac{(\frac{x}{x+y+4})(1-z^{-2})}{1-(\frac{2(4-y)}{x+y+4})z^{-1}-(\frac{x-y-4}{x+y+4})z^{-2}}=\frac{b_o(1-z^{-2})}{1-a_1z^{-1}-a_2z^{-2}} \tag{7}$$

$$y(z)=a_1y(z)z^{-1}+a_2y(z)z^{-2}+b_o(x(z)+x(z)z^{-2}) \tag{8}$$

where $x = 2k\omega_n T_s$ and $y = (\omega_n T_s)^2$. Finally, the inverse z-transform is used to obtain the discrete function of the SOGI filter, which is given as:

$$y[k]=a_1y[k-1]+a_2y[k-2]+b_o(x[k]+x[k-2]) \tag{9}$$

The result is a discrete expression for the SOGI filter that can be easily implemented in the DSP by initializing the gain coefficients (i.e., $a_1, a_1,\ b_0$) and then calculating (9) at each sampling period. Fig. 5.4 illustrates the effect of applying the SOGI filter to a voltage signal

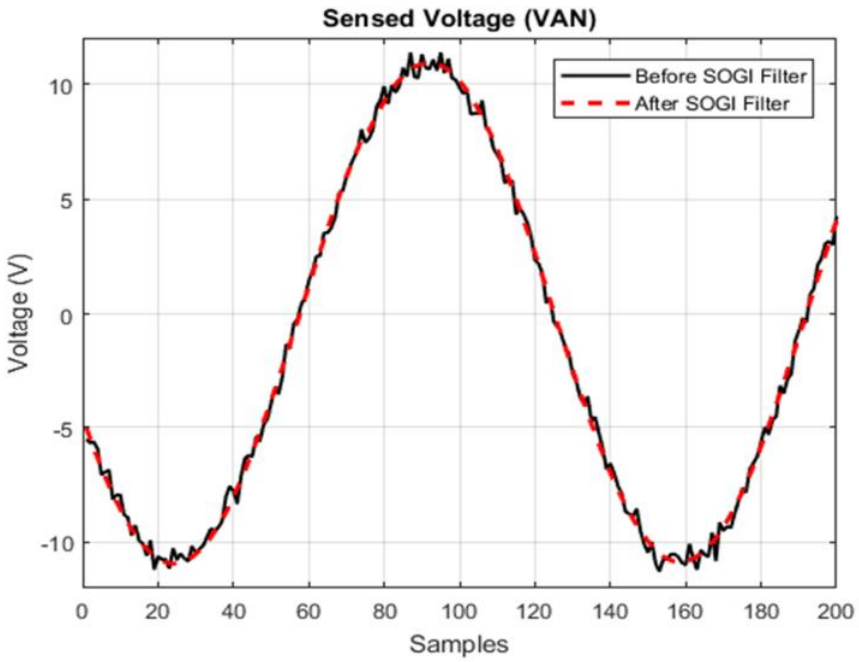


Fig. 5.4: Effect of the SOGI filter on a voltage waveform.

processed by the DSP. From the figure, the SOGI filter reduces the high-frequency noises in the signal and produces a smoother sinusoidal waveform.

5.2.3 DQ0 to α-β Transformation

The inverse Park transformation will be used to converter the output reference voltage of the current controller in the DQ0 rotating reference frame to the α-β stationary reference frame, such that the SVPWM algorithm from [1] can be implemented. This function is derived by finding the inverse matrix of the Park transformation derived in [1], which is given as:

$$\mathbf{V}_{\alpha\beta 0} = (\mathbf{H}_{\text{park}})^{-1}\mathbf{V}_{\mathbf{dq0}} \tag{10}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_o \end{bmatrix} = \begin{bmatrix} \cos(\theta) & -\sin(\theta) & 0 \\ \sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_d \\ v_q \\ v_o \end{bmatrix} \tag{11}$$

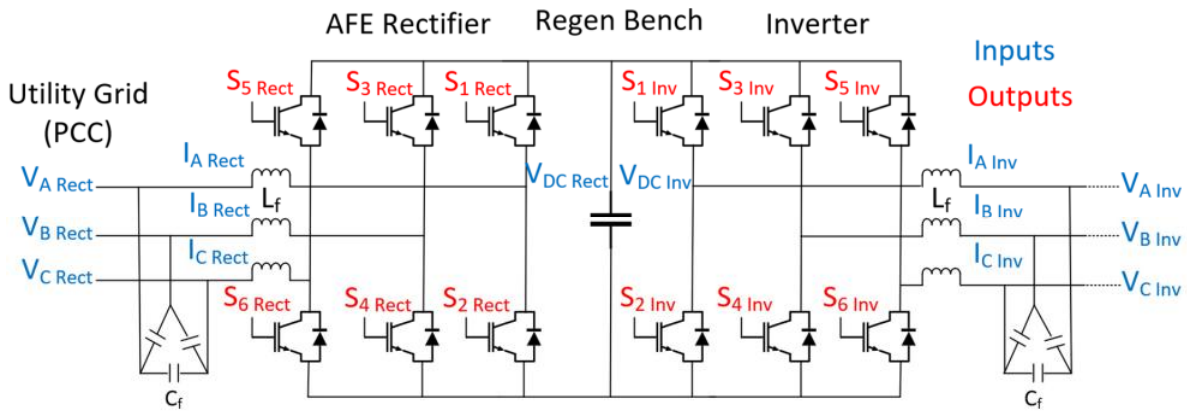


Fig. 5.5: Schematic of the back-to-back VSCs of a regen bench.

5.3 Developing a Single-DSP System

The schematic of the back-to-back VSCs of a regen bench is illustrated in Fig 5.5. To control the operation of the AFE rectifier and inverter with a single DSP, the DSP should be fast enough to execute the control algorithms of both VSCs and have enough input /output (I/O) pins. From the figure, a total of twelve output pins are needed to drive the gates of the MOSFETs and fourteen input pins are required to sample the currents and voltages of interest.

Currently, two Texas Instruments TMS320F2812 DSPs are used in each regen bench at NCREPT to control the operation of the VSCs (i.e., one for the AFE rectifier and one for the inverter). However, these DSP units have become outdated because they use the fixed-point numerical system, which has an inherent tradeoff between range and resolution [6]. Conversely, the TMS320F28335 DSP uses the floating-point numerical system, which allows an easier and more convenient implementation of different control algorithms. For this reason, the control boards designed by ABB Baldor with the TMS320F2812 DSP are being replaced with new control boards with the TMS320F28335 DSP. Replacing those boards will allow the control of both VSCs using a single DSP. Thus, a single TMS320F28335 DSP board will be used in the scaled-down prototype to control the VSCs of a regen bench. The DSP module configuration to

Table 5.1: ADC Module Input Signals

Regen-Bench Inverter ADC Input Channel	Regen-Bench AFE Rectifier ADC Input Channel	Input Analog Signals
ADCINA0	ADCINB0	Phase A converter-side current (I_A)
ADCINA1	ADCINB1	Phase B converter-side current (I_B)
ADCINA2	ADCINB2	Phase C converter-side current (I_C)
ADCINA4	ADCINB4	DC bus voltage (V_{DC})
ADCINA5	ADCINB5	Phase A filter capacitor voltage (V_A)
ADCINA6	ADCINB6	Phase B filter capacitor voltage (V_B)
ADCINA7	ADCINB7	Phase C filter capacitor voltage (V_C)

accomplish this goal will be discussed next.

5.3.1 Analog-to-Digital Converter Module

An ADC is a device that converters analog signals coming from voltage and current sensors into digital signals that can be processed by the DSP. The ADC module in the TMS320F28335 DSP has two independent eight-channel modules. This means that a total of sixteen input signals can be sampled every time that the ADC is "called". Although there are many input channels, there is only one ADC in the DSP. For this reason, two separate eight-input multiplexors, ADCA and ADCB, are integrated into the ADC module to determine which input channel is sampled at a time. These multiplexers can operate together or independently. In this case, the ADC module is initialized into the cascade mode to form an equivalent sixteen-channel multiplexer. This was done because a total of fourteen voltage and current signals must be sampled in order to implement the controller of a regen bench in a single DSP, as illustrated in Fig. 5.5. A list of these signals and their ADC input channels is presented in Table 5.1.

One of the most important features of an ADC is its resolution. The ADC of the TMS320F28335 DSP allows analog inputs from 0 V to 3 V, whose results are stored in a 12-bit register. This means that when a 3 V analog signal is applied to the input of the ADC, its digital output is 4095. Similarly, applying 0 V produces a digital output of 0. From this information, the

resolution of the ADC can be calculated as:

$$ADC_{\text{Resolution}} = \frac{3\text{ V}}{2^{12}} = 0.73242\text{ mV} \tag{12}$$

The next step is to configure the registers that control the operation of the ADC. The module is initialized to the "start/stop" mode, where the ADC only starts sampling the input channels when it receives a start-of-conversion (SOC) signal from an external source. While there are many options for this external source, the submodule was configured such that the Enhanced Pulse Width Modulator (ePWM) module would trigger the SOC sequence. The initialization of the ePWM module to trigger the SOC of the ADC is covered in the next section.

One of the most convenient features of the ADC module for implementing PWM algorithms is the ability to generate interrupts. Usually, these PWM algorithms require that a control signal be updated at least every switching period. As such, these interrupts will trigger the execution of interrupt service routines (ISRs) at least once every switching period to update those PWM control signals. In this case, the ADC module is initialized to generate an interrupt trigger at every end-of-sequence (EOS). That is, every time the ADC finishes sampling all the input channels, a trigger is generated to execute the ISR.

5.3.2 Enhanced Pulse Width Modulator Module

The TMS320F28335 DSP has six ePWM modules that simplify the implementation of PWM algorithms. Each of those modules is comprised of two outputs, ePWMxA and ePWMxB, proving a total of 12 outputs. These are just enough outputs to control the three-phase two-level topology of the VSCs. The mapping of the ePWM module outputs to the GPIO pins of the DSP is given in Table 5.2. In addition, the mapping of the I/O signals of the VSCs from Fig 5.5 to the scaled-down prototype board is presented in Fig. 5.6. In order to use the ePWM modules to

Table 5.2: EPWM Module Output Signals

Regen-Bench Inverter				
ePWM Module	ePWM Module Outputs	GPIO Pin	VSC Phase	Symbol
EPWM1	EPWM1A EPWM1B	GPIO00 GPIO01	Phase A	$S_{1\ Inv}$ $S_{2\ Inv}$
EPWM2	EPWM2A EPWM2B	GPIO02 GPIO03	Phase B	$S_{3\ Inv}$ $S_{4\ Inv}$
EPWM3	EPWM3A EPWM3B	GPIO04 GPIO05	Phase C	$S_{5\ Inv}$ $S_{6\ Inv}$
Regen-Bench AFE Rectifier				
ePWM Module	ePWM Module Outputs	GPIO Pin	VSC Phase	Symbol
EPWM4	EPWM4A EPWM4B	GPIO06 GPIO07	Phase A	$S_{1\ Rect}$ $S_{2\ Rect}$
EPWM5	EPWM5A EPWM5B	GPIO08 GPIO09	Phase B	$S_{3\ Rect}$ $S_{4\ Rect}$
EPWM6	EPWM6A EPWM6B	GPIO10 GPIO11	Phase C	$S_{5\ Rect}$ $S_{6\ Rect}$

implement the SVPWM algorithm developed in [1], the registers of the six modules must be properly initialized. Although only the main registers of the module will be discussed in this thesis, the description of all available registers is given in [8].

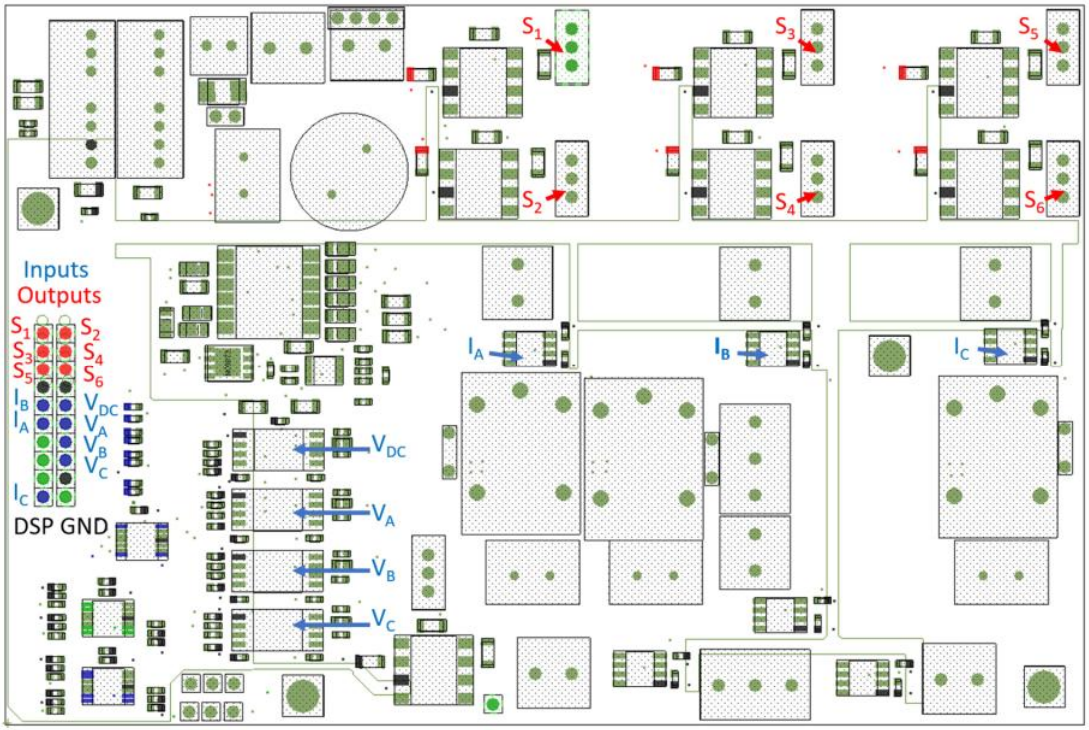


Fig. 5.6: Mapping of I/O signals of the VSC to the scaled-down prototype board.

One of the main features of the ePWM modules is the in-built time-based counter that can be used to emulate the carrier waveform of the PWM algorithms. This register was set to the up-down count mode in order to create a symmetrical triangular carrier waveform, instead of an asymmetrical sawtooth in the up or down mode. This mode was selected because it was the only one which allowed having the sampling frequency of the controller at twice the switching frequency without having to use other DSP modules.

The next step is to configure the length or period of the time-based counter. This period is measured in clock cycles, which is set to 150 MHz. This means that the counter of the ePWM modules is increased by one every 6.67 ns. Then, the counter needs to keep increasing until it reaches half of the switching period since the triangular waveform was selected. As such, the period of the timer is calculated as [8]:

$$TBPRD = \frac{1}{2}\left(\frac{TBCLK}{f_{sw}}\right) = \frac{1}{2}\left(\frac{150\text{ MHz}}{4\text{ kHz}}\right) = 18{,}750\text{ clock cycles} \tag{13}$$

Next, the counter-compare submodule within each ePWM module must be configured. The registers of this submodule determine the actions that the module performs when the time-based counter reaches certain values. In this case, the counter is compared with the control signals generated by the SVPWM algorithm in order to determine whether to turn on or off the MOSFETs. These control signals are loaded to the counter-compare registers every sampling period when the counter reaches zero or the value of TBPRD, which was calculated in (13). Moreover, double buffer registers, called shadow registers, are enabled to allow the control signals to be loaded to the active registers of the module only at strategic points in time, which prevents data corruption [8]. This submodule is configured such that when the triangular the waveform has a higher value than the control signal, the output of PWM module is 1. Similarly,

output of the module is 0 when the carrier waveform is lower than the control signals.

Then, the dead-band submodule of the modules is initialized in order to automatically introduce a deadtime on the rising edge of output EPWMxA and on the falling edge of output EPWMxB. Moreover, just like the time-based counter, the dead-band is specified in terms of the numbers of clock cycles. In this case, both the rising and falling delay times have been initialized to 200 clock cycles, which translates to a deadtime of 1.3µs. This value was conservatively selected following the guidelines from [9], [10]. Next, an active-high complementary mode is implemented in this submodule in order to send complementary signals to the top and bottom MOSFETs of the VSCs.

Finally, the event-trigger submodule is initialized in order to send the ADC SOC signals. As mentioned before, these signals indicate the times the ADC starts sampling the signals from the different input channels. In this case, the submodule is configured such that EPWM1A sends the SOC signal when the time-based counter reaches the value of TBPRD from (13) while EPWM1B sends the signal when the counter reaches zero. As a result, the sampling frequency of the controller is twice its switching frequency.

The operation of the ePWM module with the configuration discussed in this section is illustrated in Fig. 5.7. A triangular waveform is generated by the time-based counter of the module and compared with a control signal in order to generate the complementary PWM outputs of a VSC phase. Then, a SOC signal is sent to the ADC to start sampling the voltages and currents when the counter reaches zero and TBPRD. When it finishes sampling, the ISR is executed to calculate the value of the new control signal. That is loaded into the shadow register, but it is not loaded to the active register of the module until the end of the sampling period.

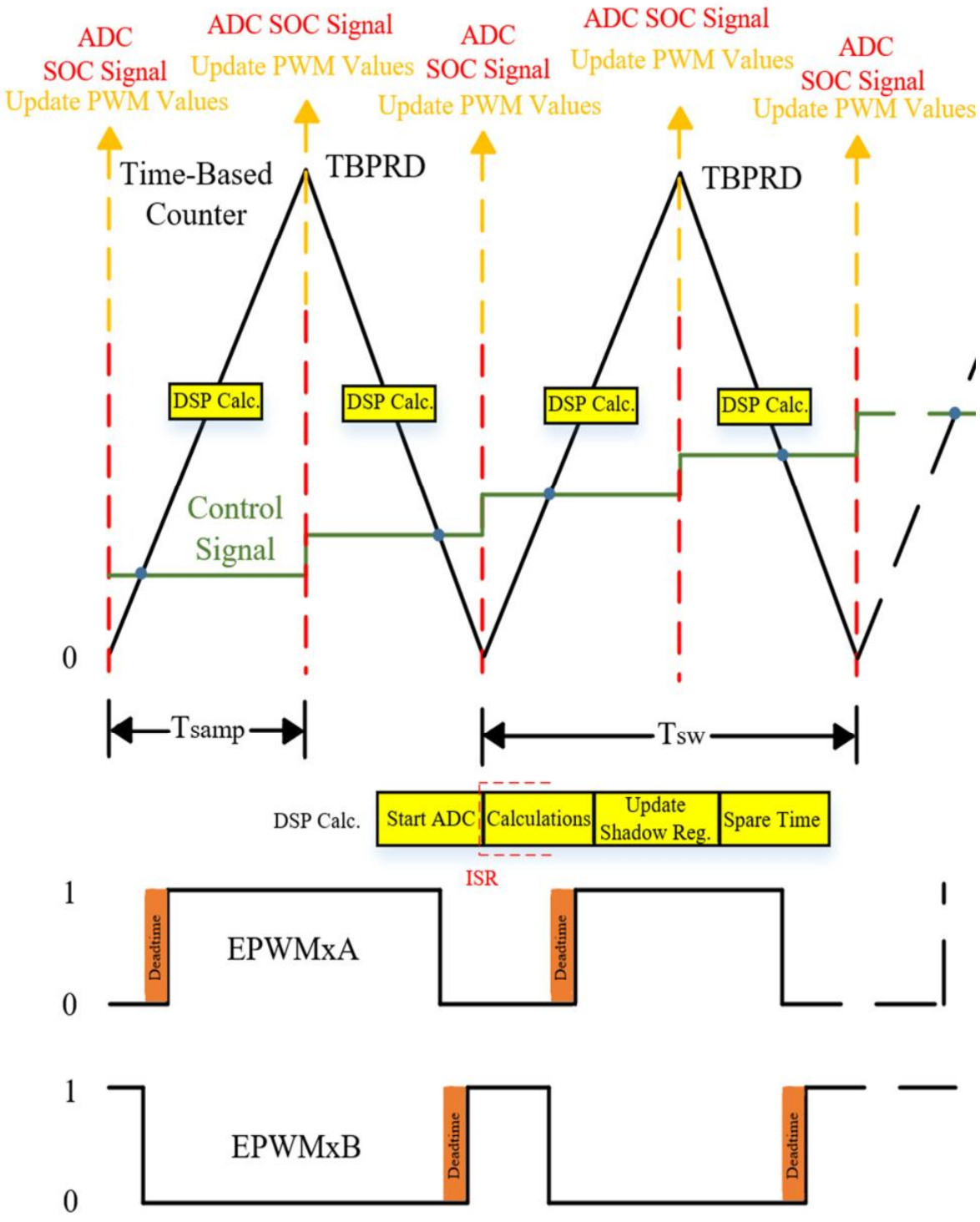


Fig. 5.7: Operation of the ePWM module.

5.4 Controller Implementation in the DSP

5.4.1 Scaling of the ADC Results

In order to implement the different control functions, the digital representation of the voltages and currents of the VSCs (i.e., after being sampled by the ADC) must be transformed into actual system values in the DSP. To calculate these measurement values, the outputs of the ADC must be scaled with respect to the resolution of the ADC as well as the configuration of the conditioning circuitry of the sensors.

In the case of the isolated voltage sensors, a voltage divider circuit is used to scale down the actual voltage from 66 V to 2V. Therefore, the digital representation of this voltage is calculated as:

$$ADC_{Digital} = (\frac{2\ \mathrm{V}}{66\ \mathrm{V}})(\frac{2^{12}}{3\ \mathrm{V}})(V_{\mathrm{Re}al}) \tag{14}$$

Thus, to transform the digital representation of the voltages to actual values, the outputs of the ADC must be multiplied by the inverse gain of (14); that is:

$$V_{\mathrm{Re}al} = (\frac{66\ \mathrm{V}}{2\ \mathrm{V}})(\frac{3\ \mathrm{V}}{2^{12}})(ADC_{Digital}) \tag{15}$$

As discussed in Chapter 4, an issue with the voltage sensors is that since the single-ended inputs of the sensors are referred to the ground of the DC bus, the voltage measured at the filter capacitors is neither a line-to-line or a line-to-neutral voltage. However, the three-phase line-to-neutral voltages must be calculated to implement the control functions of the controller. To calculate these voltages, first, the line-to-line voltages are obtained by subtracting the single-ended measurement of (15) from one another. Then, the line-to-neutral voltages are calculated by using basic vector operations as follows:

$$\mathbf{V_{AN}} = -(\mathbf{V_{BC}} + 2\mathbf{V_{CA}})/3 \tag{16}$$

$$\mathbf{V_{BN}} = -(\mathbf{V_{CA}} + 2\mathbf{V_{AB}})/3 \tag{17}$$

$$\mathbf{V_{CN}} = -(\mathbf{V_{AB}} + 2\mathbf{V_{BC}})/3 \tag{18}$$

A similar process is performed for the isolated current sensors. The main differences are that the outputs of the current sensors have a DC offset of 2.5 V at no-load, and a gain of 185 mV/A. This means that when 1 A is flowing the current sensor should output 2.685 V. Moreover, a voltage divider circuit is used to scale down the output voltage of the sensor from 5 V to 3 V. Therefore, the digital representation of the input current is calculated as:

$$ADC_{Digital} = (\frac{3\text{ V}}{5\text{ V}})(\frac{2^{12}}{3\text{ V}})(2.5\text{ V} + \frac{185\text{ mV}}{A})(I_{Real}) \tag{19}$$

Thus, to transform the digital representation of the currents to actual values, the outputs of the ADC must be multiplied by the inverse gain of (19) as follows:

$$I_{Real} = (\frac{5\text{ V}}{3\text{ V}})(\frac{3\text{ V}}{2^{12}})(2.5\text{ V} + \frac{185\text{ mV}}{A})^{-1}(ADC_{Digital}) \tag{20}$$

5.4.2 DSP Control Flow

Fig. 5.8 illustrates the DSP implementation of the control algorithms used to operate the VSCs of the scaled-down regen bench as grid-connected AFE rectifier and inverter. After initializing the DSP modules, as described in section 5.3, the ADC starts sampling the voltages and currents of the VSCs when it receives a SOC trigger signal from the ePWM module every 125 μS (period of an 8 kHz signal). Since the sampling frequency is equal to twice the switching frequency, the stability of the system should be improved, as explained in Chapter 2. Then, when the ADC finishes sampling all the input channels, it generates an interrupt that will trigger the

execution of the ISR. Inside the ISR, the digital outputs of the ADC are first transformed back into actual values. Then, the SOGI filter is used to dampen the high-frequency noises from the voltage measurements. Next, the DSP executes the PLL algorithm to obtain the phase angle of the grid voltage to transform the VSC voltages and currents into the DQ-reference frame.

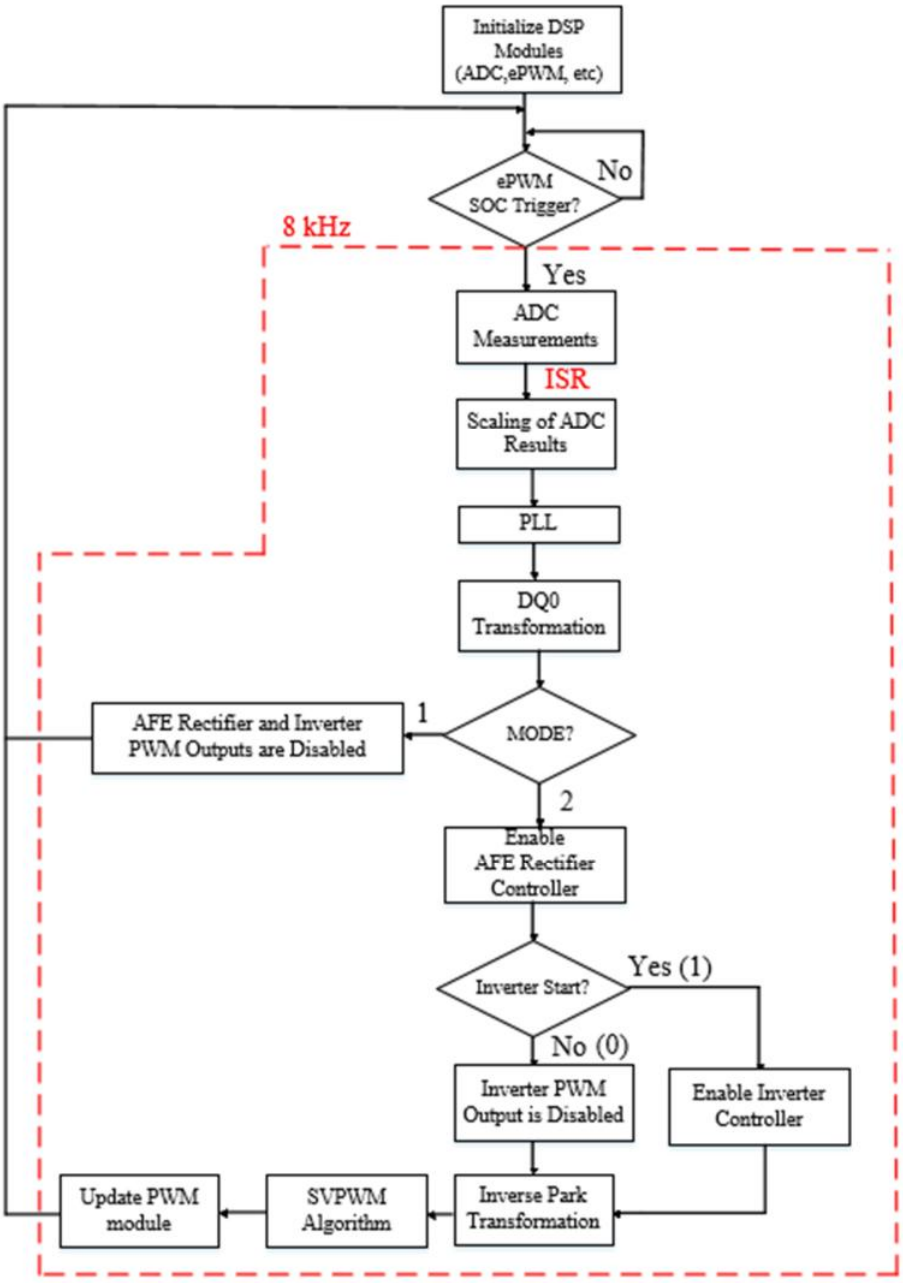


Fig. 5.8: Flowchart of the DSP processes.

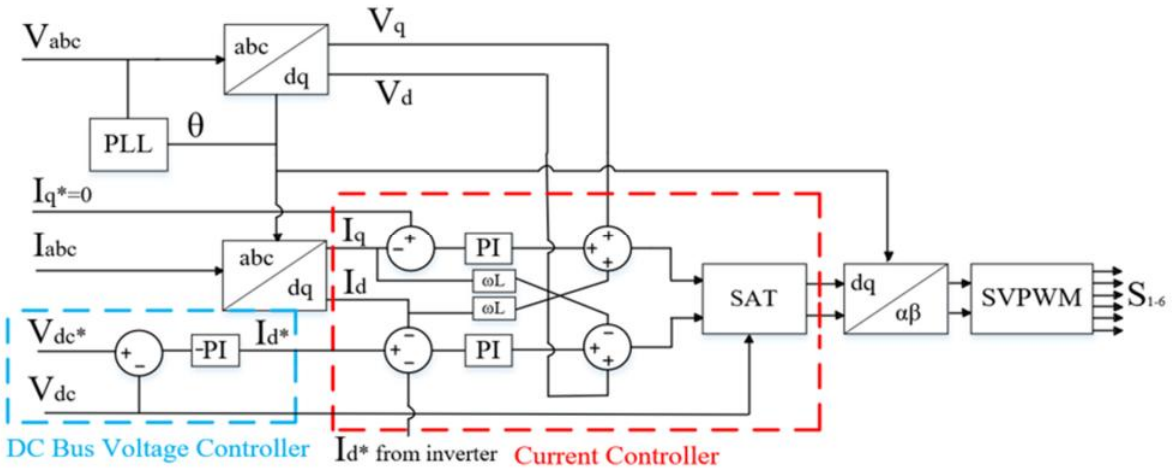


Fig. 5.9: Control diagram of a grid-connected AFE rectifier.

The next action depends on the mode selected by the user. By default, the controller starts in mode 1. In this mode, the outputs of the PWM are disabled and, thus, neither the AFE rectifier or the inverter are operating. As a result, the VSCs act as a full-wave three-phase uncontrolled bridge rectifier. When the user sends a command to set the mode to 2, the PWM outputs of the AFE rectifier are enabled and the DSP executes the rectifier controller, which is illustrated in Fig. 5.9. This controller uses two PI compensators, as discussed in section 5.2, to regulate the voltage of the DC bus; one for the voltage controller and one for the current controller. The first controller senses the error between a reference and its measured voltage and produces a reference current to reduce that error. For instance, if the voltage of the DC bus was less than the commanded reference, the voltage controller will generate a specific reference to draw more current from the grid in order to increase the voltage level of the bus. Then, a current controller is used to properly track the reference current generated by this voltage controller. Finally, a saturation block (SAT) is implemented to prevent the converter from going into the overmodulation region [6]. More information about this controller, its derivation and design process can be found in [1].

While the AFE rectifier starts operating as soon as the mode is set to 2, the operation of the inverter will depend on a variable in the DSP called “Inverter Start.” If this variable is set to 0, the PWM outputs of the inverter are disabled and only the rectifier will be operating; this is the default setting of the controller at startup. However, writing a 1 to this variable enables the PWM outputs of the inverter and the execution of the current controller shown in Fig. 5.10. This current controller uses PI compensators to ensure that the current injected into the grid follows a reference current provided by the user. Like the rectifier controller, a saturation block is implemented to avoid the overmodulation region.

Then, the output reference voltages produced by those controllers are transformed from the DQ0 reference frame to the α-β stationary frame using the inverse Park transformation, as presented in section 5.2. With the output reference voltage in the stationary frame, the SVPWM algorithm is executed to generate the control signals for the ePWM modules. Finally, these control signals are compared with the triangular carrier waveform to generate the gate signals for the MOSFETs of the AFE rectifier and inverter in the scaled-down regen bench.

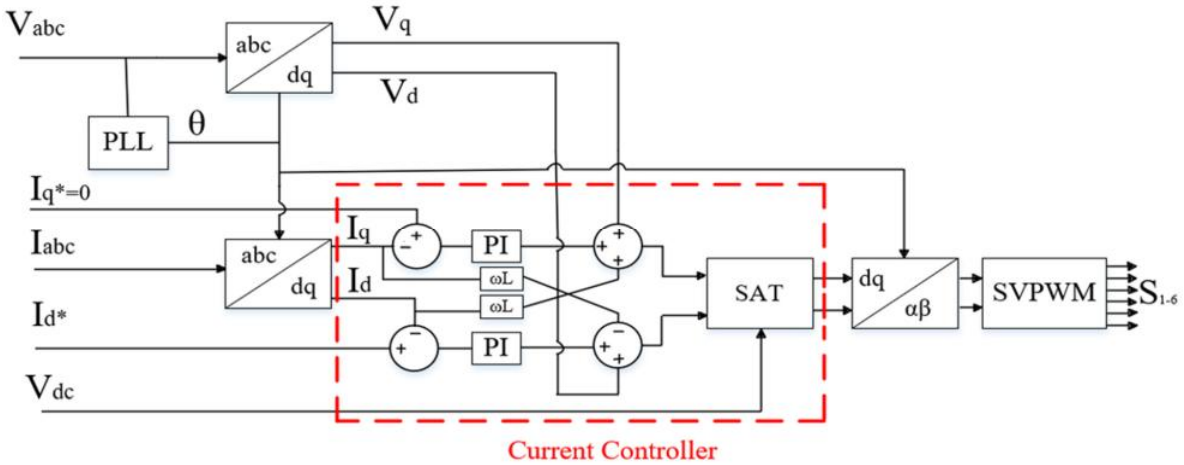


Fig. 5.10: Control diagram of a grid-connected inverter.

5.5 Conclusions

The process for implementing the controller of a grid-connected AFE rectifier and an inverter in a single TMS320F28335 DSP was addressed in this chapter. This included the derivation of some discrete functions for the controllers as well as the highlights for initializing the ePWM and ADC modules in the DSP. Moreover, the complete copy of the C program used in this project is given in Appendix A and Appendix B. Thus, the prototype board was designed in Chapter 4 and the controller implemented in a DSP in this chapter. The results of the prototype system testing are presented in Chapter 6.

5.6 References

[1] Escala, Edgar, "Developing Primary and Tertiary Controllers for Microgrids Using HIL Tools" (unpublished). MSEE Thesis, University of Arkansas

[2] Texas Instruments, C28x Solar Library Module User's Guide, 2014.

[3] F. J. Rodriguez, E. Bueno, M. Aredes, L. G. B. Rolim, F. A. S. Neves and M. C. Cavalcanti, "Discrete-time implementation of second order generalized integrators for grid converters," *2008 34th Annual Conference of IEEE Industrial Electronics*, Orlando, FL, 2008, pp. 176-181.

[4] Texas Instruments, "Software Phase Locked Loop Design Using C2000™ Microcontrollers for Three Phase Grid Connected Applications," Application Note SPRABT4A, 2013.

[5] Kiam Heong Ang, G. Chong and Yun Li, "PID control system analysis, design, and technology," in *IEEE Transactions on Control Systems Technology*, vol. 13, no. 4, pp. 559-576, July 2005.

[6] Liu, Yusi, "Realization of a High Power Microgrid Based on Voltage Source Converters" (2017). Doctoral Dissertation, Univeristy of Arkansas.

[7] S. Golestan, M. Monfared and J. M. Guerrero, "Second order generalized integrator based reference current generation method for single-phase shunt active power filters under adverse grid conditions," *IEEE 4th Annual International Power Electronics, Drive Systems and Technologies Conference*, Tehran, 2013, pp. 510-517.

[8] Texas Instruments, "TMS320x2833x,2823x Enhanced Pulse Width Modulator (ePWM) Module," Reference Guide SPRUG04A, 2009.

[9] Broadcom Inc., "2.5 Amp Output Current IGBT Gate Drive Optocoupler," HCPL-3120 datasheet, March 2018.

[10] Vinson, Jones, "Correcting Current Imbalances in Three-Phase Four-Wire Distribution Systems" (2016). MSEE Thesis, University of Arkansas.

CHAPTER 6

TESTING OF THE SCALED-DOWN REGEN BENCH PROTOTYPE

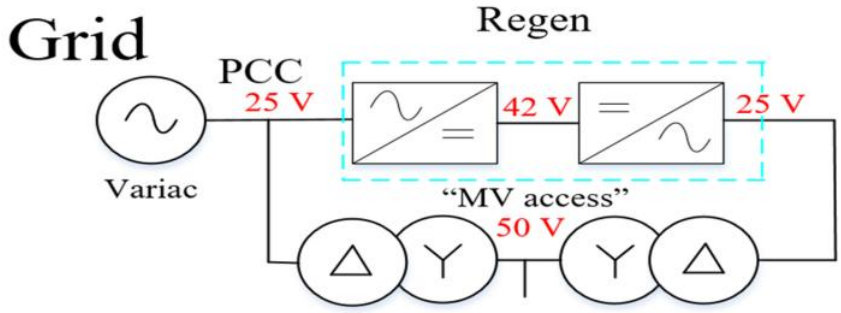
6.1 Introduction

In this chapter, the experimental results of the scaled-down regen bench prototype will be presented and analyzed. Two tests will be first conducted to ensure that there are no stability issues in the system. First, a single scaled-down regen bench connected to the grid to verify the proper operation of the prototype. Then, two regen benches connected in parallel to warrant the absence of resonance issues due to interactions among the converter output filters. Finally, the analysis of the experimental results and solutions to improve the performance of the system will be presented.

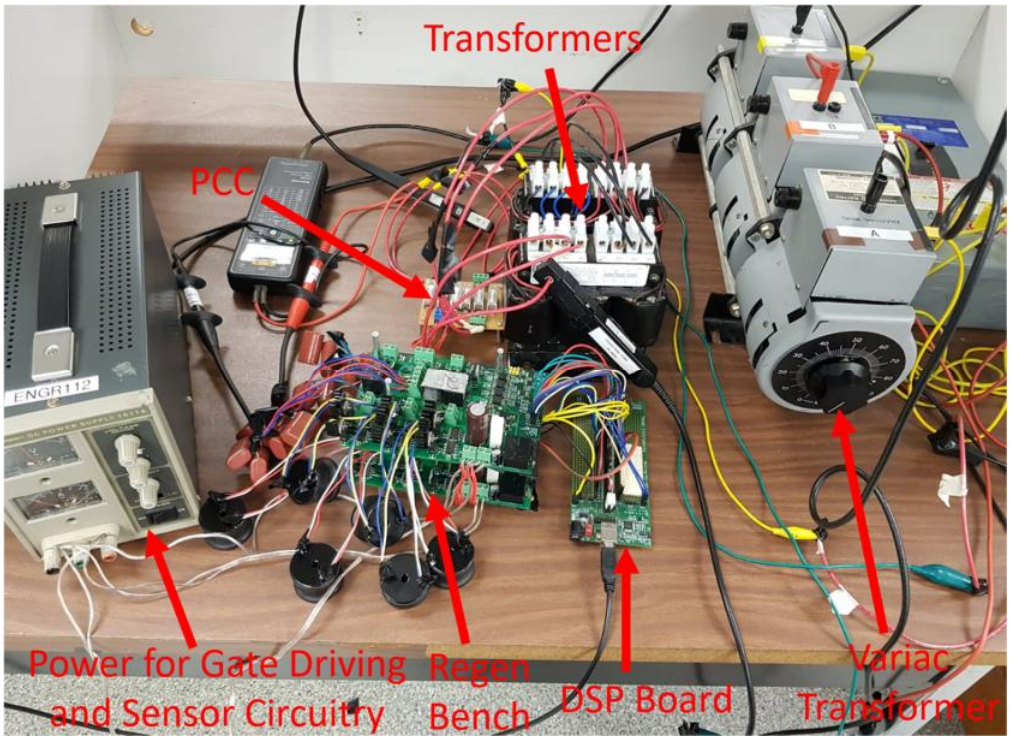
6.2 Testing of a Single Scaled-Down Regen Bench

The experimental setup used to test the scaled-down regen bench prototype is illustrated in Fig. 6.1. The system consists of:

- Two boards designed in Chapter 4 that implement as the inverter and active-front-end (AFE) rectifier of the regen bench.
- A variable autotransformer (variac) that behaves as the grid, and the point of common coupling (PCC) for the inverter and AFE rectifier.
- A single DSP board to control the operation of the inverter and rectifier, as described in Chapter 5.
- Two transformers that provide galvanic isolation and break the common-mode path between the rectifier and inverter stages of the regen bench [1].
- A DC power supply for the gate driving and sensor circuitry of the converters.



(a)



(b)

Fig. 6.1: (a) One-line diagram, and (b) photograph of a single scaled-down regen bench.

6.2.1 Transient Response of a Single Regen Bench

Although the main focus of the thesis is to ensure the stability of the regen bench under steady-state condition, the dynamics of the inverter and rectifier are initially tested to verify that the prototype is working as expected. As such, the step response of the rectifier and inverter are obtained and compared with theoretical and simulation results. In this case, the simulation results

are generated by modifying the simulation files from [2] with the parameters of the scaled-down prototype.

Fig. 6.2 illustrates the transient response of the AFE rectifier when applying a step change in the DC bus voltage from 20 V to 30 V. The voltage controller of the AFE rectifier was designed such that it would have a settling time of about 63.7 ms. As such, the values of the PI controllers were selected using the design procedure from [2] and presented in Table 6.1. In this case, the PI controller was design to achieve an overdamped response in order to avoid any controller instability once multiple regen benches were tested in parallel. There is good agreement between the experimental and simulation results. Moreover, the DC-bus voltage was close to the designed value since the settling time of the experiment results was around 69.4 ms.

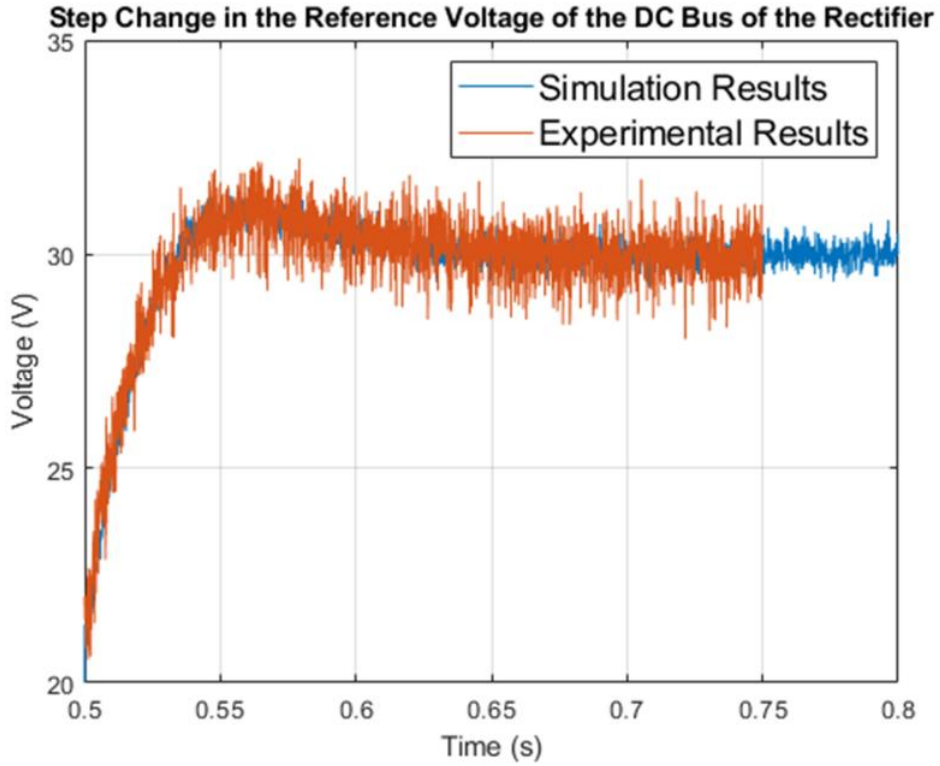


Fig. 6.2: Step change in the reference voltage of the DC bus of the AFE rectifier.

Table 6.1: PI Controller Values for the Regen Benches

DC Bus Voltage Controller		Current Controller	
Parameter	Value	Parameter	Value
Proportional Gain ($K_{P\ V}$)	-0.2262	Proportional Gain ($K_{P\ C}$)	0.6668
Integral Gain ($K_{I\ V}$)	-7.1061	Integral Gain ($K_{I\ C}$)	1921

Similarly, Fig. 6.3 shows the transient response of the inverter when applying a step change in the reference current from 0 A to 1 A. The PI gains of the current controller are the same as the ones in Table 6.1 and the settling time is 10 times smaller than the one in the voltage controller of the rectifier (i.e., 6.37 ms). The experimental and simulation results are closed to one another. The main difference between them is that the experimental results have a slightly higher overshoot, which could be due to some parametric discrepancies between the experiment and simulation setups. In addition, the settling time for the experimental result was around 7.2 ms, which is close to the designed value.

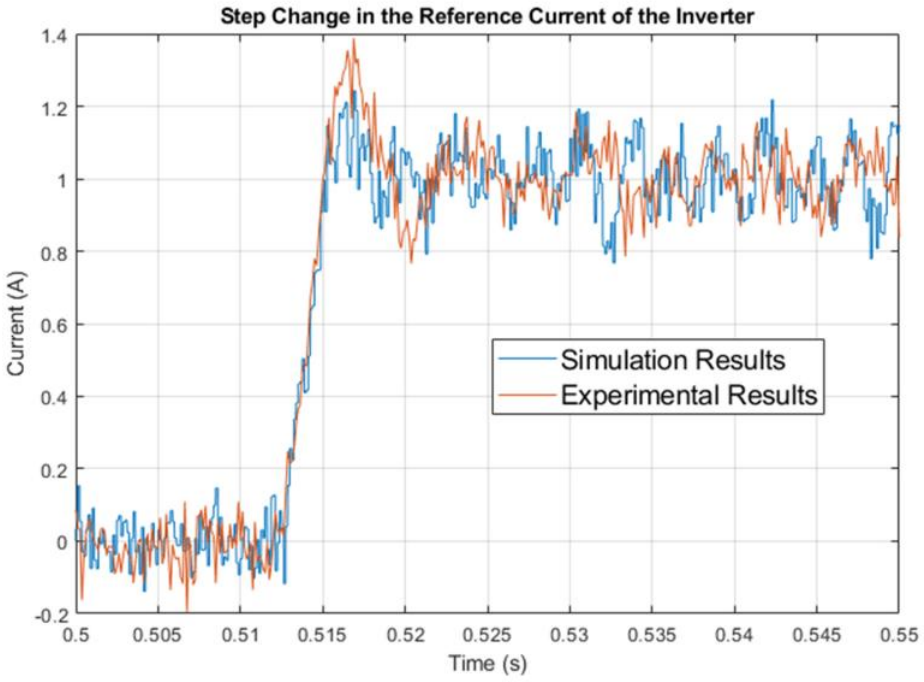
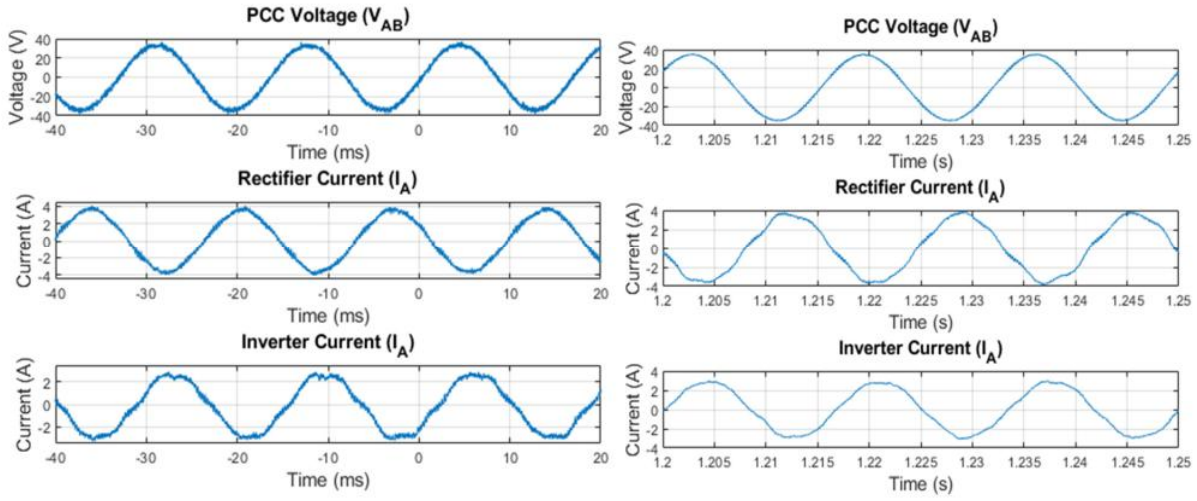


Fig. 6.3: Step change in reference current of the inverter.

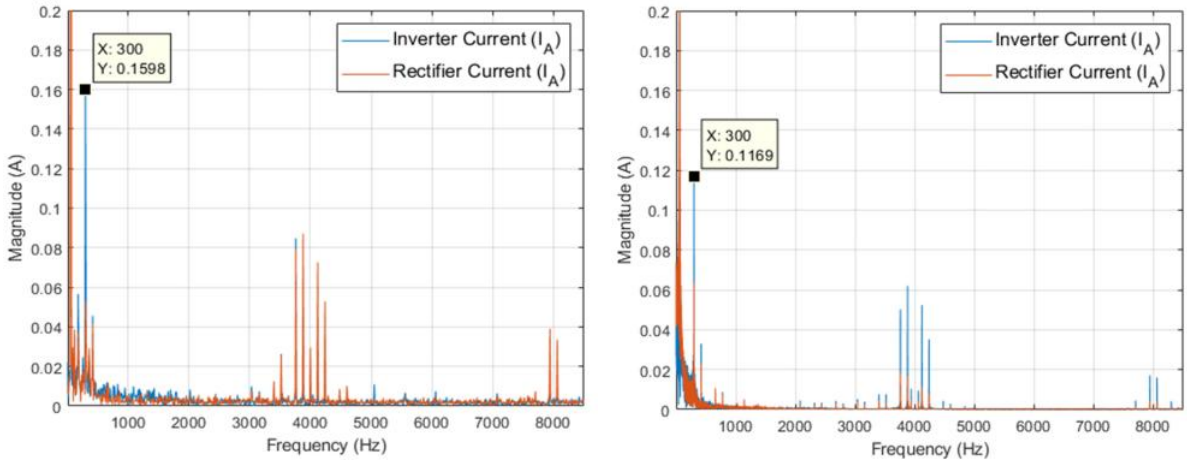
6.2.2 Steady-State Response of a Single Regen Bench

The steady-state waveforms of a single regen bench are illustrated in Fig. 6.4. In this case, the inverter is given a reference peak current of 3 A and the rectifier is given a DC bus reference voltage of 42 V. The peak current of the inverter waveform is not 3 A (around 2.84 A) because the reference is given to the inverter-side current while the one being displayed in the figure is the grid-side current. As such, since there are some losses associated with the equivalent series resistance (ESR) of the LC filter, it will not be exactly the same as the reference value. From the figure, the rectifier is providing near 111.2 W to compensate not only for the power injected by the inverter (around 86.9 W) but also for the losses in the system. The latter includes the losses due to the two transformers (around 10 W), the bleeding resistors (around 3.52 W) and other passive components. Thus, the power is being recirculated in the regen bench and the variac only provides the power to cover for the losses in the system. The simulation results presented in Fig. 6.4(b) show good agreement with the experimental results, with both results having similar peak currents values.



(a) (b)

Fig. 6.4: Steady-state waveforms of a single regen bench: (a) experimental results, and (b) simulations results.



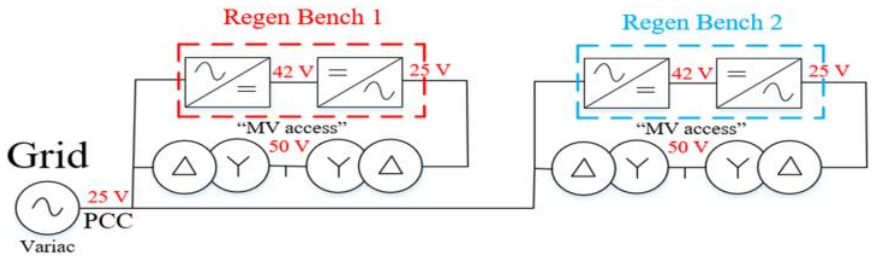
(a) (b)

Fig. 6.5: FFT of the rectifier and inverter currents: (a) experimental results, and (b) simulations results.

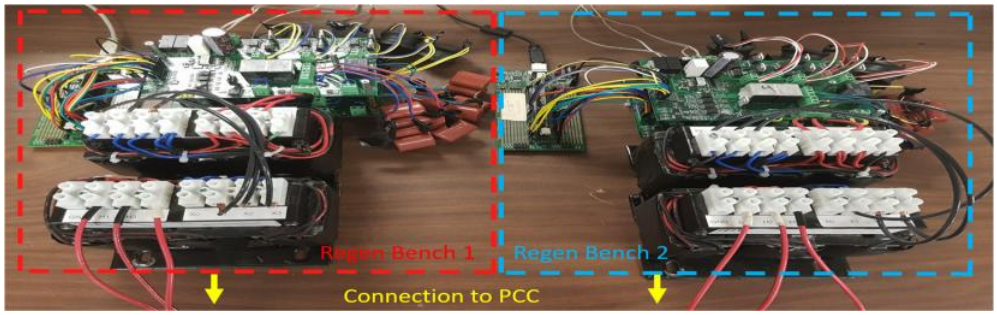
The fast Fourier transform (FFT) of the current waveforms of the inverter and rectifier are presented in Fig. 6.5. At low frequencies, the main issue is the presence of a 5th harmonic, which is in both the simulation and experimental results. The main reasons for this harmonic are the distorted magnetizing current drawn by the transformers, the deadtime added to the switching transitions, and the voltage drops in the semiconductors [3]-[5]. There are some references that propose different control algorithms to compensate these low-frequency harmonics, but they are out of the scope of this thesis [4], [5]. At higher frequencies, the main harmonics are around 4 kHz and 8 kHz, which is expected due to the switching frequency of the converters (i.e., 4 kHz). In this case, there are no significant harmonics after 8 kHz since the filter of the converters is proving enough attenuation at higher frequencies.

6.3 Testing of Two Parallel Scaled-Down Regen Benches

The next step is to test the operation of two parallel scaled-down regen benches connected to the grid. The experimental setup in this case is similar to the one used with a single regen bench and is illustrated in Fig. 6.6. This setup is the same as the one implemented in



(a)

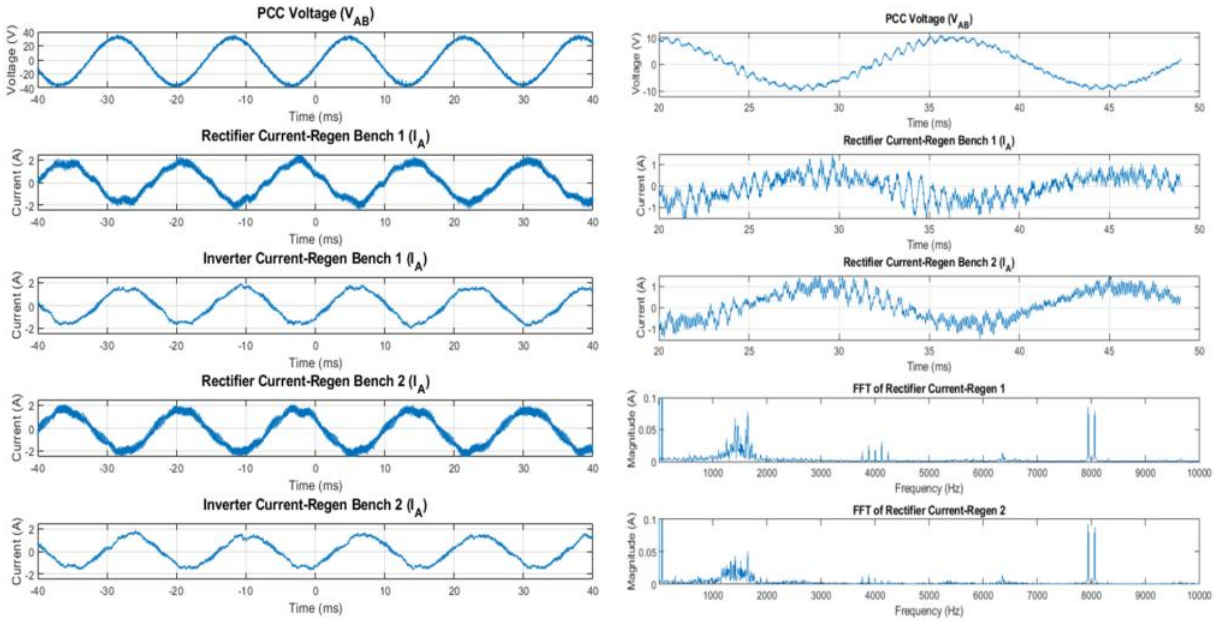


(b)

Fig. 6.6: (a) One-line diagram, and (b) photograph of two scaled-down regen benches.

the high-power testbed at NCREPT, which had instabilities issues. In the section, only the steady-state response of the system will be analyzed to verify that the system is in a stable region of operation.

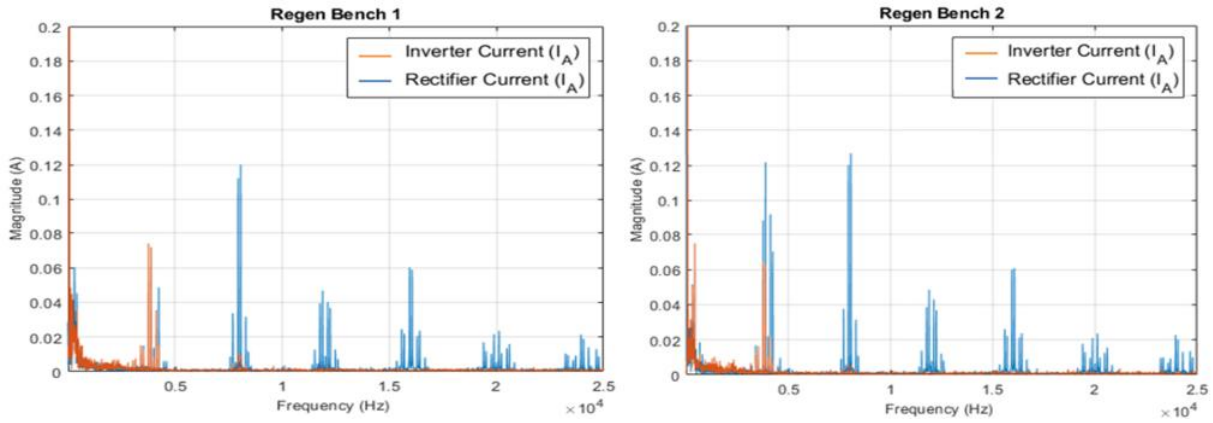
The experimental waveforms under steady-state condition of the two parallel regen benches are illustrated in Fig. 6.7(a). In this case, both inverters are given a reference peak current of 1.75 A and the rectifiers are given a DC bus reference voltage of 42 V. From the figure, there are no resonance issues due to interactions among the converter output filters as described in [6]-[8]. This is due to the use of the active damping algorithm from Chapter 2 and a proper selection of the PI controller parameters. Conversely, Fig. 6.7(b) shows that when no active damping algorithm is implemented, there is a severe distortion in the current and voltage waveforms due to a resonance around 1.5 kHz, which can be seen in the FFT of the rectifier currents.



(a) (b)

Fig. 6.7: Experimental waveforms in steady state of two regen benches (a) with and (b) without the active damping algorithm.

However, the currents of the inverters look similar to the case with a single grid-connected regen bench, but the ones for the rectifiers appear to have a higher content of high-frequency harmonics. This can be observed in the FFT of the signals in Fig. 6.8, where the rectifier currents have significant switching harmonics up to 25 kHz. In the case of the inverter, however, the switching harmonics are considerably attenuated after 8 kHz. The main reason for this behavior is that since the two transformers of the regen bench are in series with the output of the inverter, their leakage inductances are lumped with the inverter's LC filter to form an LCL filter, which has better damping capabilities at high frequencies [1]. Nevertheless, this is not the case for the rectifier, which only has an LC filter at its output. While this would the higher switching harmonic content in the rectifier than in the inverter, it does not explain why this issue was not obversed when a single regen bench was operating. To properly understand this issue, the frequency response of the rectifier operating with a single and two parallel regen benches is examined.



(a) (b)

Fig. 6.8: FFT of the rectifier and inverter currents for (a) regen bench 1, and (b) regen bench 2.

Assuming that the DC link capacitor is large enough to decouple the dynamics of the inverter and rectifier, a regen bench can be modeled as shown in Fig. 6.9, where Z_1 is the impedance of the inverter-side inductance, Z_2 is the impedance due to the leakage inductance of the transformers, Z_3 is the filter capacitive impedance, Z_g is the grid impedance, and the second subscript refers to the converter number. From the figure, it becomes clear that the inverter has an LCL filter while the rectifier only has an LC filter. Then, the principle of superposition can be used to remove the influence of all voltage sources except for the rectifier, which is illustrated in the auxiliary circuit illustrated in Fig. 6.10.

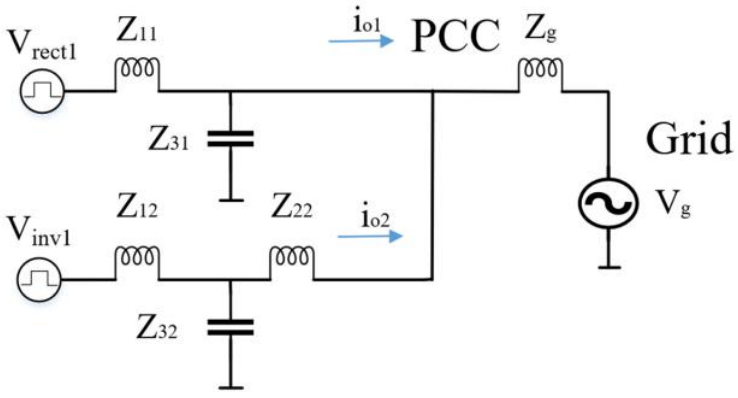


Fig. 6.9: Schematic of a grid-connected regen bench.

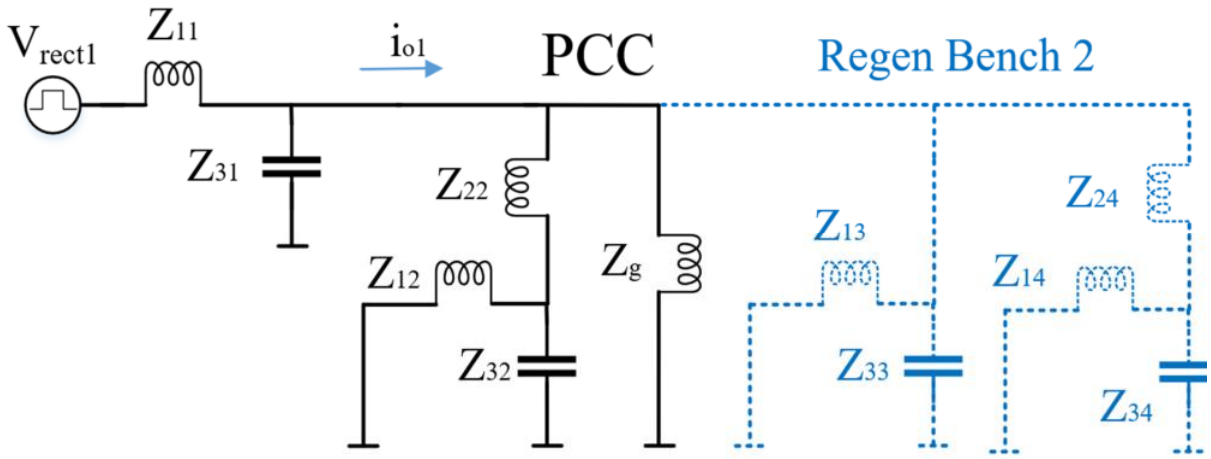


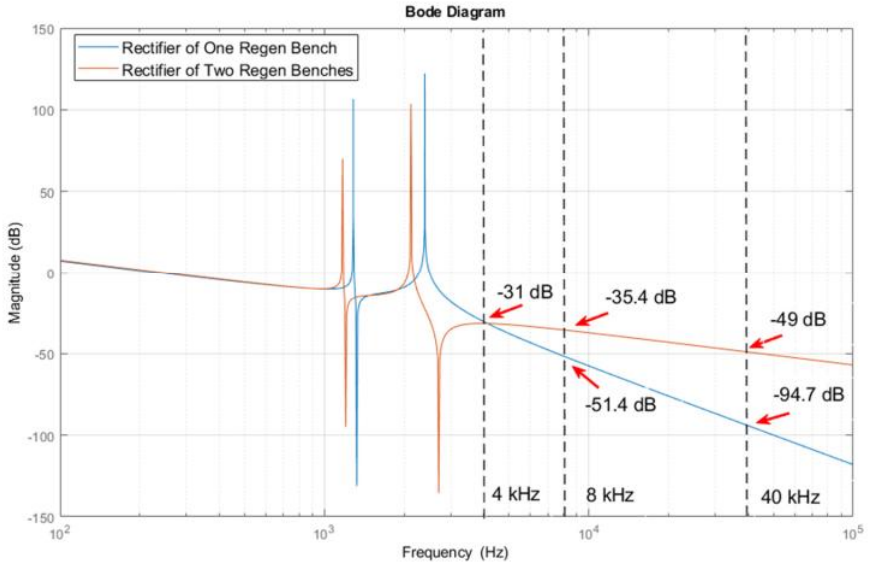
Fig. 6.10: Auxiliary circuit used to derive the transfer function of the rectifier.

Using this figure, the transfer function of the rectifier grid-side current i_{o1} (i.e., the one shown in Fig. 6.7) with respect to its own voltage can be derived for the case of a single and two parallel regen benches. Since these derivations lead to high-order transfer functions, they will not be presented here. However, the MATLAB™ script used to derive them is given in the Appendix B.1.

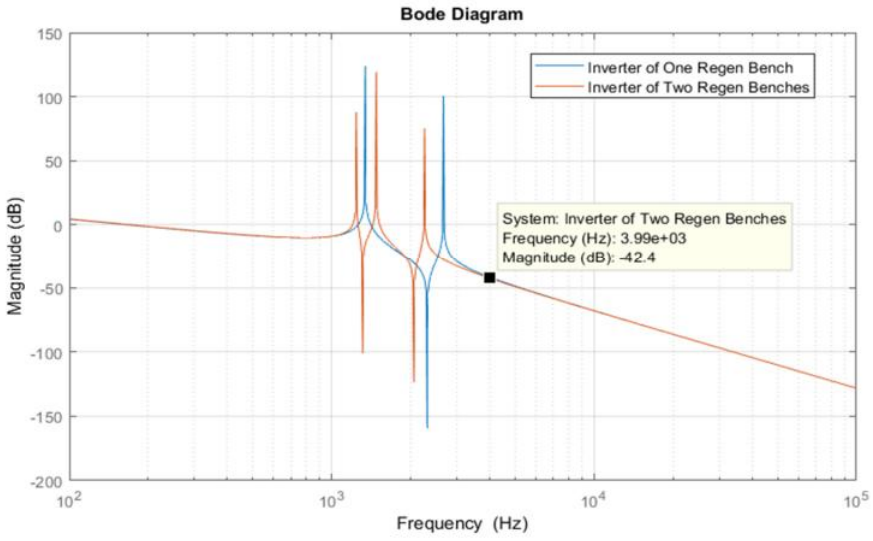
Fig. 6.11(a) shows the frequency responses of the rectifier when a single and two parallel regen benches are operating. Although both cases show similar attenuation of harmonics at 4 kHz (about -31 dB), the rectifier response with two regen benches shows much worse harmonic attenuation at higher frequencies. In fact, the damping capability of the rectifier filter is decreased from about -63.3 dB/decade to around -18 dB/decade. As a result of this improper attenuation, a higher content of high-frequency switching harmonics will be present in the grid current, as illustrated in Fig. 6.8.

This analysis can also be applied to the inverter to obtain its frequency response, which is illustrated in Fig. 6.11(b). Because the inverter has an LCL filter instead of an LC filter, it has a better attenuation of harmonics at the switching frequency (around -42.4 dB) and its damping

capability remains the same at higher frequencies, regardless of how many regen benches are operating in the system. Therefore, an LCL filter must be used at the output of the rectifier in order to improve its frequency response when multiple regen benches are operating in parallel.



(a)



(b)

Fig. 6.11: Frequency response of (a) a rectifier and (b) an inverter with a single and two parallel regen benches, respectively.

6.4 Conclusions

The experimental results of the scaled-down prototype with a single and two parallel- and grid-connected regen benches were presented in this chapter. Due to the proper design of the prototype controllers and the use of an active damping algorithm, there were no stability issues due to the interactions among the converter output filters. However, there was a significant degradation of the damping capability of the rectifier filter when multiple regen benches were connected in parallel to the grid. This makes it unable to properly attenuate high- frequency switching harmonics and causes distortion in the current extracted from the grid. Thus, an LCL filter must be used at the output of the rectifiers to properly attenuate those switching harmonics.

6.5 References

[1] Y. Liu, C. Farnell, J. C. Balda and H. A. Mantooth, "A 13.8-kV 4.75-MVA microgrid laboratory test bed," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 697-702.

[2] Escala, Edgar, "Developing Primary and Tertiary Controllers for Microgrids Using HIL Tools" (unpublished). MSEE Thesis, University of Arkansas.

[3] Du, Yang & Lu, Dylan & James, Geoffrey & Cornforth, David. (2013). "Modeling and analysis of current harmonic distortion from grid connected PV inverters under different operating conditions". *Solar Energy*. 94. 182-194. 10.1016/j.solener.2013.05.010.

[4] G. Shen, X. Zhu, M. Chen and D. Xu, "A New Current Feedback PR Control Strategy for Grid-Connected VSI with an LCL Filter," *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, 2009, pp. 1564-1569.

[5] S. Han, T. Jo, J. Park, H. Kim, T. Chun and E. Nho, "Dead time compensation for grid-connected PWM inverter," *8th International Conference on Power Electronics - ECCE Asia*, Jeju, 2011, pp. 876-881.

[6] S. G. Parker, B. P. McGrath and D. G. Holmes, "Regions of Active Damping Control for LCL Filters," in *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 424-432, Jan.-Feb. 2014.

[7] M. Lu, X. Wang, P. C. Loh and F. Blaabjerg, "Resonance Interaction of Multiparallel Grid-Connected Inverters with LCL Filter," in *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 894-899, Feb. 2017.

[8] J. L. Agorreta, M. Borrega, J. López and L. Marroyo, "Modeling and Control of N - Paralleled Grid-Connected Inverters With LCL Filter Coupled Due to Grid Impedance in PV Plants," in *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 770-785, March 2011.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

7.1 Conclusions

As explained in Chapter 1, the concept of microgrids offers innovative solutions to the issues affecting the current electrical infrastructure through the integration of distributed energy resources (DERs) [1], [2]. However, it also brings some challenges, especially in ensuring the proper control and stability of the multiple power electronic converters that are used to interface those DERs to the microgrid [3], [4]. These challenges are worsened in high-power microgrids due to the interactions among the converter output filters, which might lead to stability issues as those seen in the high-power microgrid testbed at the National Center for Reliable Electric Power Transmission (NCREPT) at the University of Arkansas [5], [6].

The modeling and stability analysis of a high-power microgrid with multiple parallel- and grid-connected converters using the system parameters from the microgrid testbed at NCREPT was presented in Chapter 2. Moreover, the stability range of the microgrid under different conditions, including using active damping and different feedback control signals, was examined through the root locus technique. The analysis demonstrated that the high-power microgrid testbed at NCREPT was operating in an unstable region and as a result an active damping algorithm must be implemented to guarantee the stability of the microgrid. In addition, the analysis in Chapter 1 can be expanded to develop general guidelines to avoid resonance and stability issues when connecting power converters into a microgrid. As such, the following guideline was developed to show the process for adding one more converter to a microgrid:

- Obtain the LCL filter parameters of the new converter.

- Calculate the interactive and common resonance frequencies (f_{res}, f_{res_1}).
- Obtain the switching (f_{sw}) and sampling (f_s) frequencies.
- Determine which feedback control signal (i.e., inverter- or grid-side current) is being used and whether an active damping algorithm is being implemented.
- Refer to Fig. 2.8 to ensure system stability.
- Adjust the current controller gains if necessary.

Similarly, the model and analysis of the stability of a high-power microgrid with multiple parallel- and grid-connected converters with different LCL filter parameters was established in Chapter 3. Additionally, the chapter provided a method to simplify the stability analysis of multiple converters with different LCL filters that have some variations in their power ratings. The analysis presented in this chapter is critical in the case that a new DER is integrated into the microgrid testbed, or if a DER is tested in parallel with the regen benches.

The construction of the scaled-down prototype of the high-power microgrid at NCREPT was addressed in Chapter 4. The prototype was designed with the same per-unit value as the high-power regen benches to have a similar open loop-response between them. Thus, solutions to improve the system stability and advanced control algorithms could be tested first in the scaled-down prototype before deploying them in the high-power microgrid. Then, the process for implementing the controller of a grid-connected rectifier and inverter in a single DSP was presented in Chapter 5.

With the board designed and the controller implemented in the DSP, the experimental results from the scaled-down prototype were captured and analyzed in Chapter 6. No resonance or stability issues were found when operating a single or two parallel scaled-down regen benches due to the proper design of the controllers and the use of the active damping algorithm from

Chapter 2. Nevertheless, the damping capability of the rectifier filter was found to decrease when multiple regen benches were operating in parallel, which prevents the attenuation of high-frequency switching harmonics in the grid-side current. This issue was not found in the inverter, however, because of the equivalent LCL filter that forms when the leakage inductances of the transformers lump with the inverter LC filter. Consequently, an LCL filter should be used at the output of the rectifiers to increase the power quality of its grid-side current.

7.2 Recommendations for Future Work

The recommendations for potential future work are presented as follows:

- A proportional-resonant (PR) controller in the stationary frame and a dead-time compensation method could be implemented in the scaled-down prototype to compensate for the low-frequency harmonics found in the experimental results [7], [8].
- The code for emulating interfaces based on power electronics for wind generators and central solar inverters could be developed and implemented [9], [10].
- A hierarchical control scheme for microgrids which include the primary, secondary and tertiary controllers could be studied and implemented [3], [11].
- The islanded mode of operation of the high-power microgrid testbed at NCREPT could be further studied and implemented in the scaled-down prototype [5], [12]. This includes developing and testing the control algorithms for the variable-voltage variable-frequency (3VF) converter and ensuring the stable operation between the 3VF and the multiple regen benches.

- A variac was used to slowly ramp up the voltage at the point of common coupling. However, this is not available in the high-power microgrid at NCREPT. Thus, a start-up algorithm should be developed to connect the regen benches to the grid to avoid high inrush currents.
- The control algorithms developed in the scaled-down prototype should be implemented and tested in the high-power microgrid.

7.3 References

[1] H. Farhangi, "The path of the smart grid," in *IEEE Power and Energy Magazine*, vol. 8, no. 1, pp. 18-28, January-February 2010.

[2] N. Hatziargyriou, H. Asano, R. Iravani and C. Marnay, "Microgrids," in *IEEE Power and Energy Magazine*, vol. 5, no. 4, pp. 78-94, July-Aug. 2007.

[3] L. Meng, M. Savaghebi, F. Andrade, J. C. Vasquez, J. M. Guerrero and M. Graells, "Microgrid central controller development and hierarchical control implementation in the intelligent microgrid lab of Aalborg University," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 2585-2592.

[4] M. Lu, X. Wang, P. C. Loh and F. Blaabjerg, "Resonance Interaction of Multiparallel Grid-Connected Inverters With LCL Filter," in *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 894-899, Feb. 2017.

[5] Y. Liu, C. Farnell, J. C. Balda and H. A. Mantooth, "A 13.8-kV 4.75-MVA microgrid laboratory test bed," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 697-702.

[6] Y. Liu, C. Farnell, H. A. Mantooth, J. C. Balda, R. A. McCann and C. Deng, "Resonance propagation modeling and analysis of AC filters in a large-scale microgrid," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 143-149.

[7] G. Shen, X. Zhu, M. Chen and D. Xu, "A New Current Feedback PR Control Strategy for Grid-Connected VSI with an LCL Filter," *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, 2009, pp. 1564-1569.

[8] S. Han, T. Jo, J. Park, H. Kim, T. Chun and E. Nho, "Dead time compensation for grid-connected PWM inverter," *8th International Conference on Power Electronics - ECCE Asia*, Jeju, 2011, pp. 876-881.

[9] Y. Ma, L. Yang, J. Wang, F. Wang and L. M. Tolbert, "Emulating full-converter wind

turbine by a single converter in a multiple converter based emulation system," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 3042-3047.

[10] J. Wang *et al*., "Regenerative power converters representation of grid control and actuation emulator," *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, Raleigh, NC, 2012, pp. 2460-2465.

[11] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. de Vicuna and M. Castilla, "Hierarchical Control of Droop-Controlled AC and DC Microgrids—A General Approach Toward Standardization," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 1, pp. 158-172, Jan. 2011.

[12] Y. Liu, C. Farnell, K. George, H. A. Mantooth and J. C. Balda, "A scaled-down microgrid laboratory testbed," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 1184-1189.

APPENDIX A

DIGITAL SIGNAL PROCESSOR CODE

The C code uploaded to the DSP to implement the control algorithms in Chapter 5 is presented below.

A.1 The Main.c File

```
#include "DSP28x_Project.h"     // Device Headerfile and
Examples Include File


extern struct ADC_RESULTS ADC_inv,ADC_rect; // This is where the
results from the adc will be stored (Currents, Voltages)
extern struct CMP_OUT PWM_inv,PWM_rect; // Output of the Current
Controller
extern Uint16 MODE;// Mode of Operation, it is set to always
start at mode 1: MODE 1 ALL switches OFF, MODE 2 Current
Controller , MOde 3 Open Loop

// ADC Scaling values - Use to converter outputs of the adc to
actual value of voltage and currents
float DSP_ADC_Scale = (7.326E-4);// 3V/4095 or (3/2^12
resolution of ti dsp)
float Volt_Scale= (32.6456); // (31.6e3/(1e6+31.6e3))^-1 values
of resistor can be picked voltage divider
float R_Div_Scale2=  (1.6667);      // (15e3/(10e3+15e3))^-1
float   Current_Scale = (5.4054);  //Scaling factor for Current
Sensor (185mV/A)^-1
float temp; //Variable for temporarily storing adc results

//USE FOR DEBUGGING
#define DEBUG_MAIN 0 // Set to 1 to enable, 0 to disable
#if (DEBUG_MAIN)
int ConversionCount=0;
float Voltage1[400];
#endif

float EPwm_TBPRD = (TBCLK/PWMCARRIER); //Counter of the EPWM
Register, TBCLK and PWMCARRIER are defined in parameters.h

// Define the interrupts routine
```

```
//In this case an interrupt is triggered when the ADC has all
the results,
//The interrupts is triggered twice, one at the beginning and
middle of the switching period.
interrupt void adc_isr(void);
extern int Inverter_Start; // Define if the inverter starts or
not

void main(void)
{

// Step 1. Initialize System Control:
// PLL, WatchDog, enable Peripheral Clocks
// This function is found in the DSP2833x_SysCtrl.c file.
   InitSysCtrl();

   // ADC CLOCK
   EALLOW;
   #if (CPU_FRQ_150MHZ)     // Default - 150 MHz SYSCLKOUT
     #define ADC_MODCLK 0x3 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2
= 150/(2*3)   = 25.0 MHz
   #endif
   #if (CPU_FRQ_100MHZ)
     #define ADC_MODCLK 0x2 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2
= 100/(2*2)   = 25.0 MHz
   #endif
   EDIS;

   // Define ADCCLK clock frequency ( less than or equal to 25
MHz )
   // Assuming InitSysCtrl() has set SYSCLKOUT to 150 MHz
   EALLOW;
   SysCtrlRegs.HISPCP.all = ADC_MODCLK;
   EDIS;

// Step 2. Initalize GPIO:
// This function is found in the DSP2833x_Gpio.c file. Configura
las entradas
// salidas y los pullups para usar con el inverter. Includes the
configuration
// as PWM, SCI, etc.
   InitGpio();

// Step 3. Clear all interrupts and initialize PIE vector table:
// Disable CPU interrupts
   DINT;
```

```
// Initialize the PIE control registers to their default state.
// The default state is all PIE interrupts disabled and flags
// are cleared.
// This function is found in the DSP2833x_PieCtrl.c file.
   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell
Interrupt
// Service Routines (ISR).
// This will populate the entire table.  This is useful for
debug purposes.
// The shell ISR routines are found in DSP2833x_DefaultIsr.c.
// This function is found in DSP2833x_PieVect.c.
   InitPieVectTable();

// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.
   EALLOW;  // This is needed to write to EALLOW protected
register
   PieVectTable.ADCINT = &adc_isr;
   EDIS;    // This is needed to disable write to EALLOW
protected registers

// Step 4. Initialize the Device Peripherals.
// ADC
   InitAdc();           //in DSP2833x_Adc.c
// ePWM1, ePWM2, ePWM3
   InitEPwm();          // in DSP2833x_EPwm.c


// To ensure precise timing, use write-only instructions to
write to the entire register. Therefore, if any
// of the configuration bits are changed in ConfigCpuTimer and
InitCpuTimers (in DSP2833x_CpuTimers.h), the
// below settings must also be updated.
// This starts the clocks of the PWMs and timerCPU for the
interrupt every Ts
   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;   // Enable TBCLK
within the ePWM
   EDIS;
```

```
// Enable CPU int1 which is connected to CPU-Timer 0
    IER |= M_INT1; // Enable CPU Interrupt 1

   // Enable ADCINT in PIE
   PieCtrlRegs.PIEIER1.bit.INTx6 = 1;

// Enable global Interrupts and higher priority real-time debug
events:
   EINT;          // Enable Global interrupt INTM
   ERTM;          // Enable Global realtime interrupt DBGM

   //FOR DAVID'S BOARD ONLY-SOFT START- RELAYS
    GpioCtrlRegs.GPAMUX2.bit.GPIO30 = 0;    //
    GpioCtrlRegs.GPAPUD.bit.GPIO30 = 0; // enable pull-up
    GpioCtrlRegs.GPADIR.bit.GPIO30 = 1; // output
    GpioDataRegs.GPACLEAR.bit.GPIO30 = 1;

    GpioCtrlRegs.GPAMUX2.bit.GPIO31 = 0;    //
    GpioCtrlRegs.GPAPUD.bit.GPIO31 = 0; // enable pull-up
    GpioCtrlRegs.GPADIR.bit.GPIO31 = 1; // output
    GpioDataRegs.GPACLEAR.bit.GPIO31 = 1;

// Step 6. IDLE loop. Just sit and loop forever
   //Main loop will idle forever but the current controller will
be executed everytime there is an adc interrupt
   for(;;)
     {
       // MIGHT BE A GOOD IDEA TO INCLUDE SOME PROTECTION SCHEME
       // FOR EXAMPLE EPWM TRIPZONE
       asm("          NOP");

     }

}

interrupt void  adc_isr(void)
{

    //DSP ADC-Channel A- INVERTER
    //ADCA0-IA
    temp = 0;
    temp = AdcRegs.ADCRESULT0 >> 4; // ADCINA0
    ADC_inv.IA= (3.0f/scale_IA_inv)*((float)temp-offset_IA_inv);
//Manually Calibrated- This changes for each board- WIll be
different for chris board
    //ADCA1-IB
    temp = 0;
```

```
    temp = AdcRegs.ADCRESULT1 >> 4; // ADCINA0
    ADC_inv.IB=(3.0f/scale_IB_inv)*((float)temp-offset_IB_inv);
//Manually Calibrated- This changes for each board- WIll be
different for chris board
    //ADCA2-IC
    temp = 0;
    temp = AdcRegs.ADCRESULT2 >> 4; // ADCINA0
    //ADC_inv.IC= 3.0f/432.0f*((float)temp-2060.0f);
    ADC_inv.IC=(3.0f/scale_IC_inv)*((float)temp-offset_IC_inv);
//Manually Calibrated- This changes for each board- WIll be
different for chris board
    //ADCA4-Vdc
    temp = 0;
    temp = AdcRegs.ADCRESULT3 >> 4; // ADCINA0
    ADC_inv.Vdc= temp*DSP_ADC_Scale*Volt_Scale;
    //ADCA5 VA
    temp = 0;
    temp = AdcRegs.ADCRESULT4 >> 4; // ADCINA0
    ADC_inv.VA=  temp*DSP_ADC_Scale*Volt_Scale;
    //ADCA6 VB
    temp = 0;
    temp = AdcRegs.ADCRESULT5 >> 4; // ADCINA0
    ADC_inv.VB= temp*DSP_ADC_Scale*Volt_Scale;
    //ADCA7 VC
    temp = 0;
    temp = AdcRegs.ADCRESULT6 >> 4; // ADCINA0
    ADC_inv.VC= temp*DSP_ADC_Scale*Volt_Scale;

    //DSP ADC-Channel B- RECTIFIER
    //ADCB0 IA
    temp = 0;
    temp = AdcRegs.ADCRESULT7 >> 4; // ADCINA0
    ADC_rect.IA=(3.0f/scale_IA_rect)*((float)temp-
offset_IA_rect); //Manually Calibrated- This changes for each
board- WIll be different for chris board
    //ADCB1 IB
    temp = 0;
    temp = AdcRegs.ADCRESULT8 >> 4; // ADCINA0
    ADC_rect.IB =(3.0f/scale_IB_rect)*((float)temp-
offset_IB_rect); //Manually Calibrated- This changes for each
board- WIll be different for chris board
    //ADCB2 IC
    temp = 0;
    temp = AdcRegs.ADCRESULT9 >> 4; // ADCINA0
    ADC_rect.IC= (3.0f/scale_IC_rect)*((float)temp-
offset_IC_rect); //Manually Calibrated- This changes for each
board- WIll be different for chris board
```

```
    //ADCB4 Vdc
    temp = 0;
    temp = AdcRegs.ADCRESULT10 >> 4; // ADCINA0
    ADC_rect.Vdc= temp*DSP_ADC_Scale*Volt_Scale;
    //ADCB5 VA
    temp = 0;
    temp = AdcRegs.ADCRESULT11 >> 4; // ADCINA0
    ADC_rect.VA=  temp*DSP_ADC_Scale*Volt_Scale;
    //ADCB6 VB
    temp = 0;
    temp = AdcRegs.ADCRESULT12 >> 4; // ADCINA0
    ADC_rect.VB= temp*DSP_ADC_Scale*Volt_Scale;
    //ADCB7 VC
    temp = 0;
    temp = AdcRegs.ADCRESULT13 >> 4; // ADCINA0
    ADC_rect.VC= temp*DSP_ADC_Scale*Volt_Scale;

    //DEBUG
    //USE to store the values of signals from the adc to view
them in the grapher
    //One would use this in case, one needs to be sure that the
sensors or configuration above is correct
    #if (DEBUG_MAIN)
    Voltage1[ConversionCount]= ADC_rect.IC;
    #endif


    ////////////////////////////MODE OF OPERATION
/////////////////////////////////
        //MODE 1 ALL switches OFF
        //MODE 2 Current Controller
        //MODE 3 Open Loop TEST
    //Register of EPWM1,EPWM2, and EPWM3 refers to the inverter
    //Register of EPWM4,EPWM5, and EPWM6 refers to the rectifier

    if (MODE == 1)
        {
        //NOTE: MIGHT NEED TO CHANGE THIS LATER
        //another way of doing this is to disable the output of
the EPWMs in MODE 1. Then, feedforward the voltage to get dfinal
and qfinal
        //and update the registers of the EPWM. THEN, in MODE 2,
the outputs are enabled.
        //The reason for doing this is to avoid having high
inrush current at the beggining, when changing from MODE 1 to
MODE 2.
```

```
        //Adjusting the Complementary Switches to be OFF-
Otherwise one switch would be OFF and the OTHER ON
            //For Inverter
            EPwm1Regs.DBCTL.bit.POLSEL = 0;
            EPwm2Regs.DBCTL.bit.POLSEL = 0;
            EPwm3Regs.DBCTL.bit.POLSEL = 0;
            EPwm1Regs.AQCTLB.bit.CAU = AQ_SET;
            EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;
            EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;
            EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;
            EPwm3Regs.AQCTLB.bit.CAU = AQ_SET;
            EPwm3Regs.AQCTLB.bit.CAD = AQ_CLEAR;

            //For Inverter Rectifier
            EPwm4Regs.DBCTL.bit.POLSEL = 0;
            EPwm5Regs.DBCTL.bit.POLSEL = 0;
            EPwm6Regs.DBCTL.bit.POLSEL = 0;
            EPwm4Regs.AQCTLB.bit.CAU = AQ_SET;
            EPwm4Regs.AQCTLB.bit.CAD = AQ_CLEAR;
            EPwm5Regs.AQCTLB.bit.CAU = AQ_SET;
            EPwm5Regs.AQCTLB.bit.CAD = AQ_CLEAR;
            EPwm6Regs.AQCTLB.bit.CAU = AQ_SET;
            EPwm6Regs.AQCTLB.bit.CAD = AQ_CLEAR;
        }

    if (MODE == 2)
    {
        //Set PWM Register to complementary mode
        //If Inverter start=1, then set to complementary,
otherwise inverters stays in mode 1 and does not switch
        if(Inverter_Start==1)
        {
        EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
        EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
        EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
        }
        else
        {
        EPwm1Regs.DBCTL.bit.POLSEL = 0;
        EPwm2Regs.DBCTL.bit.POLSEL = 0;
        EPwm3Regs.DBCTL.bit.POLSEL = 0;
        EPwm1Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm3Regs.AQCTLB.bit.CAD = AQ_CLEAR;
```

```
        }
        //Set Rectifier to Complementary Mode
        EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
        EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
        EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
    }

    if (MODE == 3)
    {
        //Set PWM Register to complementary mode
        //This part is the same as Mode 2 above
        if(Inverter_Start==1)
        {
        EPwm1Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
        EPwm2Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
        EPwm3Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
        }
        else
        {
        EPwm1Regs.DBCTL.bit.POLSEL = 0;
        EPwm2Regs.DBCTL.bit.POLSEL = 0;
        EPwm3Regs.DBCTL.bit.POLSEL = 0;
        EPwm1Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm1Regs.AQCTLB.bit.CAD = AQ_CLEAR;
        EPwm2Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm2Regs.AQCTLB.bit.CAD = AQ_CLEAR;
        EPwm3Regs.AQCTLB.bit.CAU = AQ_SET;
        EPwm3Regs.AQCTLB.bit.CAD = AQ_CLEAR;
        }
        //Set Rectifier to Complementary Mode
        EPwm4Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
        EPwm5Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
        EPwm6Regs.DBCTL.bit.POLSEL = DB_ACTV_HIC;
    }

   //Call current controller
    controller_STEP();

   //Debugging
   //This will reset the counter in the array where the values
are stored, otherwise the values will be stored once and not
anymore
    #if DEBUG_MAIN
   if(ConversionCount == 400)
              {
                 ConversionCount = 0;
              }
```

```
            else
            {
                ConversionCount++;
            }
    #endif

    // Update the counter of the EPWM REGISTER
    ////////////////////////INVERTER/////////////////////////
    // Adjust duty for output EPWM1A
    EPwm1Regs.CMPA.half.CMPA = PWM_inv.CMP1*EPwm_TBPRD;
    // Adjust duty for output EPWM2A
    EPwm2Regs.CMPA.half.CMPA = PWM_inv.CMP2*EPwm_TBPRD;
    // Adjust duty for output EPWM2A
    EPwm3Regs.CMPA.half.CMPA = PWM_inv.CMP3*EPwm_TBPRD;
    ////////////////////////Rectifier/////////////////////////
    // Adjust duty for output EPWM1A
    EPwm4Regs.CMPA.half.CMPA = PWM_rect.CMP1*EPwm_TBPRD;
    // Adjust duty for output EPWM2A
    EPwm5Regs.CMPA.half.CMPA = PWM_rect.CMP2*EPwm_TBPRD;
    // Adjust duty for output EPWM2A
    EPwm6Regs.CMPA.half.CMPA = PWM_rect.CMP3*EPwm_TBPRD;


    // Reinitialize for next ADC sequence
    AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;         // Reset SEQ1
    AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;       // Clear INT SEQ1
bit
    PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;   // Acknowledge
interrupt to PIE
}


//===========================================================
=============
// No more.
//===========================================================
=============
```

A.2 The Controller.c File

```
#include "IO_variables.h"
#include "parameters.h"

//-------------------------------------------------------------
-----------
//INTERFACE VARIABLES:

//-------------
//ANALOG INPUTS (in Amperes and Volts)
//-------------
//      There will be one for inverter and one for rectifier
//       ADC.Vdc; DC link Capacitor Voltage
//       ADC.VA; Capacitor Voltage VA-Negative Rail of Vdc
//       ADC.VB;Capacitor Voltage VB-Negative Rail of Vdc
//       ADC.VC;Capacitor Voltage VC-Negative Rail of Vdc
//       ADC.IA;Phase A Current
//       ADC.IB;Phase B Current
//       ADC.IC; Phase C Current
//-----------
//PWM OUTPUTS (normalized between 0 and 1)
//-----------
//PWM.CMP1
//PWM.CMP2
//PWM.CMP3
//-------------------------------------------------------------
-----------

//----------------
//Global variables
//----------------
struct ADC_RESULTS ADC_inv,ADC_rect;
struct CMP_OUT PWM_inv,PWM_rect;

// DEBUG
#define DEBUG_Controller 0
#define OPEN_LOOP_RECTIFIER 0
#define INVERTER_TEST 0



//Global Variables
float S1_inv= 0;
float S2_inv= 0;
float S3_inv= 0;
float S1_rect= 0;
```

```
float S2_rect= 0;
float S3_rect= 0;

float radian= 0; //radians for MODE 3-Open Loop
float dfinal=0; float qfinal=0;
Uint16 MODE=1;// MODE 1 ALL switches OFF, MODE 2 Current
Controller , MOde 3 Open Loop
float dfinal2,qfinal2,vdcovertwo;
float temp1,temp2;
float Idref1_inv=0; float Iqref1_inv=0; float Idref1_rect=0;
float Iqref1_rect=0;
float VAB_inv=0;float VBC_inv=0; float VCA_inv=0;float
VAN_inv=0;float VBN_inv=0; float VCN_inv=0;
float VAB_rect=0;float VBC_rect=0; float VCA_rect=0;float
VAN_rect=0;float VBN_rect=0; float VCN_rect=0;
int Inverter_Start =0;

float Ts =2*pi/(PWMCARRIER/SINEFREQ);
//Reference LEVEL- REferences steps defined in parameters.h
float Vdcref= 25;
float VdcrefMax = 35;
float Idrefmax=0;
int Initialize = 1; // Initializes the Functions only once.
Prevents functions for being constantly initialized
float GainC=0.3355; //GainC= we*(LL+Lg);

//Define and Initialize
//PI FUNCTIONS for current and voltage controller
PI_controller Voltage_Controller_Vdc, Current_Controller_D_inv,
Current_Controller_Q_inv,
Current_Controller_D_rect, Current_Controller_Q_rect;

//SOGI Filter to Smooth voltage signals. Eliminated offset and
reduces noise
SPLL_1ph_SOGI_F PARKS_Va_inv, PARKS_Vb_inv, PARKS_Vc_inv;
SPLL_1ph_SOGI_F PARKS_Va_rect, PARKS_Vb_rect, PARKS_Vc_rect;
SPLL_1ph_SOGI_F PARKS_Ia_rect, PARKS_Ib_rect, PARKS_Ic_rect;

//3 Phase-PLL Function
SPLL_3ph_SRF_F spll1;

//ABC to DQ Function
ABC_DQ0_POS_F abc_dq0_voltage1_rect,abc_dq0_voltage1_inv;
ABC_DQ0_POS_F abc_dq0_current1_rect,abc_dq0_current1_inv;

//SPACE VECTOR MODULATION FUNCTION
SVGENDQ svgen_dq1_inv,svgen_dq1_rect;
```

```
//DQ to ALPHA BETA FUNCTION
iPARK_F modulation1_inv,modulation1_rect;

//DIGITAL LOW PASS Filter
//LOW_PASS IA_LOWPASS,IB_LOWPASS,IC_LOWPASS; // Not BEING USED
IN THIS PROJECT

//DEBUGGGING
#if (DEBUG_Controller)
//float debug[10];
//float record=0;
//int   counter1=0;
float Voltage1[400];
float Voltage2[400];
float Voltage3[400];
int ConversionCount=0;
//int jump=0;
#endif

////////////////////////////Interrupt//////////////////////////
////////
/////////////////////////////////////////////////////////////
////////

//This function is run every Ts
void controller_STEP(){

// Initializes the Functions only once. Prevents functions for
being constantly initialized
if(Initialize == 1)
{
    ////////////////////////PI Controller//////////////////
    ////////////////////////INVERTER//////////////////////////
    // PI Configuration Current- DQ
        Current_Controller_D_inv.TS =(1/PWMCARRIER) ; //
        Current_Controller_D_inv.KI =Ki_inv ; //
        Current_Controller_D_inv.KP = Kp_inv;
        PI_controller_init(&Current_Controller_D_inv);

        Current_Controller_Q_inv.TS =(1/PWMCARRIER) ; //
        Current_Controller_Q_inv.KI =Ki_inv ; //
        Current_Controller_Q_inv.KP = Kp_inv;
        PI_controller_init(&Current_Controller_Q_inv);

    ////////////////////////Rectifier//////////////////////////
```

```
                // PI Configuration Current- DQ
        Current_Controller_D_rect.TS =(1/PWMCARRIER) ; //
        Current_Controller_D_rect.KI =Ki_rect ; //
        Current_Controller_D_rect.KP = Kp_rect;
        PI_controller_init(&Current_Controller_D_rect);

        Current_Controller_Q_rect.TS =(1/PWMCARRIER) ; //
        Current_Controller_Q_rect.KI =Ki_rect ; //
        Current_Controller_Q_rect.KP = Kp_rect;
        PI_controller_init(&Current_Controller_Q_rect);

        // PI configuation Vdc
        Voltage_Controller_Vdc.TS =(1/PWMCARRIER) ; //
        Voltage_Controller_Vdc.KI =kivdc ; //
        Voltage_Controller_Vdc.KP = kpvdc;
        PI_controller_init(&Voltage_Controller_Vdc);


        ////////////////////////////SOGI
FILTER/////////////////////////////
        //Initialize

SPLL_1ph_SOGI_F_init(SINEFREQ,((float)(1.0/(PWMCARRIER))),&PARKS
_Va_inv);

SPLL_1ph_SOGI_F_coeff_update(((float)(1.0/(PWMCARRIER))),(float)
(2*pi*SINEFREQ),&PARKS_Va_inv);


SPLL_1ph_SOGI_F_init(SINEFREQ,((float)(1.0/(PWMCARRIER))),&PARKS
_Vb_inv);

SPLL_1ph_SOGI_F_coeff_update(((float)(1.0/(PWMCARRIER))),(float)
(2*pi*SINEFREQ),&PARKS_Vb_inv);


SPLL_1ph_SOGI_F_init(SINEFREQ,((float)(1.0/(PWMCARRIER))),&PARKS
_Vc_inv);

SPLL_1ph_SOGI_F_coeff_update(((float)(1.0/(PWMCARRIER))),(float)
(2*pi*SINEFREQ),&PARKS_Vc_inv);


SPLL_1ph_SOGI_F_init(SINEFREQ,((float)(1.0/(PWMCARRIER))),&PARKS
_Va_rect);
```

```
SPLL_1ph_SOGI_F_coeff_update(((float)(1.0/(PWMCARRIER))),(float)
(2*pi*SINEFREQ),&PARKS_Va_rect);


SPLL_1ph_SOGI_F_init(SINEFREQ,((float)(1.0/(PWMCARRIER))),&PARKS
_Vb_rect);

SPLL_1ph_SOGI_F_coeff_update(((float)(1.0/(PWMCARRIER))),(float)
(2*pi*SINEFREQ),&PARKS_Vb_rect);


SPLL_1ph_SOGI_F_init(SINEFREQ,((float)(1.0/(PWMCARRIER))),&PARKS
_Vc_rect);

SPLL_1ph_SOGI_F_coeff_update(((float)(1.0/(PWMCARRIER))),(float)
(2*pi*SINEFREQ),&PARKS_Vc_rect);

        //IGNORE DO NOT WANT TO USE THE SOGI ON CURRENTS
/*

SPLL_1ph_SOGI_F_init(SINEFREQ,((float)(1.0/(PWMCARRIER))),&PARKS
_Ia_rect);

SPLL_1ph_SOGI_F_coeff_update(((float)(1.0/(PWMCARRIER))),(float)
(2*pi*SINEFREQ),&PARKS_Ia_rect);


SPLL_1ph_SOGI_F_init(SINEFREQ,((float)(1.0/(PWMCARRIER))),&PARKS
_Ib_rect);

SPLL_1ph_SOGI_F_coeff_update(((float)(1.0/(PWMCARRIER))),(float)
(2*pi*SINEFREQ),&PARKS_Ib_rect);


SPLL_1ph_SOGI_F_init(SINEFREQ,((float)(1.0/(PWMCARRIER))),&PARKS
_Ic_rect);

SPLL_1ph_SOGI_F_coeff_update(((float)(1.0/(PWMCARRIER))),(float)
(2*pi*SINEFREQ),&PARKS_Ic_rect); */

        ////////////////////////////3 PHASE
SRPLL////////////////////////////
        //Initialize
        SPLL_3ph_SRF_F_init(SINEFREQ,((float)(1.0/PWMCARRIER)),
&spll1);
```

```
////////////////////////////////////////////////////////////

        //////////////////////////ABC to
DQ//////////////////////////
        //Define and Initialize
        ABC_DQ0_POS_F_init(&abc_dq0_voltage1_inv);
        ABC_DQ0_POS_F_init(&abc_dq0_current1_inv);
        ABC_DQ0_POS_F_init(&abc_dq0_voltage1_rect);
        ABC_DQ0_POS_F_init(&abc_dq0_current1_rect);
        ////////////////////////////DQ to ALPHA-
BETA//////////////////////////
        //Define and Initialize
        iPARK_F_init(&modulation1_inv);
        iPARK_F_init(&modulation1_rect);

        //////////////////////////Space Vector
Modulation//////////////////////////
        SVGENDQ_init(&svgen_dq1_inv);
        SVGENDQ_init(&svgen_dq1_rect);

        ////////////////////////////LOW
PASS////////////////////////////////
        //IGNORE
/*
        IA_LOWPASS.hh=(1/PWMCARRIER);
        IA_LOWPASS.Tf=1/(2*pi*500);
        LOW_PASS_init(&IA_LOWPASS);

        IB_LOWPASS.hh=(1/PWMCARRIER);
        IB_LOWPASS.Tf=1/(2*pi*500);
        LOW_PASS_init(&IB_LOWPASS);

        IC_LOWPASS.hh=(1/PWMCARRIER);
        IC_LOWPASS.Tf=1/(2*pi*500);
        LOW_PASS_init(&IC_LOWPASS);*/
}
    //PREVENTS FUNCTIONS TO BE INITIALIZE MANY TIMES
    Initialize=0;

    //VOLTGE IS MESAURED FROM LINE TO NEGATIVE RAIL OF THE DC
LINK BUS
    //NEEDS TO BE CONVERTED FIRST TO LINE TO LINE AND THEN TO
LINE TO NEUTRAL
    ////////////////////////INVERTER//////////////////////////
    //Calculating Line to Line Voltage
    VAB_inv = ADC_inv.VA-ADC_inv.VB;
```

```
    VBC_inv = ADC_inv.VB-ADC_inv.VC;
    VCA_inv = ADC_inv.VC-ADC_inv.VA;
    //Calculating Line to neutral Voltage
    VAN_inv= -(VBC_inv+2*VCA_inv)/(3);
    VBN_inv= -(VCA_inv+2*VAB_inv)/(3);
    VCN_inv= -(VAB_inv+2*VBC_inv)/(3);
    //Calling the SOGI on the Voltage
    PARKS_Va_inv.u[0] = VAN_inv;
    PARKS_Vb_inv.u[0] = VBN_inv;
    PARKS_Vc_inv.u[0] = VCN_inv;
    SPLL_1ph_SOGI_F_FUNC_SOGIQSG(&PARKS_Va_inv);
    SPLL_1ph_SOGI_F_FUNC_SOGIQSG(&PARKS_Vb_inv);
    SPLL_1ph_SOGI_F_FUNC_SOGIQSG(&PARKS_Vc_inv);
    VAN_inv=(PARKS_Va_inv.osg_u[0]);
    VBN_inv=(PARKS_Vb_inv.osg_u[0]);
    VCN_inv=(PARKS_Vc_inv.osg_u[0]);

    ////////////////////////Rectifier/////////////////////////
    //Calculating Line to Line Voltage
    VAB_rect = ADC_rect.VA-ADC_rect.VB;
    VBC_rect = ADC_rect.VB-ADC_rect.VC;
    VCA_rect = ADC_rect.VC-ADC_rect.VA;
    //Calculating Line to neutral Voltage
    VAN_rect= -(VBC_rect+2*VCA_rect)/(3);
    VBN_rect= -(VCA_rect+2*VAB_rect)/(3);
    VCN_rect= -(VAB_rect+2*VBC_rect)/(3);
    //Calling the SOGI on the Voltage
    PARKS_Va_rect.u[0] = VAN_rect;
    PARKS_Vb_rect.u[0] = VBN_rect;
    PARKS_Vc_rect.u[0] = VCN_rect;
    SPLL_1ph_SOGI_F_FUNC_SOGIQSG(&PARKS_Va_rect);
    SPLL_1ph_SOGI_F_FUNC_SOGIQSG(&PARKS_Vb_rect);
    SPLL_1ph_SOGI_F_FUNC_SOGIQSG(&PARKS_Vc_rect);
    VAN_rect=(PARKS_Va_rect.osg_u[0]);
    VBN_rect=(PARKS_Vb_rect.osg_u[0]);
    VCN_rect=(PARKS_Vc_rect.osg_u[0]);


    //ENABLE PLL FOR RECTIFIER WHEN HAVING THEM BOTH WORKING
TOGETHER
    //PLL with Rectifier because VLL in Capacitors is the same
as the grid
    //Calling PLL
    abc_dq0_voltage1_rect.a = VAN_rect;
    abc_dq0_voltage1_rect.b = VBN_rect;
    abc_dq0_voltage1_rect.c = VCN_rect;
    abc_dq0_voltage1_rect.sin = (float)sin((spll1.theta[1]));
```

```
    abc_dq0_voltage1_rect.cos = (float)cos((spll1.theta[1]));
    ABC_DQ0_POS_F_MACRO(abc_dq0_voltage1_rect);
    spll1.v_q[0] = (abc_dq0_voltage1_rect.q);
    // SPLL call
    SPLL_3ph_SRF_F_FUNC(&spll1);


    //CONVERT VOLTAGE AND CURRENT TO D-Q
    ////////////////////////Rectifier//////////////////////////
    //From ABC to DQ- Voltage
    abc_dq0_voltage1_rect.a = VAN_rect;
    abc_dq0_voltage1_rect.b = VBN_rect;
    abc_dq0_voltage1_rect.c = VCN_rect;
    abc_dq0_voltage1_rect.sin = (float)sin((spll1.theta[0]));
    abc_dq0_voltage1_rect.cos = (float)cos((spll1.theta[0]));
    ABC_DQ0_POS_F_MACRO(abc_dq0_voltage1_rect);


    /////////////IGNORE DO NOT WANT TO USE THE SOGI or DIGITLA
LOW PASS FILTER ON CURRENTS
    /*  ////From ABC to DQ- Current

      IA_LOWPASS.U_0=ADC_rect.IA;
      LOW_PASS_FUNC(&IA_LOWPASS);
      ADC_rect.IA= IA_LOWPASS.out_0;

      IB_LOWPASS.U_0=ADC_rect.IB;
      LOW_PASS_FUNC(&IB_LOWPASS);
      ADC_rect.IB= IB_LOWPASS.out_0;

      IC_LOWPASS.U_0=ADC_rect.IC;
      LOW_PASS_FUNC(&IC_LOWPASS);
      ADC_rect.IC = IC_LOWPASS.out_0;*/
/*
    //Calling the SOGI on the Voltage
    PARKS_Ia_rect.u[0] = ADC_rect.IA;
    PARKS_Ib_rect.u[0] =ADC_rect.IB;
    PARKS_Ic_rect.u[0] = ADC_rect.IC;
    SPLL_1ph_SOGI_F_FUNC_SOGIQSG(&PARKS_Ia_rect);
    SPLL_1ph_SOGI_F_FUNC_SOGIQSG(&PARKS_Ib_rect);
    SPLL_1ph_SOGI_F_FUNC_SOGIQSG(&PARKS_Ic_rect);
    ADC_rect.IA=(PARKS_Ia_rect.osg_u[0]);
    ADC_rect.IB=(PARKS_Ib_rect.osg_u[0]);
    ADC_rect.IC=(PARKS_Ic_rect.osg_u[0]);*/
    /////////////IGNORE DO NOT WANT TO USE THE SOGI or DIGITAL
LOW PASS FILTER ON CURRENTS
```

```
    //From ABC to DQ- CURRENT
    abc_dq0_current1_rect.a = ADC_rect.IA;
    abc_dq0_current1_rect.b = ADC_rect.IB;
    abc_dq0_current1_rect.c = ADC_rect.IC;
    abc_dq0_current1_rect.sin = (float)sin( (spll1.theta[0]));
    abc_dq0_current1_rect.cos = (float)cos( (spll1.theta[0]));
    ABC_DQ0_POS_F_MACRO(abc_dq0_current1_rect);

    ////////////////////////INVERTER/////////////////////////

    #if (INVERTER_TEST)
    //DISABLE WHEN HAVING THEM BOTH WOKRING TOGETHER
            //Calling PLL
            abc_dq0_voltage1_inv.a = VAN_inv;
            abc_dq0_voltage1_inv.b = VBN_inv;
            abc_dq0_voltage1_inv.c = VCN_inv;
            abc_dq0_voltage1_inv.sin =
(float)sin((spll1.theta[1]));
            abc_dq0_voltage1_inv.cos =
(float)cos((spll1.theta[1]));
            ABC_DQ0_POS_F_MACRO(abc_dq0_voltage1_inv);
            spll1.v_q[0] = (abc_dq0_voltage1_inv.q);
            // SPLL call
            SPLL_3ph_SRF_F_FUNC(&spll1);
    #endif


    //From ABC to DQ- Voltage
    abc_dq0_voltage1_inv.a = VAN_inv;
    abc_dq0_voltage1_inv.b = VBN_inv;
    abc_dq0_voltage1_inv.c = VCN_inv;
    abc_dq0_voltage1_inv.sin = (float)sin((spll1.theta[0]));
    abc_dq0_voltage1_inv.cos = (float)cos((spll1.theta[0]));
    ABC_DQ0_POS_F_MACRO(abc_dq0_voltage1_inv);
    ////From ABC to DQ- Current
    abc_dq0_current1_inv.a = ADC_inv.IA;
    abc_dq0_current1_inv.b = ADC_inv.IB;
    abc_dq0_current1_inv.c = ADC_inv.IC;
    abc_dq0_current1_inv.sin = (float)sin( (spll1.theta[0]));
    abc_dq0_current1_inv.cos = (float)cos( (spll1.theta[0]));
    ABC_DQ0_POS_F_MACRO(abc_dq0_current1_inv);

    //FOR DEBUGGING
    #if (DEBUG_Controller)
    Voltage1[ConversionCount]= ADC_rect.IA;
    Voltage2[ConversionCount]= ADC_rect.IB;
    Voltage3[ConversionCount]=ADC_rect.IC;
```

```
      if(ConversionCount == 400)
      {
          ConversionCount = 0;
      }
      else
      {
          ConversionCount++;
      }
     #endif

//////////////////////////////MODE OF OPERATION
//////////////////////////////////
     //MODE 1 ALL switches OFF
     //MODE 2 Current Controller
     //MODE 3 Open Loop TEST

     if (MODE == 1)
     {
        // Adjust duty for output EPWM1A
        S1_inv=1;
        S2_inv=1;
        S3_inv=1;
        S1_rect=1;
        S2_rect=1;
        S3_rect=1;
     }

     if (MODE == 2)
     {
     ////////////////////////////Rectifier/////////////////////////////
         if(Vdcref < VdcrefMax)
         {
         Vdcref += Vdcrefstep;
         }
         if(Vdcref > VdcrefMax)
         { Vdcref= VdcrefMax;}

         Voltage_Controller_Vdc.err=Vdcref-ADC_rect.Vdc;
         PI_controller_FUNC(&Voltage_Controller_Vdc);
         //Idref1_rect=Voltage_Controller_Vdc.out;
         //
Idref1_rect=((Idref1_rect*ADC_rect.Vdc)/(3*abc_dq0_voltage1_rect
.d))-Idref1_inv;
         Idref1_rect=Voltage_Controller_Vdc.out-Idref1_inv;
         Iqref1_rect=0;

         //Current Controller
```

```
        Current_Controller_D_rect.err= Idref1_rect-
abc_dq0_current1_rect.d;
        PI_controller_FUNC(&Current_Controller_D_rect);
        Current_Controller_Q_rect.err=Iqref1_rect-
abc_dq0_current1_rect.q;
        PI_controller_FUNC(&Current_Controller_Q_rect);
        //Current Decoupling
        dfinal=  abc_dq0_voltage1_rect.d +
Current_Controller_D_rect.out -(abc_dq0_current1_rect.q*GainC) ;
        qfinal=  Current_Controller_Q_rect.out +
(abc_dq0_current1_rect.d*GainC)  +abc_dq0_voltage1_rect.q;//
        // Saturation  Block
        dfinal2= dfinal*dfinal;
        qfinal2=qfinal*qfinal;
        vdcovertwo= ADC_rect.Vdc/sqrt3;
        temp1= sqrt(dfinal2+qfinal2);
        temp2= sqrt(dfinal2+qfinal2+0.0001);
        if (vdcovertwo < temp1)
        {
        dfinal= dfinal/temp2;
        qfinal= qfinal/temp2;
        }
        if (vdcovertwo > temp1)
        {
        dfinal= dfinal/vdcovertwo;
        qfinal= qfinal/vdcovertwo;
        }
        //FROM DQ to alpha beta
        modulation1_rect.d = dfinal;
        modulation1_rect.q = qfinal;
        modulation1_rect.sin = sin(spll1.theta[0]);
        modulation1_rect.cos = cos(spll1.theta[0]);
        iPARK_F_FUNC(&modulation1_rect);
        //CAll Space vector modulation
        svgen_dq1_rect.Ualpha =  modulation1_rect.alpha;
        svgen_dq1_rect.Ubeta = modulation1_rect.beta;
        svgendq_calc(&svgen_dq1_rect);
        //Assign Duty
        S1_rect =   (svgen_dq1_rect.Ta+1.0)/2;  //
        S2_rect =   (svgen_dq1_rect.Tb+1.0)/2; //
        S3_rect =   (svgen_dq1_rect.Tc+1.0)/2;

    ////////////////////////INVERTER/////////////////////////

        if (Inverter_Start==1)
        {
        if(Idref1_inv < Idrefmax)
```

```
        {
        Idref1_inv += Idrefdstep;
        }
        if(Idref1_inv > Idrefmax)
        { Idref1_inv= Idrefmax;};
        Iqref1_inv=0;

        //Current Controller
        Current_Controller_D_inv.err= Idref1_inv-
abc_dq0_current1_inv.d;
        PI_controller_FUNC(&Current_Controller_D_inv);
        Current_Controller_Q_inv.err=Iqref1_inv-
abc_dq0_current1_inv.q;
        PI_controller_FUNC(&Current_Controller_Q_inv);
        //Current Decoupling
        dfinal=  abc_dq0_voltage1_inv.d +
Current_Controller_D_inv.out -(abc_dq0_current1_inv.q*GainC) ;
        qfinal=  Current_Controller_Q_inv.out +
(abc_dq0_current1_inv.d*GainC)  +abc_dq0_voltage1_inv.q;//
        // Saturation  Block
        dfinal2= dfinal*dfinal;
        qfinal2=qfinal*qfinal;
        vdcovertwo= ADC_inv.Vdc/sqrt3;
        temp1= sqrt(dfinal2+qfinal2);
        temp2= sqrt(dfinal2+qfinal2+0.0001);
        if (vdcovertwo < temp1)
        {
        dfinal= dfinal/temp2;
        qfinal= qfinal/temp2;
        }
        if (vdcovertwo > temp1)
        {
        dfinal= dfinal/vdcovertwo;
        qfinal= qfinal/vdcovertwo;
        }
        //FROM DQ to alpha beta
        modulation1_inv.d = dfinal;
        modulation1_inv.q = qfinal;
        modulation1_inv.sin = sin(spll1.theta[0]);
        modulation1_inv.cos = cos(spll1.theta[0]);
        iPARK_F_FUNC(&modulation1_inv);
        //CAll Space vector modulation
        svgen_dq1_inv.Ualpha =  modulation1_inv.alpha;
        svgen_dq1_inv.Ubeta = modulation1_inv.beta;
        svgendq_calc(&svgen_dq1_inv);
        //Assign Duty
        S1_inv =   (svgen_dq1_inv.Ta+1.0)/2;  //
```

```
        S2_inv =    (svgen_dq1_inv.Tb+1.0)/2; //
        S3_inv =    (svgen_dq1_inv.Tc+1.0)/2; //
        }

        else
        {
        S1_inv=1;
        S2_inv=1;
        S3_inv=1;
        }


    }

    if (MODE == 3)
    {

//////////////////////////Rectifier////////////////////////////
    #if (OPEN_LOOP_RECTIFIER)
        dfinal=GAIN;
        qfinal=0;
    #endif

    #if (!OPEN_LOOP_RECTIFIER)
        if(Vdcref < VdcrefMax)
                {
                Vdcref += Vdcrefstep;
                }
                if(Vdcref > VdcrefMax)
                { Vdcref= VdcrefMax;}

                Voltage_Controller_Vdc.err=Vdcref-ADC_rect.Vdc;
                PI_controller_FUNC(&Voltage_Controller_Vdc);
                Idref1_rect=Voltage_Controller_Vdc.out;

//Idref1_rect=Voltage_Controller_Vdc.out;
        //
Idref1_rect=((Idref1_rect*ADC_rect.Vdc)/(3*abc_dq0_voltage1_rect
.d))-Idref1_inv;
        Idref1_rect=Voltage_Controller_Vdc.out-Idref1_inv;

                //Current Controller
                Current_Controller_D_rect.err= Idref1_rect-
abc_dq0_current1_rect.d;
                PI_controller_FUNC(&Current_Controller_D_rect);
                Current_Controller_Q_rect.err=Iqref1_rect-
abc_dq0_current1_rect.q;
```

```
                PI_controller_FUNC(&Current_Controller_Q_rect);
                //Current Decoupling
                dfinal=  abc_dq0_voltage1_rect.d +
Current_Controller_D_rect.out -(abc_dq0_current1_rect.q*GainC) ;
                qfinal=  Current_Controller_Q_rect.out +
(abc_dq0_current1_rect.d*GainC)  +abc_dq0_voltage1_rect.q;//
                 // Saturation  Block
                dfinal2= dfinal*dfinal;
                qfinal2=qfinal*qfinal;
                vdcovertwo= ADC_rect.Vdc/sqrt3;
                temp1= sqrt(dfinal2+qfinal2);
                temp2= sqrt(dfinal2+qfinal2+0.0001);
                if (vdcovertwo < temp1)
                {
                dfinal= dfinal/temp2;
                qfinal= qfinal/temp2;
                }
                if (vdcovertwo > temp1)
                {
                dfinal= dfinal/vdcovertwo;
                qfinal= qfinal/vdcovertwo;
                }
    #endif


        //FROM DQ to alpha beta
        modulation1_rect.d = dfinal;
        modulation1_rect.q = qfinal;
        modulation1_rect.sin = sin(spll1.theta[0]);
        modulation1_rect.cos = cos(spll1.theta[0]);
        iPARK_F_FUNC(&modulation1_rect);
        //CAll Space vector modulation
        svgen_dq1_rect.Ualpha =  modulation1_rect.alpha;
        svgen_dq1_rect.Ubeta = modulation1_rect.beta;
        svgendq_calc(&svgen_dq1_rect);
        //Assign Duty
        S1_rect =   (svgen_dq1_rect.Ta+1.0)/2;  //
        S2_rect =   (svgen_dq1_rect.Tb+1.0)/2; //
        S3_rect =   (svgen_dq1_rect.Tc+1.0)/2; //

        if (Inverter_Start==1)
        {
        //Assigns gains PWM Modulation
        //Gain is Change in Parameters.h
        dfinal=GAIN;
        qfinal=0;
```

```
        //FROM DQ to alpha beta
        modulation1_inv.d = dfinal;
        modulation1_inv.q = qfinal;
        modulation1_inv.sin = sin(radian);
        modulation1_inv.cos = cos(radian);
        iPARK_F_FUNC(&modulation1_inv);
        //CAll Space vector modulation
        svgen_dq1_inv.Ualpha =  modulation1_inv.alpha;
        svgen_dq1_inv.Ubeta = modulation1_inv.beta;
        svgendq_calc(&svgen_dq1_inv);
        //Assign Duty
        S1_inv =    (svgen_dq1_inv.Ta+1.0)/2;  //
        S2_inv =    (svgen_dq1_inv.Tb+1.0)/2; //
        S3_inv =    (svgen_dq1_inv.Tc+1.0)/2; //

        //Generate Angular Reference
        radian += (Ts);
        if(radian > 2*pi)
        {
        radian -= (2*pi);
        }
        }
        else
        {
        S1_inv=1;
        S2_inv=1;
        S3_inv=1;
        }


    }

    //-------------------------------------------------------------
-----------
    //PWM outputs (normalized between 0 to 1)
    PWM_inv.CMP1=S1_inv;
    PWM_inv.CMP2=S2_inv;
    PWM_inv.CMP3=S3_inv;
    PWM_rect.CMP1=S1_rect;
    PWM_rect.CMP2=S2_rect;
    PWM_rect.CMP3=S3_rect;

}

////////////////////////////Functions//////////////////////////
////////
```

```
////////////////////////////////////////////////////////////////
////////

  ////////////////////PI CONTROLLER//////////////////////
////////////////////Was developed by Vinson Jones//////////////

void PI_controller_init(PI_controller *PI_controller_obj)
{
    PI_controller_obj->PIconstant= -(PI_controller_obj->KP) +
(PI_controller_obj->KI)*(PI_controller_obj->TS);
    PI_controller_obj->err = 0;
    PI_controller_obj->err_1 = 0;
    PI_controller_obj->out = 0;
    PI_controller_obj->U_1 = 0;
    PI_controller_obj->excess = 0;
}

void PI_controller_FUNC(PI_controller *PI_controller_obj)
{

    PI_controller_obj->out = PI_controller_obj->U_1 +
(PI_controller_obj->PIconstant)*(PI_controller_obj->err_1) +
(PI_controller_obj->KP)*(PI_controller_obj->err);


    PI_controller_obj->err_1 = PI_controller_obj->err;


    PI_controller_obj->U_1 = PI_controller_obj->out;
}
////////////////////SOGI FLTER//////////////////////
////////////////////Was developed by Vinson Jones//////////////
void SPLL_1ph_SOGI_F_init(int Grid_freq, float32 DELTA_T,
SPLL_1ph_SOGI_F *spll_obj)
{
    spll_obj->u[0]=(float32)(0.0);
    spll_obj->u[1]=(float32)(0.0);
    spll_obj->u[2]=(float32)(0.0);

    spll_obj->osg_u[0]=(float32)(0.0);
    spll_obj->osg_u[1]=(float32)(0.0);
    spll_obj->osg_u[2]=(float32)(0.0);

    spll_obj->osg_qu[0]=(float32)(0.0);
    spll_obj->osg_qu[1]=(float32)(0.0);
    spll_obj->osg_qu[2]=(float32)(0.0);
```

```
    spll_obj->u_Q[0]=(float32)(0.0);
    spll_obj->u_Q[1]=(float32)(0.0);

    spll_obj->u_D[0]=(float32)(0.0);
    spll_obj->u_D[1]=(float32)(0.0);

    spll_obj->ylf[0]=(float32)(0.0);
    spll_obj->ylf[1]=(float32)(0.0);

    spll_obj->fo=(float32)(0.0);
    spll_obj->fn=(float32)(Grid_freq);

    spll_obj->theta[0]=(float32)(0.0);
    spll_obj->theta[1]=(float32)(0.0);

    spll_obj->sin=(float32)(0.0);
    spll_obj->cos=(float32)(0.0);

    // loop filter coefficients for 20kHz
    spll_obj->lpf_coeff.B0_lf=(float32)(166.9743);
    spll_obj->lpf_coeff.B1_lf=(float32)(-166.266);
    spll_obj->lpf_coeff.A1_lf=(float32)(-1.0);

    spll_obj->delta_T=DELTA_T;
}

void SPLL_1ph_SOGI_F_coeff_update(float32 delta_T, float32 wn,
SPLL_1ph_SOGI_F *spll)
{
    float32 osgx,osgy,temp;
    spll->osg_coeff.osg_k=(float32)(0.5);
    osgx=(float32)(2.0*0.5*wn*delta_T);
    spll->osg_coeff.osg_x=(float32)(osgx);
    osgy=(float32)(wn*delta_T*wn*delta_T);
    spll->osg_coeff.osg_y=(float32)(osgy);
    temp=(float32)1.0/(osgx+osgy+4.0);
    spll->osg_coeff.osg_b0=((float32)osgx*temp);
    spll->osg_coeff.osg_b2=((float32)(-1.0)*spll-
>osg_coeff.osg_b0);
    spll->osg_coeff.osg_a1=((float32)(2.0*(4.0-osgy))*temp);
    spll->osg_coeff.osg_a2=((float32)(osgx-osgy-4)*temp);
    spll->osg_coeff.osg_qb0=((float32)(0.5*osgy)*temp);
    spll->osg_coeff.osg_qb1=(spll-
>osg_coeff.osg_qb0*(float32)(2.0));
    spll->osg_coeff.osg_qb2=spll->osg_coeff.osg_qb0;
}
```

```
void SPLL_1ph_SOGI_F_FUNC_SOGIQSG(SPLL_1ph_SOGI_F * spll_obj)
{
    // Update the spll_obj->u[0] with the grid value before
calling this routine

    //-------------------------------//
    // Orthogonal Signal Generator   //
    //-------------------------------//
    spll_obj->osg_u[0]=(spll_obj->osg_coeff.osg_b0*(spll_obj-
>u[0]-spll_obj->u[2])) + (spll_obj->osg_coeff.osg_a1*spll_obj-
>osg_u[1]) + (spll_obj->osg_coeff.osg_a2*spll_obj->osg_u[2]);

    spll_obj->osg_u[2]=spll_obj->osg_u[1];
    spll_obj->osg_u[1]=spll_obj->osg_u[0];

    spll_obj->osg_qu[0]=(spll_obj->osg_coeff.osg_qb0*spll_obj-
>u[0]) + (spll_obj->osg_coeff.osg_qb1*spll_obj->u[1]) +
(spll_obj->osg_coeff.osg_qb2*spll_obj->u[2]) + (spll_obj-
>osg_coeff.osg_a1*spll_obj->osg_qu[1]) + (spll_obj-
>osg_coeff.osg_a2*spll_obj->osg_qu[2]);

    spll_obj->osg_qu[2]=spll_obj->osg_qu[1];
    spll_obj->osg_qu[1]=spll_obj->osg_qu[0];

    spll_obj->u[2]=spll_obj->u[1];
    spll_obj->u[1]=spll_obj->u[0];
}

////////////////////3 PHASE PLL//////////////////////
////////////////////TI SOLAR LIBRARY//////////////////////
void SPLL_3ph_SRF_F_init(int Grid_freq, float32 DELTA_T,
SPLL_3ph_SRF_F *spll_obj)
{
    spll_obj->v_q[0]=(float32)(0.0);
    spll_obj->v_q[1]=(float32)(0.0);

    spll_obj->ylf[0]=(float32)(0.0);
    spll_obj->ylf[1]=(float32)(0.0);

    spll_obj->fo=(float32)(0.0);
    spll_obj->fn=(float32)(Grid_freq);

    spll_obj->theta[0]=(float32)(0.0);
    spll_obj->theta[1]=(float32)(0.0);

    // loop filter coefficients for 20kHz
```

```
    spll_obj->lpf_coeff.B0_lf=(float32)(223.7341299*0.01);
    spll_obj->lpf_coeff.B1_lf=(float32)(-220.5864768*0.01);
    spll_obj->lpf_coeff.A1_lf=(float32)(-1.0);

    spll_obj->delta_T=(float32)DELTA_T;
}

void SPLL_3ph_SRF_F_FUNC(SPLL_3ph_SRF_F *spll_obj)
{
    //update v_q[0] before calling the routine
    //---------------------------------//
    // Loop Filter                     //
    //---------------------------------//
    spll_obj->ylf[0]=spll_obj->ylf[1] + (spll_obj-
>lpf_coeff.B0_lf*spll_obj->v_q[0]) + (spll_obj-
>lpf_coeff.B1_lf*spll_obj->v_q[1]);
    spll_obj->ylf[1]=spll_obj->ylf[0];
    spll_obj->v_q[1]=spll_obj->v_q[0];

    spll_obj->ylf[0]=(spll_obj-
>ylf[0]>(float32)(200.0))?(float32)(200.0):spll_obj->ylf[0];
    //---------------------------------//
    // VCO                             //
    //---------------------------------//
    spll_obj->fo=spll_obj->fn + spll_obj->ylf[0];

    spll_obj->theta[0]=spll_obj->theta[1] + ((spll_obj-
>fo*spll_obj->delta_T)*(float32)(2*3.1415926));
    if(spll_obj->theta[0] > (float32)(2*3.1415926))
        spll_obj->theta[0]=spll_obj->theta[0] -
(float32)(2*3.1415926);

    spll_obj->theta[1]=spll_obj->theta[0];
}
////////////////////ABC TO DQ//////////////////////
void ABC_DQ0_POS_F_init(ABC_DQ0_POS_F *v){
    v->a=0;
    v->b=0;
    v->c=0;
    v->alpha=0;
    v->beta=0;
    v->z=0;
    v->d=0;
    v->q=0;
}

void ABC_DQ0_POS_F_FUNC(ABC_DQ0_POS_F *v){
```

```
    v->alpha=(0.6666666667)*(v->a-0.5*(v->b+v->c));
    v->beta=(0.57735026913)*(v->b-v->c);
    v->z =0.57735026913*(v->a+v->b+v->c);
    v->d=v->alpha*v->cos+v->beta*v->sin;
    v->q=-v->alpha*v->sin+v->beta*v->cos;
}

//////////////////////DQ to ALPHA BETA////////////////////////
//////////////////////TI SOLAR LIBRARY////////////////////////
void iPARK_F_init(iPARK_F *v)
{
    v->alpha=0;
    v->beta=0;
    v->zero=0;
    v->d=0;
    v->q=0;
    v->z=0;
}

void iPARK_F_FUNC(iPARK_F *v)
{
    v->alpha = v->d*v->cos - v->q*v->sin;
    v->beta  = v->d*v->sin + v->q*v->cos;
    v->zero  = v->z;
}
//////////////////////SPACE VECTOR
MODULATION////////////////////////
//////////////////////SVGEN_DQ from TI////////////////////////

void svgendq_calc(SVGENDQ *v)
{
    float Va,Vb,Vc,t1,t2;
    Uint32 Sector = 0;  // Sector is treated as Q0 -
independently with global Q

    // Inverse clarke transformation
    Va=v->Ubeta;
    Vb= (-0.5*v->Ubeta)+ (0.8660254*v->Ualpha);//0.8660254 =
sqrt(3)/2
    Vc=(-0.5*v->Ubeta)-(0.8660254*v->Ualpha);//0.8660254 =
sqrt(3)/2


    //60 degree Sector determination
    if (Va>0)
    { Sector = 1;}
    if (Vb>0)
```

```
    {  Sector = Sector + 2;}
    if (Vc>0)
    {  Sector = Sector + 4;}

    // X,Y,Z (Va,Vb,Vc) calculations
    Va=v->Ubeta; //X=Va
    Vb= (0.5*v->Ubeta)+ (0.8660254*v->Ualpha); //Y=Vb
    Vc=(0.5*v->Ubeta)-(0.8660254*v->Ualpha); //C=Vc

    if (Sector==0)  // Sector 0: this is special case for
(Ualpha,Ubeta) = (0,0)
    {
       v->Ta = 0.5;
       v->Tb = 0.5;
       v->Tc = 0.5;
    }
  if (Sector==1)  // Sector 1: t1=Z and t2=Y (abc ---> Tb,Ta,Tc)
  {
       t1 = Vc;
       t2 = Vb;
       v->Tb = 0.5*(1-t1-t2);     // tbon = (1-t1-t2)/2
       v->Ta = v->Tb+t1;                                 // taon =
tbon+t1
      v->Tc = v->Ta+t2;                                 // tcon =
taon+t2
  }
  else if (Sector==2) // Sector 2: t1=Y and t2=-X (abc --->
Ta,Tc,Tb)
  {
      t1 = Vb;
       t2 = -Va;
       v->Ta = 0.5*(1-t1-t2);                    // taon = (1-t1-
t2)/2
       v->Tc = v->Ta+t1;                                  // tcon =
taon+t1
       v->Tb = v->Tc+t2;                                  // tbon =
tcon+t2
  }
  else if (Sector==3)  // Sector 3: t1=-Z and t2=X (abc --->
Ta,Tb,Tc)
  {
       t1 = -Vc;
       t2 = Va;
      v->Ta = 0.5*(1-t1-t2);      // taon = (1-t1-t2)/2
       v->Tb = v->Ta+t1;                                 // tbon =
taon+t1
```

```
        v->Tc = v->Tb+t2;                                   // tcon =
tbon+t2
  }
  else if (Sector==4)  // Sector 4: t1=-X and t2=Z (abc --->
Tc,Tb,Ta)
  {
        t1 = -Va;
        t2 = Vc;
        v->Tc = 0.5*(1-t1-t2);       // tcon = (1-t1-t2)/2
        v->Tb = v->Tc+t1;                                   // tbon =
tcon+t1
        v->Ta = v->Tb+t2;                                   // taon =
tbon+t2
  }
  else if (Sector==5)  // Sector 5: t1=X and t2=-Y (abc --->
Tb,Tc,Ta)
  {
        t1 = Va;
        t2 = -Vb;
        v->Tb =0.5*(1-t1-t2);       // tbon = (1-t1-t2)/2
        v->Tc = v->Tb+t1;                                   // tcon =
tbon+t1
        v->Ta = v->Tc+t2;                                   // taon =
tcon+t2
  }
  else if (Sector==6)  // Sector 6: t1=-Y and t2=-Z (abc --->
Tc,Ta,Tb)
  {
        t1 = -Vb;
        t2 = -Vc;
        v->Tc = 0.5*(1-t1-t2);       // tcon = (1-t1-t2)/2
        v->Ta = v->Tc+t1;                                   // taon =
tcon+t1
        v->Tb = v->Ta+t2;                                   // tbon =
taon+t2
  }



// Convert the unsigned GLOBAL_Q format (ranged (0,1)) -> signed
GLOBAL_Q format (ranged (-1,1))
    v->Ta = 2*(v->Ta-0.5);
    v->Tb = 2*(v->Tb-0.5);
    v->Tc = 2*(v->Tc-0.5);

    }
```

```
    void SVGENDQ_init(SVGENDQ *v)
    {
    v->Ualpha=0;
    v->Ubeta=0;
    v->Ta=0;
    v->Tb=0;
    v->Tc=0;
    }

      ////////////////////LOW PASS FILTER//////////////////////
    void LOW_PASS_FUNC(LOW_PASS *LOW_PASS_obj)
    {
        LOW_PASS_obj->out_0 = (1-LOW_PASS_obj->AA)*LOW_PASS_obj-
>out_0 + LOW_PASS_obj->AA*LOW_PASS_obj->U_0;

        LOW_PASS_obj->out_1 = LOW_PASS_obj->out_0;
    }


    void LOW_PASS_init(LOW_PASS *LOW_PASS_obj)
    {
        LOW_PASS_obj->U_0 = 0;
        LOW_PASS_obj->out_0 = 0;
        LOW_PASS_obj->out_1 = 0;
        LOW_PASS_obj->AA = LOW_PASS_obj->hh/((LOW_PASS_obj-
>Tf+LOW_PASS_obj->hh));

    }
```

APPENDIX B

MATLAB SCRIPTS

B.1 Bode Plots of a Single and Two Parallel Regen Benches

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Rectifier with a Single and Two Regen
clc
clear
s=tf('s');
% Parameters
L1=560e-6; %Inverter-side Inductance
L2=330e-6; %Grid-side Inductance
C=3*18.6e-6; % Capacitor Filter
Lg=100e-6; % Grid Inductance
% Impedances
Z1=s*L1;
Z2=s*L2;
Z3=1/(s*C);
Zg=s*Lg;
%Transfer Function with a single regen
zeq1=Z1*Z3/(Z1+Z3);
zeq2= zeq1+Z2;
zeq3=zeq2*Zg/(Zg+zeq2);
H_single_regen= Z3/(Z1*zeq3+Z1*Z3+zeq3*Z3);
%Transfer Function with two regens
zeq1=minreal(Z1*Z3/(Z1+Z3));
zeq2= minreal(zeq1+Z2);
zeq3=minreal(zeq2/2);
zeq4=minreal(zeq3*zeq1/(zeq3+zeq1));
zeq5=minreal(zeq4*Zg/(Zg+zeq4),5e-4);
H_two_regens= minreal((Z3/(Z1*zeq5+Z1*Z3+zeq5*Z3)),5e-4);
opts = bodeoptions('cstprefs');
opts.PhaseVisible = 'off';
opts.FreqUnits = 'Hz';
figure(1)
bode(H_single_regen,H_two_regens,opts)
legend('Rectifier of One Regen Bench', 'Rectifier of Two Regen
Benches')

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Inverter with a single and Two Regen benches
clear
clc
s=tf('s');
```

```
% Parameters
L=560e-6; %Inverter-side Inductance
C=3*18.6e-6; % Capacitor Filter
Lg=100e-6; % Grid Inductance
% Impedances
Z1=s*L;
Z2=s*330e-6;
Z3=1/(s*C);
Zg=s*Lg;
% Equivalent impedance with a single regen
zeq1=Z1*Z3/(Z1+Z3);
zeq2=zeq1*Zg/(Zg+zeq1);
zeq3=zeq2+Z2;
H_single_regen= Z3/(Z1*zeq3+Z1*Z3+zeq3*Z3);
% Equivalent Impedance with two regens
zeq1=minreal(Z1*Z3/(Z1+Z3),1e-4);
zeq2= minreal((zeq1+Z2),1e-4);
zeq1=minreal(zeq1/2,1e-4);
zeq3=minreal(zeq1*zeq2/(zeq2+zeq1),1e-4);
zeq4=minreal(zeq3*Zg/(Zg+zeq3),1e-4);
zeq5=minreal(zeq4+Z2,1e-4);
H_two_regens= minreal(Z3/(Z1*zeq5+Z1*Z3+zeq5*Z3),50e-3);
opts = bodeoptions('cstprefs');
opts.PhaseVisible = 'off';
opts.FreqUnits = 'Hz';
figure(2)
bode(H_single_regen,H_two_regens,opts)
legend('Inverter of One Regen Bench', 'Inverter of Two Regen
Benches')
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```