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Silicon Germanium BiCMOS Comparator Designed for Use in An Extreme Environment Analog to Digital Converter

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Abstract

This thesis demonstrates the process of creating a radiation hardened and extreme temperature operating comparator from start to finish in the 90 nm SiGe 9HP process node. This includes the entire design flow from examining comparator topologies, to designing the initial comparator circuits, to simulating the comparator over a temperature range of -196°C to 125°C, and finally the testing of the fabricated circuit. To verify the circuit would work at low temperatures, several new device models were created that could be used for simulations at -196°C. In addition to its properties as a standalone comparator, the circuit was also used as a building block in a SAR ADC that would be used for extreme environments.

Acknowledgements

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Chapter 1 - Introduction

One of the most important aspects of space travel and interplanetary exploration is being able to gather information and collect data about the surrounding environment. To accomplish these tasks there must be a system of sensors and circuits to collect and transfer the data that is captured. One of the most basic system building blocks of these circuits is the analog-to-digital converter (ADC). As the name implies, this circuit's purpose is to convert analog data from sensors or any other source to a digital output that can be stored.

Unfortunately, most electronic circuits are vulnerable to the harsh environments present in outer space as well as on other planets. These unforgiving conditions include large Megarad doses of radiation as well as cryogenic (less than -55°C) temperatures [1]. Therefore, it is usually necessary to encase electronic circuits in protective warm boxes that ensure the survival of the circuits in these conditions.

The purpose of this work is to explore the design of a Silicon-Germanium (SiGe) comparator for a Successive Approximation Register (SAR) ADC that will work in both cryogenic temperatures as well as while being exposed to radiation without the need for protective environments. This will allow the circuits to have a much smaller footprint on the overall size of the system.

1.1 Previous Circuits for Space Applications

The University of Arkansas Mixed-Signal Computer-Aided Design (MSCAD) lab was previously involved in designing circuits in a SiGe process for extreme environments. Some of these circuits include differential amplifiers [2], SRAM and ROM memory cells [3], DC motor

drives [4], and comparators [5]. This project is a continuation of the research efforts that were put into those applications and builds upon their efforts and successes.

1.2 Analog to Digital Converter

The circuit that was to be designed for this NASA Space Technology Research Opportunities Early Stage Innovations (or NASA STRO-ESI) project was an analog-to-digital converter using a charge-sharing Successive Approximation Register (SAR) topology. The goal for this project was to ensure that the integrated circuits in the ADC would be resilient to radiation strikes as well as continue to operate under cryogenic temperatures. In addition to this, the ADC should also exhibit low power consumption.

The SAR ADC in this work was built upon the principles of passive charge-sharing. The way this works is that when the ADC samples an input voltage, depending on the SAR algorithm, the sampled voltage will either have charge added or subtracted from it via a network of capacitors [6]. The output of the comparator tells the control block whether to add or subtract the charge. The output of the comparator is also stored in the control block's digital memory as each bit of the digital output. In this way, the analog voltage will be converted to a digital output from the MSB to the LSB. The diagram demonstrating the SAR ADC architecture is shown in Figure 1.1.

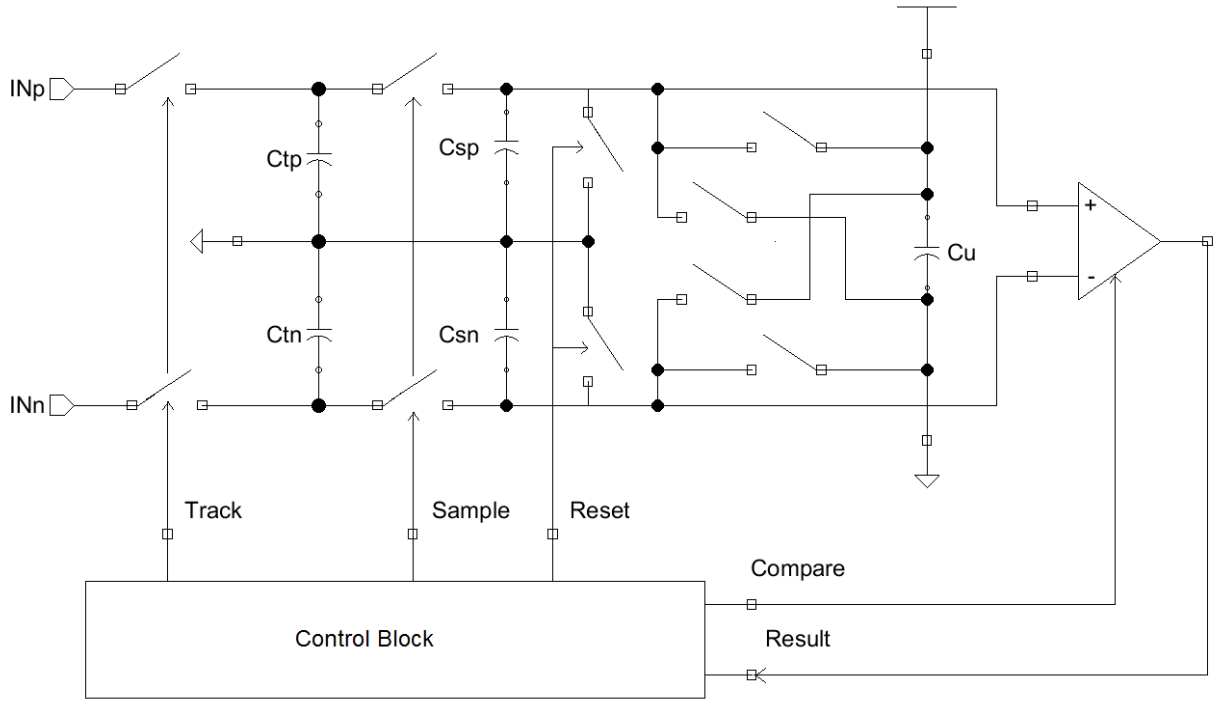


Figure 1.1. SAR ADC block diagram.

The C_{tp} and C_{tn} capacitors are the tracking capacitors that track the input voltages IN_p and IN_n until the control block gives the signal to stop tracking. At this point the sampling capacitors C_{sp} and C_{sn} split the charge equally with the tracking capacitors once the sample signal is provided by the control block.

In this diagram, the Cu capacitor is one of 11 capacitors in a network. Each capacitor is sized so that a progressively smaller amount of charge is added or subtracted as the ADC gets closer to the LSB of the output. Thus, these 11 capacitors plus the initial sample capacitors make up the 12 bits of the ADC circuit.

1.3 Comparator in SAR ADC

The comparator's role in the SAR ADC is simple—but very important. It decides whether the SAR ADC should be adding or subtracting charge from the sample capacitors based on the magnitude of the voltages at each input. The output of the comparator will then need to be

captured and stored by the control block to complete the conversion of that bit. Therefore, it is important that the comparator work correctly for every bit in the ADC or the entire output of the ADC block will be invalid. This thesis will focus on the design, simulation, and test of the comparator used in the ADC block.

Chapter 2 - Background

2.1 Process Background

The 9HP process is a high-performance Silicon-Germanium (SiGe) process that was developed by IBM. It is a 90 nm process that features an advanced Heterojunction Bipolar Transistor (HBT). This HBT device is so named because it features a base layer that is a different semiconductor material than the emitter layer [7] therefore creating a heterojunction.

The SiGe HBT device in the 9HP process demonstrates excellent radiation hardness [8], [2] when compared to CMOS devices. In fact, the HBT devices have demonstrated the ability to continue working even after being exposed to a 200 Megarad total ionizing dose (TID) of radiation [1]. Since the space environment has an exposure rate of about 10^{-4} to 10^{-2} rad/s [9], this large tolerance to radiation makes it ideal for use in space. This makes the SiGe HBT a logical choice for a circuit that needs to be hardened against exposure to radiation.

In addition to the SiGe HBT device, it was also noted that the PFET device in the 9HP process demonstrates better radiation hardness than the NFET device because of "problems with hot carrier effects and trapped charge in the shallow trench isolation" [2]. To mitigate potential problems with radiation in the comparator circuit, a decision was made to use only PFET and HBT devices wherever possible. This includes all the mixed signal circuitry in the input to the comparator. The only place that the NFET devices would be allowed is in the buffer circuits that drive the inputs to the asynchronous digital state machine of the ADC. This decision was necessary to allow the comparator to output a completely digital signal that would interface correctly with the digital state machine as the NPN devices did not work well when simulated as digital buffers.

2.2 Specifications for Comparator

Over the years, many different topologies have been used for comparator circuits. Depending on the purpose and technical specifications there are different reasons to use each topology. Some of the specifications that were considered when looking at the different types of comparator topologies were settling time, propagation delay, power dissipation, operating temperature range, and common-mode input voltage range.

One of the design goals for the SAR ADC was to have a minimum sampling rate of 1 MS/s (Mega samples per second) and a maximum sample rate of 5 MS/s. Since the ADC was designed to be a 12-bit data converter and the maximum length of each comparison should be 1 µs, the delay from an input being applied to the comparator and the output propagating should not take longer than:

$$\frac{1\ \mu s}{12\ \text{comparisons}} = 83.3\ \text{ns} / 1\ \text{comparison} \qquad [\ 2.1\ ]$$

And the minimum time per comparison should be:

$$\frac{200\ \text{ns}}{12\ \text{comparisons}} = 16.7\ \text{ns} / 1\ \text{comparison} \qquad [\ 2.2\ ]$$

This delay of 83.3 ns was the very maximum time across all temperatures that the comparator would take to output a comparison and the delay of 16.7 ns was the minimum. Therefore, a design goal of no less than 15 ns of propagation delay at room temperature was chosen for the comparator.

Because of the way that the SAR ADC makes comparisons, the input voltages into the comparator might have a differential voltage of 1 mV. Therefore, another design goal was set for the comparator to have a minimum resolution of 1 mV across temperatures.

The final design goal was for the comparator to have a common mode input range of the bottom half of the supply voltage (0 V to 0.6 V). As explained in [6], the way the charge sharing SAR ADC works is by capturing the input voltages on the tracking capacitors and then splitting the charge to the two sampling capacitors. This has the effect of halving the ADC input range so the highest input voltage the comparator will see at its inputs is VDD/2.

The design goals that were set for the comparator are shown in Table 2.1.

Table 2.1. Design goals for comparator.

Parameter	Value
Supply Voltage	1.2 V
Temperature Range	-196°C ~ 125°C
Propagation Delay	15 ns
Common Mode Input Range	0 V ~ 0.6 V

2.3 Creating Cryogenic Models to Simulate 9HP Devices

The device models included in the process design kit for the BiCMOS 9HP process were verified to simulate accurately across a temperature range of -55°C—125°C. However, it was desirable to verify that the ADC would work at cryogenic temperature ranges (down to -196°C) before the circuits were taped out. For this reason, it was necessary to create device models that would accurately represent the operation of the circuits at cryogenic temperatures. To achieve this goal the MSCAD lab at the University of Arkansas worked with Dr. John Cressler's lab at Georgia Tech to supplement the included device models of the 9HP process design kit with several cryogenic models.

Due to the device modeling effort on a previous project, the team at Georgia Tech had already developed cryogenic PFET and NFET models for the IBM 9SF process. Since the 9SF process is similar to the 9HP process, it was decided to see if the already developed models

would work for the transistors in the 9HP design kit. Thus, the input characteristics for the devices in both processes were compared as shown in Figure 2.1.

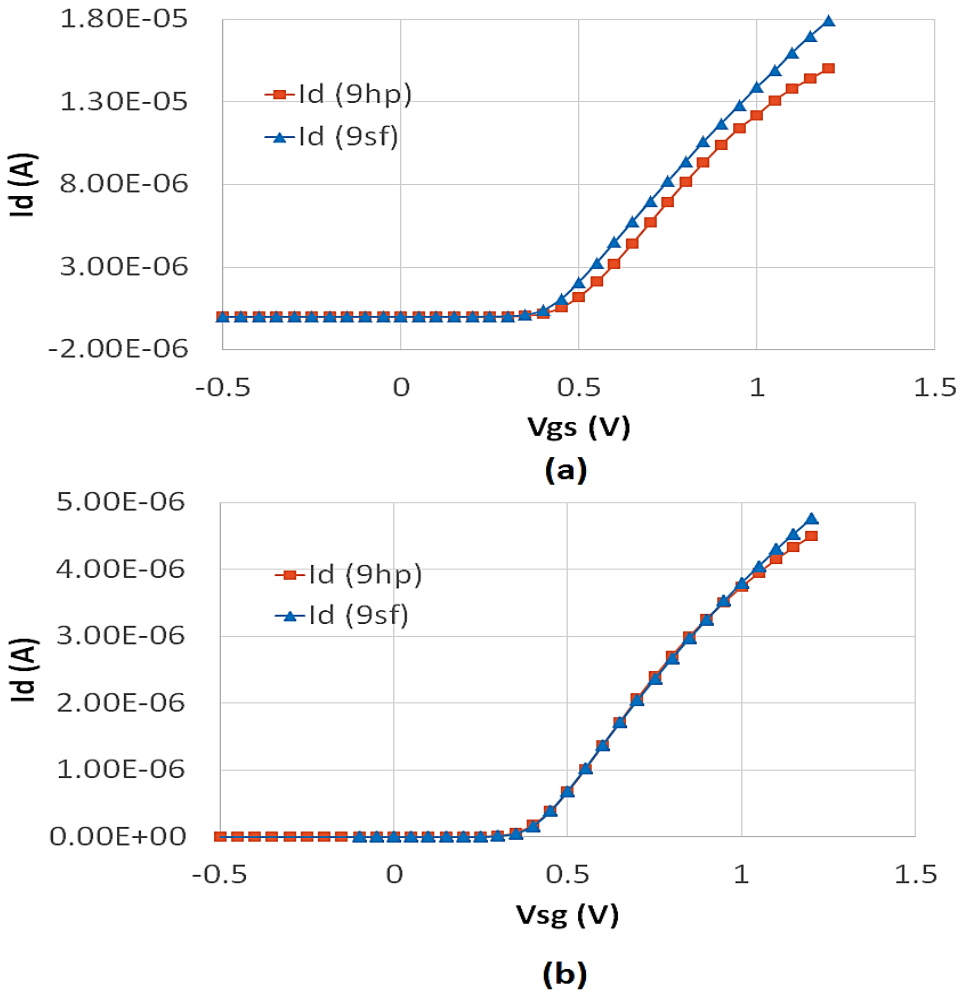


Figure 2.1. Comparison of 9HP and 9SF threshold voltage for (a) NFET and (b) PFET devices.

Since the transistor characteristics were very similar it was decided to simply reuse the cryogenic models that had been previously developed for the 9SF process.

The next device that was modeled was the NPN HBT. The team at Georgia Tech had previously measured the performance of the HBT device at cryogenic temperatures. They provided the data to the MSCAD lab at the University of Arkansas where it was used to develop

a cryogenic model for the HBT. A comparison of the measured data provided by Georgia Tech versus the simulated HBT model at -196 °C is shown in Figure 2.2.

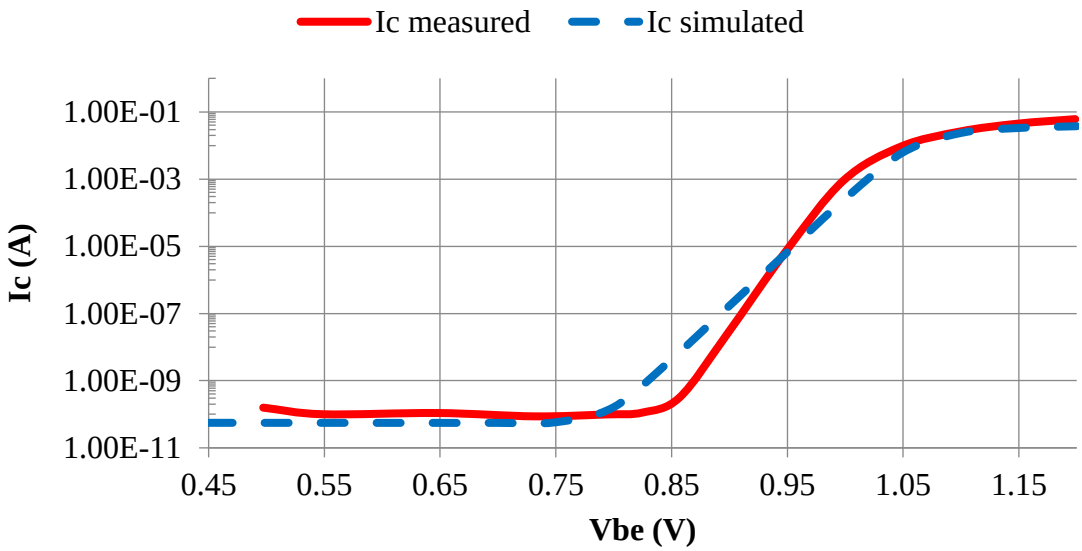


Figure 2.2. Graph of measured and simulated cryogenic (-196°C) 9HP HBT device DC sweep.

2.4 Selecting a Comparator Topology

After narrowing down the desired specifications that would be necessary to achieve the comparator's goals in the system, the next step was to compare several different comparator topologies and balance the pros and cons for each choice.

2.4.1 Open Loop Operational Amplifier

One of the oldest ways to compare two voltages is to simply use an operational amplifier in the open-loop configuration. Op amps are characterized by having very large open loop voltage gain as shown in Equation 2.3 [10]:

$$V_{out} = A_V * (V_{INP} - V_{INM}) \qquad [\ 2.3\ ]$$

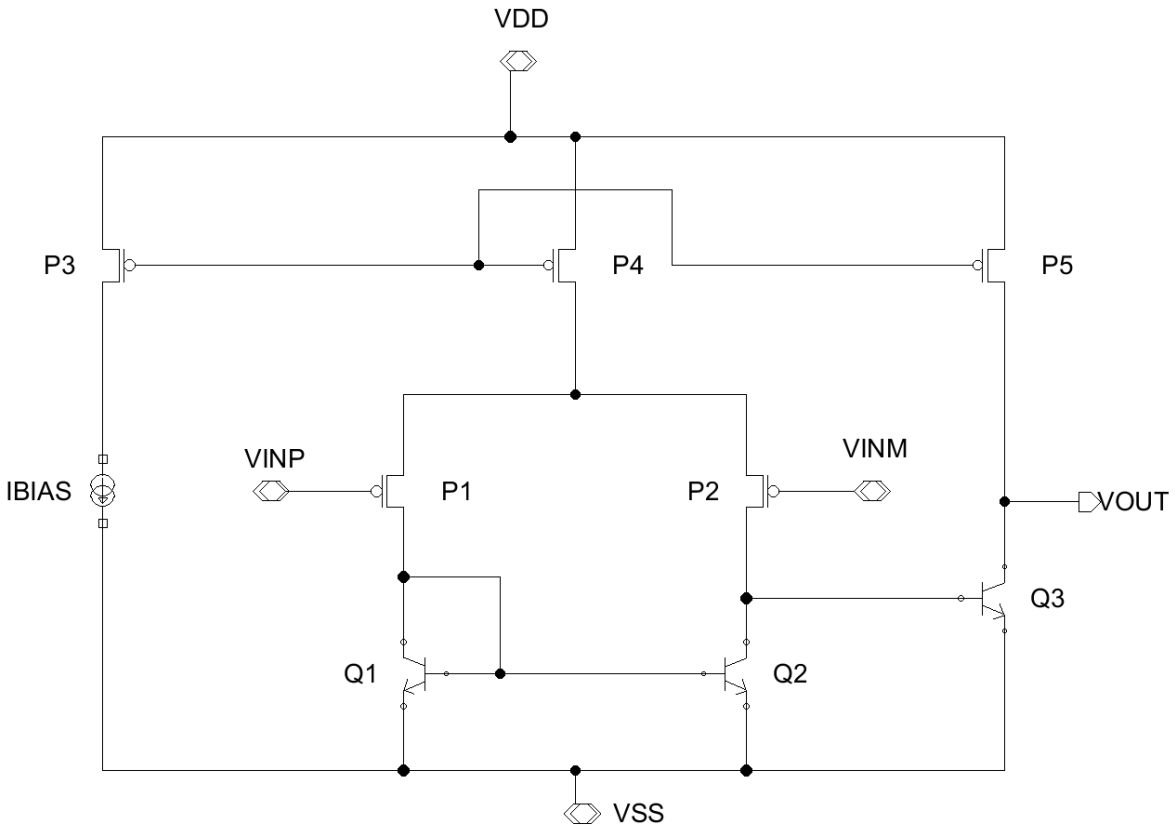


Figure 2.3. Open loop op amp topology used as comparator.

When the non-inverting input is larger than the inverting input, the output will be driven to the positive rail. When the inverting input is larger than the non-inverting input, the output of the op amp is driven to the most negative rail. This is the behavior that is expected of a comparator.

However, the downsides of using an operational amplifier outweigh the benefits. Op amps in comparator configuration typically will demonstrate slower speeds and less stability than a comparator that is purposefully designed for comparing analog voltages. This is due to the fact that op amps are meant to be operated in closed loop configurations where, due to feedback, the various stages of the circuit do not become oversaturated [11]. When the open-loop op amp is driven with too much differential voltage, the recovery time will be much slower when compared to a circuit with feedback.

2.4.2 Clocked Regenerative Feedback Comparator

One comparator design that might be considered for use in a high-speed system is a clocked comparator. An example of a clocked comparator from [12] is shown in Figure 2.4.

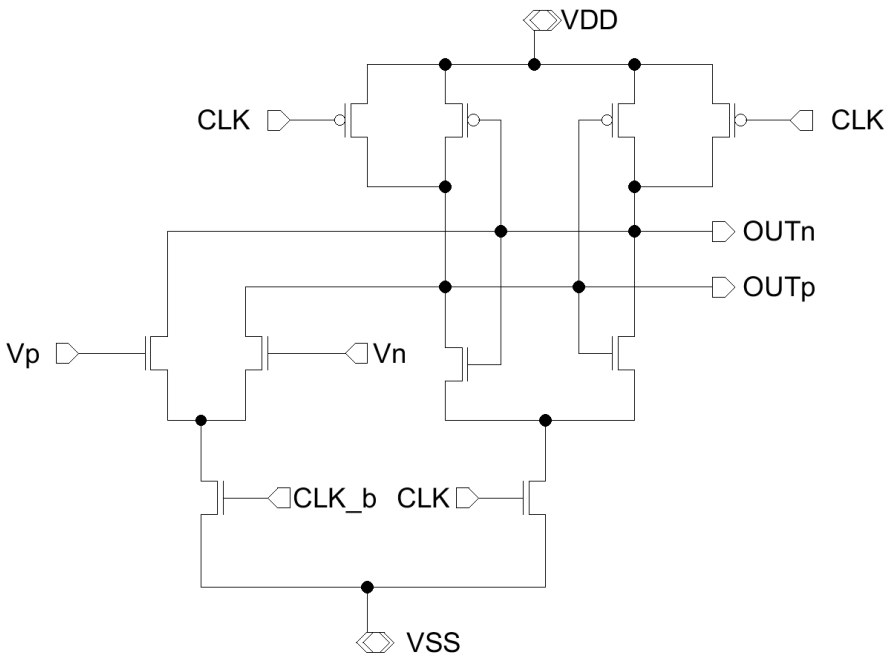


Figure 2.4. Example of clocked comparator.

The way this comparator works is by using the clock signal to operate two distinct stages: the amplification stage and the regenerative stage. When the “CLK” signal is in the low state the comparator is in the amplification stage and the difference in voltage between “Vp” and “Vn” is amplified and fed to the regenerative stage. Once the “CLK” signal turns to the high state then the regenerative stage latches to the amplified differential voltage from the amplification stage.

Some of the benefits of this comparator topology are that it is designed for use in low supply voltage processes and has very low propagation delay due to the regenerative stage (this particular topology demonstrated operating frequencies up to 7 GHz [12]) . However, the design of the SAR ADC was to be completely asynchronous and therefore the comparator should be

able to run in continuous time without a timed clock signal. Therefore, any comparator topology that uses any kind of timing signals for sampling or latching was incompatible with the design goals of the project. Thus, this topology was ruled out.

2.4.3 Dynamic Latched Feedback Comparator

The next topology was a latched comparator that uses positive feedback to increase the gain of the input stage and thus reduce the systematic offset voltage [5]. This topology also had the advantage of being used in a successful SiGe comparator that was designed and tested in a previous extreme environment project [5]. The difference between the latch comparator input of Figure 2.5 and the dynamic latched comparator of [5] is that instead of using NFETs for the dynamic latch, this version of the latch will use HBT devices in order to meet the specification of only using PFET and HBT devices in the analog portion of the comparator.

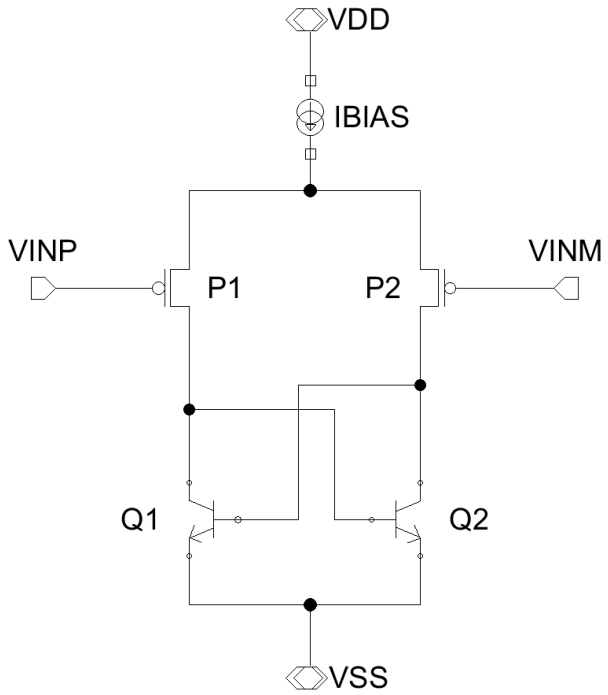


Figure 2.5. PFET input with latched HBT load.

To continue with a similar style of topology as the previous SiGe comparator, the latched HBT load input stage was also paired with a push-pull stage that helps to source enough current to drive the output digital buffers. Once again, the NFET devices from [5] were replaced with HBT devices as shown in Figure 2.6.

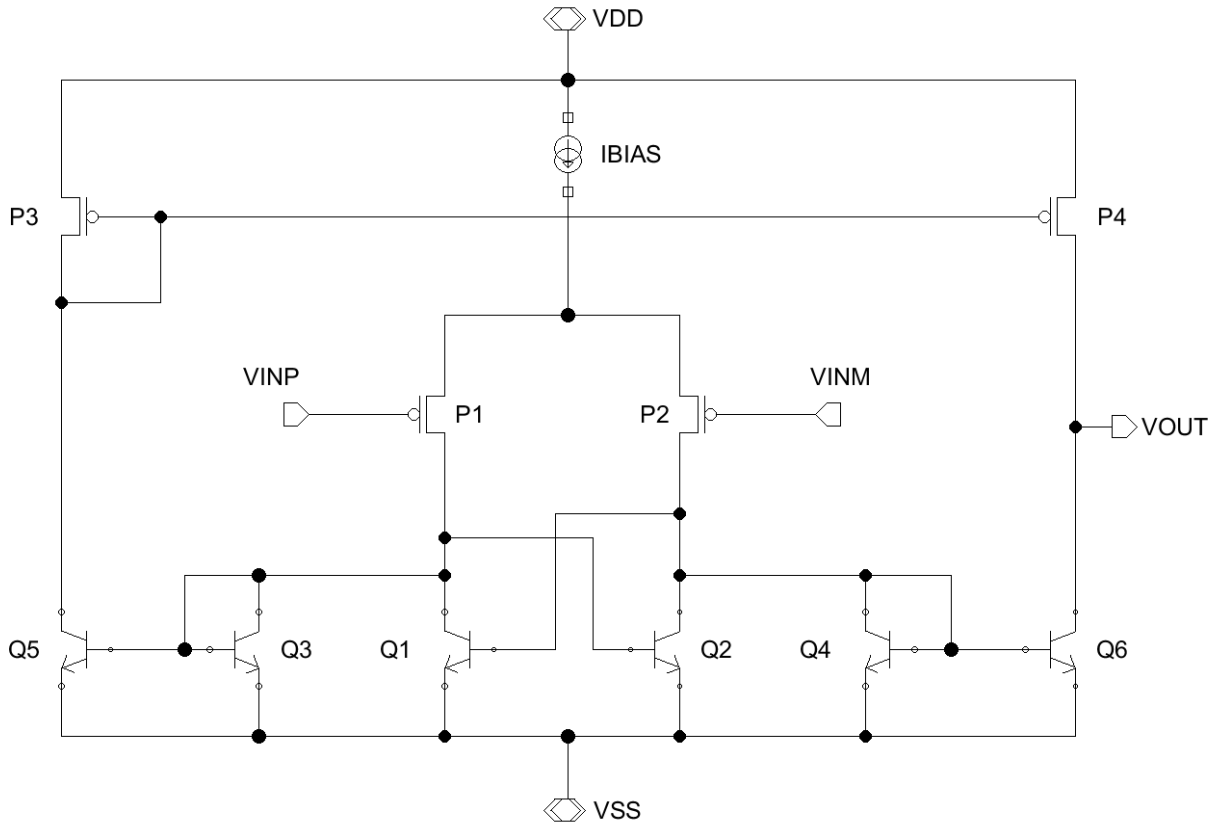


Figure 2.6. Dynamic latched comparator with push-pull output stage.

Chapter 3 - Designing the Comparator

Once the topology was chosen for the comparator, the next step was to design the comparator one stage at a time. At this phase of development, it was decided that there would be at least three stages of the comparator. These stages consisted of an input stage, a positive latch stage, and a digital buffer stage. In addition to these three main stages of the comparator it was also necessary to design a current mirror to supply the bias current to the comparator. Finally, since this comparator design should work independently of any external reference or support circuitry, it was necessary to design a current reference that could be used to bias the comparator.

3.1 Designing the Input Stage

The first stage of the comparator that was designed was the cross-coupled regenerative latch circuit. This is the stage where the input voltages would be received by the comparator and where the initial comparison happens. For this reason, it was important to design this stage so that there was as little systematic offset as possible to ensure that the comparator can resolve an output for input voltages that have a very small difference between them.

The selection for the bias current was chosen based on a value that would not increase the drain voltages of the PMOS pair too high to keep the input pair in saturation but at the same time would still allow the HBT devices to provide enough current gain. In addition to this, the effects of temperature on the collector voltage of the HBT had to be kept in mind as well.

3.1.1 Gain Considerations

To find a suitable bias current for the input stage, the HBT was simulated as shown in Figure 3.1.

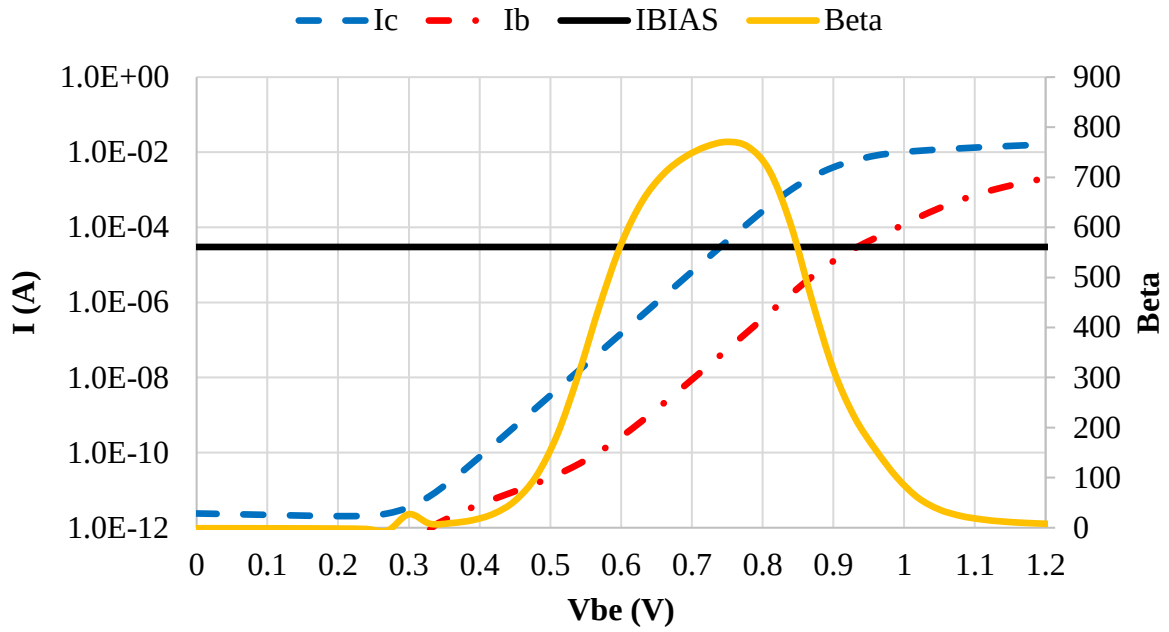


Figure 3.1. Gummel plot for NPN HBT device at room temperature.

The beta value is defined as the current gain of the HBT device, i.e. output current divided by input current. The beta value is thus calculated by dividing the collector current, $I_{C,}$ by the base current, I_B. As shown in Figure 3.1 the maximum gain occurs at a V_{BE} of about 0.75 V.

If a bias current for the input stage is chosen as 30 µA, then the beta value is about the maximum of 800 and the V_{BE} value needed is only about 0.73 V at room temperature. This V_{BE} value is very important because due to the cross-coupled HBT devices, as the V_{BE} goes higher, the headroom for the rest of the circuitry in the leg decreases. Since the supply voltage for this process is 1.2 V, the headroom is only 0.45 V at room temperature. This effect is explored in more detail in the next section.

3.1.2 Temperature Considerations

The next consideration for the bias current is the behavior of the NPN HBT devices across temperature since the goal for this comparator was to work from -196°C to 125°C. Because the 9HP process has a nominal supply voltage of 1.2 V a bias current must be chosen that will allow

the HBT devices to work across the temperature range and keep the rest of the circuitry working within the allotted voltage headroom.

The amount of voltage headroom allowed for the input PFETs and the bias circuitry is based on the selected input topology for the comparator. The HBT devices are used as a cross-coupled active load so as the collector current increases so does the corresponding base to emitter voltage, as shown in Figure 3.1.

Using the test results provided by Dr. John Cressler and his team at Georgia Tech, a comparison was made between the HBT at room temperature (27°C) and at cryogenic temperature (-196°C). The results are shown in Figure 3.2.

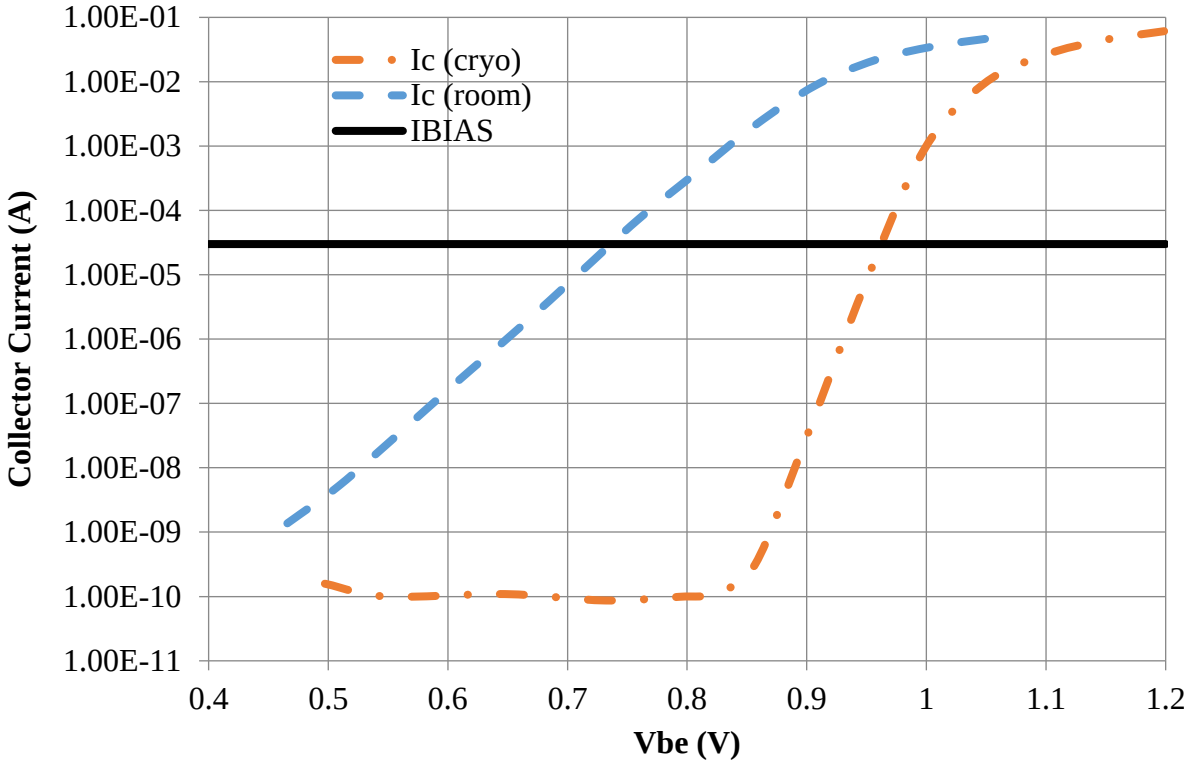


Figure 3.2. Measured results of NPN HBT at cryogenic and room temperature.

Figure 3.2 shows that at cryogenic temperatures there is a large difference in operating voltage on the HBT device. At a collector current of 30 µA the base to emitter voltage is

approximately 0.73 V at room temperature and 0.96 V at cryogenic temperature. This means that if the bias current was chosen to be 30 µA then the headroom would vary from 0.47 V to 0.24 V for the input PFETs and the bias current generator. More simulations would be necessary to make sure that this is a valid choice.

3.1.3 Sizing the Input Pair

Assuming the chosen bias current of 30 µA was valid and would work across the temperature range, the next step in designing the comparator was choosing sizes for the input pair. First, the length of the input pair was chosen to be 0.2 µm, which is twice the minimum length, as per the recommendation of Dr. Cressler. Then, the input pair width was chosen and simulated to find a suitable value for the width. The initial sizes of the input transistors were thus chosen to be a width of 7.04 µm and length of 0.2 µm as shown in Figure 3.3. Since the HBT devices are quite large, they were initially sized at close to their minimum size, which is a length of 0.6 µm and a width of 10 µm. Due to the 9HP process design rules, the width of 10 µm was unchangeable and thus was not a usable parameter in the circuit design. The input stage with the device sizes is shown in Figure 3.3.

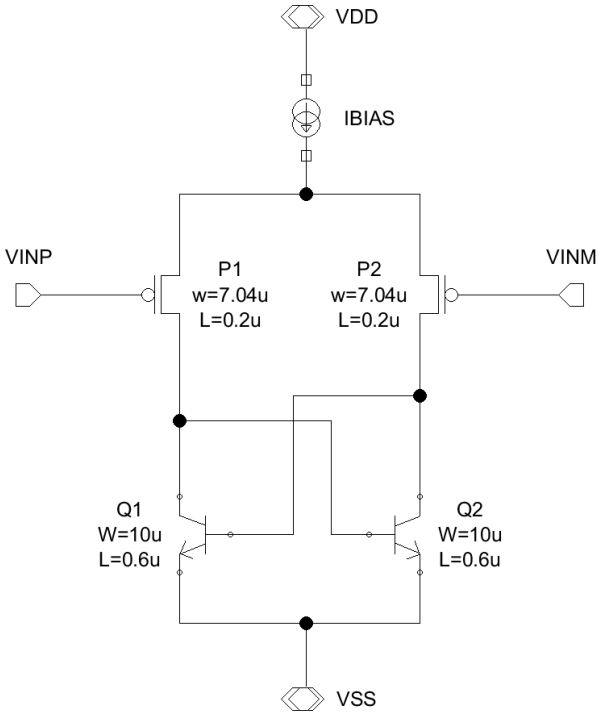


Figure 3.3. First design of input stage of comparator.

Before beginning the layout of the comparator, it was decided to increase the sizes of the input pair so that the effects of any potential process defects (and therefore mismatch between the comparator inputs) would have a lessened impact on the performance of the comparator. Thus, the input pair's width and length were doubled as shown in Figure 3.4. By doubling both the width and the length of the input pair the bias current requirements of the input stage was kept the same since the ratio of width to length did not change.

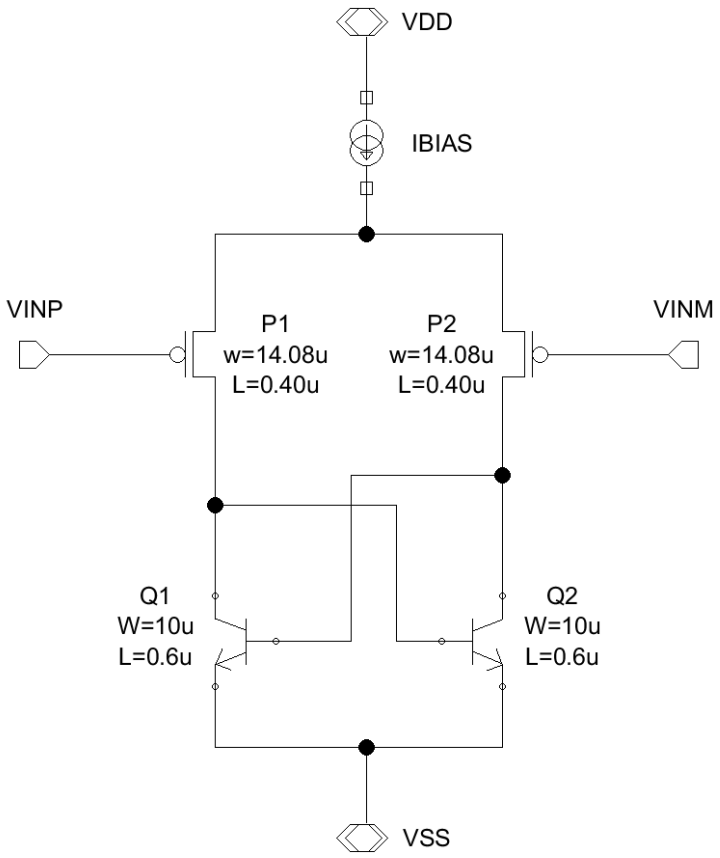


Figure 3.4. Final size of input PFET transistors.

3.2 Designing the Push-Pull Stage

After sizing the input stage, the subsequent step was to design the next gain stage: the push-pull stage. Similar to the push-pull stage demonstrated in a previous SiGe comparator [5] this stage is designed to mirror the current changes in the input stage of the comparator. The push-pull stage of the comparator is shown in Figure 3.5.

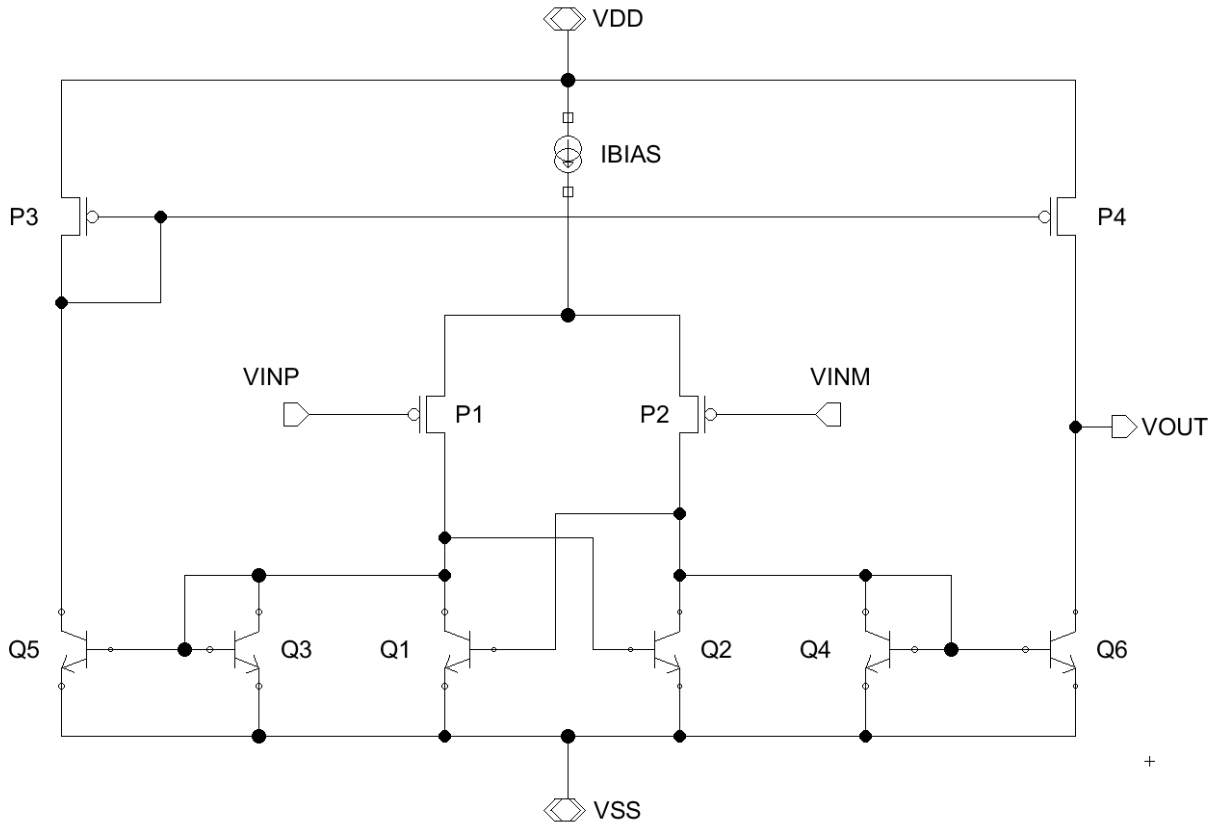


Figure 3.5. Input stage with push-pull current mirror output.

3.2.1 Operation of the Push-Pull Stage

The way this stage works is by mirroring the cross-coupled HBT devices of the input stage into a leg that will either sink or source current depending on the inputs to the comparator. The mirroring devices are Q3 and Q4 which mirror the current that is passing through Q2 and Q1, respectively. The output of Q3 and Q4 is then mirrored to the push-pull stage of P3/Q5 and P4/Q6, which as the name suggests will either push or pull (i.e. source or sink) current depending on what Q3 and Q4 are doing.

For example, when VINP > VINM the current through Q1 increases, which decreases the amount of IBIAS current that passes through Q2. The device Q4 mirrors this increase in current. This translates to a mirroring of the increased current to the leg of P4 and Q6. This change is

reflected at the voltage VOUT which is pulled closer to ground since the device Q6 is being turned on and thus sinking current.

While those changes are occurring in devices Q1/Q4/Q6, the device Q3 mirrors the lower current in Q2 which in turn begins to turn off the device Q5. The device Q5 will begin to turn off the gate-drain connected transistor P3 (in diode configuration). The drain (and thus the gate) of device P3 moves closer to the supply. Since P3 and P4 share a gate connection, P3 turning off will begin to turn off P4 which will hasten the transition of the P4/Q6 branch to sinking current.

When VINP < VINM, the trends in the current and voltage changes are the opposite of what was described for VINP > VINM. The overall effect of the push-pull stage is that when VINP > VINM, VOUT trends toward VSS and when VINP < VINM the VOUT node will trend towards VDD. Since this behavior is the opposite of what is expected for a comparator, the VOUT signal will pass through a digital inverter.

A figure illustrating the trends of the currents and voltages in the comparator when VINP > VINM is shown in Figure 3.6. The small arrows indicate trends in currents, not the direction of the current itself. The large arrow outline indicates trends in the voltages.

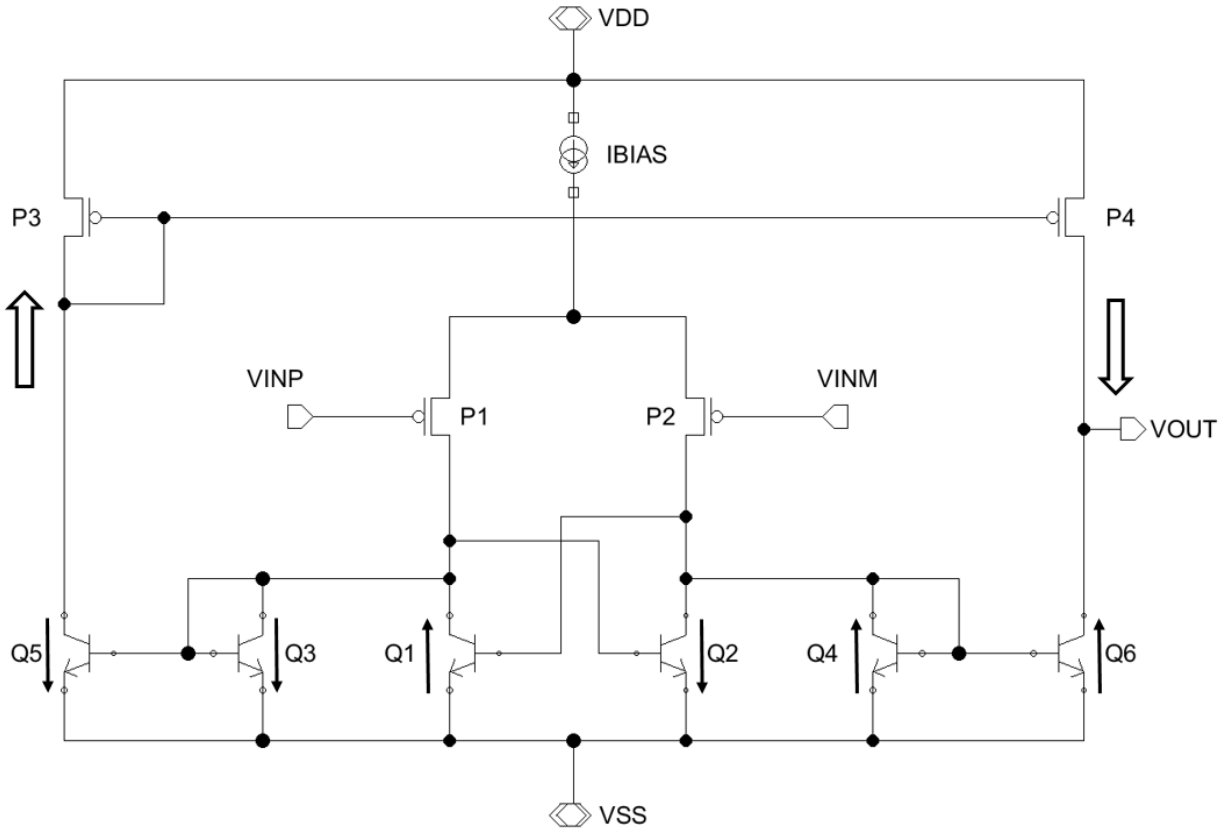
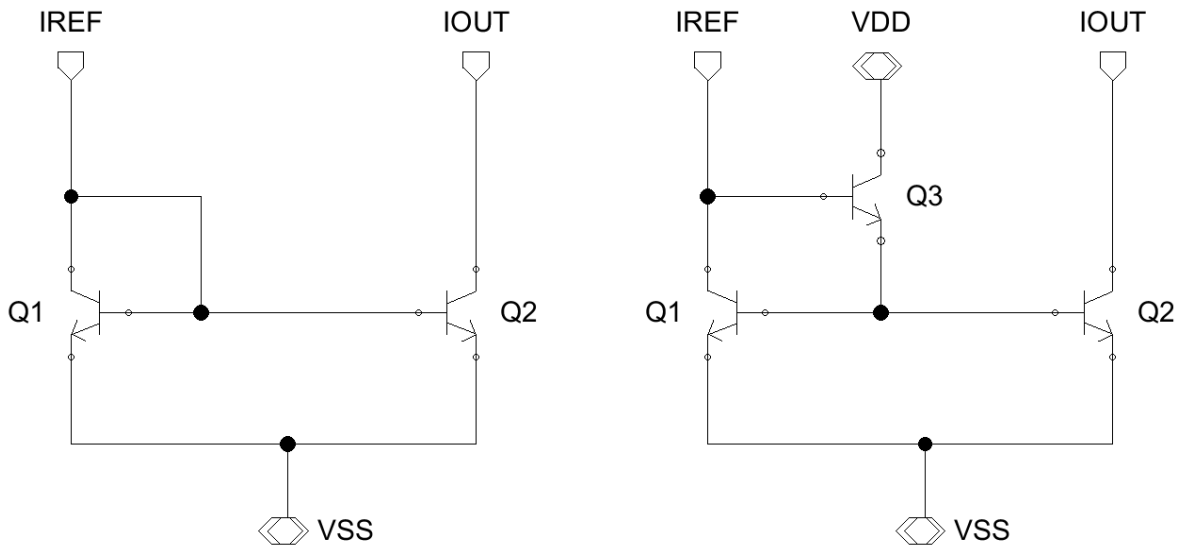


Figure 3.6. Current (small arrows) and voltage (large arrows) trends in the comparator for when VINP > VINM.

3.2.2 Extra Considerations for Creating the Push-Pull Stage

Normally in a situation where a bipolar transistor is used in a current mirror it would be necessary to include some sort of compensation to reduce the reliance of the current mirror output on the gain of the device [10]. One form of this compensation is a base-current compensation as shown in Figure 3.7b.



(a) **(b)**

Figure 3.7. Comparison of (a) simple current mirror and (b) base-current compensated current mirror [13].

Normally the output of the current mirror is based on the simple equation:

$$I_{OUT} = I_{REF} \frac{1}{1 + 2/\beta} \qquad [\ 3.1\ ]$$

However, with the inclusion of the additional transistor Q3 the output current equation becomes:

$$I_{OUT} = I_{REF} \frac{1}{1 + 2/\beta^2} \qquad [\ 3.2\ ]$$

The output of the compensated current mirror therefore has a much smaller dependence on the current gain (the β value) of the NPN BJT devices as compared to the simple current mirror. However, the NPN HBT devices that are used in this process have a much higher current gain than the typical BJT devices. As shown in Figure 3.1 the peak current gain of the HBT device used in this design is almost 800. This high gain value creates the opportunity to use simple current mirrors with high accuracy.

3.2.3 Sizing the Devices

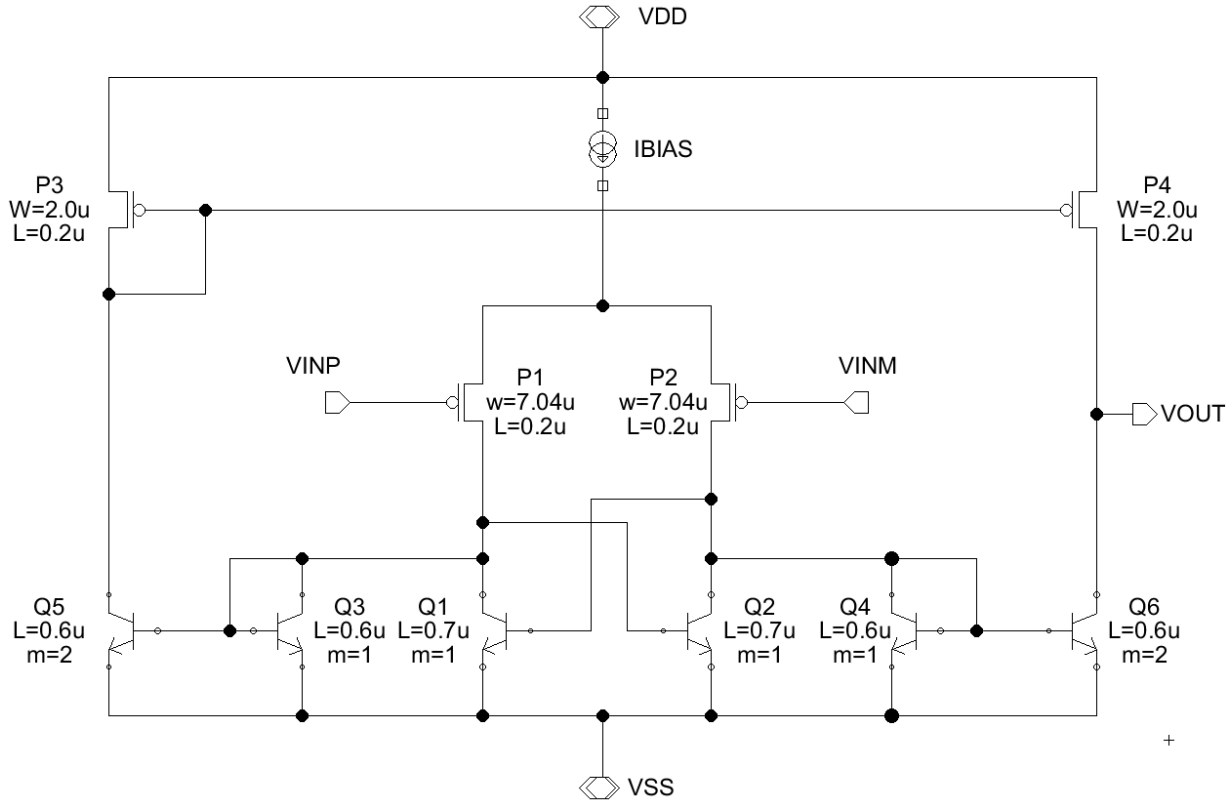


Figure 3.8. Correctly sized input stage of comparator with current mirrors.

As shown in Figure 3.8 the devices Q5 and Q6 were given an extra device to multiply the current that they are mirroring. Thus, instead of mirroring a flat 1:1 ratio the push-pull branch outputs a 2:1 ratio compared to the input stage. This helps to drive the digital inverters and increases the speed of the output transitions.

In addition to the extra device for Q5 and Q6 the length of Q1 and Q2 was increased slightly to 0.7 µm. This provided a slightly better ratio for the current mirror and provided better results for the offset in simulation.

The sizes of P3 and P4 were chosen based on simulations for the push-pull stage to choose a correct ratio that would provide the correct amount of feedback for the mirroring BJTs. The sizes went through several iterations until the correct behavior was displayed.

3.2.4 Differential Output for the Comparator

Because the output of the comparator will be the input for asynchronous digital logic circuits which utilize null convention logic (NCL), it was decided that the push-pull stage should be duplicated so that there is a differential output. NCL is defined as "a symbolically complete logic circuit that would have no time relationships at all and would be completely insensitive to the propagation delays among its component elements" [14]. NCL works by using dual rail logic to create three valid states [15]. These states are described in Table 3.1.

Table 3.1. NCL output states.

	RAIL1 = 0	**RAIL1 = 1**
RAIL0 = 0	NULL	1
RAIL0 = 1	0	INVALID

To better facilitate the integration of the comparator block into the ADC system the push-pull stage was duplicated to have the inverted output as well as the regular output. All the sizes were kept the same for this duplicate branch and the new topology is shown in Figure 3.9.

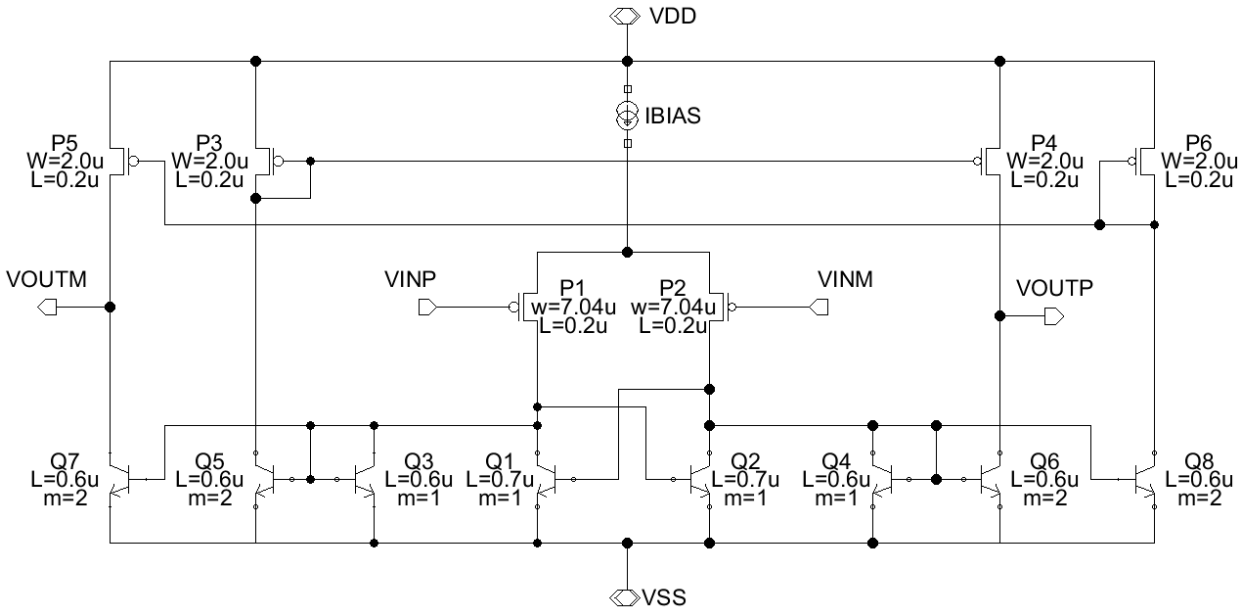


Figure 3.9. Comparator topology with differential output.

3.3 Adding Third Stage Differential Amplifier

After simulating the comparator with all the pieces designed so far it was noticed that at low input overdrive voltages ($\mathrm{VINP} - \mathrm{VINM} < 5\ \mathrm{mV}$) the output would not always reach a decision state. Sometimes it would begin to reach one decision state and then halfway through the output changing it would switch to the opposite state. To ensure that the comparator would not register any false outputs at low overdrive voltages it was decided to add a third stage to increase the gain at the cost of propagation delay. Since the topology of the comparator already had differential output it was possible to leverage the independent output branches to arrive at a quicker decision for both outputs.

3.3.1 Choices for Differential Amplifier Topology

There were a couple of topology choices that were looked at for the third stage of the comparator. The first and simplest choice was a self-biasing differential amplifier. An example of this topology is shown in Figure 3.10.

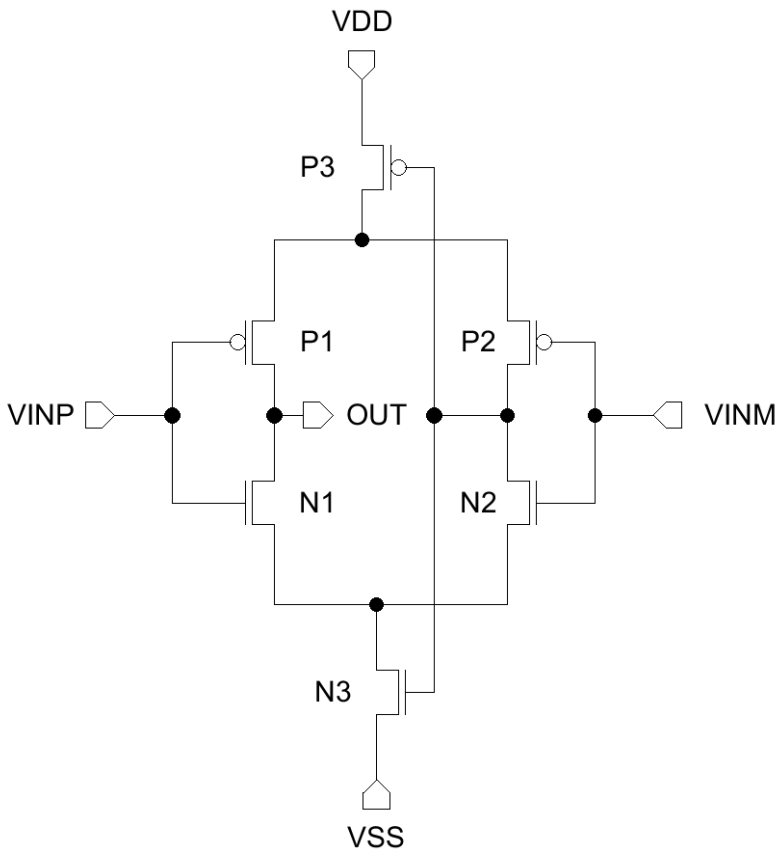


Figure 3.10. Self-biasing differential amplifier topology.

The obvious advantage of this choice for the third output stage is that it does not require an external bias current. It also has high gain with nearly infinite input resistance [16]. However, the disadvantage of this topology is that it would need to use NFET devices instead of the HBT devices. This would defeat the stated design goal of only using PFET and HBT devices for the mixed-signal stages of the comparator so this topology was not used for the third stage.

Another topology that was considered for the third gain stage was a simple long-tailed pair with a current-mirror load as shown in Figure 3.11. Obviously, this topology would need a bias current but it can easily be arranged by adding another output branch from the current mirror that will be used for the input of the comparator stage.

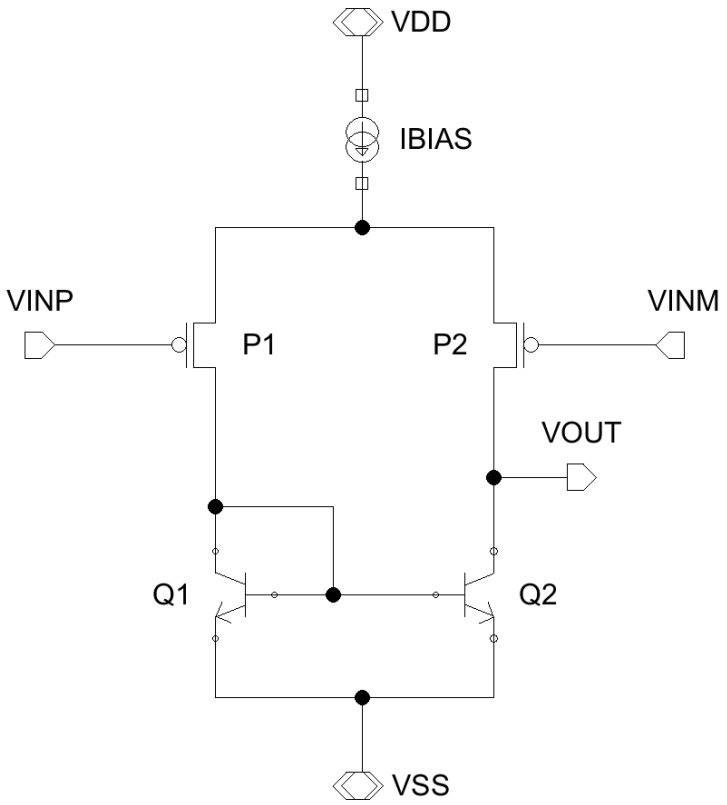


Figure 3.11. Long-tailed pair differential amplifier topology.

After considering both candidates for the third stage differential amplifier, it was decided to select the long-tailed pair as the choice for the third stage of the comparator. Some of the reasons for selecting it was because it was quick and simple to design and since it was possible to use the HBT devices for the current-mirror load it would stay within the design paradigm of only using PFET and HBT devices for the mixed-signal aspect of the design.

3.3.2 Sizing the Devices and Choosing a Bias Current

The first step in designing the differential amplifiers was to size the input devices. Since the inputs to these differential amplifiers can be expected to have a large overdrive voltage, it is not necessary to size these devices to provide a large amount of gain. The main consideration is to simply use as little bias current as possible to keep added power consumption of this stage to a minimum. For this reason, the devices were sized as shown in Figure 3.12 below.

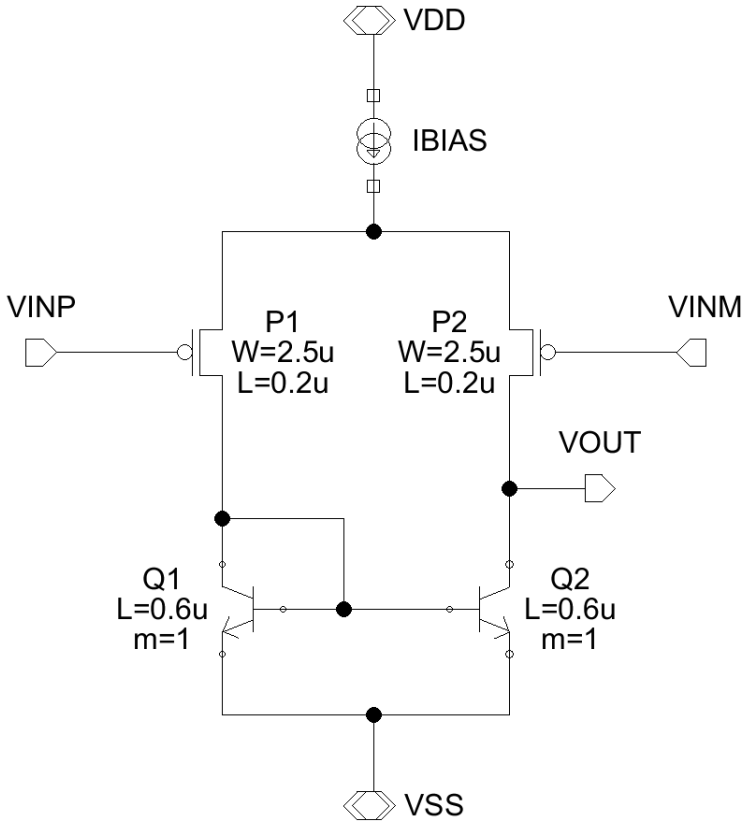


Figure 3.12. Initial sizes of differential amplifier for third stage of comparator.

To find a suitable bias current to provide to the differential amplifier, a series of simulations were run to give an idea of the propagation delay of this stage. The results of this sweep are shown in Figure 3.13.

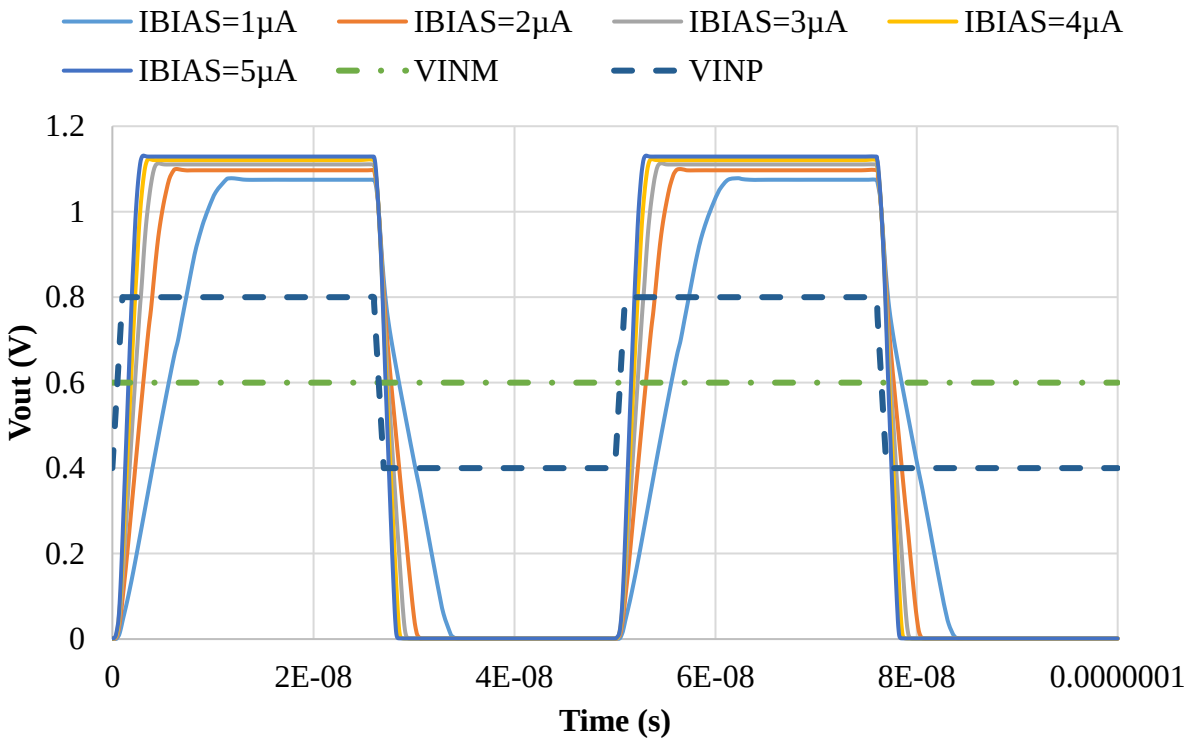


Figure 3.13. Sweep of bias currents for differential amplifier.

As shown in the simulation sweep of the bias current, the gain in the diff amp is very low for the 1 µA bias current. However, as the bias current is increased the gain of the differential amplifier increases. Using a bias current of either 4 µA or 5 µA would work with this topology. However, since the current mirror would need to generate the bias current for both the differential amplifier and the input to the comparator it was decided that 5 µA would work better since it is a factor of 30 µA.

3.3.4 Simulating the third stage with the Rest of the Comparator

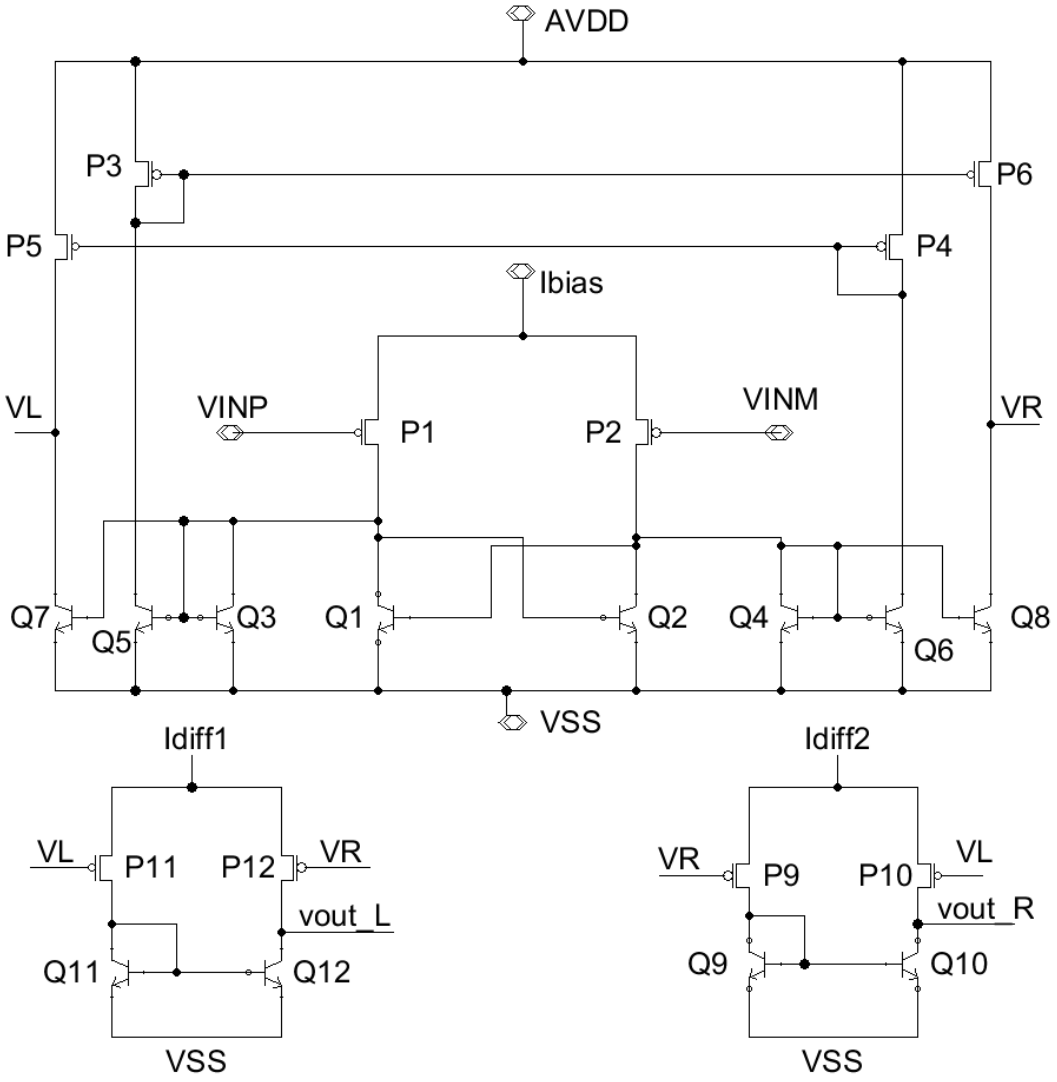
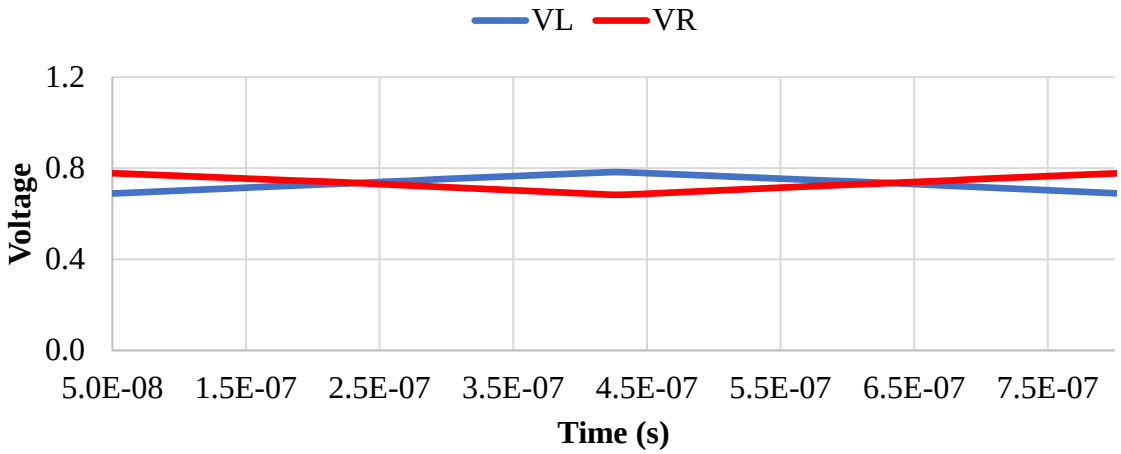
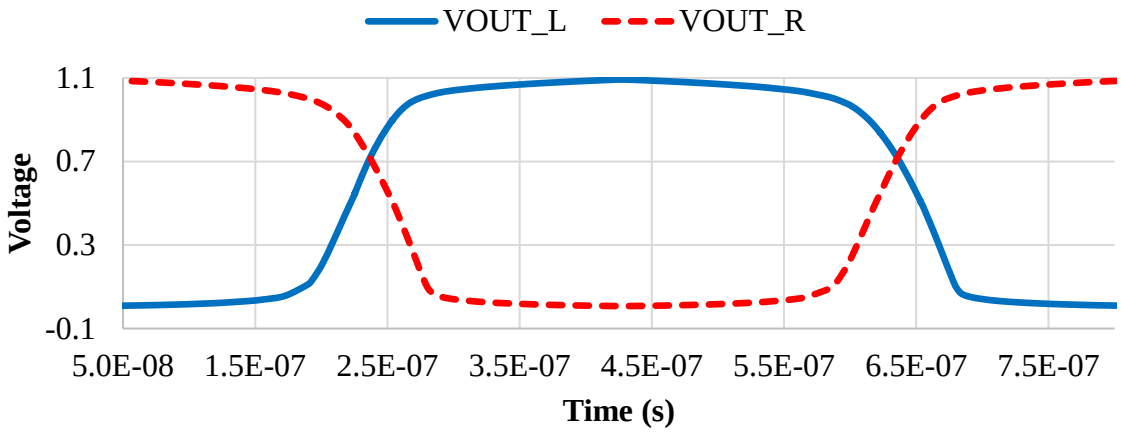


Figure 3.14. Comparator with all analog stages completed.

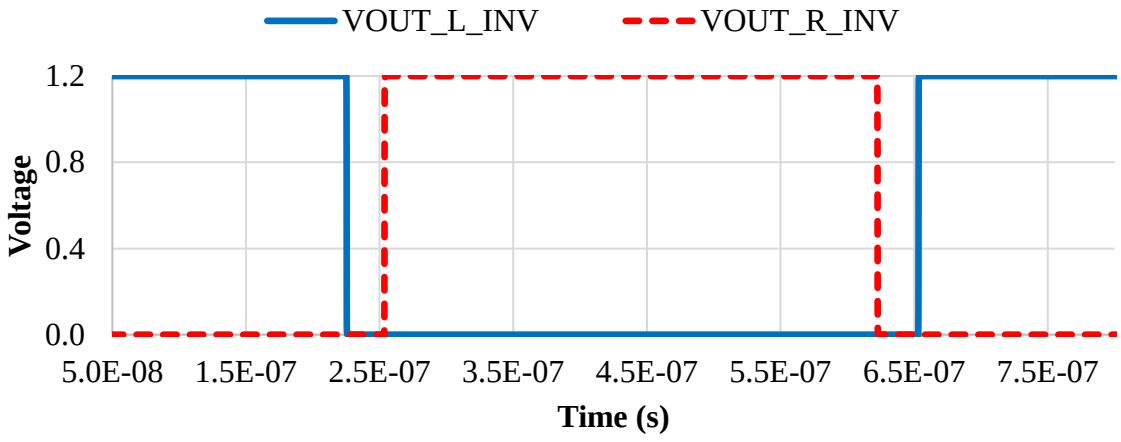
The comparator with all three stages is shown in Figure 3.14. To make sure that the design of the input stage was suitable for use in the comparator, all three stages of the comparator were simulated together with ideal bias sources. The VINM input was given a 0.35 V input and the VINP was given a triangular wave input from 0.349 V to 0.351 V. The outputs of the push-pull stage (VL/VR), third stage diff amp (VOUT_L/VOUT_R), and the digital inverters (VOUT_L_INV/VOUT_R_INV) are shown in Figure 3.15.



(a)



(b)



(c)

Figure 3.15. Simulation results with differential amplifier in comparator: (a) push-pull output, (b) differential amplifier output, and (c) buffered output.

Chapter 4 - Designing the Bias Circuits

Once the design of the core three stages was complete the next step was to design the circuits biasing for the analog circuits. This includes a current generator and a current mirror to transfer the bias current to the comparator as well as the two differential amplifiers.

4.1 Designing the Current Source

The main consideration for the current source for the comparator is that it could not have an external precise voltage source. This design decision was made to keep with the spirit of a completely independent ADC circuit that does not need any external support circuitry. Therefore, the circuit that was designed must generate any necessary bias voltages internally. Additionally, it must continue to supply enough bias current for the comparator to operate even at -196^{o}C.

4.1.1 Zero Temperature Coefficient Current Source

The first circuit that was checked for efficacy was the zero-temperature coefficient (ZTC) current source. The zero-temperature coefficient of a MOSFET is defined as “the bias point when the transistor has mutual compensation of mobility and threshold voltage temperature effects” [17]. This effect is possible in a MOSFET because of the interaction of the threshold voltage and the charge carrier mobility on the saturation current as shown in Equation 4.1.

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \qquad [\ 4.1\ ]$$

As described in [18], as the temperature of a MOSFET in saturation increases, the threshold voltage and charge carrier mobility both decrease. However, the decrease in threshold voltage increases the drain current and the decrease in charge carrier mobility decreases the drain current. Thus, the drain current can be held at a steady value across temperature if the MOSFET

can be biased so that the effects of the threshold voltage and the charge carrier mobility offset each other.

Conversely, as the temperature decreases, the threshold voltage and charge carrier mobility both increase. This has the inverse effect as before where the higher threshold voltage decreases the drain current but the higher charge carrier mobility increases the drain current. A summary of these cause and effects is shown in Table 4.1.

Table 4.1. Effects of temperature changes on saturation current of MOSFET.

Temperature Change from Nominal		Effect on Threshold	Effect on Charge Mobility
$T \uparrow$	$\Longrightarrow$	$V_T \downarrow$	$\mu \downarrow$
$T \downarrow$	$\Longrightarrow$	$V_T \uparrow$	$\mu \uparrow$

Therefore, knowing how the MOSFET will behave with respect to the change in temperature makes it possible to find an appropriate bias point for a MOSFET where the changes in threshold voltage will cancel out the changes in charge mobility so that the saturation current will not change too much over temperature.

To find this ZTC point, a DC sweep was performed on a PFET device with a width of 10.0 µm and a length of 2.0 µm to find the ideal source-to-gate voltage. As shown in Figure 4.1 the currents do not exactly line up at any one point so the strategy was to choose a bias voltage that would give the closest output across all simulated temperature points. The ZTC point that was chosen for this PFET device in 9HP was 0.56 V. This generated a bias current very close to 30 µA for the simulated temperature range of -55^{o}C to 125^{o}C.

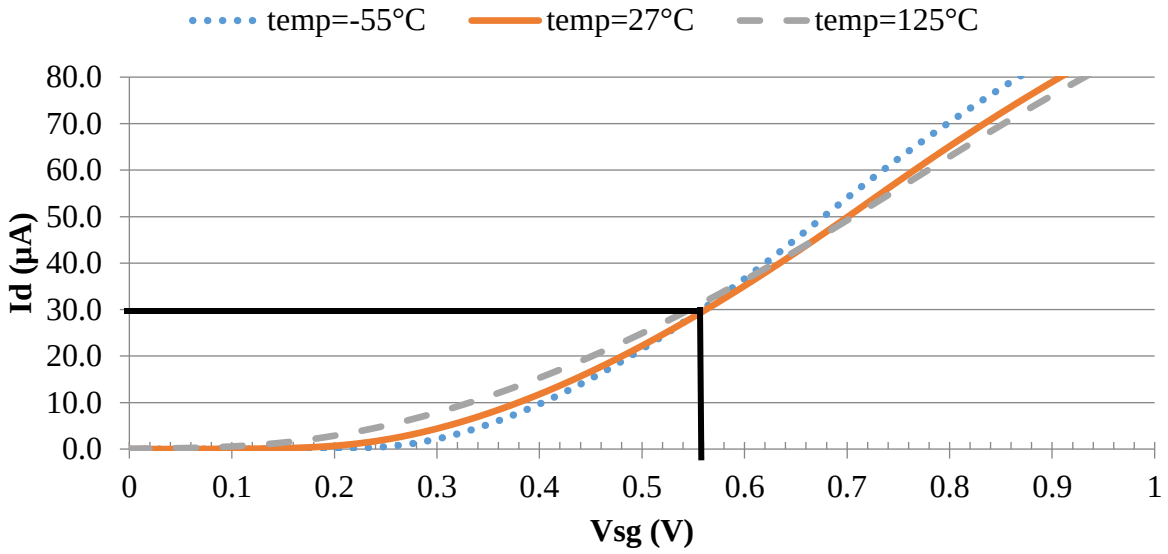


Figure 4.1. DC sweep of bias current generating transistor.

Now that the ZTC bias point of the current generating transistor is known, the next step is to design a circuit that will generate a stable voltage over temperature. The bias voltage generator was designed as described in [18]. This circuit is shown in Figure 4.2.

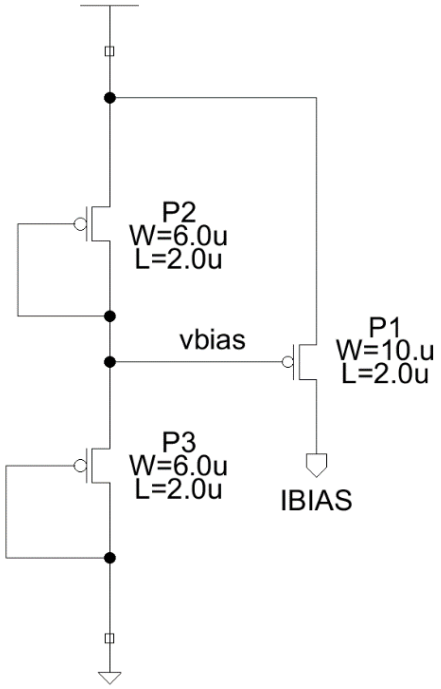


Figure 4.2. Current source biased with zero temperature coefficient voltage source.

The way this current source works is by biasing transistor P1 at a voltage point that will change over temperature to always output the same current. Transistors P2 and P3 are two diode-connected transistors. They were sized by sweeping the width of the transistors to find an output voltage that would match the ZTC point of the current generating transistor. The output of this ZTC current generator circuit is shown in Figure 4.3.

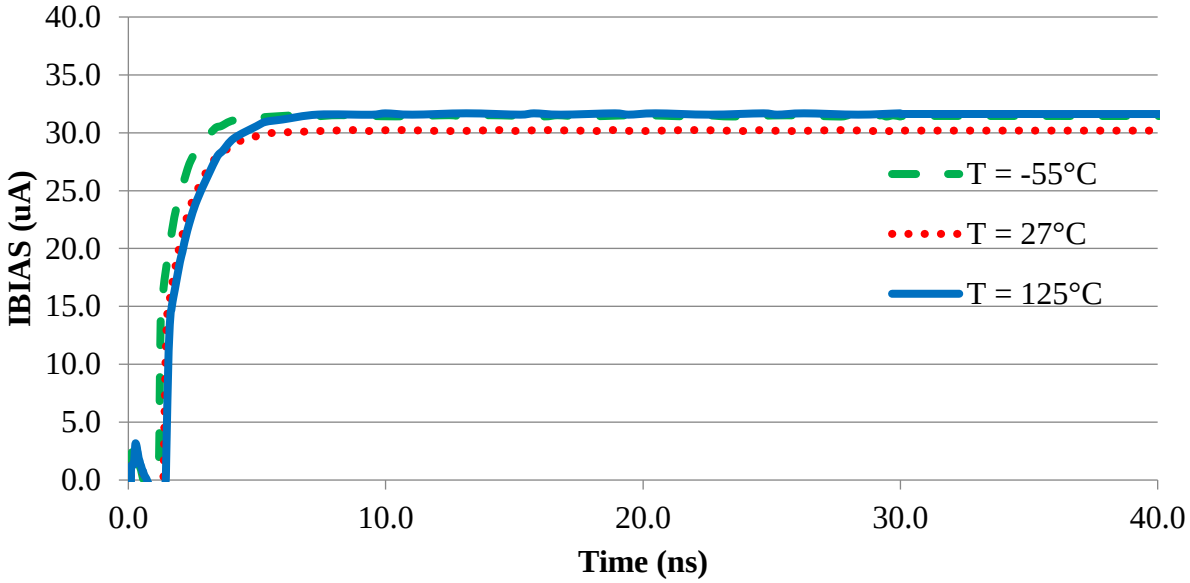


Figure 4.3. Transient simulation of ZTC current generator output.

The output was very close to the target over temperature. After a startup period of about 2 ns, the output current was within 2 µA of the target 30 µA through the entire temperature range of -55°C to 125°C.

Unfortunately, this method of generating a bias current had some issues at cryogenic temperature when combined with an HBT mirror to transfer the bias current to the comparator stages. At cryogenic temperatures, the voltage generated by P2 and P3 would not be able to offset the very low drain to source voltage of P1. This is because—as mentioned in previous chapters—the HBT device has a large collector to emitter voltage at cryogenic temperatures. This effect decreases the available voltage headroom for the bias current generating PFET. The

maximum output current at cryogenic temperature was only about 15 µA which was not enough bias current to run the comparator accurately.

4.1.2 Triple Cascade Current Source Biased with Digital Signal

Since it would not be feasible to design the circuitry to generate a stable enough voltage to bias a transistor, it was decided that the next order of action would be to instead rely on the common VSS node. Therefore, the biasing circuit was chosen to be a simple amplifier connected in the common-source configuration as shown in Figure 4.4, but the V_i voltage as simply VSS.

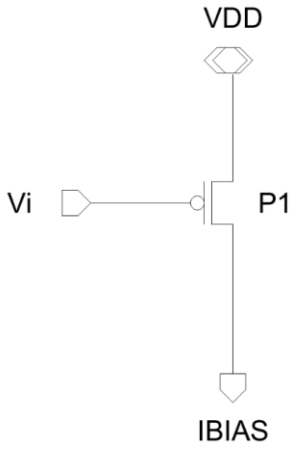


Figure 4.4. Basic current source transistor (common-source amplifier).

However, to use VSS to generate the correct bias current the transistor P1 would end up having a very small width and a large length. This would be undesirable because it would increase the chance that the negative effects of process variation would affect the width to length ratio of the current generating transistor. To have normal proportioned transistors that are larger to increase process reliability, several transistors were connected in a cascade configuration.

Having several cascaded transistors in series helps to increase the output resistance and therefore decrease the current generated. After simulating several sizes and quantities of transistors it was settled on four transistors as shown in Figure 4.5.

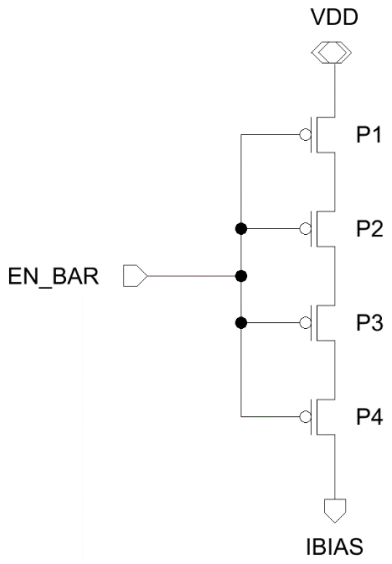


Figure 4.5. Four cascaded PMOS transistors biased with VSS voltage.

To transfer the initial bias current to the input stage and differential amplifiers, the generated IBIAS was put through a simple HBT current mirror. The full circuit with the device sizes is shown in Figure 4.6.

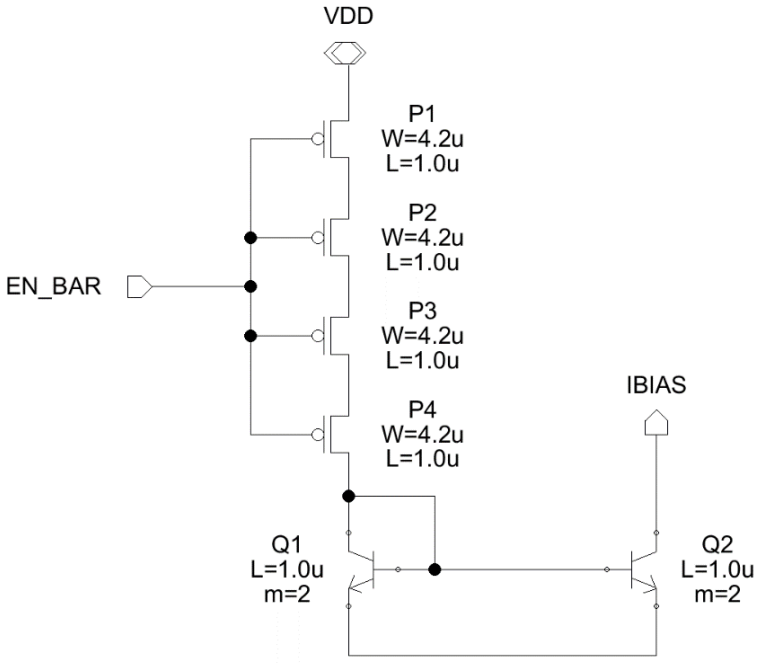


Figure 4.6. Current generator topology with device sizes.

Once a topology was chosen for the current source, it was necessary to simulate the circuit to verify that it operates as expected over the temperature range. The circuit was simulated at both the normal temperature range of operation (-55°C to 125°C) as well as at cryogenic temperature (-196°C) as shown in Figure 4.7.

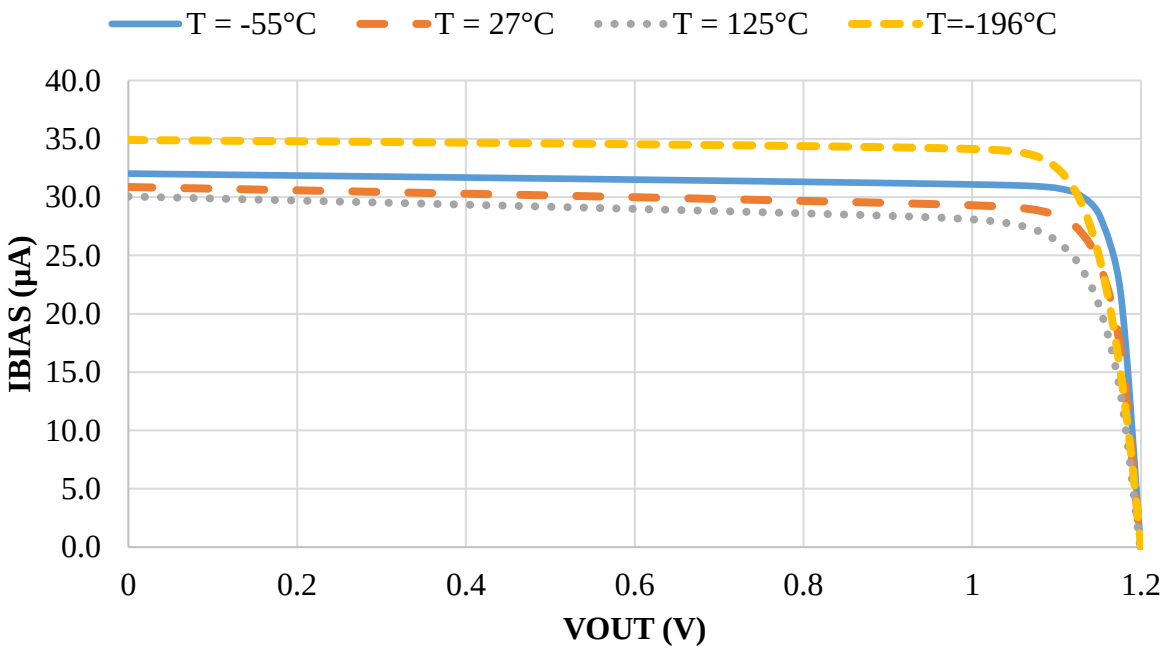


Figure 4.7. Current source simulation results at -196°C, -55°C, 27°C, and 125°C.

4.2 Designing the Current Mirror

After the output stage was completed for the comparator, the next step was to design the current mirror for the bias current. There were several different topologies that were considered for use in this stage. These topologies included a basic PMOS current mirror, a cascoded current mirror, and a wide swing current mirror.

4.2.1 Simple Current Mirror Topology

The first topology is the simple current mirror discussed previously. This current mirror has the advantage of requiring minimal voltage overhead allowing more headroom for the circuitry

below it. This is because for the PMOS device to remain in the linear cutoff region, the output voltage of the current mirror must stay within the following constraint:

$$V_{out} \leq V_{SG} - V_{tp} \qquad [\ 4.2\ ]$$

In Equation 4.2, V_{SG} is the source to gate voltage of the PMOS devices and V_{tp} is the threshold voltage of the PMOS device. This gives the current mirror a good range of operation and allows more devices to operate in the circuitry below.

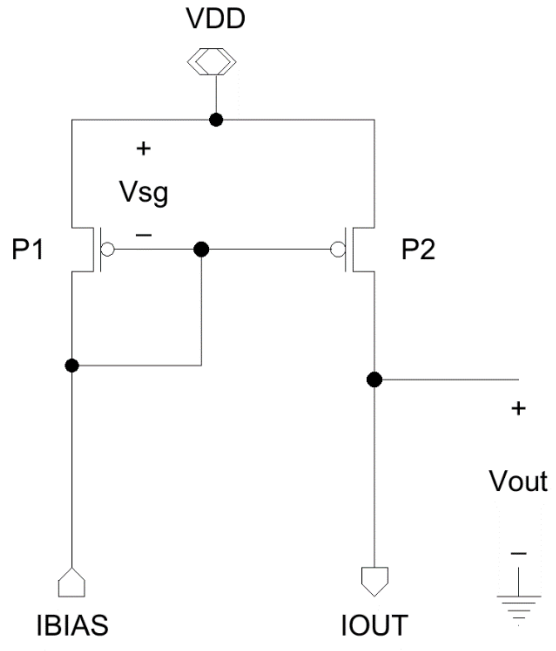


Figure 4.8. Simple current mirror topology.

However, this topology also has a big tradeoff. The output resistance of the simple current mirror is directly related to the MOSFET's output resistance. Since the linearity of the current mirror's output current is inversely related to the output resistance it is beneficial for the current mirror to have a higher output resistance. The simulated output current of the basic current mirror vs the output voltage is shown in Figure 4.9 below.

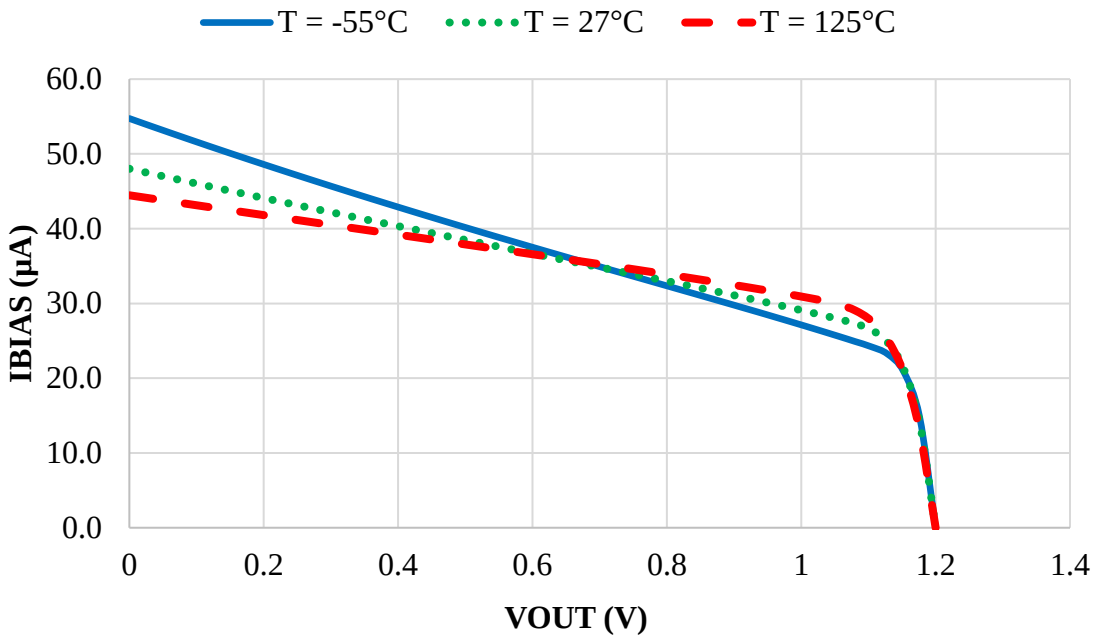


Figure 4.9. Simulated current vs output voltage of the simple current mirror topology.

As shown in the simulation results of the simple current mirror, because the output resistance is not very high for the current mirror, the output does not look stable over the entire range of the output voltage. Since the current mirror is expected to deliver an accurate current over a variety of different output voltages this basic current mirror topology was ruled out for use in the comparator topology.

4.2.2 Cascoded Current Mirror Topology

The next topology that was tested for use in the comparator was the cascoded current mirror. Cascoding is a technique used in many different circuits. The definition of cascoding is to "use a transistor connected in the common-gate/common-base configuration to provide current buffering for the output of a common-source/common-emitter amplifying transistor" [10]. This technique is used to create the circuit shown in Figure 4.10.

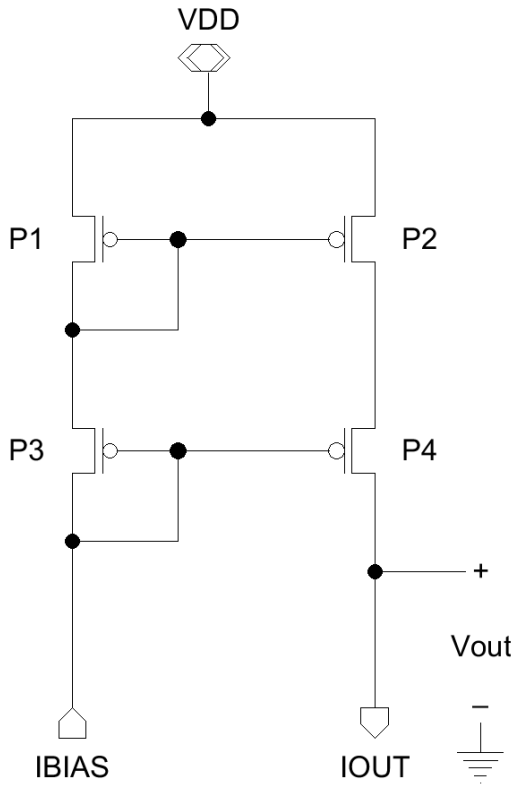


Figure 4.10. Cascoded current mirror topology.

The cascoded device is shown to be P4, and it is used to provide the current buffering for P2. The effect of this buffering is that the output resistance of the current mirror is increased by the transconductance and resistance of the cascode transistor P4 as shown in Equation 4.3 below.

$$r_o = g_{m4} r_{o4} r_{o2} \qquad [\ 4.3\ ]$$

This increased output resistance is good for the linearity of the output current of the current mirror since the slope of the current is inversely related to the resistance [10]. This result is shown in Figure 4.11.

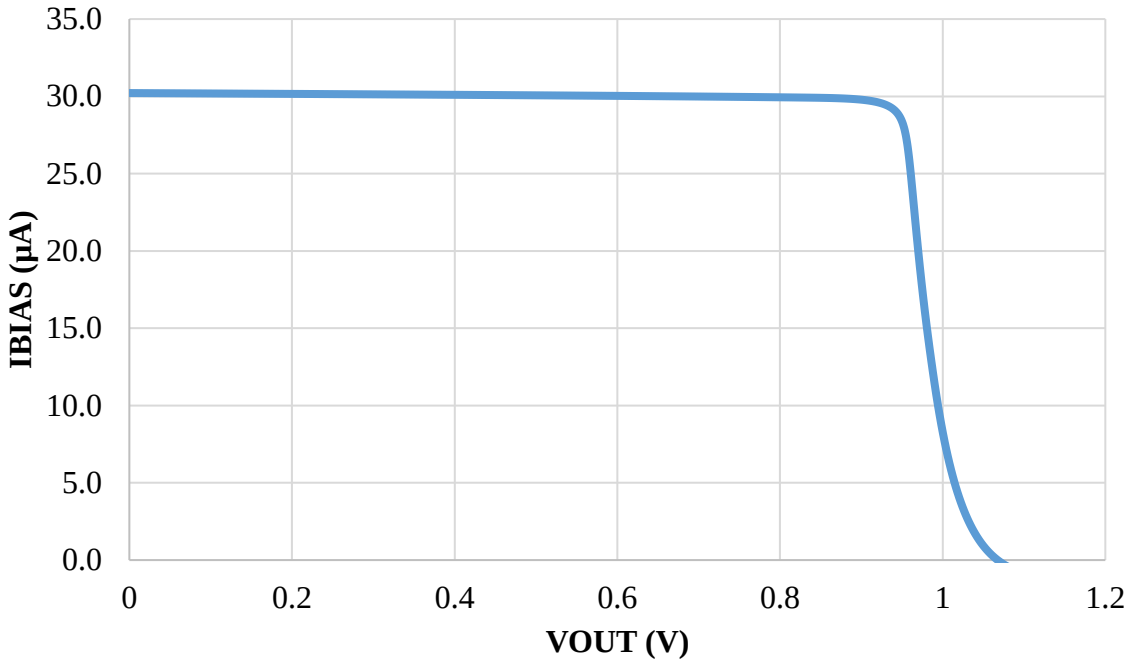


Figure 4.11. Output sweep of cascoded current mirror.

However, now that the cascode transistor is introduced into the circuit it also causes an increase in voltage overhead needed for the circuit. Instead of the output voltage simply needing to be lower than the overdrive voltage it now must be lower than:

$$V_{out} \leq V_{tp} + 2(V_{SG} - V_{tp}) \qquad [\ 4.4\ ]$$

Because of this decrease in available headroom, the ability of the input stage of the comparator to operate at lower temperatures was called into question. At lower temperatures, the HBT devices in the input stage require up to 0.95 V of headroom. This leaves only 0.25 V available for the current mirror out of the 1.2 V supply voltage. This is verified by the simulation in Figure 4.11 that shows that the bias current begins dropping to a critically low value at an output voltage of 0.95 V.

Therefore, it is determined that the cascode current mirror will not be suitable for lower temperatures without applying a higher separate supply voltage to the current mirror stage. For

this reason, the use of this cascoded current mirror topology was passed on for use in the comparator.

4.2.3 Wide Swing Current Mirror

The final current mirror topology that was examined for use in the comparator was the wide swing current mirror. This topology is used to provide the same benefits of the simple current mirror and the cascode current mirror while mitigating the disadvantages that both of those topologies face. An example of this topology is shown in Figure 4.12.

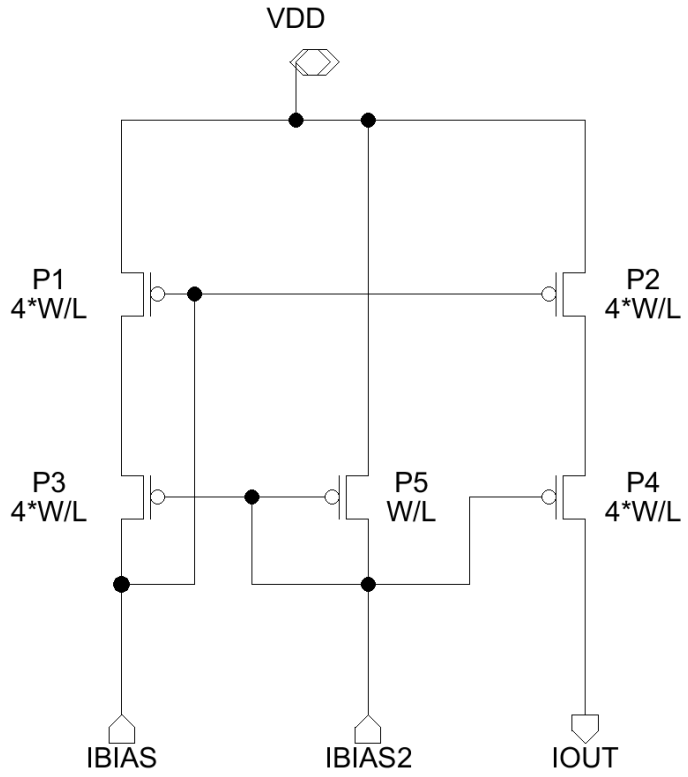


Figure 4.12. Example of wide swing current mirror.

This topology is similar to the cascoded current mirror except for the additional PFET device (P5) that is used to bias the transistor closest to the output. P1 and P3 now work together to create a gate source voltage for P2 [19]. This allows both P2 and P4 to have lower source to

drain voltages when compared to the cascoded current mirror. To prove this, a relationship must be established between the overdrive voltages of each of the devices.

$$V_{OV} = V_{OV1} = V_{OV2} = V_{OV3} = V_{OV4} \quad [4.5]$$

Since the four main devices are all the same size and have the same current, they must have the same overdrive voltage. However, since the new device P5 is four times smaller than devices P1—4, it is related to other overdrive voltages by the following:

$$I_D = 0.5k_n'(0.25 * W/L)(V_{OV5})^2 \quad [4.6]$$

$$\Longrightarrow I_D = 0.5k_n'(0.25 * W/L)(V_{OV5})^2 \quad [4.7]$$

$$\Longrightarrow (V_{OV5})^2 = 4 * I_D/(0.5k_n'(W/L)) \quad [4.8]$$

$$\Longrightarrow V_{OV5} = \sqrt{4 * I_D/(0.5k_n'(W/L))} \quad [4.9]$$

$$\Longrightarrow V_{OV5} = 2 * V_{OV} \quad [4.10]$$

Once the relationships between the overdrive voltages are known, it is possible to solve for the source to drain voltages of the transistors. First however, it is necessary to solve for the gate voltage for P5.

$$V_{OV5} = V_{SG5} - V_t \quad [4.11]$$

$$\Longrightarrow [2 * V_{OV}] = [V_{DD} - V_{G5}] - V_t \quad [4.12]$$

$$\Longrightarrow V_{G5} = V_{DD} - V_t - 2 * V_{OV} \quad [4.13]$$

Now that P5's gate voltage is known the source to drain voltage for P1 can be solved.

$$V_{SD2} = V_{SD1} = V_{DD} - V_{S3} \quad [4.14]$$

$$\Longrightarrow V_{SD1} = V_{DD} - [V_{G5} + V_{SG3}] \quad [4.15]$$

$$\Longrightarrow V_{SD1} = V_{DD} - ([V_{DD} - V_t - 2 * V_{OV}] + [V_{OV} + V_t]) \quad [4.16]$$

$$\Longrightarrow V_{SD1} = V_{OV} \quad [4.17]$$

As can be seen in Equation 4.17, the source to drain voltage for both P1 and P2 is the overdrive voltage V_{OV}. This is the minimum source to drain voltage that the transistors can have and still be in saturation. The next step is to find the source to drain voltage for P3 that allows it to stay in saturation as well.

$$V_{SD3} = V_{S3} - V_{D3} \quad [4.18]$$

$$\Longrightarrow V_{SD3} = V_{S3} - [V_{G1}] \quad [4.19]$$

$$\Longrightarrow V_{SD3} = [V_{G5} + V_{SG3}] - [V_{DD} - V_t - V_{OV}] \quad [4.20]$$

$$\Longrightarrow V_{SD3} = [V_{DD} - V_{OV}] - V_{DD} - V_t - V_{OV} \quad [4.21]$$

$$\Longrightarrow V_{SD3} = V_t \quad [4.22]$$

Since both P2 and P4 must remain in saturation for the current mirror to work, the relationship between the output voltage and the overdrive voltages of the devices is:

$$V_{SD} > V_{SG} - V_t \quad [4.23]$$

$$V_{OUT} < V_{DD} - 2 * V_{OV} \quad [4.24]$$

4.25

Therefore, this circuit will allow the comparator to work over a much larger range due to the mirror circuit allowing an output voltage within two V_{OV} of the supply voltage. The simulation of the wide swing current mirror at -55°C, 27°C, and 125°C is shown in Figure 4.13.

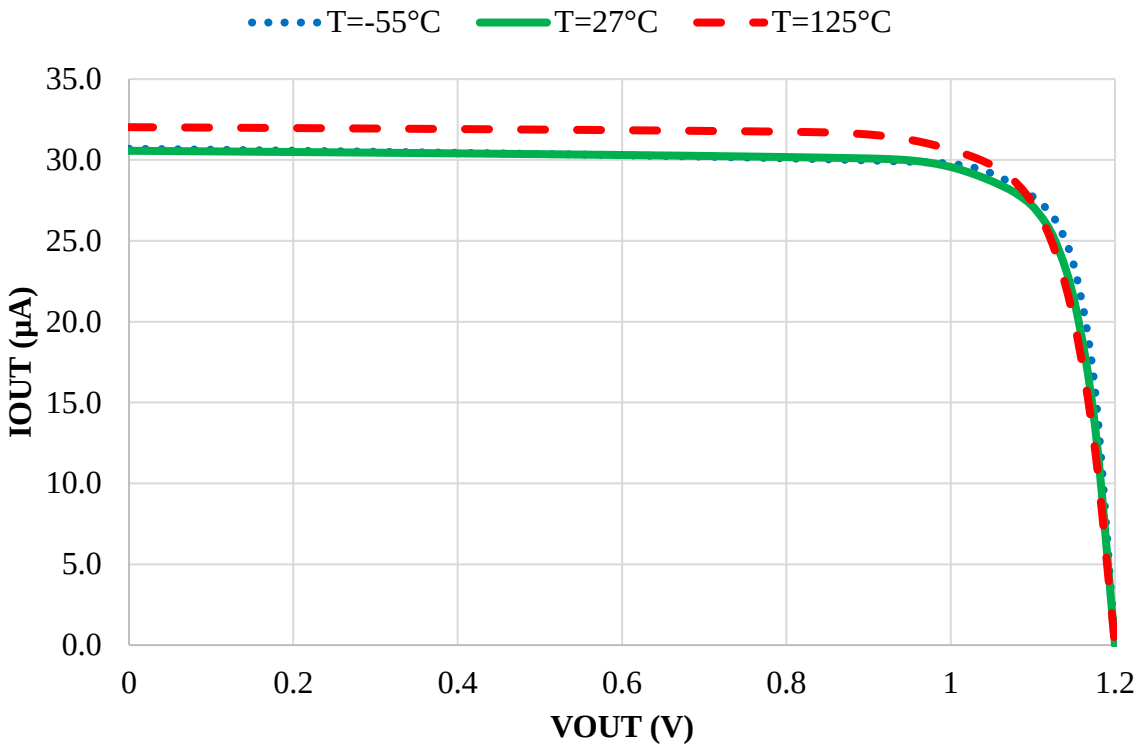


Figure 4.13. Simulation of wide swing current mirror at -55°C, 27°C, and 125°C.

As shown in Figure 4.13, the output of the wide swing current mirror remains stable even for very large output voltages up to and over 1.0 V. The cascoded current mirror topology would output less than 10 µA of current at this voltage load so this wide swing current mirror topology gave an excellent performance boost to the current mirror behavior.

4.3 Changes to Improve Comparator Performance

4.3.1 Improving Comparator Performance at Low Temperatures

One more change that will help the circuit perform even better at lower temperatures is increasing the supply voltage to a value higher than the recommended amount in the design manual. The main requirement that must be met in the devices to safely raise the supply voltage is that the source to gate voltage of all the devices must remain under the recommended 1.2V to prevent gate-oxide breakdown. This would cause catastrophic damage to the device.

To make sure that increasing the supply voltage of the current mirror would not cause gate oxide breakdown, a dc analysis was performed on the circuit to see what the different source to gate voltages were. After analyzing the circuit, it was found that none of the devices have a V_{SG} value that is out of the acceptable range.

4.3.2 Decreasing Bias Current Generator Power Usage

The final change to the bias circuits is to decrease the generated current to reduce some of the power usage of the comparator. The wide-swing mirror needs two identical bias currents to operate so this lowers the power of the bias current generator from:

$$P = (1.2V) * (30\mu A) * 3 \quad [4.26]$$

$$\Rightarrow P = 108\mu W \quad [4.27]$$

To a power of:

$$P = (1.2V) * (10\mu A) * 3 \quad [4.28]$$

$$\Rightarrow P = 36\mu W \quad [4.29]$$

This yields a total power savings of 72 µW. The power savings are even greater when the 1.5V supply voltage is applied to the circuit for operating at low temperatures.

Since the differential amplifiers need 5 µA and the comparator needs 30 µA it was decided to resize the current generator to output 10 µA and then, using the current mirror, it was given a 1:2 ratio to go to the differential amplifiers and a 3:1 ratio for the comparator. The final current generator and current mirror bias circuit designs are shown in Figure 4.14.

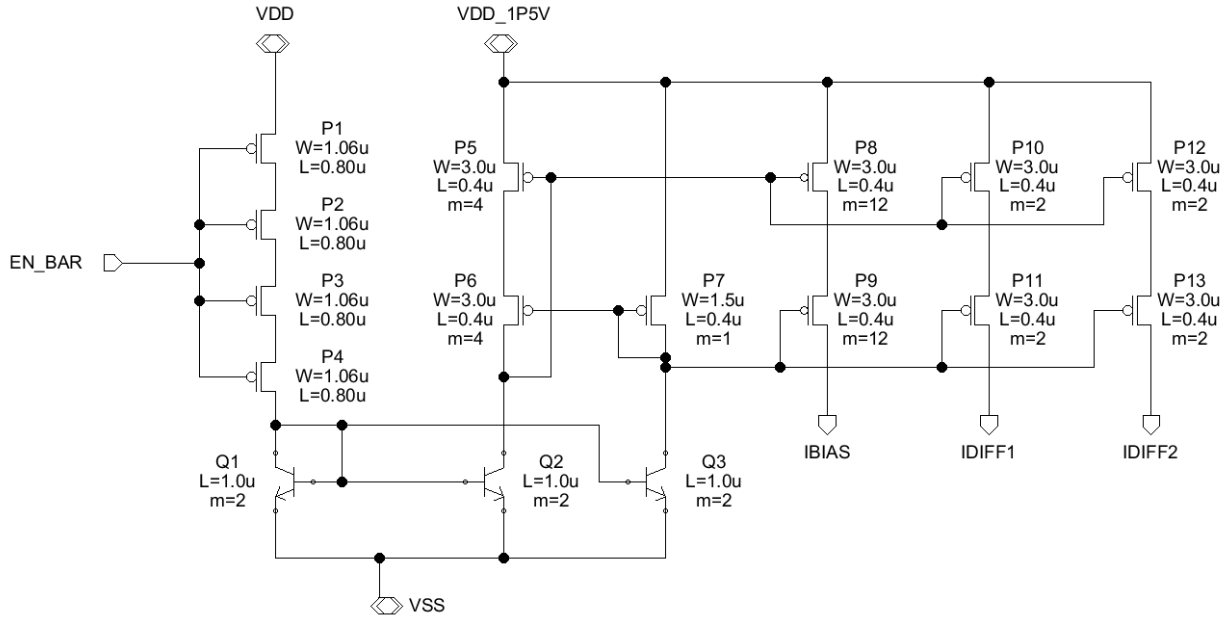


Figure 4.14. Current generator and wide-swing current mirror circuitry.

Chapter 5 - Designing the Digital Cells

The final stage of designing the comparator was to design the digital cells necessary to buffer the output of the differential amplifiers. The differential amplifiers do not have a fully digital output due to the HBT devices not quite pulling the output to the VSS voltage level. Thus, a CMOS buffer is necessary to ensure compatibility with the digital state machine.

5.1 Digital Cells

The next step in designing the comparator is to buffer the output so that it is fully compatible to be the input to the digital state machine that will be controlling the analog to digital converter. Normally this would involve telescoping several digital inverters to get the required output to drive the next digital stage. However, since this comparator needs to be resistant to radiation strikes, it is necessary to mitigate the possibility of a radiation strike causing a glitch at the output.

5.1.1 Initial Design of Buffer

A radiation hardened output buffer consists of a radiation hardened by design digital inverter as described in [1]. The inverter is shown in Figure 5.1.

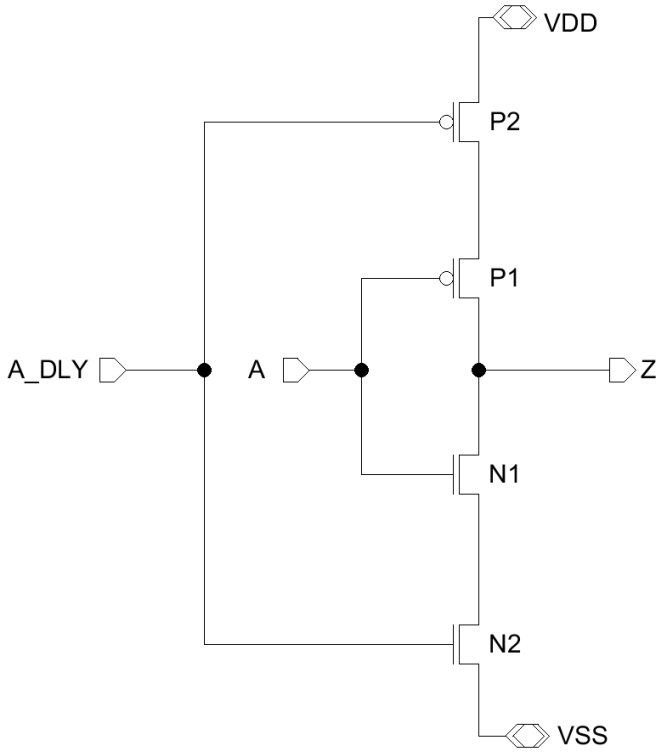


Figure 5.1. Radiation hardened inverter using a guard gate design.

The radiation hardened by design (RHBD) inverter utilizes a guard gate design where both the inputs ‘A’ and ‘A_DLY’ must be the same in order to drive the output ‘Z’ [1]. This design will therefore suppress glitches at the input to the buffer due to radiation strikes if the glitch to the inputs lasts less time than the delay duration of ‘A_DLY’.

In the radiation hardened inverter the control signal ‘A’ is passed through a standard inverter that is shown with devices P1 and N1. The control signal ‘A’ is also fed through a delay block so that the signal ‘A_DLY’ rising or falling edge occurs after ‘A’. The signal ‘A_DLY’ thus controls the inverter changing from a 0 to 1 output or vice versa through the cutoff devices P2 and N2. If a glitch occurs at the input to the inverter ‘A’ and lasts for less than the delay through the delay block, then the glitch signal will effectively be blocked from appearing at the output ‘Z’. The usage of the RHBD inverter is shown in Figure 5.2.

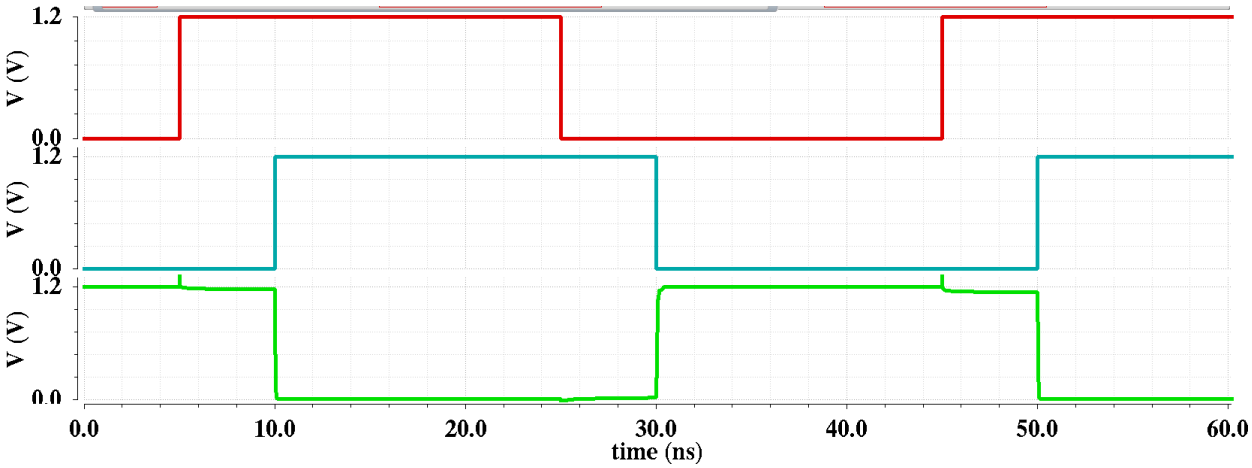


Figure 5.2. Input and output of guard gate inverter circuit.

5.1.2 Radiation Hardened Buffer Design

The guard gate inverter explained previously requires a delay circuit to the input. However, the comparator needs the output to change quickly. Thus, it was decided to tie the "A_DLY" input to the "A" input. This would remove the need for the large delay circuits and lower the propagation delay of the comparator output at the expense of some of the inherent radiation hardness of the design. The inverter design used to buffer the output is shown in Figure 5.3.

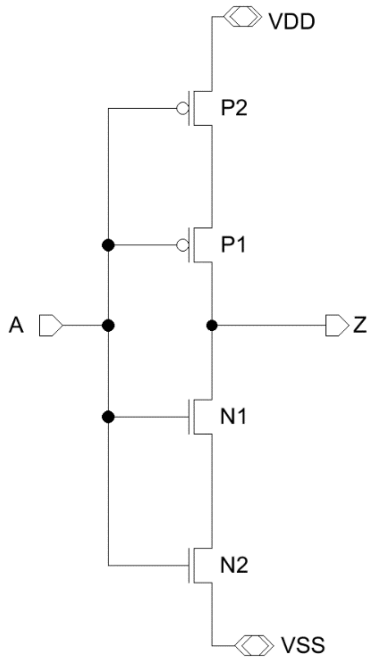


Figure 5.3. Radiation hardened inverter design.

Two different sizes of this RHBD inverter were designed. They were sized so that the smaller inverter can drive the larger inverter. In this way, the two inverters will be combined to be a non-inverting buffer that can drive the inputs of other digital logic. The sizes of the inverters were based on the sizes provided from the digital cells designed by students in the computer engineering department at the University of Arkansas and are shown in Table 5.1.

Table 5.1. Transistor sizes of the RHBD inverters.

	Size 1	**Size 2**
W/L PFET	0.12u/0.2u	1.2u/0.2u
W/L NFET	0.2u/0.2u	0.66u/0.2u

The final digital buffer design is shown in Figure 5.4.

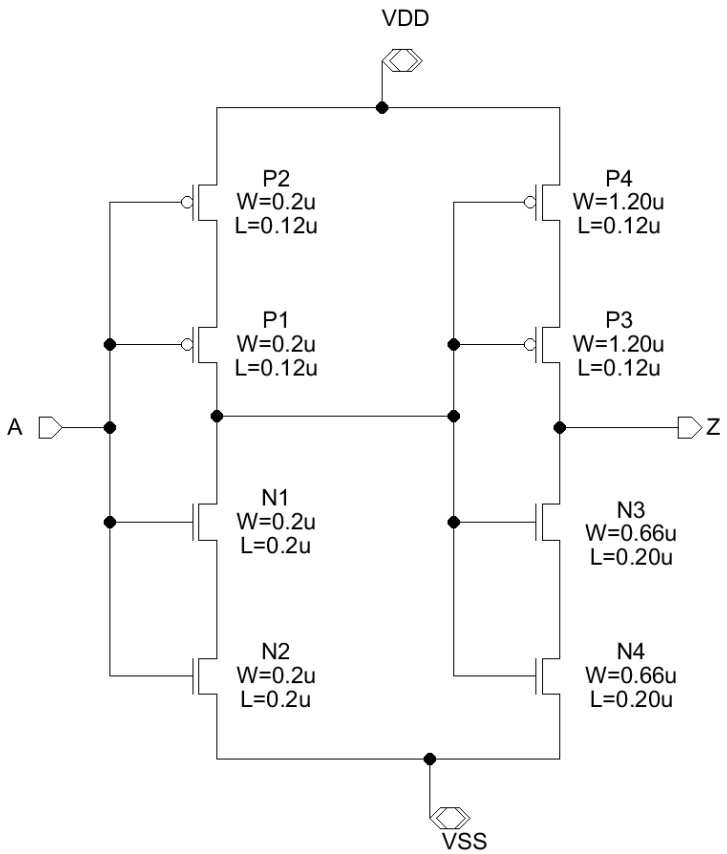


Figure 5.4. RHBD digital buffer topology with transistor sizes.

To see how much delay is added to the entire propagation delay of the comparator, the output of the RHBD buffer was compared to the output of a similarly sized digital buffer without the extra transistors. An identical signal “INPUT” was provided to both buffers. As shown in Figure 5.5, the additional delay added by the eight-transistor buffer was only about 1 ns.

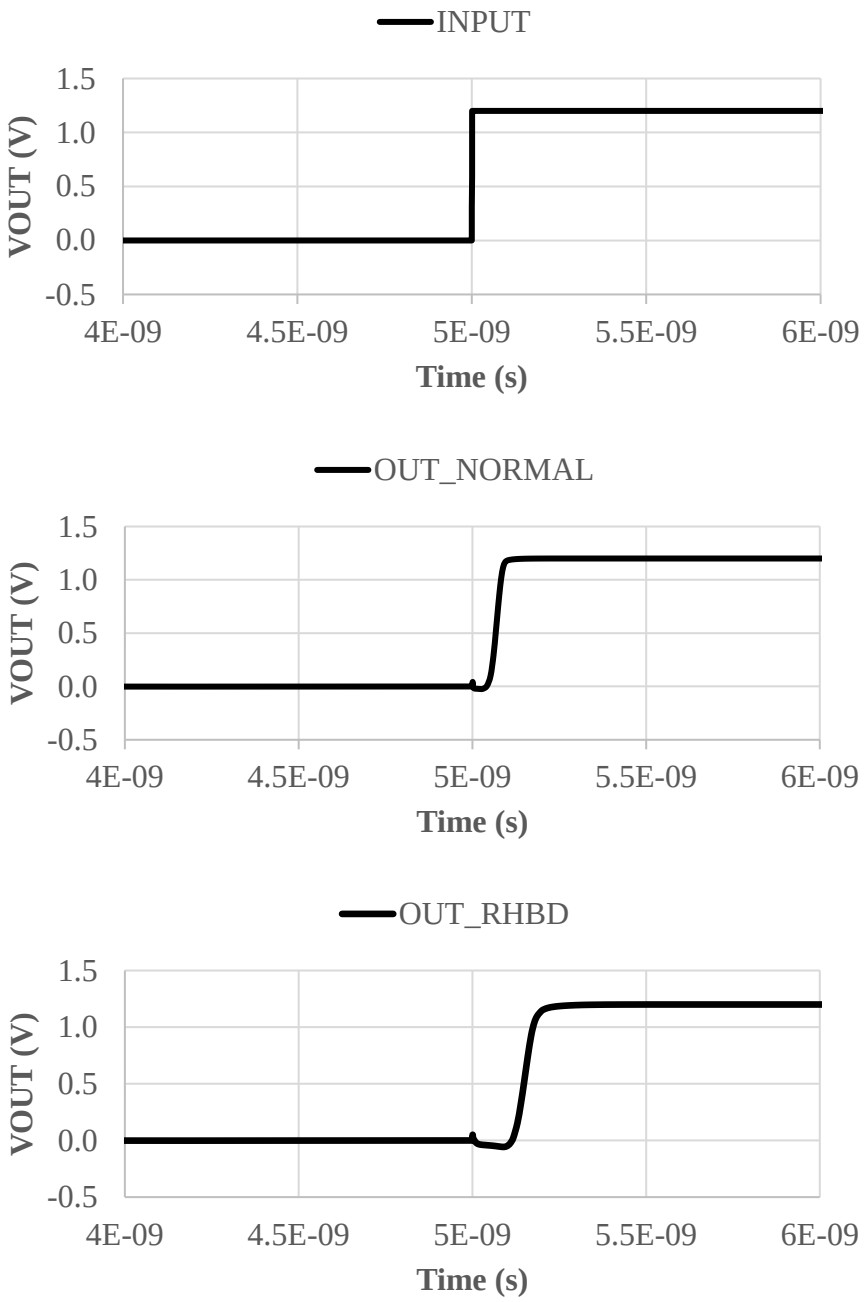


Figure 5.5. Output comparison of RHBD digital buffer and normal digital buffer.

5.1.3 NAND and NOR Digital Gates

The final cells necessary to implement the digital control circuitry were the NAND and NOR gates. These were designed with the minimum sized devices recommended by the digital circuits from [15]. Since the output of these NAND and NOR gates are buffered by the radiation hardened buffers and inverters, it was decided that any glitches that might occur due to a radiation strike would not affect the overall operation of the comparator. The schematic and the final sizes of these devices are shown in Figure 5.6.

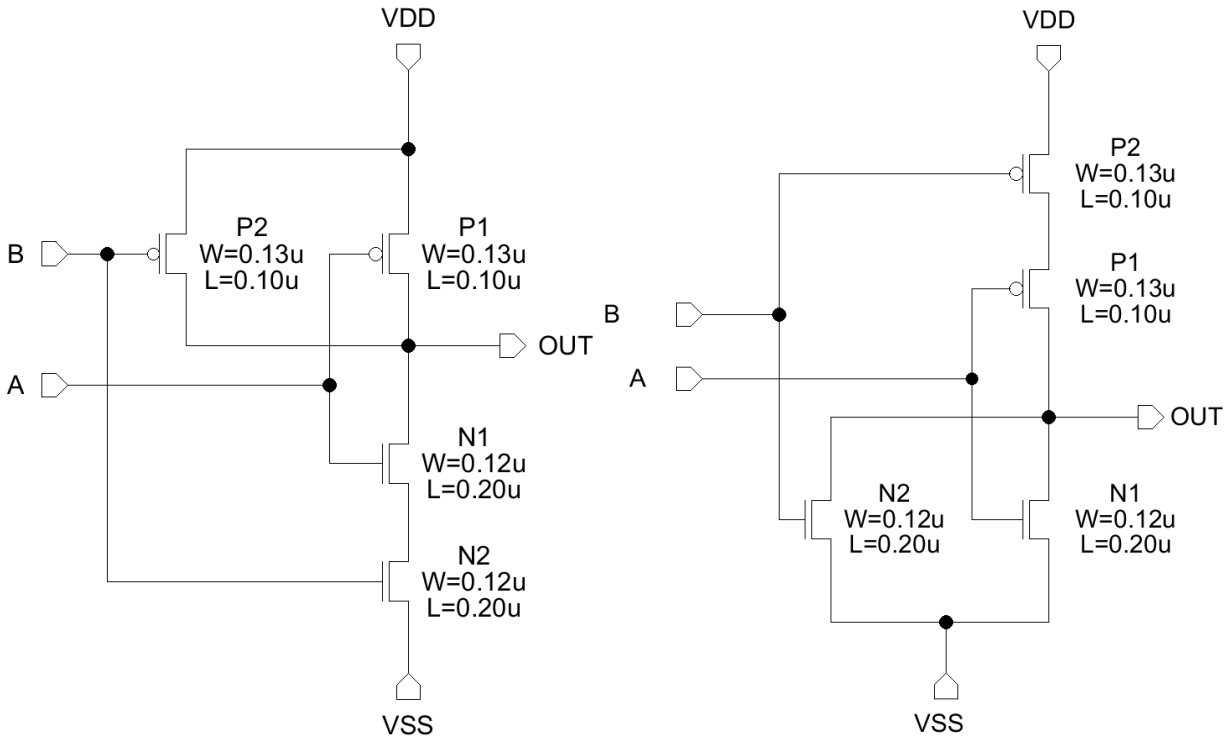


Figure 5.6. Topologies for (a) NAND circuit and (b) NOR circuit.

5.2 Adding Enable/Disable Functionality to Comparator

Since the digital state machine only needs to use the comparator for the small portion of time that the ADC is operating, it was decided to add enable/disable functionality to the comparator. This would reduce the power usage of the comparator circuit when it is not needed by the digital state machine.

5.2.1 Delay Buffers for Comparator Output

After simulating the entire comparator, it was noticed that there was an issue with the first comparison after switching from the disabled state to the enabled state. This manifested itself as a short glitch in the output of the comparator for certain inputs. The cause of this issue was traced to the fact that when the bias circuits are enabled it takes several nanoseconds for the bias current to propagate and the output can show a glitch while this is occurring.

To prevent this glitch, a delay was added to the enable signal of the comparator output. This ensures that there would not be any false outputs shown by the comparator. To implement the delay a signal delay circuit block was needed. The block used is a rad hard by design delay block implemented with capacitors at the input. This circuit was designed and simulated to work at cryogenic temperatures by the Computer Engineering lab at the University of Arkansas as described in [15]. The topology is shown in Figure 5.7.

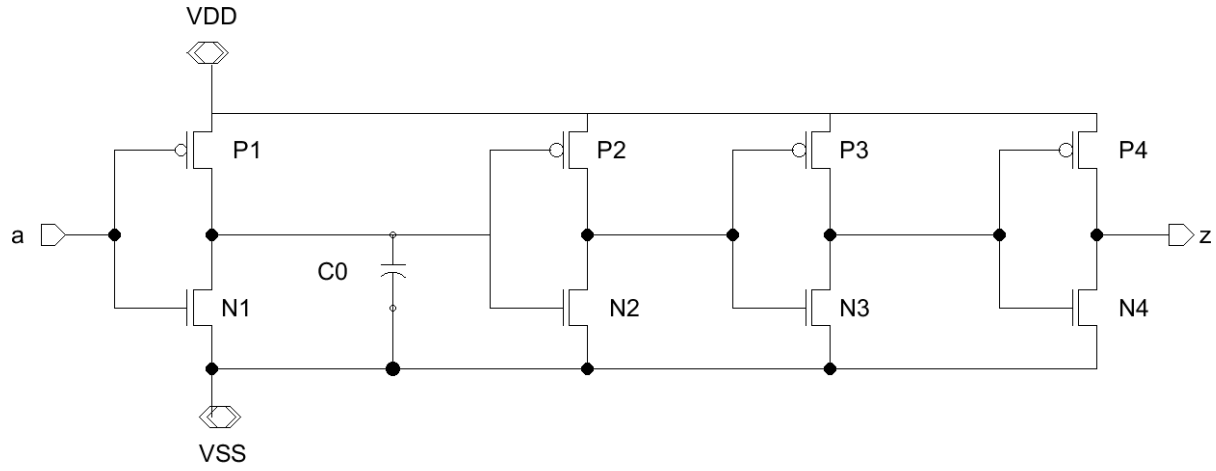


Figure 5.7. RHBD delay buffer circuit.

The delay buffer circuit works by increasing the transition time for the transistors in the digital inverter chain. The advantage of using this delay circuit topology for the 9HP process is

that the capacitors are naturally radiation hardened and stable over temperature [15]. The delay block for this comparator provides a delay of approximately 5 ns for the comparator input.

5.2.2 Designing the Enable Switches

As mentioned in the previous section, enabling the comparator output must occur several nanoseconds after enabling the bias circuitry to give the bias current the opportunity to propagate and thus to prevent glitches at the output while the comparator is starting up. The circuit enabling this behavior is shown in Figure 5.8.

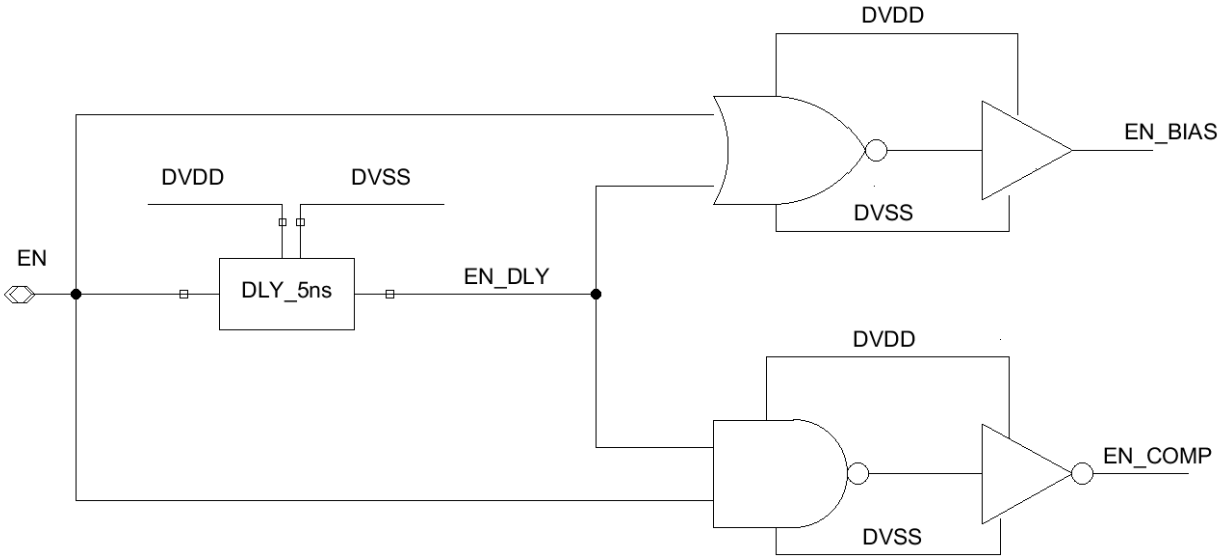


Figure 5.8. Comparator enable digital control circuitry.

As shown in Figure 5.8 the output to the comparator will only turn on when both “EN” and “EN_DLY” have a high input. Since the bias circuitry is active low, when the “EN” signal is given to the comparator the “EN_BIAS” signal immediately becomes low and will stay that way while either enable signal is active high.

On the other side for the enable comparator signal, the enable output is active high so the output is only activated after the 5ns delay of the “EN_DLY” signal. As soon as the “EN” signal goes low the output of the comparator will turn off. The output states are shown in Table 5.2.

Table 5.2. State table for digital input circuitry.

EN	EN_DLY	EN_BIAS	EN_COMP
0	0	1	0
0	1	0	0
1	0	0	0
1	1	0	1

5.2.3 Designing the Output Digital Circuit

The digital output circuit needed to suppress the output whenever the EN_DLY signal is low to suppress any glitches while the bias circuitry is starting up. The state table is shown in Table 5.3.

Table 5.3. State table for digital output circuit.

EN	EN_DLY	VOUTP	VOUTM
0	0	0	0
0	1	0	0
1	0	0	0
1	1	$\overline{\text{VOUT\_R}}$	$\overline{\text{VOUT\_L}}$

The circuit used to buffer the digital output is shown in Figure 5.9.

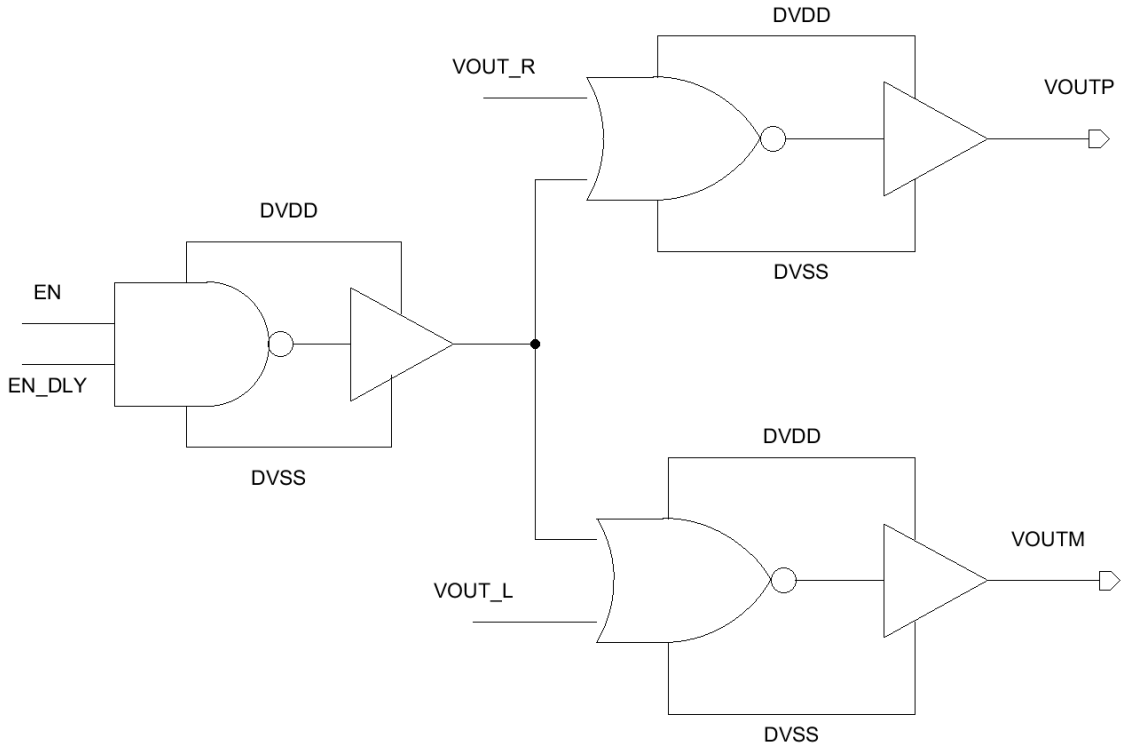


Figure 5.9. Digital output circuit.

5.2.4 Adding Pull-Up Devices to gates of Push-Pull Transistors

The last step to finish adding the enable/disable functionality to the comparator was to add pull-up devices to the push-pull stage of the comparator. These devices would pull the gates of the PFETs in the push-pull stage to the VDD rail and thus prevent current flowing through the PFETs when the comparator is disabled. The pull-up transistors were sized the same as the push-pull PFETs whose gates they were connected to. (W=2.0 µm, L=0.2 µm). These devices are labeled P7 and P8 in the schematic of the full comparator shown in Figure 5.10 below.

5.3 Full Comparator Circuit

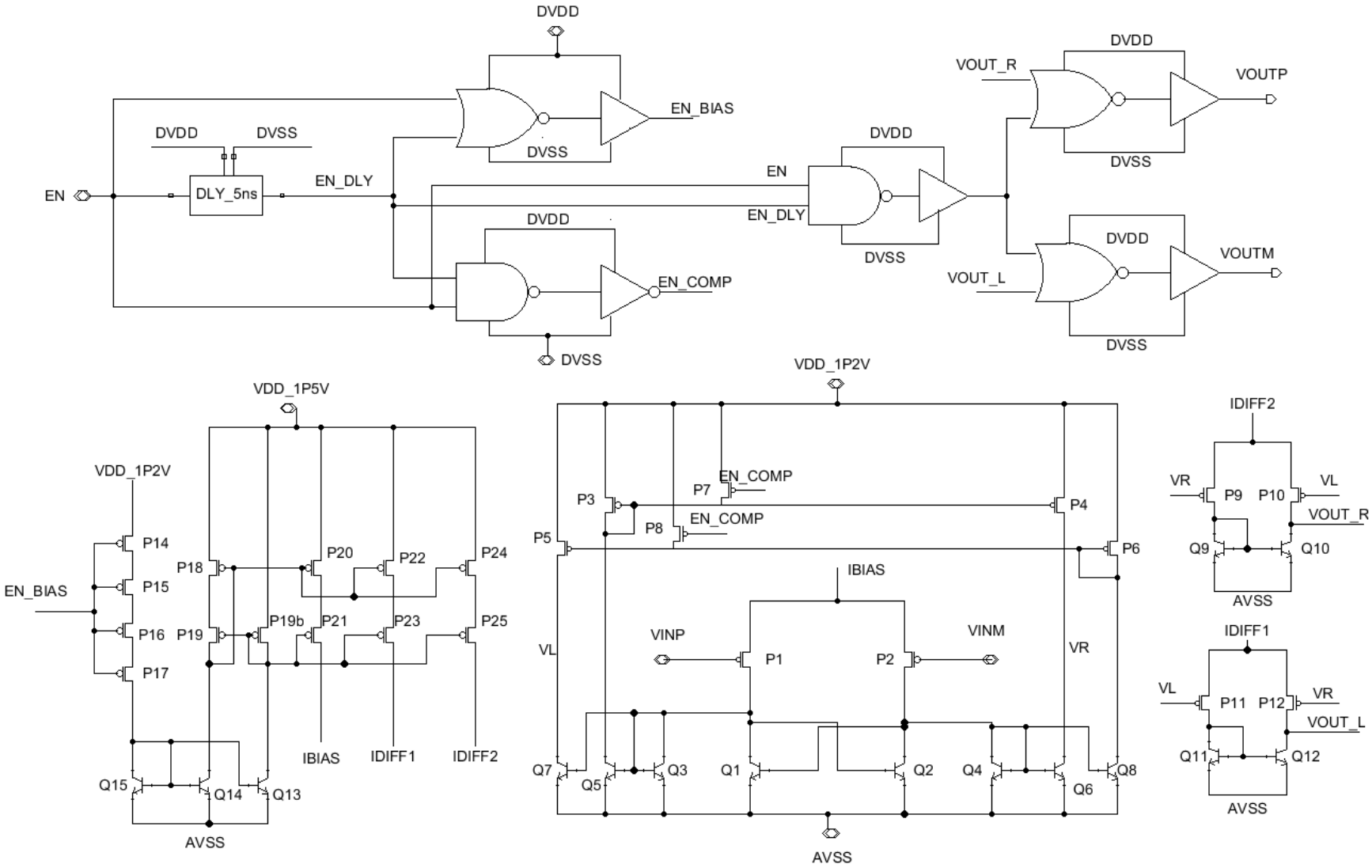


Figure 5.10. Full comparator schematic with both digital and analog stages.

Chapter 6 - Layout of the Comparator

6.1 Layout Strategies

The layout of the comparator was done in Cadence Virtuoso using the layout editor. There were several techniques that were followed for the layout to achieve good circuit performance as well as radiation hardness for the comparator.

6.1.1 Common Centroid Layout

One of the most common techniques to achieve good matching between devices is called the common centroid layout. This is a layout technique that involves averaging the process variations that occur across two or more matched devices by laying out the devices in a pattern with a common center point [20].

There are several rules that should be followed for a common centroid layout. A common centroid layout should be an array of devices that share a common centroid, are symmetric about both axes, are dispersed throughout the array, and the array should be as compact as possible. These four rules of common-centroid layout are called the rule of coincidence, the rule of symmetry, the rule of dispersion, and the rule of compactness [21].

An example of a common-centroid layout for two separate devices A and B is shown in Figure 6.1.

A	B	B	A
B	A	A	B

Figure 6.1. Example common-centroid layout pattern.

This example layout pattern follows all the rules of a common-centroid layout and thus is less susceptible to stress induced mismatch between the two devices.

6.1.2 Guard Rings for Radiation Hardness

The main layout technique used to ensure that the circuits were radiation hardened was to add guard rings around each PFET device. As described in [1], using a guard ring helps to reduce the total ionizing dose (TID) effects of radiation to the devices. In addition to increasing the overall TID resistance of the circuit, using guard rings also helps increase latchup immunity and reduce noise in the circuit due to substrate coupling [1].

6.2 Layout Cell Blocks

6.2.1 Input Stage

The input comparator stage consisted of the input PFET pair, the cross-coupled HBT pair, and the push-pull stage with both PFETs and HBT devices. The layout is shown in Figure 6.2.

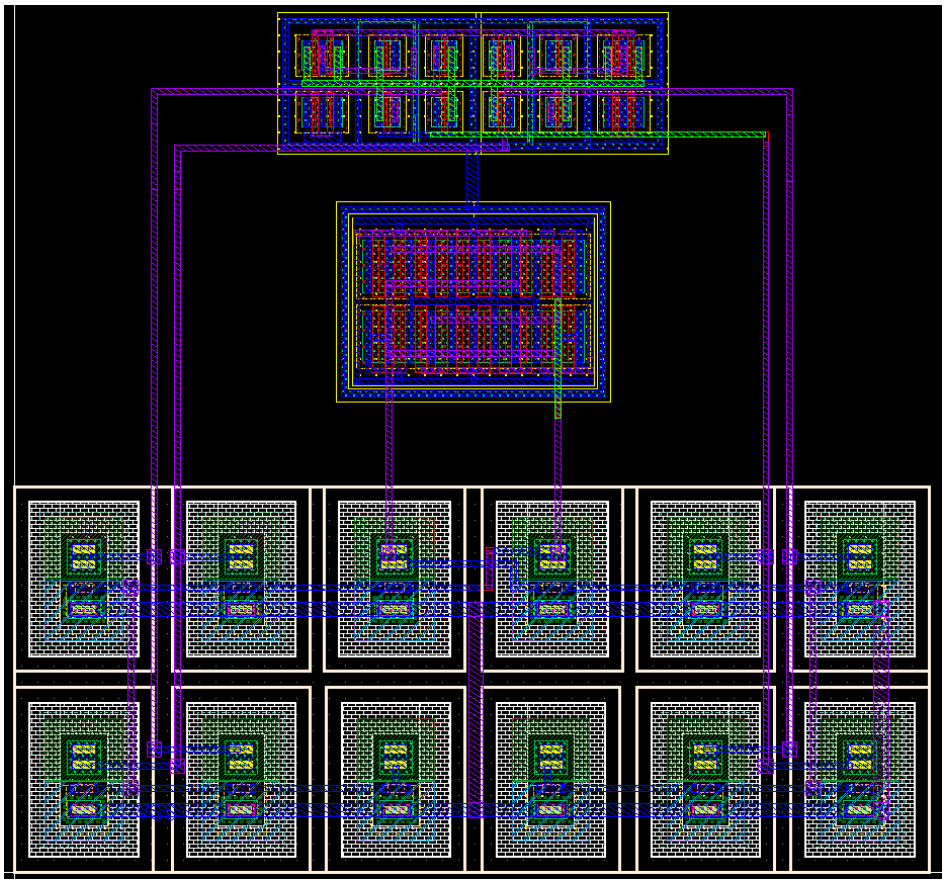


Figure 6.2. Input stage of comparator layout.

The input PFET pair is the array of devices in the middle directly above the HBT devices. It was laid out in two rows of interdigitated devices in a common centroid pattern. Another feature that was added to the input pair was the dummy transistors on both ends of the rows of devices. The purpose of the dummy transistors is to reduce the etch variations at the edge of the layout that could cause mismatch between input devices [21]. The common centroid pattern used for the input pair of transistors was based on one of the recommended patterns described in [21]. This pattern is shown in Table 6.1.

Table 6.1. Layout pattern for input pair PFETs of comparator.

Dummy	A	B	B	A	A	B	B	A	Dummy
Dummy	B	A	A	B	B	A	A	B	Dummy

The push-pull PFETs are shown at the very top of Figure 6.2 and each pair of PFETs is connected in a common centroid pattern as well. The pattern for these PFETS is shown in Table 6.2 where A and B are the pairs of devices and C is the enable/disable PFET device.

Table 6.2. Layout pattern for push-pull PFETs and bootstrap transistors.

C1	A1	B1	A2	B2	C2
Dummy	B1	A1	B2	A2	Dummy

The reason for the large gap between the input PFETs and the HBT devices for the push-pull stage is because of the process rules. The minimum distance between the N-well of the PFETs and the well of the HBT devices was quite large.

6.2.2 Current Mirror

The layout for the current mirror was a little more complicated to find a common-centroid pattern. The decision was made to split the top and bottom transistor pairs to two separate arrays

of devices since the top and bottom devices in the current mirror each share a common gate connection. Given the branch names shown in Figure 6.3, the pattern that was used for the bottom devices in the current mirror is shown in Table 6.3. The top devices had the same pattern as the bottom devices, but with a dummy transistor in place of transistor P5.

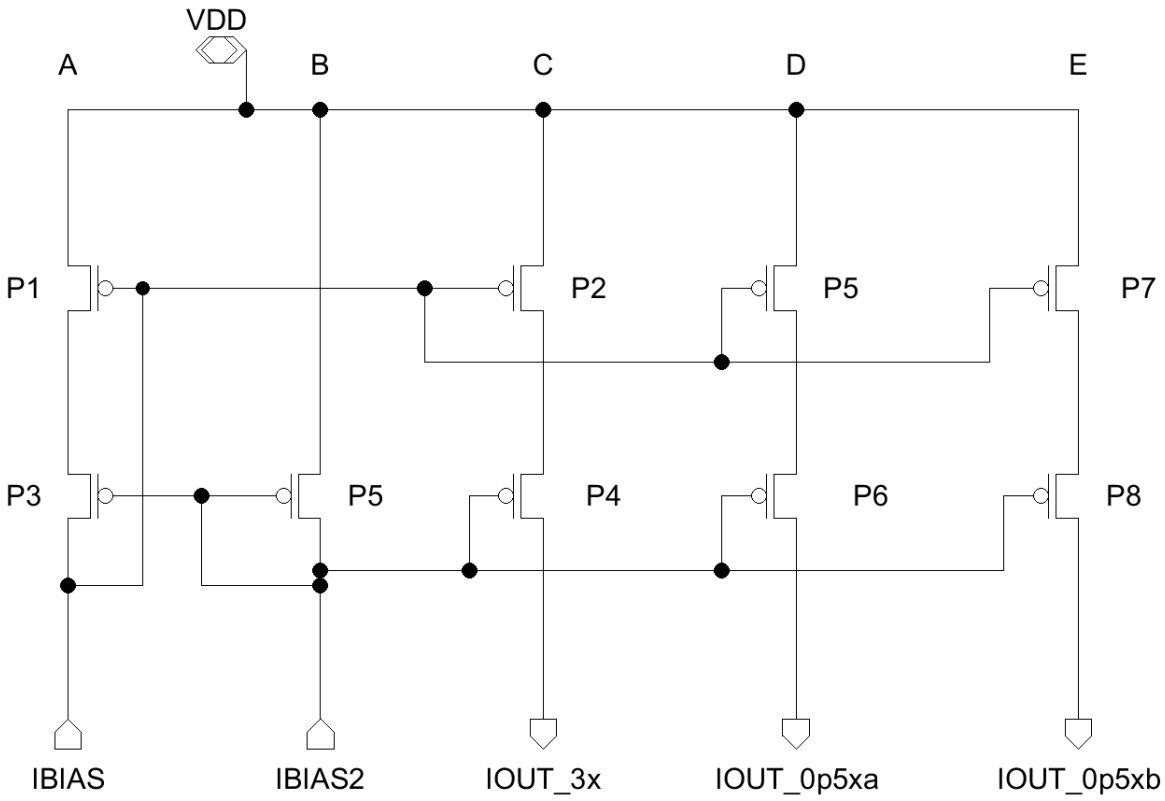


Figure 6.3. Current mirror schematic.

Table 6.3. Layout pattern for current mirror.

Dummy	D	C	C	E	Dummy
C	C	A	A	C	C
C	C	A	A	C	C
Dummy	E	C	C	D	B

The main reason that more dummy devices were not used in the wide swing current mirror is because of size constraints since adding dummy devices to the sides of all edge devices would have increased the size of both arrays quite drastically. However, this should not have too much of an adverse effect on the current mirror because the only devices with an open edge are the P2 and P4 transistors which are the largest and are therefore less susceptible to error caused by the etch variations at the edge of the devices. The layout for the current mirror is shown in Figure 6.4.

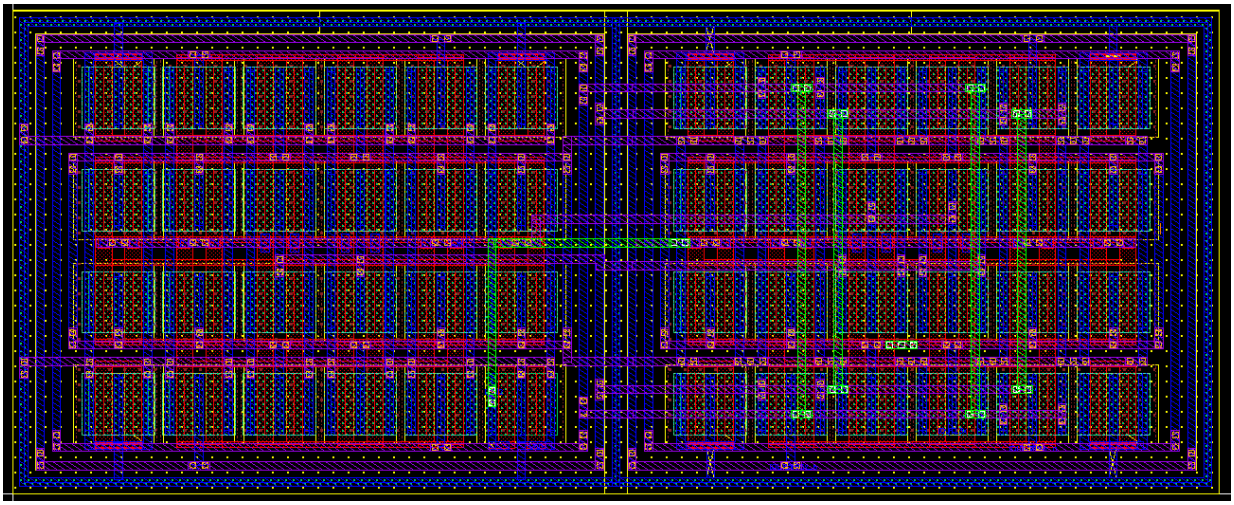


Figure 6.4. Wide-swing current mirror for comparator.

6.2.3 Digital Circuits Individual

The digital cell layouts were based on the layouts done previously for the 90 nm SiGe digital cells [15]. The most important consideration for the digital cells was that the guard rings and the inputs/outputs would line up correctly when two or more cells were placed next to each other. This allowed for the digital circuits to be created by abutting each standard cell via the guard ring. An example of a NOR standard cell layout is shown in Figure 6.5.

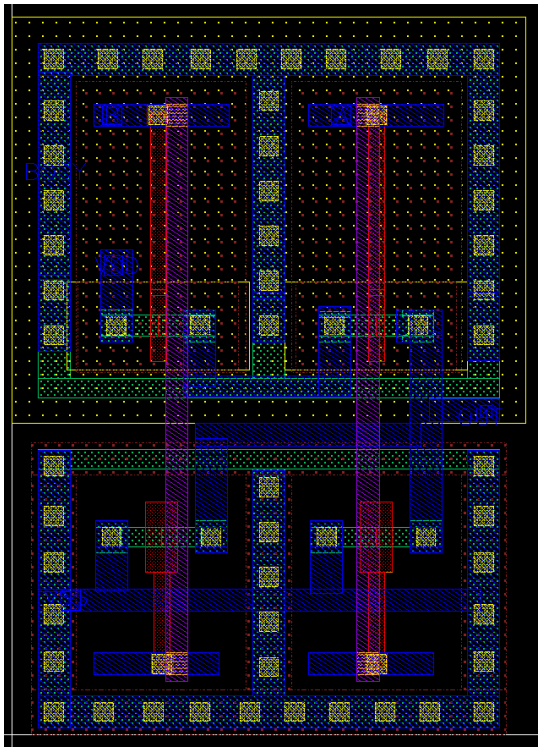


Figure 6.5. NOR gate standard cell layout.

6.2.4 Digital Circuits Group

The input and output digital circuits were then laid out by placing each standard cell in a row. Since the interconnect of each individual standard cell was done in the first two metal layers, the connections between standard cells was made by using the third metal layer. The input and output digital circuits are shown in Figure 6.6. As mentioned in [15], because the capacitor is a dual MIM (metal-insulator-metal) capacitor that uses the upper metal layers of the process all of these transistors and interconnect can be placed underneath the capacitor to save space.

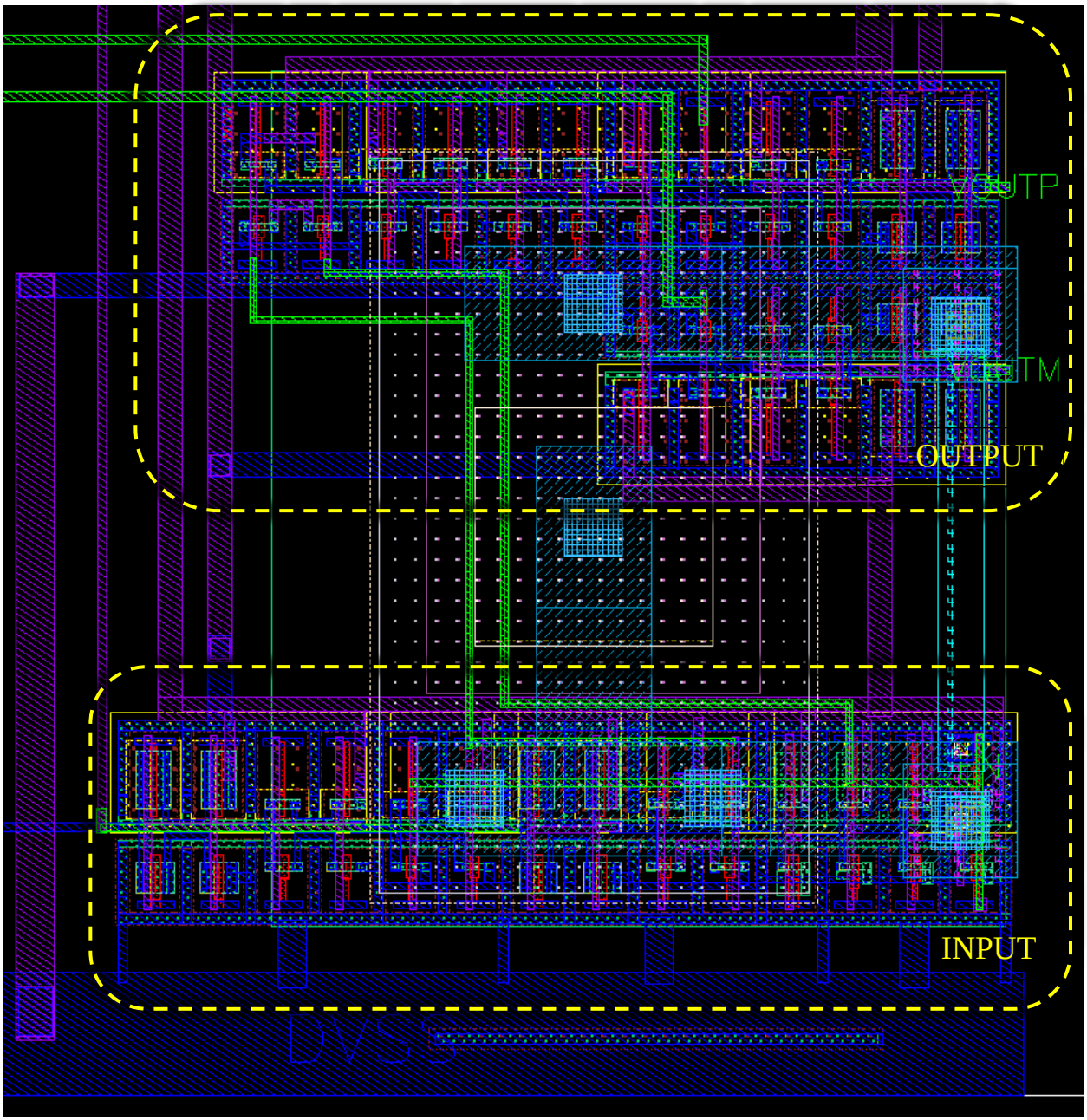


Figure 6.6. Input digital cells (bottom row) and output digital cells (top row).

6.2.5 Full Circuit Layout

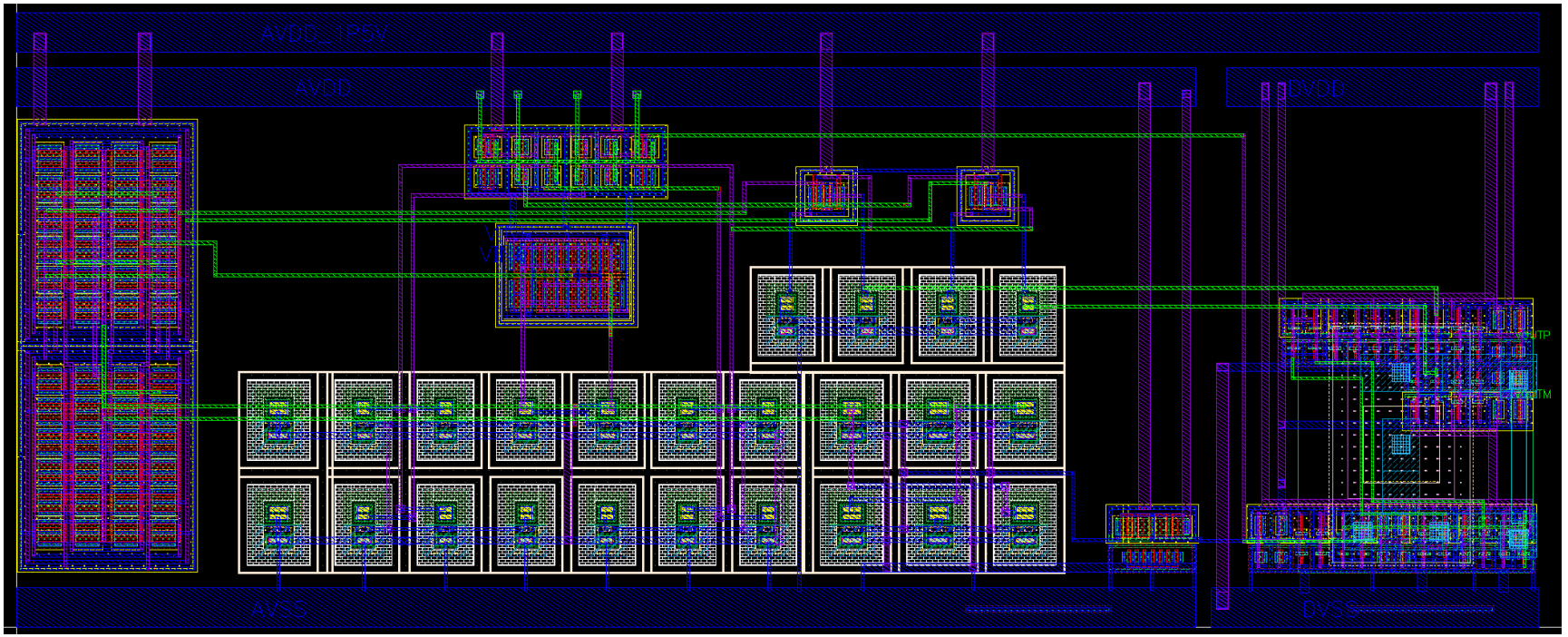


Figure 6.7. Full comparator layout.

The digital circuits were placed as far as possible from all the analog circuits. This helps keep the noisy digital circuits from causing any unnecessary errors to the analog circuits. This is the reason for a lot of the blank space on the right side of the layout.

All the differential circuits were placed and routed as symmetrically as possible to reduce mismatch between the circuits. The HBT devices were all placed at the bottom of the layout as close as possible to the PFETs. Some dummy HBT devices were placed on the edges of the array when possible.

The final size of the layout including power and ground rails was 99.785 µm x 40.155 µm which equates to a total area of 4,006.870 μm^2. Unfortunately, 752.070 μm^2 of this area was made up of either empty space or just metal layers (18.8% of total area).

All this empty space was largely unavoidable due to two reasons. The first reason was that in the process of orienting the input stages of the comparator symmetrically with the HBT devices there just was not enough room to fit the current mirror anywhere convenient to close off the empty space. The second reason was that it was not known originally whether the digital power supply of the comparator would be connected to the power supply of the other digital circuits in the ADC system. Thus, it was desired to separate the digital circuits from the analog circuits in the comparator. This left an empty area of 447.920 μm^2 between the digital circuits and bias current generator circuit and the rest of the comparator.

Chapter 7 - Simulation of the Comparator

The testbench schematic set up for the simulations of the comparator is shown in Figure 7.1. The DVDD and AVDD are always connected to (separate) 1.2 V power supplies to prevent the noisy digital circuits from causing error to the analog circuits. The AVDD_1P5 pin can be connected to either a 1.2 V supply or a 1.5 V supply if faster cryogenic performance is desired.

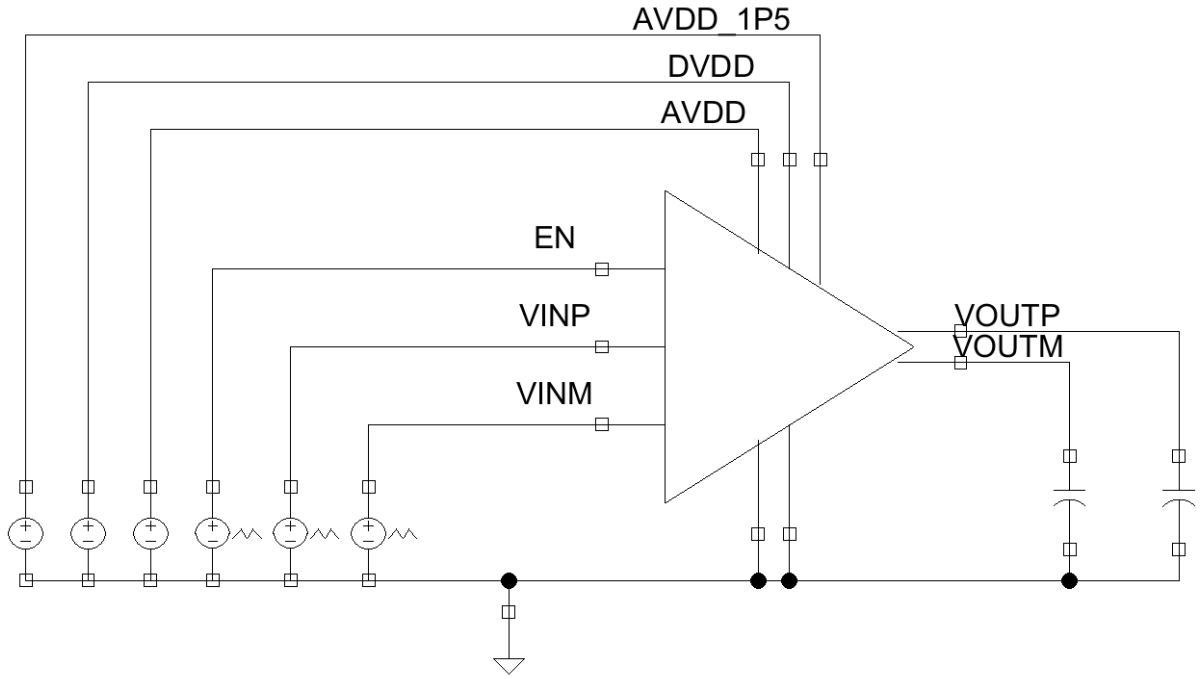


Figure 7.1. Testbench schematic for comparator.

All the simulations presented in this chapter were performed using the parasitic resistances and capacitances that were extracted from the layout. Doing the simulations under these conditions helped to more accurately predict how the circuit would behave once it was fabricated.

In addition to simulating the comparator at the standard temperature range of -55°C to 125°C it was also simulated under cryogenic conditions (when temperatures reach as low as -196°C). To accomplish this, the standard process design kit models were replaced with the cryogenic

models that were developed by the University of Arkansas MSCAD lab as well as by the faculty and students at Georgia Tech as described in Section 2.3.

7.1 DC Simulation Results

The first simulation was a simple DC sweep of the VINP input. The VINM input was held at a constant 0.35 V while the VINP input was swept from 0.348 V to 0.352 V with a step size of 1 µV. The results of this simulation are shown in Figure 7.2.

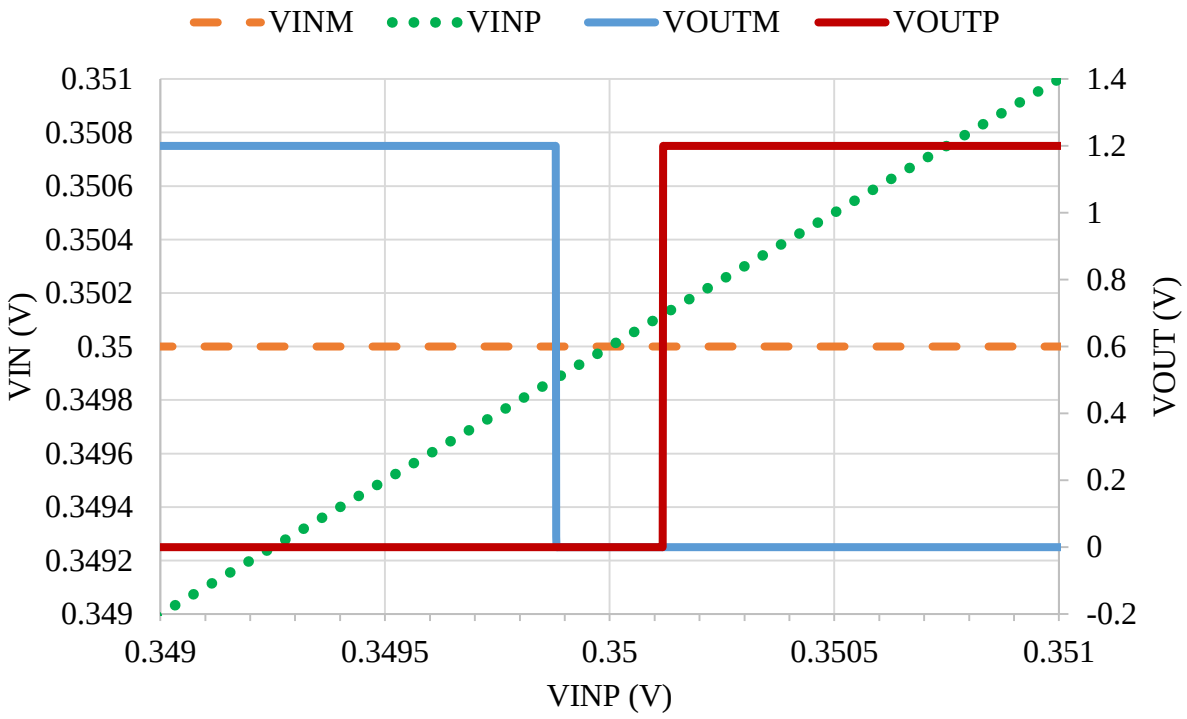


Figure 7.2. DC sweep of VINP.

The DC simulation of the comparator shows a slight offset for both the VOUTP and VOUTM where both outputs are a digital "0". This systematic offset for both the VOUT signals is about 120 µV. As shown in Table 3.1, this corresponds with an NCL state of "NULL" so this is an acceptable output for the comparator while switching. The only invalid state of the

comparator would be if both the outputs of the comparator were to exist in the digital "1" state at the same time.

7.2 Input Offset Voltage Simulation Results

The next step was to run transient simulations with the parasitic information extracted from the layout of the comparator. The first transient simulation that was run was the input offset voltage measurement. This simulation was performed by connecting a triangle signal to the VINP input that starts at a value of $\mathrm{VINM} - 50\ \mathrm{mV}$ and then increases to a value of $\mathrm{VINM} + 50\ \mathrm{mV}$ over the period of 10 µs. This simulation was run eleven times with VINM at a different reference voltage from 0.05 V to 0.55 V. Then, the worst case and best case offset voltages were captured. The results of this input offset simulation are summarized in Table 7.1.

Table 7.1. Input offset voltage.

Temperature	V_{OS} Rising	V_{OS} Falling
T=-196°C Worst Case	2.60 mV	2.46 mV
T=-196°C Best Case	0.10 mV	0.09 mV
T=-55°C Worst Case	4.10 mV	3.88 mV
T=-55°C Best Case	0.45 mV	0.18 mV
T=27°C Worst Case	2.74 mV	2.73 mV
T=27°C Best Case	0.26 mV	0.02 mV
T=125°C Worst Case	1.70 mV	1.69 mV
T=125°C Best Case	0.12 mV	0.19 mV

As can be seen from Table 7.1, the best-case offset voltage at all temperatures was well within the design goal of 1 mV. However, the worst-case offsets (which were measured at the fringes of the input range of the comparator) did not reach the design goal of 1 mV offset voltage. This was expected since the maximum gain of the comparator occurs at the middle of the input common-mode range (around 0.3 V to 0.4 V common-mode input).

To balance this offset problem in a future design, it will be necessary to design an offset compensation circuit for the input stage. The compensation circuit would need to be designed to have a programmable offset and once the systematic offset of the comparator has been measured it would be possible to set the compensation network to an amount that would correct the offset issues.

7.3 Propagation Delay Simulation Results

The next simulation that was run was to simulate the propagation delay of the comparator across all temperatures. The results are shown in Figure 7.3 and summarized in Table 7.2.

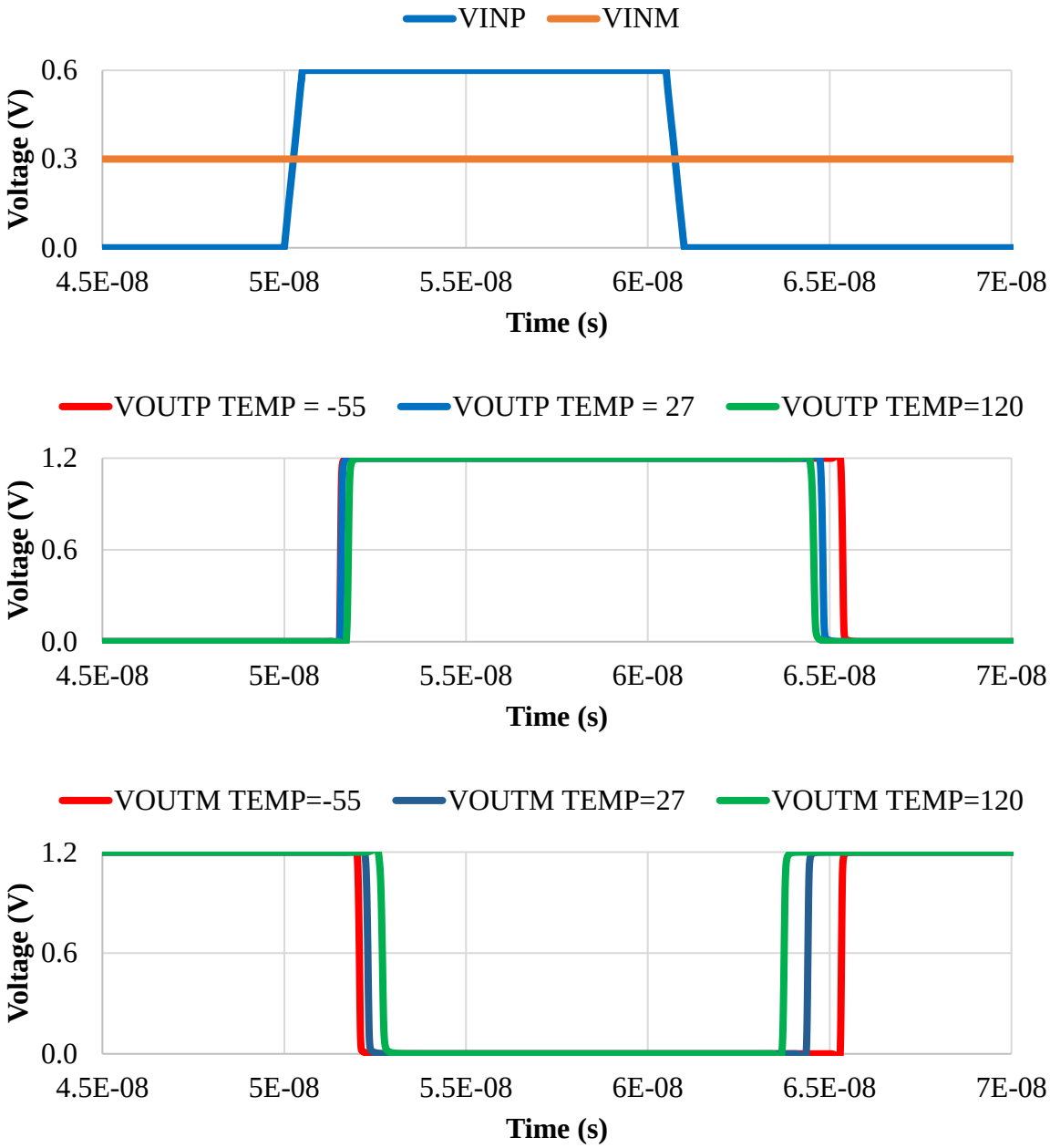


Figure 7.3. Propagation delay of comparator output signal at -50°C, 27°C, and 120°C.

Table 7.2. Propagation delay results across temperature.

Temperature	VOUTP Rising Delay	VOUTM Rising Delay	VOUTP Falling Delay	VOUTM Falling Delay
-196°C	1.0 ns	3.0 ns	3.0 ns	1.0 ns
-55°C	1.0 ns	4.4 ns	4.4 ns	1.5 ns
27°C	1.0 ns	3.4 ns	3.8 ns	1.8 ns
120°C	1.3 ns	2.8 ns	3.6 ns	2.3 ns

The same simulation for propagation delay was run again but this time capturing the propagation delay of the output after the enable signal changes from the off to on state. The results of this simulation are summarized in Table 7.3.

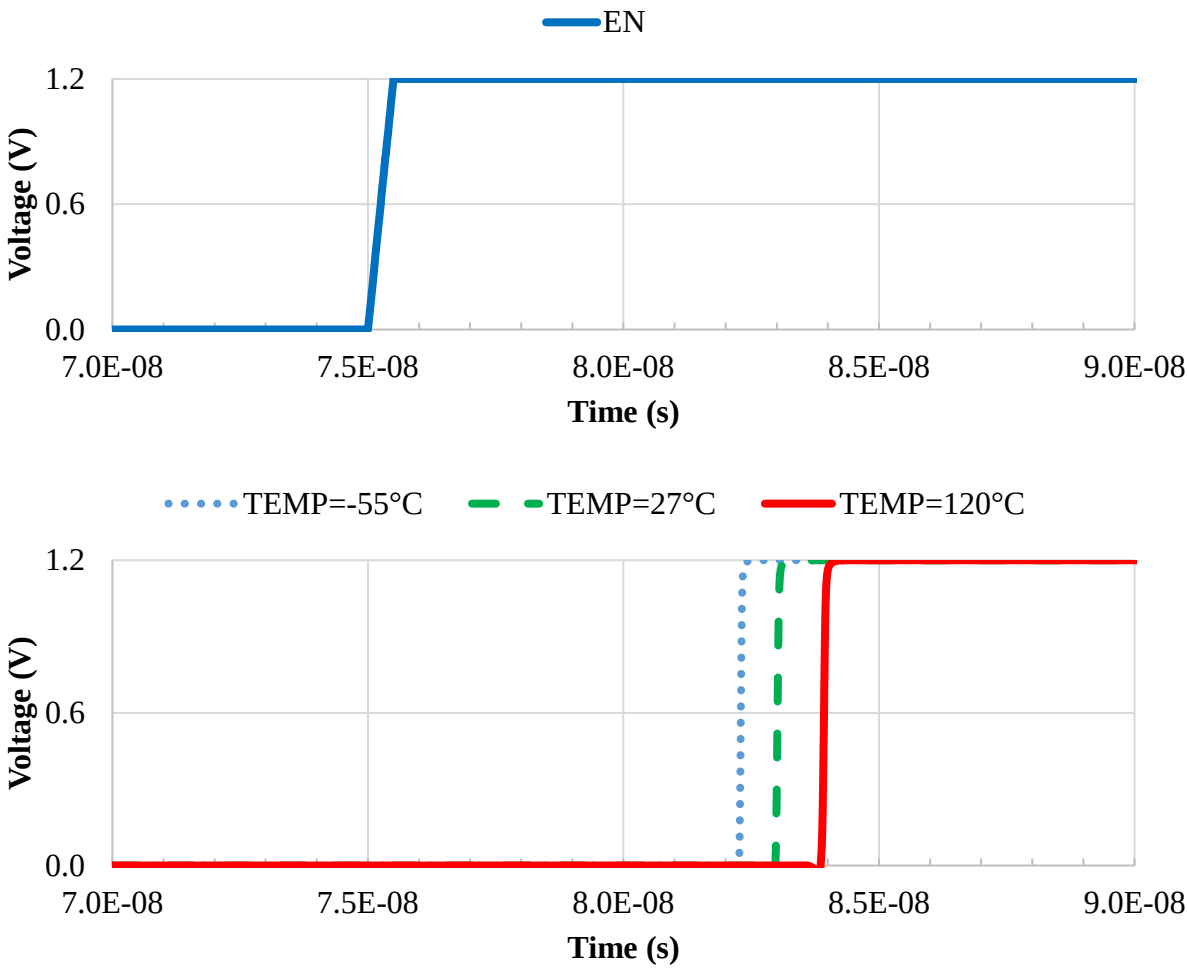


Figure 7.4. Propagation delay of comparator after being enabled from disabled state.

Table 7.3. Propagation delay after being enabled summary.

Temperature	VOUT Rising Delay
-196°C	4.4 ns
-55°C	6.8 ns
27°C	7.5 ns
120°C	8.5 ns

These simulation results show that the simulated propagation delays are well within the specification which called for a maximum of 15 ns delay.

7.4 Simulated Power Results

The next simulation that was run was to simulate the power usage of the comparator. The comparator enable signal was set to a digital "0" and the current drain of the comparator was captured while the bias circuits and output were disabled. Then, the comparator enable signal was set to a digital "1" and the current drain of the comparator was measured while the comparator was fully on. This was done at the temperature points of -196°C, -55°C, 27°C, and 120°C. The results of this simulation are summarized in Table 7.4.

Table 7.4. Simulated current drain of comparator when AVDD_1P5V is connected to 1.2 V.

Temperature	EN = 0		EN = 1	
	Current	Power	Current	Power
-196°C	1.10 µA	1.32 µW	134.01 µA	160.81 µW
-55°C	0.68 µA	0.82 µW	105.01 µA	126.01 µW
27°C	0.93 µA	1.12 µW	110.34 µA	132.41 µW
120°C	1.74 µA	2.09 µW	105.39 µA	126.47 µW

The simulated current drain of the comparator is about was expected. Although no specific power amount was specified in the design of the comparator, this amount of power use is similar to the power drain of similar comparators in previous SiGe process nodes. For example, the SiGe comparator in [5] has an output steady state power that varied from 112 µW to 193 µW across temperature. This is slightly disappointing since the 9HP process has a lower supply voltage (1.2 V compared to 3.3 V) than the comparator in [5]. However, the extra steady state current is unavoidable due to the extra stages and the differential output of this comparator which demands twice the current in everything but the input stage.

Chapter 8 - Testing Results

To test the comparator at room temperature (25°C), the fabricated test chips were packaged and placed on a breakout board. Input was provided by a Tektronix waveform generator and the measurements were taken with Tektronix oscilloscope. The room temperature test setup for the comparator test chip is shown in Figure 8.1.

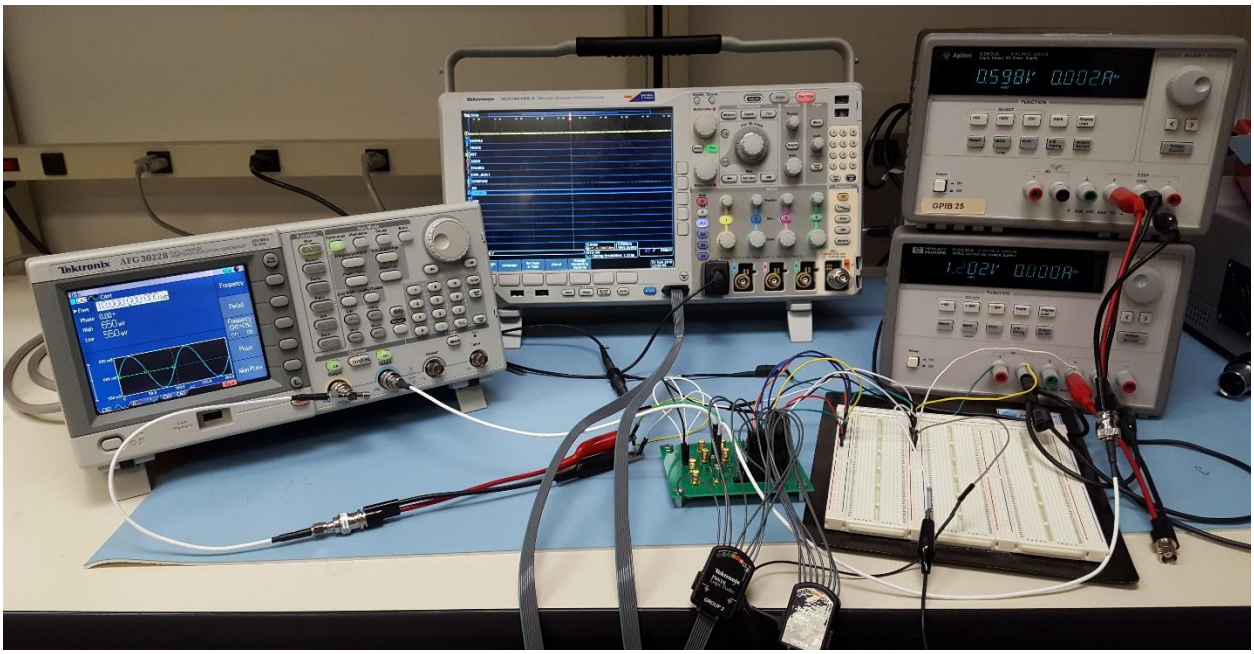


Figure 8.1. Test setup for comparator.

To test the usability of the comparator at lower temperatures, liquid nitrogen was used to lower the temperature to as low as -175°C. For the purposes of testing the comparator the chip was placed in a test chamber and the temperature was brought down to -55°C and the required tests were performed on the test chip. Then, the temperature was brought down further to -175°C and the tests were performed again.

8.1 Input Offset Voltage Measurements

The first measurement that was taken was the offset voltage. A common mode voltage was applied to the VINM input of the comparator and then the comparator was given a triangle wave

input that extended from VINM-100 mV to VINM+100 mV. VINM was varied from 0.05 V to 0.55 V with a step size of 0.05 V. The output of these measurements at room temperature is shown in Figure 8.2.

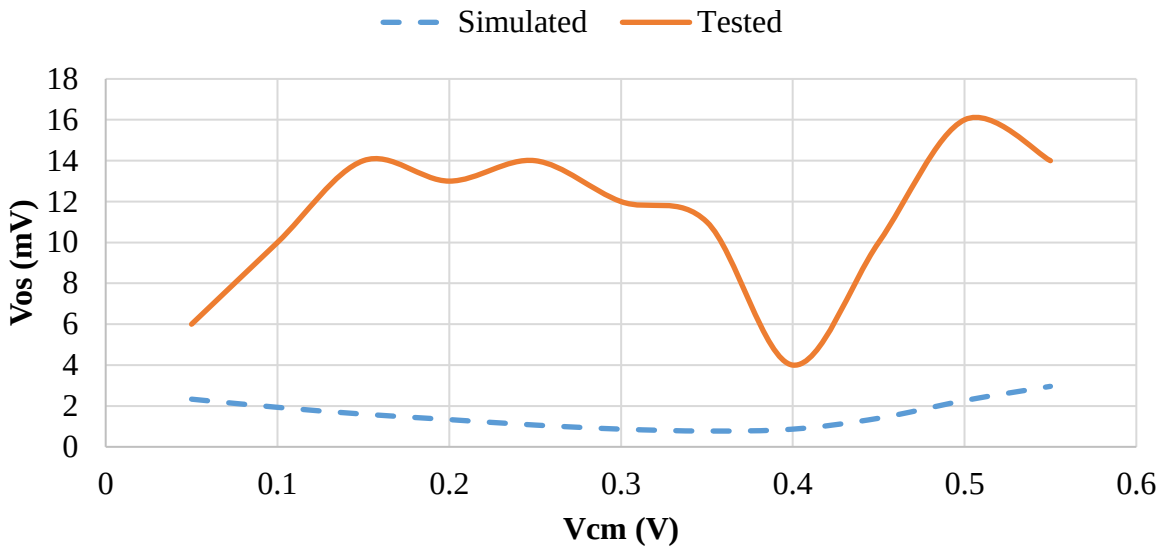


Figure 8.2. Comparison of simulated and measured offset voltage of comparator at room temperature.

Overall the test results matched some of the trends seen from the simulated results but for the most part it was much larger than what was expected. The trend that did match included having a larger offset voltage at the outer most of the usable common mode input range (0.1 V to 0.5 V). As the common mode voltage approached the middle of the range (0.3 V - 0.4 V) the offset voltage decreased as the gain of the comparator increased.

Unfortunately, the overall values of the comparator's offset were much higher in the test chip compared to the simulated version. This was likely due to random offset that occurred during the fabrication of the chip. This seems to be confirmed as the various chips that were tested each displayed a differing amount of offset. An overall comparison of the offset voltages is shown in Table 8.1.

Table 8.1. Input offset voltage results summarized.

Type	V_{OS} Best	V_{OS} Worst	V_{OS} Average
Simulated (25°C)	0.26 mV	2.96 mV	1.58 mV
Tested (25°C)	4.0 mV	16.0 mV	11.3 mV

At lower temperatures, the test chip showed no output below the 0.3 V common mode input. At both -55°C and -175°C the offset of the comparator showed this same pattern of no output below 0.3 V common mode and then increasing the offset as the common mode voltage increased. The results of the measurements are shown in Figure 8.3.

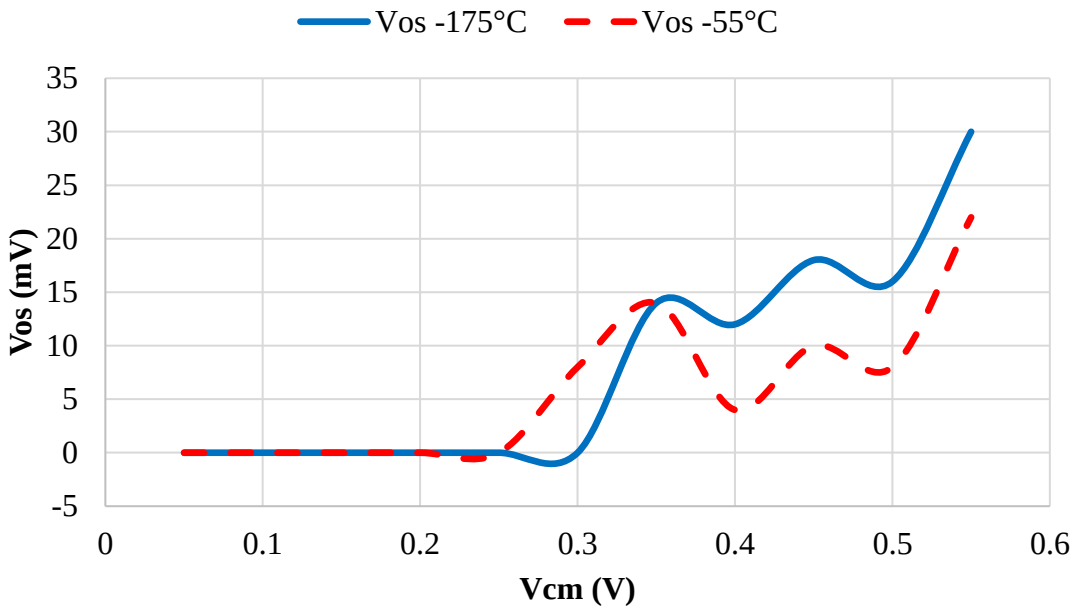


Figure 8.3. Measured voltage offset results for -55°C and -175°C.

Even though much of the data was missing at lower temperatures, the test data continued the trend of the minimum amount of offset measured at a common mode voltage of 0.4 V. Unfortunately, this offset voltage was still quite large compared to the expected values but it matched the room temperature trends and in the case of the -55°C results it was very close to the output of the room temp tests.

8.2 Propagation Delay Measurements

The second measurement that was taken was the propagation delay of the comparator. A common mode voltage was applied to the VINM input of the comparator and then a pulse wave input that extended from 0 V to 0.6 V was applied to the VINP input of the comparator. Then, the comparator was enabled by applying a digital '1' signal to the EN pin of the comparator. The total time from the EN signal turning on and the output of the comparator changing was then measured.

The faster propagation delays occur at the higher overdrive voltages and the slower propagation delays occur at lower overdrive voltages. Overall, the trends of the propagation delay were the same between the simulated and tested results. However, the propagation delay results were much slower for the test chip compared to the simulation results as shown in Table 8.2.

Table 8.2. Propagation delay results summarized.

Type	VOUT Propagation Delay Best	VOUT Propagation Delay Worst
Simulated (25°C)	1.0 ns	3.4 ns
Tested (25°C)	9.41 ns	23.4 ns
Simulated (-55°C)	0.9 ns	4.9 ns
Tested (-55°C)	24.5 ns	28.49 ns
Simulated (-175°C)	1.0 ns	4.1 ns
Tested (-175°C)	21.8 ns	32.1 ns

The amount of propagation delay for the comparator was likely much higher due to the test setup. Since there was lots of parasitic influences on outputs due to the probes it could likely have influenced the output time of the comparator.

8.3 Power Measurements

The steady state power usage of the comparator is shown in Table 8.3. The measured test results were very close to the expected steady state power output from the simulations. The main

difference was the 2.48 µW discrepancy of steady state power drain when the comparator is disabled. This is likely due to some parasitic drain in the test setup. Due to the test chamber set up, the power drain was only measured at room temperature.

Table 8.3. Steady state current drain and power usage of comparator when on and off.

Type	EN = 0		EN = 1	
	Current	**Power**	**Current**	**Power**
Simulated	0.93 µA	1.116 µW	110.34 µA	132.408 µW
Tested (25°C)	3.0 µA	3.6 µW	117.0 µA	140.4 µW

Chapter 9 – Summary and Conclusion

In this thesis, the design and verification of an extreme environment comparator in a 90nm SiGe process was presented. The comparator was designed using a "BiPMOS" approach of only using Heterojunction Bipolar Transistor devices and PFET devices in the radiation sensitive analog stages. This design decision was taken because of the inherent radiation hardness of these devices compared to the NFET devices of the process that are more susceptible to radiation damage. The comparator topology was comprised of three analog stages and digital buffers. The analog stages were an input stage consisting of PFET input devices and cross-coupled HBT devices, two push-pull stages that provide differential output, and two differential amplifiers that amplify the outputs of the push-pull stages.

The comparator was simulated to work at temperatures from -196°C to 125°C. In addition to this, a radiation analysis was performed on the comparator that simulated radiation strikes that could cause single event upsets in transistors. Based on these simulations, this comparator did not show any glitches at the output caused by the radiation strike.

Testing was performed on the comparator test chip at temperatures of -175°C, -55°C, and 25°C and it was demonstrated to work correctly. However, the comparator did exhibit much worse input offset voltage as well as slower propagation delay for the comparator that would make it difficult to use in its intended application of the SAR ADC. However, these results did show that the comparator would work at the extreme environment conditions of outer space.

Some of the future work that can be done with this comparator is to test the circuit with real radiation strikes to see if it prevents glitches at the output due to single event transients as well as remains operational after large doses of radiation. This would verify its rad-hard by design philosophy and demonstrate that the process and design steps chosen for this circuit were sound.

In terms of the comparator usage in the SAR ADC, it was found that the large offset voltage would make it difficult to get accurate conversions from the ADC. To counter these effects, it will be necessary to implement some sort of offset compensation network. There are examples of this that use capacitor networks to counter the effects of the input offset voltage of the comparator [6]. By designing another comparator circuit in the future that adds this functionality it would be possible to get better results from a future data converter that is built with this comparator.

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