5-2018

Application of Modular Multilevel Converters (MMC) Using Phase-Shifted PWM and Selective Harmonic Elimination in Distribution Systems

Thouhidul Islam
University of Arkansas, Fayetteville

Application of Modular Multilevel Converters (MMC) Using Phase-Shifted PWM and Selective Harmonic Elimination in Distribution Systems

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

by

Thouhidul Islam
Bangladesh University of Engineering and Technology
Bachelor of Science in Electrical Engineering, 2012

May 2018
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

_____
Juan C. Balda, PhD
Thesis Director

_____
Roy A. McCann, PhD
Committee Member

_____
Yue Zhao, PhD
Committee Member

ABSTRACT

Reducing the size and weight of a power electric system is a prodigious challenge to researchers as the development of the latest technologies emerge in the field of electrical engineering. A similar urge is there to develop a light-weight mobile power substation (MPS) to use in the electric power distribution systems during emergency conditions. This thesis proposes a power electronics based solution using the modular multilevel converter (MMC) topology to design the MPS system. The market-available power semiconductor devices are analyzed and suitable devices are selected to design the system. The phase-shifted pulse width modulation (PS-PWM) and selective harmonic elimination (SHE) switching algorithms are selected to modulate the MMC terminals. To validate the proposed techniques simulation files are built in MATLAB/SIMULINK^{TM}. Simulation results are presented and analyzed to verify the theoretical claims. These simulation results prove the feasibility of designing the MPS system with the proposed techniques.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my advisor, Dr. Juan C. Balda, for his guidance and inspiration throughout my Master's degree. His constructive advices and critiques aided me progress my research in a timely manner. I would also like to thank my thesis committee members Dr. Roy A. McCann and Dr. Yue Zhao.

The work accomplished for this thesis was supported by the consortium "Grid-Connected Advanced Power Electronics" popularly known as "GRAPES". I would like to express my gratitude for their financial support for pursuing my graduate studies.

Finally, I would like to thank my loving parents, my elder brothers, sister and my caring wife for being a source of inspiration all the way.

DEDICATION

This MSEE thesis is dedicated to my parents, my elder brothers A. H. M. Kamal, and Riadul Islam, my only sister Shahana Akter and my wife Taslima Akter. I would not have accomplished this degree without your continuous help and support.

TABLE OF CONTENTS

1 INTRODUCTION 1
1.1 Introduction 1
1.2 Overview of the MPS System 2
1.3 Objectives of the Thesis 4
1.4 Organization of the Thesis 5
1.5 References 6
2 MODULAR MULTILEVEL CONVERTER FUNDAMENTALS 8
2.1 Introduction 8
2.2 Basic Structure and Operating Principle of the MMC 8
2.3 Parameter Selection of the MMC 11
2.3.1 Phase Power 11
2.3.2 Capacitor Selection 13
2.3.3 Inductor Selection 14
2.4 Design Example 15
2.5 Conclusions 16
2.6 References 17
3 SELECTION OF POWER SEMICONDUCTOR DEVICES FOR MMC TERMINALS 19
3.1 Introduction 19
3.2 Conduction and Switching Loss Analysis 20
3.3 Switching Frequency Analysis 21
3.4 Selection of the IGBT Ratings 24
3.5 Conclusions 29
3.6 References 29
4 SWITCHING ALGORITHMS FOR MMC STAGES 32
4.1 Introduction 32
4.2 Phase-Shifted Pulse Width Modulation 34
4.3 Selective Harmonic Elimination 36
4.4 Conclusions 43
4.5 References 44

5 CONTROLLER DESIGN FOR MMC STAGES 48
5.1 Introduction 48
5.2 Active and Reactive Power Controllers 49
5.3 Rectifier DC Voltage Controllers 50
5.4 Inverter Current Controllers 54
5.5 SM Capacitor Voltage Balancing 59
5.5.1 Average voltage controller for the SM capacitors 59
5.5.2 Instantaneous voltage controller of the SM capacitors 61
5.5.3 Average voltage balancing controller of the arm 62
5.6 Generation of the Reference Voltages for the PS-PWM Algorithm 62
5.7 Matlab/Simulink™ Models Used for Generating Switching Signals 63
5.8 Switching Signal Generation for The SHE Algorithm 68
5.9 Conclusions 68
5.10 References 69
Appendix A.1 71
Appendix A.2 74
Appendix A.3 75
6 SIMULATION RESULTS OF THE MPS SYSTEM 77
6.1 Introduction 77
6.2 PS-PWM Based Operation 79
6.3 SHE Based Operation 86
6.4 MPS Operation 92
6.5 Conclusions 96
6.6 References 97
7 CONCLUSIONS AND RECOMMENDATIONS FOR THE FUTURE WORK 98
7.1 Conclusions 98
7.2 Recommendations for the Future Work 100

LIST OF FIGURES

Fig. 1.1: The MPS system under consideration 3
Fig. 2.1: Basic structure of a three-phase MMC terminal 9
Fig. 2.2: Schematic of a HBSM 10
Fig. 2.3: Theoretical output voltage of an MMC inverter terminal 11
Fig. 2.4: Ideal model of a three-phase MMC terminal 12
Fig. 3.1: Thermal representation of IGBT module 22
Fig. 3.2: Schematic diagram of a heat pipe 24
Fig. 3.3: The MPS system under consideration 25
Fig. 4.1: PS-PWM for a five-level converter 35
Fig. 4.2: A three-phase MMC terminal 36
Fig. 4.3: Graphical representation of the state signal of SM 38
Fig. 4.4: Pulse pattern for a SM 40
Fig. 5.1: Block diagram for the active and reactive power controllers 50
Fig. 5.2: Block diagram of the rectifier dc voltage controller 51
Fig. 5.3: Step response of the rectifier dc voltage controller 52
Fig. 5.4: Bode diagram of the rectifier dc voltage controller 52
Fig. 5.5: Block diagram of the rectifier dc voltage controller with a pre-filter 53
Fig. 5.6: An inverter terminal injecting power to the grid 54
Fig. 5.7: The block diagrams of the inverter currents controllers 55
Fig. 5.8: Step response of the inverter current controller 56
Fig. 5.9: Bode diagram of the inverter current controller 57
Fig. 5.10: Block diagrams of the inverter current controllers with a pre-filter 57
Fig. 5.11: The current controller generating the signal V* 58
Fig. 5.12: A single-phase MMC terminal 60
Fig. 5.13: Average voltage controller of the SMs capacitor 61
Fig. 5.14: Instantaneous voltage controller of the SMs capacitor 61
Fig. 5.15: Average voltage balancing controller of the arm 62
Fig. 5.16: The generation of the reference voltage: (a) upper arm, (b) lower arm 63
Fig. 5.17: The model used for the calculation of the average SM capacitor voltage 64
Fig. 5.18: The model used for the average voltage controller of SM capacitor voltages 64
Fig. 5.19: The model used for the instantaneous voltage controller 65
Fig. 5.20: The model used for the arm voltage balancing controller 66
Fig. 5.21: Switching signal generation for the SMs 67
Fig. 6.1: Simulation set-up of MMC #1 terminal 78
Fig. 6.2: MMC #1 terminal voltage and current waveforms 80
Fig. 6.3: DC-link voltage and current 80
Fig. 6.4: Simulation set-up of MMC #4 terminal 81
Fig. 6.5: MMC #4 terminal voltage and current waveforms 82
Fig. 6.6: Tracking of the system active power 82
Fig. 6.7: MMC #4 terminal voltage and current waveforms with a change in load 83

Fig. 6.8: The phase and circulating current waveforms 84
Fig. 6.9: The phase and circulating current waveforms 84
Fig. 6.10: The phase and arm current waveforms 85
Fig. 6.11: SM capacitor voltage waveforms 85
Fig. 6.12: Simulation set-up of MMC #2 terminal 86
Fig. 6.13: The gate signal of the first SM of the upper arm 87
Fig. 6.14: MMC #2 terminal voltage and current waveforms 88
Fig. 6.15: MMC #2 terminal voltage and current waveforms with a change in load 88
Fig. 6.16: The simulation set-up of MMC #3 terminal 89
Fig. 6.17: MMC #3 terminal voltage and current waveforms 90
Fig. 6.18: SHE-based dc-link voltage and current waveforms 90
Fig. 6.19: SHE-based phase and arm current waveforms 91
Fig. 6.20: SHE-based SM capacitor voltage 92
Fig. 6.21: FFT analysis of output voltage 92
Fig. 6.22: The MPS simulation set-up 93
Fig. 6.23: MMC #1 terminal voltage and current waveforms in the MPS system 94
Fig. 6.24: DC- link voltages of the MPS system 95
Fig. 6.25: MMC #4 terminal voltage and current waveforms in the MPS system 95
Fig. 6.26: MMC #4 terminal behavior with a change in the power demand 96

LIST OF TABLES

Table 2.1: System and the selected parameters of a MMC terminal 16
Table 3.1: System parameters of the MPS system.....25
Table 3.2: Properties of the selected IGBT modules 27
Table 3.3: Losses of the selected IGBT modules in MMC #1 and MMC #2 terminals 27
Table 3.4: Losses of the selected IGBT modules in MMC #3 and MMC #4 terminals 27
Table 3.5: Maximum achievable switching frequencies.....28
Table 3.6: Thermal resistance of the heat sink to ambient.....28
Table 3.7: Component count for the four MMC terminals 29
Table 4.1: Calculated angles to eliminate the 5th harmonic for different modulation indexes.....43
Table 6.1: Simulation parameters of the MPS system 77
Table 6.2: Gains of the different controllers.....78
Table 6.3: Three-phase transformer parameters 93
Table 6.4: Gains of the different controllers for the MPS operation 93

CHAPTER 1

INTRODUCTION

1.1 Introduction

Applications of power electronics in power systems are gaining in popularity due to numerous exciting features that have paved the way for this revolution. Power electronics have been used extensively in the last few decades starting from high-voltage direct current (HVDC) transmission to injection of renewable energy into the grid. New areas of a power system have been explored efficiently with the help of power electronics. With the implementation of large-scale converters becoming very convenient, traditional pieces of equipment have been replaced with power electronics based solutions. Mobile power substations (MPS) are traditionally used all over the world exclusively in emergency services, new services, and temporary services. The advantages of MPSs are as follows:

- Minimal installation time
- Low installation cost
- Minimal on-site assembly
- Minimal on-site foundation
- Easily movable

Most of the MPSs are based on 50/60 Hz systems. Major drawbacks of these MPSs are their sizes and weights. Based on their power and voltage rating their sizes and weights can vary significantly. During an emergency condition these MPSs are needed to be transported by road. All the highways have a certain weight limit, for example the weight limit of the state of

Arkansas highways is 80,000 lbs [1]. If an MPS weights more than the road capacity, it needs to be transported in multiple vehicles and the transformer oil may need to be drained. The assembly of the MPS is then performed on-site. The complete process is sometimes very troublesome and time consuming requiring a significant logistic support. A power electronics based design can solve these problems by reducing the size and weight of the MPS. A description of the MPS system under consideration is provided in the next section.

1.2 Overview of the MPS System

The MPS system under consideration is the connection of two three-phase feeders having different rated voltages by a transformer to serve during emergency conditions. The transformer connects a 25 kV three-phase feeder to a 13.8 kV three-phase feeder to transfer a power up to 20 MVA. There are two different topologies available in the literatures to design this type of system: non-isolation and isolation [2]- [4]. Non-isolated back to back multilevel converters can handle the system. However, the complexity is very high in this topology as the voltage level changes significantly. In addition to that, a separate grounding system in non-isolation topology is required which increases the size and weight of the overall system. In isolation topology a solid-state transformer (SST) is used which provide the required grounding. Due to these advantages, isolated topology is selected to design the MPS system which is represented in Fig. 1.1. Two converter units working as rectifiers and two others as inverters. The transformer and its associated converters are operating at a medium frequency.

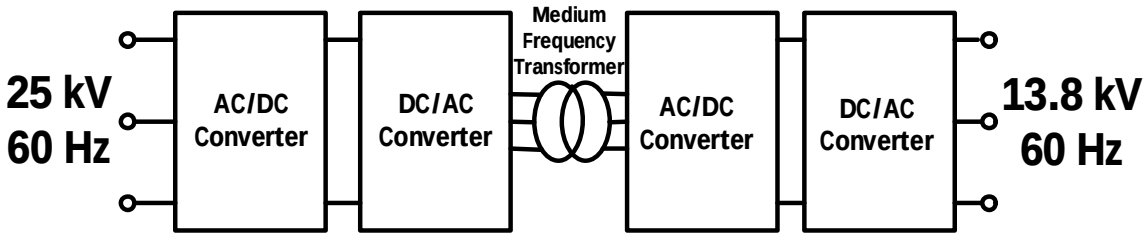

Fig. 1.1: The MPS system under consideration

The technologies that are available for these types of converter designs are Current Source Converters (CSC) and Voltage Source Converters (VSC) [5]. Generally, CSC is a thyristor based technology which is used in the power range of 1.2 GW or above [6]. The main drawbacks of this technology are requiring a strong ac system and bulky filters and only controlling the active power. VSC has some distinct advantages over the CSC technology: basically, it is a controlled switch based technology that can control the active and reactive powers independently; thus, controllability is far better than the CSC technology [7]. Due to the above advantages, VSC technology is considered in this work. However, two-level VSC technology still requires bulky filters which are overcome by using a multilevel structure [8]. The major multilevel converter topologies are diode-clamped multilevel converter, flying capacitor converter and modular multilevel converter (MMC) [9]. Diode-clamped converter is most accepted in medium-voltage applications [10]. However, voltage imbalance in the dc-link capacitor is a severe problem for this topology [10]- [16]. Availability of high-voltage diodes is another major drawback. Flying capacitor converter is also available in the market. It requires less number of switches with increased number of capacitors. With the increase in the number of levels, the capacitor count increases significantly. Balancing the capacitor voltage is also very complex [12]. The latest addition in the multilevel converter field is the MMC [17], having the following advantages [18]-[19]:

- Capable of better fault management because it can reduce the short circuit current as well as capable of isolating the system from ac side faults.
- Scalable to any desired level; thus, medium and high-voltage realizations are possible.
- Voltage stresses on the switching devices can be controlled with increasing number of levels.
- The fabrication process is much faster due to its modular design, and it is less expensive too.
- Extremely low total harmonic distortion (THD).
- Minimization of ac filters.

Thus, applications of the MMC have increased extensively due to these unique advantages. Therefore, the MMC topology is selected over the other VSC topologies in this research.

1.3 Objectives of the Thesis

The medium-voltage MPS design based on power electronics is altogether a new concept. The main goal of this thesis is to develop a solution for the above problem. The major objectives are listed below:

- A light weight solution that fulfils the road maximum weight limits.
- A compact design so that it can be transported in a single truck. It also ensures a minimal space requirement for the installation.
- A design with low total harmonic distortions.
- A reasonable efficient design.
- A cost-effective design.

The objectives are achieved by thorough analysis of the MPS system with the proposed MMC topology. Maximum achievable switching frequency for the available power semiconductor devices and losses will be calculated. Finally, a simulation model will be built in Matlab/Simulink^{TM} to evaluate the design and proposed ideas.

1.4 Organization of the Thesis

The thesis is organized chronologically with the following chapters

- Chapter 2 discusses the fundamentals of the MMC topology. Basic structure and operation principle are explained, the generalized selection procedure for passive components of the MMC are discussed.
- Chapter 3 presents the selection of the power semiconductor devices. Conduction and switching loss analyses are conducted and based on these results the operating frequency analysis is conducted. Finally, power semiconductor devices are selected based on the above calculations.
- Chapter 4 analyses the switching algorithms for the MMC stages. Two MMC stages are operating in phase shifted-pulse width modulation (PS-PWM) and the other two stages are operating under selective harmonic elimination (SHE). Fundamentals of these two algorithms are discussed in this chapter as well.
- Chapter 5 explains the controller design for the MMC stages. Controller design for PS-PWM and SHE algorithms are discussed within the chapter.
- Chapter 6 demonstrates the simulation results. Results of the PS-PWM and the SHE based MMC stages are presented separately. Finally, the results of the complete MPS system are presented.
- Finally, Chapter 7 provides the conclusions and recommendations for future work.

1.5 References

[1] Arkansas Department of Transportation, “Size and Weight Laws” Available online at: https://www.arkansashighways.com/highway_police/map21/Size_Weight.pdf

[2] G. V. T. Bascopé, and I. Barbi. "Generation of a family of non-isolated DC-DC PWM converters using new three-state switching cells," in *IEEE 31st Annual Power Electronics Specialists Conference*, vol. 2, pp. 858-863, 2000.

[3] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala. "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," in *IEEE transactions on industry applications 27*, no. 1: 63-73, 1991.

[4] D. Rothmund, G. Ortiz, Th. Guillod, and J. W. Kolar. "10kV SiC-based isolated DC-DC converter for medium voltage-connected Solid-State Transformers," in *Applied Power Electronics Conference and Exposition (APEC), IEEE*, pp. 1096-1103, 2015.

[5] J. Arrillaga, Y.H. Liu, and N.R. Watson *Flexible Power Transmission, The HVDC Options*, West Sussex: John Wiley & Sons 2007.

[6] R. Rudervall, J. Charpentier, and R. Sharma, “High voltage direct current (HVDC) transmission systems technology review paper,” *Energy Week*, pp. 7-8, 2000.

[7] M.P. Bahrman, B.K. Johnson, "The ABCs of HVDC transmission technologies," *Power and Energy Magazine, IEEE*, vol. 5, no. 2, pp. 32-44, 2007.

[8] A. M. Abbas, P.W. Lehn, "PWM based VSC-HVDC systems — A review," *Power & Energy Society General Meeting, PES '09. IEEE*, pp. 1-9, 2009.

[9] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, Bin Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent Advances and Industrial Applications of Multilevel Converters," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553-2580, 2010.

[10] G. P. Adam, Olimpo Anaya-Lara, Graeme Burt, and J. R. McDonald. "Comparison between flying capacitor and modular multilevel inverters," *in 35th Annual Conference of the IEEE Industrial Electronics Society–IECON Porto, Portugal*. 2009.

[11] M. Saeedifard, R. Iravani, and J. Pou. "Analysis and control of DC-capacitor-voltage-drift phenomenon of a passive front-end five-level converter," in *IEEE Transactions on Industrial Electronics* 54, no. 6, pp. 3255-3266, 2007.

[12] J. S. Lai and F. Z. Peng, “Multilevel Converter–A New Breed of Power Converters,” in *IEEE Transactions on Industry Applications, Vol. 32, No. 3*, pp. 509-517, 1996.

[13] M. Marchesoni, M. Mazzucchelli, F. V. P. Robinson, and P. Tenca. "A minimum-energy-based capacitor voltage balancing control strategy for MPC conversion systems," in *Industrial Electronics, 1999. ISIE'99. Proceedings of the IEEE International Symposium on*, vol. 1, pp. 20-25. IEEE, 1999.

[14] G. Sinha and T. A. Lipo, "A Four-Level Rectifier-Inverter System for Drive Applications," in *IEEE Industry Applications Magazine*, pp. 66-74, 1998.

[15] C. Newton and M. Sumner, "Multilevel Converter: A Real Solution to Medium/High-Voltage Drives," in *IEE Power Engineering Journal, Vol. 12, Issue 1*, pp. 21-26, 1998.

[16] J. Pou, R. Pindado, and D. Boroyevich. "Voltage-balance limits in four-level diode-clamped converters with passive front ends," in *IEEE Transactions on Industrial Electronics* 52, no. 1, pp. 190-196, 2005.

[17] A. Lesnicar and R. Maruardt, "An Innovative Modular Multilevel Converter Topology Suitable for a Wide Power Range," in *IEEE Power Tech Conference, Vol. 3, Bologna, Italy*, pp. 23-26, 2003.

[18] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, M.A.M. Prats, "The age of multilevel converters arrives," in *Industrial Electronics Magazine, IEEE*, vol. 2, no. 2, pp. 28-39, 2008.

[19] M. Hagiwara and H. Akagi, "PWM Control and Experiment of Modular Multilevel Converters," in *IEEE Power Electronics Specialists Conference*, pp. 154-161, 2008.

CHAPTER 2

MODULAR MULTILEVEL CONVERTER FUNDAMENTALS

2.1 Introduction

The Modular Multilevel Converter (MMC) is the latest breed of converters used in medium and high-voltage applications [1]- [2]. It has distinguished advantages over other types of voltage source converters such as flying capacitor converter (FCC) and diode clamped converter as mentioned in Chapter 1. The fundamentals of the MMC topology will be presented in this chapter. Initially, its basic structure and operating principle will be analyzed with simple circuit representations. The passive components selection procedure will be analyzed subsequently. Finally, the passive components will be calculated using a procedure explained for a MMC terminal.

2.2 Basic Structure and Operating Principle of the MMC

The MMC consist of several submodules (SM), which are the building blocks. There are three topologies that have been proposed so far, the half-bridge SM (HBSM), full-bridge SM (FBSM), and clamp double SM (CDSM) [3]. One of the motivating factors of this research was to design a system with minimal weight. Therefore, the HBSM structure considered here has a lower component count and higher efficiency. However, the HBSM structure is unable to block dc side faults without the help of a breaker [4]. A basic structure of a three-phase MMC terminal is presented in Fig. 2.1. The SM topology is shown in Fig. 2.2. Each phase of the MMC is termed a "leg" and each leg has one "upper arm" and one "lower arm". Each arm consists of N SMs; thus, a total number of $6N$ SMs are required to form a three-phase MMC terminal. Positive current

charges the SM capacitor whereas negative current discharges the SM capacitor. The inductors *La* are required to minimize the circulating currents.

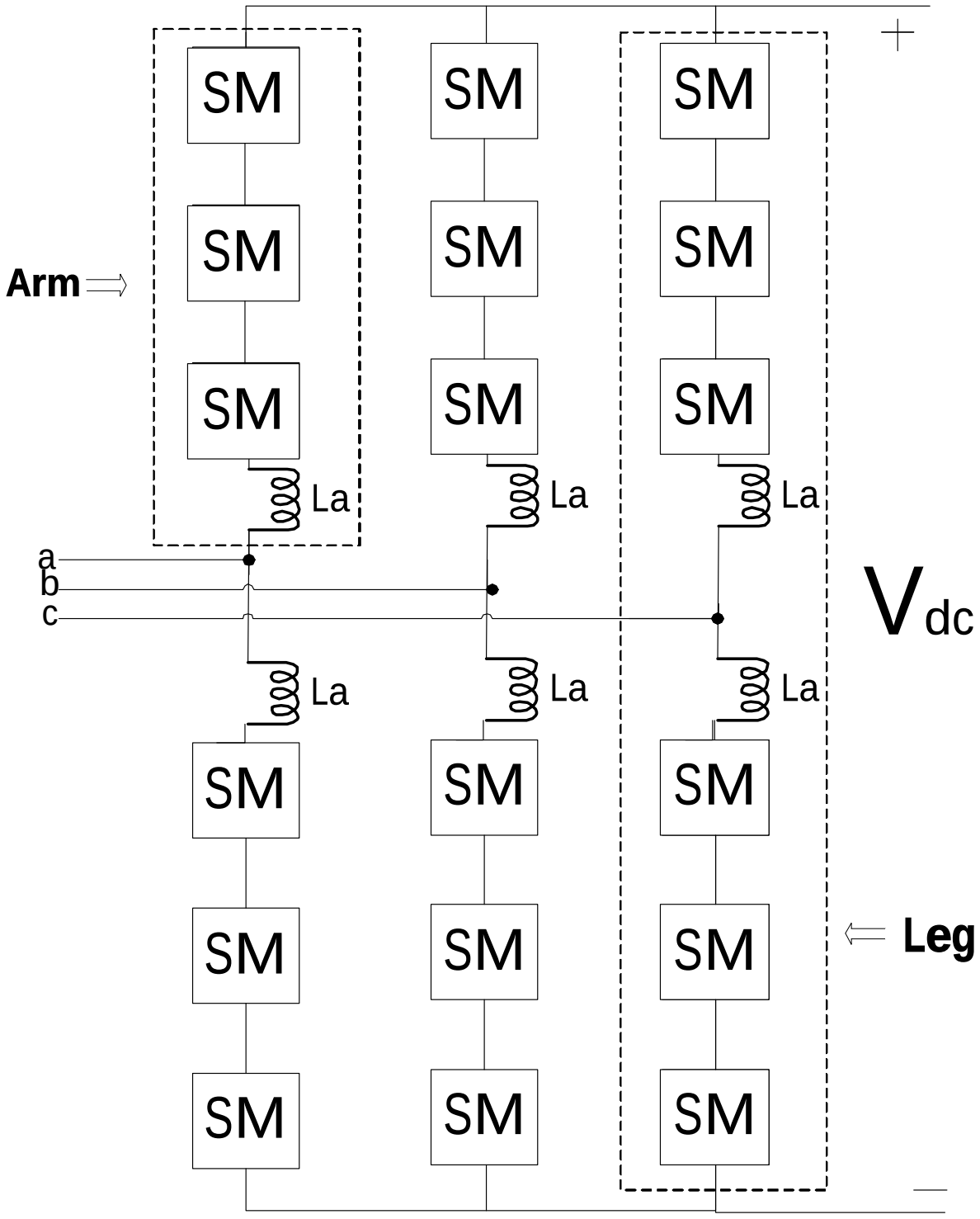

Fig. 2.1: Basic structure of a three-phase MMC terminal

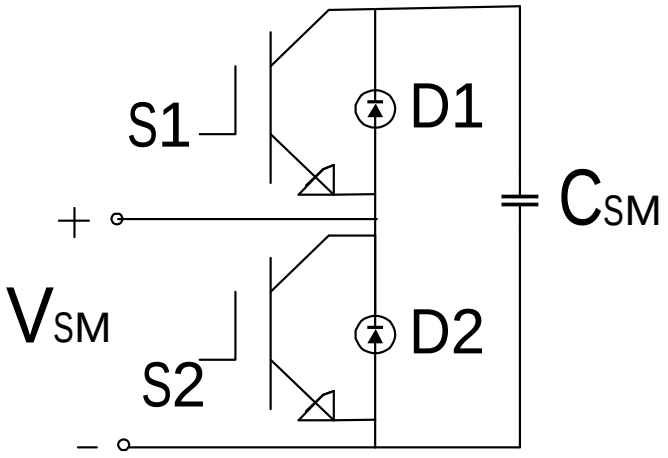

Fig. 2.2: Schematic of a HBSM

The MMC operates by inserting or bypassing the SM capacitor and forming the desired output voltage in a staircase shape [5]. The number of levels of this staircase is equal to the number of SM per arm. The SM capacitor is inserted when switch S1 is on (current flows out of the SM), and bypassed when switch S2 is on (current does not flow in to the SM). Freewheeling diodes take care of the current when both switches are turned off. Switches S1 and S2 operate in a complementary manner. Thus, both switches cannot be turned on at the same time. Moreover, when an upper arm SM is inserted a lower arm SM is bypassed and vice versa. Thus, the operations of the upper and lower arms are also complementary to each other [6]. It ensures that the total number of inserted SMs is always N. Therefore,

$$N_{on} = n_{up} + n_{bottom} = N \tag{2.1}$$

where N_{on} is the total number of inserted SMs, n_{up} represents the total number of inserted SMs in the upper arm and n_{bottom} represents the total number of inserted SMs in the lower arm. These N number of SMs hold the full dc-link voltage across the MMC leg. A typical seven level MMC output voltage is represented in Fig. 2.3.

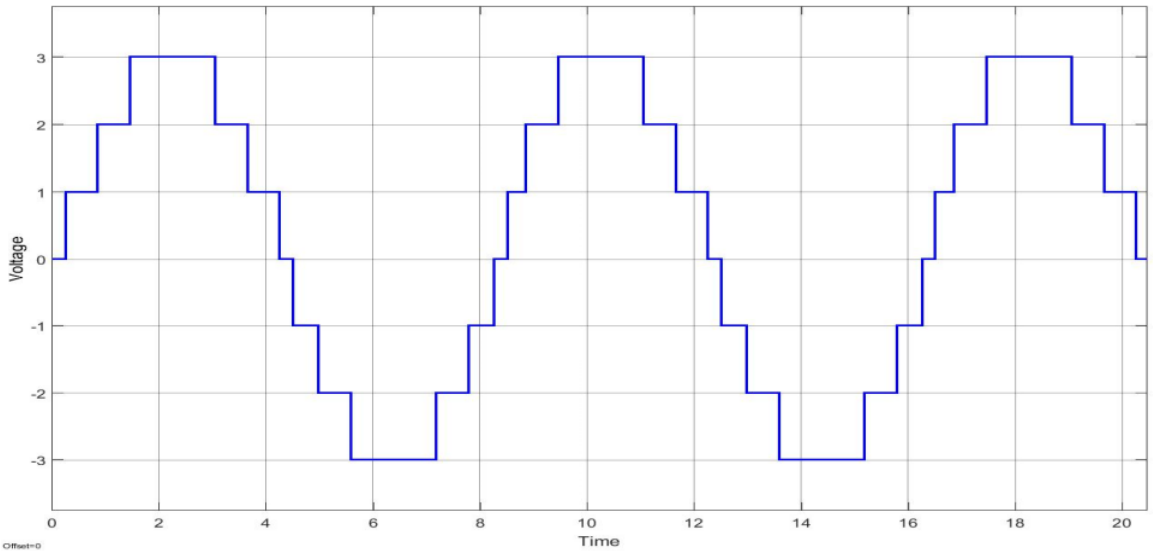

Fig. 2.3: Theoretical output voltage of an MMC inverter terminal

2.3 Parameter Selection of the MMC

The passive component selection is one of the major tasks for any electrical and electronic system; however, it is complicated for an MMC system. An arm of the MMC has two passive components, an SM capacitor, an arm inductor including its resistance. The SM capacitor stores the energy whereas the arm inductor controls the circulating current. A large number of literature [7]- [12] have discussed the selection process of these passive components, which are analyzed in this section.

2.3.1 Phase Power

Initially, the arm inductance is neglected when determining the size of the SM capacitor. An infinite number of SMs is assumed. Thus, they behave as ideal voltage sources as represented in Fig. 2.4. Assuming sinusoidal phase currents, Kirchhoff's current law is used to define the upper arm current as [12] (Fig. 2.4):

$$i_{au}(t) = \frac{1}{3}I_{dc} + \frac{1}{2}i_a(t) = \frac{1}{3}I_{dc} + \frac{1}{2}\hat{I}_a \sin(\omega_0 t + \varphi) \quad (2.2)$$

where ω_0 is the fundamental angular frequency of the system in radians per second, φ is the phase displacement between the arm voltage and current, and $\hat{I}_a$ is the peak phase current. As the upper and lower arms are symmetrical the phase current also spilt up symmetrically among the upper and lower arm currents. Kirchhoff's voltage law is applied to define the upper arm voltage as:

$$\vartheta_{au}(t) = \frac{1}{2}V_{dc} - \vartheta_a(t) = \frac{1}{2}V_{dc} - \hat{V}_a \sin(\omega_0 t) \tag{2.3}$$

where $\hat{V}_a$ is the peak phase voltage.

The relationship between the dc and ac variables are defined by [10]:

$$m = \frac{3}{2}\frac{\hat{I}_a}{I_{dc}} \tag{2.4}$$

$$k = 2\,\frac{\hat{V}_a}{V_{dc}} \tag{2.5}$$

The model is considered ideal and lossless; therefore, the dc side power should be equal to the ac side power:

$$P_{dc} = V_{dc}I_{dc} = 3\,\frac{1}{2}\hat{V}_a\hat{I}_a\cos\varphi \tag{2.6}$$

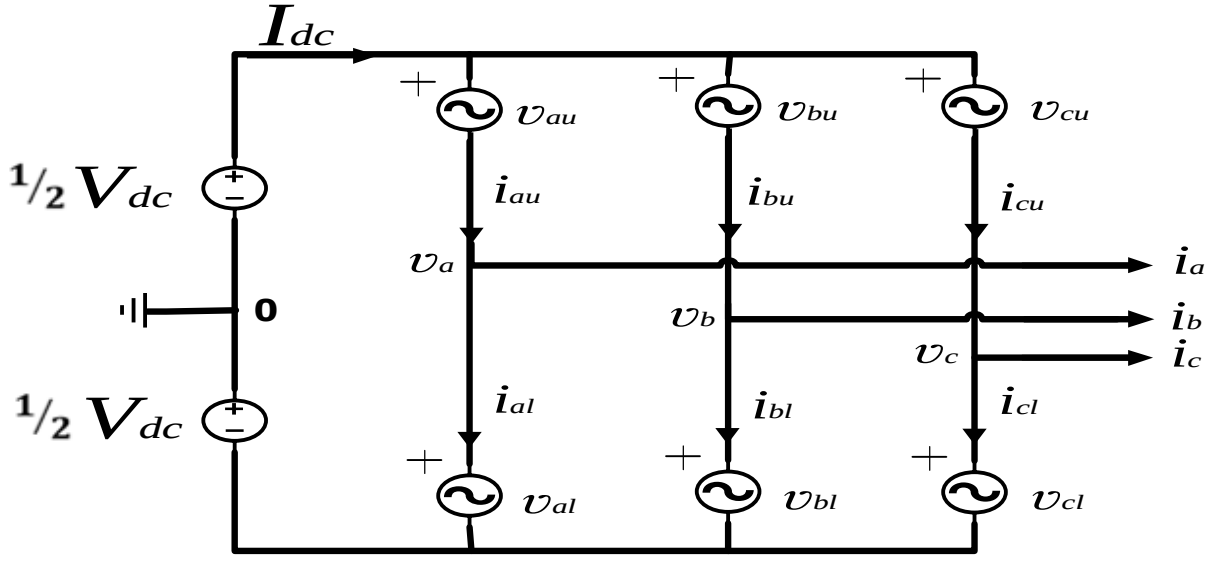

Fig. 2.4: Ideal model of a three-phase MMC terminal

Using (2.4), (2.5), and (2.6), the relation between m and k is derived as follows [7]:

$$m = \frac{2}{k\cos\varphi} \tag{2.7}$$

Using these new variables in (2.2) and (2.3), the arm current and arm voltage are expressed by:

$$i_{au}(t) = \frac{1}{3} I_{dc}[1 + m\sin(\omega_0 t + \varphi)] \tag{2.8}$$

$$\vartheta_{au}(t) = \frac{1}{2} V_{dc}[1 - k\sin(\omega_0 t)] \tag{2.9}$$

Power in each arm is calculated by multiplying (2.8) and (2.9) yielding:

$$P_{au}(t) = \frac{1}{6} P_{dc}[1 + m\sin(\omega_0 t + \varphi)][1 - k\sin(\omega_0 t)] \tag{2.10}$$

$$= \frac{1}{6} P_{dc}\,[m\sin(\omega_0 t + \varphi) - k\sin(\omega_0 t) + \frac{1}{2} m\,k\cos(2\omega_o t + \varphi)]$$

2.3.2 Capacitor Selection

Pulsation energy ΔW can be obtained by integrating (2.10) using the following limits [7]:

$$x_1 = -\varphi - \arcsin\left(\frac{1}{m}\right) \tag{2.11}$$

$$x_2 = \pi + \arcsin\left(\frac{1}{m}\right) - \varphi \tag{2.12}$$

The pulsation energy then become:

$$\Delta W = \frac{1}{\omega_0} \int_{x_1}^{x_2} P_{au}(\omega_0 t)\,d\omega_0 t$$

$$= \frac{P_{dc}}{6\omega_0}\left[2m\frac{\sqrt{m^2-1}}{m} - 2k\frac{\sqrt{m^2-1}}{m}\cos\varphi + \frac{2\sqrt{\frac{m^2-1}{m}}}{m}\right]$$

$$= \frac{2P_{dc}}{3k\omega_0\cos\varphi}\left[1 - \left(\frac{k\cos\varphi}{2}\right)^2\right]^{\frac{3}{2}} \tag{2.13}$$

The change of energy in each SM is obtained by:

$$\Delta W_{SM} = \frac{2P_{dc}}{3Nk\omega_0\cos\varphi}\left[1 - \left(\frac{k\cos\varphi}{2}\right)^2\right]^{\frac{3}{2}} \tag{2.14}$$

The energy stored in each capacitor can be represented by [7]:

$$\frac{1}{2} C_{SM} V_{SM}^2 = \frac{1}{4\varepsilon} \Delta w_{SM} \tag{2.15}$$

Finally, SM capacitance can be calculated by:

$$C_{SM} = \frac{P_{dc}}{3\varepsilon N k \omega_0 V_{SM}^2 cos\varphi} [1 - \left(\frac{k cos\varphi}{2}\right)^2]^{\frac{3}{2}} \tag{2.16}$$

where ε is the ripple factor of the SM capacitor voltage, which lies in between 0 to 0.5, and V_{SM} is the average SM voltage.

2.3.3 Inductor Selection

The arm inductor selection is related to the circulating current or the resulting voltage difference across it. Sizing the arm inductor is very important because circulating currents will be too large to handle if it is too small. These high currents can damage the switching devices. If selected too low, the voltage difference across it will be very high and very difficult to balance. The circulating current can be expressed as:

$$i_{za} = \frac{1}{2}(i_{au} + i_{al}) \tag{2.17}$$

The voltage difference across the arm inductor is defined by [13]:

$$v_{diff} = 2R_a i_{za} + 2 L_a \frac{d}{dt} i_{za} \tag{2.18}$$

where R_a is the arm inductor resistance and L_a is the arm inductance. Neglecting the resistance, (2.18) can be rewritten as:

$$v_{diff} = 2 L_a \frac{d}{dt} i_{za} \tag{2.19}$$

The circulating current has a prominent second-order harmonic I_{2f} which contributes in the selection of the arm inductance which is sized using [11]:

$$L_a = \frac{1}{8\omega_0^2 C_{SM} V_c}\left(\frac{P_{dc}}{3\cos\varphi I_{2f}} + V_{dc}\right) \tag{2.20}$$

where V_C is the dc component of the SM capacitor voltage and I_{2f} is the peak value of the double-fundamental-frequency circulating current. Equation (2.20) was derived by assuming that L_a< 0.02 p.u [11]. A value of 2% was selected as the inductance. The percent impedance is calculated as follows:

$$\%\ \mathrm{L} = \frac{2\pi f_0 I_a L_a}{V_a} \times 100\ \% \tag{2.21}$$

where I_a is the rms line current, V_a is the rms phase to neutral voltage and f_0 is the fundamental frequency.

2.4 Design Example

The system explained in chapter 1 is used to determine the SM capacitance, and the arm inductance. The system parameters used to determine these passive components are listed in Table 2.1. The SM capacitance value is calculated using (2.16) with a ripple factor of 0.1. The arm inductance is calculated using (2.21). The second-order circulating current is then calculated using (2.20). These calculated values are also listed in the Table 2.1.

Table 2.1: System and the selected parameters of a MMC terminal

Parameter	Values
Power rating, S	6 MVA
Line-to-line rms voltage, v_{LL}	25 kV
Line current, I_a	138.56 A
Phase-to-neutral voltage, V_a	14.43 kV
DC-Link voltage, V_{dc}	44 kV
Number of levels	11
Average SM capacitor voltage, V_{SM}	4 kV
Operating frequency, f	60 Hz
SM capacitance, C_{SM}	293 μF
Arm inductance, L_a	8.29 mH
Second-order circulating current, I_{2f}	182.6 A

2.5 Conclusions

MMC has many exciting features to meet the requirements of medium and high-voltage system design. It is capable to reduce the THD of the output voltage as it produces a staircase voltage; thus, it eliminates the requirements for large ac side filters found in line-commutated converter terminals. The HBSM is selected as it has a lower component count and higher efficiency than other configurations. The next chapter will describe the selection procedure of the power semiconductor devices.

2.6 References

[1] G. P. Adam, Olimpo Anaya-Lara, Graeme Burt, and J. R. McDonald. "Comparison between flying capacitor and modular multilevel inverters," *in 35th Annual Conference of the IEEE Industrial Electronics Society–IECON Porto, Portugal*. 2009.

[2] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, M.A.M. Prats, "The age of multilevel converters arrives," in *Industrial Electronics Magazine, IEEE,* vol. 2, no. 2, pp. 28-39, June 2008

[3] R. Marquardt, "Modular Multilevel Converter: An universal concept for HVDC-Networks and extended DC-Bus-applications," in *Proceedings of Power Electronics Conference (IPEC), 2010 International*, pp. 502-507, 2010. 25

[4] S. Kenzelmann, A. Rufer, M. Vasiladiotis, D. Dujic, F.Canales, Y. R. de Novaes, "A Versatile DC-DC Converter for Energy Collection and Distribution using the Modular Multilevel Converter", in *EPE Conference Birmingham*, 2011.

[5] E. Abildgaard, Exploring the Properties of a Modular Multilevel Converter Based HVDC Link. With Focus on Voltage Capability, Power System Relations, and Control System, M.S. Thesis, Department Electric Power Engineering, Norwegian University of Science and Technology, Norway.2012.

[6] E. Solas, G. Abad, J. A. Barrena, A. Cárcar, and S. Aurtenetxea, "Modulation of Modular Multilevel Converter for HVDC application," in *Proceedings of Power Electronics and Motion Control Conference (EPE/PEMC), 14th International*, pp. T2- 84- T2- 89, 2010.

[7] R. Marquardt, A. Lesnicar, and J. Hildinger. "Modulares stromrichterkonzept für netzkupplungsanwendung bei hohen spannungen," in *ETG-Fachtagung, Bad Nauheim, Germany 114*, 2002.

[8] M. Vasiladiotis, Analysis, Implementation and Experimental Evaluation of Control Systems for a Modular Multilevel Converter, M.S. Thesis, Department. Electrical. Engineering, Royal Institute of Technology, Stockholm, Sweden 2009.

[9] L. M. Cunico, G. Lambert, R. P. Dacol, S. V. G. Oliveira, and Y. R. de Novaes. "Parameters design for modular multilevel converter (MMC)," in *Power Electronics Conference (COBEP)*, pp. 264-270. IEEE, 2013.

[10] Y. Zhang, G. P. Adam, T. C. Lim, S. J. Finney, and B. W. Williams, "Analysis and experiment validation of a three-level modular multilevel converters," in *Proceedings of IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE & ECCE)*, pp. 983- 990. 2011.

[11] Q. Tu, Z. Xu, H. Huang, and J. Zhang. "Parameter design principle of the arm inductor in modular multilevel converter based HVDC," in *International Conference on Power System Technology (POWERCON)*, pp. 1-6, 2010.

[12] Y. Zhang, G. P. Adam, T. C Lim, S. J. Finney, and B. W. Williams, “Mathematical Analysis and Experimet Validation of Modular Multilevel Converters,” in *Journal of Power Electronics*, vol. 12, no. 1, pp. 33, 39, 2012.

[13] A. Antonopoulos, L. Angquist, H.P. Nee, "On dynamics and voltage control of the Modular Multilevel Converter," in *Proceedings of 13th European Conference on Power Electronics and Applications*, EPE '09. pp. 1-10 Sept. 2009.

CHAPTER 3

SELECTION OF POWER SEMICONDUCTOR DEVICES FOR MMC TERMINALS

3.1 Introduction

Suitable selection of the power semiconductor devices is the most important task for any power electronic system, since the rating of the switching device determines the minimum number of levels required in the power electronic converter. The selection depends largely on the power rating, fundamental frequency, and switching frequency of the system. Thermal design of the whole system also contributes significantly in the selection process. Examples of available popular power semiconductor devices in the market are silicon controlled rectifier (SCR), gate turn-off thyristor (GTO), insulated-gate bipolar transistor (IGBT), integrated gate-commutated thyristor (IGCT), and metal-oxide-semiconductor field-effect transistor (MOSFET). Generally, SCR and GTO are used in high-voltage and high-current applications like power transmission systems. However, both devices cannot operate at high switching frequencies [1]- [3]; so, their operation is limited to a few hundred Hz. IGCT is one of the latest additions to power semiconductor devices having few distinguishable advantages over the traditional ones. Advantages include a relatively higher overload capacity, less on-state losses, high cyclic resistance, and can also operate in the range of a few kHz. Silicon MOSFETs are used in low power applications. However, they can operate up to a few hundred kHz. MOSFET designs are continuously improving by making use of wide bandgap materials [4]. Researchers are developing silicon carbide and gallium nitride based MOSFETs instead of traditional silicon-based devices. These modified devices can operate in moderately higher power and temperature conditions. The most popular among all the semiconductor devices is the IGBT, used in almost

all power ratings as well as at high switching frequencies. Basically, they are voltage controlled devices that require very low control power; therefore, requiring very simple gate driver circuitry. In medium-voltage applications where the systems are frequently switched, IGBT performs slightly better than IGCT [5]. Due to these advantages, the IGBT is selected in this research. A variety of IGBTs having different current and voltage ratings are available in the market. In this chapter, the IGBT selection procedure will be analyzed with the help of maximum operating frequency and thermal analyses.

3.2 Conduction and Switching Loss Analysis

Typically, an IGBT module has a built-in freewheeling diode in it; thus, power is consumed by both. There are two types of losses in an IGBT module: conduction and switching. The conduction loss of the IGBT is expressed by [6]- [7]:

$$P_{CT} = V_{CE(ON)} * I_{PK}\left(\frac{1}{2\pi} + \frac{m_a cos\varphi}{8}\right) + r_{CE} * I_{PK}^2 \left(\frac{1}{8} + \frac{m_a cos\varphi}{3\pi}\right) \quad (3.1)$$

where $V_{CE(ON)}$is the collector-to-emitter voltage during conduction, I_{PK} is the peak of the operating sinusoidal current, m_a is the modulation index, $r_{CE}$is the conduction resistance between the collector and emitter, and φ is the power factor angle.

Conduction loss of the diode could be expressed by [6]- [7]:

$$P_{CD} = V_{D(ON)} * I_{PK}\left(\frac{1}{2\pi} - \frac{m_a cos\varphi}{8}\right) + r_D * I_{PK}^2 \left(\frac{1}{8} - \frac{m_a cos\varphi}{3\pi}\right) \quad (3.2)$$

where $V_{D(ON)}$ is the forward bias voltage drop across the diode and $r_D$is the conduction resistance of the diode. The total IGBT switching energy has two parts, switching on and switching off energies. Total IGBT switching energy is expressed by [7]:

$$E_{SWT} = (a + bI_{PK} + cI_{PK}^2)\frac{V_{DC}}{V_{nom}} \quad (3.3)$$

where a, b, and c are variables dependent on the characteristics of the switch and can be extracted from the characteristic waveforms of the switch. V_{DC} is the operating voltage of the switch and V_{nom} is the rated nominal voltage of the corresponding switch which is used in the datasheet to determine the values of a, b, c.

The switching loss of the IGBT is represented by [7]:

$$P_{SWT} = f_{SW}\left(\frac{a}{2} + \frac{b}{\pi} I_{PK} + \frac{c}{4} I_{PK}^2\right) \frac{V_{DC}}{V_{nom}} \tag{3.4}$$

where f_{SW} is the switching frequency of the system.

The reverse recovery energy of the diode is represented by [7]:

$$E_{RRD} = (\mathrm{a} + \mathrm{b} I_{PK} + \mathrm{c} I_{PK}^2) \frac{V_{DC}}{V_{nom}} \tag{3.5}$$

again, a, b, c are variables depending on the characteristics of the built-in freewheeling diode and can be extracted from the characteristic waveforms of that diode.

Finally, silicon diodes have the reverse recovery losses, which is represented by [7]:

$$P_{RRD} = f_{SW}\left(\frac{a}{2} + \frac{b}{\pi} I_{PK} + \frac{c}{4} I_{PK}^2\right) \frac{V_{DC}}{V_{nom}} \tag{3.6}$$

3.3 Switching Frequency Analysis

The thermal representation of an IGBT module is shown in Fig. 3.1, where, $R_{th(j-c)IGBT}$, $R_{th(c-s)IGBT}$, $R_{th(j-c)Diode}$, $R_{th(c-s)Diode}$ and $R_{th(s-a)}$ represents the IGBT thermal resistance of the junction to the case, and case to heat sink, and diode junction to case, and case to heat sink, and heat sink to ambient, respectively.

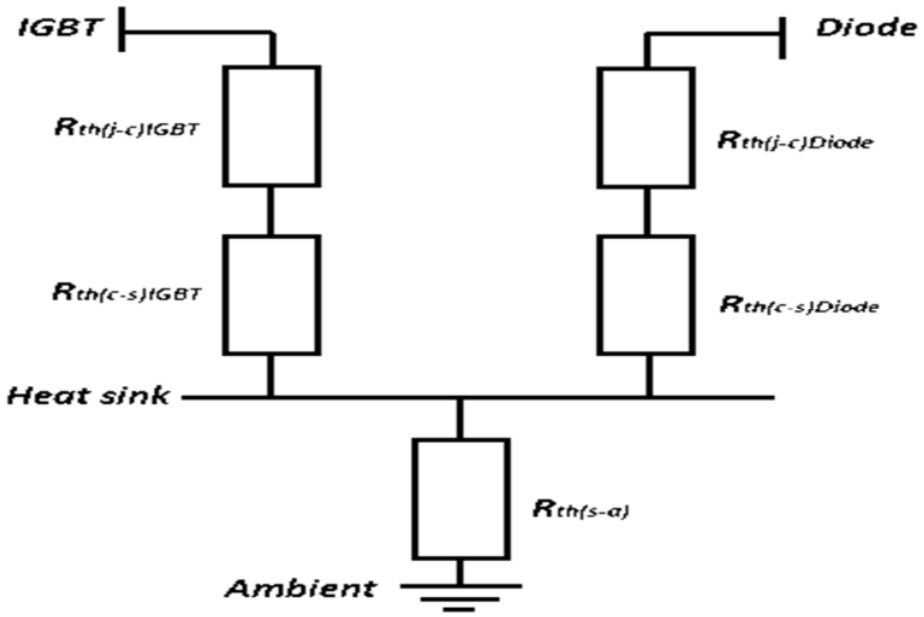

Fig. 3.1: Thermal representation of IGBT module

Junction temperature is defined by [8]:

$$T_j = T_a + \Delta T_{j-c} + \Delta T_{c-s} + \Delta T_{s-a} + 15℃ \tag{3.7}$$

where T_a represents the ambient temperature, ΔT_{j-c} represents the temperature difference between the junction and the case which is expressed as:

$$\Delta T_{j-c} = \text{total loss in IGBT} * R_{th(j-c)IGBT} \tag{3.8}$$

$$= (P_{CT} + P_{SWT}) * R_{th(j-c)IGBT}$$

Similarly, ΔT_{c-s} represents the temperature difference between the case and the heat sink which is expressed as

$$\Delta T_{c-s} = \text{total loss in IGBT} * R_{th(c-s)IGBT} \tag{3.9}$$

$$\Delta T_{c-s} = (P_{CT} + P_{SWT}) * R_{th(c-s)IGBT}$$

Finally, ΔT_{s-a} represents the temperature difference between the heat sink and ambient which is expressed as:

$$\Delta T_{s-a} = \text{total loss in IGBT module} * R_{th(s-a)} \quad (3.10)$$

$$T_S - T_a = (P_{CT} + P_{SWT} + P_{CD} + P_{RRD}) * R_{th(s-a)}$$

An additional safety margin of 15℃ is added to the calculation of junction temperature; this seems to be normal industry practice.

Maximum achievable switching frequency can be then calculated as:

$$f_{SW,\,MAX} = \left(\frac{\pi}{(E_{SWT}+E_{RRD})}\right)\left(\frac{(T_s-T_a)}{R_{th(s-a)}} - P_{CT} - P_{CD}\right) \quad (3.11)$$

$R_{th(s-a)}$ depends on the type of thermal management scheme used in the design. Traditional thermal management schemes use liquid cooling technology where water and oil are used as the coolant [9]. The major drawback of the liquid cooling system is that it requires pumps, valves, heat exchangers, etc. Therefore, a large infrastructure is required. The main goal of this research was to develop a compact and lightweight solution to the existing problem. Thus, the liquid cooling technology was not a suitable solution. Air cooling technology provides additional features not associated with the liquid cooling technology. It requires less space and minimal infrastructure, fans are used as blowers with ducting facilities, and is very cost effective.

A heat pipe scheme could be used in the air cooling system [10]. Generally, a heat pipe is a sealed vessel consisting of three sections: an evaporator, an adiabatic, and a condenser as shown in Fig. 3.2. Working fluids are required for heat exchange and may include water, methanol, or acetone. Semiconductor devices are mounted in the evaporator section.

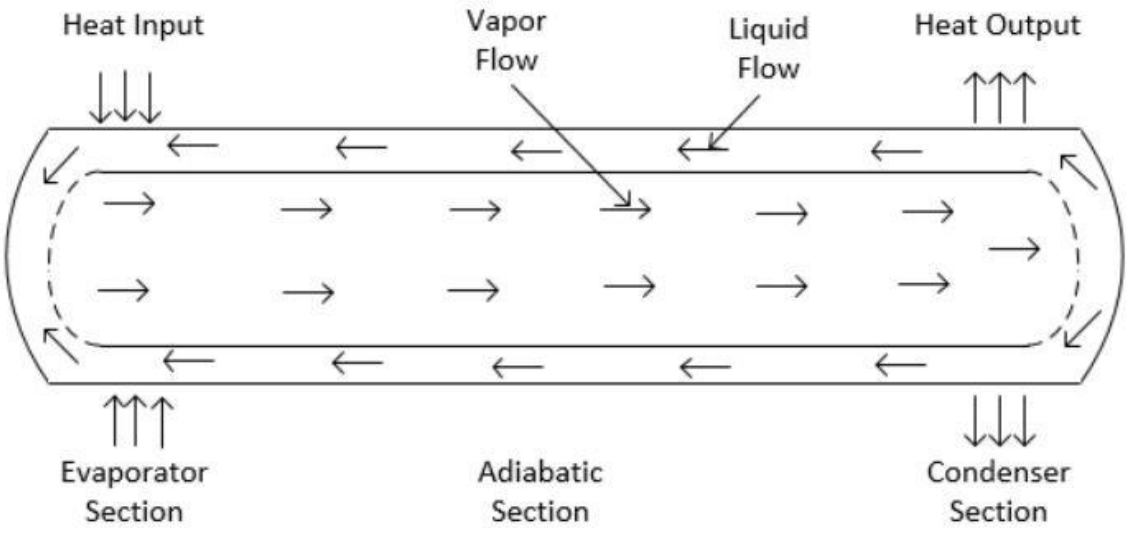

Fig. 3.2: Schematic diagram of a heat pipe

Liquid vaporizes at the evaporator section absorbing the heat generated in the device. The vapor then travels towards the condenser section through the adiabatic section with the help of fans. Finally, the generated vapor turns in to a liquid in the condenser section which is circulated towards the evaporator section again by gravity. Heat is released into the environment from the condenser. A heat pipe scheme could be considered in this research for additional advantages over the other traditional thermal management schemes.

3.4 Selection of the IGBT Ratings

The MPS system under consideration has four MMC terminals which are shown in Fig. 3.3. One capacitor-less dc-link is placed in between MMC #1 and MMC #2 and the other capacitor-less one between MMC #3 and MMC #4. The system is designed for 6 MVA. The complete system parameters are represented in Table 3.1.

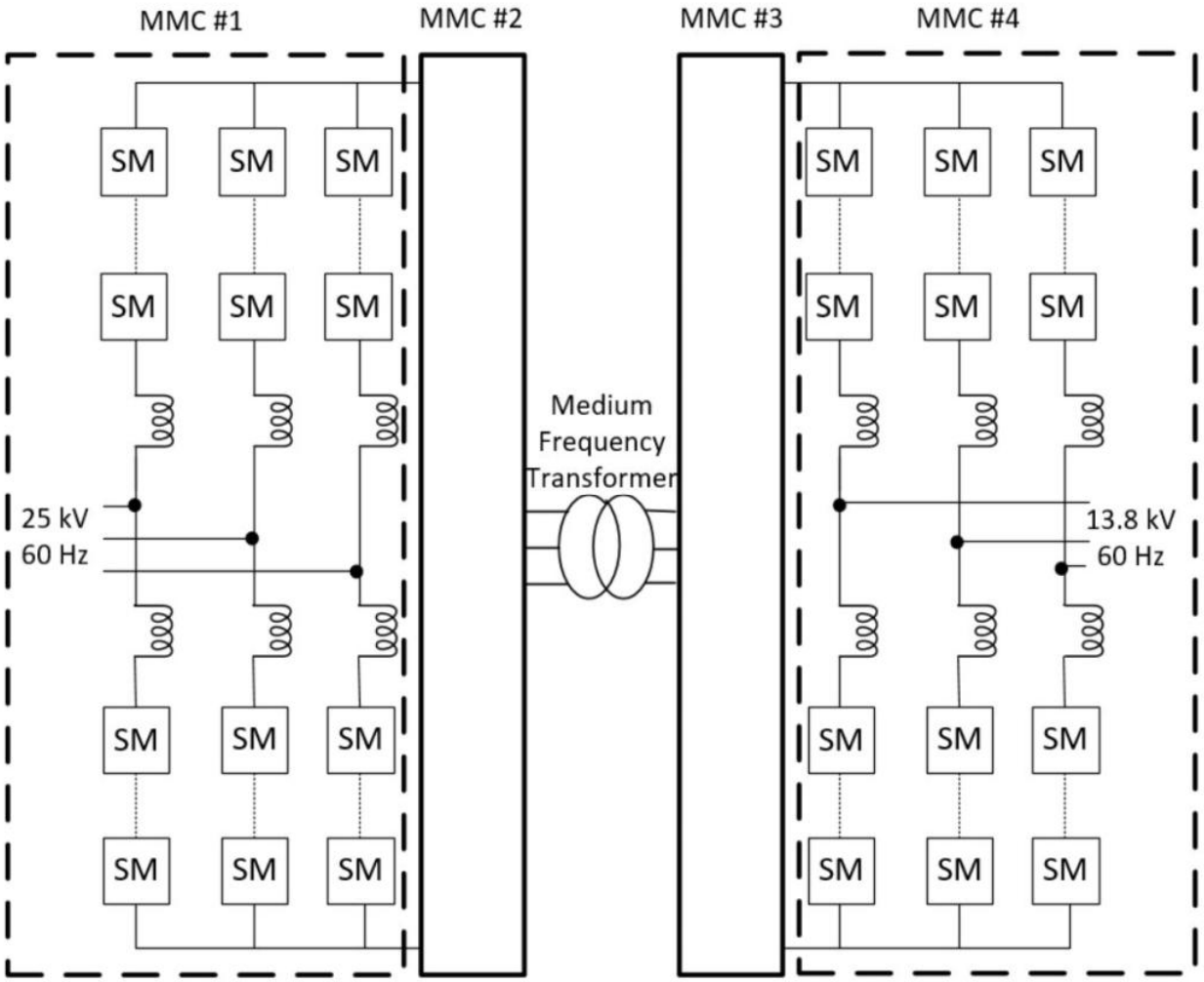

Fig. 3.3: The MPS system under consideration

Table 3.1: System parameters of the MPS system

Properties	**MMC #1**	**MMC #2**	**MMC #3**	**MMC #4**
Rated rms voltage- line-to-line (in kV)	25	25	13.8	13.8
DC link voltage- 25 % over design (in kV)	44	44	24	24
Rated rms current (in A)	139	139	251	251
Peak current (in A)	196	196	355	355
Peak current used- 30% over design (in A)	255	255	462	462

Safety margins are key factors in designing any power system. As indicated in Table 3.1, higher values than the rated current and voltage were considered in the design as safety precautions. The current and voltage ratings of the MMC #1 and MMC #2 are similar, and likewise, the ratings of the MMC #3 and MMC #4 are similar. The sets of MMC #1, MMC #2 and MMC #3, MMC #4 were analyzed separately. Many data sheets available in the market were analyzed to identify a suitable IGBT [11]- [21]. Several assumptions were made [10]:

- Maximum heat sink temperature is 85℃
- Ambient temperature is 40℃
- Thermal resistance of heat pipe is 15℃/kW
- Worst case condition was considered; thus, all the datasheet values were taken for 125℃

Conduction losses of the IGBT and built-in diode were calculated using (3.1) and (3.2), respectively. Switching losses of the IGBT and reverse recovery losses of the built-in diode were calculated using (3.4) and (3.6). Finally, the maximum achievable switching frequency was calculated using (3.11). After the completion of the analysis, four IGBT modules were chosen according to their voltage ratings to design the system [18]- [21]. The properties of these four IGBT modules are listed in Table 3.2. Losses of the IGBT modules for MMC #1 and MMC #2 are listed in Table 3.3 whereas the losses of IGBT modules for MMC #3 and MMC #4 are listed in Table 3.4. Finally, the maximum achievable switching frequencies of MMC #1, MMC #2 and MMC #3, MMC #4 are listed in Table 3.5. Switching losses in Table 3.3 and Table 3.4 are calculated based on a switching frequency of 1 kHz, selected all by taking a reasonable operating frequency for the medium-frequency transformers. The thermal resistance of heat sink to ambient for the corresponding switching frequency is listed in Table 3.6.

Table 3.2: Properties of the selected IGBT modules

Device module	**Collector-emitter voltage, V_{CE} (in kV)**	**DC collector current, I_C (in A)**	**Peak collector current, I_{CM} (in A)**	**DC voltage, V_{CC} (in kV)**
CM750HG-130R	6.5	750	1500	4
5SNA 0800J450300	4.5	800	1600	3
5SNA 0800N330100	3.3	800	1600	2
5SND 0800M170100	1.7	800	1600	1.2

Table 3.3: Losses of the selected IGBT modules in MMC #1 and MMC #2 terminals

Device module	**Conduction loss of IGBT, P_{CT} (in W)**	**Conduction loss of Diode, P_{CD} (in W)**	**Switching loss of IGBT, P_{SWT} (in W)**	**Reverse recovery loss of Diode, P_{RRD} (in W)**
CM750HG-130R	277.5	32.4	1006	216.5
5SNA 0800J450300	197.4	23.3	690.7	203.7
5SNA 0800N330100	220.8	16.7	372.4	229.2
5SND 0800M170100	123.7	11.6	82.8	57.3

Table 3.4: Losses of the selected IGBT modules in MMC #3 and MMC #4 terminals

Device module	**Conduction loss of IGBT, P_{CT} (in W)**	**Conduction loss of Diode, P_{CD} (in W)**	**Switching loss of IGBT, P_{SWT} (in W)**	**Reverse recovery loss of Diode, P_{RRD} (in W)**
CM750HG-130R	579	47.6	1846	391.5
5SNA 0800J450300	481.8	52	1251	372.5
5SNA 0800N330100	499.6	34.6	582.5	334.2
5SND 0800M170100	360.5	26	127.3	79.6

Table 3.5: Maximum achievable switching frequencies

Device module	**MMC #1 (in Hz)**	**MMC #2 (in Hz)**	**MMC #3 (in Hz)**	**MMC #4 (in Hz)**
CM750HG-130R	2200	2200	504	504
5SNA 0800J450300	3107	3107	624	624
5SNA 0800N330100	4592	4592	2537	2537
5SND 0800M170100	20454	20454	12631	12631

Table 3.6: Thermal resistance of the heat sink to ambient

Device module	**MMC #1 (in ℃/kW)**	**MMC #2 (in ℃/kW)**	**MMC #3 (in ℃/kW)**	**MMC #4 (in ℃/kW)**
CM750HG-130R	29.4	29.4	9.2	9.2
5SNA 0800J450300	40.4	40.4	10.8	10.8
5SNA 0800N330100	53.6	53.6	29.5	29.5
5SND 0800M170100	163	163	75.8	75.8

Selection of the IGBT determines the size, weight, cost, and complexity of the overall system. Considering these parameters, IGBT module CM750HG-130R was selected for MMC #1 and MMC #2 and IGBT module 5SNA 0800N330100 was selected for MMC #3 and MMC #4. Considering the safety margin, a switching frequency of 1 kHz was chosen for the system. The peak of the reverse recovery current (I_{RR}) is another important property of IGBT. The device will be damaged if the system reverse recovery current exceeds the limit of the IGBT given by the peak collector current I_{CM}. Limit of the I_{RR} was also considered during the selection process. The required number of component in MMC terminals are listed in Table 3.7.

Table 3.7: Component count for the four MMC terminals

Device	MMC #1	MMC #2	MMC #3	MMC #4
IGBT	132	132	144	144
SM Capacitor	66	66	72	72
Arm Inductor	6	6	6	6

3.5 Conclusions

In this chapter, the power semiconductor devices were selected for the four MMC terminals. Suitable switching algorithms are required to control these switching devices; Chapter 4 will analyze different switching algorithms and the fundamentals of the selected modulation techniques will be presented.

3.6 References

[1] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications, and Design, Third Edition. New York: John Wiley & Sons Inc, 2003.

[2] M. H. Rashid, Power Electronics: Circuits, Devices, and Applications, Fourth Edition. Pearson, 2013.

[3] X. Zhou, Z. Xu, A. Q. Huang, and D. Boroyevich, “Comparison of high power IGBT, IGCT and ETO for pulse applications”, in *Proceeding of Annual Power Electronics Seminar*, vol. 2, pp. 506–510,2002.

[4] J. Millan, "Wide band-gap power semiconductor devices*." in IET Circuits, Devices & Systems 1*, no. 5, pp. 372-379, 2007.

[5] M. Buschendorf, J. Weber, and S. Bernet. "Comparison of IGCT and IGBT for the use in the modular multilevel converter for HVDC applications," in *Systems, Signals and Devices (SSD), 2012 9th International Multi-Conference on*, IEEE, pp. 1-6, 2012.

[6] D. Graovac, M. Purschel. "IGBT power losses calculation using the data-sheet parameters." Infineon Application Note V1.1, 2006.

[7] ABB, “Application Note 5SYA 2053-04.
Available online at:
http://search-ext.abb.com/library/Download.aspx?DocumentID=5SYA2053-04&LanguageCode=en&DocumentPartId=&Action=Launch

[8] Infineon, “Using web based tools for the thermal design of a power converter”. Applied Power Electronics Conference, 2016.
Available online at:
http://www.epapers.org/apec2016-is/ESR/paper_details.php?PHPSESSID=0rnf98o32ph8ck8qqejdrffct1&paper_id=1076

[9] M. Ouchi, Y. Abe, M. Fukagaya, H. Ohta, Y. Shinmoto, M. Sato, and K. Iimura. "Thermal management systems for data centers with liquid cooling technique of CPU," in *13th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, pp. 790-798, 2012.

[10] Mersen, “Thermally Managing High Power Devices Using Heat Pipe Assemblies”. *Applied Power Electronics Conference*, 2016.
Available online at:
http://www.apec-conf.org/Portals/0/Industry%20Session%20Presentations/2016%20Industry%20Sessions.pdf.

[11] ABB, “HiPak IGBT Module 5SNA 1600N170100”. Available online at:
http://search.abb.com/library/Download.aspx?DocumentID=5SYA1564-02&LanguageCode=en&DocumentPartId=&Action=Launch

[12] ABB, “HiPak IGBT Module 5SND 0500N330300”. Available online at:
http://search-ext.abb.com/library/Download.aspx?DocumentID=5SYA%201433-00&LanguageCode=en&DocumentPartId=&Action=Launch

[13] ABB, “HiPak IGBT Module 5SNA 1000N330300”. Available online at:
http://search.abb.com/library/Download.aspx?DocumentID=5SYA%201418-03&LanguageCode=en&DocumentPartId=&Action=Launch

[14] ABB, “HiPak IGBT Module 5SNA 0650J450300”. Available online at:
http://search.abb.com/library/Download.aspx?DocumentID=5SYA%201598-04&LanguageCode=en&DocumentPartId=&Action=Launch

[15] ABB, “HiPak IGBT Module 5SNA 0500J650300”. Available online at:
http://search-ext.abb.com/library/Download.aspx?DocumentID=5SYA%201413-

02&LanguageCode=en&DocumentPartId=&Action=Launch

[16] ABB, “HiPak IGBT Module 5SNA 0750G650300”. Available online at: http://search.abb.com/library/Download.aspx?DocumentID=5SYA%201600-03&LanguageCode=en&DocumentPartId=&Action=Launch

[17] Infineon, “IGBT Module FZ750R65KE3”. Available online at: https://www.infineon.com/dgdl/Infineon-FZ750R65KE3-DS-v03_01-EN.pdf?fileId=db3a304325afd6e00126461fd3936974

[18] ABB, “HiPak IGBT Module 5SND 800M170100”. Available online at: http://search.abb.com/library/Download.aspx?DocumentID=5SYA1589-01&LanguageCode=en&DocumentPartId=&Action=Launch

[19] ABB, “HiPak IGBT Module 5SNA 0800N330100”. Available online at: http://search.abb.com/library/Download.aspx?DocumentID=5SYA%201591-02&LanguageCode=en&DocumentPartId=&Action=Launch

[20] ABB, “HiPak IGBT Module 5SNA 0800J450300”. Available online at: http://search-ext.abb.com/library/Download.aspx?DocumentID=5SYA1402-01&LanguageCode=en&DocumentPartId=&Action=Launch

[21] Mitsubishi, “HV IGBT Modules CM750HG-130R”. Available online at: https://www.mitsubishielectric-mesh.com/products/pdf/CM750HG-130R_n.pdf

CHAPTER 4

SWITCHING ALGORITHMS FOR MMC STAGES

4.1 Introduction

MMC modulation strategies vary mostly with the selection of switching frequency as it does for any multilevel converter [1]. These strategies can be classified as:

- High switching-frequency modulations
- Fundamental switching-frequency modulations

Different types of high switching-frequency modulation are available such as [2]- [3]:

- Carrier-based pulse width modulation (CB-PWM)
- Space-vector modulation (SVM)
- Staircase and nearest level modulation

The SVM uses the redundant states for balancing the capacitor voltage [4]. However, calculations and control of the SVM become very complex with increasing number of levels. Generation of switching signals and implementation are very simple in the staircase modulation [5]- [10]. However, voltage balancing of the SM capacitors are complex and it can be simplified with the use of nearest level modulation such as shown in [8]. An interesting trapezoidal modulation strategy was applied in a MMC for medium and high-voltage dc-dc transformers [11]. The most popular high-frequency modulations are in the CB-PWM group, and can be classified as [12]:

- Level-shifted PWM (LS-PWM)

- Phase shifted PWM (PS-PWM)
- Hybrid PWM

Hybrid PWM is the combination of other types of PWM and used rarely. LS-PWM provides the best harmonic performance among all the PWM techniques. However, the voltage balancing technique is performed by an external method known as “sort and select” [3], [13]. LS-PWM is classified as follows [3], [14]:

- Phase disposition PWM (PD-PWM)
- Phase opposite disposition PWM (POD-PWM)
- Alternative phase opposite disposition PWM (APOD-PWM)
- Variable carrier PWM

Different types of LS-PWM were applied in [15]- [16]. In PD-PWM all the in-phase carriers are spread among different levels between +1 and -1, whereas the POD-PWM the carriers are 180° phase shifted. In APOD-PWM, the carriers above zero are in-phase and carriers below zero are 180° phase shifted. Variable types of carriers spread in different levels in variable carrier PWMs. The most popular CB-PWM is PS-PWM and used in [17]- [18]. The “sort and select” algorithm of LS-PWM is omitted in the PS-PWM and the SM capacitor voltage is balanced with a PI controller [19]- [21]. The implementation of PS-PWM is very simple and performs better than LS-PWM when the number of levels are high which is the case of the MPS [22]. Finally, the fundamental-switching-frequency modulation includes:

- Selective harmonic elimination (SHE)
- Fundamental frequency
- Multiple transitions

SHE is the most popular one among the fundamental-switching-frequency modulations and widely used in [23]- [24] since it allows to eliminate the most important harmonics. In this research, the selected switching frequency is 1 kHz for all four of the MMC terminals as mentioned in Chapter 3. The fundamental frequency of MMC #1 and MMC #4 is 60 Hz; thus, one of the high-frequency modulation strategies need to be selected for these two MMC terminals: PS-PWM is selected due to the advantages mentioned earlier. A detail analysis of the PS-PWM will be presented in section 4.2. The operating frequency of MMC #2, MMC #3 and medium-frequency transformer will decide the size and weight of the MPS system. If selected too large, the switching devices may not be capable of operating at this frequency and if selected too low, the size of the system will not be reduced significantly. Considering all the factors, the operating frequency of these corresponding sections are selected to be 1 kHz. The SHE algorithm is chosen for MMC #2 and MMC #3 to gain the maximum benefits; that is, to eliminate low-order harmonics and minimize MPS size and weight. A complete analysis will be conducted in section 4.3.

4.2 Phase-Shifted Pulse Width Modulation

A multilevel converter using PS-PWM requires multiple carriers to generate the switching signals. These multiple carriers spread throughout a time-period that corresponds to the switching cycle. The number of carriers required for a multilevel converter is equal to the number of levels in the output voltage, so a 10-level converter requires 10 carriers. The phase shift between the carriers can be calculated by [25]:

$$\emptyset = \frac{360}{N_C} \tag{4.1}$$

where N_C is the number of carriers.

Thus, the time interval between the carrier signals is expressed by:

$$T_d = \frac{1}{N_C f_{SW}} \tag{4.2}$$

where f_{SW} is the switching frequency of the carrier signals. A theoretical PS-PWM switching signals of a five levels converter are shown in Fig. 4.1.

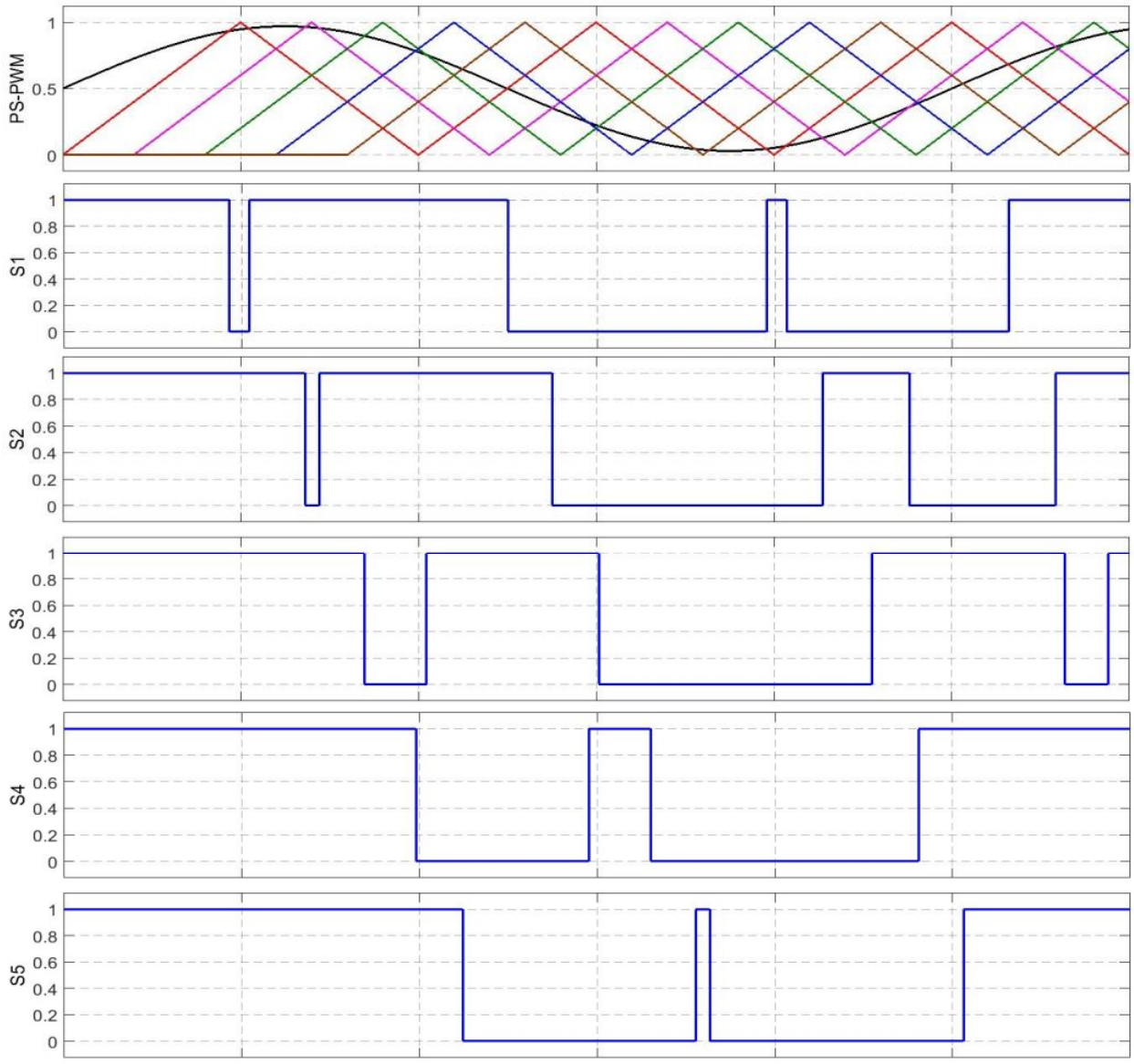

Fig. 4.1: PS-PWM for a five-level converter

4.3 Selective Harmonic Elimination

The concept of SHE emerged in multilevel power converters to reduce the switching losses and increase the overall efficiency of the converter while eliminating low-order harmonics. Different SHE methods were used in the multilevel converters [26]- [33]. A real-time SHE implementation was discussed in [34]. Application of SHE in MMCs is a new trend and applied in [23], [24], and [35]. The SM capacitor voltage balancing is the main challenge in MMC. Predefined repetitive pulse patterns were applied to minimize the capacitor energy deviation in [23]. The complete methodology of this SHE technique will be analyzed here which is applied in this research as well. A three-phase MMC terminal is shown in Fig. 4.2.

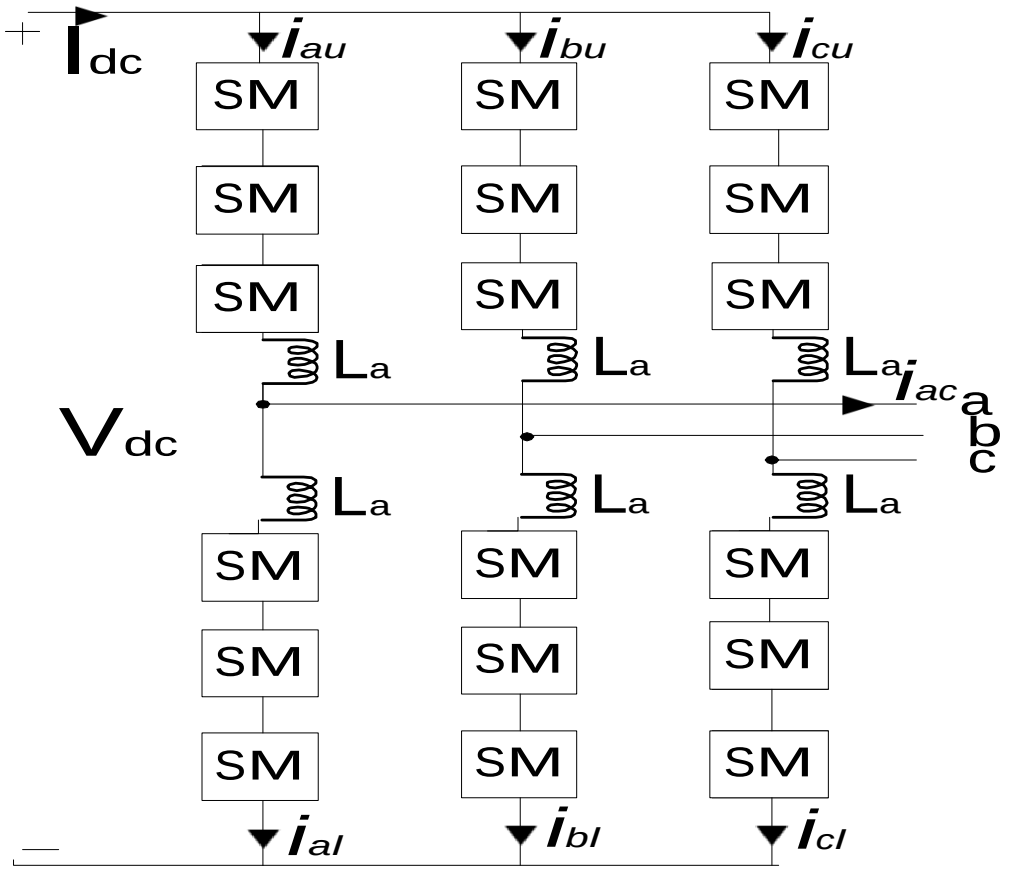

Fig. 4.2: A three-phase MMC terminal

N series-connected SMs are in a single arm and La is denoted as the arm inductance. The MMC terminal is operating as an inverter and the ac-side quantities can be expressed by:

$$i_{ac} = \hat{I}_{ac} \cos(\omega t + \varphi) \tag{4.3}$$

$$v_{ac} = \hat{V}_{ac} \cos(\omega t) \tag{4.4}$$

where ω and φ are the angular frequency and the phase displacement between the voltage and current, respectively. The ac-side and circulating currents can be expressed using the arms current as:

$$i_{ac} = i_{au} - i_{al} \tag{4.5}$$

$$i_{zu} = \frac{i_{au}+i_{al}}{2} \tag{4.6}$$

The steady-state circulating current can be expressed by the dc-side current as:

$$i_{zu} = I_{dc} + \sum_{n=1}^{\infty} \hat{\imath}_{zu,n} \cos(n\omega t + \alpha_n) \tag{4.7}$$

The state of the SM is defined by s_k, which is equal to one and zero when the SM *k* is inserted and bypassed, respectively. Thus, this signal can be expressed as a square pulse by:

$$s_k = \frac{\alpha_k}{\pi} + \sum_{n=1}^{\infty} \frac{2\sin(n\alpha_k)}{n\pi} \cos(n\omega t - n\gamma_k) \tag{4.8}$$

where $2\alpha_k$ is the width of the signal, and γ_k is the center of the square pulse. The nominal value of α_k is $\frac{\pi}{2}$. The graphical representation of the state signal is shown in Fig. 4.3.

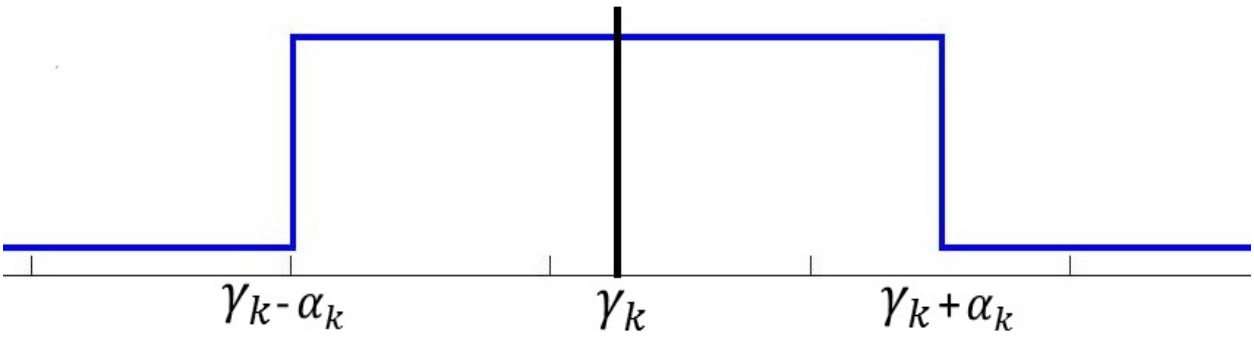

Fig. 4.3: Graphical representation of the state signal of SM

The upper and the lower arm voltages can be represented in term of the state signal as [36]:

$$v_{al} = \sum_{k=1}^{N} v_{SM,l} s_k \tag{4.9}$$

$$v_{au} = \sum_{k=N+1}^{2N} v_{SM,u} s_k \tag{4.10}$$

where $v_{SM,l}$, and $v_{SM,u}$ are voltages across the arm SM capacitors.

Equation (4.9) can be rewritten using (4.8) as:

$$v_{al} = \boldsymbol{\vartheta}_0 \sum_{n=1}^{N} [\, \frac{\alpha_k}{\pi} + \sum_{n=1}^{\infty} \frac{2\sin(n\alpha_k)}{n\pi} \cos(n\omega t - n\boldsymbol{\gamma}_k)] \tag{4.11}$$

$$v_{al} = \boldsymbol{\vartheta}_0 \sum_{n=1}^{N} [\, \frac{\alpha_k}{\pi} + \hat{\boldsymbol{\vartheta}}_{d,n} \cos(n\omega t) + \hat{\boldsymbol{\vartheta}}_{q,n} \sin(n\omega t)] \tag{4.12}$$

where $\boldsymbol{\vartheta}_0$ is the nominal SM capacitor voltages. $\hat{\boldsymbol{\vartheta}}_{d,n}$, and $\hat{\boldsymbol{\vartheta}}_{q,n}$ can be expressed as:

$$\hat{\boldsymbol{\vartheta}}_{d,n} = \boldsymbol{\vartheta}_0 \sum_{k=1}^{N} \frac{2\sin(n\alpha_k)}{n\pi} \cos(n\boldsymbol{\gamma}_k) \tag{4.13}$$

$$\hat{\boldsymbol{\vartheta}}_{q,n} = \boldsymbol{\vartheta}_0 \sum_{k=1}^{N} \frac{2\sin(n\alpha_k)}{n\pi} \sin(n\boldsymbol{\gamma}_k) \tag{4.14}$$

The *N* variables, $\boldsymbol{\gamma}_1$ through $\boldsymbol{\gamma}_N$ can be used to control both the magnitude and phase of the output voltage, and to eliminate selected harmonics. Equations (4.13) and (4.14) can be used for that purpose.

The fundamental-frequency components can be obtained by equating the first two equations to the reference values such as:

$$\widehat{\boldsymbol{\vartheta}}_{d,1} = \widehat{\boldsymbol{\vartheta}}_{\boldsymbol{d},\mathbf{1},ref} \tag{4.15}$$

$$\widehat{\boldsymbol{\vartheta}}_{q,1} = \widehat{\boldsymbol{\vartheta}}_{\boldsymbol{q},\mathbf{1},ref} \tag{4.16}$$

where $\widehat{\boldsymbol{\vartheta}}_{\boldsymbol{d},\mathbf{1},ref}$ and $\widehat{\boldsymbol{\vartheta}}_{\boldsymbol{q},\mathbf{1},ref}$ are the reference values of the output signal. Remaining equations are then set to zero to eliminate the selected harmonic.

$$\widehat{\boldsymbol{\vartheta}}_{d,n} = 0 \tag{4.17}$$

$$\widehat{\boldsymbol{\vartheta}}_{q,n} = 0 \tag{4.18}$$

where n is the selected harmonic that is to be eliminated. By solving these N equations, the value of the angles γ_k can be calculated. Balancing the SM capacitor voltage is the main task of MMC design. When a SM is inserted, a certain amount of energy transfer takes place which can be either positive or negative. However, average energy transfer in a SM must be zero. Net charge transfer in a SM can be calculated using the state signal s_k and the corresponding arm current. The net charge transfer in an upper and lower arms SM can then be expressed as:

$$q_{l,net,k} = \int_0^T s_k i_{al}\, dt,\ \ k \leq N \tag{4.19}$$

$$q_{u,net,k} = \int_0^T s_k i_{au}\, dt,\ \ k > N \tag{4.20}$$

where T is the time-period. The state signal is defined in such a way that it only contains odd-order harmonics whereas the arm current has the even order harmonics. Therefore, the harmonic components will not contribute to the charge transfer. Equation (4.19) reduces to:

$$q_{l,net,k} = \left[\frac{I_{dc}}{2} - \frac{\hat{\imath}_{ac}}{2\pi}\cos(\gamma_k + \varphi)\right]\mathrm{T} \tag{4.21}$$

$$q_{l,net,k} = \left[\frac{I_{dc}}{2} - \frac{\hat{\imath}_{ac}}{2\pi}\cos(\gamma_k)\cos(\varphi) + \frac{\hat{\imath}_{ac}}{2\pi}\sin(\gamma_k)\sin(\varphi)\right]\mathrm{T} \tag{4.22}$$

Equation (4.22) can be split into two parts such as:

$$q_{A,k} = [\frac{I_{dc}}{2} - \frac{\hat{\imath}_{ac}}{2\pi}\cos(\gamma_k)\cos(\varphi)]T \quad (4.23)$$

$$q_{R,k} = [\frac{\hat{\imath}_{ac}}{2\pi}\sin(\gamma_k)\sin(\varphi)]T \quad (4.24)$$

Considering a lossless system, the dc-side power should be equal to the ac-side power.

Therefore, dc-side power can be expressed as:

$$V_{dc}I_{dc} = \frac{\hat{v}_{ac}\hat{\imath}_{ac}}{2}\cos\varphi \quad (4.25)$$

The modulation index M is defined as [36]:

$$M = \frac{\hat{v}_{ac}}{\frac{V_{dc}}{2}} \quad (4.26)$$

Equation (4.25) is then simplified as:

$$I_{dc} = \frac{M}{4}\hat{\imath}_{ac}\cos\varphi \quad (4.27)$$

and (4.23) can be rewritten as:

$$q_{A,k} = [\frac{M}{8} - \frac{1}{2\pi}\cos(\gamma_k)]\, T\,\hat{\imath}_{ac}\cos\varphi \quad (4.28)$$

The angles γ_k should be selected in such a way that the net charge in (4.22) becomes zero. To maintain the fundamental-frequency switching, each SM will get one pulse per fundamental frequency period. However, pulses will be centered at different angles in the subsequent periods as shown in Fig. 4.4.

Fig. 4.4: Pulse pattern for a SM

Therefore, the pulse pattern for a SM can be expressed by a vector as:

$$\beta_k = [\gamma_1 \quad \gamma_2 \quad \gamma_3 \quad \ldots \quad \gamma_N] \tag{4.29}$$

The pulse pattern can be used for the next SM of the same arm shifted it by one fundamental frequency period. Thus, the pulse pattern for the next SM is expressed by:

$$\beta_{k+1} = [\gamma_N \quad \gamma_1 \quad \gamma_2 \quad \ldots \quad \gamma_{N-1}] \tag{4.30}$$

Same pulse pattern is used to control all the SM; thus, the sum of the inserted voltages will be periodic with the fundamental-frequency period. The fundamental-frequency component will produce the output voltage of (4.4) only if (4.12) is expressed by a cosine function. Thus, the sum of all sine components should be zero. This condition provides two constraints for the angles γ_k:

$$\sum_{k=1}^{N} sin\ (\gamma_k) = 0 \tag{4.31}$$

$$\sum_{k=1}^{N} cos\ (\gamma_k) = M\ N\frac{\pi}{4} \tag{4.32}$$

Appling (4.31) and (4.32) in (4.22) will make sure that the sum of net transfer of charge in all the SMs is zero. The angles γ_k should be selected as pairs that are symmetrically distributed around zero with an opposite sign. However, the center angle for an odd number of SMs should be placed at zero and the rest of the angles should be selected as pairs that are symmetrically distributed around zero with an opposite sign. The selection of pulse patterns also ensures the minimal distortion for the imposed voltage. This can be achieved by comparing the voltage levels with a sinusoidal reference such that:

$$\text{m} = N\frac{1+M_{ref}\cos(\omega t)}{2} \tag{4.33}$$

where M_{ref} is the desired modulation index. Nearest integer towards m will decide the number of SMs that should be inserted. Thus, a SM should be inserted or bypassed when the fractional part of m is equal to 0.5 which can be represented by:

$$\mathrm{m}\,(t_k) = \mathrm{k} - \frac{1}{2} \tag{4.34}$$

where k is an integer from one to N. This condition on the imposed voltage will make sure that a staircase shape is obtained in the output voltage. The time when a SM is turned-off is defined by:

$$t_k = \frac{1}{\omega}\left(\gamma_k + \frac{\pi}{2}\right) \tag{4.35}$$

Combining (4.33) to (4.35) yields

$$\gamma_k = \arccos\left[\frac{1}{M_{ref}}\left(\frac{2k-1-N}{N}\right)\right] - \frac{\pi}{2} \tag{4.36}$$

Different values of M_{ref} will provide different angles γ_k, some of them can be complex valued. This happens when the quantized step reference does not correspond to the actual number of levels. This occurs for a lower value of M_{ref} where all the available *N* SMs are not required to produce the output voltage. The problem can be solved by taking the real-valued angles using (4.36) and replacing the complex valued angles by $\pm\ \frac{\pi}{2}$. The complex-valued angles always occurred in a pair, the positive imaginary part can be replaced by $+\frac{\pi}{2}$ and the negative by $-\frac{\pi}{2}$. The net charge transfer due to the active and reactive power flows in each fundamental-frequency period can be calculated by (4.23) and (4.24). These net charge transfer can create a large ripple in the SM capacitor. A specific selection procedure of the pulse pattern can solve this problem, in particular, every pulse that results in a positive net transfer of charge is followed by one or more pulses that result negative net transfer of charge.

The initial pulse can be selected as the pulse responsible for the largest positive $q_{A,k}$ and a positive $q_{R,k}$. The next pulse should be the pulse responsible for the lowest negative value of $q_{A,k}$ and a negative $q_{R,k}$. The procedure should continue for the complete sets of angles. A five-level simulation was conducted in this research. The angles γ_k calculated for different values of *M* to eliminate the 5th harmonic, are listed in Table 4.1.

4.4 Conclusions

This chapter analyzed different switching algorithms that can be implemented in MMC terminals. From this analysis, the PS-PWM and SHE algorithms were selected as the switching algorithms to run the simulations in Matlab/Simulink™. Different sets of controllers are required for different switching techniques. The controller designs for the PS-PWM and SHE will be presented in Chapter 5.

Table 4.1: Calculated angles to eliminate the 5th harmonic for different modulation indexes

M	**0.85**	**0.90**	**0.95**	**1**
$\boldsymbol{\gamma_1}$	59.17	58.05	57.36	53.13
$\boldsymbol{\gamma_2}$	31.88	29.56	28.42	23.02
$\boldsymbol{\gamma_3}$	0	0	0	0
$\boldsymbol{\gamma_4}$	-31.88	-29.56	-28.42	-23.02
$\boldsymbol{\gamma_5}$	-59.17	-58.05	-57.36	-53.13

4.5 References

[1] J. Rodriguez, J. S. Lai, and F. Z. Peng. "Multilevel inverters: a survey of topologies, controls, and applications." *IEEE Transactions on Industrial Electronics* vol. 49, no. 4, pp: 724-738, 2002.

[2] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. De Novaes. "A versatile DC/DC converter based on modular multilevel converter for energy collection and distribution." *In Renewable Power Generation, IET Conference on*, IET, pp. 1-6, 2011.

[3] G. Konstantinou, J. Pou, S. Ceballos, R. Darus, and V. G. Agelidis. "Switching frequency analysis of staircase-modulated modular multilevel converters and equivalent PWM techniques." In *IEEE Transactions on Power Delivery*, vol. 31, no. 1 pp: 28-36, 2016.

[4] A. Lesnicar, R. Marquardt, "A new modular voltage source inverter topology". In *EPE Conference*, 2003.

[5] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for Modular multilevel converter." In *IEEE Transactions on Power Delivery*, vol. 26, no. 1, pp. 298–306, 2011.

[6] Q. Jiangchao and M. Saeedifard, "Reduced switching-frequency voltage-balancing strategies for modular multilevel HVDC converters." In *IEEE Transactions on Power Delivery*, vol. 28, no. 4, pp. 2403–2410, 2013.

[7] P. Hu and D. Jiang, "A level-increased nearest level modulation method for modular multilevel converters." In *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1836–1842, 2015.

[8] H. Pengfei, J. Daozhuo, L. Yiqiao, Z. Yuebin, L. Zhiyong, and G. Jie, "Zero tracking error nearest level modulation for modular multilevel converters," In *Industrial Electronics Society, 39th Annual Conference of the IEEE*, pp. 1422–1426, 2013.

[9] P. Meshram and V. Borghate, "A Simplified nearest level control (NLC) voltage balancing method for modular multilevel converter (MMC)." *In IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 450–462, 2015.

[10] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, V. G. Agelidis, and R. Picas, "A modified voltage balancing algorithm for the modular multi-level converter: Evaluation for staircase and phase-disposition PWM." In *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4119–4127, 2015.

[11] I. A. Gowaid, G. P. Adam, S. Ahmed, D. Holliday, and B. W. Williams, "Analysis and design of a modular multilevel converter with trapezoidal modulation for medium and high voltage DC-DC transformers." In *IEEE Transactions on Power Electronics*, vol. 30, no. 10 pp: 5439-5457, 2015.

[12] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modelling, control schemes and applications of modular multilevel converters." In *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4–17, 2015.

[13] M. Saeedifard and R. Iravani, "Dynamic performance of a modular multilevel back-to-back HVDC system." In *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2903–2912, 2010.

[14] C. Sandu, N. Carnu, and V. C. Costea, "Medium Voltage Modular Multi-Level Inverter," M.S. Thesis, Department of Energy Technology., Aalborg Univ., Aalborg, Denmark, 2008.

[15] D. Siemaszko, A. Antonopoulos, K. Ilves, M. Vasiladiotis, L. Angquist, and H. P. Nee, "Evaluation of control and modulation methods for modular multilevel converters." In *Power Electronics Conference (IPEC)*, pp. 746-753, 2010.

[16] G. Konstantinou, M. Ciobotaru, and V. G. Agelidis, "Analysis of multi-carrier PWM methods for back-to-back HVDC systems based on modular multilevel converters." In *IECON 37th Annual Conference on IEEE Industrial Electronics*, pp. 4238–4243, 2011.

[17] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, losses and semiconductor requirements of modular multilevel converters." In *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2633–2642, 2010.

[18] M. Zhang, L. Huang, W. Yao, and Z. Lu, "Circulating harmonic current elimination of a CPS-PWM based modular multilevel converter with plug-in repetitive controller." In *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 2083–2097, 2014.

[19] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D.Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters." *In IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 297–310, 2015.

[20] K. Ilves, L. Harnefors, S. Norrga, and H. P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier PWM." In *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp.: 268-283, 2015.

[21] M. Hagiwara and H. Akagi, "Control and experiment of pulse width modulated modular multilevel converters." In *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737–1746, 2009.

[22] M. Vasiladiotis, “Analysis, Implementation and Experimental Evaluation of Control Systems for a Modular Multilevel Converter,” M.S. Thesis, Department of Electrical Engineering, Royal Institute of Technology, Stockholm, Sweden 2009.

[23] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, “A new modulation method for the modular multilevel converter allowing fundamental switching frequency.” *In IEEE Transactions on Power Electronics,* vol. 27, no. 8, pp. 3482–3494, 2012.

[24] G. Konstantinou, M. Ciobotaru, and V. G. Agelidis, “Selective harmonic elimination pulse width modulation of the modular multilevel converter.” In *IET on Power Electronics*, vol. 6 no. 1, pp. 96–107, 2013.

[25] D. A. Guzman, “High voltage direct current energy transmission using modular multilevel converters,” M.S. Thesis, Department Electrical Engineering, University of Arkansas, Fayetteville, USA, 2013.

[26] R. P. Aguilera, P. Acuña, P. Lezana, G. Konstantinou, B. Wu, S. Bernet, and V. G. Agelidis. "Selective harmonic elimination model predictive control for multilevel power converters." In *IEEE Transactions on Power Electronics* vol. 32, no. 3, pp.: 2416-2426, 2017.

[27] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, “A review of multilevel selective harmonic elimination PWM: Formulations, solving algorithms, implementation and applications.” In *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4091–4106, 2015.

[28] S. Kouro, B. La Rocca, P. Cortes, S. Alepuz, B. Wu, and J. Rodrıguez, “Predictive control based selective harmonic elimination with low switching frequency for multilevel converters.” In *IEEE Energy Conversion Congress and Exposition*, pp. 3130–3136, 2009.

[29] V. G. Agelidis, A. I. Balouktsis, and C. Cossar, “On attaining the multiple solutions of selective harmonic elimination PWM three-level waveforms through function minimization.” In *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 996–1004, 2008.

[30] J. Napoles, J. Leon, R. Portillo, L. Franquelo, and M. A. Aguirre, “Selective harmonic mitigation technique for high-power converters.” In *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2315–2323, 2010.

[31] A. Marzoughi, and H. Iman-Eini. "Selective harmonic elimination for cascaded H-bridge rectifiers based on indirect control." *In Power Electronics and Drive Systems Technology (PEDSTC)*, 3rd, pp. 79-85, 2012.

[32] A. J. Watson, P. W. Wheeler, and J. C. Clare, "A Complete Harmonic Elimination Approach to DC Link Voltage Balancing for a Cascaded Multilevel Rectifier." In *IEEE Transactions on Industrial Electronics,* vol. 54, no.6, pp.2946-2953, 2007.

[33] J. Vassallo, J. C. Clare, and P. W. Wheeler. "A power-equalized harmonic-elimination scheme for utility-connected cascaded H-bridge multilevel converters." *In Industrial Electronics Society, The 29th Annual Conference of the IEEE*, vol. 2, pp. 1185-1190, 2003.

[34] S. Bhadra, and H. Patangia. "Implementation of real-time selective harmonic elimination using microcontrollers." In *Power Electronics for Distributed Generation Systems (PEDG), IEEE 5th International Symposium*, pp. 1-5, 2014.

[35] M. Moranchel, E. J. Bueno, F. J. Rodriguez, and I. Sanz. "Selective Harmonic Elimination modulation for Medium Voltage Modular Multilevel Converter." In *Power Electronics for Distributed Generation Systems (PEDG), IEEE 7th International Symposium* on, pp. 1-6, 2016.

[36] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, and H. P. Nee. "Circulating current control in modular multilevel converters with fundamental switching frequency." *In Power Electronics and Motion Control Conference (IPEMC), IEEE 7th International*, vol. 1, pp. 249-256, 2012.

CHAPTER 5

CONTROLLER DESIGN FOR MMC STAGES

5.1 Introduction

Controller design for an MMC terminal is very complicated because several controllers are required in a coordinated manner to achieve a stable operation of a MMC system; in particular:

- SM capacitor voltage controller
- Circulating current controller
- Arm voltage balancing controller

The PS-PWM switching strategy uses all these controllers simultaneously [1]. A new technique will be used for the SHE as mentioned in Chapter 3 where a predefined pulse pattern will be used to switch the devices [2]. This technique takes care of controlling the SM capacitor voltage without any supplementary controllers. However, an additional controller is required to eliminate the harmonics from the circulating current. Additionally, several controllers are required for rectification and inversion operations. Traditionally, a sending-end MMC terminal controls the dc-link voltage and reactive power for rectification operation and a receiving-end terminal controls the active and reactive powers for inversion operation. In the MPS system, there are two sets of rectifiers and inverters, one operating at 60 Hz, and another operating at 1 kHz. Thus, a different set of controllers will have different control set points. These controllers will be analyzed in the sections 5.2, 5.3, and 5.4. The design of three controllers mentioned in the top of this page will be discussed in section 5.5. Finally, the simulation models and Matlab^{TM} coded files will be presented in the appendices.

5.2 Active and Reactive Power Controllers

The Park transformation is used to analyze the power controllers. A stationary 'abc' frame is transformed into the rotating 'dq' frame [3]. Finally, the inverse Park transformation is used to convert from the 'dq' frame into the 'abc' frame. The description and Matlab/Simulink^{TM} model of the Park and inverse Park transformations are provided in Appendix A.1. Active and reactive powers of a three-phase balanced system can be represented by [4]- [5]:

$$P(t) = Re\,[\frac{3}{2}\, v_a(t) i_a^*(t)] \tag{5.1}$$

$$Q(t) = Im\,[\frac{3}{2}\, v_a(t) i_a^*(t)] \tag{5.2}$$

where v_a, i_a, and i_a^* are the phase voltage, line current, and complex conjugate of the line current, respectively. Replacing these in (5.1) and (5.2) by transforming them into the 'dq' frame yields:

$$P(t) = \frac{3}{2}[v_{d\_grid}(t) i_{d\_grid}(t) + v_{q\_grid}(t) i_{q\_grid}(t)] \tag{5.3}$$

$$Q(t) = \frac{3}{2}[-v_{d\_grid}(t) i_{q\_grid}(t) + v_{q\_grid}(t) i_{d\_grid}(t)] \tag{5.4}$$

where $v_{d\_grid}(t)$, $v_{q\_grid}(t)$, $i_{d\_grid}(t)$, and $i_{q\_grid}(t)$ are the grid voltages and currents in the dq axes, respectively. In steady-state conditions and considering, $v_{q\_grid}(t) = 0$, (5.3) and (5.4) reduced to:

$$P(t) = \frac{3}{2}[v_{d\_grid}(t) i_{d\_grid}(t)] \tag{5.5}$$

$$Q(t) = \frac{3}{2}[-v_{d\_grid}(t) i_{q\_grid}(t)] \tag{5.6}$$

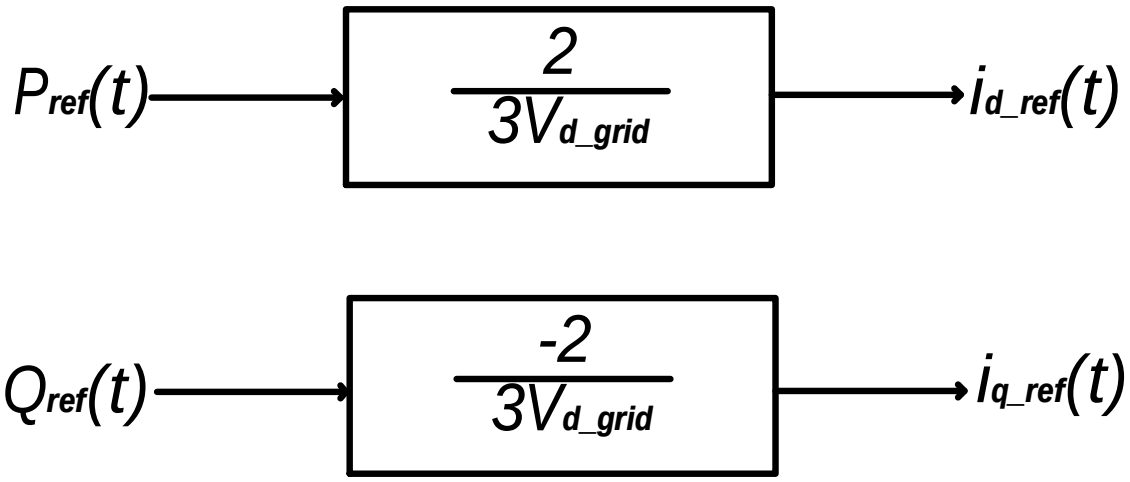

Fig. 5.1: Block diagram for the active and reactive power controllers

The grid voltage of the system is assumed constant; thus, both the active and the reactive powers can be controlled by the grid currents $i_{d\_grid}(t)$ and $i_{q\_grid}(t)$. The currents of the dq axes can be obtained from the reference commands for the active and the reactive power controllers as:

$$i_{d\_grid}(t) = \frac{2}{3V_{d\_grid}} P_{ref}(t) \tag{5.7}$$

$$i_{d\_grid}(t) = \frac{2}{3V_{d\_grid}} Q_{ref}(t) \tag{5.8}$$

The block diagram generating the current reference commands is illustrated in Fig. 5.1.

5.3 Rectifier DC Voltage Controllers

The concept of the dc-link voltage controller was developed as in [6] and provides the reference for the current controller to keep the dc-link voltage constant. To design this dc-link voltage controller, a simplified two-level rectifier was built in Matlab/Simulink™ which is shown in

Appendix A.2. The transfer function of this simplified model can be compared with an MMC-based rectifier. The transfer function in the s-domain is represented by [7]:

$$G_{DC}(s) = \frac{1}{sC_{DC}} \tag{5.9}$$

where C_{DC} is the dc-link capacitance formed by the cumulative contribution of the SM capacitances. The simulation file used to check the stability of the designed PI controller is shown in Fig. 5.2. The initial value of the dc-link was selected as 30 mF using [7], then tuned into the desired value of 35 mF. This dc-link voltage controller works as an outer loop controller which provides the reference for the current controller that needs to be faster than the voltage controller. The bandwidth of the controllers determines the system response speed. Thus, selection of the bandwidth is inter-related. Traditionally, the inner loop response is selected ten times faster than the outer loop and it is customary to have the bandwidth for the inner loop to be smaller than the one-fifth of the switching frequency [6]. Therefore, the bandwidth of the voltage and current controllers are set at 125 rad/s (20 Hz) and 1256 rad/s (200 Hz), respectively. The damping factor of the controllers is set to 0.707. Matlab™ code is used to calculate the proportional and integral gains of the controllers which are provided in Appendix A.3. The step response and the Bode plot of the dc voltage controller are shown in Fig. 5.3 and Fig. 5.4, respectively.

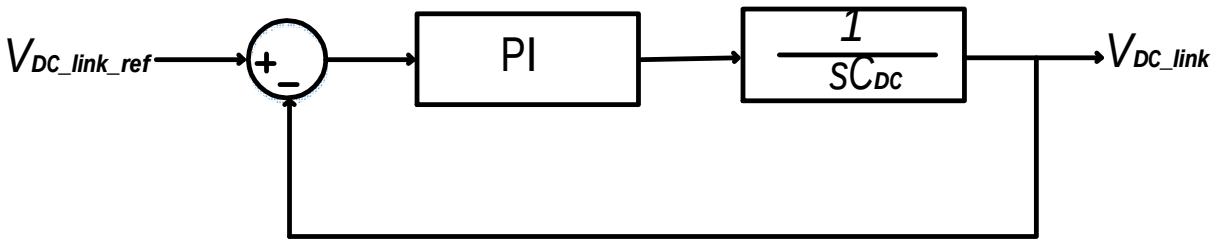

Fig. 5.2: Block diagram of the rectifier dc voltage controller

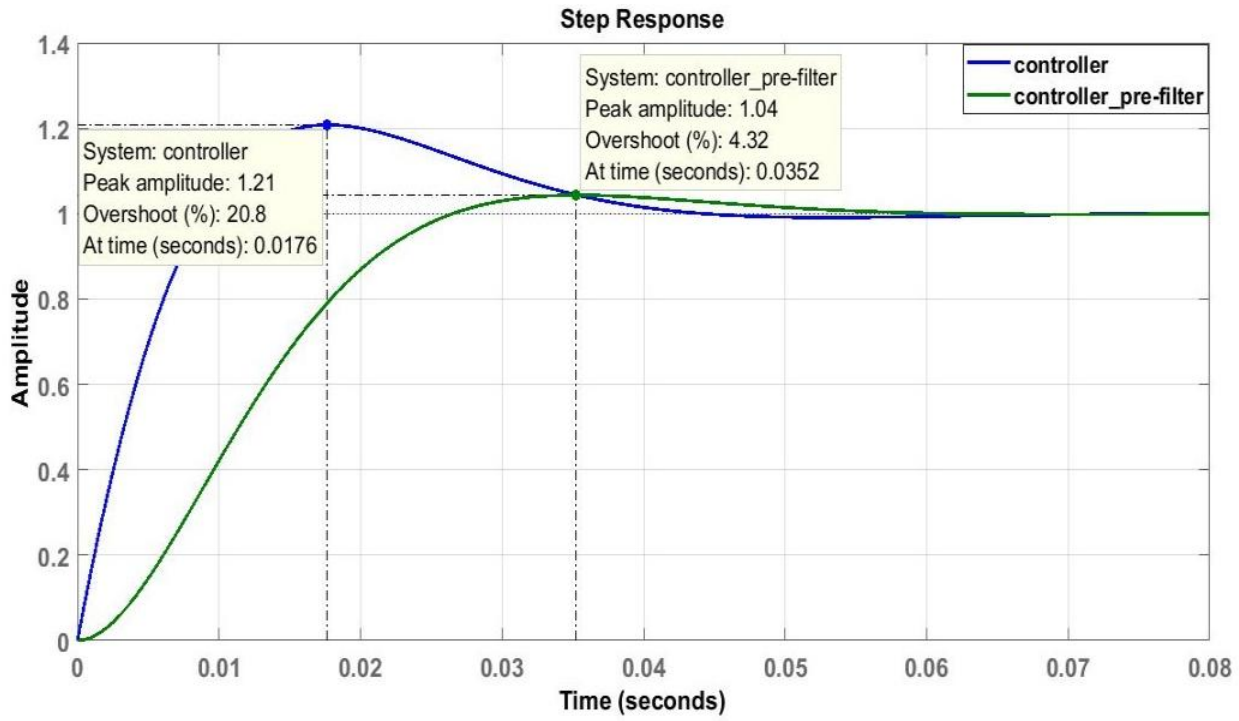

Fig. 5.3: Step response of the rectifier dc voltage controller

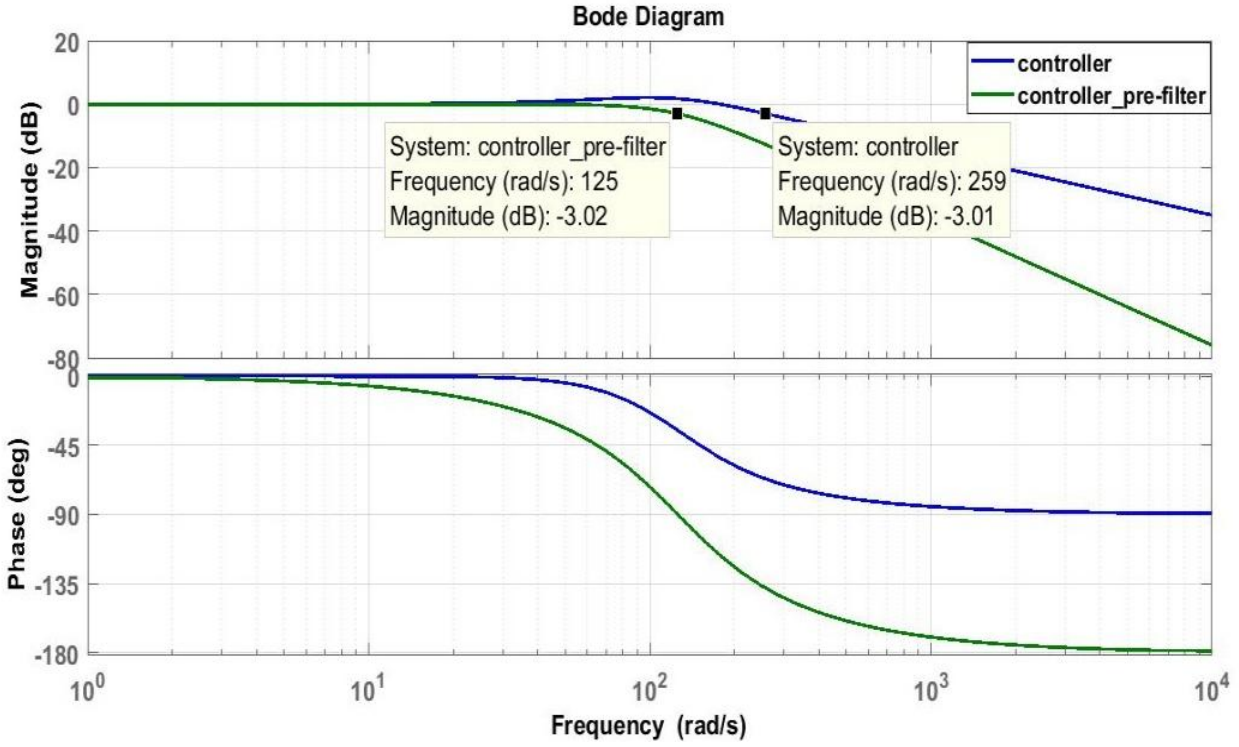

Fig. 5.4: Bode diagram of the rectifier dc voltage controller

The proportional and the integral gains are:

$$k_{p\_v} = 6.22\ \Omega^{-1} \tag{5.10}$$

$$k_{i\_v} = 552.7\ \Omega s^{-1} \tag{5.11}$$

The blue lines in Fig. 5.3 and Fig. 5.4 represent the performance of the voltage controller. A 20.8% overshoot is observed which can damage the switching devices. Moreover, the crossover frequency is twice than the desired value and this fast response can create instability between the voltage and current controllers. To cope with this problem, a pre-filter is designed to compensate for the dynamic response and shown in Fig. 5.5 [4]. The transfer function of this pre-filter is given by:

$$T_{pre-filter} = \frac{1}{1+s\frac{k_{p\_v}}{k_{i\_v}}} \tag{5.12}$$

The green lines in Fig. 5.3 and Fig.5.4 represent the step response and the Bode diagram of the dc voltage controller with the pre-filter. The overshoot of the system is reduced to 4.32% at 0.0352 seconds, a time slightly more than that without the pre-filter. The contribution of this small change in time is insignificant. The introduction of this pre-filter also reduced the crossover frequency to 125 rad/s which was the initial design objective of the voltage controller.

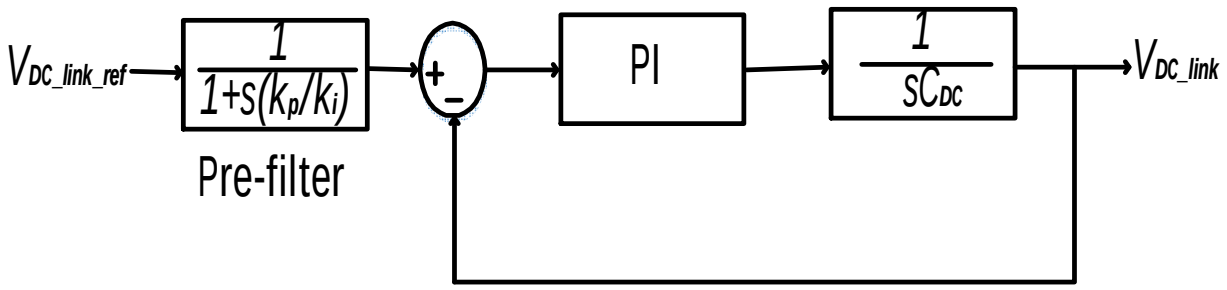

Fig. 5.5: Block diagram of the rectifier dc voltage controller with a pre-filter

5.4 Inverter Current Controllers

A MMC based inverter terminal can produce near sinusoidal voltages and currents when the number of levels is very high [7]- [9]. Therefore, a simplified equivalent circuit is displayed in Fig. 5.6. Applying Kirchhoff's voltage law yields:

$$\vartheta_{inv} = L_{grid} \frac{di_{grid}}{dt} + i_{grid} R_{grid} + \vartheta_{grid} \tag{5.13}$$

Transforming (5.13) into the 'dq' frame yields:

$$L_{grid} \frac{di_{d\_grid}}{dt} = \vartheta_{d\_inv} - \vartheta_{d\_grid} - i_{d\_grid} R_{grid} + \omega_0 L_{grid} i_{q\_grid} \tag{5.14}$$

$$L_{grid} \frac{di_{q\_grid}}{dt} = \vartheta_{q\_inv} - \vartheta_{q\_grid} - i_{q\_grid} R_{grid} - \omega_0 L_{grid} i_{d\_grid} \tag{5.15}$$

where L_{grid} represents the grid inductance, R_{grid} represents the grid resistance, ϑ_{d_inv} and ϑ_{q_inv} represents the inverter voltages in the dq axes, ϑ_{d_grid} and ϑ_{q_grid} represents the grid voltages in the dq axes and ω_0 represents the angular frequency.

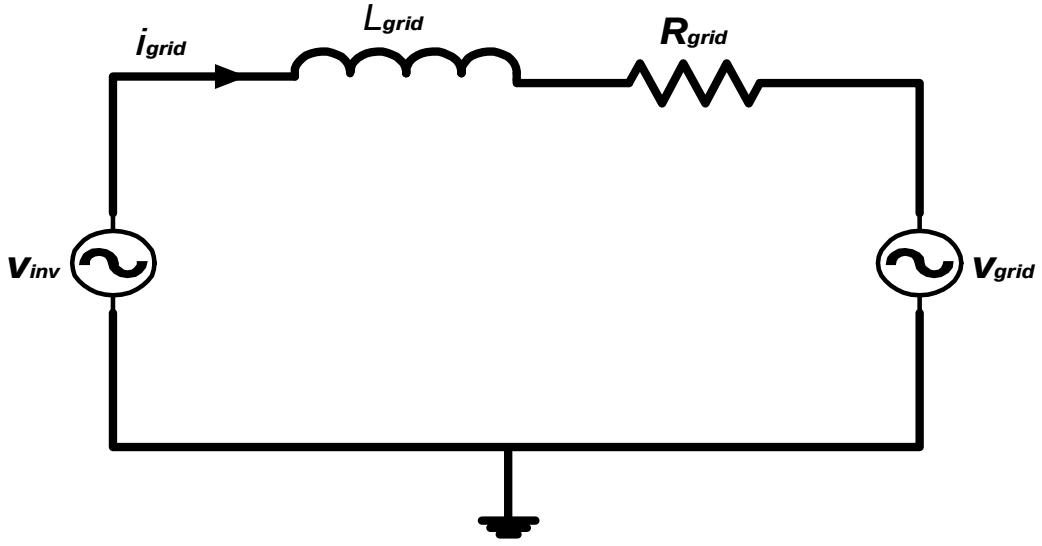

Fig. 5.6: An inverter terminal injecting power to the grid

The system stability can only improve if the cross-coupling terms in (5.14) and (5.15) are eliminated. This is achieved by selecting the voltages as [6]:

$$\acute{v}_d = \vartheta_{d\_inv} - \vartheta_{d\_grid} + \omega_0 \, L_{grid} \, i_{q\_grid} \tag{5.16}$$

$$\acute{v}_q = \vartheta_{q\_inv} - \vartheta_{q\_grid} - \omega_0 \, L_{grid} \, i_{d\_grid} \tag{5.17}$$

where $\acute{v}_d$, $\acute{v}_q$ are the outputs of the PI controllers.

By replacing (5.16) and (5.17) into (5.14) and (5.15) and solving them in the Laplace domain yields:

$$\frac{i_{d\_grid}}{\acute{v}_d} = \frac{1}{s \, L_{grid} + R_{grid}} \tag{5.18}$$

$$\frac{i_{q\_grid}}{\acute{v}_q} = \frac{1}{s \, L_{grid} + R_{grid}} \tag{5.19}$$

The block diagrams of the current controllers are shown in Fig. 5.7.

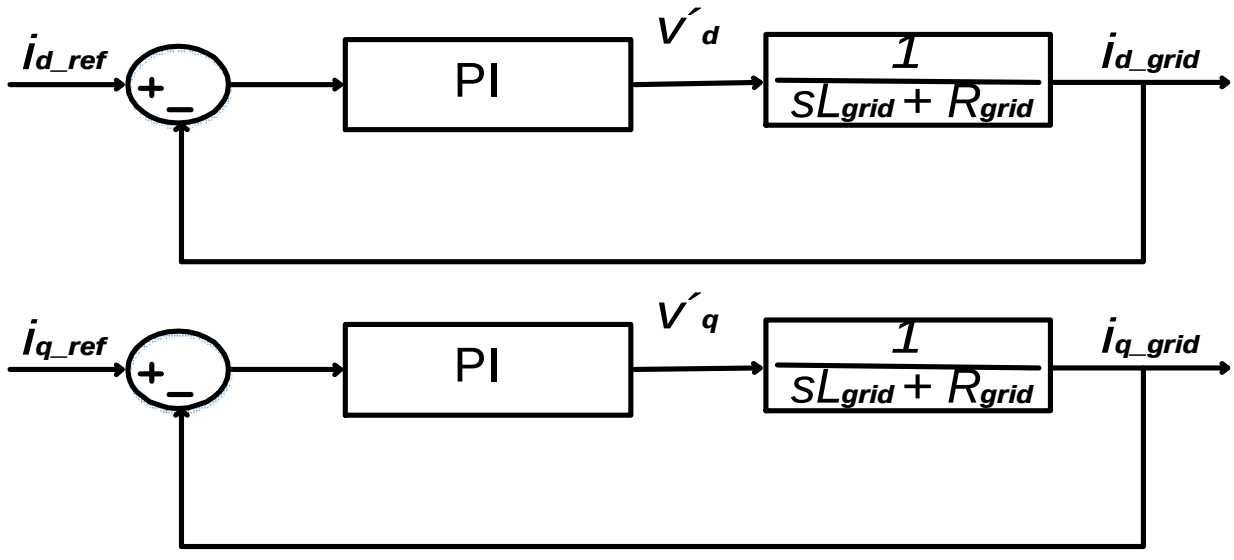

Fig. 5.7: The block diagrams of the inverter currents controllers

As mentioned in section 5.3, the bandwidth of the current controllers is set at 1256 rad/s (200 Hz). The damping factor of the controllers is set to 0.707. Matlab^{TM} code is used to calculate the proportional and integral gains of the current controllers provided in Appendix A.3.

The proportional and integral gains are:

$$k_{p\_i} = 48.3\ \Omega \tag{5.10}$$

$$k_{i\_i} = 4.42 \text{ x } 10^4\ \Omega s^{-1} \tag{5.11}$$

The step response and the Bode plot of the current controller are shown in Fig. 5.8 and Fig. 5.9, respectively. The blue lines in Fig. 5.8 and Fig. 5.9 represent the performance of the current controller. A 19.6% overshoot is observed which can damage the switching devices. Moreover, the crossover frequency is almost twice than the desired value and this fast response will create instability between the voltage and current controllers.

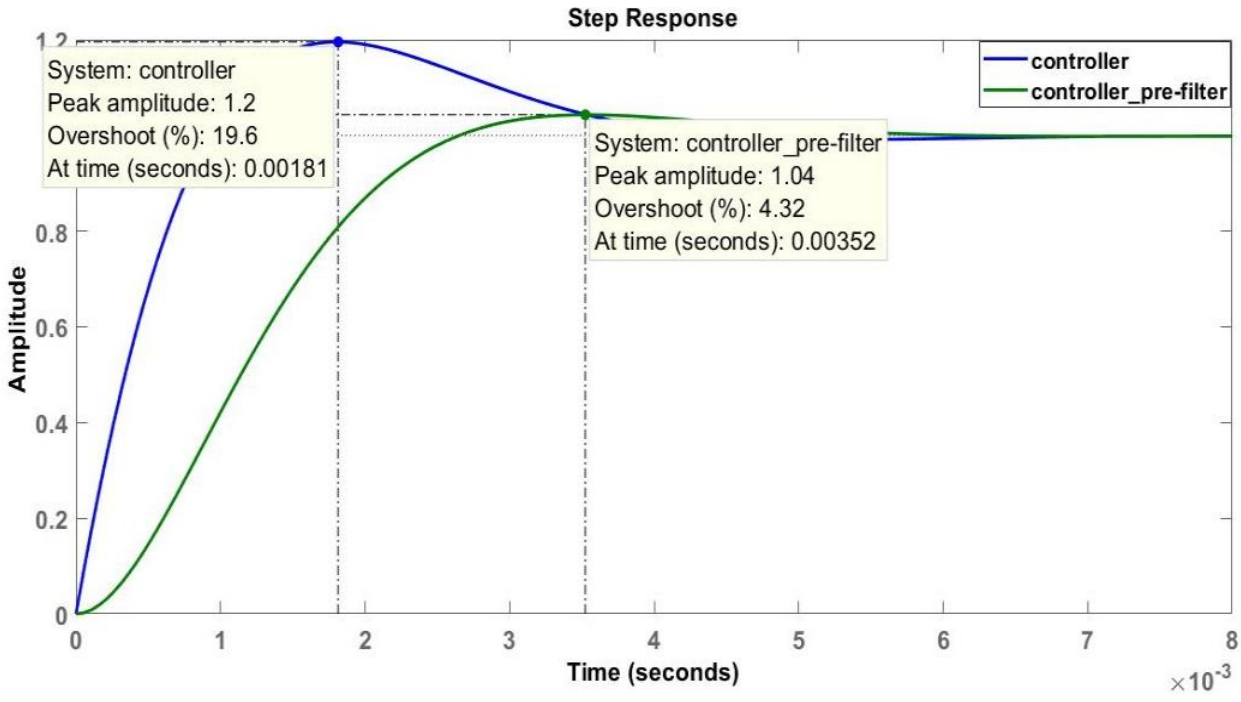

Fig. 5.8: Step response of the inverter current controller

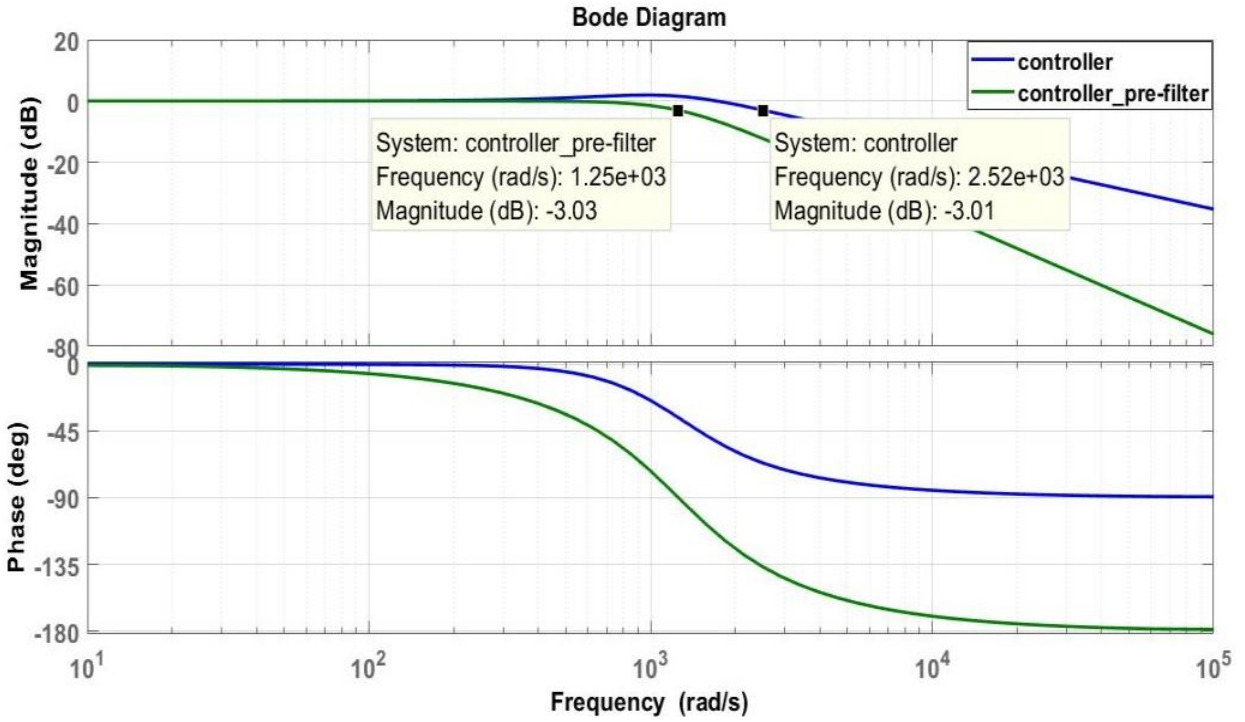

Fig. 5.9: Bode diagram of the inverter current controller

As previously, a pre-filter is designed to compensate the dynamic response which is shown in Fig. 5.10.

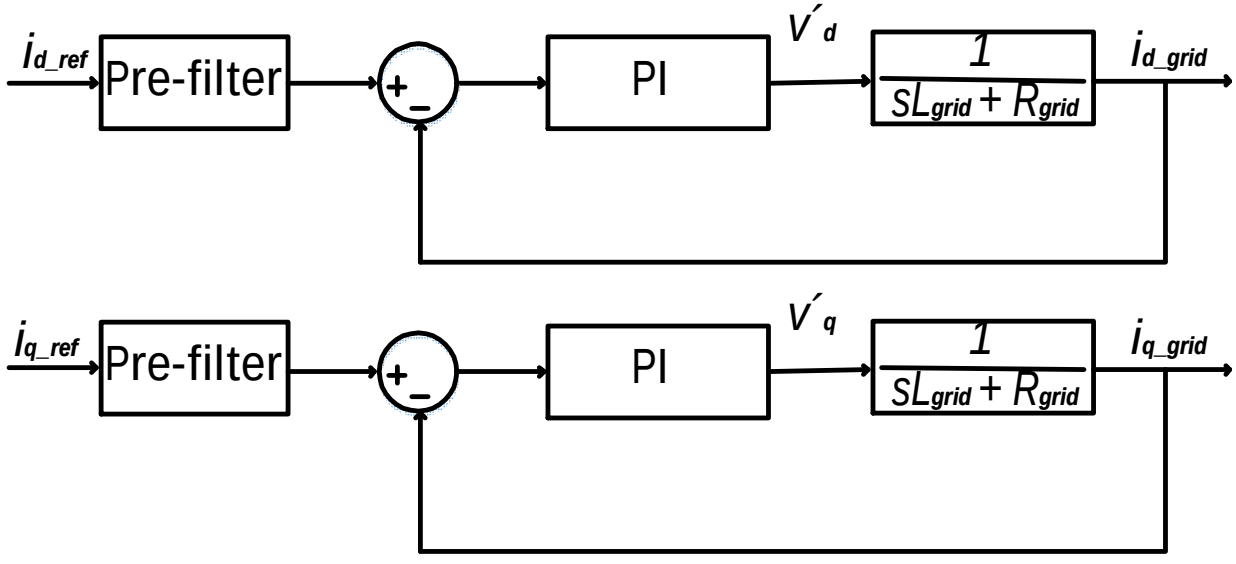

Fig. 5.10: Block diagrams of the inverter current controllers with a pre-filter

The green lines in Fig. 5.8 and Fig.5.9 represent the step response and Bode diagram of the current controller with the pre-filter. The overshoot of the system is reduced to 4.32% at 0.0035 seconds, a time slightly more than the controller without the pre-filter. The contribution of this small change in time is insignificant. The cross-over frequency also reduced to 1250 rad/s with the integration of the pre-filter. The current controller generates the signal *V** to use in the PS-PWM algorithm to control the switching devices as shown in Fig. 5.11.

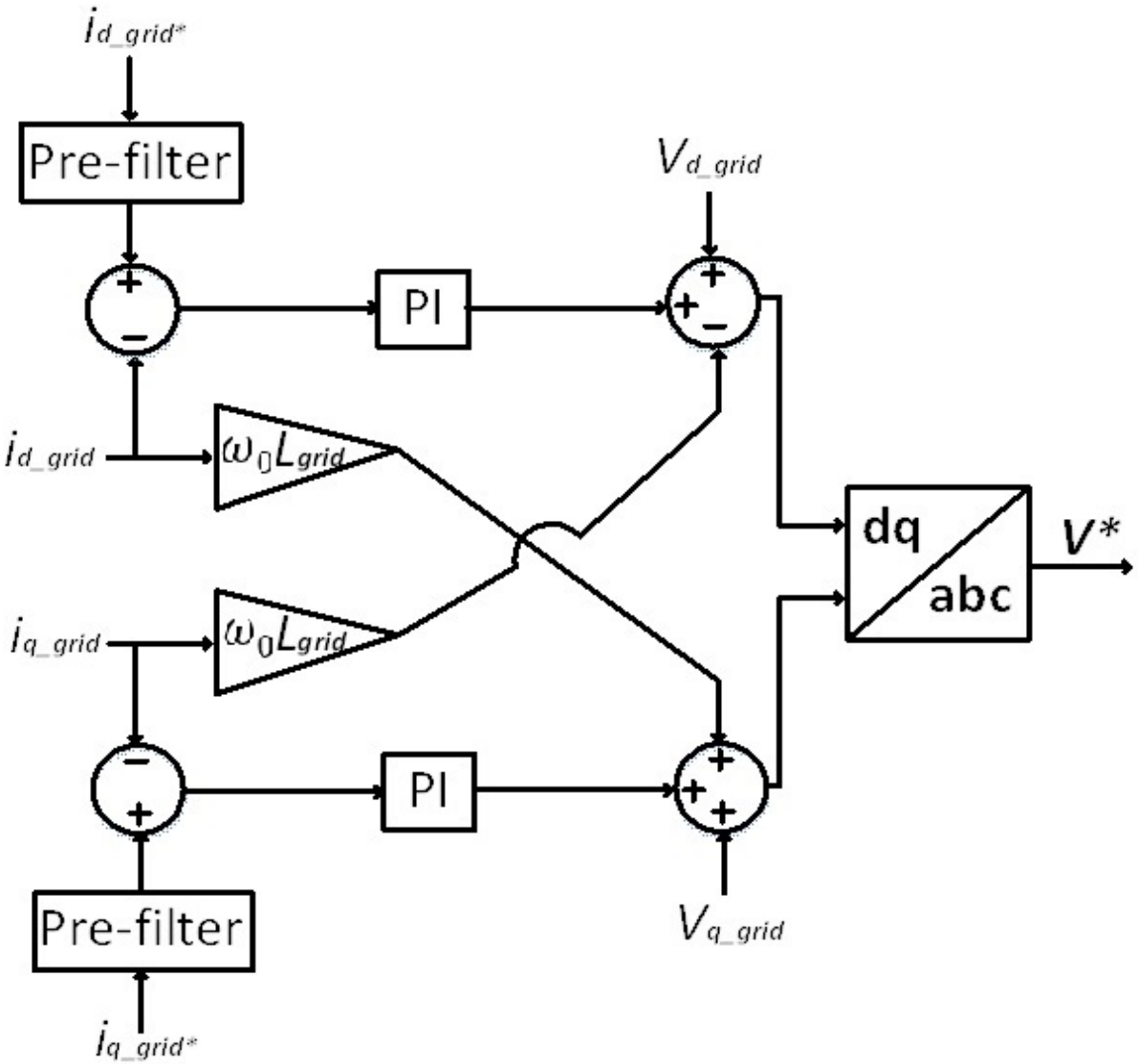

Fig. 5.11: The current controller generating the signal V*

5.5 SM Capacitor Voltage Balancing

The SM capacitor voltage and the circulating current in the leg of a MMC play important roles to stabilize the system. One of the major and more difficult tasks in the MMC-based system is to balance the SM voltages and control the circulating current. Many research works already proposed different techniques handling these issues [8]- [20]. Half-bridge SM balancing techniques were proposed in [15]- [19]. In this research, the technique proposed in [1] and [9] is used to balance the SM capacitor voltage of MMC #1 and MMC #4. These two terminals use the PS-PWM switching algorithms whereas MMC #2 and MMC #3 use the SHE technique proposed in [2] and [20]. Three different types of controllers are required for balancing the SMs. These controllers will be analyzed in this section.

5.5.1 Average voltage controller for the SM capacitors

A voltage difference is created between the dc-link and the phase-legs of an MMC by charging and discharging of SM capacitors. This voltage difference creates a circulating current which is demonstrated in Fig. 5.12. The circulating current is expressed using the upper and lower arm currents as:

$$i_{zu}(t) = \frac{i_{au}(t) + i_{al}(t)}{2} \tag{5.12}$$

where $i_{au}$and i_{al} are the upper and lower arm currents. The proposed average voltage controller has two loops: voltage and current ones [9]. The voltage loop produces the reference of the circulating current which is injected into the current loop as shown in Fig. 5.13. A proportional-integral controller is used in the voltage loop and a proportional controller is used in the current loop [9].

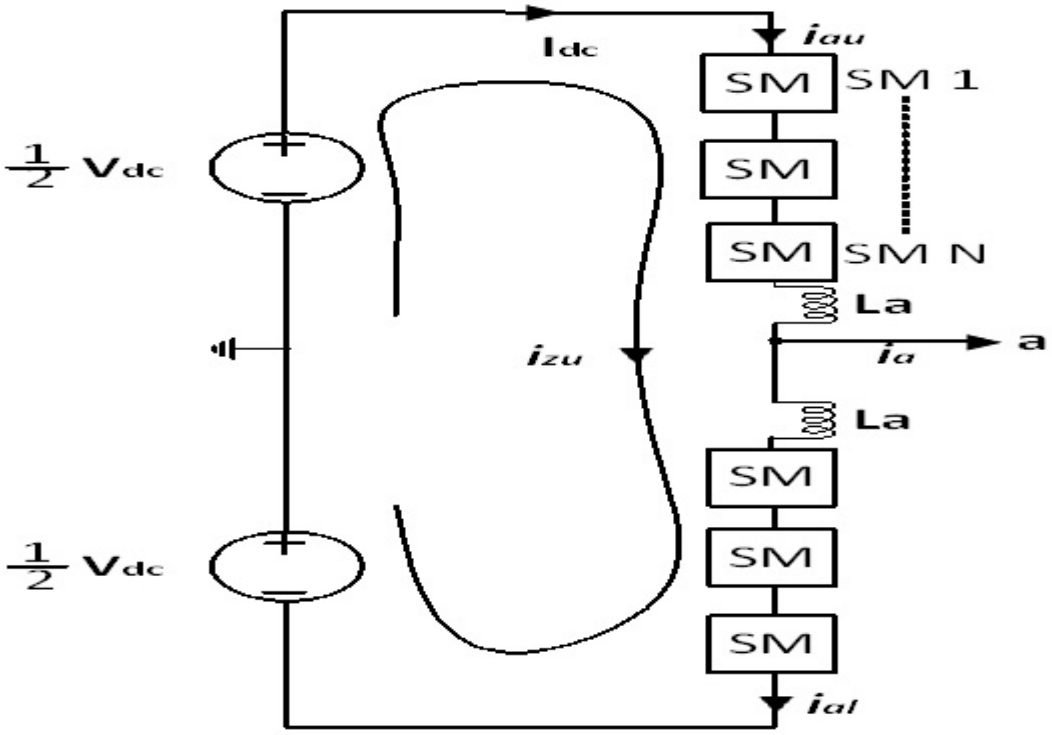

Fig. 5.12: A single-phase MMC terminal

The current loop should respond faster than the voltage loop; in order to achieve this behavior, the bandwidth of the current loop controller should be ten times larger than that of the voltage loop controller. The average SM capacitor voltage is determined by:

$$\bar{V}_{ca} = \frac{1}{2N} \sum_{j=1}^{2N} V_{cja} \tag{5.13}$$

where V_{cja} is the voltage of the j[th] SM capacitor. The voltage drop across the arm inductor is neglected here; thus, the average voltage should be $\frac{V_{dc}}{2N}$. The proposed PI controller is expressed by [9]:

$$i_{zu}^{*} = k_1(\bar{V}_{ca}{}^{*} - \bar{V}_{ca}) + k_2 \int (\bar{V}_{ca}{}^{*} - \bar{V}_{ca})dt \tag{5.14}$$

$$V_{xa} = k_3 \, (i_{zu} - i_{zu}{}^{*}) \tag{5.15}$$

where i_{zu}^{*} and $\bar{V}_{ca}$* are the references to the circulating current and average SM capacitor voltage, respectively. The gains of the controllers are k_1= 0.3 A/V, k_2= 3 A/(Vs), and k_3= 1 V/A [9]. These gains were selected after multiple simulations.

5.5.2 Instantaneous voltage controller of the SM capacitors

As the name implies, this controller simply forces the instantaneous voltage of the SM capacitor to follow the reference value which is $\frac{V_{dc}}{N}$. It is a proportional controller which uses the directions of the upper and lower arm currents. The block diagram of the controller is shown in Fig. 5.14 and described by:

$$V_{yja} = \pm\, k_4\, (\overline{V^*}_{cja} - \bar{V}_{cja}) \tag{5.16}$$

The gain of the proportional controller is selected as k_4= 0.5 [9].

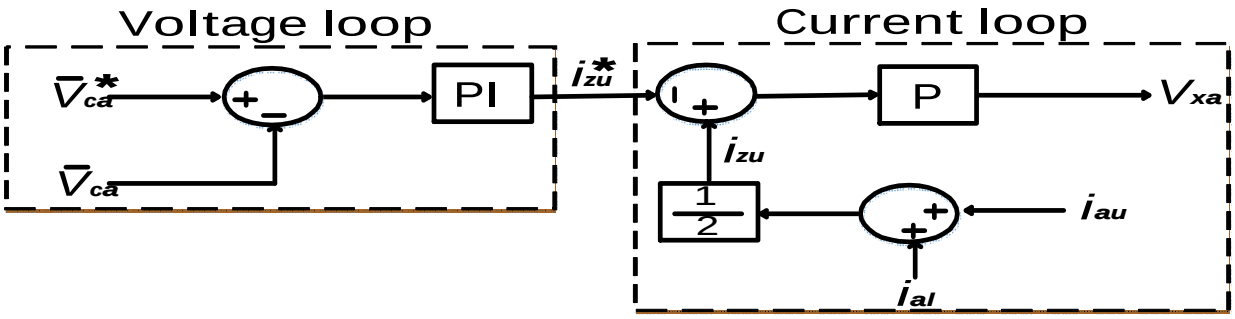

Fig. 5.13: Average voltage controller of the SMs capacitor

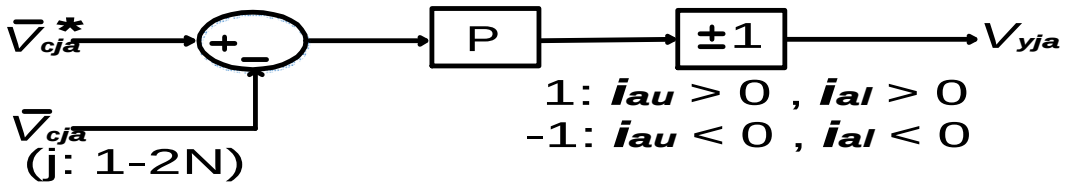

Fig. 5.14: Instantaneous voltage controller of the SMs capacitor

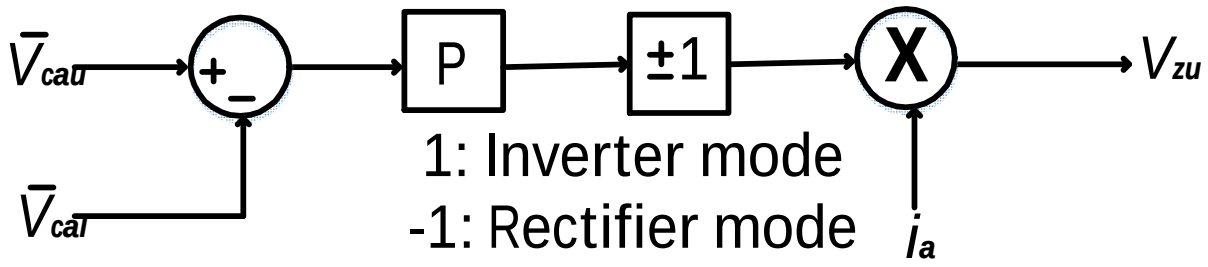

Fig. 5.15: Average voltage balancing controller of the arm

5.5.3 Average voltage balancing controller of the arm

The controller explained in sections 5.5.2 and 5.5.3 are unable to stabilize the MMC terminal in the rectifier mode [9]. The average voltage balancing controller shown in Fig. 5.15 is proposed to overcome this problem [9]. This controller minimizes the voltage difference between the upper and lower arms. The control algorithm is expressed by:

$$V_{zu} = \pm k_5 \, (\bar{V}_{cau} - \bar{V}_{cal}) \tag{5.17}$$

where '+1' and '-1' indicate inverter and rectifier modes, respectively. $\bar{V}_{cau}$and $\bar{V}_{cal}$ represent the average voltages of the upper and lower arms, respectively. The proportional gain is selected as k_5= 0.5 A^{-1} [9].

5.6 Generation of the Reference Voltages for the PS-PWM Algorithm

The reference signal for the switching devices is generated by combining the output of all the controllers. Since the upper and lower arms operate in a complementary manner, the reference signals also follow similar patterns. The generation of the reference signal is shown in Fig. 5.16.

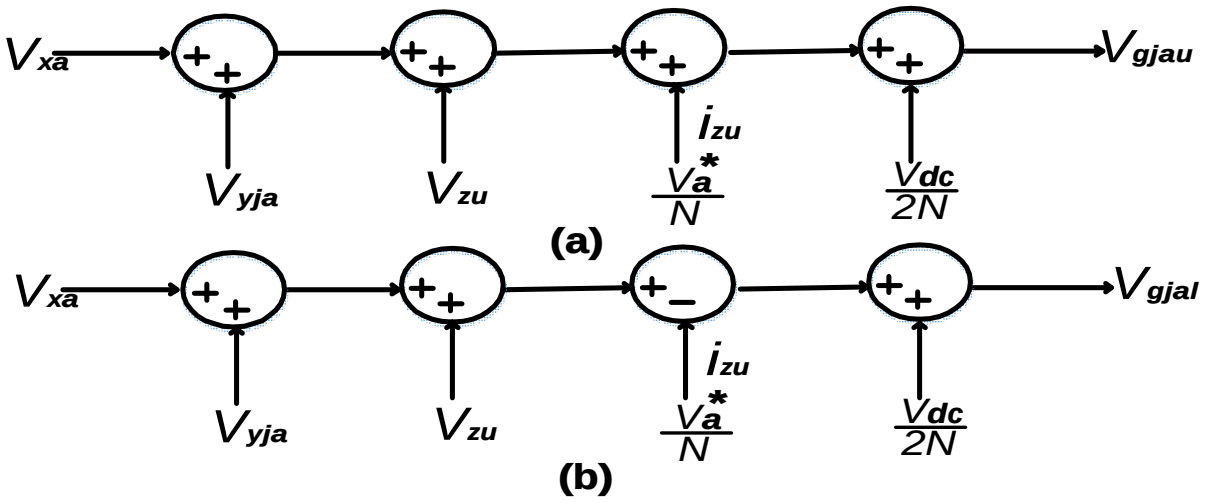

Fig. 5.16: The generation of the reference voltage: (a) upper arm, (b) lower arm

The reference signals for the upper and lower arms are expressed by [1]:

$$V_{gjau} = V_{xa} + V_{yja} + V_{zu} + \frac{V_a^*}{N} + \frac{V_{dc}}{2N} \tag{5.18}$$

$$V_{gjal} = V_{xa} + V_{yja} + V_{zu} - \frac{V_a^*}{N} + \frac{V_{dc}}{2N} \tag{5.19}$$

where V_{gjau} is the reference signal for the upper arm SMs, V_{gjal} the reference signal for the lower arm, V_{xa} the output signal of the average voltage controller, V_{yja} the output of the instantaneous voltage controller, V_{zu} the output of the arm average voltage controller, V_a^* the output of the current controller and V_{dc} the dc-link voltage. The Matlab/Simulink™ implementation of the PS-PWM algorithm is provided in the next section.

5.7 Matlab/Simulink™ Models Used for Generating Switching Signals

The average value of SM capacitor voltage was required for the average voltage controller. The model used to calculate this value is shown in Fig. 5.17. The balance control block in Fig. 5.17

containing the average voltage controller of the SM capacitor voltages is shown in Fig. 5.18. The proportional and integral controllers gains of Fig. 5.18 were provided in section 5.5.1.

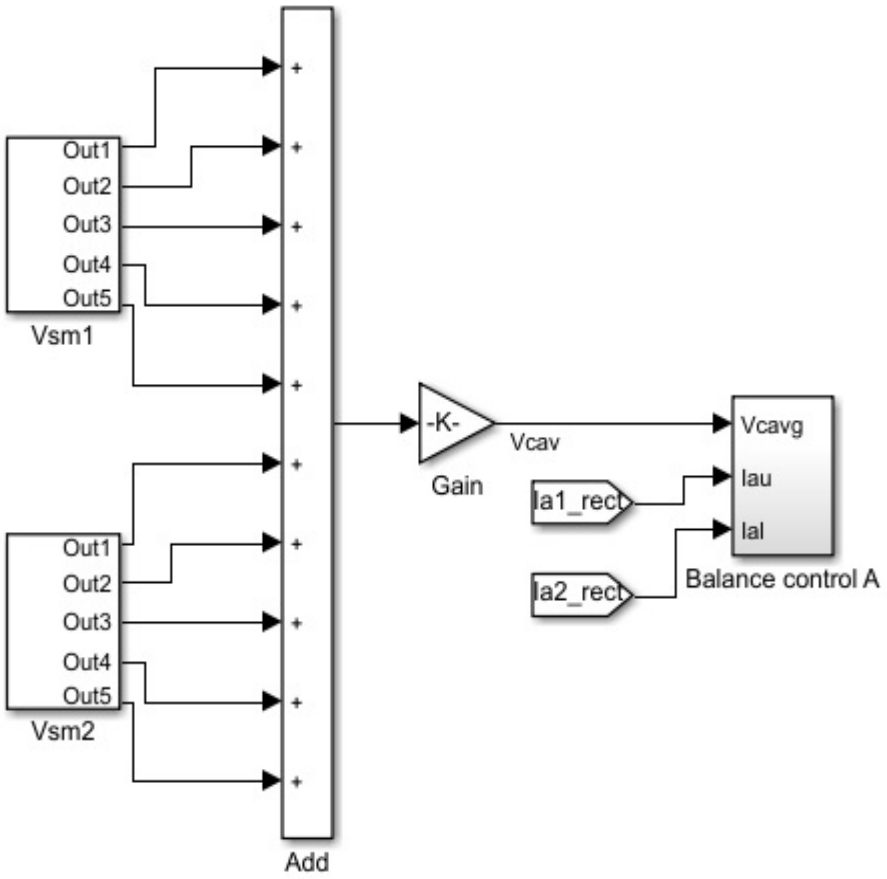

Fig. 5.17: The model used for the calculation of the average SM capacitor voltage

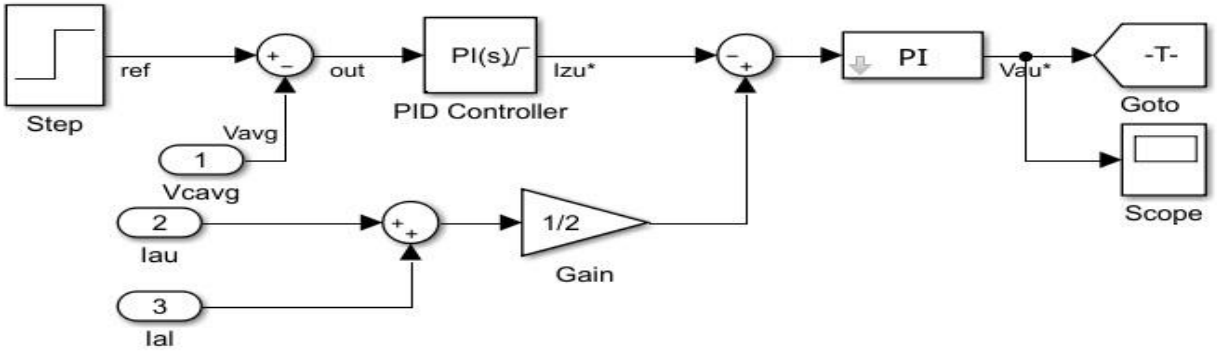

Fig. 5.18: The model used for the average voltage controller of SM capacitor voltages

The instantaneous voltage controller of the SM capacitors is shown in Fig. 5.19. The selected proportional controller gain is 0.5. The arm-balancing controller is presented in Fig. 5.20. The selected proportional controller gain is 0.5 A^{-1}.

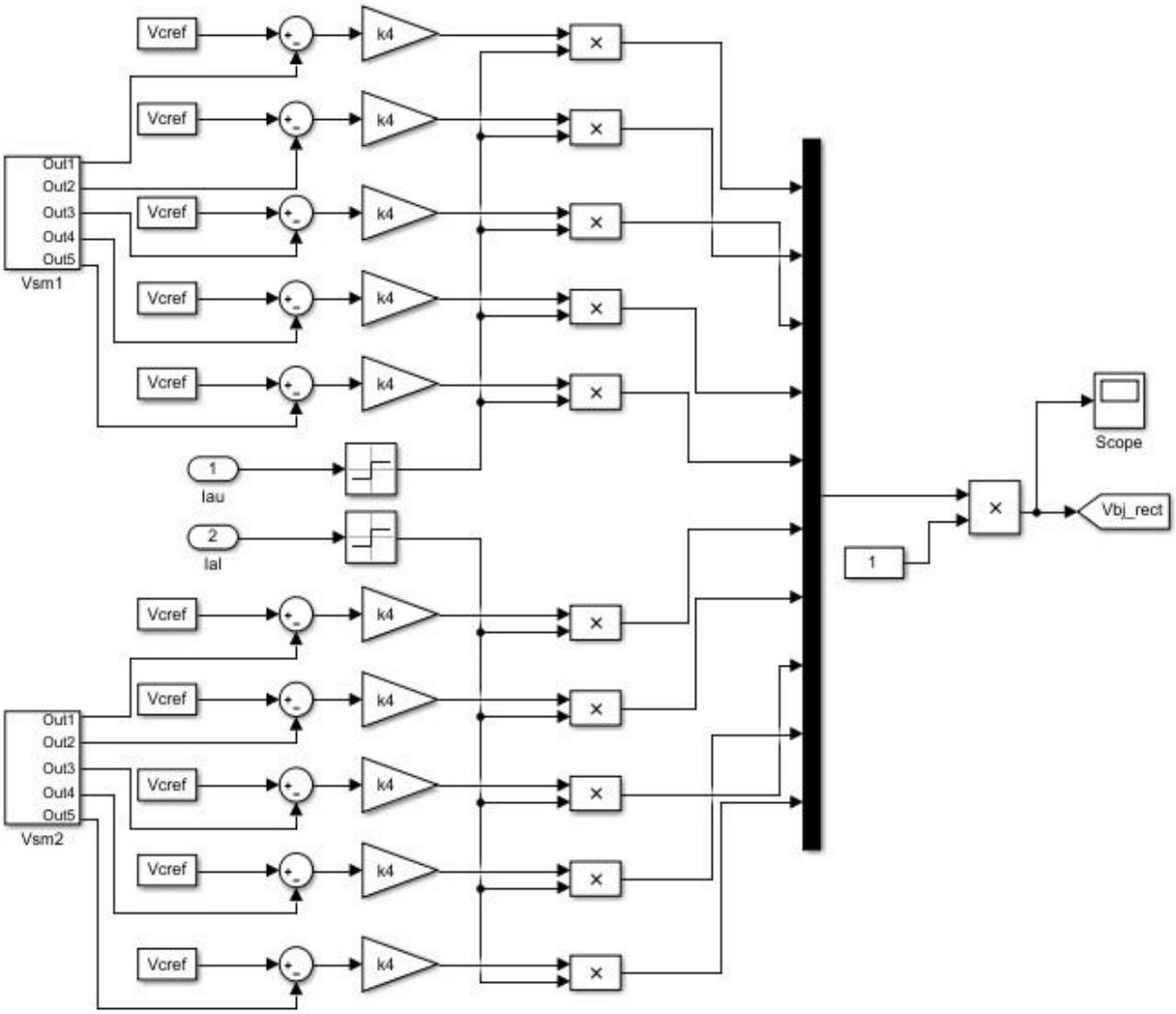

Fig. 5.19: The model used for the instantaneous voltage controller

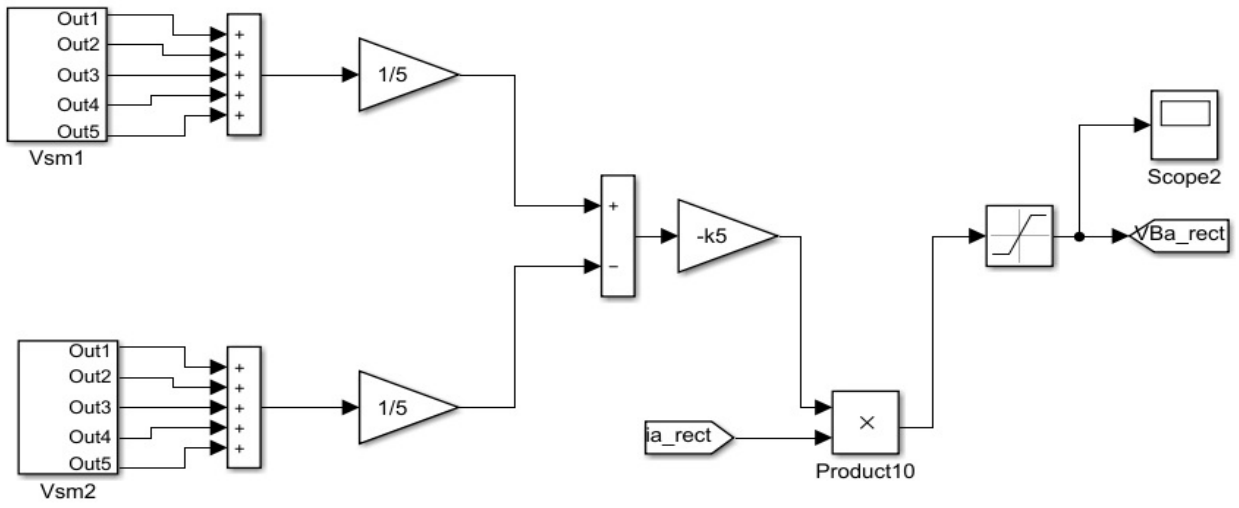

Fig. 5.20: The model used for the arm voltage balancing controller

Finally, the generation of the switching signal is given in Fig. 5.21. The reference voltage generation procedure was explained in section 5.6. These reference voltages are then normalized with respect to the actual SM capacitor voltages. Finally, these normalized signals are used as the carrier signals to generate the corresponding gate signals.

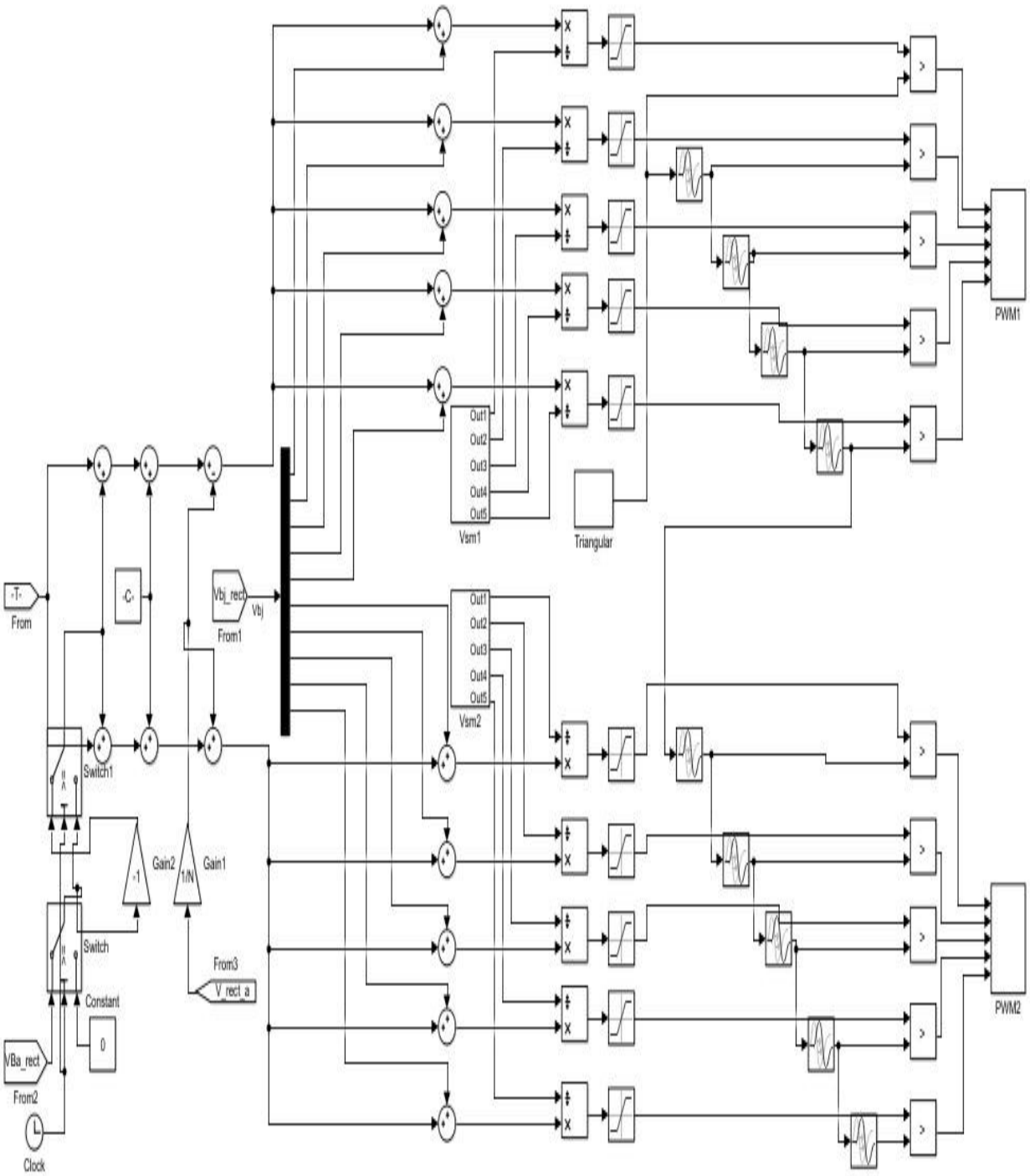

Fig. 5.21: Switching signal generation for the SMs

5.8 Switching Signal Generation for The SHE Algorithm

As mentioned in section 4.3 of chapter 4, the center of the square pulse γ_k is calculated based on the reference modulation index. A two-dimensional look-up table is produced in Matlab/Simulink^{TM} where a specific reference modulation index will trigger a value of γ_k. Finally, the m-file will generate the switching pulses based on the value of γ_k. The pulse width is kept at π to ensure that there will be no even order harmonics in the output voltage. The balancing of the SM capacitor voltages is achieved by selecting the pulse pattern mentioned in section 4.3 of Chapter 4. The next chapter will present the simulation results for all four MMC terminals.

5.9 Conclusions

This chapter discussed various procedure used for designing various controllers. The proposed controllers' performances are evaluated by means of simulations and the results of both the PS-PWM and SHE algorithms are presented in the Chapter 6 that also provides the combined results of the PS-PWM and SHE algorithms.

5.10 References

[1] M. Hagiwara and H. Akagi, “Control and experiment of pulse width modulated modular multilevel converters,” *in IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737–1746, 2009.

[2] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, “A new modulation method for the modular multilevel converter allowing fundamental switching frequency,” *in IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3482–3494, 2012.

[3] P.C. Krause, “Reference-Frame Theory,” in *Analysis of Electric Machinery*, 1st ed. McGraw Hill, 1986. pp 133-157.

[4] D. A. Guzman, High voltage direct current energy transmission using modular multilevel converters, M.S. Thesis, Department of Electrical Engineering, University of Arkansas, Fayetteville, USA, 2013.

[5] A. Yazdani and R. Iravani, “Space phasors and two-dimensional frames,” in *Voltage-Sourced Converters in Power Systems - Modeling, Control and Applications*, 1st ed. Hoboken, NJ John Wiley pp. 105.

[6] M. S. Huertas, The use of power electronics for emulating electric power distribution feeders, M.S. Thesis, Department of Electrical Engineering, University of Arkansas, Fayetteville, USA, 2008.

[7] T. Rybarski and B. Sfurtoc, Optimization of multilink DC transmission for supergrid future concepts, M.S. Thesis, Department of Energy Technology, Aalborg University, Aalborg, Denmark, 2012.

[8] M. Saeedifard and R. Iravani, “Dynamic performance of a modular multilevel back-to-back HVDC system,” in *IEEE Transactions on Power Delivery*, vol. 25, no. 4, pp. 2903, 2912, 2010.

[9] M. Hagiwara, R. Maeda, and H. Akagi, “Control and analysis of the modular multilevel cascade converter based on double-star chopper-cells (MMCC-DSCC),” in *IEEE Transactions on Power Electronics*, vol. 26, no. 6, pp. 1649, 1658, 2011.

[10] E. Solas, G. Abad, J. A. Barrena, A. Cárcar, and S. Aurtenetxea, “Modulation of modular multilevel converter for HVDC application,” in *14th International Power Electronics and Motion Control Conference (EPE/PEMC)*, pp. 84-89, 2010.

[11] A. Antonopoulos, L. Angquist, H-P. Nee, "On dynamics and voltage control of the Modular Multilevel Converter," in *13th European Conference on Power Electronics and Applications*, pp. 1-10, 2009.

[12] M. Abdelsalam, M. Marei, S. Tennakoon, and A. Griffiths. "Capacitor voltage balancing strategy based on sub-module capacitor voltage estimation for modular multilevel converters," in *CSEE Journal of Power and Energy Systems* Vol. 2, no. 1, pp. 65-73, 2016.

[13] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," in *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28-39, 2008.

[14] S. Lu, K. Li, X. Deng, S. Li, and Z. Zhao. "An improved submodule unified pulse modulation scheme for a hybrid modular multilevel converter," in *CES Transactions on Electrical Machines and Systems* Vol. 1, no. 3 pp. 322-333, 2017.

[15] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, R. Picas, and V. G. Agelidis, "A modified voltage balancing algorithm for the modular multilevel converter: evaluation for staircase and phase-disposition PWM," in *IEEE Transactions on Power Electronics*, vol. 30, pp. 4119-4127, 2015.

[16] L. He, K. Zhang, J. Xiong, and S. Fan, "A repetitive control scheme for harmonic suppression of circulating current in modular multilevel converters," in *IEEE Transactions on Power Electronics*, vol. 30, pp. 471-481, 2015.

[17] Z. Li, P. Wang, Z. Chu, H. Zhu, Y. Luo, and Y. Li, "An inner current suppressing method for modular multilevel converters," in *IEEE Transactions on Power Electronics*, vol. 28, pp. 4873-4879, 2013.

[18] A. J. Korn, M. Winkelnkemper, P. Steimer, and J. W. Kolar, "Capacitor voltage balancing in modular multilevel converters," in *6th IET International Conference on Power Electronics, Machines and Drives*, pp. 1-5, 2012.

[19] Q. Tu, Z. Xu and J. Zhang, "Circulating current suppressing controller in modular multilevel converter," *in 36th Annual Conference of the IEEE Industrial Electronics Society*, pp. 3198-3202, 2010.

[20] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, and H. P. Nee. "Circulating current control in modular multilevel converters with fundamental switching frequency," *in Power Electronics and Motion Control Conference (IPEMC), IEEE 7th International*, vol. 1, pp. 249-256, 2012.

Appendix A.1

Simulation Model of The Park's Transformation

The dq transformation of the grid voltages and currents in Matlab/Simulink™ is shown in Fig. A.1 and Fig. A.2. The PLL produces the angle "Theta", which is used in the dq transformation, as shown in Fig. A.3. The proportional and integral controllers gains for PLL are set at 2 and 0.1, respectively [4]. The functions $f_1(u)$, $f_2(u)$, $f_3(u)$, and $f_4(u)$ perform the following operations:

$$f_1(u) = u(1) - \frac{1}{2}\{u(2) + u(3)\} \quad \text{(A.1.1)}$$

$$f_2(u) = \frac{\sqrt{3}}{2}\{u(2) - u(3)\} \quad \text{(A.1.2)}$$

$$f_3(u) = p(1)\cos\theta + p(2)\sin\theta \quad \text{(A.1.3)}$$

$$f_4(u) = -p(1)\sin\theta + p(2)\cos\theta \quad \text{(A.1.4)}$$

where $u(1)$, $u(2)$, $u(3)$ and $p(1)$, $p(2)$ are the input signals for the functions $f_1(u)$, $f_2(u)$ and $f_3(u)$, $f_4(u)$, respectively. $u(1)$, $u(2)$, $u(3)$ denote three phase voltages and three line current of the grid for the dq transformation of the grid voltage and current, respectively. $p(1)$ and $p(2)$ are the α, β components of the grid voltage and current.

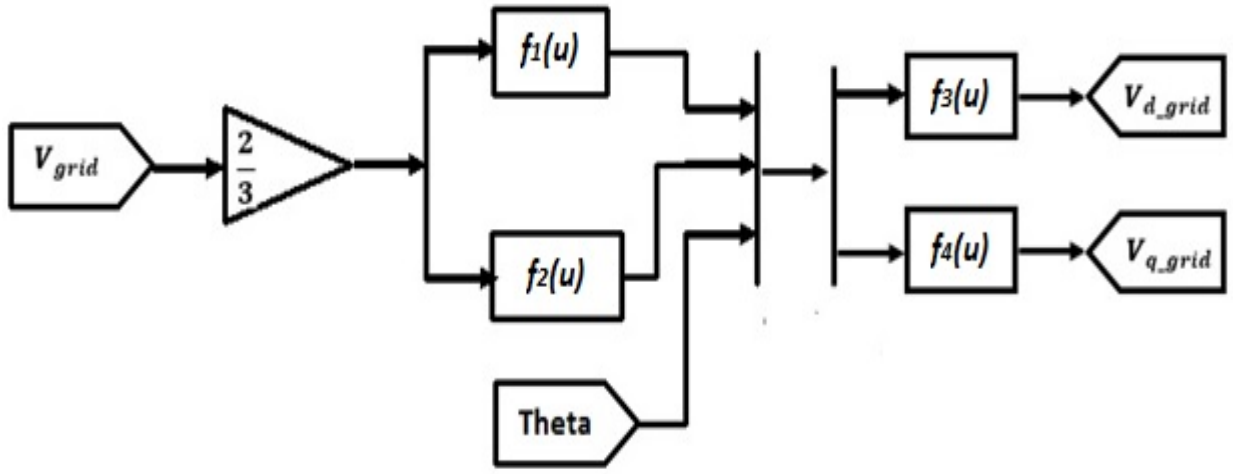

Fig. A.1: The dq transformation of the grid voltages

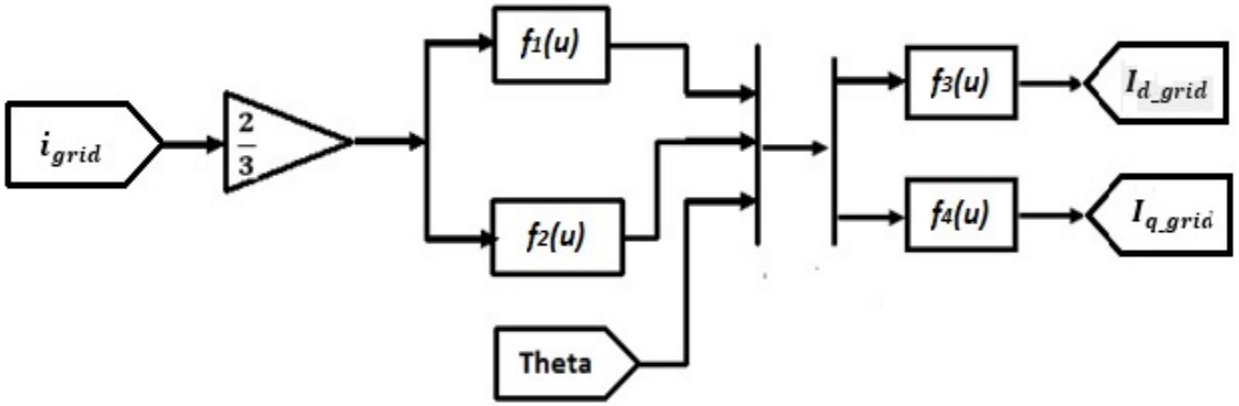

Fig. A.2: The dq transformation of the grid currents

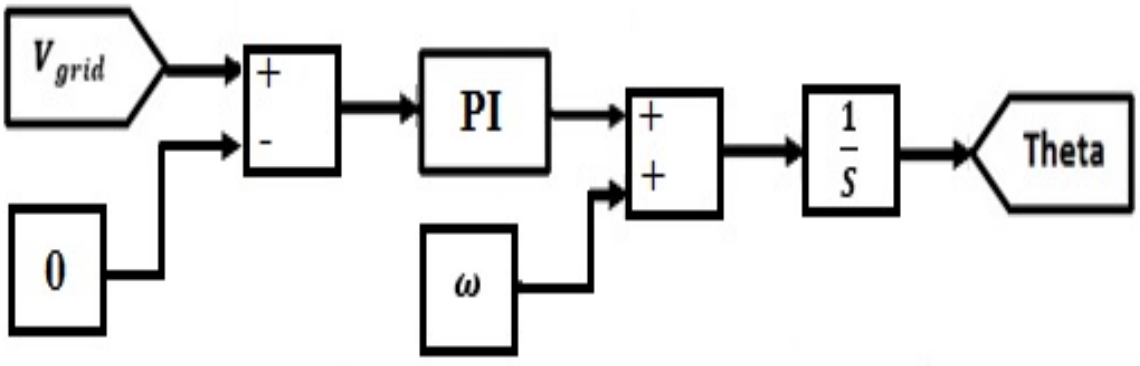

Fig. A.3: Angle "Theta' generation in PLL

The inverse Park's transformation is shown in Fig. A.4. The functions $f_5(u)$, $f_6(u)$, $f_7(u)$, $f_8(u)$, and $f_9(u)$ perform the following operations:

$$f_5(u) = q(1)\cos\theta - q(2)\sin\theta \quad \text{(A.1.5)}$$

$$f_6(u) = q(1)\sin\theta + q(2)\cos\theta \quad \text{(A.1.6)}$$

$$f_7(u) = r(1) \quad \text{(A.1.7)}$$

$$f_8(u) = -\frac{1}{2} r(1) + \frac{\sqrt{3}}{2} r(2) \quad \text{(A.1.8)}$$

$$f_9(u) = -\frac{1}{2} r(1) - \frac{\sqrt{3}}{2} r(2) \quad \text{(A.1.9)}$$

where $q(1)$, $q(2)$, and $r(1)$, $r(2)$ are the input signals for the functions $f_5(u)$, $f_6(u)$ and $f_7(u)$, $f_8(u)$, $f_9(u)$, respectively.

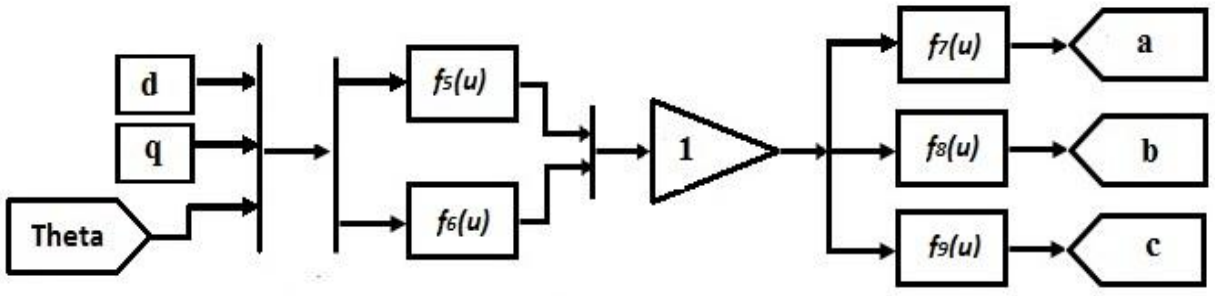

Fig. A.4: Inverse Park's transformation

Appendix A.2

Simulation Model for a Two-Level Rectifier

The two-level rectifier model used to evaluate the gains of the controllers is shown in Fig. A.5. The simulation model was developed in [4] and modified for this research. The control block contains the dc-voltage controllers mentioned in section 5.3. The rectifier block is modeled with ideal switches and switched with the signals generated in the control block.

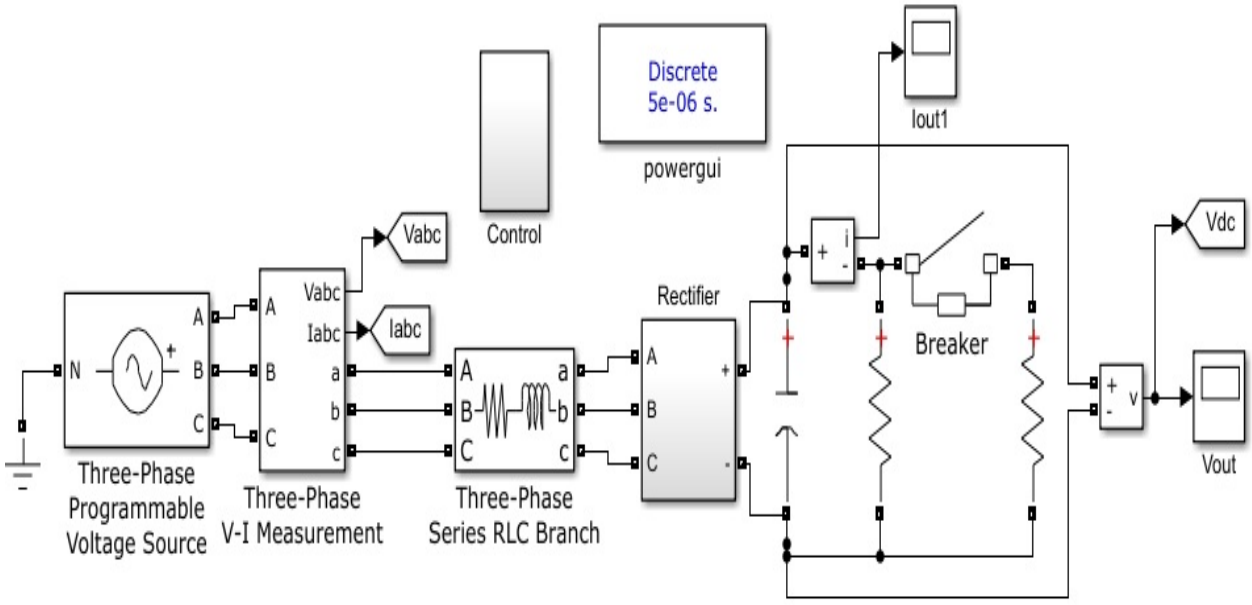

Fig. A.5: Two-level rectifier model in Matlab/Simulink™

Appendix A.3

Matlab™ Codes Used to Determine the Gains of the Controllers

The dc-link voltage and current controller's gains were calculated using Matlab™. The step-response and the Bode diagram were also generated in Matlab™. The code used for the dc-link voltage controller is provided below:

```
C = 35e-3; %dc-link capacitance
Gdc = tf(1,[C 0]); %dc cap transfer function
d=sqrt(2)/2; %damping
fcdc=20; %controller natural frequency in Hz
wndc=2*pi*fcdc; %controller natural frequency in rad/s
ki_v=C*wndc^2; %integral gain of the dc-link voltage controller
kp_v=2*d*wndc*C; %proportional gain of the dc-link voltage
controller
Cdc=tf([kp_v ki_v],[1 0]); %Vdc controller tf
% Pre-filter %
Fdc=tf(1,[kp_v/ki_v 1]); %pre-filter tf to minimize overshoot
controller = feedback(Gdc*Cdc,1);
controller_pre_filter = Fdc*feedback(Gdc*Cdc,1);
% Stability plots %
figure(3)
step(controller,controller_pre_filter)
figure(4)
bode(controller,controller_pre_filter)
```

The code used for current controller is provided below:

```
L=28e-4;
R=0.64;
Ginv = tf(1,[L R]); %Transfer function
% To calculate the gains of the current controller %
d = sqrt(2)/2; %damping
fci=200; %controller natural frequency in Hz
wn=2*pi*fci; %controller natural frequency in rad/s
ki_i=L*wn^2; %integral gain of current controller
kp_i=2*d*wn*L-R; %proportional gain of current controller
Cc=tf([kp_i ki_i],[1 0]); %current controller tf
% Pre-filter %
Fi=tf(1,[kp_i/ki_i 1]); %pre-filter tf to minimize overshoot
controller=feedback(Ginv*Cc,1);
controller_pre_filter=Fi*feedback(Ginv*Cc,1);
% Stability plots %
figure(1)
step(controller,controller_pre_filter)
figure(2)
bode(controller,controller_pre_filter)
```

CHAPTER 6

SIMULATION RESULTS OF THE MPS SYSTEM

6.1 Introduction

Simulation models of different MMC terminals are produced in Matlab/Simulink™ using two different PWM switching strategies. The PS-PWM-based terminal behavior will be discussed in section 6.2 and the SHE-based terminal behavior will be analyzed in section 6.3. Finally, the combined response of the MPS system is discussed in section 6.4. The controllers developed in Chapter 5 are used in the simulation models to evaluate the overall performances of the system. The system parameters and values of the passive components used in the simulations are listed in Table 6.1. The gains of the different controllers are listed in Table 6.2.

Table 6.1: Simulation parameters of the MPS system

Properties	**MMC #1**	**MMC #2**	**MMC #3**	**MMC #4**
Active power (MW)	6	6	6	6
Rated rms line-line voltage (kV)	25	25	13.8	13.8
DC-link voltage (kV)	44	44	24	24
Rated rms current (A)	138.6	138.6	251	251
Peak current (A)	196	196	355	355
Operating frequency (Hz)	60	1000	1000	60
Switching frequency (Hz)	1000	1000	1000	1000
SM capacitance (mF)	0.6	0.3	1	2
Arm inductance (mH)	8.29	0.5	0.15	2.53

Table 6.2: Gains of the different controllers

	DC-Voltage Controller		Current Controller		SM Capacitor Voltage Controllers				
Parameter	k_{p_v}	k_{i_v}	k_{p_i}	k_{i_i}	k_1	k_2	k_3	k_4	k_5
Value	6.22	552.7	48.3	4.42 x 10^4	0.3	3	1	0.5	0.5

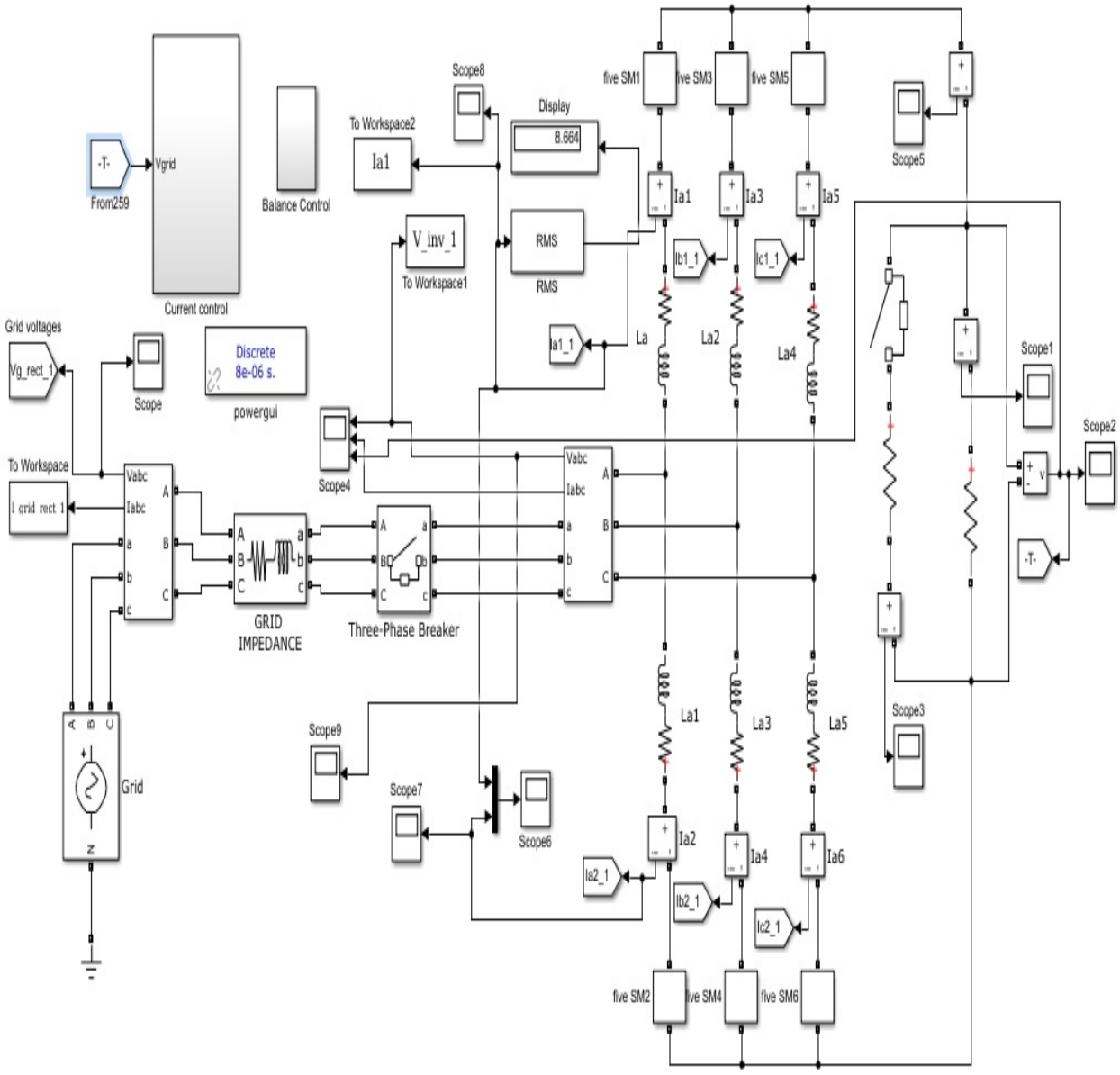

Fig. 6.1: Simulation set-up of MMC #1 terminal

6.2 PS-PWM Based Operation

MMC #1 and MMC #4 terminals are operating under the PS-PWM algorithm where the first one operates as a rectifier and the later operates as an inverter. The simulation model of MMC #1 terminal is presented in Fig. 6.1 when the terminal is delivering power to a resistive load. The phase-to-neutral voltage of the terminal, having a peak value of 20.41 kV, is shown at the top of Fig. 6.2. The line current of the terminal, having a peak value of 196.1 A, is at the bottom of Fig. 6.1. The values and the wave-shape match the theoretical values. The dc-link voltage and current are shown in Fig. 6.3 and the average values are 44.1 kV and 136.06 A, respectively. The circuit breaker is closed at 0.02 s and the system stabilize within 0.05 s. Overshoots were not observed in the voltage and current. However, the dc-link voltage contains a ripple of ±16% because the designed system has only five levels and each level corresponds a voltage of 8.8 kV. When the number of levels increases significantly this ripple will reduce accordingly for example if the system is simulated with 11 levels, the system would have a ripple of ±9%. DC-link current also carries this ripple which is generated from the voltage ripple. Although the load is resistive, there are grid and arm inductance in the system which cause the phase difference between the voltage and current. The shape of the dc current simply flows the dc-link voltage which had that significant ripple.

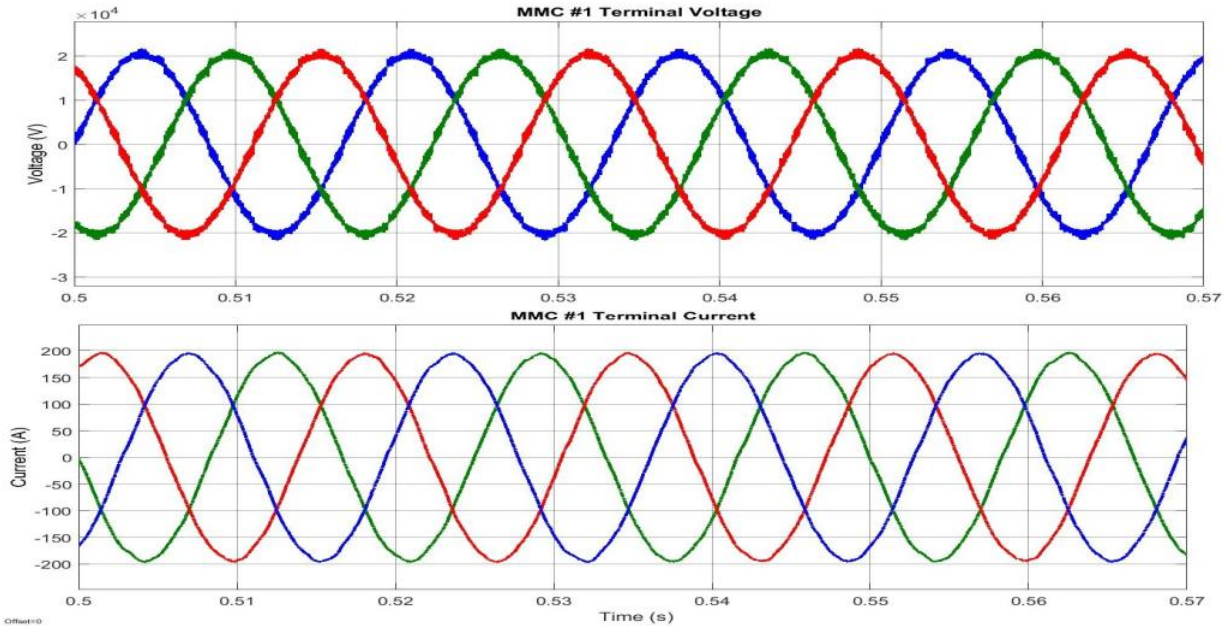

Fig. 6.2: MMC #1 terminal voltage and current waveforms

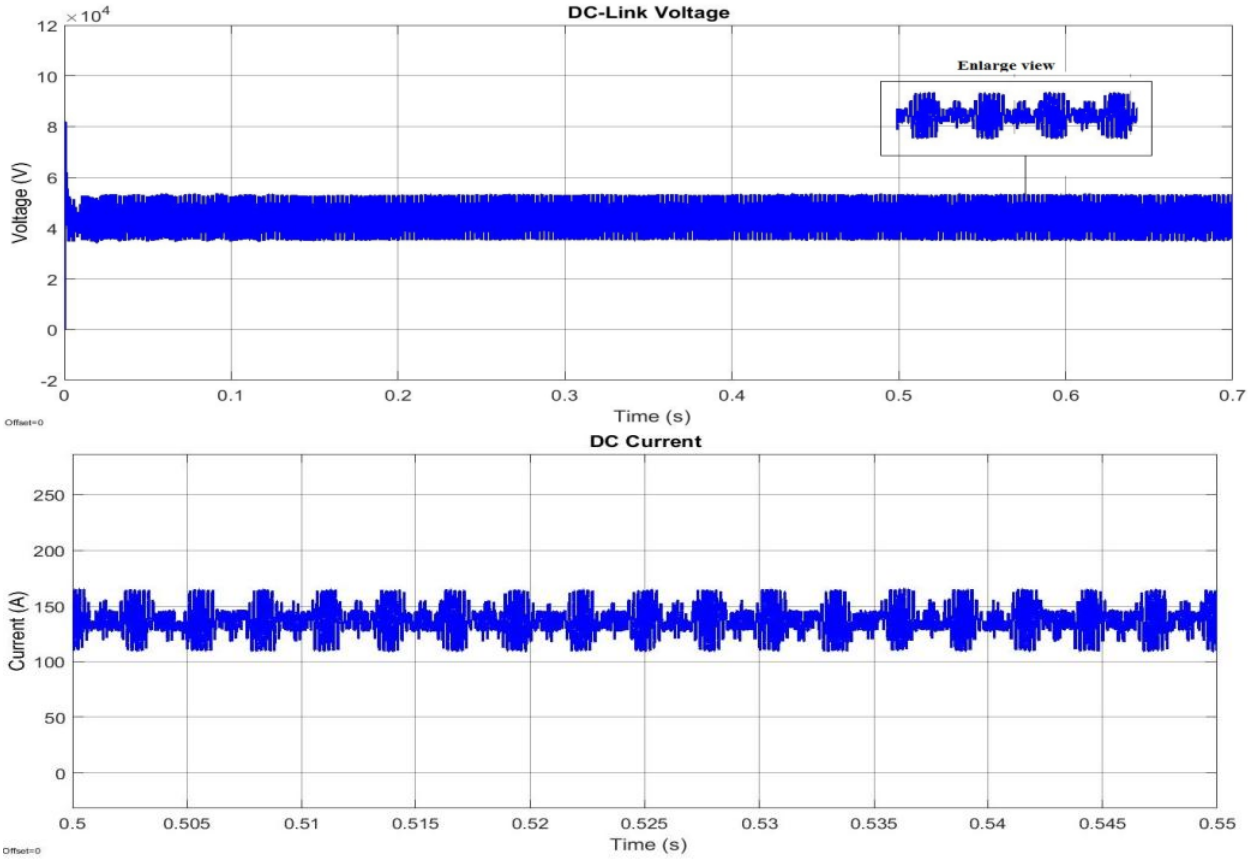

Fig. 6.3: DC-link voltage and current

The simulation model of MMC #4 terminal is shown in Fig. 6.4. The dc-link voltage is represented as a dc voltage source injecting 6 MW power into the inverter terminal. A resistive load is used in this terminal as well. The phase-to-neutral voltage and line current of this terminal are shown in Fig. 6.5. The peak values of the voltage and current are 11.3 kV and 353.9 A and are in accordance with the theoretical values. The behavior of this terminal with a change in load is also verified by changing the load command with the results are shown in Fig.6.6. At time 0.15 s, the load is suddenly doubled from 3 MW to 6 MW and the power controllers react accordingly.

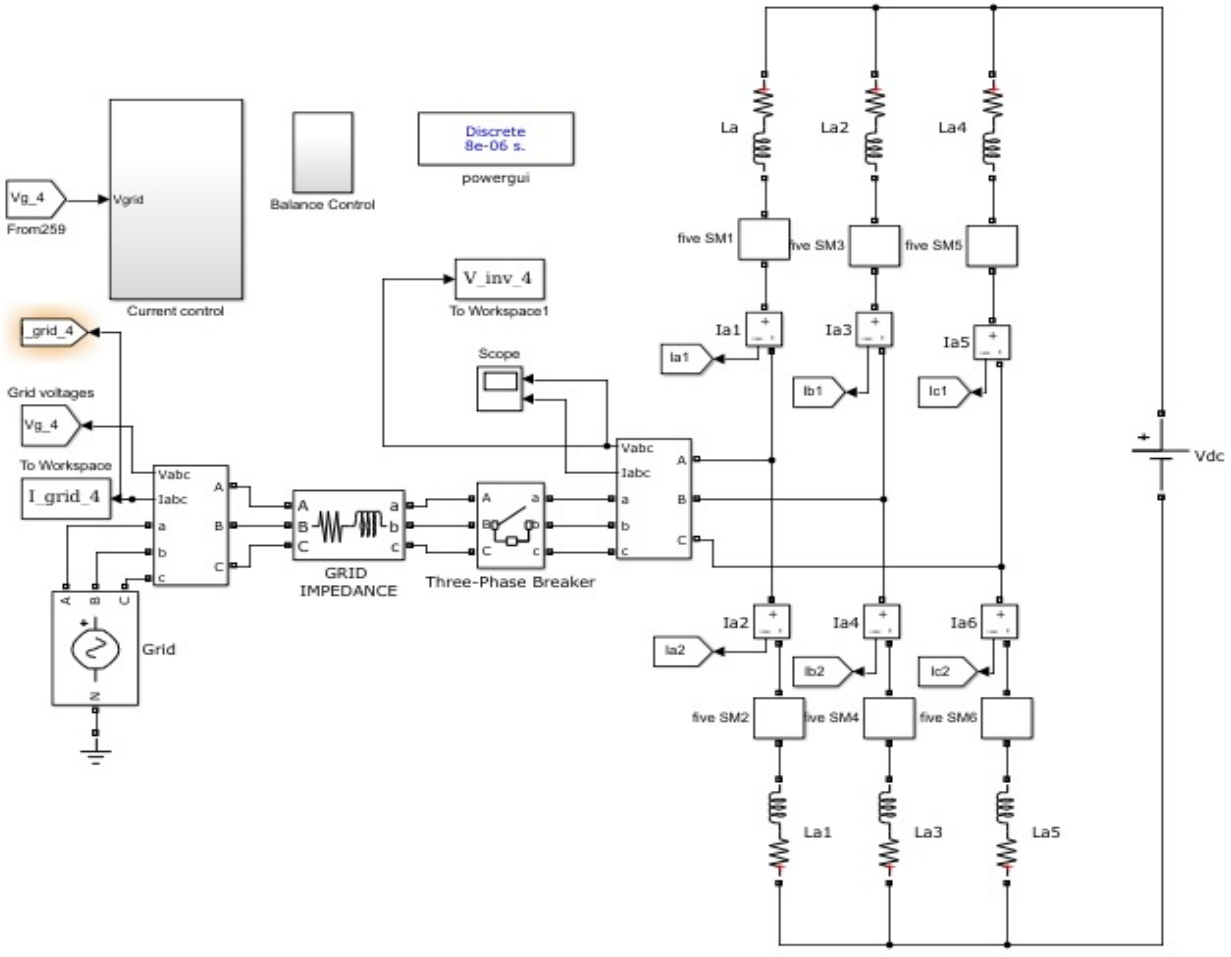

Fig. 6.4: Simulation set-up of MMC #4 terminal

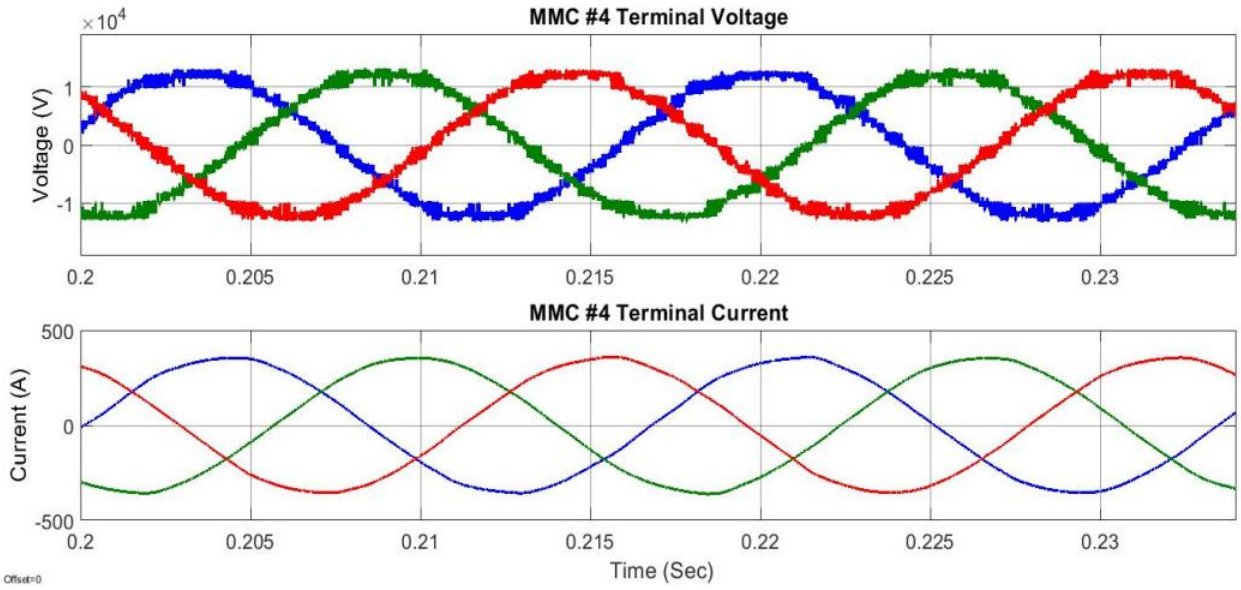

Fig. 6.5: MMC #4 terminal voltage and current waveforms

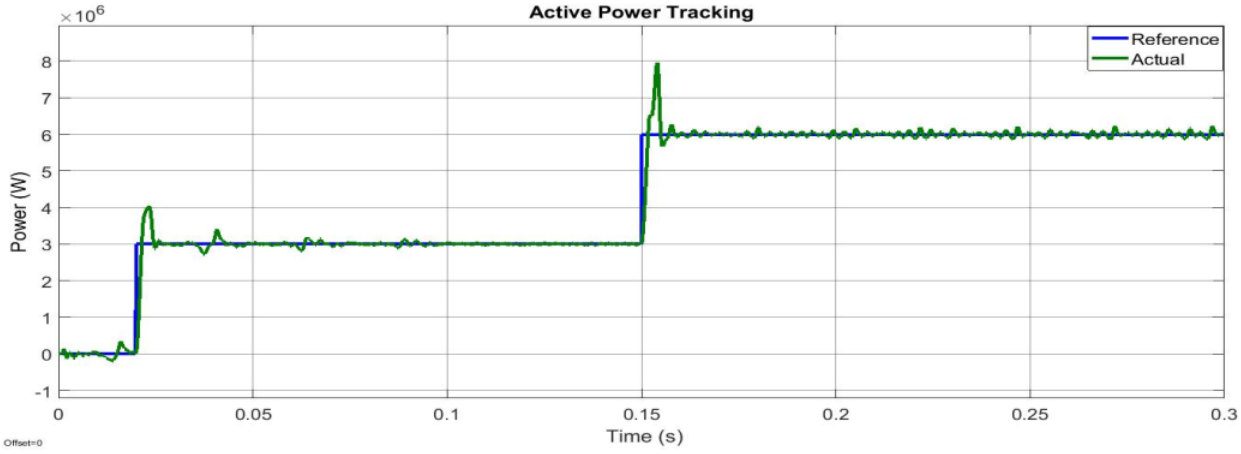

Fig. 6.6: Tracking of the system active power

The blue line is the reference signal that is commanded and the green line is the actual signal which is tracking the reference signal. The changes in voltage and current are shown in Fig. 6.7. This sudden disturbance in the system is automatically handled by the controllers within a second. The peak values of the voltage and current reached peak values of 12.54 kV, and 496.4 A, respectively; and these overshoots do not cross the safe operating area of the system.

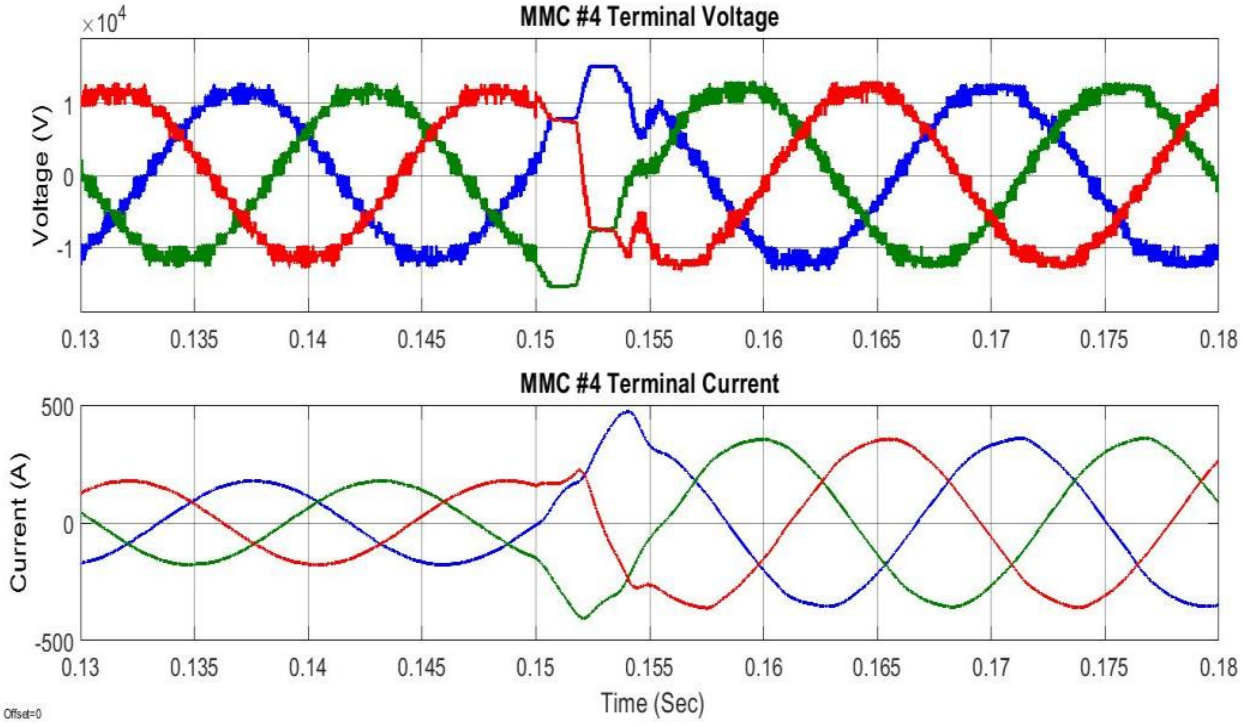

Fig. 6.7: MMC #4 terminal voltage and current waveforms with a change in load

The behavior of the phase and circulating currents are demonstrated in Fig. 6.8. The phase current (blue line) has a peak value of 351 A, which is very close to the theoretical value of 340 A and verifies that the system is operating at 60 Hz. The green line represents the circulating current which contains a significant 2nd order harmonic. The FFT analysis of the circulating current is conducted and shown in Fig. 6.9, shows that the 2nd order harmonics has the magnitude of 3.9 times of the fundamental component. A dc-offset current is present due to the contribution of the system dc current. The peak value of the circulating current is 200 A which is in accordance with its theoretical value.

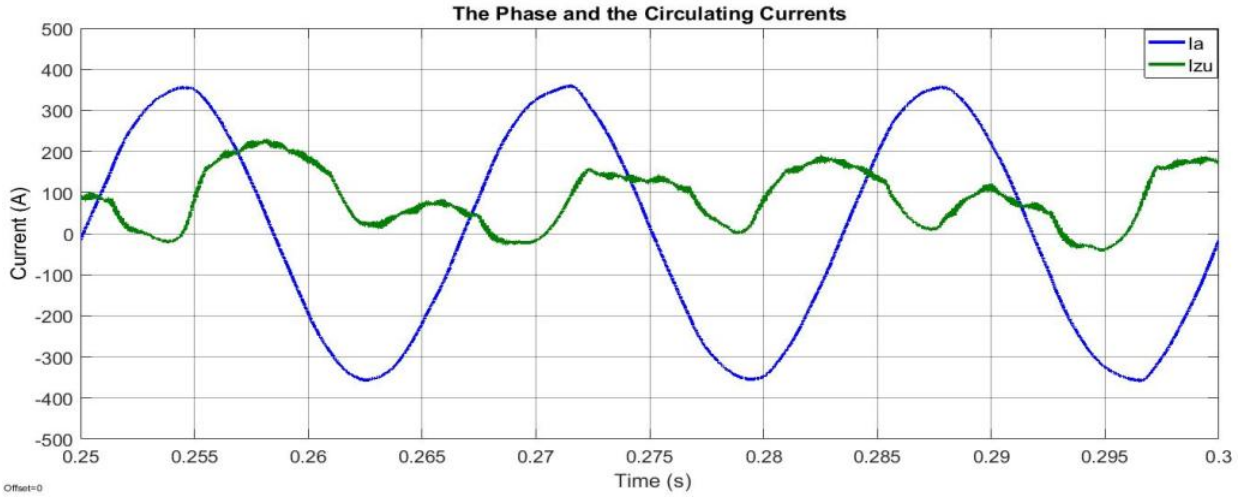

Fig. 6.8: The phase and circulating current waveforms

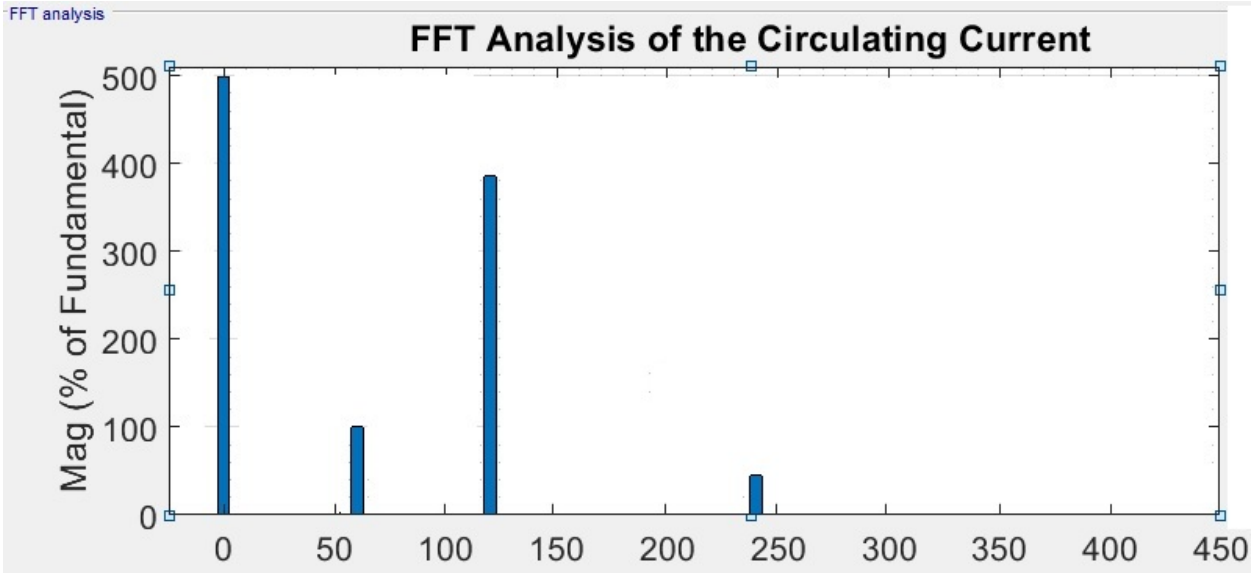

Fig. 6.9: The phase and circulating current waveforms

The upper (green line) and lower (red line) arm currents with the phase current (blue line) are shown in Fig. 6.10. Both upper and lower arm currents contain significant 2nd order harmonics due to the circulating current which is presented in Fig. 6.9. These currents are out of phase as expected. The upper and lower arms of the MMC terminal operate in a complementary manner. This concept is verified by observing the SM capacitor voltages of the upper and lower arms.

The blue and green lines in Fig. 6.11 represent the first SM capacitor voltages of the upper and lower arms, respectively. The selection objective of the SM capacitor size was to keep the ripple voltage within ±10%; the average SM capacitor voltage is 4.8 kV and contains ±6.25% ripple. The behavior observed in the simulation results of the PS-PWM based terminals were similar with the behavior observed in [1]- [4].

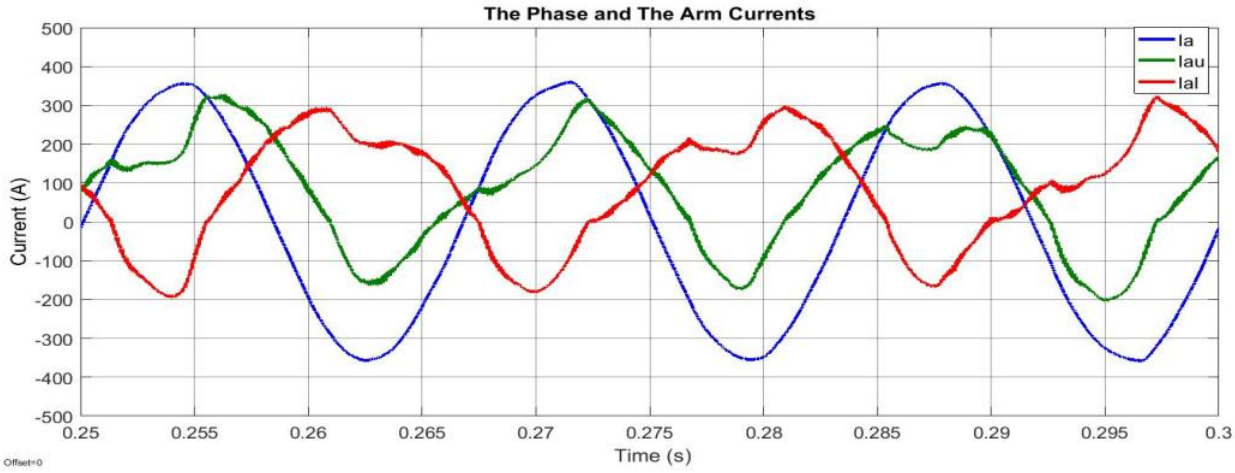

Fig. 6.10: The phase and arm current waveforms

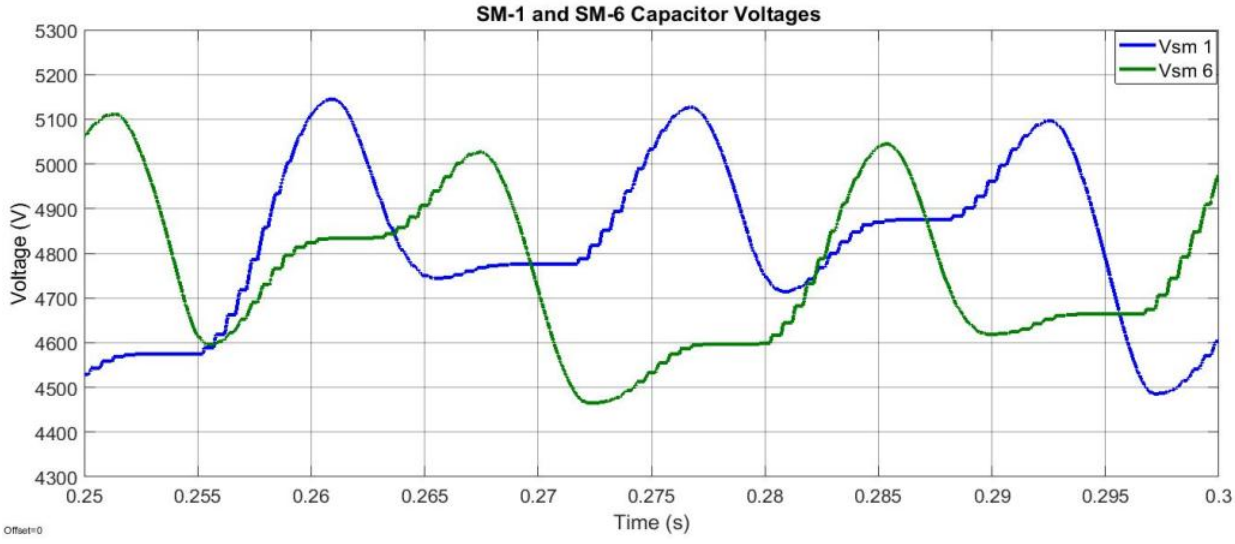

Fig. 6.11: SM capacitor voltage waveforms

6.3 SHE Based Operation

The MMC #2 and MMC #3 terminals operated using the SHE algorithm where the first one operates as an inverter and later operates as a rectifier with resistive loads. The simulation model of MMC #2 terminal is presented in Fig. 6.12. The circuit configuration is identical to the MMC #4 terminal. The operating and switching frequencies are kept at 1 kHz.

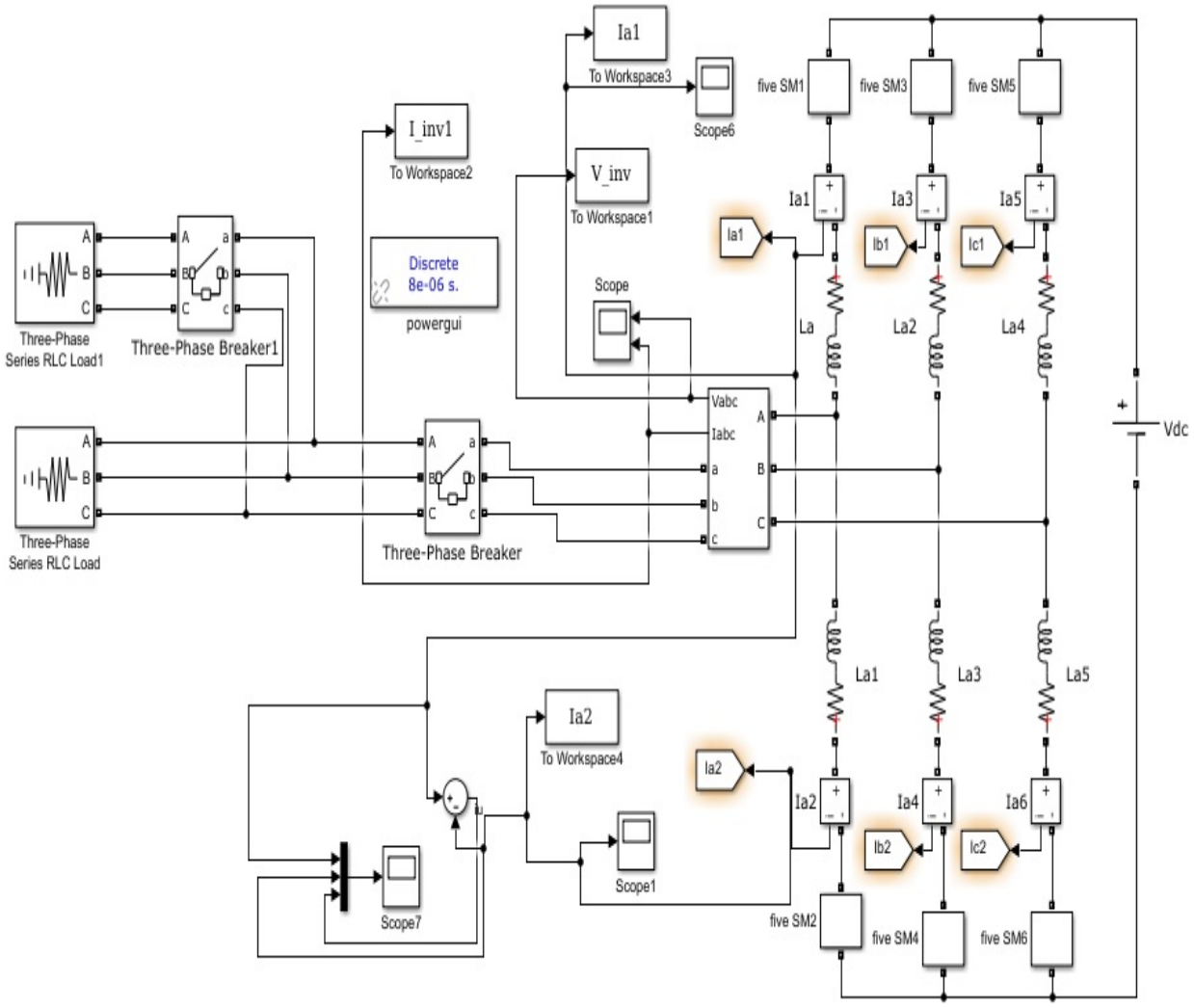

Fig. 6.12: Simulation set-up of MMC #2 terminal

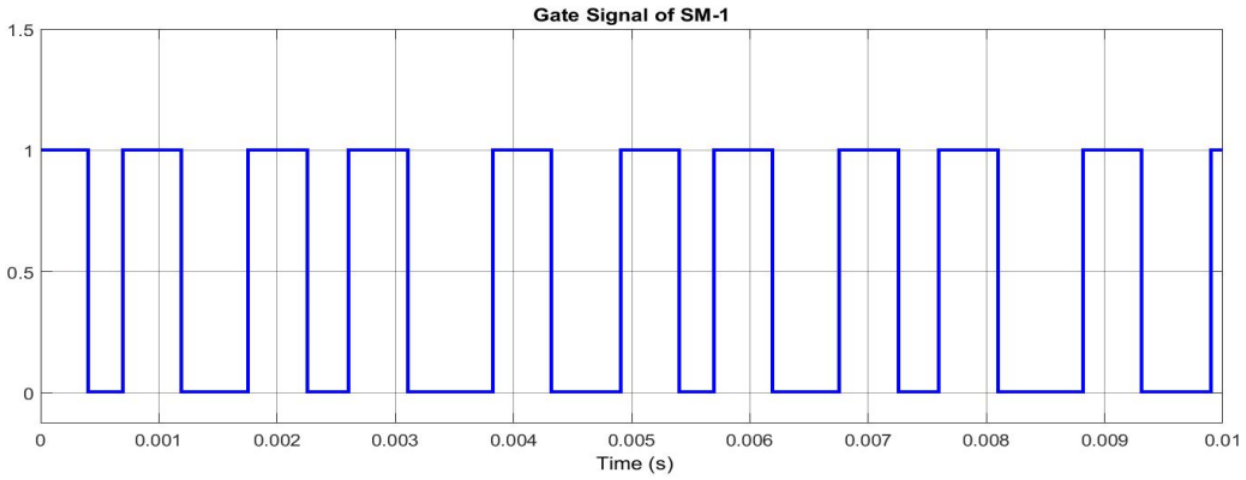

Fig. 6.13: The gate signal of the first SM of the upper arm

The firing angles values listed in Table 4.1 are used in the simulations to balance the SM capacitor voltages. The procedure explained in section 4.3 is used in the simulations. The pulse pattern used to switch the first SM of the upper arm is expressed by the vector:

$$\beta_k = [\gamma_1 \quad \gamma_4 \quad \gamma_3 \quad \gamma_5 \quad \gamma_2] \tag{6.1}$$

This gate signal is shown in Fig. 6.13 which shows that the gate signal is periodic to five fundamental cycles. The line-to-line voltage and line current of this terminal are shown Fig. 6.14. The dc-link voltage applied to MMC #2 terminal is 44 kV. The line-to-line voltage of a three-phase inverter terminal is calculated by [5]:

$$v_{LL} = 0.612\, m_a V_{dc} \tag{6.2}$$

where v_{LL}, m_a, and V_{dc} are the line-to-line voltage, modulation index and dc-link voltage, respectively. A peak value of 38 kV is observed in the line-to-line voltage waveform for unity modulation index which follows (6.2). The peak line current is 200 A which is close to the theoretical value.

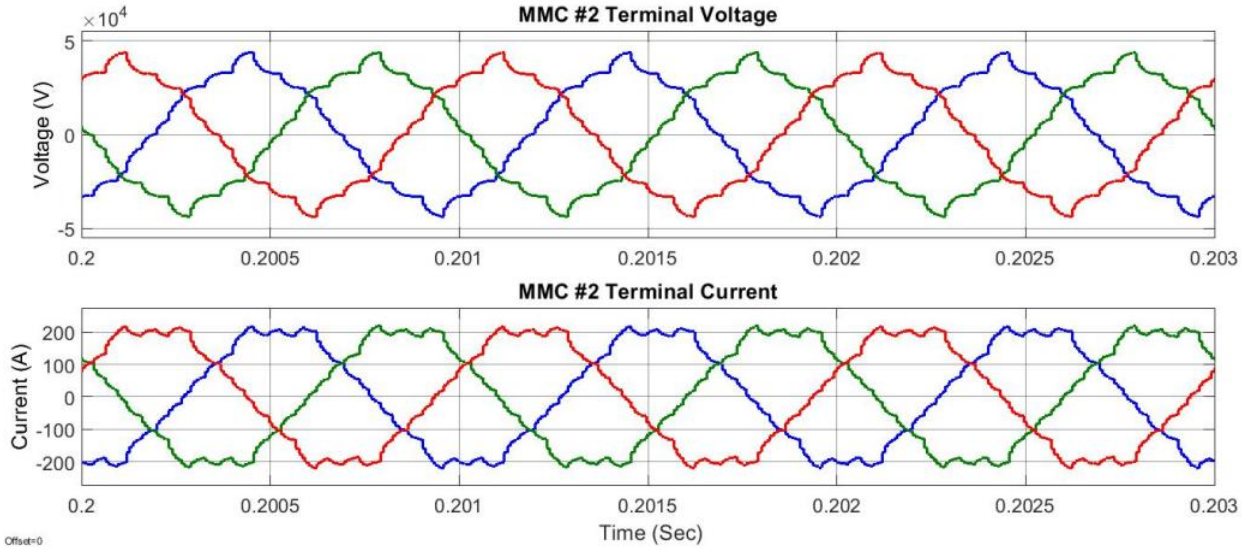

Fig. 6.14: MMC #2 terminal voltage and current waveforms

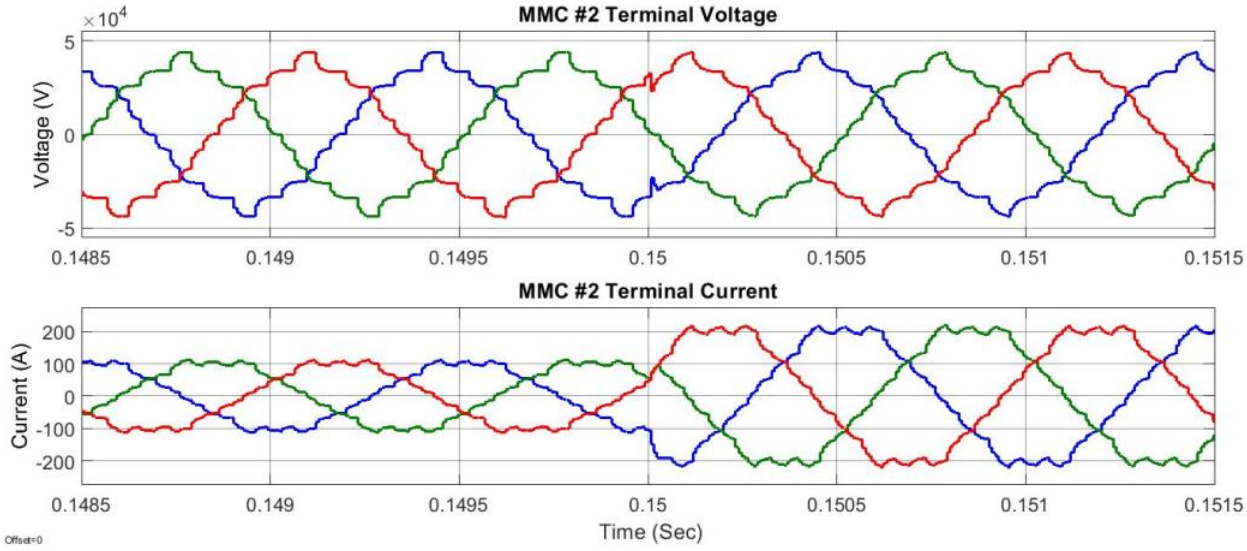

Fig. 6.15: MMC #2 terminal voltage and current waveforms with a change in load

An identical approach is used to determine the behavior of this terminal under disturbances. The load is again doubled at 0.15s and the response of the voltage and current waveforms are shown in Fig. 6.15. The system became stable within a cycle. There is no overshoot observed in the voltage and the current.

The simulation set-up of MMC #3 terminal is shown in Fig. 6.16 which is identical to MMC #1 terminal. The phase-to-neutral voltage and line current waveforms having the peak values of 11.25 kV and 357 A, respectively, are shown in Fig. 6.17. The values are similar to the theoretical values.

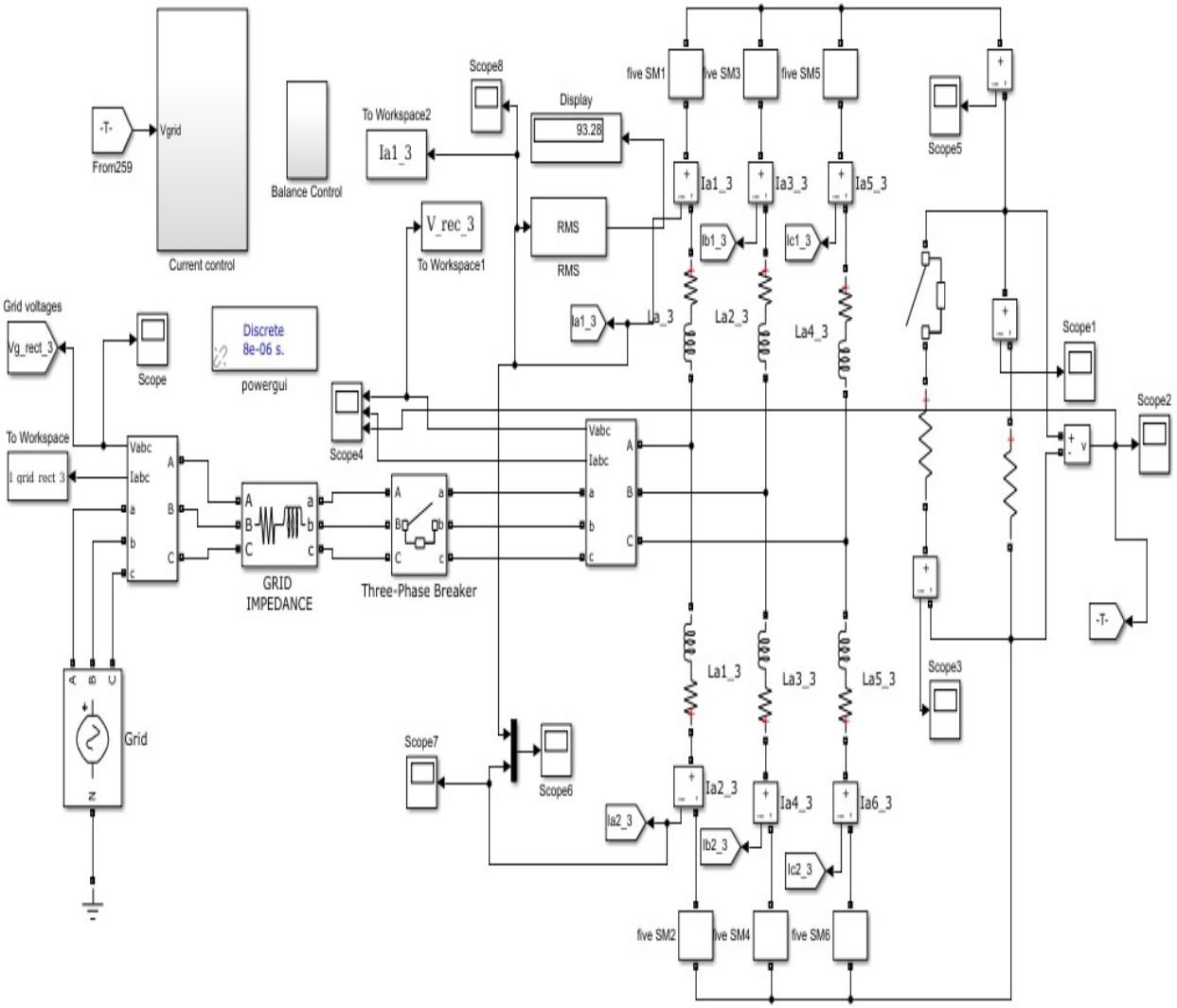

Fig. 6.16: The simulation set-up of MMC #3 terminal

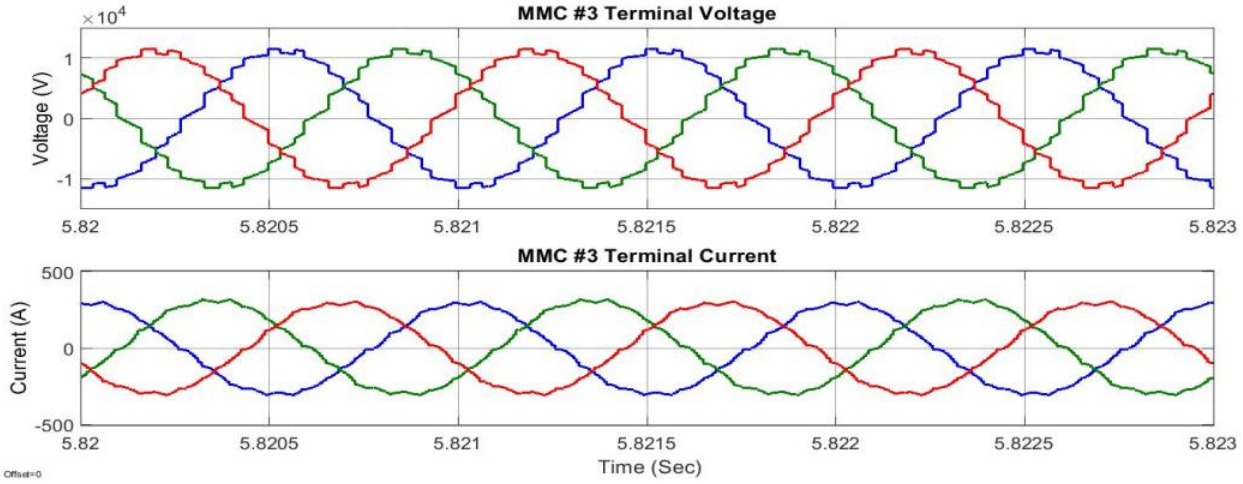

Fig. 6.17: MMC #3 terminal voltage and current waveforms

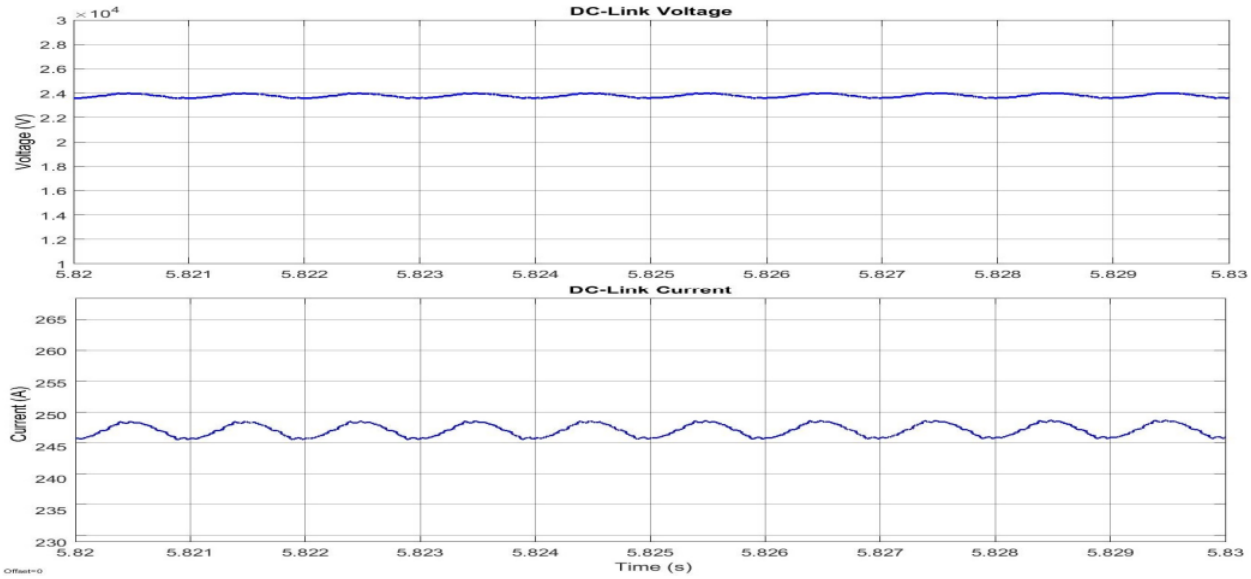

Fig. 6.18: SHE-based dc-link voltage and current waveforms

The dc-link voltage and current waveforms having the average values of 24 kV and 247 A, respectively, are shown in Fig. 6.18. The ripple in dc-link voltage is less than 1%, and significantly less than that for the PS-PWM algorithm because the proposed SHE algorithm only produces the pre-defined voltage whereas the PS-PWM algorithm continuously forces the system to follow the controllers command to generate the desire voltage.

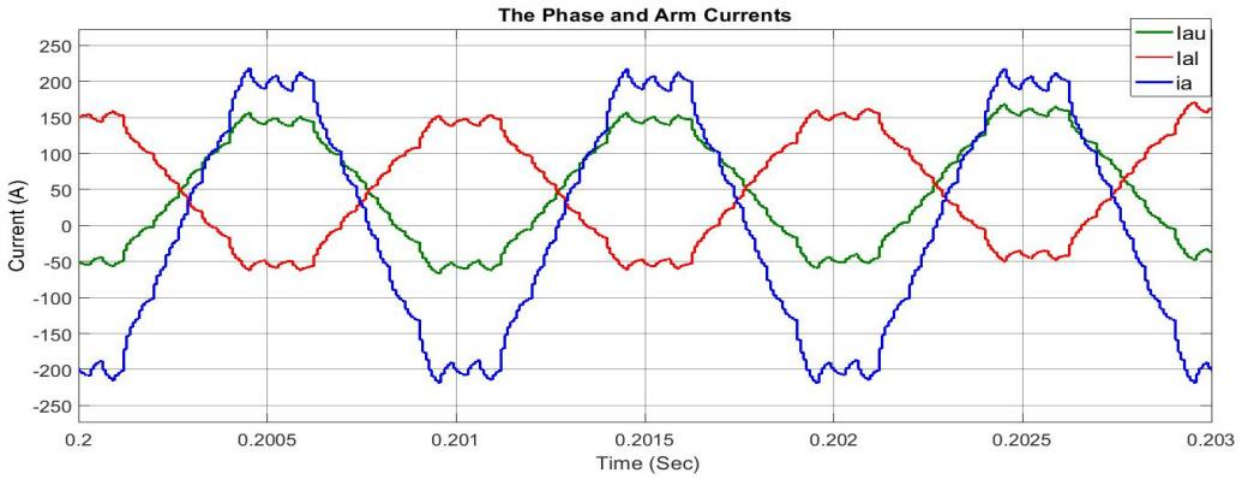

Fig. 6.19: SHE-based phase and arm current waveforms

The simulation results of the SHE-based algorithm are in accordance with those in [6]- [7]. The phase, upper, and lower arm current waveforms are shown in Fig. 6.19. The peak value of the phase current is 200 A which is close to the theoretical value. The upper (green) and lower (red) arm currents are out of phase as expected. Subtracting of the lower arm current from the upper arm current produces the phase current which verifies the theoretical claims. The balancing technique used in the switching algorithm is verified by examining SM capacitor voltage which is shown in Fig. 6.20. An average value of 8.85 kV is observed in the SM capacitor voltage which is very close to the theoretical value of 8.8 kV. The period of the SM capacitor voltage is 5 ms which is five times of the fundamental period because there are five different pulses in five consecutive fundamental cycles used to balance the SM capacitor voltage. A ±5.1% ripple is observed in the SM capacitor voltage which is well within the desired level of 10%. The angles were calculated to eliminate the 5^{th} order harmonic in the output voltage. The FFT analysis of output voltage is shown in Fig. 6.21, showing the elimination of the 5^{th} order harmonic. However, the 7^{th}, 11^{th}, 13^{th} and higher order harmonics were present and a THD of 6.02% is observed in the output voltage.

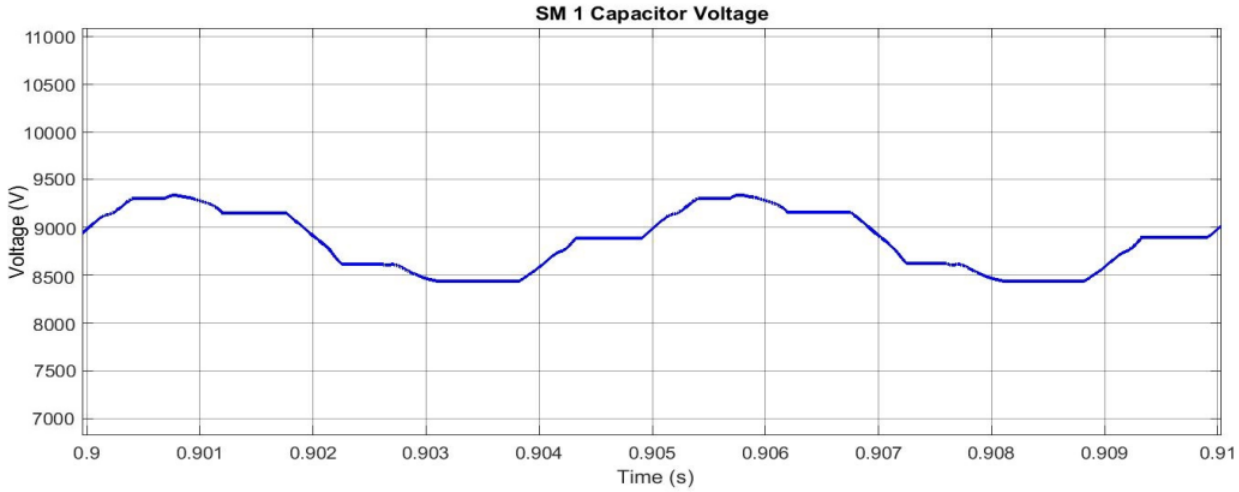

Fig. 6.20: SHE-based SM capacitor voltage

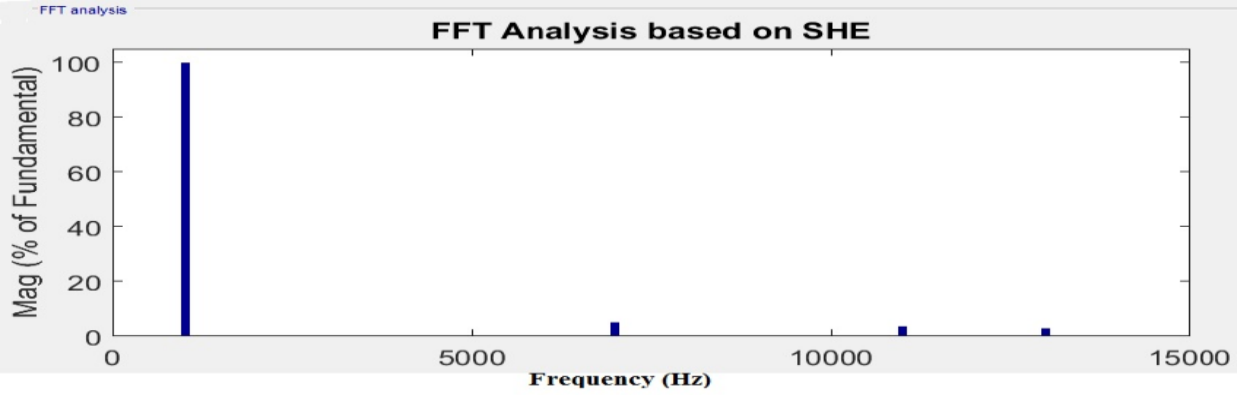

Fig. 6.21: FFT analysis of output voltage

6.4 MPS Operation

A three-phase transformer is connected in between MMC #2 and MMC #3 terminals whose parameters are given in the Table 6.3. MMC #1 and MMC #4 terminal are connected to MMC #2 and MMC #3 terminals, respectively, to form the MPS system which is shown in Fig. 6.22. The gains of the dc-link voltage and current controllers are increased four times than the earlier values to get a stable system, because these controllers were designed to perform separately. The new values of the gains are given in the Table 6.4. When the four MMC terminals connected, the

performance of one terminal depends on the other terminals. The bandwidth of the MPS system is different than the individual MMC terminals; thus, the modification was required to get a stable system.

Table 6.3: Three-phase transformer parameters

	Winding 1 Parameter		**Winding 2 Parameter**		**Magnetization Component**	
Parameter	R1	L1	R2	L2	Rm	Lm
Value	0.002 (pu)	0.08 (pu)	0.002 (pu)	0.08 (pu)	500 (pu)	500 (pu)

Table 6.4: Gains of the different controllers for the MPS operation

	DC-Voltage Controller		**Current Controller**		**SM Capacitor Voltage Controllers**				
Parameter	k_{p_v}	k_{i_v}	k_{p_i}	k_{i_i}	k_1	k_2	k_3	k_4	k_5
Value	25	2111	193	1.77×10^5	0.3	3	1	0.5	0.5

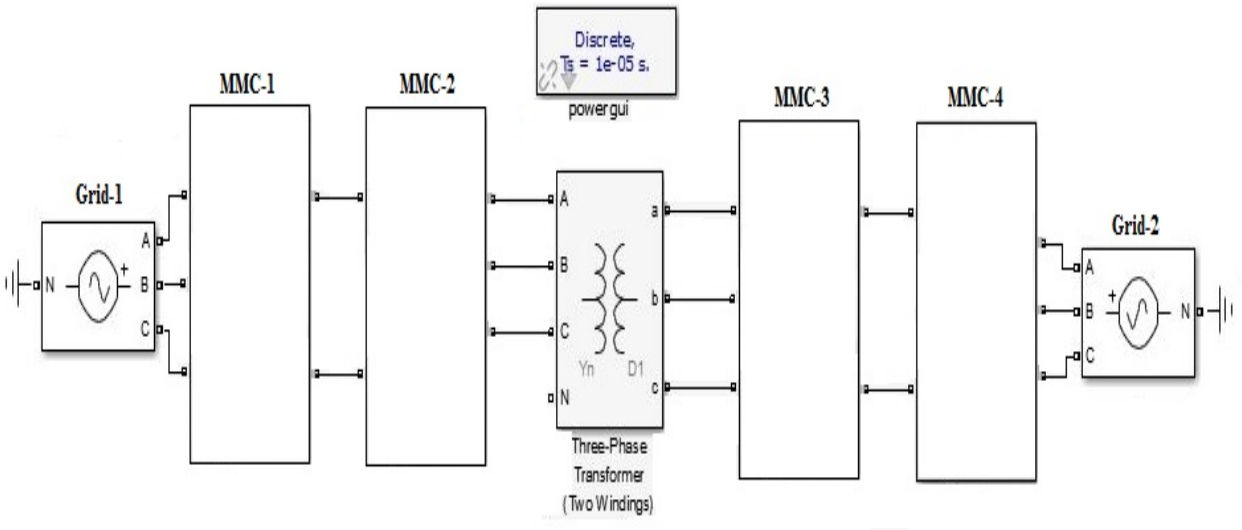

Fig. 6.22: The MPS simulation set-up

The voltage and current waveforms of MMC #1 terminal are shown in Fig. 6.23. The peak values of the line-to-line voltage and current are 35.36 kV and 197 A, similar to the theoretical values. However, these waveforms exhibit large ripples of $\pm 12.7\%$ as the system is no longer operating with ideal voltage sources and controller performances deteriorate in the MPS system.

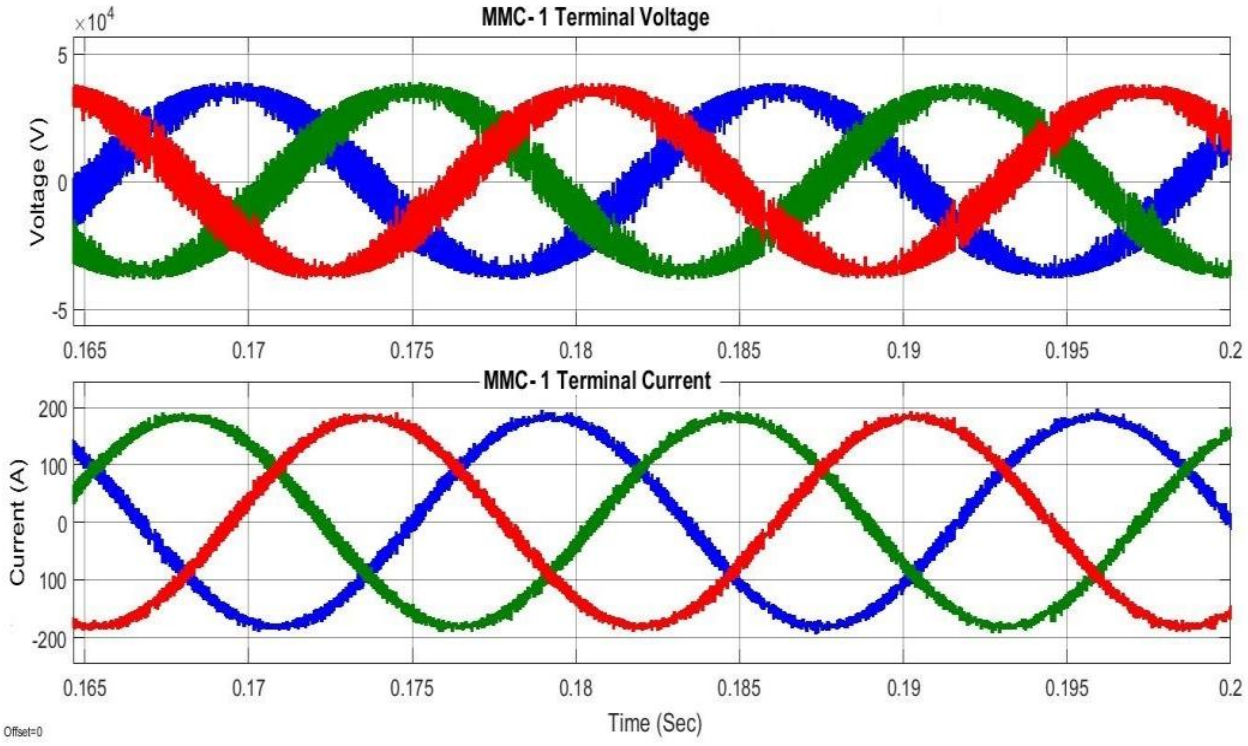

Fig. 6.23: MMC #1 terminal voltage and current waveforms in the MPS system

The dc-link voltages are presented in Fig. 6.24. The MMC #4 line-to-line voltage and current waveforms are shown in Fig. 6.25. The peak values of the line-to-line voltage and current are 19.52 kV and 355 A, close to the theoretical values. However, a large ripple of ±14.7% is present in the dc-link voltage which contributes in the ripple of the output voltage.

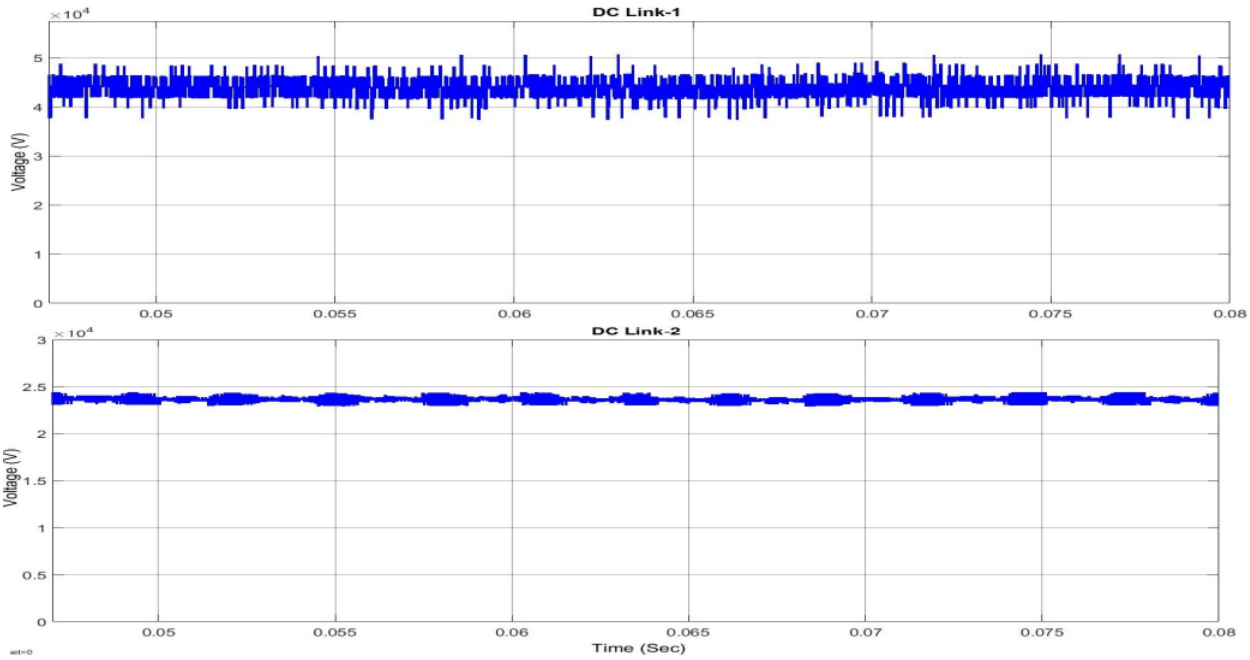

Fig. 6.24: DC- link voltages of the MPS system

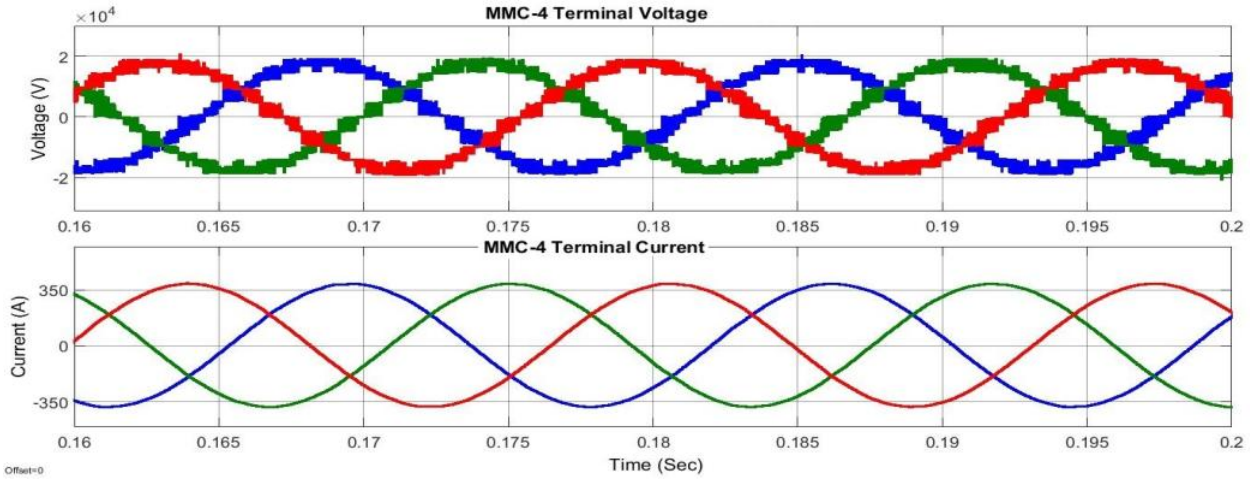

Fig. 6.25: MMC #4 terminal voltage and current waveforms in the MPS system

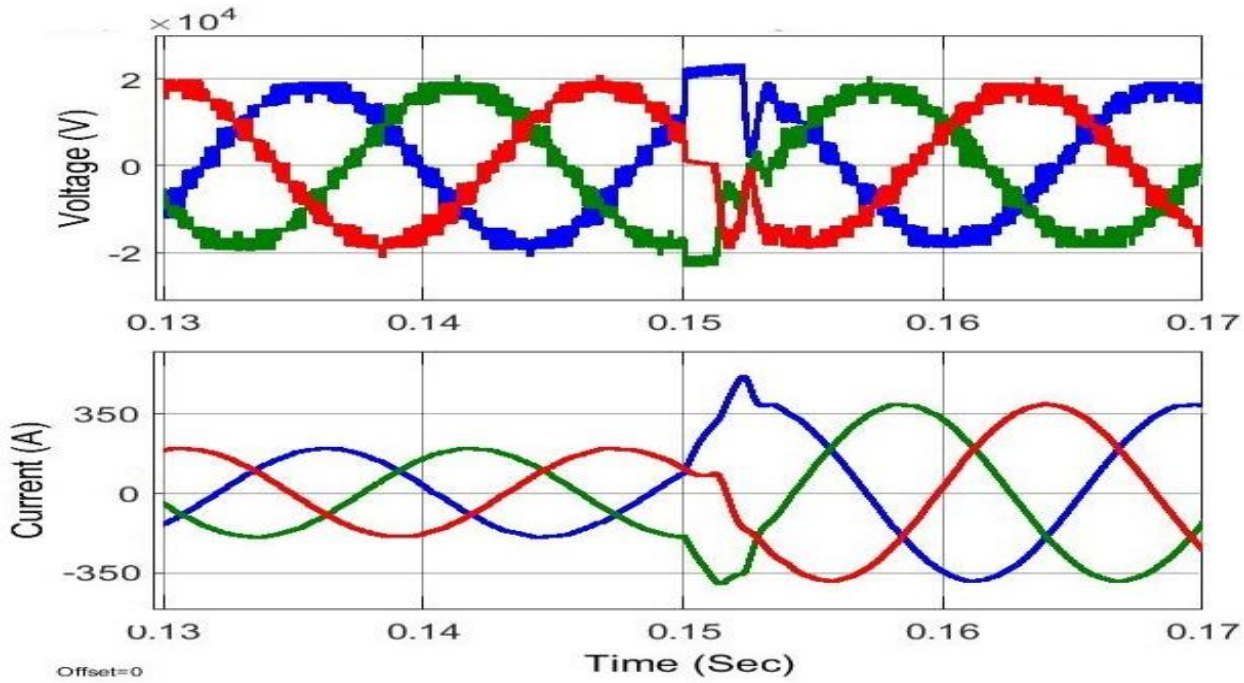

Fig. 6.26: MMC #4 terminal behavior with a change in the power demand

A power demand command is changed at 0.15 s in MMC #4 terminal to observe the change in behavior; the results are shown in Fig. 6.26. The peak values of the voltage and current waveforms are 22 kV and 510 A, respectively due to this disturbance. The overshoot values are well within the safe operating area of the designed MPS system. The system became stable within a cycle. The partial results of the MPS system are published in [8].

6.5 Conclusions

The simulation results verified the theoretical claims indicated in earlier chapters. However, the performance of the system could be improved for example, the ripples in the dc-link and line-to-line voltages. The next chapter will provide the conclusions and recommendations for future work.

6.6 References

[1] M. Hagiwara and H. Akagi, “Control and experiment of pulse width modulated modular multilevel converters,” in *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1737–1746, 2009.

[2] M. Hagiwara, R. Maeda, and H. Akagi, “Control and analysis of the modular multilevel cascade converter based on double-star chopper-cells (MMCC-DSCC),” in *IEEE Transactions on Power Electronics,* vol. 26, no. 6, pp. 1649, 1658, 2011.

[3] D. A. Guzman, High voltage direct current energy transmission using modular multilevel converters, M.S. Thesis, Department of Electrical Engineering, University of Arkansas, Fayetteville, USA, 2013.

[4] A. Antonopoulos, L. Angquist, H-P. Nee, "On dynamics and voltage control of the Modular Multilevel Converter," in *13th European Conference on Power Electronics and Applications,* pp. 1-10, 2009.

[5] N. Mohan, T. M. Undeland, and W. P. Robbins, Power Electronics: Converters, Applications, and Design, Third Edition. New York: John Wiley & Sons Inc, 2003.

[6] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, “A new modulation method for the modular multilevel converter allowing fundamental switching frequency,” *in IEEE Transactions on Power Electronics,* vol. 27, no. 8, pp. 3482–3494, 2012.

[7] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, and H. P. Nee. "Circulating current control in modular multilevel converters with fundamental switching frequency," in *Power Electronics and Motion Control Conference (IPEMC), IEEE 7th International*, vol. 1, pp. 249-256, 2012.

[8] C. Deng, T. Islam, and J. C. Balda. "Design of medium-frequency transformers with silicon steel for mobile power substations," *in 8th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG),* pp. 1-7, 2017.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS FOR THE FUTURE WORK

7.1 Conclusions

The main objective of this research was to develop a compact and light-weight MPS system which can connect two medium-voltage feeders. The available technologies were analyzed and the MMC-based solution was proposed. The selection of switching algorithms and devices were analyzed and a suitable solution was proposed. Finally, the simulation model was built and the theoretical claims were verified. The achievement of this research can be summarized as follows:

- A brief description of the traditional MPS and its applications was provided. A power electronics based solution was proposed. Available technologies were discussed based on different references. Finally, the MMC topology was selected for its advantages.
- Fundamentals of MMC were analyzed. The half and full-bridge structures of the SM were discussed and the HB-SM was selected because of its lower component count and higher efficiency. The selection procedure for the SM capacitor and arm inductor were derived based on simple mathematical models. Design examples were provided on the selection procedure for these passive components.
- The availability of the switching devices in the present market was analyzed. The IGBT was selected as the switching device due to its advantages over the other switching devices in terms of current ratings. Different types of IGBT losses were calculated using the datasheet values. A thermal management technology was proposed using heat pipes. The maximum achievable switching-frequencies were calculated for selected switching

devices. The switching-frequency was set to 1 kHz. IGBT module CM750HG-130R was selected for MMC #1 and MMC #2 terminals and IGBT module 5SNA 0800N330100 was selected for MMC #3 and MMC #4 terminals. The characteristics of these switching devices were analyzed and the required numbers of components were calculated.

- Different modulation strategies based on the switching-frequency were discussed. The PS-PWM topology was selected for the MMC #1 and MMC #4 terminals. The fundamentals of the PS-PWM algorithms were analyzed. The operating-frequency of the MMC #2, MMC #3 terminals, and transformer was set to 1 kHz. The SHE algorithm was selected for the modulation of these two terminals. The fundamentals of the SHE algorithm was discussed with mathematical derivations and examples. A specific pulse pattern was described to balance the SM capacitor voltages based on the energy transfer of the SM capacitors.
- The active and reactive power controllers were analyzed using the Park's transformation. The dc-link voltage controller was analyzed with the help of step-responses and Bode diagrams. Matlab^{TM} code was used to evaluate the proportional and integral gains of the controller. A similar procedure was used for the current controllers. A two-level model was built in Matlab/Simulink^{TM} to validate the gains of the voltage and current controllers. The average voltage controller of the SM capacitor was described and the gains were calculated. The theory of the instantaneous voltage controller for the SM capacitor was discussed. The arm voltage balancing technique was used to overcome the limitations in rectification operation. These three controllers mentioned above were combinedly to stabilize the MMC terminals and reduce the circulating current. The switching signal generation for both the PS-PWM and SHE algorithms were discussed.

- Different simulation models were built in Matlab/Simulink^{TM} for different MMC terminals. The four MMC terminals were designed separately based on the specifications of the MPS system. Their performances were evaluated and verified with the theoretical behaviors. The simulation results were explained with graphical representations. Finally, the four MMC terminals were combined with a medium-frequency transformer. The combined behaviors of the proposed MPS were presented and verified.

7.2 Recommendations for the Future Work

There are few suggestions to improve this research that includes:

- A further analysis of the SM capacitor voltage balancing with the modern proposed techniques. The evaluation of these techniques can be used to compare with the proposed technique in this research.
- HB-SM structure is unable to block the dc-side faults; thus, an FB-SM structure performance can be evaluated.
- In this research, the hard-switching technique was used which reduced the overall efficiency of the MPS system. Therefore, the possibilities of using a soft-switching technique such as zero-voltage switching (ZVS) or zero-current switching (ZCS) can be evaluated to improve the efficiency.
- The dc-link voltage contains significant ripple when modulated by the PS-PWM algorithm. This behavior is observed when the number of levels is low. Therefore, a modified simulation model can be built using a large number of levels to evaluate the ripple in the dc-link voltage.
- The performance of the MPS system can be enhanced by reducing the ripples in the line-to-line voltages.

- The circulating current contains large 2nd order harmonics. A controller can be developed to mitigate this harmonic.
- The switching device used in this research uses the silicon-based technology. New silicon-carbide-based switching devices are available in the market. The performance of the new devices can be analyzed and compared with the devices used in this research. Furthermore, the prospect of using IGCT instead of IGBT can be evaluated for future applications.
- A small prototype can be built to evaluate the simulation results.
- A detail calculation can be conducted to evaluate the weight and volume of the system.
- A new simulation model can be developed to evaluate the discrete nature of the controllers designed in the research.