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Five-Level Flying Capacitor Converter used as a Static Compensator for Current Unbalances in Three-Phase Distribution Systems

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Five-Level Flying Capacitor Converter used as a Static Compensator for Current Unbalances in Three-Phase Distribution Systems

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by

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ABSTRACT

This thesis presents and evaluates a solution for unbalanced current loading in three-phase distribution systems. The proposed solution uses the flying capacitor multilevel converter as its main topology for an application known as Unbalanced Current Static Compensator. The fundamental theory, controller design and prototype construction will be presented along with the experimental results. The Unbalanced Current Static Compensator main objective is the balancing of the up-stream currents from the installation point to eliminate the negative- and zero-sequence currents originated by unbalanced single-phase loads.

Three separate single-phase flying capacitor converters are controlled independently using a d-q rotating reference frame algorithm to allow easier compensation of reactive power. Simulations of the system were developed in MATLAB/SIMULINK™ in order to validate the design parameters; then, testing of the UCSC prototype was performed to confirm the control algorithm functionality. Finally, experimental result are presented and analyzed.

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DEDICATION

To my beloved parents, Rita & Ramiro, my brothers Rodolfo & Raul and my wonderful girlfriend Valedis. Thanks for being my source of inspiration all the way.

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CHAPTER 1

INTRODUCTION

1.1 Motivations for this Research Work

Nowadays society has developed a high dependence on energy. Renewable energy sources (RES) have presented a rapid growth in the last few years [1]. With the aging electrical infrastructure and the global demand rising, more research has been devoted at improving the life, operational reliability, security and efficiency of the existing grid to meet the expected growth in the number of customers and centralized load centers [1]. Simultaneously, environmental concerns encourage a reduced and more sustainable conversion, distribution and usage of energy that have brought in the construction of energy-efficient buildings [2], development of electric vehicles and the installation of RES [3,4]. The major benefit of using RES is their capability of emitting no or less CO2 than conventional power plants. These include photovoltaic systems (PV), wind turbines, biomass, biogas, geothermal generation, and hydro power plants. In most cases, wind and solar farms are not available on-demand but only at specific times and, because of authorities' subsidies and renewable energy mandates, large amounts of single-phase distributed generation have been installed at medium- and low-voltage levels [5].

This unrestricted energy trading is one of the main causes that creates high stresses on distribution networks. Likewise, fluctuating generation from distributed generation (DG) provokes less predictable and controllable power flows in the network, thus demanding more efforts to ensure the desired system power quality. For instance, the fluctuations could be related to oscillations from solar and wind generations that, as mentioned before, are not available all the time since they depend on weather conditions [6]. In the past, the power flow was normally directed towards customer loads connected to the network, which allowed for an easier correction

of voltage deviations and circulation of current in the neutral conductor of four-wire systems. With the continuous development of new technologies, the anticipation of the load profile has become relatively a process involving a randomly determined sequence of observations, each of which is analyzed using stochastic algorithms [7]. In addition, a limited number of signals is measured and not all of them are recorded, which eventually give more uncertainty to the network operator, as determining accurately the amount of consumed and produced power, and the locations has not become so trivial. It is fundamental to balance the supply and demand of active and reactive powers because any unbalance behavior may affect the system frequency or voltage, and in the worst scenario, the system may collapse resulting in a blackout.

This lack of accuracy created the concept of voltage regulation, where voltage and current at the medium-voltage (MV) transformer terminals are measured and a transformer tap changer is employed to guarantee a constant voltage at a desired point in the distribution line. Usually, the voltage range varies $\pm$ 5% of the rated voltage of the network [8, 9]. Now, excessive voltage increment arises with the inclusion of large amount of DG units in the distribution grid, and the previous solution becomes obsolete due to the possibility of deteriorating the voltage profiles instead of improving them.

To handle these challenges in a cost-effective way, innovative solutions of operating the networks are of great interest. International research focuses on increasing the flexibility of electricity consumption using storage to smooth out power fluctuations [10], and on controlling the power flows using new hardware and software technologies [11, 12]. Technological advances in power electronics have become a viable solution because it now allows more flexible and dynamic control of compensation devices for use in improving the distribution voltage levels, enhancing line power factor, and reducing overall distribution losses. Devices that grant all these

benefits have been categorized as distribution flexible alternating current transmission systems or D-FACTS [13].

In the past, electric utilities used static compensators like shunt capacitor banks and synchronous condensers. However, their slow reaction times to network faults, the low power quality in the case of the capacitor banks have put them aside. A variety of D-FACTS has now been developed [13-15]:

a. Distribution static synchronous compensator (D-STATCOM)
b. Dynamic voltage restorer (DVR)
c. Unified power quality conditioner (UPQC)
d. Unbalance current static compensator (UCSC)

The D-STATCOM is a device similar to the static VAR compensator but using IGBTs and added stability control capability. In summary, it consists in a self-commutated converter with a DC voltage source, where the output must be in phase with the AC system. It is mostly used for voltage stabilization, flicker suppression, power factor correction and harmonic control. Depending on the difference of the voltage magnitude between the D-STATCOM and the grid, the system could be considered as lagging or leading [16, 17]. The DVR is a modern device used in distribution systems to mitigate voltage sags/swells and provide harmonics reduction [18]. The DVR operation is by injecting ac voltages in between the supply feeder and the load at the point of common coupling (PCC). By adjustments in the voltage magnitude and phase shift, improvements of the voltage quality are obtained [18]. Another application to improve power quality is the UPQC; this type of D-FACTS consists of double converters connected by a dc capacitor with each other. It offers high controllability and great protection against system faults

at the utility side due to its capability of dynamic voltage restoration and fault current limitation [19].

1.2 Previous Research at the UofA Department of Electrical Engineering

The D-FACTS mentioned above do not take into consideration the current unbalances in three-phase systems. DG interconnection to the grid is generally present as single-phase loads, thus creating a considerable difference between phases of distribution feeders. In consequence, the system operates with negative- and zero-sequence components due to the unbalance behavior. Negative-sequence current in the feeder leads to the generation of a magneto motive force (MMF), which is harmful to synchronous generators due to the imminent interference with the positive sequence MMF [20]. Zero-sequence currents might cause overheat when produced in wye-connected ungrounded transformers [21]. Furthermore, the unbalance will provoke overcurrent in the neutral wire that is never desired, as it is dangerous, and occasionally makes the conductor to be oversized [22].

Different existing solutions to realize a low-voltage unbalance current static compensator (UCSC) where reviewed in [23] and [24]; nonetheless, the approach of these solutions is limited due to the requirement of having the active component of the load balanced. A new UCSC project was then proposed by both to solve the unbalanced load problem. At last, after analyzing various topologies, three single-phase full-bridge converters were chosen by virtue of its simpler control algorithm, independent control for each phase and full utilization of the DC link voltage. The proposed solution is shown in Figure 1-1. The major drawbacks of this topology are the great number of harmonic contents beside the fundamental frequency and the high dv/dt switching stress component originated by two-level conventional converters, both reducing power quality and generating power losses, as well as the inclusion of three single-phase distribution transformers to

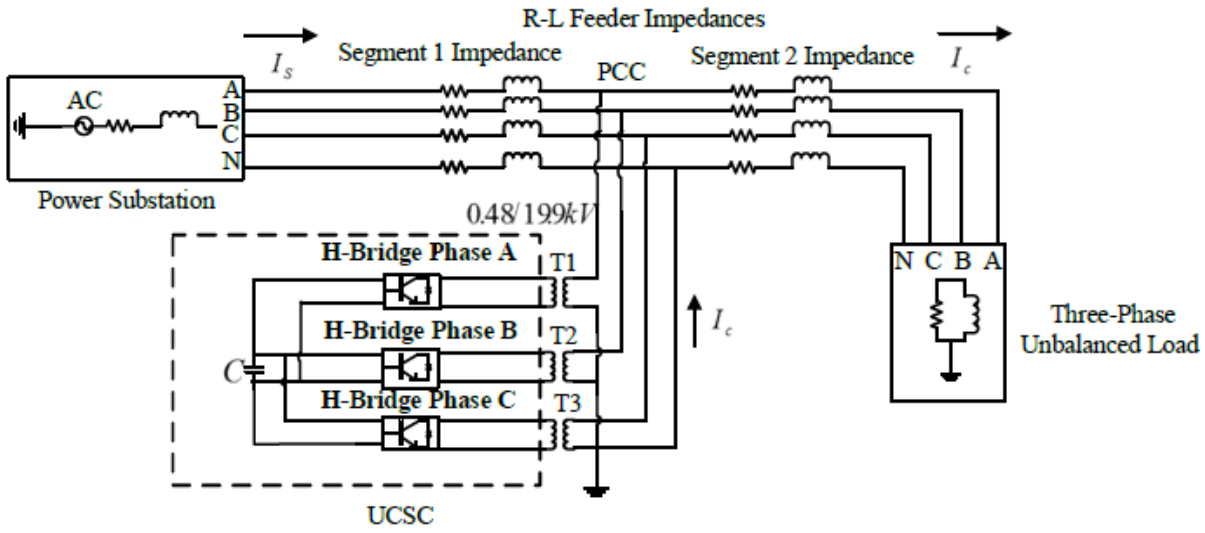

Figure 1-1. UCSC solution with three single-phase full-bridge inverters [23]

boost the voltage to the required MV distribution substation. Finally, for high-power applications where size, efficiency and cost are significant; new topologies had to be explored, like the multilevel converters that will be presented below.

1.3 Multilevel Converters

Multilevel converters were initially developed for high-voltage (HV) and high-power applications, with the clear advantage over conventional topologies that they do not need the implementation of a distribution transformer to step-up the voltage [25]. Consequently, a considerable reduction of size and cost of the prototype are guaranteed. Moreover, many configurations have been proposed aiming to deal with highly desirable characteristics such as low blocking voltage by switching devices and reduced waveform distortion [26]. The limit in the number of levels is mainly determined by the complexity of the controller and the increased number of components (capacitors, diodes, switches) that influence directly the cost of the converter. At higher levels, the output waveform of a multilevel converter becomes smoother,

getting closer to a sine wave; thus, significant THD reduction is achieved. The most widely used multilevel configurations at the present time are:

a. Neutral-point-clamped converter (NPC)
b. Cascade H-bridge converter (CHBC)
c. Modular multilevel converter (MMC)
d. Flying capacitor converter (FCC)

1.3.1 Neutral-point-clamped converter

The NPC configuration is one of the most common topologies for low-, medium- and high-voltage applications, especially in motor drive and photovoltaic energy systems because of advantages like:

a. THD is reduced for higher number of levels eliminating the need of filters.
b. The ability to control reactive power flows.
c. Reduction of dv/dt when compared with two-level conventional topologies.

An n-level NPC typically consists of series-connected dc-bus capacitors and clamping diodes to produce an output phase waveform of n levels. DC-bus common point G is connected to a neutral point with the clamping diodes. Switches S_{1a} & S_{1b} and S_{2a} & S_{2b} work as complementary pairs to each other. For a three-level NPC, each capacitor will sustain half of the dc-bus voltage and every switching device will only handle one capacitor voltage level. This will be possible due to the arrangement of the clamping diodes. The schematic of the three-level NPC is shown in Figure 1-2.

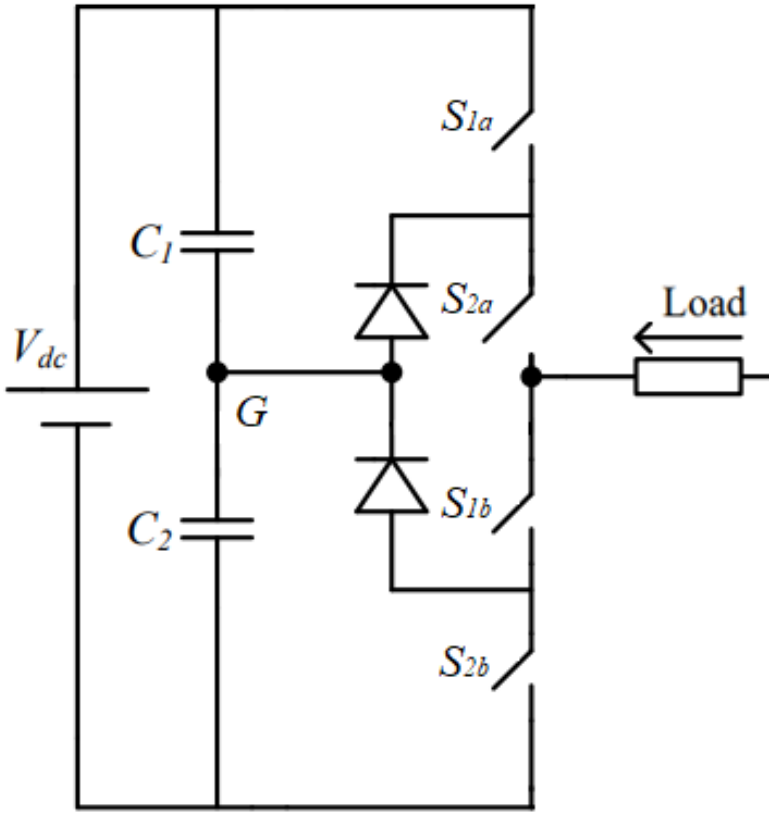

Figure 1-2. Three-level neutral-point-clamped converter

The most unfavorable disadvantage is the capacitor voltage-unbalance problem. If a simple modulation strategy is used, there is no guarantee that the capacitor voltages will converge to the average value, creating asymmetry at the output voltage of the converter. Feedback controllers or specific PWM approaches must be used to monitor the capacitor voltage values bringing a more complex control algorithm when using higher levels. Another challenge appears when dealing with the blocking voltage of each clamping diode, the voltage will suddenly change depending on its position in the circuit. For high-voltage applications, those variations in the blocking voltage introduce operational limits to the converter. By adding more clamping diodes in series, this complication could be solved but a more expensive converter will have to be developed [27].

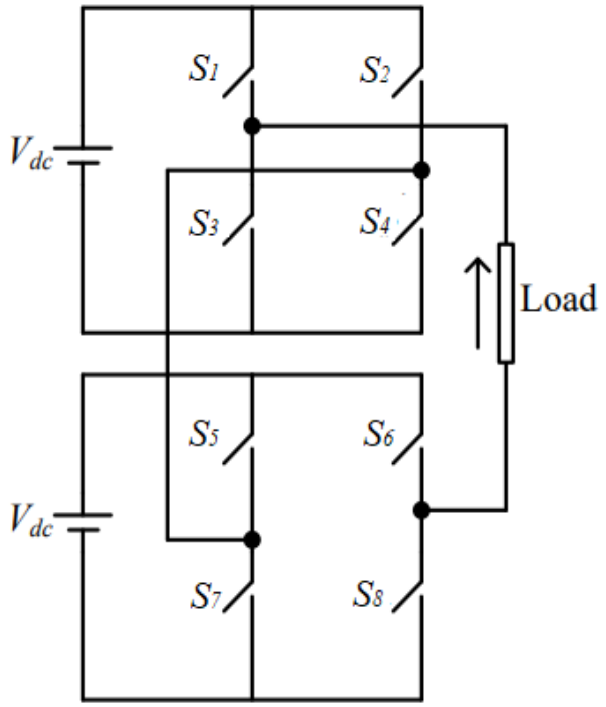

Figure 1-3. Five-level cascaded H-bridge converter

1.3.2 Cascade H-bridge converter

The level in a CHBC is defined by $n = 2s + l$, where n is the output phase voltage and s is the number of dc sources. For instance, the five-level CHBC, as seen in Figure 1-3 will include two dc sources and two single-phase H-bridges. The DC sources must be isolated and each one will be linked with a single-phase H-bridge. On the AC side, a series connection of the H-bridge inverters is desired to generate the different voltage levels in the output. Interesting characteristics extracted from this topology are the following:

a. Low electromagnetic interference (EMI) and reduced total harmonic distortion (THD) when compared with conventional two-level inverters.
b. No neutral point clamping circuits when compared with the NPC or voltage balancing capacitors.

c. Lower number of components to achieve the same number of voltage levels when compared with other multilevel converters.

The need of adding separated and floating dc sources with each leg bring limited number of possible applications. Separated DC sources are essential for the topology because using a single DC sources lead to short-circuit in some switching configurations [28].

1.3.3 Modular multilevel converter

This type of converter is based on a series connection of half-bridge or full-bridges sub-modules [29]. Every sub-module has a capacitor connected with a rated voltage of Vdc/n, where n refers to the number of sub-modules. Figure 1-4 illustrates a three-level MMC. The levels in the output voltage of a MMC are defined as $n + 1$. The main advantages of this topology are:

a. Low THD and low dv/dt on devices and lower losses when compared to conventional topologies.
b. Its modular structure with redundant identical modules makes feasible an easier substitution of failed modules.
c. No dc-bus voltage limitation.

The balancing of the capacitor voltages becomes an issue for this topology because of the need for monitoring all capacitor voltages. In addition, a circulating current having a double fundamental frequency component increases losses and should be addressed carefully in the design [29].

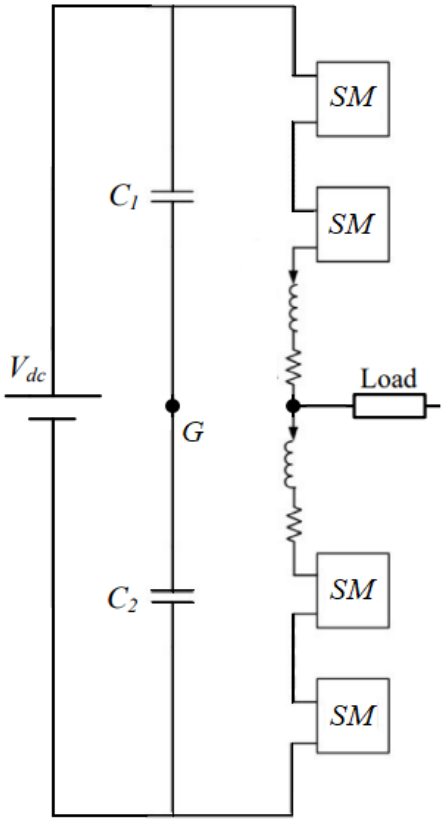

Figure 1-4. Modular multilevel converter topology

1.4 Proposed Solution Using the Flying Capacitor Converter

The topology selected for the new version of the UCSC is the FCC based on the following characteristics:

a. The arrangement of the switches with the capacitors allow many redundant states for producing the specific output voltage, which leads to a simpler controller and better efficiency.
b. Less number of devices is required when compared to NPC and MMC.
c. Active and reactive power flow are easily controlled, making this topology the best candidate for high voltage ac or dc transmission.

d. Full utilization of the DC link is available, in contrast with two-level conventional topologies.
e. The module capacitance is inversely proportional to the switching frequency.

The final goal of the research group is to build a three-phase UCSC that has three eleven-level FCCs (one per phase) rated for 13.8 kV and 1 MVA. All the switching devices will be HV Silicon Carbide MOSFETs. The system will be able to compensate for negative- and zero-sequence currents generated by unbalanced loads from DG and provide limited reactive power compensation. A line-to-neutral LCL filter is going to be connected at the output of each FCC. The application is planned to be installed just after the MV distribution substations, as a measure to compensate for the maximum load.

1.5 Objectives of the Thesis

The main objective of this research work is developing a prototype of the FCC-UCSC to validate the control algorithms and to determine the control implementation procedures in a digital signal processor (DSP) F28379D of Texas Instruments. The selected setup is a five-level with the intention of testing a simple system that can be expanded for higher levels. Power MOSFETS with the following characteristics were selected as the power semiconductor of choice: 10 A, 200 V and a switching frequency of 10 kHz. To authenticate the performance of the constructed prototype some steps were followed:

a) The theoretical background behind the operation of the FCC was first understood.
b) Simulations were developed to analyze potential upgrades.
c) The prototype was built and tested, and the experimental results were analyzed, compared and discussed.

1.6 Organization of the Thesis

The thesis is organized as follows:

a. The fundamentals of the FCC topology, the basic structure and operation principles are explained in Chapter 2. Analysis of the various modulation techniques to achieve capacitors self-voltage balancing are also evaluated
b. The single–phase d-q reference frame control algorithm used for the application is explained in Chapter 3
c. Simulations results of the UCSC are presented in Chapter 4
d. Design and construction of the prototype and the F28379D DSP configuration and setup are described in Chapter 5
e. The experimental results are analyzed and evaluated in Chapter 6
f. Finally, the conclusions and recommendations for future work are provided in Chapter 7.

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CHAPTER 2

FUNDAMENTALS OF FLYING CAPACITOR CONVERTERS

2.1 Introduction

The FCC topology originally proposed in [1] is relatively recent compared to the NPC or the cascaded H-bridge topologies. The biggest difference when compared to the NPC is the replacement of the diodes with flying capacitors, or floating capacitors, to clamp the voltages of the power switches nodes. When compared with other topologies, the FCC offer the following advantages [1-4]:

a) Simpler control design for the power switches.
b) Reduction in the capacitance when operating at high frequencies.
c) Enhanced power converting quality (Less dv/dt, THD and EMI) at an increased number of voltage levels; however, improvement is not proportional with the level augmentation.
d) Output filters size is significant reduced.
e) DC link and output voltages can be higher than the individual power switch blocking capability; though, the differences in the flying capacitor voltage need to be kept between certain voltage ranges as a measure to maintain the self-balancing property.

The possibility of redundancy in the switching states by using flying capacitors is a significant peculiarity [5, 6]. It is used to achieve the desired level in the output while regulating the capacitor voltages. Nevertheless, the most attractive feature is the natural voltage balance characteristic [6, 7]: voltage unbalance causes higher voltage ripples, output distortion and eventual power switches failure. Furthermore, it has no limit range for the modulation index and is applicable for dc/dc, dc/ac and ac/dc modes [1]. For greater performance and output quality, just

one switching state should change per voltage transition and flying capacitors must be charged and discharged equitably [2,4]. As a result, a smooth and nearly ideal sinusoidal waveform can be generated at the output. This chapter will introduce the FCC circuit topology and operation and analyze Pulse-width modulation (PWM) switching techniques used to achieve self-voltage balancing.

2.2 Circuit Topology and Operation

The main concept of the FCC is the use of capacitors in a series connection with two power switches as clamped switching cells [1]. The output voltage levels will rely on the combination of the flying capacitors voltages and the dc link. The middle output levels are generated when the load current passes through the flying capacitor paths, therefore, several combinations of switching states are possible. The number of levels depend on the number of power semiconductor devices connected in series. An 'N' level FCC inverter requires the following:

$$K = N - 1 \tag{2-1}$$

$$S = 2(N - 1) \tag{2-2}$$

$$M = (N - 1)(N - 2)/2 \tag{2-3}$$

where K refers to the number of FCC cells, S is the total number of switching devices and M is the number of flying capacitors if it assumed that they all have the same voltage rating. The topology configuration for $N = 5$ is shown in Figure 2-1, which is the one selected for the project.

For a five-level FCC, the voltage across each flying capacitor corresponds to one quarter of the dc source voltage. The output voltage consists of five different voltage levels $+V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$, and $-V_{dc}/2$, where V_{dc} is the voltage of the dc bus. There are eight switching devices that must operate as complementary pairs: when the top is turned ON "1", the bottom

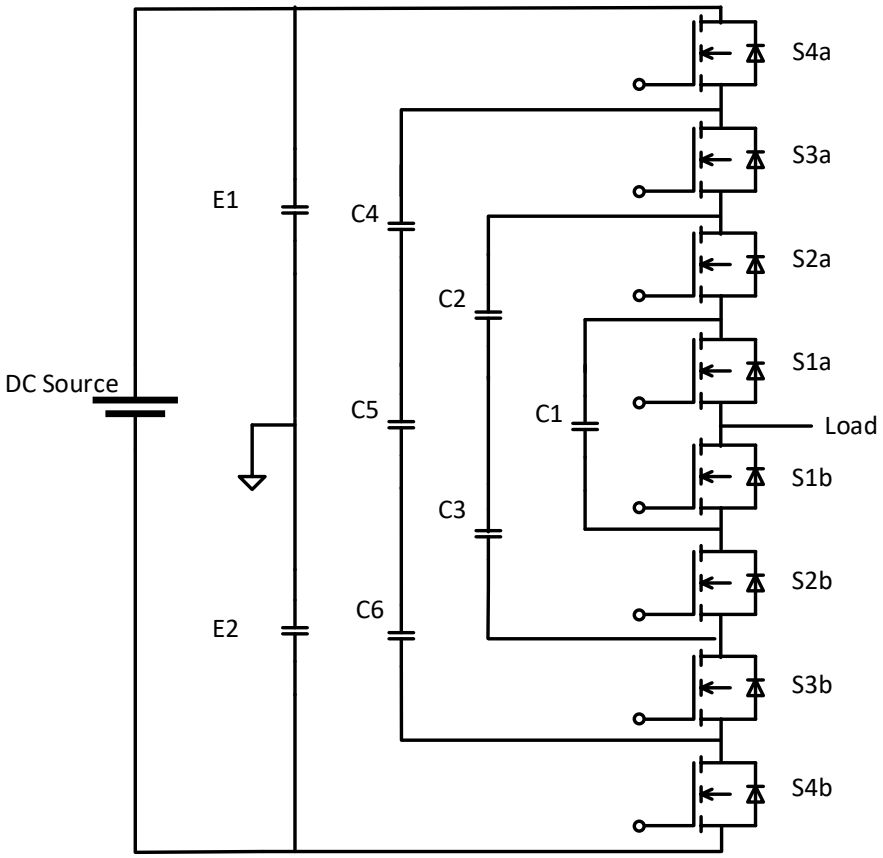


Figure 2-1. Circuit configuration of a five-level FCC

switch must be OFF "0" to mitigate the presence of a short circuit. In this case, switches S_{1a}& S_{1b}, S_{2a}& S_{2b}, S_{3a}& S_{3b} and S_{4a}& S_{4b} are complementary to each other. Using Kirchhoff's voltage (KVL) and current laws (KCL), the phase voltage V_p and the currents through the flying capacitors i_{c1}, i_{c2} and i_{c3} can be written as:

$$V_p = -\frac{V_{dc}}{2} + S_{4a}V_{dc} + (S_{3a} - S_{4a})V_{c3} + (S_{2a} - S_{3a})V_{c2} + (S_{1a} - S_{2a})V_{c1} \quad (2\text{-}4)$$

$$i_{c1} = (S_{2a} - S_{1a})i_{LOAD} \quad (2\text{-}5)$$

$$i_{c2} = (S_{3a} - S_{2a})i_{LOAD} \quad (2\text{-}6)$$

$$i_{c3} = (S_{4a} - S_{3a})i_{LOAD} \quad (2\text{-}7)$$

Table 2-1. All possible switching states combinations for a five-level FCC

S_{4a}	S_{3a}	S_{2a}	S_{1a}	Output Voltage	i_{c1}	i_{c2}	i_{c3}
0	0	0	0	-Vdc/2	0	0	0
0	0	0	1	-Vdc/4	0	0	-
0	0	1	0	-Vdc/4	0	-	+
0	0	1	1	0	0	-	0
0	1	0	0	-Vdc/4	-	+	0
0	1	0	1	0	-	+	-
0	1	1	0	0	-	0	+
0	1	1	1	Vdc/4	-	0	0
1	0	0	0	-Vdc/4	+	0	0
1	0	0	1	0	+	0	-
1	0	1	0	0	+	-	+
1	0	1	1	Vdc/4	+	-	0
1	1	0	0	0	0	+	0
1	1	0	1	Vdc/4	0	+	-
1	1	1	0	Vdc/4	0	0	+
1	1	1	1	Vdc/2	0	0	0

where V_{c3} is the sum of the voltages of capacitors C4, C5 and C6, V_{c2} of capacitor C2 and C3 and V_{c1} is the voltage of C1. Based on Equations (2-4), (2-5), (2-6) and (2-7), the phase output voltage and the flying capacitor current directions are determined for all switching states and are shown in Table 2-1. The possible switching states combinations are represented in binary notation as the control state of the upper switches. As evidenced, there are redundant switching modes capable of generating $V_{dc}/4$, 0 and $-V_{dc}/4$ voltage levels. In addition, the inverse of the switching states combinations that generate $V_{dc}/4$ will result in a load voltage of $-V_{dc}/4$. Changes between each middle output voltage level impacts directly with either charging or discharging the flying

Table 2-2. Comparison between various multilevel topologies

	NPC	CHBC	MMC	FFC
Levels	5	5	5	5
Switches	8	8	16	8
Sources	1	2 (isolated)	1	1
Capacitors	2	0	10	8
Clamping Diodes	12	0	0	0

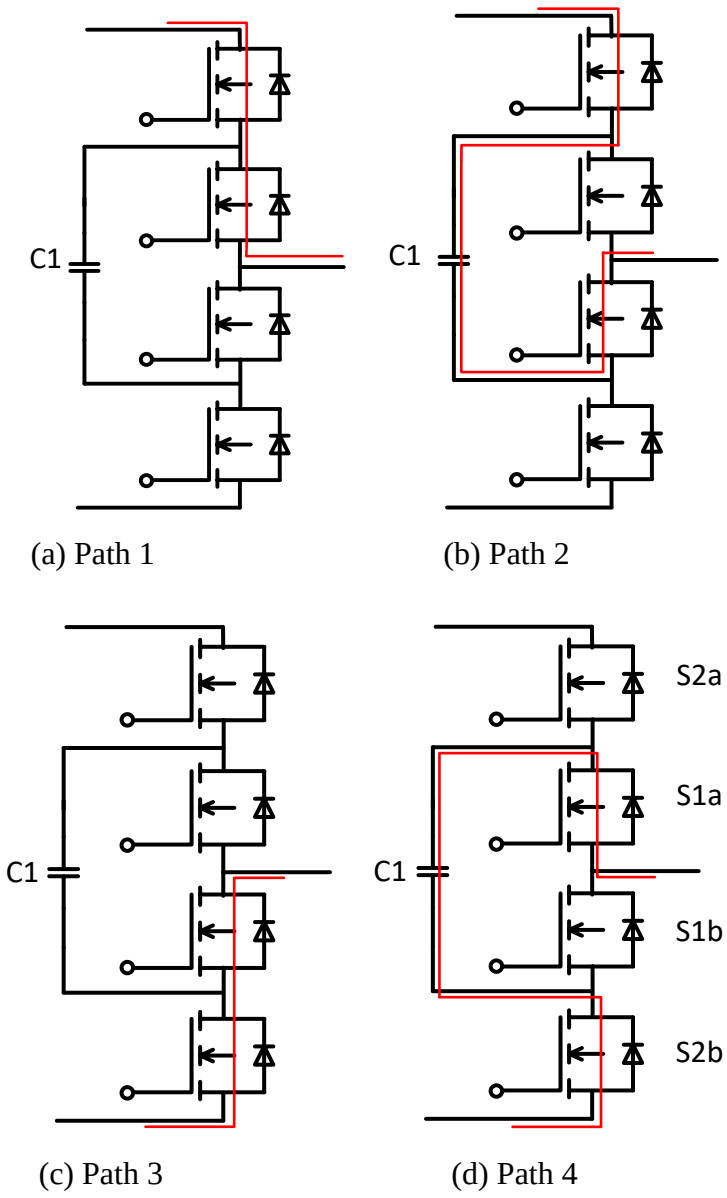
capacitors. Table 2-2 displays the comparison of important parameters between all multilevel topologies that have been discussed previously.

2.3 Switching Techniques for Flying Capacitor Balancing

As long as the controller goes into every state of charging and discharging at a middle output level, the FCC will be operating with capacitor voltage self-balancing [8-10]. If not, the capacitor voltage will be unbalanced when there is a slight difference in the charge and discharge periods. Switching delays are the main cause of unbalances because the flying capacitors iterate the charge and discharge operations in the period established by the PWM frequency [8-10]. In order to preserve balance in each capacitor voltage, some conditions shall be met [2]:

a. For every voltage step, there must be just one switching state changing.
b. Power switches shall be used equally.

Figure 2-2 illustrates the possible arrangement that can happen during the operation of three-level flying capacitor converter [3]. Recalling that the upper switches are working as complementary pairs with the bottom switches, if the position of path 2 and path 4 work over consecutive cycles; there will not be net change in the charge of the capacitors if the switching period is the same for both paths. As well, in the positions of path 1 and path 3, both switches shall



(a) Path 1 (b) Path 2

(c) Path 3 (d) Path 4

Figure 2-2. Possible current paths of a three-level flying capacitor converter.

share the same angular period to ensure they have the same losses and are used uniformly. Another important feature is discussed in [11]: the inherent self-balancing function of the flying capacitor voltage due to compensative change in the load current.

Several switching techniques have been developed to control multilevel converters [4, 5, 12, 13]. High-frequency switching methods are widely implemented in dc/ac and ac/dc multilevel

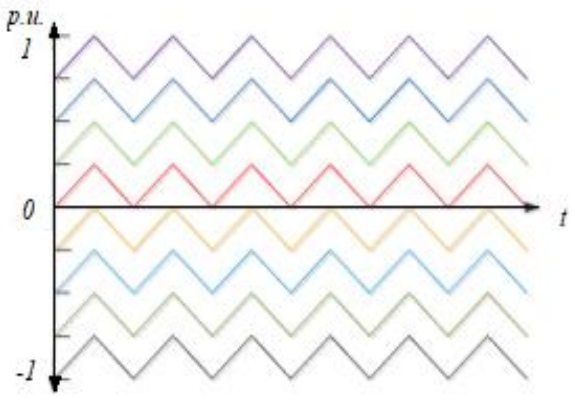


Figure 2-3. Phase-disposition PWM carrier waveforms

converters due to satisfactory performance and ease of implementation. Two different methods arise when controlling FCCs: the phase disposition pulse-width modulation (PD-PWM) and the phase-shift PWM (PS-PWM), also known as carrier-based phase shifted modulation.

2.3.1 PD-PWM

With the PD-PWM, the natural voltage balance of the capacitors may be accomplished based on carrier rotation for different switches [14]. This technique uses different triangular waveforms that are arranged on top of each other, without phase shift, for every switching module as presented in Figure 2-3. The carrier signals are compared with a reference to generate the expected output signal. Whenever a carrier is higher than the reference, the PWM output will be low; contrarily if the carrier is lower than the reference then the PWM output is high. Its main disadvantage is the need of an extra carrier rotation technique due to the presence of unbalancing in the capacitor voltages at higher number of voltage levels. Also, the carrier amplitudes need to be modified depending on the reference magnitude at each voltage level. A simplified approach was discussed in [15], yet the natural balance solution is not fast enough.

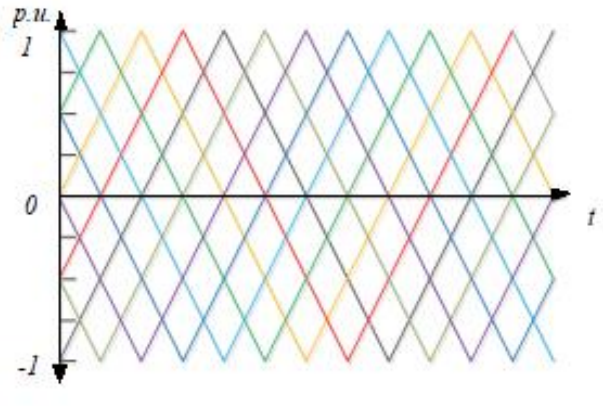


Figure 2-4. Phase-shift PWM carrier waveforms

2.3.2 PS-PWM

PS-PWM requires the same number of carriers like the PD-PWM, each carrier is associated to a complementary pair of power semiconductor devices as shown in Figure 2-4. These carriers shall have the same amplitude, frequency and a phase shift of $360°/(n - 1)$, where n is the level of the FCC. In the case of a five-level FCC, the PS-PWM needs four carriers phase-shifted by 90°. The reference signal is compared with the carriers to define the output voltage level.

When PS-PWM is employed, the charging and discharging durations of two different switching states are equal in the same carrier period [13]. As a result, the natural voltage balancing is achieved considering that the average voltage of the flying capacitors does not require the implementation of an additional complex controller to constantly monitor the capacitor voltages.

2.3.3 Other modulation techniques

The active balancing modulation method require measurements to define the appropriate switching state and set the voltage-balancing characteristic in the capacitors [16]. However, extra control implementation is needed due to the not-uniform switching usage distribution, which has been declared as an essential part to preserve the voltage balance. A closed-loop control method

based on states averaging techniques is proposed in [17] to balance the capacitor voltage. In [18], the voltage balancing uses an optimum switching transition scheme based on evaluating a cost functions. However, it produces larger voltage ripples than the simple PS-PWM. Predictive control is implemented in [19, 20] to decide which converter redundancies will be used for capacitor balancing. In [21], a state machine is used to allocate the switching events of the converter in a cyclical way. It avoids narrow switching pulses and preserves the natural balancing property. At certain extreme regions of the duty ratio, the PS-PWM does not guarantee the self-balancing in the capacitors. An improved PS-PWM (iPS-PWM) was presented in [16], resulting in faster balancing dynamics in those duty ratio ranges.

2.4 Conclusion

An overview of the fundamental concepts of the FCC was presented in this chapter in order to understand the necessary background information to be considered during the UCSC system design stage. The major challenge comes with the selection of an appropriate modulation technique to achieve capacitor voltage balancing. It has been shown that PS-PWM scheme achieves natural balancing of FCCs, therefore this algorithm has been selected for the initial design. Furthermore, iPS-PWM will be included in a separate case to compare both techniques and select the most effective.

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CHAPTER 3

UNBALANCED CURRENT STATIC COMPENSATOR: COMPONENTS AND CONTROL ALGORITHM

3.1 Introduction

The UCSC application is designed to compensate for the negative- and zero-sequence currents generated by single-phase unbalanced loads and DG. Significant improvement is achieved with the FCC inclusion, as power factor control and potentially harmonic current elimination can be addressed effectively at medium- and high-voltage power systems [1]. The UCSC system is connected at the PCC and each phase is monitored separately. If the currents flowing from the distribution substation to the loads are not balanced, then the three-phase FCC will inject or draw current until the expected balance is obtained. The controller uses the average of the substation currents and the d-q synchronous-rotating reference frame. The UCSC system parameters will be defined in this chapter along with the explanation of the control algorithm.

3.2 UCSC System Parameters

As mentioned previously, the energy storage capacitor in the dc link will sustain up to 200 V and the power semiconductor devices will be switched at 10 kHz. The output current injected or drawn from the grid will be synchronized at a fundamental frequency of 60 Hz. Figure 3-1 illustrates the three-phase UCSC system.

3.2.1 DC link & flying capacitor sizing

Reduction of the capacitor size for both dc link and flying capacitors have become a primary concern due to the direct impact they play on the price, physical size, lifetime and failure rate of the application [2]. Theoretical investigations of the dc link design have been explored in

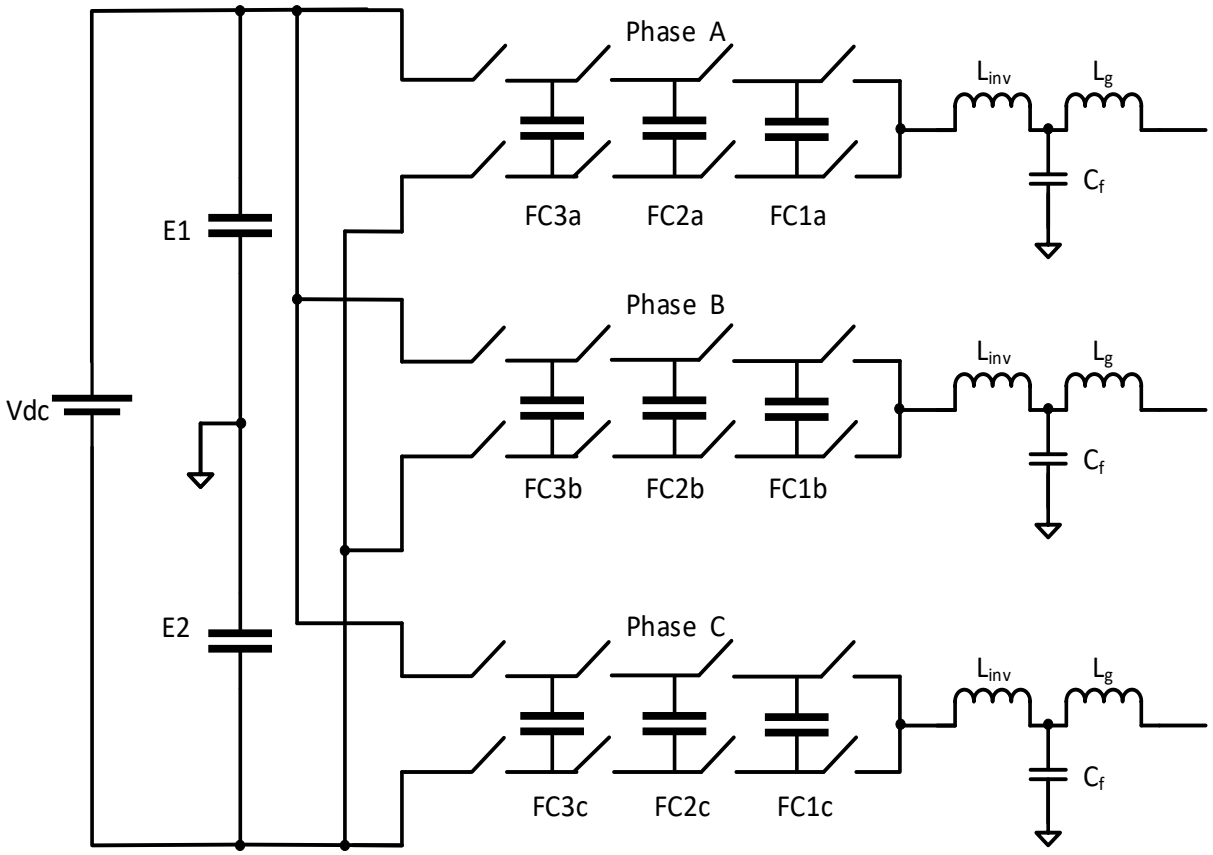

Figure 3-1. Three-phase FCC UCSC diagram

[2-4]: current and voltage ripple expressions were calculated and PWM algorithms are used to determine the minimum capacitance for lower harmonics. The system described in this thesis uses a dc source connected to the dc link; thus, the dc link voltage ripple becomes negligible and not so much effort has to be spent in the dc-capacitor selection. However, equation (3-1) was utilized to calculate the dc link capacitance C_{dc} as a measure to allow the dc source removal and the addition of a dc link controller for future testing scenarios:

$$C_{dc} = \frac{i_{dc}}{2\Delta V_{dc}\omega} \tag{3-1}$$

where i_{dc} is the input-current ripple, ΔV_{dc} is the dc link voltage ripple [5].

Similar to the dc link capacitor, the voltage ripple of flying capacitors needs to be considered carefully as it plays a major role in the eventual size of the components [6]. Lower

capacitance enables the replacement of conventional electrolytic capacitors with thin film capacitors, providing fewer losses, extended lifetime and higher reliability at the cost of a slightly increased voltage imbalance [7]. Despite this, the inherent self-voltage balancing property of FCCs can address this issue as discussed in Chapter 2. A study of the minimum required capacitance C_{fc} is presented in [6] and the expression of a flying capacitor ripple voltage is given as:

$$\Delta V_{fc} = \frac{I_o(1 - m_a)}{2C_{fc}f_{sw}} \tag{3-2}$$

where I_o is the output current amplitude, m_a the modulation index and f_{sw} the PWM switching frequency.

3.2.2 Power semiconductor devices

Traditionally, power MOSFETs have been widely used in low-voltage, low-current and high-switching frequency applications [8]. Lower rise and fall times, high-blocking voltage capability and small conduction losses are some advantages that MOSFETs offer when compared to IGBTs [8, 9]. Nowadays, with the development of silicon carbide (SiC) MOSFETs, even better characteristics have been achieved such as ON-state resistance reduction, overall smaller size at high-voltage levels, improved efficiency and better power dissipation [10]. Based on this, SiC MOSFET have become the favorite semiconductor device for use in medium- and high-voltage power electronics applications [11]. For the purpose of this thesis, the IRL640A N-Channel Logic MOSFET produced by Fairchild Semiconductor is selected for the low-voltage UCSC prototype due to its lower cost and satisfactory characteristics. The main parameters of this device will be discussed in Chapter 5.

Table 3-1. UCSC system parameters

Grid frequency (f)	60 Hz
Switching frequency (f_{sw})	10 kHz
DC link maximum voltage (V_{dc})	200 V
DC link capacitor (C_{dc})	780 uF
Flying capacitor (C_{fc})	4.7 uF
Inverter side inductor (L_1)	2.2 mH
Grid side inductor (L_2)	0.5 mH
Filter capacitor (C_f)	4.7uF
Damping resistor (R_f)	10 Ω

3.2.3 LCL filter

THD improvement is highly desirable when connecting a power electronic converter to the grid [11]. The simpler solution is the addition of a single inductance at the output of the converter; however, it was proven in [12] that LCL filters provide better dynamic response and are smaller. The comprehensive guideline presented in [13] has been used to design the LCL output filter for the system.

Damping resistors are connected in series with the capacitor to eliminate certain resonances in the response created by the inclusion of the filter. The inductors were set to 2.2 mH and 0.5 mH given that these inductors were constructed beforehand in a previous research project [5]. Table 3-1 summarizes the systems parameters selected for simulations and testing procedures.

3.3 Reference Current Algorithm

Beside the development of the switching topology, the controller design can be considered the most challenging task. The correct implementation of modern control systems ensure the safety of users, equipment and environment. The UCSC control algorithm from Figure 3-2 uses the measurements from the substation currents, PCC voltages, loads currents and the output currents from the converter.

A proportional-integral (PI) compensator has been selected to guarantee zero steady-state error and fast tracking of the references. PI controllers require a constant or slow variable reference signal to compensate effectively but have a simpler structure and lower dynamic order than other compensators. The transfer function if given by [14]:

$$G_c(s) = \frac{\left(k_p s + k_i\right)}{s} \tag{3-3}$$

where k_p is the proportional term which increase the speed of the controller and reduces the steady-state error while k_i is the integral term that reduce the rise time of the response and completely tends to eliminate the steady-state error [15].

3.3.1 Single-phase d-q synchronous-rotating transformation

Three-phase systems operate with time-variable ac waveforms on each phase; therefore, d-q synchronous-rotating reference frame needs to be implemented to transform a-b-c instantaneous values to dc equivalent values [16]. Transformation to the α-β stationary reference frame allows the conversion of the three-phase system problem in an equivalent two control loop problem, though the compensator will need to be of high order and the closed-loop bandwidths will need to be larger than the reference frequency [16]. Consequently, the controller design will be more

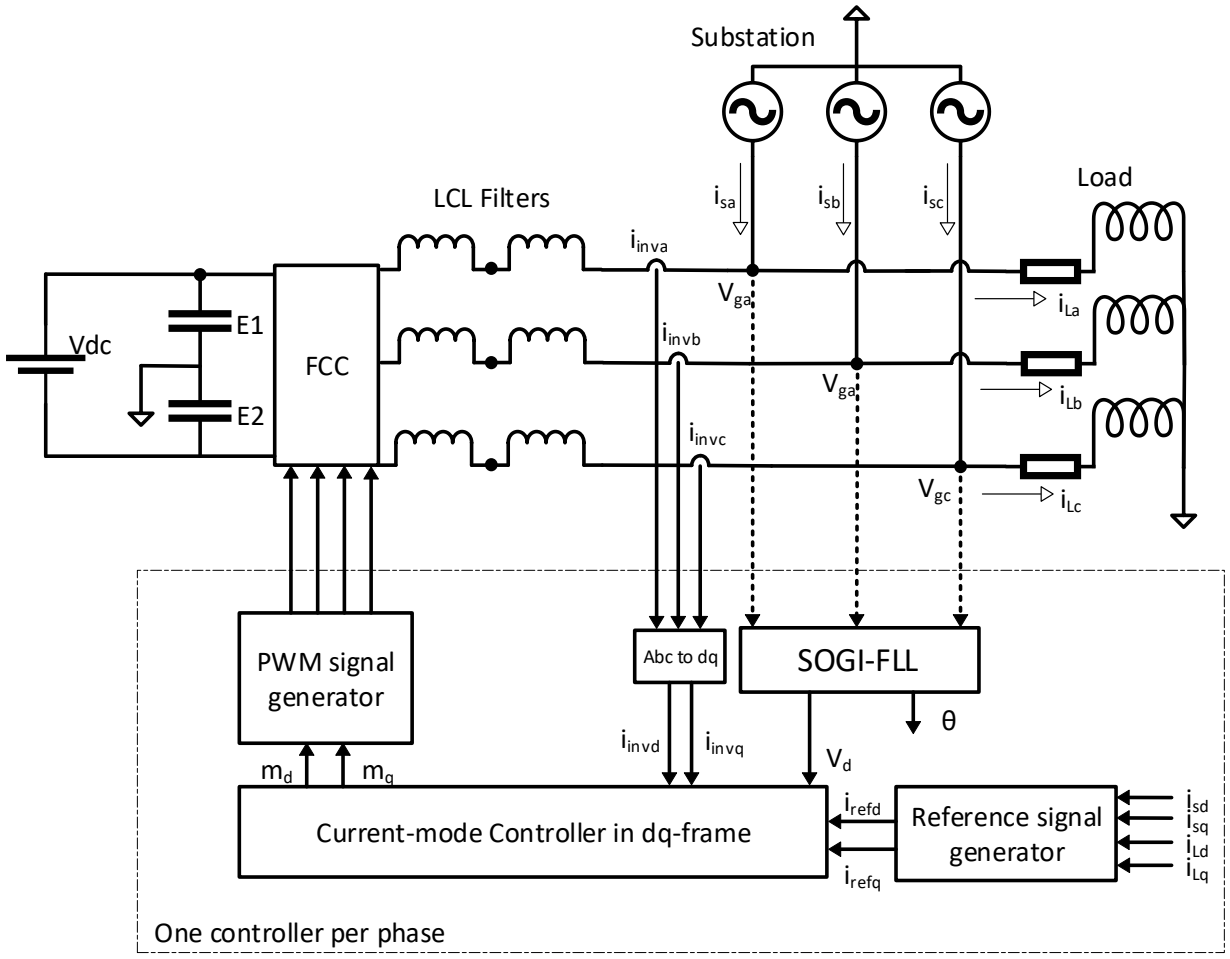

Figure 3-2. Schematic diagram of the UCSC control algorithm

sophisticated. The α-β-0 transformation, also known as the Clarke's transformation is given by [17]:

$$\begin{bmatrix} \alpha \\ \beta \\ 0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{3-4}$$

and the transformation from α-β-0 to the d-q-0 reference frame is given by:

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} cos(\theta) & sin(\theta) & 0 \\ -sin(\theta) & cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \\ 0 \end{bmatrix} \tag{3-5}$$

Direct transformation from the a-b-c instantaneous values to the d-q synchronous-rotating reference frame can be accomplished using the Park's transformation:

$$\begin{bmatrix} d \\ q \\ 0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} cos(\theta) & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta + \frac{2\pi}{3}\right) \\ sin(\theta) & sin\left(\theta - \frac{2\pi}{3}\right) & sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} & \frac{\sqrt{2}}{2} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{3-6}$$

However, these expressions are not useful for unbalanced three-phase systems, as the zero component will contain non-zero values, returning the unwanted third control loop problem [13]. This issue can be solved using single-phase d-q synchronous-rotating frame transformations with a modification of equation (3-5) [17]:

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} cos(\theta) & sin(\theta) \\ -sin(\theta) & cos(\theta) \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \tag{3-7}$$

For single-phase systems, it becomes impossible to determine the phase data of the signal as a second variable is needed to compare with the established zero phase reference. In [17], the creation of a fictitious variable in-quadrature or delayed with the single-phase current or voltage measurement was proposed using a single-phase d-q reference frame controller. A comparison between the use of Hilbert transformation, adding a transport delay and the inverse Park transformation was analyzed in [18]. All these methods are capable of generating the orthogonal signal but still bring many drawbacks such as nonlinearity, low harmonic filtering, frequency dependence, and greater complexity when compared with the second-order generalized integrator (SOGI).

3.3.2 Second-order generalized integrator

The SOGI combines the advantages of all previous orthogonal generators and allows for harmonic filtering without delay, frequency independence and ease of implementation [19]. The block diagram of the SOGI presented in Figure 3-3 can be modeled using the following equations:

$$\frac{Y(s)}{U(s)} = \frac{\omega_o s}{s^2 + {\omega_o}^2} \tag{3-8}$$

$$\frac{Y'(s)}{U(s)} = \frac{{\omega_o}^2}{s^2 + {\omega_o}^2} \tag{3-9}$$

where ω_o is the center frequency of the SOGI and is required to be equivalent to the input signal frequency to obtain the correct orthogonal signal [19].

The only drawback of the SOGI is the presence of a resonance in the response, which causes the output signal amplitude to increase infinitely [20]. A feedback loop is added from the output as shown in Figure 3-4 to eliminate the resonance issue and the structure is now defined as SOGI Orthogonal Signal Generator (SOGI-QSG). Equations (3-10) and (3-11) display the transfer function of the direct and orthogonal outputs.

$$\frac{Y(s)}{U(s)} = \frac{k\omega_o s}{s^2 + k\omega_o s + {\omega_o}^2} \tag{3-10}$$

$$\frac{Y'(s)}{U(s)} = \frac{k{\omega_o}^2}{s^2 + k\omega_o s + {\omega_o}^2} \tag{3-11}$$

where *k* represents the damping factor and modifies the bandwidth of the system [20]. Frequency independence comes with the inclusion of an extension of the SOGI known as SOGI Frequency Locked Loop (SOGI-FLL) [20, 21].

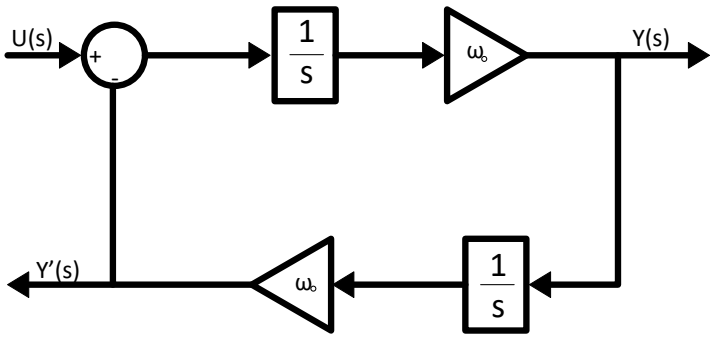

Figure 3-3. SOGI structure in the frequency domain

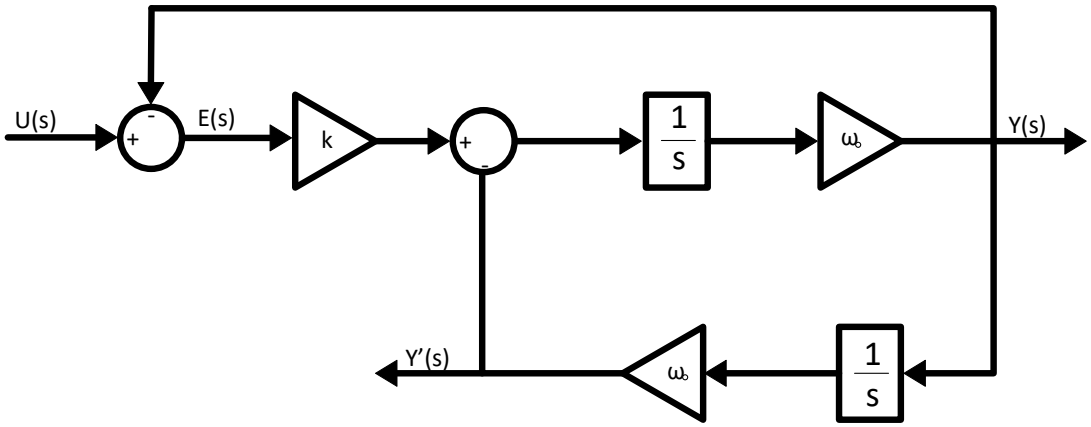

Figure 3-4. SOGI-QSG structure in the frequency domain

3.3.3 Single-phase SOGI-FLL

The main idea behind a Phase Locked Loop (PLL) is to obtain important information from each substation phase like frequency, magnitude and phase angle [18, 19]. These angles are used to synchronize the output voltage generated by the converter at the PCC to obtain unity power factor and generate the converter reference signal. Unlike the PLL, this structure is most used in variable-frequency applications or to overcome sudden phase angle jumps during transient grid faults [21]. The difference between the in-phase output and the input signal is calculated, then multiplied by the in-quadrature signal and amplified by a factor $-\gamma$ to cancel out the error component. Allowing the input frequency ω estimation that ultimately becomes the SOGI

resonance frequency ω_o [20]. The error signal and the SOGI-FLL block diagram are given in equation (3-12) and Figure 3-5, respectively:

$$\frac{E(s)}{U(s)} = \frac{(s^2 + {\omega_o}^2)\, v}{s^2 + k\omega_o s + {\omega_o}^2} \tag{3-12}$$

With the implementation of the SOGI-FLL, the in-phase and in-quadrature outputs can be considered as α-β stationary reference frame variables. Equation (3-7) can be employed to transform from α-β to d-q. If the q-axis component value is different from zero, the estimated error is added to the approximated grid frequency, which will eventually decrease or increase the phase angle that will be used in the next cycle. Figure 3-6 illustrates one single-phase SOGI-FLL cycle.

3.3.4 Reference current generation

Load and converter currents from each phase are passed through the SOGI filter, then equation (3-7) is applied to transform to the d-q synchronous-rotating reference frame. At the PCC, the KCL equation can be written as:

$$i_{sd} + i_{invd} + i_{Ld} = 0 \tag{3-13}$$

The d-axis components of the load currents are averaged and subtracted from the substation d-axis currents calculated in equation (3-13). A PI compensator is then applied to each reference signal and the resultant output signal is the d-axis reference current that will go into the current-mode controller. Figure 3-7 shows the whole process diagram.

3.4 Current-Mode Controller

Although, some grid-application converters use voltage-mode control, it has disadvantages like vulnerability against overcurrent due to the exclusion of a current closed loop [22]. Current-mode controllers offer robustness versus initial parameters changes, improved dynamics, higher

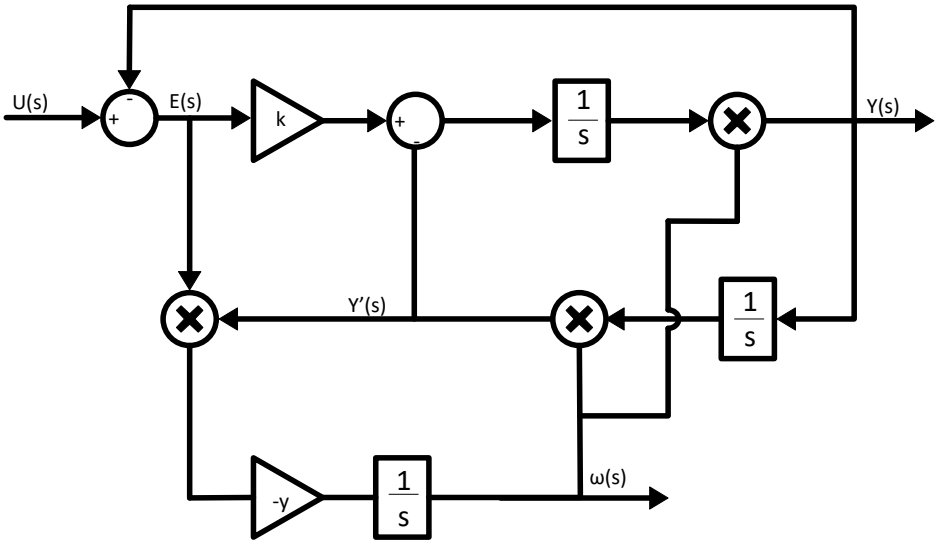

Figure 3-5. SOGI-FLL structure in the frequency domain

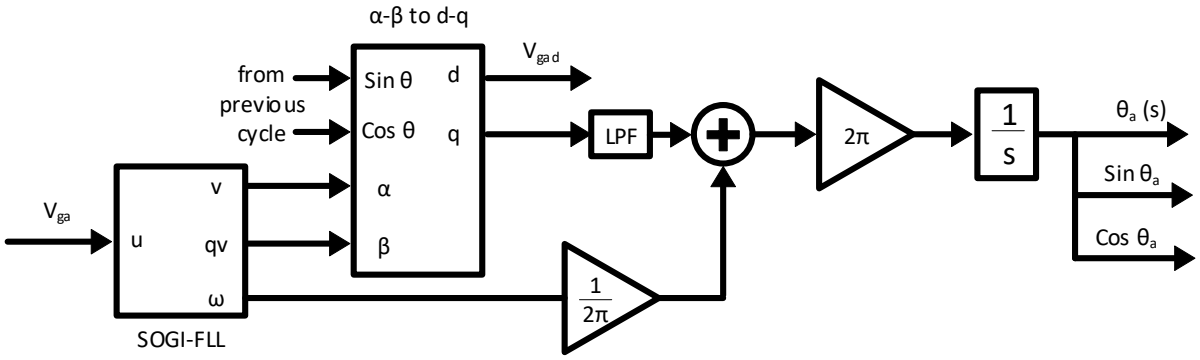

Figure 3-6. Single-phase SOGI-FLL cycle

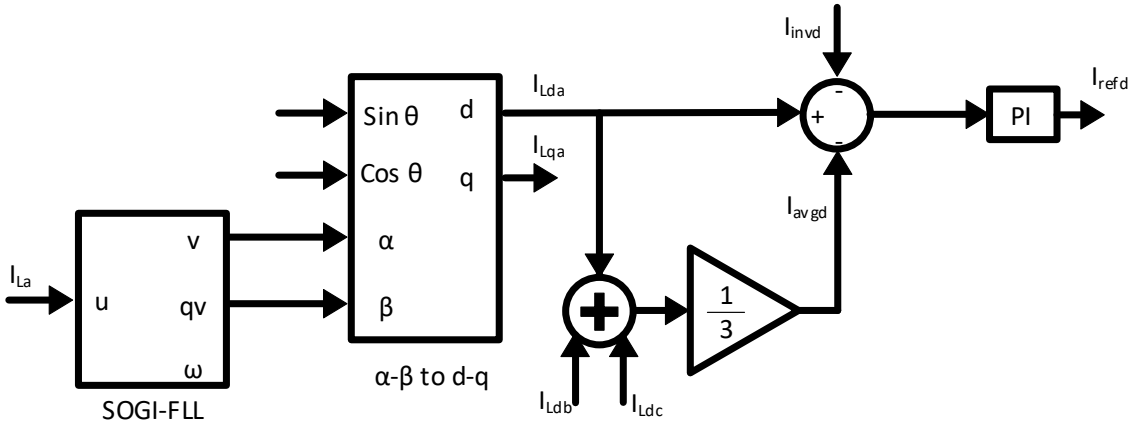

Figure 3-7. Single-phase reference current generation

precision and a dedicated control scheme that protects against overcurrent [23]. Figure 3-8 illustrates the d-q decoupled current-mode controller block diagram. Independent PI compensators are used to track both d- and q-axis references. In [24], an equivalent circuit of a single-phase voltage-source converter for grid-applications is presented as shown in Figure 3-9 where the LCL filter capacitor is neglected. Using this representation, the decoupled output voltage v_{od}, v_{oq} of the converter can be expressed in the d-q synchronous-rotating reference frame as:

$$\begin{bmatrix} v_{od} \\ v_{oq} \end{bmatrix} = R \begin{bmatrix} i_{invd} \\ i_{invq} \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_{invd} \\ i_{invq} \end{bmatrix} + \begin{bmatrix} 0 & -\omega L_t \\ \omega L_t & 0 \end{bmatrix} \begin{bmatrix} i_{invd} \\ i_{invq} \end{bmatrix} + \begin{bmatrix} v_{gd} \\ 0 \end{bmatrix} \tag{3-14}$$

$$L_t = L_{inv} + L_g \tag{3-15}$$

where v_{gd} represent the feed-forward term of the grid voltage and i_{invd}, i_{invq} are the output currents of the converter [24]. Therefore, PI compensator outputs are added together with the inverter and grid inductors filter voltages, and the feed-forward term to generate the voltage references used in the PWM scheme.

3.4.1 Active and reactive power control

The implementation of a controller that monitors each phase separately provides independent control of active and reactive power flow, with the decoupling of d- and q-axis components [24]. Assuming a single-phase PCC voltage v_g and inverter output current i_{inv} have the following form:

$$v_g = V_g \cos(\omega_o t) \tag{3-16}$$

$$i_{inv} = I_{inv} \cos(\omega_o t - \emptyset) \tag{3-5}$$

the inverter output current i_{inv} can be expressed as:

$$i_{inv} = I_{invd} \cos(\omega_o t) - j I_{invq} \sin(\omega_o t) \tag{3-6}$$

$$i_{invd} = I_{inv} \cos(\emptyset) \tag{3-7}$$

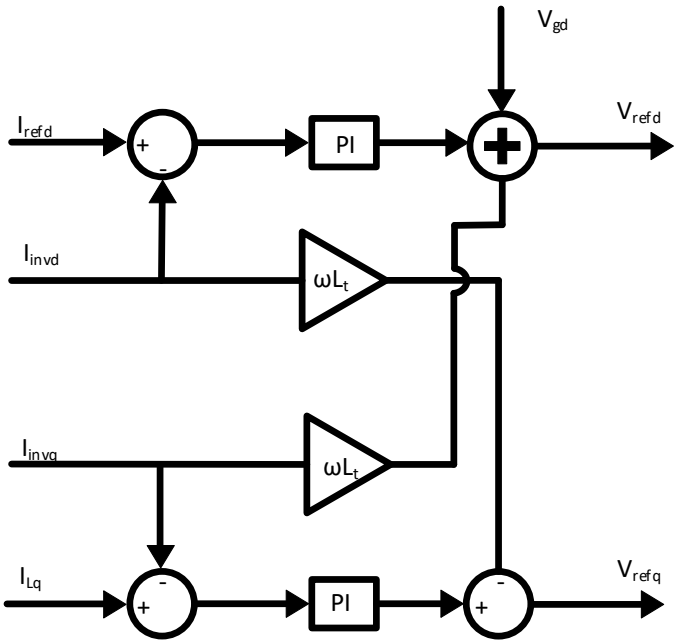

Figure 3-8. D-Q decoupled current-mode controller block diagram

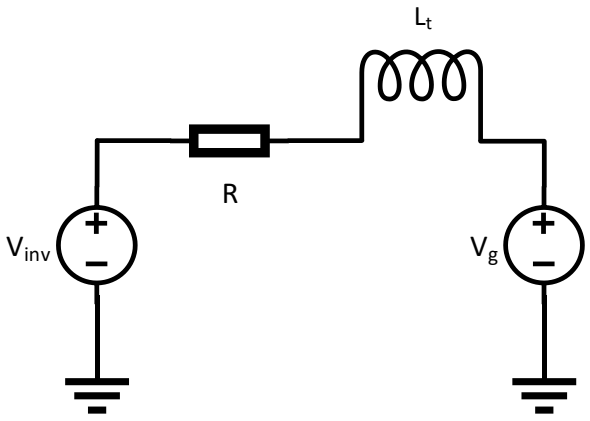

Figure 3-9. Equivalent circuit of a single-phase voltage-source converter for grid-applications.

$$i_{invq} = -I_{inv}\sin(\emptyset) \tag{3-20}$$

where V_g, I_{inv} refer to the amplitude of the PCC voltage and the inverter output current; while I_{invd}, I_{invq} are the inverter output current amplitude components in d-q rotating reference frame. Active and reactive power in grid-connected applications is calculated as follows [24]:

$$P = \frac{V_g I_{inv}}{2} \cos(\emptyset) \tag{3-21}$$

$$Q = \frac{V_g I_{inv}}{2} \sin(\emptyset) \tag{3-22}$$

and considering equations (3-19) and (3-20) then:

$$P = \frac{v_{gd} i_{invd}}{2} \tag{3-23}$$

$$Q = \frac{v_{gd} i_{invq}}{2} \tag{3-24}$$

These calculations apply for each phase; thus, compensation of active and reactive power is accomplished independently by i_{invd} and i_{invq} current loops respectively. For reactive power compensation the q-axis current reference is the q-axis component of the load current. Thus, power factor correction at the PCC is dependent of the load current value since the imaginary current component produces all reactive power.

3.5 PWM Signals Generation

The PWM algorithm generates the commands used for each switching device as explained in Chapter 2. The voltage references from the current-mode controller should be transformed back to the α-β stationary reference frame with the inverse of equation (3-7). Synchronization with the grid is guaranteed if the phase angle θ generated in the SOGI-FLL is used during the transformation. In addition, the control signal is normalized for harmonic reduction using the instantaneous dc link voltage [5].

3.6 Conclusion

In this chapter, important parameters such as the semiconductor device (MOSFET), the LCL filter design and the capacitor sizing were defined in order to proceed with the

implementation of simulations. Also, the current-mode control algorithm used for the UCSC has been presented. It can be summarized in three steps:

a. Reference current generation

b. Current-mode controller algorithm

c. PWM signals generation

3.7 References

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CHAPTER 4

UCSC SIMULATION MODELS AND RESULTS ANALYSIS

4.1 Introduction

Software modeling is an essential process that provides great contribution when building a prototype, as efficiency can be improved significantly and the control algorithm performance can be enhanced. Although continuous-time domain simulations can be used to verify power converters models, discrete-time domain simulations provide more realistic results [1]. A review of discrete-time implementations methods will be presented in this chapter. First, an open-loop single-phase five-level FCC model was developed in MATLAB/SIMULINK™ using the parameters in Table 3-1. Analytical calculations where compared with the simulation results to confirm the model functionality. Then, a closed-loop three-phase five-level FCC was simulated as a controlled-voltage source to set the controller parameters depending on the desired switching frequency and bandwidth. Thirdly, a LCL filter model was implemented in the controller to remove the inrush currents normally occurring during synchronization. At last, the UCSC model was connected to a grid to test substation current balancing and reactive power compensation modes.

4.2 Discrete-Time Implementation Methods for Real-Time Simulations

Digital control circuits such as DSPs (Digital Signal Processors) and FPGAs (Field Programmable Gate Arrays) have been widely used for signal processing in power electronic applications. Discretization of the continuous time domain is required when implementing any structure, like the SOGI-FLL or PI compensators, on these circuits. Therefore, the discrete-time

Table 4-1. Discretization methods and their transfer functions

Method	**Transfer Function**
Euler Forward	$s = \frac{z-1}{T_{samp}}$
Backward Euler	$s = \frac{z-1}{zT_{samp}}$
Tustin (Trapezoidal, Bilinear)	$s = \frac{2}{T_{samp}} \frac{z-1}{z+1}$
Zero-order hold	$X(z) = (1-z^{-1})Z\left\{L^{-1}\left\{\frac{X(s)}{s}\right\}\right\}$
Zero-pole matching	$z = e^{sT_{samp}}$
First-order hold	$X(z) = \frac{(1-z^{-1})}{T_{samp}z^{-1}} Z\left\{L^{-1}\left\{\frac{X(s)}{s^2}\right\}\right\}$

transformation shall be considered to develop a more accurate system simulation. Table 4-1 shows different discrete approximations methods used to transform a continuous s-domain transfer function in a discrete z-domain transfer function [2].

When choosing a specific discretization method, the discretized structure needs to be considered because numerical integration methods and non-integration methods can provide different results [2]. A comparison between different numerical integration methods is presented in [3]. In summary, Forward Euler and Backward Euler methods present poor orthogonality and magnitude inaccuracy when compared with the Tustin method or high-order integrators. Depending on the discretized structure, non-integration methods may not be stable or include permanent steady-state errors [2]. Therefore, the Tustin method was selected for the project because high-order integrators require extra memory space while improvement is not significant.

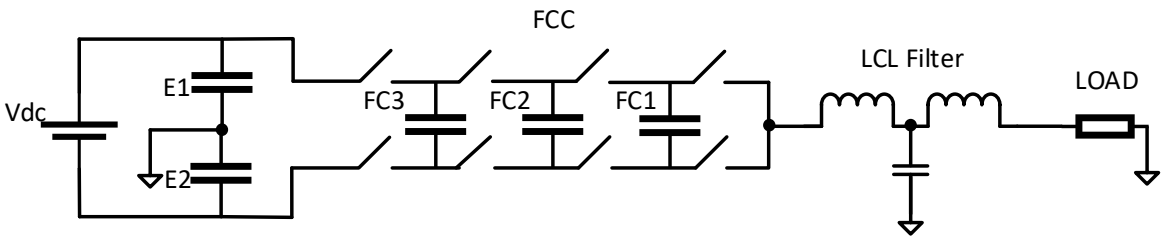


Figure 4-1. Single-phase five-level FCC

4.3 Open-Loop Single-Phase Five-Level FCC Model

Important features of the FCC operation were considered during the first simulations: initial flying-capacitor charging process, balancing dynamics, capacitor voltage ripples and converter outputs. The single-phase five-level FCC from Figure 4-1 was implemented in MATLAB/SIMULINK™ using the UCSC parameters from Table 3-1. The load was set to 60 Ω, and a sinusoidal waveform was used as the reference signal for the PWM. The modulation index m_a could be changed between 0 and 1. Current and voltage load output waveforms are shown in Figure 4-2 where the current has been amplified by 20 for illustrative purposes.

As mentioned in Chapter 2, a comparison between the effectiveness of the PS-PWM and the iPS-PWM has been included in order to determine the most appropriate modulation technique for the FCC. For a five-level FCC, the PS-PWM uses four carrier waveforms phase-shifted by 90° as illustrated in Figure 4-3, where carrier 1 (blue), carrier 2 (red), carrier 3 (yellow) and carrier 4 (purple) generate the PWM signals for the switching devices. It has been confirmed with frequency and time domain analyses that at certain duty ratio regions, the natural balancing property was not present [4-6]. Consequently, the iPS-PWM scheme was designed in [7] to solve the previous problem and to limit switching losses; in particular, by using consecutive switching states during each level change and applying equal period at inverse switching states. Figure 4-4 shows the iPS-

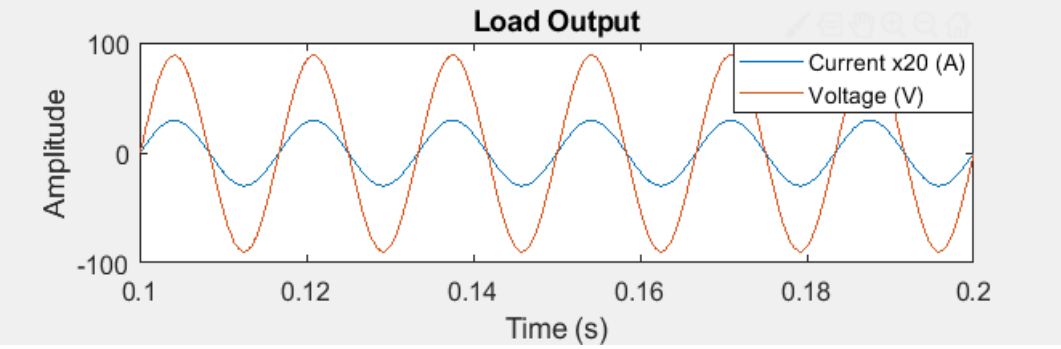


Figure 4-2. Current and voltage load output waveforms

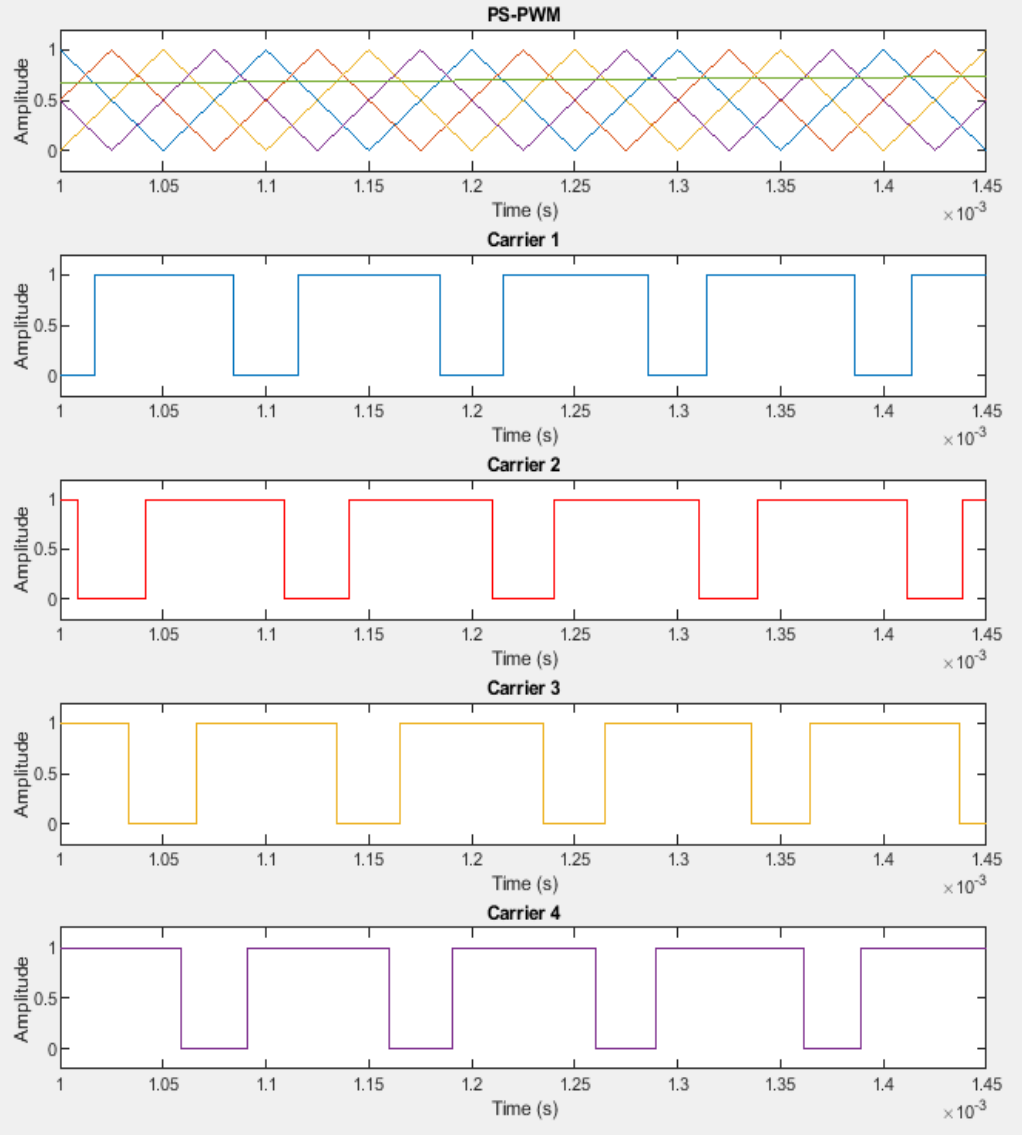


Figure 4-3. Phase-shifted pulse-width-modulation technique

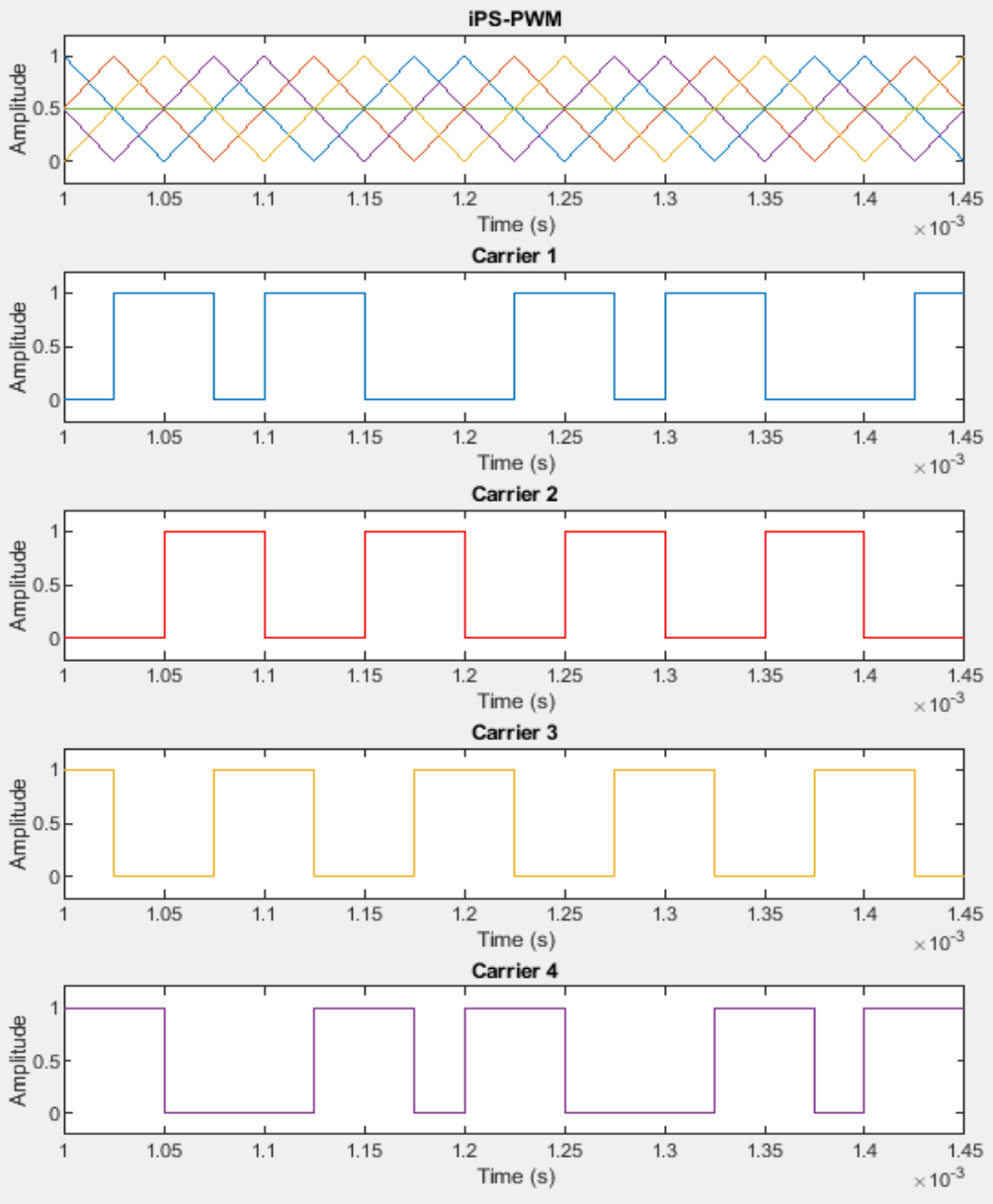


Figure 4-4. Improved phase-shifted pulse-width-modulation technique

PWM carrier waveforms and gate signals. The main difference in the carrier waveforms is the alternation of two carrier signals (Carriers 1 and 4) after half of the PWM period, which is two-times the PS-PWM period. The other two carrier signals (Carriers 2 and 3) maintain the triangular waveform.

4.3.1 Flying capacitor pre-charge

Pre-charging the flying capacitors has been a major concern when dealing with FCCs and is often considered the major drawback of the topology [8]. Mainly this is due to the requirement that the flying capacitors need to be fully charged before initiating operation in order to achieve efficient functionality, and thus, to avoid the need of an additional controller to initialize the capacitors balancing. The most common approach used in power converters to avoid high peak currents during the start-up procedure is the use of pre-charging resistors between the dc-bus and the dc link capacitor; after pre-charge, a switch that is in parallel with the resistor is closed to maintain normal operation [9]. In [9], it was demonstrated that with the PS-PWM and by increasing the dc-bus voltage slowly with a controlled ramp inrush currents are avoided without the need of a pre-charging circuit due to the non-linearities created by the clamping diodes in the switches. The presence of inrush currents in the start-up is shown in Figure 4-5 during pre-charge of the FCC without the use of a controlled ramp. Figure 4-6 presents different pre-charge scenarios using ideal switches, the PS-PWM and the iPS-PWM with a ramp time of 0.05 s and these modulation indexes:

a. iPS-PWM with $m_a = 0.9$
b. PS-PWM with $m_a = 0.9$
c. iPS-PWM with $m_a = 0.5$
d. PS-PWM with $m_a = 0.5$
e. iPS-PWM with $m_a = 0$
f. PS-PWM with $m_a = 0$

the 60 Ω load is connected to the FCC at $t = 0.3$ seconds by closing an ideal switch.

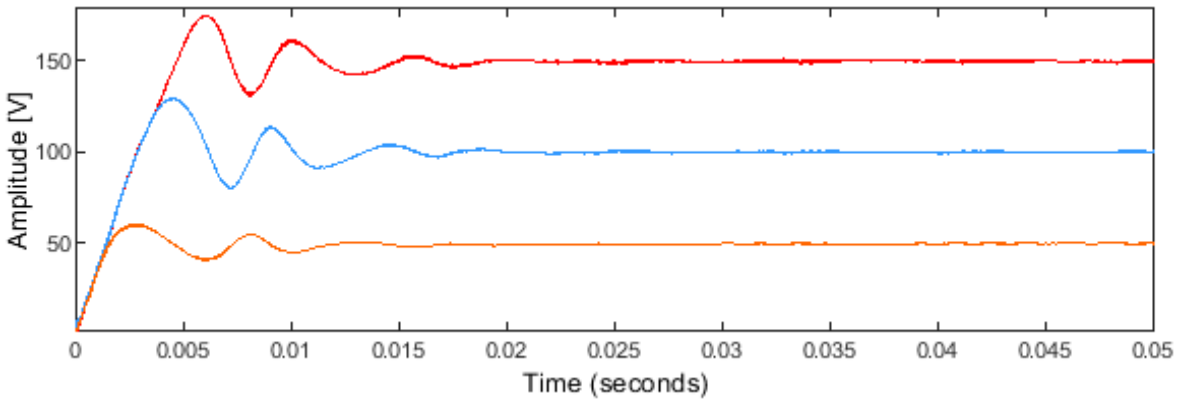


Figure 4-5. Flying capacitors FC3 (red), FC2 (blue) and FC1 (orange) voltage waveforms during pre-charge with PS-PWM and without the use of a controlled ramp for the dc-bus.

With the iPS-PWM, the flying capacitors are charged uniformly and a steady state is obtained approximately at 0.1 seconds. In contrast, the PS-PWM has a slow balancing problem with FC1 and FC3 due to their infinite common-mode time constant [7]. Figure 4-6(f) shows that flying capacitors could not be pre-charged with $m_a = 0$ because of the infinite time constant, and therefore capacitors FC1 and FC3 are always in anti-series connection. In [6], the analysis of a single-phase FCC voltage balance dynamics explains that as both capacitors have the same voltage unbalance, there is no effect on the output voltage and the self-balancing property cannot be obtained.

During normal operation (t > 0.3s), the flying capacitors are being charged and discharged rapidly depending on the switching state changes. Self-balancing voltage dynamics are dependent on many factors such as load parameters, high-frequency switching losses and hysteresis core losses [9]. As mentioned in section 4.3, the iPS-PWM uses consecutive switching states during each level, equal switches usage, and the same period at inverse switching states; thus from Figure 4-7(a) it is confirmed that voltage dynamics are improved, because the capacitor voltage charges and discharges uniformly when compared to optimal operation using the PS-PWM. Figure 4-7(b)

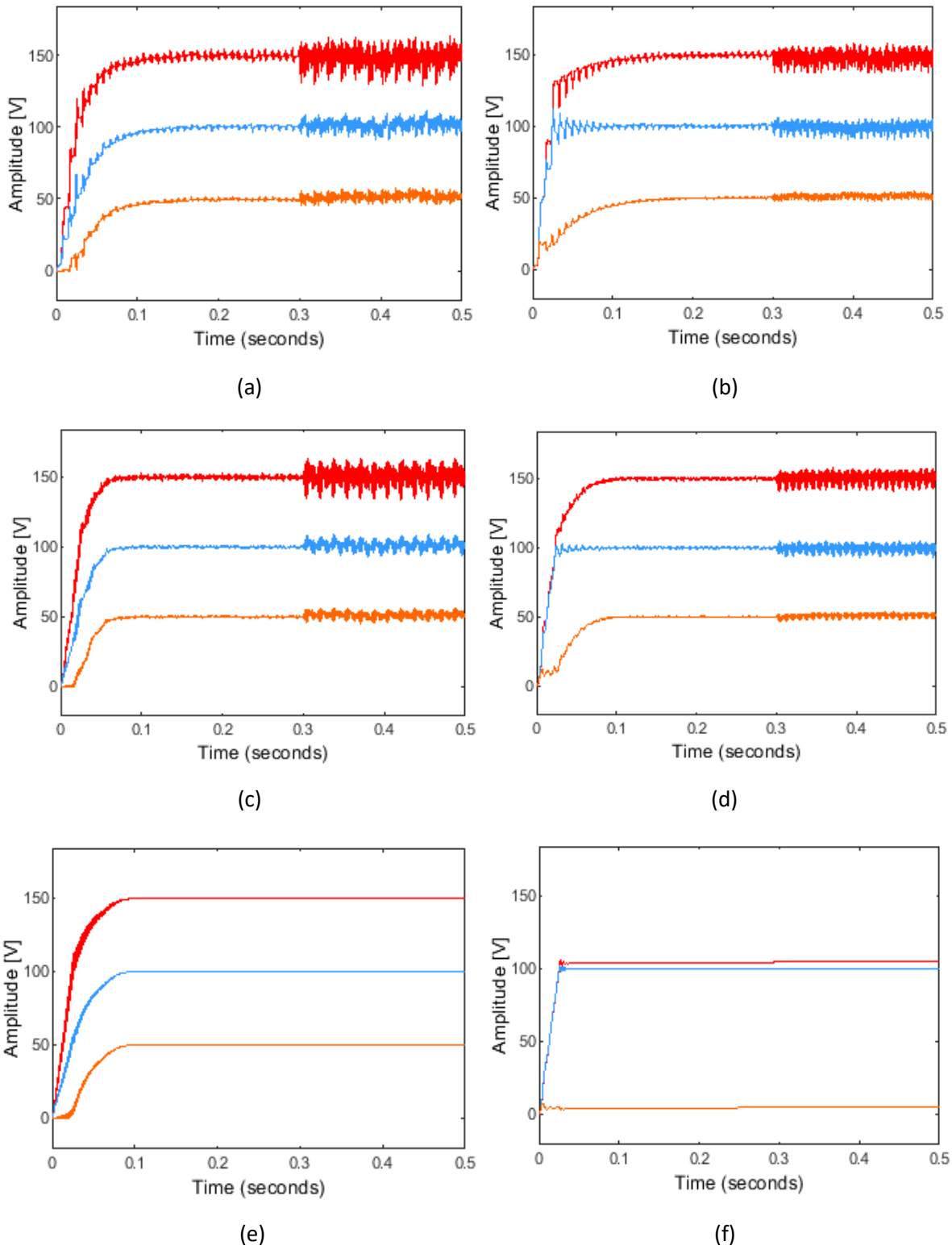
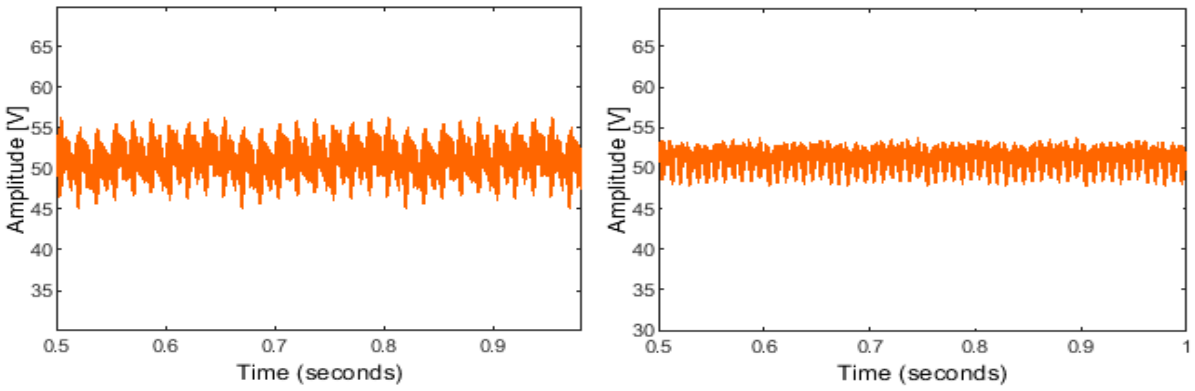


Figure 4-6. Flying capacitors FC3 (red), FC2 (blue) and FC1 (orange) voltage waveforms during pre-charge using PS-PWM (right) and iPS-PWM (left)



(a) (b)

Figure 4-7. Steady-state condition of the flying capacitor (FC1) voltage with a 60 Ω load connected using PS-PWM (right) and iPS-PWM (left)

shows that the capacitor voltage ripple is smaller but not uniform with the PS-PWM, and the converter efficiency is lower as more than one MOSFET is switched at the same time. In addition, the voltage ripple oscillations are stable because the same pattern is repeated with a longer simulation time.

Additional passive components known as balance boosters (BBs) are usually added to the converter in order to further improve balancing dynamics during the pre-charging phase [10]. External balance boosters (EBBs) provide a low-impedance path by placing a resistor in parallel with the filter inductor, while internal balance boosters (IBBs) offer better dynamics during flying capacitor pre-charging with the inclusion of a resistor in parallel with the switching devices as shown in Figure 4-8 [10]. 1 kΩ resistors where connected in parallel with each MOSFET and with all filter inductors. Simulations prove that both PWM schemes are now viable at all ranges of m_a and pre-charging of the flying capacitors is faster.

It can be concluded that after adding BBs there is not a significant difference between the use of the PS-PWM and the iPS-PWM during pre-charging, thus the PS-PWM will be the main

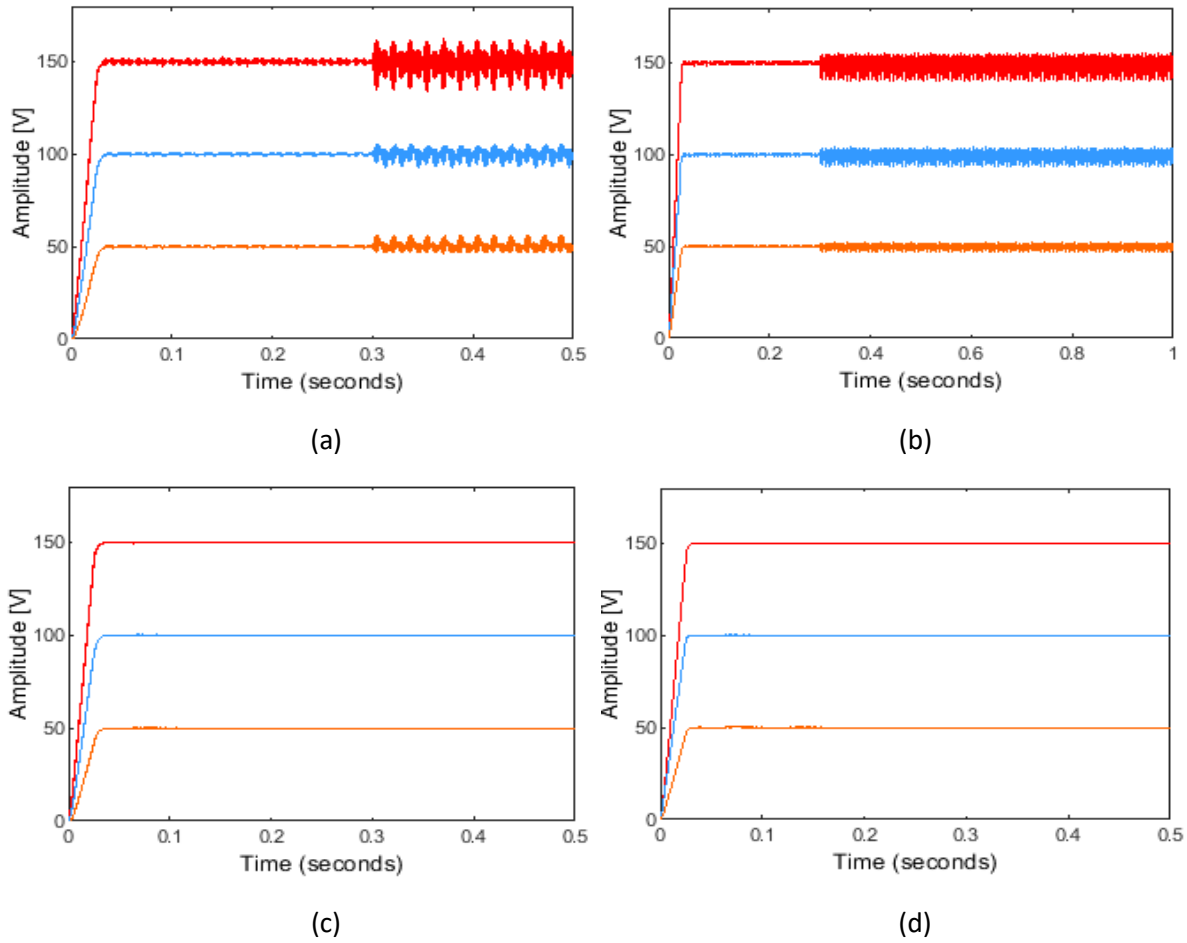


Figure 4-8. Flying capacitors FC3 (blue), FC2 (orange) and FC1 (yellow) voltage waveform during pre-charge using PS-PWM (right) and iPS-PWM (left) and balance boosters.

modulation technique during the experimental procedure as it is easier to implement in a DSP.

4.4 UCSC Simulations

After successfully modeling important characteristics of a single-phase FCC, the UCSC current control algorithm described in Chapter 3 was evaluated in three-phase models.

4.4.1 Controller tuning

First, the converter was implemented as a controlled voltage source using sinusoidal waveforms for the SOGI-FLL and the reference inverter current. Starting with the simplest case

helped with the controller parameters tuning and as a future reference to use during prototype testing. The PI compensator constant k_p and k_i can be determined using the method described in [11]. Assuming the compensator zero s to be

$$s = \frac{-k_i}{k_p} \tag{4-1}$$

and substituting into the open-loop transfer function G(s) from Figure 4.8 yields

$$G(s) = \frac{k_p}{Ls}\left(\frac{s + \frac{k_i}{k_p}}{s + \frac{R_{on}}{L_g + L_{inv}}}\right) \tag{4-2}$$

the open-loop transfer function of the controller takes the following form:

$$G(s) = \frac{k_p}{(L_g + L_{inv})s} \tag{4-3}$$

Now, the controller design can be rewritten as a first-order system with the following expression:

$$\frac{Y(s)}{X(s)} = \frac{1}{\tau_i s + 1} \tag{4-4}$$

where τ_i represents the integral time constant which is chosen depending on the expected bandwidth and the current-controller speed. Using equation (4-3) and the closed-loop transfer function of the block diagram from Figure 4-9, k_p is calculated as follows:

$$k_p = \frac{L_g + L_{inv}}{\tau_i} \tag{4-5}$$

Substituting into equation (4-2) k_i becomes:

$$k_i = \frac{R_{on}}{\tau_i} \tag{4-6}$$

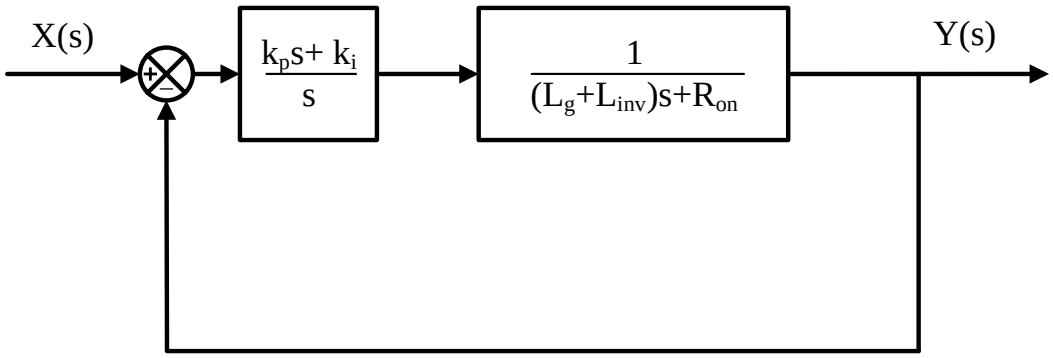


Figure 4-9. Simplified block diagram of the current-mode controller

The value of $\tau_i = 0.3\,ms$ was chosen after several simulations depending on the results of controller.

4.4.2 UCSC synchronization with the grid

In order to synchronize the UCSC with the grid, the output voltage of the converter had to increase rapidly to match the PCC voltage, creating an instantaneous high current during the start-up. These inrush currents that are generally much higher than the rated current of the system can activate the overcurrent protections of the power converter or will require oversize of the components to handle them. Lasting over a few milliseconds, the simple solution is to remove these high currents during the start-up procedure. In [12], a LCL filter model was implemented in parallel with the reference controller in order to synchronize the grid voltage v_g at the PCC with the UCSC output voltage v_{inv} before the connection is made. The LCL filter model from Figure 4-10 calculates the grid inductor current i_g using the superposition principle and the measurements from v_g and v_{inv}. The relationships between i_{g1} & v_g, and i_{g2} & v_{inv} are calculated using Figure 4-11 and are expressed as:

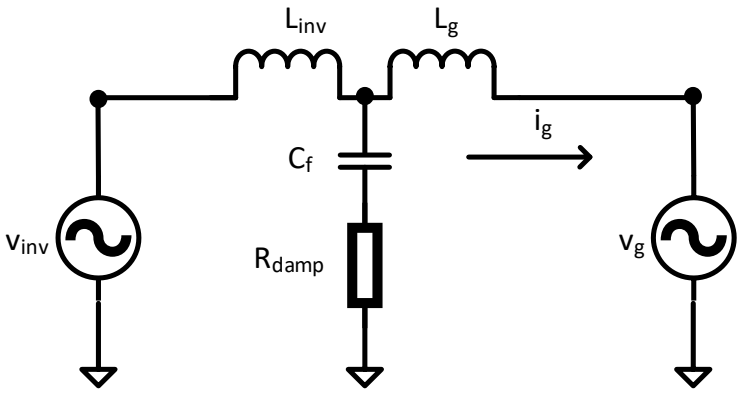


Figure 4-10. LCL filter model used for the UCSC synchronization with the grid

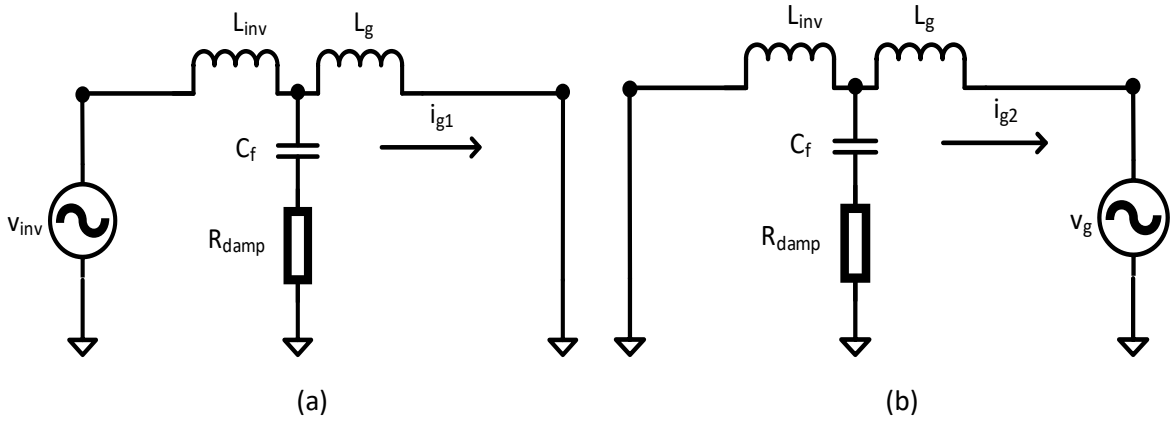


Figure 4-11. Superposition principle applied in the LCL filter model to calculate the transfer functions i_{g1} /v_{inv}, and i_{g2} / v_g

$$\frac{i_{g1}}{v_{inv}} = \frac{R_{damp}C_f s + 1}{L_{inv}L_g C_f s^3 + (L_{inv}+L_g)R_{damp}C_f s^2 + (L_{inv}+L_g)s} \tag{4-7}$$

$$\frac{i_{g2}}{v_g} = -\frac{L_{inv}C_f s^2 + R_{damp}C_f s + 1}{L_{inv}L_g C_f s^3 + (L_{inv}+L_g)R_{damp}C_f s^2 + (L_{inv}+L_g)s} \tag{4-8}$$

$$i_g = \mathrm{i_{g1}} + \mathrm{i_{g2}} \tag{4-9}$$

The error signal goes into the current controller; after i_g equals to zero, synchronization will not cause any inrush current in the system. Later, the current controller starts working normally as previously described.

4.4.3 Up-stream currents balancing and reactive power compensation

The UCSC connected to the grid was modeled using three load resistors and three voltage sources at $60\ V(line-to-line)$ to analyze the substation currents balancing capability. Figure 4-12 presents the inverter output currents, load currents, substation balanced currents and neutral current, respectively. From $t = 0.00\ s$ to $t = 0.07\ s$, the dc bus is increased with a controlled ramp, the flying capacitors are pre-charged and the synchronization procedure is initialized. An ideal switch is closed at $t = 0.07\ s$ and UCSC is connected to the grid. At $t = 0.18\ s$, the UCSC operates in current balancing mode. While the substation currents become balanced, the inverter currents increase depending on the amount of current needed at each phase; as well, the neutral current will decrease close to zero. Figure 4-13 shows the initial and the steady-state conditions of the system.

Reactive power compensation was modeled with the inclusion of three inductors in series with the load resistors, the simulations results are is illustrated in Figure 4-14. Similar to the previous case, the UCSC start-up procedure takes between $t = 0.00\ s$ and $t = 0.07\ s$. Reactive compensation mode starts at $t = 0.1\ s$ where the inverter inject currents to the grid in order to improve the power factor at the PCC. The UCSC is fully operational after $t = 0.18\ s$. Initial and steady-state conditions waveforms are presented in Figure 4-15. Figure 4-16 shows the flying capacitor self-balancing behavior without the use of an additional controller. The ripple voltage of the flying capacitors increase proportionally with the inverter currents, therefore at 0.3s when the neutral current has been reduced close to zero, the system is almost stable. After some seconds when the current have been balanced, the ripple voltage will oscillate uniformly (t > 0.5 s).

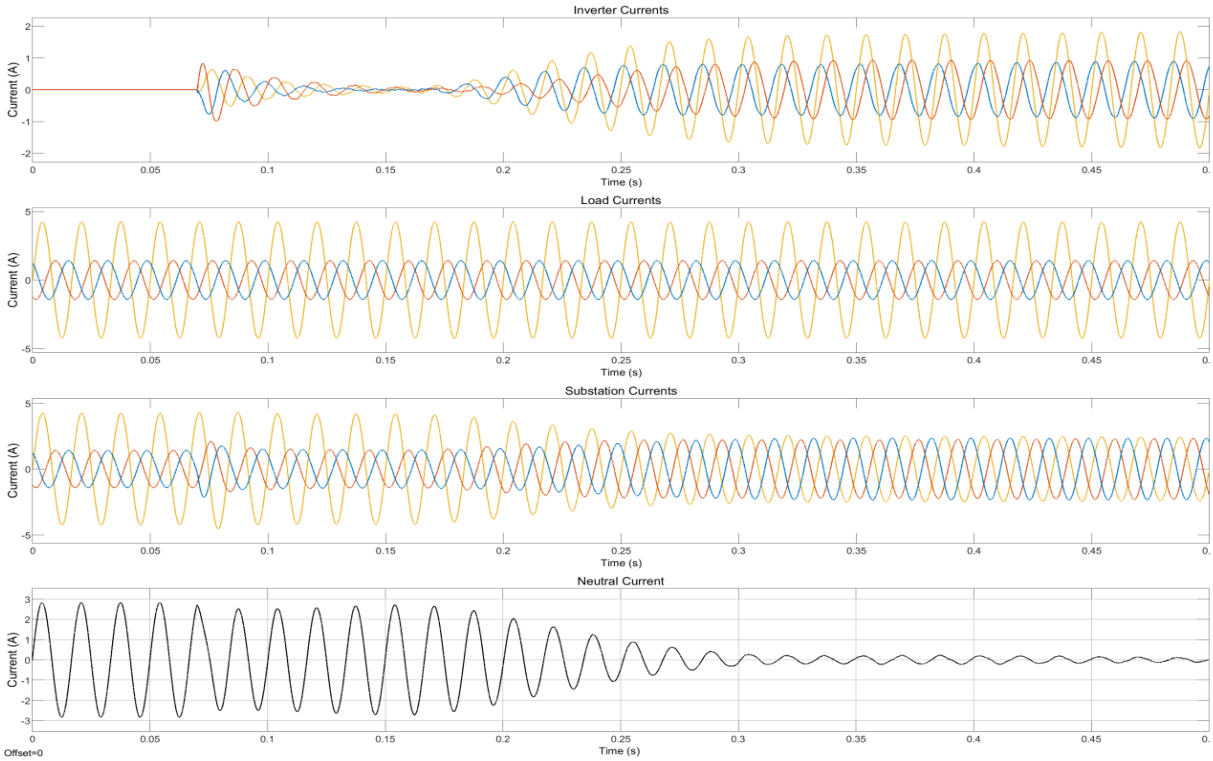


Figure 4-12. UCSC, load, substation and neutral current waveforms during up-stream currents balancing mode.

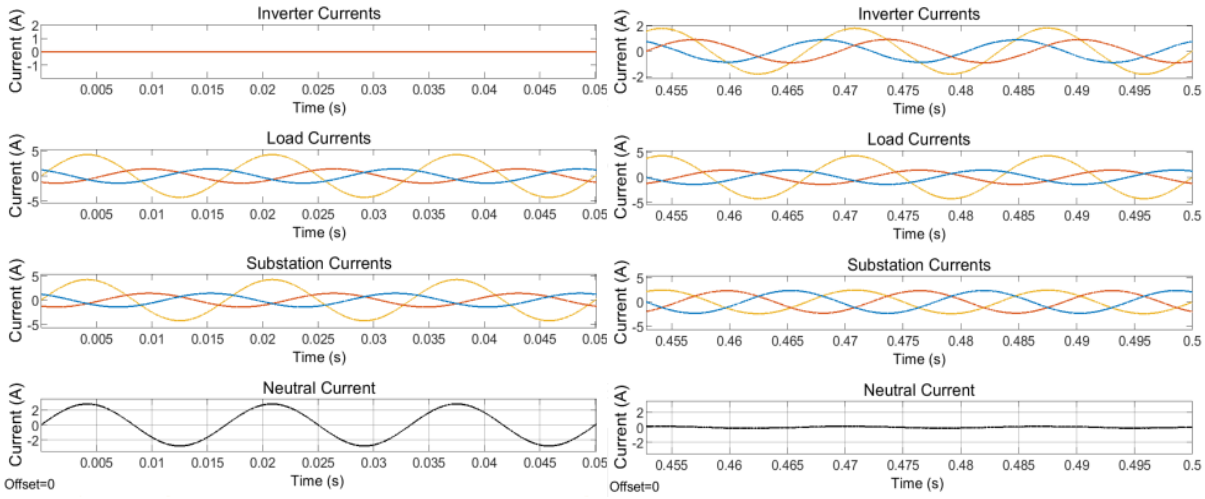


Figure 4-13. Initial and steady-state conditions during UCSC up-stream currents balancing mode

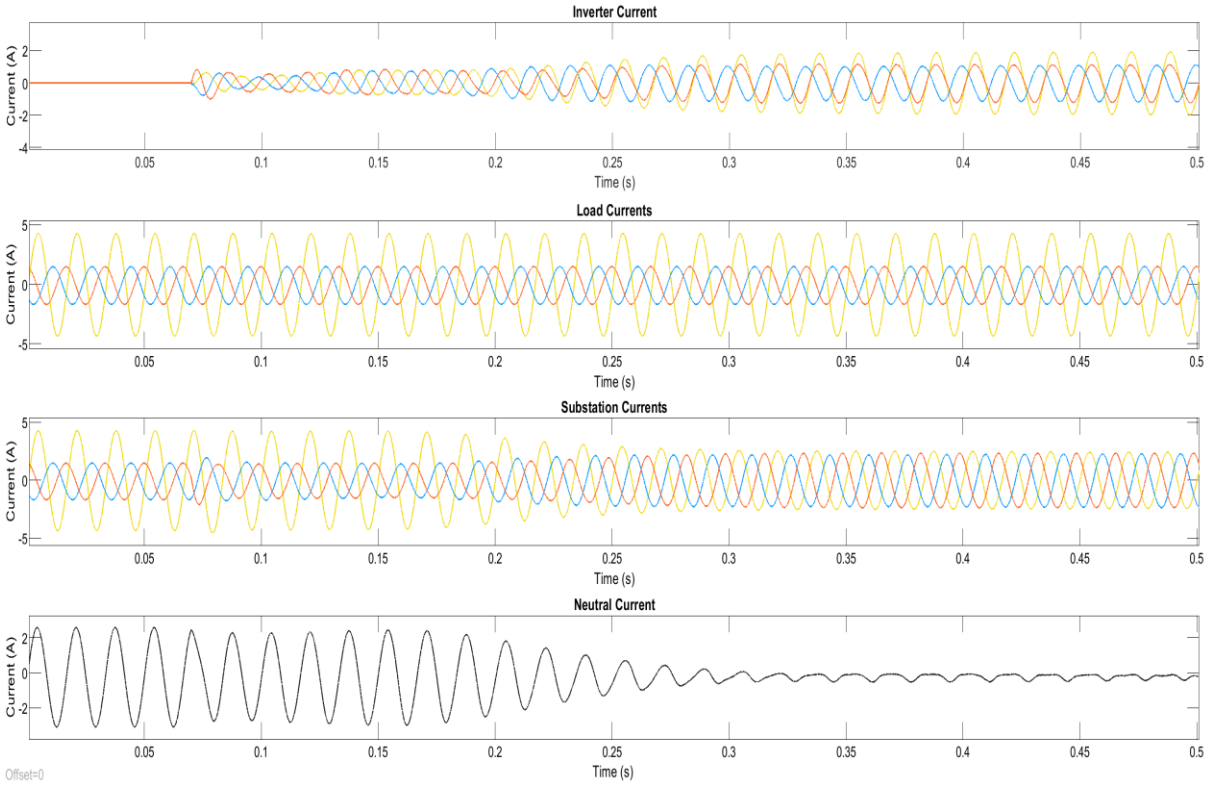


Figure 4-14. UCSC, load, substation and neutral current waveforms during reactive compensation and up-stream currents balancing modes

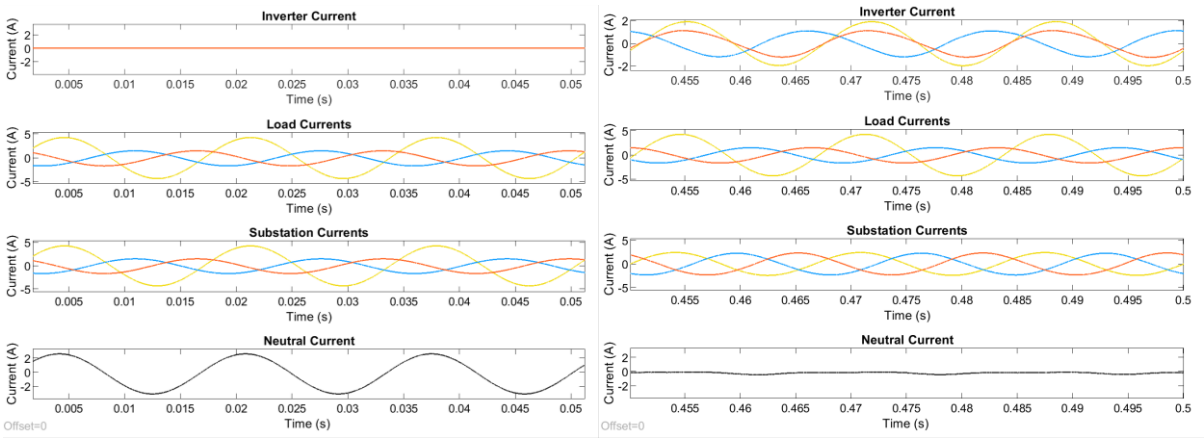


Figure 4-15. Initial and steady-state during UCSC reactive compensation and up-stream currents balancing modes

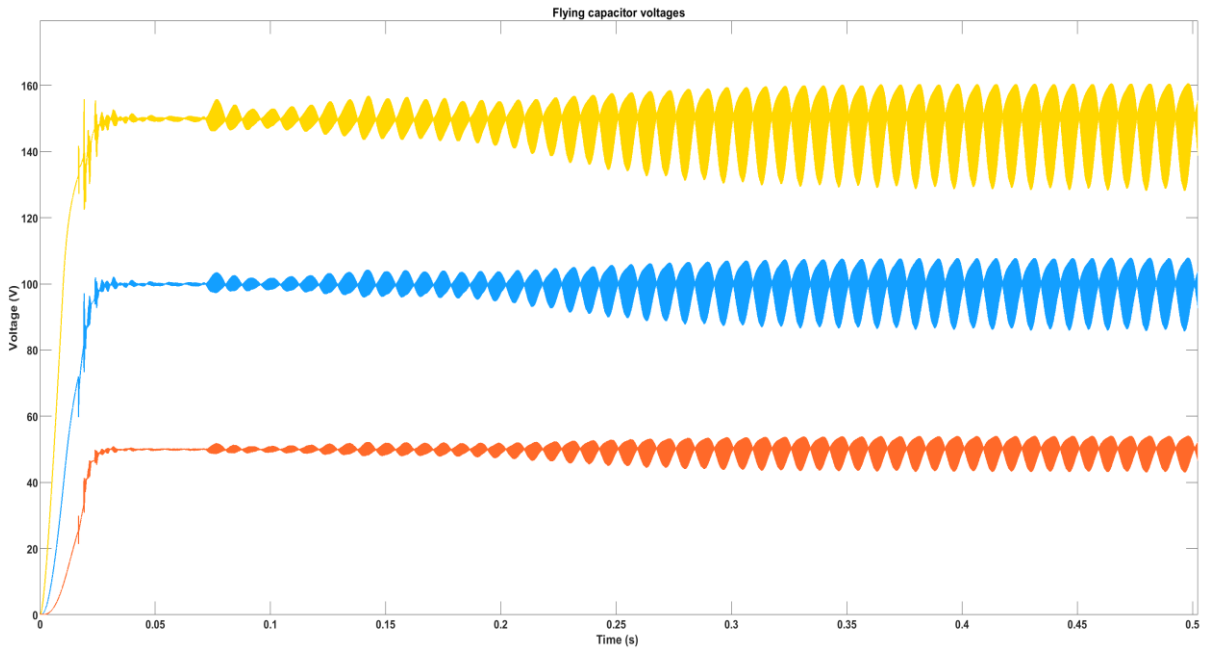


Figure 4-16. Flying capacitors FC3 (yellow), FC2 (blue) and FC1 (orange) during UCSC operation

4.5 Conclusions

In summary, the Tustin method has been selected to discretize structures like SOGI-FLL and PI compensators in order to develop more accurate simulations. After the inclusion of EBBs and IBBs, the PS-PWM have been confirmed as the main modulation technique for the project. Simulations results have confirmed the viability of the control algorithm and the selected UCSC parameters. The next steps are the prototype design, control implementation in a DSP and experimental results that will be addressed in the next chapter.

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CHAPTER 5

UCSC PROTOTYPE DESIGN AND IMPLEMENTATION

5.1 Introduction

This chapter will focus on the UCSC prototype design and the implementation of the control algorithm in a F28379D DSP. First, important considerations when designing a PCB such as component placement, PCB routing and grounding are mentioned because good PCB layout practices improve efficiency and reduce the overall PCB size. Gate drivers and sensors circuits need to be conditioned carefully to avoid the effect of parasitics and EMI noises; therefore, the schematic of each circuit is shown in detail. Thermal management of semiconductor devices can be addressed with natural or forced air flows. The heat sink size is calculated for natural air flow as temperature rise in the devices is not critical for the envisioned laboratory operating condition. In addition, this chapter will present the advantages of using the TMS320F28379D Dual-Core Delfino™ DSP from Texas Instruments and explain the method used to implement the ADC and EPWM modules in order to perform the UCSC control algorithm.

5.2 UCSC Prototype Design

5.2.1 PCB design

During the design process, significant effort is invested in the circuit schematic; thus, designers shall avoid poor layout practices in order to save time, money and to obtain better performance. Good layout practices should improve the integrated circuits (ICs) operations and allow the reduction of EMI. The PCB layout guideline presented in [1] has been used for this project and can be summarized in three sections:

a. Main power and DSP signal paths

b. Component placement and PCB routing

c. Ground planes and loops

The main power path includes the converter topology and LCL filter, while the DSP signal paths refers to the gate drivers and sensing circuits. It is important to design both circuits separately as they have different functions and may be rated differently. For higher currents and voltages, circuit layout needs to be considered critical as safety and operational requirements [2, 3] demand proper distances between traces to avoid flashover.

Components such as decoupling capacitors need to be placed as close as possible to IC pins in order to reduce high-frequency harmonics in the output waveforms or sudden voltage variations from the input signals. Traces between passive components shall be kept short, with the required width, and avoid the use of PCB vias through different layers [1]. Poor component placement contributes to the appearance of parasitic inductances and capacitances in the prototype. Parasitic inductances are an unwanted effect mostly caused by trace orientations or conductors self-inductances [4]. Parasitic capacitances are originated due to the overlap of traces between layers or two parallel traces very close to each other on the same layer. Both types of parasitics can increase the switching losses and thus impact directly the converter efficiency [5, 6].

Ground planes are usually located on the layer under the signal paths because, as a return path, it will produce field cancellation and reduction of parasitic inductances [1]. They simplify the layout task: as the ground now could be accessed from almost every point and may help to reduce the size of the PCB. Also, reduction of EMI is possible as the ground plane links to noisy power traces above it, providing some distributed capacitance similar to the decoupling capacitors function [7]. Ground loops need to be avoided when designing a PCB, as differences in the ground potential affect the correct operation of the main circuit. They are usually originated when devices

Table 5-1. IRL640A N-channel logic MOSFET main parameters

Drain-to-Source Voltage (V_{DS})	200 V
Gate-to-Source Voltage (V_{GS})	±20 V
Continuous Drain Current (I_D)	18 A
Static Drain-Source On-State Resistance ($R_{DS(on)}$)	0.18 Ω
Total Power Dissipation (P_D)	110 W
Operating Junction Temperature Range (T_J)	-55 to 150 ºC
Junction-to-Case Thermal Resistance ($R_{\theta JC}$)	1.14 ºC/W
Case-to-Sink Thermal Resistance ($R_{\theta CS}$)	0.5 ºC/W
Rise Time (t_r)	8 ns
Fall Time (t_f)	15 ns

are connected together by long cables and share the same ground point via different paths. The inclusion of a ground plane in the bottom layer partially solves this problem [1].

5.2.2 Gate driver circuit design

As previously mentioned, the semiconductor device selected for the UCSC application is the IRL640A N-Channel Logic MOSFET produced by Fairchild Semiconductor whose main parameters are listed in Table 5-1 [8]. The 0.6 A I_{OLpeak} HCPL-3120 gate driver optocoupler from Broadcom Inc. is used to drive the power switching modules. This IC provides the required isolation between the main power circuit and DSP signal, and eliminates the need for negative gate drive due to the 1V maximum low-level voltage (V_{OL}) [9]. According to [9], the minimum gate driver resistor R_g is calculated as:

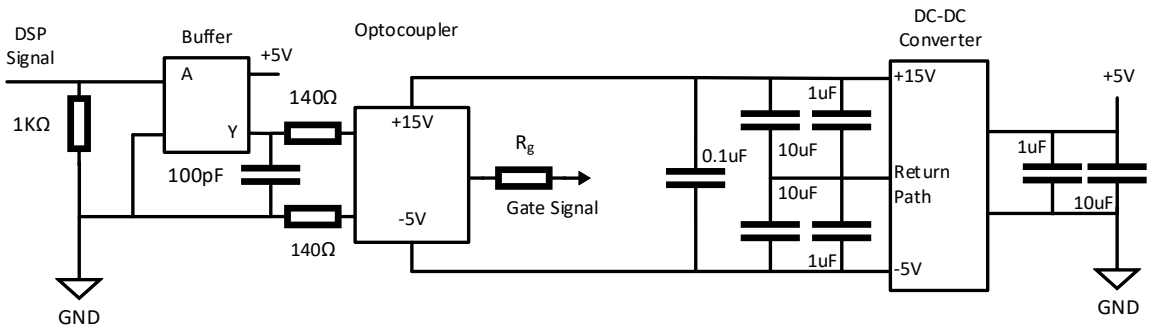


Figure 5-1. Gate driver schematic circuit

$$R_g = \frac{V_{CC} - V_{EE} + V_{OL}}{I_{OLpeak}} = 30\ \Omega \tag{5-1}$$

where V_{CC} and V_{EE} are chosen to be +15 V and -5V, respectively, based on the V_{DS} rating of the MOSFET. Each MOSFET has its own gate driver circuit; however, the control side of all gate drivers are powered by the same +5V power supply that shares the DSP ground. In order to power each power-source of the gate driver optocoupler, MGJ2D051505SC isolated +15V/-5V dc-dc converters are utilized. Finally, the input DSP signals are passed through SN74LVC1G17 Single Schmitt-Trigger Buffer from Texas Instruments because the optocoupler requires a limited current of 16 mA in its input [10]. The complete gate driver circuit is shown in Figure 5-1.

5.2.3 PCB layout

The PCB was designed using Cadence Allegro PCB Designer® with four layers (TOP, MIDTOP, MIDBOT and BOT) to reduce the overall size of the prototype and avoid the use of PCB vias, which increase the effect of parasitics. Figure 5-2 illustrates TOP (green) and MIDBOT (purple) layers, eight gate drivers circuitry cells and the flying-capacitor module in the middle. The flying-capacitors board is connected perpendicular to the main board in order to reduce space and to allow the inclusion of the voltage sensor circuits as shown in Figure 5-3. TOP layer was used for the DSP signal traces, the gate driver return path and the parallel path

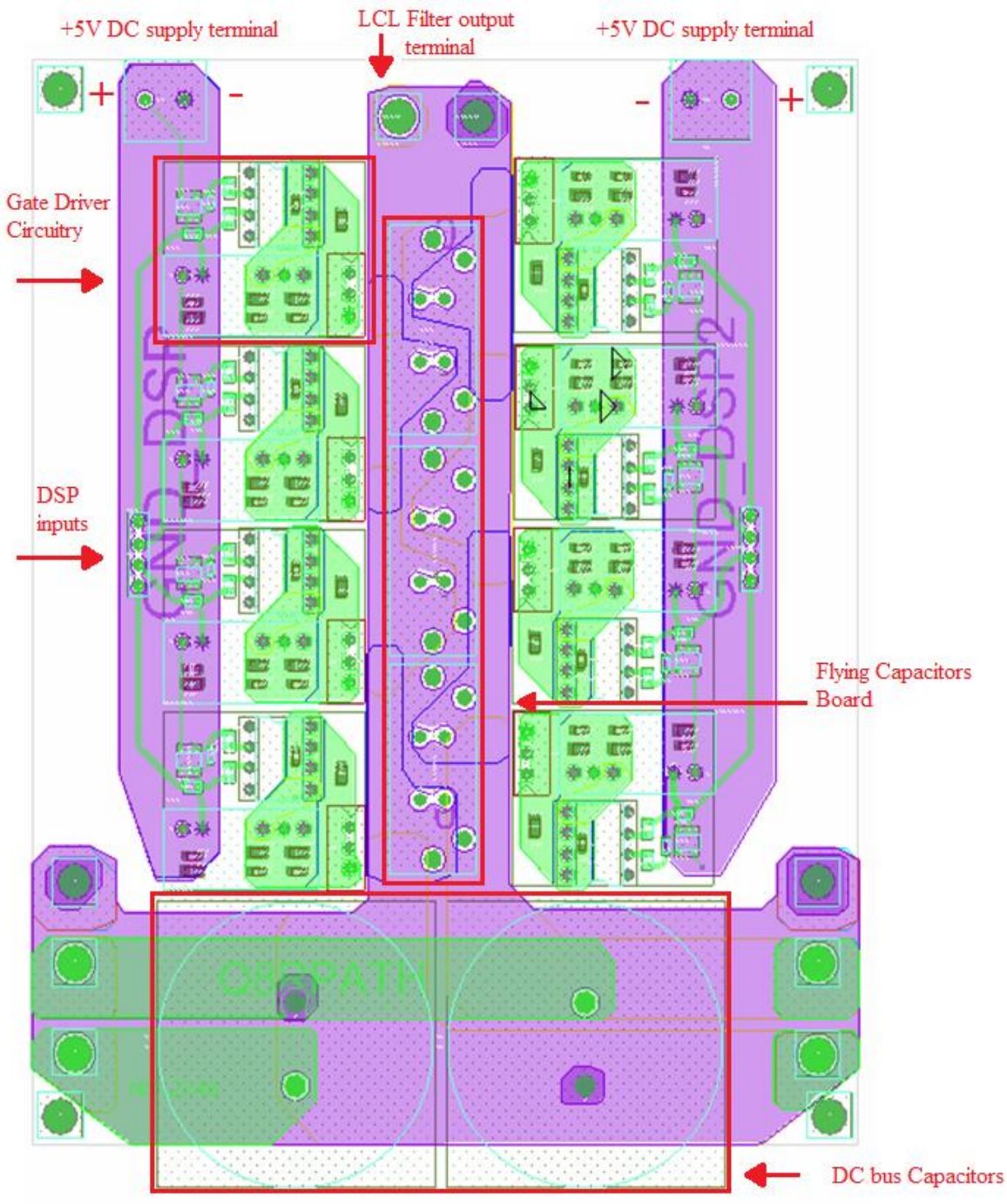


Figure 5-2. PCB layout of the TOP (green) and MIDBOT (purple) layers

between dc capacitors, while the MIDBOT is used for the main ground plane and the DSP ground plane. The three-phase system uses three identical single-phase boards that share the same dc-bus voltage by a parallel connection of the dc-link capacitors. Main power traces were added in BOT

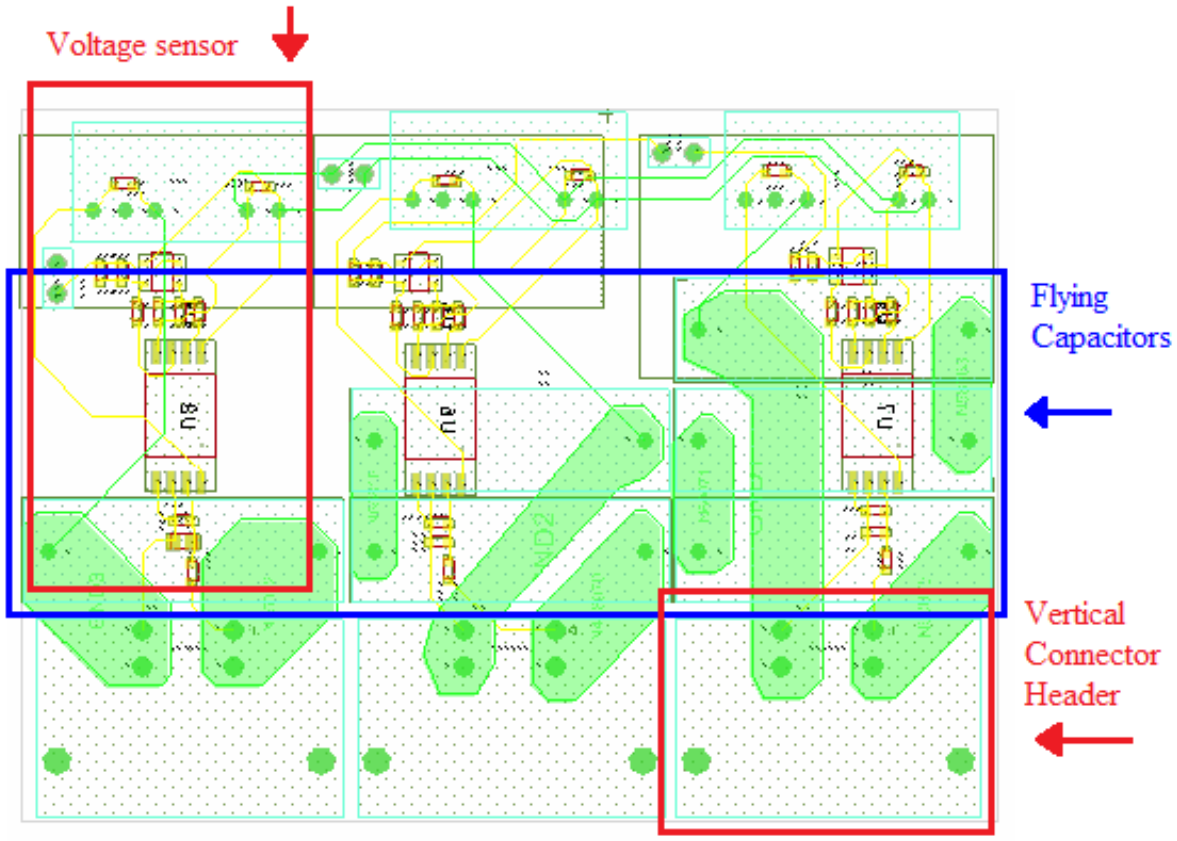


Figure 5-3. Flying-capacitors PCB

(yellow) and MIDTOP (blue) layers as shown in Figure 5-4. In addition, the MIDTOP layer includes the +5V power supply and the V_{CC} voltage that powers the optocoupler.

Component placement was chosen based on the schematic diagram from Figure 4-1, where the FCC n-level could be easily expanded if necessary. It is accomplished by adding extra flying capacitor cells before the LCL filter. This type of layout gives the shortest connection between gate drivers and MOSFETs, which helps to reduce switching losses and improve converter efficiency.

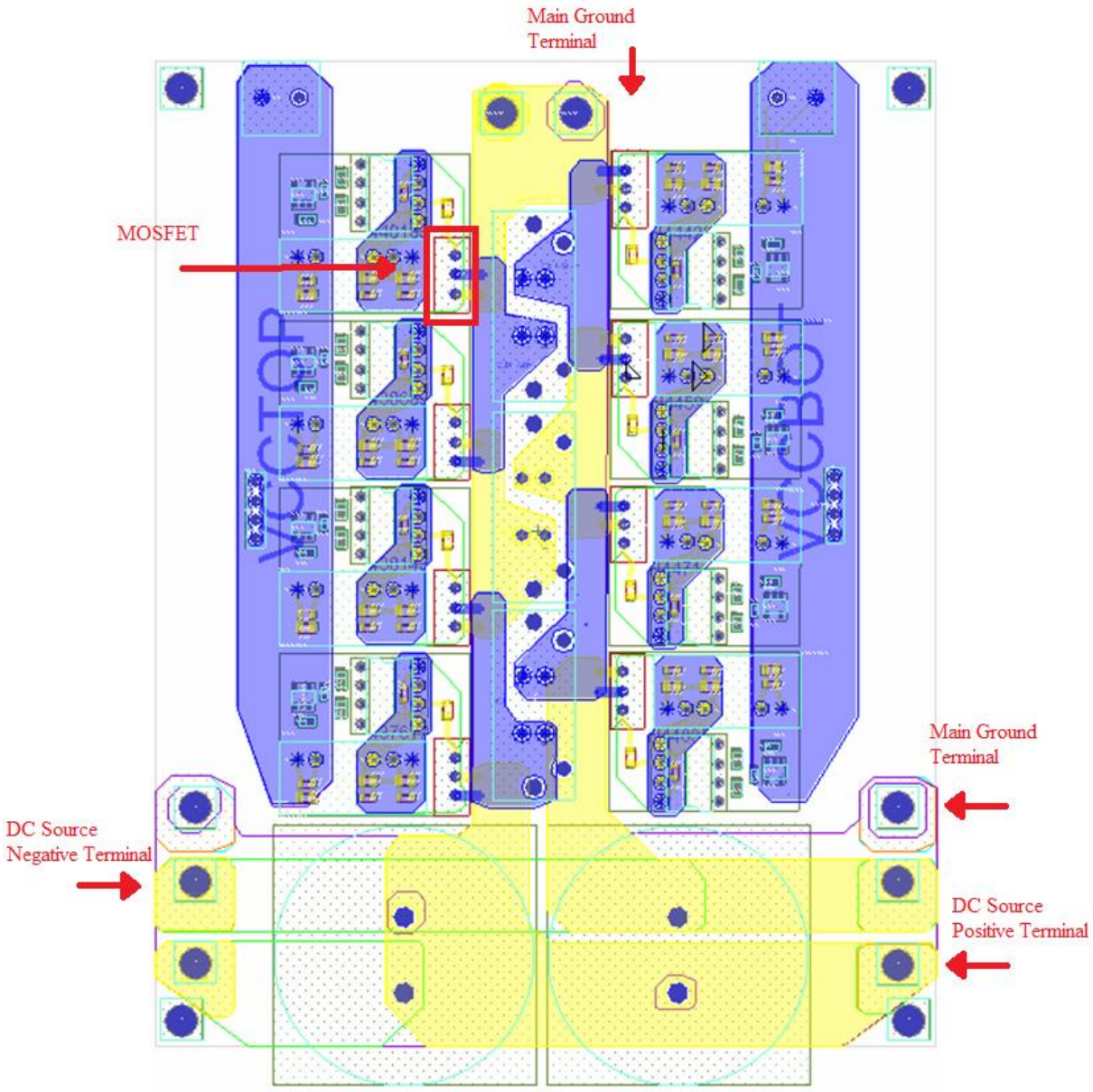


Figure 5-4. PCB layout of the BOT (yellow) and MIDTOP (blue) layers

5.2.4 Sensor and measurement circuits

As described in the control algorithm section in Chapter 3, each phase voltage measurement at the PCC is used in the SOGI-FLL algorithm to determine the phase angle. The average of the load currents along with the substation and inverter currents set the reference for the current controller. Furthermore, the flying-capacitor and dc-link capacitor voltages are

measured to analyze the self-balancing property. Therefore, several current and voltage signals need to be sensed with accurate circuits to ensure correct operation of the system.

Even though different points in the system need to be measured, the same current and voltage sensing circuits can be employed for all cases. A low-offset linear Hall current sensor ACS724 from Allegro Microsystems was selected to measure the currents because it offers high precision, common-mode field rejection, high-bandwidth and the output conversion into a proportional voltage with 2.5 V offset that can be easily sent to the DSP [11]. The current sensing circuit uses a voltage divider to scale down the maximum rated 5 V measured signal into a proportional 3 V signal, and an operational amplifier OPA322 from Texas Instruments in order to accommodate the signal for the DSP ADC. The schematic diagram of the isolated current sensors circuit is presented in Figure 5-5.

The voltage sensing circuit scales down the input signal into a proportional 2 V signal with a voltage divider and then uses the optically-isolated voltage sensor HCPL-7840 from Avago Technologies. This IC provides high accuracy, stability and linearity under extreme noise conditions, and produces a differential voltage at the output [12]. Similar to the current sensing circuit, the measured signal is converted into a single-ended signal by an operational amplifier. In this case, the differential signal does not have an offset, so the differential operation amplifier from Figure 5-6(a) is modified to add a 1.5 V offset to the single-ended signal that will connect to the ADC. The output voltage V_o of the differential amplifier is expressed as [13]:

$$V_o = GV_{in} + V_{bias} \tag{5-2}$$

and

$$V_{in} = V_{out+} - V_{out-} \tag{5-3}$$

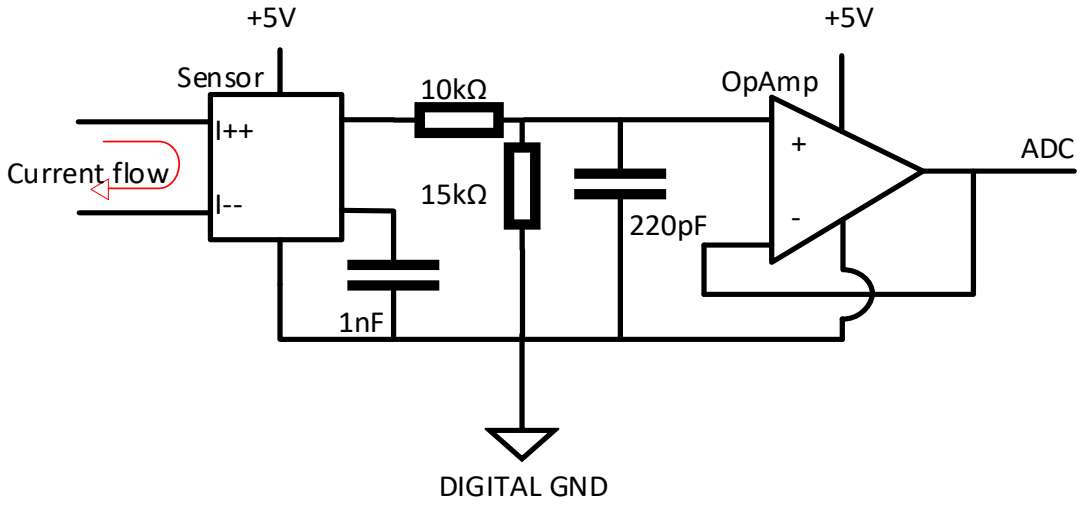


Figure 5-5. Schematic diagram of the isolated current sensor circuit

$$G = \frac{R_2}{R_1} \tag{5-4}$$

$$R_2 = \frac{R_4 R_3}{R_4 + R_3} \tag{5-5}$$

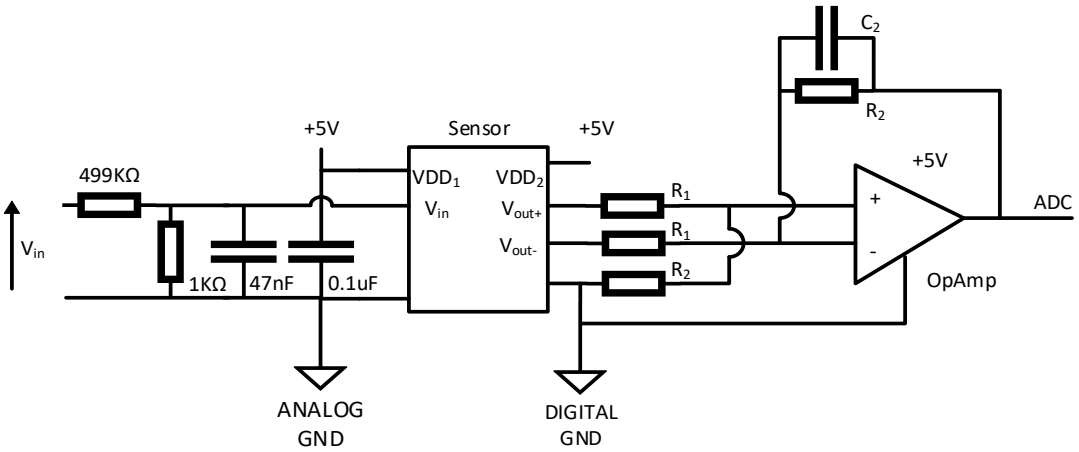
$$V_{bias} = \frac{R_4}{R_4 + R_3} V_s \tag{5-6}$$

where G refers to the gain of the amplifier, V_i the input voltage, V_{bias} the voltage offset. The circuit is modified to the one shown in Figure 5-6(b) in order to insert an offset to the amplifier output. Resistors $R_1$and R_2 were chosen to be 10 kΩ while V_s uses the +5 V supply voltage, then:

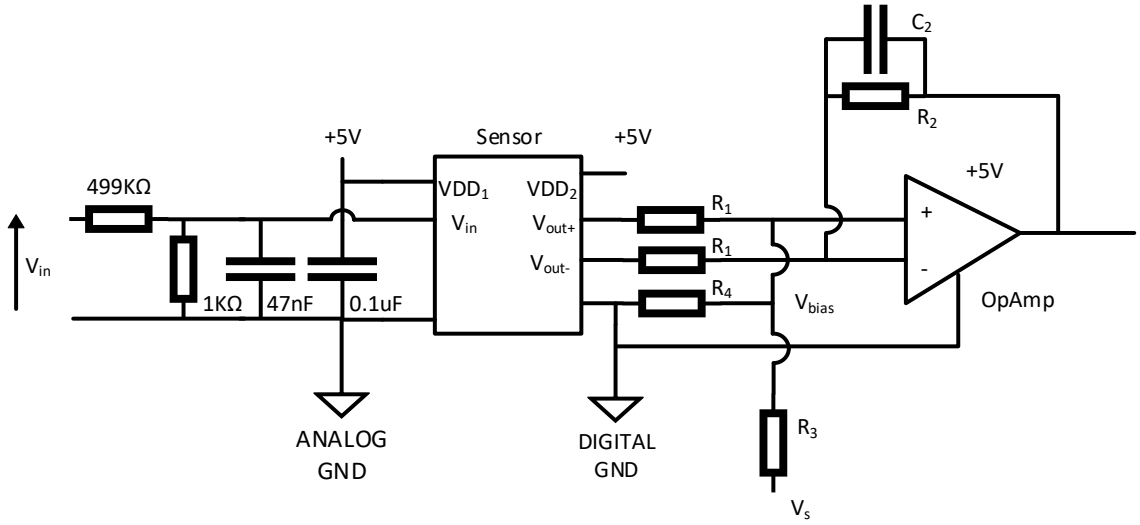
$$R_3 = 33.3\ k\Omega \tag{5-7}$$

$$R_4 = 14.3\ k\Omega \tag{5-8}$$

$$V_o = V_{in} + 1.5\ V \tag{5-9}$$



(a)



(b)

Figure 5-6. Schematic diagrams of the isolated voltage sensor circuit with and without dc offset

For the sake of avoiding the effect of undesired parasitics inductances between the sensing circuits and the ADC input and to filter potential EMI noises, RC filters with a high cut-off frequency were placed next to each ADC pins [16]. Using a midpoint of 2047 bits, the filtered ADC input signal presents a negative offset as visible in Figure 5-7; thus, the adjustment of the midpoints for each ADC pin is required.

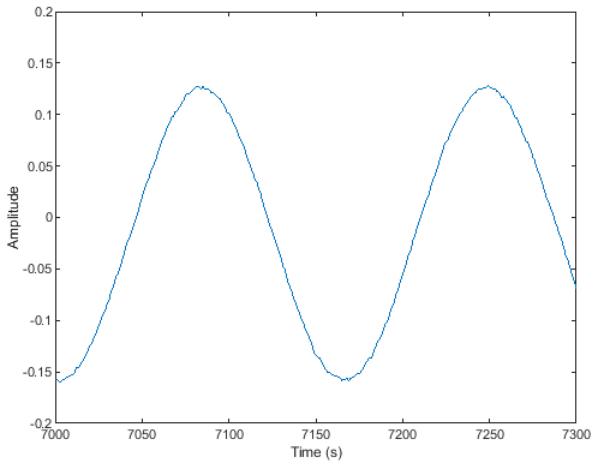


Figure 5-7. Load current measurement in the ADC module.

5.2.5 MOSFET heat sink design

The total power dissipation P_{TOT} of a MOSFET is given by the sum of the conduction P_{on} and commutation losses P_{sw} that impact proportionally in the overall temperature rise of the semiconductor device [4]. In order to mitigate this problem, thermal pads and heat sinks are included for power dissipation. The sink-to-ambient thermal resistance $R_{\theta SA}$ gives the maximum value for the heat sink sizing and is calculated as follows [14]:

$$R_{\theta SA} = \frac{T_J - T_a}{P_{TOT}} - R_{\theta JC} - R_{\theta CS} \tag{5-10}$$

and

$$P_{TOT} = P_{on} + P_{sw} \tag{5-11}$$

$$P_{on} = R_{DS(on)} {I_{LOAD}}^2 D \tag{5-12}$$

$$P_{sw} = V_{LOAD} I_{LOAD} f_{sw} (t_r + t_f) \tag{5-13}$$

If $R_{\theta SA}$ gives a negative value then the switching frequency or the ambient temperature must be decreased, if the negative sign remains then the semiconductor devices needs to be changed. Using the parameters from Table 5-1 and equations (5-10), (5-11), (5-12) and (5-13): the sink-to-ambient thermal resistance $R_{\theta SA}$ becomes $23.9\,^{o}C/W$ and the Channel 5700 AAVID Boyd Corporation heat sink from [15] is selected.

5.3 Implementation of the Control Algorithm in a F28379D DSP

As mentioned previously, DSPs modules are widely used for real-time control applications; therefore, the TMS320F28379D Dual-Core Delfino™ DSP from Texas Instruments has been selected for the UCSC 5-level FCC project. Although, previous research work has chosen the TMS320F28335 Delfino™ DSP [16, 17], the decision to look for a better DSP with improved characteristics was made based on several drawbacks that limited the implementation of the control algorithm described in Chapter 3. The main issue with the TMS320F28335 Delfino™ DSP is the lack of available PWM channels; in consequence, more than one control card is required. Even though, communication between F28335 DSPs is possible through serial communication interphase (SCI) or with the "Master/Slave" module: implementation of auxiliary modes, like overcurrent protection, and the debugging process become difficult and highly inefficient. A comparison between both C2000 Delfino™ DSP is presented in Table 5-2 [18]. TMS320F28379D Dual-Core Delfino™ DSP provides many new features such as:

a. Higher speed up to 200 MHz per CPU.
b. Reduction of system latency with the addition of a Trigonometric Math Unit (TMU) accelerator for faster execution of common trigonometric math operations
c. Expanded Flash and RAM memory
d. 24 PWM channels as required for the three-phase 5-level FCC

Table 5-2. C2000 Delfino™ DSP characteristics

	TMS320F28379D	**TMS320F28335**
Speed (MHz)	200	150
FPU	Yes	Yes
TMU accelerator	Yes	No
Flash (KB)	1024	512
RAM (KB)	204	68
PWM channels	24	18
Timers	24	16
12-bit ADC channels	24	12
16-bit ADC channels	12	0
GPIO pins	169	88

e. Increased number of timers, ADC channels and general-purpose input/output (GPIO) pins.

Fast processes (such as the current controller, overcurrent protection checking and PWM disable) use a designed flag bit known as ‘ccbit’ in the UCSC control algorithm. This ‘ccbit’ is now triggered by the ADCA1 interrupt instead of the CPU timer interrupt used in [16] in order to make sure conversions are completed before the results are read.

5.3.1 Analog-to-digital converter

The ADC module is used to convert the real-time measurements into series of discrete samples. Each module consists of a single sample-and-hold circuit that allows simultaneous

sampling or independent operation of multiple ADCs. To configure the ADC module, the ADC clock is pre-scaled by a factor of the system clock (SYSCLK) to generate the acquisition window. Then, the 12-bit or 16-bit resolution is chosen depending on the desired acquisition window to determine the quantization range when converting into digital values. 12-bit ADC resolution allows analog inputs from 0 V to 3 V and a digital output of 4095. The configuration process is shown in Appendix A.

The ACQPS field, that controls the sampling switch duration when the analog measurement is being taken, is defined during the initialization and can be calculated using the following expression [19]:

$$ACQPS = (T_{S+H})(SYSCLK) - 1 \tag{5-14}$$

where T_{S+H} represents the time to charge the sample and hold the ADC signal in the capacitor.

Furthermore, start-of-conversions (SOCs) are used for triggering and conversion of a single ADC channel. It is possible to configure multiple SOCs for the same trigger, channel, or acquisition window. The trigger operators available in the F28379D DSP are:

a. CPU Timers
b. GPIOs
c. ePWM channels

Table 5-3 presents the measured signals with their corresponding ADC input channels.

5.3.2 Enhanced pulse width modulator

The enhanced pulse-width modulator (ePWM) peripheral is used to implement the PWM algorithm described in previous chapters with minimal software intervention [19]. Each PWM

Table 5-3. ADC input channels with their corresponding pin and measured signal

ADC Input Channel	Pin	Measurement
ADCINA0	09	Phase A inverter current
ADCINA1	11	Phase B inverter current
ADCINA2	15	Phase C inverter current
ADCINA3	17	Phase A Load current
ADCINA4	23	Phase B Load current
ADCINA5	25	Phase C Load current
ADCINB0	12	Phase A Substation voltage
ADCINB1	14	Phase B Substation voltage
ADCINB2	18	Phase C Substation voltage

module contains two PWM output channels: ePWMxA and ePWMxB that are usually configured in dual-edge asymmetric operation or active-high complementary mode. All modules can be synchronized together using the PWM timer-base period (TBPRD) and the master module in order to allow operation as a singular system. An in-built time-based counter is used to emulate the symmetrical triangular carrier waveforms of the PS-PWM. “Up-down count” mode is chosen because “up” or “down count” modes create asymmetrical sawtooths carrier waveforms not suitable for the UCSC application [16]. The F28379D DSP has 24 PWM channels that are accessed through the GPIOs peripherals presented in Table 5-4.

Some changes were made to the original PWM code from [16] looking to simplify the algorithm and to include improved features. First, the timer period is calculated based on the F28379D DSP clock frequency of 200 MHz and the following equation:

Table 5-4. EPWM channels with their corresponding GPIO and dock station pin.

EPWM Channel	GPIO	Pin	EPWM Channel	GPIO	Pin
EPWM1A	GPIO0	49	EPWM7A	GPIO12	61
EPWM1B	GPIO1	51	EPWM7B	GPIO13	63
EPWM2A	GPIO2	50	EPWM8A	GPIO14	62
EPWM2B	GPIO3	52	EPWM8B	GPIO15	64
EPWM3A	GPIO4	53	EPWM9A	GPIO16	65
EPWM3B	GPIO5	55	EPWM9B	GPIO17	67
EPWM4A	GPIO6	54	EPWM10A	GPIO18	66
EPWM4B	GPIO7	56	EPWM10B	GPIO19	68
EPWM5A	GPIO8	57	EPWM11A	GPIO20	69
EPWM5B	GPIO9	59	EPWM11B	GPIO21	71
EPWM6A	GPIO10	58	EPWM12A	GPIO22	70
EPWM6B	GPIO11	60	EPWM12B	GPIO23	72

$$TBPRD = \frac{1}{2}\left(\frac{TBCLK}{f_{sw}}\right) = \frac{1}{2}\left(\frac{200\ MHz}{10\ KHz}\right) = 10000\ clock\ cycles \qquad (5\text{-}15)$$

PS-PWM modulation technique requires a phase shift of 90º between carrier waveforms; this is accomplished with the use of TBPHS and PHSDIR registers that produce a phase shift in the ePWM counter register. The combinations written in these registers that generate the carrier triangular waveforms for a three-phase FCC are shown in Table 5-5. DSP ADC start of conversion (SOC) signals are used to trigger the events instead of the CPU timer interrupts, these signals indicate when the ADC will begin sampling the input channels. For instance, ePWMxA triggers

Table 5-5. EPWM module configuration to generate a PS-PWM algorithm

EPWM Channel	Master	TBPHS	PHSDIR
EPWM1	Yes	0	UP
EPWM2	No	5000	DOWN
EPWM3	No	10000	DOWN
EPWM4	No	5000	UP
EPWM5	No	0	UP
EPWM6	No	5000	DOWN
EPWM7	No	10000	DOWN
EPWM8	No	5000	UP
EPWM9	No	0	UP
EPWM10	No	5000	DOWN
EPWM11	No	10000	DOWN
EPWM12	No	5000	UP

the SOC when the time-based counter reaches TBPRD, while ePWMxB will trigger the SOC when counter reaches zero. Finally, the dead-band sub-modules are initialized to control the falling- and rising-edge delay times between gate signal transitions.

5.4 Conclusions

In summary, the most important points when designing a PCB were addressed in this chapter. Four layers are used in the PCB to connect the gate drivers through the MOSFETs with the main power path; however, these circuits are isolated from each other. Moreover, the sensing

and measurement circuits used isolated sensors and operational amplifiers to transform the input signal into a single-ended signal suitable for the DSP ADC. The implementation code of the UCSC control algorithm in the F28379D DSP was presented in Appendix A. Initialization and configuration of the ADC and EPWM modules allowed improvements in the converter efficiency and avoided the use of more than one DSP control card. Finally, the prototype system testing and results discussion will be presented in Chapter 6.

5.5 References

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CHAPTER 6

UCSC PROTOTYPE EXPERIMENTAL RESULTS

6.1 Introduction

The experimental results of the UCSC prototype will be analyzed in this chapter. Three different tests will be conducted similar to those made during the simulations shown in Chapter 4. First, a single-phase FCC prototype will be tested using a resistive load to ensure correct operation of the converter, gate driver functionality and flying-capacitor pre-charge. Secondly, the system will be tested with a closed-loop controller to behave as a controlled voltage source. This step is going to be implemented to ensure that the sensing and measurement circuits are accurate and the DSP code setup was correctly implemented. Finally, the UCSC control algorithm will be tested in the three-phase prototype and the experimental results presented and evaluated.

6.2 Experimental Setup

The UCSC prototype presented in Fig. 6.1 was constructed based on the simulations results and PCB design considerations discussed in previous chapters. The experimental setup consists of the following parts:

a. The five-level flying-capacitor converter boards that include the gate drivers and the dc-bus capacitors,
b. The LCL filters with their corresponding measurement circuit,
c. A F28369D DSP used to control the UCSC system,
d. A variable ac source (variac) used to generate substation voltages,
e. A dc source to power gate drivers and sensing circuitry, and

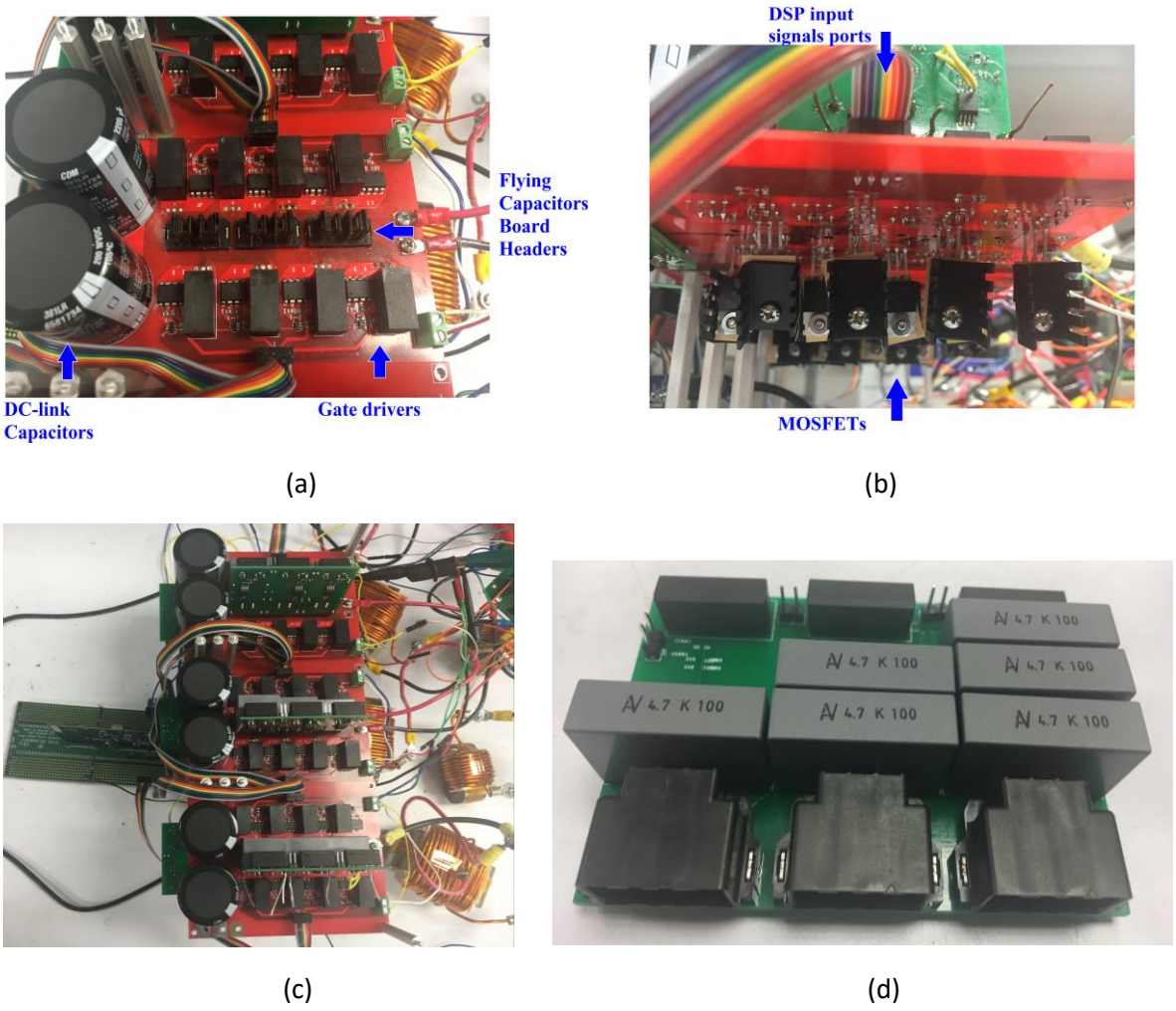


Figure 6-1. (a) FCC PCB top side, (b) FCC PCB bottom side, (c) Three-phase FCC prototype and (d) Flying capacitors board

f. The load represented by three resistors of 50, 50, and 25 Ω in series with three-phase line inductors of 0.6 mH.

6.3 Open-Loop Single-Phase Five-Level FCC Test

Before building the UCSC system, one single-phase five-level FCC was tested in order to confirm the PCB functionality and initial characteristics such as: flying-capacitor pre-charging process by ramping the dc source, balancing dynamics, open-loop outputs, code initialization and ePWM signals generation. Three different versions of the board were constructed as a result of

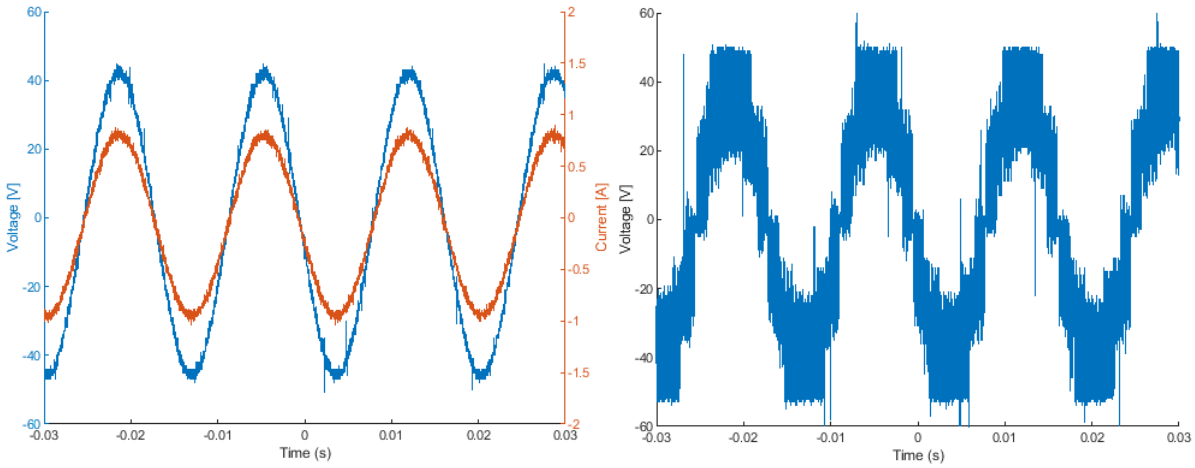
performing these open-loop tests. Improved components placement and gate drivers circuitry design, addition of dc-bus capacitor parallel paths for three-phase testing, perpendicular flying-capacitors boards and separated LCL filter circuits were the main changes during this stage.

The single-phase five-level FCC was tested using the UCSC parameters from Table 3-1, a dc-bus of 100 V and a resistive load of 50 Ω. PWM signals used a sinusoidal waveform as the reference signal with a modulation index m_a of 0.9. Load current and voltage output waveforms are shown in Figure 6-2(a). The voltage amplitude corresponds with $0.9 * Vdc/2$ because, following the combinations presented in Table 2-1, the maximum instantaneous voltage is achieved when all of the top switches are 'ON'. In addition, the current amplitude is confirmed using Ohm's law as follows:

$$V_o = \frac{m_a * V_{dc}}{2} = \frac{0.9 * 100}{2} = 45\ V \tag{6-1}$$

$$I_o = \frac{V_o}{R_{Load}} = \frac{45}{50} = 0.9\ A \tag{6-2}$$

The voltage waveform at the output of the converter before the LCL filter is presented in Figure 6-2(b) in order to visualize the five-level output of the FCC. This five-level output voltage waveform presents undesired ringing during each level increase due to a low-size flying capacitor selection. The expression from equation (3-2) used to design the capacitors is dependent on the switching frequency, a predefined ripple voltage and the modulation index. During the design phase, the flying capacitors were chosen incorrectly using a modulation index of 0.9 and a ripple voltage of 5V. Both values do not produce the worst-case scenario that occurs for very low modulation index. As a result, high and not uniform charging and discharging peaks occur that



(a) (b)

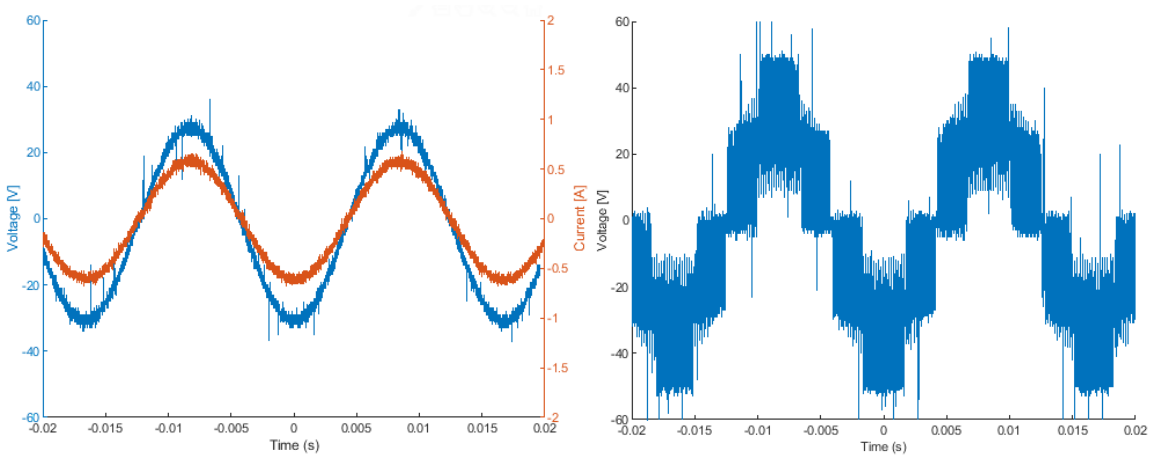
Figure 6-2. (a) Open-loop experimental current and voltage output waveforms, (b) Five-level FCC voltage output waveform measured before the LCL filter

impact directly in the output waveform. However, the LCL filters were effective at eliminating these oscillations and sinusoidal current and voltage waveforms are obtained as displayed in Figure 6.2(a).

6.4 Single-Phase FCC Tested as a Controlled Voltage Source

The next phase was to validate the control algorithm setup and the measurement conditioning circuits. This step was very important because it allows confirming the correct implementation of the ADC module in the DSP, the SOGI-FLL structure functions, PI controller functions and current-mode controller explained in chapter 3. The main difference with the UCSC control algorithm is the use of sinusoidal impossd by waveforms, instead of the grid voltage and load current measurements.

First, the experimental setup will consists of a single-phase FCC tested as a controlled voltage source using a dc bus of 100 V, a closed-loop controller connected directly to a 50Ω resistor. The inverter output current was used as the measured signal, while two sinusoidal



(a) (b)

Figure 6-3. Experimental current and voltage output waveforms when behaving as a controlled voltage source, (b) Five-level FCC voltage output waveform measured before the LCL filter

waveforms with amplitude of 30 V and 0.625 A were added in the DSP as the reference for the grid voltage and the expected load current, respectively. In order to set these references in the DSP, a scale from -1 to 1 needs to be used; therefore, these reference signals are 3.0 V and 1.0 V when written into the code. The initial operating condition were the same used in the open-loop test but the modulation index was set at 1.0. Figure 6-3 shows that the load current has been decreased to the expected value of 0.625 A while maintaining the same five-level FCC output voltage before the LCL Filter. The spikes displayed in Figure 6-3(b) can be attributed the probe characteristic impedance, EMI noise and the effect of parasitics due to long cables used to build the UCSC system.

6.5 Experimental Results of the Three-Phase FCC prototype

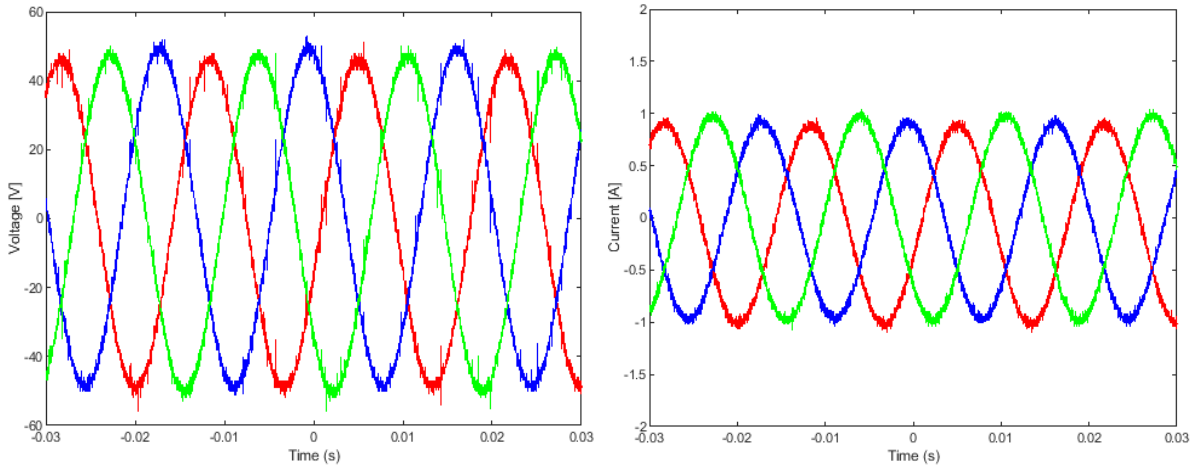
The same procedure was followed when testing the three-phase FCC prototype. First, the correct operation with an open-loop control algorithm was verified; then, the closed-loop controller using the system as a controlled voltage source was validated. Both tests were employed in order

to acquire similar results when compared with the single-phase FCC experimental tests. Using the same dc-bus voltage of 100 V, a modulation index of 1.0 for all phases and three 50 Ω resistors; the results are shown in Figure 6-4 for the open-loop controller. The current and voltage outputs have at their peaks values of 1 A and 50 V, respecively, with 120° phase shift between phases.

For the closed-loop controller test, the reference grid voltage for the three phases was established at 30 V; however, the load current reference signals were set at 0.25 A for phase A, 0.5 A for phase B and 0.75 A for phase C. The experimental result presented in Figure 6-5 confirm the capability of the algorithm to control the inverter current based on any load current reference and following the phase angle determined by the reference grid voltages.

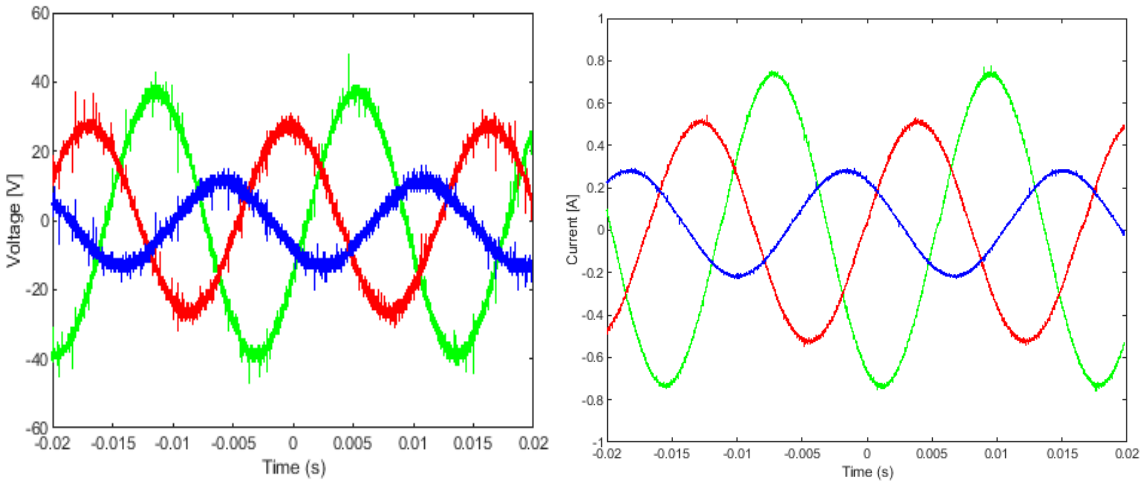
During this stage, the main issues that had to be addressed were related to the sensors and measurement circuits as numerated below:

a. Modification of operational amplifiers gains,



(a) (b)

Figure 6-4. Experimental current and voltage output waveforms of the three-phase FCC with a modulation index of 1.0



(a) (b)

Figure 6-5. Experimental current and voltage output waveforms of the three-phase FCC when operating as a controlled voltage source

b. Incorporation of RC filters before the ADC pins,

c. Tuning the ADC midpoints in the controller code to reduce negative offset,

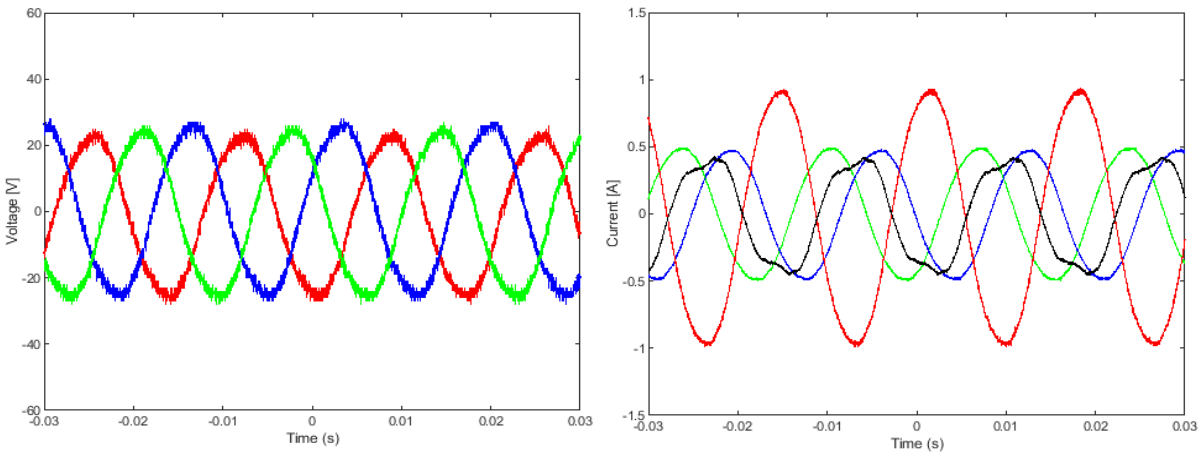
d. Separation of the analog and digital grounds by including +5V dc-dc converters, and

e. Avoid daisy chain connections when powering DSP signals and sensor circuits.

Another challenge was the configuration of the ePWM and ADC modules in the F28379D. The 24 PWM channels had to be configured along with 9 ADC ports, and both modules had to be synchronized together like discussed in the previous chapter.

6.6 Testing of the UCSC Prototype

In order to generate unbalanced grid conditions, the load at phase A was changed to a resistor of 25 Ω. The variac used to generate the substation voltages was set to 25 V and the switch connected to the FCC was opened. Figure 6-6 displays the grid voltages at the PCC and the



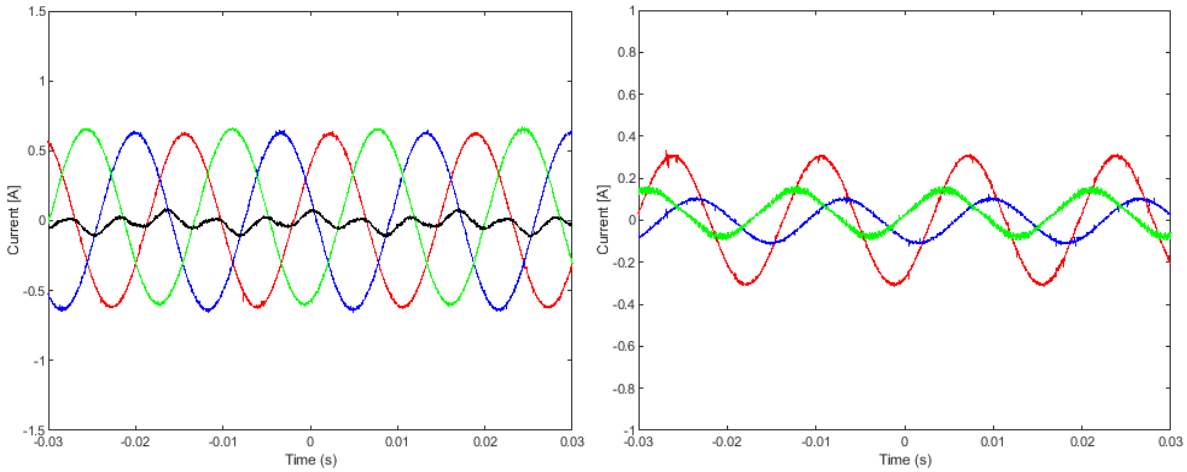
(a) (b)

Figure 6-6. (a) Voltage waveforms measured at the PCC, and (b) Unbalanced load current and neutral current (black) before UCSC operation

unbalanced currents that the UCSC prototype will need to compensate. The neutral current from the four wire three-phase systems is shown in Figure 6-6(b) in black.

After the FCC has been pre-charged, the switch is closed and the UCSC starts operating. The substation currents are balanced during full operation of the UCSC prototype while the neutral current is decreased, these results are shown in Figure 6-7(a). Substation current balancing goes towards the average of the load currents (0.67 A) and the converter phases inject or draw current from the grid as illustrated in Figure 6-7(b).

The fundamental component of the neutral current has been reduced effectively to a value of 7.9% of the neutral current at unbalanced conditions. Nevertheless, some third-harmonic component remains due to the influence of asymmetry in the voltages amplitude and phase angles of the variac, distortion caused by harmonic currents produced by non-linear equipment in the laboratory because the UCSC prototype is not completely isolated or the effect of the dead-time during switching transitions as they cause distortions in the inverter outputs [1 – 3].



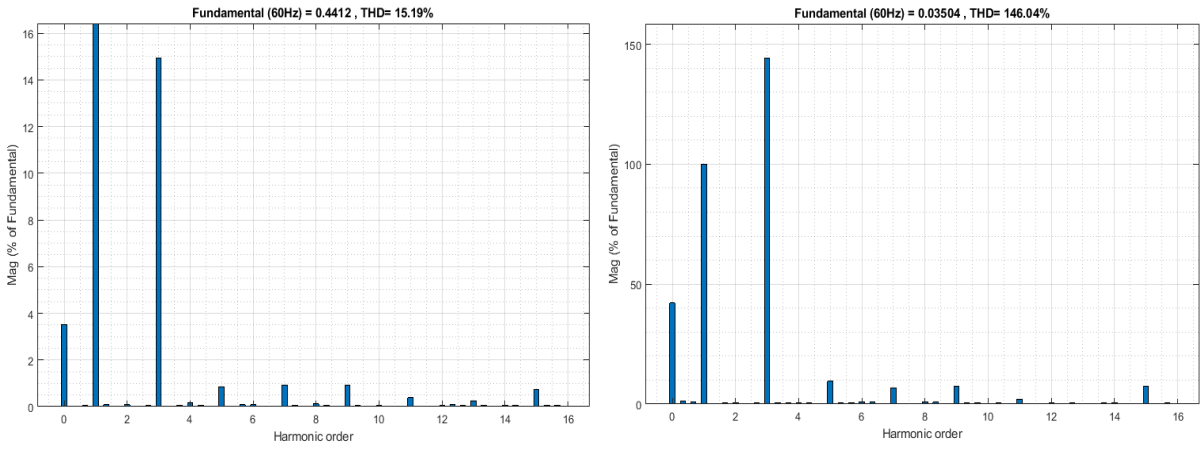
(a) (b)

Figure 6-7. (a) Balanced substation current waveforms during UCSC operation, and (b) Inverter current waveforms during UCSC operation

The fast Fourier transforms (FFT) of the neutral current before and during UCSC operation are presented in Figure 6-8. The FFT confirms a reduction from 0.44 A to 0.036 A of the peak fundamental current component in the neutral wire with the presence of a 3rd harmonic component.

6.7 Flying-Capacitor Balancing Dynamics

From the results visible in Figure 6-9, the capacitor voltages during UCSC operation correspond to the expected values of $V_{c3} \approx 75\,V$, $V_{c2} \approx 50\,V$ and $V_{c1} \approx 25\,V$, as discussed in Chapter 2, if a dc-bus voltage of 100 V is applied and all flying capacitor voltages are pre-charged to the same initial voltage (25 V). The slight difference between the measurement voltage and the nominal value is mainly due to the presence of devices voltage drop not considered in the algorithm. The flying-capacitor voltage waveforms are similar to the simulated results from Figure 4-7(b) with the PS-PWM scheme. As mentioned in previous chapters, this modulation technique



(a) (b)

Figure 6-8. FFT analysis of the neutral current before and during UCSC operation

does not use the most efficient combination of switching states; therefore, the charging process of some flying capacitors is not uniform and some MOSFETs have bigger periods during switching. The ripple voltages for the flying capacitors are:

$$\Delta V_{c3} = 17 \text{ V}$$

$$\Delta V_{c2} = 12 \text{ V}$$

$$\Delta V_{c1} = 6 \text{ V}$$

The flying-capacitor ripple voltage was set to 5 V and for a capacitance of 4.7uF. As mentioned before, the design approach was not done properly because, following equation (3.2), a modulation index of 0.9 used for the open-loop test does not give the minimum required capacitance at the highest UCSC operation point. Thus, these selected values are relatively high if a dc-bus of 100 V is used. To solve this problem a lower voltage ripple should be used and a lower modulation index had to be chosen in order to size the capacitor correctly. Another option could be to increase the switching frequency. Poor design of the flying capacitors is evidenced in Figure 6.9 as the ripple voltages are not uniform and may not be stable at a certain voltage point. However,

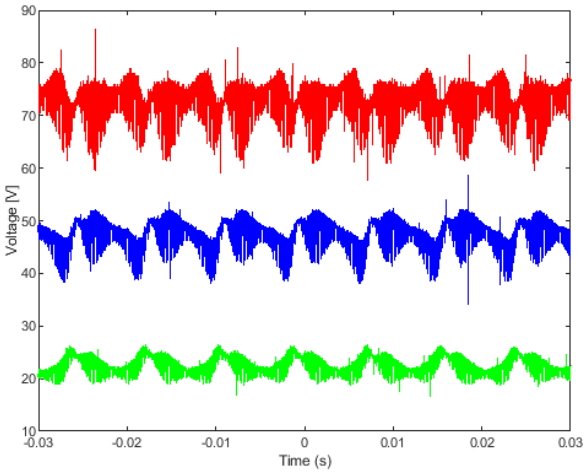


Figure 6-9. Voltage waveforms of the flying capacitors FC1a (green), FC2a (blue) and FC3a (red) during UCSC operation

experimental results have proven that high voltage ripple does not have a major impact in the UCSC operation. Still, capacitors lifetime may be reduced drastically due to this issue, so it is necessary to reduce this value in order to achieve better efficiency and reduce possible future maintenance costs.

6.8 Conclusions

The UCSC prototype using flying-capacitor converters was used to compensate an unbalanced system. The substation currents were balanced to the reference average value of 0.67 A and the fundamental component of the neutral current was decreased from 0.44 A to 0.035 A. Several stages were revised before the validation of the UCSC controller in order to confirm the PCB functionality and correct operation of the sensor and measurement circuits. Results presented in this chapter proved that the UCSC control algorithm is effective at compensating for negative- and zero-sequence current components and can be used at higher levels of voltage.

The flying capacitors were not designed properly as the modulation index used for the open-loop tests was also applied for the UCSC operation. In consequence, the voltage ripple for

each FC was too high and the charging and discharging were not uniform and unstable. Following this, it can be concluded that by lowering the modulation index during capacitor sizing, this problem could be overcome in the FCC prototype by increasing the switching frequency of the system; the flying capacitor waveform could have showed better results.

6.9 References

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CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

The development and integration of DG, such as wind or solar farms, in distribution networks have produced less predictable and uncontrollable power flows that diminish the power quality of the grid [1]. The UCSC has been presented in Chapter 1 as a new solution to overcome the current unbalances that are present in three-phase systems due to the interconnection of large single-phase DG and unbalanced loads while maintain the reactive power compensation capability that most D-FACTS provide. The topology selected for the UCSC systems was the flying-capacitor converter because it allows for easily active and reactive power flow control, full utilization of the dc-link when compared with conventional two-level converters and the capability of generating the output voltage through different redundant states that allow a simpler controller and greater efficiency. Furthermore, the inherent self-balancing voltage characteristic of the flying capacitors which eliminate the requirement of additional controllers to balance the capacitor voltages in contrast with other multilevel topologies [2 - 4].

An overview of the fundamentals of the FCC was presented in Chapter 2. Different modulation techniques such as the PS-PWM, the PD-PWM and active balancing methods were analyzed in order to conclude that the PS-PWM (and its variant the iPS-PWM) are the most suitable switching techniques that guarantee the capacitor voltage self-balancing property. The UCSC system parameters along with the control algorithm that was later used to develop the simulations and build the prototype were presented in Chapter 3. A current-mode control algorithm that uses the measurements from the substation currents, PCC voltages, loads currents and output

currents from the converter was selected to balance the up-stream substation currents and compensate for reactive power. In order to facilitate the active and reactive power control, each phase is controlled independently with the use of single-phase d-q synchronous-rotating frame transformations. This was followed in Chapter 4 by the implementation of real-time simulations in Matlab/Simulink™ in order to validate the control principles detailed before and confirm the parameters selection criteria. Simulations results confirmed the viability of the proposed solution and enabled the design and construction of the UCSC prototype.

The prototype was constructed following important PCB considerations aiming to reduce parasitic inductances and capacitances, overall system size and the effect of EMI noises during normal operation. The configuration and setup of the controller in a F28379D DSP was described in Chapter 5. The UCSC prototype using flying-capacitor converters was tested in the laboratory to compensate for unbalanced load currents. Experimental results presented in Chapter 6 confirmed the balancing of the substation currents and reduction of the fundamental component of the neutral current. The UCSC has been found effective at reducing the fundamental neutral current component in 92.04 % from 0.44 A to 0.035 A, while the substation current were balanced to the average of the three load currents (0.67 A). The presence of a third harmonic component in the neutral current during UCSC operation can be attributed to the effect of asymmetry in the voltage amplitudes and phase angles of the variac, and also due to the distortion caused by harmonic currents produced by non-linear equipment in the laboratory. Including a controller section in the UCSC algorithm to mitigate these harmonic currents generated from the source, could further improve the results given by this prototype.

In addition, the flying capacitor natural balancing property was analyzed. With the use of PS-PWM, the flying capacitor voltages are balanced at the expected values of $V_{c3} \approx 75$ V, $V_{c2} \approx$

50 V and Vc1 ≈ 25 V using a dc-bus of 100 V and all flying capacitor voltages pre-charged to the same initial voltage. Voltage ripple of each flying capacitors was close to the design value of 5 V using the calculated capacitance of 4.7uF. However, it was concluded that the size of the flying capacitors was not optimal as the design was done for the open-loop test and the modulation index was not for the worst-case scenario during UCSC operation. Although the voltage ripple design value of 5 V is relatively high, it did not present any unexpected effect during UCSC operation; however, in order to preserve the lifetime of the UCSC components, the voltage ripple should be reduced to a lower value or the flying capacitor size needs to be increased. Because the capacitor voltages are charged and discharged using the PS-PWM scheme, they do not use the most efficient combination of switching states; therefore, not identical waveforms were produced with at frequency of 120 Hz. Also, these waveforms were affected as some MOSFETs have bigger periods during switching.

7.2 Recommendations for Future Work

The following recommendations are presented as potential future research work:

a. Redesign the system with a different flying capacitor sizing equation (3.2)
b. The controller algorithm was successfully tested in a low-voltage application; however, testing the controller in a medium-voltage application could provide additional results for analysis at different operating conditions. The use of SiC MOSFETs allows for direct connection to MV distribution networks and shall be addressed carefully as powering the gate driver circuitry becomes a more complex challenge [5]. The use of a self-powering device circuit might become a preferable solution as presented in [6].

c. The incorporation of a solution to protect the system against over-voltage events such as lighting strikes. These types of events are very common during normal grid operation and if not taken into consideration they can be harmful to the power electronics devices if the voltage breakdown limit is surpassed [5].

d. Another possible topic to address is the effect of internal faults in the converter. Reliability, security and efficiency are of great concerns when working with power electronic applications. In the case that a semiconductor device or flying capacitor suddenly fails, the system must be prepared to work at a lower capacity or automatically shut down to avoid undesirable behavior during operation [7].

e. Even though the operation of the UCSC controller algorithm that uses single phase d-q synchronous-rotating frame has been confirmed in this thesis; the successfully implementation of an α - β stationary reference frame controller could produce an interesting comparison for further discussion and improvement.

f. During the design phase, the sensors and measurement circuits were built in different small PCBs. In consequence, many long cables had to be used to power the circuitry and connect the ADC single-ended signals to the DSP. The length of these wires contributes in great manner to the increase of parasitic inductances which are unsuitable for high-frequency signals. The easier solution could be to design a bigger PCB that contains all sensors circuits and eliminate the need of jump wires.

7.3 References

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