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## Measuring Characteristic Shrinkage Variability Due to Metal Loading Effects in Low Temperature Co-Fired Ceramic Using Image Processing

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

by

John Ezekiel Zumbro John Brown University Bachelor of Science in Engineering, 2016

> December 2018 University of Arkansas

This thesis is approved for recommendation to	the Graduate Council	
H. Alan Mantooth, Ph.D. Thesis Director		
Simon Ang, Ph.D. Committee Member	J. Ambrose Wolf, Ph.D. Committee Member	

#### **ABSTRACT**

Low temperature co-fired ceramic (LTCC) has many benefits when it comes to electronic packaging due to the low dielectric loss, reliability in extreme environments, and high breakdown voltage. Though the ceramic has a lot of benefits it is not widely used due to the high cost and complexities associated with manufacturing. One of these issues with manufacturing is compensating for the shrinkage of the ceramic, this is accomplished by using an expansion factor, creating the "green" or manufactured design. This expansion factor is approximated through knowledge of the ceramic factors such as the metal loading, layers of ceramic tape, firing profile, lamination pressures, etc. While this expansion factor method has been studied and equations have been derived for compensation for the shrinkage, there is little evidence that the equations correctly compensate for the complexities of the design. Due to the lack of understanding of how different design parameters play a role in the shrinkage of the panel, this thesis will look to address the fundamental issue of measuring the shrinkage effects due to metal loading using a shrinkage characterization method called shrinkage field mapping. Due to the increased measurements needed for shrinkage field mapping, image processing is used to extract dimensions without dramatically increasing measurement time for the High-Density Electronics Center LTCC process. With the change in the shrinkage measurements, a 0.07-0.25% characteristic shrinkage difference can be measured from changing the volume of metal inside by 1.22mm<sup>3</sup> in a DuPont 9k7 50mm x 50mm panel. These measurements were confirmed by three different fabrication experiments.

#### ACKNOWLEDGEMENTS

Thanks be to God for his never-ending grace.

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#### 1 INTRODUCTION

#### 1.1 OVERVIEW OF THE PROJECT

The Kansas City National Security Campus (KCNSC) and Sandia National Laboratory (SNL) have partnered with eight universities (University of Arkansas, Kansas State University, University of Kansas, Michigan State University, Missouri University of Science and Technology, University of Oklahoma, University of Nebraska Lincoln, and Georgia Institute of Technology) to improve the state-of-the-art in radar technology. As a part of this endeavor, research includes investigations into all aspects of the electronic system, which includes the materials used in the different integrated circuits, the packaging of the system, and finally the system level integration. This research is conducted at multiple universities to access the different technologies and develop processes and technology at each university. Specifically, for the University of Arkansas, the research is focused on the improvements to the fabrication and use of Low Temperature Co-fired Ceramic (LTCC) which is manufactured at the High-Density Electronics Center (HiDEC).

#### 1.2 OBJECTIVE AND SIGNIFICANCE

The objective of this thesis is to setup the frame work to better understand the effects of design parameters on LTCC shrinkage without dramatically altering the HiDEC thick-film fabrication process. This was centered around two aspects of the LTCC; first the tools used to document the fabrication of ceramic, and the second being the extraction of the shrinkage from the fired panel. By changing the documents that are used to layup and layout the ceramic, different analytical tools such as metal loading per unit area, and measurements in the processing tools can be used to correlate the design to the shrinkage. The shrinkage is calculated by measuring the final dimensions of the fired panel using image processing and correlating those dimensions back to the computer aided design (CAD) documents. This method provides quantifiable data on how design

parameters effect LTCC shrinkage which provides a path forward for achieving more accurate LTCC designs while quantifying the effects of metal loading.

Image processing is a widely used tool for collecting dimensional data quickly, it provides a means to extract dimensional data that can be used in different applications or collection schemes. This change from sampling the design using a manual process to an image process allows for the ceramic to be measured at a faster rate to give more accurate feed back to the manufacturer. This faster feedback provides a quick insight into how the ceramic is behaving so that changes can be made before the next fabrication run. When additive manufacturing of LTCC becomes more feasible, the next design can just be printed in the same day provides new faster turn time for producing designs. The image data of the final design also provides the means to assemble a database of designs that can be used for analyzing the expansion factor based on the type of ceramic used.

#### 1.3 THESIS ORGANIZATION

Chapter two describes the current High-Density Electronics Center thick-film fabrication methods. The background for the measurement methods and shrinkage calculation methods will be presented in Chapter 3. The methods for the image processing will be presented in Chapter 4, with the analytical results to follow in Chapter 5. Finally, Chapter 6 will be the conclusion, with Future work in Chapter 7.

# 2 HIGH-DENSITY ELECTRONICS CENTER THICK-FILM FABRICATION METHODS

Thick-film technology is often used in extreme environments, pressures, or in other high reliability applications where common organic PCBs are unable to withstand the environmental conditions or in high reliability applications. The High-Density Electronics Center (HiDEC) has all the

equipment required for LTCC fabrication. The following section of the thesis describes a fabrication process for the DuPont<sup>TM</sup> 9k7 GreenTape<sup>TM</sup> used in this work along with the documentation for the thesis. This section will consist of details regarding the following steps: blanking, preconditioning, via punch, via fill, screen printing, stack and tack, lamination, cut to size, sintering, post fire processing, and singulation. This flow can be seen in Fig. 2.1, with most of the processes being able to be accomplished in parallel for the 11-step serial process. The post processing singulation and processes will not be described since the focus is on the characterization of the shrinkage based on the design due to the co-fire process.

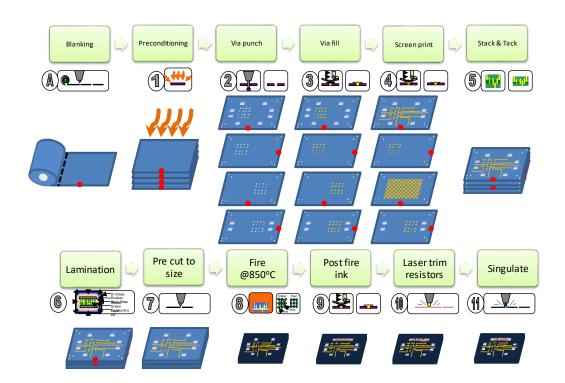


Fig. 2.1. LTCC fabrication process flow (E. Porter - Electronic Packaging Presentation)[1]

## 2.1 DESIGN GENERATION

The LTCC fabricated at the University of Arkansas consists of generating a series of documentation the correspond to both the layout (XY direction) and layup (Z direction). The

desired layout, or the fired design, is typically constructed in an electronic computer-aided design tool, such as Keysight ADS, Cadence Allegro, or KiCAD. These programs then export RS-274 files (Gerber files) that can then be converted to an AutoCAD design exchange file (DXF) so that then the manufactured file can be created by expanding the desired design by an expansion factor shown in (1).

$$Expansion Factor = \frac{1}{1 - \frac{estimated \% shrinkage}{100}}$$
(1)

These layout files are required for generating the hole punch files for punching, stencil files for via filling, and the screen-printing files. As a note for the thesis, the layout files and processes to convert the files are not changed from the current HiDEC process; there are only additional files that are added to the thesis for the documentation of the process and the layup, also known as the Z-stackup.

The layup files are typically constructed in PowerPoint and only contain to the stacked layers that are in the layup files as seen in Fig. 2.2. In the current process, the layup documents only serve as reminders for the person fabricating the LTCC design, since it is easy to confuse the tape layers due to the lack of reference markings. The layup file in the thesis is changed to an Excel file which allows software to read layers in the documentation that correspond to the layout of the file. This creates the means for a software program to calculate the layers, total ceramic thickness, and amount of metal contained in the design, along with any other key design parameters that affect the ceramic. After the layout and layup documents have been created the next step is to panelize the design for fabrication.

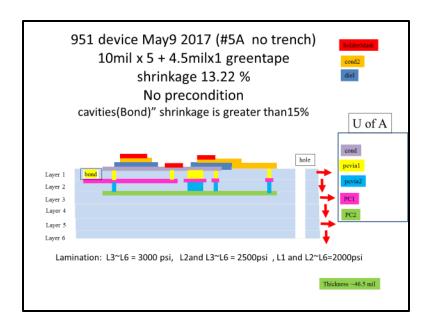


Fig. 2.2. PowerPoint layup file of example LTCC

### 2.1.1 DESIGN PANELIZATION AND EXPANSION

The panelization of the LTCC design is a critically important step if the product is to have a good yield of the original design. This process is common in the Printed Circuit Board (PCB) design since the designs that are being manufactured do not take up the entire panel used in the fabrication process. However, when transitioning to LTCC panelization there must be a consideration on the stresses introduced in the panel due to the metal loading effects associated with the design. The impact of this metal loading has not been extensively measured or calculated thus the importance of keeping the design as symmetrical as possible is highly important.

To panelize a design at HiDEC, there are a few considerations that must be taken into account such as the tape system and the size of the panel. The tape system will drive how much metal can be used so that metal loading effects will not need to be considered. The tape will also provide the maximum expansion factor that a design can be fabricated at, which is ultimately driven by the shrinkage of the tape. This means that the more the tape shrinks, the smaller the design that can be fabricated. The second consideration is the lamination plates that will be used

will also affect the maximum size that can be produced. These lamination plates have two common patterns at HiDEC, the large 139.7 mm square or a smaller 64.53 mm square. These dimensions correspond to the 2.387 mm diameter holes that are punched in the tape to provide mechanical pin alignment when fabricating the panels. The smaller 63 mm plate is often used to reduce the number of times screen printing, and via filling are used to fill tape. After the design has been panelized at the given dimensions, the next step is to expand the tape by an expansion factor. This expansion factor is based on how the design is going to behave, or the predicted shrinkage for that specific design as seen in (1). After the tape has been expanded the next step is to prepare the physical tape for fabrication of the design.

#### 2.2 BLANKING AND PRECONDITIONING

To begin the physical process of LTCC fabrication, the tape is first blanked, or cut to size. This size is dependent on the lamination plates that will be used for the lamination process. For HiDEC, the tapes are 150mm x 150mm in the XY plane. Other sizes of tape can be purchased however the common system for HiDEC is the 150mm tape without cutting the tape down to size. These tapes are often purchased from ceramic tape manufactures.

After blanking the tapes, the next step is to precondition the tape. This step is optional depending on the ceramic system, but typically used in good practice. In the specific case using DuPont<sup>TM</sup> 9k7 GreenTape<sup>TM</sup>, the preconditioning process consists of letting the tape soak at a temperature of 100°C for 20 minutes to remove any storage effects.

### 2.3 PUNCHING

After blanking and preconditioning the tape, the next step is to begin the process of fabricating the design within the ceramic. These steps will include via punching, via filling, and screen printing

in that order. However simple that process seems on paper, it requires many more steps than the three that are listed, thus performing each process as a parallel process for the tape layers reduces the amount of time to fabricate the LTCC panels.

Punching out the ceramic tape is as simple as it sounds. In HiDEC, there is a mechanical hole punch that punches though the tape like a hole punch in paper. This process is limited to a 1:1 aspect ratio, meaning that the diameter of the smallest hole that can be punched in the tape is equal to the thickness of the tape. The tape is not limited to be cut out using a punching process, there are other processes such as micro-machining and laser-machining, but both have their flaws when machining ceramic designs.

For manufacturing LTCC at HiDEC, there are two Unichem MP415 punch machines that can be used for making the design. The two machines can each hold four unique punches, and they commonly consist of the following diameters of vias: [0.1524 0.254 0.508 2.387] mm and [0.1524 0.3048 0.508 2.387] mm for respective machines. The machines are limited to running 8000 punches per file due to the limited memory of the machine. These via punch files are commasseparated value (CSV) files with the number of the punch being used in the first column and with the xy-location of the via in the next two columns. The punch number corresponds to the arrays above, so a one in the punch position would call a 0.1524mm punch on both machines, but a two on machine 1 would correspond to a 0.254 mm via vs a 0.3048 via on the other machine. This allows the same CSV file to be used on the two different machines for the corresponding design. This is the process that was used for the fabrication of the test coupons; the same design file was used but just processed on two different machines.

#### 2.4 VIA FILL

The via fill process at the University of Arkansas is quite simple yet difficult to process large quantities of designs. The standard via fill process needs the following tools: a lamination plate, four alignment pins, tissue paper, the tape being filled, a Mylar mask used for the lamination, a finger squeegee, and the desired via fill material. The procedure is quite simple, first the lamination plate is cleaned with isopropanol alcohol and allowed to dry. Once dry the tissue paper is then placed on the lamination plate with the four pins into the alignment holes holding the tissue paper in place. The tape is then placed top side down on the tissue paper with the mask to follow. The mask covers any vias that are not going to be filled during the process. The next step is to use the finger squeegee to fill the vias with the conductive paste, after all the vias have been filled the next step is to remove the mask from the backside of the tape. While keeping the tissue paper connected to the front side of the tape the next step is to wipe the extra via fill from the backside of the tape. This guarantees that the tape is clean for future processing and it also guarantees that the via fill material will not be removed from the backside of the tape when the Mylar backing in removed in the stack and tack step. After the backside of the tape has been cleaned the next step is to remove the tape from the tissue paper. After the tape is separated from the tissue paper, the next step is to look underneath the microscope to verify that no vias were left unfilled. After inspection, the tape is then placed in an oven at 80°C for 5 minutes to allow the vias to dry.

## **2.4.1 ISSUES**

Since the current HiDEC process does not use a stencil and a via filling machine, there has been a post processing issue where the vias have been breaking any thin-film that has been applied. These have been seen having at 30 µm ceramic posting around the via. This issue traces back to a process mentioned in the literature where Mylar masks are used instead of metal stencils. [2]

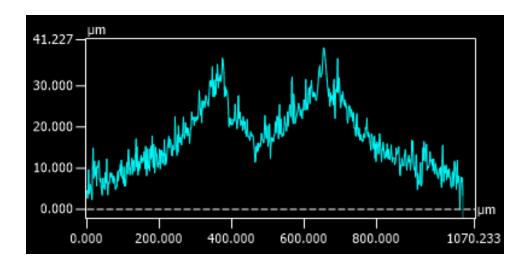


Fig. 2.3. Via crowning profile effect seen on sample 10A

#### 2.5 SCREEN PRINT

After via filling and drying the next step is to screen print the conductors on the surface of each tape. These conductors are made from Gerber files that contain via alignment marks and the design that is going to be manufactured for that specific layer. To operate the screen printer, the first step is to align the cameras to the screen. This is accomplished by printing the alignment marks on a sacrificial tape. The table is not moved, and the cameras are then aligned to the via alignment marks on the tape. After the cameras are locked in position, the sacrificial tape is then removed from the vacuum stone allowing the tape to be printed to be put on the stone for screen printing. The table is then realigned to the actual tape via holes where the tape is then prepared for screen printing. This screen printing is typically only printed in one direction but can be printed multiple times if the tape is not filled during the first screen print. After screen printing the tape is unloaded and then put in the drying furnace for ten minutes at 80°C.

#### 2.6 STACK AND TACK

After all the tapes have been filled and printed, the next step is to align all the tapes and stack them together on the lamination plates. These lamination plates are thick steel or aluminum which are

machined flat with the same locations as the alignment vias described before. The tapes are stacked from the top layer face down to the bottom layer, the mylar is removed after each tape is aligned on the stack. The pins are holding the back of the tape.

#### 2.7 LAMINATION

After all the tapes are stacked the top lamination plate is put on top of the stack and the entire stack is then wrapped in latex wrapping. The wrapping allows for the lamination plates to maintain separation from the vacuum bags so that the wrinkles in the vacuum bags do not puncture the bag allowing water to get into the bag ruining the ceramic. The latex wrapping is sealed in 2-3 bags then placed into the isostatic laminator. At this point the cycle is engaged and the pressure chamber is cycled up to 20.68 MPa at 65-70°C for 10 minutes. After lamination the next step is to remove all the protection and move on to cutting the ceramic to the firing size.

#### 2.8 CUT TO SIZE

The final step before sintering is to remove the outside edges of the ceramic, this step creates a cleaner edge than having non-uniform stacking of the external layers. This step of cutting to size is typically not the ideal cut of the ceramic, and it is not designed to be a high precision cut. If high precision is needed, a dicing saw can be used after the ceramic has been fired.

#### 2.9 SINTERING

The final step is to take the green ceramic and form the fired final ceramic. The sintering process allows the glass to recrystallize, or form crystal structures, around the alumina particles creating the dielectric constant used for 9k7. This process typically takes 24 hours using the HiDEC furnaces and can be seen in the DuPont GreenTape™ Guidelines.[3] There are additional steps after this, such as post-fire processes that are thin and thick-film related processes. [4]

#### 2.10 SHRINKAGE CHARACTERIZATION

The shrinkage of the panel is estimating by comparing measurements in Fig. 2.4 and to the CAD documents and using Eq. (2) to calculate the percent shrinkage. This is deduced from only a few points around the outside of the panel which are used to capture the entire panel. For the purpose of thesis, this method is called the traditional method for characterization since it is one of the most common methods for characterizing the LTCC.

$$\%shrinakge = \frac{\Delta l}{l_o} * 100 \tag{2}$$

#### 2.11 DOCUMENTATION

Depending on the project, a PowerPoint slide is constructed with the process information for the panel, while also contains the original design documents. In addition to the design documents, there is typically a scan of the flat panel that is then cropped to approximately the same size of the panel seen in Fig. 2.5. There is also a measurement of the alignment vias used to generate a report of the expanded size seen in Fig. 2.4. This measurement method is called the traditional measurement method for calculating shrinkage in this thesis.

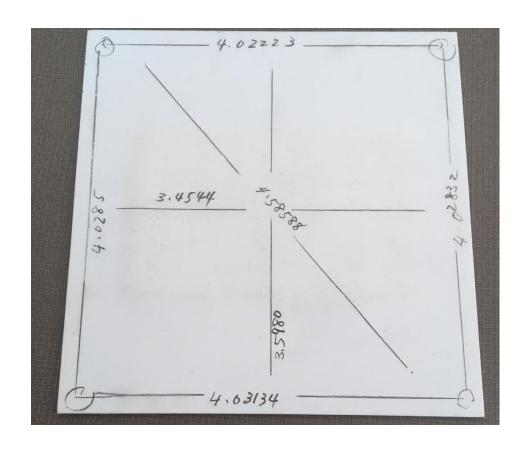


Fig. 2.4. Image of shrinkage calculation using a 10-point shrinkage calculation on technology demonstration panel A00 (shrinkage estimation panel)

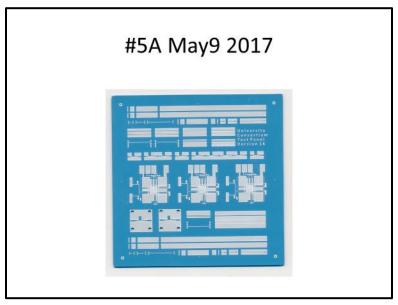


Fig. 2.5. PowerPoint slide consisting of computer scan of the example LTCC module

#### 3 BACKGROUND

Low temperature co-fired ceramic shrinkage is often studied by different parties producing a range of electronic devices, including microelectromechanical systems (MEMS), multi-chip modules (MCMs), interposers, and printed circuit boards (PCB) [5]–[13]. Due to the various applications, often the research behind the work is focused to demonstrate the intended purpose of the application, thus there is not additional work on any of the issues associated with manufacturing for that application. Since LTCC that has been applied to a broad range of applications, there is a general assumption that it as a well-developed electronic technology, however LTCC is still a fickle material to manufacture due to the lack of knowledge of how the design affects the shrinkage of the device. This issue is represented by the DuPont GreenTape<sup>TM</sup> Guidelines image of the effect of metal loading on a ceramic design seen in Fig. 3.1. This shows how an electronic design can affect the fired product. This challenge of characterizing differential ceramic shrinkage for different designs has been the biggest hindrance for producing different high-precision designs in a cost-effective manner [14]. This is backed by the lack of information found in predicting the effect of the design on the ceramic shrinkage.

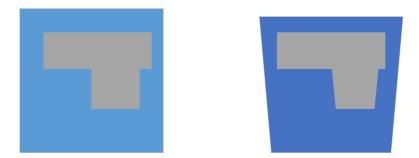


Fig. 3.1. (left) Green ceramic with ground plane (right) fired ceramic with ground plane [3].

In most publications, there have only been a few shrinkage measurements as seen in Fig. 2.4, which estimates the shrinkage of the panel [15]. This leads to an assumption that in most of

the studies on the effect of process parameters on the shrinkage of LTCC, the single percent shrinkage is based on this method of calculating the shrinkage for the panel. While this can be an accurate estimate of the shrinkage measurement, it may not be the most ideal way to describe panel if the main goal is to extract the effect of metal loading on the panels. Thus, additional methods must be considered while not overlooking what previous methods have used to describe shrinkage.

#### 3.1 HONEYWELL FM&T DESIGN OF EXPERIMENTS

For Girardi et al., the main focus of their study was to develop an equation that described how to manufacture LTCC. The intention of this study was to vary factors such as layer count, metal loading percentage, and lamination pressure to determine how much of a factor each manufacturing process had on the shrinkage of the final product [16]. These sweeps of the different parameters then boiled down to an equation that displayed the final shrinkage as a function based on the metal loading percentage, lamination pressure, and layer count as seen in Eq. (3). While this study swept factors that affected the DuPont<sup>TM</sup> 951 GreenTape<sup>TM</sup>, it did not consider any information about the effect of the sintering process on the tape. Based on how these factors were studied, this work provided an idea of the contributing factors to the shrinkage of a ceramic panel, however missed the mark in the simplification in the overall process.

% firing shrinkage (3)  
= 
$$14.4988 - (0.0171450 \text{ x \% metal loading})$$
  
-  $(0.00045361 \text{ x pressure}) - (0.034790 \text{ x layer count})$ 

## 3.2 DENSIFICATION EFFECT ON SHRINKAGE

As seen in Girardi, et al, there were only a limited number of factors swept in the DOE and thus effects such as the firing profile were left out of the experiment. In Dai and Hsieh, the target of the

study was to fabricate low pass filters while also varying the firing profile to determine what effect the firing profile has on the DuPont<sup>TM</sup> 9k7 substrate. As seen in Fig. 3.2, this work demonstrates that there is a change in the shrinkage of the module with respect to the firing profile [17]. Dai and Hsieh demonstrated that the firing profile plays a significant part on the product of the ceramic and therefore has to be carefully monitored when fabricating test structures that analyze LTCC shrinkage. The product did not include any details on if the change in length was specific for a design or dimension based on the input into the structure other than just the measurements of the change in length over the original length.

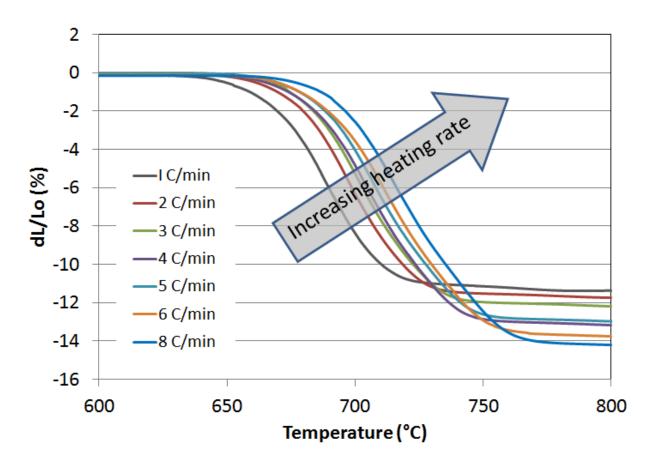


Fig. 3.2. Effect of increasing heating rate from Dai and Hsieh [17]

#### 3.3 DETERMINATION OF LTCC SHRINKAGE VARIATIONS

In this study the main goal was to correlate the LTCC manufactures certificate of analysis (COA) on the shrinkage to the shrinkage experienced in the LTCC panel when fabricating the design. This not only provided a basis on how the tape was behaving but it could also correlate the effects of the design being manufactured to the tape used in the fabrication. This provided the means to correlate the design back to original manufacturing of tapes. At the end of the study the main effect was accomplished by using another design of experiments-derived equation. This new equation consisted of parameters such as incoming COA, lamination pressure, metal loading, and mechanical features, and firing shrinkage [15]. Since each of these effects leave out the effect of the via fill, this provided an area of study and again the focus of the thesis since the amount of metal loading was only based on the conductor layers and not the amount of metal inside the vias.

#### 3.4 SHRINKAGE FIELD MAPPING

To finally conclude the different ceramic models presented, the last study did not follow the same design of experiments philosophy when studying the ceramic, rather the experiment focused on how the shrinkage was characterized. Lenz et al. took a ceramic tape with a specific lamination profile to assemble the tape with 100 punch locations to measure the change in length. The dimensions were then taken manually with a measurement microscope, and the dimensional data was correlated back into shrinkage and plotted as a function of distance. This plot was fit to a parabolic regression that was then used to described as the characteristic shrinkage, C<sub>0</sub>, with the inhomogeneous shrinkage defined by C<sub>1</sub> in Eq. (4)[14]. These constants now provided a means of qualitative measuring and characterizing the ceramic with new metrics that provided more information other than a number on how much a ceramic shrunk.

$$S_{Lxy}(r) = C_0 + C_1 r^2 (4)$$

$$\Delta S_{Lxy}(r) = S_{Lxy}(r) - C_0, \qquad \Delta S_{Lxy} = 0 \pm 0.05\%$$
 (5)

The second equation of the shrinkage, S, with respect to the length in the xy-direction was then calculated with respect to the polar distance. The inhomogeneous region,  $\Delta S_{Lxy}$ , was then calculated from the best fit regression and was determined to be between 0.05% over the entire panel. These equations provided a new method provided the means to qualify the ceramic and some of the effects seen in the ceramic. It also took a long time to take all the dimensions due to the manual process of optical measurements. This did not allow for quick calculations of the shrinkage and meant that processing a design would take a significant amount of time rather than being able to quickly iterate though different designs. There was also no consideration for how the data was fit or how unfilled vias affected the shrinkage. These features could be critical for improving the analysis of the ceramic and the homogeneous region defined in Eq. (5).

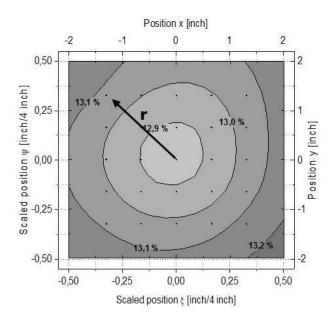


Fig. 3.3. Scaled position vs shrinkage plot from Lenz et al.[14]

#### 4 METHODS

These issues with past studies not allowing the quantification of shrinkage and new methods of shrinkage characterization now lead to the goal of this thesis, to develop a tool that allows for measuring shrinkage quickly and accurately without directly effecting the HiDEC design or fabrication processes. Since the current HiDEC method of characterizing shrinkage is the more common or traditional method with the dimensional data provided by a manually operated micromeasurement microscope, there was an opportunity to compare two different aspects of the ceramic characterization. First, the methods used to take the dimensions to see if the dimensions could be sped up and second the characterization methods used to analyze the ceramic. This section will compare the current dimensional data collection available at HiDEC, the documentation used to then introduce the design coupon used to determine the metal loading, then walk through how the dimensional data is extracted using image processing.

#### 4.1 DIMENSION DATA COLLECTION

For collecting the dimensions of the fired ceramic, there are currently three different tools at HiDEC that can accomplish this process, these tools are the manually manipulated micromeasurement tool, nScrypt 3Dn-Tabletop, and image processing using a photo scanner. These methods were then compared based on metrics that were important metrics for the LTCC process that included adding additional documentation on the process, the accuracy of the method, scalability, and the time required for the processing. A decision table, **Table 4.1**, was assembled to decide on which process would be the best fit, with the lowest score representing the best option.

Table 4.1. Decision Table for Dimensional Collection Tool

	Additional documentation	Method Accuracy	Time Required	Scalability	Total
Micro- measurement	3	2	3	3	11
nScrypt	3	1	2	2	8
Image Processing	1	3	1	1	6

Since image processing added additional documentation and provided a faster process with the ability to scale to higher resolution imaging sources. Image processing was selected since the images used could come directly from the HiDEC scanner and would have enough resolution to resolve the vias. To take the dimensions on the ceramic using image processing was straightforward, however there was a significant amount of documentation that needed to be added to the HiDEC LTCC manufacturing process to document how the panel was created and relate the layout documents to the image.

#### 4.2 **DOCUMENTATION**

With the main goal being to not alter the general LTCC process, the justification to the change in the documentation allows for the ceramic to be analyzed by software. This was accomplished by a few changes which manly focused on including a process manufacturing document. This document now allowed the ceramic fabrication process to be recorded, which allowed for documentation to describe the detailed fabrication steps. The next step in the software documentation was to separate the CAD layout documents into two separate files. In the current method, the expanded and original size documents are contained within the same AutoCAD file. This does not allow the layup file to properly assess the design based on the layout file, by separating the expanded panel and the original panel, this now allowed a common layup file to be

generated that was able to analyze the expanded and original sized panel. By also moving the layup file from PowerPoint to Excel, this now allowed MATLAB to read the file into a centralized location that provided a framework for the ceramic to be analyzed. This now allows a common structure of LTCC manufacturing while enabling the software to track the design parameters along with the process parameters used in the manufacturing. Since there were no modifications preformed on the HiDEC manufacturing process, the additional information of measuring the firing profile, lamination pressure, and other process variables, the variability of the process was unable to be tracked; Thus, there were assumptions that had to be made on the manufacturing process.

#### 4.2.1 LAYUP FILE

The layup file is one of the most critical documents since it explains how the LTCC is to be handled. This file attempts to summarize the complexities of the LTCC such as alternating directions of the tape and the material being used in the file. The information in the layup file references the specific material to be used, but it does not contain reference into the batch information. This document is also filled out in a colorful fashion so that the LTCC operator has a reference for how the tape layers stack along with a reference on if there are cavities located inside the tape. An example of this layup file can be seen in Fig. 4.1.

ead:	UARK (Zeke Zumbro)								
	Print or Image Da	nt n	La	jer Informa	tion				Orie
	Type	Material				Description/AutoCAD Layer		Tape Information	Alt
	Турс	1-lacellal	100	erraamber	OF IT IN YIGH GHOT	Description and COND Eager		rape information	I CHI
	Alignment	CROSS	•			TP10mil			
	Boundary	Hot Knife				cutline			
			П						
	Via Fill	LL601		TP1		TP msk	Ag	9K7X	
	Punch				Machine 2	TP10mil			
			Н.				-		+
			Η.						+
	Via Fill	LL601	$^{\dagger\dagger}$	TP2		TP msk	Ag	9K7X	
	Punch				Machine 2	TP10mil			
			Ш						
			-						+
	Via Fill	LL601	+	TP3		TP msk	Ag	9K7X	_
	Punch	22001			Machine 2	TP10mil	~9	OKIA	
			$\top$						
	Via Fill	LL601		TP4		TP msk		9K7X	-
	Punch	LL601		1174	Machine 2	TP10mil	Ag	9878	₩.
	1 dion		+		1-1doffile 2	11 1011111			
	Via Fill	LL601	$\perp$	TP5		TP msk	Ag	9K7X	-
	Punch		+		Machine 2	TP10mil			
			-						+
			Τİ						
	Via Fill	LL601		TP6		TP msk	Ag	9K7X	
	Punch				Machine 2	TP10mil			

Fig. 4.1. Layup file example of the 10\* and 12\* tiles used in research

#### 4.2.2 LAYOUT FILE

The layout file can be made from different software, but it simply contains reference to the via punch locations, and screen layouts for each screen used in the design. This file has the most information used for the system since this is how each layer's metal is calculated and it also contains reference to where the metal is in the design. This layout file is related back to the layup file in the fact that the layer names can be used to describe how the specific layer is handled. This file does not have to be limited to AutoCAD, however it is the easiest source to modify and add additional layers and scale the original file to create the manufacturing files.

#### 4.2.3 IMAGE FILE

The image file type for the beginning of the project was tagged image file format (TIFF) due to the less "lossy" nature of the file format, however others could be selected with other options selected to maintain the image quality needed for the image processing, but other sacrifices could be made to allow for the algorithms to work the same. This file needs to be a high-resolution image

of the LTCC and it could be replaced with other images of the structures. This image file for the case in this thesis was only the top image of the LTCC, additional images could be used for the back and if other equipment was purchased, these images might consist of internal metal layers and via structures that could be used to analyze layer to layer shrinkage.

Initial scanned images were 600dpi resolution, but by changing scanners to a HP4370 series the resolution was able to increase to 1200dpi. This allowed for scanning of accurate via locations which allowed for changing the search algorithms for a via. The scanner was also driven by different software so that the entire scan area was not imaged providing a faster scan with less area to be processed by the software. The differences in the scanners are highlighted in Fig. 4.5.

#### **4.2.4 LOG FILE**

The log file, or the process traveler, is the simplest of the documents generated in the LTCC process. This file contains reference to the physical materials used in the manufacturing process including the batch numbers, lamination profiles, and other information important in the manufacturing process. This file is the first file read by the system to so that it could then look for the rest of the files associated in the log file. A sample of this is seen in Fig. 4.2.

Panel Name:	72C	Description	Start	November 1, 2017
Quantity:	1	Test panel for design and shrinkage	Finish	November 3, 2017
Fabrication Step		Comments	Files	Serial Number
File	UAR		C2-TDP-Tiles_8.7design.dxf	C2-TDP-Tiles_1xdesign.dxf
Таре	UAR	9K7X - 6 x 10 mil (L1-L6: 10mil) - Precondition	10mil_via_1xdesign_20171110.xlsx	BN24-1001
Punching	UAR	Machine 2 - LL601		BRP267
Screen Printing	UAR			
Lamination	UAR	L1-L6: 3000psi		
Firing	UAR	UAR 9K7 box oven profile - 5572 Center		
Measurement	UAR	72C - Cross - [Vertical, Horizontal]	1200	120
Panel Name:	72B	Description	Start	November 1, 201
Quantity:	1	Test panel for design and shrinkage	Finish	November 3, 201
Fabrication Step		Comments	Files	Serial Number
File	UAR		C2-TDP-Tiles_8.7design.dxf	C2-TDP-Tiles_1xdesign.dxf
Таре	UAR	9K7X - 6 x 10 mil (L1-L6: 10mil) - Precondition	10mil_via_1xdesign_20171110.xlsx	BN24-1001
Punching	UAR	Machine 1 - LL601		BRP267
Screen Printing	UAR			
Lamination	UAR	L1-L6: 3000psi		
Firing	UAR	UAR 9K7 box oven profile - 5572 Bottom		
Measurement	UAR	72B - Cross - [Vertical, Horizontal]	1200	120

Fig. 4.2. Log File snapshot of the 72C and 72B tiles

#### 4.3 ASSUMPTIONS

As a part of the fabrication there were three assumptions that went with the making of the panels so that the HiDEC fabrication process was not extensively altered to produce the panels used in this thesis. The assumptions could be removed in future work, but additional documentation that would have been needed in the process to validate the process parameters were constant during the fabrication process. The combination of these assumptions would be best represented as a black box over the HiDEC LTCC process with the general conclusion that the process remained the same though the three different fabrications.

The first assumption is that during the HiDEC thick-film process all the manufacturing parameters remained the same for each of the panels during fabrication. This is only assumed since there is not a piece of equipment that can be recorded by a computer. The second assumption is that every panel is perfectly planar to the photo scanner. This assumption provides the basis to allow the photos to be uniformly processed so that the shrinkage is properly calculated for each via. In future work this assumption can be removed assuming that there are different measurements

for determining the z-depth of the panel such as a stereographic measurement or just a height scan of the panel. Additional effects such as metal loading locations can also be measured and additional effects such as cracking in full thickness tape features (FTTFs) could be measured and predicted. The final assumption is that uniform shrinkage is measured for each via through the entire Z direction of the panel. This uniform shrinkage is to say that the via rods that run though the entire z dimension of the panel are accurate measuring sticks for how that region of the panel is shrinking. This means that taking relative measurements to the center of the panel allows for accurate measurements of the shrinkage of the panel. This assumption is only specifically for the symmetrical design in the thesis, but this would need to be continued to be true for future complex LTCC designs as well.

#### 4.4 TEST COUPON

A specific design test coupon was used to correlate the shrinkage of the oven profile and the metal loading effect of the vias of the panel. The test coupon was drawn from a modified coupon created by a Missouri Science and Technology (MS&T) senior design project with additional alignment vias seen in the AutoCAD layout in Fig. 4.3. These alignment vias provided a way to allow the software to correct for any misalignment when the scans were generated. The coupons were fabricated in a way to take advantage of the equipment, meaning that the only differences between the fabrication files would be that they use the two different via punch machines to manufacture the files. The profiles were selected to consist of 6 ceramic layers to mitigate any sort of warping seen in the ceramic due to the metal loading effects. The vias were also filled with LL601 paste since the sliver system was selected for low cost fabrication.

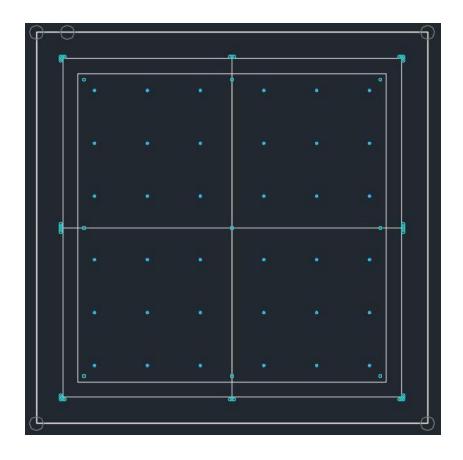


Fig. 4.3. AutoCAD screen shot of test coupon.

After via filling and cutting the coupons to size there were two different lamination profiles that were applied to the panels. To simplify the naming convention the 12\* corresponds to the panels that were punched with 12 mil vias, the 10\* corresponds to the panels that were punched with 10 mil vias. There were different limitation pressures as mentioned in the log table, the first consisted of a 2-stage lamination with the two adjoining layers being laminated first then the entire coupon being laminated together after that. The \*A and \*C coupons were laminated using just the single step lamination. These different lamination profiles were an attempt to mitigate the 30µm crowning effect around the via seen in Fig. 2.3. To minimize some of the effects of the firing profile, the tiles were placed on a setter plate in the same proximity to one another, this allowed

the tiles to be fired at the same time so that any issues with the firing profile could be mitigated, the placement on the setter can be seen in Fig. 4.4.

**Table 4.2. Lamination Profiles Used for Fabrication of Modules** 

Lamination	A	В	С
Step 1	L1-L6: 3000psi	L1-L2: 3000psi	L1-L6: 3000psi
		L3-L4: 3000psi	
		L5-L6: 3000psi	
Step 2		L1:2-L3:4-L5:6:	
		2500psi	

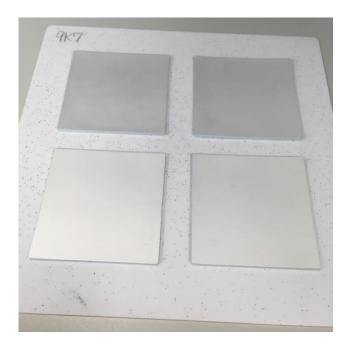


Fig. 4.4. Example of 50mm x 50mm tiles on setter plate after firing.

The metal loading difference between the two panels are solely based on the filled vias inside of the panel. The amount of metal inside the panel could be calculated from a cylinder volume equation, multiplied by the number of vias that were being filled. For this instance, there

were 36 vias allowing the difference in metal loading be a simple scalar, for the 304.8 $\mu$ m (12mil) via panels they had a metal content of 4.003 mm<sup>3</sup> while the 254 $\mu$ m (10mil) via panels had 2.780 mm<sup>3</sup>. This difference was assumed to be measurable though the system. The 9 blank vias were 508 $\mu$ m (20mil) in diameter to start which left an approximate volume of 2.780mm<sup>3</sup> in the green state.

#### 4.5 IMAGE PROCESSING

The image processing script worked though the specific image that was referenced by the log file. This image typically had a resolution of 1200 pixel per inch (PPI or dots per inch (DPI)) and was taken by a common document scanner. This scan is then used to correlate different features that could be related back to the original manufactured documents to calculate the shrinkage of LTCC back to the original files. The whole purpose of this script is to condition the image so that it can be analyzed using a different analytical tool later and so that larger categories for the via locations could be used to describe the panel.

# 4.5.1 DOTS PER INCH (DPI) SIGNIFICANCE

The pixel has two important roles in this thesis, first it determines how large the panel is based on the density of the pixels and second it determines the color range that is needed for the thresholding value that is used for removing all unneeded pixels associated with the images. This is important due to the large image size that is required to handle the 100 mm x 100 mm ceramic squares. The reduction of the number of pixels that is handled by the software is important in order to speed up the system while not affecting the analysis at the end of the process. Since the images were scanned at a 25.4/1200 mm per pixels, the pixel size could be calculated at 21.16µm. The effect of the pixel can be seen in Fig. 4.5, when looking at the high-resolution image. The vias in the image become

described by more pixels, allowing for the image processing software to better approximate the center of the via.

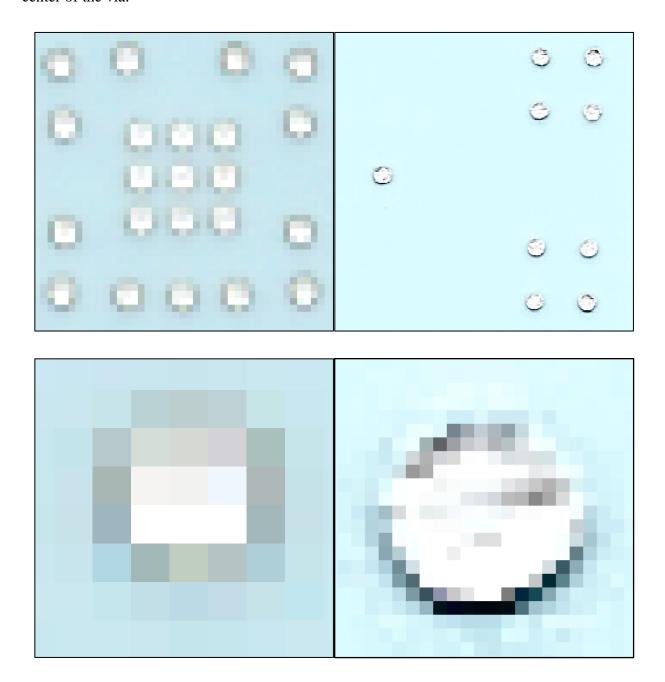


Fig. 4.5. (top left) Zoomed in image of 600dpi via structure (top right) zoomed image of 1200dpi via structure (bottom left) single via in 600dpi (bottom right) single via in 1200 dpi

#### 4.5.2 INITIAL IMAGE PROCESSING

The main LTCC panel image could typically be controlled by the scanner to only have a small 0.25" boarder around the LTCC. The first step was to condition the image by removing the background, this was accomplished by running a few MATLAB commands to determine the "regions" of the image. These regions in the image were determined by reducing the amount of colors in the image from 256 down to 32 colors, allowed a larger window for the thresholding of different colors to determine the panel location. Since the ceramic had a distinct color it was easy to program the computer to only identify the corresponding color and by turning all the other colors to black and saving a new image, the computer was then able to save a new grey scale image that could be analyzed, as seen in Fig. 4.6. The MATLAB function, bwboundaries(), could then find all the boarders of the binary image and then could be queried to determine the areas of the regions, seen in Fig. 4.7. The next step was to find the largest area and crop the size of the ceramic, creating the bounding box of the ceramic. Since the binary image has the same pixel size as the original image, the bounding box from the binary image could be used in the original image to create a smaller size image speeding up the coming algorithms. The smaller image was now approximately the size of the ceramic tile that was being manufactured.

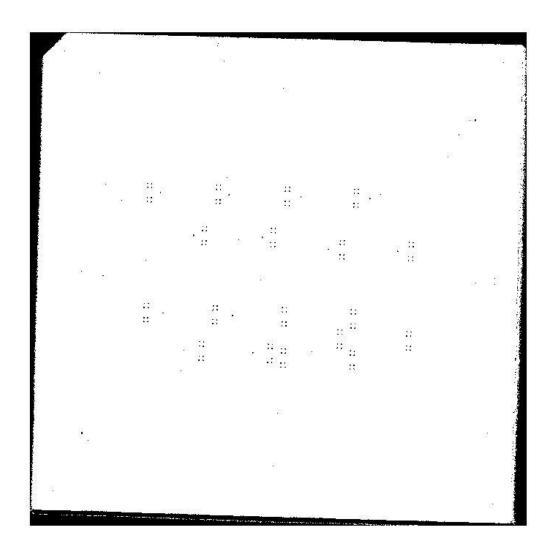


Fig. 4.6. Cropped binary image after processing the map data and filtering for the color of the ceramic.

# 4.5.3 ROTATION AND ALIGNMENT OF THE IMAGE

Since no alignment is perfect on the scanner, the smaller image is typically oriented with a slight theta offset with respect to a XY plane. To correct for this rotation and offset, an alignment layer is created in the layout document which only contains reference to vias that are not filled during the LTCC process. A MATLAB function called *imfindcircles()* is then used to find all the vias

based on the given input radius range, and returned back the approximate size and xy-coordinates of the via. The radius range is determined from the number of pixels that it takes to describe a via, and for this specific application there were either 5 or 15 pixels which corresponded to a radius that was between 105.8-317.4µm. After returning a list of possible via locations, the next step was to align them to the closest point on the 1x layout panel. This was accomplished through a series of thresholding values that filtered the results only if they met requirements based on the angle and the distance the coordinates were found at with respect to different alignment marks. After relating the alignment vias to the 1x panel, the theta rotation is was then calculated so that the panel perfectly aligned with the original CAD and the XY plane. After rotation, the new image also went back though the original cropping of additional boarders to remove any black boaders around the entire panel.

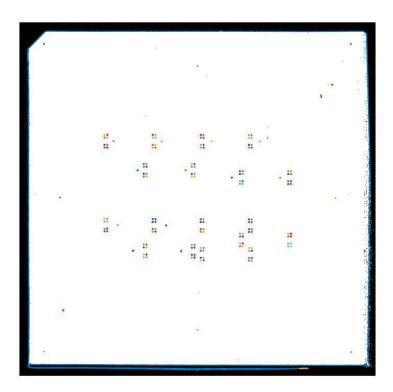


Fig. 4.7. Cropped rotated image with regions shown in multiple colors.

#### 4.5.4 CORRELATION OF VIA LOCATIONS

The small cropped image and 1x panel are aligned leaving the next step to determine the locations of all the vias within the image and relate them back to the 1x panel. This was accomplished again with the *imfindcircles()* command which returned a list of possible centers for all the vias. The via locations were found and the center point of the panel was calculated from the alignment points, an algorithm was then used to determine the likelihood that the found via matched the 1x panel via, these were sorted based on the distance to the center and the angle at which the via should be located. With additional thresholds around the tolerable distance from the center to the via location, the vias are then put into an ordered list so that the 1x panel via locations now matches the image in processing order. At this point the image and the 1x panel match, and since the expanded panel has the exact same order for the same vias, a distance for shrinkage of the each via is calculated and put onto a large matrix, the distance matrix, that related each point to a different point in Eq. (6). The distance matrix, M, is size n x n with the distance calculated from each point to one another with n being the number of vias found in the image. This can also be used for the manufacturing documents to compare those to the image as well. As expected, the distance matrix matches a hollow matrix where the diagonal is zero, due to the zero distance of the same via to itself.

$$\mathbf{M}_{ij} = \sum_{i=1}^{n} \sum_{j=1}^{n} \sqrt{\left( \left( p_{jx} - p_{ix} \right)^{2} + \left( p_{jy} - p_{iy} \right)^{2} \right)}$$
 (6)

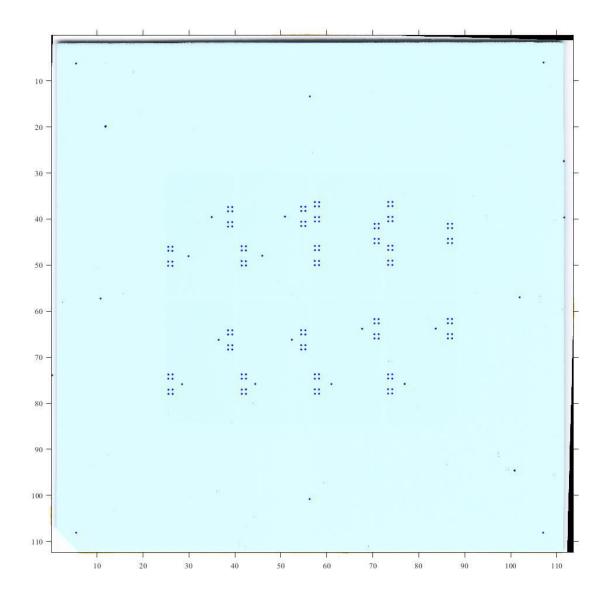


Fig. 4.8. Panel with mm dimensions with locations of the image process points

# 4.5.5 SHRINKAGE CALCULATION

After calculating the distance matrixes for the expanded panel, 1x panel, and image panel, the shrinkage can be easily calculated by taking the difference of the expanded matrix to the image panel, then dividing by the expanded matrix as seen in Eq. (7). Once the percent shrinkage matrix is calculated, there is not much else to do than analyze the data to better understand how the data is fits over a regression curve, which is calculated using Eqs. (8) and (9).

$$\mathbf{M}_{\% \, shrinkage} = \left(\frac{\mathbf{M}_{expanded} - \mathbf{M}_{final}}{\mathbf{M}_{expanded}}\right) * 100 \tag{7}$$

$$S_{parabolic}(r) = C_2 r^2 + C_1 r + C_0 \tag{8}$$

$$S_{linear}(r) = C_1 r + C_0 \tag{9}$$

This percent shrinkage matrix in Eq. (7) can then be used to calculate the effects of the shrinkage with respect to any distance, however, for most instances the shrinkage is considered to be centered around the middle of the panel. The due to the lack of explanation in Lens et al, on why the linear effect of the parabolic regression was removed, Eqs. (8) and (9) were used to determine the coefficients for the parabolic expansion, and linear expansion denoted by the letter "C" in the equations. The two approximations were evaluated for this work, which consisted of the following terms  $C_2$ ,  $C_1$ , and  $C_0$  where all refer to the constants that describe the rate change with  $C_2$  having the units of percent shrinkage per mm²,  $C_1$  having the units of percent shrinkage per mm, and  $C_0$  being defined as the characteristic shrinkage having the percent shrinkage as its unit. It was also assumed the variable r in Eqs. (8) and (9) only referred back to the coordinate system used for determining the shrinkage with respect to a variable. Once these terms were defined, the analysis on how these terms were affected could begin.

# 4.6 SHRINKAGE FIELD MAPPING REGRESSION

Since the data had been generated for the corresponding tiles, the next step was to validate the data using different regression tools such as a parabolic fit and linear fit as seen in Eqs. (8) and (9). The distances used for the regression were varied from the distance to the center along the x and y-dimension, absolute x and y-distances, and polar distance as well. To capture how well the line fit the data, a window of  $\pm 0.25\%$  was used to determine what percentage of data points fell in that

window. These results were then compiled in the table comparing the measurement methods, shrinkage methods, and algorithm methods for the shrinkage field mapping. These different regression lines are seen in the figures below with the  $\pm 0.25\%$  threshold windows for each of the fit models. This now concludes the methods for extracting data for the different best fit models.

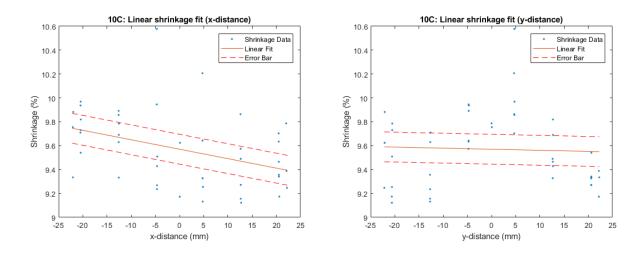


Fig. 4.9. Linear regression fit of shrinkage versus x-distance (left) y-distance (right).

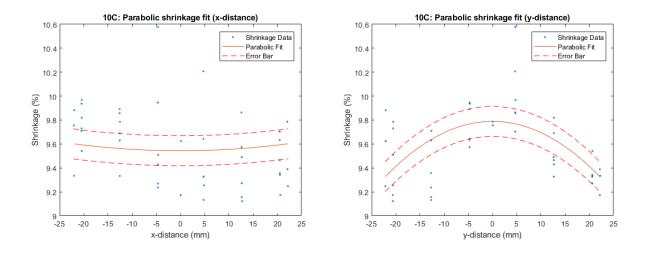


Fig. 4.10. Parabolic regression fit of shrinkage versus x-distance (left) y-distance (right).

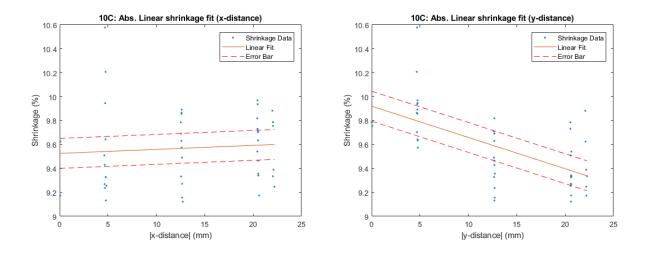


Fig. 4.11. Linear regression fit of shrinkage versus absolute x-distance (left) absolute y-distance (right).

# 5 ANALYTICAL RESULTS

The methods behind the data have been presented and the data is ready to be analyzed. With the focus of the thesis not to change anything in the HiDEC process, the first step in the analysis is to validate the image processing tool. This is accomplished by comparing the system to available measurement systems such as a micro-measurement microscope and the nScrypt tabletop. After validation of the dimensional extraction tool, the next step is to compare the methods for shrinkage characterization. This will be broken down into three sections relating to the methods currently used for characterization: the traditional characterization, the center point characterization, and the shrinkage field mapping characterization. The shrinkage field mapping method will be the most extensive section since it expands on the work by Lenz by adding a faster measurement process, while also providing the measurements on how design affects the characteristic shrinkage of the LTCC panel [14].

### 5.1 COMPARISON OF THE MEASUREMENT SYSTEMS

With measurement system there is always the metric of how accurate the measurement method can correctly measure the dimension without any error. In the imaging processing method, the limiting factor was its ability to extract the via center from the large pixel size of the image. To compare the time and accuracy of the measurement systems, a panel of 45 vias was selected and measured using each of the measuring systems available. The time for each measurement system used was documented and displayed in **Table 5.1** along with the compared accuracy of each of the models.

Table 5.1. Measurement System Metrics for Panel 10C

	Accuracy	Measurement	Statistical	Statistical
		Time 45	Comparison to	Comparison to
		(10C)	micro-measure	nScrypt
Micro-measure	±0.1μm	45 minutes		Mean: 25µm
				STD: 21µm
nScrypt	±0.5µm	30 minutes	Mean: 25µm	
			STD: 21µm	
Image	21.16µm (pixel	5 minute (scan)	Mean: 80µm	Mean: 72.2μm
<b>Processing (HP</b>	size)	30 seconds	STD: 31.6µm	STD: 34µm
4650)		(image		
		processing)		

From **Table 5.1**, it can be seen that the manual measurements produced an average of  $25\mu m$  difference between the two systems. This error is assumed to be the operator error associated with the system, however when comparing the manual systems to the image processing system the error increases to approximately  $75\mu m$ . This increase in error is due to the large pixel size as discussed before and is the limiting factor for the error. This effect of the limiting measurement error size can be seen in Fig. 5.1, this is assumed based on Eq. (2) where an additional term of the measurement error is added to the change in length to create Eq. (10). The  $e_{measure}$  is assumed to be the worst-case scenario for the measurement, and this accounts for the measurement error in the equation.

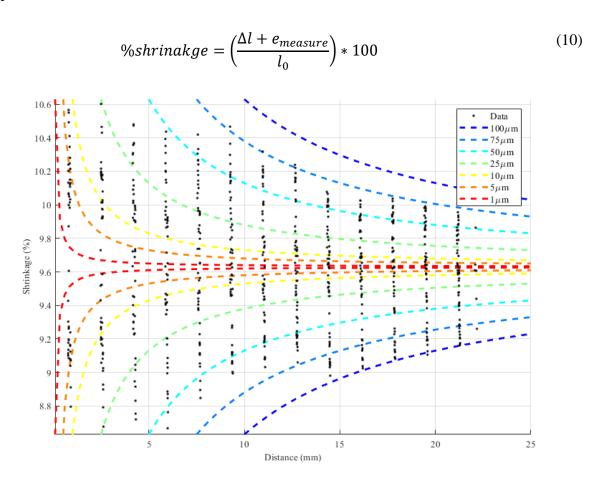


Fig. 5.1. Design sweep of increasing accuracy of the measurement tool with additional module data.

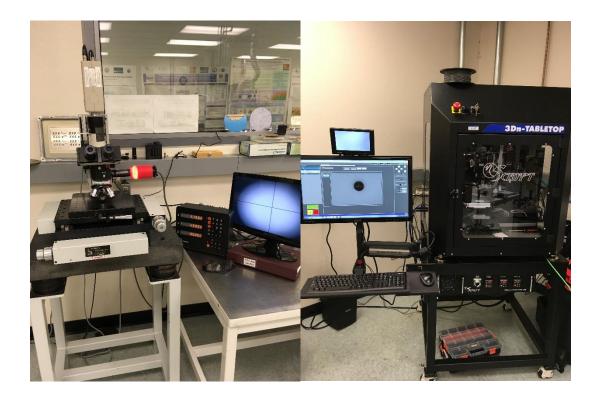


Fig. 5.2. HiDEC measurement systems micro-measurement (left) nScrypt 3Dn-tabletop (right).

One of the main advantages of the image processing system is that there is not a user processing the measurements, thus the error of the measurement is only based on the system and not the user. This issue can be seen when comparing the two manual systems, the nScrypt and the micro-measure system, since there was an average error of 25µm with a standard deviation of 21µm the repeatability of measuring the same ceramic varies based on the user, causing issues in the accuracy of the results. Another disadvantage of using the manual systems is the time it takes to measure the ceramic, the micro-measure system took 45 minutes to extract the data, and the nScrypt took 30 minutes. Using image processing the time was reduced to about 5 minutes of scanning the ceramic with only about 30 seconds of extracting and coordinating the dimensions of the ceramic. In research the time associated with measuring the shrinkage does not often matter, however for a low-cost low-production facility, reducing time for measurements is important since the overall process is very manual.

### 5.2 SHRINKAGE CHARACTERIZATION METHODS

As seen in the measurement methods, the image processing produced a larger error for the models, yet a faster measurement time. Since there were going to be a series of measurements using for all the tiles used in this study, the image processing tool was selected for all the measurements to follow due to the fastest ability to measure the dimensions. There is a final analysis at the end comparing the effects of using the less accurate measurement system which prove that the image process is indeed valid for extracting dimensions, but not ideal for high precision applications.

#### 5.2.1 TRADITIONAL SHRINKAGE CHARACTERIZATION

In the traditional measurements of the LTCC panel most of the measurements would consist of measuring the distance between two alignment points, then take the difference, and then dividing by the original distance found in the CAD document, an example of this would be to take the distance from point 1 (P1) to point 2 (P2) as seen in Fig. 5.3. The direction of this angle could then be specified so that the Y-direction could then be used to see how the shrinkage was affected by the design by that direction. As more dimensions are taken from the different points in Fig. 5.3, the additional measurements provide an average that describes the X-direction and diagonal of the panel. The center alignment point, P9, is removed from this analysis since typical LTCC designs do not include a center via (P9), this P9 will be added later in the center point measurement method.

From taking those series of measurements, Table 5.2 is created allowing the measurement values of the different points with respect to one another. From Table 5.2, an average of the dimensions can be put into another table estimates such as the mean, x-direction, y-direction, and diagonal components of the shrinkage seen in **Table 5.3**. From this table comparing the measurements of the six panels: 10A, 10B, 12A, 12B, 10C, and 12C, is easily plotted to see if there is a threshold that can be applied to the data to draw out any correlation as seen in Fig. 5.4.

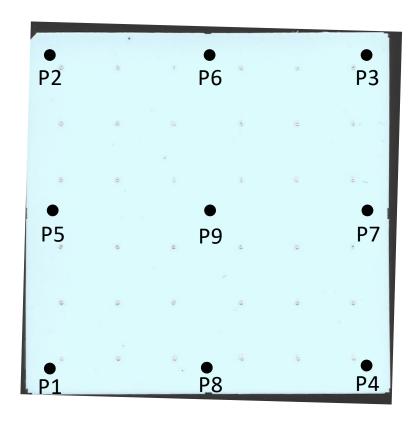


Fig. 5.3. Image of alignment via locations on test coupon

Table 5.2. Shrinkage Measurements for the Traditional Measurement Method System

TRADTIONAL	10A	12A	10B	12B	10C	12C
P1-P2	9.29%	9.66%	9.37%	9.41%	9.29%	9.75%
P2-P3	9.69%	9.78%	9.55%	9.48%	9.71%	9.75%
P3-P4	9.45%	9.40%	9.39%	9.50%	9.26%	9.82%
P4-P1	9.66%	9.79%	9.60%	9.44%	9.68%	9.62%
P5-P7	9.66%	9.84%	9.54%	9.47%	9.79%	9.86%
P6-P8	9.45%	9.59%	9.48%	9.50%	9.38%	9.91%
P1-P3	9.65%	9.76%	9.68%	9.59%	9.65%	9.84%
P2-P4	9.40%	9.55%	9.28%	9.33%	9.31%	9.62%

Table 5.3. Deduced Shrinkage Measurements for the Traditional Measurement Method

TRADTIONAL	10A	12A	10B	12B	10C	12C
MEAN	9.54%	9.68%	9.49%	9.47%	9.53%	9.81%
X-DIRECTION	9.66%	9.84%	9.54%	9.47%	9.79%	9.86%
Y-DIRECTION	9.46%	9.59%	9.48%	9.50%	9.38%	9.91%
DIAGONAL	9.52%	9.66%	9.48%	9.46%	9.48%	9.73%

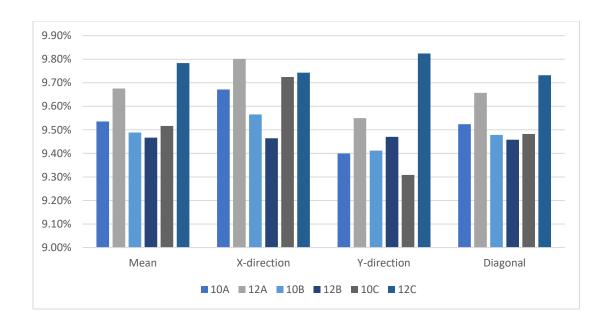


Fig. 5.4. Bar graph of percent shrinkage versus the measurement method for calculating the shrinkage.

With the main goal being to compare the shrinkage to the metal loading design parameter, the traditional measurements did not provide any sort of threshold or some correlation that could be easily deduced. This can be seen from the random shrinkage bars in Fig. 5.4, where there is no obvious correlation of the shrinkage bars with the different metal loading in the panels.

# 5.2.2 CENTER POINT SHRINKAGE CHARACTERIZATION

Unlike the traditional method with uses all sorts of measurements across the panel, the center point method assumes that the panel is uniformly shrinkage around a center point. This assumption results in all the shrinkage measurements are calculated around the point labeled, P9. The same shrinkage calculations are put into Table 5.4, and the same directional deductions put in

Table 5.5.

Table 5.4. Shrinkage Measurements for Center Point Alignment Method

CENTER POINT	10A	12A	10B	12B	10C	12C
P9-P1	9.51%	9.49%	9.50%	9.34%	9.83%	10.09%
P9-P2	9.50%	9.58%	9.04%	9.31%	9.35%	9.61%
P9-P3	9.79%	10.04%	9.86%	9.84%	9.47%	9.60%
P9-P4	9.29%	9.52%	9.51%	9.34%	9.27%	9.63%
P9-P5	9.65%	9.67%	9.45%	9.25%	9.63%	9.75%
P9-P6	9.71%	9.87%	9.46%	9.69%	9.25%	9.79%
P9-P7	9.67%	10.00%	9.63%	9.69%	9.94%	9.97%
P9-P8	9.20%	9.30%	9.49%	9.31%	9.51%	10.03%

Table 5.5. Deduced Shrinkage Measurements for the Center Point Measurement Method

СР	10A	12A	10B	12B	10C	12C
MEAN	9.54%	9.68%	9.49%	9.47%	9.53%	9.81%
X-DIRECTION	9.66%	9.84%	9.54%	9.47%	9.79%	9.86%
Y-DIRECTION	9.46%	9.59%	9.48%	9.50%	9.38%	9.91%
DIAGONAL	9.52%	9.66%	9.48%	9.46%	9.48%	9.73%

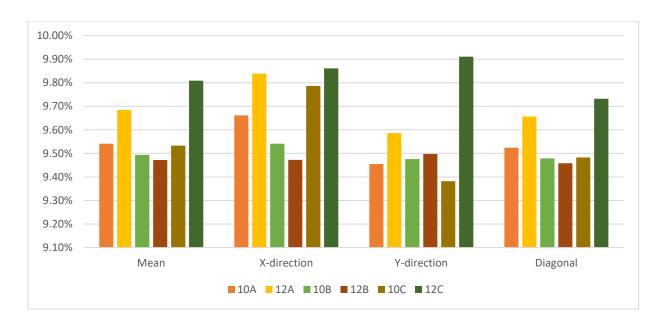


Fig. 5.5. Bar graph of percent shrinkage versus the measurement method for calculating the shrinkage.

Using the data in Fig. 5.5, there is not a conclusive threshold that distinguishes the difference in the via fill amount. There is a distinct step change in all the data relating the 10\* to 12\* of the respective number, however that step change varies in magnitude across the entire data set. The conclusion that the center point method might have added some insight into the fabrication, however it did not yield the expected results.

### 5.2.3 SHRINKAGE FIELD MAPPING CHARACTERIZATION

By including all of the vias in the characterization technique, there is now an ability to track how the shrinkage behaves per unit area rather than the entire panel. The methods for now deducing the shrinkage change since the entire design is used rather than a measured distance. This fundamental shift in measuring the shrinkage is important since it changes the thought that shrinkage is uniform across the panel to shrinkage is uniform in areas of the panel. This new approach provides a way to describe the shrinkage by fitting the data with different polynomials.

These best fit regression models consist of linear and polynomial fits as seen in Eqs. (8) and (9) of the shrinkage data compared to the distance.

For the different regression characterizations, the distance is not limited to just a cartesian system, but rather also polar distances and absolute distances along a specific direction. The tables below contain the characteristic shrinkage for each of the methods measured. The number at the end of the row type refers to the type of fit applied to the data where 1 is linear and 2 is parabolic. The first few letters describe what method was used to describe the shrinkage, R is polar, or Euclidean, distance, X is x-direction, Y is y-direction, and M is the average of the x- and y-directions. Additional metrics such as x-direction absolute distance (XA) and y-direction absolute distance (YA) and the mean absolute distance (MA) are also analyzed. These methods are then plotted in different tables below and provide means of quickly comparing the table.

Table 5.6. Linear Shrinkage Table of Each Ceramic Measured

	X1		Y	1	M1	
	C1	C0	C1	C0	<b>C</b> 1	C0
10A	0.00%	9.51%	0.01%	9.51%	0.01%	9.51%
12A	0.02%	9.64%	0.01%	9.64%	0.01%	9.64%
10B	0.01%	9.51%	0.00%	9.51%	0.01%	9.51%
12B	0.01%	9.58%	0.01%	9.58%	0.01%	9.58%
10C	-0.01%	9.57%	0.00%	9.57%	0.00%	9.57%
12C	0.01%	9.83%	-0.01%	9.83%	0.00%	9.83%

Table 5.7. Parabolic Shrinkage Table of Each Ceramic Measured

		<b>X2</b>			<b>Y2</b>			M2	
	C2	<b>C</b> 1	C0	C2	<b>C</b> 1	C0	C2	<b>C</b> 1	C0
10A	0.00%	0.00%	9.37%	0.00%	0.01%	9.53%	0.00%	0.01%	9.45%
12A	0.00%	0.02%	9.51%	0.00%	0.01%	9.67%	0.00%	0.01%	9.59%
10B	0.00%	0.01%	9.51%	0.00%	0.00%	9.49%	0.00%	0.01%	9.50%
12B	0.00%	0.01%	9.62%	0.00%	0.01%	9.58%	0.00%	0.01%	9.60%
10C	0.00%	-0.01%	9.54%	0.00%	0.00%	9.79%	0.00%	0.00%	9.67%
12C	0.00%	0.01%	9.97%	0.00%	-0.01%	9.87%	0.00%	0.00%	9.92%

Table 5.8. Radial Shrinkage Table of Each Ceramic Measured

	F	R1		R2	
	C1	C0	C2	C1	C0
10A	0.01%	9.29%	0.00%	0.03%	9.11%
12A	0.01%	9.45%	0.00%	0.04%	9.23%
10B	0.00%	9.48%	0.00%	-0.01%	9.54%
12B	0.00%	9.63%	0.00%	0.03%	9.36%
10C	-0.02%	9.95%	0.001%	-0.074%	10.412%
12C	-0.01%	10.11%	0.000%	-0.004%	10.029%

Table 5.9. Absolute Shrinkage Table of Each Ceramic Measured

	X	<b>A1</b>	YA	<b>\1</b>	MA1	
	C1	C0	C1	C0	<b>C</b> 1	C0
10A	0.02%	9.29%	0.00%	9.57%	0.01%	9.43%
12A	0.01%	9.45%	0.00%	9.69%	0.01%	9.57%
10B	0.00%	9.52%	0.00%	9.48%	0.00%	9.50%
12B	0.00%	9.63%	0.00%	9.57%	0.00%	9.60%
10C	0.00%	9.53%	-0.03%	9.92%	-0.01%	9.72%
12C	-0.02%	10.07%	0.00%	9.88%	-0.01%	9.97%

After closely studying the data tables, the contributing factors of the C2 and C1, percent shrinkage per mm<sup>2</sup> and percent shrinkage per mm, can be neglected due to the lack of significance on the effect of the shrinkage. By only analyzing the C0 of each of the metrics a comparison graph is constructed as seen in Fig. 5.6. From the bar graph of just the characteristic shrinkage deduced from the shrinkage field mapping, for each of the pairs of modules there can be seen a step change when comparing the 10\* and 12\* modules in their respective group. Additionally, since there are a variety of regression methods that can be applied, it was decided to reduce the model to only contain reference to the means or the shrinkage with respect to the polar distance.

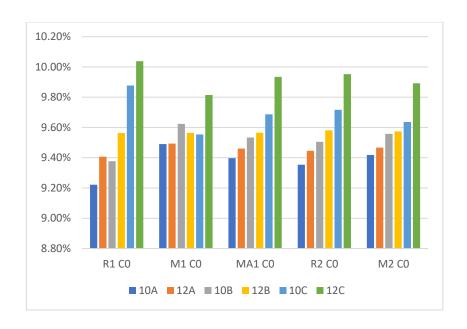


Fig. 5.6. Bar graph of shrinkage field mapping characteristic shrinkages using different regression techniques.

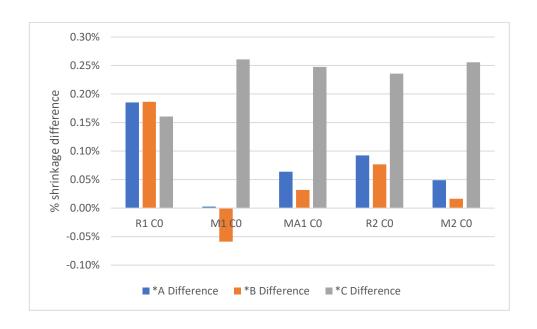


Fig. 5.7. Differential shrinkage plotted for each algorithm.

After forming the data into Fig. 5.7, the regressions produced results that showed that the different via size affected the linear fit shrinkage over a polar distance with an average 0.16% difference for all three modules. While all the other methods produced varying results, this result

did confirm that there was a relative shrinkage difference that could be determined from the different amount of metal loading. This shrinkage field mapping was able to produce a result that was expected, the design parameters do effect the metal loading effects of the LTCC.

### **5.3 SYSTEM ANALYTICS**

Since the measurement system used to deduce the shrinkage field mapping is the most inaccurate method, an additional analysis using the \*C modules was done to confirm the results of the previous systems. To compare all the systems a window metric of  $\pm 0.25\%$  was applied to the curve fit data, the amount of data points that fell within this tolerance were then divided by the total number of points that could have fallen into this window. These results were then compiled into **Table 5.10**, where only about 28% of the data is falling into this window for all the designs with most of the data falling in R1, M1, MA1, R2, and M2 in that respective order.

Table 5.10. ±0.125% Shrinkage Algorithm Metric Windowing Values for the Fabricated Modules

	R1	M1	MA1	R2	M2
10A	25.00%	27.27%	29.55%	25.00%	25.00%
12A	30.95%	26.19%	30.95%	30.95%	30.95%
10B	29.55%	22.73%	29.55%	25.00%	34.09%
12B	31.82%	20.45%	31.82%	36.36%	31.82%
10C	27.27%	27.27%	27.27%	34.09%	29.55%
12C	37.21%	34.88%	39.53%	41.86%	27.91%

Since 30% of the data does not accurately depict most of the data it was then determined that additional work was required to demonstrate that the characteristic shrinkage can be used to

determine if there is different metal loading in the panel. To validate the results from the image processing 10C and 12C were sampled using the nScrypt and micro-measurement systems and then the data was put through the same algorithms used for the image processing. This data was again formatted into similar tables and compared against the same regression as the shrinkage field mapping section with the main intention of comparing the output results of the more accurate system.

Table 5.11. Characteristic Shrinkage of 10C and 12C with Different Measurement Systems

	R1 C0	M1 C0	MA1 C0	R2 C0	M2 C0
10C	9.88%	9.55%	9.69%	9.64%	9.72%
12C	10.04%	9.81%	9.93%	9.89%	9.95%
10C-nScrypt	9.71%	9.51%	9.59%	9.57%	9.62%
12C-nScrypt	10.00%	9.70%	9.83%	9.79%	9.86%
10C-micro	9.69%	9.53%	9.59%	9.57%	9.61%
12C-micro	10.00%	9.71%	9.84%	9.80%	9.87%

As seen in **Table 5.11**, the results produced almost similar characteristic shrinkages to the image processing method, except for a linear fit of the xy-dimensions. When the data was formatted using the  $\pm 0.25$ , as expected almost 50% of the data was described by most of the algorithms with R1, R2, and MA1 describing over 60% of the data with similar characteristic shrinkages.

Table 5.12. ±0.125% Shrinkage Algorithm Metric Windowing Values for the Other Systems

	R1	M1	MA1	R2	M2
10C-nScrypt	84.09%	56.82%	77.27%	84.09%	56.82%
12C-nScrypt	67.44%	48.84%	62.79%	67.44%	53.49%
10C-micro	70.45%	63.64%	70.45%	70.45%	54.55%
12C-micro	69.77%	41.86%	67.44%	69.77%	48.84%

This comparison only validated that the measurement tools accuracy was able to better measure the characteristic shrinkage more accurately when it came to the best fit of the data, and because of the better fit on the data, the regression tool only amplified the relative difference between the different metal loaded LTCC panels, as seen in Fig. 5.8.

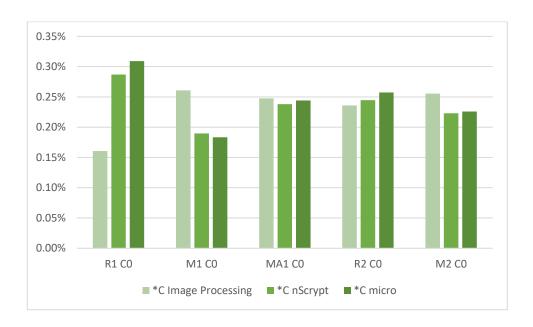


Fig. 5.8. Differential shrinkage measurements for all the measurement systems for the \*C modules.

The shrinkage mapping produced similar results to the previous methods with the mean absolute fit of the data producing the larger 0.25% difference. While this result is different than the 0.16% from the image processing tool, these results confirmed that the image processing method, while faster and less accurate, produce similar almost identical results to the slower measurement systems.

### 6 CONCLUSION

Without modifying the current process, other than including documentation that could be read by different software, analytical results such as the effect of the via size on the characteristic shrinkage can be measured along with reducing the time needed to characterize a ceramic tile. This process can be scaled to measure large quantities of sample points on the ceramic tile, while also incorporating more accurate systems would provide a higher detail of accuracy when it comes to the via measurements. Even with a home-built solution, relatively accurate results were able to be measured while also providing a means to monitor the effect of the processes as they occur on the final product. There must still be work done on the effects of the LTCC process on the absolute value of the panel shrinkage, since the data provided had a large range of absolute shrinkage values. The accuracy of the shrinkage field mapping characterization method will greatly improve the ceramic processing at the University of Arkansas.

#### 7 FUTURE WORK

To improve the state of the art of this system, one must consider reducing the pixel size associated with the measurements, because it is the limiting factor associated with this current method. However, there are challenges associated with accurately measuring the location of the via, and in the grand scheme of things the only thing that matters is the coordinate of the via, so replacing the system with an automatic optical inspection tool could solve this problem of having a large scan time and image processing time.

In the same vein, regarding the generated documentation, additional documentation needs to be built into the HiDEC process to better document the process. The documentation used in the thesis only has a limiting measurement protentional and does not include every detail associated with manufacturing such as lamination pressure over time, temperature over time, flatness of the lamination plates, etc. All of these can be accounted for in the traveler but must continue to be used in the data collection to provide greater insights into the absolute shrinkage of the LTCC panel. By documenting the entire process, this allows the assumptions made in this thesis meaningless since there would be quality control and system controls put on the manufacturing process, which would better document the entire process.

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# 9 APPENDIX

# 9.1 **FUNDING**

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# 9.2 10 AND 12 MODULES SHRINKAGE MAPS

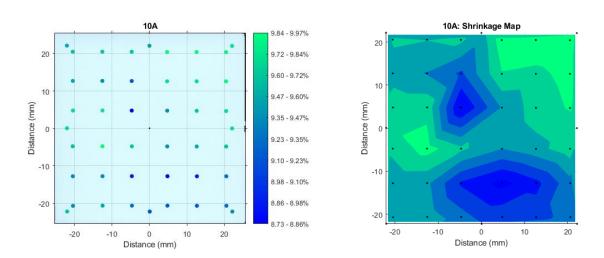


Fig. 9.1. Locations of shrinkage measurements (left) Shrinkage contour map of 10A (right)

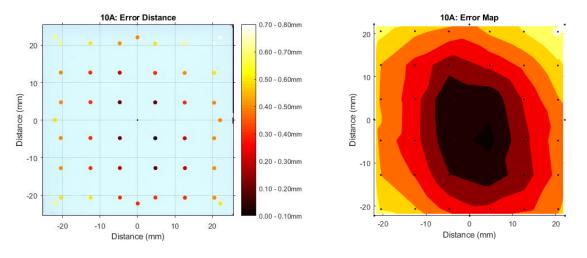


Fig. 9.2. Error distance from center (left) Error contour map of 10A (right)

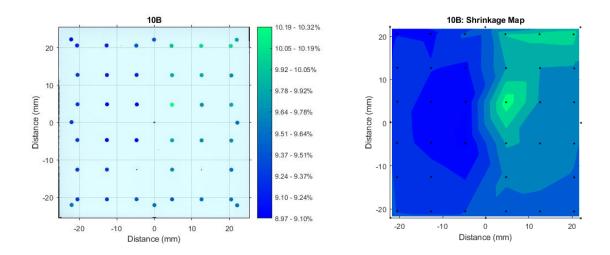


Fig. 9.3. Locations of shrinkage measurements (left) Shrinkage contour map of 10B (right)

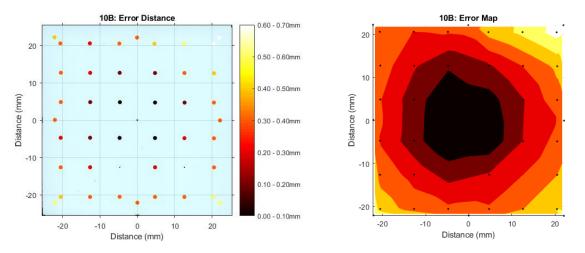


Fig. 9.4. Error distance from center (left) Error contour map of 10B (right)

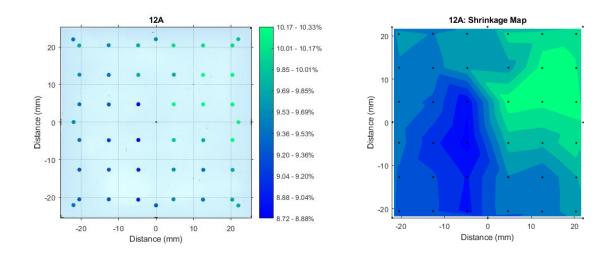


Fig. 9.5. Locations of shrinkage measurements (left) Shrinkage contour map of 12A (right)

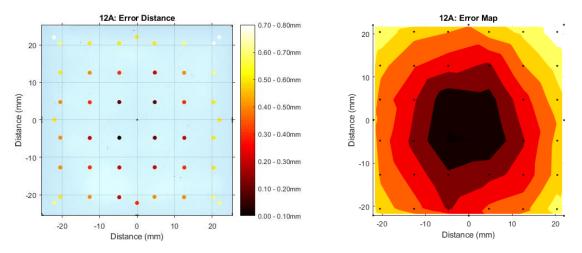


Fig. 9.6. Error distance from center (left) Error contour map of 12A (right)

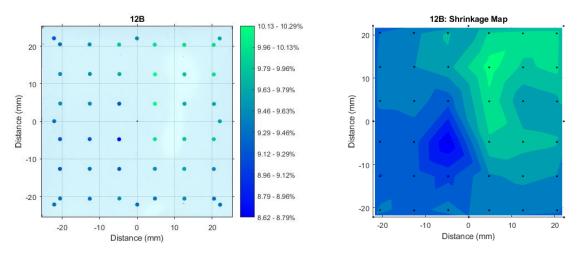


Fig. 9.7. Locations of shrinkage measurements (left) Shrinkage contour map of 12B (right)

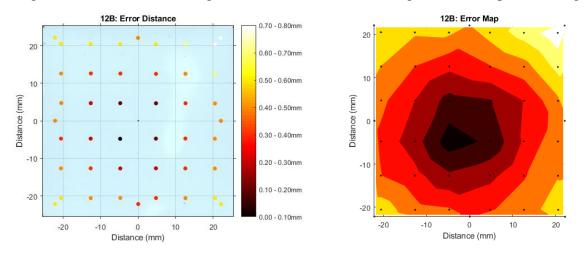


Fig. 9.8. Error distance from center (left) Error contour map of 12B (right)

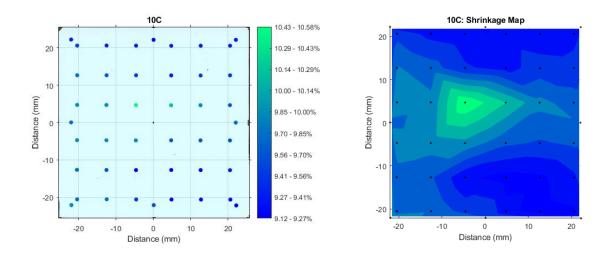


Fig. 9.9. Locations of shrinkage measurements (left) Shrinkage contour map of 10C (right)

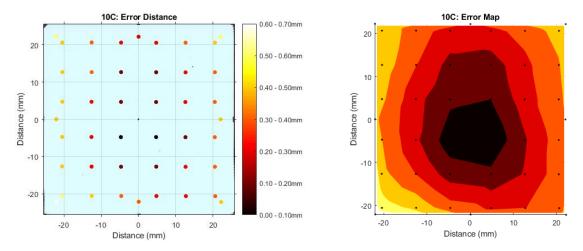


Fig. 9.10. Error distance from center (left) Error contour map of 10C (right)

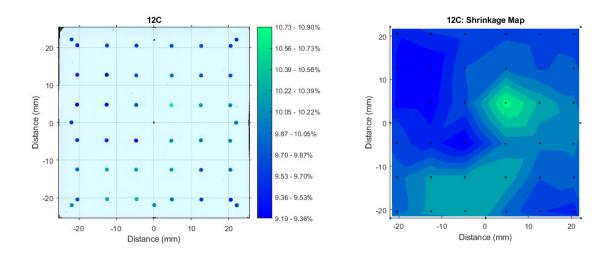


Fig. 9.11. Locations of shrinkage measurements (left) Shrinkage contour map of 12C (right)

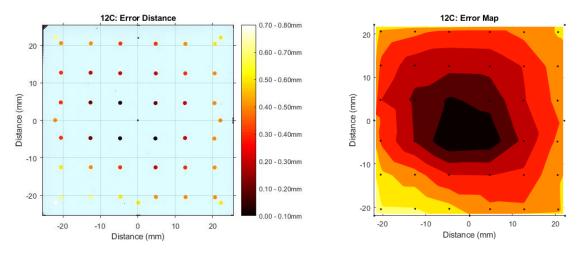


Fig. 9.12. Error distance from center (left) Error contour map of 12C (right)