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An RS-485 Transceiver in a Silicon Carbide CMOS Process

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An RS-485 Transceiver in a Silicon Carbide CMOS Process

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Abstract

This thesis presents the design, simulation and test results of a silicon carbide (SiC) RS-485 transceiver for high temperature applications. This circuit is a building block in the design and fabrication of a digital data processing and control system. Automation processes for extreme environments, remote connection to high temperature locations, deep earth drilling, and high temperature data acquisition are some of the potential applications for such a system. The transceiver was designed and developed in a 1.2 µm SiC-CMOS process by Raytheon Systems, Ltd. (UK). It has been tested with a supply voltage of 12 V and 15 V, temperatures from 25°C to 400°C, half-duplex and full-duplex configurations, and with 2400 ft of category 5e (cat5e) cable. At 400°C, the rise and fall times are 32 ns and 24 ns respectively. The transceiver has been tested with a silicon RS-485 transceiver over temperature in order to characterize the device performance when acquiring data from a hot environment and transmitting it to a cooler environment and vice versa. Finally, high temperature performance over time is demonstrated over 150 hours at 300°C.

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Lastly, I would like to thank my family and friends in Panama and Fayetteville. Thank you for believing I could and for cheering me up when I needed it. A special thanks to the Ramirez family for giving me a home away from home.

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Dedication

This thesis is dedicated to my mother, Maria Teresa Herrera, my father, Didimo Ricardo Benavides, and my brothers, Jose Antonio Benavides Herrera and Ricardo Antonio Benavides Herrera. Thank you for always believe in me, for all the sacrifices, and late-night calls. I could not have done it without your support and unconditional love.

Table of Contents

List of Figures

List of Tables

CHAPTER 1 INTRODUCTION

Over the last decade, wide bandgap semiconductors have gained interest in the power electronics industry for fast switching, high temperature and high voltage. Wide bandgap technologies, such as gallium nitride (GaN) and silicon carbide (SiC), offer significant advantages over silicon (Si) in certain applications [1] – [3]. In comparison to Si, GaN and SiC have higher thermal conductivity, lower intrinsic carrier concentrations, higher breakdown voltage and wider bandgap. These properties enable transistors with higher voltage operation and higher switching speeds, allowing circuits to operate at higher temperatures [4]. In addition, heat removal is facilitated, as well as miniaturization, lower power loss and low cost in electronic systems. On the other hand, the special properties of SiC make it a desirable material for extremely high temperature and high voltage applications. These characteristics include its higher critical electric field, wider bandgap energy and high thermal conductivity [5], as well as the maturity of SiC substrates and process technology among wide bandgap semiconductor materials.

A data acquisition and transmission system across high temperature differentials, between different systems and over long distances is necessary for high temperature industrial applications. Some applications that use the RS–485 standard for data transmission include motor and motion control; industrial and building automation; process control networks; remote terminals; and security systems. The RS–485 is widely employed because of key features such as its wide common-mode range, bidirectional communication, differential transmission over long distances, and the connection of multiple drivers and receivers on the same bus. Conventional Si devices require complex and expensive cooling systems for state of the art harsh environment applications [6], since traditional Si integrated circuits (ICs) are limited to 150°C. Silicon carbide devices, such as an operational amplifier [7] and 8–bit data converters [8] are building blocks for a high

temperature data acquisition system. However, data transmission is necessary to bring the technology closer to a large–scale data processing and data acquisition system for extreme environment applications such as aerospace, deep earth drilling, heavy transport and aviation.

The main objective of this thesis is the redesign of a SiC complementary metal oxide semiconductor (CMOS) RS–485 capable of transmitting data collected in a hot environment to a room temperature environment for automotive applications. In this way, the compatibility of the SiC RS–485 transceiver with a conventional Si based commercial off–the–shelf RS–485 transceiver will be validated.

1.1 Thesis Organization

The thesis is divided into the following chapters.

- Chapter 1: Introduction – Motivation and background of the work are presented here.
- Chapter 2: Background – A general description of the wide bandgap materials with an emphasis on silicon carbide is presented in this chapter. The Raytheon HiTSiC CMOS process and its devices are discussed, as well as circuits designed in this process during the fabrication runs: Vulcan I and Vulcan II. An overview of the RS-485 standard and the design of the Vulcan II RS-485 are described.
- Chapter 3: Circuit Design and Simulation – This chapter describes the complete design process – determining the specification of the circuits from system requirements, developing design equations and using them to build schematics, and simulation of the circuits.
- Chapter 4: Testing and Characterization – This chapter covers the test set up, and procedures performed to test the RS–485 designed in Vulcan II. The test results for different configurations are presented and the results obtained are discussed.

- Chapter 5: Conclusions and Future Work – A summary of the design and test results is presented in this chapter. Goals for future development of a high temperature SiC RS–485 are also discussed.

CHAPTER 2 BACKGROUND

2.1 Wide Bandgap Materials

Silicon devices have dominated the power electronics, information and communications technologies for over 60 years. The properties of silicon that have led to its dominance in the semiconductor industry include its natural abundance and low cost, its natural oxide, and its respectable thermal conductivity, mobility and critical field, not to mention easy manufacturing techniques that have given rise to a mature and very well established process. However, the silicon technology exhibits some limitations regarding operating temperature, switching frequency, and blocking voltage [9]. These limitations have led to an interest in wide bandgap semiconductors. Gallium nitride and SiC have been proposed as the best alternatives to replace traditional Si in extreme environment applications. Some of the properties of these wide bandgap semiconductors are listed in Table 2.1 [10]. Silicon carbide has different crystalline structures called polytypes. The three most common are 3C-SiC, 4H-SiC and 6H-SiC. Polytype 4H-SiC has been the primary focus of recent research and device production.

Table 2.1. Properties of Wide Bandgap Semiconductors Compared to Silicon

PROPERTY	4H-SiC	GaN	Si
Bandgap Energy (eV)	3.26	3.39	1.12
Critical Electric Field (MV/cm)	2.2	3.3	0.23
Intrinsic Carrier Concentration at 300 K (cm^{-3})	8×10^{-9}	2×10^{-10}	1.0×10^{10}
Relative Permittivity	9.7	9.0	11.8
Electron Mobility ($cm^2/V.s$)	950	800(1)	1400
Thermal Conductivity (W/cm.K)	3.8	1.3(2)	1.5

(1) Value for bulk material
(2) Value for epitaxial layer

Overall, gallium nitride and SiC have a wider bandgap energy and higher critical electric field than silicon. A higher bandgap energy reduces the leakage current, since less carriers are generated in the depletion region; while a higher critical field means a higher breakdown voltage. Gallium nitride has a wider bandgap and higher critical electric field than SiC. However, its thermal conductivity is lower, which means that the material does not perform as well at high temperatures. A higher thermal conductivity means the semiconductor can easily dissipate heat. Silicon carbide has three times higher thermal conductivity than silicon. In addition, the intrinsic carrier concentration affects the leakage current at high temperatures. The extremely low intrinsic carrier concentration value for SiC makes it a suitable material for high temperatures. Also, the higher critical electric field and thermal conductivity values for SiC lead to a low device resistance and faster switching devices. The electron mobility value of a semiconductor dictates how much current a particular device can carry. In this way, it is an indication of how fast a circuit can performs. SiC has a lower value for electron mobility compared to silicon, which combined with its low intrinsic carrier concentration leads to SiC being slower at room temperature but suitable for operation at high temperatures because of low leakage currents.

2.2 Silicon Carbide CMOS Process

The RS–485 was designed in a 1.2 µm SiC CMOS process technology developed by Raytheon Systems Limited (UK) called High Temperature Silicon Carbide (HiTSiC®) [11]. The components available in this process include: NMOS and PMOS devices, on-chip resistors, diodes, and capacitors. The process key features are given below:

- 4H-SiC process
- N-type substrate
- Supply voltage of 15 V

- Single metal layer, two layers of polysilicon (one being high sheet resistance poly)
- Operating temperatures greater than 300°C

In this process, the PFET devices are built on the N-substrate, while the NFETs have a P-type well. The bodies of all the PFETs are connected to the highest voltage in the chip, which in this process is the substrate. A cross section of the process is shown in Fig. 2.1.

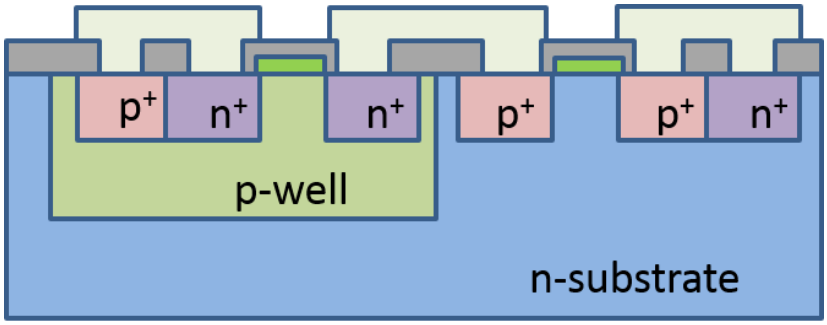


Fig. 2.1. Simplified Cross-Section of the Raytheon HiTSiC CMOS Process

A mixed–signal process design kit (PDK) was developed for Cadence Virtuoso by a team led by the Mixed Signal Computer Aided Design (MSCAD) laboratory at the University of Arkansas to facilitate the design process. Berkeley short–channel insulated gate FET models (BSIM4) were also developed for the SiC FETs [12]. The BSIM4 models were binned at temperatures of 25°C, 100°C, 200°C, and 300°C for the SiC FETs. Process corner models were developed in order to allow designers to learn and understand the behavior from wafer to wafer and reticle to reticle on a single wafer. These models were designed for typical, slow, and fast NFET and PFET devices.

There were two fabrication runs made by Raytheon. The first run, known as Vulcan I, was completed in August 2013, with wafers returning in February 2014. A high temperature phase-locked loop, an operational transconductance amplifier, a Schmitt trigger as well as control logic blocks are some examples of the mixed-signal circuits designed and implemented in this run [13],

[14], [15]. The second fabrication run, referred to as Vulcan II, was completed in September 2014. The wafers returned in April 2015. The RS–485 being reported here was designed and fabricated in the second fabrication run along with other devices such as a gate driver [16], an 8-bit DAC [17], a comparator [18], a linear voltage regulator [19] and digital control circuits [20].

2.3 Overview of an RS-485 Transceiver

The RS-485 is a standardized physical layer for transmission of digital data over a balanced twisted pair medium. The Telecommunications Industry Association (TIA) and Electronic Industries Alliance (EIA) jointly published the standard as TIA/EIA-485-A. The transmission line standard describes the physical layer of the interface of the RS-485. It defines the electrical characteristics of drivers and receivers that could be used to implement a balanced multipoint transmission line. The RS-485 interface is usually used with a protocol such as Interbus, BACnet, Modbus or Profibus, and it is one of the most used physical layer bus designs in industrial and instrumentation applications. The RS-485 circuit consists of a driver with differential outputs and a receiver with differential inputs as shown in Fig. 2.2.

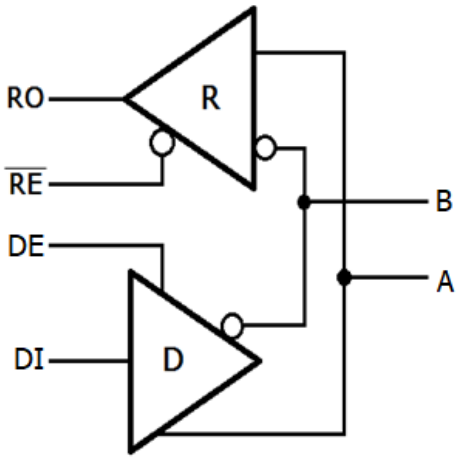


Fig. 2.2. Differential Driver and Receiver

The pins shown in Fig. 2.2 are described in Table 2.2.

Table 2.2. Pin Description for RS-485 Standard

SIGNAL NAME	DESCRIPTION
DI	Transmit Data Input
DE	Transmit Data Enable for driver
$\overline{RE}$	Transmit Data Enable for receiver
RO	Receiver Output
A	Bus Connection
B	Bus Connection

An RS-485 transceiver must have a driver that can be disconnected from the transmission line when a particular node (driver, receiver or transmitter) is not transmitting. The DE pin enables the driver when DE is set to a logic high (DE = 1), while it puts the driver in a tristate condition when DE is set to low (DE = 0). When the driver is in the tristate condition, it is disconnected from the bus and allows other nodes to transmit over the same twisted pair cable. The receiver also has an enable pin which is called $\overline{RE}$ and it enables the receiver when $\overline{RE}$ is set to a logic low ($\overline{RE} = 0$). The signals A and B are the two lines in the differential pair.

The key features of the RS-485 are [21]:

- Differential data transmission
- Bidirectional communication
- Multiple driver and receiver connections
- Wide common-mode range
- Maximum data rate of 10 megabits per second (Mbps) at 40 ft
- Maximum cable length of 4000 ft at 100 kilobits per second (kbps)

2.3.1 Differential Data Transmission

An RS-485 transmission channel requires a pair of signal lines to exchange information (Fig. 2.3) using at minimum a single driver and receiver. A differential data transmission means that the voltage on one line equals the inverse of the voltage on the other line. If a logic high is received on the input of the driver (DI = 1), line A is driven more positive than line B on the output of the driver ($V_{OA} > V_{OB}$). If a logic low is received on the input of the driver (DI = 0), line B is driven more positive than line A ($V_{OB} > V_{OA}$) on the driver output.

Similarly at the receiver, the receiver output is logic high (RO = 1) if line A is more positive than line B on the input of the receiver ($V_{IA} – V_{IB} > 200$ mV) and if line B is more positive than line A ($V_{IB} – V_{IA} > 200$ mV) on the input of the receiver, the output of the receiver is a logic low (RO = 0)

The differential data transmission for the RS-485 standard is for the driver to provide a differential output of a minimum 1.5 V across a 54 Ω load for drivers, whereas the standard towards receivers is to detect a differential input down to 200 mV.

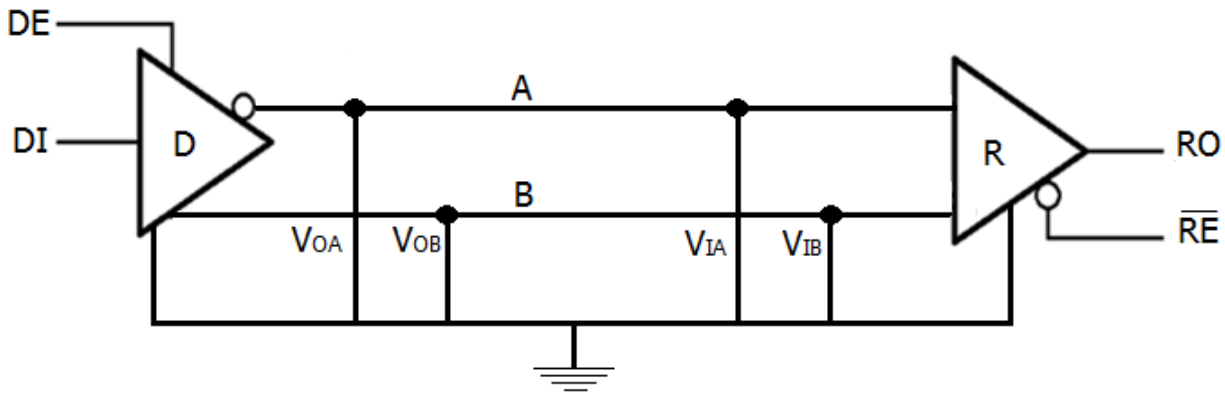


Fig. 2.3. Differential Signaling Interface Circuit

The circuit shown in Fig. 2.3 has equal noise coupling into the system on both signals, since one signal emits the opposite of the other signal and electromagnetic fields cancel each other.

2.3.2 Network Topology

The standard suggests that the nodes (drivers, receivers or transceivers) be networked in a bus topology as shown in Fig. 2.4. In this topology each node is connected to a single cable via short network stubs. This central cable is the backbone of the network and is known as the bus. In this topology the data being transferred may be accessed by any node. The bus can be designed for half-duplex or full-duplex transmission.

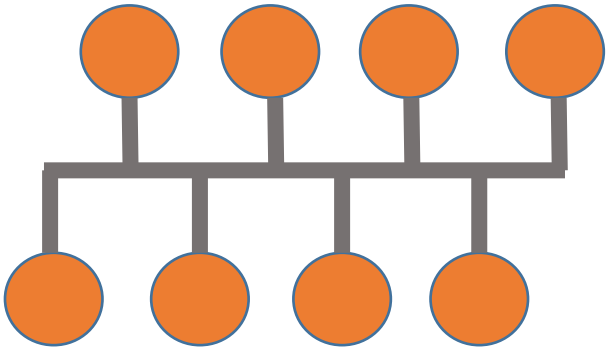


Fig. 2.4. Bus Network Topology

A half-duplex configuration requires one signal pair (two wires). It allows multiple drivers and receivers to be on the same bus and data transmission in both directions, but only one driver can send data at a time. The enable pins for the driver and receiver are used to enable only one driver to send data at a time. A half-duplex bus configuration in RS-485 is shown in Fig. 2.5.

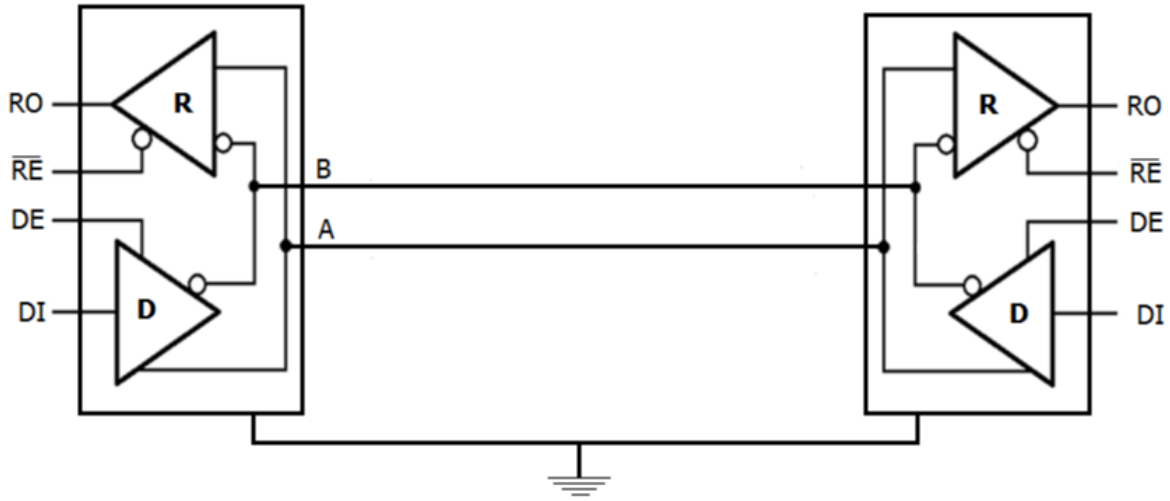


Fig. 2.5. Half-Duplex Bus Configuration

Full-duplex implementation requires two signal pairs (four wires) and transceivers with separate bus access lines for the driver and the receiver. This configuration allows for simultaneous communication in both directions. It allows a node to simultaneously transmit data on one signal pair, while receiving data on the other pair. A full-duplex bus configuration in RS-485 is shown in Fig. 2.6.

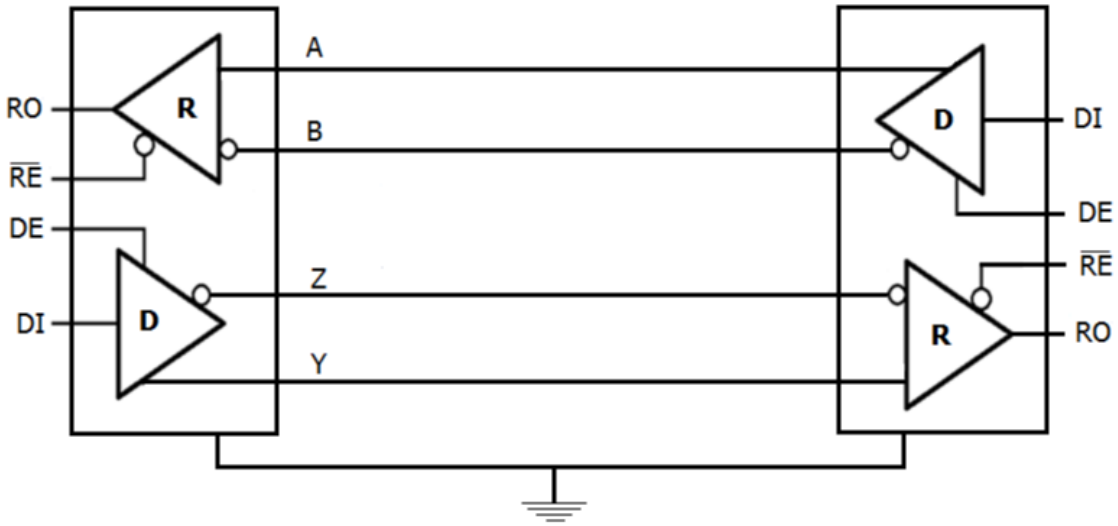


Fig. 2.6. Full-Duplex Bus Configuration

2.3.3 Termination

In order to avoid signal reflections on the line, data transmission lines should be terminated, and stubs should be as short as possible. On long lines, the reflections continue long enough to cause the receiver to misread logic levels, while on short lines, the reflections occur sooner and have no effect on the logic levels received. For a proper termination it is required to match the terminated resistor to the characteristic impedance of the transmission cable. The RS-485 standard recommends a 24 AWG twisted pair cable with a capacitance of 16 pF/ft and 120 Ω characteristic impedance. In this way, the transmission line should be terminated with 120 Ω resistors. A parallel or AC termination could be implemented to terminate the transmission line.

A parallel termination consists on placing two termination resistors in the network regardless of how many nodes are connected. For a half-duplex configuration, both ends of the cable must be terminated. For a full-duplex configuration, the master receiver and slave receiver need to be terminated.

An AC termination consists of placing a resistor and capacitor in series across the bus (between line A and line B). The value of the capacitor is calculated using the following equation

$$C_T(\text{pF}) > \frac{2\ (one\text{-}way\ cable\ delay\ (\text{ps}))}{Characteristic\ Impedance\ (\Omega)} \tag{2.1}$$

The length of a stub, the distance between a node and the bus, should be less than ¼ of a wavelength of the frequency equal to the inverse of the bit period.

2.3.4 Data Rate versus Cable Length

The maximum bus length is limited by the losses of the transmission line and the signal jitter at a given data rate. The jitter is the time deviation from the ideal timing of a data-bit event [22]. A conservative cable length versus data rate of a conventional RS-485 is shown in Fig. 2.7.

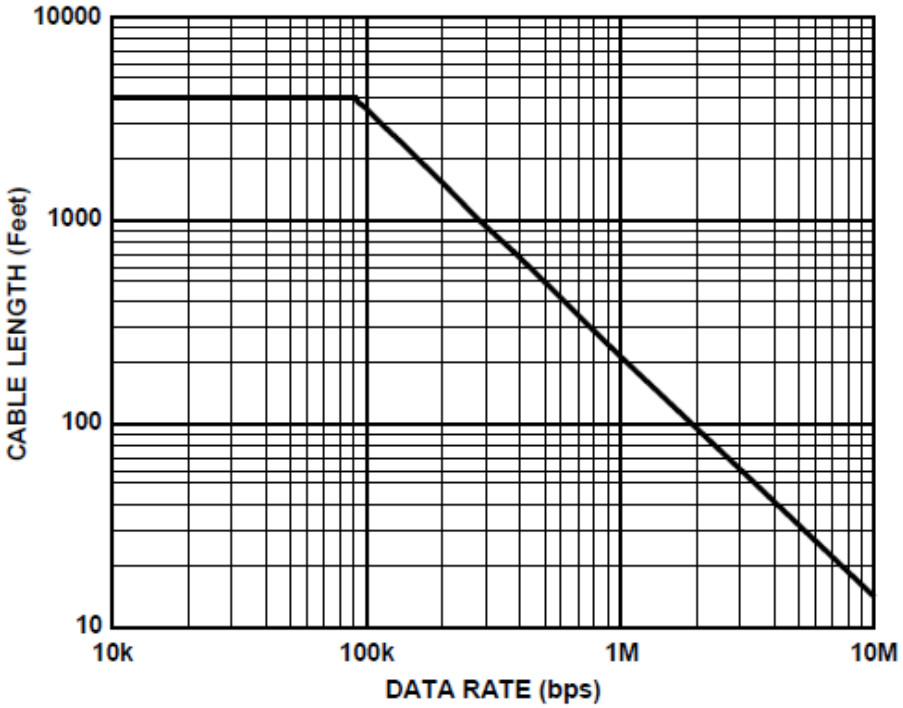


Fig. 2.7. Cable Length vs. Data Rate [23]

When low data rates are used, it is possible to use longer cables. This is the lower frequency range. Here the cable length is limited by the line resistance which approaches the value of the termination resistor. The application is limited to a shorter cable when high data rates are used. Here the driver's rise time mainly determines the data rate and the losses of the transmission line can be neglected [21]. The standard recommends a maximum data rate of 10 Mbps, which according to the graph would be at about 15 ft.

2.3.5 Fail-Safe Operation

The absence of an input signal causes conventional receivers to assume random output states when the input signal is zero. Loss of signal (LOS) can be caused by the following three situations [21]:

- Open circuit: loss of signal due to the disconnection of a transceiver from the bus, or a wire break
- Short circuit: signal loss caused by an insulation fault connecting the wires of a transmission line to another
- Idle-bus: loss of signal that occurs when none of the drivers connected on the bus is active

Fail-safe operation forces the receiver output to assume a determined state under a LOS condition. The differential input threshold voltage (V_{TH}) of a receiver is the receiver input voltage at which a transition, either from low to high or otherwise, of the receiver output is guaranteed. For a standard RS-485, the differential input threshold voltage is ± 200 mV. Table 2.3 shows a truth table for a differential receiver where $\overline{RE}$ is the enable pin of the receiver, $V_{IA} - V_{IB}$ is the differential input, and RO is the output of the receiver.

Table 2.3. Truth Table of a Differential Receiver

$\overline{RE}$	$V_{IA} - V_{IB}$ (inputs)	RO
0	≥ 200 mV	1
0	≤ -200 mV	0
0	-200 mV $\leq (V_{IA} - V_{IB}) \leq 200$ mV	X
1	X	High-Z

In this way, when the differential input is less than or equal to -200 mV ($V_{IA} - V_{IB} < -200$ mV), the receiver output will be low (RO = 0). When the differential input is larger than or equal to 200 mV ($V_{IA} - V_{IB} > 200$ mV), the receiver output is high (RO = 1).

During the bus idle condition, the differential voltage on the bus $(V_{OA} - V_{OB})$ is 0 V. In this way, the receiver output is undefined during the bus idle condition and the receiver assumes random output states. The literature indicates that standard receivers use an external fail-safe circuit that consists of pull-up/pull-down resistors in order to solve this condition [23]. The resistive voltage divider generates sufficient differential bus voltage to drive the receiver output to a determined state. However, a receiver with a true fail-safe operation will have a V_{TH} from -200 mV to -30 mV, which eliminates the need for pull-up/pull-down resistors. As Fig. 2.8 shows, the receiver output is high during the bus idle condition with a true fail-safe bias since $V_{OA} - V_{OB} > -30$ mV. In this way, if all the receivers connected on the bus have a true fail-safe operation, the receiver output will always be defined.

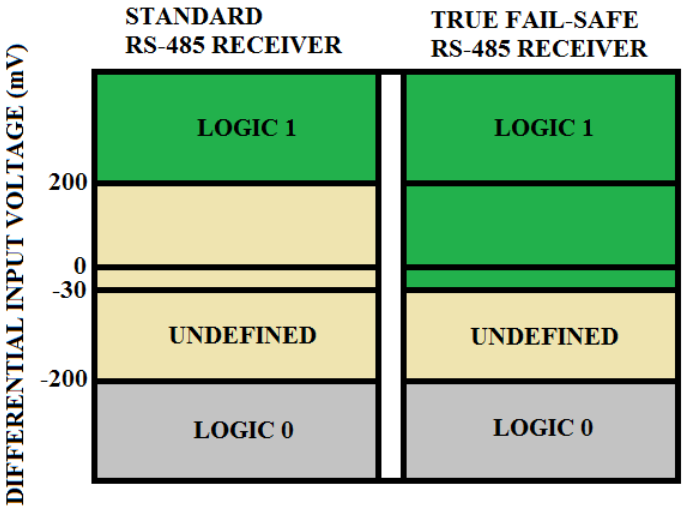


Fig. 2.8. Receiver Input Threshold Voltage

2.3.6 Bus Loading and the Unit Load Concept

The output of a driver depends on the current it must supply into a load. The total load current increases when adding transceivers to the bus. The receiver input impedance for the RS-485 is specified as larger than or equal to 12 kΩ. To estimate the maximum number of bus loads possible, RS-485 standard uses the concept of unit load (UL). A unit load is defined as a load impedance of 12 kΩ. Standard drivers must be able to drive up to 32 nodes. The maximum number of transceivers on the bus is 256 with a UL of 1/8 and with a minimum receiver input impedance of 96 kΩ. Fail-safe bias contributes up to 20 ULs of bus loading. In this way, to calculate the maximum number of transceivers using both standard RS-485 transceivers and true fail-safe transceivers the following equation is used

$$N = \frac{32\ UL_{STANDARD} - 20\ UL_{FAILSAFE}}{UL\ per\ transceiver} \tag{2.2}$$

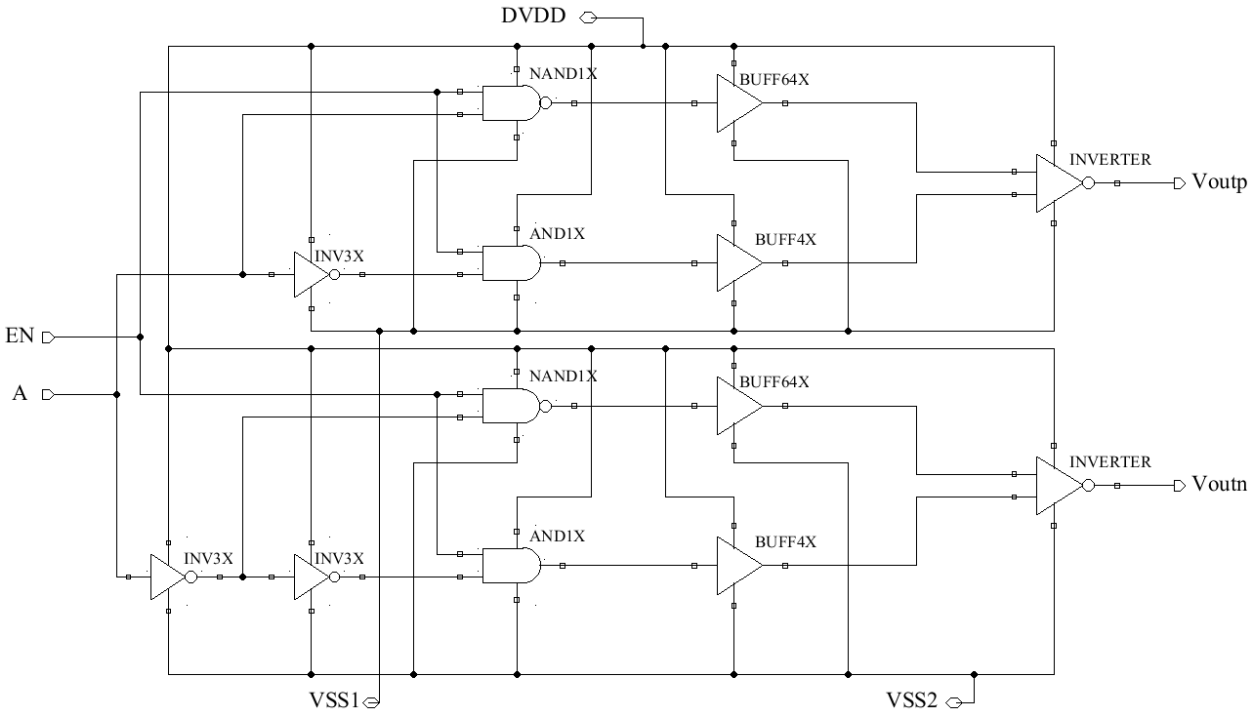
Thus, the maximum number of transceivers on the bus with a 1/8 UL is 96 devices.

2.3.7 RS–485 Design in Vulcan II

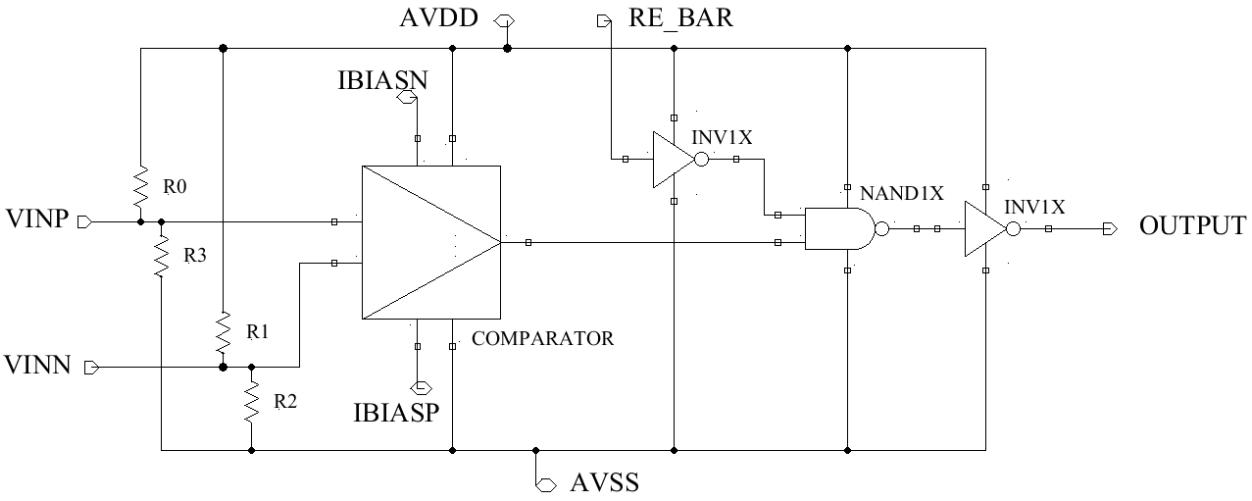
The Vulcan II RS-485 was designed to acquire and transmit data with a power supply input of 12 V. The schematics of the line driver and the receiver are presented in Fig. 2.9. The driver shown in Fig. 2.9 (a) was designed to have a tri–state differential output. It must be capable of driving the outputs no less than 2 V apart and sourcing or sinking no less than 33 mA. In order to achieve the current specification in the output stage, the inverter utilizes a PFET with an effective width (W) and length (L) of $W/L = 6{,}480\ \mu m/1.2\ \mu m$ and an NFET with $W/L = 960\ \mu m/1.2\ \mu m$. The transistor layout for the PFET consists of 324 parallel transistors of $W/L = 20\ \mu m/1.2\ \mu m$ and the NFET layout consists of 48 parallel transistors with the same W/L ratio as the PFET. The targeted transition time for the driver is 100 ns. In this way, the driver must

transition from TRUE to FALSE, FALSE to TRUE, TRUE or FALSE to IDLE, or from IDLE to TRUE or FALSE in no more than 100 ns. The driver was designed to drive up to 2400 ft of 24 AWG shielded twisted-pair wire for both a full duplex and a half duplex mode. In order to target the cable length specified, the driver was designed for a data rate of 200 kilobits per second (kbps).

The objective for the receiver, shown in Fig. 2.9 (b), was to achieve true fail–safe operation over a full–duplex bus configuration. The true fail-safe operation for the receiver was similar to the explanation given in chapter 2 for all the cases where $\overline{RE}$ is low, however when it is high, V_{OUT} is zero instead of High-Z. This behavior is achieved by designing an active low buffer. The input impedance of the receiver was specified as 12 kΩ and the receiver must be able to drive a load of 0.5 pF. The receiver uses an integrated comparator to obtain the difference between the inputs from a twisted cable. The comparator is based on a three–stage comparator optimized for integration in the RS–485 receiver with an enhanced output buffer stage. An integrated resistive voltage divider is used to convert the inputs from the twisted cable to the input common mode range of the comparator. The simulation of the Vulcan II RS-485 will be covered in chapter 3. The testing and characterization of the transceiver will be described in chapter 4.



(a)



(b)

Fig. 2.9. Schematic Presentations for (a) Line driver and (b) Receiver.

CHAPTER 3 CIRCUIT DESIGN AND SIMULATION

This chapter discusses the design process and the simulation results of the SiC RS–485. The chapter is divided into four sections – the design procedure, the design specifications, the circuit design, and the simulations of the SiC RS–485.

3.1 Design Procedure

The design process of the SiC RS–485 involves defining the specifications of the transceiver, defining the process kit, hand calculations, simulations, layout, fabrication and testing. It is necessary to have a clear idea about the needs of the system and the objective of the circuit at each step of the design process.

The general steps for IC design are the following [24]:

1. Define the function of the design – RS–485 transceiver for high temperature applications.
2. Implementation – silicon carbide CMOS process.
3. Simulation – estimate the device parameter based on hand calculations to predict the performance of the circuit.
4. Geometrical description – make the layout of the circuit and perform the physical verification checks.
5. Simulation including parasitics – simulate the circuit with the parasitic effects introduced by the layout.
6. Fabrication – the circuit is submitted for fabrication once the previous steps have been obtained.

7. Testing and Verification – create a test and verification plan to determine if the fabricated circuit meets the design specifications and compare it with simulation results.

After analyzing the data obtained from the first fabrication run of the circuit, the next step is to start a new design process taking in consideration the improvements identified

3.2 Design Specifications

The design specifications for the SiC RS-485 are to acquire and transmit data with a power supply input of 12 V for an operating temperature range of 25°C to 300°C. The principal objective is to provide a transceiver capable of data acquisition in a hot environment and transmit the data to a cooler environment or vice versa for automotive applications.

The line driver must have a tri-state differential output, which must be capable of driving the outputs no less than 2 V apart and sourcing or sinking no less than 33 mA, according to the application specification. The RS-485 interface designates that one of the two lines in the differential pair more be more positive, V_{OUTP}, than the other line, V_{OUTN}, when a logic high is received on the input of the transmitter. In addition, the driver must be able to transition in no more than 100 ns and have a half-duplex configuration. The target for the cable length was 2400 ft of category 5e (cat5e) cable.

The receiver specifications were to have a true fail–safe operation, as explained in chapter 2. In addition, the receiver must be designed for a full–duplex bus configuration and it must be able to drive a 15 pF load. The key design specifications of the RS-485 transceiver are given in Table 3.1.

Table 3.1. RS-485 Design Specifications

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	VDD	12	V
Temperature Range	T_A	25 - 300	°C
Driver Input to Output	TPLH	100	ns
	TPHL	100	ns
Driver Rise or Fall Time	TR	100	ns
	TF	100	ns
Driver Enable to Output High	TZH	100	ns
Driver Enable to Output Low	TZL	100	ns
Driver Disable Time from Low	THZ	100	ns
Driver Disable Time from High	TZL	100	ns
Differential Driver Output	VOD	2	V
Driver Load Capacitance	C_T	16	pF/ft
Receiver Differential Threshold Voltage	VTH	$-200 \leq V_{TH} \leq -30$	mV
Receiver Input Resistance	RIN	12	kΩ
Receiver Load Capacitance	C_{LOAD}	15	pF

3.3 Circuit Design

The first step in the design process of the SiC RS-485 was to determine the necessary size of the PFET and NFET. As already explained, process corner were designed for typical, slow and fast NFET and PFET devices. The typical-fast (TF) model type was chosen to be the nominal device type for this design because it matched the most recently fabricated Vulcan II devices most closely. Hence, the circuits were designed with TF characteristics. The process parameters were determined as such:

- NFET threshold voltage, Vtn = 3.5 V
- PFET threshold voltage, |Vtp| = 6.5 V
- NFET mobility factor, kn′ = 4.0 μA/V^2

- PFET mobility factor, kp′ = 0.4 µA/V^2
- Nominal device size, W/L = 20 µm/1.2 µm for the PFET and W/L = 4 µm/1.2 µm.

In cases where smaller device aspect ratios were necessary, smaller devices were used. The W/L ratios of the transistors are calculated using the drain current equation and the process parameters. The drain current equations for an n-channel MOSFET and a p-channel MOSFET are given below,

$$I_d = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_{tn})^2 \tag{3.1}$$

$$I_d = \frac{1}{2} k'_p \frac{W}{L} \left(V_{SG} - |V_{tp}|\right)^2 \tag{3.2}$$

The design and simulation of the line driver and receiver are described in this section.

3.3.1 Line Driver

The tri-state differential output specification was the first parameter to be evaluated. Tri-state logic circuits have a third state called the high impedance state or “High-Z”, where the circuit is in an open condition that is neither at a logic “High” or “Low”. These circuits have two inputs: an enable (EN) signal input that turns “ON” or “OFF” the circuit, and a data input (A) signal. The truth table for an active high tri-state buffer is shown in Table 3.2. From this table the OUTPUT follows A when EN is high.

Table 3.2. Active High Tri-State Buffer

EN	A	OUTPUT
0	0	High-Z
0	1	High-Z
1	0	0
1	1	1

The digital logic for the line driver was designed with an active high tri-state buffer. A buffer is a driver for a large load. The most common buffer is a chain of inverters. As specified, the driver should have two outputs, V_{OUTP} and V_{OUTN}, in opposite directions. The positive output of the driver was designed first. Using Table 3.2 and knowing that the output value V_{OUTP} was coming out of an inverter, the following was concluded:

- For V_{OUTP} = High-Z, both the PFET and NFET of the inverter must be OFF
- For V_{OUTP} = 1, the PFET must be ON and the NFET must be OFF
- For V_{OUTP} = 0, the PFET must be OFF and the NFET must be ON

In this way, the truth table shown in Table 3.3 was created.

Table 3.3. Driver Positive Output Truth Table

EN	INPUT	V_{OUTP}	OUT1	OUT2
0	0	High-Z	1	0
0	1	High-Z	1	0
1	0	0	1	1
1	1	1	0	0

In this inverter with output V_{OUTP}, the OUT1 value is the gate value of the PFET while OUT2 is the gate value of the NFET. It was noted that the OUT1 values are the same ones as for an NAND gate. The OUT2 values are very similar to an AND gate but it must be 1 when INPUT is 1 instead of 0. Table 3.4 shows the truth tables for the NAND and AND gates. An inverter is needed to invert the input values and be able to obtain the logic gate AND.

Table 3.4. Truth Table for NAND and AND Gates

EN	INPUT	NAND	AND
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

Then, the size of the PFET and NFET of the output stage were calculated. First, the drain voltage was calculated for the PFET and NFET to operate in the triode region. Equation 3.3 and equation 3.4 are the triode region equations for a PFET and an NFET.

$$V_{DG} > |V_{tp}| \tag{3.3}$$

$$V_{GD} > V_{tn} \tag{3.4}$$

The drain voltage V_D is 12 V, in this way,

$$\mathbf{6.5\ V} < \boldsymbol{V_{D\_PFET}} < \mathbf{12\ V}$$

$$\mathbf{0\ V} < \boldsymbol{V_{D\_NFET}} < \mathbf{8.5\ V}$$

Using these V_D values and the parameters values already given, equation 3.1 and 3.2 were used to calculate the width of the transistors. A current of 50 mA was used to provide the adequate margin over the minimum 33 mA specification. The width values obtained are the following:

$$W_{PFET} = 16.7\ mm$$

$$W_{NFET} = 1.0\ mm$$

In electronics, multiplicity denotes that there are multiple, parallel copies of the device in the layout. This multiplicity was implemented as fingered devices in the layout sharing alternating drain/sources. The multiplicity was calculated using the following equation,

$$m = \frac{W_{CALCULATED}}{W_{NOMINAL}} \tag{3.5}$$

where $W_{CALCULATED}$ is the width of the PFET and NFET calculated previously. The calculated multiplicity to drive the current specification for the PFET and NFET are $m_{PFET} = 833$ and $m_{NFET} = 50$. A DC Sweep of a test bench of the PFET and NFET with the calculated multiplicity was performed. From the simulation results it was concluded that to achieve the current specification, the multiplicity must be increased for both the PFET and the NFET. The final design of the output stage has a $m_{PFET} = 920$ and $m_{NFET} = 94$.

According to Ohm's Law, a huge amount of current is drawn from a source if we have a power source and a low impedance load without a buffer. This causes high disturbances. Adding a buffer helps because of their high input impedance. In this way, no matter what value the load impedance is, the circuit will draw little current and the load does not affect the source. The buffer sizes needed to drive the output stage were calculated using the following equations:

$$C_{in} = W_1 + W_2 \tag{3.6}$$

$$C_{load} = W_{CALCULATED} \tag{3.7}$$

$$Capacitor\ Load = H = \frac{C_{load}}{C_{in}} \tag{3.8}$$

$$Buffer\ Ratio = h = \sqrt[n]{H} \tag{3.9}$$

where C_{in} is the input capacitance of the unit inverter with nominal device sizes, and n is the number of inverters. In this way it was calculated that the buffer sizes for the PFET was 4 inverters with a 5x ratio, and the buffer size for the NFET was 4 inverters with a 4x ratio. A schematic for the positive output of the driver is shown in Fig. 3.1.

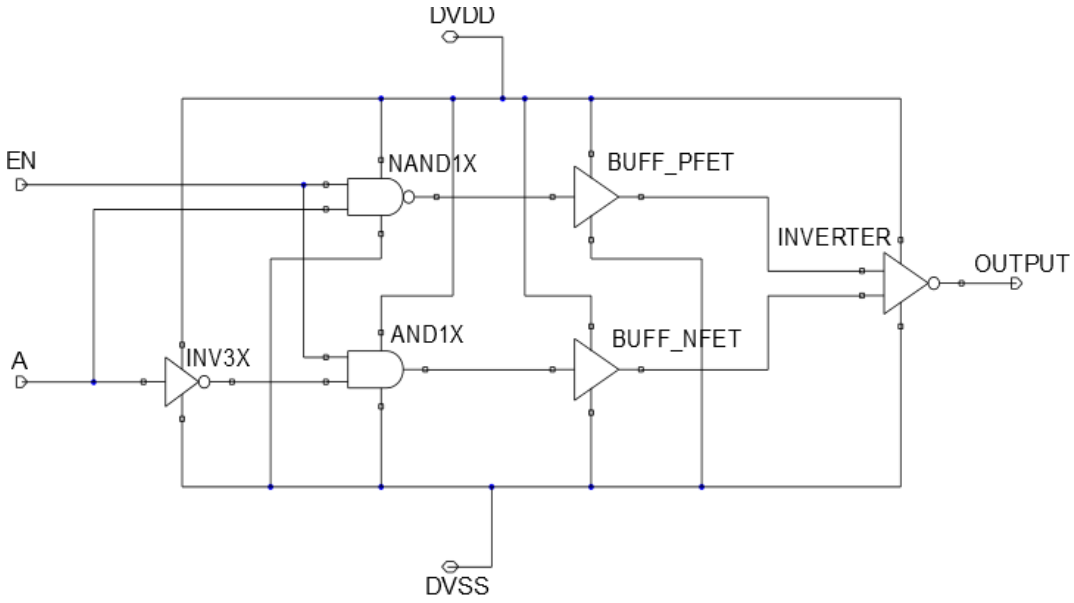


Fig. 3.1. Schematic of the Positive Output of the Driver

Next, the negative output of the driver was designed. As already explained, V_{OUTN} is the same as V_{OUTN} but in the opposite direction. An inverter was added to invert the values of the input. In this way, V_{OUTP} is the output of a tri-state buffer, while V_{OUTN} is the output of a tri-state inverter. The schematic of the line driver is shown in Fig. 3.2.

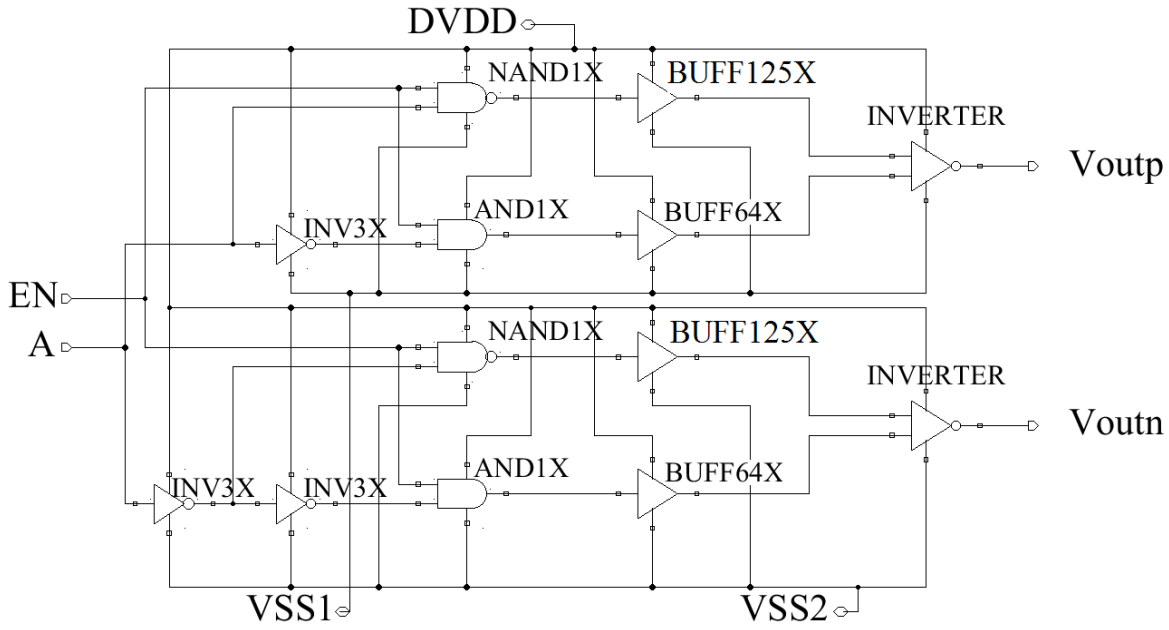


Fig. 3.2. Line Driver Schematic

The device sizes used for the line driver circuit are described in Table 3.5

Table 3.5. Device Sizes for the Line Driver Circuit

CIRCUIT BLOCK	DEVICE SIZE (µm/µm)
NAND1X	PFET = 20/1.2 (m=1)
	NFET = 8/1.2 (m=1)
INV 3X	PFET = 20/1.2 (m=3)
	NFET = 4/1.2 (m=3)
AND1X	PFET = 20/1.2 (m=1)
	NFET = 4/1.2 (m=1)
BUFF125X	PFET = 20/1.2 (m=1)
	PFET = 20/1.2 (m=5)
	PFET = 20/1.2 (m=25)
	PFET = 20/1.2 (m=125)
	NFET = 4/1.2 (m=1)
	NFET = 4/1.2 (m=5)
	NFET = 4/1.2 (m=25)
	NFET = 4/1.2 (m=125)
BUFF64X	PFET = 20/1.2 (m=1)
	PFET = 20/1.2 (m=4)
	PFET = 20/1.2 (m=16)
	PFET = 20/1.2 (m=64)
	NFET = 4/1.2 (m=1)
	NFET = 4/1.2 (m=4)
	NFET = 4/1.2 (m=16)
	NFET = 4/1.2 (m=64)
INVERTER	PFET = 20/1.2 (m=920)
	NFET = 20/1.2 (m=94)

3.3.2 Receiver

The tri-state specification for the receiver was the first condition to be assessed. Table 3.6 shows a truth table for a true fail-safe differential receiver where $\overline{RE}$ is the enable pin of the receiver, $V_{INP} - V_{INN}$ is the differential input, and V_{OUT} is the output of the receiver.

Table 3.6. Truth Table for a True Fail-Safe Differential Receiver

$\overline{RE}$	$V_{INP} - V_{INN}$ (inputs)	V_{OUT}
0	≥ -30 mV	1
0	≤ -200 mV	0
0	-200 mV $\leq (V_{INP} - V_{INN}) \leq -30$ mV	X
1	X	High-Z

An integrated self-biased comparator similar to the one used for the Vulcan II receiver was used to obtain the difference between the inputs from the cat5e cable. This comparator is also optimized with an enhanced output buffer stage for integration in the RS-485 receiver. An integrated resistive voltage divider was also used to convert the inputs from the cable to the input common mode range of the comparator, since the comparator differential input is 20 mV and -20 mV. In this way, if the twisted differential input is -200 mV or lower, the comparator differential input is -20 mV, and its output is low. On the other hand, if the twisted differential input is equal to or greater than -30 mV, the comparator differential input is 20 mV, and its output is high. A schematic of the integrated resistive voltage divider is shown in Fig. 3.3.

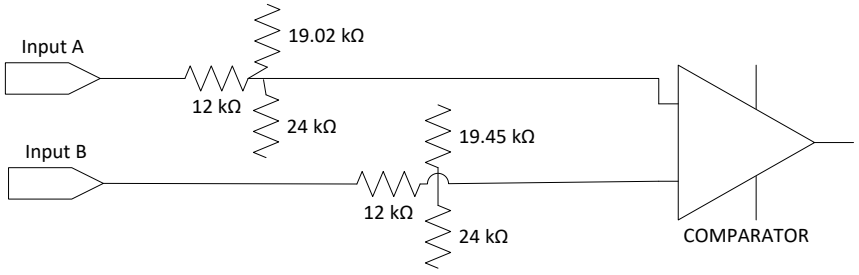


Fig. 3.3. Receiver Integrated Resistive Voltage Divider

From integrating Table 3.6 and the comparator to the receiver's design, a truth table for the receiver was created. Table 3.7 shows the receiver's truth table.

Table 3.7. Receiver Truth Table

$\overline{\mathbf{RE}}$	Comparator Output	V_{OUT}
0	0	0
0	1	1
1	0	High-Z
1	1	High-Z

Using Table 3.7 and knowing that the output value was coming out of an inverter, the following was concluded:

- For V_{OUT} = High-Z, both the PFET and NFET of the inverter must be OFF
- For V_{OUT} = 1, the PFET must be ON and the NFET must be OFF
- For V_{OUT} = 0, the PFET must be OFF and the NFET must be ON

In this way, the following truth table was created.

Table 3.8. Receiver Output Truth Table

$\overline{\mathbf{RE}}$	Comparator Output	V_{OUT}	OUT1	OUT2
0	0	0	1	1
0	1	1	0	0
1	0	High-Z	1	0
1	1	High-Z	1	0

In this inverter with output V_{OUT}, the OUT1 value is the gate value of the PFET, while OUT2 is the gate value of the NFET. It was noted that the OUT2 values are the same ones as for

a NOR gate. Using Boolean algebra, the OUT1 values were translated into two logics gates: two inverters and a NOR.

Next, the driving current for the output stage was calculated using the equation for a capacitor's current

$$I = C_{LOAD} * \frac{dV}{dt} = C_{LOAD} * \frac{\Delta V}{t_R} \tag{3.10}$$

The value for ΔV was calculated using the 10% and 90% of the power supply of 12 V. The rise time was calculated as 20 ns (0.4% of clock period). In this way the driving current was

$$I = 7.20\ mA$$

After this, the buffer sizes to drive the output stage were calculated as shown with the line driver. The calculated buffer size for the PFET was 2 inverters with a ratio of 5x, and for the NFET the buffer size was 2 inverters with a ratio of 4x. The schematic of the active low tri-state buffer is shown in Fig. 3.4.

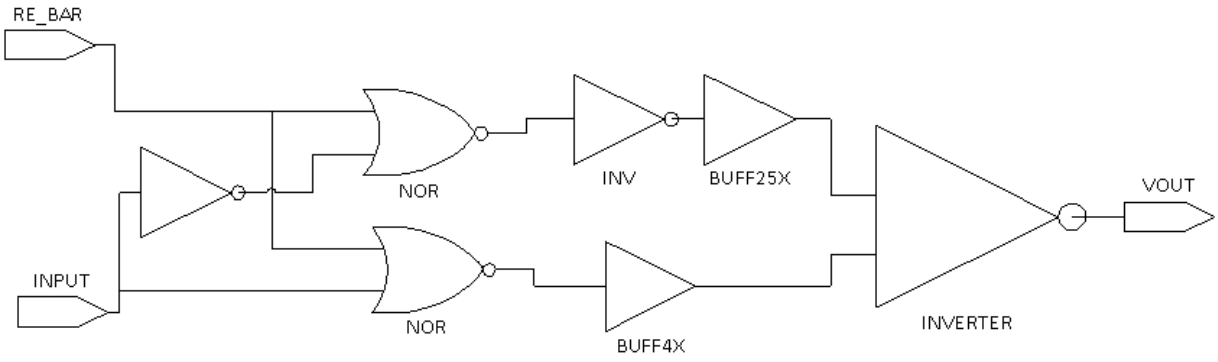


Fig. 3.4. Schematic of the Active Low Tri-State Buffer

The schematic of the receiver is shown in Fig. 3.5.

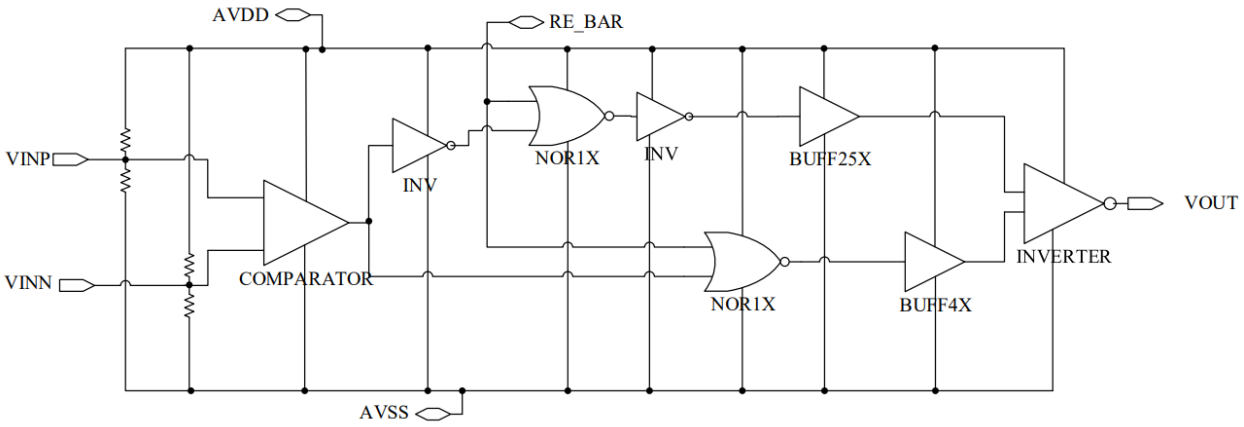


Fig. 3.5. Receiver Schematic

The device sizes used for the receiver circuit are described in Table 3.9.

Table 3.9. Device Sizes for the Receiver Circuit

CIRCUIT BLOCK	DEVICE SIZE (µm/µm)
INV1X	PFET = 20/1.2 (m=1)
	NFET = 4/1.2 (m=1)
NOR	PFET = 20/1.2 (m=1)
	NFET = 8/1.2 (m=1)
BUFF25X	PFET = 20/1.2 (m=1)
	PFET = 20/1.2 (m=5)
	PFET = 20/1.2 (m=25)
	NFET = 4/1.2 (m=1)
	NFET = 4/1.2 (m=5)
	NFET = 4/1.2 (m=25)
BUFF4X	PFET = 20/1.2 (m=1)
	PFET = 20/1.2 (m=4)
	NFET = 4/1.2 (m=1)
	NFET = 4/1.2 (m=4)
INVERTER	PFET = 20/1.2 (m=134)
	NFET = 20/1.2 (m=14)

3.3.3 Category 5e Cable Design

Category 5e cable is a twisted pair cable standard widely known for Ethernet cabling. It was chosen to drive the transceiver because it is a 24 AWG cable, it is readily available, and it is similar to the cable often used with RS-485 type systems. It has a typical capacitance of 15.85 pF/ft and a characteristic impedance of 100 Ω.

A model for the cat5e cable was designed to simulate the transceiver driving over 4 meters. Transmission lines are represented with the lumped-element circuit model, which consists of four elements: resistance, inductance, conductance and capacitance [25]. The first step into designing the cable model was to measure the inductance, capacitance and resistance of the cat5e cable with an LCR meter. First, 10 m of cable were cut to get the four pairs: blue, green, orange, and brown. Each pair has a different pitch, which is the distance per twist, to minimize crosstalk. Measurements on the sample of cat5e yielded the results shown in Table 3.10.

Table 3.10. Cat5e pairs Measurements

PAIR COLOR	CENTIMETERS PER TURN	TURNS PER METER
Blue	1	97
Green	0.9	112
Orange	0.5	168
Brown	0.7	148

The blue and green pair were measured with the HP 4284A Precision LCR Meter. The parallel and series values for capacitance-resistance and inductance-resistance were measured with the short and open measurement functions from the machine. In order to have an average value of the parameters, every 0.5 m the cable was cut and measured. First, 4 m of cable were measured, then 3.5 m of cable, 3.0 m and so on. In addition to this, the impedance, inductance and capacitance of the cable were calculated. The following equations were used,

$$Z_0 = \frac{120}{\sqrt{e_r}} * ln\left(\frac{2s}{D}\right) \tag{3.11}$$

$$L_{twisted_{pair}} = 10.16\text{x}10^{-9} * ln\left(\frac{2s}{D}\right) \tag{3.12}$$

$$C_{twisted_{pair}} = e_r * \left(\frac{0.7065}{ln\left(\frac{2s}{D}\right)}\right) \tag{3.13}$$

where Z_0 is the impedance, e_r the substrate dielectric, s is the separation between wires, and D is the diameter of the wire. The datasheet of the cable manufacturer states that the dielectric is solid PE or polyethylene, which have a relative permittivity of 2.5. The diameter of the wire is 0.51054 mm according to the datasheet. From measuring the cable, the distance between the wire is 0.1 cm.

In this way, the following parameters values were obtained,

$$Z_0 = 110\ \Omega$$

$$L_{twisted_{pair}} = 0.54724\ \mu\text{H/m}$$

$$C_{twisted_{pair}} = 45.67\ \text{pF/m}$$

The model of the cable with the average values measured from the LCR meter is presented in Fig. 3.6.

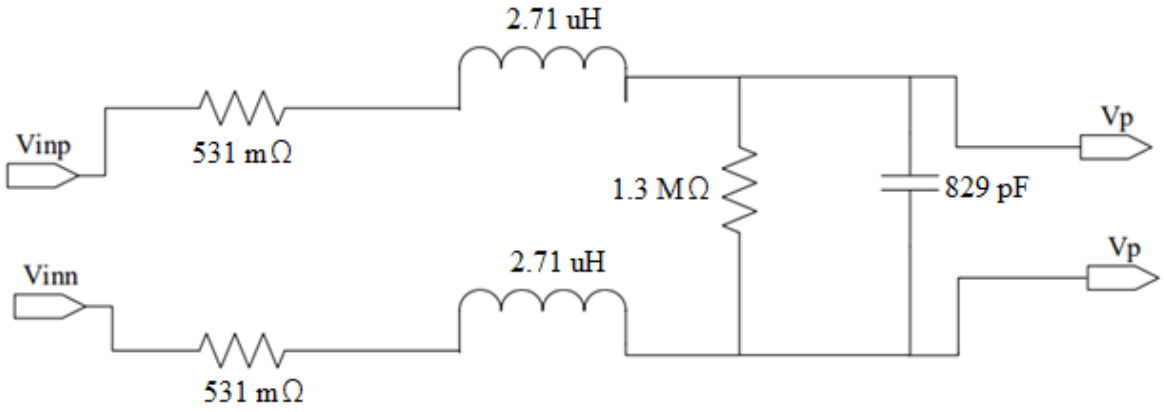


Fig. 3.6. Model for 4 m of Cat5e Cable

3.4 Simulations

This section describes the simulations from the Vulcan II RS-485 described in Chapter 2 and the redesigned design described in this chapter.

The transceivers were simulated over temperature with isothermal BSIM4 models using Cadence Virtuoso Analog Design Environment for temperatures of 25°C, 100°C, 200°C, and 300°C. In the same way, they were both simulated with and without driving a 4 m balanced transmission line model with frequencies of 20 kHz and 100 kHz for the input signal. The simulations results presented are for the TF model which most closely matched the fabricated devices on the Vulcan II fabrication run.

3.4.1 Vulcan II RS-485

The Vulcan II RS-485 was simulated with a power supply input of 15 V, frequency of 100 kHz with a half-duplex configuration. The specification for the driver switching characteristics is 100 ns.

The driver output skew to output is calculated from the measured driver input to output values as,

$$TSKEW = |TPLH - TPHL| \tag{3.14}$$

The differential receiver skew (TSKD) is calculated from the measured receiver input to output values as,

$$TSKD = |TPLH - TPHL| \tag{3.15}$$

The switching characteristics from simulating the transceiver without cable are presented on Table 3.11.

Table 3.11. Vulcan II RS-485 Simulations without Cable

PARAMETER	SYMBOL	25°C	100°C	200°C	300°C	UNITS
Driver Differential Voltage	VDIFF	10.17	8.81	12.67	12.24	V
Driver Input to Output	TPLH	46	35	33	33	ns
	TPHL	48	37	34	34	ns
Driver Output Skew to Output	TSKEW	2	2	1	1	ns
Driver Rise or Fall Time	TR	26	15	17	17	ns
	TF	18	13	12	12	ns
Driver Enable to Output High	TZH	48	40	34	34	ns
Driver Enable to Output Low	TZL	43	37	31	30	ns
Driver Disable Time from Low	TLZ	20	13	11	12	ns
Driver Disable Time from High	THZ	46	28	31	31	ns
Receiver Input to Output	TPLH	257	78	184	186	ns
	TPHL	289	4891	226	222	ns
Differential Receiver Skew	TSKD	32	4813	42	36	ns

The driver differential voltage is greater than 2 V for all temperatures. The transition time specification is achieved for all the driver parameters. For the driver switching parameters, the values decreased as the temperature increases.

The switching characteristics from simulating the transceiver with the cable are presented on Table 3.12.

Table 3.12. Vulcan II RS-485 Simulation with a 4 m Cable

PARAMETER	SYMBOL	25°C	100°C	200°C	300°C	UNITS
Driver Differential Voltage	VDIFF	10.25	8.85	12.75	12.31	V
Driver Input to Output	TPLH	34	33	25	25	ns
	TPHL	39	33	29	29	ns
Driver Output Skew to Output	TSKEW	5	0	4	4	ns
Driver Rise or Fall Time	TR	52	61	53	52	ns
	TF	45	58	47	46	ns
Driver Enable to Output High	TZH	46	36	33	33	ns
Driver Enable to Output Low	TZL	43	34	31	31	ns
Driver Disable Time from Low	TLZ	22	22	13	13	ns
Driver Disable Time from High	THZ	40	28	25	26	ns
Receiver Input to Output	TPLH	261	7	189	191	ns
	TPHL	306	13	238	234	ns
Differential Receiver Skew	TSKD	45	6	49	43	ns

The driver differential voltage was also achieved as all values were greater than 2 V for all temperatures. The transition time specification is achieved for all the driver switching parameters. The values decrease over temperature except for the driver rise and fall times which increase at 100°C.

3.4.2 SiC RS-485

First, the line driver was simulated with a transient analysis with a C_T = 16 pF, a 12 V supply, frequencies of 20 kHz and 100 kHz for the input signal and a resistance of 120 Ω. The switching characteristics are presented on Table 3.13. The specification for the driver switching characteristics is 100 ns.

Table 3.13. Driver Simulation Switching Characteristics

PARAMETER	SYMBOL	25°C	100°C	200°C	300°C	UNITS
Driver Input to Output	TPLH	65	48	46	45	ns
	TPHL	62	46	44	43	ns
Driver Output Skew to Output	TSKEW	3	2	2	2	ns
Driver Rise or Fall Time	TR	23	18	17	16	ns
	TF	18	13	12	11	ns
Driver Enable to Output High	TZH	61	41	39	38	ns
Driver Enable to Output Low	TZL	68	49	49	48	ns
Driver Disable Time from Low	TLZ	44	31	29	28	ns
Driver Disable Time from High	THZ	47	34	31	30	ns

All the switching characteristics decrease as temperature increases. The transition time was achieved for the switching characteristics specification.

Then, the receiver was simulated with a 12 V supply, C_{LOAD} = 15 pF and voltage supplies that simulate the differential input from the twisted cable. The receiver propagation delays over temperature are presented on Fig. 3.7. The TSKD on the graph is calculated as shown in equation 3.15.

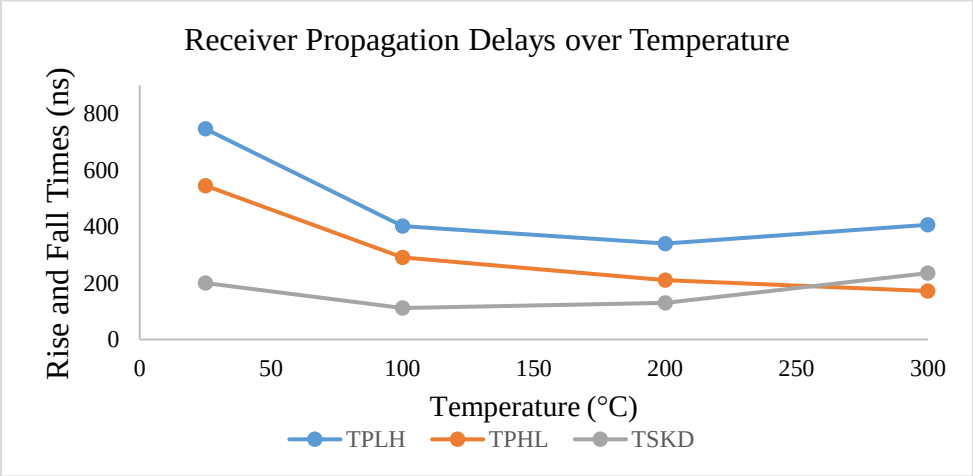


Fig. 3.7. Receiver Propagation Delays over Temperature

The propagation delays values decrease over temperature, except for the propagation from low to high, which increases after 200°C.

Then, the transceiver was simulated with and without driving a 4 m balanced transmission line model with a 12 V supply and frequencies of 20 kHz and 100 kHz for the input signal. The switching characteristics from simulating the transceiver without cable are presented on Table 3.14.

Table 3.14. RS-485 Simulation without Cable

PARAMETER	SYMBOL	25°C	100°C	200°C	300°C	UNITS
Driver Input to Output	TPLH	63	47	45	44	ns
	TPHL	67	49	46	45	ns
Driver Output Skew to Output	TSKEW	4	2	1	1	ns
Driver Rise or Fall Time	TR	37	21	25	24	ns
	TF	26	19	18	17	ns
Driver Enable to Output High	TZH	68	50	48	46	ns
Driver Enable to Output Low	TZL	68	55	42	41	ns
Driver Disable Time from Low	TLZ	30	32	19	18	ns
Driver Disable Time from High	THZ	65	50	45	44	ns
Receiver Input to Output	TPLH	346	170	235	231	ns
	TPHL	354	234	267	255	ns
Differential Receiver Skew	TSKD	8	64	32	24	ns

The switching characteristics from simulating the RS-485 without the cable model met the transition time specification. At 100°C, the receiver propagation delay was lower than the simulation values observed for the other temperatures.

The switching characteristics from simulating the transceiver with the cable are presented on Table 3.15. The transceiver was simulated driving a 4 m balanced transmission line model with a 12 V supply and a frequency of 100 kHz for the input signal.

Table 3.15. RS-485 Simulation with a 4 m Cable

PARAMETER	SYMBOL	25°C	100°C	200°C	300°C	UNITS
Driver Input to Output	TPLH	52	39	37	36	ns
	TPHL	57	43	41	40	ns
Driver Output Skew to Output	TSKEW	5	4	4	4	ns
Driver Rise or Fall Time	TR	58	60	63	62	ns
	TF	50	56	55	55	ns
Driver Enable to Output High	TZH	64	47	45	44	ns
Driver Enable to Output Low	TZL	63	47	46	44	ns
Driver Disable Time from Low	TLZ	47	26	24	23	ns
Driver Disable Time from High	THZ	67	39	37	36	ns
Receiver Input to Output	TPLH	297	186	158	142	ns
	TPHL	441	260	208	191	ns
Differential Receiver Skew	TSKD	144	74	50	49	ns

The same behavior as when simulating the transceiver without the cable was observed. The transition time was met for the driver transition times. The receiver propagation delays decreased over temperature, with the propagation delay values from high to low higher than from low to high.

CHAPTER 4 TESTING AND CHARACTERIZATION

The Vulcan II RS-485 described in chapter 2 was sent for fabrication in September 2014. In order to reproduce the test benches used when designing and verifying the circuit, a detailed test plan was developed, and a printed circuit board was created. This chapter discusses the fabrication, testing and characterization of the RS-485 transceiver tested over temperature.

4.1 Chip Fabrication, Packaging and Test Set Up for High Temperature

The SiC CMOS RS-485 designed for the Vulcan II run was fabricated as part of a 21 mm by 12.5 mm multi-site reticle on a 100 mm SiC wafer. Raytheon Limited Systems fabricated 5 wafers were the circuits designed by the MSCAD team at the University of Arkansas were organized in a total of twelve subsites. The die micrograph form the Vulcan II fabrication run is shown in Fig. 4.1 with the transceiver highlighted in red.

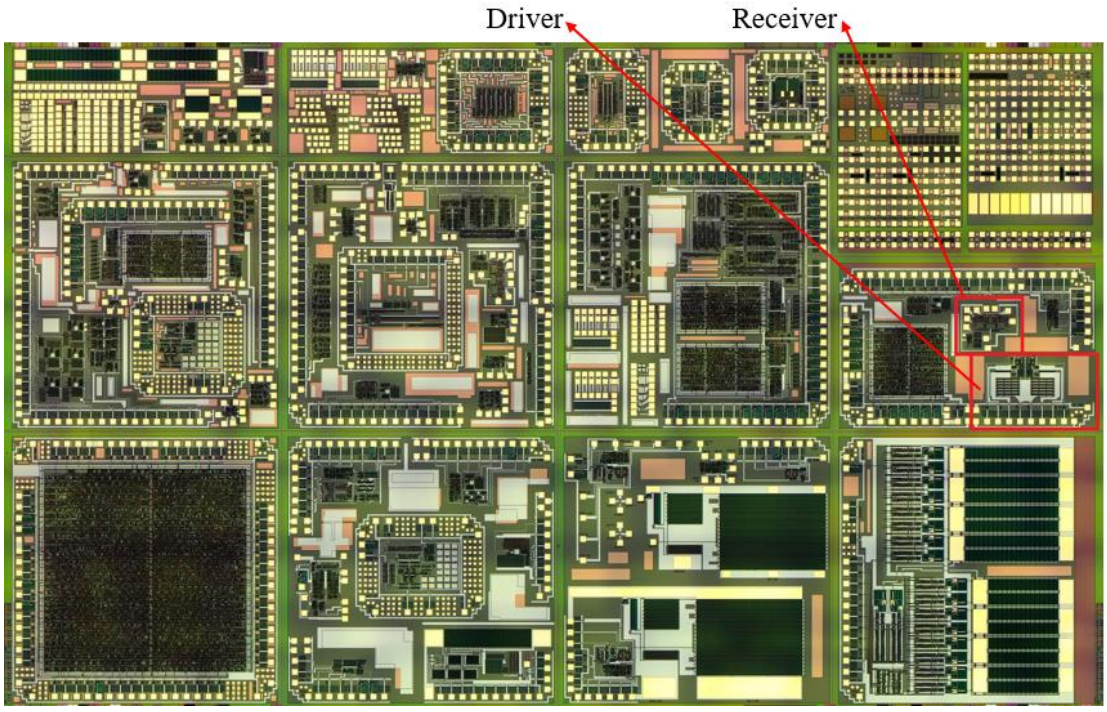
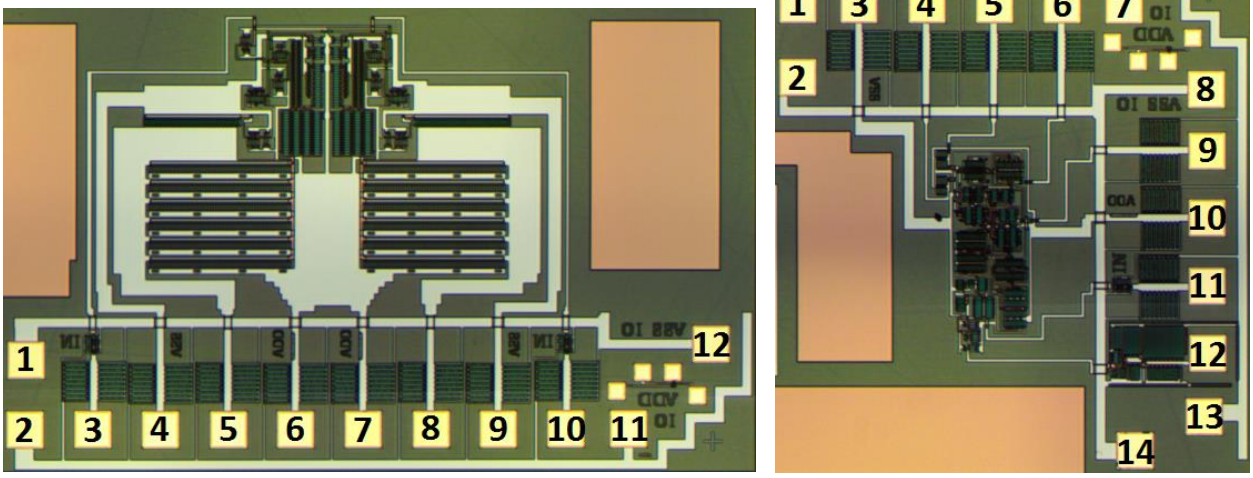


Fig. 4.1. Vulcan II Complete Die Micrograph and Location of the Circuits on the Full Reticle

The transceiver die with pin numbers is shown in Fig. 4.2. Including the pad frame, the dimensions of the driver and receiver circuits are 2283 µm by 1386.4 µm and 1544.8 µm by 1434.6 µm respectively.



(a) (b)

Fig. 4.2. Pin Configuration of the Die Micrograph of the (a) Driver and (b) Receiver

Table 4.1 shows the name and description of each pin. A total of 24 pads custom pad frames with balanced power distribution and voltage clamping protection circuits were used.

Table 4.1. Pin Description of the Driver and Receiver

DRIVER		
PIN NUMBER	**NAME**	**DESCRIPTION**
1	VSSIO	Power Supplies
2	VDDIO	Power Supplies
3	A	Input of the driver
4	VSS2	Power Supplies
5	V_{OUTN}	Negative output of the driver
6	VDD2	Power Supplies
7	VDD1	Power Supplies

RECEIVER		
PIN NUMBER	**NAME**	**DESCRIPTION**
1	VDDIO	Power Supplies
2	VSSIO	Power Supplies
3	VSS	Power Supplies
4	V_{INN}	Negative input of the receiver
5	V_{INP}	Positive input of the receiver
6	R_IBN	Comparator bias connection
7	VDDIO	Power Supplies

Table 4.1 Pin Description of the Driver and Receiver (Cont'd)

DRIVER		
PIN NUMBER	**NAME**	**DESCRIPTION**
8	V_{OUTP}	Positive output of the driver
9	VSS1	Power Supplies
10	EN	Enable Pin
11	VDDIO	Power Supplies
12	VSSIO	Power Supplies

RECEIVER		
PIN NUMBER	**NAME**	**DESCRIPTION**
8	VSSIO	Power Supplies
9	R_IBP	Comparator bias connection
10	VDD	Power Supplies
11	$\overline{RE}$	Enable pin of the receiver
12	V_{OUT}	Output of the receiver

First, the circuits were tested for functionality. Heartbeat measurements on the Semiprobe probe station in the MSCAD laboratory were done on wafer level and at room temperature. The circuits were then diced into sub-sites of 5 mm by 5 mm at the University of Arkansas High Density Electronics Center (HiDEC) and then individual die were attached to a 68 pin ceramic leaded chip carrier (LDCC) package with a silver epoxy. The pad frames were then gold-wire bonded to the ceramic package lead frame. A K&S 4700 wirebonder at HiDEC was used to create the 1 mil gold ball bonds between the die and the package. The bonding plan for the RS-485 is shown in Fig. 4.3.

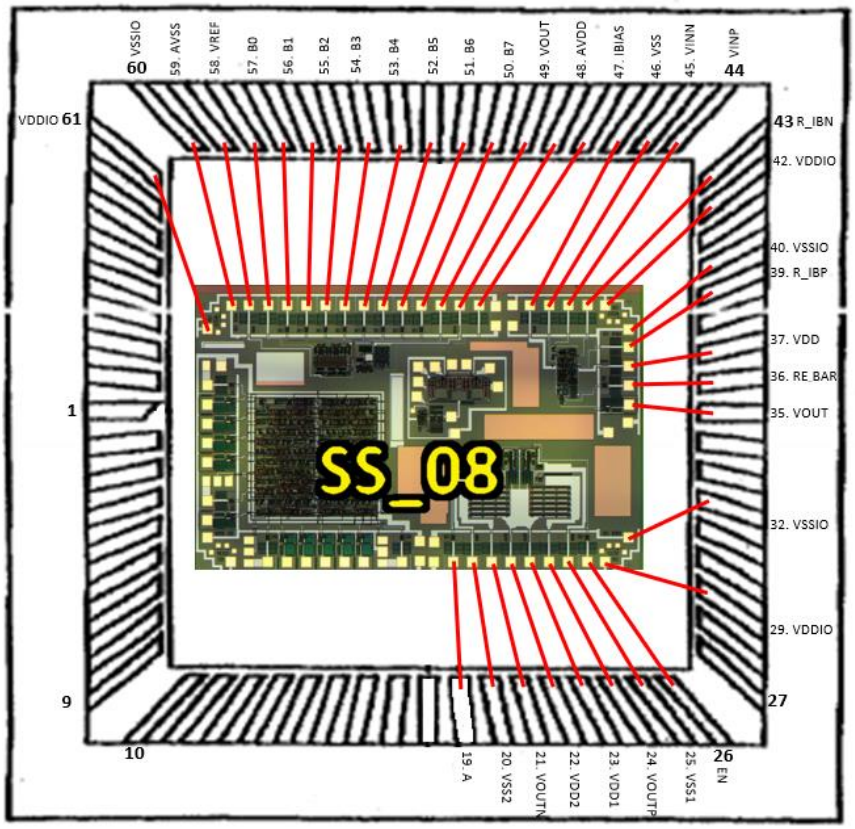


Fig. 4.3. Bonding Plan

Next, the chip-in-package was soldered on a Rogers-4350 printed circuit board (PCB) to enable testing at high temperatures. Header pins were soldered unto this PCB using high temperature solder to allow for connections to a function generator, a DC power supply, a mixed domain oscilloscope and a breakout board. The mechanical design of the PCB supports mounting to a high temperature test fixture consisting of an aluminum chuck that can be placed on a hot plate. The aluminum apparatus used thermally insulating stand-offs for support and a metal stand that clamps to the bottom of the package to the aluminum chuck through an opening in the PCB. This enabled the package to be heated safely with an easily controlled thermal time constant of approximately 55°C/min. The high temperature test set up of the circuit is shown in Fig. 4.4.

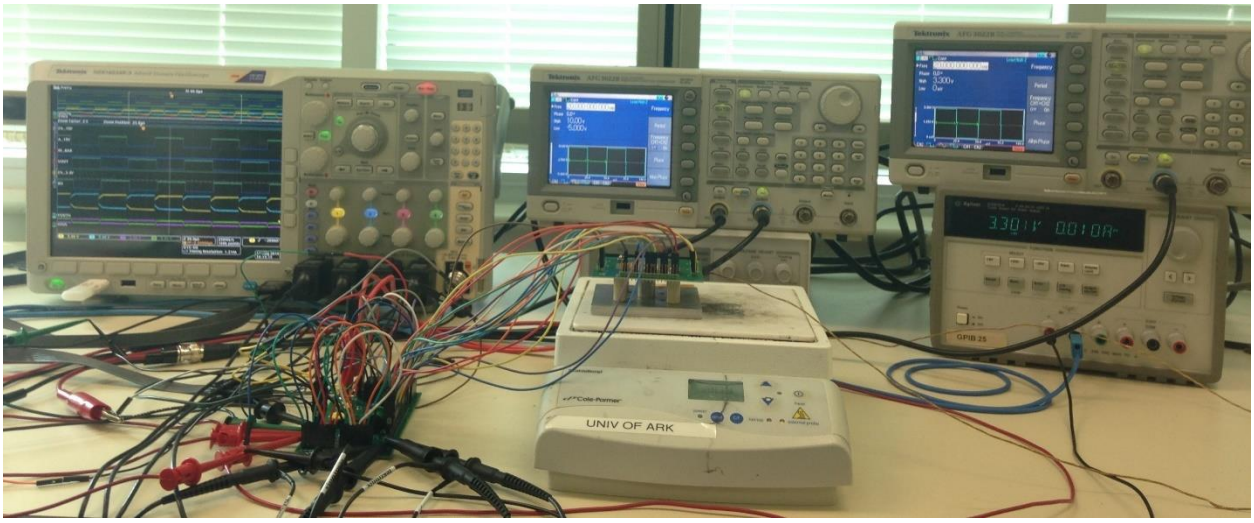


Fig. 4.4. High Temperature Testing Set up

In order to characterize the transceiver, a breakout board was designed. This board was designed to test the RS-485 in a half and full duplex configuration with different cable length configurations. The full duplex configuration was achieved by connecting a commercial silicon 3.3 V RS-485 to the CMOS SiC RS-485 through 2400 ft of cat5e cable. This board was used to simulate the room temperature side of the system; hence it was not placed over the hot plate.

Category 5e cable was used to test the transmission length specification of the SiC transceiver. As already discussed on chapter 2 and 3, "true" RS-485 cable has an impedance of 120 Ω, while the cat5e cable has one of 100 Ω. An impedance mismatch causes reflections at the driver and at the receiver and decreases the achievable data rate [26]. In order to match the impedances, a termination network was added to the receiver's differential pair. The termination network consisted of a 120 Ω resistor between V_{INP} and V_{INN}, one 680 Ω resistor between V_{INP} and VCC and one 680 Ω resistor between V_{INN} and ground. The same termination network was made for the receiver's inputs of the Si transceiver. RJ-45 connectors were used on the board to test the transceiver with the cat5e cable.

4.2 Experimental Results

First the DC electrical characteristics of the transceiver were measured at 25°C without the cable. Table 4.2 shows an average of the measured values and a comparison of the Vulcan II transceiver with the Maxim's Integrated MAX485 and MAX491 RS-485 [27]. The values obtained are similar to the MAX485 and MAX491 transceivers.

Table 4.2. Measured DC Electrical Characteristics

PARAMETER	SYMBOL	VULCAN II RS-485			MAXIM INTEGRATED MAX485 / MAX491			UNITS
		MIN	AVG	MAX	MIN	TYP	MAX	
Differential Driver Output (no load)	V_{OD1}	-	3.6	-	-	-	5	V
Differential Driver Output (with load)	V_{OD2}	-	1.6	-	1.5	-	5	V
Driver Common-Mode Output Voltage	V_{OC}	-	4.6	-	-	-	3	V
Receiver Differential Threshold Voltage	V_{TH}	-200	-	-30	-200	-	200	mV
Receiver Input Resistance	R_{IN}	12	-	-	12	-	-	kΩ

4.2.1 Test 1: SiC Driver with SiC Receiver

The transceiver was tested at supply voltages of 12 V and 15 V from temperatures of 25°C to 400°C. The inputs EN and A were connected to a function generator to supply a square signal of amplitude 12 V and 15 V with a frequency of 5 kHz for the EN signal. The input $\overline{RE}$ was set to low. In this way, V_{OUT} follows the output of the comparator at all times. Transmission frequencies from 20 kHz to 100 kHz were utilized with 600 ft (182 m), 1200 ft (365 m), and 2400 ft (731 m) of cat5e cable. A half-duplex configuration was used to test the SiC driver with the SiC receiver. RS-485 transceivers have enable pins for the driver and the receiver since the transmitter must be tri-stated while receiving data in this configuration.

The measured switching characteristics over temperature without a cable for the Vulcan II transceiver at 15 V and 100 kHz are presented in Fig. 4.5. On the driver and receiver propagation delays graphs, the skew was calculated as explained on equations 3.14 and 3.15.

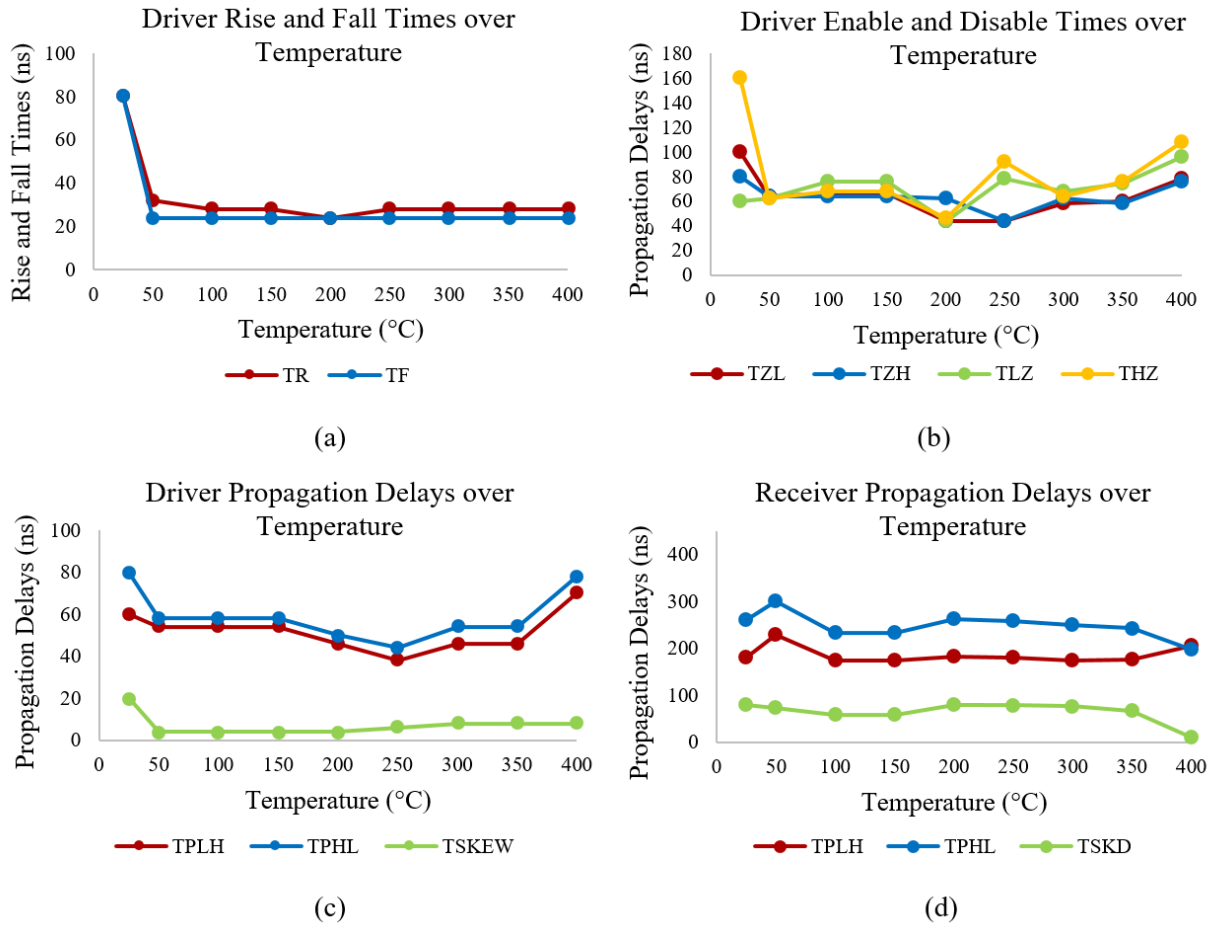


Fig. 4.5. Graphs of the Measured Switching Characteristics of the SiC RS-485 with a Half-Duplex Configuration over Temperature without Cable

The driver rise and fall times decrease after 25°C with stable values over the rest of the temperatures. The driver enable times, TZL and TZH, have a similar behavior with the same values over temperature except at 25°C and 200°C. After 25°C, TZL is constant until it decreases at 200°C, while TZH is constant until it decreases at 250°C. After 250°C, they both increase over temperature. For the driver disable times, TLZ and THZ, the behavior over temperature is the same with the exception at 25°C where the value for THZ is 160 ns. This is the largest measured

propagation time over temperature for this configuration. Both TLZ and THZ have constant values at 100°C and 150°C, then decrease at 200°C, have a peak at 250°C, decrease at 300°C and then they start increasing over temperature.

The driver propagation delays over temperature have the same behavior, being the propagation from high to low, TPHL, higher at all temperatures. As the driver to output skew shows, the highest value is 20 ns at 25°C. The driver propagation delays are constant from 50°C to 150°C, then decrease, and after 250°C they both increase. The receiver propagation delays increase after 25°C, decrease after 50°C, are constant for 100°C and 150°C and they increase after 150°C. After 200°C, TPHL slowly decreases over temperature, while TPLH decreases until 300°C and then increases over temperature.

Table 4.3 shows the measured values of the SiC RS-485 at 25°C for 15 V compared with the values for the commercial transceivers MAX485 and MAX491.

Table 4.3. Test 1 Measured Switching Characteristics without Cable

PARAMETER	SYMBOL	VULCAN II RS-485	MAXIM INTEGRATED MAX485 / MAX491			UNITS
		25°C	MIN	TYP	MAX	
Driver Input to Output	TPLH	60	10	30	60	ns
	TPHL	80	10	30	60	ns
Driver Output Skew to Output	TSKEW	20		5	10	ns
Driver Rise or Fall Time	TR	80	3	15	40	ns
	TF	80	3	15	40	ns
Driver Enable to Output High	TZH	80		40	70	ns
Driver Enable to Output Low	TZL	100		40	70	ns
Driver Disable Time from Low	TLZ	60		40	70	ns
Driver Disable Time from High	THZ	160		40	70	ns

Table 4.3 Test 1 Measured Switching Characteristics without Cable (Cont'd)

PARAMETER	SYMBOL	VULCAN II RS-485	MAXIM INTEGRATED MAX485 / MAX491			UNITS
		25°C	MIN	TYP	MAX	
Receiver Input to Output	TPLH	180	20	90	200	ns
	TPHL	260	20	90	200	ns
Differential Receiver Skew	TSKD	80		13		ns

The transition time for the driver characteristics were achieved for most of the parameters, but for the driver disable time from high since it was 160 ns. Overall, the Vulcan II RS-485 results are slightly higher than the Maxim Integrated transceivers values.

Table 4.4 shows an average of the measured values of the switching characteristics when testing the transceiver with 4 m of cat4e cable for 15 V.

Table 4.4. Test 1 Measured Switching Characteristics with a 4 m Cable

PARAMETER	SYMBOL	25°C	100°C	200°C	300°C	400°C	UNITS
Driver Input to Output	TPLH	120	70	70	60	100	ns
	TPHL	120	90	80	70	100	ns
Driver Output Skew to Output	TSKEW	0	20	10	10	0	ns
Driver Rise or Fall Time	TR	80	40	80	60	40	ns
	TF	60	40	60	60	40	ns
Driver Enable to Output High	TZH	160	110	90	140	160	ns
Driver Enable to Output Low	TZL	130	80	50	110	110	ns
Driver Disable Time from Low	TLZ	230	150	110	150	130	ns
Driver Disable Time from High	THZ	220	110	100	170	170	ns
Receiver Input to Output	TPLH	250	230	200	220	200	ns
	TPHL	220	220	180	220	250	ns
Differential Receiver Skew	TSKD	30	30	40	20	50	ns

The results are slightly higher than the values shown in Fig 4.5. The rise and fall times and driver input to output parameters meet the transition time specification, except for the driver to input

values at 25°C. The driver enable to output high/low, and the driver disable time from low/high are slightly higher than 100 ns. The receiver propagation delays values are similar to the measured values for testing the transceiver without cable.

The measured switching characteristics of the Vulcan II transceiver when driving a 2400 ft cat5e cable at 15 V and 100 kHz are presented on Fig. 4.6.

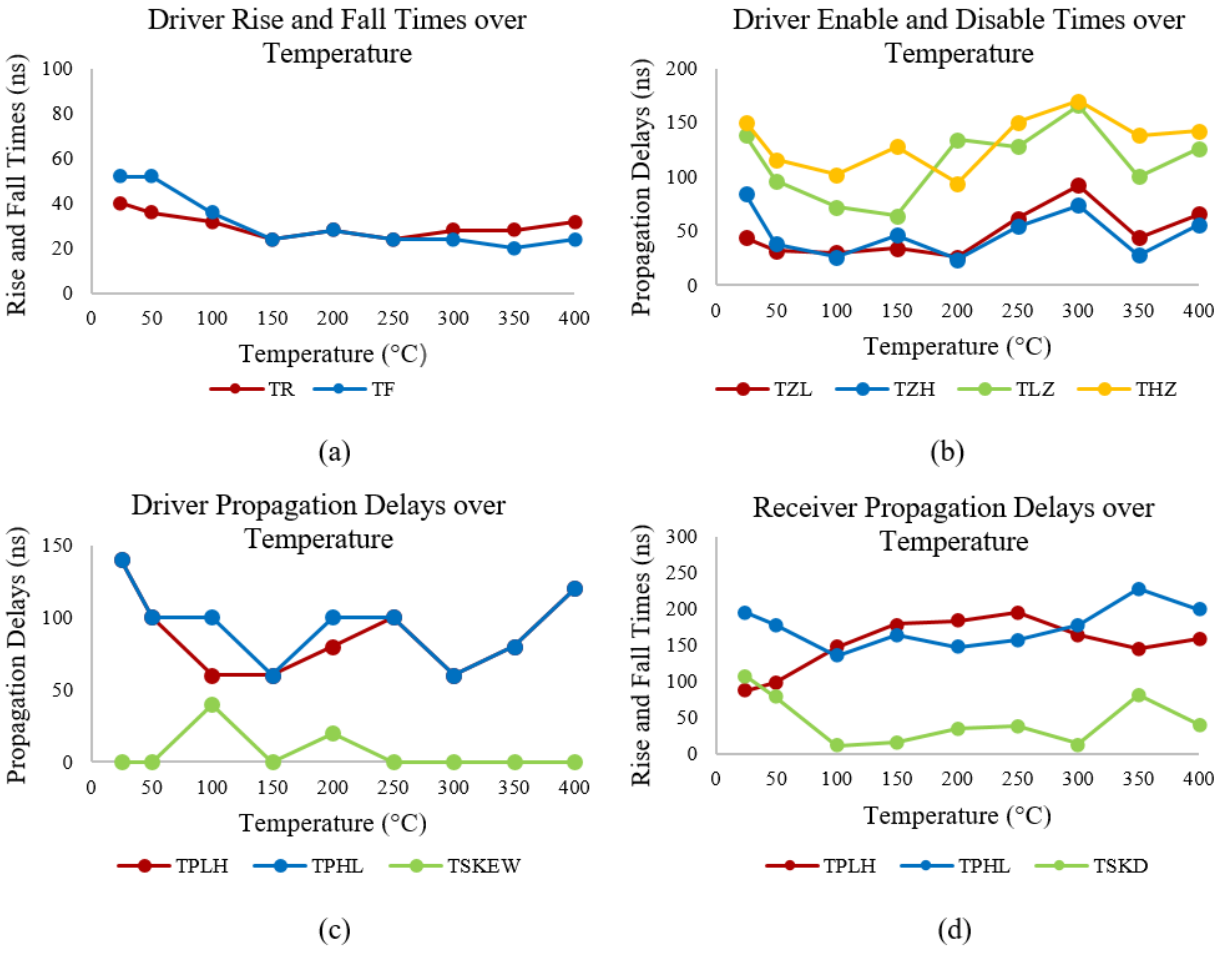


Fig. 4.6. Graphs of the Measured Switching Characteristics of the SiC RS-485 with a Half-Duplex Configuration over Temperature with 2400 ft of Cat5e Cable

The driver rise and fall times decrease after 25°C, increase at 200°C and decrease at 250°C. Then, the rise time increases over temperature, while the fall time decreases at 350°C and increases at 400°C. The driver enable times, TZL and TZH, have a similar behavior and all their values meet

the specification transition time. For the driver disable times, TLZ and THZ, the behavior over temperature is similar except from 150°C to 250°C. They both decrease from 25°C to 100°C and from 300°C to 400°C. Their values are slightly higher than 100 ns for most of the temperatures.

The driver propagation delays over temperature have the same behavior, except at 100°C and 200°C, as shown by the skew. They both decreased after 25°C, increased after 150°C, decrease after 250°C and then increase over temperature. The transition time specification is met for most of the temperatures, except at 25°C and 400°C. The receiver propagation delays have a similar behavior from 100°C to 300°C. However, after 25°C, TPHL decreases while TPLH increases.

4.2.2 Test 2: SiC Transceiver with Si Transceiver

The SiC transceiver was connected to a Si 3 V – 5.5 V RS485 with a full-duplex configuration. In this way, the SiC driver was connected to the Si receiver, and the Si driver was connected to the SiC receiver. When in this configuration, the RS-485 transceiver's enable pins for the driver and the receiver are only necessary if the device is designed to be connected to multiple receivers (multi-drop). The full duplex configuration was tested at supply voltages of 12 V for the SiC transceiver, and 3.3 V for the Si transceiver from temperatures of 25°C to 400°C. Transmission frequencies of 20 kHz and 100 kHz were utilized with 2400 ft of cat5e cable. For this configuration, the enable pins for both transceivers are HIGH all the time, while the enable pin for both receivers are OFF. In this way, both drivers are transmitting all the time, while the receivers are acquiring at all times.

The measured switching characteristics for this configuration with 2400 ft of cat5e cable are presented on Table 4.5.

Table 4.5. Test 2 Measured Switching Characteristics with a 2400 ft Cable

PARAMETER	SYMBOL	25°C	100°C	200°C	300°C	400°C	UNITS
Driver Input to Output	TPLH	130	110	100	110	90	ns
	TPHL	120	100	100	110	90	ns
Driver Output Skew to Output	TSKEW	10	10	0	0	0	ns
Driver Rise or Fall Time	TR	50	30	30	20	50	ns
	TF	10	40	60	40	30	ns
Receiver Input to Output	TPLH	600	330	170	190	240	ns
	TPHL	540	380	390	350	390	ns
Differential Receiver Skew	TSKD	60	50	220	160	150	ns

The driver rise and fall times meet the transition time requirement. The driver input to output were slightly higher than the 100 ns transition specification. The receiver input to output values are higher than with any other configurations. The driver enable to output high/low, and the driver disable time from low/high were not measured on this configuration because the enable pins were ON all the time.

4.2.3 Reliability Test

The SiC RS-485 was tested at 300°C for 150 hours using the same high temperature test set up as described previously. The test consisted of placing the board on a hot plate for 50 hours, then allowing it to cool for 64 hours (while the circuit is off) and then placing the board again on the hot plate for another 100 hours. The ramp rate from room temperature to 300°C was 55°C/min. For this test the SiC RS-485 was connected to the Si transceiver with a 2400 ft cat5e cable for 12 V and 100 kHz. A power consumption of 0.6 W was recorded for the 150 hours the device was on the hot plate. During this time, the device consumed 50 mA, achieving the current specification.

Table 4.6 shows an average of the measured values for the reliability test. The driver enable to output high/low, and the driver disable time from low/high were not measured on this configuration because the enable pins were ON all the time.

Table 4.6. Reliability Test for Vulcan II Transceiver

PARAMETER	SYMBOL	300°C	UNITS
Driver Input to Output	TPLH	90	ns
	TPHL	95	ns
Driver Output Skew to Output	TSKEW	5	ns
Driver Rise or Fall Time	TR	40	ns
	TF	30	ns
Receiver Input to Output	TPLH	200	ns
	TPHL	370	ns
Differential Receiver Skew	TSKD	170	ns

All the driver parameters achieved the transition time specified. The receiver input to output values are comparable to the values obtained for the full-duplex configuration at 300°C presented on Table 4.5.

4.2.4 Eye Diagram

In order to evaluate the physical quality of the signal, an eye diagram test was performed for the SiC transceiver with a half-duplex configuration. Eye diagrams allow key electrical parameters of the quality of a signal to be visualized and determined. Eye diagrams are used to calculate the relation between data rate and cable length for drivers and receivers for a twisted pair cable. In order to establish the data rate versus cable lengths curves, it is necessary to calculate the peak to peak jitter from the eye pattern.

The pulse coding used was a form of non-return to zero (NRZ) where a high pulse represents a logic one and a low pulse a logic zero. Equation 4.1 was used to calculate the peak-to-peak jitter, where t_{tcs} is the measured threshold crossing skew and t_{ui} is the unit interval. Fig. 4.8 shows how t_{tcs} and t_{ui} were obtained.

$$\text{Peak-to-Peak Jitter} = \frac{t_{tcs}}{t_{ui}} \times 100\% \tag{4.1}$$

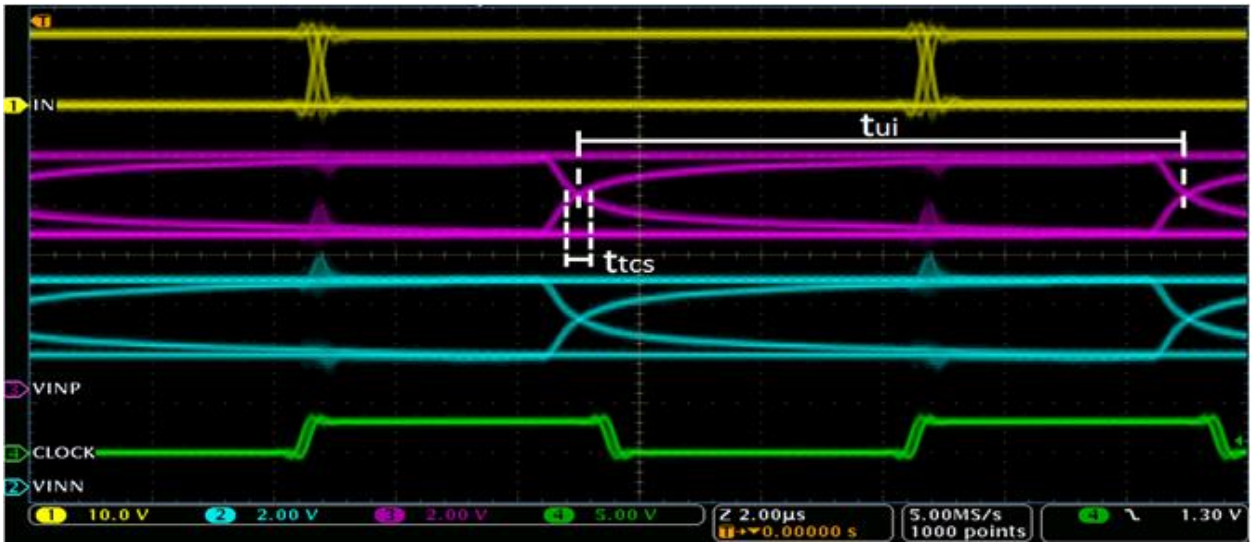


Fig. 4.7. Eye Diagram for 100 kHz and 2400 ft of Cat5e Cable

Table 4.7 shows the peak-to-peak jitter values for the differential input of the receiver using different configurations of frequencies and cable length at room temperature.

Table 4.7. Eye Diagram Peak-to-Peak Jitter Results

CABLE LENGTH (ft)	FREQUENCY (kHz)	SIGNAL NAME	BIT PERIOD (µs)	PEAK TO PEAK JITTER (%)
2400	100	V_{INP}	10	1.6
2400	100	V_{INN}	10	1.8
2400	20	V_{INP}	50	1.2
2400	20	V_{INN}	50	1.2
1200	100	V_{INP}	9.98	1.2
1200	100	V_{INN}	10	1.4

Table 4.7. Eye Diagram Peak-to-Peak Jitter Results (Cont'd)

CABLE LENGTH (ft)	FREQUENCY (kHz)	SIGNAL NAME	BIT PERIOD (µs)	PEAK TO PEAK JITTER (%)
1200	20	V_{INP}	50	1.2
1200	20	V_{INN}	50	1.6
600	100	V_{INP}	9.98	1.6
600	100	V_{INN}	10	1.6
600	20	V_{INP}	50	1.6
600	20	V_{INN}	50	1.6
0	100	V_{INP}	10	2.0
0	100	V_{INN}	9.98	2.0
0	20	V_{INP}	50	2.4
0	20	V_{INN}	50	2.2

Measured results in Table 4.8 show a bit period of 50 µs for 20 kHz and almost 10 µs for all signals at 100 kHz. The peak-to-peak jitter stays at 1% for 600 ft, 1200 ft, and 2400 ft, while it increases to 2% without a cat5e cable.

4.2.5 Discussion of the Experimental Results

The experimental results shown on Fig. 4.5, Fig. 4.6, Table 4.4 and Table 4.5, demonstrate that the SiC RS–485 transceiver is capable of operating at temperatures as high as 400°C over 2400 ft of cat5e cable.

Table 4.8 shows the simulated and measured values for the Vulcan II RS-485 with a power supply of 15 V, frequency of 100 kHz with a half-duplex configuration without a cable.

Table 4.8. Vulcan II RS-485 Simulation and Measured Values without a Cable

PARAMETER	SYMBOL	SIMULATION VALUES		MEASURED VALUES		UNITS
		25°C	300°C	25°C	300°C	
Driver Input to Output	TPLH	46	33	60	46	ns
	TPHL	48	34	80	54	ns
Driver Output Skew to Output	TSKEW	2	1	20	8	ns
Driver Rise or Fall Time	TR	26	17	80	28	ns
	TF	18	12	80	24	ns
Driver Enable to Output High	TZH	48	34	80	62	ns
Driver Enable to Output Low	TZL	43	30	100	58	ns
Driver Disable Time from Low	TLZ	20	12	60	68	ns
Driver Disable Time from High	THZ	46	31	160	64	ns
Receiver Input to Output	TPLH	257	186	180	174	ns
	TPHL	289	222	260	250	ns
Differential Receiver Skew	TSKD	32	36	80	76	ns

The switching characteristics decrease as temperature increases for both the simulated and measured values. The transition time specification is achieved for all the driver simulation values. However, for the measured values, the transition time was achieved for most of the driver measured values, but for the driver disable time from high at 25°C. The receiver input to output values decrease over temperature for both the simulated and measured values. Overall, the measured values are slightly smaller than for the simulation values.

A comparison from the Vulcan II RS-485 simulation results and the measured results with a 4 m cable is shown in Table 4.9.

Table 4.9. Vulcan II RS-485 Simulation and Measured Values with a 4 m Cable

PARAMETER	SYMBOL	SIMULATION VALUES		MEASURED VALUES		UNITS
		25°C	300°C	25°C	300°C	
Driver Input to Output	TPLH	34	25	120	60	ns
	TPHL	39	29	120	70	ns
Driver Output Skew to Output	TSKEW	5	4	0	10	ns
Driver Rise or Fall Time	TR	52	52	80	60	ns
	TF	45	46	60	60	ns
Driver Enable to Output High	TZH	46	33	160	140	ns
Driver Enable to Output Low	TZL	43	31	130	110	ns
Driver Disable Time from Low	TLZ	22	13	230	150	ns
Driver Disable Time from High	THZ	40	26	220	170	ns
Receiver Input to Output	TPLH	261	191	250	220	ns
	TPHL	306	234	220	220	ns
Differential Receiver Skew	TSKD	45	43	30	20	ns

The switching characteristics decrease as temperature increases for both the simulated and measured values. The transition time specification is achieved for all the driver simulation values. However, for the measured values, the transition time was achieved for most of the driver measured values, but for the driver input to output values at 25°C, the driver enable to output high/low and driver disable time from high/low for both temperatures. The receiver input to output values decrease over temperature for both the simulated and measured values. Overall, the measured values are slightly smaller than the values for the simulation values, but for TPHL at 300°C.

The rise and fall times for the half–duplex configuration with a without cable begin to decrease after 25°C. These results show that at high temperature, SiC circuits perform better. This behavior can be attributed to the release of carrier charges from interface traps in strong inversion at high temperatures, a phenomenon that is common in SiC semiconductor devices [28], [29]. The interface between the substrate and silicon dioxide in SiC MOSFETs is not very smooth. As a result, the surface roughness and the interface trapped charges make the mobility of SiC MOSFETs very low at room temperature [29]. As the temperature increases, the probability of carriers being trapped becomes smaller, and the mobility increases [30]. The higher threshold voltage and mobility values improve the performance until the temperature reaches 200 ℃. Almost all the interface states are empty at temperatures higher than 200 ℃. In this way, mobility starts to fall, and the gain of the devices decreases [31].

The results for the propagation delays are related to the movement of the threshold voltage over time, multiple thermal cycles and the stress it causes on the devices. During temperature cycling, the mismatch in thermal expansion coefficients between the pad and the wirebond increases and may cause the bond to fail [32]. In addition, aging and multiple temperature cycles were found to cause high offset issues that led to performance degradation and the non–functionality of circuits [33].

The experimental results on Table 4.5 for the full duplex configuration show a more complicated dynamic. These results for the rise and fall times are related to the effect of the temperature cycles on the devices and the signal degradation due to the long cable. Normal cat5e distance is limited to 328 ft when dealing with normal protocols because of transmission windows.

The typical limit temperature for traditional silicon MOSFET integrated circuits is around 125°C [34], while silicon on insulator technology goes up to 200°C [35], [36]. The SiC CMOS RS–485 performs its digital logic function for the whole temperature range of 25 – 400°C. This performance makes the SiC RS–485 a viable solution for high temperature industrial applications.

CHAPTER 5 CONCLUSIONS AND FUTURE WORK

This thesis has presented the overall design of an RS-485 in a SiC CMOS process technology. The first SiC transceiver was designed for operation from room temperature to 300°C over 2400 ft of cat5e cable. The circuit was subsequently fabricated and tested up to 400°C with different cable lengths. A full-duplex configuration was used to test the transceiver with a Si 3.3 V transceiver over 2400 ft of cat5e cable. Therefore, demonstrating the implementation of a data acquisition and transmission system from a hot to a cooler environment.

The main objective was to design a circuit that would function with good performance characteristics in order to compete with the commercial silicon transceivers. The device has been tested at supply voltages of 12 V and 15 V. Test results have shown that the device performance better at higher temperatures due to the nature of the SiC material. Reliability testing was conducted on the SiC transceiver at 300°C for 150 hours. This device brings us closer to a large-scale data processing and control system for extreme environments without the need of expensive and complicated thermal management needed for conventional silicon devices.

Future work will include the implementation of the device in a SiC data acquisition board. This integration could lead to a data acquisition system for high temperature application such as deep earth drilling, industrial control systems, automated protocols, and aerospace systems.

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