5-2017

Short-Circuit Protection for Low-Voltage DC Distribution Systems Based on Solid-State Circuit Breakers

Sharthak Munasib
University of Arkansas, Fayetteville

Short-Circuit Protection for Low-Voltage DC Distribution Systems Based on Solid-State Circuit Breakers

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

by

Sharthak Munasib
Bangladesh University of Engineering and Technology
Bachelor of Science in Electrical Engineering, 2012

May 2017
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

_____
Dr. Juan C. Balda
Thesis Director

_____
Dr. Simon S. Ang
Committee member

_____
Dr. Yue Zhao
Committee member

ABSTRACT

Proper short-circuit protection in dc distribution systems has provided an austere challenge to researchers as the development of commercially-viable equipment providing fast operation, coordination and reliability still continues. The objective of this thesis is to analyze issues associated with short-circuit protection of low-voltage dc (LVDC) distribution systems and propose a short-circuit protection methodology based on solid-state circuit breakers (SSCBs) that provides fault-current limiting (FCL). Simulation results for a simplified notional 1-kVdc distribution system, performed in MATLAB/SIMULINK™, would be presented to illustrate that SSCB solutions based on reverse-blocking integrated gate-commutated thyristors (RB-IGCT) are feasible for low-voltage dc distribution systems but requires connecting several devices in parallel to open fast-rising fault currents. To validate the implementation of the FCL function, the coordination between upstream and downstream SSCBs during a fault at different operating conditions of the system is presented. In addition, several fault-detection techniques would be compared by means of the let-through energies, and the impact of FCL on the thermal handling requirements of the RB-IGCT would also be discussed.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my advisor, Dr. Juan C. Balda, for his guidance and encouragement throughout my Master's degree. His constructive advices and critiques helpmed me progress my research in a timely manner. I would also like to thank my thesis committee members Dr. Simon S. Ang and Dr. Yue Zhao.

The work accomplished for this thesis was supported under research contract from ONR and ABB (Raleigh, NC). I would like to express my gratefulness for their financial support for pursuing my graduate studies.

Finally, I would like to thank my caring parents, my younger brother, and my lovely wife for being a source of inspiration all the way.

DEDICATION

This MSEE thesis is dedicated to my parents, my younger brother Swapno, and my wife Joyotree. I would not have accomplished this degree without your continuous help and reassurance.

TABLE OF CONTENTS

1 Introduction 1
1.1 DC Electric Power Distribution 1
1.2 Protection Challenges Associated with DC Distribution Systems 3
1.3 Literature Review of the Proposed SSCB Topologies 5
1.4 Thesis Objectives 8
1.5 Organization of the Theis 9
1.6 References 10
2 Notional Low-Voltage DC Distribution System 14
2.1 Introduction 14
2.2 System Description 14
2.3 System Simulations 17
2.4 Modeling of SSCB 18
2.4.1 Commonly used semiconductors for SSCBs 18
2.4.2 Development of the IGCT 19
2.4.3 Modeling of an RB-IGCT as Solid-state Switch in a SSCB 19
2.4.4 Switching Characteristics 21
2.5 Summary 22
2.6 References 23
3 Short-Circuit Protection Methodology incorporating a Fault-Current-Limiting Function 24
3.1 Introduction 24
3.2 Fault Behavior of Notional Low-Voltage DC Distribution System 25
3.3 Proposed FCL Control Circuit based on Overcurrent Protection 29
3.4 Fault Analysis under FCL operation Integrated with Controller Delays 31
3.5 Fault Analysis without Energy-Storage Filter Capacitor at 1kVdc Load-Center Bus 33
3.6 Coordination between Upstream and Downstream SSCBs during FCL Operation 37
3.7 Summary 41
3.8 References 41
4 Impact of FCL Function on the Operation of the Notional 1-kVDC System 42
4.1 Introduction 42
4.2 Fault-Current Detection Techniques 42
4.3 Let-through Energy Comparison between Different Fault-Detection Techniques 44
4.4 Comparison of Undervoltage and Overcurrent Threshold 44
4.5 Impact of Fault-Current-Limiting on RB-IGCT's Thermal Handling Requirement 46
4.6 Impact of Fault-Current-Limiting on Metal-Oxide Varistors 52

4.7 Summary 55
4.8 References 55
5 Conclusions and Recommendations for Future Work 57
5.1 Conclusions 57
5.2 Recommendations for Future Work.....59
Appendix A 60

LIST OF FIGURES

Fig. 1.1: Notional MVDC ring bus topology 2
Fig. 1.2: Schematic diagram for SiC SGTO Fault Current Limiter 6
Fig. 1.3: Schematic diagram for Emitter Turn-off DC Circuit Breaker 7
Fig. 1.4: Schematic diagram of solid-state protection device 7
Fig. 1.5: A unidirectional self-powered SSCB using a normally-on SiC JFET 8
Fig. 2.1: Circuit diagram of a post-regulated isolated dc-dc converter powering a simplified 1kVdc zone 15
Fig. 2.2: Single-bus single-breaker configuration for 1kVdc zone 15
Fig. 2.3: Current waveforms at the 1-kVdc load center bus, DC Load 1, DC Load 2 and AC Load Center input under rated steady-state conditions 17
Fig. 2.4: GTO model in Simulink™: (a) symbol (b) equivalent circuit 20
Fig. 2.5: Circuit-based modeling of the RB-IGCT 20
Fig. 2.6: RB-IGCT turn-off waveforms 22
Fig. 3.1: (a) Circuit schematic1-kVdc load center during a pole-to-pole fault at "DC Load 1", (b) equivalent circuit during the fault 26
Fig. 3.2: Fault-current contributions from the buck and energy-storage capacitor for a pole to-pole fault at DC Load 1 (without short-circuit protection at the 1-kVdc load center) 27
Fig. 3.3: Fault-current control circuit implementing FCL function (a) block diagram (b) Simulink representation 29
Fig. 3.4: XOR Gate: (a) structure (b) truth table 30
Fig. 3.5: Current waveforms at the the buck converter output, 1-kVdc load center filter capacitor, DC Load 1, DC Load 2, AC Load for a pole-to-pole fault at "DC Load 1" at t = 0.5 s 31
Fig. 3.6: Voltage waveforms at the buck converter output, load center and ac load buses for a pole-to-pole fault at "DC Load 1" at t=0.5 s 32
Fig. 3.7: Current waveforms at the buck converter output, DC Load 1, DC Load 2, AC Load for a pole-to-pole fault at "DC Load 1" at t = 0.5 s (filter capacitor at load-center bus removed) 35
Fig. 3.8: Voltage waveforms at the buck converter output, dc load and ac load buses for a pole-to-pole fault at "DC Load 1" at t = 0.5 s; load capacitors sized for 10% voltage ripple 35
Fig. 3.9: Voltage waveforms at the buck converter output, dc load and ac load buses for a pole-to-pole fault at "DC Load 1" at t = 0.5 s; load capacitors sized for 5% voltage ripple 36
Fig. 3.10: Voltage waveforms at the buck converter output, dc load and ac load buses for a pole-to-pole fault at "DC Load 1" at t = 0.5 s; load capacitors sized for 1% voltage ripple 36
Fig. 3.11: Current waveforms at the buck converter output, DC Load 1, DC Load 2, AC Load for a pole-to-pole fault at "DC Load 1" at t = 0.5 s (case 1) 37
Fig. 3.12: Voltage waveforms at the buck converter output, dc load and ac load buses for a pole-to-pole fault at "DC Load 1" at t = 0.5 s (case 1) 38
Fig. 3.13: Current waveforms at the buck converter output, DC Load 1, DC Load 2, AC Load for a pole-to-pole fault at "DC Load 1" at t = 0.5 s (case 2) 39
Fig. 3.14: Voltage waveforms at the buck converter output, dc load and ac load buses for a pole-to-pole fault at "DC Load 1" at t = 0.5 s (case 2) 40

Fig. 4.1: Simplified circuit diagram for 1-kVDC load center for simulation of FCL impact on MOV 53
Fig. 4.2: RB-IGCT turn-off waveforms 53

CHAPTER 1

INTRODUCTION

1.1 DC Electric Power Distribution

The use of direct current (dc) for low-voltage distribution systems has recently gained momentum, as validated by recent trends and developments in the power industry. Traditionally, alternating current (AC) systems have been adopted worldwide as the main means of distribution. The main systems of an electrical power grid can be classified as - generation, transmission and distribution of power to loads [1,2]. Conventionally, each of these stages handles ac power and the necessary AC equipment have been in use for years. But with advancements in power electronic equipment, research community and industry alike have become intrigued in discussing the possibilities of developing effective dc distribution system architectures and relevant power electronic and protection devices. There are three main types of dc distribution architectures that are obtained from literature [1-4,8-12]:

- Radial distribution: This is the most basic configuration for distribution of power, in which a source supplies power to one or more loads via a common point, i.e. busbar. This type of distribution system is easier to protect against faults and is comparatively cheaper to construct.
- Ring bus: The ring bus architecture, as shown in Fig. 1.1, provides an additional supply path for distribution of power, and hence, added tolerance against faults on the line.
- Zonal distribution: This distribution system incorporates distribution divided in zones, with two or more geographically separated transmission segments providing power to

the zones, increasing redundancy of supply and presenting the opportunity to optimise the power dispatch of generation across the entire network. Zones are classified based on the operation, i.e. supply zones, zones containing load centers. Of particular interest for the application of this type of distribution are shipboard power systems ,i.e. notional all-electric ship [3,4].

The potential benefits of dc power distribution in comparison with the traditional ac distribution system are [5-9]:

- Higher power transfer capability through the power line having the same voltage rating as an ac system: AC conductors deliver power dictated by the RMS voltage, whilst the insulation level of the cables is determined using the peak voltage. However, DC conductors can transmit power using the full voltage rating of the cable. This provides a higher power transfer than ac systems by a factor of √2. Other attributes include zero skin effect and zero reactive voltage drop. All of these combine to facilitate reduction of conductor sizes, and hence, cost [5].
- Convenient interfacing of multiple non-synchronous sources in the same dc bus : This could facilitate the integration of renewable energy sources in dc microgrids. For

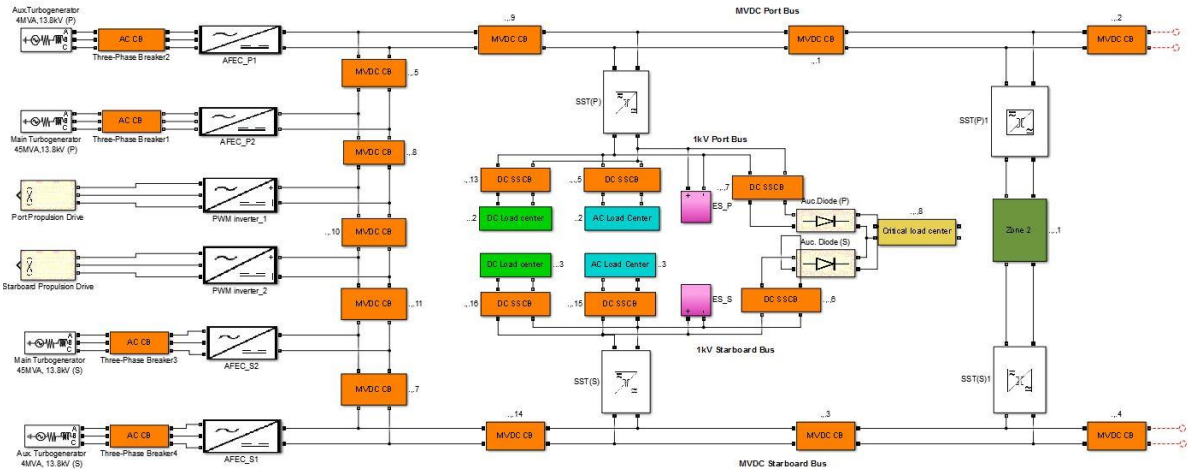


Fig. 1.1. Notional MVDC ring bus topology

onboard distribution systems such as all-electric ships or more-electric aircrafts, this is equivalent to the integration of frequency-decoupled generators that operate with the prime mover speed at optimum into the dc distribution bus. This ensures better dynamic performance of the system with improved connection of multiple sources [6].

- Reduction of power conversion stages starting from the source side moving on to the load side;
- Overall increase in system efficiency complemented by reduced weight and volume [7].

These advantages are driving a major shift in the use of dc distribution systems in recent years. Typical applications range from large scale multiterminal dc systems to physically compact power networks such as dc microgrids [8,9], shipboard power systems [10] and aircraft applications [11,12]. The discussion of benefits presented above directly apply to all of these applications, thus justifying the need for an analysis of the challenges and opportunities posed by the applications. One of the prime challenges, protection against faults in dc systems, will be briefly discussed in the next section along with the proposed solutions in literature.

1.2 Protection Challenges Associated with DC Distribution Systems

Any protection system design needs to abide by the following criteria [8]:

- Reliability
- Selectivity
- Stability
- Speed
- Sensitivity

An important concern with compact dc systems is the isolation of faults without disrupting the operation of the entire dc system. Typical faults that are evident are : short-circuit

faults, ground or pole-to-pole faults, and open-circuit faults, existing in architectures like multi-terminal dc lines and multi-source distribution systems. Fault currents in dc systems have much higher rates of rise compared to ac systems because the commonly-employed filter dc capacitors at the output of power converters normally discharge through low cable impedances [8]. This often requires over dimensioning of components, and makes it difficult to accomplish coordination among downstream and upstream protection devices because the time for the downstream device to open before the upstream device operates is very short [13]. So, it may be possible that an upstream breaker trips simultaneously with a downstream breaker. So, coordination of inverse time vs. current characteristics in dc systems is still an up-and-coming research topic.

Unlike traditional ac systems where a natural zero crossing of the current is utilized for opening a circuit breaker and fault isolation, short-circuit currents in dc systems must be interrupted at high values to open the faulted branch. Major approaches for dc microgrid short-circuit protection can be divided into “breaker-less” and “breaker-based” schemes [16-17]. The former utilizes coordinated control of power converters to interrupt first the current and then no-load mechanical contactors to isolate the faulted section, as well as reconfigure and re-energize the system [18-19]. A “breaker-based” approach should provide more flexibility because the circuit breaker should isolate the fault but enable continued operation of the non-faulted system faster. The challenge is developing a compact and power-dense SSCB with the capability of rapid energy dissipation [16].

Mechanical circuit breakers have been used as the go-to solution for the traditional ac distribution systems for a number of decades now. But in comparison with the fault current behavior in a dc system, these breakers suffer from several disadvantages. A comparatively slow

response time, thus exposing the network components to an extremely high amplitude of fault current, risks severe damage to both equipment and personnel. The longer time also results in voltage sags near the faulted portion of the system, which threaten the required continuous operation of critical loads which would then require equipment like UPS for constant power flow. Another major disadvantage is the lack of natural zero-crossing of current, meaning the presence of arc cannot be ignored by controlling the switching of the circuit breaker. All of these demerits have prompted the researchers to look for solutions that are able to meet the protection requirements for dc distribution systems. Due to recent advances of semiconductor devices capable of interrupting high fault currents within microseconds for fault-current-limiting applications, SSCBs have proved to be the potentially effective solution. SSCB solutions proposed in literature along with their applications will be briefly discussed in the following section.

1.3 Literature Review of the Proposed SSCB Topologies

Cost-effective commercial dc SSCBs are not yet available, although many prospective topologies are offered in the literature [15-36]. The semiconductor devices usually used are: thyristors, insulated gate bipolar transistors (IGBTs), integrated gate commutated thyristors (IGCTs), and gate turn-off thyristors (GTO). The major disadvantages remain to be the on-state losses, robustness to overvoltages, and solution cost. So far, significant research has only been done on HVDC or MVDC systems, but for low-voltage dc distribution, the research stage is still very preliminary [21-24].

For traditional ac distribution systems, a significant amount of research implementing thyristor-based fault-current-limiting solutions have been described in [27,28]. Thyristors have the advantages of low conduction losses and high short-circuit current capability. GTOs were

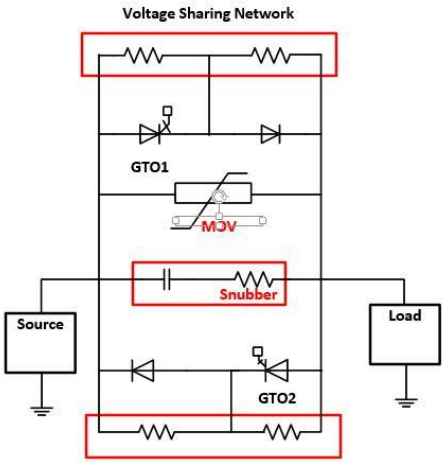


Fig. 1.2. Schematic diagram for SiC SGTO Fault Current Limiter

considered because of not only their lower conduction losses and higher short-circuit current capabilities compared to IGBTs, but also for not requiring auxiliary circuits for turn off. References [29-31] presented proposals based on super GTOs making use of silicon carbide materials.

A new topology for a fault current limiter was proposed using a combination of a silicon controlled rectifier (SCR) and an IGBT forming the main switch in [32]. An input buffer was necessary to absorb energy during fault current limiting. The purpose of using SCR in the main conducting path is to get a comparatively lower voltage drop since electromechanical circuit breakers have ideally zero voltage drops. RCD or a voltage-clamped snubber was used across the semiconductor devices for energy absorption when interrupting an inductive circuit.

A modification of dc circuit breakers based on thyristors with forced current commutation performed in two stages to counter overvoltages usually observed in a single stage commutation has been suggested [33]. The prototype was built to handle a maximum rate of rise of fault current of 12 A/s for a 700 V dc source with a source inductance of about 60 μH. Complete current interruption was achieved within 5 ms for short-circuit conditions.

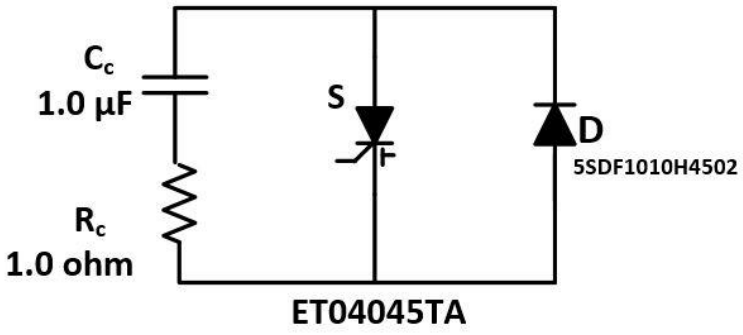


Fig. 1.3. Schematic diagram for Emitter Turn-off DC Circuit Breaker

The structure of Emitter Turn-off (ETO) thyristor-based DC circuit breaker is shown in Fig. 1.3 [34]. An RC snubber in parallel is provided to limit rate of voltage rise and a diode provides freewheeling path. The ETO was chosen for its built-in current sensing feature because of the emitter switch voltage providing an indication of the current flowing during the on-state. The gate drive circuit for over-current protection was designed such that the emitter switch voltage is above a certain reference value. The main features include fast switching, built-in current sensing and voltage-control capability. A 1.5 kA/2.5 kV DC circuit breaker prototype was built, which provides a compact structure and a fast response time of about 5 µs.

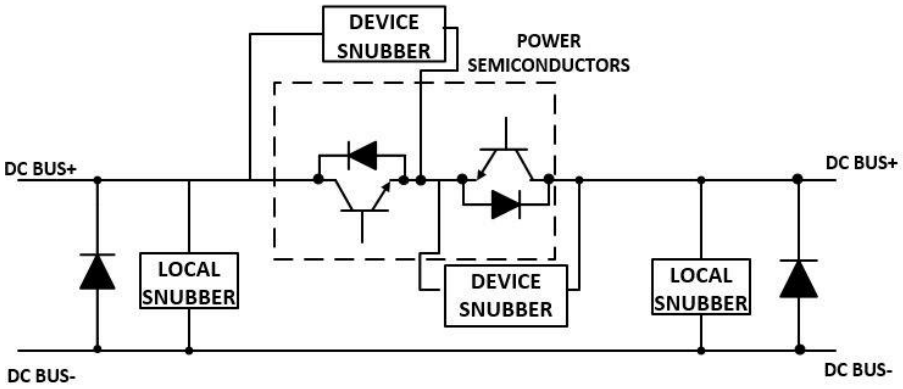


Fig. 1.4. Schematic diagram of solid-state protection device

A bidirectional Solid-State Protection Device is shown in Fig. 1.4 [35]. The power semiconductor devices suggested for this application are IGBT or IGCT. IGBT- and IGCT-based SSPDs are proposed, which are rated at 1000V, 1800A and 1000V, 1000A respectively. These devices implement fault interruption by quickly driving the fault current to zero. Wide-Band-Gap (WBG) devices (i.e., mainly SiC or GaN devices) are the latest addition to SSCB applications. One topology uses SiC JFET for a self-powered SSCB which senses voltage across the JFET to send a signal to the driver circuit to reverse-bias the JFET, as shown in Fig. 1.5 [36]. Experimental results show a current-capability of 180 Amps interrupted within 0.8 μs for a 400-V dc system.

There are many topologies for SSCBs proposed by researchers, among which the more important ones are discussed above. The topologies try to address the concerns regarding the short-circuit protection of dc distribution systems mentioned in Section 1.2. The use of an SSCB to implement short-circuit protection for low-voltage dc distribution systems will be elucidated in the following section.

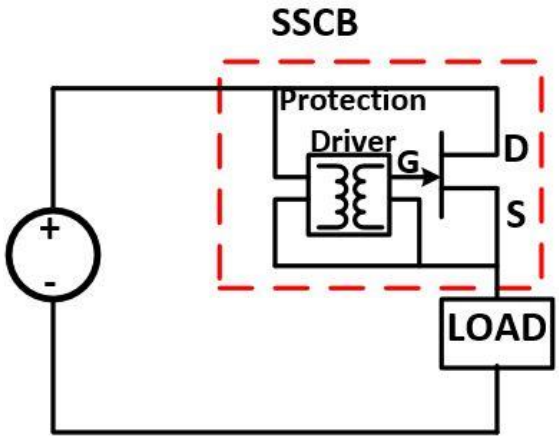


Fig. 1.5. A unidirectional self-powered SSCB using a normally-on SiC JFET

1.4 Thesis Objectives

The integration of power converters influences the fault characteristics of dc distribution systems, which asks for challenging protection schemes. The main objective of this thesis is to develop a solution that would be able to provide fault-current limiting, delivering unhampered power to unfaulted loads and achieve coordination between the upstream and downstream protection devices. To accomplish this objective and to augment the analysis to be applied to complex dc distribution systems, the following activities should be accomplished:

- Simulation setup for a simplified 1kVdc zone powered by an isolated post-regulated dc-dc converter,
- Matlab/Simulink™ simulation studies showing a potential application of the FCL function with coordination between upstream and downstream SSCBs,
- Comparison of different fault current threshold techniques along with sensitivity analysis of undervoltage threshold technique compared to overcurrent threshold,
- Impact of fault-current-limiting (FCL) on RB-IGCT's thermal handling requirements, and
- Impact of fault-current limiting on Metal-Oxide Varistors (MOV).

1.5 Organization of the Thesis

Development of a notional low-voltage dc system will be presented in chapter 2, starting with an overview of system followed by brief descriptions of the components and modeling of the SSCB using RB-IGCT. A detailed short-circuit analysis of the simplified 1kVdc system, along with comparison between different fault detection techniques, and a sensitivity analysis based on cable lengths, will be described in chapter 3.

The proposed fault-current-limiting algorithm, control circuit and simulations performed in MATLAB/Simulink™, together with the algorithm's impact on the thermal capability of the RB-IGCT, will be demonstrated in chapter 4. The conclusions and the recommendations for future work are presented in chapter 5.

1.6 References

[1] T. Gonen, Electric Power Distribution System Engineering, Second Edition. Boca Raton, FL: CRC Press Taylor & Taylor Group, 2008.

[2] L. M. Faulkenberry and W. Coffer, Electrical Power Distribution and Transmission. Englewood Cliffs, NJ: Prentince Hall, 1996.

[3] Chalfant, J.S. and Chryssostomos C., "Analysis of various all-electric-ship electrical distribution system topologies." In *Electric Ship Technologies Symposium (ESTS), 2011 IEEE*, pp. 72-77. IEEE, 2011.

[4] Langston, J., et al. "Waveform-Level Time-Domain Simulation Comparison Study of Three Shipboard Power System Architectures." *Proc. 2012 Grand Challenges in Modeling and Simulation* (2012).

[5] D. Nilsson, A. Sannino, "Efficiency analysis of low- and medium voltage dc distribution systems," *Power Engineering Society General Meeting*, vol. 2, pp. 2315 – 2321, June 2004.

[6] M. E. Baran and N. R. Mahajan, "DC Distribution for Industrial Systems: Opportunities and Challenges," *IEEE Trans. Industry Applications*, vol. 39, no. 6, pp. 1596–1601, November/December 2003

[7] K. Shenai and K. Shah, "Smart dc micro-grid for efficient utilization of distributed renewable energy," in *Energytech*, 2011 IEEE, May 2011.

[8] R. Cuzner and G. Venkataramanan, "The status of DC micro-grid protection," in *Industry Applications Society Annual Meeting*, 2008. IAS '08. IEEE, Oct. 2008, pp. 1–8.

[9] D. Salomonsson, L. Soder, and A. Sannino, "Protection of low-voltage dc microgrids," *Power Delivery, IEEE Transactions on*, vol. 24, no. 3, pp. 1045–1053, July 2009.

[10] R. Schmerda, R. Cuzner, R. Clark, D. Nowak and S. Bunzel, "Shipboard Solid-State Protection: Overview and Applications," in *IEEE Electrification Magazine*, vol. 1, no. 1, pp. 32-39, Sept. 2013.

[11] S. Fletcher, P. Norman, S. Galloway and G. Burt, "Solid state circuit breakers enabling optimised protection of DC aircraft power systems," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, Birmingham, 2011, pp. 1-10.

[12] M. Komatsu, N. Ide and S. Yanabu, "A Solid-State Current Limiting Switch for Application of Large-scale Space Power Systems," in *2007 IEEE Power Electronics Specialists Conference*, Orlando, FL, 2007, pp. 1471-1476.

[13] Fletcher, S.D.A.; Norman, P.J.; Galloway, S.J.; Crolla, P.; Burt, G.M., "Optimizing the Roles of Unit and Non-unit Protection Methods Within DC Microgrids," in *Smart Grid, IEEE Transactions on* , vol.3, no.4, pp.2079-2087, Dec. 2012

[14] Cuzner, R.M.; Singh, V.; Rashidi, M.; Nasiri, A., "Converter topological and solid state protective device trade-offs for future shipboard MVDC systems," in *Electric Ship Technologies Symposium (ESTS)*, 2015 IEEE , vol., no., pp.34-39, 21-24 June 2015

[15] Park, J.-D.; Candelaria, J., "Fault Detection and Isolation in Low-Voltage DC-Bus Microgrid System," in *Power Delivery, IEEE Transactions on* , vol.28, no.2, pp.779-787, April 2013

[16] Qiu, D., Liu ,X., Soman, R., Steurer, M. and Dougal, R.A. "Primary and backup protection for fault current limited MVDC shipboard power systems." In *Electric Ship Technologies Symposium (ESTS)*, IEEE, pp. 40-47, 2015.

[17] Cairoli, P.; Dougal, R.A.; Lentijo, K., "Coordination between supply power converters and contactors for fault protection in multi-terminal MVDC distribution systems," In *Electric Ship Technologies Symposium (ESTS)*, IEEE , vol., no., pp.493,499, 22-24 April 2013

[18] Jin, C., Dougal, R.A. and Liu, S. "Solid-state Over-current Protection for Industrial DC Distribution Systems," In *4th International Energy Conversion Engineering Conference and Exhibit (IECEC)*, pp. 26-29. June 2006.

[19] Cuzner, R.; MacFarlin, D.; Clinger, D.; Rumney, M.; Castles, G., "Circuit breaker protection considerations in power converter-fed DC Systems," In *Electric Ship Technologies Symposium*, 2009. ESTS 2009. IEEE , vol., no., pp.360-367, 20-22 April 2009

[20] Agostini, F., Umamaheswara V., Daniele T., Martin Arnold, Munaf R., Antonello A., Luca R., Davide P., and Harish S.. "1MW bi-directional DC solid state circuit breaker based on air cooled reverse blocking IGCT." In *Electric Ship Technologies Symposium (ESTS)*, 2015 IEEE, pp. 287-292. IEEE, 2015.

[21] Steurer, M., Klaus F., Walter H., and Kaltenegger, K. "A novel hybrid current-limiting circuit breaker for medium voltage: principle and test results." *Power Delivery, IEEE Transactions on* 18, no. 2 (2003): 460-467.

[22] Sano, K, and Masahiro T. "A surge-less solid-state dc circuit breaker for voltage source converter based HVDC transmission systems." In *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, pp. 4426-4431. IEEE, 2012.

[23] C. Meyer, S. Schroder and R. DeDoncker, "Solid-State Circuit Breakers and Current Limiters for Medium-Voltage Systems Having Distributed Power Systems", in *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1333-1340, 2004.

[24] Kempkes, M., I. Roth, and M. Gaudreau. "Solid-state circuit breakers for medium voltage DC power.", in *Electric Ship Technologies Symposium (ESTS)*, IEEE, 2011

[25] C. Meyer, M. Hoing and R. W. De Doncker, "Novel solid-state circuit breaker based on active thyristor topologies," *Power Electronics Specialists Conference*, 2004. PESC 04. 2004 IEEE 35th Annual, 2004, pp. 2559-2564 Vol.4.

[26] G. G. Karady, "Principles of fault current limitation by a resonant LC circuit," in *IEE Proceedings C - Generation, Transmission and Distribution*, vol. 139, no. 1, pp. 1-6, Jan. 1992.

[27] O. Saadeh, E. Johnson, M. Saadeh, A. Escobar Mejía, H. C. Schinmer, B. Rowden, A. Mantooth, J. C. Balda, S. S. Ang, "A 4kV Silicon Carbide Solid State Fault Current Limiter", in *IEEE Energy Conversion Conference and Exposition* (ECCE 2012), September 15-20, Raleigh, North Carolina.

[28] Mantooth, H.A.; Saadeh, O.; Johnson, E.; Balda, J.C.; Ang, S.S.; Lostetter, A.B.; Schupbach, R.M.; , "Solid-state fault current limiters: Silicon versus silicon carbide," in *Power and Energy Society General Meeting - Conversion and Delivery of Electrical Energy in the 21st Century*, 2008 IEEE , vol., no., pp.1-5, 20-24 July 2008.

[29] A. Escobar, M. Saadeh, J.C. Balda, J. Bourne, Y. Feng, H. A. Mantooth, "A methodology to coordinate solid-state fault current limiters with conventional protective devices," in *IEEE/PES Power Systems Conference and Exposition (PSCE)*, 2011, Phoenix (AZ), 20-23 March 2011.

[30] Y. Feng, M. Saadeh, A. Escobar Mejia, J.C. Balda, S. S. Ang, H. A. Mantooth, "A Solid State Fault Current Limiter Control Algorithm", *9th International Power and Energy Conference*, October 27-29, 2010, Singapore.

[31] Y. Feng, E. Johnson, O. Osama, J.C. Balda, H. A. Mantooth, R. M. Schupbach, "Impact of Solid-State Fault Current Limiters on Protection Equipment in Transmission and Distribution Systems", *IEEE PES Transmission and Distribution Conference*, New Orleans (LA), April 19-22, 2010.

[32] McEwan, Peter M., and Sarath B. Tennakoon. "A two-stage DC thyristor circuit breaker." *Power Electronics, IEEE Transactions on* 12, no. 4, pp. 597-607. (1997)

[33] Luo, F., Jian C., Xinchun L., Yong K., and Shanxu D. "A novel solid state fault current limiter for DC power distribution network." In *Applied Power Electronics Conference and Exposition*, 2008. APEC 2008. Twenty-Third Annual IEEE, pp. 1284-1289. IEEE, 2008

[34] Xu, Z., Bin Z.,Sirisukprasert, S. Zhou,X. and Huang, A.Q. "The emitter turn-off thyristor-based DC circuit breaker." In *Power Engineering Society Winter Meeting, IEEE*, vol. 1, pp. 288-293. IEEE, 2002.

[35] Schmerda, R., Cuzner R., Robin C., Damian N., and Bunzel.,S. "Shipboard solid-state protection: Overview and applications." *Electrification Magazine, IEEE* , no.1,pp. 32-39 (2013)

[36] Z. Miao et al., "A self-powered ultra-fast DC solid state circuit breaker using a normally-on SiC JFET," In *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 767-773.

CHAPTER 2

NOTIONAL LOW-VOLTAGE DC DISTRIBUTION SYSTEM

2.1 Introduction

A notional low-voltage dc distribution system, adopted for performing short-circuit protection studies in later chapters, will be presented in this chapter. Relevant component and device data are also provided. This system can be considered as a low-voltage dc microgrid, with various loads powered through the use of power converters. This system would facilitate the study of dc faults, and the impact of filter capacitors of power converters during short-circuit conditions. A detailed understanding of the response of the converter-interfaced dc distribution systems would enable developing a concrete approach to defining protection requirements and designing control circuits.

2.2 System Description

Figure 2.1 depicts the circuit schematic of a post-regulated isolated dc-dc converter powering a simplified 1kVdc load center bus, which has two dc loads and one ac load. The Matlab/Simulink^{TM} implementation of this circuit schematic is provided in Appendix A. The parameters for the 1-kVdc load center are given in Table 2.1. The complete system parameters can be obtained by combining the parameters provided in Table 2.1 and Appendix A. The bus arrangement is similar to the single-bus, single-breaker topology normally used in conventional ac power distribution systems, which is shown in Fig. 2.2. Characteristics of this simplified 1-kVdc bus and connected loads are described below.

2.2.1 Unidirectional Post-Regulated Isolated DC-DC Converter: The medium-voltage dc side is simply modeled by an ideal voltage source rated 20 kV, and a 20kV-1kV, 7.5 MW unidirectional post-regulated isolated dc-dc converter (PRIDCC) because the interest is in evaluating the 1-kVdc zone performance under different scenarios. The PRIDCC consists of a solid-state transformer (SST) having a controlled half-bridge on the primary side, and a diode-based half bridge on the secondary side, followed by a buck converter

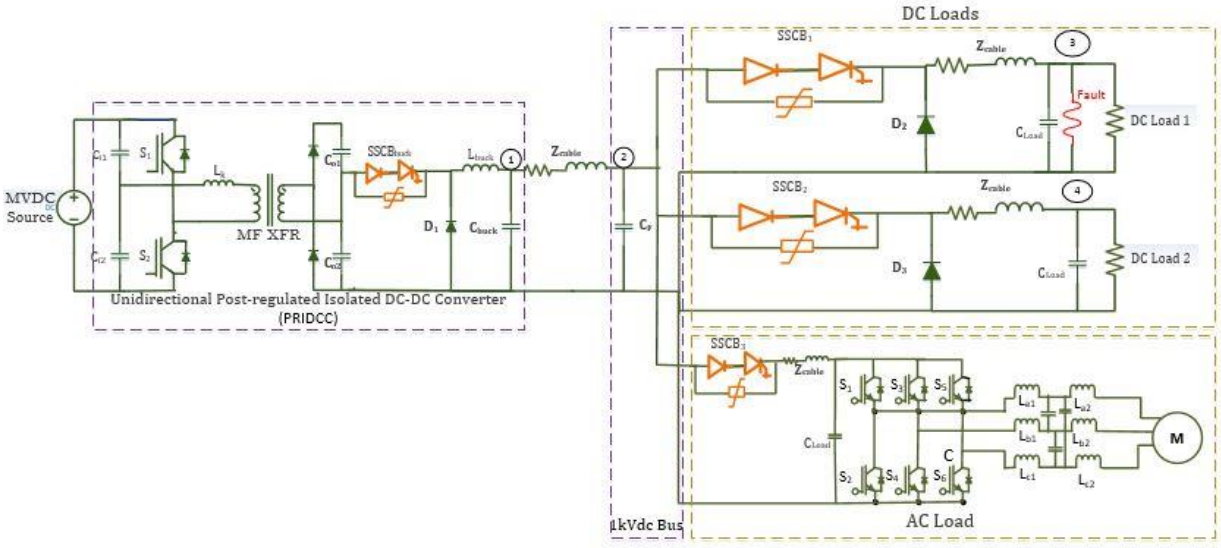


Fig. 2.1. Circuit diagram of a post-regulated isolated dc-dc converter powering a simplified 1kVdc zone

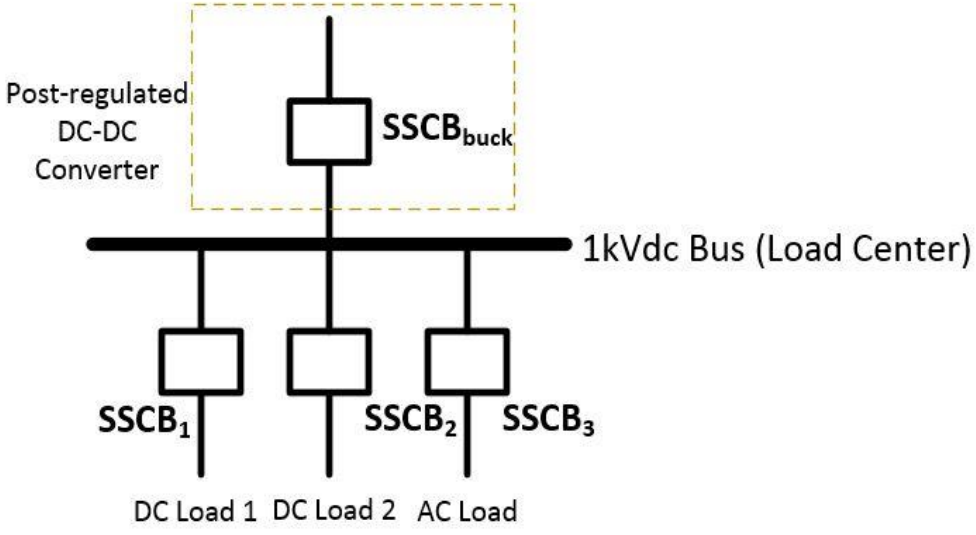


Fig. 2.2. Single-bus single-breaker configuration for 1kVdc zone

Table 2.1: 1-kVdc load center parameters

Parameters	Values	
Rated Total Power	7.5 MW	
Rated DC Load Power	2x3.25 MW	
Rated AC Load Power	1 MW	
DC Bus Voltage	1 kV	
Buck SSCB Rating	7.5 kA	
Buck SSCB Short-Circuit Threshold	15 kA	
Cable Resistance (1kV Sivacon busduct, 3.7 kA)	30 μΩ/m	
Cable Inductance (1kV Sivacon busduct, 3.7 kA)	0.07 μH/m	
Buck Converter to DC Load Center Bus Distance	100 m	
DC Load Center Bus to DC Load Distance	50 m	
LCL Filter (AC load)	L_1	235 μH/ph
	C_1	278 μF/ph
	L_2	52 μH/ph

regulating the 1kVdc output voltage. In the simulations, the SST is modeled as a simplified two-level system. The SST practical implementation would require multiple modules connected in series on the primary side and in parallel on the secondary side [1]. The use of SST is a favorable solution for microgrid systems because it provides suitable voltage conversion with galvanic isolation, controllability and high power density (i.e., lower volume and weight) [1][2].

2.2.2 *DC Loads*: There are two dc loads equally rated at 3.25 MW and protected by SSCBs and load-side freewheeling diodes providing current continuity due to load-side inductances when the load SSCB opens. A filter capacitor has been included at the load center 1-kVdc bus to provide bus voltage support during FCL operations, and its influence on short-circuit current levels will be analyzed in Chapter 4.

2.2.3 *AC Load*: There is also an ac load rated at 1 MW that represents a three-phase electric motor load fed by a three-phase inverter with an output LCL filter. The dc input side is protected by a SSCB.

2.2.4 DC Cables: The considered cable inductances have lengths of 100 m from the post-regulated buck converter to the load center 1kVdc bus (nodes 1-2) powering the dc load centers, and 50 m to each of the dc loads (nodes 2-3 and 2-4). The impact of electromechanical and solid-state circuit breaker operation on dc conductor sizing will be discussed in chapter 4.

2.3 System Simulations

MATLAB/Simulink™ was selected as the software package for modeling the simple 1-kVdc distribution system since it is the software package widely used for this type of analyses. A time step of 10 ns has been used in every simulation performed in MATLAB/Simulink™ to obtain results with high accuracy.

Figure 2.3 displays the steady-state current waveforms at the 1-kVdc load center bus, "DC Load 1", "DC Load 2" and input dc current to AC Load under rated conditions. Each of the dc loads are carrying 3.25 kA and the ac load is drawing 1 kA.

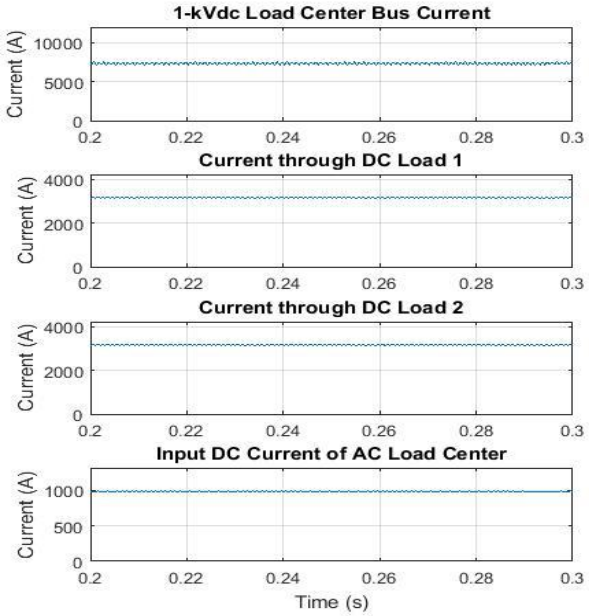


Fig. 2.3. Current waveforms at the 1-kVdc load center bus, DC Load 1, DC Load 2 and AC Load Center input under rated steady-state conditions

2.4 Modeling of SSCB

This section briefly summarizes different semiconductor devices targeted for SSCB. An RB-IGCT was selected by ABB as the solid-state switching waveforms are described next.

2.4.1 Commonly Used Semiconductors for SSCBs

The SSCB should meet protection requirements for dc microgrids due to availability of semiconductor devices capable of interrupting high fault currents within microseconds and switching under 1 kHz for fault-current-limiting applications. Semiconductor devices usually used are: silicon controlled rectifiers or thyristors, insulated-gate bipolar transistors (IGBTs), integrated gate-commutated thyristors (IGCTs), and gate turn-off thyristors (GTO). Wide-band-gap (WBG) devices (i.e., mainly SiC or GaN devices) are the latest ones added to SSCB applications. Thyristors are semi-controlled devices so they are mainly useful for AC circuit breakers since they require a zero-crossing of the current to turn naturally off [4]. They require auxiliary circuits to turn them off immediately at currents different from zero. Among the controlled devices, the RB-IGCT displays a lower on-state voltage drop compared to similarly rated commercial IGBT. For example, the ABB IGBT (5SNA 1500E250300), rated at 2.5-kV/1.5-kA, displays an on-state voltage drop of 2.5 V [7]. A similarly-rated RB-IGCT displays an on-state voltage drop of 1.25 V; approximately, half of the IGBT voltage drop. So, the RB-IGCT was selected by ABB as the solid-state switch in the SSCB because of its extremely low conduction losses and the “thyristor” high turn-off current capability [3]. The RB-IGCT is able to block voltages in both forward and reverse diretions, while only carrying current in the forward direction.

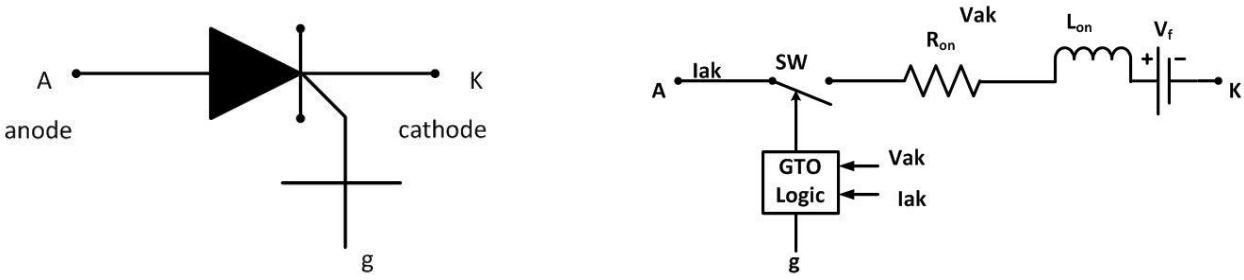
2.4.2 Development of the IGCT

IGCTs were introduced in the semiconductor device industry in mid 1990s as an enhancement to GTOs, with an improved low-inductance drive circuit, monolithically integrated diodes and a simplified power circuit [3]. Essentially, IGCTs are semiconductor devices having GTO structure and an integrated gate-drive unit. Initially, IGCTs were supposed to be used in applications such as medium-voltage drives, STATCOMs, wind energy conversion systems, etc. However, IGCTs are gaining ground as the semiconductor device of choice due to recent trends of increased usage of semiconductor devices in high-power applications with expected low conduction losses and ability to have hard-switching functionality in low operating frequencies.

2.4.3 Modeling of an RB-IGCT as Solid-State Switch in a SSCB

The development of the RB-IGCT model in Matlab/Simulink^{TM} and resulting switching waveforms are described in this section. An IGCT block is not available in "SimPowerSystems" library of Matlab/Simulink^{TM}. Thus, based on the similarities between GTOs and IGCTs as discussed above, the RB-IGCT was modeled using (1) a GTO block with a diode in series, (2) a shunt impedance in parallel with the GTO block, and (3) an inductor in series as a clamp to match the critical rate of rise of current during the device turn on.

The GTO thyristor block in Simulink^{TM} is modeled as a series connection of a resistor Ron, an inductor Lon, and a DC voltage source V_f, and an ideal switch, as shown in Fig. 2-4 [5]. The control of the switch is obtained by a logic signal based on the voltage V_{ak}, the current I_{ak}, .the gate signal g. The typical turnoff characteristic is built into the model consisting of two segments. Upon the gate signal switched to 0, the first decrease of current I_{ak} is from I_{max} to $I_{max}/10$, within the fall time t_f. In the second segment, current decreases then from $I_{max}/10$ to 0



(a) (b)

Fig. 2.4 . GTO model in Simulink^{TM}: (a) symbol (b) equivalent circuit

within the tail time T_t. The turn-off is achieved when the current I_{ak} reaches 0. The latching and holding currents are ignored in the model.

The simplified Matlab/Simulink^{TM} model of RB-IGCT incorporated in Fig. 2.5 is used to evaluate the RB-IGCT switching characteristics. Only the turn-off waveforms will be shown, as the model does not allow to model the turn-on properties of the switch. The R_Load corresponds to a dc load rated 3.25 MW and powered by a 1kV dc source, which is equal to 307 mΩ. The R_s and L_s components correspond to line resistance of 1.5 mΩ and inductance of 3.5 μH, respectively, for a distance of 50 m from the source to the load, based on the values provided in Table 2.1. An MOV is connected across the RB-IGCT-diode series branch to protect the IGCT against transient overvoltages during turn-off.

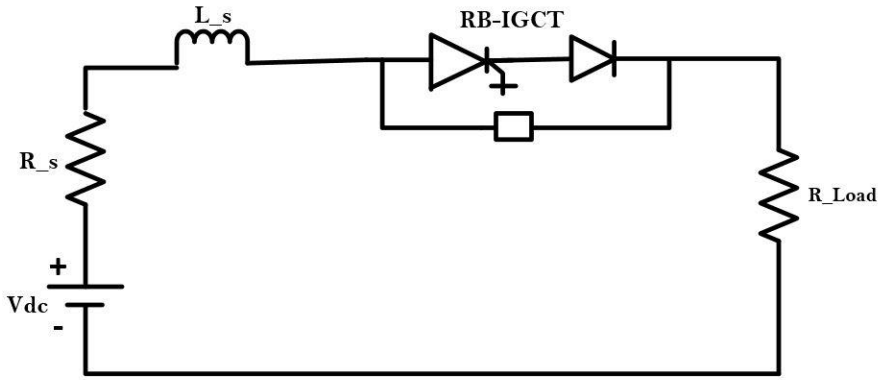


Fig. 2.5. Circuit-based modeling of the RB-IGCT

From the datasheet of the ABB 5SHZ 11H6500 6.5kV IGCT, the minimum inductance to keep the rate of the current rise below the critical value is calculated as follows [6]:

$$L_{min} = \frac{V_{dc}}{\frac{di_{cr}}{dt}} = 1\ \mu H$$

$$where, V_{dc} = 1000\ V, \frac{di_{cr}}{dt} = 1000\ A/\mu s$$

As the circuit inductance is above the minimum required inductance during IGCT turn-on, no additional inductance was required.

The resulting model parameters are given in Table 2.2.

2.4.4 Switching Characteristics

Figure 2-6 illustrates the turn-off waveforms for a single RB-IGCT rated at 1.5 kA. The total current fall time is approximately 40 μs which compares very well with the values obtained from experimental results in [3]. The MOV was not required to operate as the turn-off voltage overshoot of about 1.6 kV was well within the device breakdown voltage. The turn-off waveforms illustrate the hard switching turn-off capability.

Table 2.2: Device Parameters Used for Loss Calculations for Determining RB-IGCT's Thermal Requirements

Parameters	Values
Threshold voltage, V_T	1.1 V
Device resistance, r_T	0.1 mΩ
Average on-state current, $I_{T(AV)M}$	1.5 kA
Maximum controllable turn-off current, I_{TGQM}	3 kA
Junction-to-case thermal resistance, $R_{th(j-c)}$	8.5 K/kW
Maximum allowable junction temperature, T_{vjmax}	125 ℃

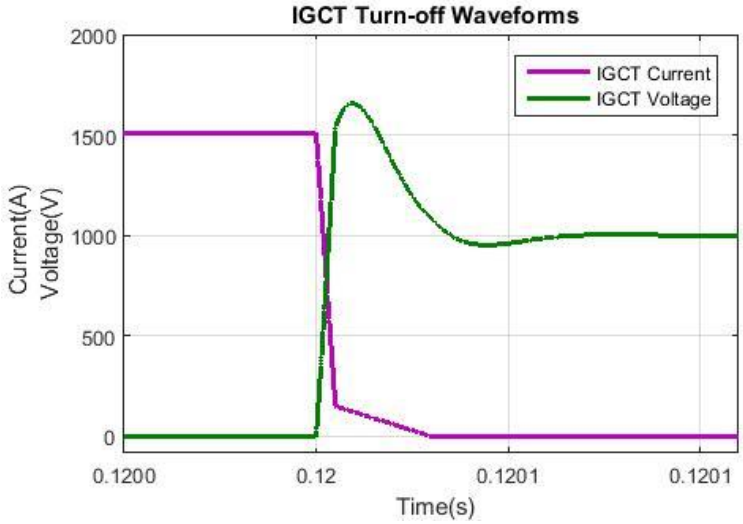


Fig. 2-6. RB-IGCT turn-off waveforms

2.5 Summary

The following activities were performed in this chapter:

- Description of a notional low-voltage dc distribution system along with relevant system parameters
- Development of RB-IGCT model in MATLAB/Simulink™
- Explanation of switching characteristics of RB-IGCT implemented in an SSCB

The following chapter will concentrate on a detailed implementation of a fault-current-limiting algorithm for short-circuit protection of the notional low-voltage dc distribution system described in this chapter.

2.6 References

[1] X. She, A. Q. Huang and R. Burgos, "Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 186-198, Sept. 2013.

[2] T. Besselmann, A. Mester and D. Dujic, "Power Electronic Traction Transformer: Efficiency Improvements Under Light-Load Conditions," in *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3971-3981, Aug. 2014.

[3] Vemulapati, U., Arnold, M., Rahimo, M., Antoniazzi, A. and Pessina, D. "Reverse blocking IGCT optimised for 1 kV DC bi-directional solid state circuit breaker," in *Power Electronics, IET* , vol.8, no.12, pp. 2308-2314, 2015.

[4] C. Meyer, M. Hoing and R. W. De Doncker, "Novel solid-state circuit breaker based on active thyristor topologies," *Power Electronics Specialists Conference*, (PESC), *2004 IEEE 35th Annual*, pp. 2559-2564, Vol.4.

[5] Mathworks, "GTO". Available online at: http://www.mathworks.com/help/physmod/sps/powersys/ref/gto.html?requestedDomain=www.mathworks.com

[6] ABB, "Reverse Blocking Integrated Gate-Commutated Thyristor 5SHZ 11H6500'. Available online at: https://library.e.abb.com/public/7f2b388387f8cef1c1257dea0043b854/5SHZ%2011H6500_5SYA1254-01%20Dec%2014.pdf

[7] ABB, "HiPak IGBT Module 5SNA 1500E250300'. Available online at: https://library.e.abb.com/public/7f2b388387f8cef1c1257dea0043b854/5SHZ%2011H6500_5SYA1254-01%20Dec%2014.pdf

CHAPTER 3

SHORT-CIRCUIT PROTECTION METHODOLOGY INCORPORATING A FAULT-CURRENT-LIMITING FUNCTION

3.1 Introduction

The main objective of a short-circuit protection methodology is to isolate faults as fast as possible to minimize safety hazards while limiting the affected area. This refers to achieving proper coordination among cascaded protection devices by adequate selection of the threshold values corresponding to the used fault-detection technique (e.g., overcurrent) [1-4]. In dc distribution systems, the short-circuit analysis is cumbersome because of the presence of power converters having their own short-circuit protection, and inrush currents of filter dc capacitors that may lead to nuisance tripping, making the choice of thresholds at different locations of the network problematic.

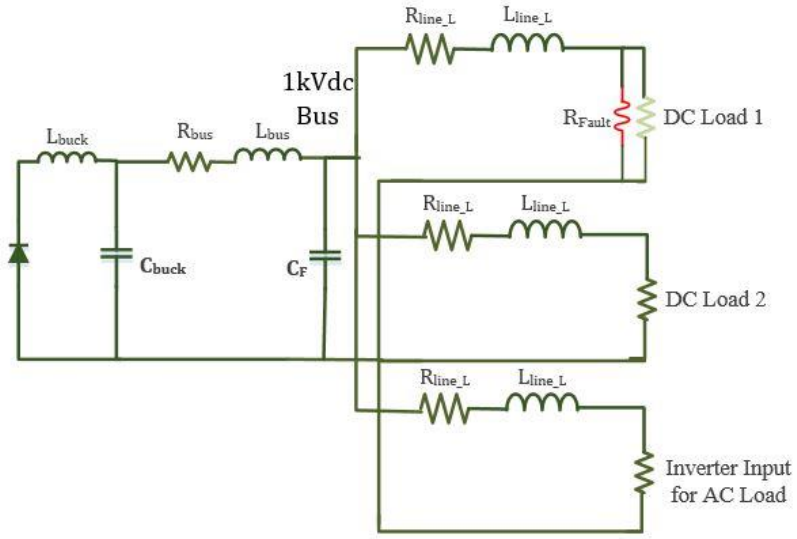
All solid-state circuit breakers (SSCB) employed in the previously mentioned low-voltage distribution system are equipped with overcurrent control circuits, which are activated upon the (fault) current reaching a set threshold value that depends on the supplied dc load. Generally, a downstream SSCB has lower threshold values than an upstream SSCB. In other words, the bus SSCB or the buck converter switch acting as SSCB has a higher threshold value than a load SSCB. Similar protection strategies for dc distribution systems have been discussed in literature [2]. Implementing a fault-current-limiting (FCL) function is of interest when the system is subjected to temporary faults to allow returning to normal operation once the fault disappears. For the execution of FCL function, a control circuit for overcurrent protection is presented in this chapter, along with the simulation results demonstrating a faulted dc load SSCB under FCL operation [3].

This chapter is organized as follows: the typical fault behavior of the notional low-voltage dc distribution systems will be evaluated along with analytical expressions, followed by a description of the proposed fault-current-limiting algorithm to maintain a specified level of short-circuit current, and an analysis demonstrating effective coordination obtained by applying the FCL algorithm at different operating conditions of the system.

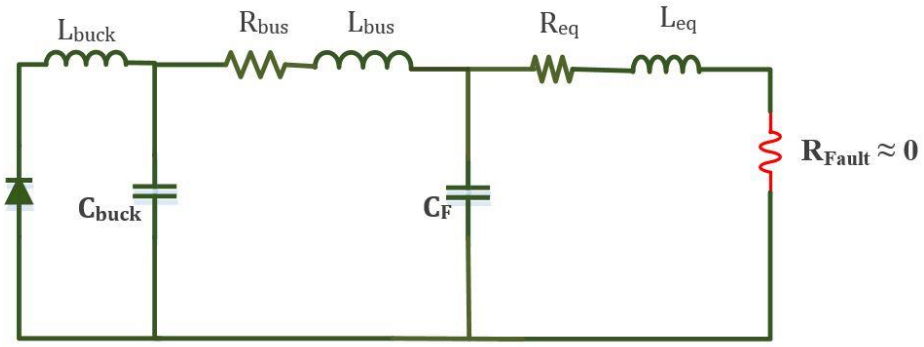
3.2 Fault Behavior of Notional Low-Voltage DC Distribution System

In a compact power converter-based dc distribution system, the charged output filter capacitors behave as high fault-current contributing sources. The fault behavior of the discharging capacitor is analogous to the natural response of an RLC circuit, where the resistance and inductance correspond to the low line impedances due to short distances. The response can be analyzed by means of the solution of second-order differential equations with an appropriately assumed initial capacitor voltage and inductor current.

The equivalent circuit of the 1-kVdc load center for a pole-to-pole fault at “DC Load 1” is presented in Fig. 3.1. Figure 3.2 shows simulation results to illustrate the fault-current contributions from the buck and energy-storage capacitors at the 1-kVdc load center in the notional low-voltage distribution system, provided in Section 2.2 of Chapter 2. Considering a pole-to-pole fault at DC Load 1, the current waveforms through equivalent faulted branch is dominated by the discharges from the buck and energy-storage capacitors, followed by the free-wheeling action performed by the buck converter diode. The buck capacitor current reaches a peak of about 32.5 kA, while the energy-storage capacitor current at the 1-kVdc load center reaches a peak of about 48 kA. Thus, the combined peak fault-current during the pole-to-pole fault reaches a magnitude of about 82 kA without the operation of any protection equipment. It is evident that a fault response of this magnitude can be potentially damaging to the active



(a)



(b)

Fig. 3.1. (a) Circuit schematic1-kVdc load center during a pole-to-pole fault at "DC Load 1", (b) equivalent circuit during the fault

components of the system, including semiconductor switches and capacitors themselves. For example, the combined peak fault current of 82 kA is about 26 times higher than the rated dc load current of 3.25 kA. Thus, the SSCB would require 26 times more devices in parallel if a dc load is faulted and the fault current is to be interrupted at the peak value. Similar over-dimensioning of the other system components based on the fault responses would result in added weight, volume and cost, affecting the expected compactness of the dc distribution system in applications such as onboard electrical systems in all-electric ships, more electric aircrafts etc.

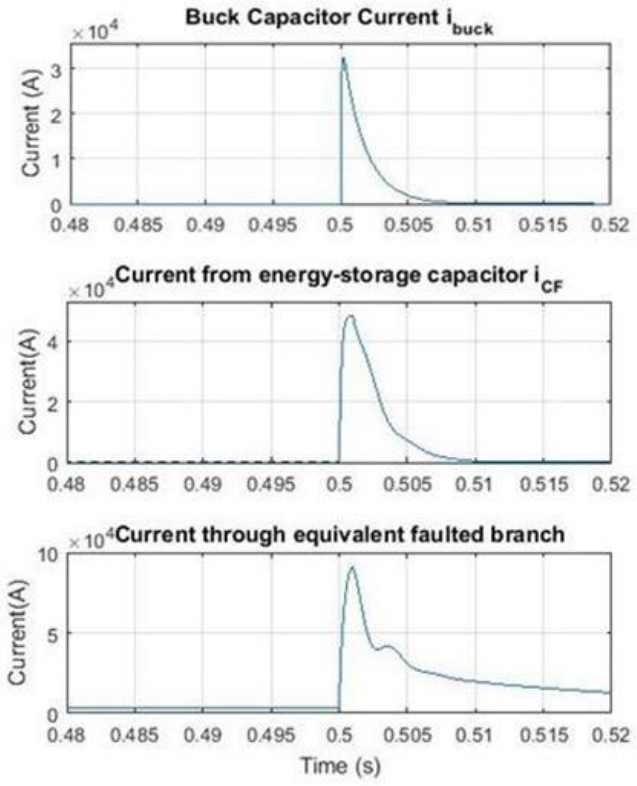


Fig. 3.2. Fault-current contributions from the buck and energy-storage capacitor for a pole-to-pole fault at DC Load 1 (without short-circuit protection at the 1-kVdc load center)

The distribution system presented in Fig. 2.1 of Chapter 2, will be used to derive the expressions. The state equations based on the two capacitor voltages and two inductor currents from Fig. 3.1(b) are written below:

$$i_{Lbus} = C_{buck}\frac{dV_{Cbuck}}{dt}$$

$$\frac{dV_{Cbuck}}{dt} = \frac{i_{Lbus}}{C_{buck}} \qquad (1)$$

$$i_{Lbus}R_{bus} + L_{bus}\frac{di_{Lbus}}{dt} = V_{Cbuck} - V_{CF}$$

$$\frac{\mathrm{di_{Lbus}}}{\mathrm{dt}} = \frac{\mathrm{V_{Cbuck} - V_{CF} - i_{Lbus}R_{bus}}}{\mathrm{L_{bus}}} \qquad (2)$$

$$i_{Lbus} + C_F\frac{dV_{CF}}{dt} = i_{Leq}$$

$$\frac{dV_{CF}}{dt} = \frac{i_{Leq} - i_{Lbus}}{C_F} \tag{3}$$

$$i_{Leq}R_{eq} + L_{eq}\frac{di_{Leq}}{dt} = V_{CF}$$

$$\frac{di_{Leq}}{dt} = \frac{V_{CF} - i_{Leq}R_{eq}}{L_{eq}} \tag{4}$$

The solution of this system of differential equations in the s-domain has been performed in MATLAB™, and the details are provided in the Appendix A. The expression for the current through the faulted branch can be written as follows:

$$i_{Leq}(t) = \sum_{k=1}^{4} \frac{e^{f(t)t}}{4f(t)^3 + 3\mathrm{L_{eq}}f(t)^2 - 2(\mathrm{C_F L_{bus}} - \mathrm{C_{buck} L_{bus}})f(t) - \mathrm{C_F R_{eq}} - \mathrm{C_F L_{bus} L_{eq}} + \mathrm{C_{buck} L_{bus} L_{eq}}}$$

where, f(t)

$$= \sqrt[k]{\mathrm{t^4} + \mathrm{L_{eq}t^3} - (\mathrm{C_F L_{bus}} - \mathrm{C_{buck} L_{bus}})\mathrm{t^2} + \left(\mathrm{C_{buck} L_{bus} L_{eq}} - \mathrm{C_F L_{bus} L_{eq}} - \mathrm{C_F R_{eq}}\right)t - \mathrm{C_F C_{buck} L_{bus} R_{eq}}}$$

k=1,2,3,4

Considering only the effect of voltage from C_{buck}, the expression of for the fault current contributed by C_{buck} current in the underdamped second-order RLC circuit is solved, and the following expression has been derived:

Applying KVL (ignoring C_F) in Fig. 3.1 (b),

$$L_{bus}\frac{di_1(t)}{dt} + i_1(t)R_{bus} + \frac{1}{C_{buck}}\int i_1(t)dt = V_{buck0} \tag{5}$$

Converting to s-domain and dividing both sides by L_{bus},

$$[sI_1(s) - I_{10}] + I_1(s)\frac{R_{bus}}{L_{bus}} + \frac{I_1(s)}{sL_{bus}C_{buck}} = \frac{V_{Cbuck0}}{sL_{bus}}$$

$$I_1(s) = \frac{\frac{V_{Cbuck0}}{sL_{eq1}} + I_{10}}{s + \frac{R_{bus}}{L_{bus}} + \frac{1}{sL_{eq1}C_F}} = \frac{\frac{V_{Cbuck0}}{L_{bus}} + sI_{10}}{s^2 + \frac{R_{bus}}{L_{bus}}s + \frac{1}{L_{bus}C_{buck}}} \tag{6}$$

Solving and transforming (6) in time domain,

$$i_1(t) = e^{-\alpha_1 t}[i_1(0)\cos\omega_{r1}t + \left(\frac{V_{Cbuck0}}{\omega_{r1}L_{bus}} + \frac{\alpha_1 i_1(0)}{\omega_{r1}}\right)\sin\omega_{r1}t]$$

Where, damping factor, $\alpha_1 = \frac{R_{bus}}{2L_{bus}}$

Resonant frequency, $\omega_{01} = \frac{1}{\sqrt{L_{bus}C_{buck}}}$

Ringing frequency, $\omega_{r1} = \sqrt{{\omega_{01}}^2 - {\alpha_1}^2}$

3.3 Proposed FCL Control Circuit for Overcurrent Protection

A control schematic for the SSCB providing short-circuit protection and implementing the FCL function in MATLAB/Simulink™ is proposed in Fig. 3.3. Figure 3.3 (a) displays the block diagram of the control circuit while 3.3(b) details the MATLAB/Simulink™

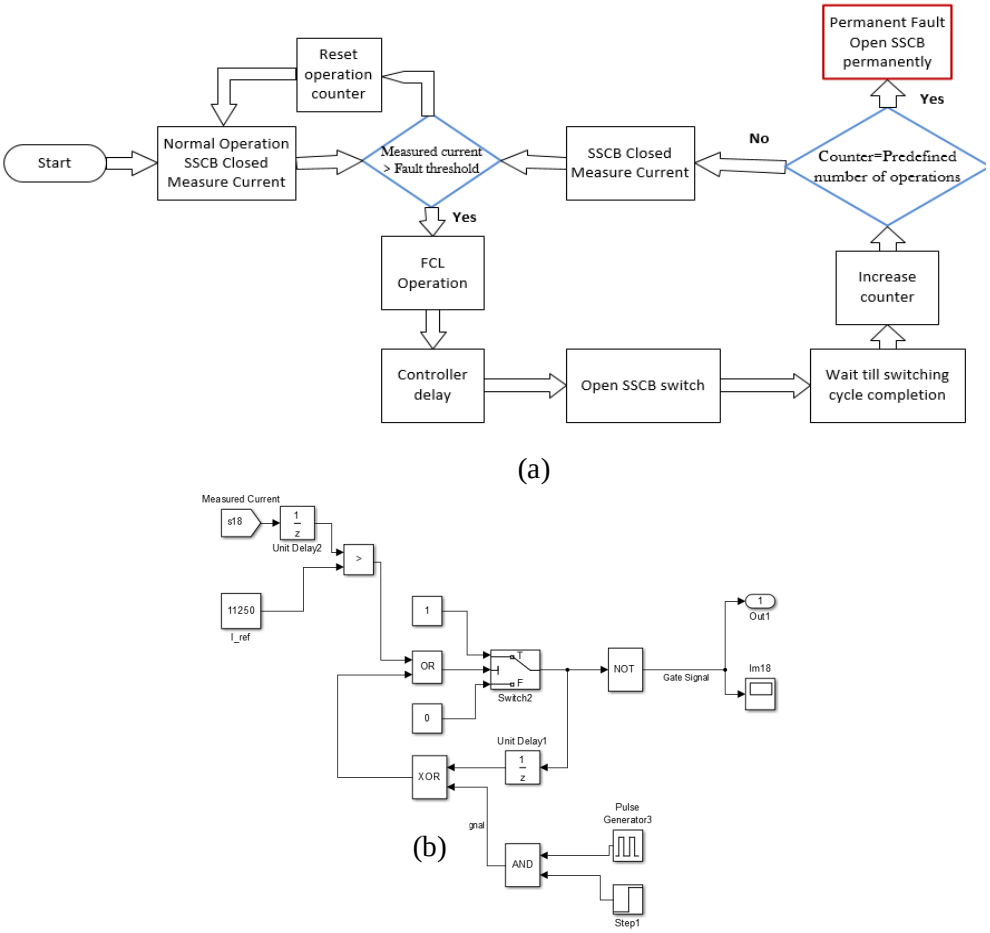
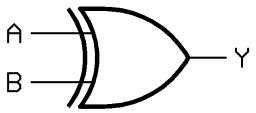


Fig. 3.3. Fault-current control circuit implementing FCL function (a) block diagram (b) Simulink representation



(a)

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

(b)

Fig. 3.4. XOR Gate: (a) structure (b) truth table

implementation. The "Switch" block sends the output which is inverted and transmitted to the gate of the SSCB. The output of the block is "1" when the input of the block is a "0" from the output of the "OR" gate. The condition for "0" is when the measured current is higher than the overcurrent threshold.

An XOR gate is used to provide the FCL mode activation signal. The output of the XOR gate is '0' when two inputs are same. Before the fault, both the detection signal and the output of switch are "0". The output of the XOR gate is '0' when two inputs are same (please, refer to Fig. 3.4 for completeness). At the application of the fault and the measured current crossing the overcurrent threshold, the "fault detection signal" provides a latched value of "1", hence, detecting the fault and making the output of XOR "1". The switch output is now "1" and the gate signal "0". To repeat this action at a rate of 1 kHz, the latched "Comparator" output block is passed through an "AND" gate with the other input being a pulse generator, so that the fault detection and consequent interruption of gate signal is repeated every 1 ms. The switching frequency under FCL operation would mainly depend on the thermal capability of the power devices; this is analyzed in Chapter 4.

3.4 Fault Analysis under FCL Operation Integrated with Controller Delays

Delays are inevitable in practical circuits due to the current sensors, analog-to-digital converters, digital signal processors and semiconductor device switching delays. The SSCB total delay has been approximated as 40 μs after evaluating several references [4-6].

Considering a positive-to-negative-pole fault at "DC Load 1" at t = 0.5 s, the current and voltage waveforms in the main "1-kVdc bus", "DC Load 1" and "DC Load 2" are illustrated in Figs. 3-5 and 3-6, respectively. The bus steady-state current before the fault is applied is 7.5 kA and there are no energy-storage capacitors at the load. The control circuit described above is activated and the SSCB protecting "DC Load 1" enters into the FCL mode while the other loads continue operating at their rated values. Most of the fault current is contributed by the energy-storage capacitor at the "1-kVdc bus" so the "DC Load 2" and "AC Load" experience minimal oscillations with the current transients diminishing within 0.15 s. The current ripple in the faulted

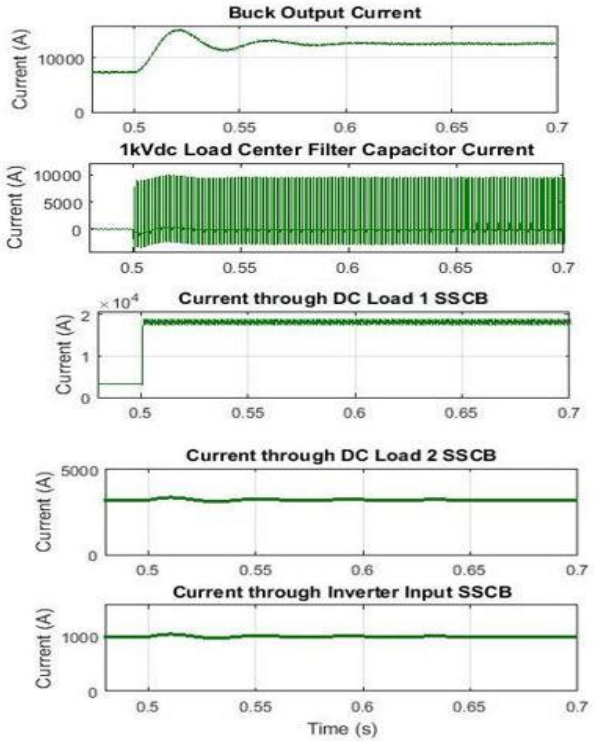


Fig. 3.5. Current waveforms at the buck converter output, 1-kVdc load center filter capacitor, DC Load 1, DC Load 2, AC Load for a pole-to-pole fault at "DC Load 1" at t = 0.5 s

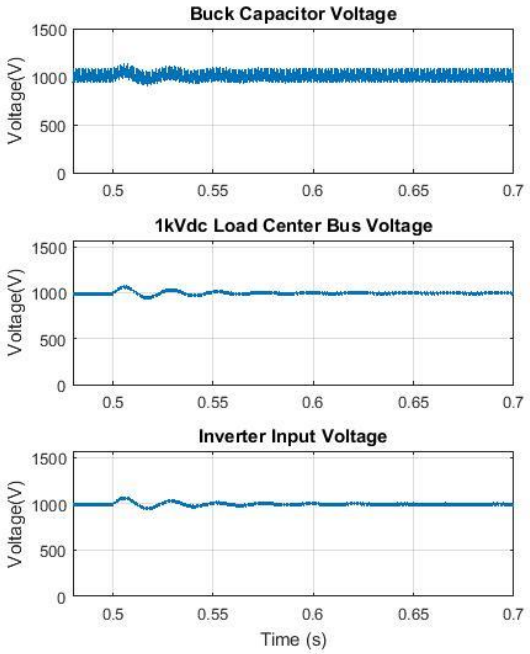


Fig. 3.6. Voltage waveforms at the buck converter output, load center and ac load buses for a pole-to-pole fault at "DC Load 1" at t = 0.5 s

load results from the SSCB opening upon the current reaching approximately 18.78 kA followed by freewheeling of the inductor current until the next switching cycle starts. Many cycles are illustrated to show the positive effect of the SSCB equipped with the FCL function. It is not anticipated that the faulted load SSCB will operate for these many cycles since the protection scheme should open the SSCB to isolate the fault after few cycles determined through a coordination analysis of the entire system.

As discussed above, the FCL function is implemented including a controller delay of 40 µs. The relevant calculations are shown below:

Line inductance from 1-kVdc bus to a dc load:

$$L_{line} = 50 \text{ m x } 0.065 \text{ µH/m} = 3.25 \text{ µH}$$

So, the approximated rise rate of the current becomes:

$$\frac{di}{dt} = \frac{V_{dc}}{L_{line}} = \frac{1000}{3.25\ \mu} = 307\ A/\mu s$$

For a 40-μs controller delay after a fault at "DC Load 1" at t = 0.5 s, the trip fault current can be approximated by:

$$I_{fault,peak} = 6.5k + 307x40 = 18.78\ kA$$

Under steady-state conditions, the voltage ripple at the output capacitor of the buck converter is 10 % or 100 V and the voltage ripple at the 1-kVdc load center bus is 1 %, or 10 V. The voltage initial transient after the fault is applied at t = 0.5 s reaches a maximum value of 5% or 50 V and diminishes to reach the steady-state value within 0.1 s. The MOV connected in parallel to the "diode/RB-IGCT" series branch in the SSCB protecting "DC Load 1" does not operate because of minimal overvoltage during device turn off under the FCL mode resulting from the distributed capacitance across the system in Fig. 2.1, in particular, at the 1-kVdc bus, providing a comparatively stiff bus voltage.

3.5 Fault Analysis without Energy-Storage Capacitor at 1-kVdc Load-Center Bus

The energy-storage capacitor at the 1-kVdc bus was removed so the buck capacitor served as the only capacitive storage upstream (load-center) from the fault. Each of the loads has now an energy-storage capacitor for voltage regulation and ride-through capabilities. Load capacitors were selected based on 1%, 5% and 10% voltage ripple. Detailed calculations are shown in Appendix A.

Table 3.1 shows impact of controller delays on the peak fault current where the dc loads have capacitors selected for 1% voltage ripple, where the dc loads have capacitors selected for 1% voltage ripple and there is no energy-storage capacitors at the 1-kVdc load-center bus. As

Table 3.1: Impact of controller delays and capacitive discharge on the peak fault current and $i^2t(t)$ for the "DC Load 1" SSCB

Controller Delay	SSCB Current (kA)	Minimum Number of SSCB Parallel Devices	$[i^2(t)t]$ for Load SSCB Current Over 10 ms (A^2s)
0 μs	6.250	3	$3.65x10^6$
7 μs	8.400	3	$3.72x10^6$
25 μs	13.925	5	$3.8x10^6$
40 μs	18.780	7	$3.92x10^6$

anticipated, the required number of power devices in parallel to sustain the higher currents increased; it doubled for this particular case.

The impact of the removal of the energy-storage capacitor is discussed below:

3.5.1 Impact on the load center bus current: Figure 3.7 illustrates current waveforms for at the buck converter output, DC Load 1, DC Load 2, AC Load for a pole-to-pole fault at t = 0.5 s with the energy-storage capacitor removed. The peak current reached now is about 8.5 kA, which is less than half of the previously observed peak fault current of 18.78 kA contributed by the energy-storage filter capacitor at the 1-kVdc bus. Thus, the removal of energy-storage capacitor resulted in a reduction of the steady-state upstream current during a fault.

3.5.2 Impact on voltage at different locations: Figures 3.8, 3.9 and 3.10 illustrate voltage waveforms at the buck converter output, dc load and ac load buses for load capacitors selected for 10%, 5% and 1% voltage ripple, respectively. Corresponding peak voltage swings are 8.2%, 4.5% and 2.3%; decreasing as expected when load capacitance increases. These voltage swings are higher compared to the system having the energy-storage capacitor at the 1-kVdc bus and no capacitors across the loads. Thus, there is

need for a trade-off while choosing the location of the energy-storage capacitors to yield acceptable voltage oscillations during short-circuit conditions.

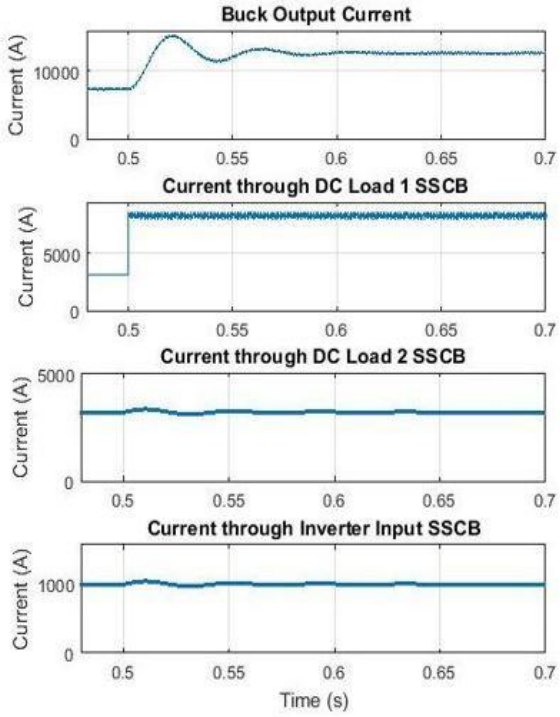


Fig. 3.7. Current waveforms at the buck converter output, DC Load 1, DC Load 2, AC Load for a pole-to-pole fault at "DC Load 1" at t = 0.5 s (energy-storage capacitor at load-center bus removed)

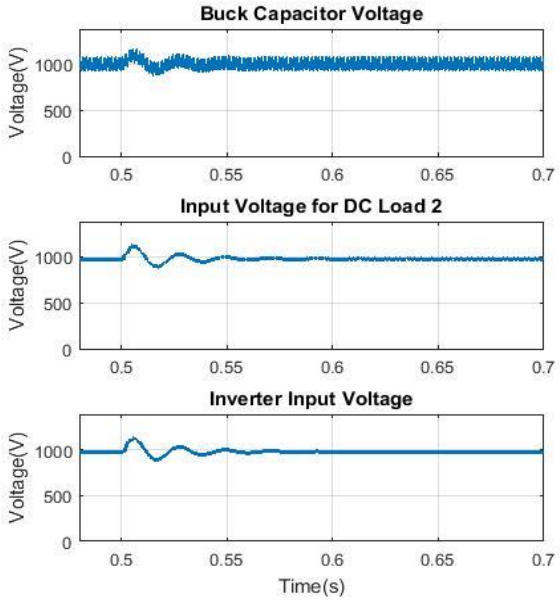


Fig. 3.8. Voltage waveforms at the buck converter output, dc load and ac load buses for a pole-to-pole fault at "DC Load 1" at t = 0.5 s; load capacitors sized for 10% voltage ripple

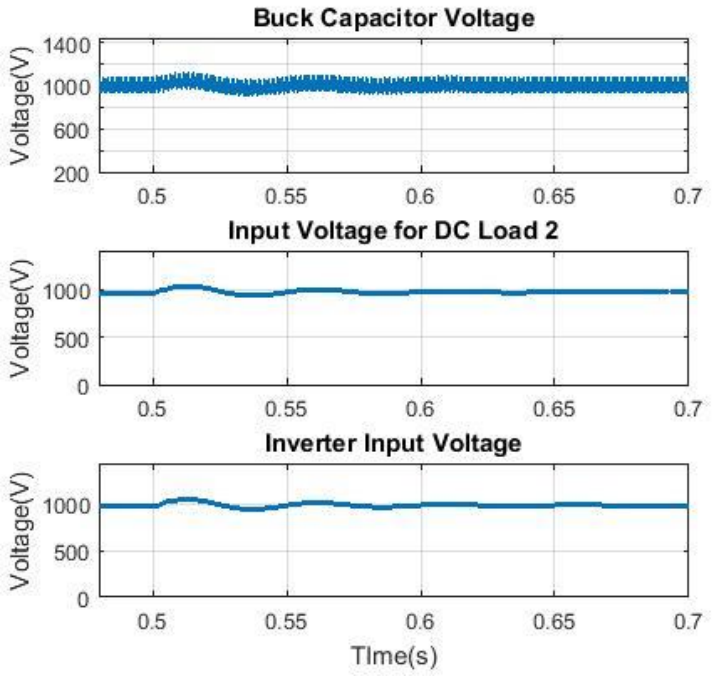


Fig. 3.9. Voltage waveforms at the buck converter output, load center and ac load buses for a pole-to-pole fault at “DC Load 1” at t = 0.5 s; load capacitors sized for 5% voltage ripple

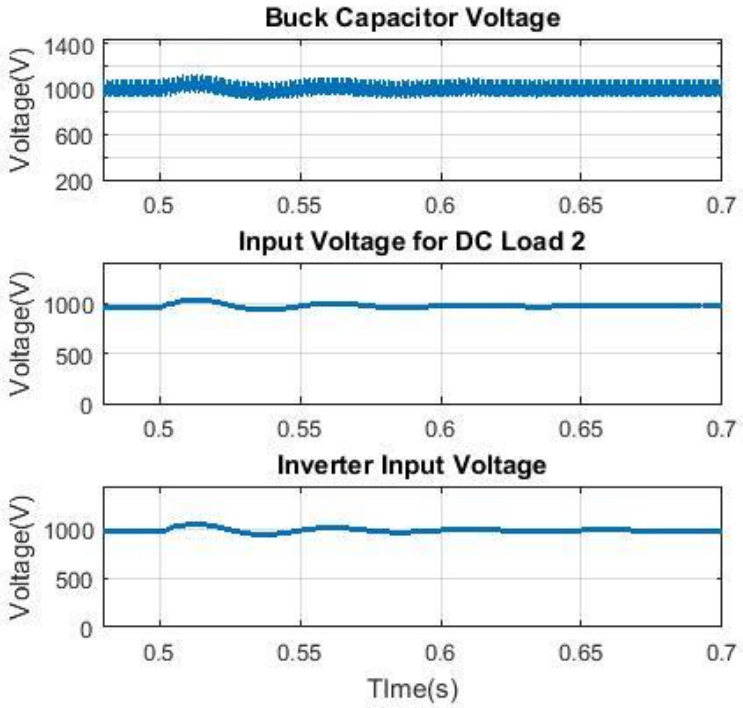


Fig. 3.10. Voltage waveforms at the buck converter output, dc load and ac load buses for a pole-to-pole fault at “DC Load 1” at t = 0.5 s; load capacitors sized for 5% voltage ripple

3.6 Coordination between Upstream and Downstream SSCBs during FCL Operation

The coordination between upstream and downstream devices during FCL operation will be considered in this section by analyzing two cases of variable load conditions. A pole-to-pole fault is applied at t = 0.5 s at "DC Load 1" in both cases.

Case 1: "DC load 1" and "DC Load 2" operate at 80% and 20%, respectively, and ac load operates at 100% rated power:

$$\text{Current through DC Load 1, } I_{Load1} = \frac{3.25\text{Mx}0.8}{1000} = 2.6 \text{ kA}$$

$$\text{Current through DC Load 2, } I_{Load2} = \frac{3.25\text{Mx}0.2}{1000} = 650 \text{ A}$$

$$\text{Current at the AC Load Center input, } I_{Load,AC} = \frac{1\text{M}}{1000} = 1.0 \text{ kA}$$

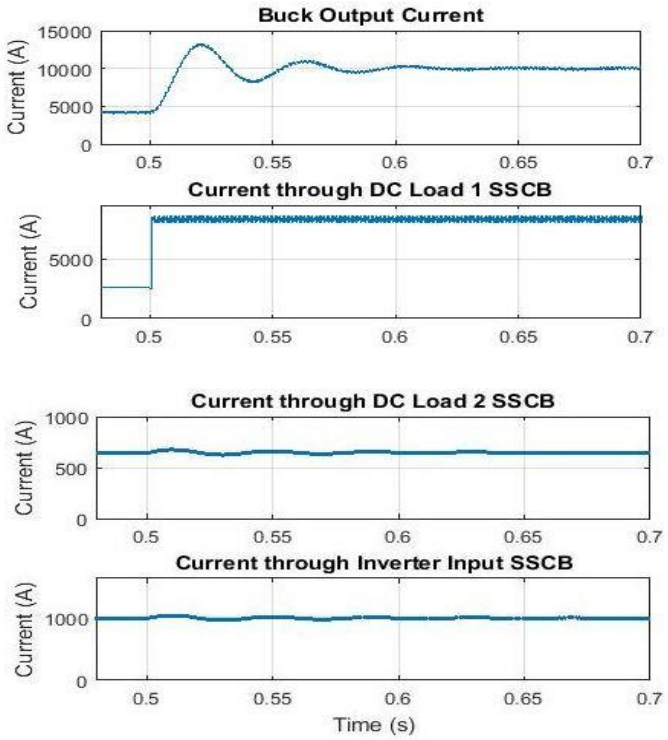


Fig. 3.11. Current waveforms at the buck converter output, DC Load 1, DC Load 2, AC Load for a pole-to-pole fault at "DC Load 1" at t = 0.5 s (case 1)

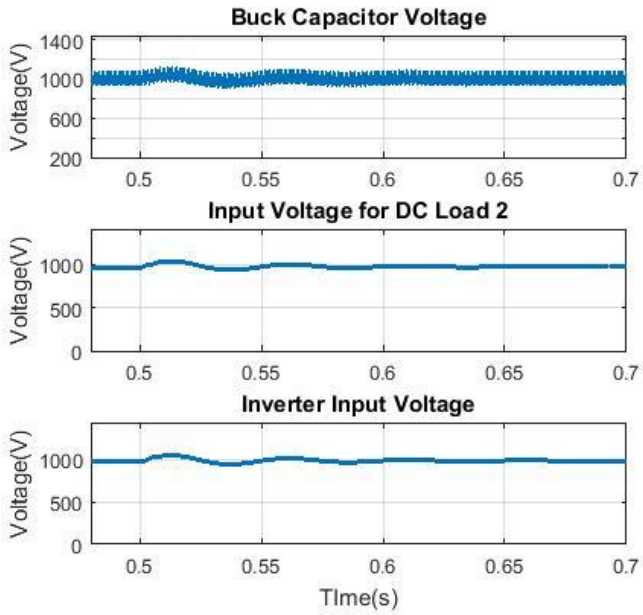


Fig. 3.12. Voltage waveforms at the buck converter output, dc load and ac load buses for a pole-to-pole fault at "DC Load 1" at t = 0.5 s (case 1)

The FCL operation has a similar effect as the case where all loads are running at rated power. The waveforms for this case are provided in Figs. 3.11 and 3.12 with the 1-kVdc bus filter capacitor removed with load capacitors in place. The buck converter output current reaches a value of 10.15 kA from the steady-state value of 4.25 kA, with the current through "DC Load 1" SSCB reaches a value of about 8.5 kA. The current drawn by unfaulted "DC Load 2" and "AC load" currents remain the same as calculated above. The unfaulted load currents show minimal oscillations pertaining to the transient in bus capacitor voltages; so these load operations are not hampered as the transients diminishes within 0.2 s continuing steady-state operation. The upstream SSCB also remains unperturbed.

Case 2: "DC load 1" and "DC Load 2" operate at 50% each, and ac load operates at 100% rated power:

$$\text{Current through each dc load}, I_{Load,dc} = \frac{3.25\text{Mx}0.2}{1000} = 1.625 \text{ kA}$$

$$\text{Current at the AC Load Center input}, I_{Load,AC} = \frac{1\text{M}}{1000} = 1.0 \text{ kA}$$

The waveforms for this case are provided in Figs. 3.13 and 3.14 with the 1-kVdc bus filter capacitor removed and load capacitors in place. The buck converter output current reaches a value of 11.125 kA from the steady-state value of 4.25 kA, with the current through "DC Load 1" SSCB reaches a value of about 8.5 kA. From these results, the faulted "DC Load 1" SSCB goes only into FCL mode while the other sections of the system continue normal operation even though FCL function was incorporated in the load SSCBs (protecting downstream loads) and the

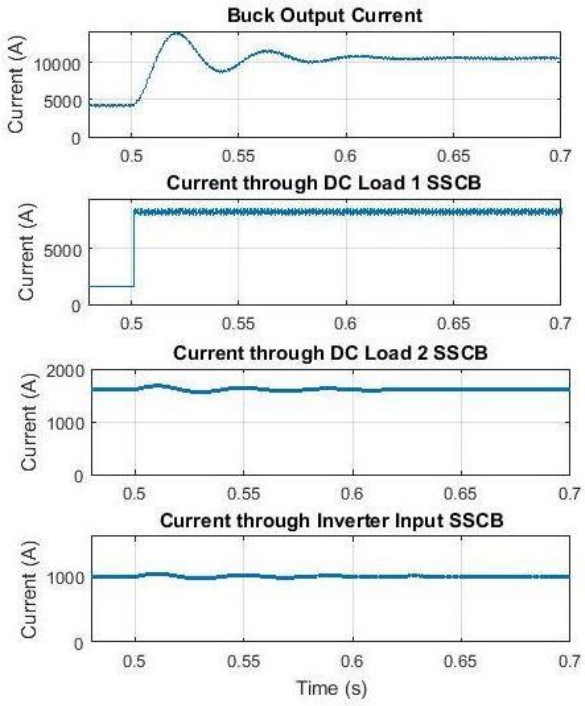


Fig. 3.13. Current waveforms at the buck converter output, DC Load 1, DC Load 2, AC Load for a pole-to-pole fault at "DC Load 1" at t = 0.5 s (case 2)

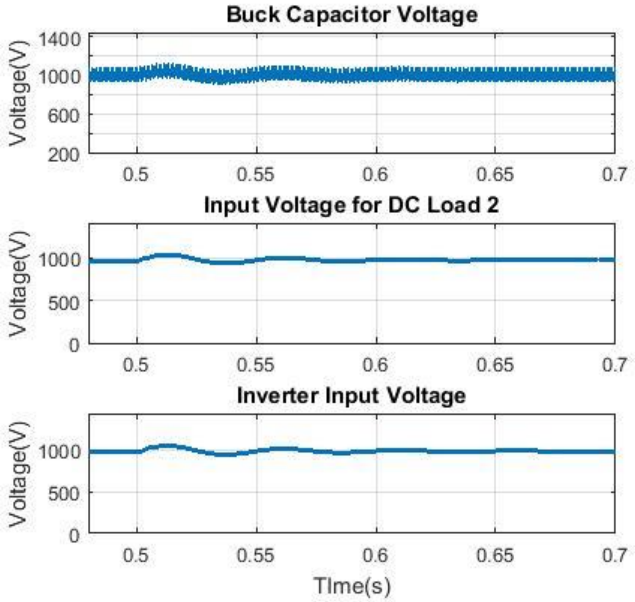


Fig. 3.14. Voltage waveforms at the buck converter output, dc load and ac load buses for a pole-to-pole fault at "DC Load 1" at t = 0.5 s (case 2)

buck-converter SSCB (located upstream). This ensures that power flows are not disrupted throughout the unfaulted portion of the load center, particularly, power flows to critical loads. This selectivity is the basis for achieving proper coordination of protection devices because only the SSCB protecting the faulted load goes into FCL mode while the other SSCBs are not affected.

This ensures that power flows are not disrupted throughout the unfaulted portion of the dc and ac load centers, particularly, power flows to critical loads. This selectivity is the basis for achieving proper coordination of protection devices because only the SSCB protecting the faulted load goes into FCL mode while the other SSCBs are not affected.

3.7 Summary

The following activities were performed in this chapter:

- Explanation of the proposed FCL control circuit and its MATLAB/Simulink™ implementation.
- Fault analysis including the impact of controller delays and capacitive discharge.
- Assessment of the coordination between upstream and downstream SSCBs during FCL operation for two operating points of the system.

The following chapter will focus on the comparison of different fault-current detection techniques for implementing FCL, and the impact of FCL operation on RB-IGCT's thermal handling requirements.

3.8 References

[1] Cuzner, R.M.; Venkataramanan, G., "The Status of DC Micro-Grid Protection," in *Industry Applications Society Annual Meeting, 2008. IAS '08*. IEEE , vol., no., pp.1-8, 5-9 Oct. 2008

[2] Jin, C., Dougal, R.A. and Shengyi, L. "Solid-state Over-current Protection for Industrial DC Distribution Systems." in *4th International Energy Conversion Engineering Conference and Exhibit (IECEC)*, pp 26-29. 2006.

[3] S. Munasib and J. C. Balda, "Short-circuit protection for low-voltage DC microgrids based on solid-state circuit breakers," *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Vancouver, BC, 2016, pp. 1-7.

[4] Fletcher, S.D.A.; Norman, P.J.; Galloway, S.J.; Crolla, P.; Burt, G.M., "Optimizing the Roles of Unit and Non-unit Protection Methods Within DC Microgrids," in *Smart Grid, IEEE Transactions on* , vol.3, no.4, pp.2079-2087, Dec. 2012

[5] Park, J.-D.; Candelaria, J., "Fault Detection and Isolation in Low-Voltage DC-Bus Microgrid System," in *Power Delivery, IEEE Transactions on* , vol.28, no.2, pp.779-787, April 2013

[6] K. G. Shin and Xianzhong Cui, "Computing time delay and its effects on real-time control systems," *IEEE Transactions on Control Systems Technology*, vol. 3, no. 2, pp. 218-224, June 1995.

CHAPTER 4

IMPACT OF FCL FUNCTION ON THE OPERATION OF THE NOTIONAL 1kVDC SYSTEM

4.1 Introduction

A notional low-voltage dc distribution system and its short-circuit protection incorporating fault-current-limiting (FCL) function was described in previous chapters. In this chapter, different fault-current detection approaches implemented towards fault-current-limiting function will be compared using the let-through energy at the fault location as the figure of merit. The RB-IGCT's thermal handling requirement and the impact of FCL operation on the MOV will also be discussed [1].

4.2 Fault-Current Detection Techniques

The FCL function considered earlier for a SSCB used an overcurrent threshold technique for activating the FCL operation mode. However, there are other major fault-detection techniques proposed in literature; in particular: undervoltage threshold, apparent resistance, current derivative and a combination of overcurrent and current derivative techniques [2-5]. These techniques are compared in terms of the let-through energies $[i^2(t)t]$. The $[i^2(t)t]$ is a measurement of thermal energy linked with the flow of current, hence useful in determining the impact of the heating of the conductors at the specified locations during short-circuit conditions. Thus, the magnitudes of $[i^2(t)t]$ would explain the stress on system components during FCL operation based on different fault-detection techniques and consequently aid in designing protection requirements.

A brief description of the techniques is as follows:

4.2.1 Overcurrent threshold: The overcurrent threshold technique is considered first since it is the simplest fault-detection technique. The FCL mode is activated if the SSCB current exceeds a specified current threshold set here at twice the rated current. An overcurrent threshold of 6.5 kA is used for the selected case study with the load rated 3.25 MW and 1 kVdc. The choice of twice the rated current is based on two main criteria: (1) avoidance of nuisance tripping following high currents occurring due to normal operation of the load, and (2) fast enough response to enable coordination with upstream SSCBs, avoiding damage to the semiconductor devices or any piece of equipment in the system.

4.2.2 Undervoltage threshold: The voltage across an output-filter capacitor decreases rapidly when subjected to a fault since power converters do not contribute significantly to replenish the capacitor charge and the fault current. In addition, the power converters would either shut down or also operate under FCL mode to protect the converter semiconductor devices. Here, the FCL mode is activated upon reaching an undervoltage threshold set at 500 V or 50% of the dc-bus rated voltage.

4.2.3 Apparent resistance: This value is calculated as the ratio of the measured voltage and current at the considered SSCB [4]. When this resistance is below a threshold set at a fraction of the rated value, the SSCB goes into FCL mode. The apparent resistance threshold is set at half of the rated apparent resistance; that is, corresponding to a fault current of twice the rated current, to be consistent with the overcurrent detection technique.

4.2.4 Current derivative threshold: This technique is based on the principle that current will rise faster under short-circuit conditions than at rated operating conditions. The current derivative of the SSCB is monitored, and the FCL mode is activated as the derivative exceeds a set threshold. Here, thresholds of 20 A/μs (or 20 MA/s) and 5 A/μs are considered.

4.2.5 Combination of overcurrent and current derivative threshold: This method combines the overcurrent and current derivative threshold techniques. The FCL mode is activated if either or both the overcurrent and current derivative thresholds are exceeded.

4.3 Let-through Energy Comparison between Different Fault-Detection Techniques

The let-through energies $[i^2(t)t]$ for the buck-inductor and "DC Load 1" currents for SSCB operation in FCL mode are used as the figure of merit to compare the effectiveness of the five considered fault-detection techniques. The let-through energy is calculated as the integral of the square of the current from the fault starting time until the SSCB would isolate the fault; the time is arbitrarily selected at 10 ms.

A pole-to-pole fault at the "DC Load 1" (shown in Fig. 2.1) is applied at t = 0.5 ms. Upon detection of the threshold crossing, the SSCB protecting "DC Load 1" enters into FCL mode, and the let-through energy is calculated onwards for 10 ms. The results are analyzed in the following section.

4.4 Comparison of Undervoltage and Overcurrent Threshold Techniques

Table 4.1 presents the let-through energies for all five techniques with the overcurrent and apparent resistance techniques having the lowest values of $[i^2(t)t]$ at the buck inductor current with a value of 4.7×10^5 A^2s for 10 ms from fault, and at the faulted "DC Load 1" SSCB with a value of 1.66×10^5 A^2s for 10 ms from fault. Thus, the overcurrent and apparent resistance techniques lead to comparatively lower thermal and mechanical stresses on the protection equipment as compared to the other techniques. The apparent resistance technique, however, is difficult to implement practically as the fault impedance between the faulted poles is required to be estimated. Thus, high fault impedances may result in erroneous calculation of the fault-current

Table 4.1: Comparison of $i^2(t)t$ for different threshold types

Threshold Type	Measured $i^2(t)t$ for Buck Inductor Current (10 ms from fault) (A^2s)	Measured $i^2(t)t$ for Load SSCB Current (10 ms from fault) (A^2s)
Overcurrent (twice the rated current)	$4.7x10^5$	$1.66x10^5$
Undervoltage (50% of rated voltage)	$5.5x10^6$	$2.2x10^6$
Apparent resistance (half of rated resistance)	$4.7x10^5$	$1.66x10^5$
Current derivative (20 A/μs)	$2.2x10^6$	$1.06x10^6$
Current derivative (5 A/μs)	$7.2x10^5$	$2.8x10^5$
Overcurrent+current derivative (20 A/μs)	$9.79x10^5$	$3.75x10^5$

threshold. Hence, overcurrent technique was used in FCL implementation. The measured $[i^2(t)t]$ values in table 4.1 are comparable to IGCT load integral values, for example, 'ABB IGCT 5SHY 2035L4520' has a limiting load integral of $5.12x10^6$ A^2s for a repetitive surge current of 32 kA for 10 ms. For the overcurrent technique, the measured $[i^2(t)t]$ for faulted "DC Load 1" SSCB current is $1.66x10^5$ A^2s for 10 ms from fault.

A sensitivity analysis is performed to compare the overcurrent and undervoltage techniques varying the threshold level of the latter from 0.5 p.u. to 0.965 p.u. The results are presented in Tables 4.2 and 4.3. The undervoltage threshold at 0.965 p.u. yields $[i^2(t)t]$ values for the buck-inductor and load-SSCB currents to be within 10% of the values obtained for the overcurrent threshold set at twice the rated current. It is concluded that the overcurrent threshold produces minimal transients during faults since the undervoltage technique having low threshold values leads to higher voltage drops and larger current overshoots during the capacitor re-charging to the rated voltage once the FCL mode is activated.

Table 4.2: Comparison of $i^2(t)t$ for buck inductor current for two threshold types

Overcurrent Threshold		Undervoltage Threshold	
Criterion	**$[i^2(t)t]$ for Buck Inductor Current Over 10 ms (A^2s)**	**Criterion**	**$[i^2(t)t]$ for Load SSCB Current Over 10 ms (A^2s)**
Twice the rated current	$4.7x10^5$	0.5 p.u.	$5.5x10^6$
		0.6 p.u.	$3.8x10^6$
		0.7 p. u	$2.6x10^6$
		0.8 p.u.	$1.9x10^6$
		0.9 p.u.	$1.47x10^6$
		0.95 p.u.	$1.12x10^6$
		0.965 p.u.	$9.86x10^5$

Table 4.3: Comparison of $i^2(t)t$ for load SSCB current for two threshold types

Overcurrent Threshold		Undervoltage Threshold	
Criterion	**$[i^2(t)t]$ for Load SSCB Current Over 10 ms (A^2s)**	**Criterion**	**$[i^2(t)t]$ for Load SSCB Current Over 10 ms (A^2s)**
Twice the rated current	$1.6x10^5$	0.5 p.u.	$2.2x10^6$
		0.6 p.u.	$1.63x10^6$
		0.7 p. u	$1.15x10^6$
		0.8 p.u.	$7.65x10^5$
		0.9 p.u.	$5.84x10^5$
		0.95 p.u.	$4.23\ x10^5$
		0.965 p.u.	$3.78x10^5$

4.5 Impact of Fault-Current-Limiting on RB-IGCT's Thermal Handling Requirement

Reliable operation of power semiconductor devices is substantially dependent on a proper thermal capability design. This is even more important for SSCB applications where the main purpose is to provide short-circuit protection to a portion of the power system without exceeding

the thermal limits of the devices themselves. Thus, the selection of the RB-IGCT for an SSCB application will be further validated by analyzing its thermal capability in FCL operation.

4.5.1 Methodology for Thermal Requirements Analysis of RB-IGCT in a SSCB

The methodology for analyzing the required thermal handling requirements of RB-IGCTs in SSCB applications consists of the following steps:

- Calculate the maximum allowable power dissipation through each RB-IGCT using the thermal impedance, maximum allowable junction temperature and case temperature provided in the device datasheet; that is:

$$P_{(AV)M} = \frac{T_{vj,max} - T_c}{R_{th(j-c)}} \tag{4.1}$$

where, $P_{(AV)M}$ = maximum allowable power dissipation;

$T_{vj,max}$ = maximum junction temperature (this temperature must be reduced by a safety margin; for example, 15^{o}C); T_c = case temperature; $R_{th(j-c)}$ = junction-to-case thermal resistance.

- For dc systems, the RMS and average currents are equal and denoted as I_{dc}; so, solve for I_{dc} using:

$$P_{(AV)M} = V_{T0} I_{dc} + r_T {I_{dc}}^2 \tag{4.2}$$

where V_{T0} = threshold voltage; r_T = device resistance both from the device datasheet.

- Verify that the selected RB-IGCT with has an higher average on-stage current $I_{T(AV)M}$ higher than the calculated I_{dc}.

- Determine the number of RB-IGCTs required to be connected in parallel taking into account the safe operating area and reliability. A rule of thumb used here is that the required current capability is twice the maximum dc current; that is:

$$n_{RB-IGCT} = \frac{2xI_{Load,max}}{I_{T(AV)M}} \tag{4.3}$$

- Calculate the device current at rated operating conditions:

$$I_{RB-IGCT} = \frac{I_{Load,rated}}{n_{RB-IGCT}} \tag{4.4}$$

- Calculate the fault current to be carried by each RB-IGCT during the FCL mode; this current has to be smaller than the maximum controllable turn-off current I_{TGQM}. As before, the number of devices would need to be recalculated if this criterion is not met.

- Calculate the losses during normal operating conditions in a single RB-IGCT, and using thermal impedance data, verify that the maximum junction temperature is not exceeded. If this criterion is not met, then the number of devices would need to be recalculated.

- Calculate the losses during the FCL mode for a single RB-IGCT and validate the junction temperature compared to the maximum allowable junction temperature. As before, the number of devices would need to be recalculated if this criterion is not met.

A simple thermal analysis based on the methodology described above under FCL operation at a dc load branch protected by a SSCB is demonstrated below based on estimated parameter values obtained from [1][6-7].

4.5.2 Calculations for Determining Operating Conditions for Thermal Analysis

According to the steps described in the previous section and using the parameters in Table 4.4 having estimated values for a 2.5-kV RB-IGCT [5], the maximum dissipated power is given by:

$$P_{(AV)M} = \frac{T_{vj,max} - T_c}{R_{th(j-c)}} = 1{,}785.8\ \text{W}$$

where, $T_{vj,max}$= 110 °C (applying a 15 °C safety margin); T_c = 85 °C; and $R_{th(j-c)}$ = 8.5 K/kW.

Using V_{T0} = 1.1 V slope resistance, $r_T = \frac{1-0.9}{1{,}600-1{,}000} = 0.1\ \text{m}\Omega$ results in $I_{dc} = 1.435\ \text{kA}$, which is lower than $I_{T(AV)M}$ of 1.5 kA.

At a rated power of 3.25 MW, the load current is $I_{Load} = \frac{3.25\ \text{M}}{1000} = 3.25\ \text{kA}$, yielding 5 devices in parallel (from equation 4.3).

Considering that the overcurrent threshold for the load SSCB is set at 6.5 kA and a 40-µs controller delay after the fault current reaches the overcurrent threshold, the peak fault current was earlier calculated as 18.78 kA.

The fault current per device is: $I_{D,FCL} = \frac{18{,}780}{5} = 3.76\ \text{kA}$ which is greater than the maximum controllable turn-off current of $I_{TGQM} = 3\ \text{kA}$.

So, 5 devices in parallel do not fulfill the current capability criterion. Therefore, the number of devices based on the value I_{TGQM} is recalculated as follows:

$$n_{RB-IGCT} = \frac{18{,}780}{3{,}000} \approx 7$$

Table 4.4 Device Parameters Used for Loss Calculations for Determining RB-IGCT's Thermal Requirements

Parameters	Values
Threshold voltage, V_T	1.1 V
Device resistance, r_T	0.1 mΩ
Average on-state current, $I_{T(AV)M}$	1.5 kA
Maximum controllable turn-off current, I_{TGQM}	3 kA
Turn-on energy, E_{on}	2.3 J
Turn-off energy, E_{off}	2.85 J
Junction-to-case thermal resistance, $R_{th(j-c)}$	8.5 K/kW
Maximum allowable junction temperature, T_{vjmax}	125 ℃

Current to be carried by a single RB-IGCT under rated conditions is now, $I_D = \frac{3{,}250}{7} =$ 464.3 A.

4.5.3 Thermal Analysis during Normal Operating Conditions

The SSCB experiences only conduction losses in this operating mode. Hence, conduction losses in the RB-IGCT,

$$P_{cond} = V_{T0} I_D + r_T {I_D}^2 = 464.3\text{x}1.1 + 0.1\text{mx}464.3^2 = 532.28\ \text{W}$$

For case temperature $T_C = 85$ ℃, the operating junction temperature is approximated by $T_j = T_C + P_{cond} R_{th(j-c)} = 89.52$ ℃ and does not exceed as expected its maximum value.

4.5.4 Thermal Analysis during FCL Mode

The SSCB experiences both turn-off and turn-on losses; there are no conduction losses in this mode because of the fast rise of the fault current. Using Table 4.4, the total switching energy loss is given by:

$$E_{FCL} = E_{on,FCL} + E_{off,FCL} = 2.85 + 2.3 = 5.15\ \text{J}$$

Considering $P_{(AV)M}$, the maximum operating switching frequency that RB-IGCT can be operated during FCL mode is (for 7 devices):

$$f_{s,max} = \frac{1{,}785.8}{5.15} = 346.75\ \text{Hz}$$

With the total switching energy loss given by:

$$P_{D,FCL} = \left(E_{on,FCL} + E_{off,FCL}\right) f_{s,max} = 1.78\ \text{kW}$$

For a case temperature $T_C = 85\ ℃$, the operating junction temperature becomes:

$$T_j = T_C + P_{D,FCL} R_{th(j-c)} = 101.3\ ℃$$

The calculated junction temperature value is under the specified maximum value of 110 ºC (that assumed a safety margin). At this point, the designer may decide on adding more RB-IGCTs in parallel to improve the thermal capability of the SSCB if a higher switching frequency is required, e.g., 1 kHz. The turn-on and turn-off switching energy losses per device would be reduced by adding more devices, and hence meeting the maximum allowable junction

Table 4.5: Loss Calculations for Determining SSCB Thermal Requirements

No. of Devices	Operating Condition	Parameter	Values
7	Normal operating condition	Conduction loss	0.53 kW
		Operating junction temperature	89.52 ℃
	FCL mode	Turn-on switching power loss	0.98 kW
		Turn-off switching power loss	0.8 kW
		Total dissipated power	1.78 kW
		Operating junction temperature	101.3 ℃

temperature requirement. The results of this simple thermal analysis are summarized in Table 4.5.

The calculations shown above provide a simple step-by-step methodology for validating the SSCB thermal requirements based on a fixed number of parallel RB-IGCTs. It has also been shown that the maximum switching frequency is dependent on the number of RB-IGCTs connected in parallel in order to comply with the maximum allowable power dissipation. If operation at a higher switching frequency is desired, the number of RB-IGCT connected in parallel should be increased to reduce the device current and thus turn-on and turn-off switching energy during FCL operation.

4.6 Impact of Fault-Current-Limiting on Metal-Oxide Varistors

Metal-Oxide Varistors (MOV) are used in SSCB applications for absorbing the stored energy in the system inductance and thus preventing overvoltages across the SSCB during turn off [8-10]. This section addresses the impact that operation FCL operation of a SSCB has upon a MOV.

4.6.1 MOV Model and Simulation

The MOV is modeled as a series branch of a 2-kV dc voltage source, a 28-mΩ resistor, a 1-nH inductor and a diode in reverse connection with respect to the RB-IGCT instead of using the MATLAB/Simulink™ model because it leads to shorter simulation times.

Several cases based on different cable lengths in “DC Load 1” branch ranging from 50 m to 200 m with no MOV in parallel with the SSCB have been run in the notional 1kVdc system presented in Chapter 2. It has been observed that, for cable lengths greater than 150 m and less than 160 m, the RB-IGCT starts experiencing overvoltages during turn-off.

The simplified circuit in Fig. 4.1 is based on the configuration of the RB-IGCT carrying 1.5 kA with a cable impedance of 6 mΩ and 14 μH corresponding to a length of 200 m. The cable length was chosen based on the findings presented in the previous paragraph. The voltage-current characteristics and RB-IGCT turn-off waveforms for one complete switching cycle are shown in Fig. 4.2. The RB-IGCT current rises when a pole-to-pole fault is applied at "DC Load 1" at t = 0.02 s. The RB-IGCT turns off upon reaching the threshold limit of 3 kA and the ensuing overvoltage is clamped at twice the voltage as expected.

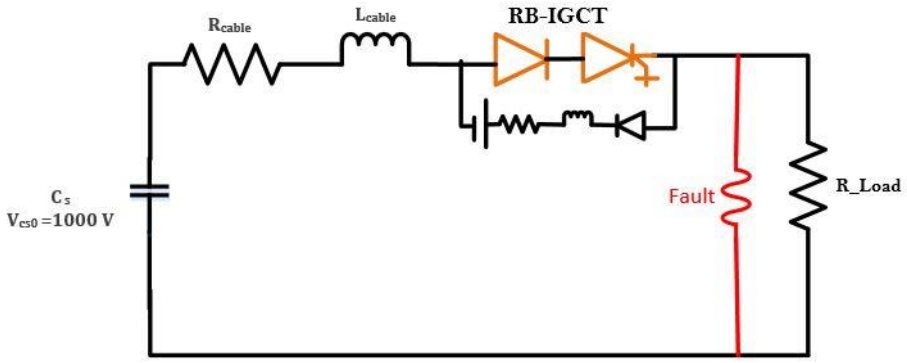


Fig. 4.1. Simplified circuit diagram for a 1kVDC load center for simulation of the FCL impact on the MOV

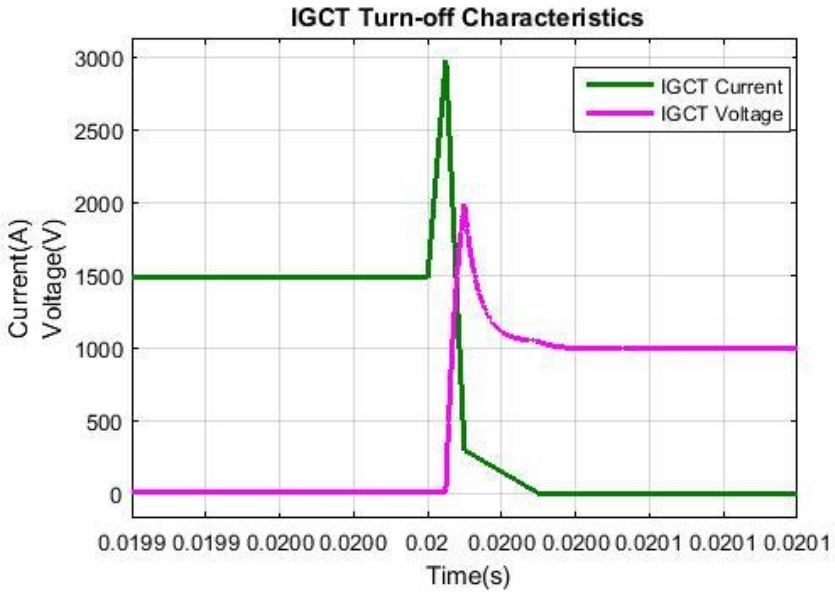


Fig. 4.2. RB-IGCT turn-off waveforms

4.6.2 Repetitive Operation of the MOV under the FCL Mode

The MOV is subjected to repetitive surges during the FCL mode. To analyze the impact upon the MOV, the absorbed energy is calculated and compared with the rated values obtained from the datasheet. The need for a cooling-down interval is also mentioned.

- *Energy absorbed by the MOV per cycle*

The energy absorbed by the MOV per cycle can be calculated as follows [8][9]:

$$E_{cycle} = KV_C I_{pk} t_i$$

where: K = constant, V_C = clamping voltage, I_{pk} = peak current, t_i = impulse duration.

For the considered case:

E_{cycle} = 1.4*2.5k*3k*100µ = 1.05 kJ.

From the datasheet of ABB surge arrester Polim R-2N [10], the energy absorption capability at a clamping voltage of 2.5 kV is $E_{capability}$ = 24x2.5 = 60 kJ. Thus, the maximum number of repetitive pulses under rated conditions is equal to $\frac{60\text{ k}}{1.05\text{ k}} = 57.14 \approx 57$. In other words, the MOV operating under the above conditions will be able to withstand 57 repetitive surges before its rated energy absorption capability is reached; i.e., 57 ms for a switching frequency of 1 kHz.

- *Cool-down interval*

For repetitive operations, the requirement of a cool-down interval can be ignored if the total energy absorbed is less than the rated energy absorption capability of the MOV. Upon reaching this limit (e.g., 57 surges considering the above case), a 45 to 60-minute cool-down interval is advised by the manufacturer before the next set of FCL operations in order to protect the MOV from severe degradation and subsequent failures [12]. The interval is

dependent on several attributes of the MOV (e.g., type of arrester material, ambient temperature etc.).

4.7 Summary

The following activities were performed in this chapter:

- Comparison of different fault-current detection approaches based on let-through energy for the application of FCL algorithm,
- Analysis of RB-IGCT's thermal handling requirements, and
- Evaluation of the impact of the FCL algorithm on the operation of MOVs

4.8 References

[1] S. Munasib and J. C. Balda, "Short-circuit protection for low-voltage DC microgrids based on solid-state circuit breakers," *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Vancouver, BC, 2016, pp. 1-7.

[2] D. Salomonsson, L. Soder, and A. Sannino, "Protection of low-voltage dc microgrids," *Power Delivery, IEEE Transactions on*, vol. 24, no. 3, pp. 1045–1053, July 2009.

[3] Fletcher, S.D.A.; Norman, P.J.; Galloway, S.J.; Crolla, P.; Burt, G.M., "Optimizing the Roles of Unit and Non-unit Protection Methods Within DC Microgrids," in *Smart Grid, IEEE Transactions on* , vol.3, no.4, pp.2079-2087, Dec. 2012

[4] Cairoli, P.; Dougal, R.A.; Lentijo, K., "Coordination between supply power converters and contactors for fault protection in multi-terminal MVDC distribution systems," In *Electric Ship Technologies Symposium (ESTS)*, IEEE , vol., no., pp.493,499, 22-24 April 2013

[5] E. Cinieri , A. Fumi , V. Salvatori and C. Spalvieri, "A new high-speed digital relay protection of the 3-kvdc electric railway lines", in *IEEE Trans. Power Del.*, vol. 22, no. 4, pp. 2262-2270, 2007

[6] ABB, “Reverse Blocking Integrated Gate-Commutated Thyristor 5SHZ 11H6500’. Available online at: https://library.e.abb.com/public/7f2b388387f8cef1c1257dea0043b854/5SHZ%2011H6500_5SYA1254-01%20Dec%2014.pdf

[7] U. Vemulapati et al., “Recent Advancements in IGCT Technologies for High Power Electronics Application”. Available online: https://library.e.abb.com/public/b8d1316db3904af0bf9371b32d478b07/Recent%20Advancements%20in%20IGCT%20Technologies%20for%20High%20Power%20Electronics.pdf

[8] J. Magnusson, R. Saers, L. Liljestrand and G. Engdahl, "Separation of the Energy Absorption and Overvoltage Protection in Solid-State Breakers by the Use of Parallel Varistors," in *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2715-2722, June 2014.

[9] Littelfuse: “Selecting a Littelfuse Varistor”. Application note. Available online at: http://www.littelfuse.com/~/media/electronics_technical/application_notes/varistors/littelfuse_selecting_a_littelfuse_varistor_application_note.pdf

[10] Vishay: “Varistors Introduction”. Application note. Available online at: http://images.vishay.com/books/VSE-DB0054-0909_Varistors_INTERACTIVE.pdf

[11] ABB Surge Arrester Polim-R..2N Datasheet. Available online at: https://library.e.abb.com/public/7d58b2c51c2bd6afc1257c2100348f7c/ABB%20Surge%20arrester%20POLIM-R%20-2ND%20-%20Data%20sheet%201HC0093995%20E01%20AB.pdf

[12] ABB: “Overvoltage Protection: Metal Oxide Surge Arresters in Medium Voltage Systems”. Application Note. Available online at: https://library.e.abb.com/public/70e9fd6933c8c644c12578d200333cb5/952_abb_awr_mittelspannung_E_low.pdf

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

5.1 Conclusions

The work presented in this thesis addressed some important issues regarding the short-circuit protection of low-voltage dc distribution systems. The following conclusions and contributions are drawn from the results presented and analyzed in the thesis:

- The RB-IGCT seems the best semiconductor device for implementing a 1-kVdc SSCB since it has the short-circuit capability of a thyristor (~ 3 kA), extremely low on-state voltage drop (~1.25 V) during normal SSCB operation, and blocks voltages in forward and reverse directions but conducts current only in the forward direction. It has low-thermal resistance, assisted by double-sided cooling and hermetic sealing resulting from its hockey-puck, thyristor-type package. All of these attributes should result in increased efficiency, compactness and reliability when compared to other controllable devices.
- Compared to the standardized opening time of 35-40 ms during a fault for electromechanical circuit breakers, the SSCB containing RB-IGCT as the semiconductor switch would exhibit an opening time of around 40 μs.
- Unavoidable controller delays require that additional devices be connected in parallel to sustain higher limiting fault currents. The evaluation of the FCL function incorporated an unavoidable controller delay that impacted the RB-IGCT's thermal requirements. FCL controller delays up to 40 μs were considered.
- The proposed fault-current-limiting algorithm ensured that the power flows were continuous in the dc zone with only the current in the faulted section limited to a user-

specified threshold. The unfaulted portion of the dc zone experienced minimal transients of short durations. For the evaluated case, the peak voltage swing was about 8.2% of the rated voltage. This behavior is very important for achieving coordination of protection devices because only the SSCB protecting the faulted load went into FCL mode while the other SSCBs were not affected.

- The impact of energy-storage filter capacitor at the 1-kVdc bus on the fault-current response has been addressed. With the filter capacitor in use, the fault current reached a peak of 18.78 kA before the SSCB on the faulted "DC Load 1" goes into FCL mode, requiring 7 RB-IGCT devices to be in parallel in the SSCB to carry the current. The removal of this filter capacitor bus resulted in a peak fault-current of 8.5 kA, requiring only 3 RB-IGCT devices to be parallel in the SSCB. Thus, removing the filter capacitor resulted in lesser number of devices in parallel, hence assuring better power density and lesser thermal stress on the system components.

- The FCL function was further evaluated using five different fault-detection techniques. The choice of the overcurrent technique was validated by comparing the let-through energies with the other considered techniques.

- The comparatively slower switching frequency ($\leq$ 1 kHz) did not have an impact on the SSCB operation. The maximum switching frequency is dependent on the number of RB-IGCTs connected in parallel in order to comply with the maximum allowable power dissipation. For example, the case study required 7 RB-IGCTs in parallel in the SSCB at a switching frequency of 346.75 Hz. If operation at a higher switching frequency is desired, the number of RB-IGCT connected in parallel should be increased to reduce the device current and thus turn-on and turn-off switching energy during FCL operation.

- The impact of FCL operation on metal-oxide varistors were evaluated by calculating the energy absorbed in each cycle by the MOV and quantifying the maximum number of cycles that the MOV can operate on before a cool-down interval is required. The application of the MOVs across SSCBs operating under FCL algorithm in dc systems require a high number of consecutive operations. A case study evaluated in Chapter 4 shows the MOV would be able to operate 57 times consecutively before its total dissipated energy exceeds its rated value.

5.2 Recommendations for Future Work

Several areas of improvement, pertaining both to the works within the thesis and the progressing research field of developing short-circuit protection for dc systems, are mentioned below:

- The proposed FCL algorithm has the potential to deliver swift, coordinated protection system operation for compact low-voltage dc distribution systems. A practical demonstration in real-time operating conditions would ensure a big step towards an optimal protection system, encompassing the firm protection requirements for the above mentioned systems.
- The applicability of the FCL operation can be extended to further analyze fault responses and associated protection schemes using SSCBs throughout different zones of notional all-electric ships. Even though the base system was a simple one having only one source and one power converter, the presented analysis should be applicable to dc distribution systems, i.e. microgrids having multiple sources and power converters. Preventing high fault currents by means of FCL operation results in reduced system costs and avoidance of over-dimensioning of system components.

Appendix A: Design Equations for System Parameters

With reference to Fig. 2.1 in Chapter 2, the values selected for different system components are addressed in this Appendix. In particular:

Buck-Converter Main Design Equations

$$V_{in} = 1200\ V, V_{out} = 1000\ V, \Delta I = 10\% = 750\ A, \Delta V = 10\% = 100\ V, f_s = 1\ kHz$$

$$D = \frac{1000}{1200} = 0.833;\ L = \frac{V_{in}D(1-D)}{\Delta I f_s} = 0.11\ mH;\ C = \frac{\Delta I}{8 f_s \Delta V} = 1875\ \mu F$$

$$\text{DC Load capacitor, } \mathrm{C_{Load}} = \frac{\mathrm{I} * \Delta \mathrm{t}}{\Delta \mathrm{V}} = \frac{3250}{1000\mathrm{x}10} = 325\ \mathrm{mF},\ \Delta \mathrm{V} = 1\% = 10\ \mathrm{V}$$

$$\text{DC Load capacitor, } \mathrm{C_{Load}} = \frac{\mathrm{I} * \Delta \mathrm{t}}{\Delta \mathrm{V}} = \frac{3250}{1000\mathrm{x}1000} = 166.25\ \mathrm{mF},\ \Delta \mathrm{V} = 5\% = 50\ \mathrm{V}$$

$$\text{DC Load capacitor, } \mathrm{C_{Load}} = \frac{\mathrm{I} * \Delta \mathrm{t}}{\Delta \mathrm{V}} = \frac{3250}{1000\mathrm{x}1000} = 32.5\ \mathrm{mF},\ \Delta \mathrm{V} = 10\% = 100\ \mathrm{V}$$

Main Equations for the SST

$$\text{Leakage inductance} = \frac{V_1 V'_2}{8 f P_0} = 0.55\ mH$$

$$\text{where } V_1 = V'_2 = 10\ kV, f = 3\ kHz, P_0 = 7.5\ MW$$

$$\text{Input capacitor, } C_i = \frac{I * \Delta t}{\Delta V} = \frac{750}{6000x1000} = 0.25\ mF, \Delta V = 10\% = 100\ V$$

$$\text{Output Capacitor, } C_0 = \frac{I * \Delta t}{\Delta V} = \frac{12500}{6000x120} = 17.36\ mF, \Delta V = 10\% = 120\ V$$

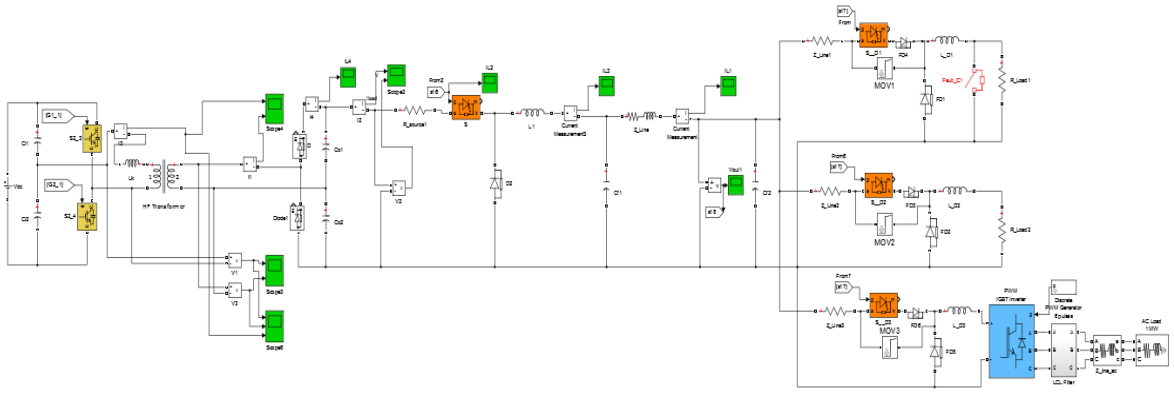


Fig. A.1. Matlab/Simulink™ implementation of notional 1-kVdc system

Selection of Kp and Ki for closed-loop SST control:

The dynamics of the output capacitor can be described as follows:

$$C_o \frac{dV_o}{dt} = K_p\left(V_{ref} - V_o\right) + K_i \int (V_{ref} - V_o)dt$$

Converting this equation to the Laplace or s-domain yields,

$$sC_oV_o = K_p\left(V_{ref} - V_o\right) + \frac{K_i}{s}(V_{ref} - V_o)$$

$$\frac{V_o}{V_{ref}}(s) = \frac{sK_p + K_i}{s^2 + s\frac{K_p}{C_o} + \frac{K_i}{C_o}}$$

which could be compared with the closed-loop transfer function of a second-order system

$$GH(s) = \frac{K}{s^2 + 2\xi\omega_n s + {\omega_n}^2}.$$

For $\xi = 0.707$ and $\omega_n = \frac{f_{PWM}}{20\xi} = 212\ rad/s$,

$$K_p = 2\xi\omega_n C_o = 14.98$$

$$K_i = {\omega_n}^2 C_o = 2247.2$$

$$Settling\ time = \frac{4}{\xi\omega_n} = 0.0266\ s$$

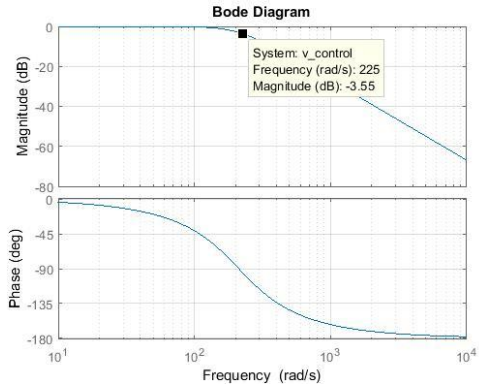


Fig. A.2. Bode plot of the PI controller

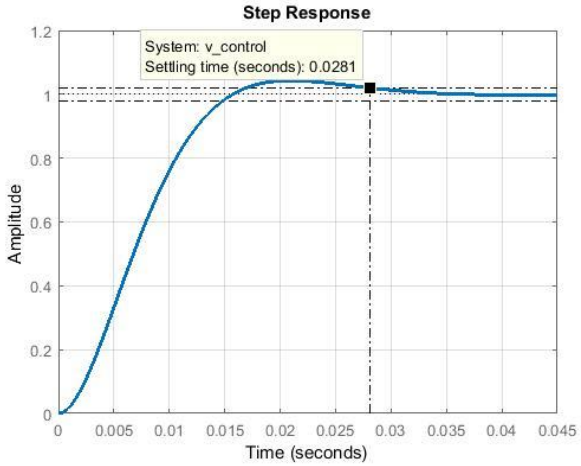


Fig. A.3. Step response of the PI controller

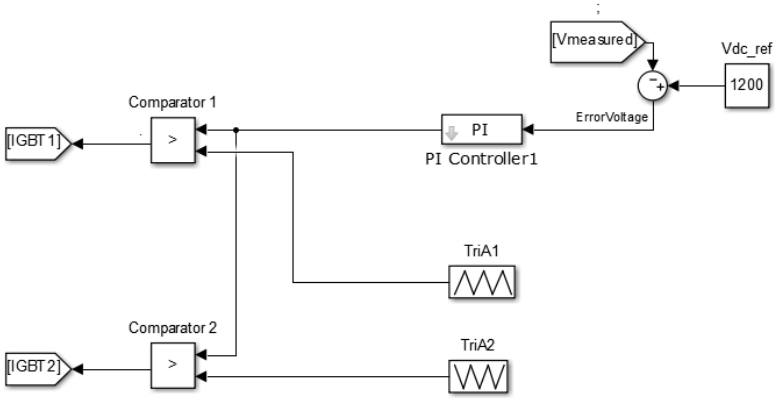


Fig. A.4. Closed-loop control block for SST

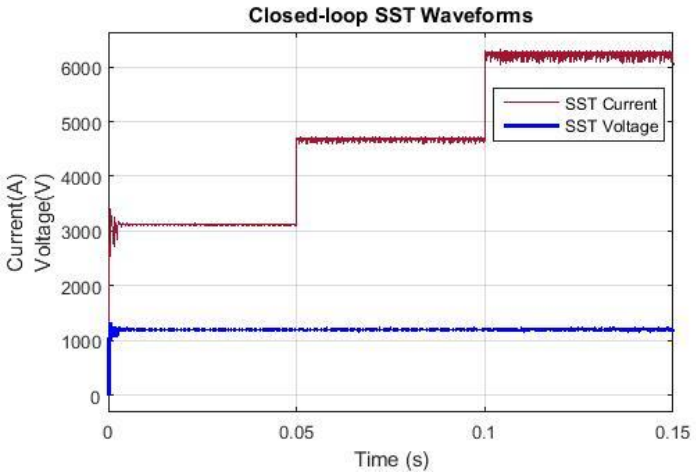


Fig. A.5. SST waveforms in closed-loop control at 50% (0-0.05s), 75% (0.05-0.1 s) and 100% (0.1-0.15 s) load conditions