5-2019

A Silicon Germanium CMOS Linear Voltage Regulator for Wireless Agricultural Applications

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A Silicon Germanium CMOS Linear Voltage Regulator for Wireless Agricultural Applications

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

by

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University of Arkansas
Bachelor of Science in Electrical Engineering, 2015

May 2019
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

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Abstract

This thesis presents the design, simulation and test results of a silicon germanium (SiGe) complementary metal-oxide-semiconductor (CMOS) linear regulator. The objective of the circuit is to power other analog devices regardless of the load current and input voltage changes. The application of this regulator is to be part of a project developing a miniaturized semiconductor platform that can be inserted into stems of crops in order to measure data inside the plant and then send it wirelessly to the user. The linear regulator was designed on a BiCMOS SiGe 0.13µm which is a GlobalFoundries process. It has been tested at room temperature and at 85 ºC with a supply voltage of 2.5 V and it holds an output of 1.2 V. The device demonstrates line regulation of 5 % % and load regulation of 0.19 % as well as rejection of the power supply satisfying the specifications proposed.

Acknowledgements

I would like to thank Dr. Alan Mantooth for the opportunity of being part of his IC design team. I am grateful for receiving me and trusting me with the tasks that I was assigned. I thank my committee members – Dr. Simon Ang, and Dr. Jia Di for supporting my work.

My sincerest gratitude goes the administrative staff. These ladies work behind curtains, and they take a lot of stress from our shoulders. The technical support team was also always there to solve any issues that came up. I would like to thank my teammates, who answered my questions and helped me out when in doubt. The help given by Maria Raquel Benavides Herrera goes beyond been a coworker, without her support and encouragement I would not have made it this far.

Lastly, I thank the University of Arkansas and the city of Fayetteville for opening its doors and receiving me. This place was my home away from home and I will be forever thankful for accepting me here.

Dedication

I would like to dedicate this thesis to my parents, Aminta del Carmen Robles Cordoba and Dionel Celiano Castillo Tristan. Thank you for your love and for being the fuel that keeps me going. Thank you for helping me fly.

I would also like to dedicate my thesis to the memory of Dr. Etilvia Maria Arjona Chang who believed in me even when I did not. Your passion, tenacity, and kindness will always be my inspiration.

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CHAPTER 1 : INTRODUCTION

As it was indicated by Moore's Law, the number of transistors on an integrated circuit doubles about every two years, which consequently has a direct effect on power consumption. Power management is, therefore, one of the most critical aspects in the integrated circuit (IC) design process. Voltage regulators are fundamental in an electronic circuit because they provide a constant voltage to the circuit they feed.

Similar to any electronic circuit, voltage regulators are designed to operate from a supply voltage. The regulator is a circuit that holds the output voltage continuously at the designed value regardless of the changes of the input voltage or load current. The designer assumes that the load voltage and the input current are within a specified range of operation. For this thesis, the regulator studied is a linear regulator which consists of control circuitry, a feedback loop, a reference voltage, and a series-connected transistor known as a "pass" device.

Linear regulators are broadly used to supply power to sub-circuits providing fast development for portable power management. The most obvious reasons for their implementation are their simplicity, small board space, low noise and low cost [1].

The linear regulator presented in this thesis has been designed with the purpose of being implemented in a project of developing a miniaturized sensing and data transmission platform. The miniaturized system can be inserted into stems of crops, in order to provide agricultural growers the capability of measuring data from inside the plant and transmitting it to central computer for processing. The power for the circuit is supplied by a microbattery with a thickness of only 1.0 mm, width of 2.3 mm, and a voltage of 2.5 V. The proposed regulator can supply a constant voltage of 1.2 V to the analog blocks the 2.5 V unregulated battery voltage as an input.

This regulator was designed in a BiCMOS SiGe 0.13µm process developed by GlobalFoundries. The transistors used have a 3.3 V V_{DS} (drain to source voltage). This process has seven metal layers which makes easier to attain a more compact device. In addition, it simplifies connections, since the metal levels allow one to alternate layers when making connections.

Data from simulation results are studied. Statistical analysis from simulation was performed to predict the behavior of transistors and capacitors, and depending on those results the size of the transistors and capacitor were selected. This thesis describes the design, simulation, and test of this linear regulator.

1.1 Thesis Structure

The thesis is divided into the following chapters.

- Chapter 1: Introduction – Motivation and background of the work are presented here.
- Chapter 2: Background – A description of the kinds of linear regulator and their subdivisions are presented in this chapter. The classification of the linear regulators is explained. A review of the pass structure review is described. In addition, important terminology about linear regulators is appended to this chapter.
- Chapter 3: Circuit Design and Simulation – This chapter describes the steps taken to design the circuit. Studying the specifications and achieving them through building schematics for simulation is described. Then, performing statistical analysis to obtain the required specifications is reported.
- Chapter 4: Testing and Characterization – This chapter describes the test setup and the procedures followed to test the linear regulator. In addition, measured results are compared with simulated results. Calculation of electrical characteristics is also obtained, and the results are discussed.

- Chapter 5: Conclusions and Future Work – A summary of the design and test results is presented in this chapter. Discussion of the future steps to improve the linear regulator are also provided.

CHAPTER 2 : BACKGROUND

In the electronics world there are two types of regulators, switching regulators and linear regulators. A switching regulator can manage both direct-current (dc) and alternating-current (ac) due to its switching attributes while the linear regulator behaves as a linear component (resistance load) from input to output. Accordingly, it supports dc-dc, dc-ac, ac-ac, and ac-dc conversion functions. The objective of this circuit is to energize capacitors and/or inductors from the supply and then drain them into the load during different cycles of the switching period, transferring input energy to the output via quasi-lossless energy-storage devices [1].

The four most commonly used switching regulators are:

- Boost: dc-dc power converter that steps up the input voltage
- Buck: dc-dc power converter which steps down the input voltage
- Buck-Boost: provides an output voltage with opposite polarity to the input voltage
- Flyback: can generate multiple outputs voltages less than or greater than the input voltage.

Linear regulators are also known as series regulators. Their function is to control the conductance of the pass device that connects the input source to the output. An amplifier maintains the output signal at an acceptable value by comparing the output voltage with a reference voltage. The output of the amplifier becomes the signal that controls the pass device, which then provides the expected output.

2.1 Classification of linear regulators

Linear regulators are classified by different characteristics such as: output current, dropout voltage, and compensation.

2.1.1 Output current

The most apparent characteristic of linear regulators is how much current or power they deliver. There are low-power regulators which are mostly used for portable applications and battery powered electronics. High-power regulators source higher currents and are mostly used to power industrial and automotive applications [1].

2.1.2 Dropout

The dropout voltage is defined as the minimum voltage required across the regulator to uphold regulation. The dropout is subdivided into high-dropout (HDO) and low-dropout (LDO) regulators. LDOs dissipate less power than HDOs. Low-dropout regulators are used on battery-powered applications with a low input supply. They can drop to 300 mV or less with a collector or drain output. High-dropout regulators drop over 600 mV [1].

2.1.3 Compensation

Frequency compensation is a technique used for op amps and linear regulators to avoid unintentional positive feedback which in most cases employs a capacitor. There are two types of compensation: external and internal. External compensation requires an output capacitor. Internally compensated regulators save area in the printed circuit board by placing a capacitance on chip [1].

2.2 Linear Regulator Stability

Stability is essential for control circuits, since they have inherent delay in the feedback loop. In regulator control systems, stability refers to the ability to maintain a constant output after a load or an input disturbance. A circuit can become unstable and oscillate when the output signal becomes superimposed due to the output lagging one full wavelength, or period of the signal [2].

Phase margin measures relative stability indicating the probability of a closed loop system to oscillate when the system suffers a disturbance. The phase margin is calculated for systems with a negative phase as the difference between -180° and the phase angle of the frequency where the response of the magnitude is 0 dB. For systems with a positive response, the phase margin is the phase itself at the frequency when the magnitude is zero. A negative phase margin stands for an unstable system while a positive phase margin yields a stable system. Nevertheless, systems with a small positive degree make an unreliable system. Generally, more than 45° is considered acceptable, and it is left to the designer's choice [2].

2.3 Related Terminology

There is certain terminology specific to linear voltage regulators. The following terms are described to ease the understanding of the subsequent chapters.

2.3.1 Dropout Voltage

It is the differential voltage between the input and the output at which the circuit no longer regulates as the input voltage decreases. The dropout voltage happens when the input voltage nears the output voltage.

In the case of a PMOS pass element, the voltage dropout (V_{DO}) is expressed as

$$V_{DO} = I_o \, R_{on} \tag{2.1}$$

where R_{on} is the on-resistance of the PMOS transistor.

2.3.2 Quiescent Current

Quiescent current is defined as the difference between the input current and the output current as shown in Eq. (2.2). In order to maximize the current efficiency, a low quiescent current is required.

$$I_q = I_i - I_o \tag{2.2}$$

Since metal oxide semiconductor (MOS) transistors are voltage driven devices, quiescent current is near a constant value with reference to the load current. Biasing currents of the band-gap reference, sampling resistor and the error amplifier are only things that contribute to the quiescent current regulator. Therefore, when power consumption is a critical specification [3].

2.3.3 Efficiency

The efficiency is calculated as the ratio of the output power to the input power. In the case of a linear regulator it comes in terms of quiescent current and the input and output voltages as follows

$$Efficiency = \frac{P_{out}}{P_{in}} = \frac{I_o V_o}{(I_o + I_q) V_i} \tag{2.3}$$

Since power dissipation relates to efficiency, the voltage difference between the input and output must be reduced. The reduction of the dropout voltage and quiescent current would also help increase the efficiency. The power dissipation is calculated as shown in Eq. (2.4).

$$Power\ Dissipation: (V_i - V_o) I_o \tag{2.4}$$

2.3.4 Line Regulation

Input voltage variation can potentially change the output voltage of a linear regulator. Line regulation is the measurement of the ability of the circuit to preserve the specified output voltage unaffected by the changes in the input voltage. Line regulation is calculated by the equation,

$$Line\ regulation = \frac{\Delta V_o}{\Delta V_i} \tag{2.5}$$

and is expressed as a percent change in the output voltage relative to the change in the input line voltage.

2.3.5 Load Regulation

The circuit's load changes can cause shifts in the output voltage. The measurement of the ability to maintain the output voltage under variable load circumstances is called load regulation, and it is expressed as follows

$$Load\ regulation = \frac{\Delta V_o}{\Delta I_o} \tag{2.6}$$

2.3.6 Power Supply Rejection

The power supply rejection ratio (PSRR), also known as ripple rejection ratio, measures how well the circuit rejects the ripple coming from the input at different frequencies (Eq. (2.7)). Ripple rejection is crucial in RF and wireless applications [4]. The relation of the line regulation is almost the same as the PSRR with the only difference being that PSRR considers the complete frequency spectrum.

$$PSRR = \frac{V_{o,ripple}}{V_{i,ripple}}\ at\ all\ frequencies \tag{2.7}$$

2.4 Pass Element Structure Review

The pass element function is to act as a resistor in the dropout region [5]. The value of this resistor will depend on the selected structure. There are bipolar and MOS transistors to be used for a pass transistor. Depending on the chosen architecture, there is an influence on the dropout voltage, quiescent current and general performance. Bipolar transistors are driven by the base current which is proportional to the collector current; therefore, a higher ground current is obtained.

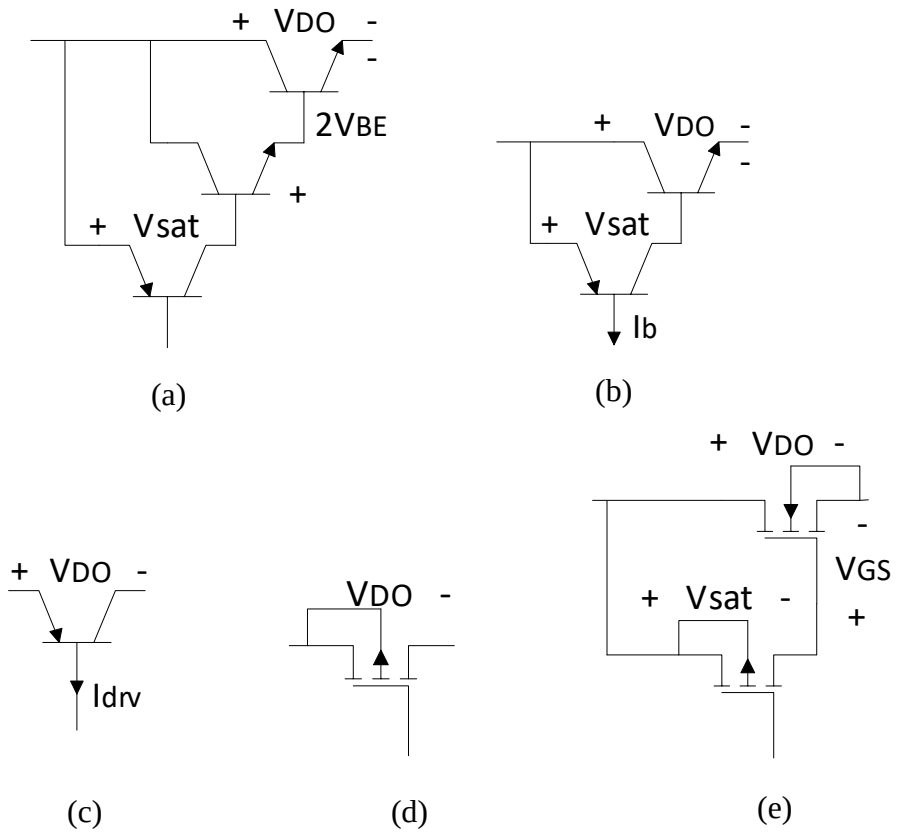

Fig. 2.1. Pass device alternatives (a) Darlington, (b) NPN, (c) PNP, (d) PMOS, (e) NMOS [6].

On the other hand, a MOS pass element is driven by the gate voltage. MOS structures allow a low voltage drop and a ground current that can be optimized [7]. Fig. 3.10 displays the alternatives for the pass device studied: Darlington, NPN, PNP, PMOS, and NMOS.

2.4.1 Darlington

A Darlington circuit is a transistor pair that provides a high level of current gain. It is shown in Fig. 3.10(a). It is a type of NPN regulator which requires at least a 1.5V dropout as Eq (2.8) shows [2]. This dropout voltage comes to be high, since most regulators work with less than 500 mV input to output voltage differential [6].

$$V_{dropout} = V_{CE}(sat) + 2V_{BE} \approx 1.6 \sim 2.5 \qquad (2.8)$$

2.4.2 NPN

Figure 3.10(b) is the NPN alternative that consists of a PNP and NPN transistor. The NPN transistor requires a base potential higher than the emitter potential so that the pass element can perform properly. The input rail through the PNP transistor provides the necessary current to drive the PNP transistor.

If the input voltage approaches the output voltage, the pass element is pushed towards saturation to ensure correct operation of the regulator. However, there is no issue when the input-to-output of the differential is high. Given that the NPN needs to maintain the necessary level of V_{BE} the value of the variable resistor cannot decrease to zero [6]. Therefore, the voltage required to maintain regulation is

$$V_{dropout} = V_{CE}(sat) + V_{BE} \geq 0.9\,V \tag{2.9}$$

2.4.3 PNP

A PNP pass device is shown in Fig. 3.10(c). It consists of a singular PNP transistor and operates in the same way as the NPN configuration. The PNP transistor, nevertheless, can maintain regulation with less voltage drop which is the big advantage of this regulator.

$$V_{dropout} = V_{CE}(sat) \approx 0.15 \sim 0.4\,V \tag{2.10}$$

One of the issues with this kind of pass device is that since it is current driven, the base current flows to the ground, but does not contribute to the ground [6].

2.4.4 PMOS and NMOS

The PMOS and NMOS structures employ MOSFET devices for the pass elements (Fig. 3.10(d) and Fig. 3.10(e)). The PMOS devices display a very low dropout voltage by themselves, while the NMOS devices would need a charge pump to have low dropout voltage. The saturation

voltage across the pass element determines the dropout voltage, which is proportional to the current flowing through the pass element. For a PMOS regulator the dropout would be

$$V_{dropout} = I_o R_{on} \approx 35 \sim 350\ mV \tag{2.11}$$

with R_{on} being the on-resistance of the pass device.

Since the MOSFET transistor structures are voltage controlled they do not require an increasing drive current when the output current increases [6].

CHAPTER 3 : DESIGN AND SIMULATION

As with most circuit designs, the design of this linear regulator started with the specifications for the circuit. The essential parameters that set the basic operating requirements for this circuit are the input supply voltage and the load current. For linear regulators, the response of the regulator to the fluctuations of these two parameters will govern how effective and how functional the design is. Another important parameter is the output voltage. The output voltage is the target voltage at the output which must be constant despite voltage changes in the supply voltage or load current changes. Table 3.1 describes the specifications for the linear regulator.

Table 3.1. Specifications for Linear Regulator

Specification	Symbol	Value
Input Voltage	VDD	2.5 V
Output Voltage	VOUT	1.2 V
Load Current	CLOAD	8 mA
Reference Voltage	VREF	1.25 V
Quiescent Current	I_Q	$\leq$ 100 µA

The input voltage is a set voltage coming from a lithium battery designed particularly the application. The constant output of 1.2 V will be the supply of a low noise amplifier (LNA) and a power amplifier (PA), since both are required to work with a low voltage supply. According to existing LNAs and PAs low voltage supply vary from 1.0 to 1.8V [8]–[11]. Hence, 1.2V is a reasonable supply for the amplifiers. A load current of 8 mA is also a realistic target when compared to the previous sources. In the worst-case scenario, the load current could go as high as 15 mA according to a simulation of the PA designed to be supplied. The voltage reference value of 1.25 V is set by a bandgap voltage reference that has been designed for this project. This value

will later be modified to the desired reference. The current consumption should not be more than 100 µA, in order to consume the least amount of power and prolong the microbattery life.

A diagram of the linear regulator is shown in Fig. 3.1 with the most important blocks: an error amplifier, pass device, voltage reference, feedback network, and capacitance load. Each of these blocks will be further described in this chapter as well as the design choices made.

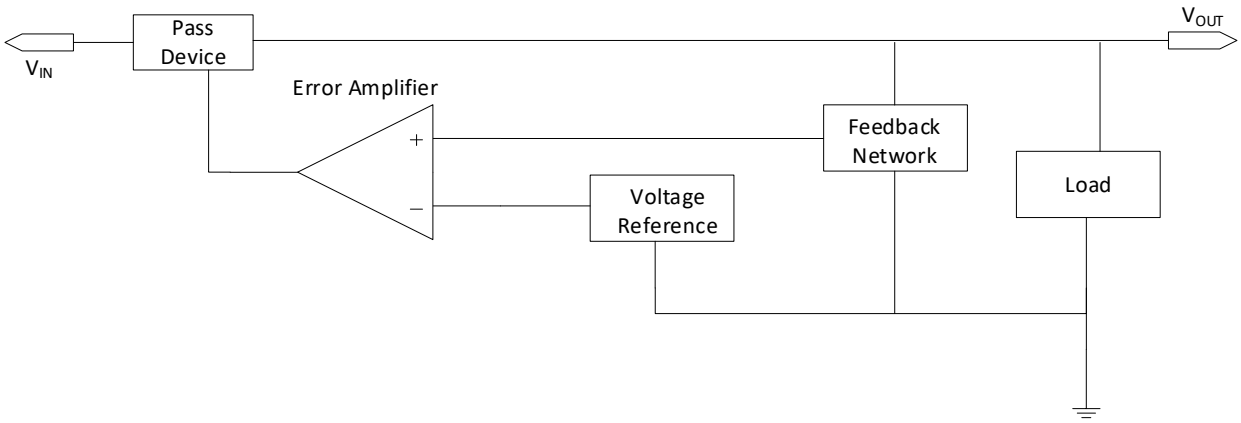

Fig. 3.1. Block diagram of a linear regulator.

3.1 Error Amplifier

An error amplifier compares the reference voltage to a scaled representation of the output, and then it amplifies the difference. It drives the PMOS transistor adjusting the gate to obtain the desired output voltage [10]. The amplifier implemented for the design is an indirect feedback, two-stage, differential amplifier [11] and it is shown in Fig. 3.2.

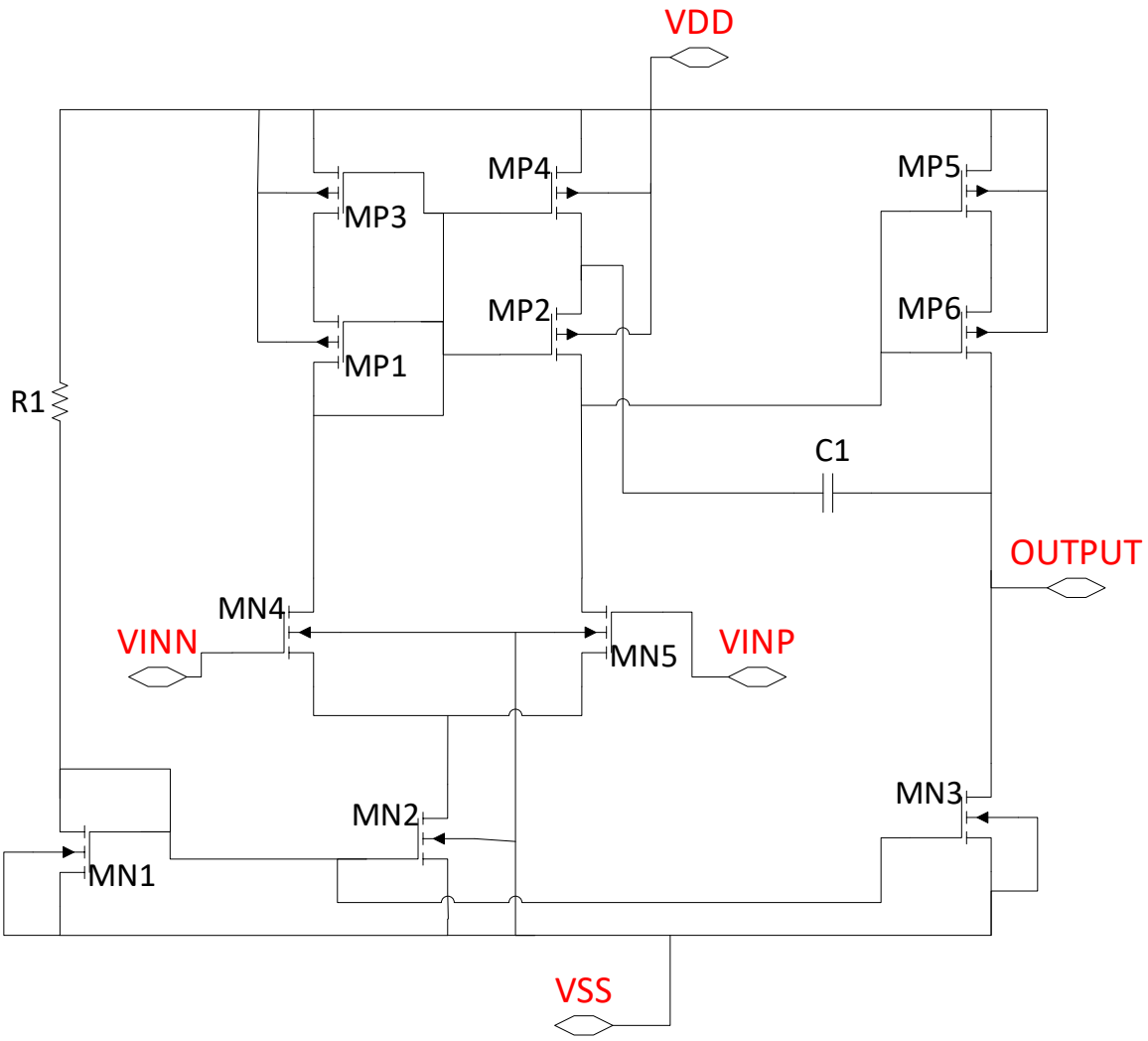

Fig. 3.2. Two-stage amplifier with indirect feedback compensation.

The circuit described by Baker sizes the width of the PFETs as double the size of the NFETs. In the case of this amplifier, the PFETs are required to be 8 times larger than the NFETs because it is observed in the simulations that with this ratio both, the NFET and the PFET, deliver about the same drain current.

MN2 and MN3 are the current sincks that biasd the diff pair MN4/MN5 and cascode amplifier output stage MP5/ MP6. Capacitor C1 is used for compensation to maintain stability in the circuit. For this application, it was recommended that a gain of 25 dB to 45 dB be achieved [10].

Simulations for the transistor values were performed under different circumstances and later the values were analyzed to select the best fit for the amplifier. In order to select the appropriate transistor values, a statistical analysis is utilized.

A response surface methodology (RSM) was used to perform these simulations. The RSM method is used for improving, developing and optimizing processes based on a group of statistical and mathematical techniques. It consists of inputting variables that potentially affect performance measures or quality characteristics of the process or product. These measures are called responses [12]. A design of experiments is executed with variables that will have an influence on the output of the amplifier. The outputs of the amplifier that were studied are the gain and the phase and the optimized variables were length, width and capacitance. The length refers to the length for all transistors, minimum width is the width for the NFETs and the width of the PFETs is 8 times larger for each case. The capacitance is the value of capacitor connecting stage one to stage two of the amplifier.

A design of experiments is performed for three different input variables and the values are shown in Table 3.2.

Table 3.2. Values of Parameters used for Response Surface Method

Minimum Width (μm)	Length (nm)	Capacitance (pF)
3	260	2
5	360	4
10	460	6

Simulations for all 27 combinations were obtained and the results were recorded to later perform the response surface in the statistical tool JMP [13]. JMP is used to analyze the data and create surface response models for contour plots and data optimization.

Based on the width and length variables, a prediction formula is obtained for the DC gain of the amplifier. A 3D surface response plot is generated as shown in Fig. 3.3. It is observed that the DC gain is higher when the width and length are at their highest values.

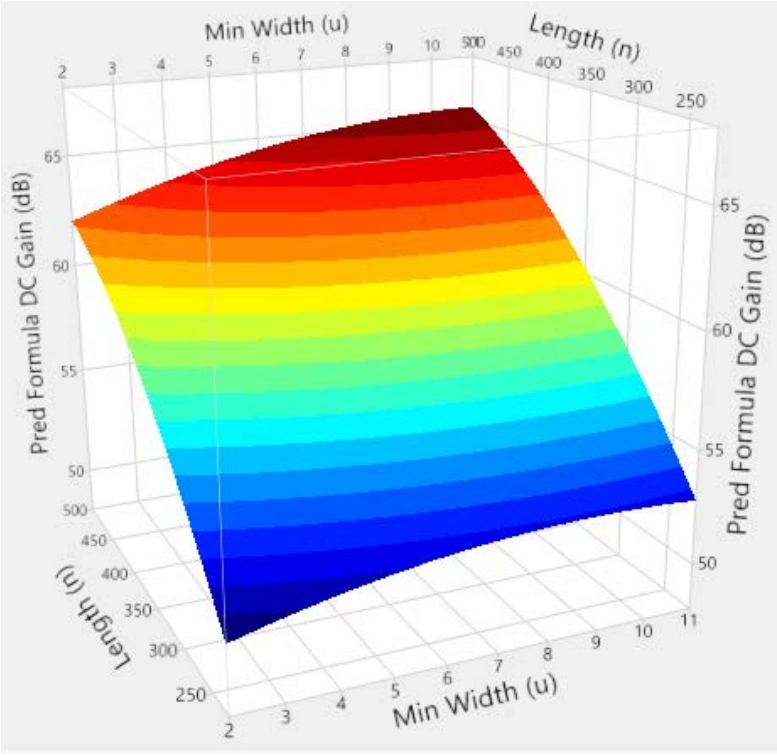

Fig. 3.3. Response surface analyzing minimum width, length, and prediction formula for DC gain of indirect feedback amplifier.

A contour plot is a technique used to denote a three-dimensional plot representing the horizontal axes and the vertical axes while the third axis is represented by lines of a constant value [14]. Fig. 3.4 is the contour plot of minimum width on the x-axis and length on the y-axis. Each of the red lines represents a different gain value.

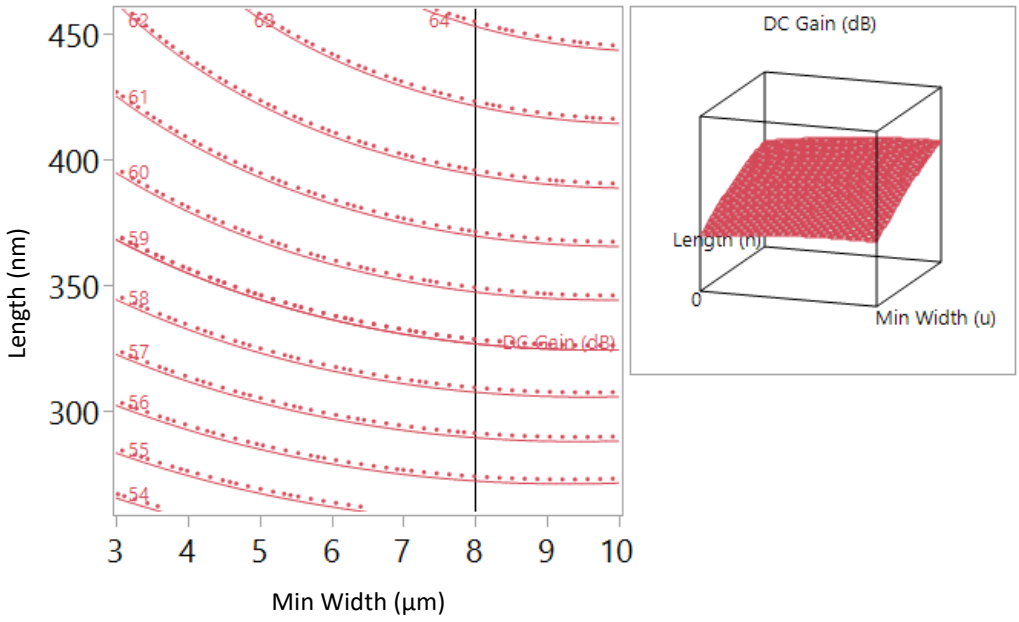

Fig. 3.4. Contour plot of minimum width, length, and prediction formula for DC gain of indirect feedback amplifier.

The minimum width for MOSFETs used in this design was 130 nm, and it is recommended to use double of the minimum length [11] which is 260 nm for the case. Based on this length, 8 µm for the width is selected since it offers a gain of 55 dB which is more than necessary for this application.

A prediction formula for the phase margin is obtained with the minimum width and capacitor variables (Fig. 3.5). It is important to note that the capacitor is considered only for the phase margin simulation because it only influences the phase margin and not the DC gain. While the value of the width decreases, the phase margin increases. On the other hand, an increment on the capacitance produces an increment on the phase of the amplifier. As shown in Fig. 3.6, a capacitor of 5 pF would be appropriate to obtain an ideal phase of 90, since the minimum width is 8 µm.

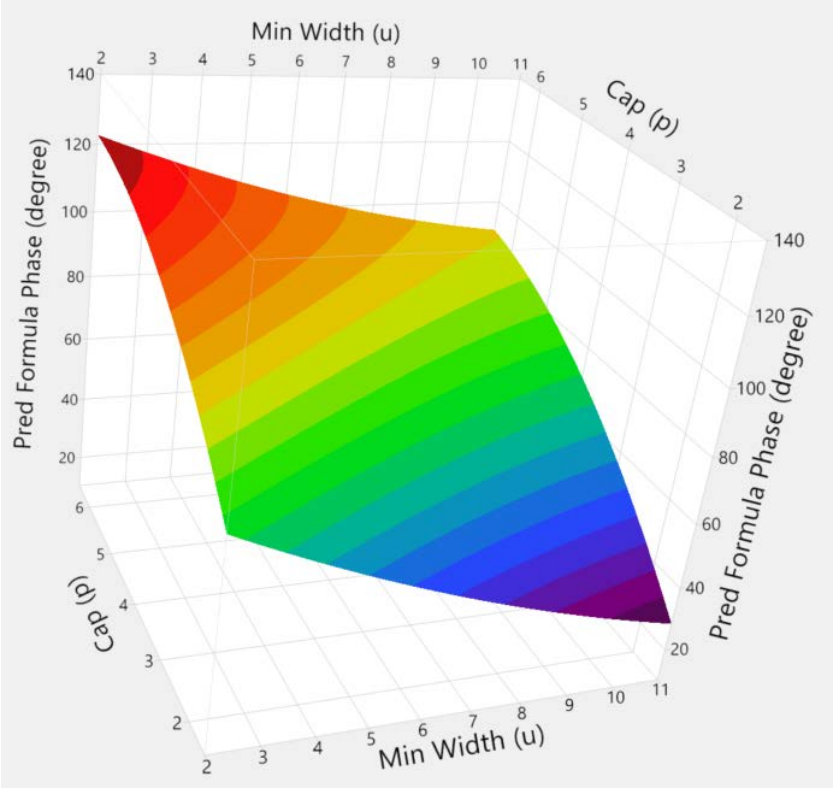

Fig. 3.5. Response surface analyzing minimum width, capacitance, and prediction formula for phase margin of indirect feedback amplifier.

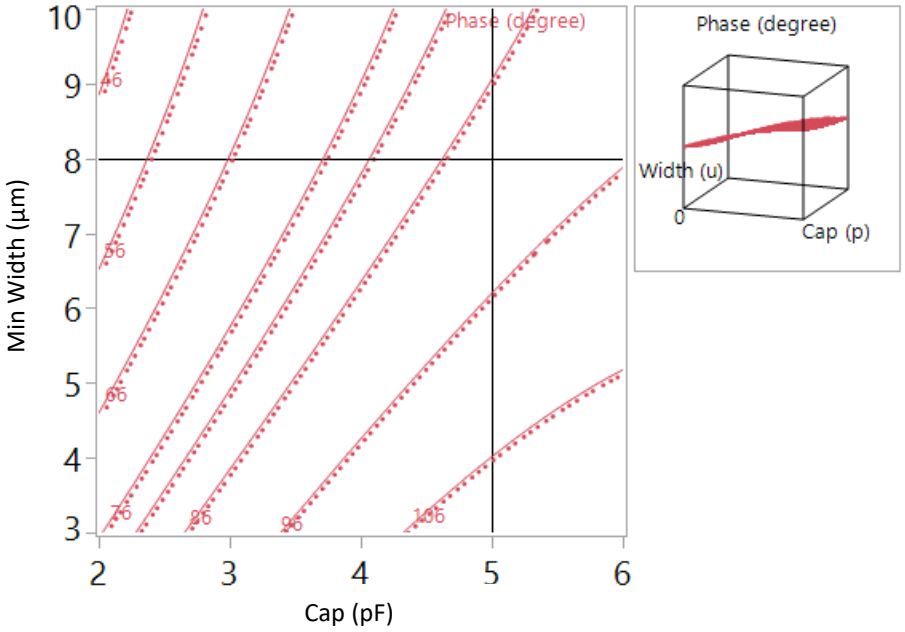

Fig. 3.6. Contour plot analyzing minimum width, capacitance, and prediction formula for phase margin of indirect feedback amplifier.

It is important to mention the resistor R1 helps achieve the desired biasing current. Connecting R1 to 2.5 V generates a current of 20 µA that MN1 mirrors to both stages of the differential amplifier.

After running the simulations with the values for capacitance, length and width, a phase margin of 87 ° is obtained along with a 54 dB of DC gain. These results fit into what the parameters studied require. The plots of DC gain and phase margin are found in Figs. 3.7 and 3.8, respectively.

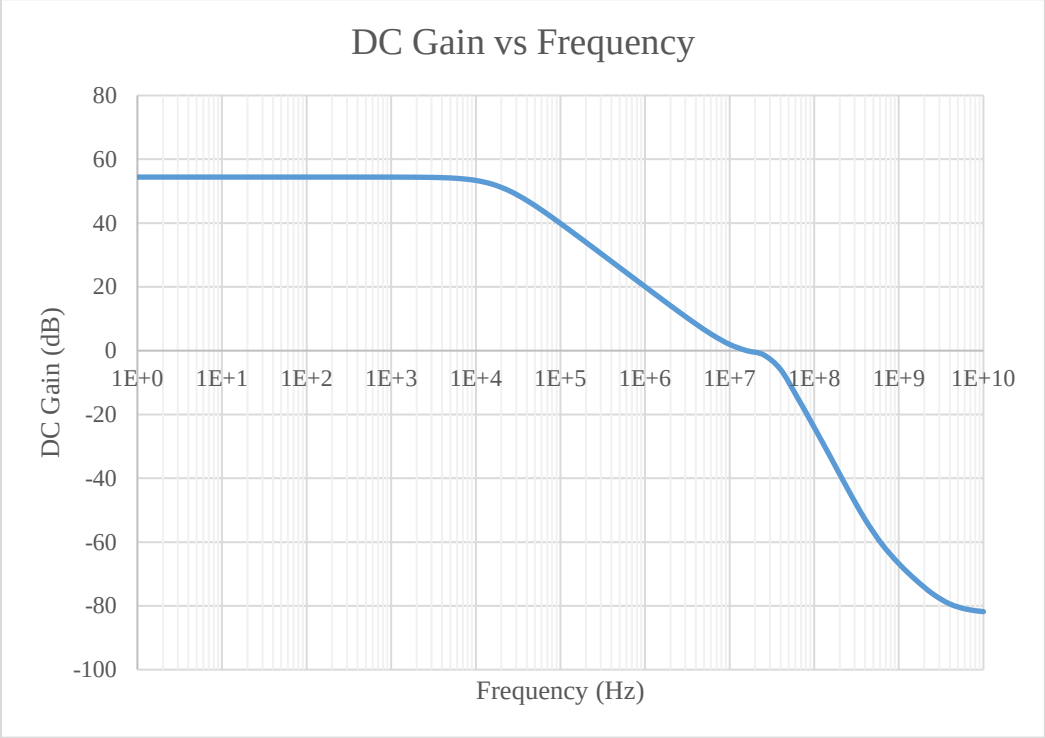

Fig. 3.7. DC gain plot of indirect feedback amplifier

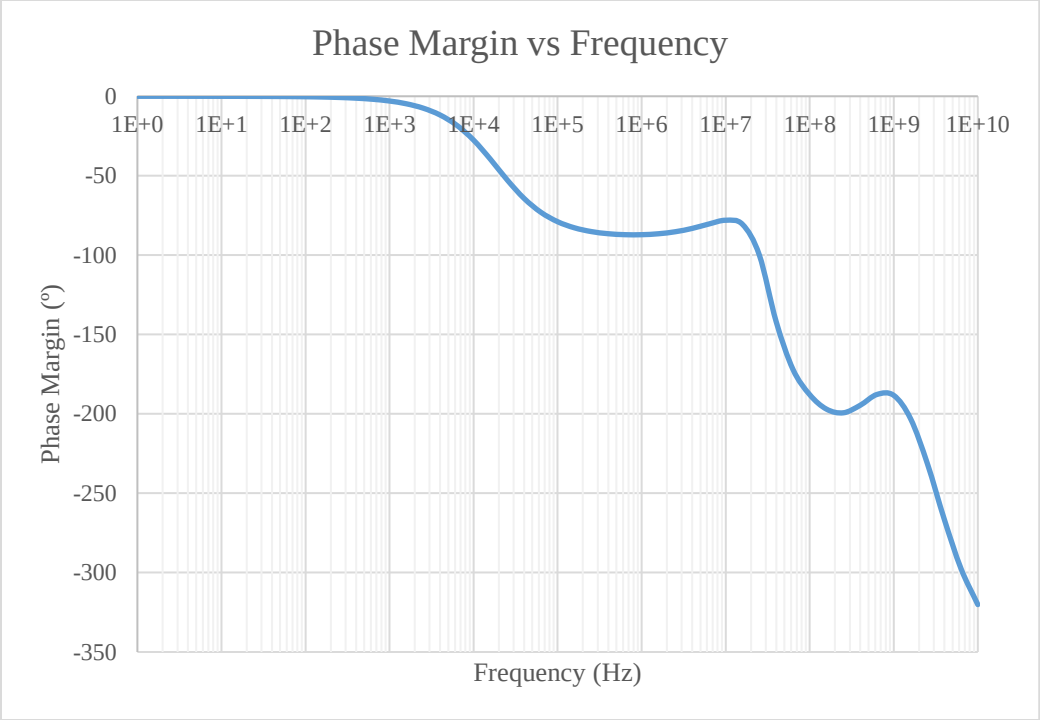

Fig. 3.8. Phase margin plot of indirect feedback amplifier

The amplifier designed is appropriate for other uses or by itself. However, after later simulations with the overall system it was required to increment the gain of the regulator. Thus, the error amplifier is enhanced by adjusting the system as described in [1]. With a resistor and a capacitor connected in series from the mirror current to the output of the first stage of the amplifier, the gain issue of the overall gain of the linear regulator is solved. The amplifier shown on Fig. 3.9 is the final design. It provides a gain of 54.42 dB with a phase margin of 36.94 ° which is adequate for the final linear regulator.

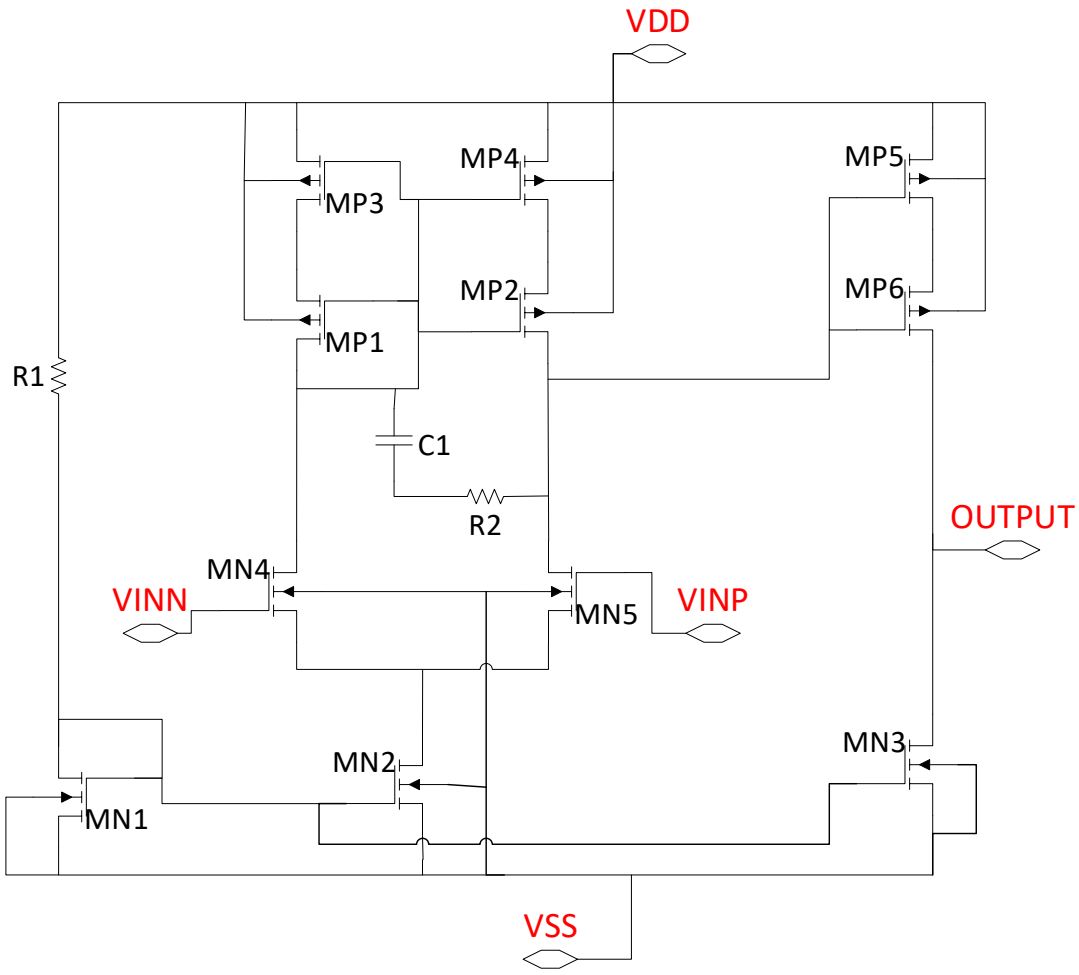

Fig. 3.9. Final 2-stage amplifier schematic.

3.2 Pass Element

Table 3.3 shows the various structures that could be used as pass elements for a linear regulator. It compares them looking at maximum output current, quiescent/ground current, dropout voltage, and speed of every pass device. Since the application of the regulator designed entails a low current usage, MOSFETs are preferred. The PMOS structure offers the best dropout voltage, and it also provides a higher speed compared to the NMOS. Therefore, a PMOS structure is selected as a pass element for the application.

Table 3.3. Pass Element Structures Comparison

Parameter	Darlington	NPN	PNP	NMOS	PMOS
I_o, max	High	High	High	Medium	Medium
I_q	Medium	Medium	Large	Low	Low
$V_{dropout}$	Vsat+2Vbe	Vsat + Vbe	Vce (sat)	Vsat + Vgs	VSD (sat)
Speed	Fast	Fast	Fast	Slow	Medium

3.3 Feedback Network

The feedback network is a simple voltage divider. The function of the network is to scale the voltage output voltage so that it is equal to the reference voltage. Then, the amplifier compares the scaled output voltage to the reference voltage to amplify the difference.

The easiest method to do a voltage divider to compare to the voltage reference is to make the output voltage half of what it is supposed to be. Consequently, a voltage divider was made repeating the same resistor. In this way, the output voltage will be half of the output voltage, which in this case is 600 mV. The following equation was used to calculate the feedback network

$$V_{feedback} = V_{out}\frac{R_2}{R_1 + R_2}$$

for the same resistor ($R_1 = R_2$)

$$V_{feedback} = V_{out}\frac{R_1}{R_1 + R_1} = V_{out}\frac{R_1}{2R_1}$$

$$V_{feedback} = \frac{V_{out}}{2}$$

A parametric simulation was used to obtain the best values for the resistors considering the DC gain and phase margin (Fig. 3.10). From the plots it can be observed that at 100 kΩ the phase margin and gain make a combination that is stable for both gain and phase. The phase is at 73.2 º, while the gain is about 70 dB. These two values continue to be approximately the same with higher resistance values. Nevertheless, incrementing the resistance would also increment the current employed by the complete circuit. Hence, 100 kΩ still is the best option for the voltage divider to be stable.

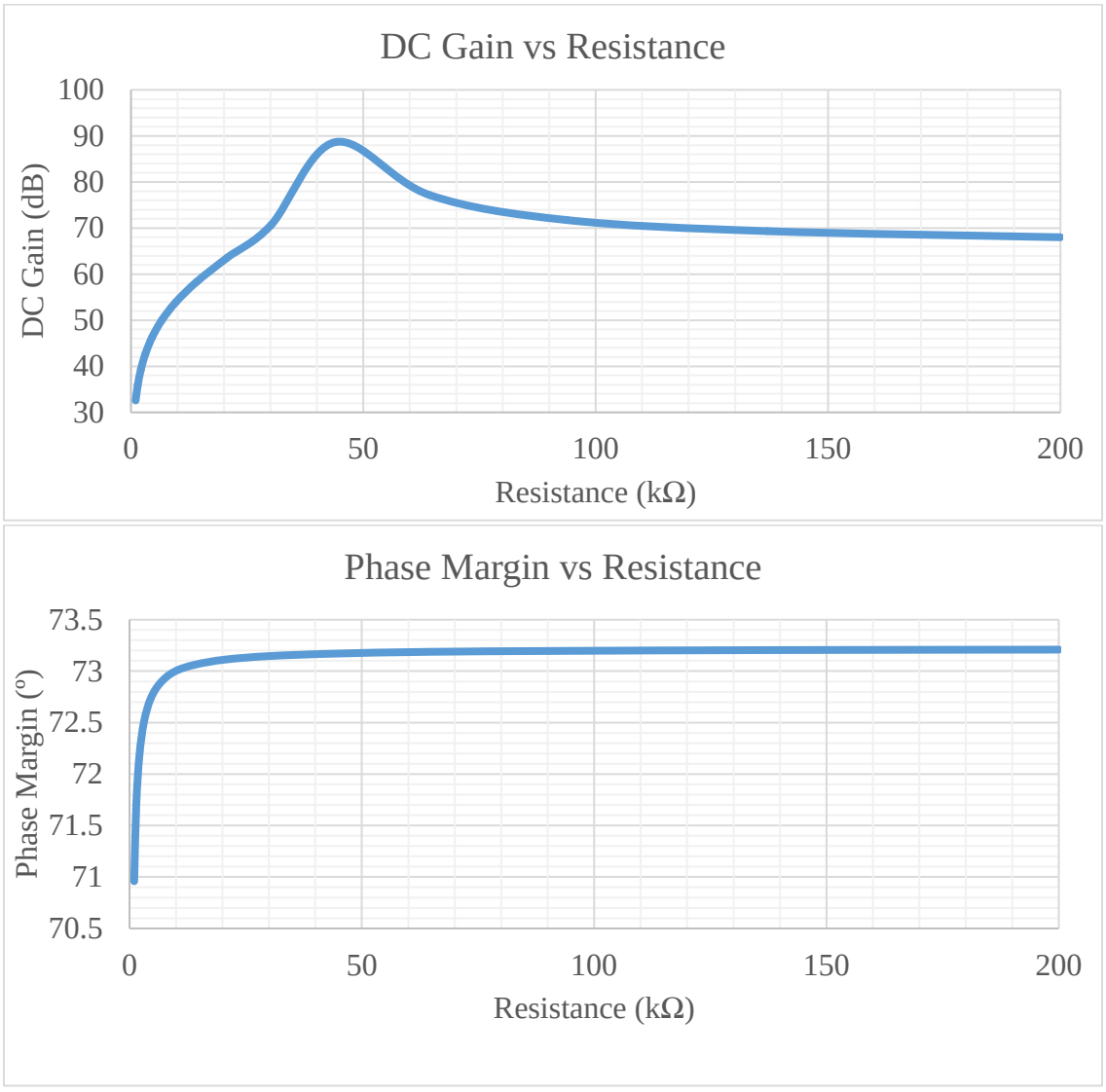

Fig. 3.10. DC gain and phase margin for resistor values on feedback network.

3.4 Voltage Reference

The voltage reference is used to compare the scaled output voltage. For this circuit, a reference voltage has been already designed, and it is 1.25 V. Since it is already known that the scaled output from the feedback network is 600 mV, it is necessary to scale the reference voltage to the same voltage. Hence, a voltage divider is also useful in this situation. Assuming one of the resistors is 100 kΩ the solution for the other resistor would be

$$V_{amp} = V_{ref}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$V_{amp}(R_1 + R_2) = V_{ref}(R_2)$$

$$R_1 = \frac{V_{ref}(R_2)}{V_{amp}} - R_2$$

Where the existing reference voltage (V_{ref}) is 1.25 V, R_2 is 100 kΩ, and the reference input to the amplifier, V_{amp}, is 600 mV. Hence, the resulting R_1 is 108.3 kΩ. Fig. 3.11 provides a diagram of the voltage divider that will be connected to the amplifier.

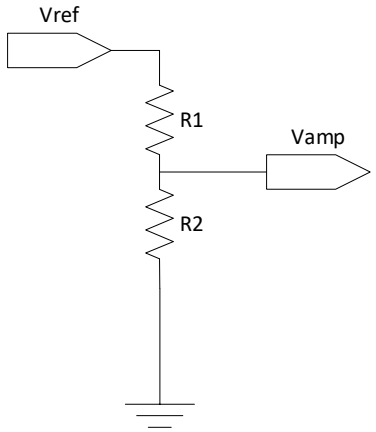

Fig. 3.11. Voltage divider for reference voltage.

3.5 Load Capacitor

The load capacitance is placed at the output of the linear regulator. It helps to stabilize the loop of the circuit. Because linear regulators need hundreds of nanoseconds to a few microseconds to respond, the load capacitor supplies the system with current temporarily [1]. The gain and phase margin in Fig. 3.13 were utilized to obtain a good fit for the linear regulator. A simulation was run from 1 µF to 5 µF and the gain stayed almost the same for all values. As it is expected, the load capacitor varies with the phase. The lower the capacitor is, the higher the phase and nearer to 90º which is best. Also, the smaller the capacitor the less area it takes which benefits the application. A 2 µF capacitor is used for the application, since it accomplishes all the requirements.

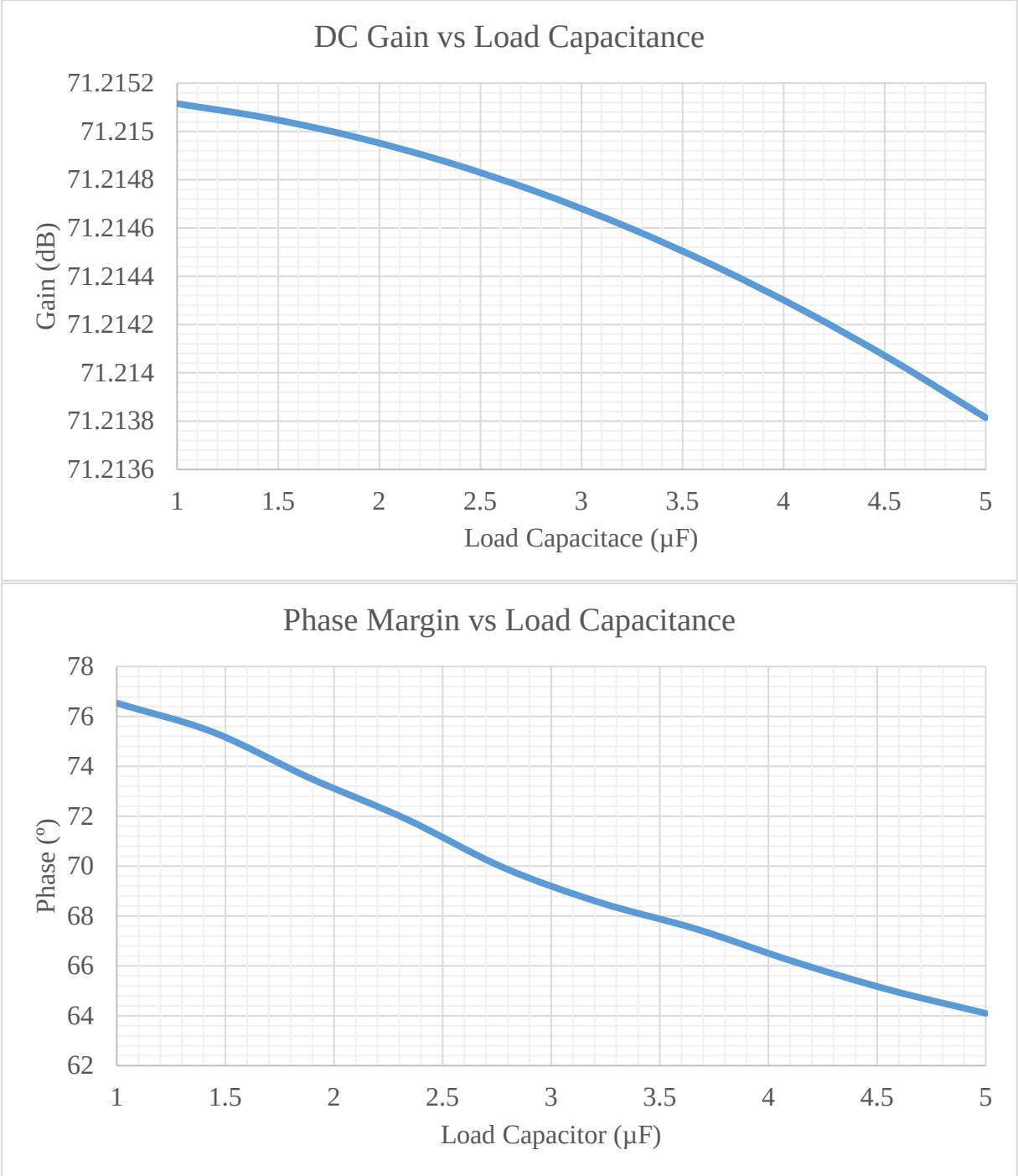

Fig. 3.12. DC gain and phase margin varying load capacitor.

3.6 Reverse-Battery Protection

The purpose is to shield the regulator from the effects of continuous reverse-battery circumstances. This kind of protection either shunts current away from the regulator circuit or blocks it. For the linear regulator designed, an NMOS transistor is the most adequate option. The source is connected to the ground of the battery, and the drain is connected to the ground of the circuit. The gate is connected to the positive of the battery or the input voltage of the circuit. In that way, with the gate being always high, the transistor will always be connecting the grounds. If the battery is connected in reverse, the NMOS transistor will never turn-on because its gate is connected to ground.

3.7 Circuit Schematic

The resulting circuit after designing all the blocks is on Fig. 3.14. It consists of the error amplifier, PFET pass element, feedback network, voltage reference, and reverse-battery protection. This schematic contains everything that was fabricated after the layout step.

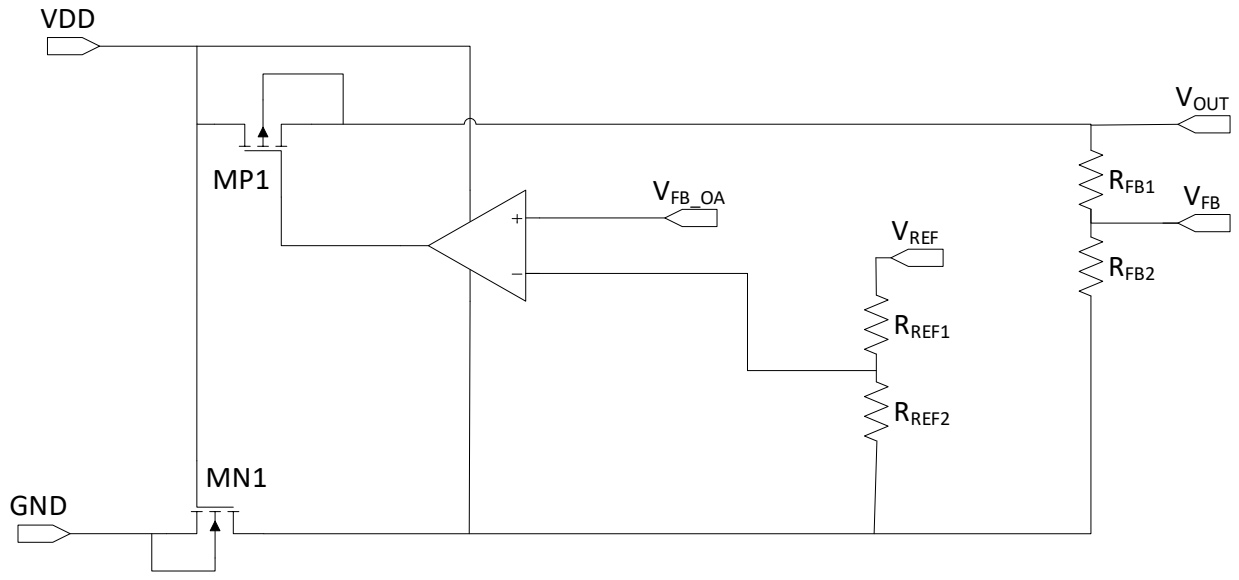

Fig. 3.13 Complete linear regulator schematic.

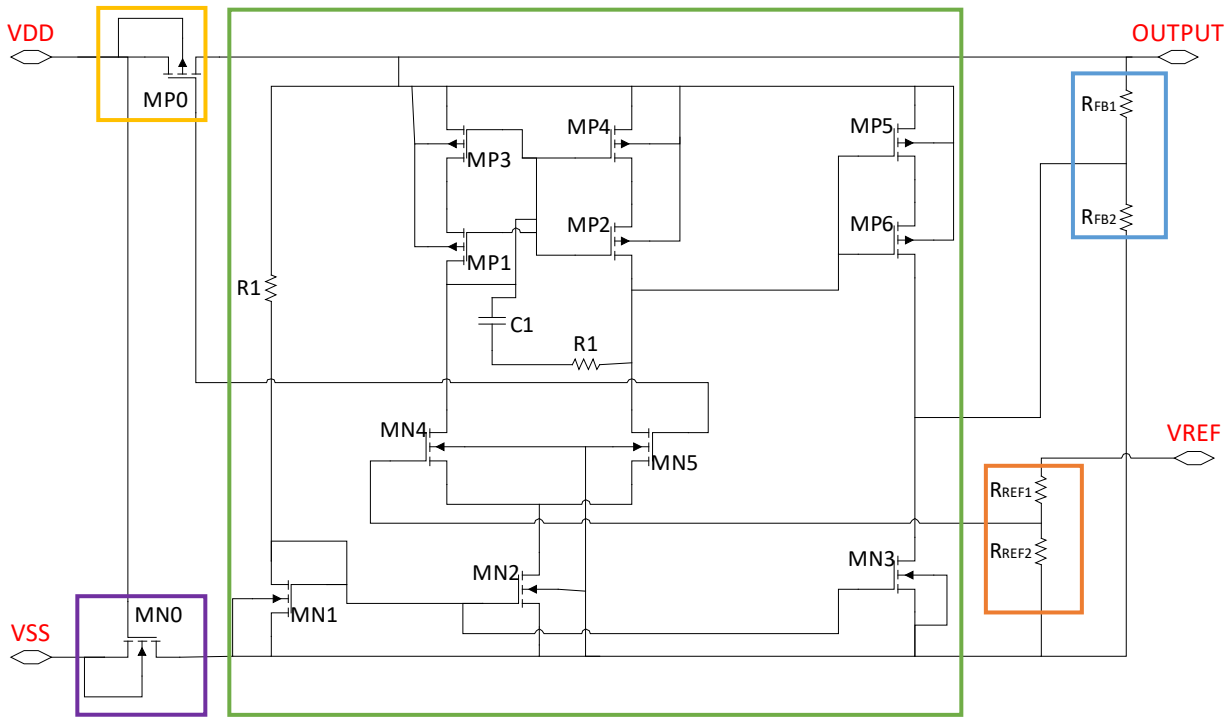

Fig. 3.14 Transistor level schematic of the linear regulator.

The transistor level representation of the regulator is shown on Fig. 3.15. Inside the green square there is the two-stage amplifier. The blue square encloses the voltage divider that makes up the feedback network. The circuit to scale the reference voltage is inside the orange square. The yellow square is the pass PMOS transistor, and the purple square has the NMOS transistor that performs the reverse-battery protection. Table 3.4 shows the device sizes for the parts that comprise the linear regulator.

Table 3.4 Device Sizes

Component	Device Size
MN0	10 µm/0.26 µm (m=10)
MN1- MN2	16 µm /0.26 µm (m=1)
MN3-MN5	8 µm /0.26 µm (m=1)
MP0	100 µm /0.26 µm (m=10)
MP1-MP6	64 µm /0.26 µm (m=1)
RFB1	100 kΩ
RFB2	100 kΩ
RREF1	108 kΩ
RREF2	100 kΩ
R1	125 kΩ
C1	20 pF

3.8 Circuit Layout

The area of the device is 216 µm by 132 µm including the capacitor of the amplifier, C1. The shape of the device is a rectangle to make it easier to fit in the whole layout of the system. The layout of C1 takes more than three fourths of the whole layout area. This is one of the reasons for the load capacitor not being part of the layout and having to be off-the-shelf. The layout is shown in Fig. 3.15.

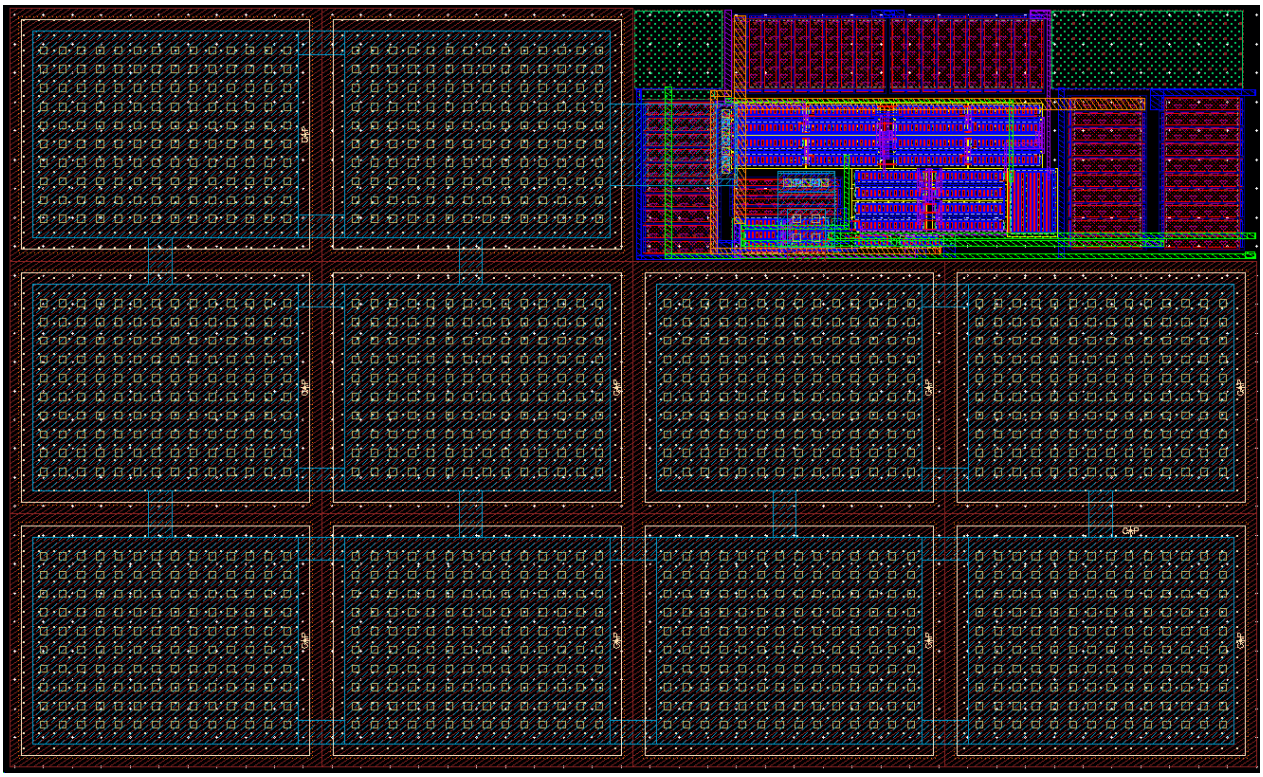

Fig. 3.15. Linear regulator layout

Common-centroid layout technique was implemented to improve the matching in the MOSFETs [11]. The process kit has seven metal layers that can be used in addition to poly, making it easier to connect the blocks of the system together. The layers were used starting from the smallest size to the largest. The first layout to be drawn was the amplifier. Because it is composed of many MOSFETs, it was preferred to use the poly layer to connect the gates of the MOSFETs. Metal one (M1) is used to make all horizontal connections, while metal two (M2) connects any vertical connection in the amplifier. By choosing two different metals for this part of the layout, there is less chance for connection errors, and the circuit becomes more compact.

CHAPTER 4 : TESTING AND CHARACTERIZATION

This chapter explains the simulations performed in order to design the linear regulator described in Chapter 3. All the simulations were carried using Cadence Virtuoso ® Custom IC Design Environment, version IC6.17-64b.500.19. In addition, this chapter presents the tested results and compares them with the simulations. Line regulation, load regulation, dropout voltage, quiescent current and power supply rejection ratio results are described in detail.

The SiGe CMOS linear voltage regulator layout along with other designs for the DCIC (Fig 4.1) first run was sent to the MOSIS Service on June 10, 2018.

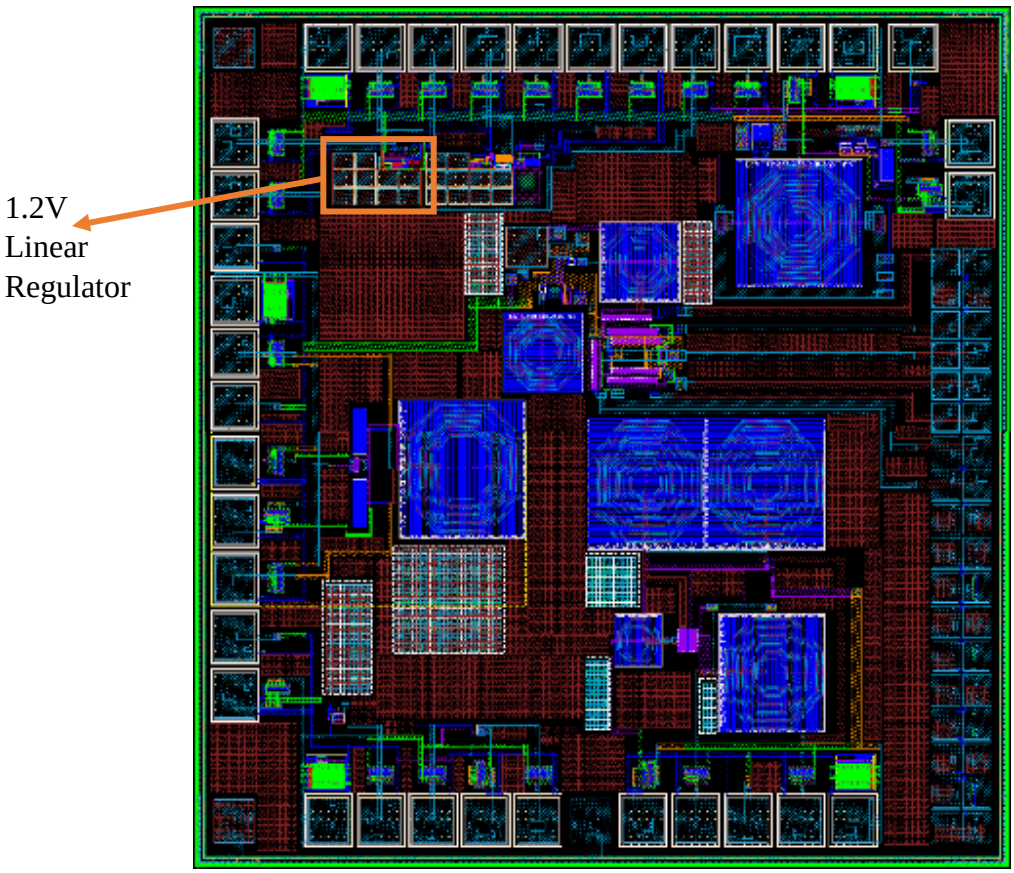

Fig. 4.1. Complete layout for the first DCIC run.

The linear regulator was fabricated in a BiCMOS SiGe 0.13µm GlobalFoundries process. The chip area was 2 mm x 2 mm including pads. On December13, 2018 the die was received. It was packaged on a 48-lead quad flat no-lead (QFN).

A printed circuit board (PCB) was designed in order to simplify the testing. Gerber files and drill files were created after designing the layout with Allegro PCB Editor from Cadence version 17.2. The layout designed is shown on Fig. 4.2 and it was sent for fabrication to PCBWay.

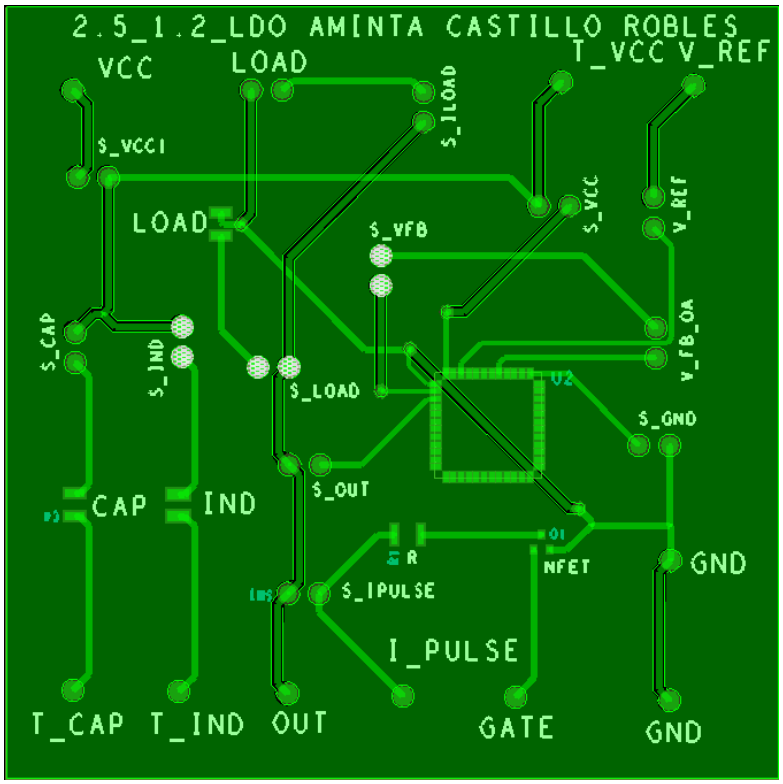

Fig. 4.2. PCB layout.

The soldered PCB with its parts is shown on Fig 4.3. Since the purpose of this regulator is to be used in agriculture, it was only tested at room temperature and up to 85 ºC.

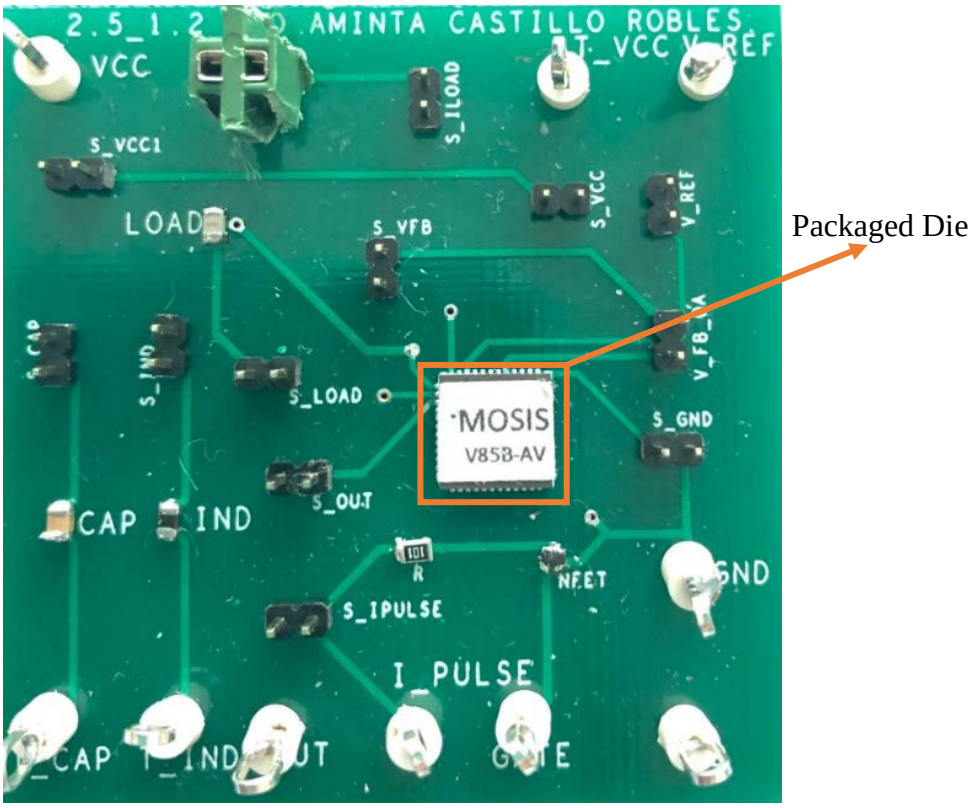

Fig. 4.3. Soldered PCB for testing.

Therefore, the results of simulations and tests are not needed to be exposed to hot plates or temperatures other than 25 ºC. The supplies and measuring equipment used are shown in Table 4.1.

Table 4.1 Instrumentation for Measurements

Instrument	**Brand**
DC Voltage Supply	Rigol DP832
AC Voltage Supply	Tektronix AFG 3022B
Oscilloscope	Tektronix MSO 4104
SourceMeter	2602B Keithley

4.1 Line Regulation and Load Regulation

The schematic for the line and load regulation tests is shown on Fig 4.4. The input voltage was connected to the VDD terminal of the regulator and varied from 1.7 V to 2.7 V to confirm line regulation.

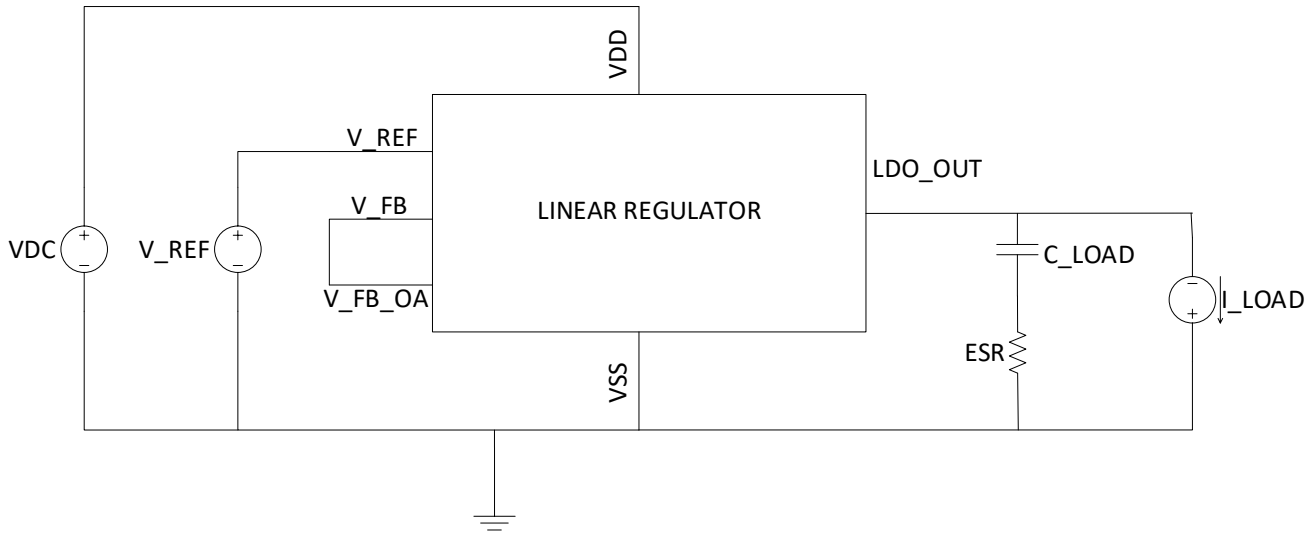

Fig. 4.4. Testbench for line and load regulation.

The load current was connected to the LDO_OUT terminal and varied from 0 mA to 20 mA to evaluate the load regulation. The reference voltage was 1.25 V and the load capacitor 2 µF. Simulation parameters are summarized in Table 4.2.

Table 4.2. Parameters for Line and Load Regulation Measurement

Parameter	Value
Input Voltage	2.3 V to 5.0 V
Reference Voltage	1.25 V
Load Current	8 mA to 20 mA
Load Capacitor	2.0 µF

4.1.1 Line Regulation

As was explained in Chapter 2, line regulation is the change between the output voltage and input voltage. The comparison between measured and simulated results is shown in Fig. 4.5. A load of 8 mA is the load expected from the PA and LNA. Line regulation starts occurring with a voltage as low as 1.9 V, and holds up to 2.7 V under this load conditions. Therefore, it regulates at the required specified voltage 2.5 V proving a good margin for lower and higher voltages. For a 2.5 V input, the output is 1.184 V.

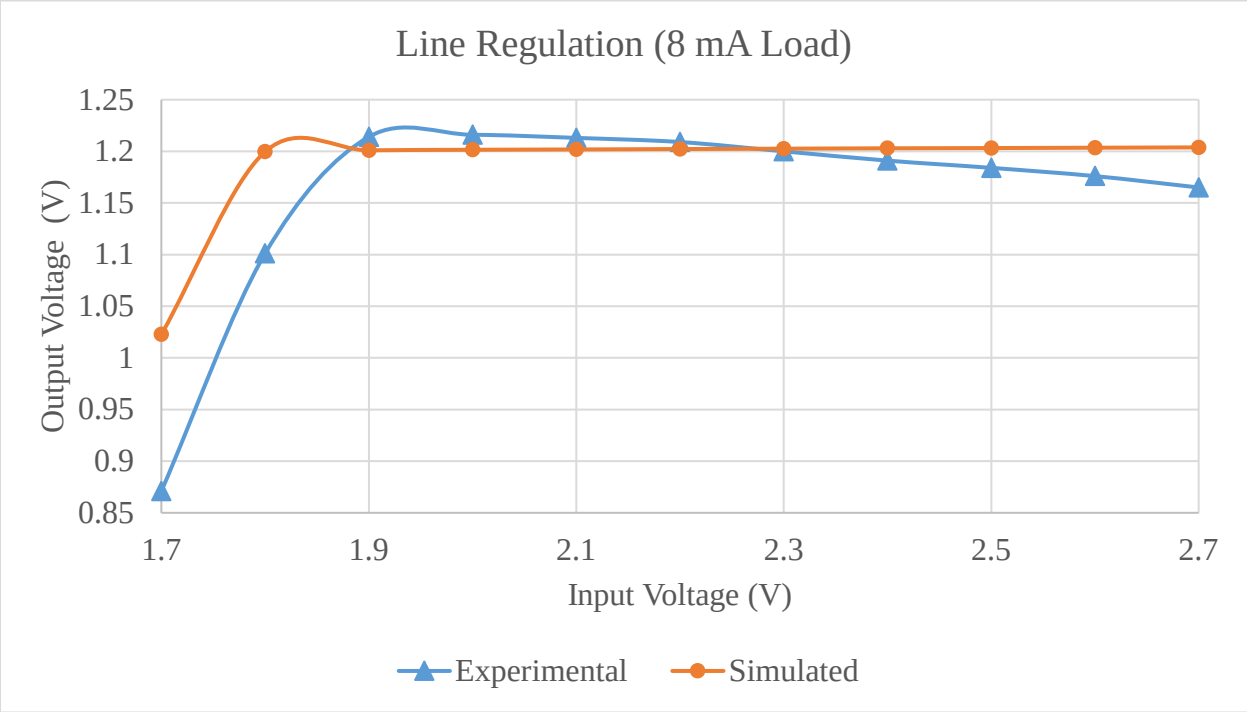

Fig. 4.5. Simulated and experimental line regulation results for 8 mA load.

Since there is a chance of having a scenario where the 8 mA load specification is exceeded, simulation and testing were performed with a 15 mA load (Fig. 4.6). In this scenario, line regulation starts at 2.2 V for simulated results and 2.4 V for the measured result. For the worst-case scenario of current load, the output voltage for a 2.5 V input is 1.208 V. In addition, the linear regulator still line regulates up to a 2.7 V input.

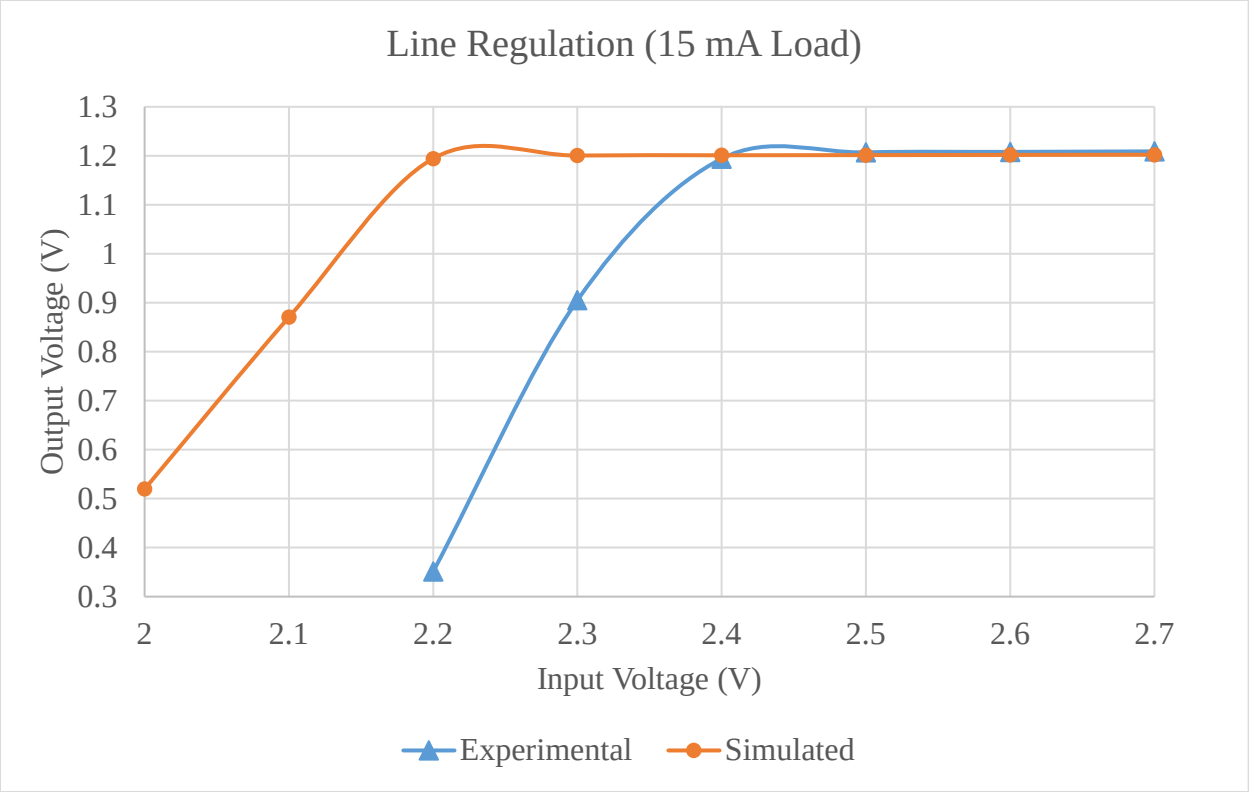

Fig. 4.6. Simulated and experimental line regulation results for 15 mA load.

4.1.2 Load Regulation

Load regulation is the relationship between the load current and the output voltage. Simulation and measured results for the 2.5 V specification are displayed in Fig. 4.7. As the plot shows, when there is no load the output is 1.2 V and it stops regulating after 16 mA for testing. It maintains an output of 1.218 V throughout the test.

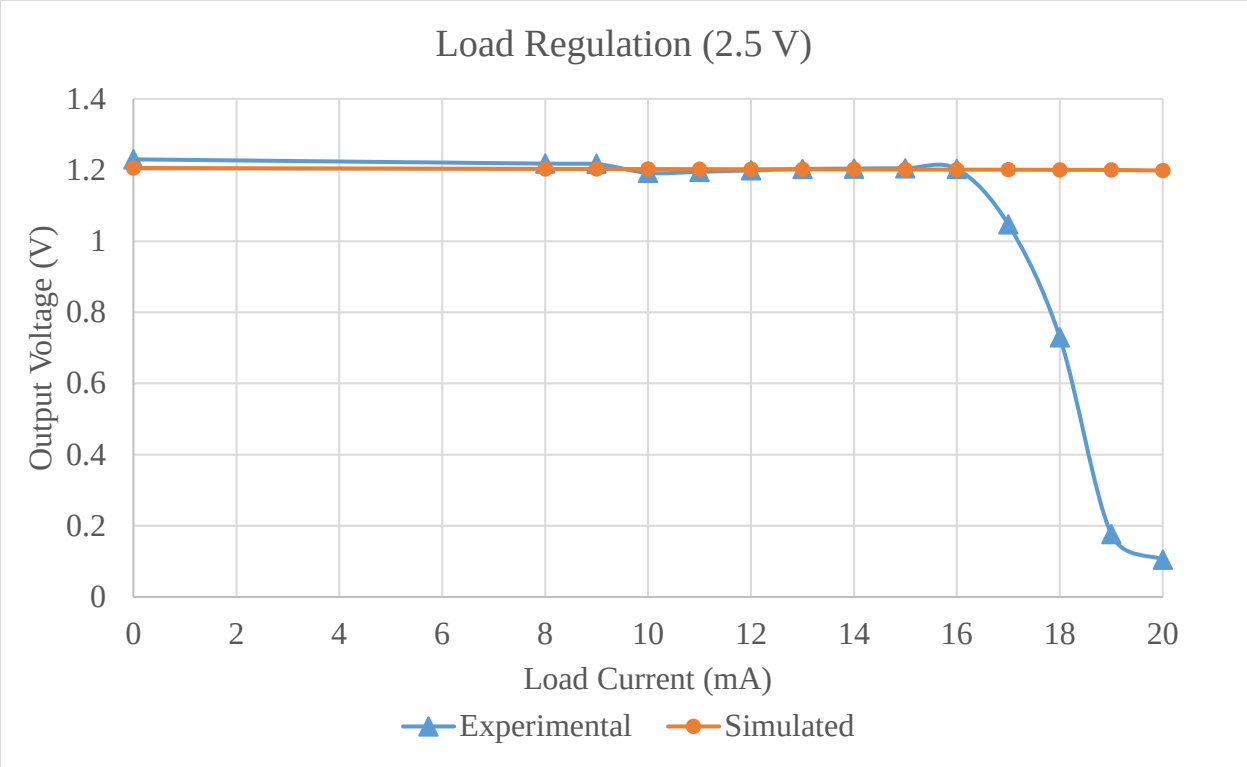

Fig. 4.7. Simulated and experimental load regulation results for a 2.5 V input voltage.

Since the battery will be discharging with time, the input voltage to the linear regulator is likely to decrease with time. Therefore, it was pertinent to simulate and test for that case. A 2.2 V input was simulated maintaining a constant 1.2 V output across different loads. This same case was measured, and the load is regulated from 0 mA up to 13 mA. The output is held at 1.170 V. The simulated and experimental results for this scenario are shown on Fig. 4.8.

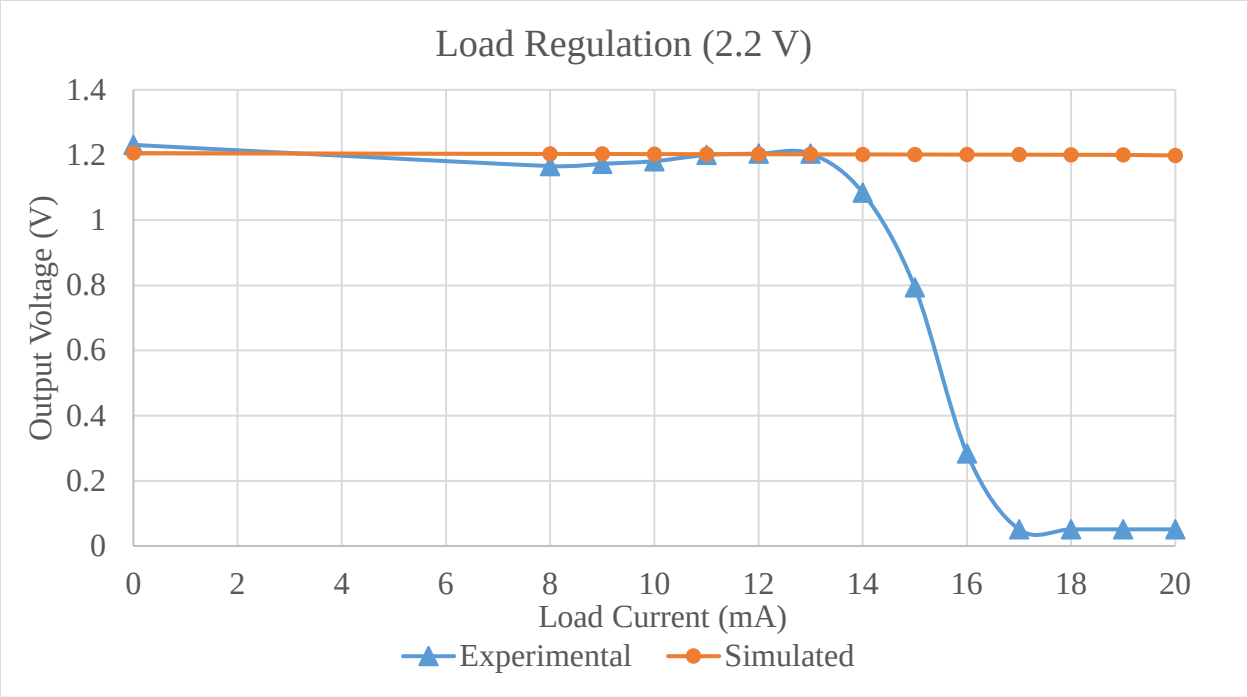

Fig. 4.8. Simulated and experimental load regulation results for 2.2 V input voltage.

The load regulation differs from the simulation results because of voltage drops occurring in the current paths. One solution to improve load regulation is to connect the regulator ground to the negative load terminal. In this way, only this current flows removing voltage drops from other currents. In addition, placing the IC regulator as near to the load as possible having a maximum possible conductor thickness to the positive connector of the load will minimize the drop in the positive lead [15].

The percentage error for load and line regulation is calculated using Eq. (4.1). The theoretical value is the one obtained through simulation while the experimental was obtained by testing the die on the board. As shown on Table 4.3, the percentage error is minimum. It is less than 3% for both best and worst case scenarios of line and load regulation.

$$Percentage\ Error = \left|\frac{Theoretical - Experimental}{Theoretical}\right| * 100\% \quad (4.1)$$

Table 4.3. Percent Error for Line Regulation and Load Regulation Output Voltage

	Test Condition	Theoretical Output (V)	Experimental Output (V)	Percent Error (%)
Line Regulation	8 mA Load	1.2	1.184	1.33
	15 mA Load	1.2	1.207	0.58
Load Regulation	2.5 V Input	1.2	1.218	1.5
	2.2 V Input	1.2	1.170	2.6

Line regulation and load regulation calculations were described by equations Eqs. (2.5) and (2.6) respectively. Since data sheets describe regulation with percentage, results are shown as percentages in Table 4.4.

Table 4.4. Calculation of Line and Load Regulation

	Condition	Simulation (%)	Measured (%)
Line Regulation	8 mA	0.45	5.00
	15 mA	0.4	1.00
Load Regulation	2.5 V	0.03	0.19
	2.2 V	0.03	0.76

4.2 Dropout Voltage

The dropout voltage is one of the most important measurements for a regulator. Below the dropout voltage, the regulator is not functional. In other words, the dropout voltage is the point where the regulator starts regulating. As shown in Fig. 4.9, the dropout voltage is 1.206 V since after that point, the output voltage stays constant. Measurements are taking with no load.

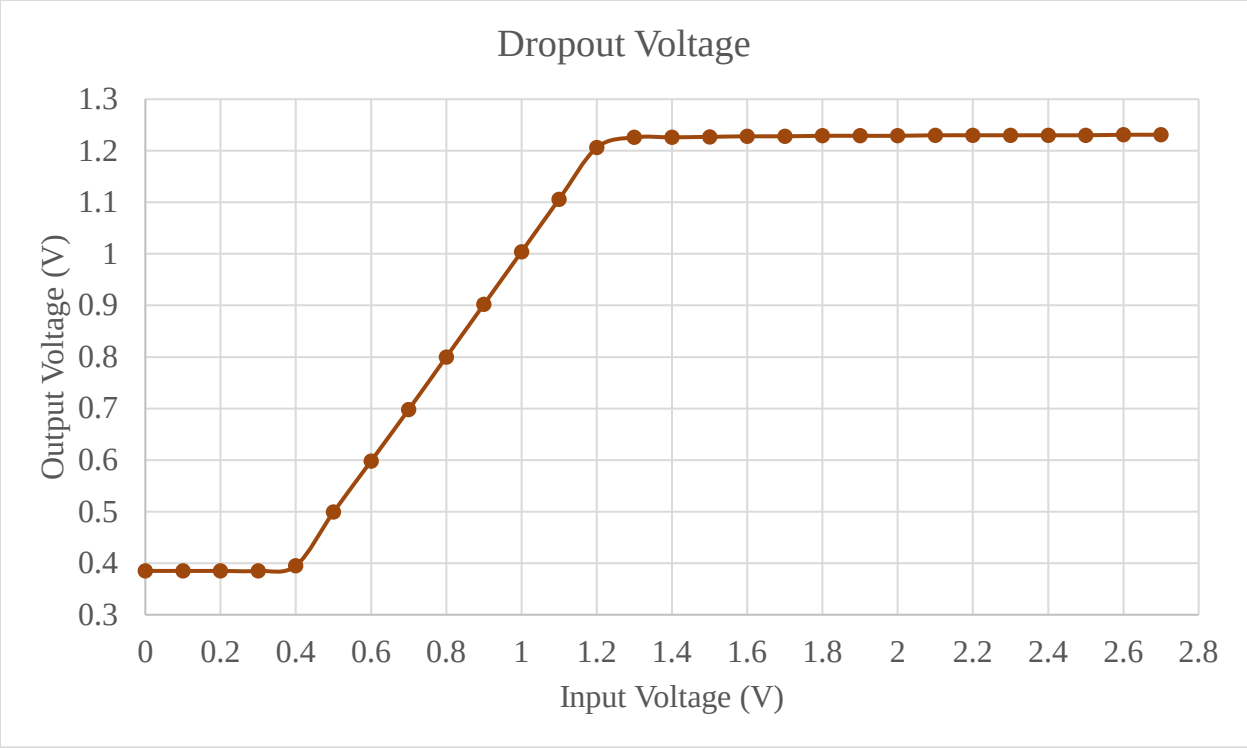

Fig. 4.9. Dropout voltage.

4.3 Quiescent Current

The quiescent current depending on the input voltage was simulated and measured (Fig. 4.10). As it is expected from a general quiescent current measurement, there is no load current at the output for this measurement. All the current travels directly to the ground of the device. The quiescent current measures the current necessary for the circuit to perform its most basic functions [16]. In the case of the linear regulator, it is to provide the expected output.

The quiescent current increases progressively as the input voltage does. The quiescent current for 2.5 V is 128 µA which is a bit over the expected value for the specification. According to the simulation, the quiescent current should have been 63 µA, which is half of what was measured. Even though the quiescent current measured is above the specification, it is still considered a low quiescent current for optimized regulators (75 µA to 150 µA) improving significantly in comparison with typical regulators which draw several milliamps [15].

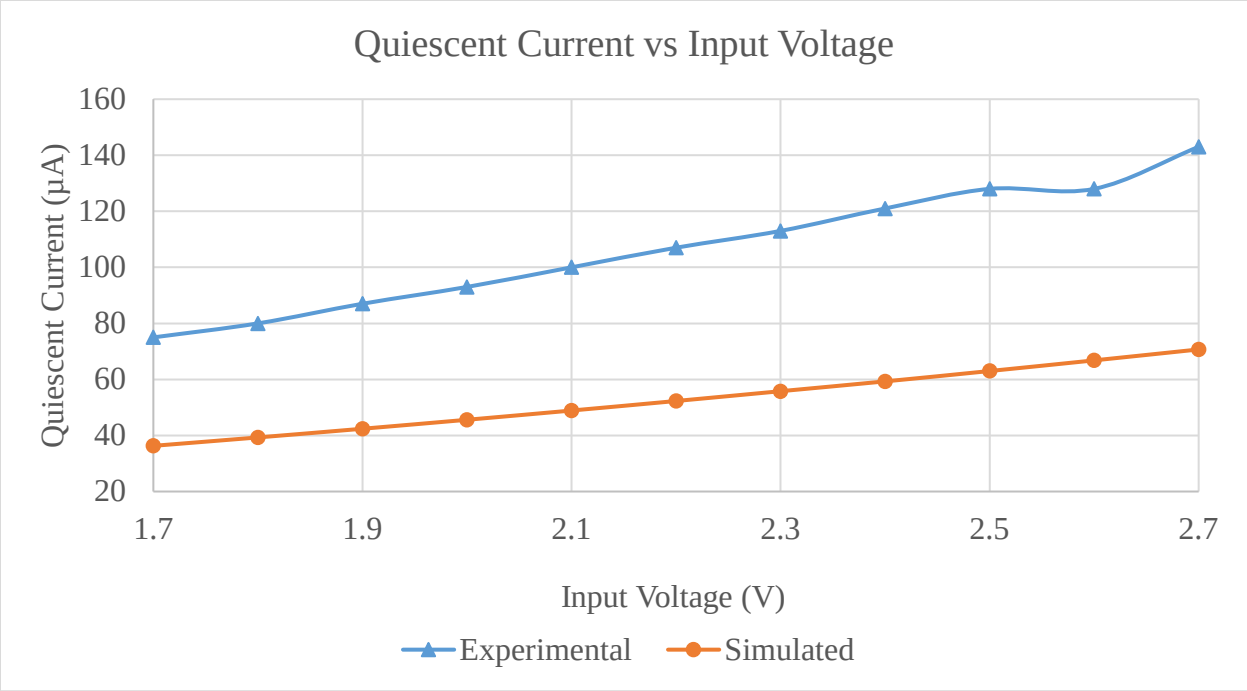

Fig. 4.10. Quiescent current vs input voltage.

4.4 Power Supply Rejection Ratio

To effectively measure PSRR it is necessary to add a ripple to the input of the regulator to later measure the output ripple. There is a variety of methods to measure the PSRR of a linear regulator. The LC summing node method is the most basic and most used for mid-ranged frequencies. It consists of adding an AC voltage supply or signal generator to the input of the linear regulator. Because the signal generator has a high impedance, it cannot directly be connected in series with the DC supply. It would obstruct the DC current through the regulator to power the output.

The solution is to add an inductor in series with the AC generator, and a capacitor in series with the DC generator as shown in Fig. 4.11. In this way, the AC generator is not shunting down the DC supply and the DC supply is not shorting out the AC supply [17]. The node becomes a summing node at the input of the linear regulator providing a ripple that will be then seen at the output.

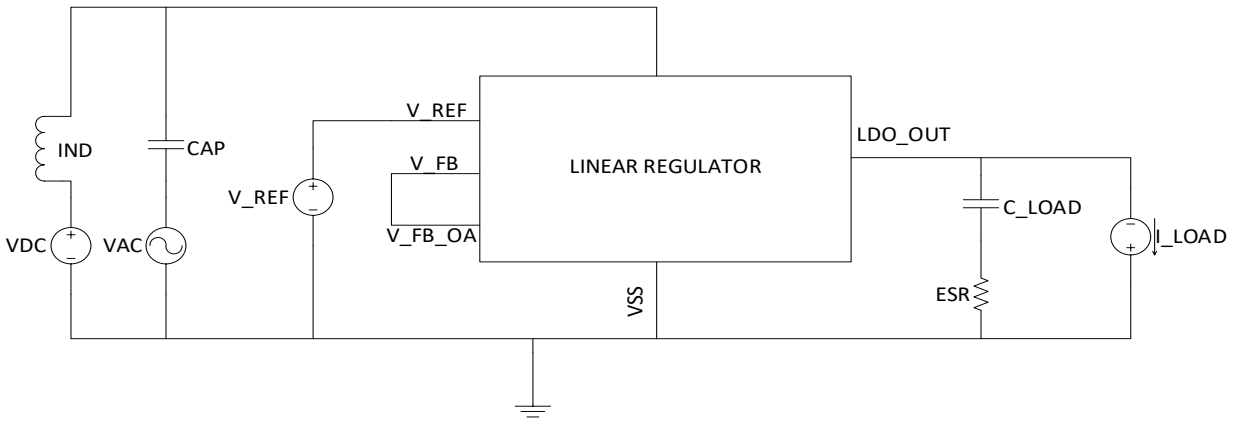

Fig. 4.11. Testbench for line and load regulation.

For this measurement the signal regulator is set to a sinusoidal voltage of 400 mV peak-to-peak at 100 kHz of frequency. The inductor in series has a value of 100 µH and the DC supply is 2.5 V in series with a 100 µF capacitor. The rest of the testbench continues to be the same as for the line and load regulation measurement. As shown in Table 4.2, the load current was 8 mA, the reference voltage 1.25 V, and the load capacitor 2.0 µF.

Table 4.5. Parameters for Power Supply Rejection Ratio Measurement

Parameter	Value
Input Voltage	AC: 400 mV at 100 kHz
	DC: 2.5 V
Reference Voltage	1.25 V
Load Current	8 mA
Load Capacitor	2.0 µF

For simulation purposes the testbench had some modifications. Since it becomes necessary to simulate the impedance of the capacitor and the inductor, resistances are placed as substitutes. The impedance of a capacitor is described by the equation 4.2. According with the equation, as frequency approaches zero (DC voltage), the resistance approaches infinity. When the frequency reaches a high value of frequency (AC voltage), the resistance approaches zero. Therefore, a very low resistance, 1 kΩ, is placed in series with the AC voltage source.

$$X_C = \frac{1}{2\pi fC} \tag{4.2}$$

The impedance of an inductor is described in Eq. (4.3). The impedance in this case is directly proportional to the frequency. Consequently, at frequencies approaching zero, the resistance becomes zero; and as frequencies reach infinity, the impedance does too. For this reason, a high resistance would block the AC voltage supply. Then, a resistor of 1 GΩ is in series with the DC voltage source.

$$X_L = 2\pi fL \tag{4.3}$$

With the purpose of studying the PSRR of the device designed, a simulation was run using the testbench described. The input had a DC voltage of 2.5 V and an AC voltage of 400 mV at 100 kHz. The output was measured and the ripple at the input and output are shown in Fig. 4.12. Eq. (2.7) was used to calculate this value as shown in Chapter 2. The PSRR was calculated and it is 43.49 dB as follows.

$$PSRR_{sim} = 20\ log\frac{V_{o,ripple}}{V_{i,ripple}} = 20\ log\frac{400\ mV}{3\ mV} = 43.49\ dB$$

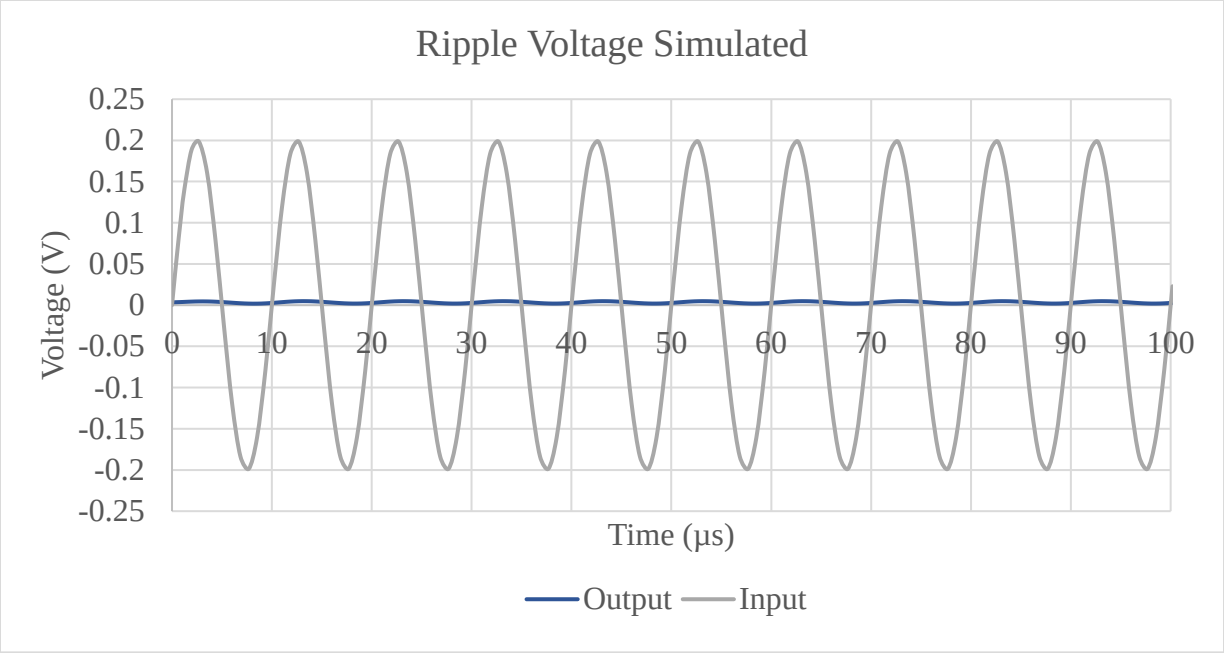

Fig. 4.12. Power supply rejection ratio simulation.

The experimental results were measured using the designed linear regulator and the response is shown in Fig. 4.13. The calculated PSRR is 28.51 dB. Again, Eq. 2.7 was used to calculate this value.

$$PSRR_{measured} = 20\ log \frac{V_{o,ripple}}{V_{i,ripple}} = 20\ log \frac{400mV}{15\ mV} = 28.51\ dB$$

4.5 Temperature Testing

In addition to testing at room temperature, the device was also tested at 85 ºC which is the highest for some manufacturer's commercial standards. The PCB is located on a hotplate at 85 ºC. The results measured are shown in Table 4.6.

Table 4.6 Output Voltage over Temperature

Input Voltage (V)	Load (mA)	Output (V)
2.5	8	1.103
	15	1.195
2.2	8	1.182

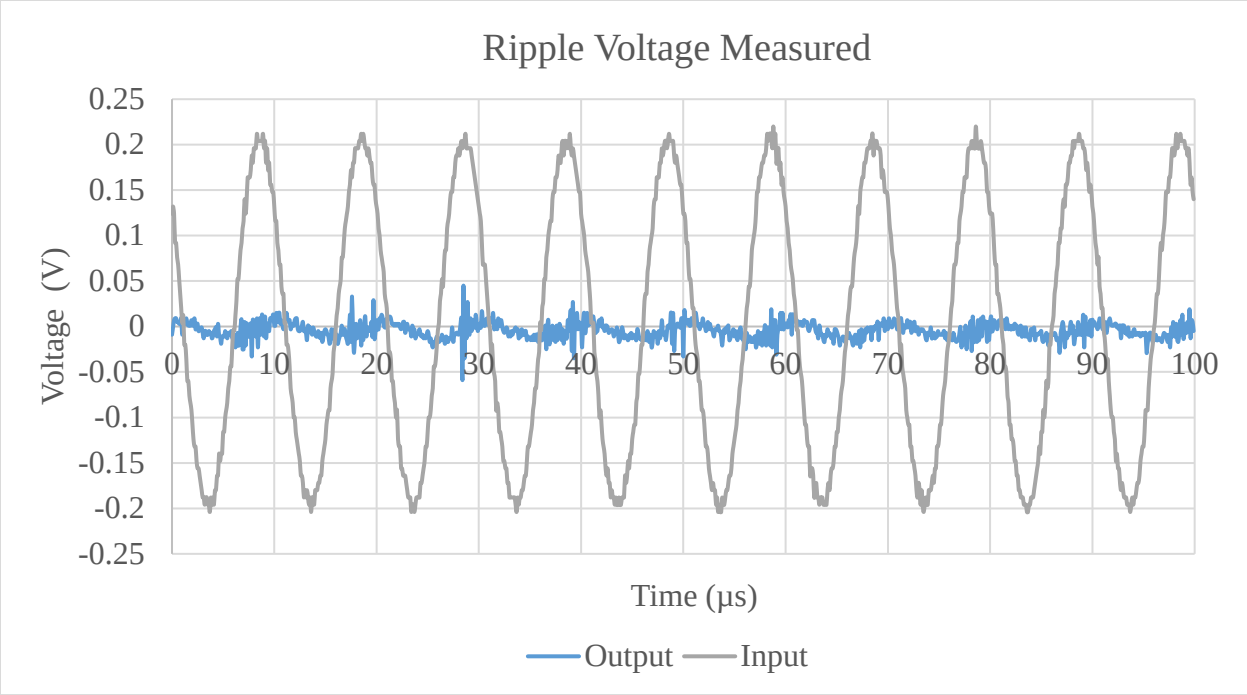

Fig. 4.13. Power supply rejection ratio measured.

After performing all the data analysis of simulated and measured results, the outcomes are presented in Table 4.7. The general conditions were a capacitive load of 2 µF, reference voltage of 1.25 V, input voltage of 2.5V, and load current of 8 mA. The input ripple was 400 mV at 100 kHz for PSRR calculation, and the quiescent current was taken with a 0 mA load.

Table 4.7. Comparison of Simulated and Measured Results

Specification	Parameter	Simulated	Measured	Units
V_{IN}	Input Voltage Range	2.5	2.5	V
V_{OUT}	Output Voltage	1.20	1.21	V
V_{REF}	Reference Voltage	1.25	1.25	V
$\Delta V_{OUT(\Delta VIN)}$	Line Regulation	0.45	5.00	%
$\Delta V_{OUT(\Delta IOUT)}$	Load Regulation	0.03	0.19	%
V_{DO}	Dropout Voltage	1.278	1.206	V
I_{CL}	Output Current Limit	19	16	mA
I_Q	Quiescent Current	63	128	µA
PSRR	Power Supply Rejection Ratio	43.5	28.5	dB

4.6 Comparison with Commercial Linear Voltage Regulator

The designed linear regulator is compared with a commercial regulator. Since there is not a regulator that has the same specifications, it is easier to compare to the closest one which is the LP 3893 from Texas Instruments. It is a high current, fast-response regulator fabricated in a CMOS process. Different to the designed regulator, this one operates with two voltages, a V_{BIAS} that provides the gate to the pass transistor and a V_{IN} that is the input that supplies the power to the load. The output is 1.2 V, V_{BIAS} is 2.3 V, I_{LOAD} is 10 mA, and the C_{OUT} is 10 µF. There is no reference voltage, since the structure of the device is different, so it is not required. The two devices are compared in Table 4.8.

Table 4.8. Comparison with a Commercial Linear Voltage Regulator

Specification	Parameter	Measured	LP3893	Units
V_{IN}	Input Voltage Range	2.5	2.3	V
V_{OUT}	Output Voltage	1.218	1.216	V
V_{REF}	Reference Voltage	1.25	----	V
$\Delta V_{OUT(\Delta VIN)}$	Line Regulation	5.0	0.01	%
$\Delta V_{OUT(\Delta IOUT)}$	Load Regulation	0.19	0.06	%
V_{DO}	Dropout Voltage	1.206 V	270 mV	-----
I_Q	Quiescent Current	128 µA	3 mA	-----
PSRR	Power Supply Rejection Ratio	28.5	23.0	dB

CHAPTER 5 : CONCLUSION

This thesis has covered the design of a CMOS linear regulator in a SiGe process technology. After simulations to confirm the specifications were accomplished, the circuit was sent to fabrication. Once back it was tested using the designed test board and the results were studied. A comparison between simulated and measured results was performed. Finally, the device was compared to a commercial silicon linear regulator.

The linear regulator was tested, and it proved to hold an output of 1.2 V with an error between measured and simulated of less 3 %. It regulates load currents up to 15 mA. Also, it shows good performance with an input voltage of 2.5 V and lower voltages like 2.2 V. Line regulation was met at 5 % and load regulation at 0.19 %. The Power Supply Rejection Ratio was calculated for a frequency of 100 k Hz. The device works at room temperature as well as 85 ºC using a hotplate. The results of the linear are compared with commercial off-the-shelf linear regulators.

Future work for this linear regulator will include an improvement on the quiescent current results. Even though the measurement was not too distant from the specification, it could be improved. The dropout voltage is sufficient for the application. However, it should be minimized, since for a lower input voltage and a higher ripple at the input, the rejection of the supply could be disturbed.

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