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A Wide Bandgap Silicon Carbide (SiC) Gate Driver for
High Temperature, High Voltage, and High Frequency Applications

A Wide Bandgap Silicon Carbide (SiC) Gate Driver for High Temperature, High Voltage, and High Frequency Applications

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

by

Ranjan R. Lamichhane
Tribhuvan University
Bachelor of Electronics and Communications Engineering, 2010

December 2013
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

_____
Dr. H. Alan Mantooth
Thesis Director

_____
Dr. Randy Brown
Committee Member

_____
Dr. Jia Di
Committee Member

ABSTRACT

The potential of silicon carbide (SiC) for modern power electronics applications is revolutionary because of its superior material properties including substantially better breakdown voltage, power density, device leakage, thermal conductivity, and switching speed. Integration of gate driver circuitry on the same chip, or in the same package, as the power device would significantly reduce the parasitic inductance, require far less thermal management paraphernalia, reduce cost and size of the system, and result in more efficient and reliable electrical and thermal performance of the system.

The design of a gate driver circuit with good performance parameters in this completely new under-development SiC process is the key to realization of this ultimate goal of integrating a SiC gate driver with a SiC power MOSFET. The objective of this joint undertaking is integration of the designed gate driver into the electronic battery charger onboard the new plug-in hybrid Toyota Prius. The ultimate goal of the project is in-vehicle demonstration and commercialization. This high frequency charger will be five times more powerful with a 10 times size reduction and significant cost reduction on the long run.

This thesis presents the design, layout, simulation, testing and verification of a gate driver circuit implemented and fabricated in the Cree SiC process. The gate driver has a rise time and fall time of 45 ns and 41 ns, respectively, when driving a SiC power MOSFET with peak current reaching around 3 A. At a switching frequency of 500 kHz, the gate driver power dissipation was around 6.5 W. The gate driver was operable over a temperature range between 25 °C and 420 °C with only slight degradation in performance parameters. This thesis will provide a comprehensive overview of gate driver design and testing phases with relevant background.

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- Ranjan R. Lamichhane

DEDICATION

I dedicate this thesis to my parents Ram Krishna and Sumitra for their eternal unfaltering love, support, and nurture. You guys rock!

I also want to dedicate this thesis to my sisters Jyotsna and Samjhana, and my brother Rabindra for always caring for me and believing in me.

I want to extend my dedication to my friends who I can always count on to have fun and share the joys and sorrows.

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ADE	Cadence Analog Design Environment
APEI	Arkansas Power Electronics International
ARPA-E	Advanced Research Projects Agency - Energy
CMOS	Complementary Metal Oxide Semiconductors
CTE	Coefficient of Thermal Expansion
DRC	Design Rule Checking
ESD	Electrostatic Discharge
GaN	Gallium Nitride
GaAs	Gallium Arsenide
GPIB	General Purpose Interface Bus
HT	High Temperature
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor
ORNL	Oak Ridge National Labs
PCB	Printed Circuit Board
PDK	Process Development Kit
PHEV	Plug-In Hybrid Electric Vehicle
PMOS	P-type Metal Oxide Semiconductor
PWM	Pulse Width Modulation
RTL	Resistor Transistor Logic
SiC	Silicon Carbide

SOI	Silicon on Insulator
U of A	University of Arkansas
USB	Universal Serial Bus

1. INTRODUCTION

Silicon-Carbide (SiC) poses a lot of promise in the field of semiconductors because of its many advantages over silicon in numerous purposes. It has the potential to revolutionize power-electronics in much the same way silicon integrated circuits revolutionized computer systems; reducing power consumption, size, and cost of power electronic systems and enhancing their speed, portability, versatility, and efficiency, especially in high-voltage and high-temperature applications [1].

In order to drive a power MOSFET into and out of conduction (i.e. turn it 'on' or 'off') fast enough so that it can be used in high frequency applications and provide good signal fidelity, an efficient, reliable, and robust gate driver circuit is required. This circuit should be able to take a low voltage and low current input control signal, amplify its voltage, and produce a high-current drive output to control the gate of high-power transistors such as an IGBT or power MOSFET. The gate driver circuit might utilize a voltage level shifter and delay circuits to achieve the required voltage translation and to reduce any shoot-through current at the final stage to improve the rise/fall time of the output signal and reduce dynamic power dissipation, in addition to current buffer stages that increase the current drive at the output stage.

The gate driver presented in this thesis is built on SiC material to drive a SiC power MOSFET. The work includes circuit topology creation, schematic/layout design and simulation, debugging, and testing of a gate driver in SiC technology targeted for high temperature applications. Gate drivers are very important part of any switching power electronics that utilizes power MOSFET switching to achieve various tasks. A multitude of systems use a switching power MOSFET with applications including, but not limited to, power supplies, voltage

converters, motor controllers, industrial automation applications, x-ray tubes, communications equipment, aviation applications, manufacturing plants, data centers, automobiles, spacecraft, etc. This particular project is focused on integration of this gate driver into a Toyota Prius plug-in hybrid electric vehicle (PHEV) charger module. The application of this high frequency charger will result in a charger system with 5 times more output power, 10 times size reduction causing reduction in weight of the system as well, and substantial cost reduction on the long run [1], [2].

Power MOSFET drive circuits often have to work at high temperature environments like server farms, automobiles, extreme industrial environments, space vehicles, etc. These applications demand a gate driver circuit that is functional, efficient, and reliable at high temperatures. With its high thermal conductivity and wide bandgap energy, SiC circuits can operate efficiently at high temperatures which are extremely suitable for applications in these scenarios [2].

A SiC power MOSFET can be switched at higher switching frequencies with smaller power dissipation when compared to their silicon counterparts. Hence, good driver circuitry able to drive the SiC power MOSFET switch at high frequencies enables usage of these power MOSFETs in high frequency applications that leads to significant reduction in size of inductors and capacitors for a given power rating thereby increasing the converter power density. This property will be enormously useful for portability and transportation applications like aircraft, automobiles, spacecraft, space stations, etc. [2].

SiC has an order of magnitude higher breakdown voltage than silicon which makes SiC superior in high voltage applications. Furthermore, the conduction loss of SiC is less than silicon

above a certain frequency (12.6 kHz for 6H-SiC) which makes SiC more appealing than silicon for high frequency switching applications [2], [3].

The integration of this SiC gate driver with the power MOSFET device in the same package, or even better in the same chip, would result in unmatched performance potential in plethora of applications which makes this integrated SiC gate driver a state of the art contribution to the field of Power Electronics. This is a first ever attempt of making a gate driver circuit in SiC material itself and is a buildup to the eventual goal of integrating SiC gate driver circuit with the SiC power MOSFET in the same chip to further improve the overall efficiency and performance of the system.

The designed SiC gate driver is capable of driving the SiC power MOSFET with rise/fall times of about 40 ns, a propagation delay time of less than 150 ns, and power dissipation of about 6 W. The designed gate driver is tested to be functional at high temperatures up to, and possibly beyond, 420 °C with little loss in performance parameters. This is first of its kind gate driver which can operate at high temperatures of 420 °C with high voltage output swing of maximum 0-30V and peak source/sink current of 3A at high frequencies beyond 500 kHz. The maximum rated high temperature gate driver up to this date was developed on SOI technology which was capable of operation up to 225 °C and at 200 kHz switching frequency [4].

2. BACKGROUND

2.1 SILICON AND SILICON-ON-INSULATOR (SOI)

Silicon technology has several limitations when it comes to high power and high temperature applications. Silicon based power electronic applications are limited to 150 °C or lower device temperatures and can withstand 10 kV blocking voltages [5]. Furthermore, silicon devices have switching speeds limited to the range of hundreds of hertz for very high power applications which is far less than what is desired by numerous applications for smooth power flow, reduced inductor and capacitor sizes, lower system cost, and overall efficient system performance [2], [5].

The minimum off-state current which is limited by reverse leakage of a *p*-*n* junction diode in silicon increases with intrinsic carrier concentration which increases exponentially with increase in temperature. This substantial leakage current at high temperatures above 150 °C in silicon leads to unacceptable I_{ON}/I_{OFF} ratios for many circuits [6], [7].

Silicon-on-insulator (SOI) technology can help develop silicon MOSFETs with better off-state current for higher temperature applications allowing circuits to operate at 200 °C – 300 °C for reasonable time periods (up to five years). With utilization of body-biasing approaches in SOI CMOS process, Fraunhofer Institute in Germany was able to produce acceptable performance with silicon up to a maximum of 350 °C for 5 V applications [8]. This is the maximum rated high temperature silicon device known to this date.

The mobile carriers (i.e. electrons and holes) in silicon, with sufficient temperature and electric field, can enter and propagate through the gate oxide leaving behind trapped charges in the oxide and oxide/semiconductor interface. This phenomenon degenerates the device

characteristics resulting in circuit performance reduction and circuit malfunctions by degrading gate insulator electrical properties and even undesired shifting in MOSFET threshold voltage [9]. Furthermore, probability of circuit failure because of electromigration increases in silicon with increase in temperature. This is caused by gradual displacement of microscopic metal traces on a silicon IC because of current flow over time [10].

2.2 SILICON CARBIDE MATERIAL

Wide bandgap semiconductors like silicon carbide (SiC) and gallium nitride (GaN) have larger bandgaps, higher breakdown electric field, and higher thermal conductivity making the devices in these technologies capable of blocking higher voltages, switching at higher frequencies, and withholding higher junction temperatures relative to silicon devices [2]. In comparison between SiC, GaN, and silicon; SiC comes out on top as a material of choice for power devices according to several figures of merit for high frequency power electronics applications [11].

Despite the impediment on rapid growth of SiC because of difficulties in material processing, inherent crystal defects, and lack of abundant wafer suppliers, SiC research and development has accelerated worldwide because of its unmatched physical properties at high power and high temperatures [2], [12]. Because of its relatively high carrier mobility and its low dopant ionization energy, 4H-SiC polytype is preferred for power devices over other polytypes.

Table 2.1 Comparison of Silicon and Silicon Carbide Material Properties [13], [14]

Quantity	Symbol (Unit)	Silicon	4H-SiC
Energy Bandgap	**E_g (eV)**	1.12	3.26
Electric Field Breakdown (1 kV operation)	**E_c (V/ cm)**	0.25×10^6	2.2×10^6
Coefficient of Thermal Expansion	**CTE (ppm/ K)**	4.1	5.1
Electron Mobility	**μ_e (cm^2/V·s)**	1400	700 – 980
Hole Mobility	**μ_h (cm^2/V·s)**	450	120
Saturated Electron Drift ($E>2 \times 10^5$ V/cm)	**v_{sat} ($\times 10^7$cm/s)**	1.0	2.0
Thermal Conductivity	**Θ_K (W/ m·K)**	150	370
Intrinsic Carrier Density (300K)	**η_i (cm^{-3})**	10^{10}	8.2×10^{-9}

2.2.1 Intrinsic Carrier Concentration and *p-n* junction Leakage

SiC semiconductor has about 10 to 35 orders of magnitude lower number of thermal electron and hole carriers present in the crystal, referred to as intrinsic carriers, as compared to silicon [2]. The concentration of these intrinsic carriers (η_i in cm^{-3}) is exponentially dependent upon the temperature of the semiconductor and is given by the equation below [9]:

$$\boldsymbol{\eta_i = \sqrt{N_C N_V}\, e^{-E_G/2kT}} \tag{2.1}$$

In Eq. (2.1), T is the temperature in Kelvin, k is the Boltzmann constant (8.62×10^{-5} eV/K), E_G is the energy bandgap of the semiconductor measured in electronvolts, and N_C and N_V are the effective electron and hole density of states for the semiconductor per cubic centimeter. The

lightly doped region of silicon device usually falls somewhere between 10^{14} and 10^{17} atoms per cubic centimeter which means that at room temperature η_i of silicon (with 1.1 eV bandgap) is around 10^{10} cm^{-3} which is negligible. But when the temperature is increased, the intrinsic carrier concentration start to increase and around 300 °C, the concentration will be almost equal to doping levels [6]. However, in case of wide bandgap devices like SiC, because of higher bandgap value of 3.23 eV for 4H SiC, the intrinsic carrier concentration is much lower than silicon, approximately 18 orders of magnitude lower, causing it to rise to significant values only beyond 600 °C [6], [15]. Since functioning of an electronic circuit absolutely relies on manipulation of the local free carrier concentration deliberately doped in the semiconductor devices during the fabrication process, the unbridled escalation of intrinsic carriers contributes to substantial degradation of device characteristics.

The intrinsic carrier concentration also makes a significant difference when considering the leakage currents of rectifying *p-n* junctions in semiconductor devices [6]. These leakage currents should be kept at very minimum values which is the current that flows when the *p-n* junction is reverse biased. This phenomenon is more pronounced at high voltage applications. The I-V behavior of *p-n* junction diode, with p-type doping much larger than the n-type doping, for reverse bias voltage and temperatures below 1000 °C is given by the equation below [6]:

$$\boldsymbol{I = -qA\eta_i\left[\frac{n_i}{N_D}\sqrt{\frac{D_P}{\tau}} + \frac{W}{2\tau}\right]} \tag{2.2}$$

In Eq. (2.2), q is the magnitude of charge of electron, A is the area of the *p-n* junction (cm^2), N_D is the n-type doping density (cm^{-3}), W is the width of the junction depletion region (cm) at applied voltage, D_P is the hole diffusion constant (cm^2/s), η_i is the intrinsic carrier concentration and τ is the effective minority carrier lifetime (s). Since the intrinsic carrier concentration of wide

bandgap semiconductors is much lower than that of silicon, it is easy to see from Eq. (2.2) that the leakage currents in SiC is intimately related to intrinsic carrier concentration. This implies that the harmful reverse-bias currents increases exponentially with increase in temperature and since the intrinsic carrier concentration of SiC is relatively very smaller than that of silicon, the leakage current in SiC is orders of magnitude smaller than silicon as well [6].

2.2.2 Thermionic Leakage

When the carriers in semiconductor devices gain sufficient energy, they undergo a process called emission where the carriers tunnel through or go over an energy barrier in the device structure. The carriers gain more energy as the temperature increases because of accumulation of thermal energy. This carrier emission function as manifested in a rectifying metal-semiconductor diode (i.e. a Schottky barrier contact) when the reverse bias voltage is appreciable (i.e. $V_A < -0.2V$ or $|V_A| > 0.2V$) can be represented as follows [6], [16]:

$$\boldsymbol{I = -AK^{*}T^{2}e^{q\Phi_B/kT}} \tag{2.3}$$

In Eq. 2.3, Φ_B is the effective potential barrier height of the junction (eV) and K^* is the effective Richardson constant of the semiconductor, A is the area of the *p-n* junction (cm^2), T is the temperature (Kelvin), k is the Boltzmann constant (8.62×10^{-5} eV/K) and q is the magnitude of charge of electron.

It can be clearly seen from Eq. (2.3) that increase in effective potential barrier height Φ_B exponentially reduces the carrier emission leakage current. The maximum Φ_B that can be obtained is always less than the semiconductor bandgap and depends on the metal, the semiconductor and the junction formation process. Usually Φ_B is less than three quarters of bandgap energy which means for silicon with 1.1 eV bandgap, Φ_B is less than 0.9V [6]. In SiC

with its 3.23 eV bandgap, refer Table 2.1, Φ_B can be twice as large which substantially reduces the junction leakage current at any given temperature by at least several orders of magnitude. This contributes in realizing effective high-voltage and high-temperature circuits using SiC which is not possible with conventional semiconductors like silicon.

2.2.3 Power Dissipation and Junction Temperature

Because of the intrinsic resistance in semiconductor devices, some of the power is always lost when current is flowing through them and the power dissipation is more pronounced when the amount of current flowing through the device is large. Furthermore, there is also dynamic power dissipation when the devices switch on and off. During switching there is always a brief period of time where both the current and voltage are large causing large instantaneous power dissipation [17]. In high frequency applications, this power dissipation becomes particularly significant [6]. Furthermore, the leakage current flowing through the *p-n* junction when it is blocking a high voltage at high temperature also leads to undesired power dissipation. All these power dissipations cause the internal temperature of the device to increase. This causes an unstable positive feedback loop of increasing temperature and power dissipation because all these power dissipations tend to increase with increase in device temperature.

In silicon high-power devices, rated to block hundreds or thousands of volts, the high electric fields give rise to significantly large reverse-bias leakage currents which in turn causes rise in internal junction temperatures that becomes problematically pronounced beyond 200 °C and ensuring proper and safe cooling of these devices becomes virtually impossible beyond this point [6]. The wide bandgap of SiC contributing to relatively much less reverse leakage at *p-n* junction, superior switching properties because of low switching loss, and its high thermal

conductivity, as listed in Table 2.1, of 4.9 W/cm·K (3-13 times higher than silicon) makes SiC very appealing in the field of high temperature power electronics [2], [6], [18], [19]. The high thermal conductivity allows for high junction temperature operation and more simple and effective thermal management.

2.2.4 Power Density and Size of Power Electronics System

The power density of a MOSFET is directly related to its current density and breakdown voltage [20]. The current density of SiC is approximately 3 to 4 times higher than Si or GaAs and has higher breakdown voltage, almost 10 times than that of silicon as can be seen in Table 2.1, which directly contributes to a superior power density of SiC [20], [13]. Because of very high power density of devices on SiC substrates (9.8 W/mm at 8 GHz), SiC has potential to shrink the size of power electronic systems by an order of magnitude [20], [13]. This significantly reduces the cost of the power equipment as well as the cost of the entire system utilizing the equipment. SiC technology has potential to allow 50% increase in power and a 90% reduction in weight and volume of a power electronics module [1].

2.2.5 Switching Speed and High Frequency Operations

SiC can attain increased switching speeds for high voltage power devices because of higher saturated electron drift as shown in Table 2.1. In high voltage applications, the effect of saturated electron drift overrides the effect of electron mobility causing an overall effect of increase in switching speed [13]. Gain in switching speed allows higher frequency operation of power devices which is appealing to numerous power electronic applications.

2.2.6 Breakdown Voltage

As shown in Table 2.1, SiC has an order of magnitude higher critical field avalanche breakdown compared to silicon. The high electric breakdown greatly increases the switching frequency of bipolar devices because of lessening of minority carrier charge storage [2]. Furthermore, higher breakdown strength results in much lower losses for SiC based devices and also allows for higher doping concentration of up to hundred times higher than with silicon [21]. The higher breakdown limit results in dramatically low conduction losses of SiC MOSFET, at least in the breakdown voltage range [21].

2.3 CREE SIC PROCESS

Cree SiC process is a 2 μm process which is fabricated on 4H-SiC crystals. The process has only an enhancement type NMOSFET as a switching device, only a single metal layer, and a poly layer with high poly sheet resistance of about 119Ω/μm^2 at room temperature. The gate oxide thickness is 400 nm. The threshold voltage for the NMOS was measured in lab to be around 3.5 V at room temperature. The high poly resistivity requires large circuit layouts to reduce the poly resistance which in turn adds large parasitic capacitances to the circuit rendering layout of large circuits extremely challenging.

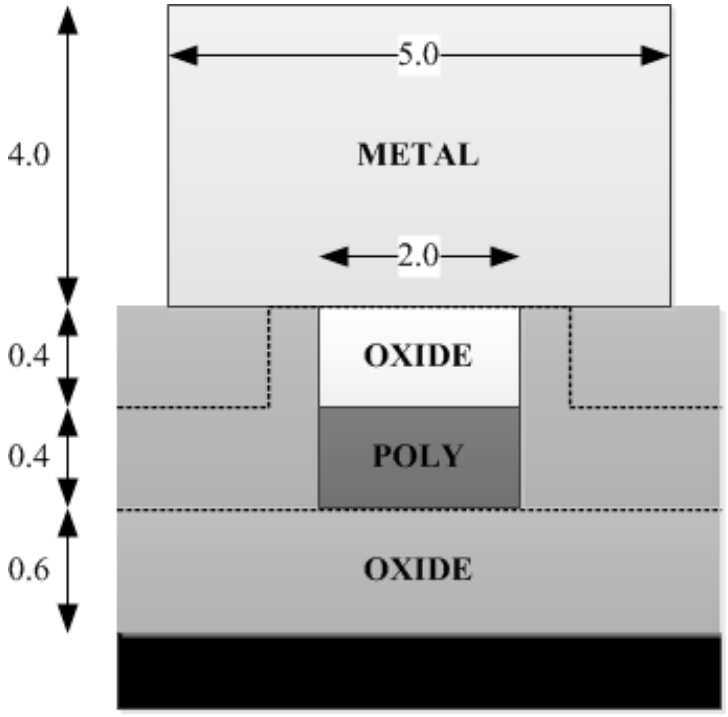


Fig. 2.1 The process stack of Cree 4H-SiC process (Shown units are in microns).

Cree has two variations of SiC process, a selective ion implantation process and an epitaxial layer growth process.

The ion implantation process is more suitable for integrating the power MOSFET with the gate-driver and other circuitry but imposes stifling limitations on circuit designers. In the implant process, there is significant leakage current from drain to source of the device when the potential difference between them exceeds 18 V and, furthermore, there is inconsistency between the process parameters in different implant process wafers and the effect exacerbates between different runs.

Cree is still struggling with figuring out how to integrate power MOSFETs with the gate driver and other circuitry in the epitaxial growth process. Nevertheless, the epitaxial process is superior to the implant process in many ways with respect to its relatively better consistency

from run to run and from wafer to wafer in the same run. Furthermore, the leakage from drain to source in the epitaxial version of process is negligible allowing the potential difference to go beyond 50 V safely, which is sufficient for properly employing the proposed gate driver topology.

For these reasons, the gate driver circuit was fabricated only in the epitaxial version of the process and the implant version of the process was eschewed. Furthermore, 32x2 is the only transistor used in the entire design of this gate driver since it was the most efficient and reliable device in this process. Desired circuit performance effects can be generated using this transistor with varying number of fingers since a 64x2 transistor is equivalent to a 32x2 transistor with two fingers.

2.4 GATE DRIVERS

Gate drivers are integral part of any power electronics system because they act as an interface between the control electronics and the power stage. Gate drivers are powerful amplifiers that take in PWM control signals and drive IGBTs and MOSFETs with the high current required by these really large devices.

A gate driver significantly affects the efficiency of power electronics system, especially in high frequency applications, and this aspect is more prominent for high voltage and high current systems [22]. A gate driver capable of switching the power device at high frequencies, beyond 200 kHz, makes it possible to realize high frequency switching applications, high efficiency power systems, and a significant reduction in size of passive components in the system [23], [24].

2.5 ELECTRONIC PACKAGING LIMITATIONS

The semiconductor packaging technology is not mature enough to properly handle operations beyond 300 °C temperature because of chemical, physical, and electrical stability challenges posed by the packaging materials and interfaces between them. Conventionally used metals and alloys like Cu, Al etc. are not suitable for packaging in high temperature operations due to undesirable oxidization and formation of intermetallic phases. Additionally, with increase in temperature, there is more pronounced increase in stress on the materials caused by mismatch in their thermal expansion coefficients (CTE). This stress experienced in the package between the die, die-bond material, and package baseplate demands for CTE match requirement between packaging materials, confining our choice in packaging material selection. Furthermore, realization of a hermetic seal for long-term high temperature operation becomes a challenge because of escalation of thermal phenomenon like diffusion and degassing at material surfaces at high temperatures giving rise to contamination of the hermetic cavity over time [6]. Several research projects are being undertaken in this area for innovative packaging materials and packaging design concepts [6].

3. STUDY OF NMOS INVERTER TOPOLOGIES

Since the Cree SiC process does not have a PMOS or depletion-NMOS, designing an efficient inverter is a challenge on its own. The generic inverter circuit with resistor as a pull-up device and NMOS as a pull-down device is inefficient. The simple inverter has unacceptable power consumption levels when the resistor values are low and is unacceptably slow when the resistor values are high. The most significant topologies that were studied are simple inverter, source-follower inverter, and chained totem-pole inverter.

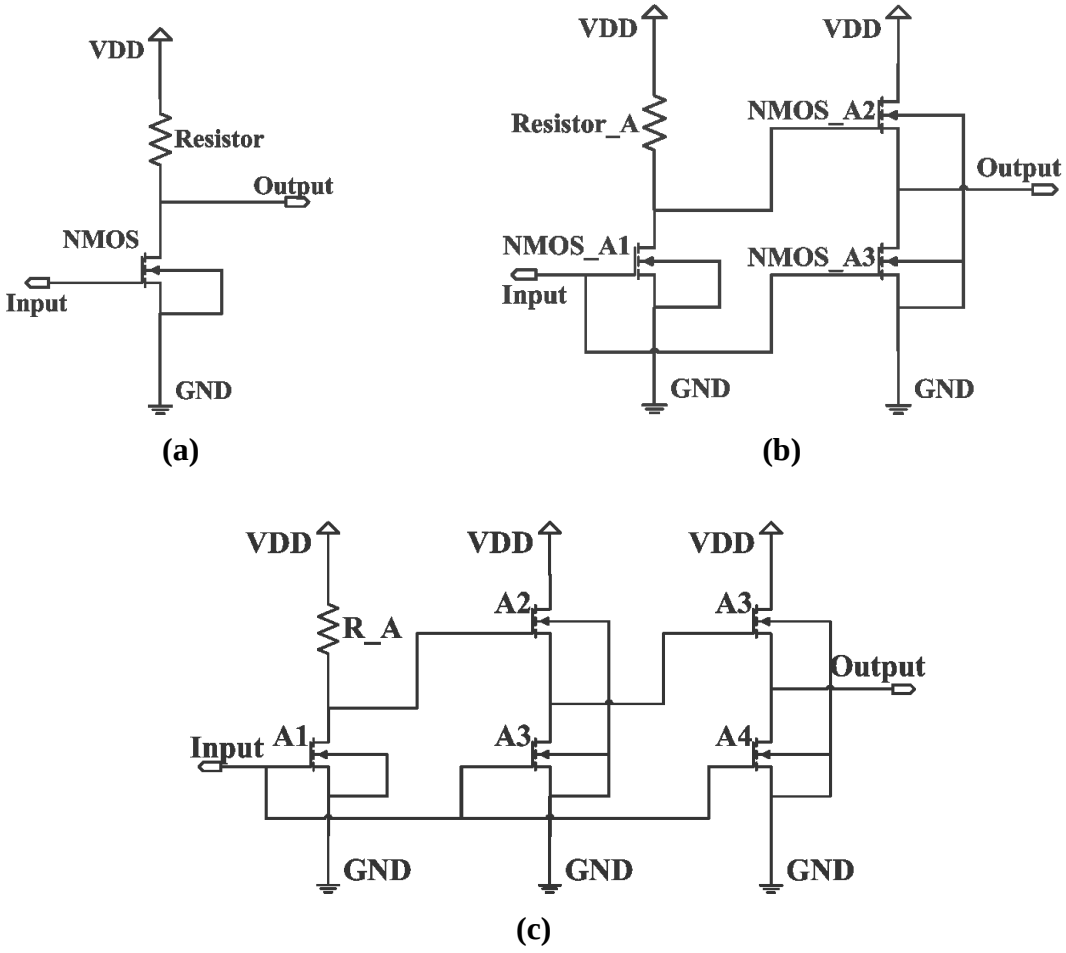


Fig. 3.1 Different inverter yopologies.
(a) Simple-inverter. (b) Source-follower inverter. (c) Dual-chain totem pole.

Table 3.1 – Summary of Inverter Topology Comparison (Load = 250 pF Capacitor)

Specifications (100 kHz)	Simple Inverter 32x2x1 R=45 kΩ		Source Follower 32x2x1 R=330 kΩ		Dual Chain Totem Pole 32x2x1 R=75 kΩ	
Input	**0 – 20**	**4.5 – 12**	**0 – 20**	**1.1 – 4.5**	**0 – 20**	**1 – 7.2**
Output	**20 – 1**	**18 – 2**	**16.9 – 1m**	**15 – 2**	**14.2 – 24m**	**12.6 – 1.4**
Power	**5 mW**		**737 uW**		**3.6 mW**	
Rise Time	**25 ns**		**25 ns**		**7.1 ns**	
Fall Time	**3.5 ns**		**2.5 ns**		**4.4 ns**	
Propagation Delay	**1 ns**		**985 ps**		**1.66 ns**	
Pros	Full Output Swing		*** Less Power consumption** * **Decent Rise Time** * Flexible Topology		* Excellent Rise Time * Decent Power Consumption	
Cons	**High-Power consumption**		Limited Output Swing		* Limited Output Swing *** Huge input Capacitance**	
Remarks	* As the resistance is increased, Rise/ Fall time will increase but Power Consumption will decrease; and vice-versa. * Also, 'V_{out}' is inversely proportional to 'R'.		* Rise time increases as we increase/decrease resistance (330K sweet spot). Power consumption decreases with increase in resistance. * It has a narrow input range for its entire output-swing.		* Rise time increases as we increase/decrease resistance (75K sweet spot). Power consumption decreases with increase in resistance. * All the bottom nMOS are connected to the same input.	

Note: In Table 3.1, 32 x 2 x 1 means transistor with 32 microns width, 2 microns length, and 1 finger.

A comprehensive study of the different inverter topologies in Fig. 3.1 was undertaken by simulating these topologies under various conditions in Cadence Virtuoso CreeSiC Program Development Kit (PDK), which was developed by University of Arkansas Mixed-Signal Computer Aided Design (MSCAD) group. The simulated results were monitored, recorded, and analyzed. The conclusions drawn are summarized and presented in the Table 3.1 above.

It was clear from the different inverter topology analysis, that 'Simple-inverter' topology as shown in Fig. 3.1(a) is very power hungry if we want a good rise time for the output signal. However, it must be noted that it is the only inverter that allows its output voltage to swing rail-to-rail.

The *source-follower* topology as shown in Fig. 3.1(b) has very low power consumption and good rise time; it is basically because the load is being charged through a transistor rather than the resistor allowing the resistor in the first stage to be big, hence decreasing power consumption. However, it must be noted that its output does not swing all the way up to the rail magnitude because of the voltage drop across drain and source of the pull-up transistor. But that is not a very significant drawback in several circumstances considering the fact that this output swing is sufficient to drive another source-follower inverter in series. Additionally, if the rail voltage is raised by several voltages, which is a safe procedure as shown by empirical evidence of lab measurements, then the output will reach the required voltage amplitude.

The *dual-chain totem-pole* topology as shown in Fig. 3.1(c) is pretty fast but the fact that all of its bottom transistors are connected to the input signal means it has a huge capacitance load on the input which is a deal-breaker in most circumstances.

However, it shall be noted that each of these topologies will have their own advantages in certain circumstances and can be utilized according to the requirements in hand. The *source-*

follower inverter topology is the handiest one given the flexibility it offers in its design and with its low power consumption and good rise time on output. The transistor *A1* in Fig. 3.1(b) can be changed along with the resistor to trade-off between rise time and power consumption of the circuit. Furthermore, it requires only a narrow input range for its entire output swing which is very useful to produce good rise time on the final signal in a chain of these inverters. For these reasons, this inverter is used extensively in design of the gate driver and gave a significant performance boost and power consumption reduction compared to designs with simple-inverters.

4. SINGLE CHIP GATE DRIVER DESIGN

The purpose of the presented gate driver design in SiC is to drive a SiC power MOSFET. It takes a pulse width-modulated (PWM) signal as an input with 0-5 V logic levels and outputs a 0-VDD (VDD is typically 20 V) on-phase signal with large current (peaks reaching 3.0 A) to drive the power MOSFET gate with good rise and fall times (around 50 ns). In this design, all of the gate driver circuit blocks are incorporated into a single chip.

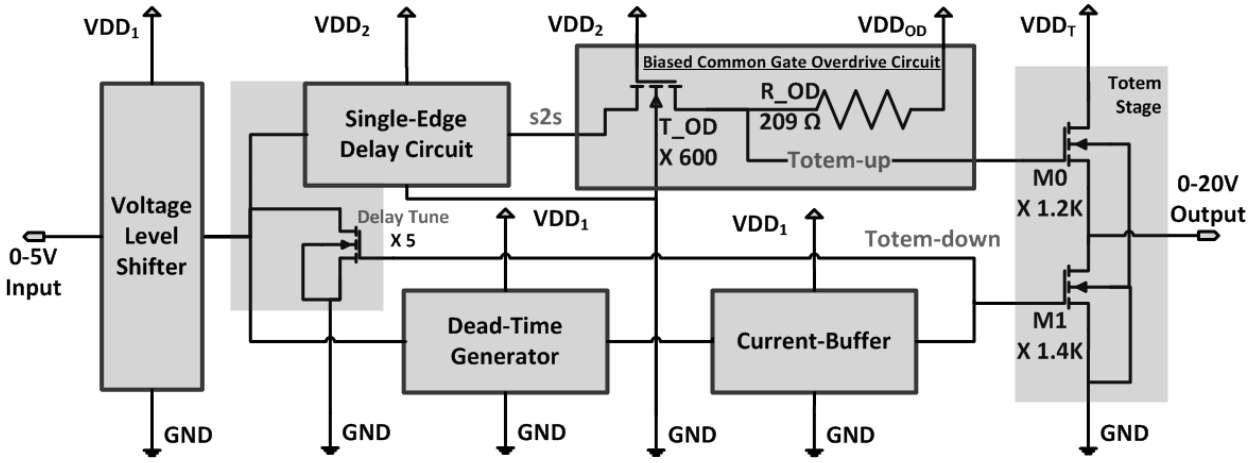


Fig. 4.1 System level block diagram of gate driver (All NMOS used are 32 x 2 devices).

The Fig. 4.1 shows the system level block diagram of the gate driver. The shaded areas are individual blocks which will be explained in detail individually later. The input 5 V logic level signal is passed through the *voltage level shifter* which shifts the input signal to VDD_1 logic level (typically 20 V) while maintaining the good rise/fall time of the input pulse. This shifted signal is then bifurcated and passed through the *dead time generator* and *single-edge delay circuit*, simultaneously. The output of the *dead time generator* is delayed, which can be manipulated to the required extent, and fed to the *current buffer* stage which outputs an inverted signal with enough current to drive pull-down device at the *totem stage*. The output of the *single-edge delay*

circuit will have only its rising edge delayed; the extent of delay can be manipulated during the design phase. The output of the *single-edge delay circuit* is fed to the *biased common-gate overdrive circuit* which drives the pull-up device at *totem stage*. The *biased common-gate overdrive circuit* has the ability to overdrive the pull-up device, without breaking the maximum gate-to-source voltage limitations of the process, resulting in better rise time of the output signal.

The shoot-through current elimination is achieved by complementary combination of the *dead time generator* and the *single-edge delay circuit*. This is utterly significant in high frequency applications where dynamic power dissipation, because of switching losses, is the major contributor to total power dissipation. The switching loss is primarily due to shoot-through current in the circuit during switching; besides charging/discharging of gate capacitors of MOSFETs used which cannot be compromised.

All transistors used in the circuits are 32x2 transistors (meaning 32 microns width and 2 microns length) because they were the best available transistor in the process. Also, using transistors with multiple fingers of a 32x2 ratio device is sufficient to achieve the desired performances.

4.1 VOLTAGE LEVEL SHIFTER

Fig. 4.2 depicts the *voltage level shifter* stage; the ‘x N’ near the transistors name indicates that the 32x2 transistor has *N* fingers. Each stage is a source-follower inverter with adjusted parameters for optimum performance and functionality. The source-follower inverter topology is employed in this stage instead of simple-inverter because of its certain advantages over the latter. This conclusion was reached after a comprehensive analysis of different possible inverter topologies using only enhancement-nMOSFETs and resistors. The first stage of Fig. 4.2 is an

inverter that will shift the input of 0-5 V to high voltage levels with good rise-time utilizing the 20 V rail voltage. Then, the signal is passed through another inverter which further shifts the voltage and also re-inverts it back to original phase which is now in appropriate magnitude level. The output of this circuit will be level-shifted signal with current large enough to drive front stages of the *single-edge delay* and *dead-time generator* circuit that follows.

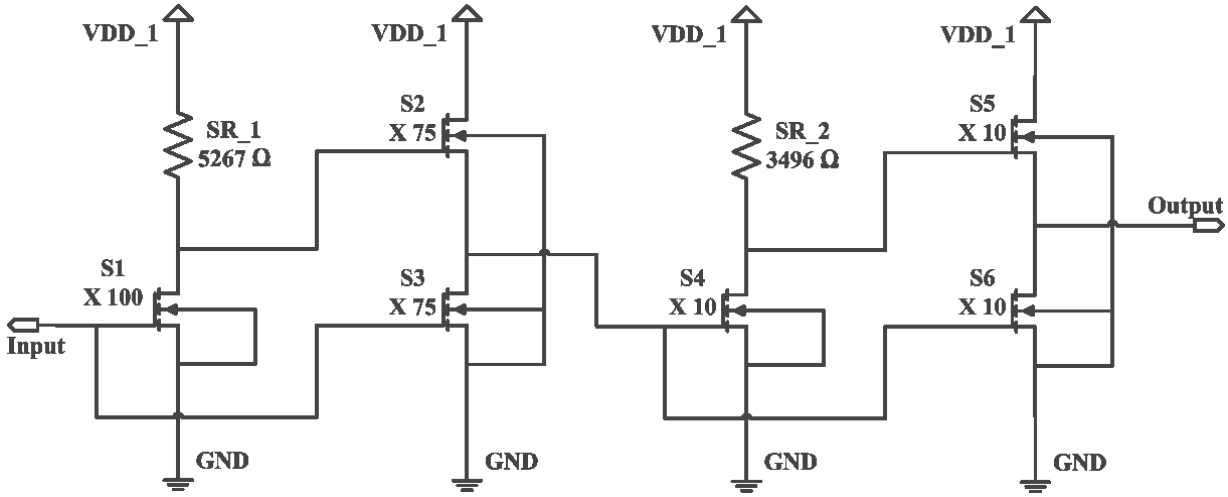


Fig. 4.2 Voltage level shifter circuit diagram.

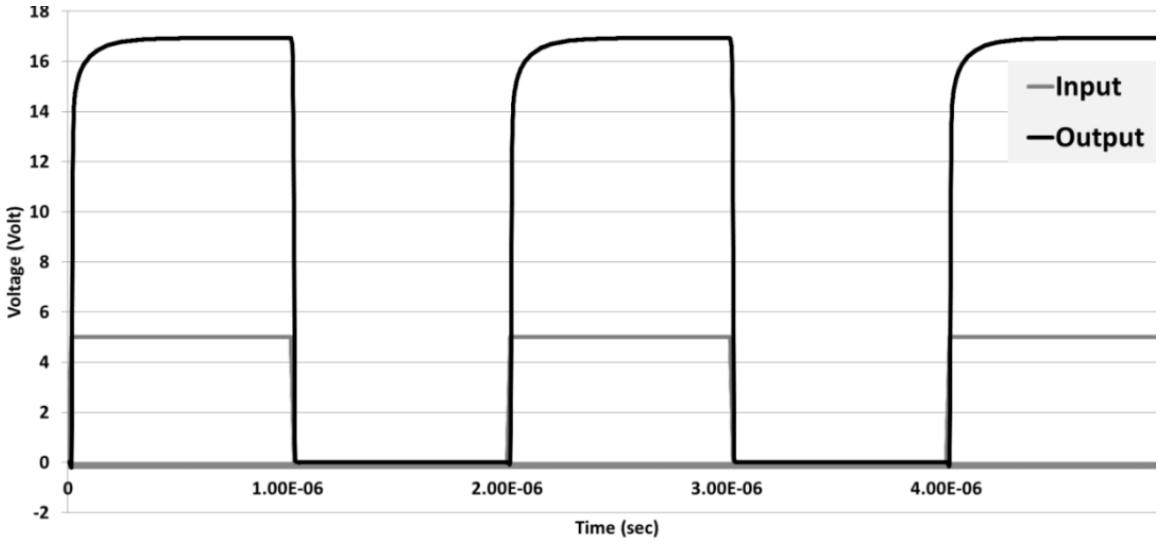


Fig. 4.3 Input/output waveforms of voltage level shifter.

4.2 DEAD TIME GENERATOR

The *dead-time generator* basically delays the entire signal. The purpose of this particular circuit is to allow the pull-up transistor to turn-off completely before the pull-down transistor starts to turn-on at the totem-stage, effectively eliminating the shoot-through current during the falling edge of the ultimate gate driver output. Please note that this circuit only eliminates the shoot-through current during the falling edge of the final output, the *single-edge delay circuit* is responsible for eliminating the shoot-through current during the rising edge of the final output which will be explained later.

The intended dead time is generated by delaying the rising edge of the totem-down signal to make sure that the pull-down device turns on only after the pull-up device is completely turned off. Since the current buffer that follows the *dead time generator* block is inverting, the rising edge of totem-down signal is basically the falling edge of output of the *dead-time generator* block. Hence, maintaining the falling speed of the *dead-time generator* output and controlling its delay serves the purpose of eliminating shoot-through at the gate driver output while maintaining the good fall-time of the final output.

Fig. 4.4 shows the transistor level diagram of the dead time generator. The *delay controller* signal is critical on controlling how much delay needs to be introduced in the signal. By making it have to charge a huge gate-capacitance (gates of *DB4*, *DB6*, and *DB7*) would store significant charge at this node on the rising edge, and by discharging this node through a relatively small *DB3 delayer* transistor would make it fall significantly slower. This delay can be controlled as desired by changing the sizes of these transistors, especially *DB3_Delayer*. If the delay needs to be significantly large, then size of *DBR_2* comes into play. Making *DBR_2* very large will increase the delay introduced on the output signal. The extra stage at the end is incorporated to

make sure the delay would actually shift the signal maintaining best speed possible. This circuit doesn't invert the input signal, it just delays the signal while maintaining a good rise/fall time.

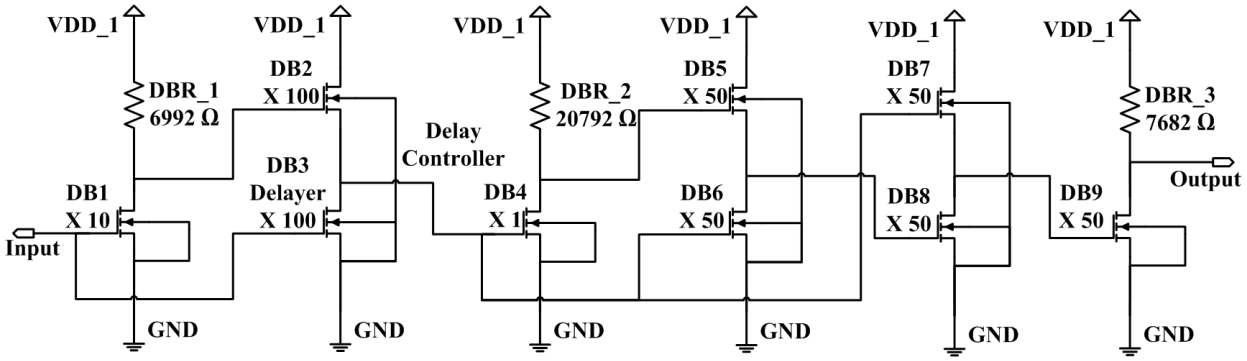


Fig. 4.4 Dead time generator circuit.

At this certain implementation shown in Fig. 4.4, this dead-time generator is employed to achieve a falling-edge delay because that is the subject of interest in this particular circuit application. Hence, the circuit has been tuned to achieve this goal of delaying the signal without any significant degradation in fall-time. The waveform in Fig. 4.5 displays that characteristic and the time-shift introduced in the signal.

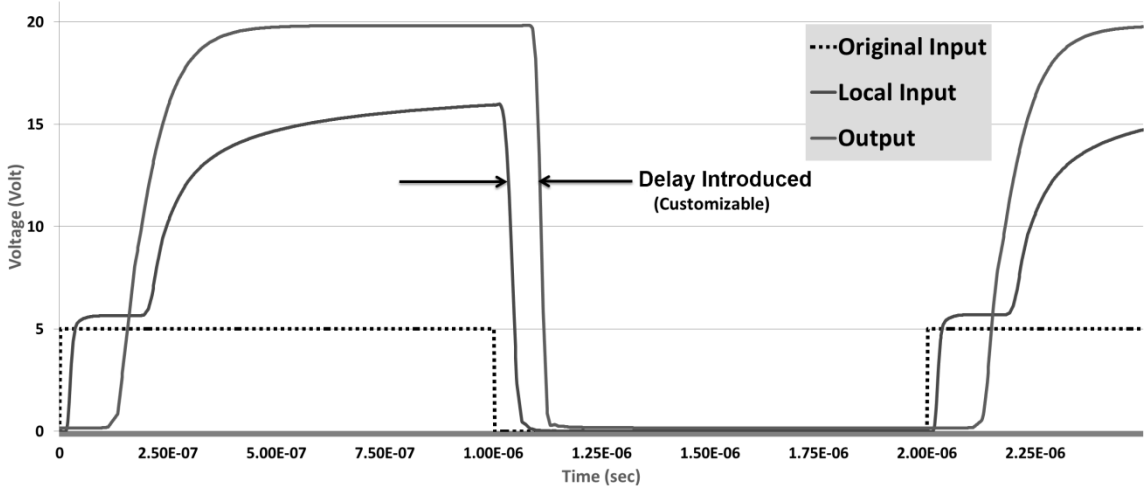


Fig. 4.5 Input/output waveforms of the dead-time generator circuit.

4.3 CURRENT BUFFER

The output of the *dead-time generator* circuit is provided as an input to the *current buffer*. This stage generates enough current drive to charge and discharge the gate of the pull-down device *M1* in the *totem stage* ON/OFF as fast as possible. This stage utilizes source-follower inverters to achieve good rise/fall time with significantly less power dissipation than other approaches. The values of each component in source-follower inverter in each stage needs to be fine-tuned to find the optimum performance parameters.

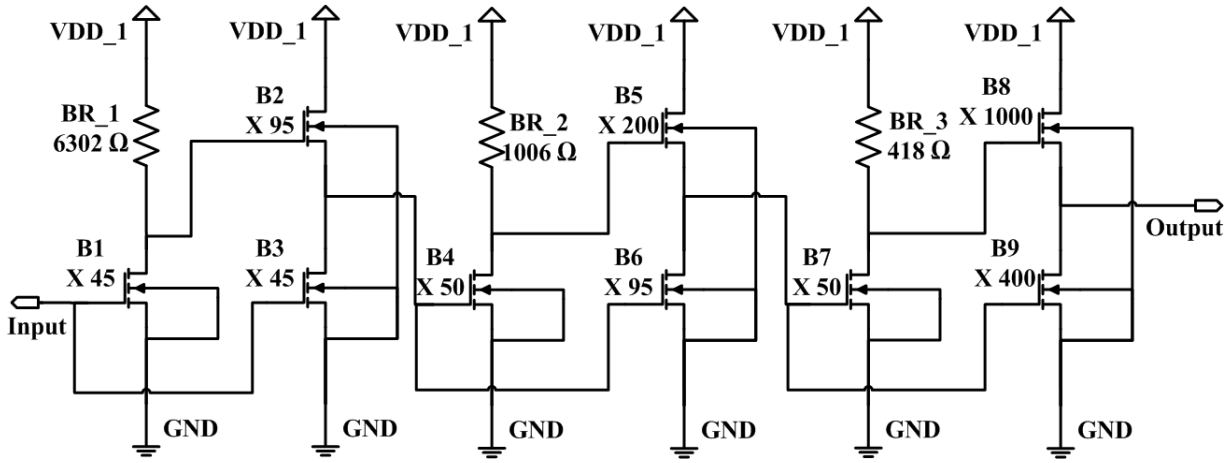


Fig. 4.6 Three stage inverting current buffer.

As can be seen in Fig. 4.7, the output waveforms have a good rise/fall time and a small propagation delay associated with them. Furthermore, it shall be noted that the output of buffer can only reach up-to 17 V because it is comprised of source-follower inverters. However, 17 V at the gate of the pull-down device in the *totem-stage* (i.e. *M1* in Fig. 4.1) is sufficient to turn the device on and hence the use of source-follower inverters is justified. Furthermore, use of a higher amplitude rail voltage i.e. 25 V would raise the output of source-follower to 20 V.

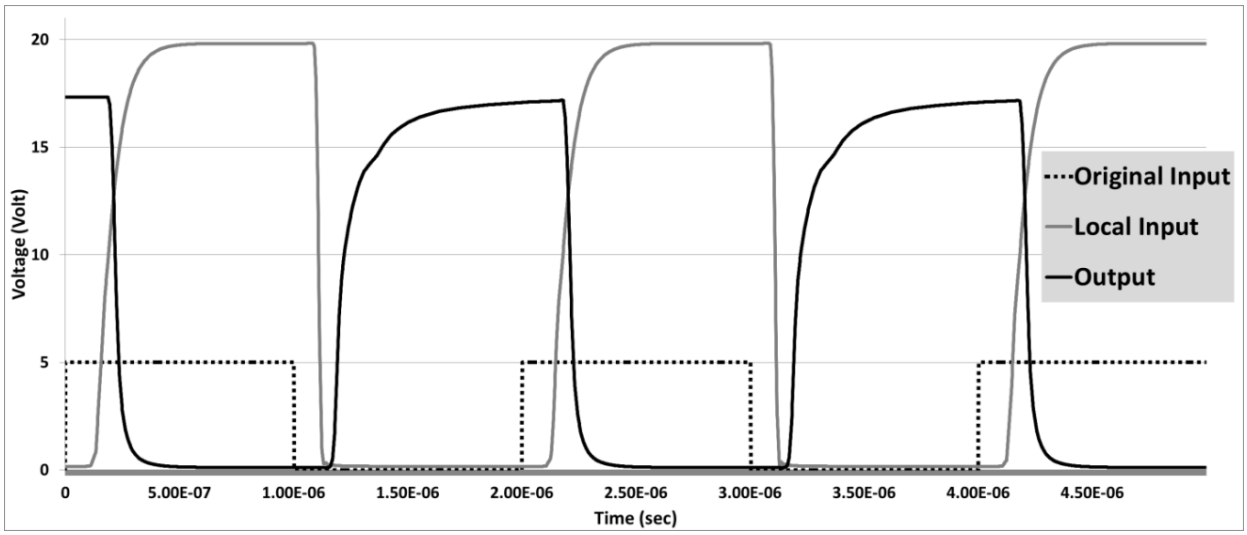


Fig. 4.7 Input/output waveforms of current buffer circuit.

4.4 SINGLE-EDGE DELAY CIRCUIT

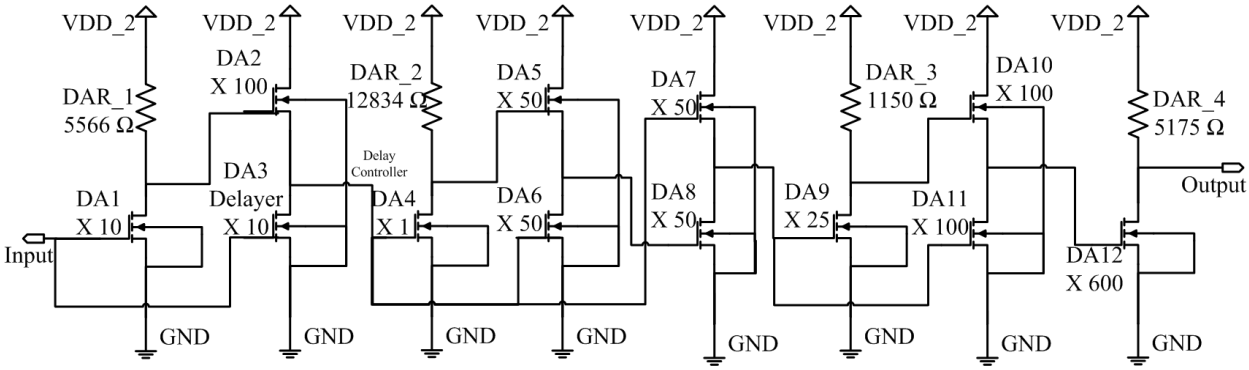


Fig. 4.8 Single-edge delay circuit.

The *single-edge delay circuit* as shown in Fig. 4.8 is employed to delay only a single-edge of the circuit to effectively eliminate shoot-through at the rising-edge of the ultimate gate driver output by making sure that the pull-down transistor is completely off before the pull-up transistor starts to turn on (at final totem-stage).

The *single-edge delay circuit* is a novel design and is flexible in implementation allowing the designer to control the amount of delay to be introduced to the desired edge of the signal by

altering the size of *DA3 delayer* transistor. This works in combination with the *delay tune* transistor, as shown in Fig. 4.1, which uses feedback to increase the extent of delay of this circuit. The *delay tune* transistor makes sure that input to this circuit doesn't rise to a significantly high level when the *totem-down* signal is high which is applied to its gate. This would make sure that the output of this stage, which will eventually cause to drive the pull-up transistor in totem-stage to turn ON, would never go *high* until the *totem-down* signal, which is the output of the current buffer, is *low* effectively eliminating the shoot-through current at the rising-edge of ultimate output of Fig. 4.1. The extra final stage of source-follower inverter is added to drive *DA12* fast enough because *DA12* needs to be a large transistor since it directly affects, in conjunction with *T_OD* transistor of gate overdrive circuit, how fast the *totem-up* signal would fall. This circuit effectively shifts the rising-edge of the input signal maintaining a good rise-time which was a tough challenge to accomplish.

The *totem-down* signal controls the gate of *delay-tune* impeding the input signal to *single-edge delay circuit* from rising as shown in Fig. 4.9. Since this input cannot rise to a strong enough value for a certain time, it cannot turn ON the *DA3 delayer* properly causing the *delay controller* to discharge very slowly. The output *s2s* will only start to rise after the *delay controller* falls to a significantly low value. This causes the delay in rising edge of *s2s* signal and as can be seen the rise-time has not been compromised for achieving the required delay. Since the signal *s2s* only rises after the *totem-down* signal has fallen down, and since *totem-up* only rises after *s2s* rises, the shoot-through condition is effectively eliminated.

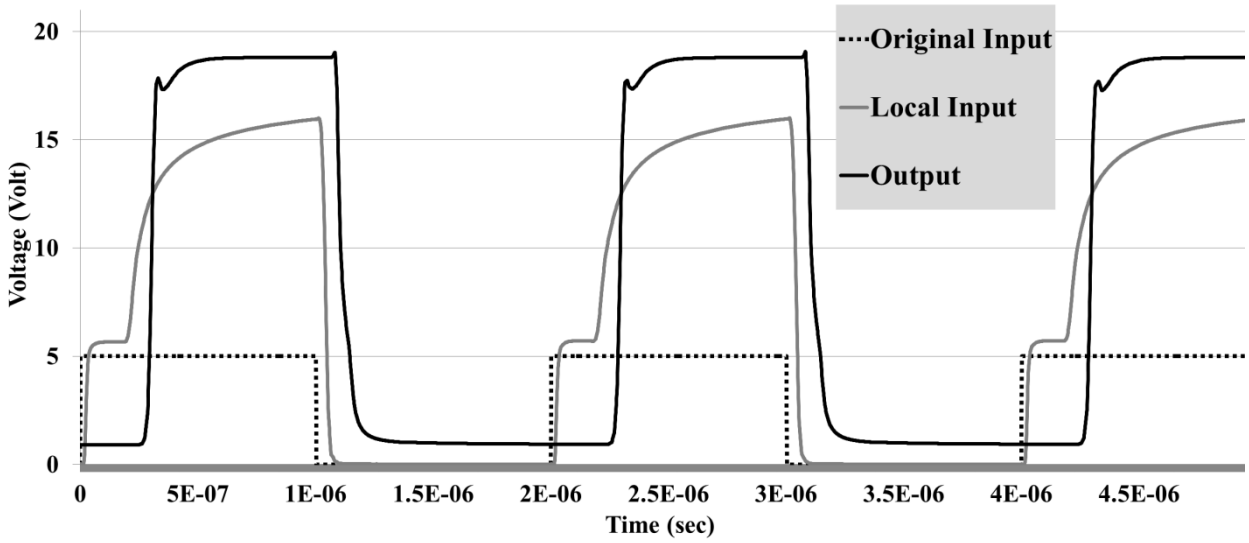


Fig. 4.9 Input/output waveforms of single-edge selay circuit.

4.5 BIASED COMMON-GATE OVERDRIVE CIRCUIT

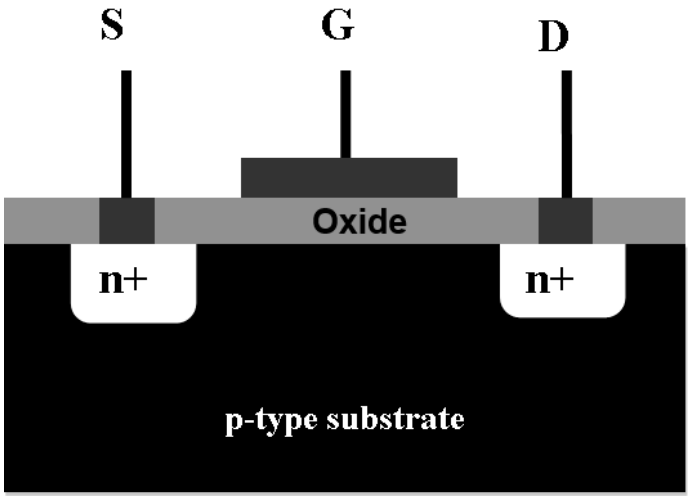


Fig. 4.10 Lateral view of a Cree MOSFET (not drawn to scale).

The output of the *single-edge delay circuit* is fed to the source of the transistor *T_OD* in *biased common-gate overdrive circuit*, as shown in Fig. 4.1, which is practically an RTL (Resistor-Transistor-Logic) inverter responsible of driving the pull-up transistor *M0* of the totem-pole output stage. This particular ingenious approach of feeding the input signal to source of

transistor turns out to be very valuable and is lynch-pin of the entire gate driver. This design approach allows overdriving the pull-up transistor (*M0*) to twice the safety limit voltage, without breaking the process voltage difference limitation of maximum 20 V potential difference across the oxide layer of any transistor, while achieving impressive performance gain. The oxide layer in this process as seen in Fig. 4.10 has a recommended safety limit of 20 V across it without breaking it. With the suggested *biased common-gate overdrive* approach, the oxide potential difference will not exceed the designated safety limit, the overdrive voltage (twice the safety limit) difference will be across the source and drain of the transistor instead which has been seen from previous tests in our lab to safely go up to 80 V.

The resistor used in this stage i.e. *R_OD* needs to be small enough to turn the transistor *M0* fast enough which results in significant amount of power dissipation. In fact, about 66% of the entire power consumed by this circuit is dissipated in this stage and this is an area where significant trade-off between power-consumed and rise-time of the final-output can be made. So, a proper trade-off according to the design requirements should be made.

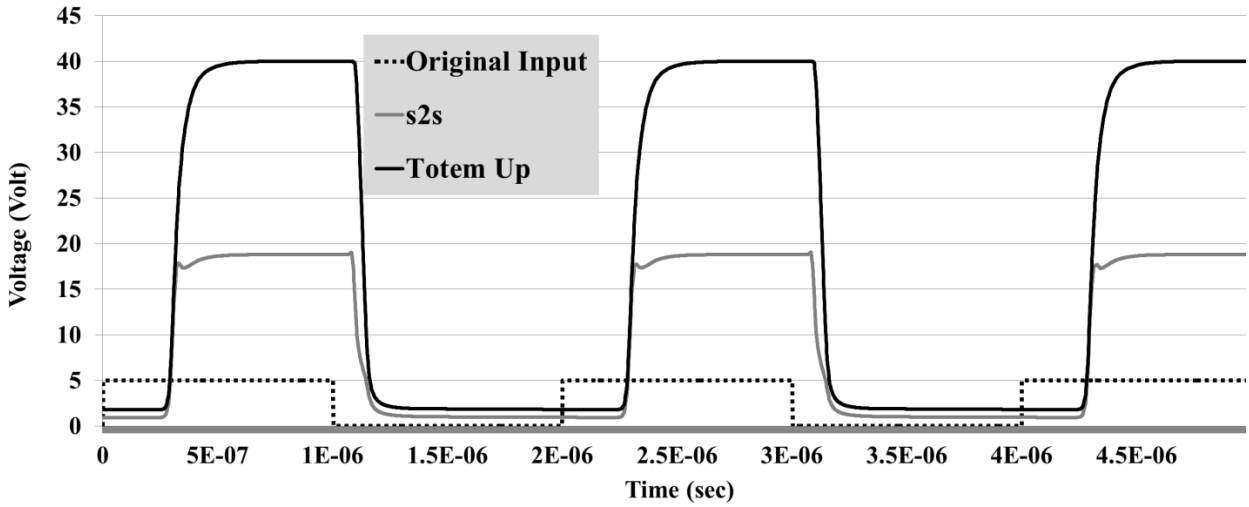


Fig. 4.11 Input/output waveforms of biased common-gate overdrive circuit.

The value of resistor *R_OD* in the *biased common-gate overdrive circuit* is very important and needs to be small enough to achieve a good rise time at the output. However, if it is very small the power dissipation would be enormous, because of the constant current flow from VDD_2 to ground (*GND*) when *totem-up* signal is low, which is undesirable in most situations. Transistors of the *biased common-gate overdrive circuit* as in Fig. 4.1 and transistor *DA12* of the *single-edge delay circuit* as in Fig. 4.8 must be carefully balanced for optimum performance. They should be small enough to restrain the power the circuit dissipates when *s2s* and *totem-up* are *low* but they should be large enough to allow drain of transistor of *biased common-gate overdrive circuit* to reach low voltage levels and to reach it fast. When *s2s* is *low*, given the small resistance value in the *biased common-gate overdrive circuit*, the sum of transistor's on-resistance must be sufficiently smaller than the resistor so that the output voltage can drop to acceptable low value as elucidated by the equations below:

When *s2s* is *low*:

$$\boldsymbol{Totem_{up} = 40\ \frac{Sum\ of\ R_{ON}}{Sum\ of\ R_{ON} + Resistor}} \tag{4.1}$$

When *s2s* is *high*:

$$\boldsymbol{Totem_{up} = 40 \frac{Sum\ of\ R_{OFF}}{Sum\ of\ R_{OFF} + Resistor}} \quad (4.2)$$

4.6 TOTEM-POLE STAGE

The totem-pole output circuit consists of huge transistors at the output stage able to drive the power MOSFET gate fast enough. These transistors turn ON and OFF alternately. The output of combinational circuit drives the upper transistor while the output of current buffer drives the lower transistor of the totem-pole. The circuit is shown in Fig. 4.1. In the current gate driver design the upper transistor *M0* is 32x2 device with 1200 fingers while the lower transistor *M1* is 32x2 device with 1400 fingers. These parameters can change according to the project requirements.

The signal waveforms of the entire circuit in Fig. 4.1 are shown in the waveforms in Fig. 4.12.

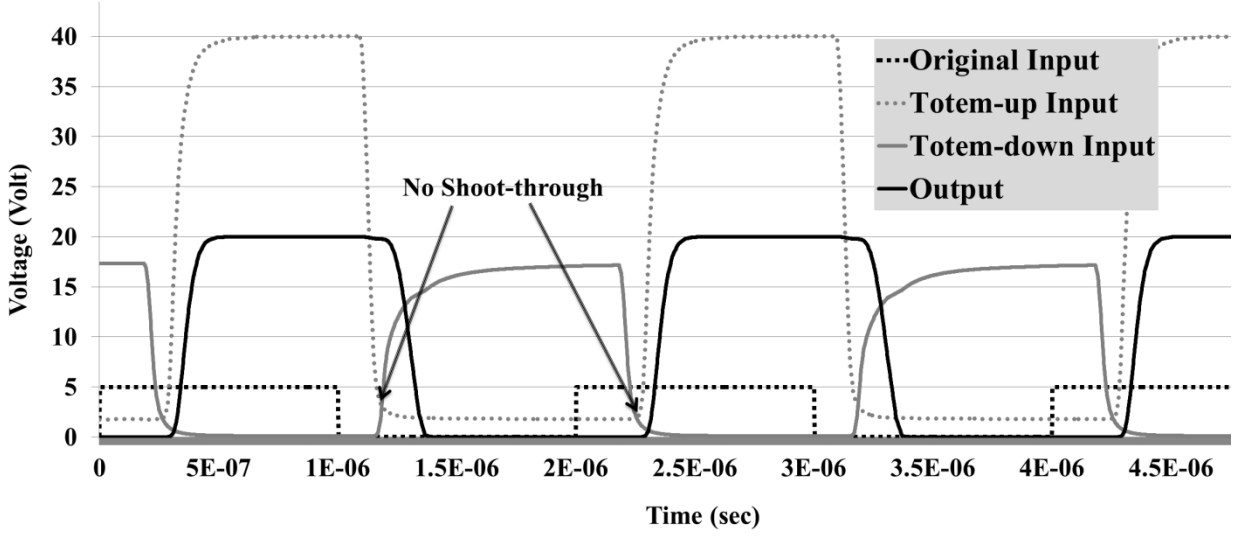


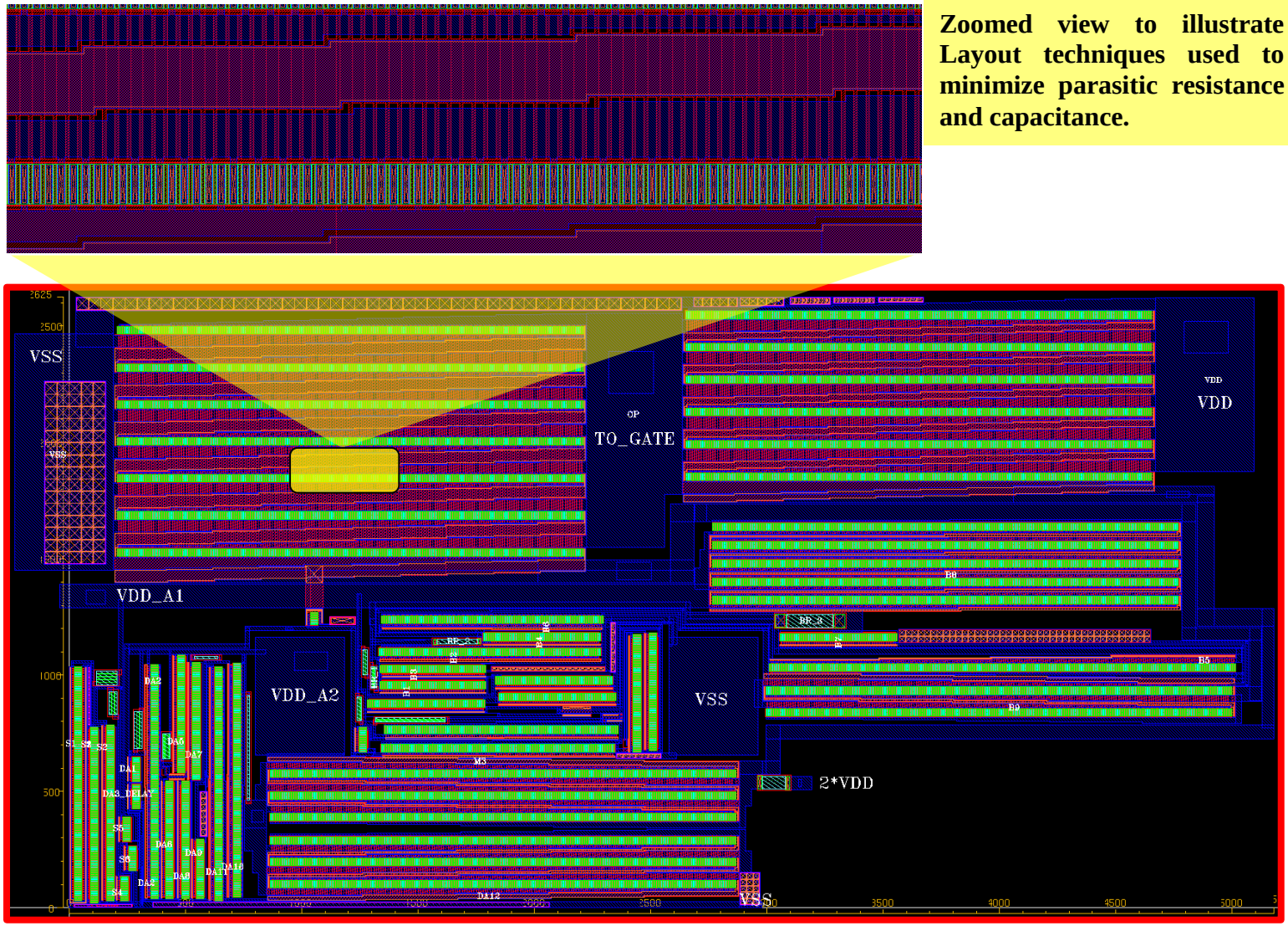
Fig. 4.12 Input/output waveforms of the totem-stage.

4.7 SINGLE CHIP GATE DRIVER LAYOUT

The layout of the gate driver shown in Fig. 4.1 is as shown in Fig. 4.13. The final dimension of the gate driver was almost a rectangle of 2.6 mm by 5.2 mm. The size of the gate driver is relatively larger because the current Cree SiC process is a 2 micron process which is huge compared to most silicon processes which are down in the 22 nm range these days. The layout seen in Fig. 4.13 is optimized by making sure that the wires see the least possible capacitance by sizing them appropriately.

Furthermore, since the process has only one metal layer and since the poly has a considerable amount of resistance in this process, reducing the resistance in the signal path was very challenging. However, these effects were diminished to the maximum extent possible by utilizing several clever and skillful layout techniques as indicated in Fig. 4.13. The zoomed section in the figure shows how the metal layer thickness is gradually and proportionally incremented as the current it carries gradually gets augmented. Furthermore, the poly connections are shorted with metal layer throughout its entire length to reduce resistance on the path of gate signal. The poly connections to the gate of transistors are made through thin strips of poly to reduce the capacitance between metal and poly layer after it was empirically established, through numerous parasitic simulations, that the capacitive effect was more pronounced than the resistive effect in that circumstance.

The metals were sized properly making them minimum width required to carry the amount of current they need to carry. The metal layer in this process is 4 microns thick and a safe current density is 1 mA per square micron. Hence, a 5 micron thickness is the appropriate size for a wire carrying approximately 20 mA current on it. The metal width contributes to the parasitic capacitance significantly and needs to be accounted for.



Zoomed view to illustrate Layout techniques used to minimize parasitic resistance and capacitance.

Fig. 4.13 Final layout of entire gate-bufffer circuitry (2625 µm x 5180 µm).

4.8 SINGLE CHIP GATE DRIVER SIMULATION RESULTS

Parasitic extraction was carried out on the layout of the gate driver after it passed Design Rule Check (DRC) and Layout Versus Schematic (LVS) tests. The characteristic of the gate driver and the results obtained are summarized in Table 4.1. It can be seen clearly that the gate driver performance is consistent over temperature. The rise/fall times only changes by about 10 ns for every 100 °C rise in temperature. The power dissipation decreases a few milli-watts and the propagation delay increases by few nano-seconds with 200 °C rise in temperature as can be seen in Table 4.1.

Table 4.1 Single Chip Gate Driver Specifications After Parasitic Extraction and Simulation

(Input: 0V – 5V 500 kHz PWM signal; Load: 4 nf Capacitor; Output: 0V – VDD; VDD = 20V; VDD_OD = 40V)

Description	20 V (VDD) 40V(VDD_OD)			22 V (VDD) 40V(VDD_OD)	25 V (VDD) 40V(VDD_OD)	25 V (VDD) 45V(VDD_OD)	25V (VDD) 50V (VDD_OD)
Temperature	27^0C	125^0C	225^0C	27^0C	27^0C	27^0C	27^0C
Output Rise Time	70 ns	79 ns	91 ns	62 ns	58 ns	49 ns	42 ns
Output Fall Time	73 ns	83 ns	95 ns	56 ns	44 ns	45 ns	43 ns
Average current drawn (VDD)	119 mA (2.4 W)	122 mA (2.4 W)	125 mA (2.5 W)	132 mA (2.9 W)	152 mA (3.8 W)	153 mA (3.8 W)	153 mA (3.8 W)
Average current drawn (VDD_OD)	84 mA (3.4 W)	78 mA (3.1 W)	74 mA (2.9 W)	81 mA (3.2 W)	78 mA (3.1 W)	88 mA (3.9 W)	98 mA (4.9 W)
Total Power Dissipation	5.8 W	5.5 W	5.4 W	6.1 W	6.9 W	7.7 W	8.7 W
Propagation Delay	263 ns	280 ns	288 ns	227 ns	188 ns	186 ns	183 ns

Fig. 4.14 verifies that gate to source/drain voltage of none of the transistors in the circuit actually goes significantly above process-defined 20 V safety limit. We can see that the *VGS* spike of *M0* transistor (pull-up device) of the *totem-stage* reaches up to 24 V, but this is just a transient behavior with rather minor amplitude spike and doesn't pose any danger to the driver reliability. Additionally, empirical experimentation data from various tests shows that the process is robust and reliable at 25 V potential across the gate oxide. The gate oxide consistently breaks down at around 35 V.

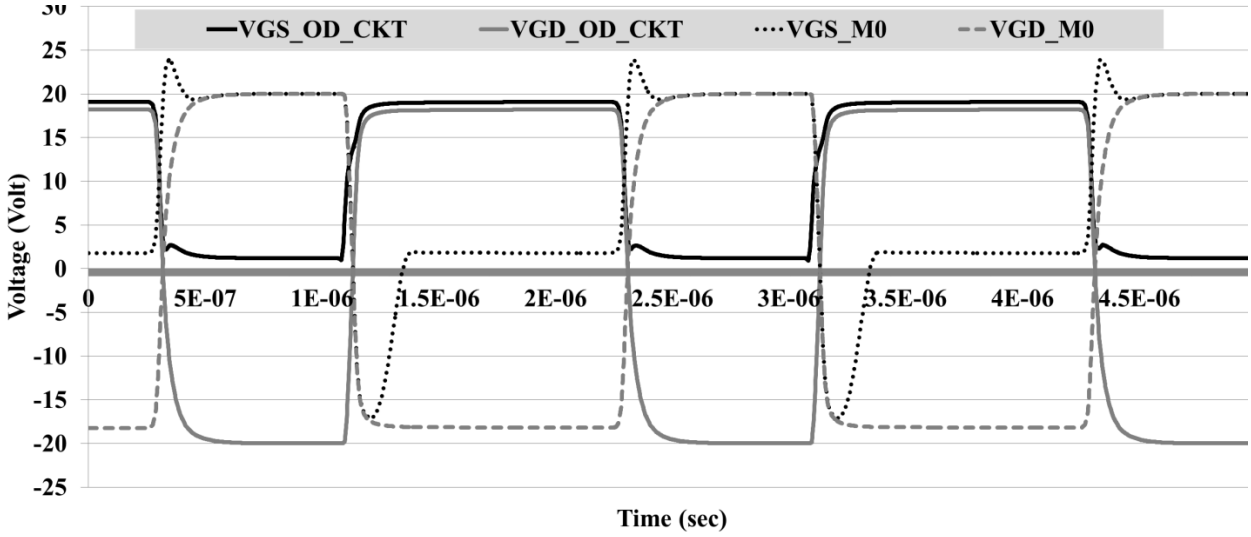


Fig. 4.14 Safety level check of the vulnerable devices for single ship design.

5. SPLIT CHIP GATE DRIVER DESIGN

Since, there are no PMOS devices in this SiC process, an NMOS device has been used as both the pull-up and pull-down device of the totem-pole stage as shown in Fig. 4.1. Furthermore, all the NMOS devices have the same substrate (substrate isolation is not possible in the current process) and the source of the devices is tied to the substrate inherently. Hence, the pull-up device in the *totem stage* responsible for the rise time of the output experiences substantial body effect, because of the increasing potential of the source with respect to body of pull-up device whenever the output starts to rise. This increases the threshold voltage of the device which substantially degrades the rise time of gate driver.

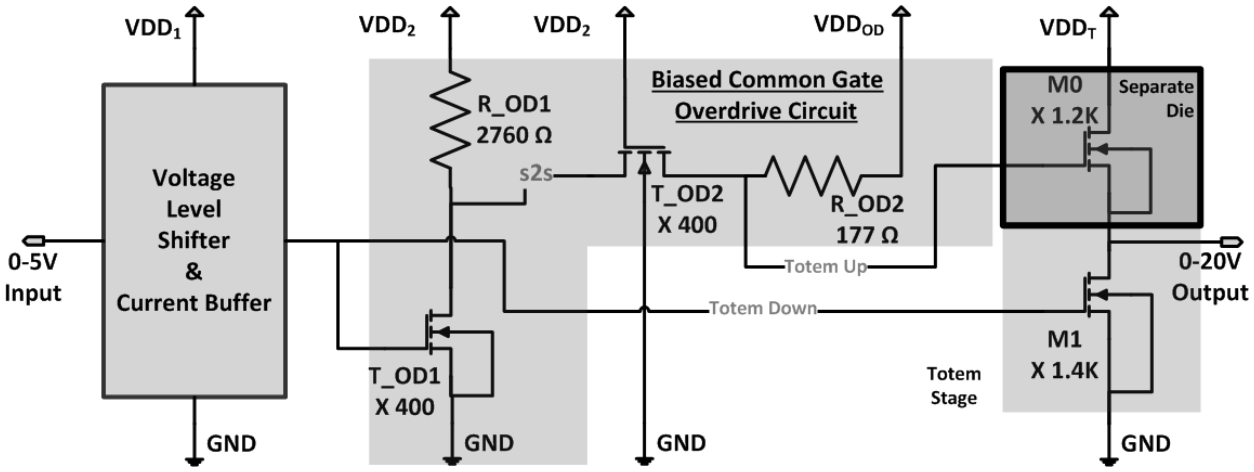


Fig. 5.1 System level block diagram of split chip gate driver.

Hence, the rise time of the gate driver can be improved by placing the pull-up device of the *totem-stage* on an entirely different die and connecting the substrate of that die with its source instead of connecting it to ground. This would keep the source and body of the pull-up device at the same potential thereby eliminating the body effect and this in turn decreases the rise time of the output. The system level block diagram of split chip gate driver design is shown in Fig. 5.1.

As can be seen in Fig. 5.1, this gate driver does not have the *single-edge delay circuit* and the *dead time generator* blocks incorporated in it to eliminate the shoot-through current. This is because those circuits were fresh and risky ideas being fabricated for the first time and are not proven to function; so this particular design is more conservative in that aspect. Elimination of those circuits in the design alters the whole system level layout a little bit and allows integrating the *voltage level shifter* and the *current buffer* stages into one block *voltage level shifter & current buffer* as seen in Fig. 5.1.

5.1 VOLTAGE LEVEL SHIFTER AND CURRENT BUFFER

The voltage level shifter and current buffer circuit consists of seven optimally sized source follower inverters in series. The first three stages shifts the input voltage level to the 0 – VDD level and the last four stages incrementally amplifies the drive current so that the final output can drive the *T_OD1* of the *biased common-gate overdrive circuit* and pull-down device *M1* of the *totem-pole* stage sufficiently fast.

In Fig. 5.2, there are seven stages of source follower inverters making it an inverting block. The seven stages are found out to be optimal tradeoff for acquiring maximum rise/fall times at the output of the block. The *X* mark followed by a number represents the multiplicity factor of the 32x2 transistors signifying the number of fingers it has.

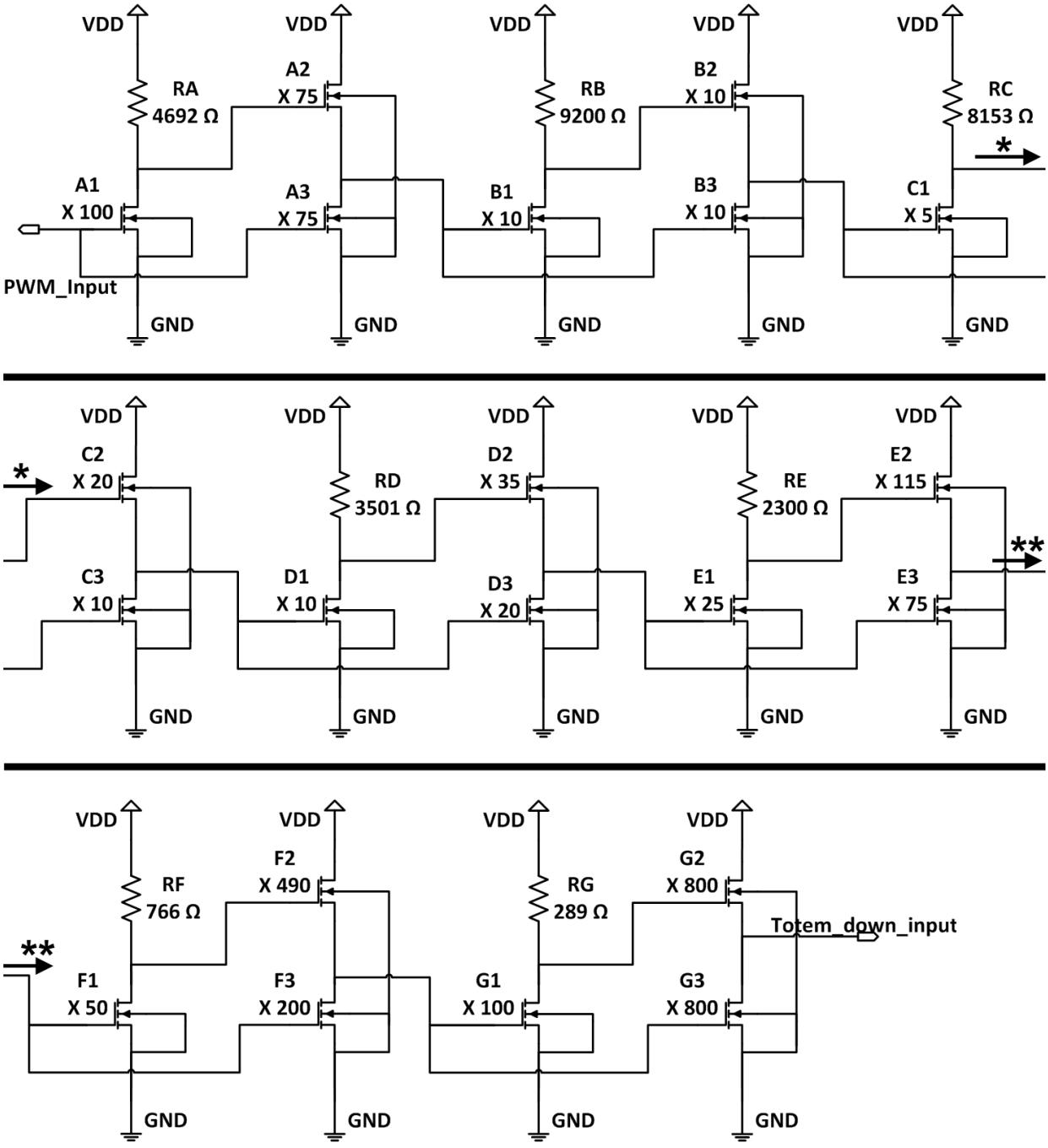


Fig. 5.2 Voltage level shifter and current buffer (in series from top to bottom).

The waveforms of the *voltage level shifter and current buffer* is as shown in Fig. 5.3. The voltage level of the output is close to the rail VDD and the rise time of the signal is good, at least

up to the point where the voltage is sufficient to turn ON the transistor being driven by this signal.

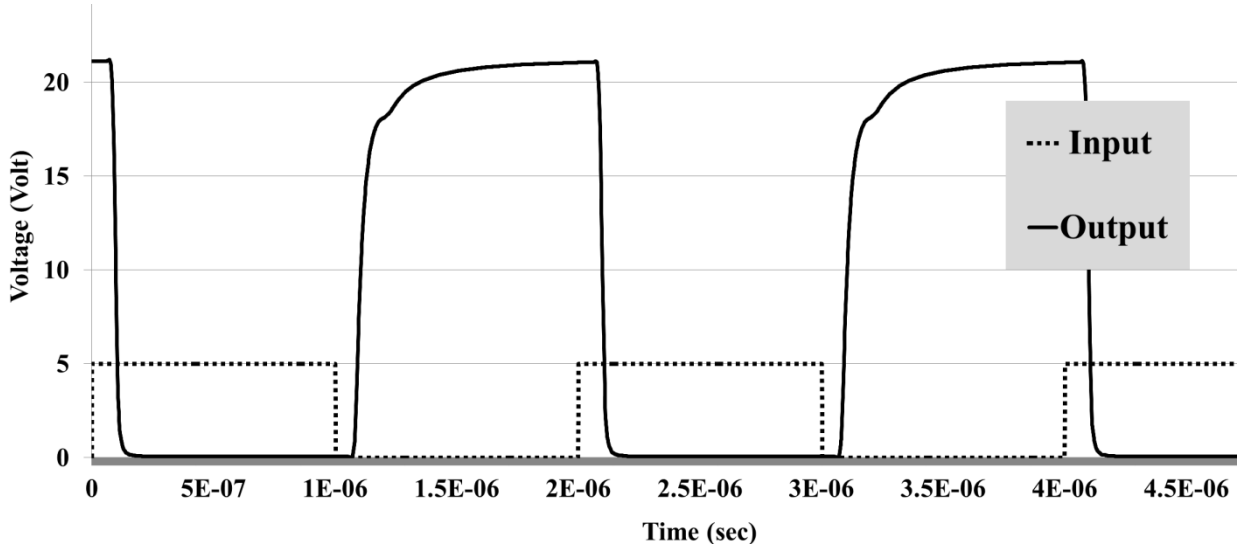


Fig. 5.3 Input and output waveforms of voltage level shifter and current buffer (rail VDD = 25 V).

5.2 BIASED COMMON-GATE OVERDRIVE CIRCUIT

This circuit is same as the one used in single chip gate driver design. The output of the *voltage level shifter and current buffer* drives the transistor *T_OD1* of *biased common-gate overdrive* circuit as shown in Fig. 5.1. This overdrive circuit is comprised of two RTL inverters connected in such a way that the output of the first RTL inverter is fed to the source of the transistor, *T_OD2* of Fig. 5.1, of second RTL inverter. This ingenious way of connecting these RTL inverters allows the circuit to safely handle twice the process-defined safe limit voltage. This circuit generates an overdrive voltage of large magnitude, up to twice the process specified gate-oxide breakdown safety limit, which can drive the pull-up device, *M0* of Fig. 5.1, significantly faster staying within the safety limit.

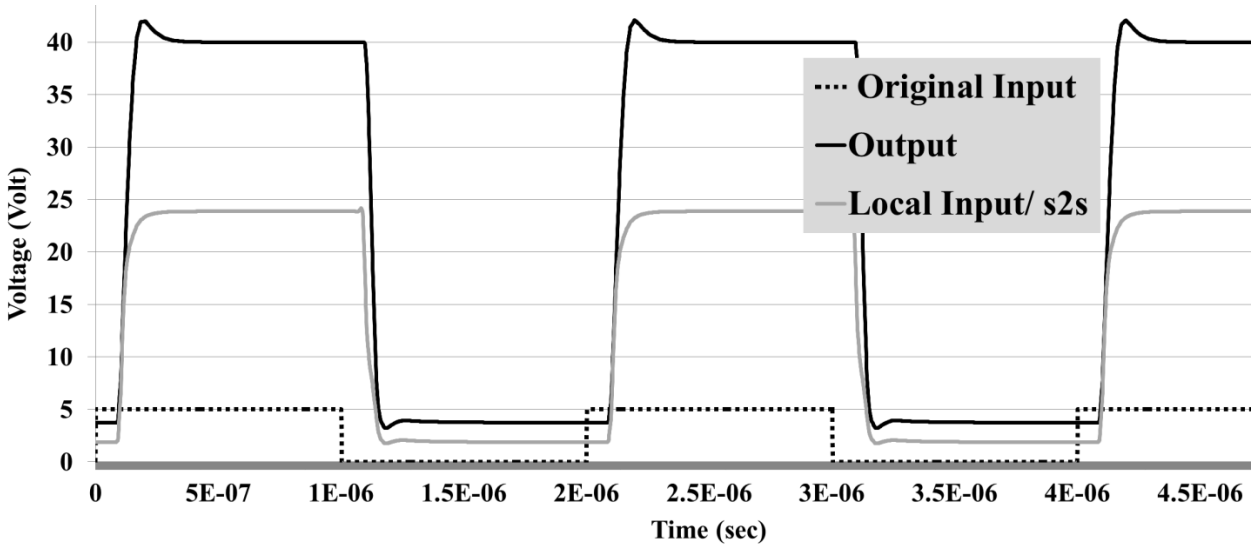


Fig. 5.4 Input and output waveforms of common gate overdrive circuit.

As can be seen in the Fig. 5.4, the output of the overdrive circuit reaches a value of 40 V which can very effectively drive the pull-up device of the *totem-pole stage*.

5.3 TOTEM POLE STAGE

The *totem pole stage* in the split chip design is a little different than the single chip design. To eliminate the body effect on the pull-up device, the pull-up device is placed in an entirely different SiC die. It was necessary to have a completely different die because in the current Cree SiC process, body of all the transistors is connected to the substrate which is connected to the ground. As can be seen in Fig. 5.1, the pull-up device *M0* in totem-stage is placed in a separate die and then wire-bonded together to achieve this. The source of the pull-up device, which is also the output of the gate-driver, is now shorted to the body of the pull-up device which eliminates the body effect since the source and body are now at the same potential.

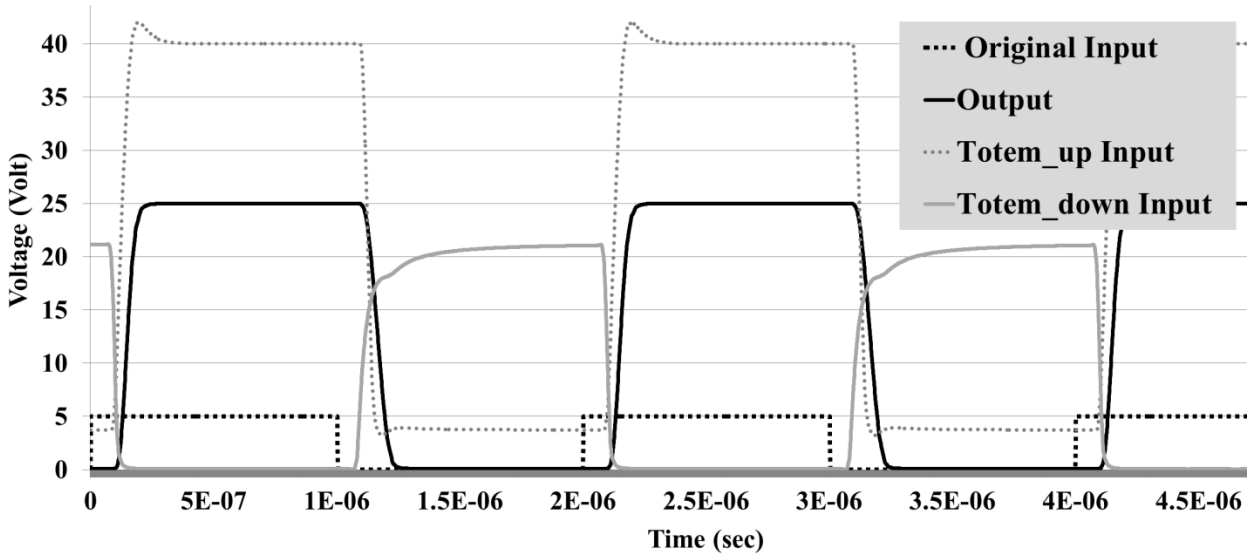


Fig. 5.5 Input/ output waveforms of the split chip gate driver.

The simulations show, referring to Fig. 5.5, that the output of the gate driver goes all the way down to 0V and up to VDD with a good rise/fall time. Refer to Table 5.1 for the actual rise/fall data for different power supply modes.

5.4 SPLIT CHIP GATE DRIVER LAYOUT

The layout of the gate driver shown in Fig. 5.1 is as shown in Fig. 5.6. The final dimension of the gate driver was almost a rectangle of 3.6 mm by 5.4 mm, but it has a lot of free spaces within the rectangle that can be used to place other circuits. The layout of this gate driver is optimized using various techniques as explained in section 4.7.

The layout of this gate driver is set up in a special way so that two dies of the same chip in Fig. 5.6 can be used to make it work as a split-chip gate driver. One die will be used for the entire circuitry except the pull-up device of the totem stage and the other die will be used just for its pull-up device of the totem stage. This approach is further illustrated in Fig. 6.9.

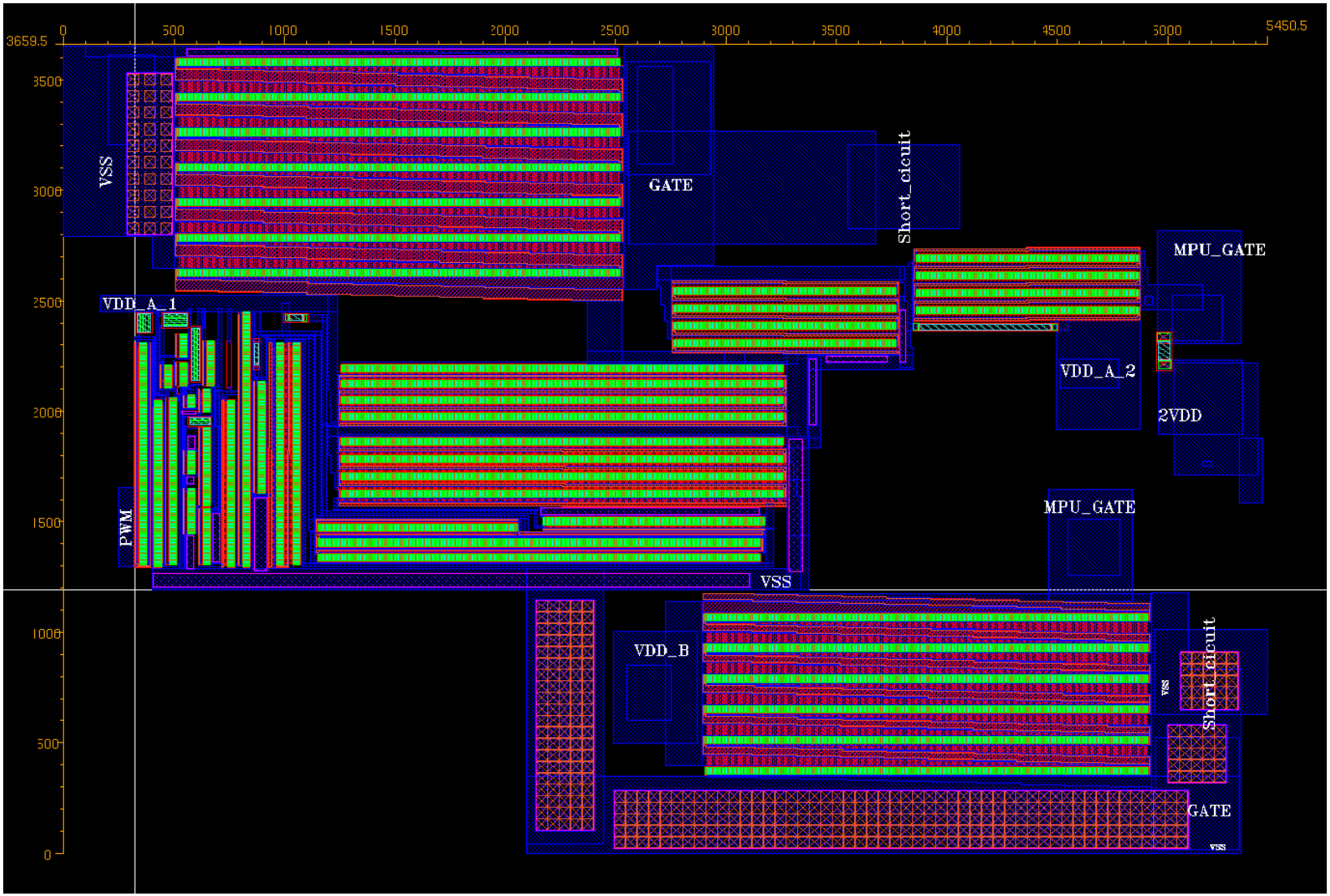


Fig. 5.6 Final layout of split chip gate driver (3660 µm x 5451 µm).

5.5 SPLIT CHIP GATE DRIVER SIMULATION RESULTS

After the layout passed DRC and LVS, parasitic extraction was performed, and the gate driver was simulated with the model obtained after parasitic extraction. The specification of the gate driver is summarized in the Table 5.1. It is clear that the rise time has improved significantly compared to the single chip design (refer Table 4.1); this is due to the absence of body-effect in the split chip design.

It can be clearly seen from Fig. 5.7 that the potential difference on any of the devices that see voltages above VDD never exceeds VDD itself (In this diagram VDD = 25 V and VDD_OD = 40 V). This diagram proves that none of the devices experience potential difference more than VDD across the gate-oxide capacitor; more specifically the gate-oxide capacitor experiences the same potential difference across it with or without the overdrive circuit, in spite of the fact that the overdrive circuit can generate a drive voltage of twice the magnitude as a normal circuit.

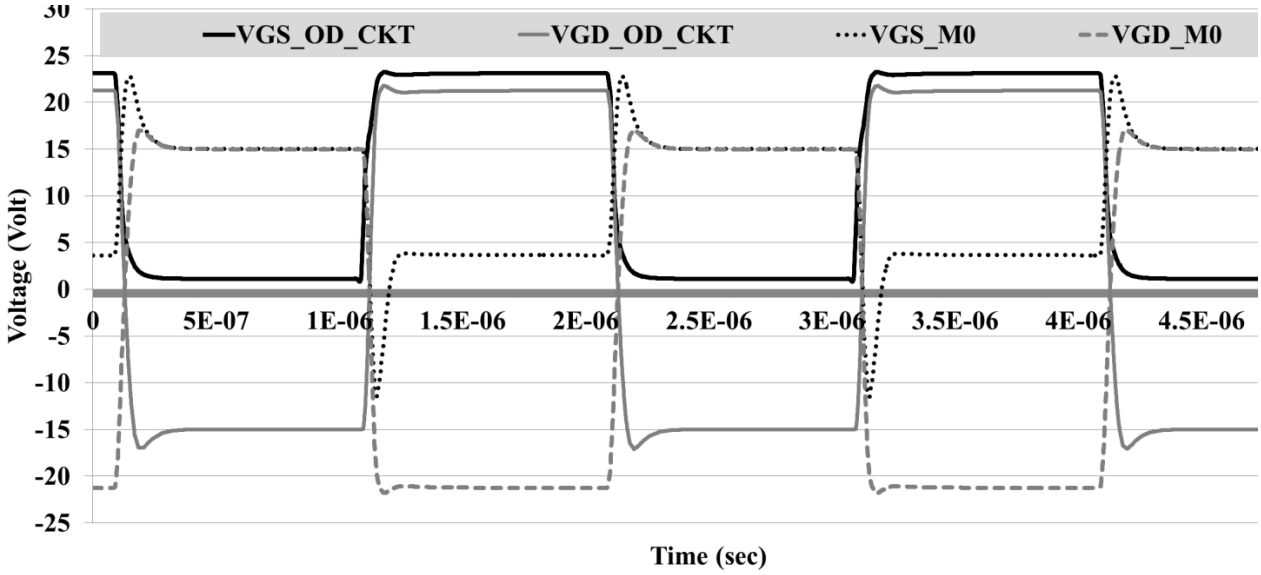


Fig. 5.7 Safety level check of vulnerable devices for split chip gate driver.

Table 5.1 Split Chip Gate Driver Specifications After Parasitic Extraction and Simulation

(Input: 0V – 5V 500 kHz PWM signal; Load: 4 nF Capacitor; Output: 0V – VDD; VDD = 25V; VDD_OD = 40V)

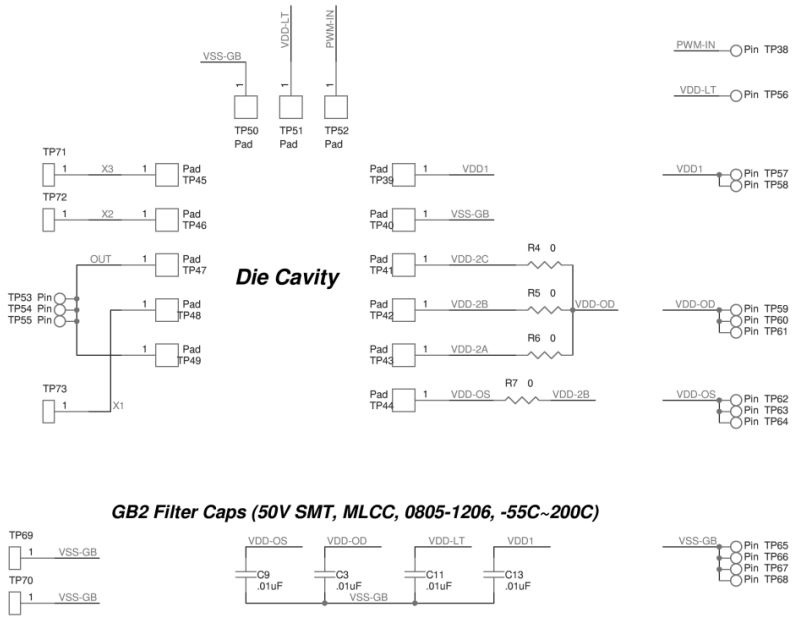
Description	20 V (VDD) 40V(VDD_OD)			22 V (VDD) 40V(VDD_OD)	25 V (VDD) 40V(VDD_OD)	25 V (VDD) 45V(VDD_OD)	25V (VDD) 50V (VDD_OD)
Temperature	27^0C	125^0C	225^0C	27^0C	27^0C	27^0C	27^0C
Output Rise Time	35 ns	40 ns	46 ns	32 ns	31 ns	28 ns	25 ns
Output Fall Time	60 ns	73 ns	83 ns	50 ns	41 ns	40 ns	40 ns
Average current drawn (VDD)	121 mA (2.4 W)	124 mA (2.5 W)	130 mA (2.6 W)	131 mA (2.9 W)	149 mA (3.7 W)	152 mA (3.8 W)	155 mA (3.9 W)
Average current drawn (VDD_OD)	76 mA (3.0 W)	69 mA (2.7 W)	64 mA (2.6 W)	77 mA (3.1 W)	78 mA (3.1 W)	88 mA (3.9 W)	97 mA (4.8 W)
Total Power Dissipation	5.4 W	5.2 W	5.2 W	6.0 W	6.8 W	7.7 W	8.7 W
Propagation Delay	35 ns	40 ns	46 ns	32 ns	31 ns	28 ns	25 ns

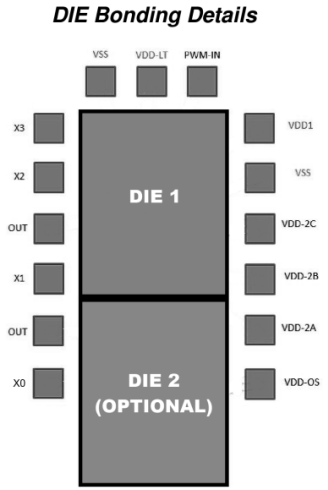
6. TESTING PARAPHERNALIA AND TEST PLAN

6.1 TEST SET UP DESIGN AND INTEGRATION

The designed gate driver was fabricated by Cree in October 2013, using their latest SiC process. ORNL, APEI, and U of A then teamed up to design a gate driver testing motherboard (as shown in Fig. 6.2) and daughterboard (as shown in Fig. 6.1 in a concerted effort. The schematic of the daughterboard for attaching the gate-driver die and wire-bonding it to the daughterboard is shown in Fig. 6.1. The schematic of motherboard which holds the daughterboard is shown in Fig. 6.2. Fig. 6.4 and Fig. 6.5 show all the four layers of the motherboard PCB.

Fig. 6.3Fig. 6.5 show the PCB Layout of the daughterboard and motherboard respectively. Fig. 6.3 shows the top and bottom layout of the daughterboard. We can clearly see two slots for installing the gate driver die in the top layout of the daughterboard i.e. Fig. 6.3 (a). The primary slot (upper slop) has holes in it running all the way down to the bottom as can be seen in the bottom layout as well which are introduced for better thermal dissipation. Furthermore, there is a short between TP19 and TP27/ TP29/ TP30 which can be utilized by not connecting the resistor R2. The resistors can be used to tune the circuits accordingly in case of substantial process variation than expected; otherwise a 0 Ω resistor will be used instead.





Gate Driver Pins	Daughterboard Pins for Single Chip	Daughterboard Pins for Split Chip
VDD_1	VDD-LT	VDD-LT
VDD_2	VDD1	VDD1
VDD_OD	VDD-2A/2B/2C	VDD-2A/2B/2C
VDD_T	VDD-OS	x0

Notes:

- Die attached in cavity and bonded to 'Pads' using 5 mil bonding wire.
- 0.01uF HT bypass capacitors placed close to cavity
- Bonding pads are _mm^2 and plated with _um soft gold
- Use 2 oz copper PCB for heat sink layers
- Use Rogers 4350B PCB Material
- Provide a large backplane connection for temperature monitoring/control
- Top die has grounded cavity (green)
- Connect grounded caviity to backplane layer using high density vias for maximum thermal conductivity.
- Bottom die has isolated cavity (blue)

SKF-1311-1R0 Schematic
SKF-1311-2R0 PCB
December - 2012

Title: **Gate Buffer Test PCB**
Size: B | Document Number: **gb2-testpcbs-v1.dsn** | Rev: 0
Date: Monday, December 03, 2012 | Sheet 1 of 1

Fig. 6.1 Daughterboard schematic for testing the gate driver. Courtesy of Oak Ridge National Laboratory [25].

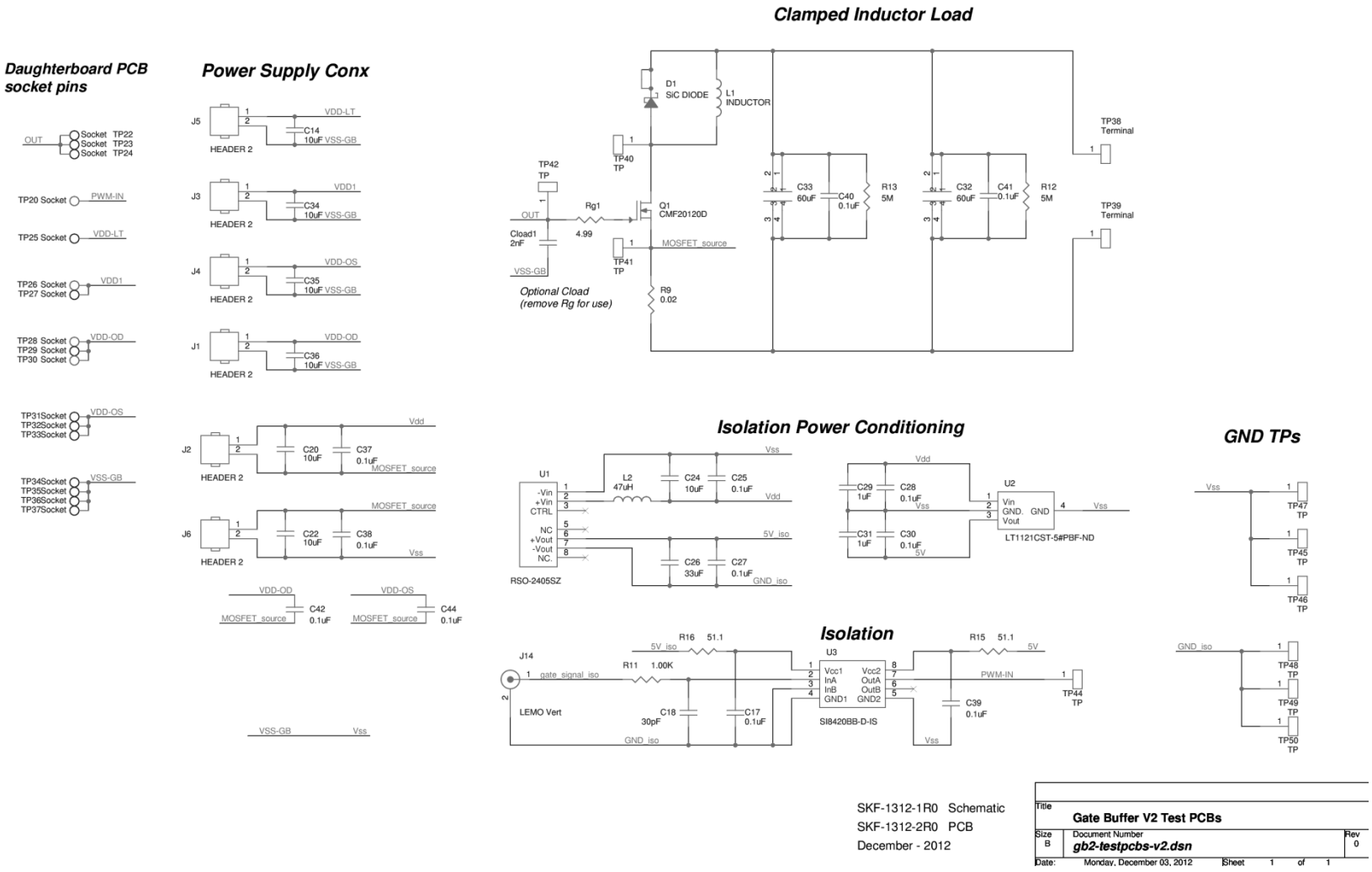
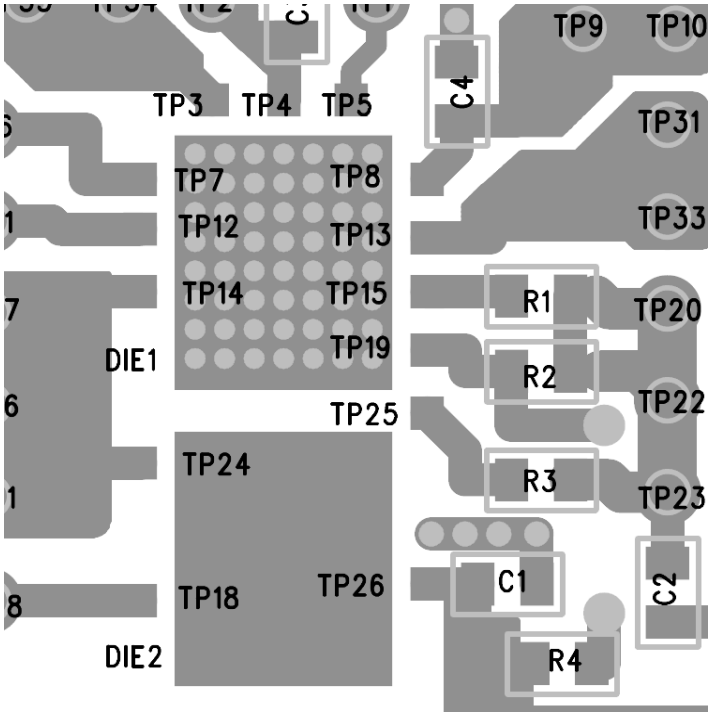
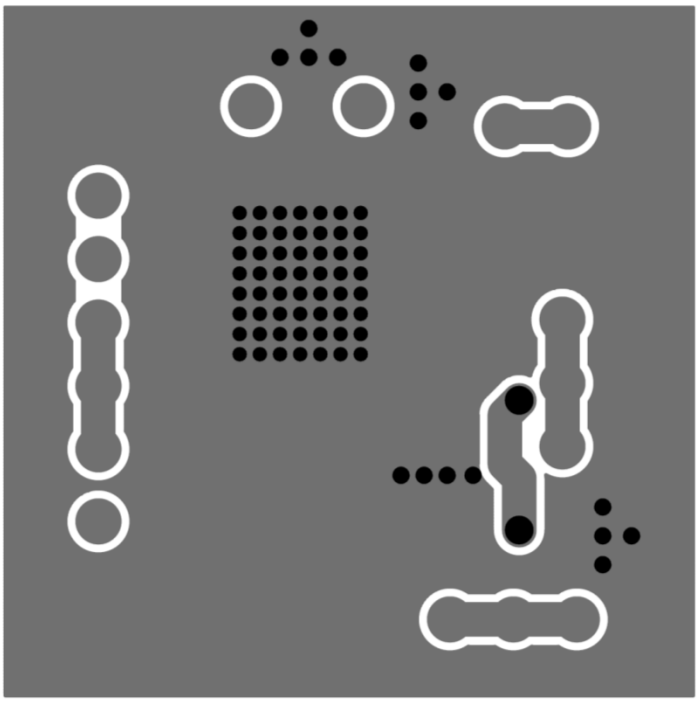


Fig. 6.2 Motherboard schematic for testing the gate driver. Courtesy of Oak Ridge National Laboratory [25].

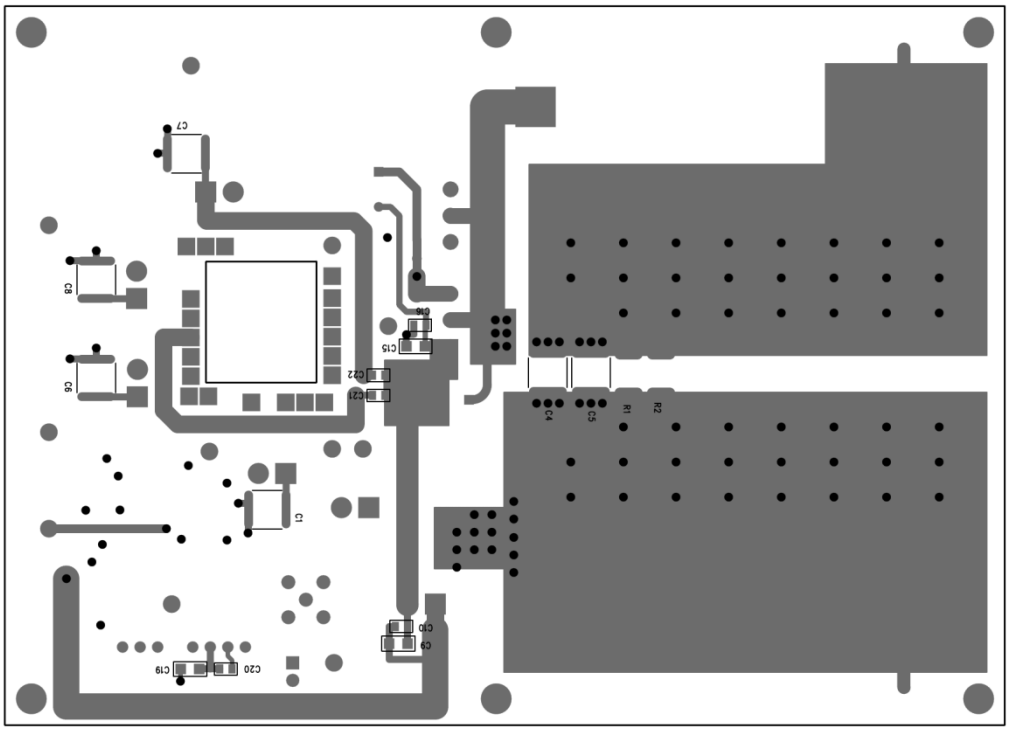


(a)

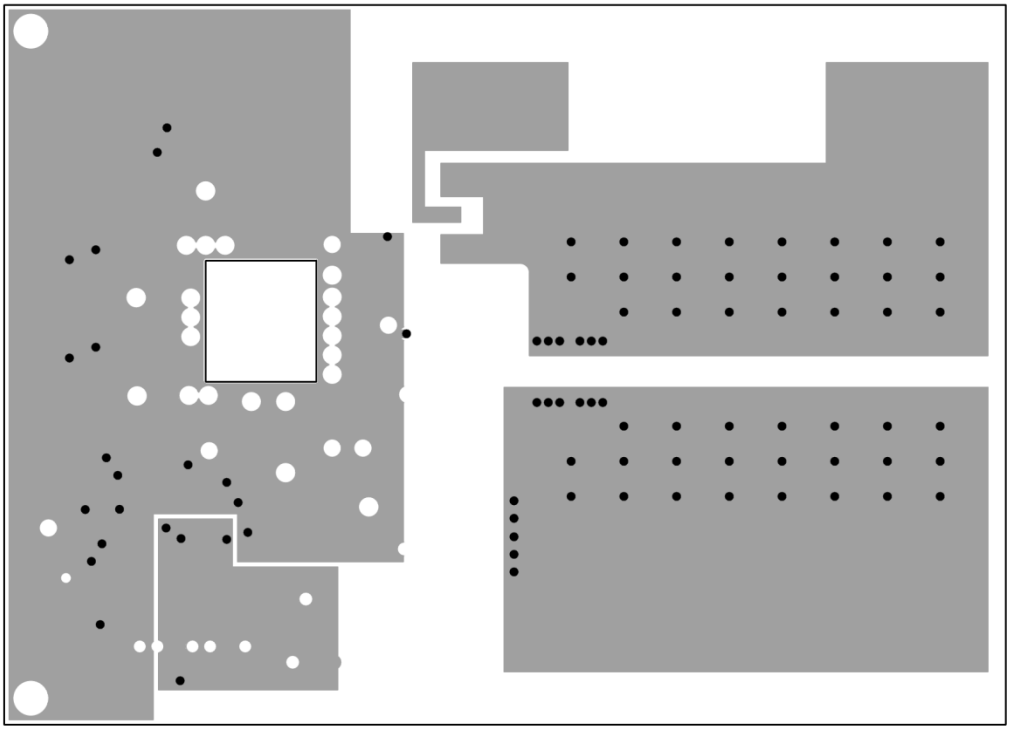


(b)

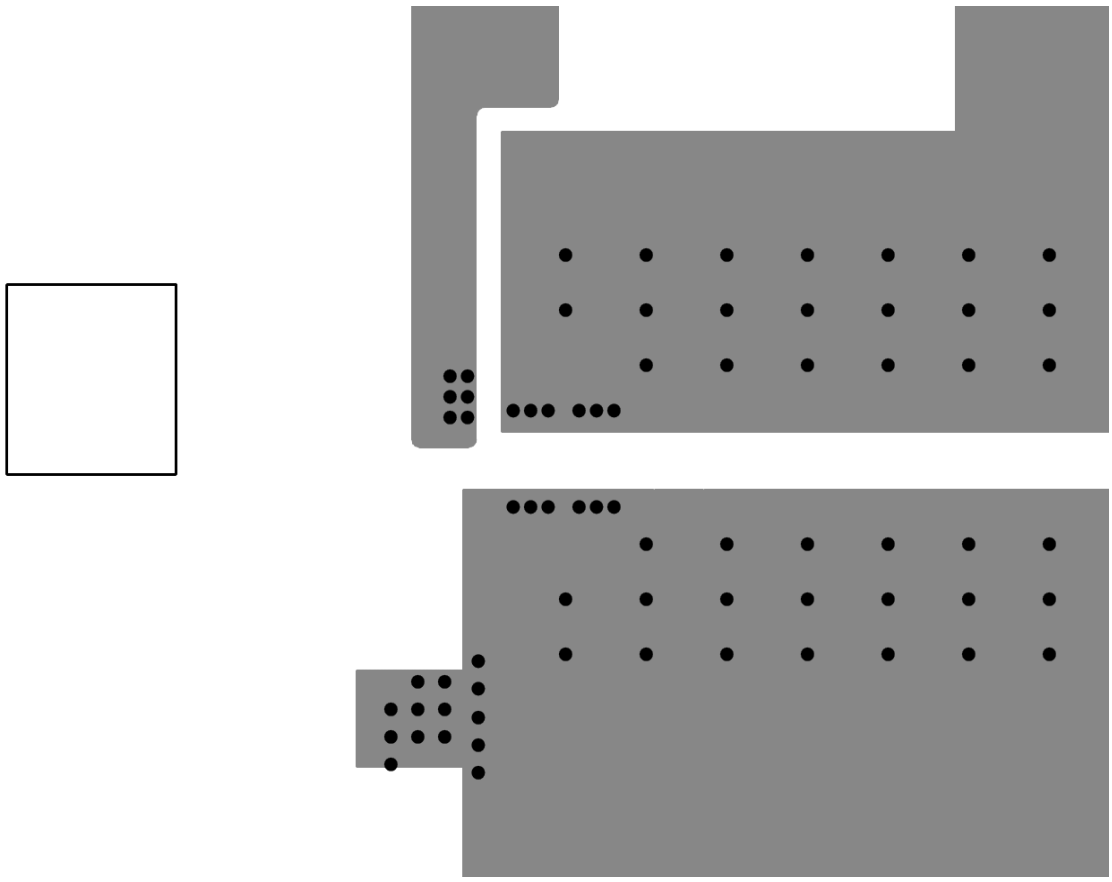
Fig. 6.3 Daughterboard layout (a) top (b) bottom. Courtesy of Oak Ridge National Laboratory [25].



(a)



(b)



(c)

Fig. 6.4 PCB layout of test circuit motherboard (a) bottom view (b) inner layer 2 (c) inner layer 3. Courtesy of Oak Ridge National Laboratory [25].

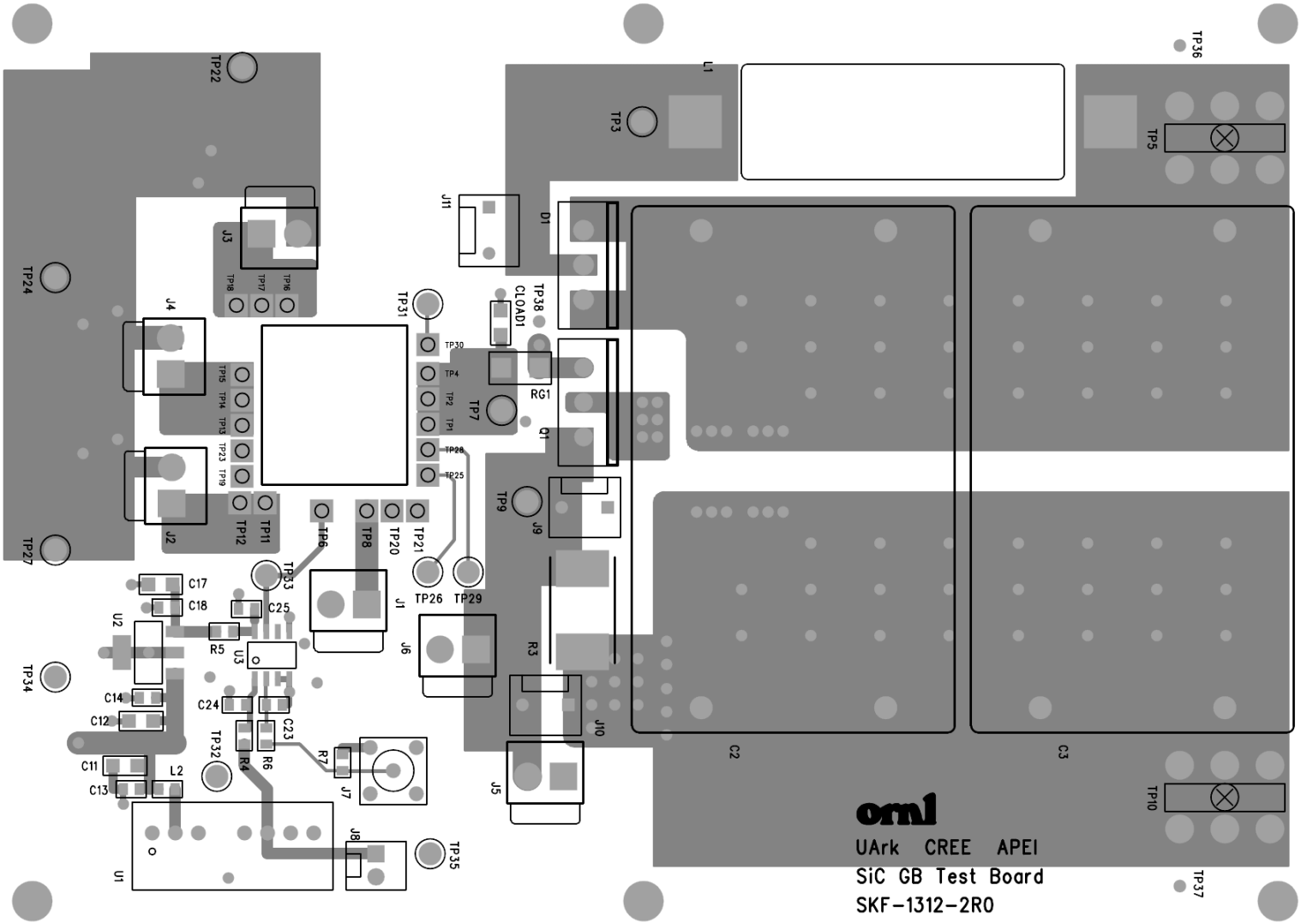


Fig. 6.5 Gate driver motherboard top layer. Courtesy of Oak Ridge National Laboratory [25].

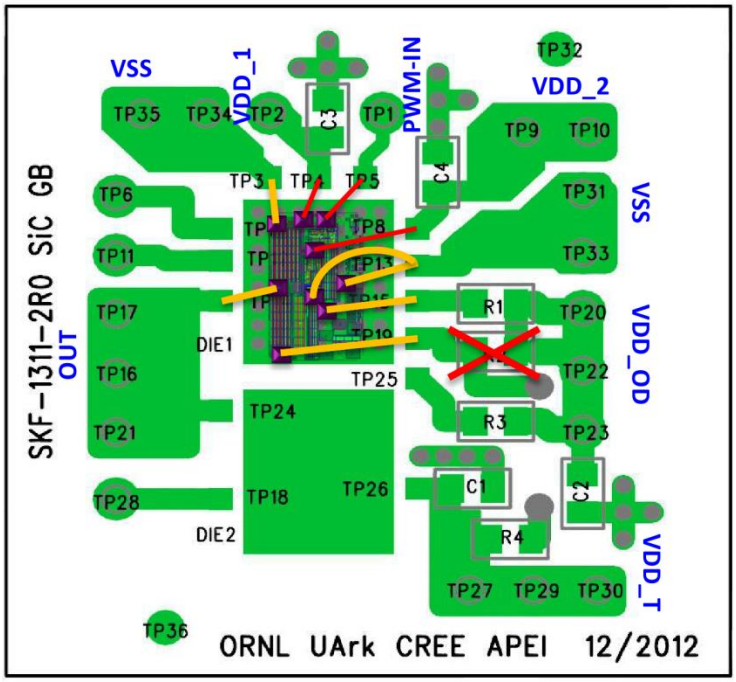


Fig. 6.6 Single chip gate driver die attach to daughterboard (yellow: thick, red: thin).

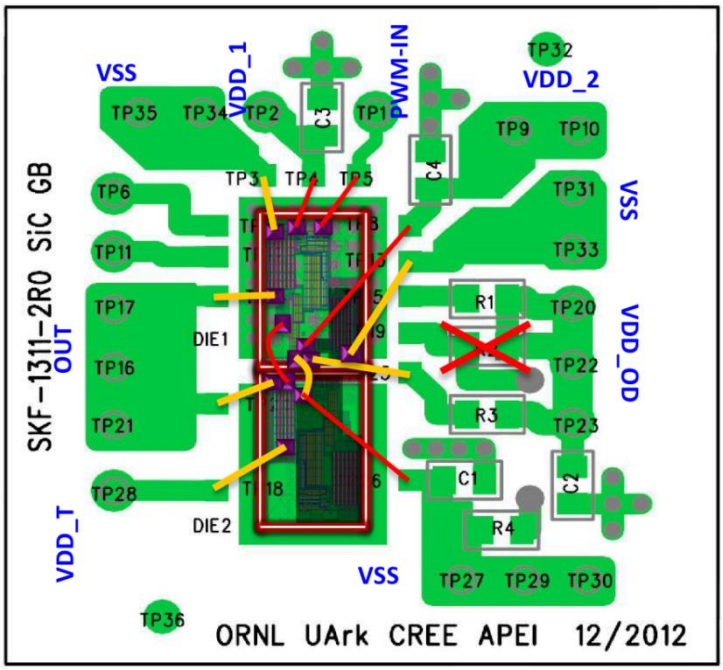


Fig. 6.7 Split chip gate driver die attach to daughterboard (yellow: thick, red: thin).

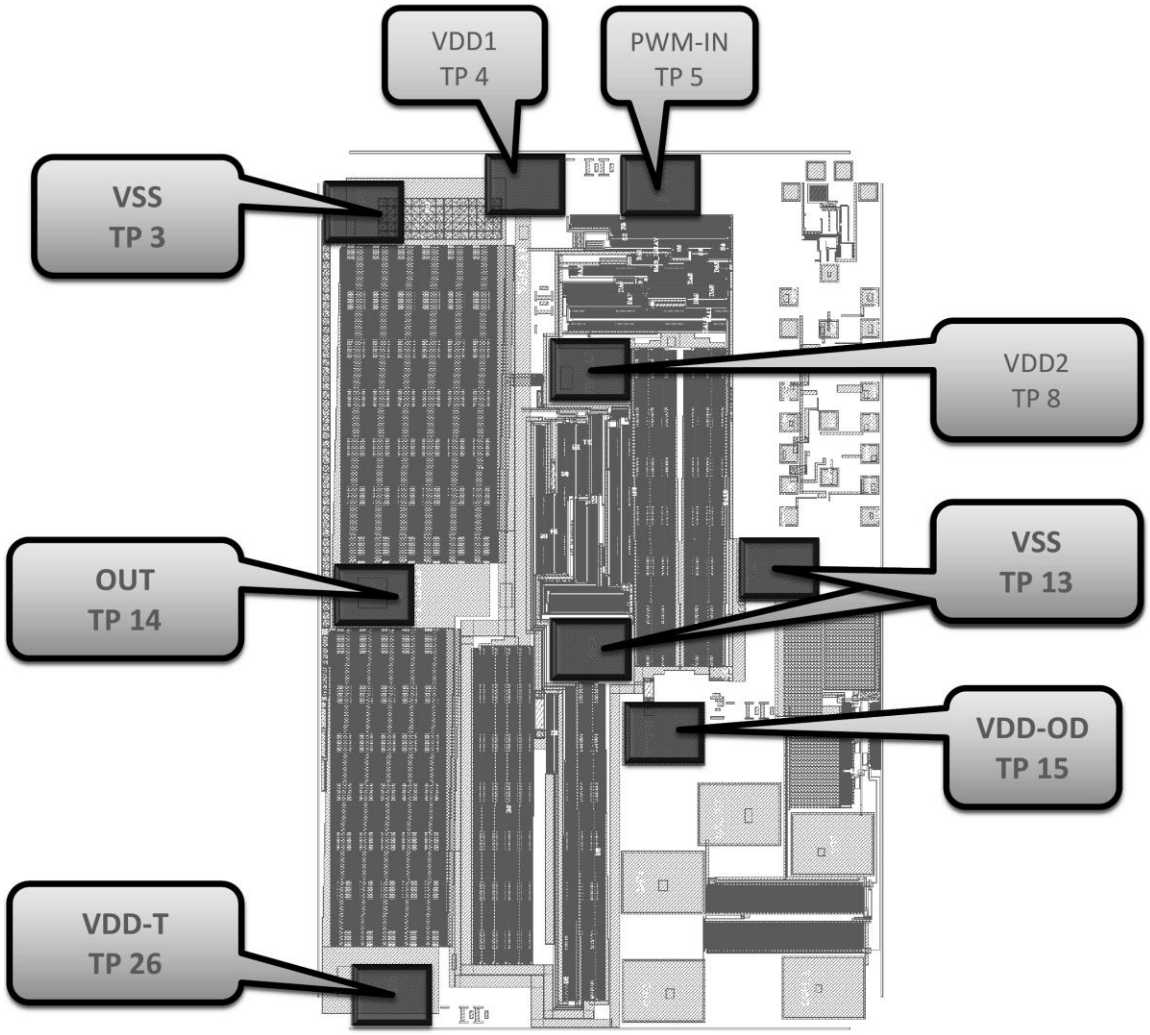


Fig. 6.8 Pin assignment and pad locations for single chip gate driver.

Fig. 6.6 and Fig. 6.7 delineate how the single chip design and split chip design gate driver dies are placed on the daughterboard respectively. The yellow wires represent thick wires (needs multiple bonds) that carries high amounts of current and the red wires represent thin wires which carries relatively small amounts of current (one bond wire is enough). Fig. 6.8 and Fig. 6.9 further illustrate how the single chip and split chip design gate driver pin assignment with the daughterboard (refer Fig. 6.3 (a)) is carried out.

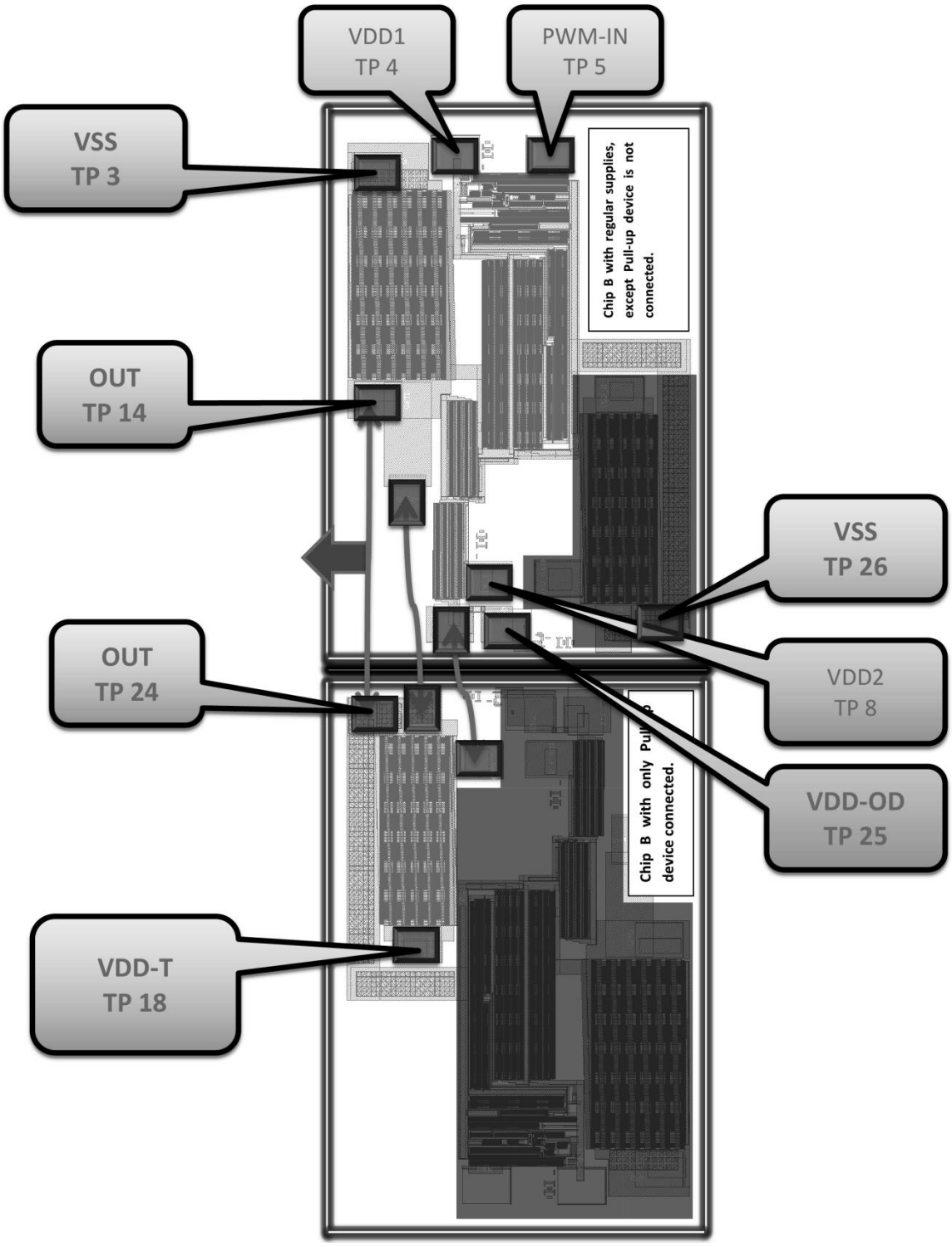
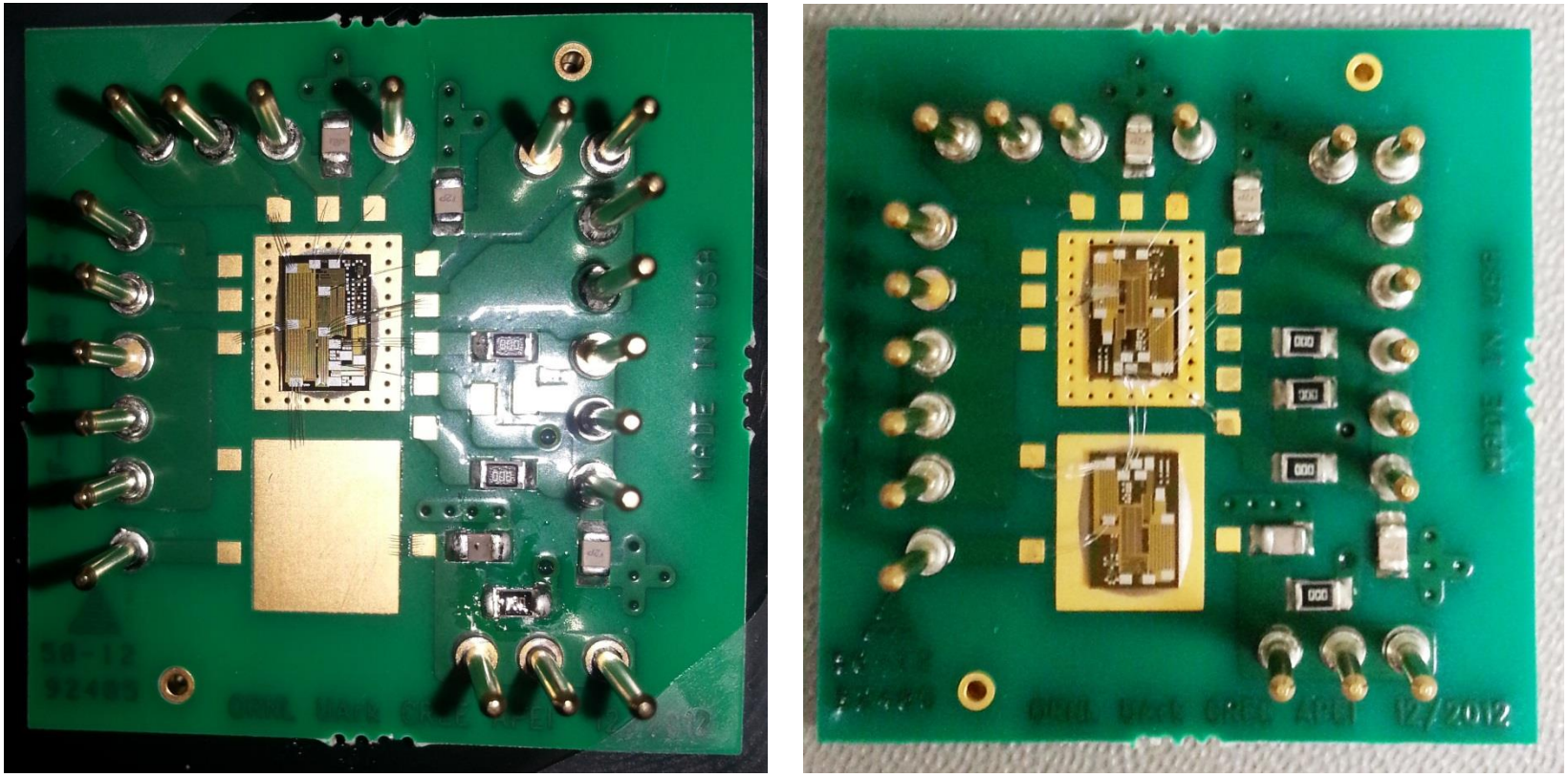


Fig. 6.9 Pin assignment and pad locations for split chip gate driver.



(a) **(b)**

Fig. 6.10 Die attached and wire bonded chips to the daughterboard (a) Single-chip (b) Split-chip.

(Lamichhane, Ranjan. February 2013. CSRC Lab. JPEG file.)

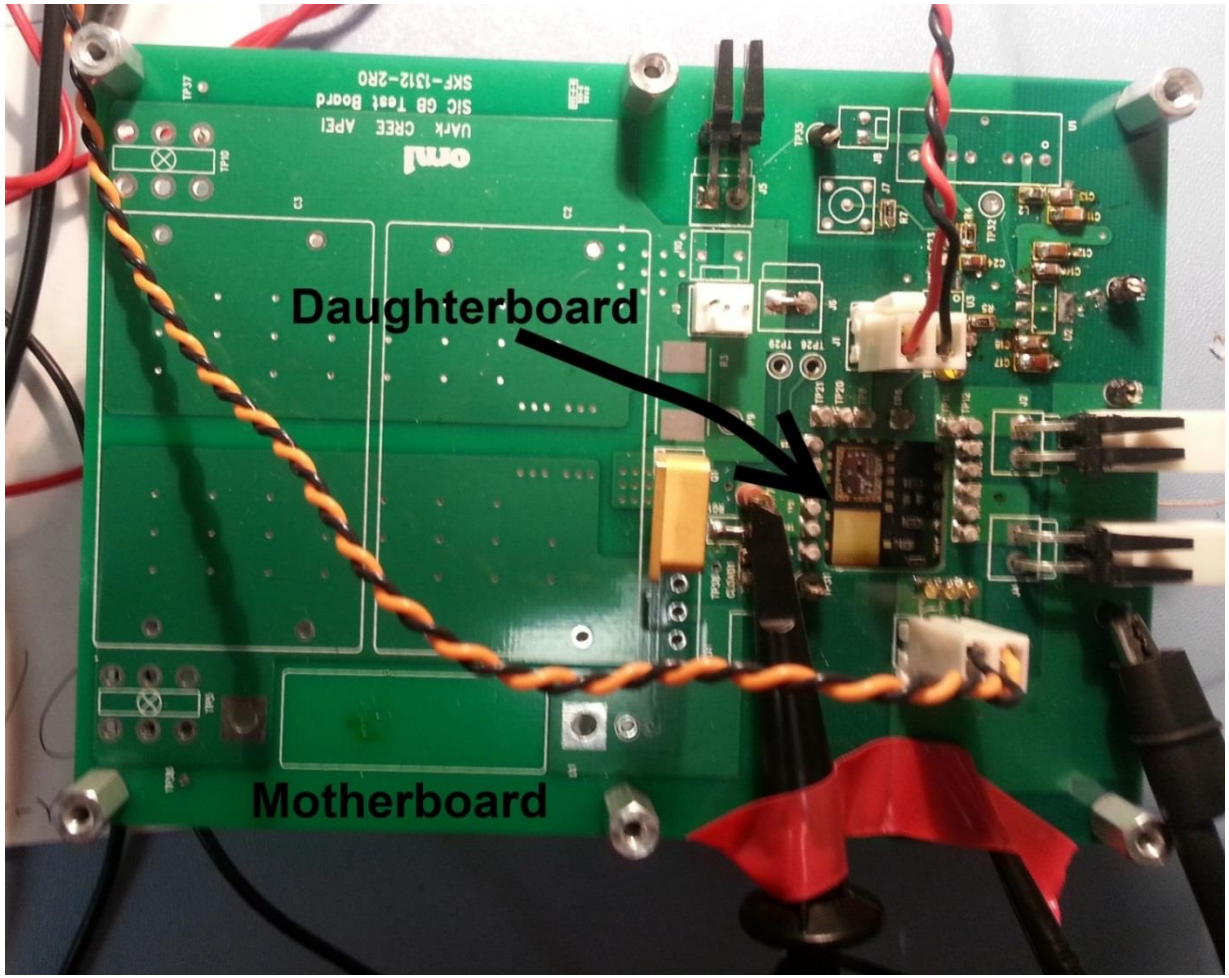


Fig. 6.11 Composite test setup with daughterboard and motherboard. The gate driver dies are attached and wire-bonded to the daughterboard.

(Lamichhane, Ranjan. February 2013. CSRC Lab. JPEG file.)

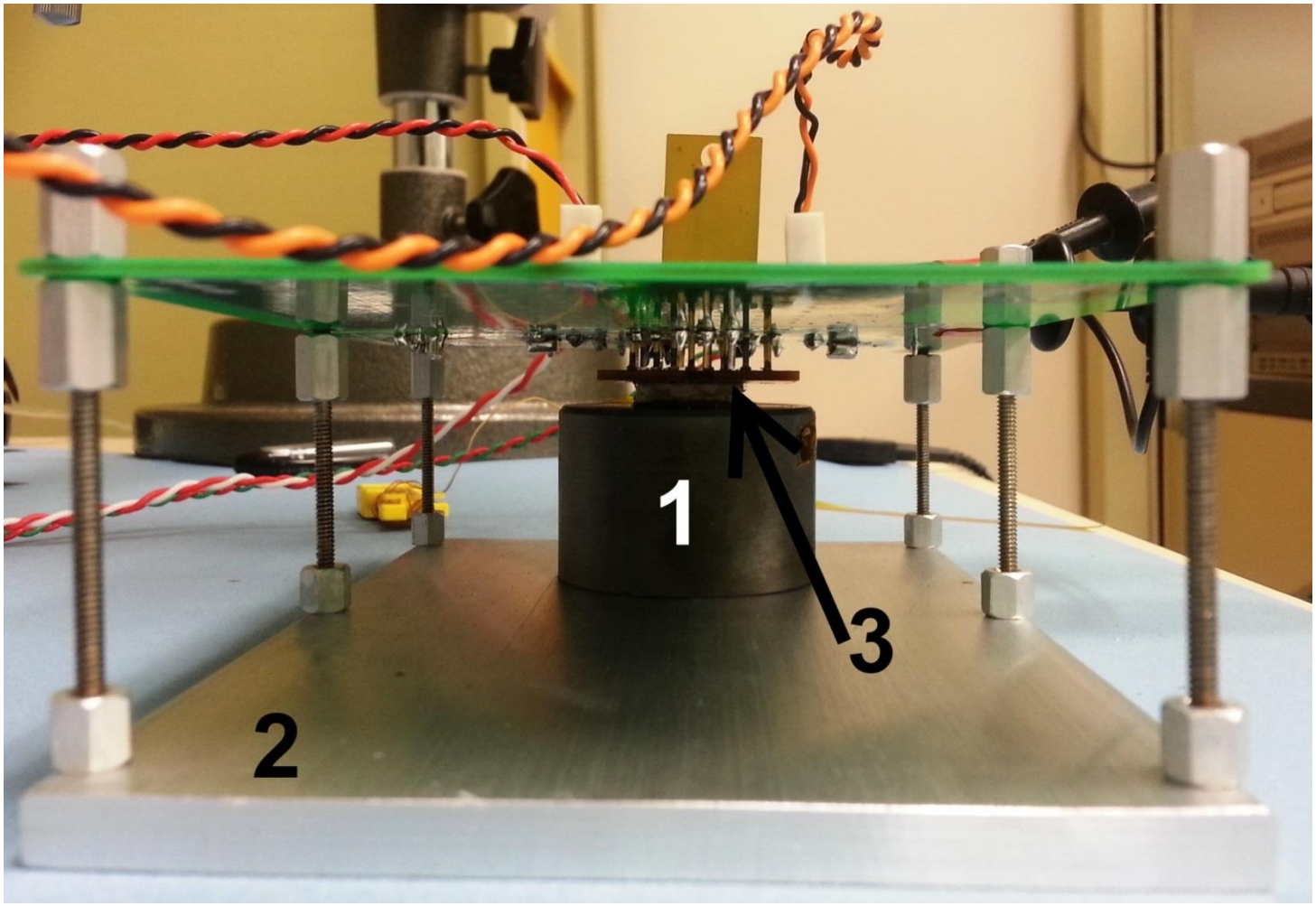


Fig. 6.12 The heat sink setup for heat dissipation (1) Copper cold finger (2) Heat sink setup (3) Cold finger and daughterboard interface where the thermal grease is applied.

(Lamichhane, Ranjan. February 2013. CSRC Lab. JPEG file.)

Fig. 6.10 (a) and (b) shows the single-chip and split-chip gate driver die attached and wire bonded to the daughterboard respectively. Fig. 6.11 shows the daughterboard attached with the motherboard which is populated with the capacitors and connection pins. Fig. 6.12 shows the thermal dissipation setup for the gate driver die. The copper cold finger touches the gate driver die with thermal grease in the contact gap to further promote the heat flow.

6.2 TEST PLAN DEVELOPMENT

The following test plan was developed, in collaboration with ORNL and APEI, to test the gate driver.

1. Install the cold finger and thermocouple to be in contact with the bottom of the daughter board. The thermocouple is placed in the slot at the interface between the cold finger and the daughter board, and thermal grease is applied at this interface.
2. Set voltage supply source values (with appropriate current limiting values), disable the supply outputs, and connect supplies to the test motherboard PCB.
3. Set the input drive signal for square wave of 0-5 V, 18 ns rise and fall time, 500 kHz, and 50% duty cycle.
4. Configure the motherboard gate driver load as a SiC MOSFET
    - Solder a Gen 1 SiC MOSFET (CMF20120D as the load).
    - Short Rg1 (0 Ω).
5. Disable the power supply outputs and input drive source to the motherboard. Insert the daughterboard to be tested into the motherboard. Note that the daughterboard should be uniquely labeled. The chip number, design type, and wafer identification should be recorded for each daughterboard tested.

6. Enable the power supply outputs and the input drive signal source. Order of powering ON the sources is important, or else the device might be damaged. Power ON the input source, then power ON the VDD and then power ON the 2VDD. Sticking with this powering sequence is important because otherwise the devices in the overdrive circuit might see high voltages across them which might damage those devices.
7. Record the gate driver input signal rise time, fall time, Vmax, and Vmin (as defined in 8.)
8. Record the data from the gate driver output ('OUT' - TP38 or J11 for SiC power-MOS) and record waveforms for each setting.
    - Rise and Fall Time (10% to 90% and 90% to 10%)
    - Vmax and Vmin (output 'zero' level and *high* level after settling)
    - Time delay from the input signal (PWM-IN) to the output (OUT) for the rising and falling edges (time difference from 50% point of the two waveforms)
9. Record the current drawn from each of the voltage supplies for each setting.
10. Monitor and record the temperature of the package during testing (thermocouple and IR when applicable). Some time may be required for temperature settling.
11. Hold the output low (0% duty cycle) and measure the current drawn from each of the voltage supplies to determine the maximum power consumption during a standby condition.
12. Perform steps 8-11 for different power mode configurations.
13. Repeat 12 for the case when the cold finger is not installed and the device has been operating under normal conditions for 1 minute, 5 minute and 10 minutes after initial startup.

- Be careful that a thermal runaway doesn't occur – closely monitor the thermocouple temperature.

14. Change daughter cards and retest. Additional testing at higher loads should be performed after all drivers have been characterized using a single MOSFET load. The loads associated with these additional tests still need to be specified.
15. Repeat 8-13 for a capacitive load of 4000 pF.
    - Measure two 2000 pF capacitors and record the values.
    - Install the two capacitors in parallel in Cload1 and remove Rg1.
    - A single 3900 pF capacitor could be used if agreed upon as it is a standard value.
    - Remove Rg1 and measure "OUT" node to "VSS-GB" to obtain rise/fall data
16. Maximum overdrive voltage tests should also be performed to determine the voltage where the gate driver fails, if desired. These tests should also be thoroughly documented and performed when all other tests have been completed and the test circuits can be tested to failure.
17. Perform controlled elevated temperatures tests and use specifics associated with dT to determine the actual die temperature. (Temperature gradient dT is the difference between the die and thermocouple temperature calculated by APEI).

NOTE: These steps will be followed for both single chip design and split-chip design.

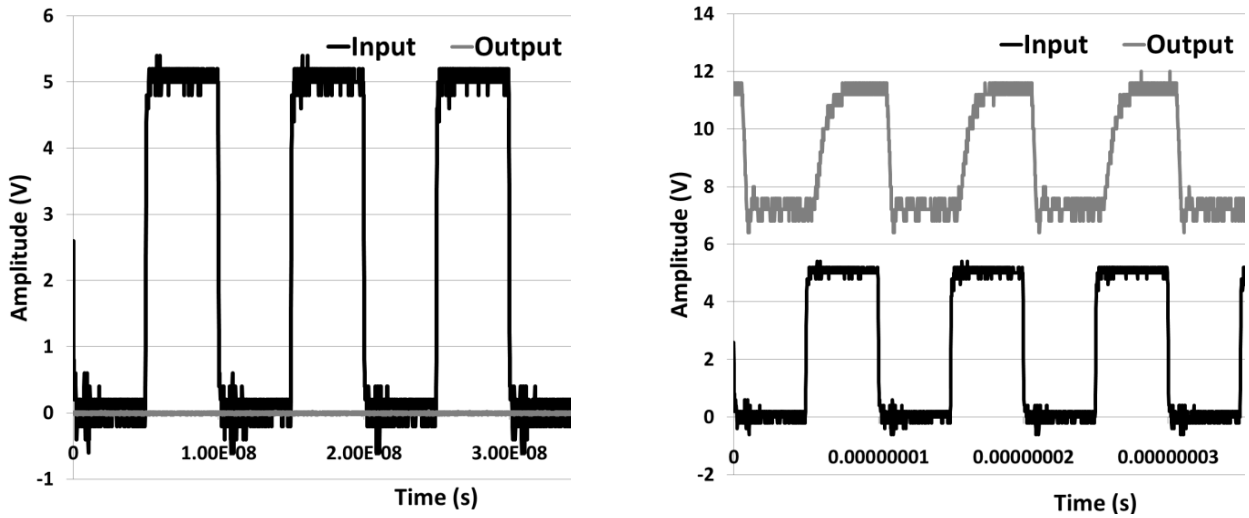
The equipment required for the testing procedure is listed in Table 6.1.

Table 6.1 Equipment Required for Testing the Gate Driver

Equipment	Description	Remarks
HAMEG Programmable Power Supply HM7044	Supply VDD1, VDD2, and VDD_OD	- Able to supply high current at high voltages - GPIB Compatible
Agilent E3631A Power Supply	Supply VDD_T	- Able to supply high current - GPIB Compatible
Fluke 73 Digital Multimeter	Measure and Verify Power Levels and Resistances	
Tektronix AFG 3022B Function Generator	Supply Input PWM Waveform	- Up to 50 MHz - Transition time up to 18 ns
Tektronix TDS 744A Oscilloscope	Observation of Waveforms	- GPIB Compatible
VICHY VC99 Multimeter	Temperature Sensor	- Thermocouple Input
Cole-Parmer StableTemp Hot Plate	Hot Plate for Temperature Testing	- Ceramic Top

7. DEBUGGING AND RECTIFICATION

Both of the gate driver chips didn't show expected outputs when they were tested with the devised test procedure. Checking and rechecking didn't yield any better result.



(a) **(b)**

Fig. 7.1 Input/output waveforms obtained during first data reading.

(a) Single chip (b) Split chip

As can be seen in Fig. 7.1, the output waveforms are nowhere close to what was expected of the gate driver output and what the simulations showed them to be. The power supply levels of the gate driver were changed, input signals were altered and waveform data on these different situations were observed without any progress on identifying the problem with the circuit. Because of the lack of progress by using testing set-up for debugging, the chips were monitored under the probe station where high visual magnification levels were accessible for debugging purposes. The chip designs were also tracked back to layout on Cadence Virtuoso in search for any possible explanation on why the chips were acting strangely.

7.1 SINGLE CHIP GATE DRIVER DEBUGGING

When the single chip gate driver was being rigorously inspected under the probe station, an unusual spot was noticed on the chip. The point of interest is the white circled area in Fig. 7.2. The zoomed view of this defect can be seen in Fig. 7.3.

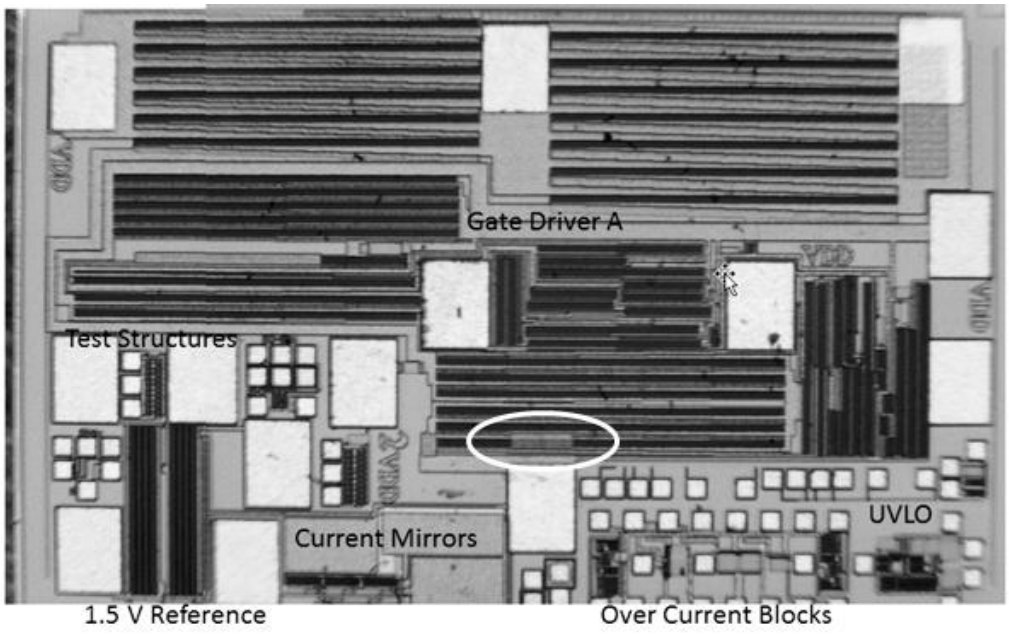


Fig. 7.2 Picture of the die of fabricated single chip gate driver (problem area is circled). (Franics, Matt. January 2013. ENRC Lab. JPEG file.)

Fig. 7.3 Zoomed view of the defect under probe station (problem area is circled).

(Lamichhane, Ranjan. February 2013. CSRC Lab. JPEG file.)

It’s visible how a row of transistors is lacking in the highlighted area in Fig. 7.3. This was a strange discovery and prompted a check on the Cadence Virtuoso layout to determine further explanation. When the final layout file in the Cadence Virtuoso was checked, nothing errant was found and everything seemed to be working and simulating as expected. Then, after some brainstorming, it was determined that the next step would be to check on the final system level integrated layout that was sent to Cree for fabrication. This yielded the explanation to the entire problem. An overlaying stray extraneous rectangular metal polygon was discovered at the system level layout. The culprit metal polygon can be clearly seen after the gate driver is deleted from the system level integrated layout in Fig. 7.5. Also, from Fig. 7.4, it can be clearly seen how this extraneous metal polygon overlays an array of transistors in that row of gate driver shorting their gate, source and drain; and ruining the entire gate driver functionality.

This shorted device is transistor *DA12* of the *single edge delay circuit* in Fig. 4.8. This would cause the *s2s* signal (refer to Fig. 4.1 and Fig. 4.8) to be connected with ground all the time which would eventually cause the transistor in the *biased common-gate overdrive circuit* to be ON all the time (refer to Fig. 4.1). This causes the signal *totem-up* to be pulled-down to ground always which forces *M0* to be OFF all the time and, hence, the final output never rises. This is exactly the case in Fig. 7.1 (a). In summary, this extraneous metal polygon shorts the gate of the pull-up device in the *totem-stage* to ground. This extraneous metal polygon slipped through in the integrated design during the chip integration phase as a result of not performing pad-to-pad layout versus schematic (LVS) analysis.

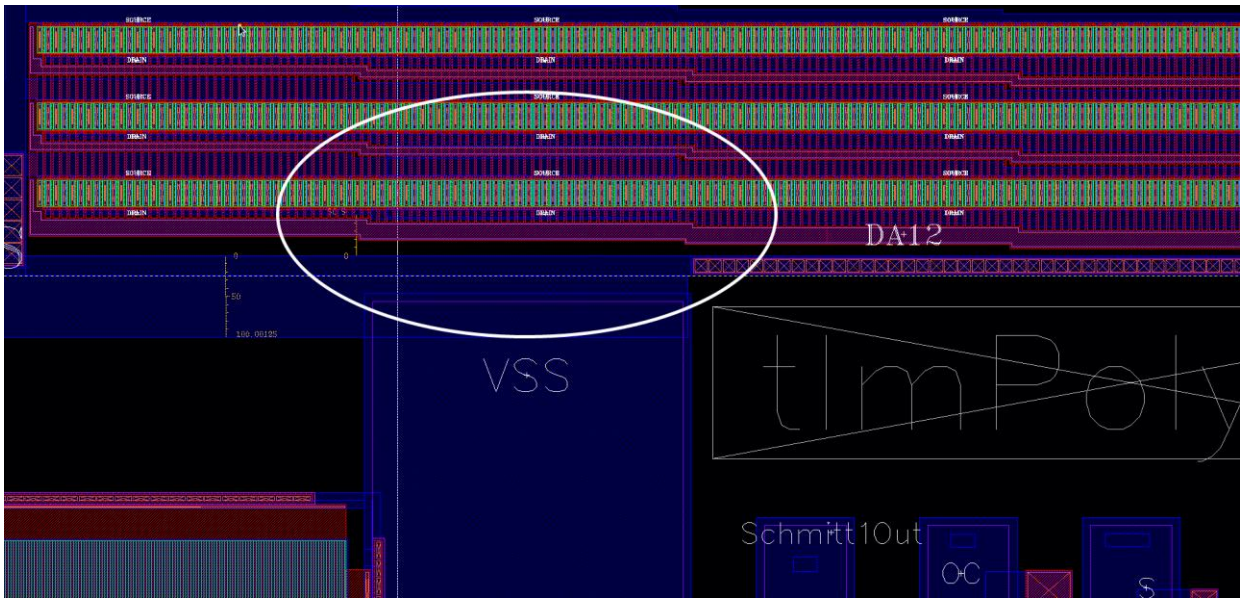


Fig. 7.4 Integrated system layout with single chip gate driver.

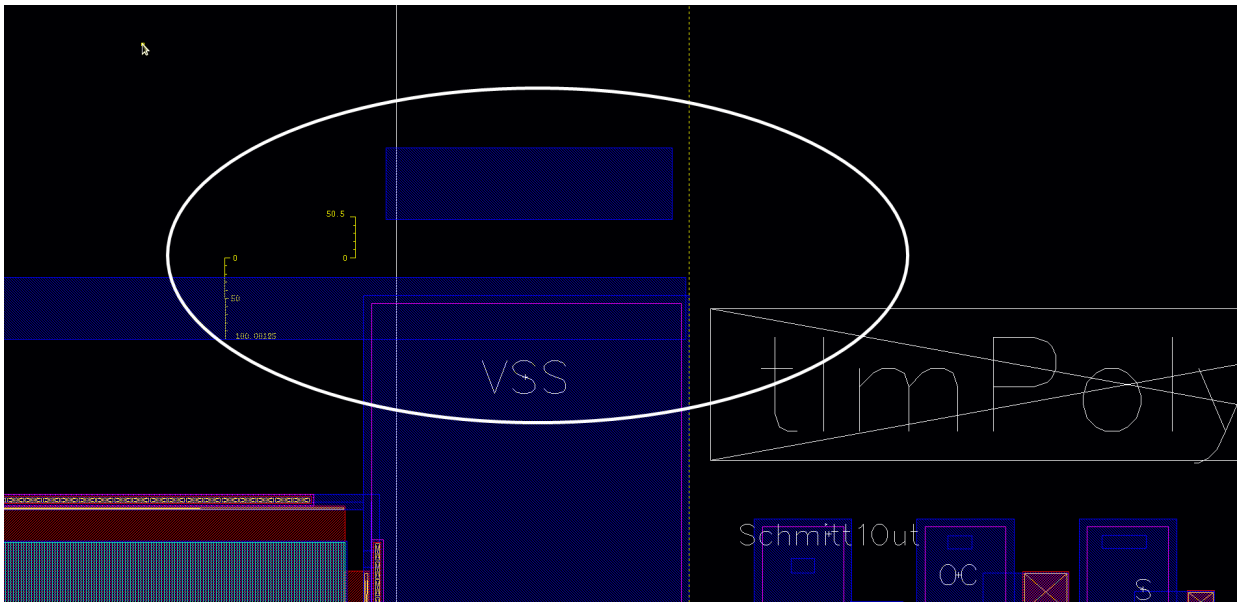


Fig. 7.5 Integrated system layout without the single chip gate driver.

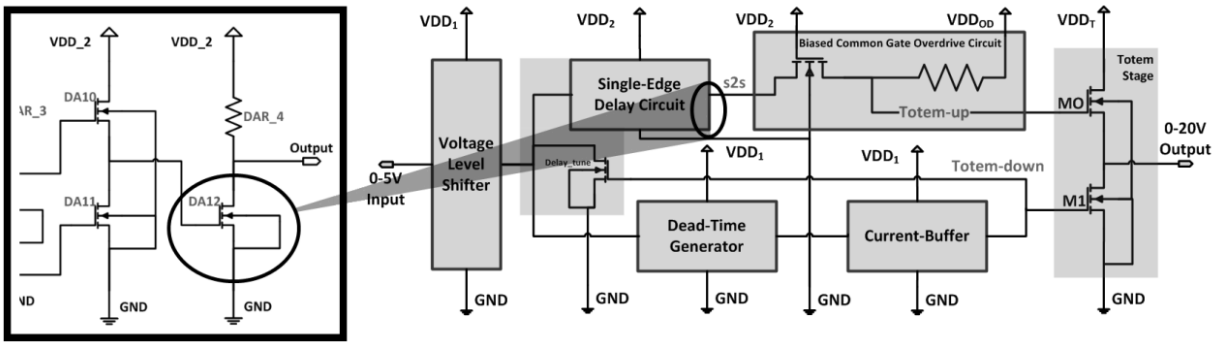


Fig. 7.6 The victim transistor due to extraneous metal polygon (refer Fig. 4.8 for the circuit on the left, enclosed in the black box, and Fig. 4.1 for the circuit on the right).

7.2 SPLIT CHIP GATE DRIVER DEBUGGING

In case of the split chip gate driver design, nothing could be discovered from visual inspection using the probe station. A number of tests were performed on this gate driver to determine the problem. The tests shown in Fig. 7.8 are carried out in the probe station. The probe station used is capable of supplying signal to the pads and sensing signals from the pads on the die, with the help of force ports and sense ports respectively driven by a Keithley semiconductor characterization system. Fig. 7.7 clearly shows the equipment used for the tests to be carried out as per Fig. 7.8.

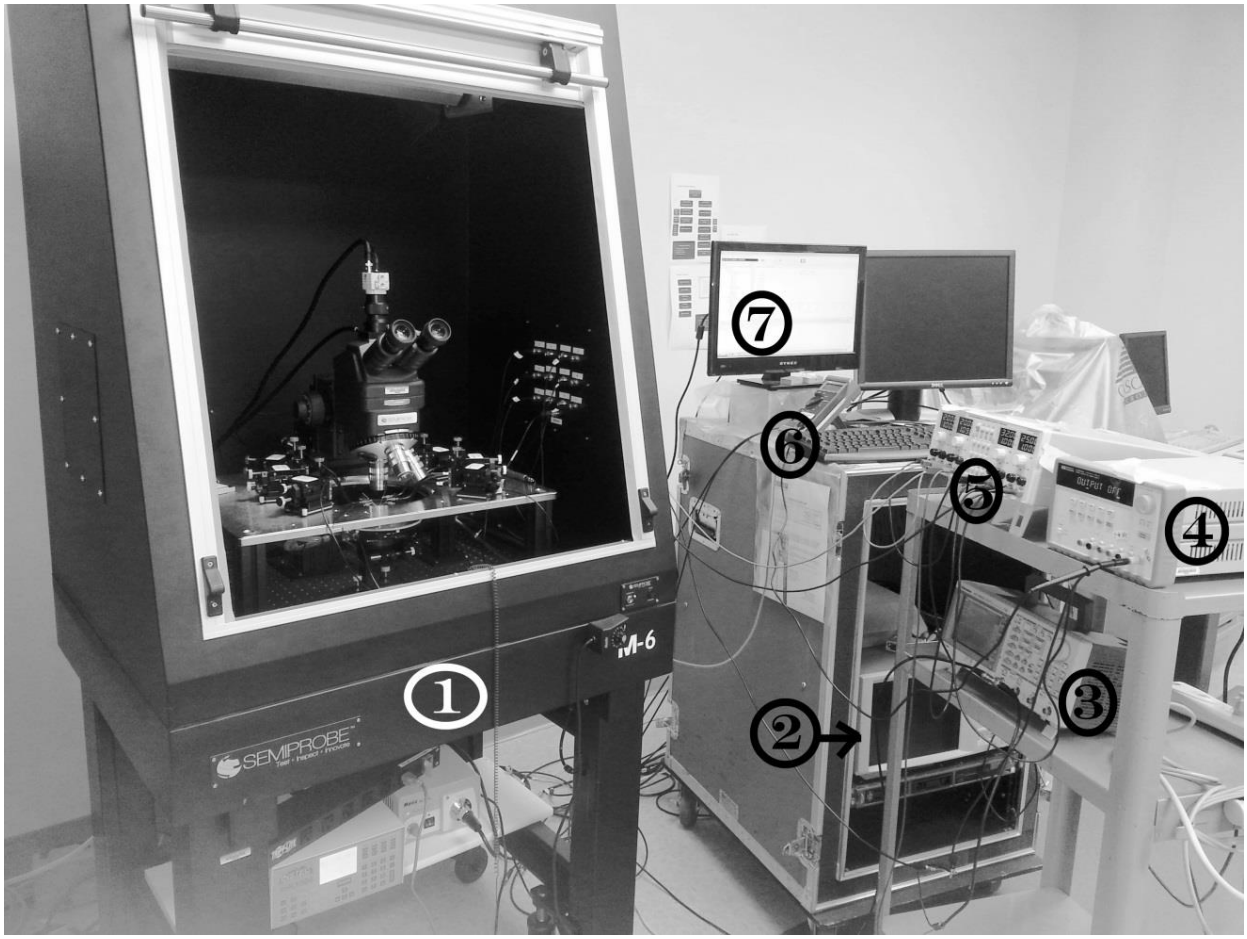
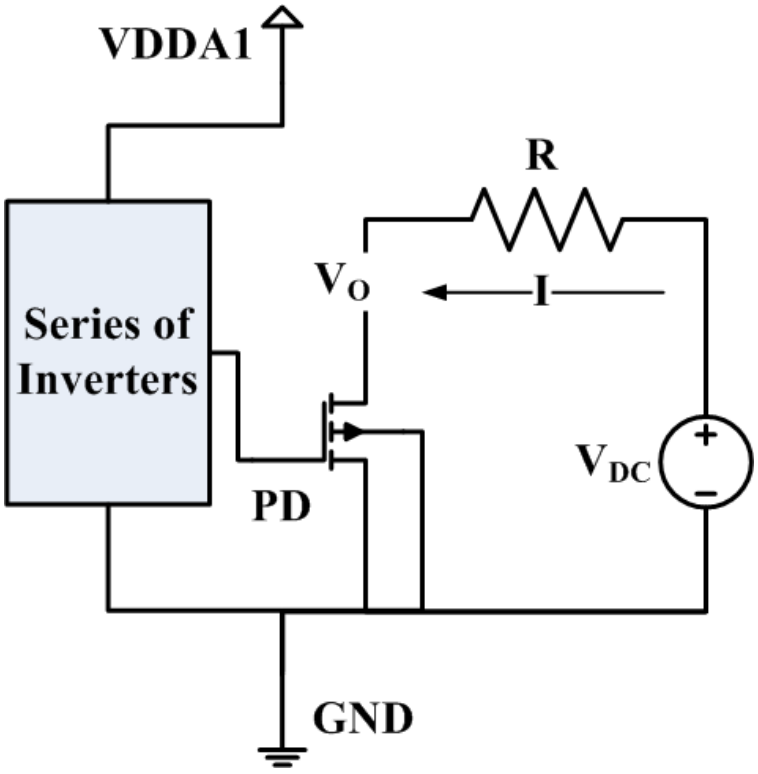
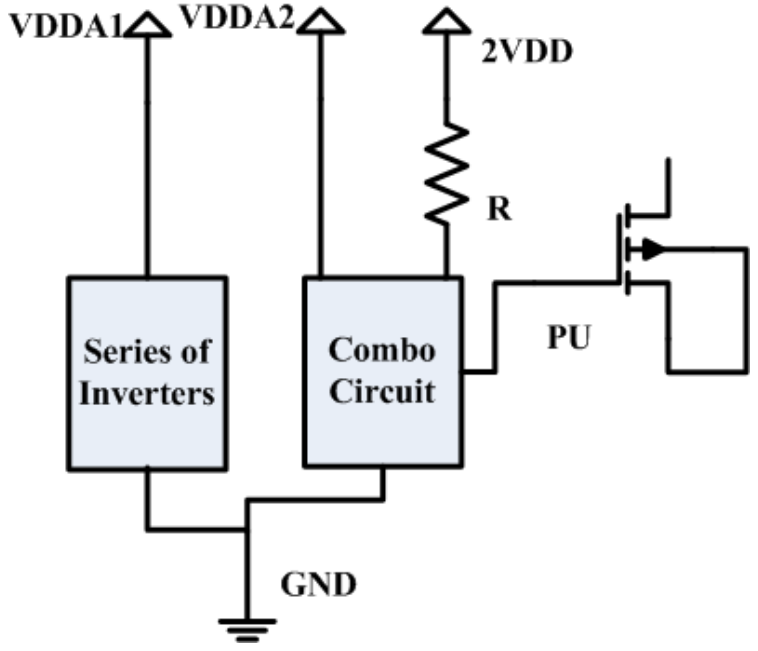


Fig. 7.7 Probe station test setup (1) Probe station (2) Keithley semiconductor characterization system (3) Tektronix function generator (4) Agilent power supply (5) HAMEG programmable power supply (6) Fluke multimeter (7) Keithley characterization software.

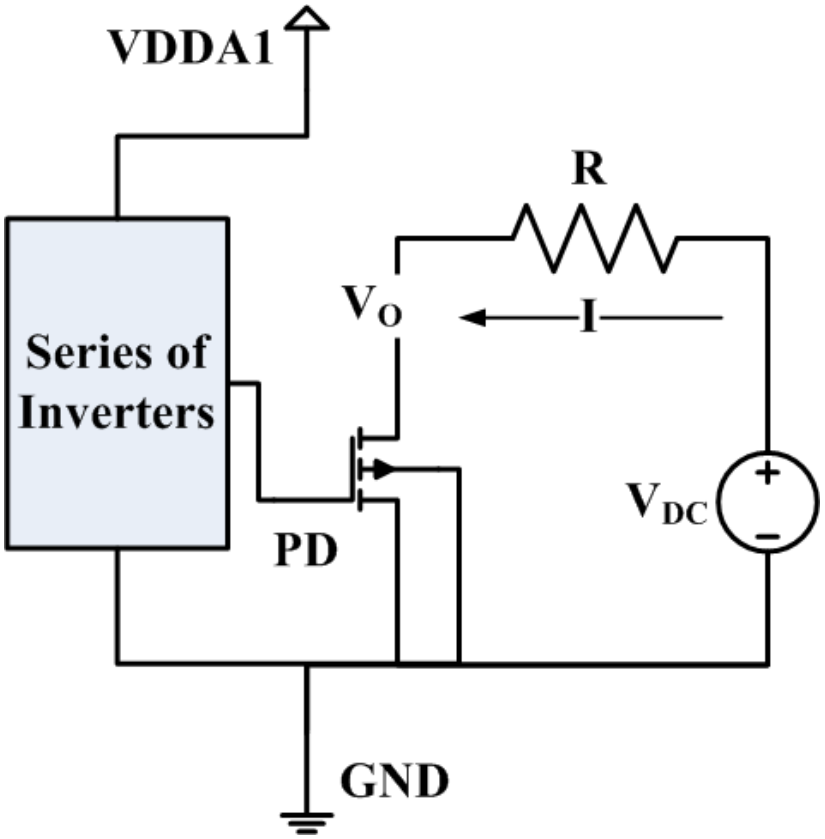
(Lamichhane, Ranjan. February 2013. CSRC Lab. JPEG file.)


VDDA1
R
Series of Inverters
V_O
I
V_{DC}
PD
GND

(a)


VDDA1
VDDA2
2VDD
R
Series of Inverters
Combo Circuit
PU
GND

(b)



(c)

Fig. 7.8 Tests carried out to debug split chip gate driver design (a) Totem-up signal test (b) Pull-up device test (c) Pull-down device test.

First of all, data from the gate of the pull-up device, which is signal *totem up* in Fig. 5.1, was measured, by probing the signal that goes to the gate of the pull-up device located in a separate die, and was found to be consistent with the requirement. The set up as shown in Fig. 7.8 (a) was used for this investigation. The data in Table 7.1 proves that signal at gate of pull-up device has the required fidelity. This also means that *totem down* signal in Fig. 5.1 is consistent with simulation results because *totem down* signal generates the *totem up* signal and if the *totem up* signal is consistent with our expectations so must be the *totem down* signal.

Table 7.1 Results obtained with test configuration in Fig. 7.8 (a).

V_{IN} (V)	VDD_1 (V)	VDD_2 (V)	VDD_OD (V)	I_1 (A)	I_2 (A)	I_{VDD_OD} (A)	GPU (V)	R (Ω)
0	15	15	30	22m	5m	124m	**2.8**	0
8	15	15	30	49m	0	0	**30**	0

For the next test, the source of the pull up device on the *totem stage* was shorted to ground and a constant voltage was applied to the drain using voltage source as shown in Fig. 7.8 (b). The pull-up device will be used as a pull-down device and the 135 Ω resistor *R* will be used as a pull-up device in this set-up. This test set-up is to primarily check the operation of the pull-up device. The data in Table 7.2 indicates that the output impedance of the transistor decreases with the increase in gate voltage which is a predicted outcome and it can be inferred that the pull-up device is functioning as expected.

Table 7.2 Results obtained with test set up in Fig. 7.8 (b).

V_{GATE} (V)	V_{TEST} (V)	V_{SOURCE} (V)	V_{DRAIN} (V)	I_{TEST} (A)	R (Ω)	Z_{PU} (Ω)
0	20	0	20	0	135	∞
5	20	0	19.75	2m	135	**9.8K**
20	20	0	19.11	7m	135	**2.7K**

For the final test, the pull-down device is used as a pull-down device and the 135 Ω resistor *R* is used as a pull-up device as shown in Fig. 7.8 (c). This test set up will investigate the working of pull-down device. As can be seen in Table 7.3, the V_O and Z_{PD} data obtained from the test results are starkly inconsistent to expected behavior.

It has been verified from test in Fig. 7.8 (a) that the totem-down signal is consistent with expectations. Given that condition, in Table 7.3, the V_O must be close to V_{DC} (I being 0) when *Vin* is *high* and V_O must be close to ground voltage (I must have high value) when V_{IN} is *low*; since totem-down is an inverted V_{IN} and is applied at gate of pull-down device. And similarly, Z_{PD} must be very large and very small respectively when V_{IN} is *high* and *low*. But, clearly that is not the case. So, there must be something wrong with the pull-down device.

Table 7.3 Significant Results Obtained With Test set up in Fig. 7.8 (c)

V_{IN} (V)	VDD_1 (V)	VDD_2 (V)	I_1 (A)	I_2 (A)	V_{DC} (V)	R (Ω)	I (A)	V_O (V)	Z_{PD} (Ω)
5	15	15	40m	0	5	135	26m	1.36	52
0	15	15	30m	6m	15	135	63m	6.42	102
8	15	x	48m	x	x	135	x	0.1	x
8	20	x	68m	x	x	135	x	0.15	x
0	20	x	93m	x	x	135	x	5.6	x
0	15	x	43m	x	x	135	x	4.8	x
0	10	x	17m	x	x	135	x	3.6	x
0	5	x	0	x	x	135	x	1.5	x
0	4	x	0	x	x	135	x	1.0	x
0	3	x	0	x	x	135	x	0.5	x

The result from this test in Fig. 7.8 (c) is very confusing because of the erratic nature of data obtained. After contemplating the data observed in this table, a pattern was discerned. In the Table 7.3, data from row 3 and below exhibit an interesting behavior. A *high* in V_{IN} forces a low in the output (drain of pull-down device), and a *low* in V_{IN} forces some potential at the drain of pull-down device. This behavior of output voltage V_O is absolutely antithetical to expectations.

Furthermore, as we decrease the supply rail voltage magnitude of VDD_1, when V_{IN} is *low*, we see that the drain potential (V_O) of pull-down device decreases with it. This behavior would make sense if somehow there's a connection between the gate and drain of the pull-down device. Because the gate of pull-down device (which is totem-down signal) would go high when V_{IN} goes *low* and vice versa; and also if the VDD_1 decreases, the gate potential of pull-down transistor will decrease with it (refer Fig. 5.1). The signal V_O in Table 7.3 is proportional to this gate voltage at pull-down device. This study incites a hypothesis that there must be some connection between the gate and drain of the pull-down device.

With this new hypothesis, the layout file in Cadence Virtuoso was checked and re-simulated for consistency. The final layout file passed DRC, LVS test and simulated without any issues. Then the final system level integrated layout that was sent for fabrication was inspected closely around the pull-down device. Nothing amiss was discovered when the system level layout was inspected as can be seen in Fig. 7.10 (a). But when the gate-driver block is deleted from this integrated layout, as in Fig. 7.10 (b), then an extraneous metal rectangular polygon is starkly visible, similar to the one discovered in single chip gate driver design. This extraneous metal polygon slipped in the integrated design during the chip integration phase.

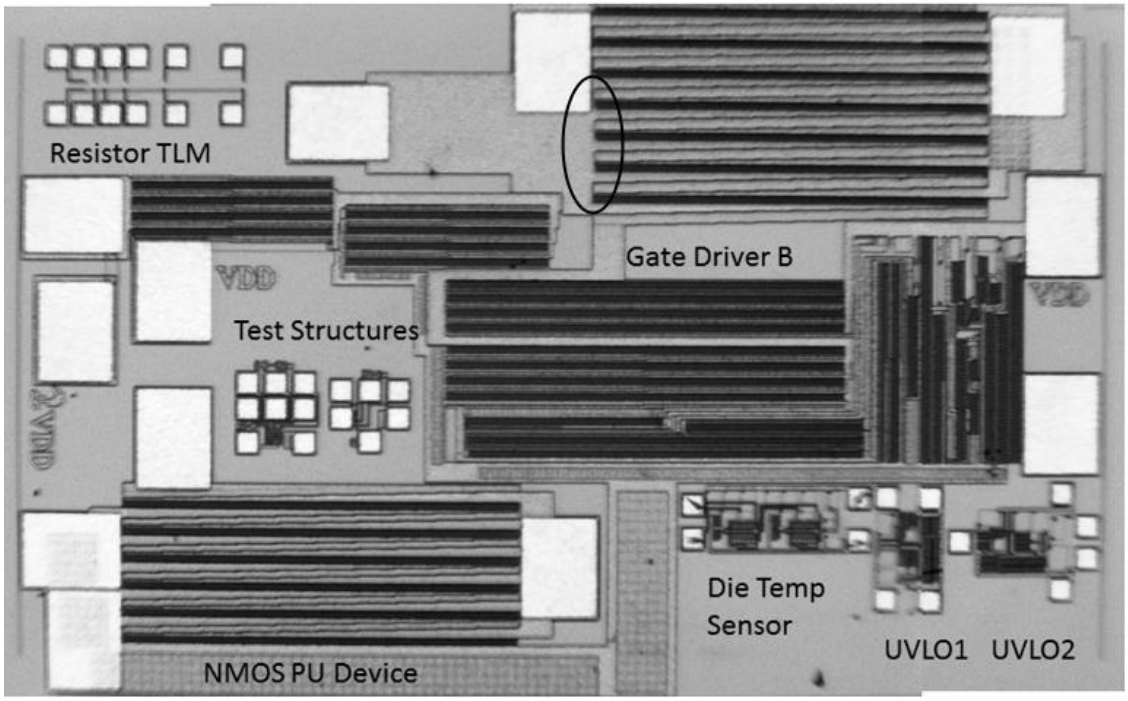
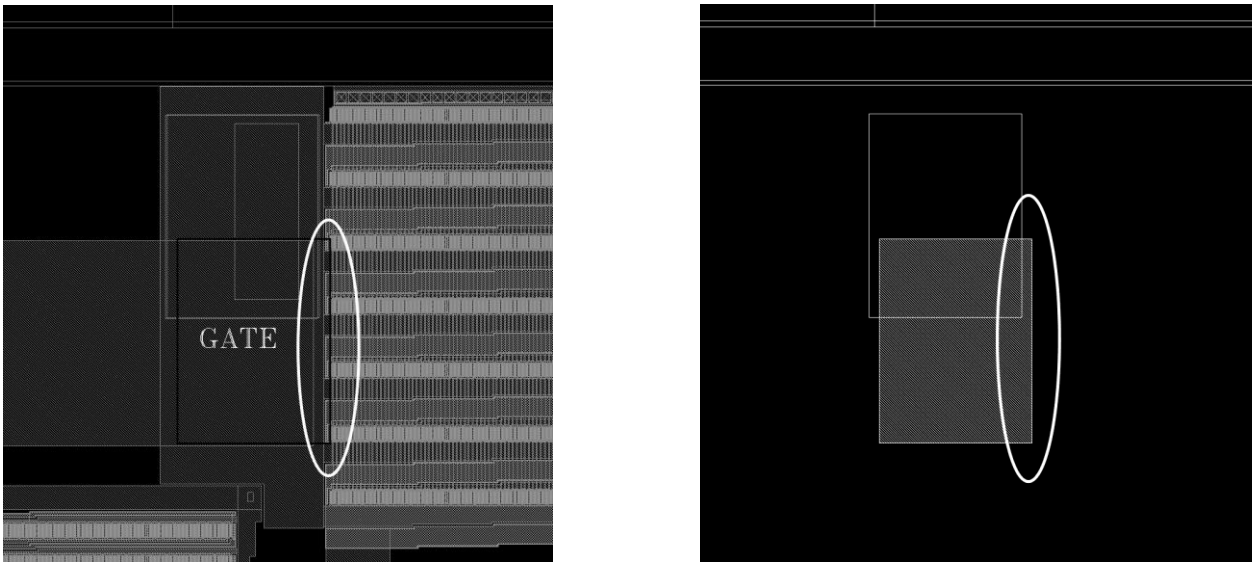


Fig. 7.9 Picture of the die of fabricated split chip gate driver (affected area is circled). (Francis, Matt. January 2013. ENRC Lab. JPEG file.)



(a) **(b)**

Fig. 7.10 Extraneous metal polygon tracked in Cadence Virtuoso (a) System level integrated layout of gate driver (culprit metal polygon is outlined in black and the affected area is circled in white) (b) Floating metal polygon visible after the gate driver is deleted.

7.3 RECTIFYNG THE GATE DRIVER USING FIB

After a considerable amount of cerebration, it was concluded that the best way to rectify the gate driver in an attempt to make it function properly was to sever the unwanted shorts of metal layer, created by the extraneous metal polygon, using a Focused Ion Beam (FIB) setup. An FIB setup can be used to generate a focused beam of ions which could be utilized to calculatedly cut through the integrated circuit in the die.

FEI Nova 200 NanoLab DualBeam workstation, shown in Fig. 7.11, at the Nanotechnology lab of University of Arkansas was used for this procedure. FEI xT server was used to place cut masks, control the sample and beam generator, and capture the sample pictures and other data. An accelerating voltage of 30 kV and a probe current of 7 nA was chosen to be appropriate values for the procedure.

Fig. 7.11 The FEI Nova 200 NanoLab dual-beam workstation.

(Lamichhane, Ranjan. March 2013. Arkansas Nano-Bio Materials Characterization Facility. JPEG file.)

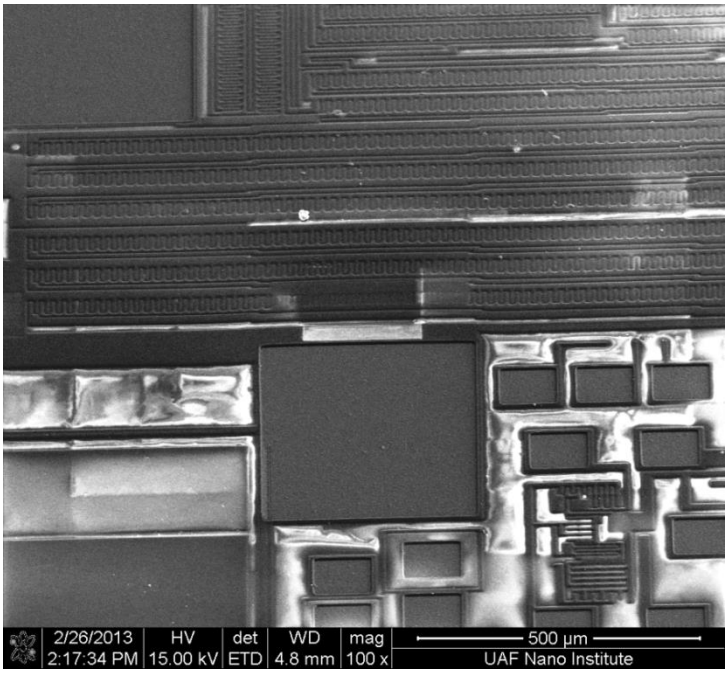


Fig. 7.12 View of the chip in the FIB workstation.

7.4 FIB CUT PLAN

The FEI Nova 200 Nanolab workstation in Nanotechnology building at University of Arkansas was used to generate a FIB to sever the metal layer in the SiC IC chip. The Cree 4H SiC P-Epitaxial process is a 20V, 2 µm minimum feature size, 1 metal layer process with a 4 um thick metal layer as shown in Fig. 7.13. There is an extra passivation layer on top, not shown in Fig. 7.13, which is approximately 6 µm thick.

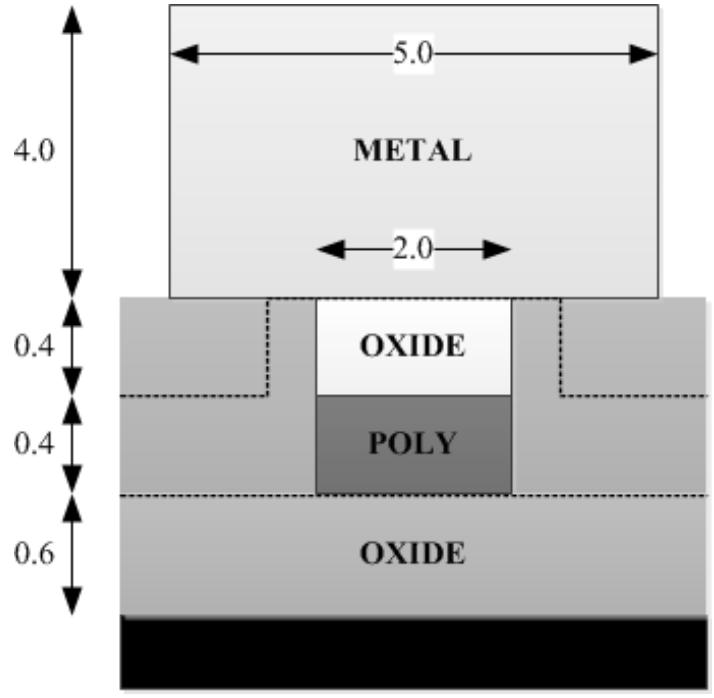


Fig. 7.13 Cree SiC process stack (all units are in µm).

7.4.1 Challenges Faced During FIB Cut Operation

It needs to be noted that the FIB procedure has several inherent imperfections that need to be artfully surmounted in order to successfully get the desired cuts with such an exacting precision that this particular undertaking poses. Some of the challenges faced during FIB procedure are listed below.

- The image that is available on the computer monitor, as shown in Fig. 7.12, while placing the cut is a greyscale image with not enough sharpness and resolution, which makes it a challenge to place cuts in micro meter precision.
- Since only the top layer (i.e. the metal layer) is visible on the die, all the other layers that lie underneath needs to be predicted by looking at the layout snapshots from the computer

and this can get really problematic when the predictions to be made are in micro meter scale.

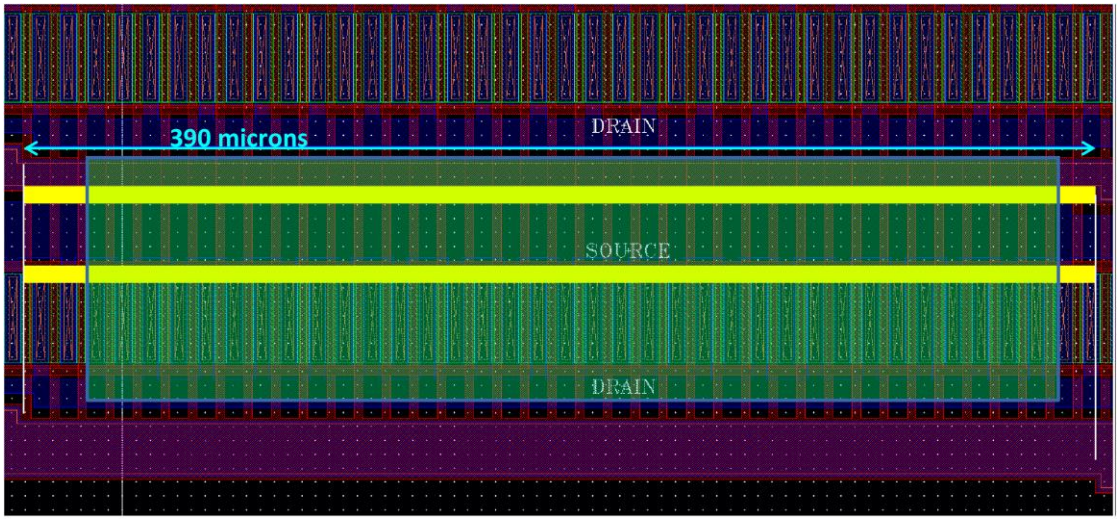
- It takes a prohibitive amount of time and cost to accomplish the procedure if the cuts are too big (i.e. too deep or too wide), and for a FIB procedure tens of microns long cuts are huge. It takes prohibitive amount of calculation and dexterity to properly place the cut masks using the computer software if the cuts are to be precise. So striking a balance between these two aspects is very important which will divide the risk to reasonable extent.
- The byproduct crumbles of materials produced during FIB cut operation may fall down to the trenches and get stuck such that the inbuilt vacuum suction may not be able to remove them. Circumventing this phenomenon will require a calculated width that will be big enough such that these crumbles won't get stuck in the trenches.

7.4.2 Single Chip Gate Driver

The FIB cut in single chip design needs to at least penetrate the Passivation Layer on Top, which is about 6 microns thick, and the Metal Layer, which is 4 microns thick. Hence, a cut of at least 10 microns depth is necessary to successfully sever the unwanted metal connection and a width of minimum 10 microns is necessary to make sure that the cut can actually go all the way down to 10 microns. The FIB cut starts to taper as it goes deeper and some of the metal crumbs produced by the sputtering of ion beam may get stuck in the trench causing an undesired short through the trench; therefore the cut needs to be of sufficient width and 10 microns was considered to be enough to circumvent this potential jeopardy. The FIB procedure to complete

the cuts, as shown in Fig. 7.14 (a) and Fig. 7.14 (b), with SEM set up at 7 nA probe current and 30 kV accelerating voltage took approximately 20 hours to finish.

(a)



(b)

Fig. 7.14 Single chip gate driver FIB cut plan (a) Zoomed view of chip in Fig. 7.2 where Red lines indicate proposed FIB cut (b) Zoomed layout of single chip design where highlighted box represents extraneous metal polygon and yellow lines represent the proposed FIB cut. (Lamichhane, Ranjan. February 2013. CSRC Lab. JPEG file.)

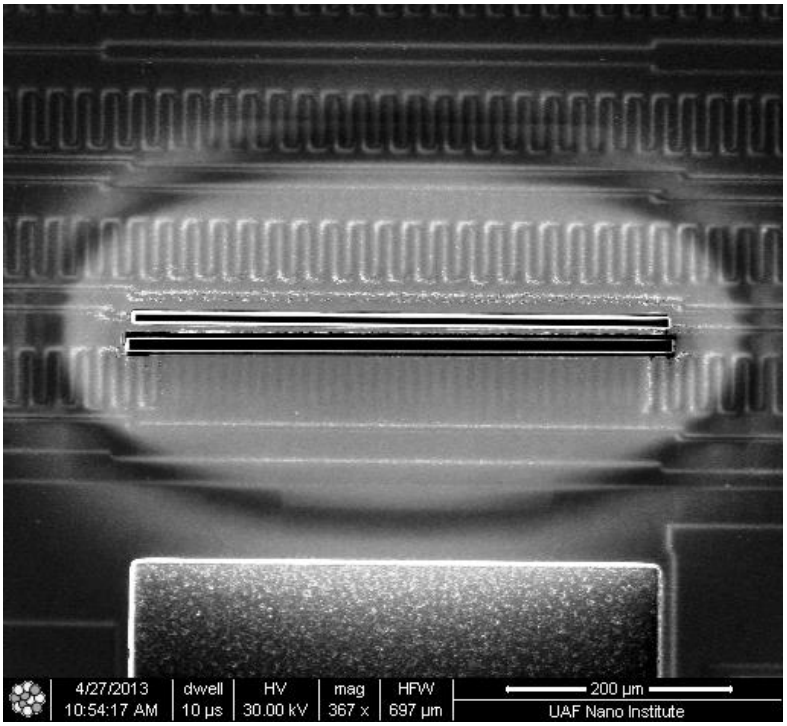


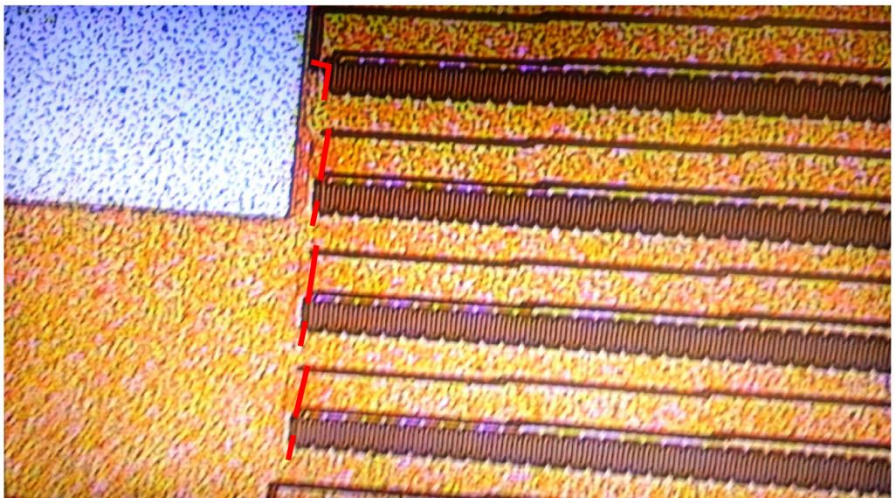
Fig. 7.15 Zoomed single chip after the FIB cuts, as seen via the FIB software.

(Lamichhane, Ranjan. March 2013. Arkansas Nano-Bio Materials Characterization Facility. JPEG file.)

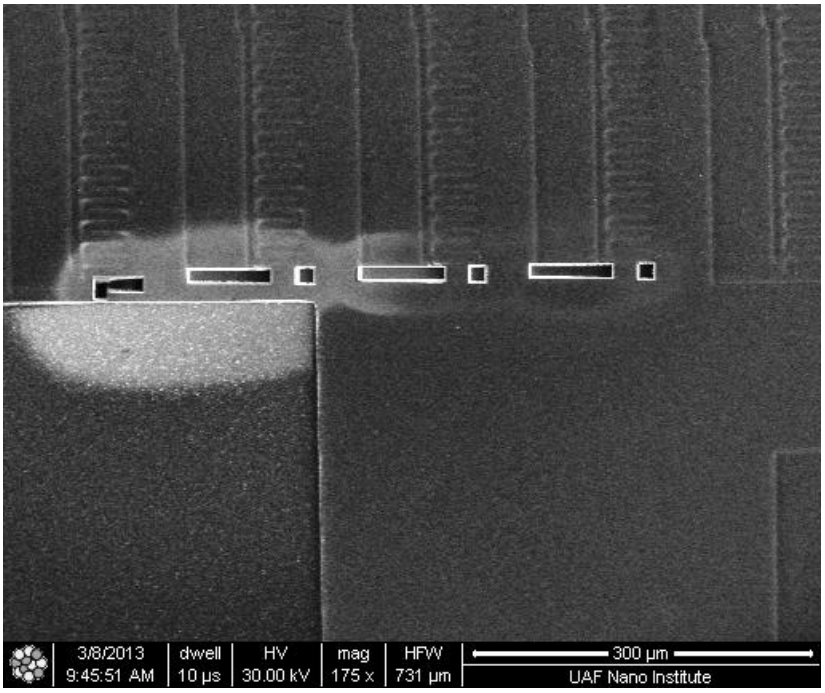
7.4.3 Split Chip Gate Driver

The FIB cut in split chip gate driver is rather complicated. This is because the extraneous metal polygon shorts the pull-down device of the gate driver in seven different places. Hence, seven different cuts needs to be made and the probability of getting a successful FIB is not very good since probability of error multiplies with the number of different FIB cut that needs to be made. Also, the fact that the cuts needs to penetrate not just the metal layer but the poly layer beneath as well, which is invisible to the eyes when placing the cut mask, makes FIB cut operation on split chip gate driver design particularly challenging.

The FIB cut in split chip design needs to penetrate at least the passivation layer, the metal layer, and the poly layer. That would require at least 11 microns to make the cut deep enough; 6 microns for Passivation, 4 microns for metal, 0.4 microns for oxide between metal and poly and 0.4 microns for poly layer. To make sure we get sufficient width for 11 microns deep cut, we need to make the width about 12 microns. It took the FIB procedure approximately 24 hours to complete the cuts as shown in Fig. 7.16 (a), with SEM set up at 7 nA probe current and 30 kV accelerating voltage. Fig. 7.17 shows the planned FIB cuts in Cadence Virtuoso layout software.



(a)



(b)

Fig. 7.16 Split chip gate driver FIB cut plan (a) Zoomed view of chip in Fig. 7.9 where red lines indicate proposed FIB cut path (b) Split chip after the FIB cuts, as seen via the FIB software. (Lamichhane, Ranjan. March 2013. Arkansas Nano-Bio Materials Characterization Facility. JPEG file.)

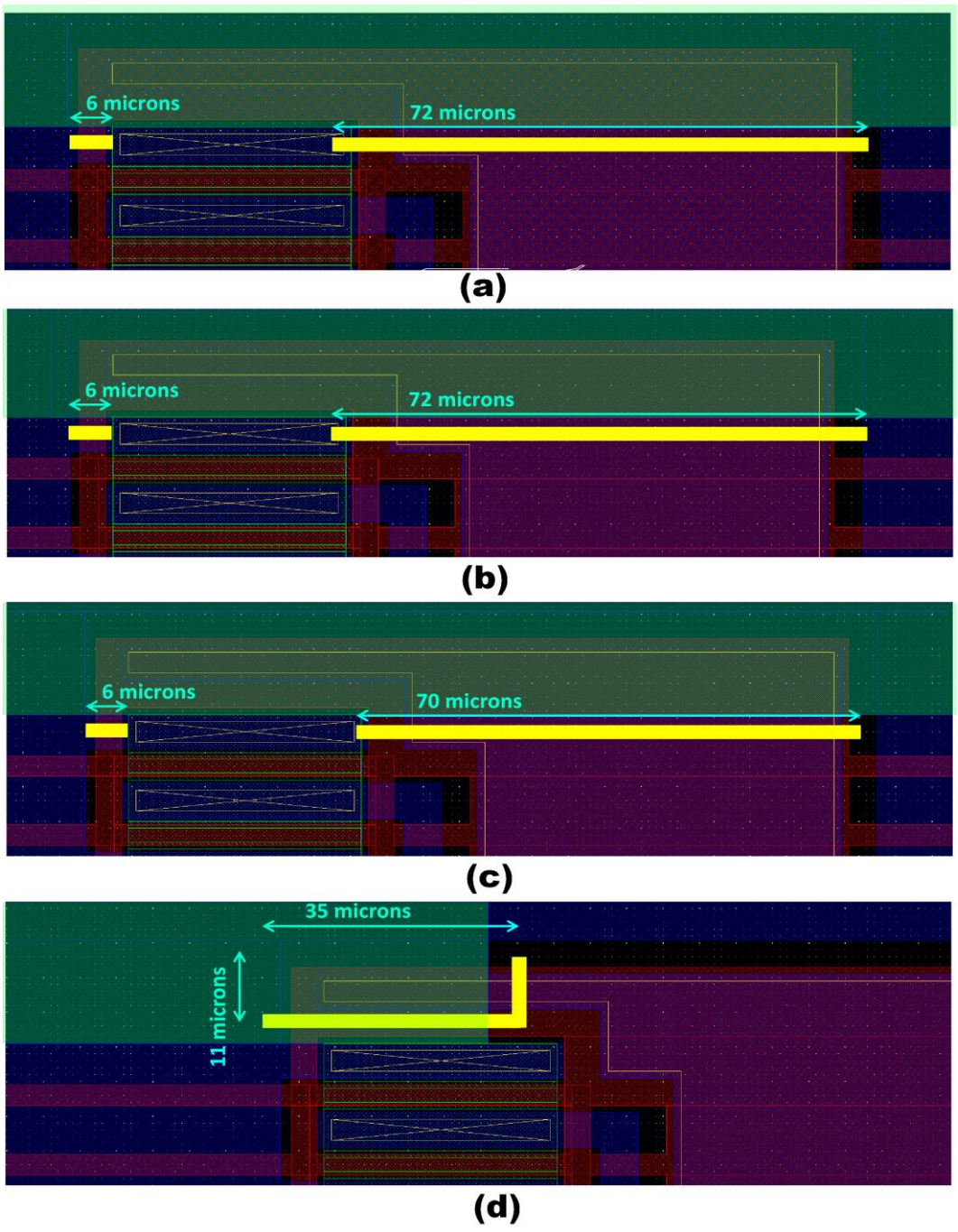


Fig. 7.17 Zoomed layout of the single chip design where highlighted box represents the extraneous metal polygon and the bold yellow lines represent the proposed FIB cut (a), (b), (c) and (d) shows the four different FIB cuts required as shown by the red Lines in Fig. 7.16 (c).

8. TESTING AND CHARACTERIZATION

8.1 SPLIT CHIP GATE DRIVER (FIB CUT ATTEMPT 1)

After FIB, the split chip design was die-attached to the daughterboard, placed on the motherboard and tested according to the developed test plan. The outputs obtained on the FIB operated die were very similar to the ones obtained before the FIB. It was inferred from these results that the FIB on split chip design was unsuccessful and the failure can be attributed to the fact that split chip design requires relatively complicated cuts and at some places rather deep cuts to be made using FIB. At some places the cuts need to go through the metal layer and through the poly layer as well. Because of the exacerbating combination of FIB challenges as explained in Section 7.4.1 and given the complication of cuts, as illustrated in Fig. 7.16 (a) and Fig. 7.17 (a), (b), (c) and (d), the FIB on the split chip gate driver design failed. And given the cost for the procedure and the relatively small chances of success, further pursuit on trying to rectify the split chip gate driver design was abandoned.

8.2 SINGLE CHIP GATE DRIVER I (FIB CUT ATTEMPT 1: WAFER DD1310-09)

The result obtained from the FIB operated single chip gate driver was encouraging. The gate driver was functioning as expected with the waveforms being in right shape and size. The gate driver was run with two load conditions, a 3.9 nF capacitive load and a CMF20120D SiC Power MOSFET. The data obtained from the FIB operated single chip gate driver die is summarized in Table 8.1 and Table 8.2. The discrepancy in rise time and power consumption is striking when compared with the single chip gate driver parasitic simulations tabulated in Table 4.1. Even

though a slight discrepancy in performance of actual chip as compared to parasitic simulations was expected, this magnitude of discrepancy was surprising.

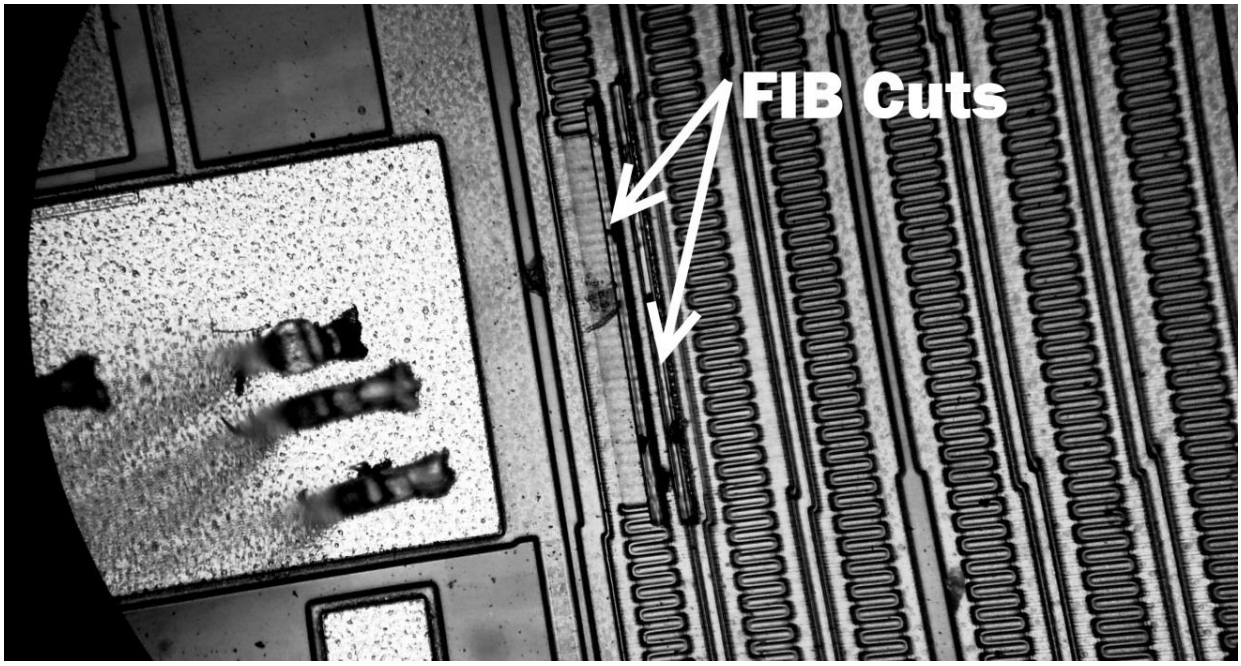


Fig. 8.1 The single chip gate driver section where the FIB cut was performed.

(Lamichhane, Ranjan. March 2013. CSRC Lab. JPEG file.)

Table 8.1 Test Results with 3.9 nF Capacitive Load and 5 V 500 kHz Square Wave Input (VDD_T = 20 V; Single Chip Design DD1310-09)

MODE	VD_1 (V)	VDD_2 (V)	VDD_{OD} (V)	I_1 (mA)	I_2 (mA)	I_{OD} (mA)	I_T (mA)	RISE (ns)	FALL (ns)	DELAY (ns)	POWER (W)	TEMP. (°C)
1	20	20	40	44	20	93	84	**124**	**61**	**191**	**6.7**	35
2	25	18	40	55	17	85	168	**99**	**39**	**139**	**8.4**	35
3	25	18	45	55	16	95	157	**62**	**38**	**135**	**9.1**	35
4	25	18	50	54	17	105	153	**46**	**38**	**131**	**9.9**	37

Table 8.2 Test Results with CMF20120D SiC PowerMOS Load and 5 V 500 kHz Square Wave Input (VDD_T = 20 V; Single Chip Design DD1310-09)

MODE	VD_1 (V)	VDD_2 (V)	VDD_{OD} (V)	I_1 (mA)	I_2 (mA)	I_{OD} (mA)	I_T (mA)	RISE (ns)	FALL (ns)	DELAY (ns)	POWER (W)	TEMP. (°C)
1	20	20	40	44	17	84	172	**148**	**55**	**176**	**8.0**	35
2	25	18	40	55	14	83	168	**132**	**40**	**137**	**8.3**	35
3	25	18	45	55	17	95	175	**86**	**39**	**131**	**9.5**	35
4	25	18	50	54	16	105	160	**62**	**39**	**127**	**10.1**	37

The last column of Table 8.1 and Table 8.2 shows the temperature of the die after operation in that mode for at least 10 minutes. The rise and fall times are calculated as time taken to transition from 10% -90% and 90% - 10% respectively of the full output amplitude (i.e. VDD_T = 20V). The propagation delay is calculated as the time interval between 50% amplitude points of input and output waveforms.

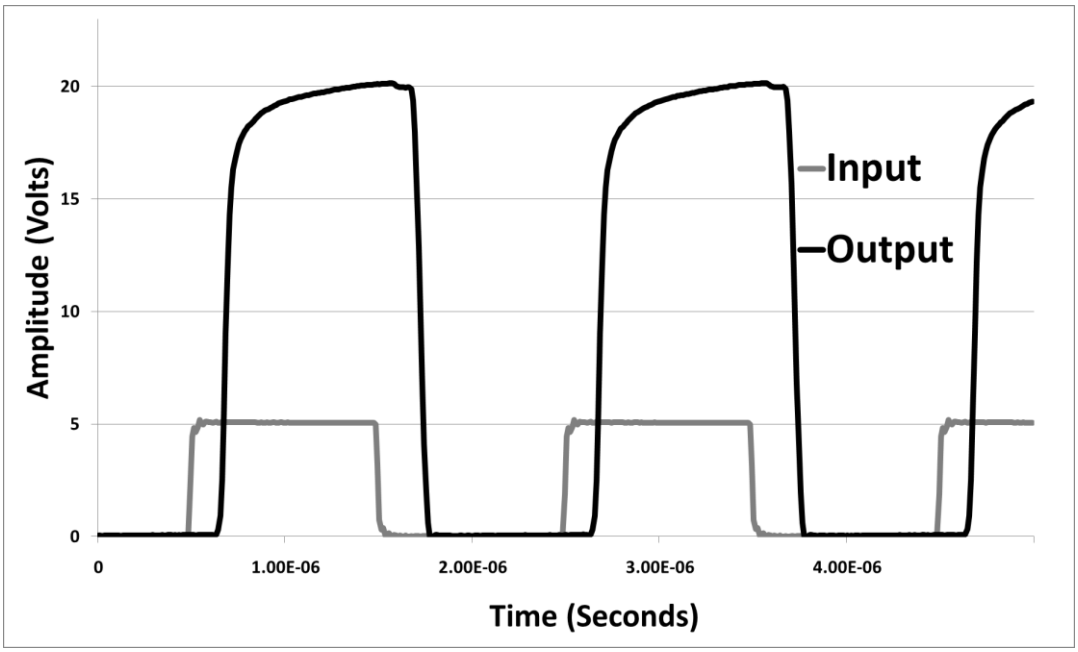


Fig. 8.2 Input/output waveforms for data in the first row of Table 8.1(Mode 1).

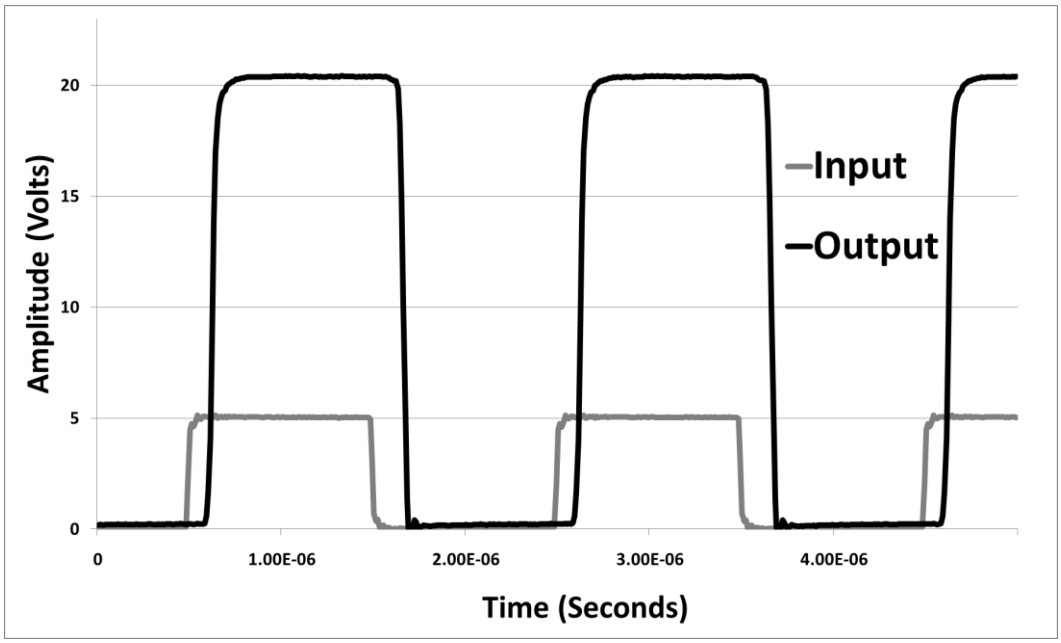


Fig. 8.3 Input/Output Waveforms for Data in Last Row of Table 8.1 (Mode 4).

It can be clearly seen that the waveforms look considerably different in Fig. 8.2 and Fig. 8.3. In Fig. 8.2, where the overdrive voltage is 40 V, the output signal struggles to rise contributing to the huge rise time as seen in data in first row of Table 8.1. However, when the overdrive is increased to 50 V, the output signal reaches the peak very fast causing the rise time to improve significantly as seen in data in last row of Table 8.1. This behavior is strange because 40 V overdrive should be enough to turn the pull-up device effectively ON unless the gate of pull-up device is not seeing the full magnitude of the overdrive voltage VDD_{OD}. An educated guess would be that the FIB cut procedure didn't absolutely sever the metal connection between the drain and source of transistor *DA12* (refer Fig. 7.6) and some current is still leaking through this transistor when it is off, causing the overdrive voltage to not go all the way up to applied VDD_{OD}.

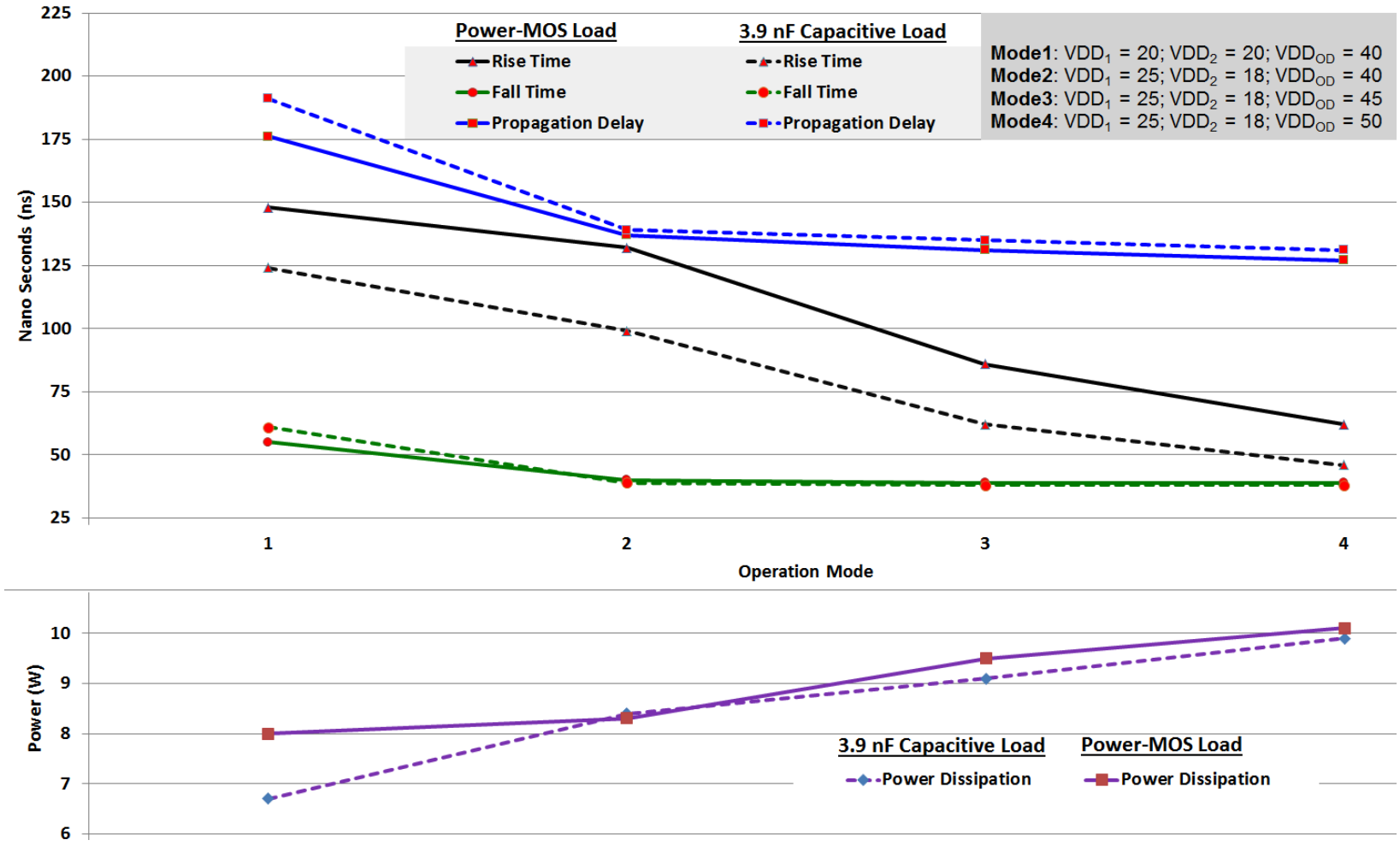


Fig. 8.4 Behavior of single chip gate driver design in different power modes.

Fig. 8.4 illustrates the change in different gate driver parameters with different mode of power supply. We can see that the rise time improves significantly when the overdrive voltage is increased i.e. from Mode 1 to 2 to 3 to 4, successively. This is because it makes the pull-up device turn ON more when there is more overdrive voltage and hence the rise time effectively decreases. The slight decrease in fall time is because of increase in VD_1 supply voltage which causes the pull-down device to turn ON more decreasing the time taken for the output signal to fall. The propagation delay will decrease slightly since when signal is rising faster which decreases the delay between 50% amplitude point of input and 50% amplitude point of output.

This particular single chip design chip abruptly stopped functioning before any more test data could be gathered out of this chip.

8.3 SINGLE CHIP GATE DRIVER II (FIB CUT ATTEMPT 2: WAFER GK0753-22)

After the first FIB cut single chip gate driver die stopped working, a second FIB cut procedure was attempted on single chip design because of the encouraging results from the first run. More wider and deeper cuts were chosen for this run because of uncalled-for performance degradation on the last one, probably due to imperfect FIB cut as hypothesized.

The performance of gate driver increased dramatically on this version of FIB cut and the results obtained were very consistent with the performance figures obtained by simulations on parasitic extracted models. A TO-247-3 package (packaged by APEI) CMF20120D SiC PowerMOS, shown in Fig. 8.5, was chosen as the load which is the actual device that the gate driver was designed to drive.

The data obtained from the test set up is summarized in Table 8.3. The measured data is better than the simulated data listed in Table 4.1.

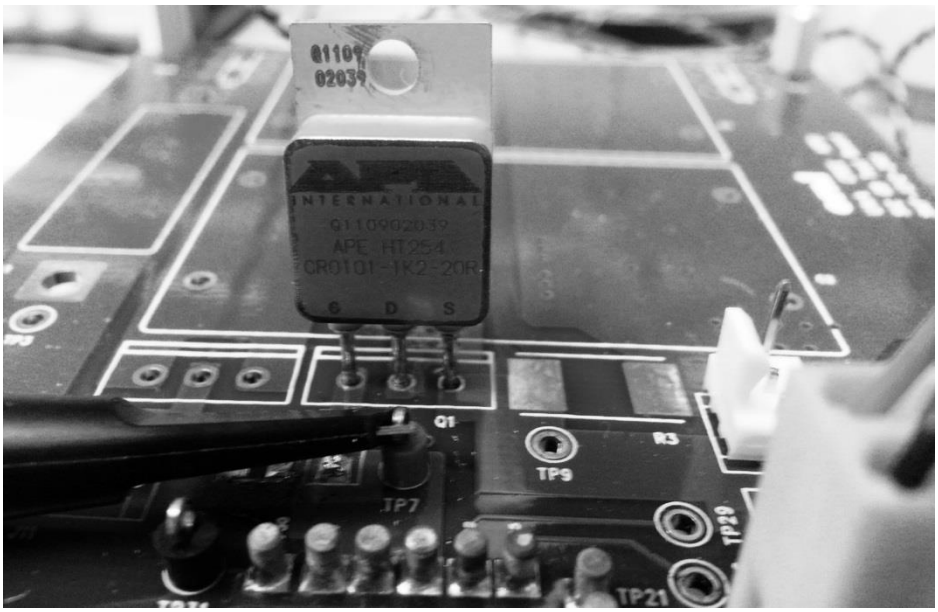


Fig. 8.5 The packaged CMF20120D SiC power MOSFET.

(Lamichhane, Ranjan. March 2013. CSRC Lab. JPEG file.)

Table 8.3 Test Results with CMF20120D SiC PowerMOS Load and 5 V 500 kHz Square Wave Input (VDD_T = 20 V; Single Chip Design GK0753-22)

MODE	VDD_1 (V)	VDD_2 (V)	VDD_{OD} (V)	I_1 (mA)	I_2 (mA)	I_{OD} (mA)	I_T (mA)	RISE (ns)	FALL (ns)	DELAY (ns)	POWER (W)
1	20	20	40	46	18	87	31	**60**	**60**	168	**5.4**
2	25	20	40	58	17	85	32	**60**	**40**	138	**5.8**
3	22	20	45	51	17	92	34	**46**	**50**	134	**6.3**
4	25	20	45	58	17	92	33	**45**	**41**	**131**	**6.6**

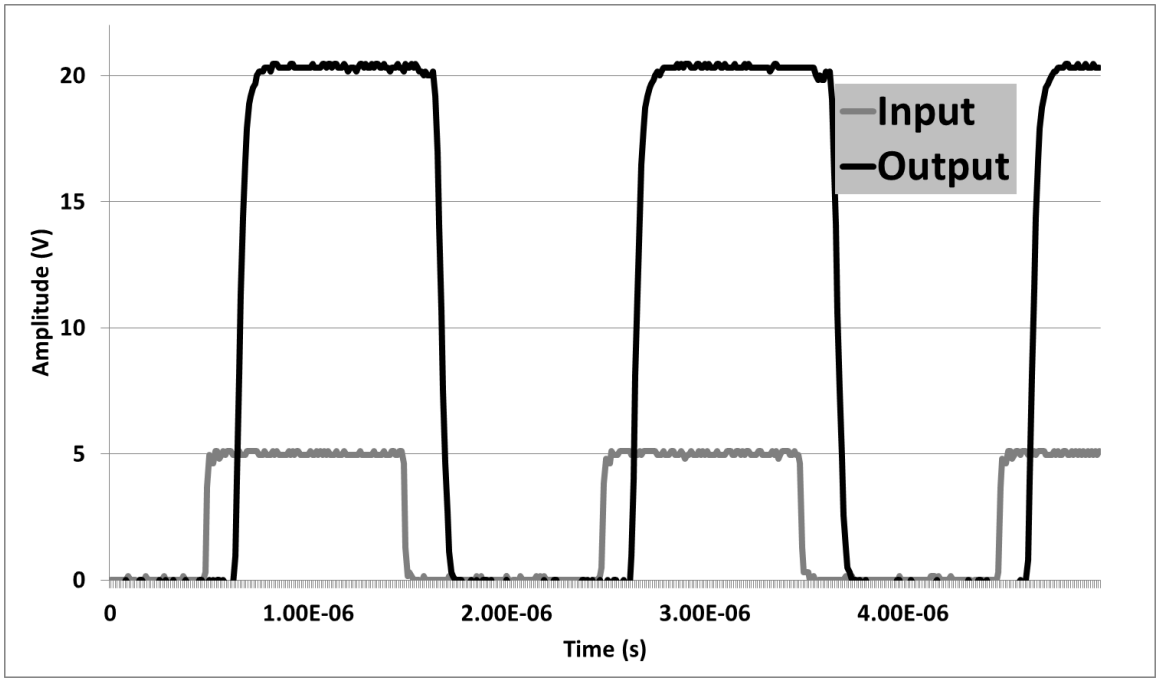


Fig. 8.6 Input/ output waveforms for data in Table 8.3 (Mode 1).

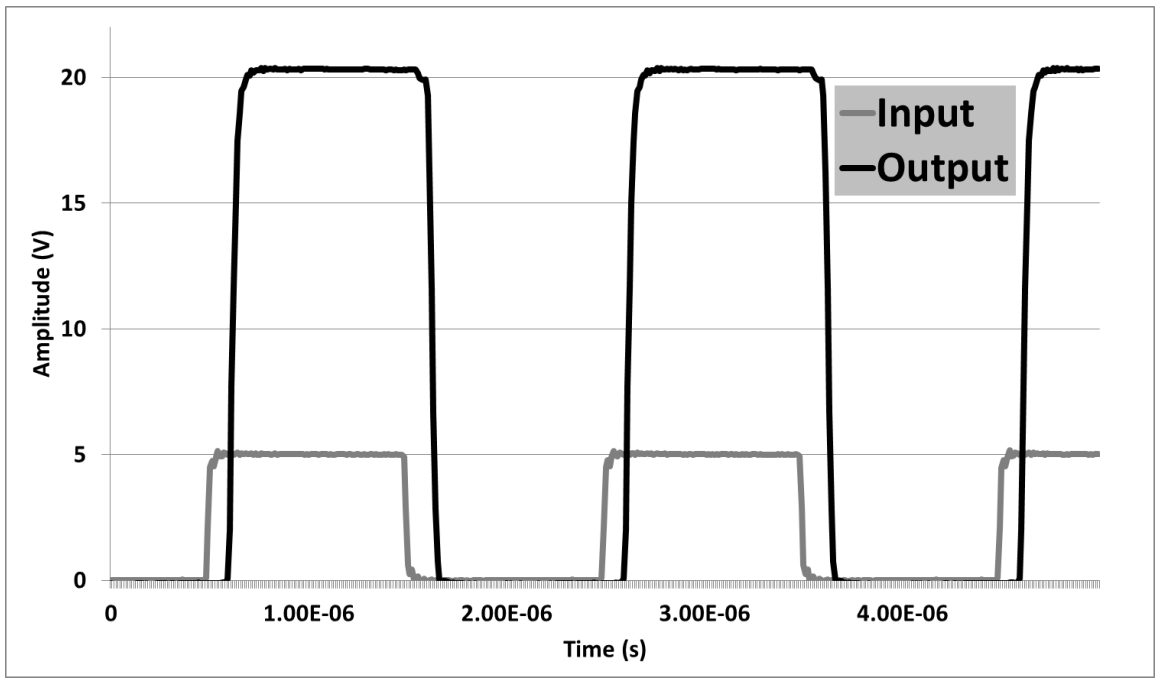


Fig. 8.7 Input/ output waveforms for data in Table 8.3 (Mode 4).

The slow rising of output signal as it reaches high amplitude as seen in Fig. 8.2 for the first FIB cut single chip design has disappeared in the second FIB cut die as seen in Fig. 8.6. This consolidates the hypothesis that the FIB procedure was not optimal on the first attempt on the single chip design gate driver die.

From Table 8.3, it can be seen that Mode 4 is the best operating condition for the gate driver and it has been seen from various tests and experiments that 25 V potential difference is safe for any part of the devices in this SiC process.

It can be clearly seen that the test data in Table 8.3 is proportional to simulation data in Table 4.1. The results are better than the simulated results because the transconductance of the fabricated MOSFET turned out to be better than the transconductance of the MOSFET model in the design kit used in Cadence Virtuoso. This statement is illustrated in Fig. 8.8; the transconductance differs significantly after the gate voltage crosses the 15 V mark. This would cause more current to flow through the devices causing their outputs to rise/fall faster and, hence, the rise/fall time would be decreased. Furthermore, the resistivity of the diffusion resistors turned out to be less than expected, which means it is less than the resistivity data in the model, which also caused the improvement in performance parameters.

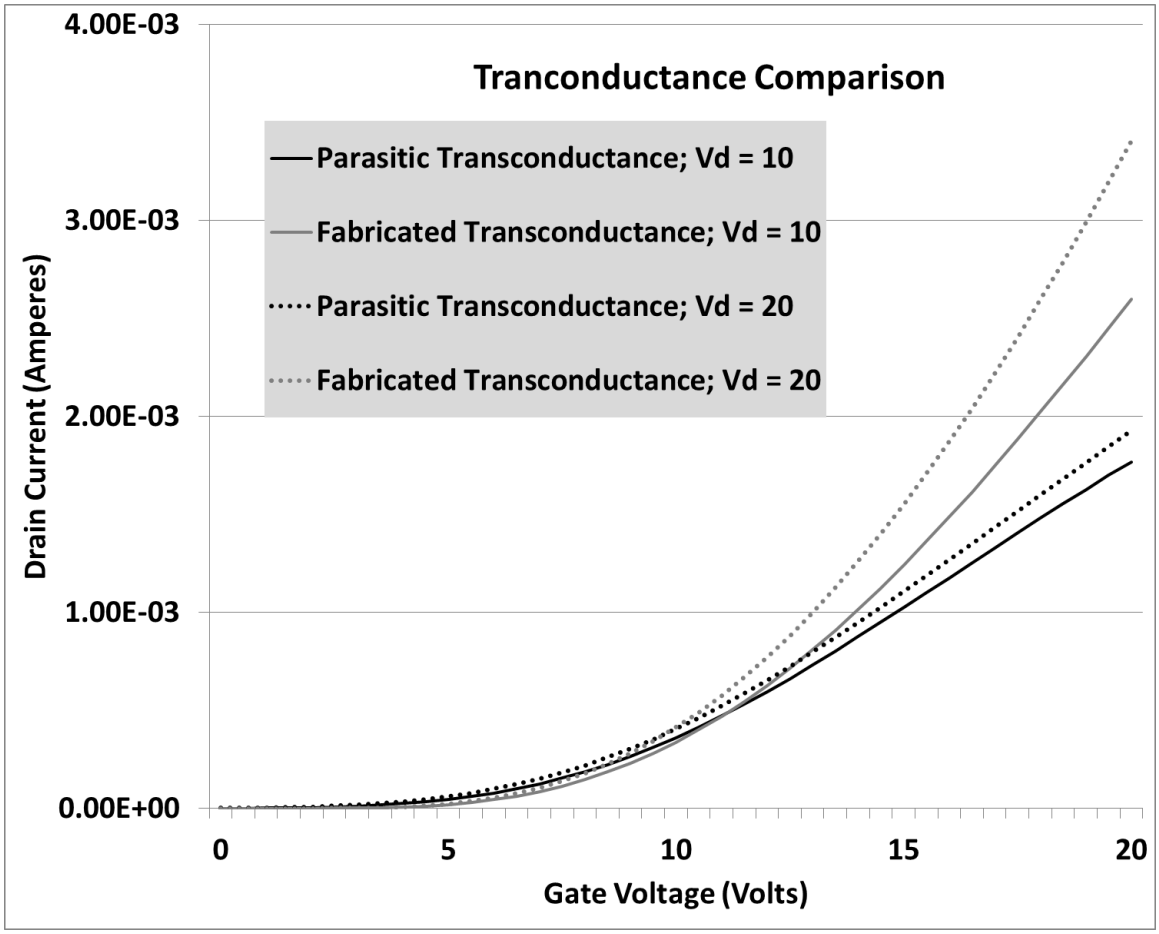


Fig. 8.8 Transconductance comparison between design kit model and fabricated chip.

8.4 OVER THE TEMPERATURE TESTING (SINGLE CHIP DESIGN FIB CUT ATTEMPT 2: WAFER GK0753-22)

After the second FIB operated single-design chip worked very effectively, the test phase moved on to the high temperature testing. A hot plate temperature testing set up was used for this purpose as shown in Fig. 8.9. The thermocouple was secured to the cold finger very close to the die contact using a thermal tape and inserted to the temperature testing port of VICHY V99 multimeter as shown in Fig. 8.9 and Fig. 8.10.

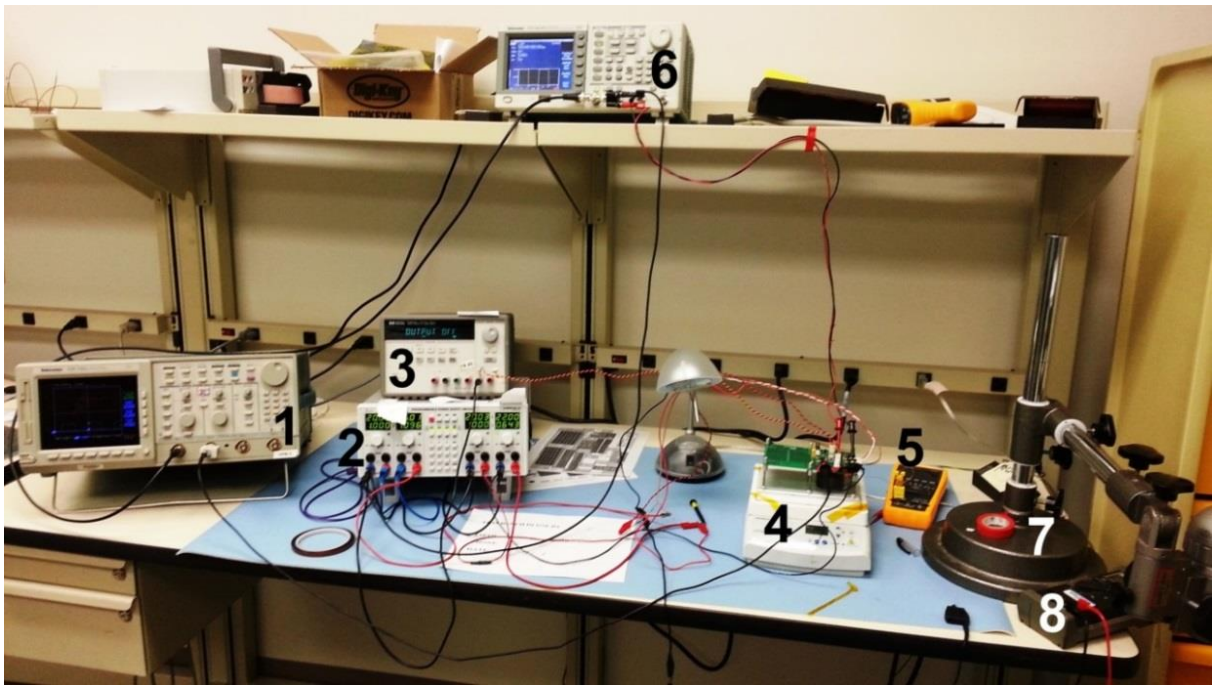


Fig. 8.9 Over the temperature test setup (1) Spectrum analyzer/ oscilloscope (2) HAMEG power supply (3) Agilent power supply (4) Hot plate (5) VICHY VC99 multimeter (6) Signal generator (7) Microscope (8) Digital multimeter.

(Lamichhane, Ranjan. June 2013. CSRC Lab. JPEG file.)

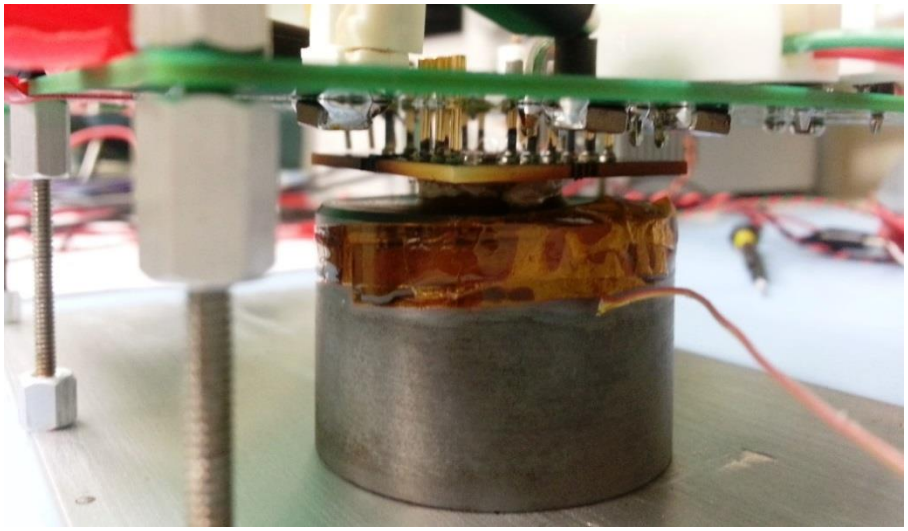


Fig. 8.10 Thermocouple contact with the cold finger secured with thermal tape.

(Lamichhane, Ranjan. June 2013. CSRC Lab. JPEG file.)

It needs to be noted that the temperature measured by the multimeter using a thermocouple is not the actual die temperature. There is a finite temperature gradient from the gate driver die to the point in the cold finger from where the temperature is being measured. APEI calculated this temperature gradient after running several tests, with a test setup that is identical to the test setup used in Fig. 8.9 and Fig. 8.10, to be 7.7 °C per Watt. The equation for calculating the die temperature is:

$$\boldsymbol{T_{Die}} = \boldsymbol{T_{Thermocouple}}(℃) + \mathbf{7.7}(\tfrac{℃}{\boldsymbol{W}}) * \boldsymbol{Power_{Dissipated}}(\boldsymbol{W}) \quad (8.1)$$

This equation will be used to determine the actual die temperature of the gate driver. According to this equation, the temperature of single chip gate driver die when the thermocouple is at room temperature with Mode 4 power supply would be:

$$\boldsymbol{T_{Die}} = \mathbf{25}\ ℃ + \mathbf{7.7}\left(\tfrac{℃}{\boldsymbol{W}}\right) * \mathbf{6.6}\boldsymbol{W} = \mathbf{75.82}\ ℃ \quad (8.2)$$

Table 8.4 -Table 8.7 shows the data collected from high temperature testing of the gate driver in different power supply modes which are summarized in a line chart in Fig. 8.11 - Fig. 8.14, respectively. The gate driver stopped working above 380 °C measured temperature, i.e. 420 °C calculated die temperature according to Eq. (8.1).

Table 8.4 Temperature Data for Mode 1 Power Supply (V_1 = 20 V, V_2 = 20 V; V_{OD} = 40 V; V_T = 20 V; V_{IN} = 0 – 5 V square wave signal of 500 kHz; V_{OUT} = 0 – 20 V; Die Temp is Calculated)

I_1 (mA)	I_2 (mA)	I_{OD} (mA)	I_T (mA)	RISE (ns)	FALL (ns)	DELAY (ns)	POWER (W)	DIE TEMP (°C)
46	18	87	31	60	60	168	5.38	63
46	17	85	30	64	59	165	5.26	91
46	17	84	30	65	57	161	5.22	104
45	17	83	30	65	57	160	5.16	117
45	17	82	30	66	55	154	5.12	132
44	17	80	31	67	54	147	5.04	148
44	17	79	31	66	53	142	5	164
43	17	77	32	65	53	137	4.92	185
43	17	75	34	65	51	133	4.88	198
42	17	74	35	64	49	130	4.84	217
42	17	72	35	64	50	128	4.76	237
40	17	70	36	64	50	126	4.66	266
40	17	69	37	65	50	125	4.64	291
39	18	67	39	65	50	123	4.6	315
38	18	65	40	66	50	124	4.52	325
38	18	65	39	67	50	123	4.5	345
38	18	64	42	67	50	124	4.52	355
36	19	62	44	71	51	125	4.46	389
36	19	60	44	72	52	125	4.38	414
36	17	59	37	76	53	123	4.16	419

Table 8.5 Temperature Data for Mode 2 Power Supply (V_1 = 25 V, V_2 = 20 V; V_{OD} = 40 V; V_T = 20 V; V_{IN} = 0 – 5 V square wave signal of 500 kHz; V_{OUT} = 0 – 20 V; Die Temp is Calculated)

I_1 (mA)	I_2 (mA)	I_{OD} (mA)	I_T (mA)	RISE (ns)	FALL (ns)	DELAY (ns)	POWER (W)	DIE TEMP (°C)
58	17	85	32	60	40	138	5.83	67
58	17	83	33	60	41	131	5.77	94
57	17	82	33	61	41	128	5.705	108
57	17	81	33	60	41	127	5.665	121
57	17	80	34	62	40	125	5.645	136
56	17	79	34	63	40	124	5.58	152
55	17	77	34	64	39	123	5.475	167
54	17	76	35	64	39	122	5.43	189
54	17	75	35	64	39	121	5.39	202
53	17	73	35	64	39	120	5.285	221
52	17	72	35	64	39	120	5.22	240
51	17	70	36	65	39	119	5.135	270
51	17	68	36	65	39	118	5.055	294
49	18	67	37	66	39	118	5.005	319
49	18	65	38	68	39	118	4.945	328
48	18	64	38	68	39	118	4.88	348
48	18	64	39	69	39	119	4.9	358
46	19	62	41	70	40	121	4.83	392
45	19	60	41	71	42	121	4.725	416
46	17	59	35	78	42	120	4.55	422

Table 8.6 Temperature Data for Mode 3 Power Supply (V_1 = 22 V, V_2 = 20 V; V_{OD} = 45 V; V_T = 20 V; V_{IN} = 0 – 5 V square wave signal of 500 kHz; V_{OUT} = 0 – 20 V; Die Temp is Calculated)

I_1 (mA)	I_2 (mA)	I_{OD} (mA)	I_T (mA)	RISE (ns)	FALL (ns)	DELAY (ns)	POWER (W)	DIE TEMP (°C)
51	17	92	34	46	50	134	6.282	70
50	17	90	34	49	50	130	6.17	98
50	17	89	34	50	49	129	6.125	111
50	17	88	34	49	48	128	6.08	124
49	17	87	35	49	47	126	6.033	139
48	17	86	35	50	47	125	5.966	155
48	17	84	36	52	46	124	5.896	170
47	17	83	36	52	45	122	5.829	192
47	17	81	37	52	45	120	5.759	204
46	17	80	37	52	44	119	5.692	224
46	17	78	38	51	44	118	5.622	243
44	17	76	38	52	44	117	5.488	272
44	17	74	39	52	44	116	5.418	297
43	18	73	41	52	45	116	5.411	322
42	18	71	42	53	45	116	5.319	331
42	18	70	42	54	45	116	5.274	351
41	18	69	44	54	45	117	5.247	360
40	19	67	46	56	46	118	5.195	395
39	19	65	46	57	47	118	5.083	419

Table 8.7 Temperature Data for Mode 4 Power Supply (V_1 = 25 V, V_2 = 20 V; V_{OD} = 45 V; V_T = 20 V; V_{IN} = 0 – 5 V square wave signal of 500 kHz; V_{OUT} = 0 – 20 V; Die Temp is Calculated)

I_1 (mA)	I_2 (mA)	I_{OD} (mA)	I_T (mA)	RISE (ns)	FALL (ns)	DELAY (ns)	POWER (W)	DIE TEMP (°C)
58	17	92	33	45	41	131	6.59	73
58	17	90	34	48	41	125	6.52	100
57	17	89	34	50	41	123	6.45	114
57	17	88	35	50	40	121	6.425	126
56	17	87	35	50	40	120	6.355	142
55	17	86	35	50	40	119	6.285	157
55	17	84	36	51	39	118	6.215	173
54	17	82	36	51	39	117	6.1	194
53	17	81	36	51	39	117	6.03	206
53	17	80	36	51	39	116	5.985	226
52	18	78	37	52	39	115	5.91	246
51	17	76	37	53	39	115	5.775	274
50	17	74	37	54	39	114	5.66	299
49	18	73	39	54	39	114	5.65	324
48	18	71	40	55	39	115	5.555	333
48	18	70	41	55	39	114	5.53	353
47	18	69	41	56	39	115	5.46	362
46	19	68	43	56	41	116	5.45	397
45	19	65	44	58	42	117	5.31	421

The charts below summarize the data obtained from measurements.

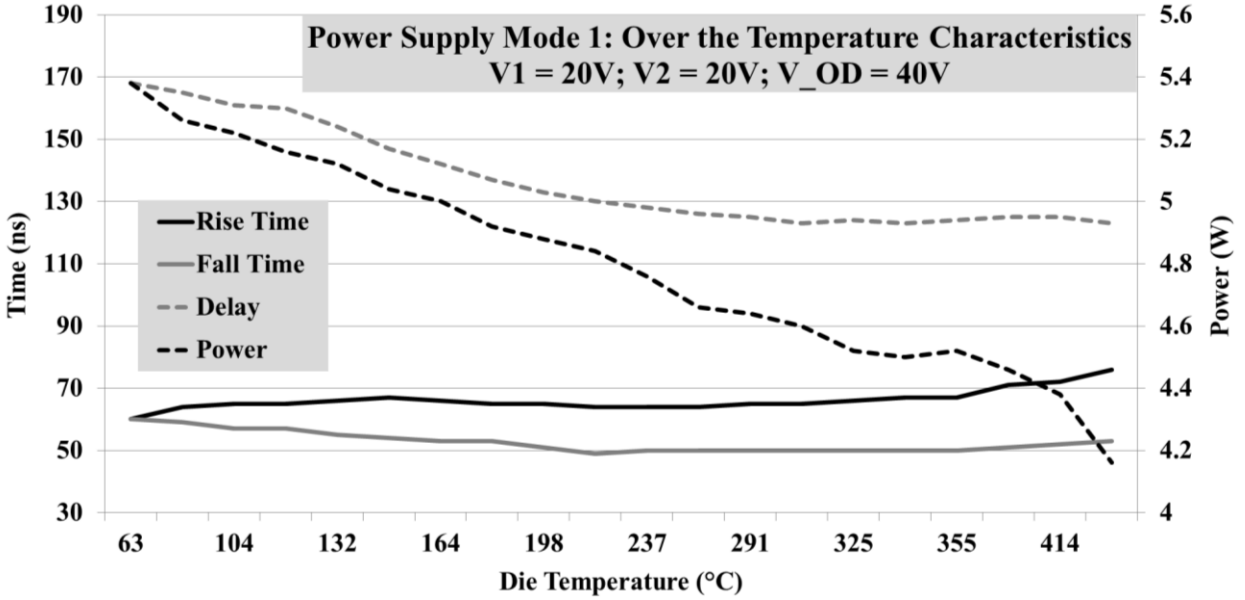


Fig. 8.11 Single chip gate driver behavior over the temperature for ‘Mode 1’ supply.

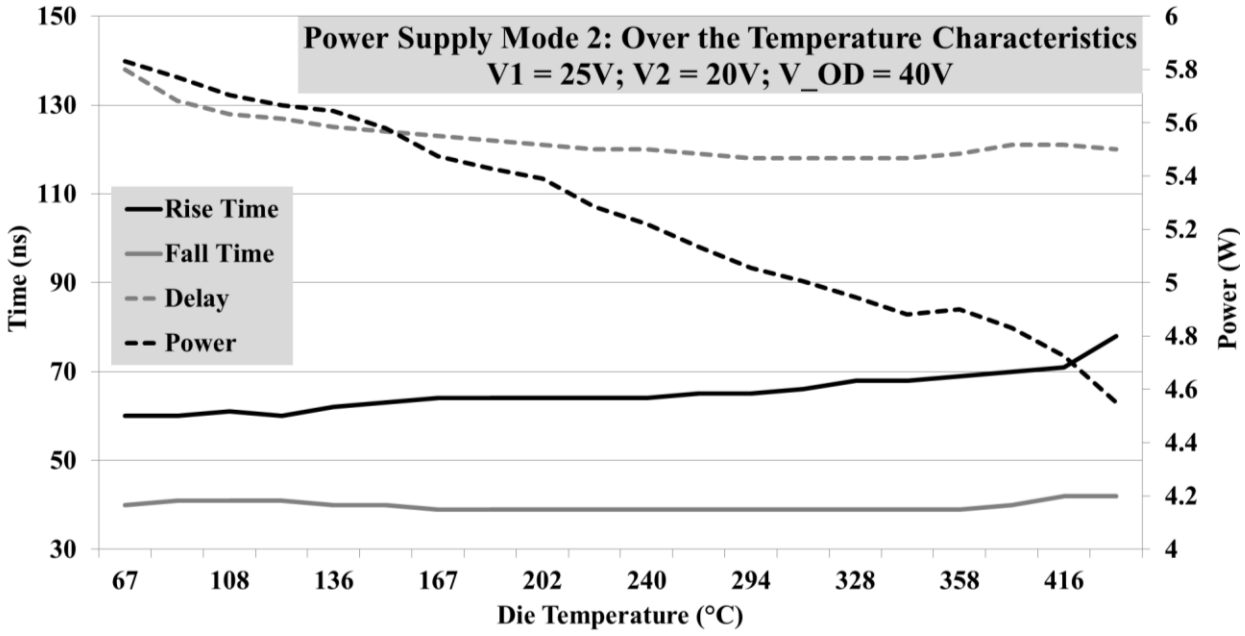


Fig. 8.12 Single chip gate driver behavior over the temperature for ‘Mode 2’ supply.

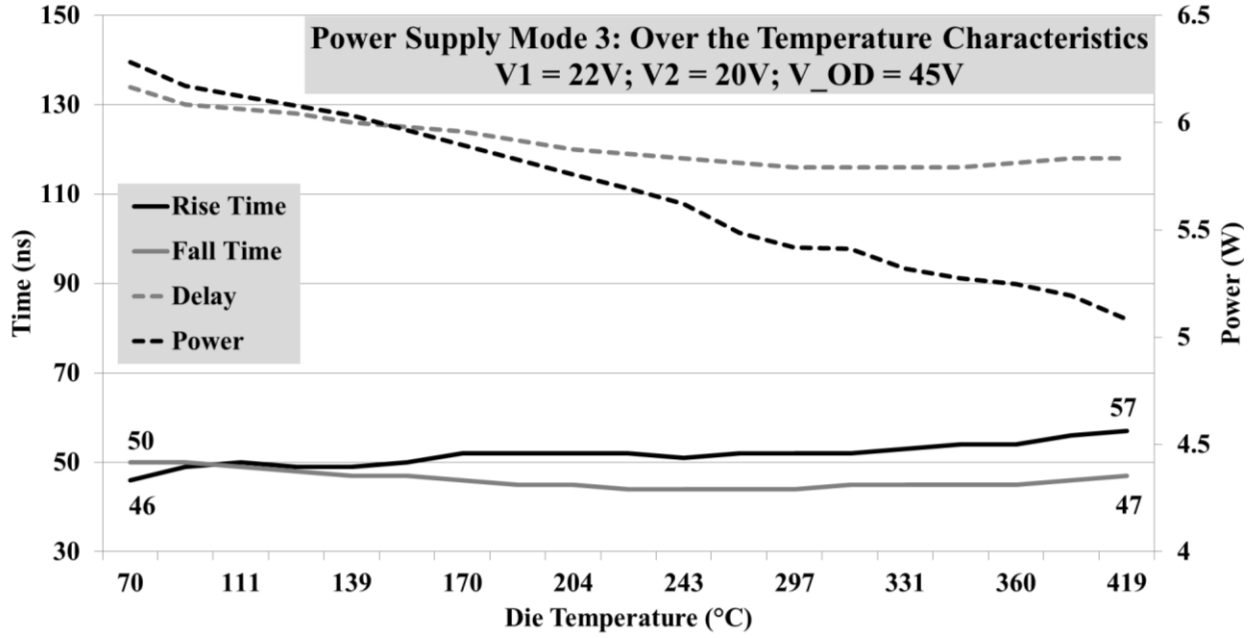


Fig. 8.13 Single chip gate driver behavior over the temperature for 'Mode 3' supply.

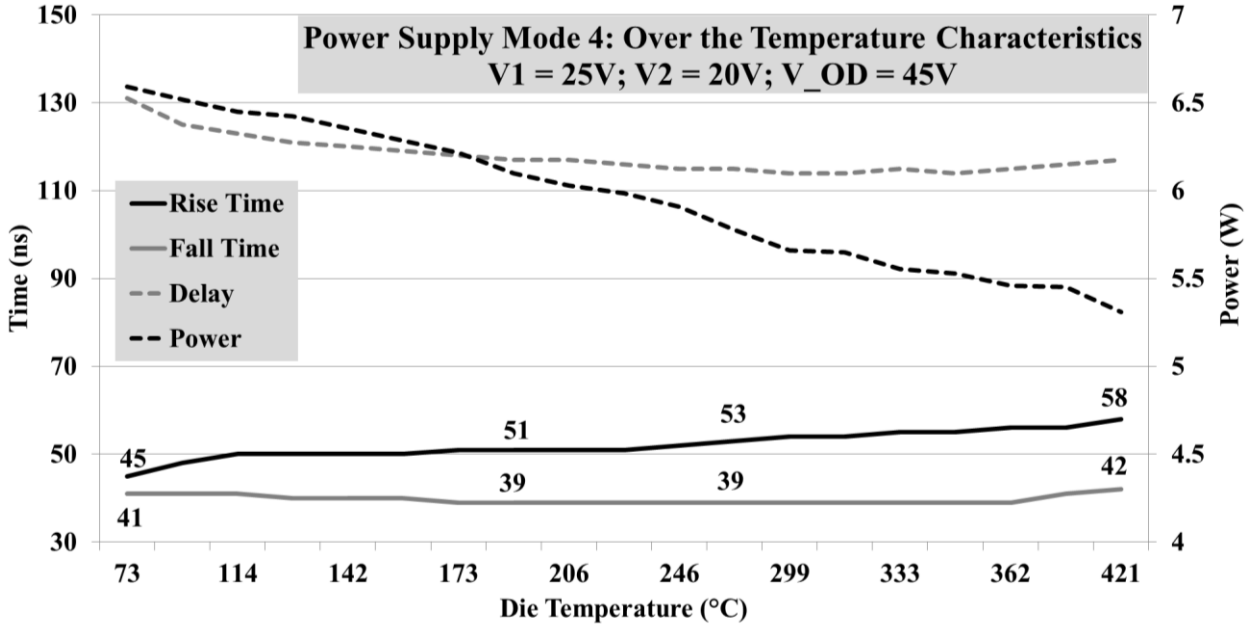


Fig. 8.14 Single chip gate driver behavior over the temperature for 'Mode 4' supply.

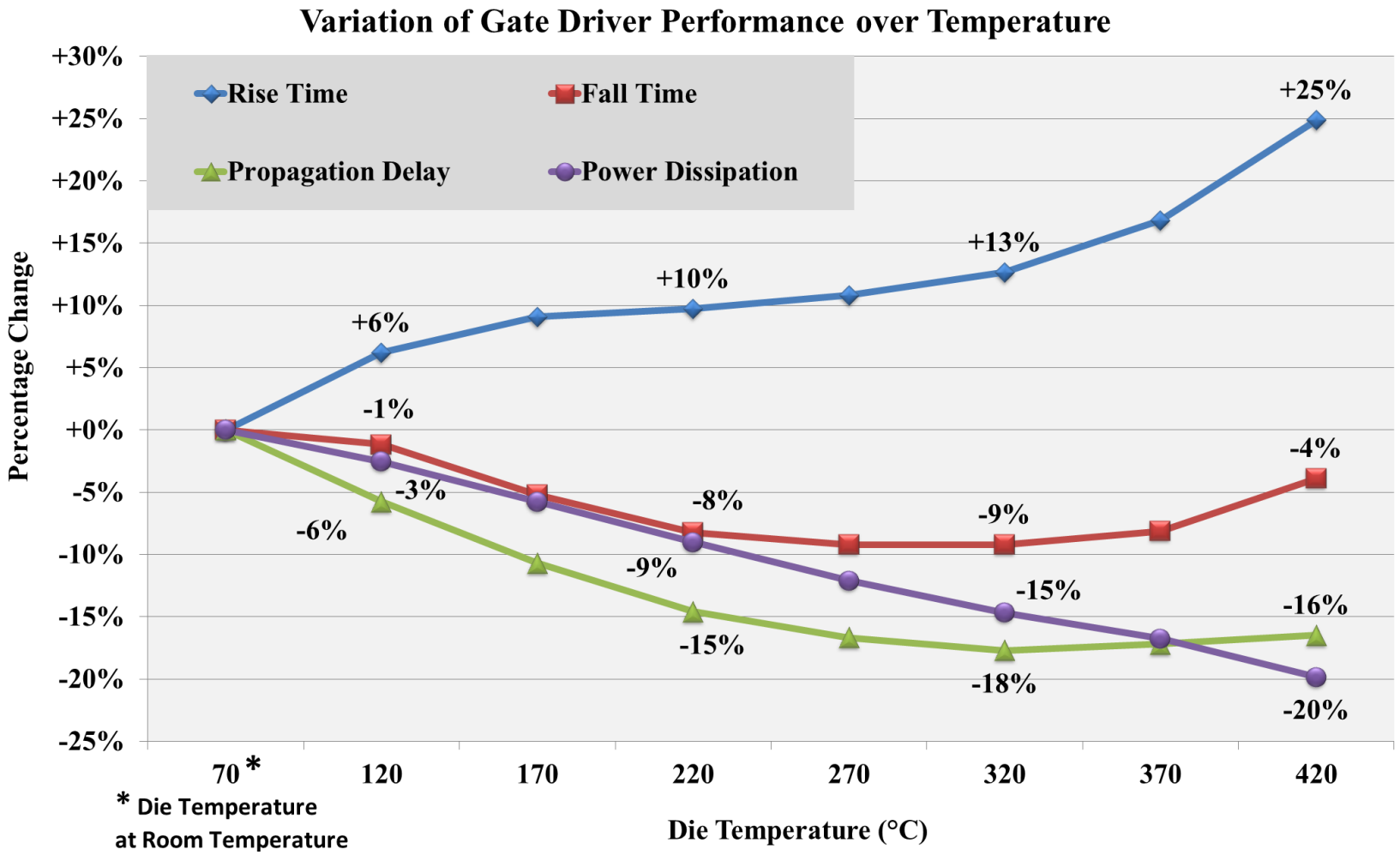


Fig. 8.15 Percentage change in gate driver parameters with increasing temperature.

As summarized in Fig. 8.15, the percentage change in gate driver specifications are minimal over temperature and the consistency shown by the gate driver over this wide range of temperature is impressive. The *rise time* is the only parameter that degrades with increase in temperature, all other parameters decrease with increase in temperature which is good.

The targeted normal operating temperature for this gate driver is 125 °C. We can see that there is only 6% of variance in the output rise time at this temperature which is very impressive. The gate driver rise time increases by only 10% even when the die temperature is at 220 °C, at which point a Silicon MOSFET based circuits would be basically useless. This is because bulk silicon MOSFET based circuits start behaving in unacceptable ways above 150 °C primarily because of high-temperature leakage current inherent to operation of silicon [6]. It can be seen in Fig. 8.15 that even at 320 °C, the SiC gate driver is functioning very well with only 13% increase in rise time; at this point i.e. beyond 300 °C even HTSOI CMOS would stop operating reliably [6]. We can see that this SiC gate driver circuit works well above the 300 °C mark and up to 420 °C and still gives acceptable performance with rise time increase of 25% relative to room temperature rise time. The most impressive thing, however, is the decrease in power consumption which indicates the transistors are not leaking significant current which is very important in high temperature applications to maintain circuit efficiency and functionality.

The transconductance of the NMOSFET in the Cree SiC process was tested using the probe station and the observed data is summarized and plotted in the chart in Fig. 8.16. This shows that the transconductance increases with increase in temperature in SiC process.

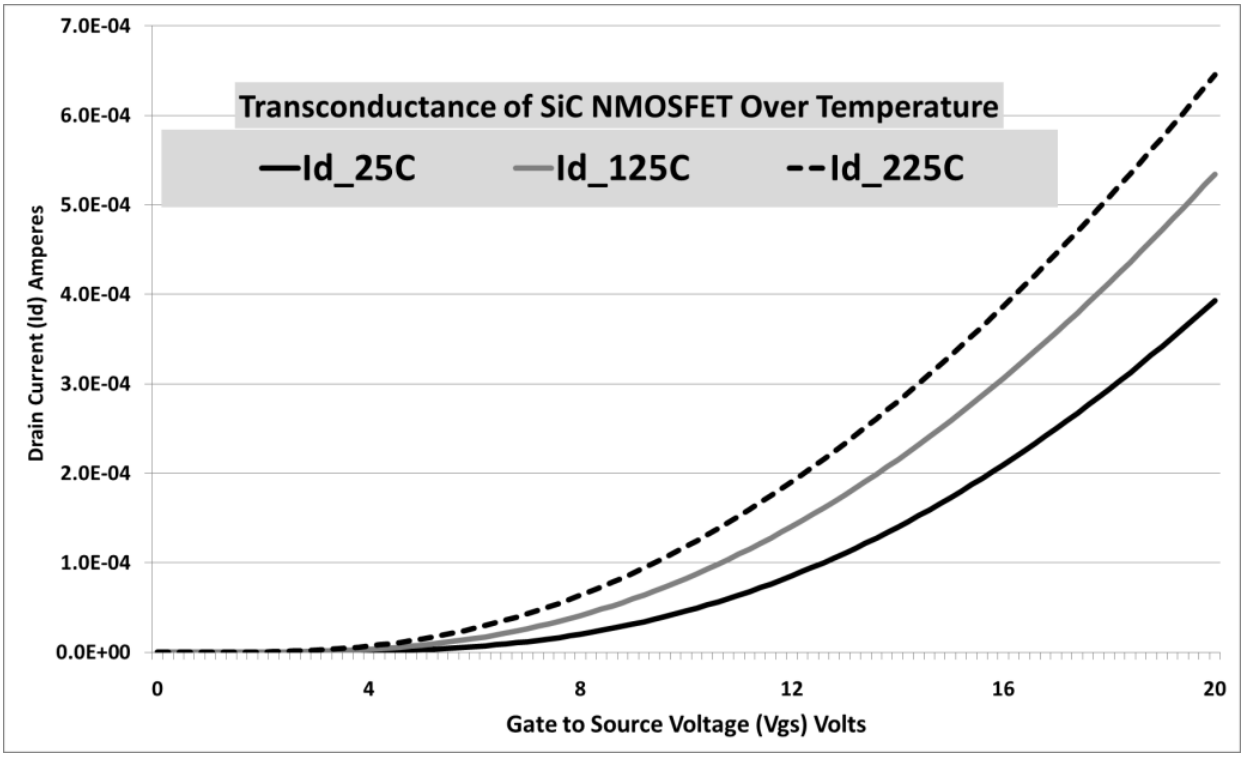


Fig. 8.16 Transconductance comparison over temperature of the parasitic extracted model.

8.4.1 Rise Time Behavior

The reason for increase in rise time with increase in temperature is because the diffusion resistance has positive temperature coefficient which means the resistivity will increase with temperature. This causes the resistor *R_OD* at *biased common-gate overdrive circuit* block to increase which directly affects the rise time of *totem-up* signal and eventually affects the *rise time* of *output* signal (refer Fig. 4.1). The effect of increase in transconductance, as shown in Fig. 8.16, with increase in temperature is outweighed by the increase of resistivity over temperature for this particular parameter because of its heavy reliance on the resistor *R_OD* of *biased common-gate overdrive circuit* (refer to Fig. 4.1).

8.4.2 Fall Time Behavior

The *fall time* decreases due to the increase in transconductance of the device as shown in Fig. 8.16. Since the *fall time* of the device is not directly associated with any resistors, the increase in resistivity doesn't affect the *fall time*.

8.4.3 Power Dissipation Behavior

The reason for decrease in power dissipation with increase in temperature is primarily due to the resistor *R_OD* at *biased common-gate overdrive circuit*, refer Fig. 4.1. This resistor dissipates a lot of power, especially when the *totem-up* signal is low, so when the value of this resistor increases with increase in temperature, the power dissipation decreases significantly. The resistor *R_OD* of the overdrive circuit dissipates almost 60% power consumed by the entire gate driver. The decrease in power dissipation is further augmented by increase in value of other resistors in the circuits as well, since this is an NMOS process and each circuit has a resistor involved in it.

8.4.4 Propagation Delay Behavior

The decrease in *propagation delay* with increase in temperature is because of the fact that the threshold voltage (V_{TH}) of the SiC MOSFET decreases with temperature and causes the device to turn on faster. The induction of *propagation delay* in the signal path is primarily because of the V_{TH} of the device which makes the signal wait for a certain amount of time before allowing it through the signal path. These delays accumulate in successive stages and manifest as final *propagation delay* at the output. When the V_{TH} of the devices decreases over temperature, these delays are shortened and, hence, the overall *propagation delay* decreases at higher temperatures.

9. CONCLUSIONS AND FUTURE WORK

9.1 CONCLUSIONS

SiC circuits will have massive impact on future power electronics systems on a vast gamut of applications decreasing their size and cost, and increasing their efficiency, robustness and reliability [26]. The gate driver circuit is a very important part of such systems directly affecting the systems prominent performance parameters like overall size, efficiency, and cost. Due to material properties of Silicon, Silicon and Silicon on Insulator technologies are unlikely to offer advantageous circuits beyond the 300 °C operating temperatures and for high-power switching applications [6]. SiC, however, with its superior properties is a very promising technology for these applications.

The presented work in this thesis comprises a gate driver in SiC technology which can operate beyond 400 °C temperature range and switch at high frequencies beyond 500 kHz. The only other SiC gate driver developed to date has rise and fall times that are more than three times greater than the presented gate driver in this thesis and clipped final output voltage [27]. Several new circuit topology and new design and layout approaches were employed to develop this gate driver to overcome several constraints imposed by the fledgling SiC process. The novel circuit topologies and approaches presented in this thesis can be used in any other present or future NMOS only process to overcome process limitations and strictures.

The fabricated gate driver was tested and found to be operable at temperatures ranging from 25 °C to beyond 400 °C with only slight variation in performance parameters. The rise and fall times with a SiC Power MOSFET load, which is a larger load than a 4 nF capacitor, was measured to be as low as 45 ns and 41 ns respectively with power dissipations of only about 6 W

at a 500 kHz switching frequency. The propagation delay is less than 200 ns which is the targeted specification.

This gate driver is the highest temperature rated gate driver to date, the maximum temperature rated gate driver that can be found in literature search can operate up to 225 °C and was designed in SOI technology [4]. The integration of this developed gate driver with SiC power MOSFETs in a power electronic system could lead to significant reduction in cost, size and complexity of the system with increased electrical performance due to better switching properties of SiC and better thermal performance due to better thermal conductivity of SiC.

This particular gate driver was developed for integration and operation demonstration in Toyota Prius Plug-In Hybrid Electric Vehicle (PHEV) with the main objective of commercialization in the future. Fig. 9.1 shows the demonstration of charger installation in the Toyota Prius PHEV. According to the program goals, this would result in a more efficient charger system with 5 times more output power and 10 times reduction in size, weight and cost.

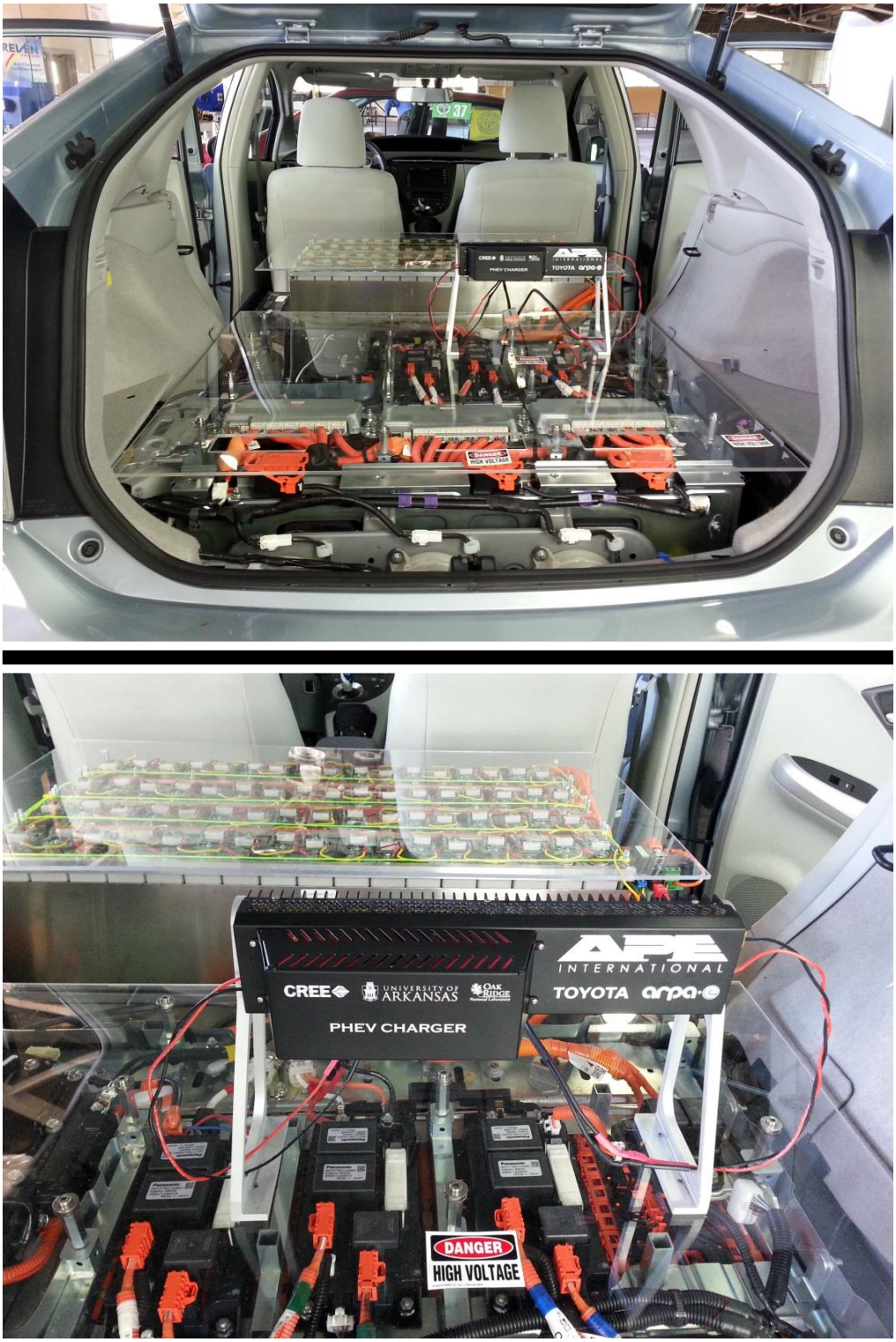


Fig. 9.1 Demonstration of the SiC charger installed in the Toyota Prius PHEV.

(APEI. April 2013. NCREPT. JPEG file)

9.2 FUTURE WORK

The designed gate driver with all its blocks and components and even the protection and sensing circuitry can be fabricated in a single chip. The present limitation, however, is that the integration with the power MOSFET itself is not possible with current Cree SiC process development stage. This would be the next step on the research and development phase on this gate driver considering the substantial performance and robustness boost that this integration would render. The overall integration would aid in significant reduction of parasitic inductance allowing for better gate driver and overall system performance.

The other possible enhancement would be to improve the process by decreasing the resistivity of poly in the process, add an extra metal layer for routing, and/or incorporate a PMOS device as well to make it a CMOS process. This would greatly increase the performance of the gate driver. As the process evolves and gets more sophisticated, required alterations can be made to the gate driver to tweak its performance and robustness to realize an overall better product.

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