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Designing and Implementing a Micro-controller based Primary-side Sensing Flyback Converter for LEDs Driver

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ABSTRACT

The fast development of LED and its applications has enabled a new generation of lighting device with higher efficiency and long lifespan. By employing a primary-side sensing flyback converter and the PIC18F micro-controller series, an LED driver could achieve two important features: (1) the compatibility with the available lighting fixtures, and (2) reducing unit price. The flyback converter was chosen for its simplicity, competitive low cost, and its ability to provide a constant output current, a necessarily important factor to an LED driver. Meanwhile, the PIC18F micro-controller series offer numerous advanced features which include but not limited to pulse-width modulation (PWM), 10-bit 13-channel Analog-to-Digital Converter (ADC) etc., which suitably meet the requirements for regulating a primary-side sensing flyback converter. The design process was first conducted in simulation stage with aid from Matlab®-Simulink and Cadence OrCAD Capture CIS (PSpice). By using PI based control scheme and making full use of built-in Analog Behavioral Modelling (ABM) blocks, the simulation-relevant difficulties due to lacking of appropriate model for the PIC18F series micro-controller were completely solved. The simulation results matched well with the intended design specifications: the output voltage is 32 VDC while the load current is 350 mA. More importantly, the simulation results demonstrated the feasibility of deploying a primary-side sensing flyback converter in conjunction with a PIC18F micro-controller as an LED driver. Next, a demo printed-circuit board (PCB) was layout by using OrCAD PCB Editor. Finally, the PIC18F4550 micro-controller was programmed to undertake control tasks of the LED driver. The experimental results reflect the project's success with all the parts of the driver harmoniously work as expected.

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Introduction

1.1 Overview

When it comes to electrical energy consumption, there is a truth that may make a lot of people to be amazed. According to the International Energy Agency, lighting accounts for 20 percent of energy consuming all over the world [1]. In fact, the omnipresence of incandescent bulb is the reason for such a high energy consuming percentile. The obsolete incandescent bulb normally converts only 5% of input energy to light and dissipates the rest to the outside environment in the form of heat. This means that one of the most popular electric device in the world is also the most inefficient electric device. Despite the introduction of some new lighting devices, likes the compact fluorescent lamp (CFL), the relatively low price and the shopping habit of most consumers make the incandescent bulb to be an indispensable one in lighting market. Consumers just do not want to buy a new lighting product and then have to replace the whole lighting fixture too. From the customer's perspective, they want to buy a new product with a low price but it must also easy to use. This is a very important thing that all designers must consider during the design process.

A solution for replacement of inefficient lighting device is using new generation light-emitting diode (LED) bulb. The development of semiconductor technology improves the lighting ability of LED significantly year over year. An LED is basically a semiconductor diode except the ability for light emitting when it is forward biased. An LED bulb is going to provide more lighting while consumes less energy. More importantly, its price will drop continuously in the near future. The latter is one of two main factors that prevent LED bulb to be welcomed on the lighting device market since the price range of an LED bulb is still relatively high compared to two of its opponent: the CFL and the incandescent bulb. Spending the same amount of money for an LED bulb, consumer could buy three CFLs, or even twenty incandescent bulbs with the same wattage. However, this correlation is being changed continuously.

Despite having an unattractive price, LED bulb is invincible when it comes to efficacy, which means that LED bulb can achieve an impressively high light output per watt. Along this outstanding feature, the durability of an LED bulb is another great advantage that is normally ignored by consumers. Many manufacturers claim that the average lifespan of an LED bulb is more than 20 years, which will possibly be the last survivor among all the appliances you buy on the same day. In addition, the long-term benefit of an LED bulb will demonstrate its uniquely high efficacy mentioned above when the total running cost is considered [2]. A research that was done by Men's Journal magazine shows that the total cost for running a lighting system of an American family with 40 bulbs of incandescent type in 20 years (three hours of daily use with national average electricity price) is more than 4 times ($6,300) the cost for the same system but using LED bulbs ($1,431). Even with the CFL bulb, which is advertised as a very economical one, the total cost for that lighting system is one-and-half higher ($2,106) than the LED system. The complete comparison is shown in Fig. 1.1. It should be noted that the total cost did not

include the expense for replacing new bulb. Since the lifespan of an LED is over 20 years, no LED bulb is expected to be replaced the whole interval. Meanwhile, each incandescent bulb could hardly work more than a year. Thus, consumers with incandescent lighting system may have to replace at least 19×40 = 760 times during 20 years (in case no more than one bulb stops working at the same time). The situation is somehow improved with CFL bulb with each of this type can last for up to 6 years but this replacement cost will undermine its ability to attract customer.

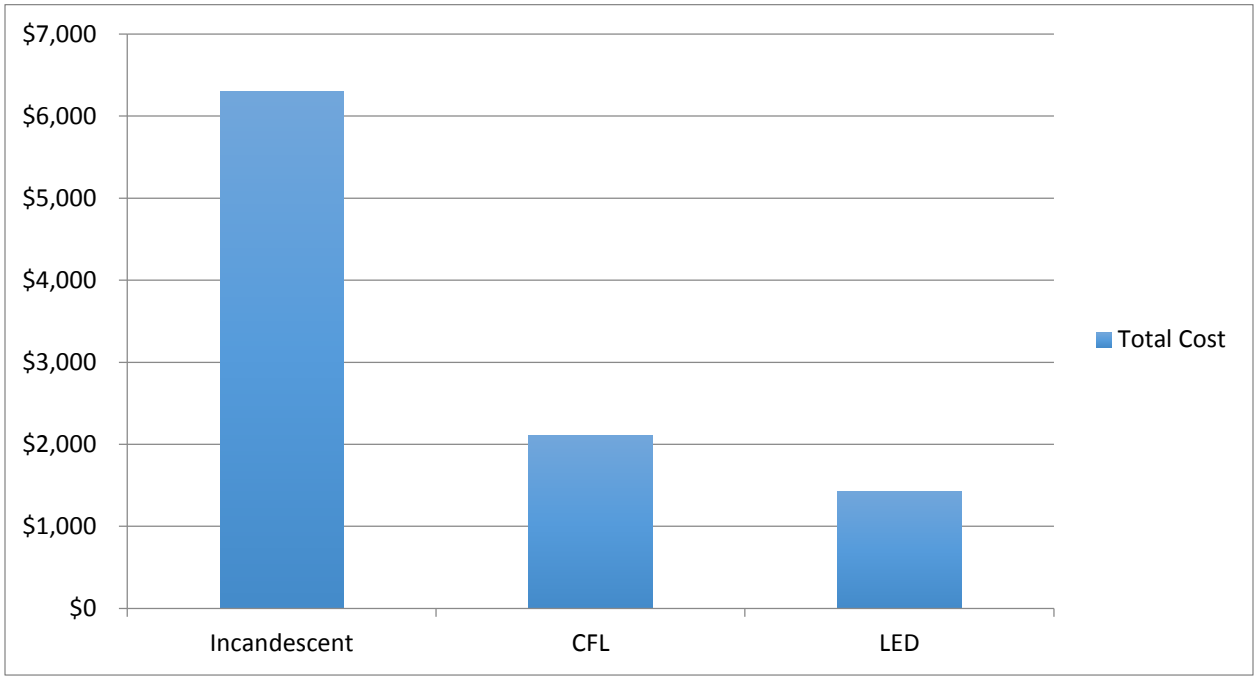


Figure 1.1 – The total cost for using Incandescent, CFL, and LED bulbs for 20 years.

As mentioned above, the prohibitively expensive price, which will soon to be reduced, is one of two main barriers that prevent LED bulb from becoming a popular lighting product. The other factor is the compatibility of the new generation LED bulbs. In spite of having the long term benefits likes long lifespan, cost saving, and environmentally friendly product, LED bulbs would

not able to persuade customers if it required them to purchase additional accessories. From design perspective, it is better to have LED bulb that works perfectly with current available fixtures. Buying a new lighting product with a little bit higher price, customers should be satisfied with their decision for many long term benefits and how easily it mounted on the available fixture at home.

1.2 Purpose and organization of this thesis

The main purpose of this thesis is to design a micro-controller based flyback converter for driving the LED lighting load. The design process starts with simulation task in Matlab/Simulink and Cadence' PSpice (OrCAD Capture CIS). After successfully obtaining design-matched results, a demo board will be designed in OrCAD PCB Editor. The artworks is then transferred to a PCB manufacturer to fabricate. Finally, the micro-controller will be programmed for driver's control purpose. A brief introduction about design specifications and considerations will be presented in Chapter 2 (Design specifications and considerations). Details about simulation works and hardware implementations will be discussed in Chapter 3 (Simulation of a micro-controller based primary-side sensing flyback converter for LED driver), and Chapter 4 (Hardware implementation), respectively. Chapter 5 is about experimental results and Chapter 6 will concludes the thesis.

Chapter 2

Design specifications and considerations

2.1 Design specifications

In order to design a driver for an LED that provides all advantages as in the previous chapter, design engineers should meticulously consider all the dimensions. Its form should be small enough to fit within the available commercial fixture, and that small driver should meet all the required technical specifications (power factor (PF), brightness, etc.). Building an LED driver based on a DC-DC switching converter with control task is undertaken by micro-controllers has recently attracted designers for various reasons. The modern micro-controllers are not only extremely powerful but also small enough to be integrated in an LED driver. They offer great a

flexibility with numerous built-in functions like pulse-width modulation (PWM), Analog-to-Digital converter (ADC), timer etc., which allow designers to do many tasks without equipping dedicated circuits. More importantly, benefiting from the development of semiconductor industry, micro-controller is becoming cheaper, greatly contributes on the effort of lowering an LED driver's price.

The work of selecting the DC-DC switching converter candidate for an LED should take into account some features like topology, performance, and implemented cost. Flyback converter emerges as an optimized choice for its simplicity, excellent input voltage-input current relationship, and low cost. The simplicity of the whole driver circuit will be greatly enhanced by regulating the output from the primary side of transformer. Using primary side sensing and regulating not only helps to save the board size by getting rid of unnecessary component like optocoupler but also eliminates its unwanted instability effects. Therefore, the LED driver's price would be further decreased while the performance is also improved.

The design specifications of a micro-controller based primary-side sensing flyback converter for LED driver is tabulated in Table 2.1. The schematic for this driver is illustrated in Fig. 2.1.

Table 2.1 – Design specifications

Input voltage (RMS)	120 VAC, 60Hz
Output voltage	32 VDC
Output current	350 mA
Switching Frequency	100 ± 10 kHz
DC-DC converter type	Flyback
Primary-Side Sensing & Regulating	Yes
Magnetizing inductance	40 µH
Secondary winding inductance	8 µH
Transformer's turn ratio	2.23/1
Micro-controller	PIC18F4550

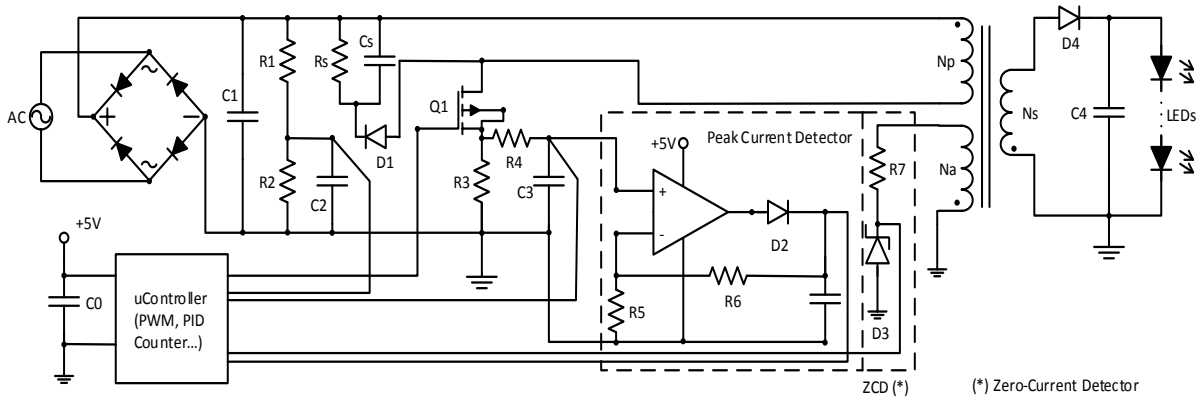


Figure 2.1 – Schematic of the LED driver with micro-controller and primary-side sensing flyback converter.

The design process of an LED driver will start with simulation, using Matlab-Simulink and Cadence's PSpice (OrCAD Capture CIS). Next, the prototyped printed circuit board (PCB) will be designed using OrCAD PCB Editor Lite, which includes in the same free package from Cadence. The artwork files then will be transferred to a PCB manufacturer to fabricate. For demonstration purpose, the components of PCB are selected based on technical specifications only. Therefore, many of components are through-hole devices, which have larger footprint. The board size should be shrunken considerably by using surface-mount devices (SMD) if the prototyped board worked flawlessly and was ready to be commercialized.

2.2 Micro-controller as a driver's controller

Dedicated mixed-signal switching controllers used to be a regular choice for flyback converter regulating work. However, it is not as flexible as most of the modern micro-controller and is gradually being replaced by numerous modern, powerful, and multi-function micro-controller families [3]. Having a lot of built-in functions, micro-controllers allow designers to add more features to the same current board by simply changing control algorithms. No circuit is required

to be added, therefore the current board would not become more complicated. It means that designers will be able to provide their customers with more utilities on the same product with not too much cost for upgrading.

Selecting an appropriate micro-controller is not an easy task. Each manufacturer likes Atmel or Microchip Technology has various families of chip that can meet every control purposes. Even in each family, there are hundreds of type which different from each other by package, amount of memory, speed etc. In general, the task of selecting a micro-controller for a specific project should be based on the following criteria [4]: (1) The ability of micro-controller to provide enough strength with a reasonable price to meet all the design requirements, (2) How easy is it to program, load, and test with the micro-controller?, and (3) The supply source of micro-controller.

The selected micro-controller for this current project is Microchip Technology's PIC18F4550 (Fig. 2.2). First of all, this 8-bit controller is equipped with 2 Capture/Compare/PWM (CCP) modules, which is suitable for controlling a flyback converter. With 4 timer modules (3 16-bit type and 1 8-bit type), 35 I/Os with 10-bit 13-channel Analog-to-Digital Converter, signal acquisition task becomes a less burdensome work [5]. The PIC18F4550's 32Kbytes of Program Memory and 2048 bytes of Data Memory are abundant for this small LED driver circuit. In addition, the price for one unit is relatively cheap, just less than $5 for 10 units [6] and it will be decreased dramatically if the order quantity exceeds 100 units. Its programmer, PicKit 3 provides us with a friendly software kit, includes C compiler for free. This product also has a stable supplying source from its manufacturer Microchip Technology or from other electronic component distributors like Digikey or Mouser. In conclusion, the PIC18F4550 micro-controller suitably meets all the requirements for this LED driver project.

Table 2.2 – Main characteristics of the micro-controller PIC18F4550

Package	DIP
Number of pin/Number of IO	40/35
Internal Oscillator	Up to 8 MHz
Timer Module	4 (Timer0 – Timer3)
CCP Module	2 (1 CCP/1 ECCP)
ADC Module	10-bit, up to 13 channel
Operating Voltage Range	2.2 – 5 V
Program Memory	24 Kbytes Flash
Data Memory	2048 bytes SRAM
Programmer	PicKit3
Integrated Development Environment	MPLAB X
Programming Language/Compiler	C/MPLAB XC 8 Compiler

Figure 2.2 – PIC18F4550 micro-controller and PicKit3 Programmer.

2.3 The Flyback Converter

Flyback converter was selected among many DC-DC switching converter topologies for a lot of its advantages compared to the other. The absence of output inductor greatly contributes to the competitive low cost for flyback converter since the board size could be shrunken while the

budget does not have to include the inductor's price (Fig. 2.3). It is replaced by a transformer, which will be able to provide an isolation between the load and the source side [7]. With no direct connection between the two sides, safety is no longer a concern for a flyback-based circuit. This transformer also stores and releases magnetic energy, each operation respectively corresponds to the non-conducting and conducting interval of the secondary side's diode.

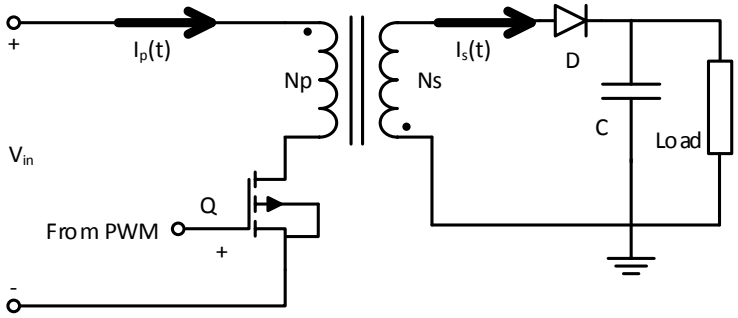


Figure 2.3 – A Flyback converter.

One characteristic that makes flyback topology to become the apparent choice for the LED driver is its ability to provide a constant output current or voltage, depends upon discontinuous current mode (DCM) or continuous current mode (CCM) operations. In the case of LED bulb, its brightness heavily depends on the forward current flowing through [8]. Thus, an LED driver should be designed with a constant current output in order to obtain the required performance. For those reasons, a flyback converter which works in DCM operation mode is the exact answer for this project. In addition, the flyback topology has an excellent linear relationship between the average input current $i_{in,avg}(t)$ and voltage $v_{in}(t)$ as

$$i_{in,avg}(t) = \frac{D^2 T}{2L_p} v_{in}(t) \tag{2.1}$$

which results in a very high power factor. In the above formula, D is the duty cycle, T is the switching period, and L_p is the magnetizing inductance of the primary winding. This superb

relationship makes flyback converter to be one of the most favorite choices when it comes to power factor correction. The lowest allowable power factor is an important requirement for new household appliances and must comply with specific regulations, depend on whether it uses for residential or commercial purpose.

Apart from conventional flyback converter, one distinctive feature of the converter in this project is the primary side regulation. Primary side sensing and regulating is the preferred method for this isolated converter since it makes the circuit to be less complicated and also makes full use of the PCB space more efficiently. This helps to save some cost and contribute to the effort of reducing price for the whole circuit. In this project, there is no need for the traditional isolated feedback circuit since the secondary side's operation can be monitored by using an auxiliary winding of transformer in companion with micro-controller's counter. The elimination of the optocoupler in the feedback circuit not only lessens the complex of circuit but also completely eradicates unwanted effects from the optocoupler due to temperature change.

Input voltage for the flyback converter in this project is a DC voltage with $V_{in,\max} = 120\sqrt{2} \approx 169$ V, which is rectified directly from the AC source. When the switching transistor Q is ON, the primary side current is increased linearly until it reaches the maximum value of:

$$I_{p\max} = \frac{V_{in,\max}}{L_p} t_{on} = \frac{169}{40\times10^{-6}} \times 0.83\times10^{-6} = 3.5 \text{ A} \qquad (2.2)$$

with t_{on} is the conducting interval of the switching transistor. This on-time can be chosen from 0.5 µs to 5 µs. The on-time value selected here is 0.83 µs, which is equivalent to 0.005% of one full cycle of 60-Hz AC source (approximately 16.6 ms). During t_{on}, the secondary side's diode

will be reverse biased due to inversed polarity and the load current is supplied by the output capacitor.

At t_{on}, the switching transistor is OFF and the polarity of the transformer's primary winding immediately inverses. The secondary side's diode is now forward biased, conducts current from the secondary winding to load. This current will decrease linearly, starts from its peak value $I_{s\max}$, which has the following relationship with primary side peak current:

$$\begin{aligned} I_{s\max} &= N \times I_{p\max} = \frac{N_p}{N_s} \times I_{p\max} = \sqrt{\frac{L_p}{L_s}} \times I_{p\max} \\ &= \sqrt{\frac{40}{8}} \times 3.5 = 7.83 \text{ A} \end{aligned} \tag{2.3}$$

If this current is designed to completely diminish before the switching transistor switches ON again, this mode is called discontinuous current mode. The expected average load current for driving a 1W LED is 0.35 A. The secondary side's diode conducting interval can be known if the moment at which the secondary side's current goes to zero (t_2) is identified. The value of t_2 may be obtained from:

$$I_{avg} = \frac{1}{2} I_{s\max} \frac{t_2}{T} = \frac{1}{2} I_{s\max} \times t_2 \times f \tag{2.4}$$

$$\Rightarrow t_2 = \frac{2 \times I_{avg}}{I_{s\max} \times f} = \frac{2 \times 0.35}{7.83 \times 10^5} = 0.89 \text{ μs} \tag{2.5}$$

This calculated value demonstrates that the operating mode is DCM because $t_2 < T = 1/f$. The DCM operating mode assures a desired constant output current, delivers an excellent transient response, and also will be able to provide power factor correction feature for the flyback converter. The DCM operating mode, however, requires some components with larger ratings.

As mentioned above, the flyback converter in this project will deploy primary-side sensing and regulating feature. An auxiliary winding of the transformer will be used to monitor the secondary side operations. Assume the inductance of auxiliary winding is 1 μH, its voltage will be:

$$V_a = V_p \frac{N_a}{N_p} = V_p \sqrt{\frac{L_a}{L_p}} = 169\sqrt{\frac{1}{40}} = 26.7 \text{ V} \tag{2.6}$$

A voltage sense is formed by a zener diode and a resistor. This voltage level will be acquired and then compared with a pre-defined threshold voltage, which is stored by the micro-controller, in order to detect the conducting interval of the secondary side's diode. The secondary side's diode conducting interval will be combined with signal from peak current detector, sample signal of input rectified voltage and the primary side switching current as four inputs of the micro-controller. The micro-controller's PWM feature processes data, then compares with an in-register stored preset value before making decision. If mismatch between the calculated and preset value is not within allowable tolerance, the duty cycle will be adjusted. Otherwise, no action will be triggered from the micro-controller.

2.4 Simulation

Simulation is vitally an important stage at the beginning of any design process. Unfortunately, it is impossible to set up a straightforward environment for PIC18F4550 micro-controller's behaviors with available tools. By exploiting the first order mathematical model for the flyback converter and using Matlab-Simulink, Cadence's PSpice (OrCAD Capture CIS) and a PID based control scheme, several critical features of the micro-controller (PWM, counter etc.) can be simulated. The simulation process will be discussed in Chapter 3.

2.5 Demo board design

In order to minimize any potential mismatch in design, the PCB design process will start with OrCAD Capture CIS for schematic drawing and then export to OrCAD PCB Editor for layout. The two parts from the same Cadence's Suite helps the design process to be proceeded seamlessly.

Most passive components have defined footprints. However, some components like transformer and micro-controller, whose footprints are not supplied by manufacturers, require manual footprint design. This work becomes less difficult with OrCAD PCB Editor's Footprint Wizard feature. In fact, this feature allows designer to draw any type of footprint, as long as the component's datasheet is available.

Since the design board here is just a demo version, the component selection was not optimized. Some parts might have large footprint and do not follow the board-shrinking spirit due to employing through-hole technology one. The board size can be enhanced by replacing through-hole devices with the same-specification, equivalent SMD parts. This task will be done if: (1) the demo board works properly, and (2) the driver is commercialized.

The PCB design task is finalized by comparing the generated artworks with their predecessor layout. Although the generated artworks can be investigated by PCB Editor itself, the design results should be viewed in a completely independent tool. If the different softwares bring out the same results, the artworks' verification is justified.

2.6 Programming

The official programming language that will be used for PIC18F4550 micro-controller is C. The Integrated Development Environment and Compiler are free to download from the

manufacturer's website (www.microchip.com). Code will be conveniently loaded to the micro-controller using PicKit3 programmer through USB interface.

Chapter 3

Simulation of a micro-controller based primary-side sensing flyback converter for LED driver

3.1 Introduction

Simulation plays a vital role in electrical engineering design process. As the electronic circuits and systems have become more complicated, computer simulation has demonstrated its usefulness in comparing the traditional design verification with breadboard [9]. With the development of modern computer technology and algorithms, the results of simulation can perfectly reflect behaviors of electrical components. Simulation helps design engineer to save not only the cost but also a lot of time since it provides useful information about every component effects on the overall result. Therefore, the LED driver design process in this project started with simulation task.

When it comes to simulation in electrical engineering, Cadence's PSpice (OrCAD Capture CIS) emerges as one of the most favorite choices for designer engineers. It is convenient, powerful,

and has very friendly user interface. PSpice not only provides a tremendous amount of parts but also motivates the designer's creativity by developing new components on his own. Because of this feature, there are thousands of self-made libraries distributed on the Internet, including both free and paid packages. In addition, many electronic vendors consider PSpice as an industrial standard and publicly supply their own product's libraries for free of charge.

Despite the fact that there are numerous ready-to-use PSpice-compatible libraries of micro-controller, it was hard to find a library which contains our chosen one, PIC18F family. The reason originated from the fact that this microchip's product series offers too many advanced features to represent in just only one mathematical model. This means that at the very first step of the simulation task, we have to find a solution to overcome the absence of PIC18F family library.

Two solutions were proposed. The first one is to construct a mathematical model for PIC18F4550 micro-controller that presents exactly all behaviors we need from this chip (PWM, counter, etc.). This solution seems to be an overwhelming as well as time-consuming work with low feasibility. The second one is to make use of Cadence's built-in Analog Behavioral Model (ABM) libraries in conjunction with PID-based control algorithm in order to present necessary features of PIC18F4550. This plan promises to provide the same equivalent results but requires a significantly smaller amount of time.

3.2 PID-based control scheme

PID is one of the most widely used controllers in industry since it provides not only good output performance in a wide range of working conditions but also the simplicity, ready-to-use tuning

strategy [10]. In this simulation, the popular three-term PID transfer function in frequency domain will be used as follows:

$$G(s) = K_P + \frac{K_I}{s} + K_D s \tag{3.1}$$

in which K_P, K_I, and K_D are proportional, integral, and derivative coefficients that represent the correspondent terms, respectively. In fact, the derivative term has the following transfer function:

$$G_D(s) = \frac{K_D s}{\tau_D s + 1} \tag{3.2}$$

with τ_D is small enough compared to the time constant of the process itself and usually can be neglected. In Simulink, there is a built-in block PID with the following transfer function:

$$G(s) = P + I\frac{1}{s} + D\frac{N}{1 + \frac{N}{s}} \tag{3.3}$$

in which N is defined as the "Filter Coefficient", which has a default value of 100. With P, I, and D play role of K_P, K_I, and K_D, we can see the relationship: $\tau_D = 1/N$. Therefore, the value of 100 for N could be left unchanged or set as large as possible while working with this built-in PID block in Simulink.

3.3 Modeling the flyback converter

A mathematical model for the primary-side sensing flyback converter is necessary for control design procedure. As the flyback converter operated in discontinuous current mode (DCM), a very high power factor will be achieved [11]. Because of this reason, the expected input

characteristics of LED are similar to a pure resistor that we use as a load in this simulation. With such resistor-like load, the control target is achieving and maintaining the output voltage of the flyback converter as close to 32 V as possible so that the current flowing through 1W LEDs is about 350 mA while the settling time and rising time should be small enough to guarantee the fast response of an LED bulb. The percent overshoot is also expected to be small as an LED is basically a diode, so that a small change above the forward biased voltage could make a significant change in current. A first-order model for the flyback converter is suitable for this research because it provides not only the simplicity but also the reasonable accuracy.

For the current flyback converter, its mathematical model was built based on the following parameters and formulae using Matlab:

- L_PRI=40*10^-6: Inductance of the transformer's primary coil (40 µH).
- L_SEC=8*10^-6: Inductance of the transformer's secondary coil (8 µH).
- Vin=1.414*120: Amplitude value of input voltage ($120\sqrt{2} \approx 169$ V).
- Np=2.25: Number of turns for the transformer's primary coil.
- Ns=1: Number of turns for the transformer's secondary coil.
- Naux=0.83: Number of turns for the transformer's auxiliary coil. An auxiliary coil will be used to detect the conducting time of the secondary side's diode without using a feedback system directly from the secondary side. The advantages of this primary-side sensing technique was introduced in Chapter 2.
- f=100*10^3: Switching frequency of the flyback converter (100 kHz).
- Vout=32: The expected value of output voltage (32 VDC).
- Iout=0.350: The expected value of output current (350 mA).

- Rout=Vout/Iout: Ohm's law used to calculate equivalent resistance of the LED with assumption that flyback converter was operated in DCM.
- Caux=100*10^-9: Capacitance of load capacitor on the auxiliary side (100 nF).
- Csec=100*10^-6: Capacitance of load capacitor on the secondary side (100 µF).

The first order transfer function of the flyback converter has a form of [12]:

$$T(s) = \frac{\text{Gain}}{\frac{1}{2}R_e C_e + 1} \tag{3.4}$$

in which R_e and C_e are the equivalent resistance and capacitance of the flyback converter. They are calculated for the simulated model as follow:

- Re=(Vout)^2/(Vout*Iout): Equivalent resistance is exactly the calculated resistance of the LED above.
- Ce=Caux+Ns/Naux*Csec: Equivalent capacitance of the model is calculated as a sum of load capacitance on the auxiliary side and the load capacitance on the secondary side referred to the auxiliary side. The factor ½ on the denominator of the transfer function accounts for those two load capacitors.

The "Gain" value depends on the mode of operation. With the intended mode being selected as DCM, formula to calculate the value for "Gain" is: Gain=Vin*Ns/Np*sqrt((Re)/(2*L_SEC*f)).

Finally, the first order transfer function in frequency domain of the flyback converter is:

$$T(s) = \frac{570.1}{0.04642s + 1} \tag{3.5}$$

Having the mathematical model for the flyback converter means the object control has been identified. We proceed to the next step: design the controller and the feedback system.

3.4 Controller and feedback system design

The chosen controller is PID-based scheme for various advantages as mentioned in Section 2 of this Chapter. For this type of controller, several ways to determine gains, called PID tuning, were introduced.

The first approach is manual tuning in which all three parameters K_P, K_I, and K_D are acquired manually with no math required [13]. Since there is no explicit mathematical formula to obtain PID's parameters, this method may bring some confusions to inexperienced designers due to complicated relationships between the adjustments of gain and design specifications. For example, the increase of K_P helps lower the steady-state error, but equally makes the percent overshoot increase with a very little impact on the settling time. Meanwhile changing K_I on the same manner brings 0 for steady-state error with the improvement for both the percent overshoot and the settling time. In addition, determining gains without a mathematical formula means the design process will be done with testing and detecting. This method might be a very time-consuming and tedious task for people with no deep insight about PID.

A widely used rule of thumb for manual tuning is to first set both K_I and K_D to 0. K_P will be adjusted increasingly until the system becomes oscillated using root locus method. The value of K_P that makes the system oscillated will be divided by 2 to obtain the proportional gain. Next, K_I will be incremented in order to achieve a reasonable rise time. The integral gain should not be too big to avoid instability for the system. Next, the derivative gain will be adjusted to meet the

design specifications of the percent overshoot and the settling time. This process seems simple at first but it requires a lot of experiments and does not guarantee the convergence.

The Ziegler-Nichols tuning method was introduced in the 1940s. It is a proven method with explicit mathematical formula for each P, PI, and PID controllers. It is useful for the case that requires an ability of disturbance rejection and a fast closed-loop step response with no excessive oscillation. The process of identifying gains establishes in the same manner with manual tuning by setting both the integral and derivative gains to zero, and then increasing the proportional gain until the system reaches its boundary of oscillation. The value of K_P that makes the system become oscillated was denoted as K_U – the ultimate gain. Measuring the period of system oscillation, we acquire T_U – the ultimate period.

From the ultimate gain K_U and the ultimate period T_U, the proportional, integral and derivative gains of P, PI, and PID controllers will be determined, depending on the type of the controller being considered. If a proportional controller is enough, its proportional gain will be set as $0.5K_U$. In case a proportional-integral controller is necessary, the proportional gain and integral gain are $0.45K_U$ and $0.54K_U/T_U$, respectively. If a full three-term PID controller is required, the proportional, integral, and derivative gains are $0.6K_U$, $1.2K_U/T_U$, and $0.6K_UT_U/8$, respectively.

Design with aid from software has emerged as the first choice for engineers in the recent two decades. With the rapid development of computer technology and algorithm, CAD/CAM tools guarantee optimized, highly reliable, consistent results in acceptable running time. The disadvantage of using tuning software is the relevant cost for purchasing and training might be relatively high. In this project, we will use a low-level aided tool, named SISO Tool for design purpose. This software, which is a built-in part of MATLAB [14], was used in companion with Simulink to design the PID controller for the flyback converter.

SISO Tool is a powerful software which supports designer in real-time tuning controllers. It is easy to use with friendly graphic user interface (GUI) and does not require any pre-course training. Being integrated in MATLAB, there is no need to pay any additional cost. Any adjustment done during the design process will be immediately demonstrated on selected graphs with almost no delay. After establishing SISO Tool in MATLAB, by default, two windows pop out as shown by Figs. 3.1 and 3.2: “Control and Estimation Tools Manager” window for setting and tuning tasks, and “SISO Design for SISO Design Task” window for presenting real-time update design results.

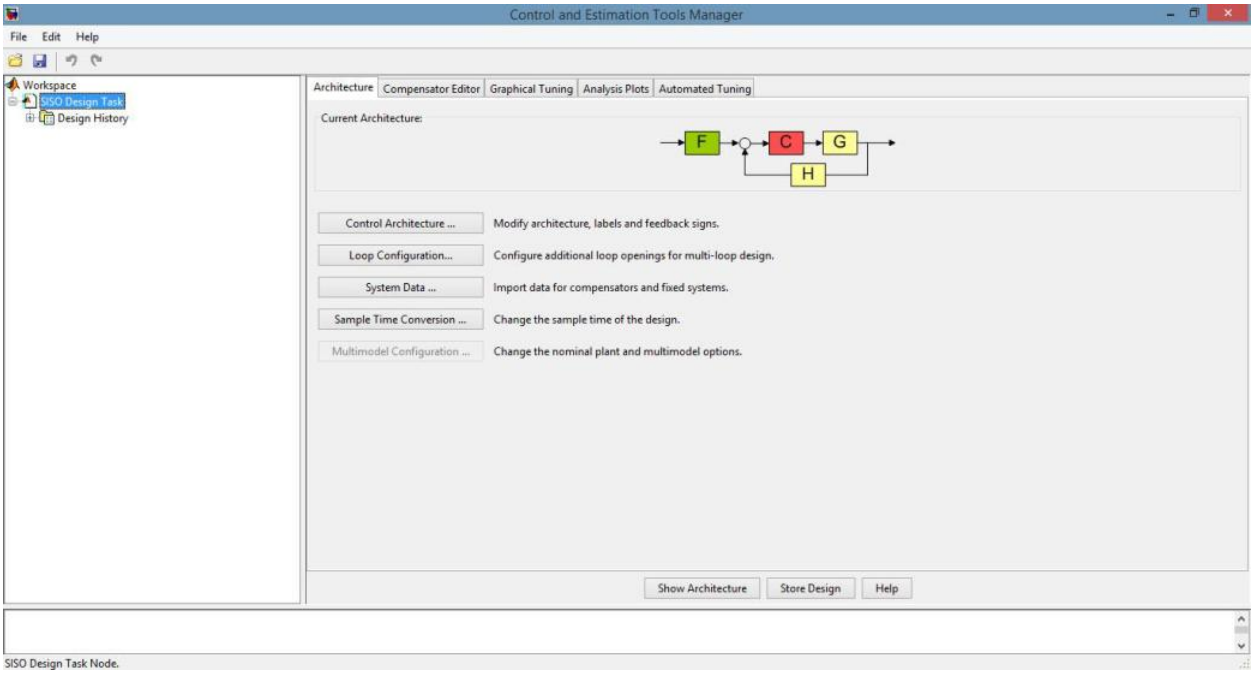


Figure 3.1 - User interface of SISO Tool. A new design can be created or a previous work can be loaded.

In “Control and Estimation Tools Manager” window, under “Architecture” tab, the software provides us with several common controls architecture in “Control Architecture” option. Because there is no special requirement for control architecture, we leave it as default with the most

common form, as shown in Fig. 3.1. The mathematical model for the flyback converter, which was found in the previous section by using numerous MATLAB commands, could be imported here to “G” block by “System Data” option. The work now is to design the compensator “C”, and the feedback gain, if necessary.

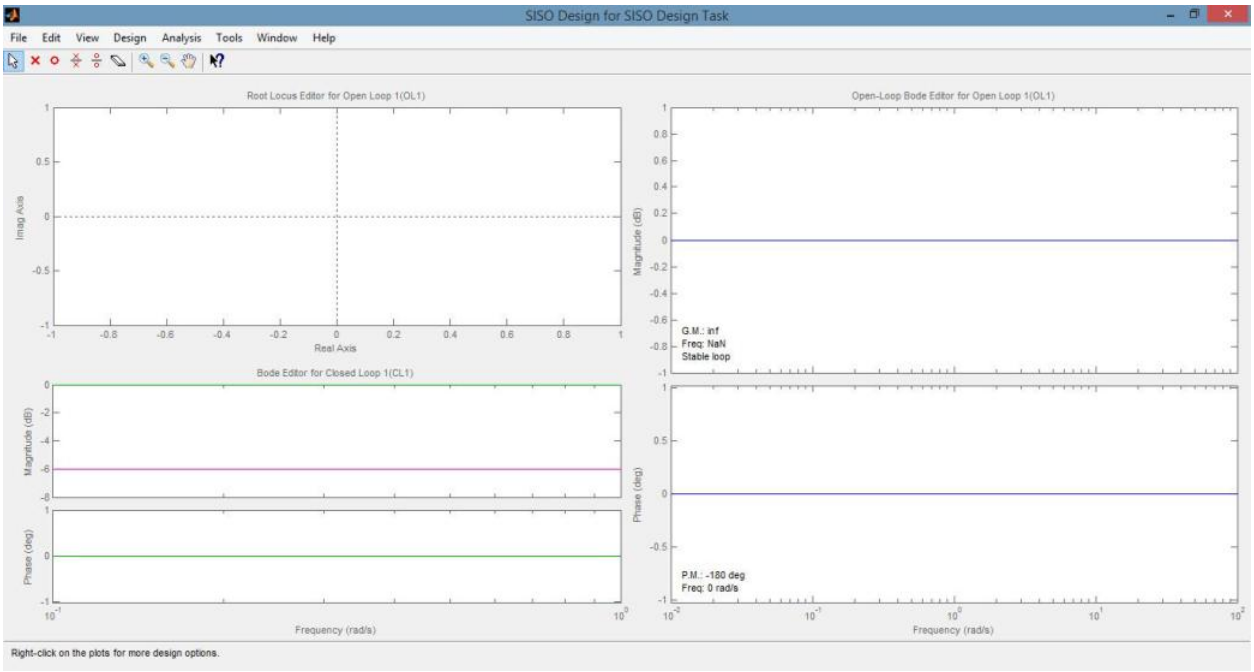


Figure 3.2 - Real-time update designed graphs. Up to 6 graphs can be shown at the same time.

As shown in Fig. 3.2, SISO Tool provides us with several graphs, which includes but is not limited to root locus, Bode plot for closed-loop, and open-loop system. However, we can add up to 6 figures to this window in order to monitor the results of tuning. This task is done by using tab “Graphical Tuning” on the “Control and Estimation Tools Manager” window. From “SISO Design” window, we are able to investigate every change of graphs by relatively adding to the controller either a pole/pair of poles, or a zero/a pair of zeros. These added poles and/or zeros will be immediately updated on the “Control and Estimation Tools Manager” window, under

"Compensator Editor" tab. The position of poles and/or zeros could also be precisely selected here and then compare with the results at "SISO Design" window.

After doing some preliminary calculations, it was found out that by putting two zeros at s_1 = -1250 and s_2 = -22700 on the left-hand plane as shown in Fig. 3.3, all design requirements can be totally satisfied. An input reference of 1.5 and a feedback gain of 0.046875 (1.5/32) were also added in order to achieve the value of 32 VDC as a result of step response. By the time two zeros were added, the system root locus graph was also updated as illustrated in Fig. 3.4.

By adding two zeros as stated above, the transfer function of designed PID controller now is:

$$C(s) = 1795\frac{(1+0.0008s)(1+4.4e-05s)}{s} = 1.51+\frac{1795}{s}+6.3164\times10^{-6}s \tag{3.6}$$

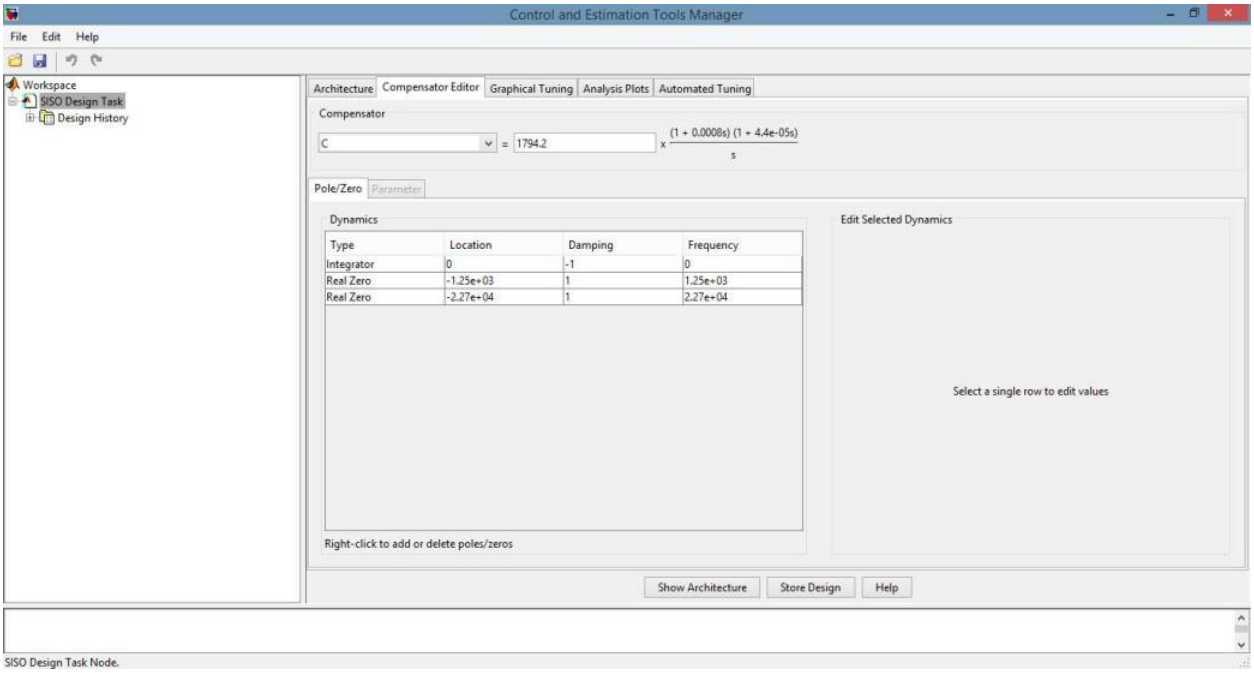


Figure 3.3 - Adding two zeros at -1250 and -22700 to the compensator. SISO Tool also shows the function of equivalent controller.

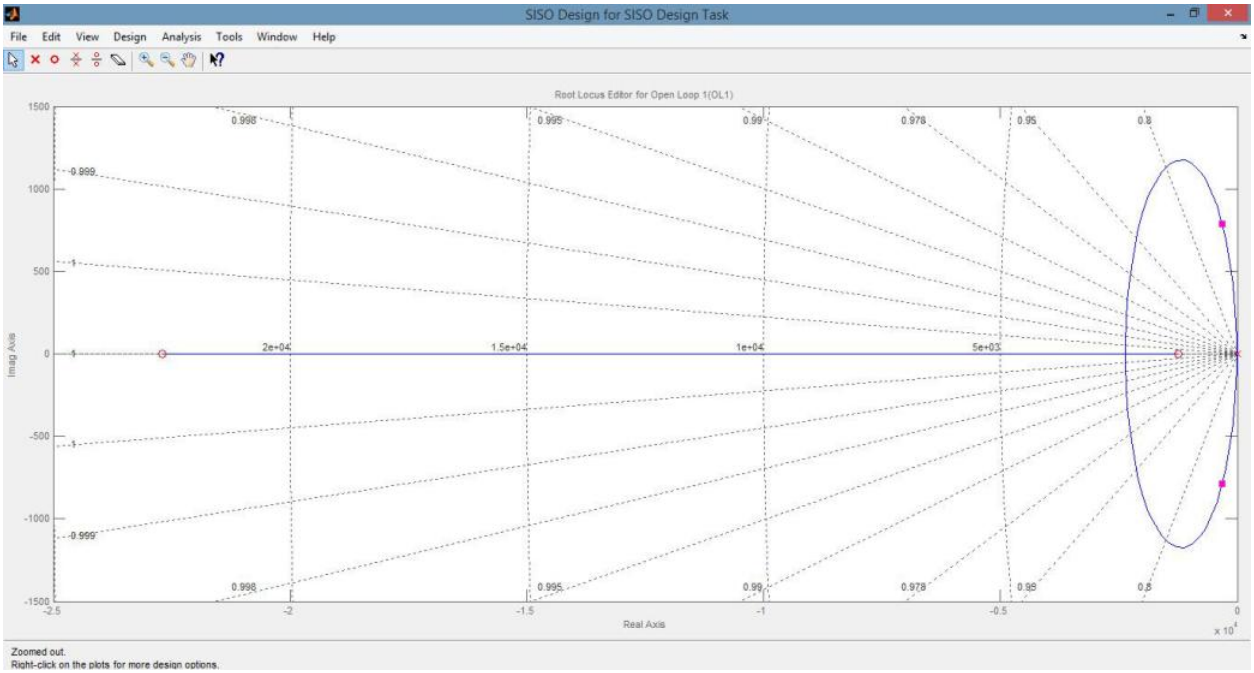


Figure 3.4 - The system's Root Locus graph was updated with two added zeros and one pole (at $s = 0$).

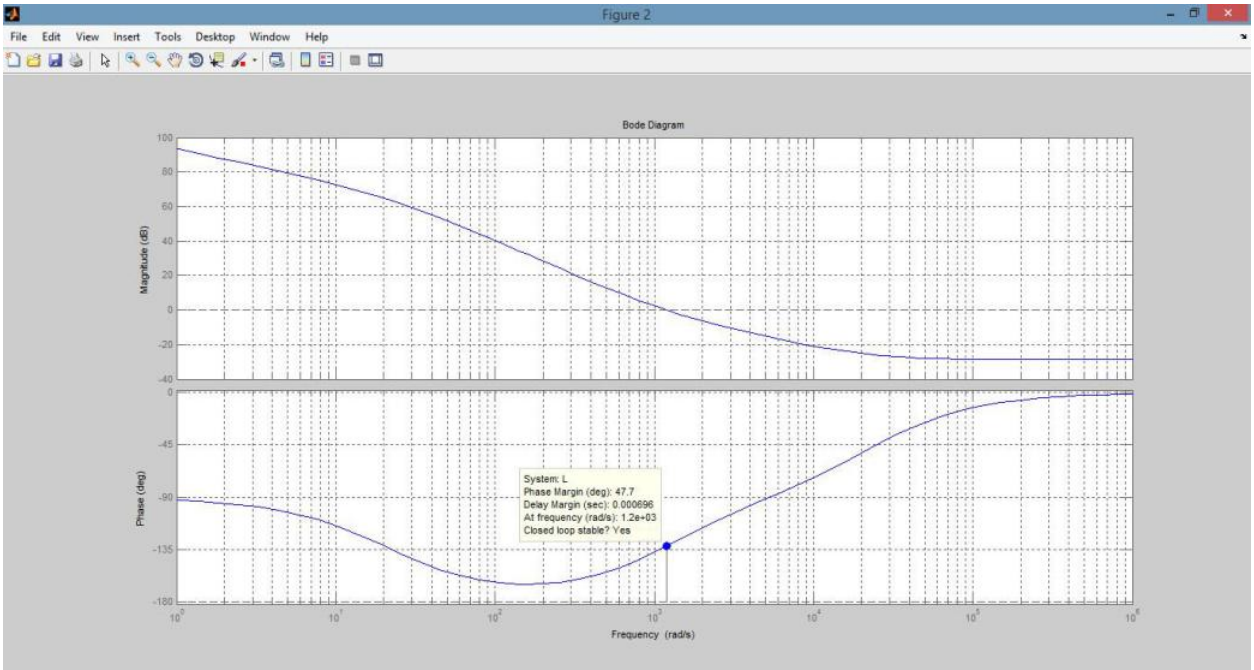


Figure 3.5 - Bode plot of the closed loop system with demonstration of stability. The closed loop system is stable and the phase margin is 47.8º.

With this PID controller, the system's stability is guaranteed with 47.8º phase margin as indicated in Fig. 3.5. This stability feature was investigated one more time by using Nyquist criterion and the same result was achieved since the system's contour does not encircle the (-1, 0) point and the number of pole for loop gain transfer function is zero [15]. Fig. 3.6 illustrates the Nyquist plot for the current system. Fig. 3.7 zoom in (-1, 0) point to show the relative position of (-1, 0) point with the contour. With such a stable system, the step response is shown in Fig. 3.8. The settling time is merely 0.00767 sec while the rising time is more impressive with just less than 0.0001 sec. The output of the model is 32 V as expected.

In order to check the design results, a simulation in Simulink was employed. The PID controller block was built as in Fig. 3.9, and the whole closed loop system was constructed as in Fig. 3.10.

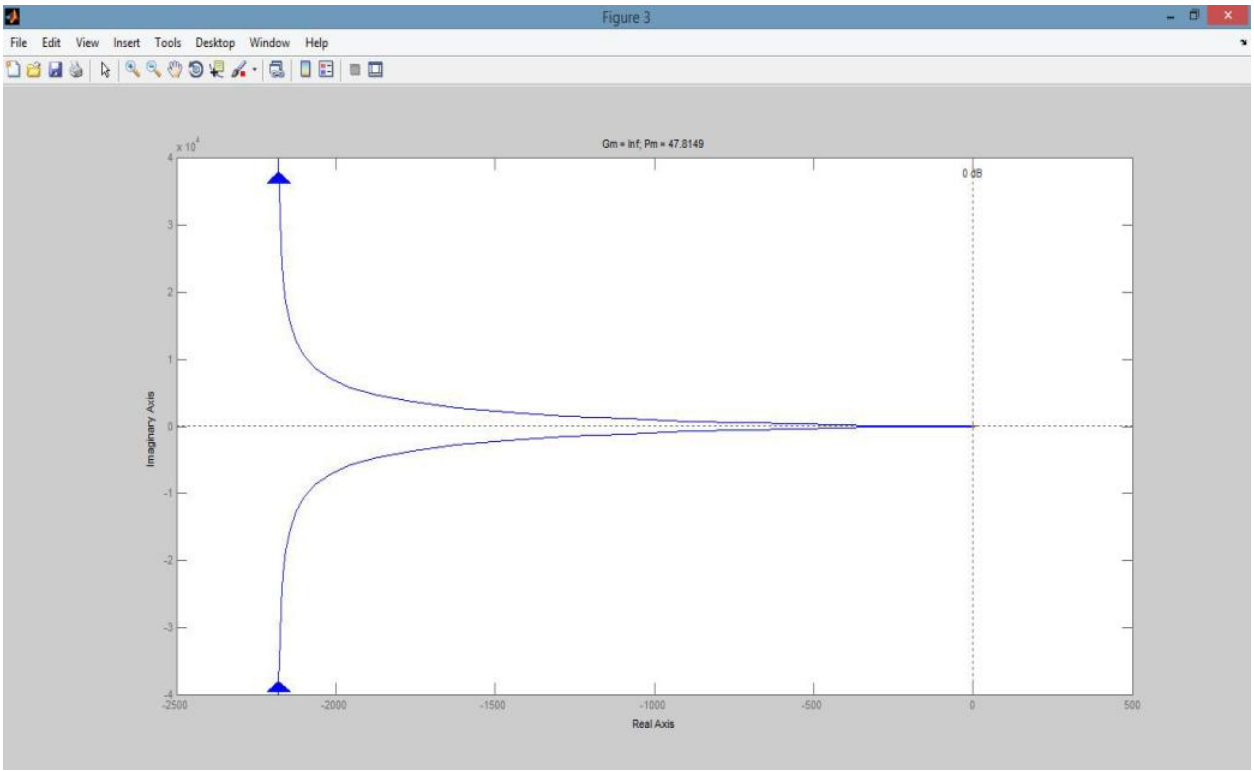


Figure 3.6 - Contour of the system loop gain demonstrated on Nyquist plot. It does not encircle the (-1, 0) point any time, showing us the credit of a stability system.

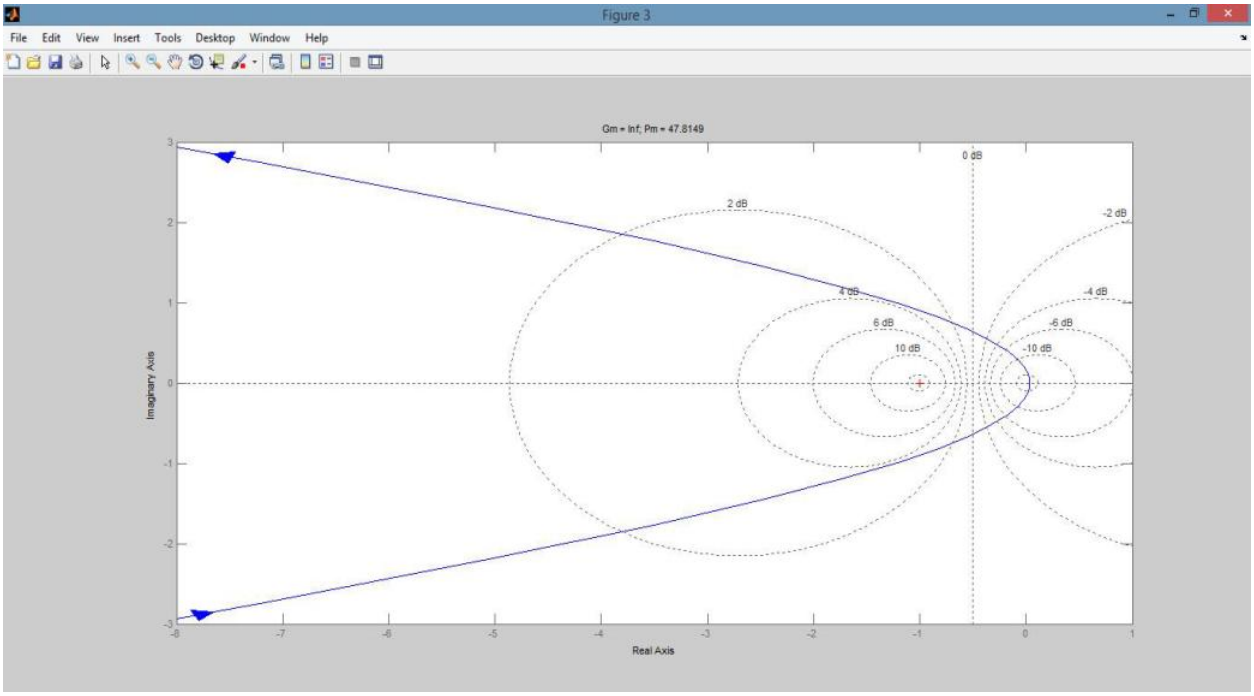


Figure 3.7 - A closer view at the (-1, 0) point.

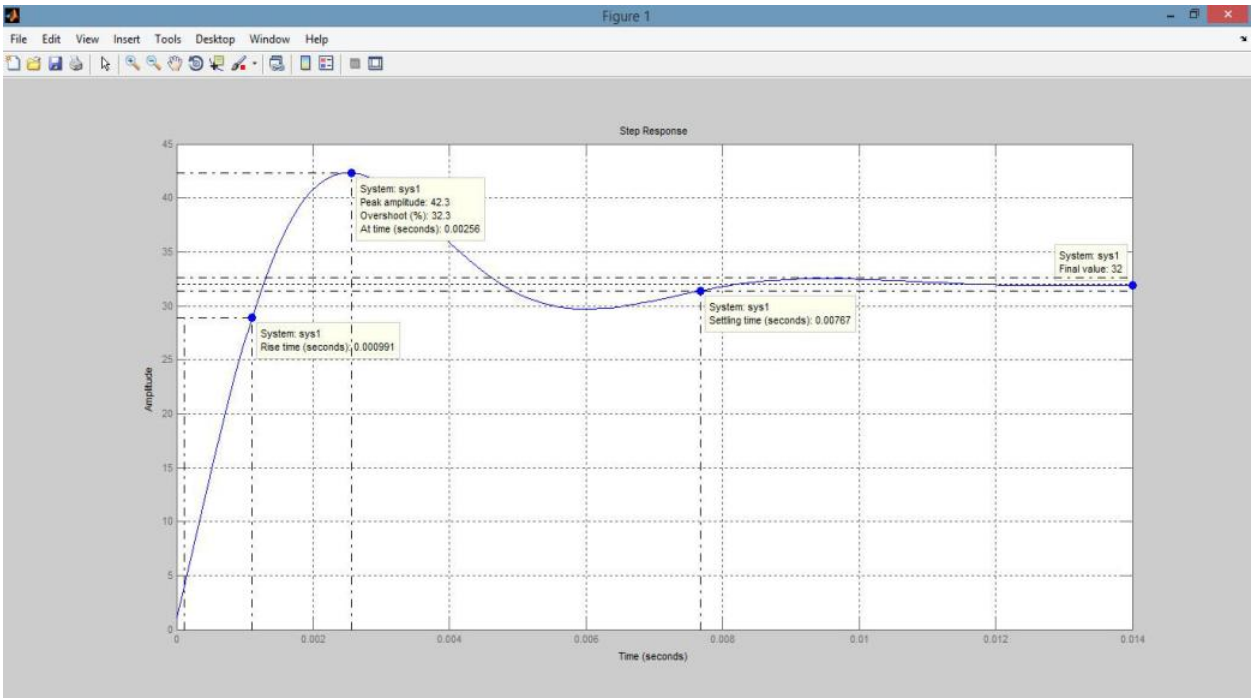


Figure 3.8 - Step response of the controlled system. The Settling Time is 0.00767 sec, The Rise Time is less than 0.0001 sec, and the Steady-State value of system's output is 32 (VDC).

After running the simulation, then comparing the responses of Simulink simulation (Fig. 3.11) with the designed result from SISO Tool (Fig. 3.8), there was almost no difference. Therefore, the designed PID controller is now ready to be implemented in PSpice simulation.

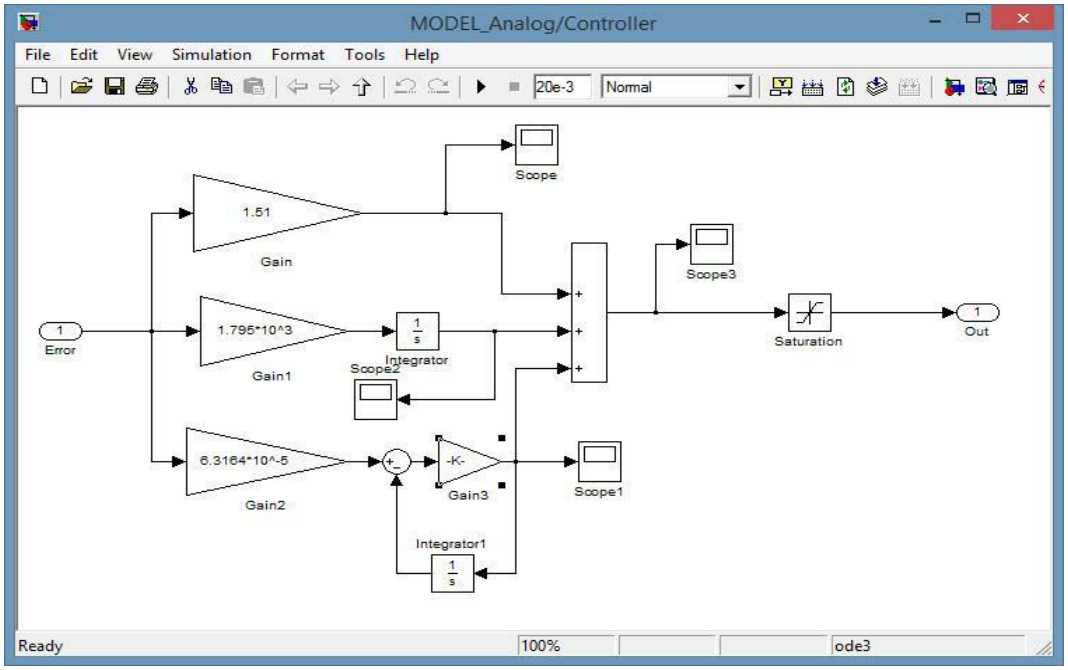


Figure 3.9 - The PID controller in Simulink.

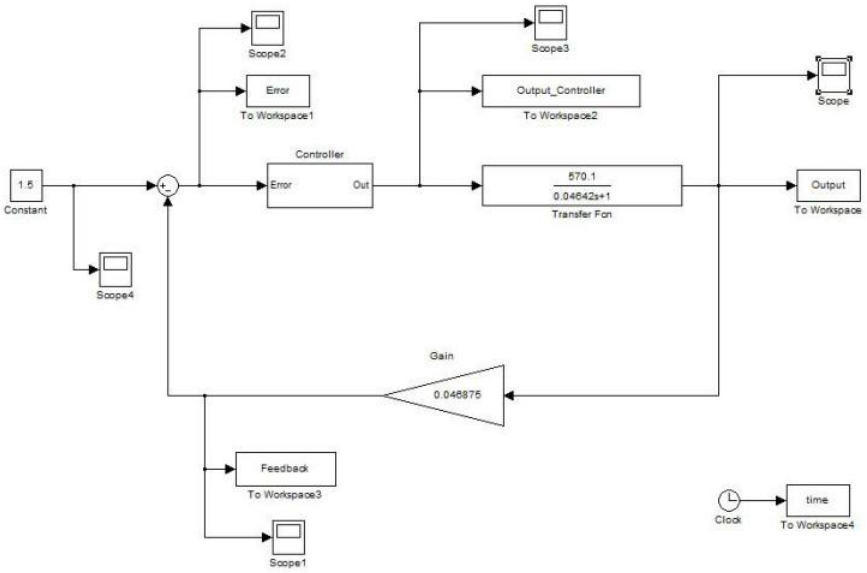


Figure 3.10 - Simulation of the closed loop system in Simulink.

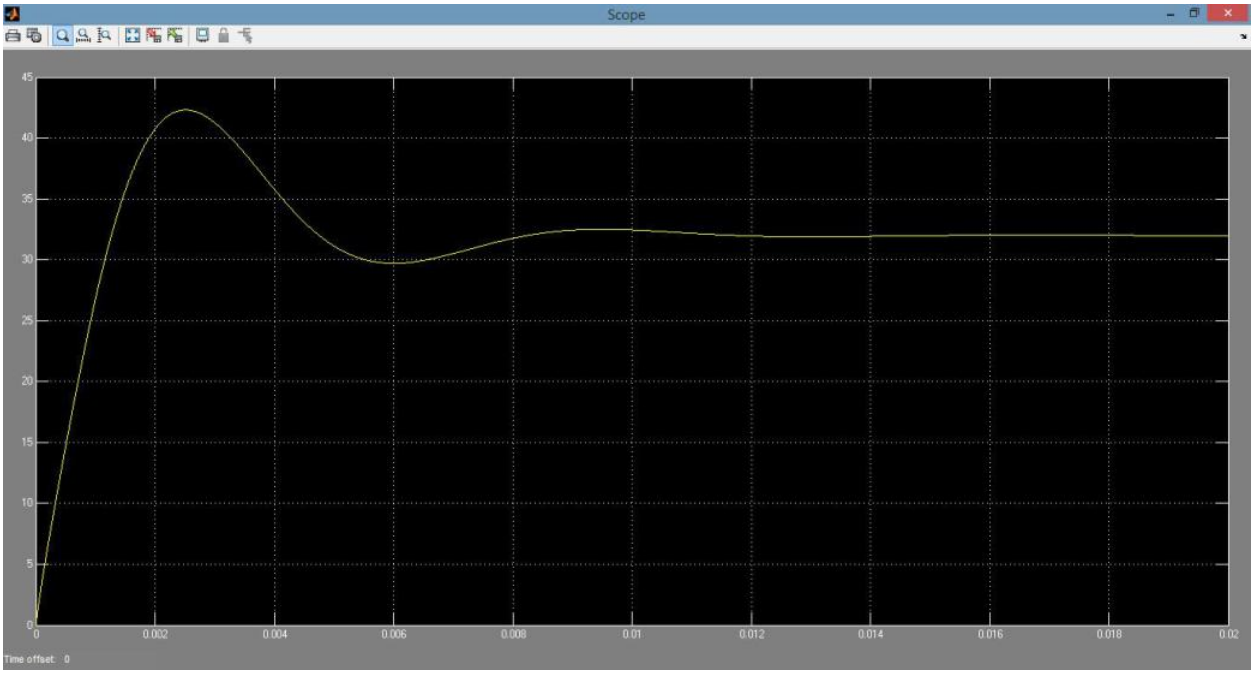


Figure 3.11 - Simulation result from Simulink. This result matched perfectly with the designed result from SISO Tool.

3.5. Simulation with Cadence's PSpice

The next step in the design process is simulating with full converter using Cadence's PSpice software. There are a lot of reasons for choosing PSpice, among them are two highlight features that make this software the most favorite one for many design engineers: (1) providing high reliable results with significantly fast running time, and (2) having a diversified library of component which seamlessly supports designer not only on stage of simulation but also on task of printed circuit board (PCB) design. The PCB design process was also implemented using several parts from Cadence Product Suite, as will be demonstrated in Chapter 4.

The schematic for full converter simulation is shown in Fig. 3.12. It can be divided into four main parts. The first part, which denoted "1" in Fig. 3.12, is the main circuit of the LED driver. It

consists of: a rectified circuit which converts 120 rms-value AC source into a DC source, a snubber circuit with function of reducing voltage stress on transistor due to switching action, a flyback topology, and a peak current detector. The second one, “2” is the PID controller which works essentially as a PI controller since the derivative gain is significantly small compared to the proportional gain and integral gain, and its impact can be neglected. The main purpose of using the third part, “3” is illustrated the function of PWM feature of PIC18F series micro-controller. The fourth part, “4”, named Zero Current Detector, has its function of detecting and calculating the conducting time of the diode on the secondary side. In practice, except the part 1 has its real, physical circuit, the other three parts were implemented by the micro-controller.

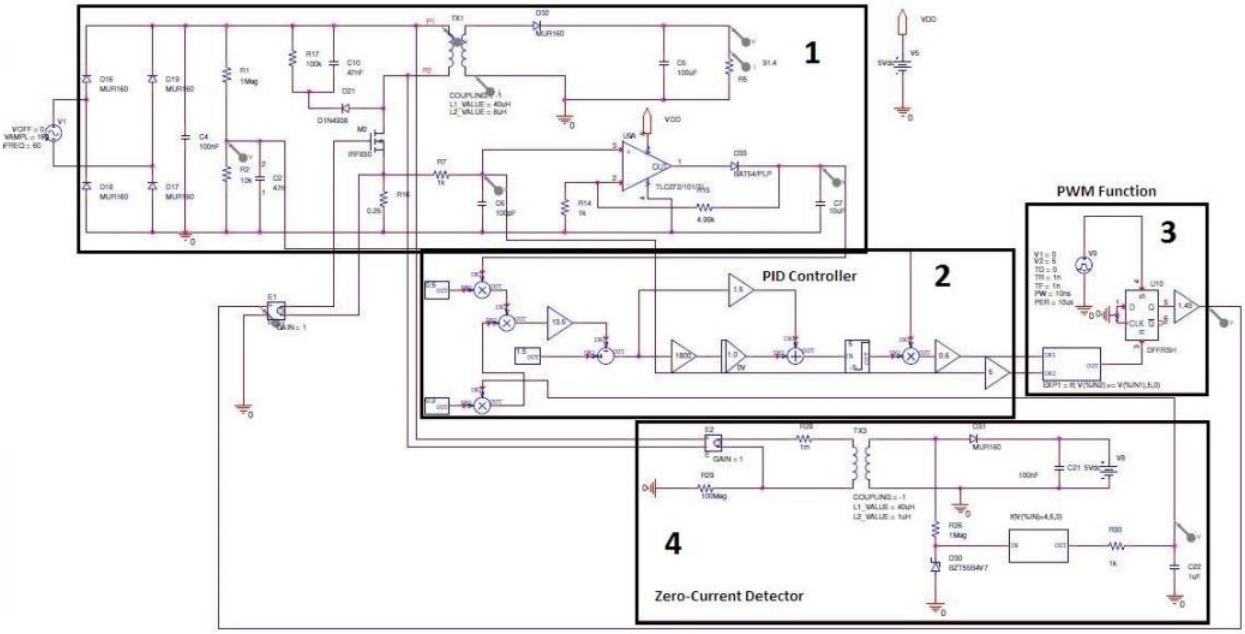


Figure 3.12 - Schematic for full converter simulation in Cadence’s PSpice.

Part “1” will connect directly to the standard household120 rms-value AC source, and then rectifying it to a DC source with its peak value of approximately 170 V. A sample waveform of rectified voltage will be extracted and feed through to the micro-controller for control purpose.

The introduction of the snubber circuit (Fig. 3.13) helps to solve the problem of an excessive voltage might be induced on the switching transistor during turn-off process due to the transformer leakage inductance [16]. It keeps the transient oscillation voltage in safe boundaries, thus lowering the power dissipation of the switching transistor.

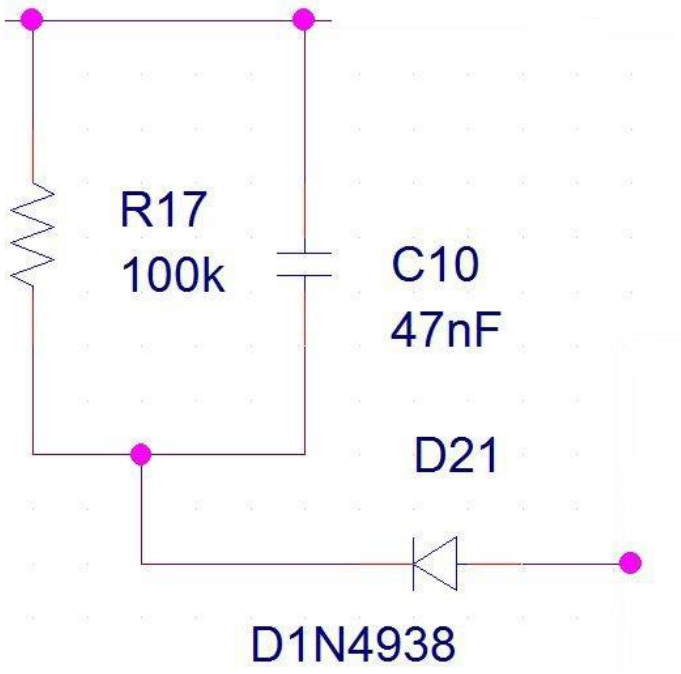


Figure 3.13 - The Snubber Dissipative Circuit.

When the switching transistor is switched off, diode D21 is forward biased. The energy from the transformer's leakage inductance due to inductive kick phenomenon will be discharged to capacitor C10 [17]. Therefore, capacitor C10 should be able to store its initial charged energy plus the energy transferred from transformer inductance. According to [16], the minimum value for C10 can be calculated from:

$$C = \frac{L_L \times I_{p\max}^2}{\Delta V_C \left(\Delta V_C + 2V \right)} \tag{3.7}$$

where L_L is the leakage inductance of the transformer. With the intended EFD-20 transformer, from its datasheet: $L_L = 4 \times 0.24 = 0.96$ μH. ΔV_C is the acceptable change of voltage across capacitor C10, that has range from 40 V to 60 V. We can choose a value of 50 V for this calculation. V is the secondary side voltage reflected to the primary side, which is calculated as N (= N_P/N_S) times of forward biased voltage of the secondary side diode (choose the value of 0.8 V) and the output voltage (32 V). Thus, V = 2.23×(32 + 0.8) = 73.14 V.

The minimum value for capacitor C10 of the snubber circuit is:

$$C = \frac{0.96 \times 10^{-6} \times 3.5^2}{50\left(50 + 2 \times 73.14\right)} \approx 1.2 \times 10^{-9} = 1.2 \text{ nF} \tag{3.8}$$

The value for resistor R17 should be chosen so that the time constant of R17-C10 circuit is much larger than the switching period (1/100 kHz = 10^{-5} s). In addition, this resistor should be able to dissipate the total transferred energy from transformer's leakage inductance as well as stored energy in capacitor C10. Also according to [16], the formula to calculate power for this resistor is:

$$P_R = \frac{L_L \times I_{p\max}^2 \times f}{2} + \frac{V^2}{R} \tag{3.9}$$

The value of C10 and R17 are tested and adjusted, if necessary, in order to minimize their impacts on the transient response. Finally, with C10 = 47 nF and R17 = 100 kΩ all the required specifications are justified. The circuit's time constant is $(47 \times 10^{-9}) \times (100 \times 10^3) = 470 \times 10^{-5}$ s, which is much larger than the switching period of 10^{-5} s. The minimum dissipative power for resistor R17 is calculated as:

$$P_R = \frac{L_L \times I_{p\max}^2 \times f}{2} + \frac{V^2}{R} = \frac{0.96\times10^{-6}\times3.5^2\times10^5}{2} + \frac{73.14^2}{10^5} = 0.641\ \text{W} \qquad (3.10)$$

The intention of using the primary-side sensing and control is attained by using a peak-current-detector circuit for obtaining secondary side's peak current with no device connected to the secondary side at all. The peak current detector, which is shown in Fig. 3.14, receives the waveform of switching current to its port 3 and outputs the maximum value of the primary side current. This value is just the value of maximum secondary side current referred to the primary side. The actual secondary side's current is proportional to the primary side's quantity by a factor of N_p/N_s – the turn ratio of transformer [18]. This peak value, along with the waveform of the primary side current will be delivered to the micro-controller to calculate and compare. In simulation, the peak current value is a factor of feedback signal calculation process while the waveform of the primary side current will be compared with the calculated quantity in order to control the PWM mechanism.

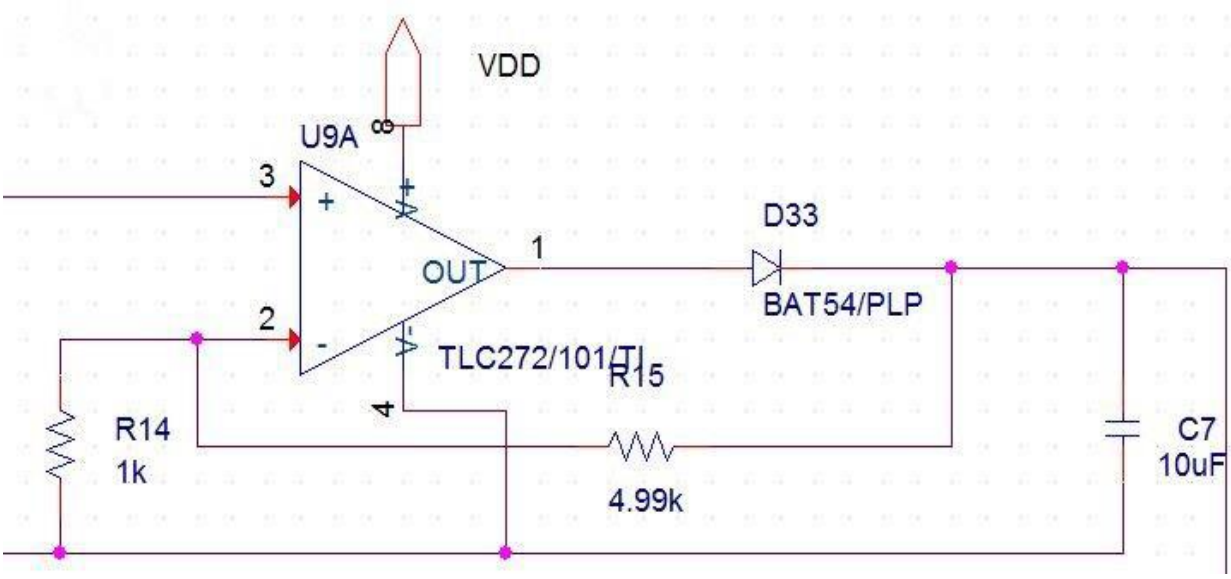


Figure 3.14 - The Peak Current Detector, a mechanism of primary side sensing for detecting the peak current of secondary side circuit without any contact.

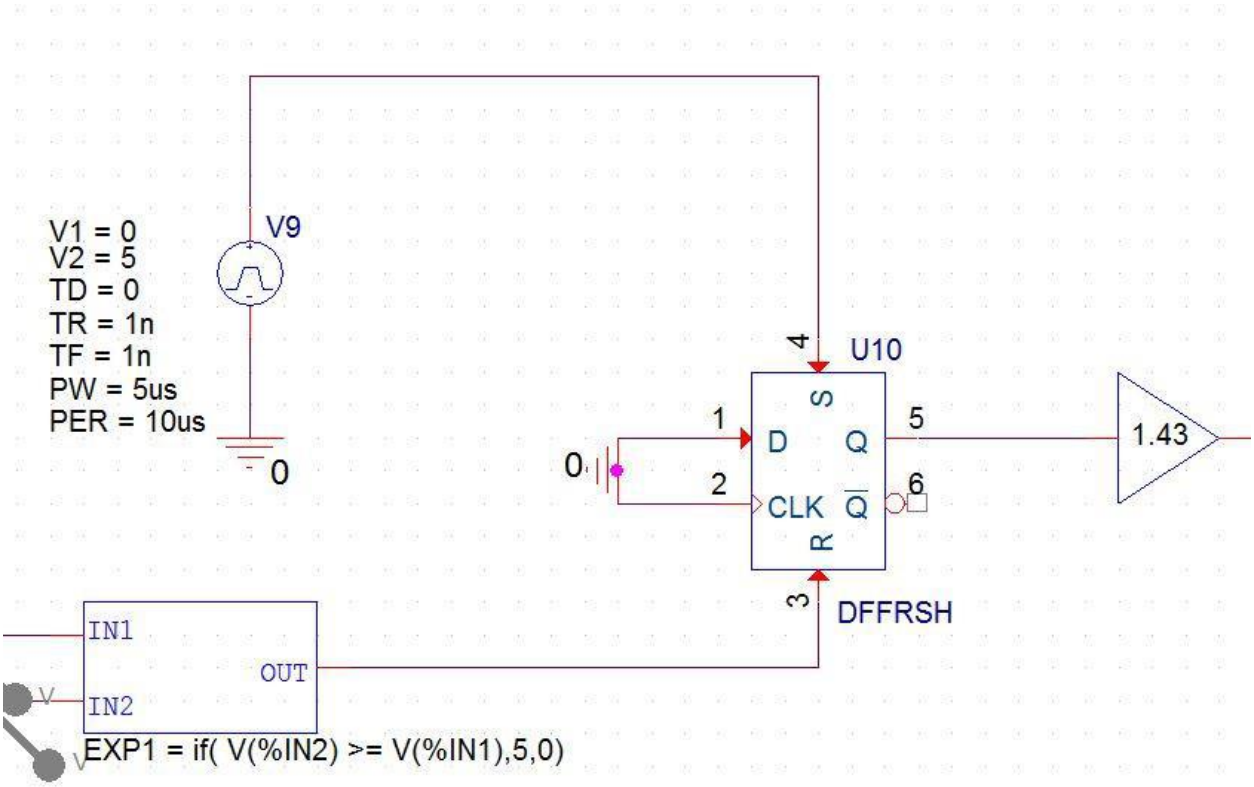


Figure 3.15 - Demonstrating the PWM mechanism in the micro-controller based LED driver simulation.

Part 3 illustrates the PWM mechanism of providing the driving signal for switching transistor M2. The post-processed signal from PID controller (IN1), which is chosen as the reference signal, will be compared with signal that represents the primary-side current which flows through the switching transistor (IN2) as shown in Fig. 3.15. If IN2 signal is greater than or equal to IN1 signal, a logic "1" will be send to "R" port on S-R latch. It means that the output of the latch will be forced to low, Q = 0 and the switching transistor M2 is OFF. The S-R latch's output will stay low as long as IN1 signal is smaller than IN2 signal. When IN2 signal is smaller than IN1 signal, a logic "0" exists at "R" port and the output of the S-R latch will be forced high, making the switching transistor to be conducted. Because the output of the S-R latch is just about 3.5 V, a

gain block of 1.43 was used to achieve 5V value to the gate of M2 as shown in Fig. 3.15. Those sequences of action describe exactly the PWM mechanism of PIC18F micro-controller, which will be implemented through programming with algorithm as in Fig. 3.16. In this simulation, ABM (analog behavioral modelling) blocks are used to demonstrate these operations. As will be shown later, ABM blocks will also be employed in parts 2 and 4 which function as the zero current detector as well as to transfer the model of PID controller from Matlab-Simulink to PSpice.

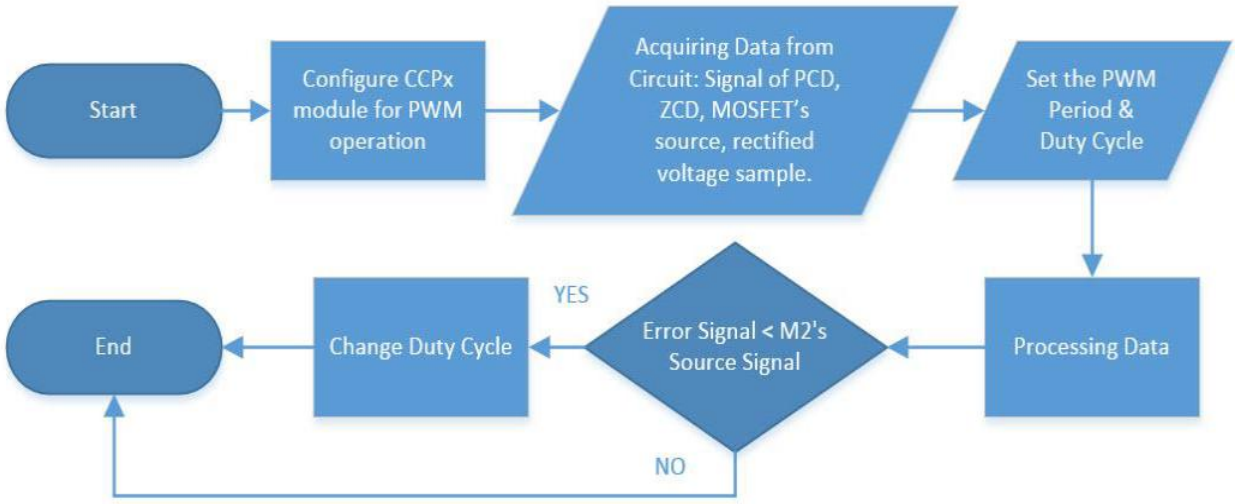


Figure 3.16 - Flowchart of PIC18F based LED driver's algorithm.

The zero current detector (Fig. 3.17) is actually a virtual circuit whose function is to monitor and calculate the conducting period of the secondary side's diode. The main advantage of the "primary-side sensing" circuit, is the absence of optocoupler, which makes it a more stable sensing circuit. In application, a multi-winding transformer is required. Therefore, along with primary and secondary windings, the third winding's voltage can be used to detect the conducting operation of the secondary side's diode. In Cadence's PSpice, however, there is no

model for multi-winding transformer [19]. Despite the fact that we can design and then use a new 3-winding transformer model, it is more convenient to use an auxiliary transformer instead. Two terminals of the main transformer's primary winding will be connected to another transformer, and a similar-secondary-side circuit will be constructed in order to investigate the secondary side's diode conducting operation. Using a voltage divider which was constructed by a resistor in series with a Zener diode, the status of the secondary side's diode can be obtained through the voltage level of Zener's cathode. After several times of running and measuring, the threshold value of voltage level of Zener's cathode at which the conducting state of secondary side's diode reversed is found to be 4 V. An ABM block with "one input, V out" was used to do that logic expression. Whenever the voltage at Zener's cathode (reflects the anode voltage at the secondary side's diode) is greater than or equal to 4V (i.e., anode voltage of the secondary side's diode is greater than 5 V), the output of the conditional ABM block is 5 V. It means that the secondary side's diode starts to conduct. Meanwhile, the dropping of voltage at Zener's cathode below the threshold of 4 V is the sign that conducting activity of the secondary side's diode is halted. The output signal from ABM block will be fed through a low-pass filter and then contributed to the calculation of output, which was used as feedback signal for PID controller. In application, all is needed to do is just monitoring the voltage of Zener's cathode (which reflects the voltage of the auxiliary winding) and using a counter of micro-controller to achieve the conducting time of the secondary side's diode.

As stated above, the derivative gain value is just $K_D = 6.3164\times10^{-5}$ which is less than 0.01 percent of either the proportional gain $K_P = 1.51$ or the integral gain $K_I = 1795$. Thus, its effect was just minuscule. In practice, the derivative gain should be as small as possible to mitigate the effects of noise. Hence, the designed PID controller (in reality, a PI controller) from Matlab-

Simulink was transferred to Cadence's PSpice in a form of PI controller using ABM blocks as shown in Fig. 3.18. This PI controller has a reference input 1.5 as in SISO Tool/Simulink design and the feedback signal is the combination of the peak current detector and the zero current detector's outputs. The specific formula of this feedback signal is [20]:

$$I_{avg,p} = \frac{1}{2} I_{p\max} \frac{t_{on\_s}}{T} \tag{3.11}$$

in which $I_{p\max}$ is obtained from the peak current detector, and the ratio between the secondary side's diode "on" time t_{on_s} and the switching period T is obtained from the zero current detector.

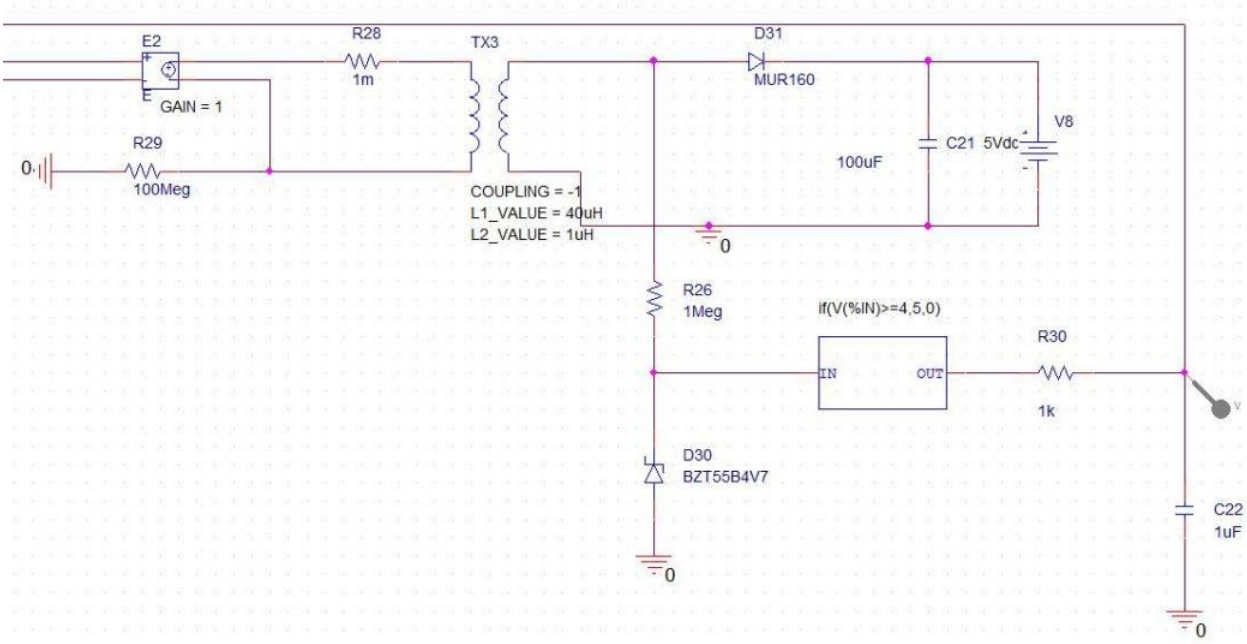


Figure 3.17 - Visualizing the Zero Current Detector by employing ABM blocks.

The output of PID controller will be multiplied with the sampled waveform of rectified voltage to make the reference signal for PWM mechanism. The signal to be compared is the switching current measured at the gate of MOSFET M2, which is converted to voltage by a 0.25Ω resistor. The flowchart of receiving, combining, processing, and comparing is illustrated in Fig. 3.19.

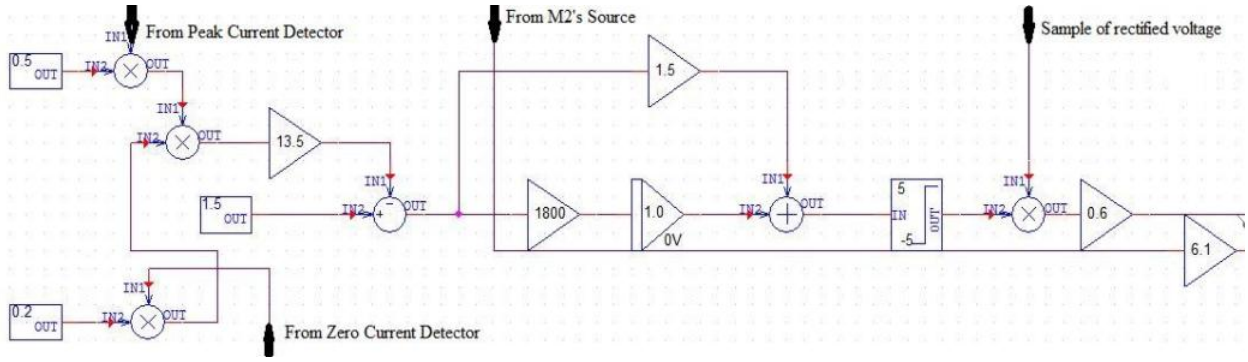


Figure 3.18 – PID controller in PSpice.

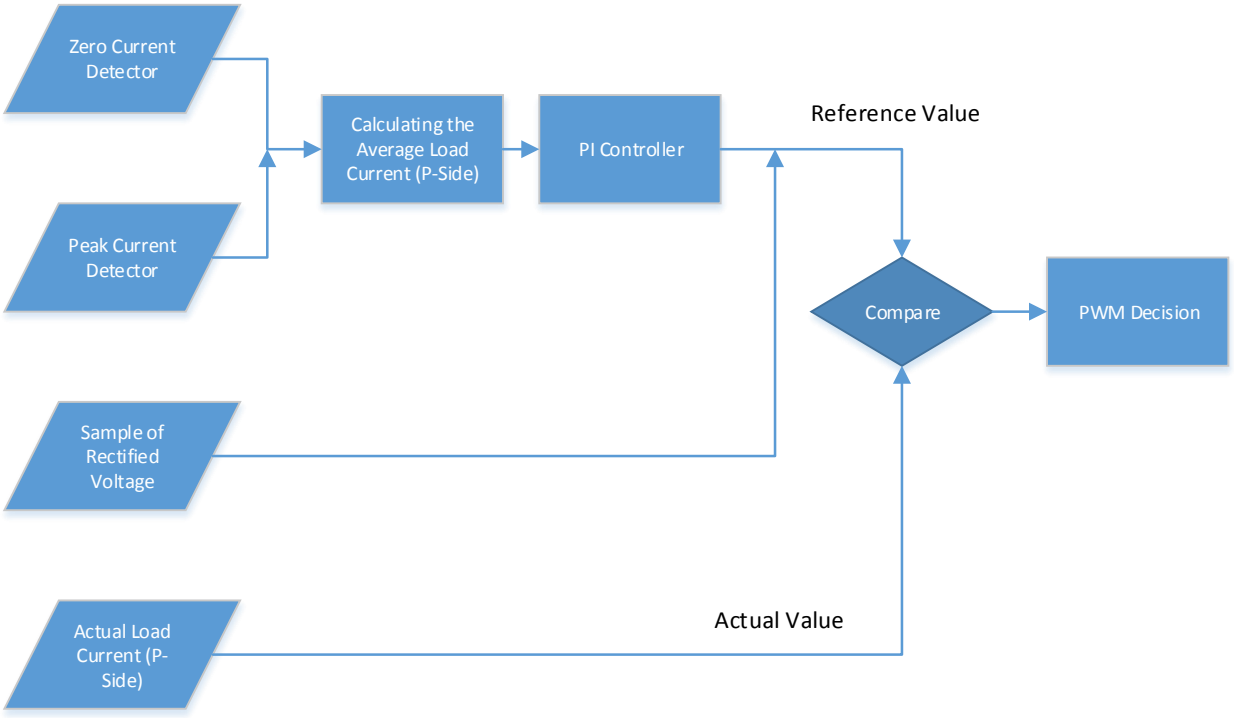


Figure 3.19 – Flowchart of control PWM mechanism in PSpice simulation.

3.6 Simulation results

After setting the simulation profile, the simulation was run several times so all the results were investigated carefully. Fig. 3.20 shows the input and output signals of the zero current detector.

The threshold voltage at which the output is high is 4V. Fig. 3.21 demonstrates the PWM mechanism which will be implemented by the micro-controller. The signal from PID (black line), which is chosen as the reference will be compared with MOSFET M2's source signal (solid purple) in order to generate PWM signal (solid pink), which will be fed to a PWM latch for full simulation of the PWM mechanism. As can be seen from Fig. 3.21, the PWM signal exists whenever the MOSFET M2's signal is at least equal to the reference. Fig. 3.22 shows the voltage at the gate of M2, the output voltage and the output current through the LED load. The average output voltage on LED load is approximately 32V while the average output current is approximately 350 mA. Under the operating of PWM mechanism, the gate voltage of M2 is 5V at intervals that correspond to the existing interval of PWM signal.

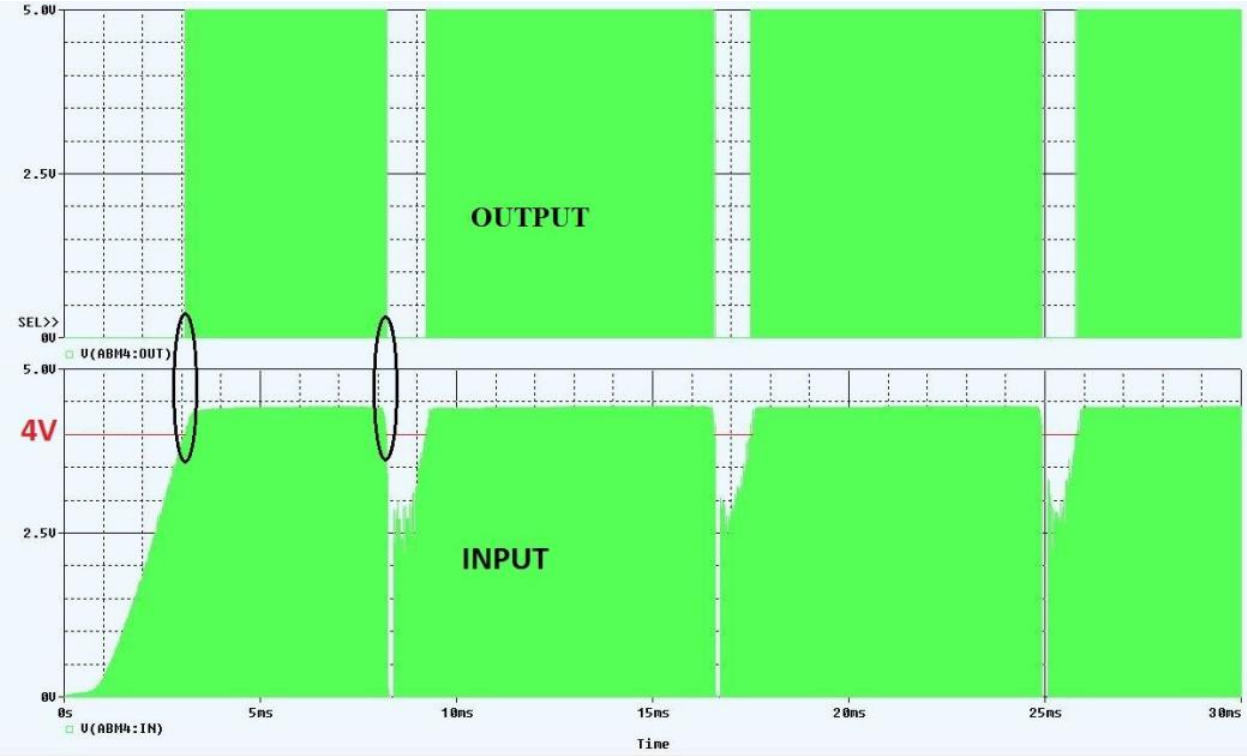


Figure 3.20 – Input and output signal of the zero current detector.

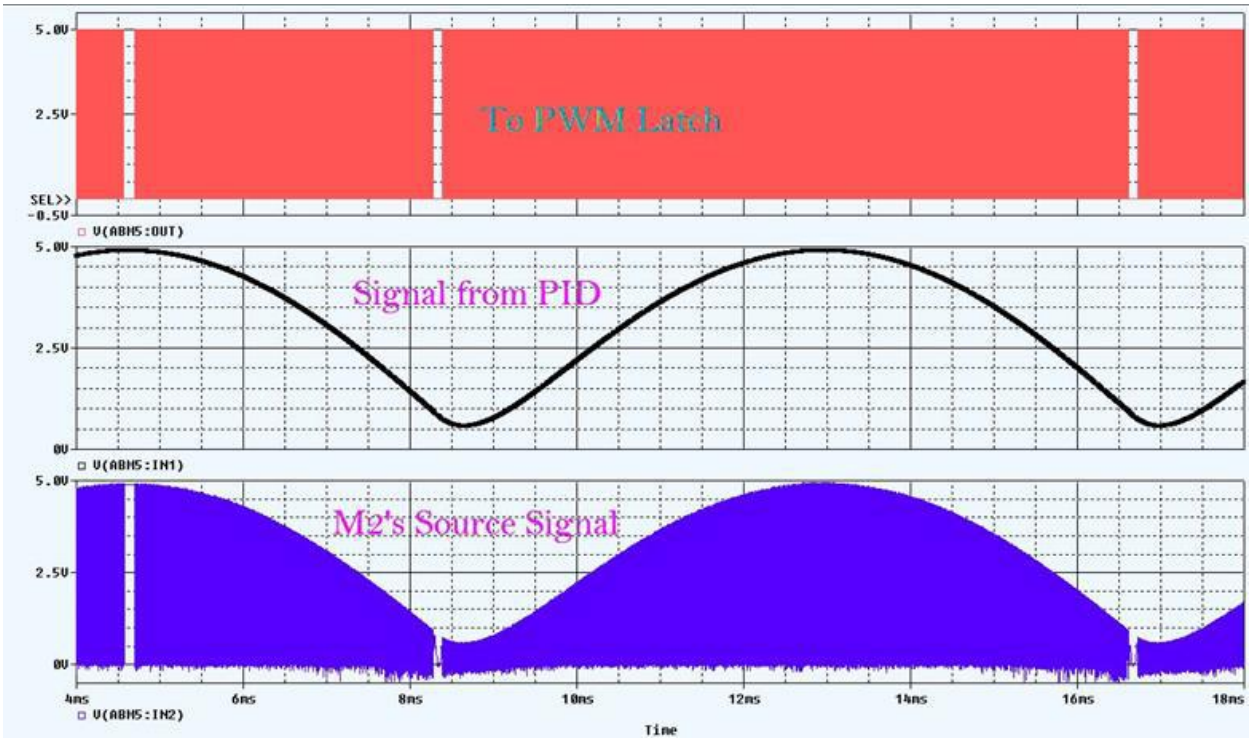


Figure 3.21 – Illustrating of PWM mechanism: comparing signal from PID to MOSFET M2's source signal and generating of PWM signal.

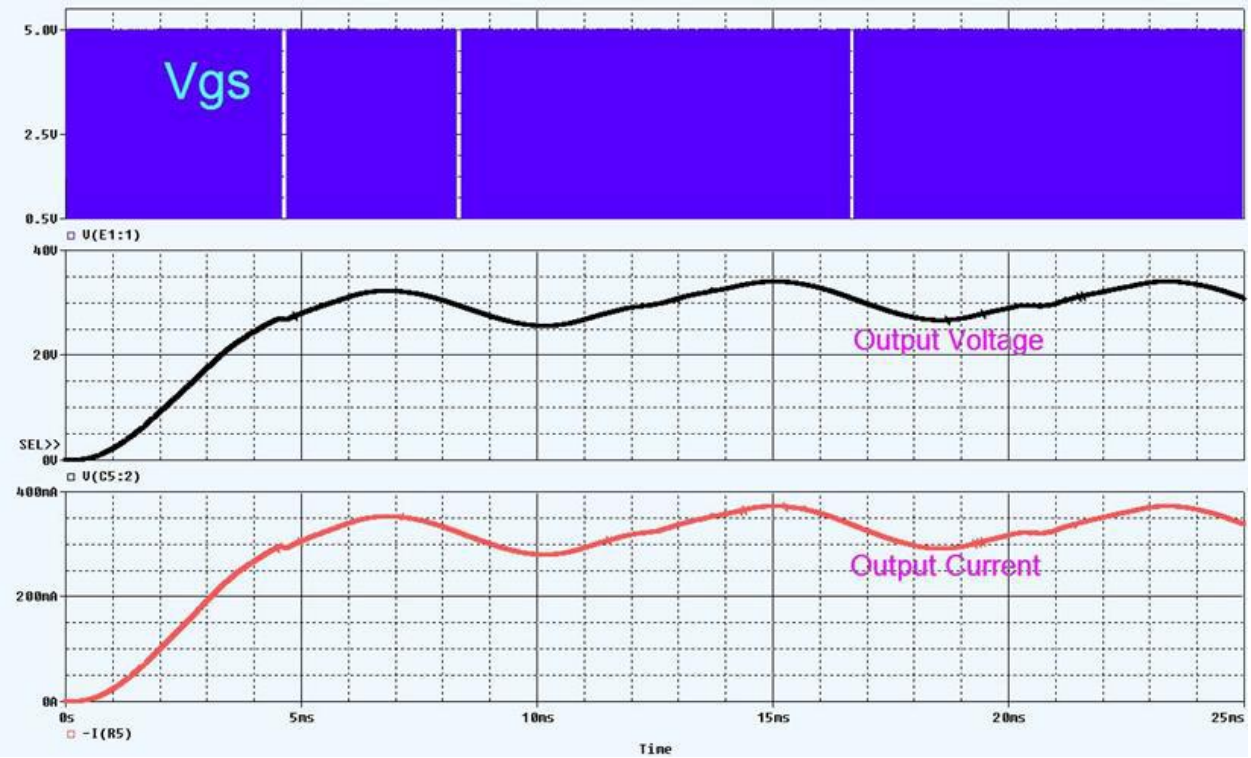


Figure 3.22 – Voltage at the gate of MOSFET M2 under PWM operation (solid), the output voltage (black), and the output current (red).

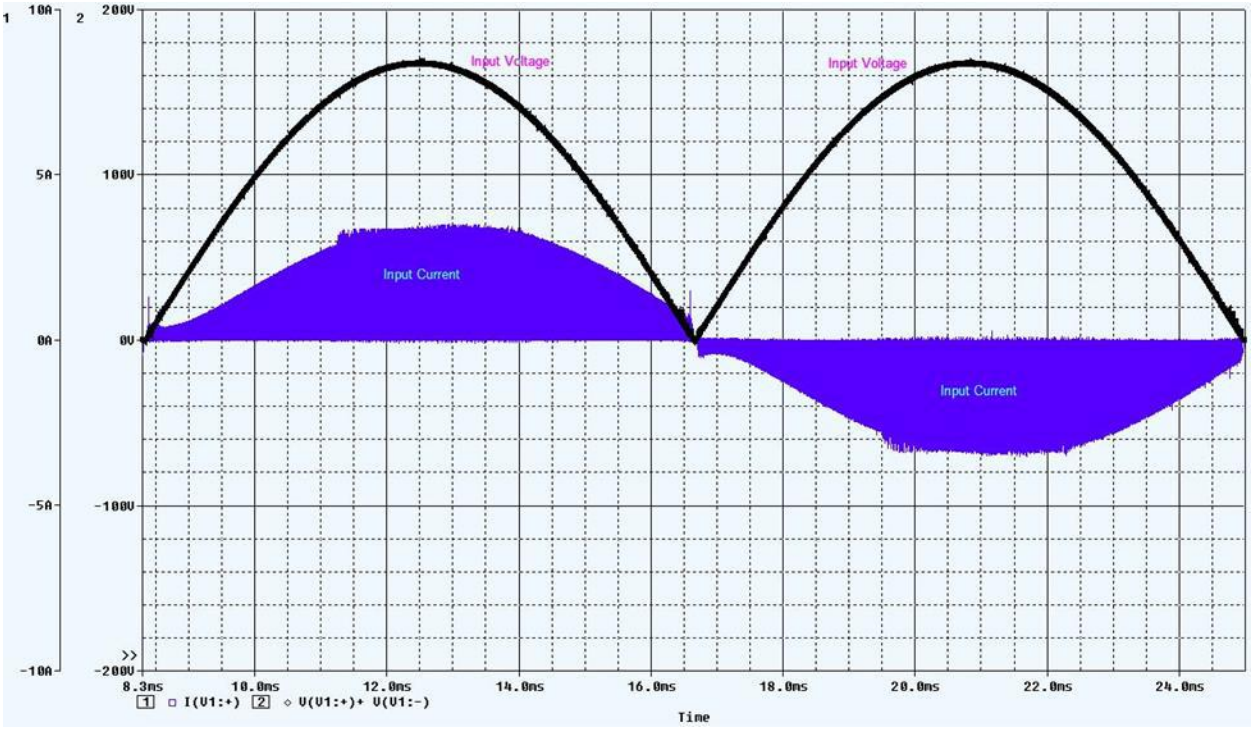


Figure 3.23 – Input Voltage and Input Current (Solid).

Fig. 3.23 shows the input voltage and input current of the converter. As can be seen, the very slight out of phase between the input voltage and input current demonstrates a very high power factor as expected from a flyback converter operating in the discontinuous current mode (DCM).

From the above figures, the simulation results closely matched the results of the intended design. The input peak current is about 3.5 A, the same value as obtained from theory-based calculations in Chapter 2. Meanwhile, Fig. 3.23 is also a useful source to estimate the power factor qualitatively. The input voltage leads the input current by approximately 0.4 ms. The 60Hz source has its full cycle of 1/60 = 16.6 ms, which is equivalent to 2π, or 360º. Thus, 0.4 ms corresponds to 0.4*360/16.6 ≈ 8.67º. Therefore, the lagging angle between the input current and the input voltage is 8.67º. By definition, the power factor of this circuit is cos(8.67º) = 0.988. This value is significantly high when compared to the ideal case since the theoretical flyback

converter is among the most favorite choice for its ability of self-power factor correction under discontinuous current mode of operation [21]. The achieved result demonstrated the nearly-perfect relationship between the input voltage and the input current of a flyback converter as mentioned in Chapter 2.

From Fig. 3.22, the average value of output voltage is approximately 32 V, and the average load current is about 350 mA. These values matched with the design expectations, and are evidence for how well the designed PID controller is. In addition, Fig. 3.22 also illustrates the conducting and non-conducting intervals of MOSFET M2. It was continuously switched ON when V_{gs} has switching pulses while being switched OFF at moments where no V_{gs} pulse exists. The existence of V_{gs} pulse contributed to the operation of PWM mechanism which is explained in Fig. 3.12. It clearly shows how signals were compared and then the PWM signal was generated.

3.7 Conclusion

By simulation and comparing the obtained results with the expected design specifications, all necessary functions of PIC18F micro-controller series for the flyback converter LED driver were examined. The design process, which was done by using both SISO Tool of Matlab and Simulink, was successful. Its design product, which was then delicately transferred to PSpice by making use of the built-in ABM blocks for full converter simulation, worked perfectly. For these reasons, the design process of this micro-controller based LED driver can proceed before the hardware implementation.

Chapter 4

Hardware Implementation

4.1 Overview

With the achieved simulation results matched well with theoretical calculations, the design process can now step up to the hardware implementation stage. There are two tasks that needed to be done: (1) Design a printed-circuit board (PCB) for the driver, and (2) Programming for the PIC18F4550 micro-controller.

Before starting a PCB design, the inventory for available components should first be checked. The top priority on selecting a component is to guarantee the system performance. It means that components must be able to provide the same technical parameters as expected. Then, the component's footprint should be as small as possible so that the board size can be reasonable. The board size is not just a cost-saving problem, it is also relevant to aesthetic consideration. For example: Apple Inc. revamped their powerhouse product MacPro in 2012 by a surprisingly way: breaking the motherboard into 3 pieces so every space inside the case is completely exploited. It results in a significant small yet beautiful workstation with extreme power, which attracts a lot of consumer's attention for its unique design [22]. In the current project, the board size plays a very important role in mission of price reducing. There are two ways to optimize the PCB size: (1)

Deploying components on both sides of the PCB, and (2) Replacing through-hole devices (THD) parts by surface-mount devices (SMD), which normally have smaller land pattern. However, the current project at first mainly concentrates on circuit performance and the easiness of implementation a demo board, so that problems relevant to board size optimizing and aesthetic consideration are temporarily ignored.

The PCB design process can be summarized as a workflow in Fig. 4.1. The details about "Checking Components" and "Preparing Footprint" stages are illustrated in Fig. 4.2 [23]-[24].

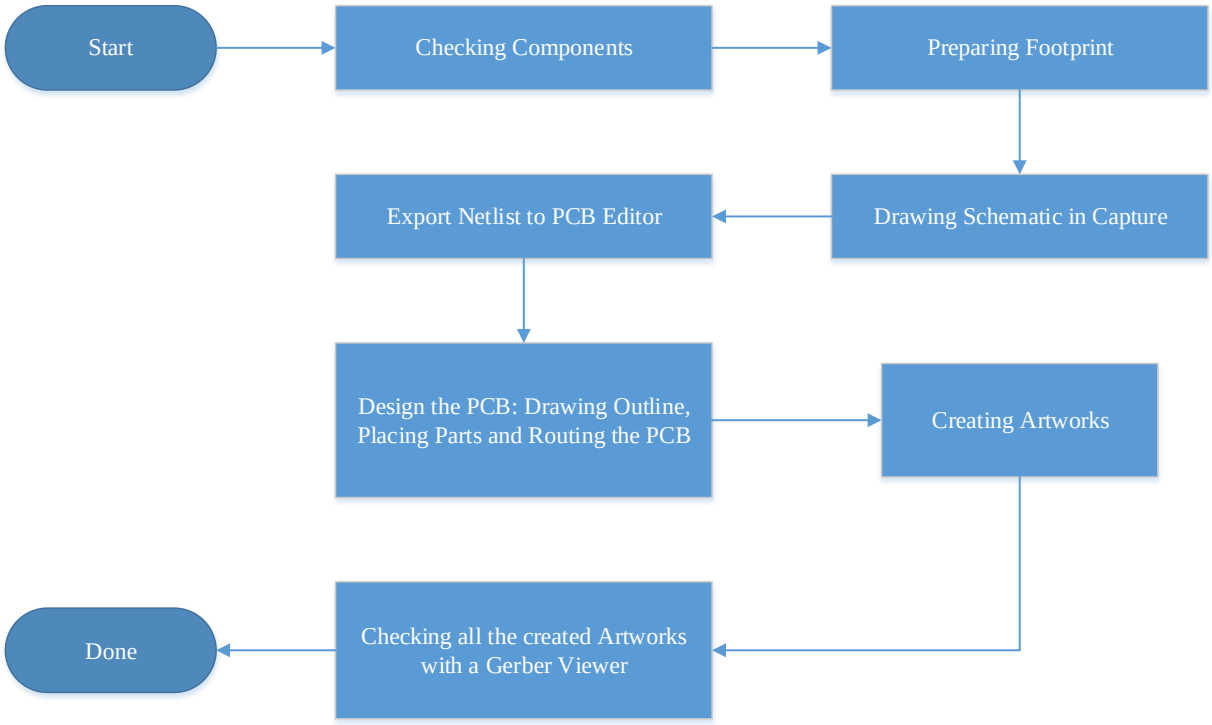


Figure 4.1 – PCB design process with OrCAD CIS Capture and OrCAD PCB Editor Lite Version [25].

The programming task for PIC18F4550 micro-controller was first executed in MPLAB X, then the resulted HEX file would be loaded into memory using a PicKit3 Programmer. There are two ways to connect the micro-controller to the PicKit3 Programmer. The first method uses

breadboard as a mediate environment to connect the micro-controller with the programmer. This method is easy to implement, however, it requires additional components (breadboard, power source for the micro-controller, wires etc.) and the micro-controller must be detached from PCB whenever to be re-programmed. The other way is designing a programmer socket right on PCB. It will make the PCB surface to be more complicated since the programmer needs at least 5 pins to connect. It is not necessary to provide power source since we can supply energy to the micro-controller directly from the PCB. However, a protection must be equipped in order to avoid unwanted phenomena during code-loading process.

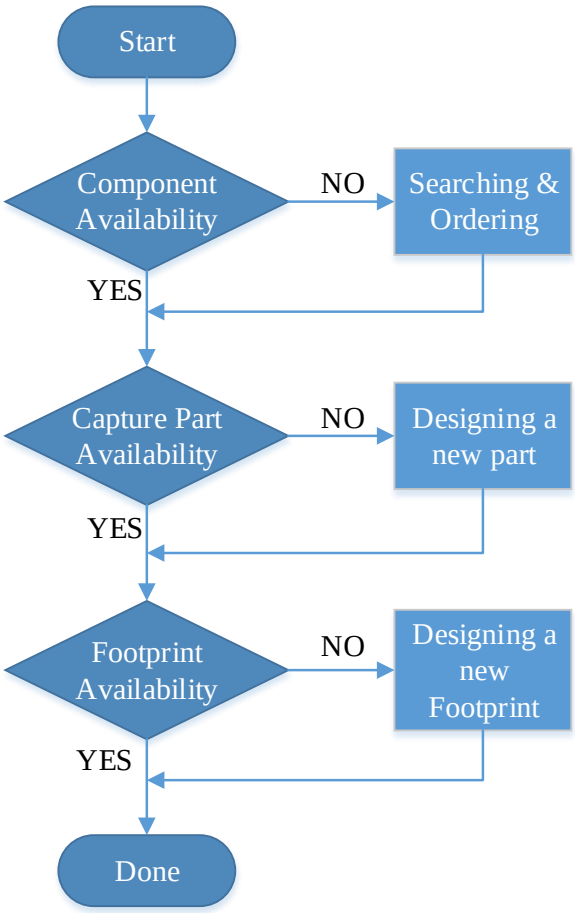


Figure 4.2 – Flowchart of Component Preparation.

4.2 Component Preparation

When it comes to a PCB design process, component preparation plays an extremely important role. A designer should be able to keep track of available component and check if it is suitable enough for the project before searching from other sources. Having the list of available components, the next step is investigating their footprints. If one part is adequate in term of technical parameters but has unapproved footprint, it must be replaced by a same-specification one with appropriate footprint. In order to design a PCB with OrCAD Capture CIS and PCB Editor, each component must have two mandatory elements: (1) a Capture part to represent in schematic, and (2) the footprint to represent in layout. Lacking of one element could result in a temporary halt in the design process.

Not all components satisfies both required elements for Capture CIS and PCB Editor as mentioned above. Except common passive parts like resistor, capacitor, and diode etc., which their Capture symbols and footprints hardly have special characteristic, component likes PIC18F4550 micro-controller or IXDN604SIA gate driver have neither compatible Capture symbol nor footprint. Some manufacturers provide their customer with either product's Capture-compatible libraries of symbol or footprint (*.dra files), some even supply both but it is not the case for this project. After searching thoroughly the Internet, we found out that the better way is to design both Capture symbol and footprint for: the PIC18F4550 micro-controller, the IXDN604SIA gate driver, and the EFD20 transformer. Fortunately, designing a new Capture symbol takes very small amount of time while PCB Editor has a greatly useful wizard tool for footprint design. All we need to find is datasheet for each component.

4.3 The PIC18F4550 micro-controller

Neither Capture symbol nor footprint is available for the PIC18F4550. However, designing Capture symbol for any component is not a difficult task. Basically, we just need to know how many pins the component has, and what sort of pin (power, passive etc.) as well as function (name) of each pin. More delicately, one can carefully draw symbol's shape so that it is similar to the real one but this work is optional. In general, we can draw any component's body in rectangular shape for simplicity.

The PIC18F4550 micro-controller in this project is a DIP-package with 40 pins, includes 35 I/Os. The designed Capture symbol for a 40-pin DIP-type PIC18F4550 micro-controller is shown in Fig. 4.3. All pins were labeled as in manufacturer's datasheet.

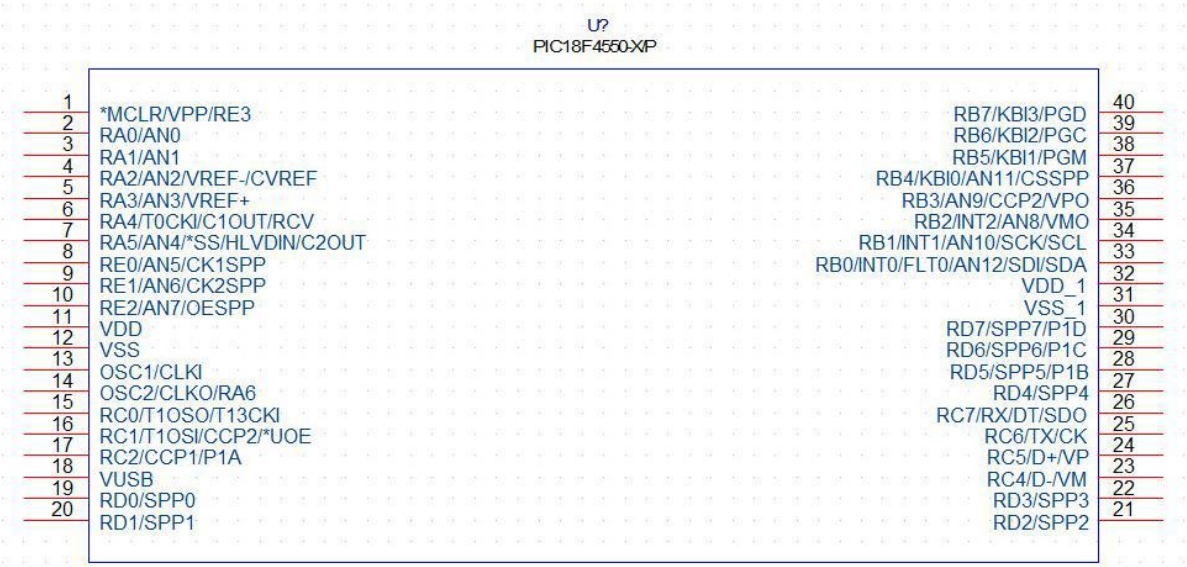


Figure 4.3 – Designed Capture symbol for a 40-pin DIP-type PIC18F4550 micro-controller.

Before establishing footprint design for the PIC18F4550 micro-controller, its packaging information must be carefully investigated. We have to prepare, at least, all the required information for the Package Symbol Wizard of PCB Editor. Table 4.1 lists all necessary package information in this case.

Table 4.1 – Packaging information for PIC18F4550 micro-controller's footprint.

Package	DIP
Number of pin/Number of IO	40
Lead pitch	100 mils
Terminal row spacing	650 mils
Package width	545 mils
Package length	2058 mils
Pad type	PAD50CIR32D.pad

When the Package Symbol Wizard is first opened, it provides an option to select various package type (Fig. 4.4). In this case, DIP is the selection. Next, a default template is loaded for the selected package and the dimension unit of the package is chosen. Almost all datasheets provide the packaging information in "inch", therefore, "mils" conversion is needed (1 inch = 1000 mils) (Fig. 4.5). The wizard process continues with "DIP Parameters" window, where all necessary dimensions are entered (Fig. 4.6). Some datasheets present package information with 3 values for each: nominal, maximum, and minimum dimension. It is recommended to input at this stage with nominal value in order to avoid any possible mismatch later. Finally, a padstack must be selected (Fig. 4.7).

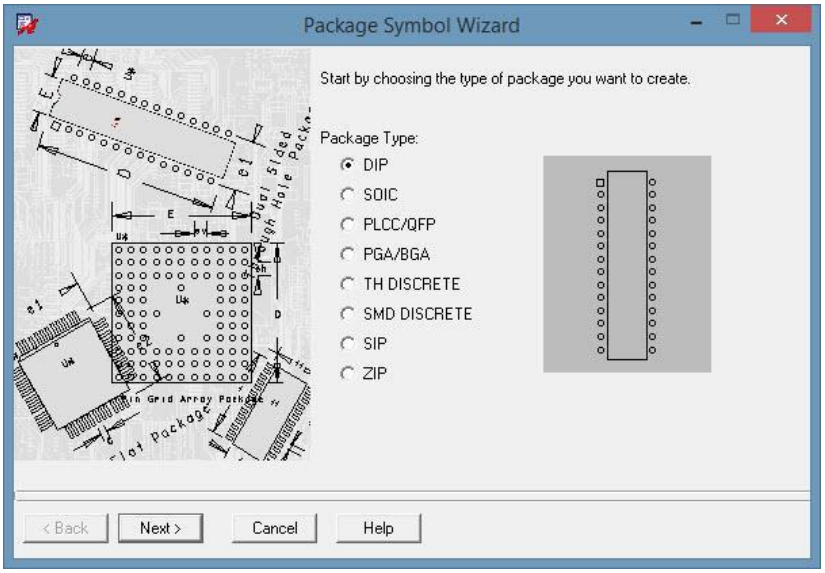


Figure 4.4 – Selecting the type of package.

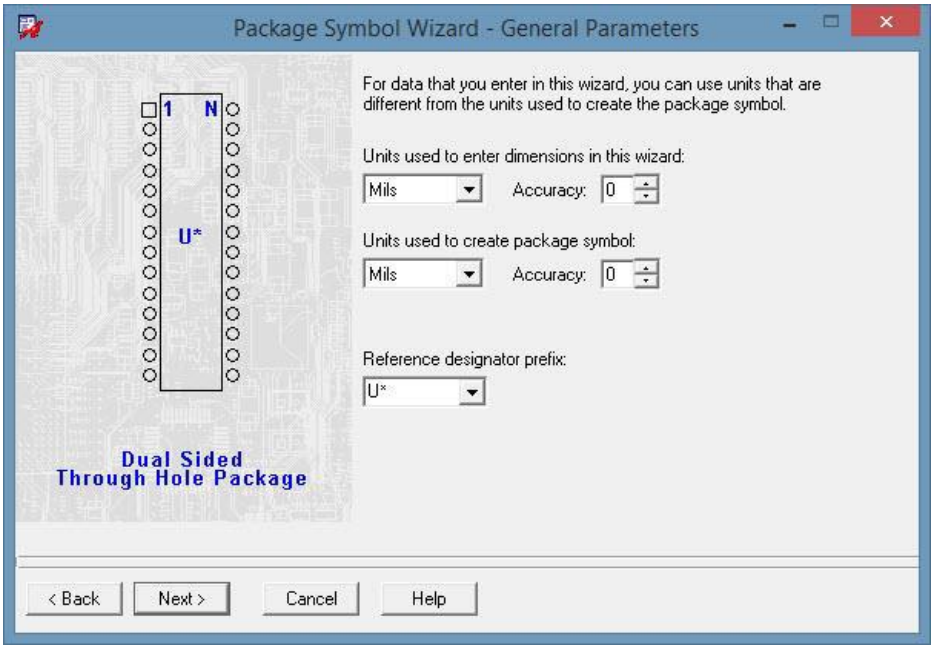


Figure 4.5 – Selecting the dimension unit. "Mils" is much convenient compared to "mm" since almost datasheets show packaging dimension in "inch", which is thousand times of "mils."

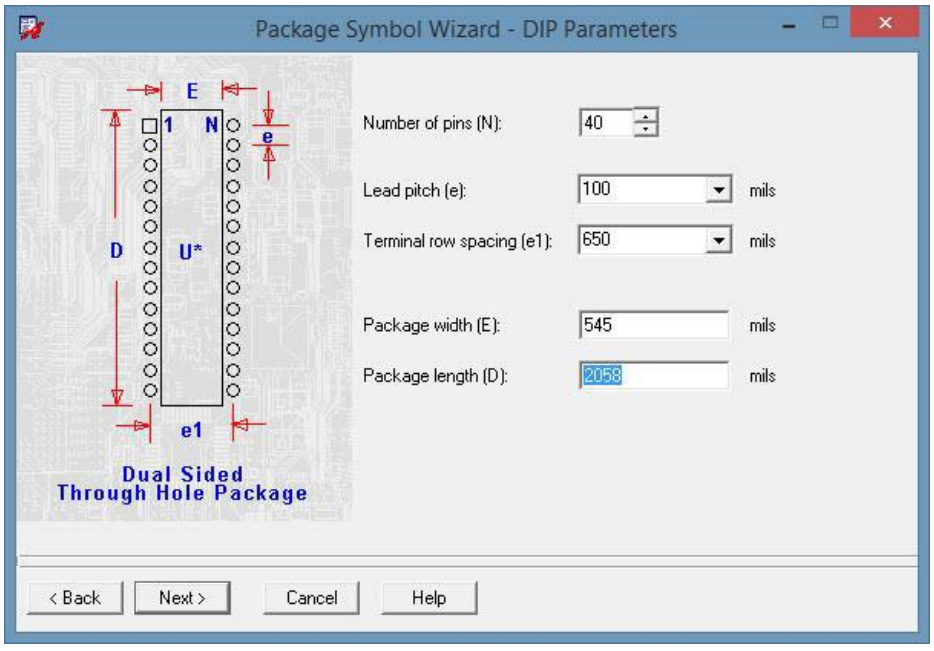


Figure 4.6 – DIP Parameters window.

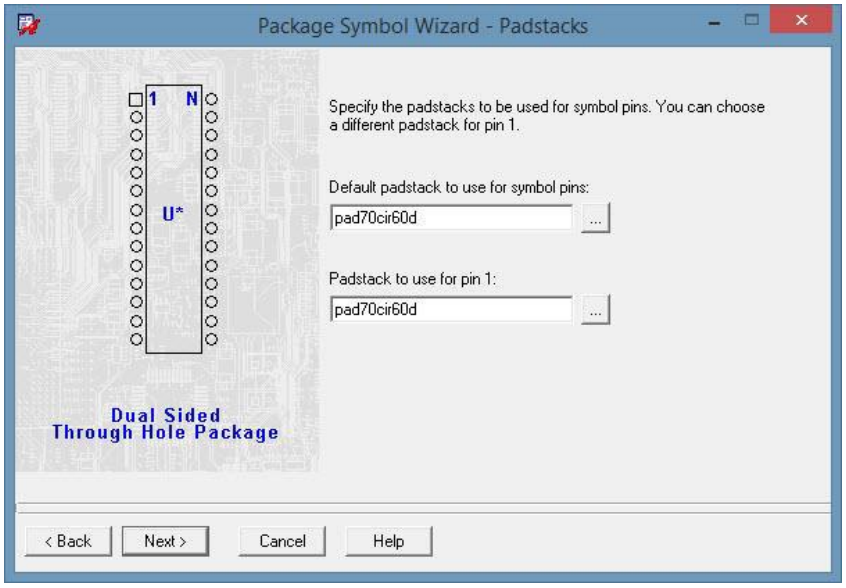


Figure 4.7 – Choosing a padstack for symbol pins. A padstack must be prepared in advanced, based on package information of datasheet.

The footprint design result for the 40-pin DIP-type PIC18F4550 micro-controller is shown in Fig. 4.8. It is named as "PIC18F4550PDIP.dra". Another important step is checking if this new footprint is compatible with the above Capture symbol. If the designed footprint can be successfully added to PCB Editor after netlist is exported from Capture, the new footprint works faultlessly with its Capture symbol. Otherwise, designer should check if any mismatch existed between the two models.

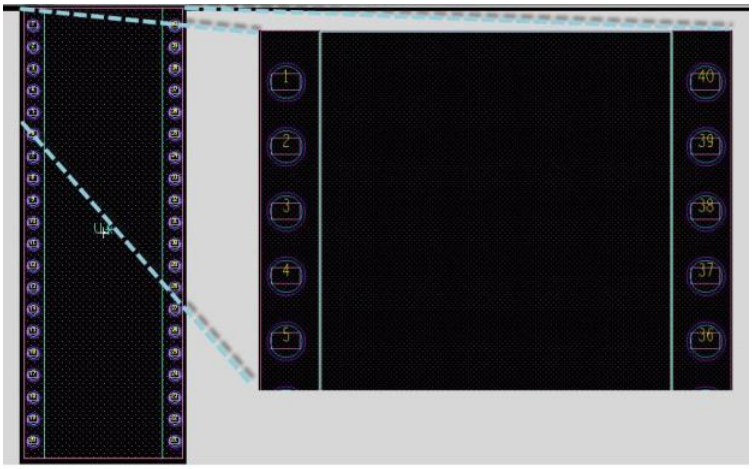


Figure 4.8 – Designed footprint for the 40-pin DIP-type PIC18F4550 micro-controller (PIC18F4550PDIP.dra).

4.4 Power supply solution for the micro-controller and other ICs

The PIC18F4550 micro-controller, the IXDN604SIA gate driver, and the TLC272 operational amplifier, all require a 5-V power supply for operation. In this project, a separate power supply is not planned. Therefore, a voltage divider will be deployed to obtain an approximately 25 VDC voltage after the bridge rectifier. Using the LM78M05 voltage regulator, a stable 5 VDC source can be achieved. Input voltage of the LM78M05 must not be smaller than 8V and the two power resistors which forms the voltage divider should be able to dissipate the maximum current flowing through. The circuit schematic for resistors' calculation is shown in Fig. 4.9.

The maximum input voltage to LM78M05 happens when there is no load and the minimum input voltage comes if the load is maximum. The maximum input voltage should be about 25 V while the minimum input voltage must be greater than 8V for the output of LM78M05 has stable value of 5 V. Assume the maximum cumulative current load for the PIC18F4550 micro-controller, the IXDN604SIA gate driver, and the TLC272 operational amplifier is 30 mA (10mA for each device). The calculation for power resistors should take into account of rated dissipative power, standard values of resistor, availability of product, footprints etc.

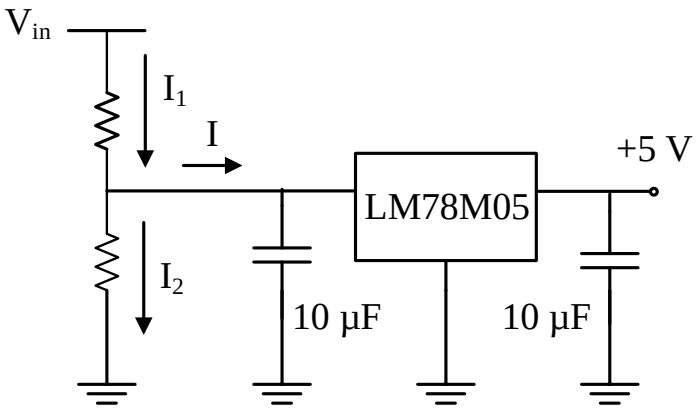


Figure 4.9 – Circuit Schematic for calculating of voltage divider's power resistors.

After doing calculation then checking with above mentioned factors, two power resistors with relevant parameters are tabulated in Table 4.2. The checking process for those two power resistors are demonstrated next.

Table 4.2 – Parameters of the selected resistors.

Parameter	Resistor	
	R_1	R_2
Resistance (Ω)	1000	180
Footprint	to220aa.dra	res400.dra
Power (W)	25	4

The maximum current flows through two resistors if there is no load connected to 5V source:

$$I_1 = I_2 = \frac{169\text{V}}{1000\Omega + 180\Omega} = 0.143\text{A} \tag{4.1}$$

Thus, the maximum drop voltage on R_2 is:

$$V_{\max} = (0.143\text{A}) \times (180\Omega) = 25.74\text{V} \tag{4.2}$$

With an assumption that the maximum load current is 30 mA, the minimum current flows through resistor R_2 is:

$$I_{2\min} = I_2 - 0.03 = 0.143 - 0.03 = 0.113\text{A} \tag{4.3}$$

Therefore, the minimum input voltage is:

$$V_{\min} = (0.113\text{A}) \times (180\Omega) = 20.34\text{V} > 8\text{V} \tag{4.4}$$

The maximum dissipative powers on each resistor are:

$$\begin{aligned} P_{1\max} &= I_1^2 \times R_1 = 0.143^2 \times 1000 = 20.45\text{W} \\ P_{2\max} &= I_1^2 \times R_2 = 0.143^2 \times 180 = 3.68\text{W} \end{aligned} \tag{4.5}$$

4.5 Capture symbol and footprint preparation for the gate driver and the transformer

Both the gate driver and the transformer have neither Capture symbol nor footprint available. The same design procedure was applied for the Gate driver and the Transformer's preparations. Two new padstacks were also designed for each component, based on the recommended land patterns from their manufacturers [26]-[27]. The new designed padstack for transformer named "SMD138REC89.pad" and the gate driver's one is "SMD62_24.pad." The package type for two components was considered to be in SOIC group. Followed the same steps as illustrated in Section 4.3 of this chapter, two footprints were designed successfully. The testing process shown that they works perfectly with designed Capture symbol. The Capture symbols for the EFD20 transformer and the IXDN604SIA gate driver are shown in Fig. 4.10 and Fig. 4.11, respectively. The designed footprint for the gate driver was named "IXDN604SIA.dra" (Fig. 4.12) while the corresponding one for the transformer is "EFD20.dra" (Fig. 4.13).

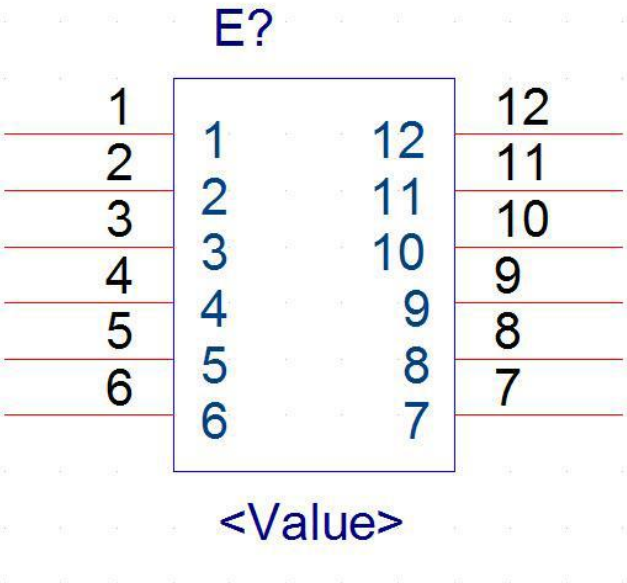


Figure 4.10 – Capture symbol for the EFD20 transformer.

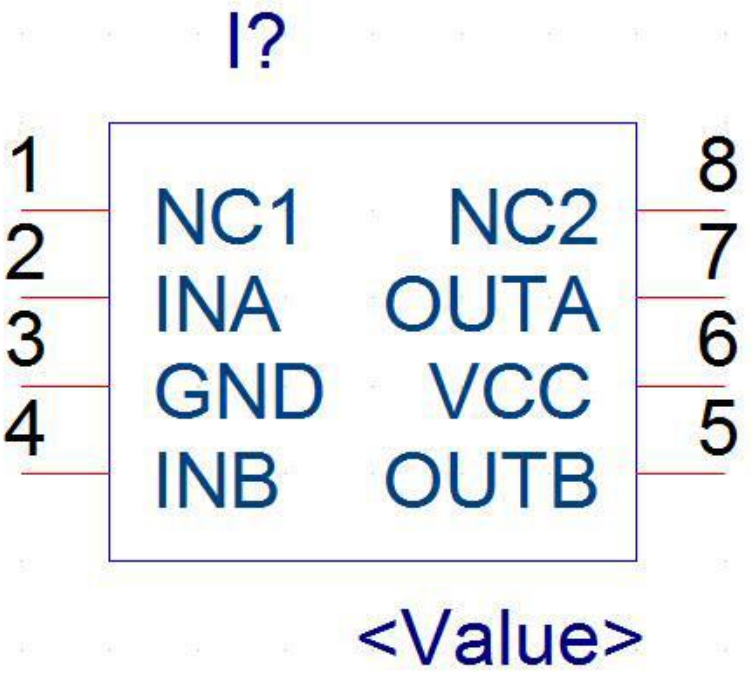


Figure 4.11 – Capture symbol for the IXDN604SIA gate driver.

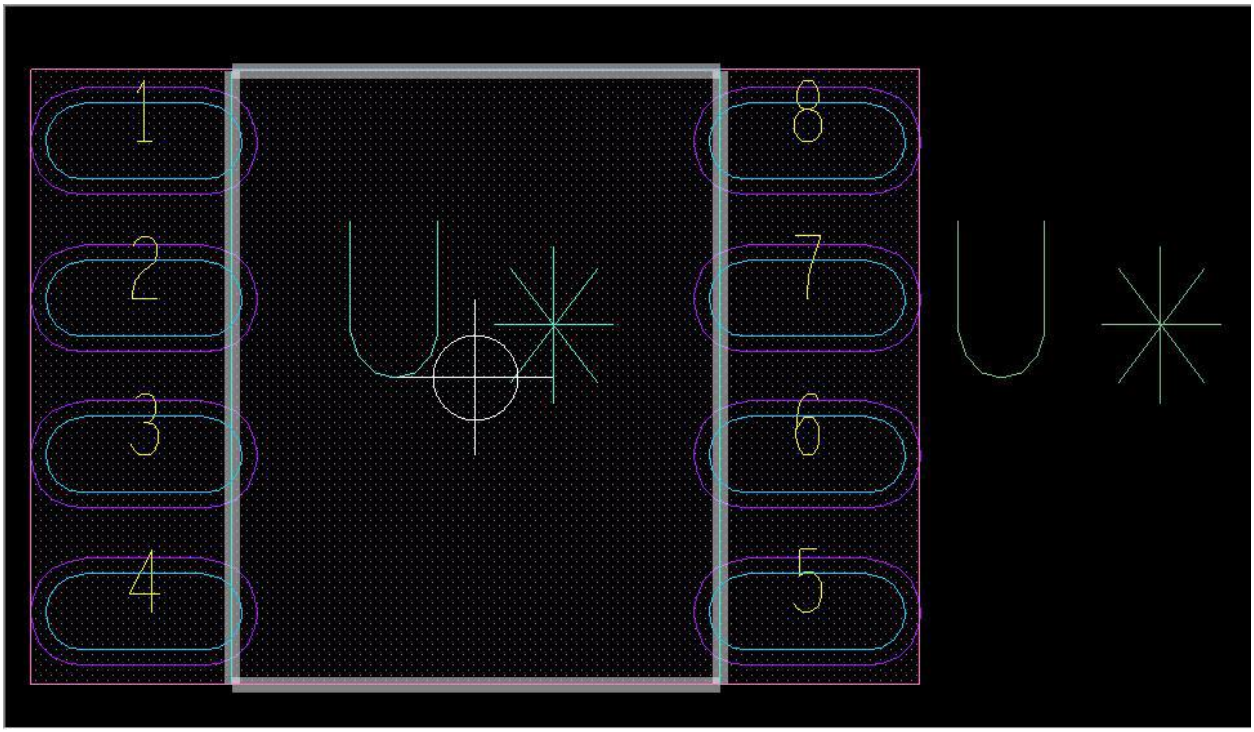


Figure 4.12 – The Gate driver IXDN604SIA's designed footprint (IXDN604SIA.dra).

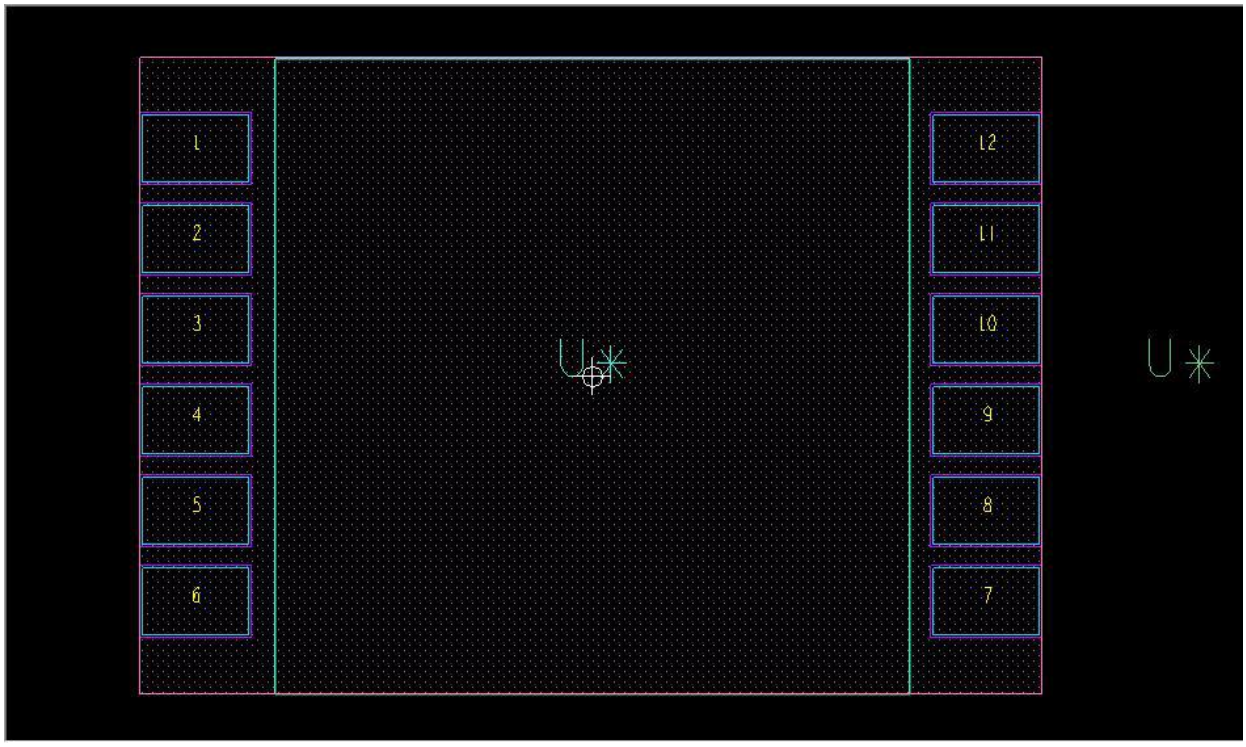


Figure 4.13 – The EFD20 transformer's designed footprint (EFD20.dra).

4.6 PCB Design

After finishing all preparations, the PCB is now ready to be layout. First of all, a schematic must be drawn in Capture CIS. At this stage of design process, the Capture part in schematic can be in any shape, as long as its number of pin matches with number of pin on the corresponding footprint. It means that any Capture part with 12 pins can be arbitrarily chosen to represent the transformer and then assign it with the "EFD20.dra" footprint to obtain an appropriate model for transformer without suffering from any error message. The most important thing is how consistently the Capture symbol matches with the footprint, no matter what it is.

The Capture schematic for the micro-controller based primary-side sensing flyback converter driver for LED is shown in Fig. 4.14. Three off-board connectors "T Point R" are added in order to directly connect the board with standard AC socket. A 10-µF capacitor is installed across the

input and output of the LM78M05 voltage regulator according to manufacturer's datasheet for this application [28]. The 10 µF output capacitor helps to improve the transient performance of the voltage regulator.

Four micro-controller's pins are employed as input to collect data. Sample of rectified voltage will be fed through pin 2 (RA0/AN0) while the voltage signal represents primary side switching current will be collected at pin 3 (RA1/AN1). Output signals of the zero current detector and the peak current detector are acquired at pin 7 (RA5/AN4) and pin 8 (RE0/AN5), respectively. All input signals are fed through pins that associated with the (Analog-to-Digital Converter) ADC channels. However, it should be noted that two channels AN2 and AN3 are reserved for VREF+/VREF- connecting in case another reference voltage signal than VDD is used for ADC converting operations. Driving signal for the MOSFET will be obtained from pin 17 (RC2/CCP1/P1A), which belongs to Capture/Compare/PWM (CCP) module no.1. This driving signal needs to be fed through the IXDN604SIA gate driver to ensure the success of switching operation.

One important design aspect about the compatibility of Capture symbol with its corresponding footprint may happen here. It is the case of diode D9, a BAT54 type, which has 3 pins. Only pin 1 and pin 3 are used to form a diode. However, if a normal Capture symbol with only two pins is employed to represent D9 in associated with an available footprint "sot23.dra" (as recommended from manufacturer's datasheet), an error will happen during layout process. The reason is "sot23.dra" has 3 pins, so that any associated Capture symbol must have the same number of pin in order to work properly.

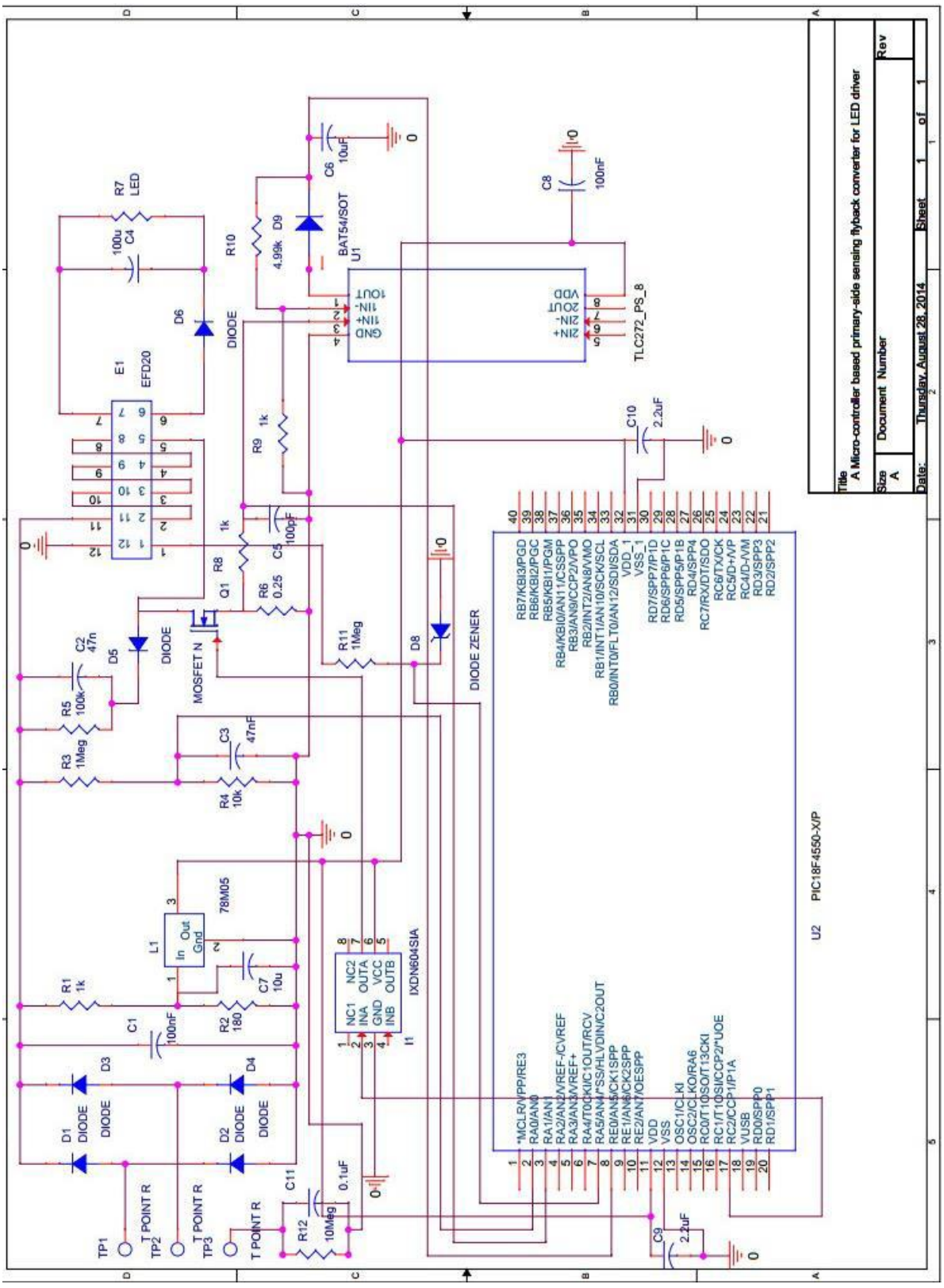


Figure 4.14 – Capture Schematic of PCB Design

Finishing with the schematic drawing, checking procedures before laying out are employed. Firstly, every components' footprint must be filled up. The exporting netlist process still works if several footprints are missed but those parts without footprint will not be able to be added to the layout. Therefore, the layout process may be interrupted just because of missing one footprint. Next, a DRC (Design Rules Check) should be conducted to see if any design rule violation exists. Meanwhile, during the checking process, a Bill of Material (BOM) should be created as a reference for future work. BOM for the current project is tabulated in Table 4.3.

Table 4.3 – Bill of Material (BOM) for the current project.

Item	Quantity	Reference	Part	Footprint
1	2	C1,C8	100nF	cap400
2	1	C2	47nF	ck15-10pf
3	1	C3	47nF	ck15-10pf
4	1	C4	100u	cap400
5	1	C5	100pF	cap400
6	1	C6	10uF	cap400
7	1	C7	10u	cap1000
8	2	C9,C10	2.2uF	cap400
9	1	C11	0.1uF	cap400
10	5	D1,D2,D3,D4,D6	DIODE	do41
11	1	D5	DIODE	do35
12	1	D8	DIODE ZENER	sod80
13	1	D9	BAT54/SOT	sot23
14	1	E1	EFD20	EFD20
15	1	I1	IXDN604SIA	IXDN604SIA
16	1	L1	78M05	to220ab
17	1	Q1	MOSFET N	to220ab
18	1	R1	1k	to220aa
19	1	R2	180	res400
20	2	R3,R11	1Meg	res400
21	1	R4	10k	res400
22	1	R5	100k	res400
23	1	R6	0.25	res400
24	1	R7	LED	res400
25	2	R8,R9	1k	res400
26	1	R10	4.99k	res1000

Item	Quantity	Reference	Part	Footprint
27	1	R12	10Meg	res400
28	3	TP1,TP2,TP3	T POINT R	tp4xx
29	1	U1	Value	soic8
30	1	U2	Value	PIC18F4550PDIP

After the netlist was successfully exported to PCB Editor, the layout process starts with setting board's parameters. The board outline could be created immediately or right after placing and routing. One convenient way to manually place parts is using "Cross-probing" feature [29]. It allows the selected component in PCB Editor to be highlighted in Capture window if the two programs are on at the same time. This feature helps designer to easily monitor and visualize the corresponding place of component on the board.

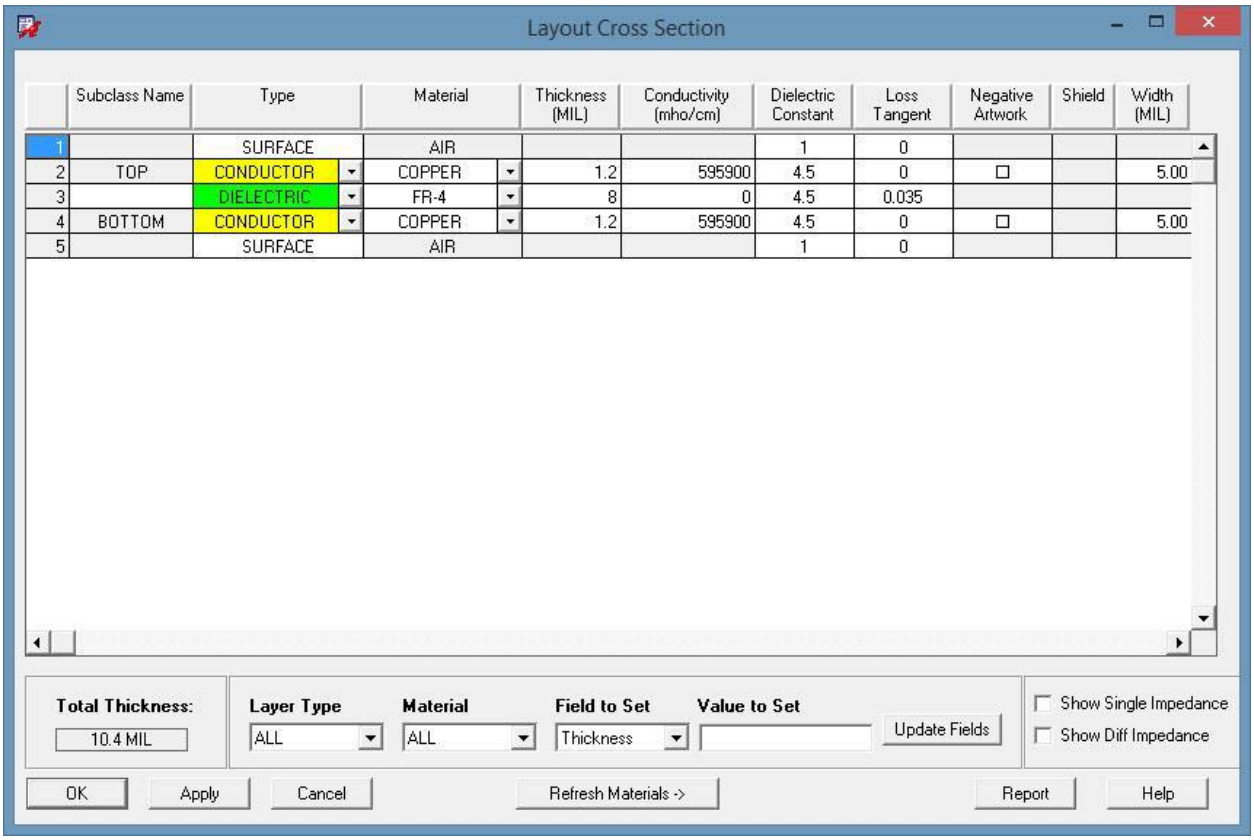


Figure 4.15 – Defining layer stack-up for the PCB. Two layers are enough for this project.

Components could be placed on both sides of the board, so that the board size might be smaller. Therefore the cost for PCB would be dramatically reduced. This type of board requires experienced designer and highly skilled soldering technique. In this project, however, only a demo board is needed for experimental purpose, thus all the components will be soldered on one side only. For the same reason, only two layers: top and bottom will be used for routing (Fig. 4.15). It is not necessary for defining more layer stack-up at this stage of the project.

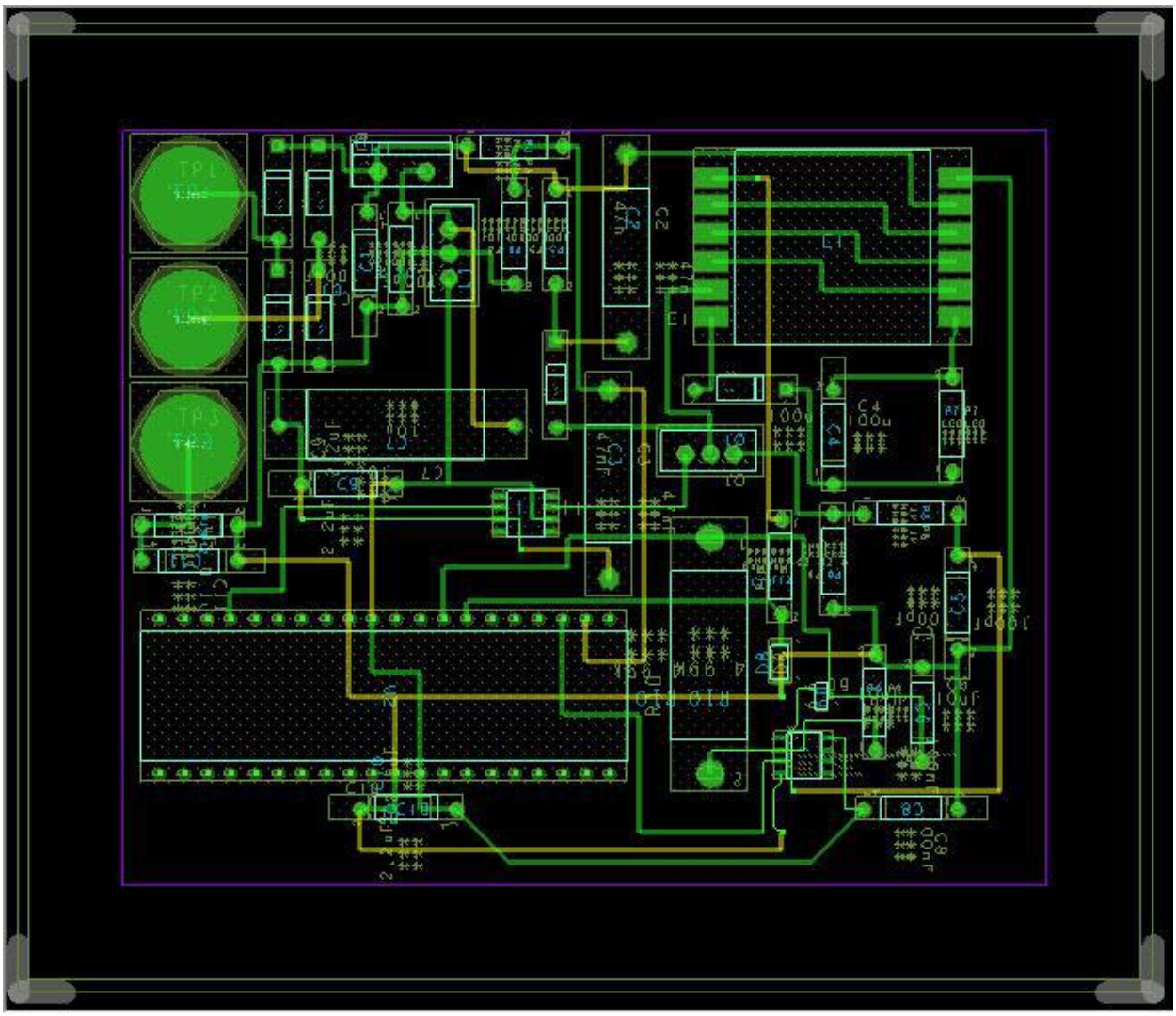


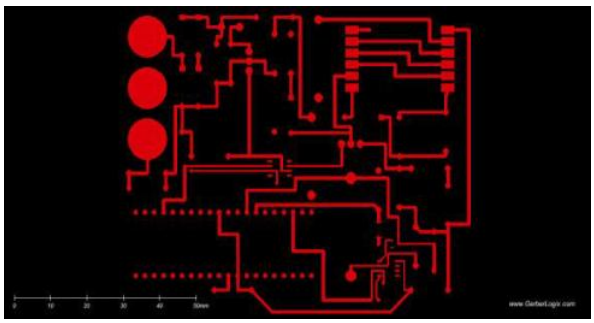
Figure 4.16 – Arrangement of Components and Routing on the PCB.

With only two layers, the routing work becomes a less complicated work even the Lite version of PCB Editor does not have “Auto Routing” feature. In order to ensure the integrity of signal, all traces must have at least 30 mils in width, except some traces come to IC’s legs, which has smaller pad area. The complete-routing board is shown in Fig. 4.16.

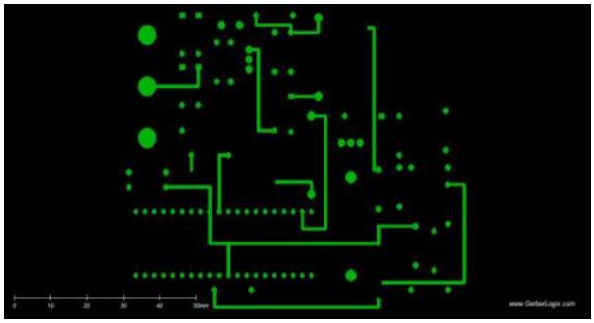
4.7 Artwork Generating

Design results of the layout process are not workable files with fabricating machine [30]. They must be converted into a compatible form under a process named “Artwork Generating.” With PCB Editor, set of resulted artwork files includes:

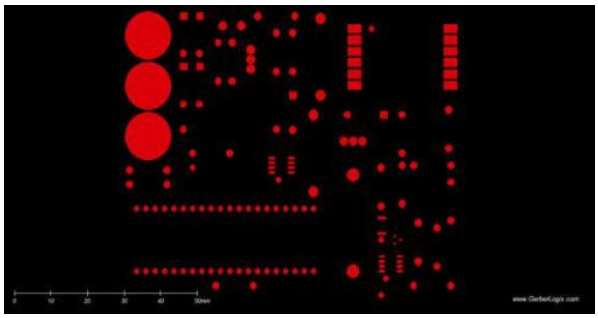
- Top.art (Fig. 4.17 (a)): Showing all routes and pads of component on the top side.
- Bottom.art (Fig. 4.17 (b)): Showing all routes and pads of component on the bottom side.
- SoldermaskTop.art (Fig. 4.17 (c)): Showing all Footprint’s Soldermasks on the top side.
- SoldermaskBottom.art (Fig. 4.17 (d)): Showing all Footprint’s Soldermasks on the bottom side.
- SilkscreenTop.art (Fig. 4.17 (e)): Showing component’s silkscreen on the top side, includes the board’s outline. Since all the components will be soldered on the top side only, there is no need to generate “SilkscreenBottom.art” file.
- LEDFLYBDRVR-1-2.drl (Fig. 4.17 (f)): Contains information about all the board’s drills.
- LEDFLYBDRVR.rou: Route file, contains information about ways to cut the board. This cutting trace is shown in Fig. 4.16 with four grey corner marks.



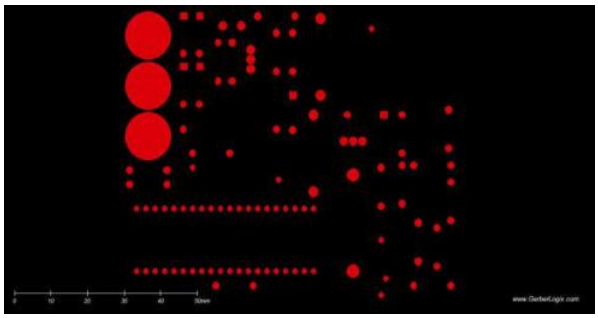
(a) Top.art



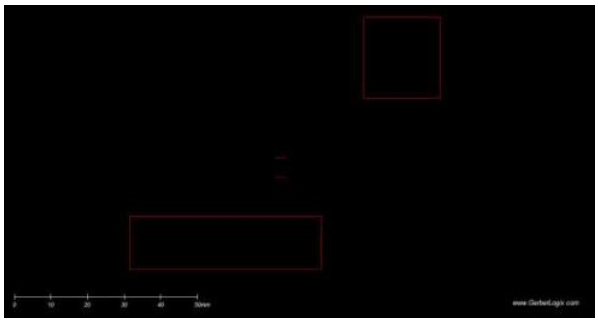
(b) Bottom.art



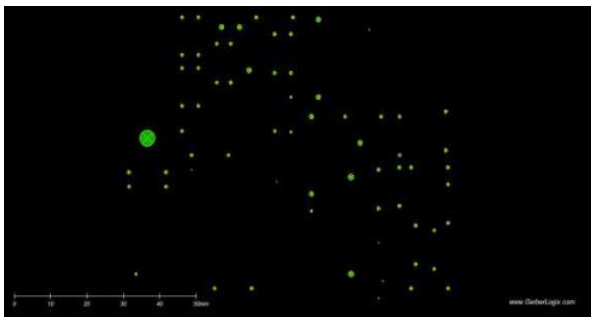
(c) SoldermaskTop.art



(d) SoldermaskBottom.art



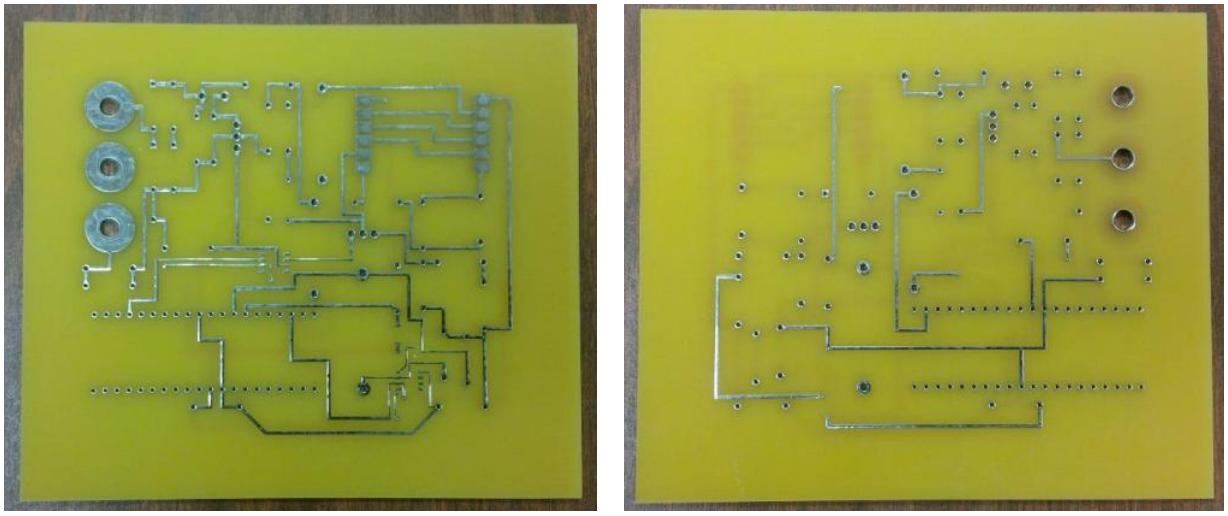
(e) SilkscreenTop.art



(f) LEDFLYBDRVR-1-2.drl

Figure 4.17 – Generated Artwork files as seen from GerberLogix Viewer.

After comparing with the intended design on PCB Editor, all the artworks are verified and ready for fabrication. The fabricated board is shown in Fig. 18 and the board with all soldered components (except the PIC18F4550 micro-controller, which is on programming process) is shown in Fig. 4.19.



(a) Top view (b) Bottom view

Figure 4.18 – Designed PCB after fabricating by Sunstone PCB Vendor.

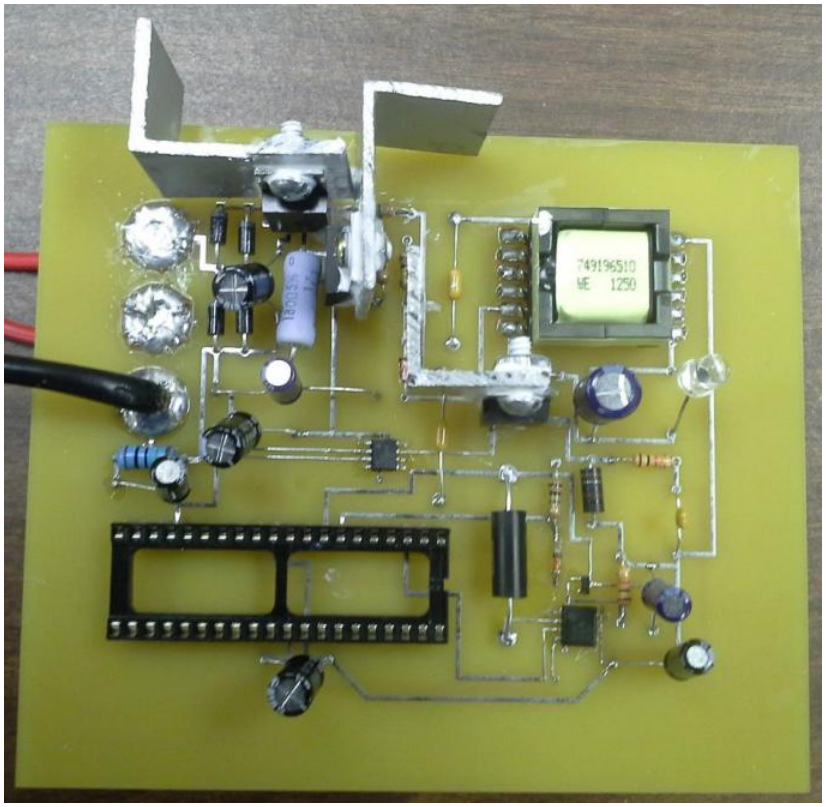


Figure 4.19 – The complete PCB with soldered components as seen from top view.

4.8 PIC18F4550 Programming

The PCB was designed with no programming socket. Therefore, the PIC18F4550 must be connected to the PicKit3 Programmer via a breadboard as in Fig. 4.20. The HEX file, which is programming's result, will be written to the micro-controller's memory when PicKit3 is connected to the computer. This section discusses all relevant programming aspects in the current project.

The Integrated Development Environment (IDE) for PIC18F4550 programming is MPLAB X v2.15 with compiler XC8. This genuine compiler from Microchip Technology offer various advantages like code-efficient benefit, auto-suggest and auto-complete writing etc. MPLAB X also supports auto-generating compiler directives (#pragma config) [31], a feature which determines a lot of micro-controller's operations, like Watchdog Timer, Voltage Regulator USB etc. The resulted HEX file as an output of MPLAB X-XC8 compiler is also smaller when compares to the previous MPLAB 8.xx version. This point is very important because it means that the code was optimized at a higher level, guarantee a higher working efficiency and memory saving.

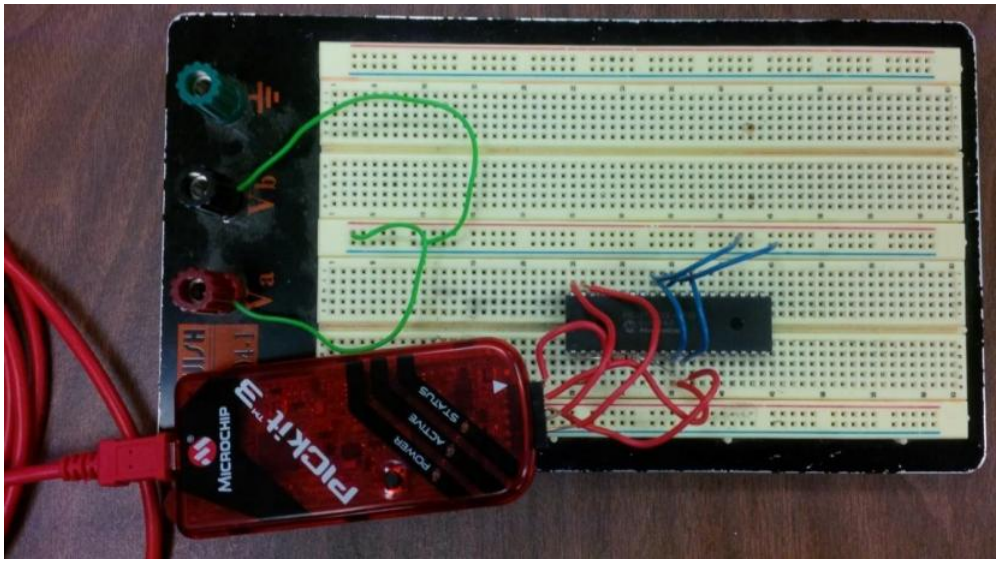


Figure 4.20 – Connecting the PIC18F4550 with PicKit3 programmer via a breadboard.

Firstly, the directives or configuration bits must be established appropriately. Even the code is compiled and properly burned to the chip, it is an inappropriate configuration bit might prevent the chip to work. Fortunately, many of default auto-setting configurations are applicable for almost every case. There is only some parameters that needed to be adjusted in order to achieve desired performance. The following settings show which configuration bits are subjected to be change from its default auto-setting value:

- #pragma config FOSC = INTOSC_EC: This directive is relevant to selecting the oscillator source. In this project, the internal oscillator 8MHz is used, therefore, the directive's value is "INTOSC_EC."
- #pragma config IESO = OFF: The "ON" value allows the oscillator source to be switchable from internal to external source and vice versa. The value now is OFF since switching to an external oscillator source is temporarily not planned.
- #pragma config WDT = OFF: This selection will turn off Watchdog Timer feature.
- #pragma config LVP = OFF: Turning off the "Single-Supply ICSP."

Next, all necessary signals must be acquired and converted using ADC channels and counters. Three input signals will be fed through analog pins and then be converted by ADC: sample of rectified voltage to AN0, signal of primary switching current to AN1, and peak current signal to AN5. Signal from zero current detector will be acquired by a timer, which is configured to work as a counter in this case. The sample codes for using ADC and counter to obtain signal are following.

- Sample code for using ADC:

```
TRISAbits.TRISA0 = 1;    //A0 is analog input
```

```
ADCON0 = 0b00000000;    //Channel 0, AD is OFF
ADCON1 = 0b00000000;    //VREF+ = VDD, VREF- = VSS, all analog input
ADCON2 = 0b10001000;    //Right justified, Fosc/2, 2TAD
ADCON0bits.ADON = 0x01;    //Enable A/D Module
__delay_ms(1);    //Time for sampling
ADCON0bits.GO_DONE = 1;    //Start AD conversion
while (ADCON0bits.GO_DONE != 0);
vsamp1 = ADRESH*256 + ADRESL;    //Merge data from two registers
vsamp2 = (vsamp1*5)/1024;    //VDD=5, 10-bit ADC
__delay_ms(1);
```

- Sample code for using timer as a counter:

```
TRISAbits.TRISA4 = 1;    //Make RA4/T0CKI an input
T0CON = 0x68;    //Timer0, 8bit, no prescaler
while ((zcd2 >= 4.3) && (INTCONbits.TMR0IF == 0)){
        T0CONbits.TMR0ON = 1;    //Turn ON Timer0
        tz = TMR0L;
 }
 T0CONbits.TMR0ON = 0;    //Turn OFF Timer 0
 INTCONbits.TMR0IF = 0;    //Clear flag
```

After having and processing signals, a suitable PWM signal must be generated. The following sample code will generate a PWM signal with 40% duty cycle.

```
TRISCbits.RC2 = 0;    //CCP1 pin is an output
PORTCbits.RC2 = 0;
PR2 = 19;    //PWM frequency is 100 kHz
T2CON = 0b00000000;    //Timer2, no prescaler or postscaler, initially OFF
CCPR1L = 7;    //40% duty cycle
CCP1CON = 0b00101100;    //Timer2 is used for PWM
T2CONbits.TMR2ON = 1;    //Turn ON Timer2
```

The value of PR2 register is calculated from the formula:

$$PR2 = \frac{F_{OSC}}{4 \times F_{PWM} \times N} - 1 \qquad (4.6)$$

where F_{OSC} is the operating frequency of micro-controller (8 MHz for a PIC18F4550 with internal oscillator), F_{PWM} is the expected frequency of PWM (100 kHz), and N is the prescaler. By choosing N = 1, PR2 = 19. With 40% duty cycle, 0.4*19 = 7.6. Thus, the value of CCPR1L register is 7 and <bit 5:bit 4> of CCP1CON register is <1:0> as shown in the sample code above. The illustrated waveform for the 100-kHz PWM with 40% duty cycle is on Fig. 4.21.

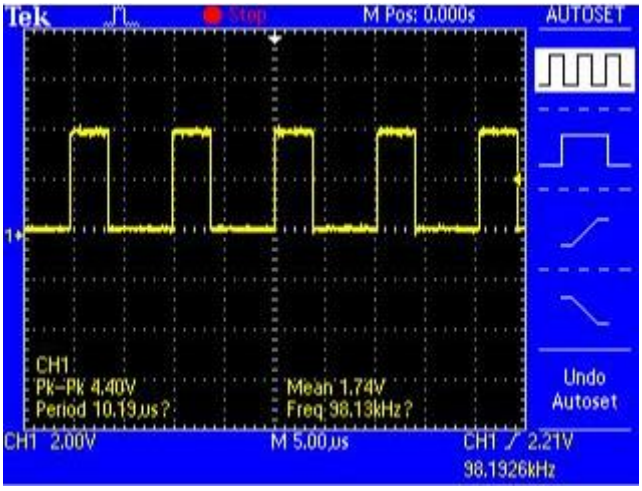


Figure 4.21 – The waveform of 100-kHz PWM with 40% duty cycle.

In the application, the duty cycle is a variable and will be adjusted in order to achieve the desired performance. The sample code for auto-adjusted PWM is shown below:

```
dc = 5;    //Start with 30% duty cycle
TRISCbits.RC2 = 0;    //CCP1 pin as an output
PORTCbits.RC2 = 0;
PR2 = 19;    //PWM frequency is 100kHz
T2CON = 0b00000000;    //Timer2 is OFF, no Prescaler or Postscaler
```

```
CCPR1L = dc;
CCP1CON = 0b00101100;    //PWM mode
T2CONbits.TMR2ON = 1;    //Turn ON Timer2
while ((isw2 > 1.1*iref)||(isw2 < 0.9*iref)){    //Compare
   while (isw2 > 1.1*iref){    //10% tolerance
      dc = dc + 1;    //Adjust the duty cycle
      if (dc > 9) break;    //The duty cycle must be less than 50%
      else {
         CCPR1L = dc;
         CCP1CON = 0b00101100;    //PWM mode
         T2CONbits.TMR2ON = 1;    //Turn ON Timer2
      }
   }
   while (isw2 < 0.9*iref){
      dc = dc - 1;
      if (dc < 2) break;
      else {
         CCPR1L = dc;
         CCP1CON = 0b00101100;    //PWM mode
         T2CONbits.TMR2ON = 1;    //Turn ON Timer2
      }
   }
}
```

The complete code which includes all the above excerpt will be compiled and then burned to the PIC18F4550. Chapter 5 discusses the experimental results of the actual system.

Chapter 5

Experimental results

5.1 Overview

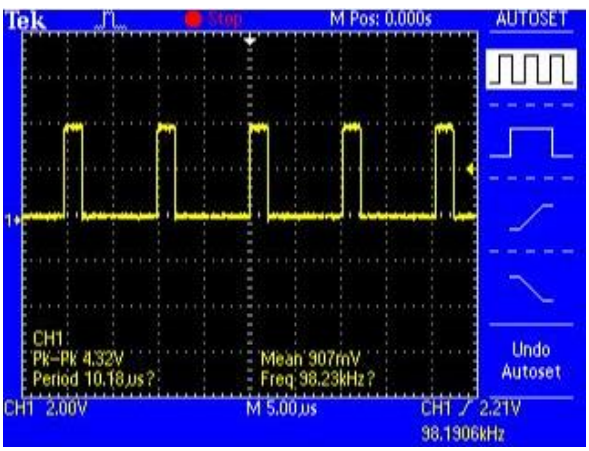
In this chapter, the important functionalities of the PIC18F4550 micro-controller in responding to the four analog input signals from the flyback converter are first investigated. The ability of the micro-controller to automatically provide PWM signals with different duty cycles and convert analog input signals to equivalent digital signal are two key features to the operation of the driver. Then, the open-loop performance of the flyback converter is examined. Finally, the closed-loop flyback converter is characterized for full converter performance.

5.2 The characteristics of PIC18F4550 micro-controller

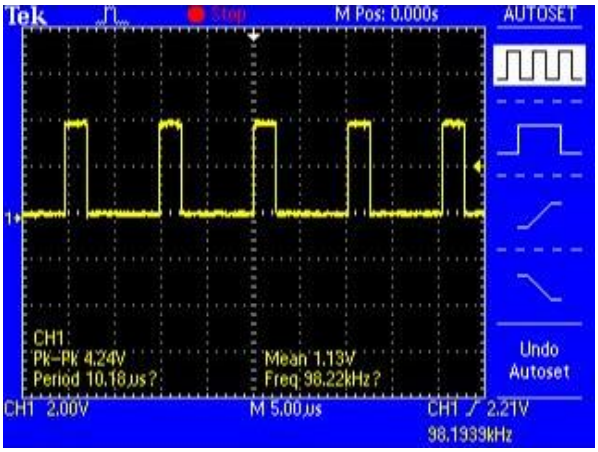
The ability to provide expected performance of the PIC18F4550 micro-controller is critically important to the project. Several key features of the PIC18F4550 must be investigated before being implemented on the actual closed-loop flyback converter.

The main purpose of the micro-controller is to generate the PWM signal with different duty cycles to drive the MOSFET switch, depending on the feedback. A micro-controller as the controller for a flyback converter should be able to provide PWM signal with various duty cycle, from 20% to 40%. By changing the content of CCPR1L register and bits <5:4> of CCP1CON register, the duty cycle of PWM signal can be adjusted. The PIC18F4550 PWM feature will be tested from 20% to 40% duty cycle with increment step of 5%. Testing the micro-controller this way also helps to detect the relationship between the varying of duty cycle with the varying of CCPR1L and CCP1CON registers' content, thus obtaining the control algorithms for the feedback PWM function.

In the previous Chapter 4, the waveform of PWM signal with 40% duty cycle was shown. In Fig. 5.1, the waveforms of PWM signal with 20%, 25%, 30%, and 35% duty cycle are revealed, which demonstrate for the ability of the micro-controller to generate various PWM signals as expected.

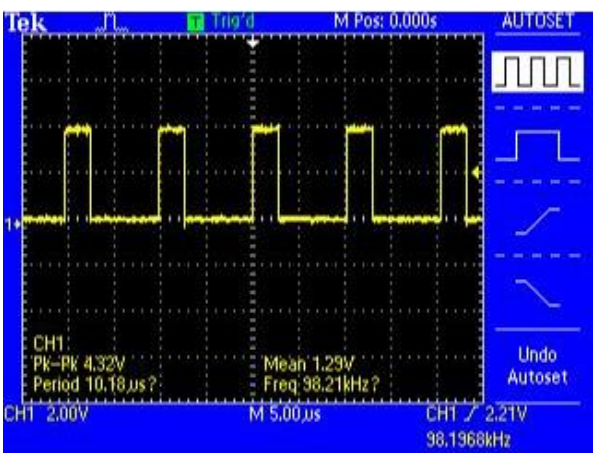


(a) PWM 100 kHz, 20% duty cycle

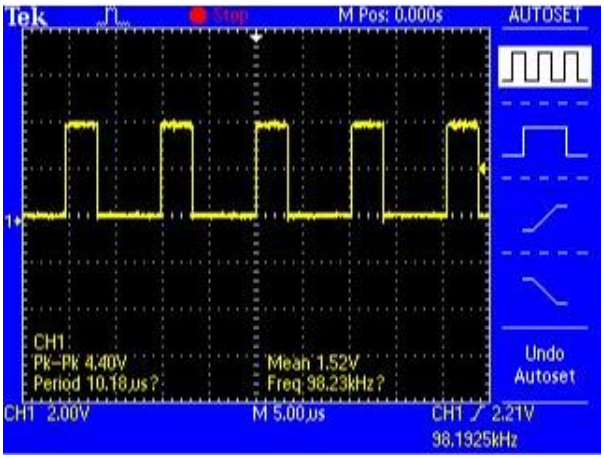


(b) PWM 100 kHz, 25% duty cycle

Figure 5.1 – Various PWM signal with different duty cycles: 20%, 25%, 30%, and 35%.



(c) PWM 100kHz, 30% duty cycle



(d) PWM 100 kHz, 35% duty cycle

Figure 5.1 – Various PWM signal with different duty cycles: 20%, 25%, 30%, and 35% (cont.).

Next, the ADC function of the PIC18F4550 micro-controller is tested. This experiment evaluates the micro-controller's ability to convert an analog input signal to digital signal. The ADC function in the PIC18F4550 is 10-bit type with 13 independent channels. The schematic for testing ADC is shown in Fig. 5.2. The physical circuit for testing ADC is shown in Fig. 5.3.

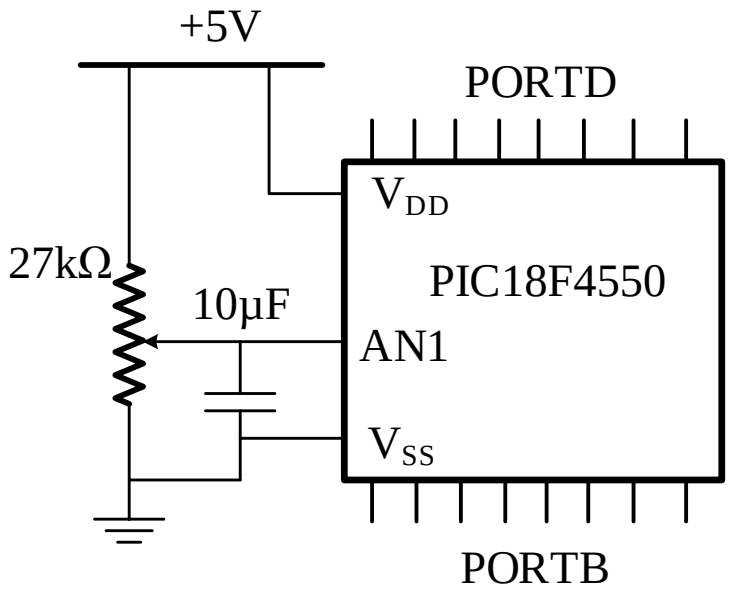


Figure 5.2 – Circuit schematic for ADC testing.

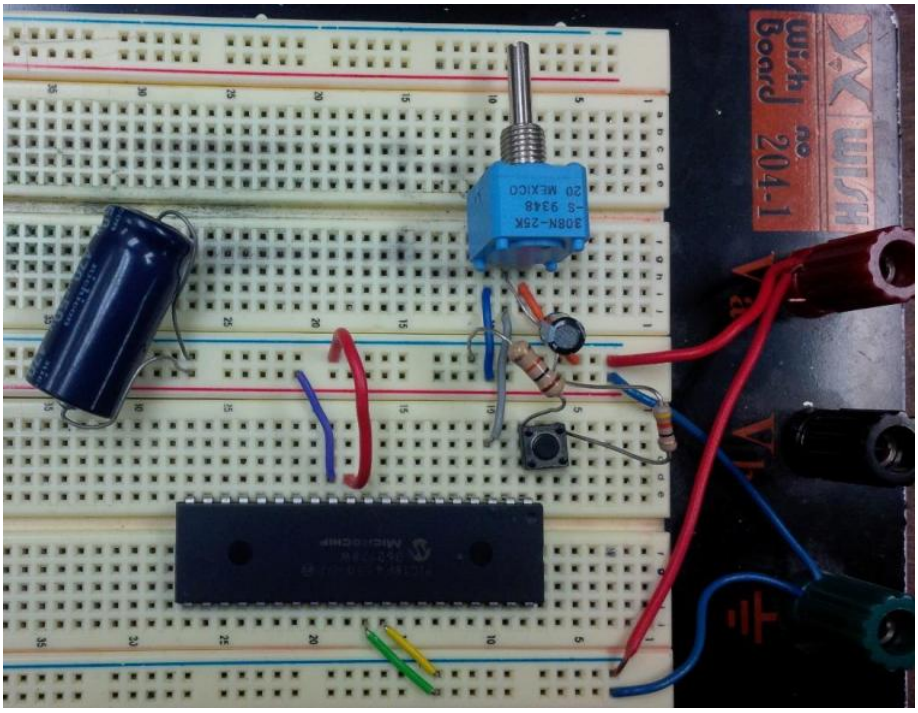


Figure 5.3 – Implementing a testing circuit for PIC18F4550's ADC function.

A variable resistor is used to create various input voltages to the channel 1 (AN1) of ADC as in the schematic. The power supply of the micro-controller is also the voltage source for the variable resistor while the ground is common. The ADC results are left justified and then fed through PORTD (ADRESH: 8 MSB bits) and PORTB (ADRESL: 2 LSB bits). By measuring the voltage level of each pin of PORTD and PORTB, the ADC results are obtained. Then, the ADC results will be compared to the input voltage to evaluate the differences.

The same code as in Chapter 4 was used for ADC function. The ADC results were forwarded to PORTD and PORTB by using simple assign instructions: "PORTD = ADRESH" and "PORTB = ADRESL." The reference voltage VREF+ for ADC function is chosen as VDD (+5V), while VREF- is VSS (ground). With 10-bit resolution, the step size is:

$$\text{Step size} = \frac{5}{2^{10} - 1} = 4.888 \text{ mV} \tag{5.1}$$

The meaning of the step size is the smallest difference between two input voltage's levels that the micro-controller can discern. Therefore, with input voltage of 5V, the result is:

$$\text{Result} = \frac{V_{in}}{\text{Step size}} = \frac{5\text{V}}{4.888\text{mV}} = 1023 \tag{5.2}$$

The equivalent binary value for the above result is 1111 1111 11. This is an expected logic value from the 8 pins of PORTD and 2 pins (RB7 and RB6) of PORTB. Table 5.1 presents the converted results for various input voltages, the percentile of difference and the corresponding duty cycles of PWM signal.

Table 5.1 – ADC testing's results.

Input Voltage (V)	PORTD (RD7-RD0)	PORTB (RB7-RB6)	Decimal Value	Expected Value	Difference (%)	Duty cycle (%)
5	1111 1111	01	1021	1023	0.195	40
2.498	0111 1101	11	503	511	1.566	30
3.98	1100 0111	11	799	814	1.843	35
2.027	0110 0110	11	410	414	0.966	20

The relatively small differences (all are less than 2%) exhibit how accurate the ADC function of the PIC18F4550 micro-controller is. With such tiny mismatches between the expected value and the achieved value, the results from ADC function of PIC18F4550 micro-controller is reliable and ready to be processed.

5.3 Open-loop performance

The open-loop performance is measured by operating the flyback converter without the micro-controller while a driving signal is fed through the MOSFET's gate. Observing the waveform of

the switching transistor's drain voltage and the waveform of driving signal (Fig. 5.4), a conclusion about the system's workability could be drawn. As can be seen from Fig. 5.4, whenever the driving signal (yellow) is high, the drain voltage of the switching transistor (blue) is dropped, which can be interpreted as the switch is being switched on. Fig. 5.5 shows a captured image on the actual converter when the switching transistor is switching with the driving gate signal. The LED load of 240mA, which comprises a matrix of LEDs with 12 columns and 12 rows, is lighted up then. The high-frequency ringing (about 400kHz) after the turn-off of the power MOSFET is due to the large flyback transformer inductance as well as its leakage inductance, the large drain-to-source capacitance of the power MOSFETs, and the light load current of the LED load. Optimization of the snubber circuit components can reduce this high-frequency ringing.

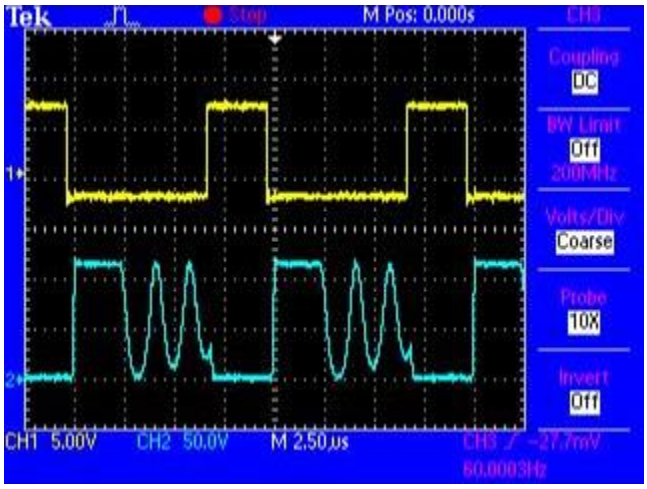


Figure 5.4 – The waveforms of the switching transistor's gate voltage (yellow) and drain voltage (blue). The droppings of the switching transistor's drain voltage are evidences for switching operation.

5.4 Closed-loop performance

With the micro-controller's necessary functionalities were scrutinizingly tested while the open-loop performance of the flyback converter was also reached the design expectation, the full closed-loop converter performance is now examined. Instead of using an external driving signal from a function generator, the PWM function of the PIC18F4550 micro-controller is now the source for switching signal. The feedback is formed with four input signals from the sample of input voltage, the primary-side switching current, the peak current detector and the zero current detector.

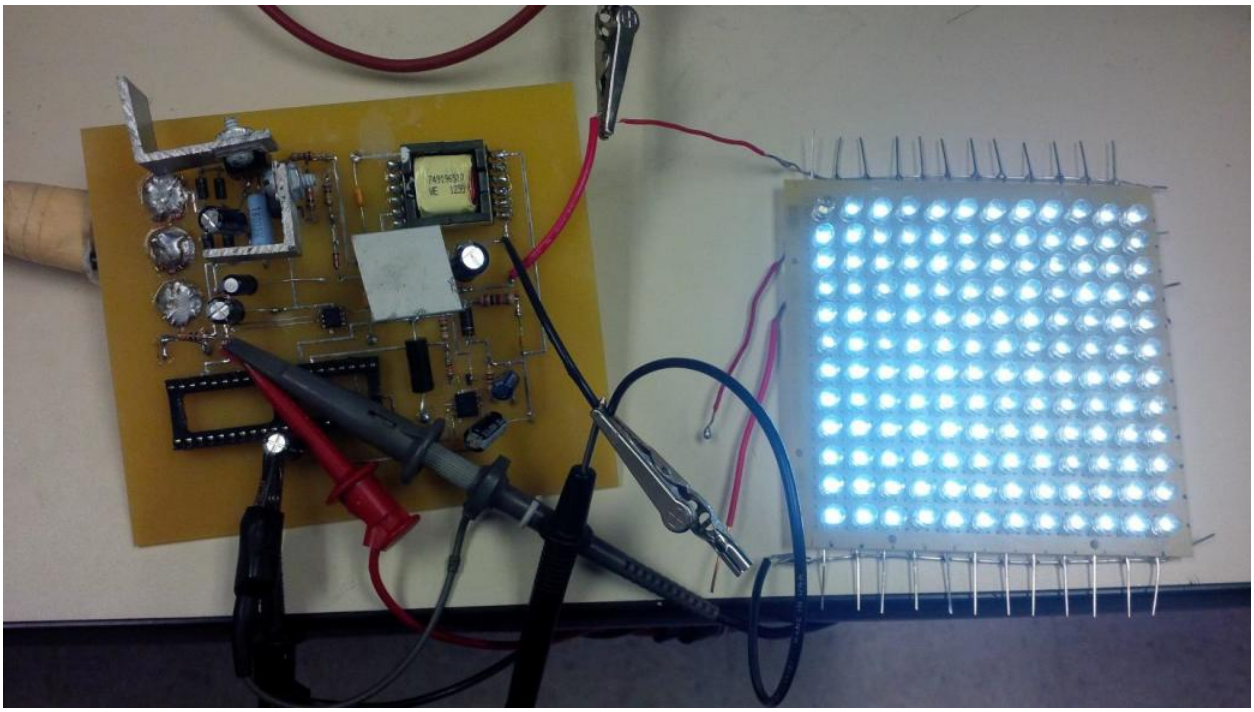


Figure 5.5 – A matrix of LEDs is lighted up by the designed driver working in open-loop mode.

The introduction of the PIC18F4550 micro-controller as a controller for the flyback converter also lighted up the LED load as in Fig. 5.5. Monitoring waveforms of the gate and drain of the switching transistor, an image likes in Fig 5.6 was captured. As can be seen from Fig. 5.6, the switching operation is successful despite some unwanted noise. Again, the high-frequency

ringing after turning-off of the power MOSFET originated from the transformer leakage inductance and the drain-to-source capacitance of the power MOSFET. The dissipative snubber circuit can be redesigned to mitigate this problem.

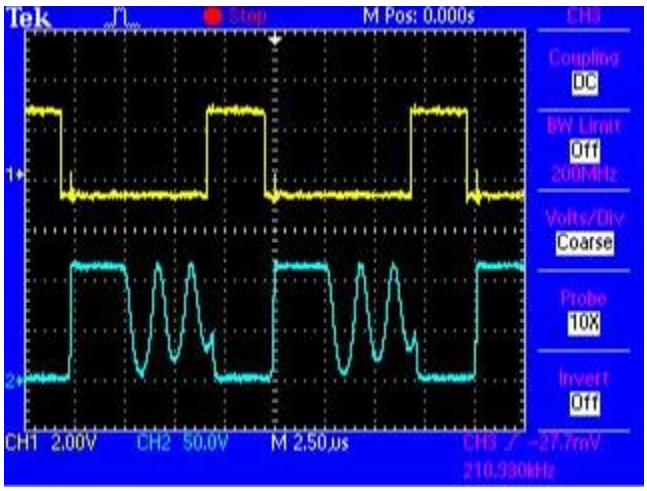


Figure 5.6 – Waveforms of switching transistor's gate (yellow) and drain (blue) in closed-loop mode.

Despite the introduction of some problem: ringing after switching off of the power MOSFET, noise, spikes etc., the flyback converter worked perfectly as the intended design. The combination of performances from the PIC18F4550 micro-controller and the open-loop flyback converter turned out to the performance of the full closed-loop converter as expected.

Chapter 6

Conclusions

6.1 Conclusion

The micro-controller based primary-side sensing flyback converter for LED driver was designed, simulated and implemented successfully. First, the simulation demonstrated the feasibility of the intended design by mimicking all necessary characteristics of the PIC18F4550 micro-controller that includes PWM and counter. The absence of a compatible model for PIC18F4550 micro-controller in simulation was completely compensated by using a PID based control scheme in companion with analog behavioral modelling blocks. Simulation results were matched well with the preliminary calculations. Then, a prototype board of the driver was designed and fabricated. Due to testing and verification only, the prototype PCB board's size was not restricted as well as optimized. On the next step, the micro-controller was programmed in C programming language. Before deploying the micro-controller on the board for observing the closed-loop performance, key features of the micro-controller were carefully checked. This process also helps to detect bugs and debug the programmed code. After demonstrating the micro-controller's ability to properly conduct ADC and PWM functions, the next task was investigating the open-loop

performance of the flyback converter. The successful testing results pointed out that the prototype board was ready for the closed-loop full converter operation. Because both the test on the micro-controller and the open-loop system gave appropriate results, the closed-loop converter's performance is predictably good.

6.2 Future works

The driver in this project was designed with work-oriented purpose only and has not been optimized yet. The next mission is to reduce the board size by replacing some through-hole devices (THDs) by surface-mounted devices (SMDs). The layout of the board can also be changed so that components could be deployed on its both sides. This new layout promised to dramatically decrease the board area, a target that this project has not accomplished. The dissipative snubber circuit should be also redesigned in order to minimize the ringing at switching offs.

The PIC18F4550 micro-controller in this project used its internal oscillator as a clock source. This 8 MHz clock source somehow limited the working efficiency since there are four ADC tasks needed to be processed. In addition, the operating frequency of the micro-controller is $F_{OSC}/4$, or 2 MHz, that is not a significant number compared to the switching frequency of 100 kHz. This is the reason why the adjusting step of PWM was only 5%. If an external oscillator with frequency up to 48MHz is equipped, the PWM adjustment should be smoother, and the ADCs tasks could work faster, therefore will improve the precision of the feedback.

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