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Design, Layout, and Testing of a Silicon Carbide-based Under Voltage Lock-out Circuit

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**DESIGN, LAYOUT, AND TESTING OF A
SILICON CARBIDE-BASED UNDER VOLTAGE LOCK-OUT CIRCUIT**

DESIGN, LAYOUT, AND TESTING OF A
SILICON CARBIDE-BASED UNDER VOLTAGE LOCK-OUT CIRCUIT

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Electrical Engineering

By

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ABSTRACT

Silicon carbide-based power devices play an increasingly important role in modern power conversion systems. Finding a means to reduce the size and complexity of these systems by even incremental amounts can have a significant impact on cost and reliability. One approach to achieving this goal is the die-level integration of gate driver circuitry with the SiC power devices. Aside from cost reductions, there are significant advantages to the integration of the gate driver circuits with the power devices. By integrating the gate driver circuitry with the power devices, the parasitic inductances traditionally seen between the gate driver and the switching devices can be significantly reduced, allowing faster switching speeds, which in turn leads to higher efficiencies, less aggressive thermal management requirements, and physically smaller passives.

Collaborators from Toyota, Cree, the University of Arkansas, Oak Ridge National Labs, and Arkansas Power Electronics International have designed, fabricated, and tested a custom gate driver circuit implemented in a low-voltage SiC-based process by Cree. This gate driver implementation is the first step toward the goal of a completely integrated system. One key sub-component of this gate driver is the Under Voltage Lock-Out (UVLO) circuit, which asserts a signal whenever the supply voltage to the die falls below a set threshold and allows circuitry both on- and off-chip to take steps to prevent damage to the system. The work presented herein is the design, layout, and testing of a UVLO circuit implemented in the low-voltage silicon carbide process available from Cree. The UVLO was demonstrated to operate over a temperature range between $-55\text{ }^{\circ}\text{C}$ and $300\text{ }^{\circ}\text{C}$. An overview of the gate driver design, the fabrication process, and the trade-offs made during the UVLO circuit design process will be

presented, as well as the integrated circuit layout workflow. A synopsis of the die testing apparatus and results will also be provided.

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Michael Dalan Glover

DEDICATION

Dedicated to my wife Starlet, who has demonstrated more patience than I probably deserve, and to my two sons Evan and Nathan, who haven't seen much of Daddy for the last few years.

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TABLE OF ACRONYMS

ADE	Cadence Analog Design Environment
AFG	Arbitrary Function Generator
APEI	Arkansas Power Electronics International
API	Application Programming Interface
ARPA-E	Advanced Research Projects Agency - Energy
CMOS	Complementary Metal Oxide Semiconductors
CMP	Chemical Mechanical Polishing
CQFP	Ceramic Quad Flat Pack
CSV	Comma-Separated Values (CSV) file
CTAT	Complementary To Absolute Temperature
CVS	Concurrent Versioning System
DBC	Direct-Bond Copper
DMM	Digital Multi-Meter
DRC	Design Rule Checking
DSP	Digital Signal Processor
DUT	Device Under Test
EHPs	Electron-Hole pairs
ESD	Electrostatic Discharge
GDSII	Graphic Database System
GPIB	General Purpose Interface Bus
HSPICE	Synopsys Hierarchical SPICE simulator

JFET	Junction Field Effect Transistor
KVL	Kirchhoff's Voltage Law
LASI	Layout System for Individuals
MIC	Mobile Ion Contaminate
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor
ORNL	Oak Ridge National Labs
PAP	Plasma-Assisted Polishing
PCB	Printed Circuit Board
PDK	Process Development Kit
PHEV	Plug-in Hybrid Electric Vehicle
PMOS	P-type Metal Oxide Semiconductor
PSG	Phosphosilicate Glass
RIE	Reactive Ion Etching
TLM	Transmission Line Model
UA	University of Arkansas
UPS	Uninterruptable Power Supply
USB	Universal Serial Bus
UVLO	Under Voltage Lock-Out

CHAPTER 1 – INTRODUCTION

The potential impact of silicon carbide (SiC) on the landscape of high-temperature power applications is significant and has been anticipated for decades. William Shockley, an early pioneer in the field of silicon-based semiconductor devices, noted as early as 1960 that silicon carbide (SiC) held key traits that make it desirable for use in high temperature applications [1]. These desirable traits, including the potential for operation at higher temperatures and higher switching speeds than can be accomplished with silicon, continue to drive silicon carbide researchers towards breakthroughs that are hoped will result in improved performance for high power energy conversion applications.

The work presented herein is the design, layout, and testing of a silicon carbide-based under voltage lock-out (UVLO) circuit. Acting as a sub-circuit of a gate driver topology, the UVLO is used to monitor a critical power rail in a system and to assert a signal whenever the voltage on the supply has fallen below some preset threshold. This allows the system controller or the driver itself to take action to prevent system damage that might occur due to the drooping supply rail.

While UVLO circuits are commonly used in many electronic designs, none could be found in the literature that could potentially be integrated (along with the remainder of the gate driver circuitry) into the same SiC substrate as the power MOSFET. Thus, the work presented is the first demonstration of this type of circuit in a process which is compatible with power MOSFET integration.

A brief overview of silicon carbide will first be presented, followed by a comparison of SiC traits with those of silicon. Following this, an overview of the gate driver project will be presented. Finally, a discussion of each fabrication run will be presented wherein the trade-offs and approaches for design, layout, and testing of the investigated UVLO topologies will be given. In addition to the UVLO, some attention will be given to the design and layout of a temperature sensor, since it also provides some useful insights into the temperature dependencies of the process. Another set of auxiliary test structures, used for characterization of resistors and contact resistance within the process, will also be discussed. Finally, conclusions that can be drawn from the work will be presented.

CHAPTER 2 – BACKGROUND

This chapter provides background information on silicon carbide, an overview of the collaborative project and processes for which the UVLO was designed, and a description of the role that the UVLO circuit plays in the gate driver system.

2.1 Silicon Carbide

Silicon carbide (SiC) is a wide-bandgap semiconductor that displays a number of desirable characteristics that make it well suited for use in power conversion systems. While the potential advantages of SiC were noted as far back as the 1950s [2] and the first SiC MOSFETs were reported in the late 1980s [3], single-crystal wafers have only been available commercially since 1991. The commercial SiC power devices that can be purchased today are available due to the gradual advancements made in the processing of SiC that have been realized since the early 1990s. In spite of improvements made over this time, some issues (such as “micropipes”) have not been completely eliminated and still present issues for device reliability [4].

Silicon carbide exhibits a hexagonal crystal structure, the asymmetry of which causes properties such as carrier mobility and electron saturation velocity to be anisotropic [3]. Silicon carbide can exist in any one of approximately 200 polytypes that are identified by the stacking sequence of tetrahedral layers in the lattice structure [2]. The most common polytypes used for device fabrication are 6H and 4H. Although the properties of silicon carbide vary by polytype, the 6H and 4H structures exhibit a number of properties that surpass those of silicon, including a thermal conductivity that is 2.5 times that of silicon and a breakdown voltage that is 10 times that of silicon [2]. Other properties such as carrier mobility are lower than that of silicon,

although the electron mobility of silicon carbide ($1000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) is still relatively close to that of silicon ($1400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$).

One important characteristic is the ability of silicon carbide devices to operate at much higher operating temperatures as compared to silicon. Due to the larger bandgap of SiC as compared to Si (3.26 [5] and 1.12, respectively), higher temperatures can be reached before the intrinsic carrier concentration (n_i) reaches a level where it dominates the doping level intentionally introduced into the substrate, rendering the device inoperative [6].

One aspect of the 4H polytype that makes it attractive for low voltage circuits is the fact that anisotropy for electron mobility (i.e., the ratio of mobility for carriers traveling in the perpendicular and transverse directions) is approximately 0.7, whereas the 6H polytype exhibits a ratio of 6 [7]. Put simply, this means that the mobility of electrons moving through the lattice in the 4H polytype is reasonably independent of the direction of flow in the lattice when compared to the 6H polytype. Since an isotropic mobility would seem to be generally preferred for the design of logic gates to better accommodate the packing of transistors into the space available, this would tend to indicate a preference for the 4H polytype for CMOS-based designs. However, as will be seen in a later section, hole mobility is considerably lower than electron mobility in 4H SiC and, as a result, 6H has traditionally been used for CMOS-based designs.

While exhibiting a lesser degree of anisotropy, 4H SiC also demonstrates an electron mobility that is higher than that of the 6H polytype, a desirable trait that impacts device characteristics such as output gain and on-state resistance (R_{on}) [2]. The Cree process being used is based on 4H-SiC; thus, the 4H polytype will be the primary focus of further discussion.

2.2 SiC Processing

In order to build usable devices, a candidate material must be compatible with certain key processes. These processes include doping, etching, and oxide growth. Doping in silicon carbide is typically accomplished either through epitaxial layer growth or by ion implantation, since the temperatures required for diffusion are greater than 1800 °C [2]. In the case of epitaxial growth, the epitaxial layer is doped during deposition, yielding a well-controlled doping profile. For the ion implantation process, it is necessary to anneal the substrate after deposition at temperatures on the order of 1650 °C in order to repair damage to the SiC lattice [8].

As with silicon, the native oxide for SiC is silicon dioxide [4]; in fact, SiC is the only wide bandgap material on which it is possible to grow a thermal oxide [9]. There are, however, a number of issues that arise when SiO₂ is grown on the SiC surface, including the tendency for interface state densities (D_{it}) to occur at the SiO₂/SiC interface which are on the order of 10 times higher than those found in Si [10]. These higher interface state densities and carrier traps that occur at the interface can have an impact on the threshold voltage of the device and increase the $R_{DS(ON)}$ of the device [9]. The most common dopants for SiC are nitrogen and aluminum [2]. Undoped SiC is typically found to be weakly n-type due to nitrogen that becomes trapped within the crystal during growth [11].

The etching of SiC can be accomplished using molten salts, such as NaOH-KOH at 350 °C [2]. While not necessary for the Cree process used herein, the fact that this is a somewhat cumbersome process for many researchers illustrates yet another challenge related to the processing of SiC. Ultimately, a considerable number of investigations seeking to simplify this

process have led to the successful patterning of SiC using dry etching techniques such as Reactive Ion Etching (RIE) [2].

2.3 SiC versus Si

A comparison of properties between 4H-Si and SiC can be seen in Table 1. As has been previously mentioned, the bandgap for 4H-SiC is nearly three times that of Si, a trait that allows SiC-based devices to operate at higher temperatures. The bandgap energy E_g represents the energy required for a valence electron in the material to break free to become a conduction electron [12]. Depending on the doping levels, thermally generated electron-hole pairs (EHPs) in a typical silicon-based device begin to overwhelm the extrinsic carriers at temperatures between 225 °C and 400 °C [13]. By contrast, 6H-SiC-based JFET circuits have been demonstrated operating near 600 °C [14]. A larger bandgap directly correlates to operation at higher temperatures, since more energy (and, therefore, a higher temperature) is required to generate enough EHPs to mask the carriers introduced through doping of the semiconductor.

TABLE 1. COMPARISON OF SILICON CARBIDE AND SILICON PROPERTIES [2]

Property [Symbol]	Units	4H-Silicon Carbide	Silicon
Bandgap energy [E_g]	eV	3.26	1.12
Thermal conductivity [Θ_K]	$W\ cm^{-1}\ K^{-1}$	3.7	1.5
Intrinsic carrier density @ 300K [η_i]	cm^{-3}	5×10^{-9}	1×10^{10}
Electron mobility [μ_e]	$cm^2\ V^{-1}\ s^{-1}$	1000	1400
Hole mobility [μ_h]	$cm^2\ V^{-1}\ s^{-1}$	115	471

Since the bandgap of SiC is larger than that of silicon, it also follows that a higher electric field potential is necessary to invert the channel in a device. This follows intuitively from an understanding that if the bandgap of SiC is three times larger than that of SiC, then

three times more energy must be required in order to invert the channel. The formula for the depth of the depletion region (W) and the electric field (E) across the depletion region is shown in Eqs. (2.1) and (2.2), respectively [12].

$$W = \sqrt{\frac{2\epsilon_s\phi_s}{qN_A}} \quad (2.1)$$

$$E = -\frac{qN_AW}{\epsilon_s} \quad (2.2)$$

Where ϵ_s is the dielectric constant of the substrate material, ϕ_s is the energy required for strong inversion in the channel in electron volts, q is the charge on an electron, and N_A is the hole concentration in cm^{-3} . After substituting Eq. (2.1) into Eq. (2.2) and solving for a ratio of E_{SiC}/E_{Si} , the expression becomes:

$$\frac{E_{SiC}}{E_{Si}} = \sqrt{\frac{\epsilon_{sSi}\phi_{sSiC}}{\epsilon_{sSiC}\phi_{sSi}}} \quad (2.3)$$

Substituting actual values into Eq. (2.3), it is found that the electric field in SiC is approximately 1.9 times higher than that in Si [15].

This higher intensity electric field has several undesirable side effects. The higher field strength causes an increase in scattering due to mechanisms such as surface roughness mobility, and can cause stress issues with the gate oxide that can lead to reliability issues [15]. Since the quality of the SiC/SiO₂ interface impacts device operation, there has been considerable effort by researchers to reduce charge trapping and to address the “dangling” Si and C bonds that occur at the surface of the SiC wafer. To address the traps at the interface, researchers have investigated the nitridation of the interface to reduce hole trapping [9] and other techniques such as high temperature hydrogen annealing [10]. An interface surface void of discontinuities is obviously desirable; therefore, a process such as Chemical Mechanical Polishing (CMP) is used to treat the surface of SiC wafers prior to processing. However, CMP still leaves subsurface damage in

the SiC lattice. New surface processing approaches, such as Plasma-Assisted Polishing (PAP), are able to yield an atomically flat surface and show considerable promise as an alternative to CMP [16].

As applied to power devices, the higher thermal conductivity of 4H-SiC is desirable, as it means that heat can be conducted away from the active regions of the substrate in a SiC-based device more efficiently than in a Si-based device. The electron mobility of SiC (μ_e) is approximately 70% that of Si. This property impacts a number of device characteristics, including transconductance (g_m), on-state resistance ($R_{DS(ON)}$), and output gain. The formula for the drain current of a MOSFET (I_d) in saturation is shown in Eq. (2.4), where μ_n is electron mobility in $\text{cm}^2/\text{V}\cdot\text{s}$, C_{ox} is capacitance of the gate in F/cm^2 , W/L is the width/length ratio of the channel, V_{GS} is the gate-to-source voltage of the MOSFET, and V_T is the threshold voltage of the MOSFET. Here it is apparent that the carrier mobility (μ_n) has a linear impact on the drain current for the given V_{GS} , and likewise on the transconductance (g_m) of the device since $g_m = I_D/V_G$.

$$I_d = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right) (V_{GS} - V_T)^2 \quad (2.4)$$

In contrast, hole mobility (μ_h) in 4H-SiC is about one-tenth less than electron mobility (μ_e). As a consequence, p-channel devices exhibit a significantly larger on-state resistance than the n-channel devices. This fact explains why CMOS-based SiC circuits are often implemented in 6H-SiC [6], [17], where the ratio μ_e/μ_h is approximately 4:1 and more closely matches that of Si.

In the NMOS Cree process, devices do not exhibit a positive temperature coefficient for $R_{DS(ON)}$ overall as would be seen in silicon-based devices [18]. In 4H-SiC, there are two dominant mechanisms at play: reduction in mobility caused by phonon scattering (the cause for

a positive temperature coefficient in silicon), and the effect of surface traps on carrier mobility (caused by Coulomb scattering) in the channel of the MOSFETs [19]. At room temperature, carrier mobility in 4H devices is significantly hampered by Coulomb scattering of carriers by traps resulting from defects at the SiC-SiO₂ interface. However, as temperature increases, these traps become less efficient at trapping and holding carriers and the resulting increase in mobility dominates over the reduction in mobility due to carrier scattering up to a temperatures near 200 °C [19].

2.4 ARPA-E Gate Driver Overview

The ultimate goal of the work started by the collaboration team was to realize an integrated, single-chip solution in the Cree SiC process for the power devices and associated gate driver circuitry that were targeted for use in a Toyota Prius charging system. The effort to fabricate a silicon carbide-based gate driver circuit was the first step towards these fully integrated systems.

It is important to note that, while other researchers have successfully fabricated SiC-based gate driver circuits before [17], there have been no previously reported efforts to fabricate gate driver circuits that could potentially be integrated into the same substrate as the power devices. Previous efforts in the literature used a 6H-SiC CMOS process that would be incompatible with the process needed to allow integration with existing power device processes, such as those used at Cree. Since complete integration was a primary goal, it was necessary to use a process compatible with the existing Cree power device process. While various processing experiments were performed using both epitaxial and implant processing techniques, this meant (as will be seen in a section to follow) that ultimately an NMOS process using only

enhancement-mode devices and resistors was necessary in order to be compatible with project goals.

A block-level diagram of the silicon carbide-based gate driver is shown in Fig. 1 with the UVLO circuit block highlighted. The principal components of the gate driver are the Gate Drive Buffer, the Fault Protection circuits, the Isolation circuits, and the logic gates needed to tie all functions together.

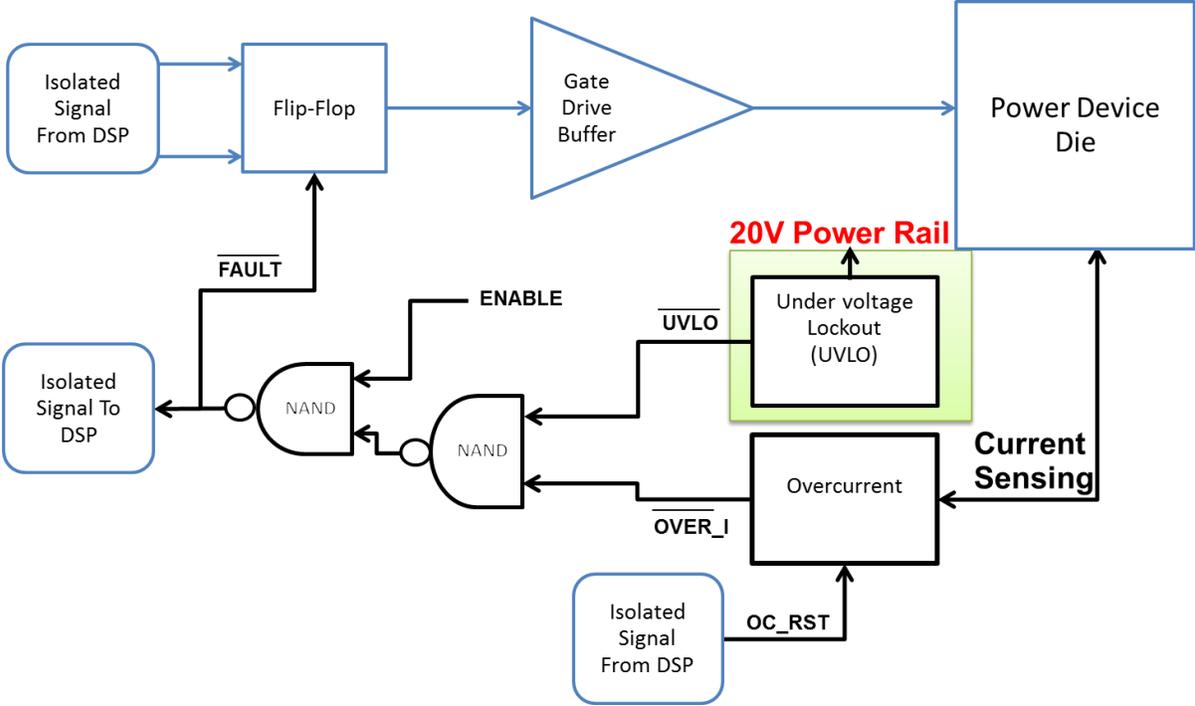


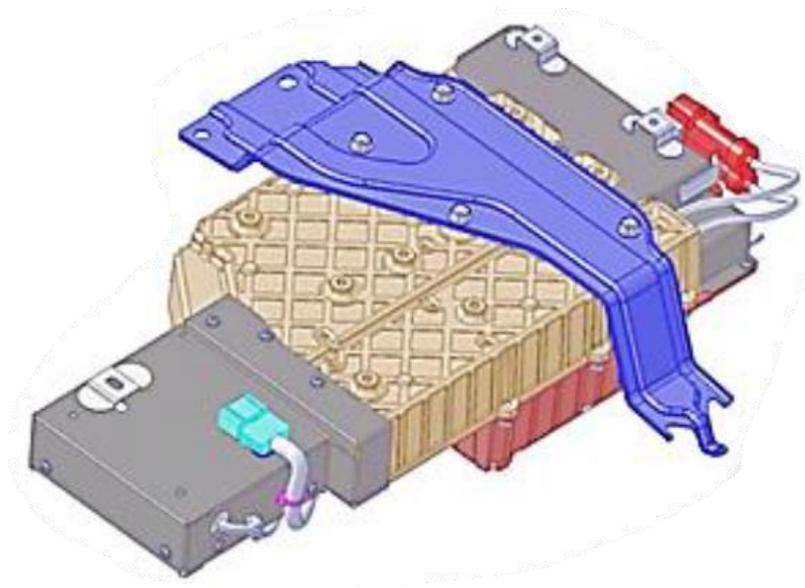
Fig. 1. SiC gate driver block diagram.

In order to provide device and system protection, the gate driver must have fault protection circuits to indicate when events such supply voltage sag or excessive current draw are occurring. The UVLO circuit addresses the issue of supply voltage sag by alerting the system whenever the supply voltage (or some other monitored voltage) has fallen below a

preset limit. A more detailed overview of UVLO circuit operation will be discussed in a later section.

2.4.1 Cost Analysis

The current charger system used in the current Toyota Prius Plug-in Hybrid Electric Vehicle (PHEV) is shown in Fig. 2. The system is roughly 387.5 in³ in volume and is stowed below the passenger seat in the car. The targeted size for the charger system being developed is 52 in³, thus it would require only one-sixth the volume of the current design [20]. In addition, the mass of the current charger is 6.6 kg, whereas the targeted weight of the new charger is approximately 1.2 kg, representing a weight reduction of more than 80%.



**Fig. 2. The 1 kW silicon-based charger used in the current Toyota PHEV [20].
Image courtesy of APEL.**

When attempting to project the potential savings realized by using the integrated driver, there are some cost details about current models (such as the cost of cooling systems) that make exacting figures for analysis a challenge at best. However, based strictly on the cost of the

charging system itself, it is possible to gain some insight into the impact of gate driver integration.

The values in Table 2 are derived from a project presentation given by Arkansas Power Electronics International, Inc. (APEI) in September 2012 [20]. These figures show an estimated cost of approximately \$400 per kW for the charging system in the current PHEV. The United States Department of Energy roadmap targets \$60 per kW and \$50 per kW for 2015 and 2020, respectively, for an onboard DC/DC converter that can be used to power car accessories [21]. These figures were used for cost analysis because the roadmap does not specifically mention a target for charging systems and because the core operation of the device is similar.

TABLE 2. ESTIMATED MANUFACTURING COSTS FOR CURRENT CHARGING SYSTEMS

Charger	Estimated Manufacturing Cost	Peak Power	Cost per kW
Current Si-based PHEV	\$407	1 kW	\$407

The pie chart in Fig. 3 shows the estimated cost of components (as a percentage of total cost) in the Toyota Prius PHEV charging system. Here, the cost of the gate drive as a percentage of total cost is found to be 10%, while the cost of the power switches comes in at 16%. For comparison, the pie chart in Fig. 4 shows the estimated cost of components in the silicon carbide PHEV charging system. In this figure, the cost of the gate drive is shown as zero, since it has been integrated with the power switches. While the resulting integrated power switches are shown to be approximately 26% of the total cost of the module, it is also noted that the cost of the heat sink and labor/assembly components as a percentage of total cost has been reduced.

Component as % of Total Cost (Toyota Prius PHEV Charger)

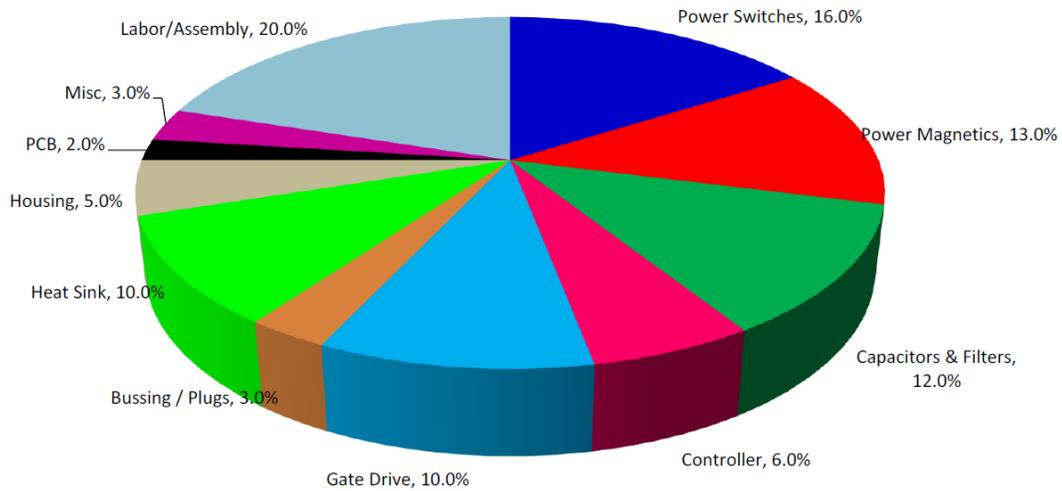


Fig. 3. Pie chart showing the estimated cost of components in the Toyota Prius PHEV charger [20]. Image courtesy of APEI.

Component as % of Total Cost (PHEV SiC Charger)

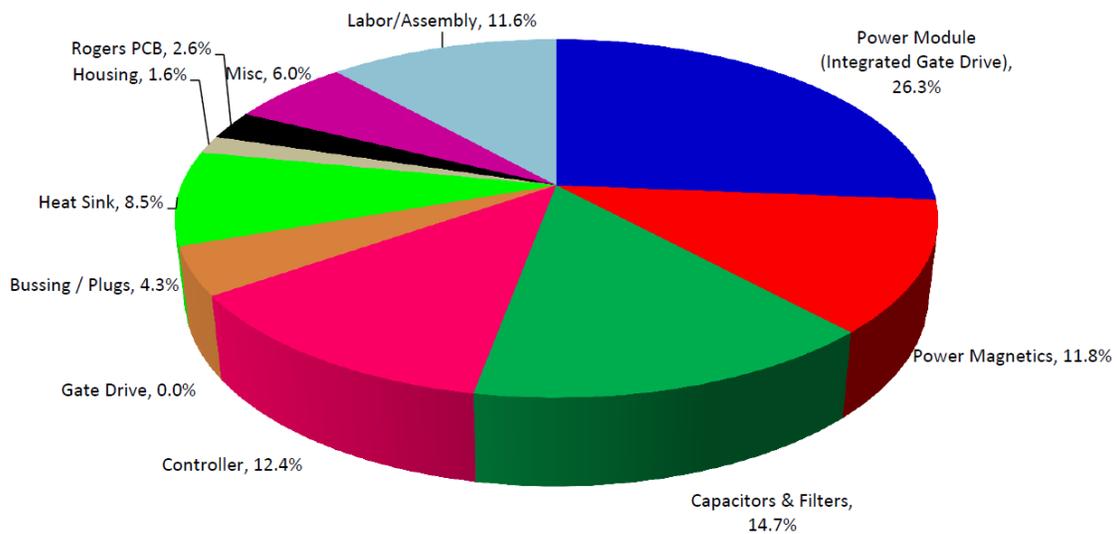


Fig. 4. Pie chart showing the estimated cost of components in a SiC PHEV charger [20]. Image courtesy of APEI.

While it is important to note that the savings realized are due to a number of factors, such as the selection of magnetics and less costly electronic packaging approaches, the integration of the gate driver circuits with the power devices does contribute to a reduction in size of the system. Using the gate driver integration allows for the aforementioned target of \$60 per kW in 2017 and assuming a 1 kW charger is needed, the cost of the charger would be \$60 as compared to the \$400 charger in use today. Assuming 100,000 units would be needed, the cost savings would be \$34M in 2017.

It is important to understand that the assumptions that are in-place for this final figure represent only one possible scenario, and that the ultimate impact on the overall cost of the vehicle is difficult to gauge without more extensive knowledge of the other vehicle systems affected. However, it seems reasonable to say that the performance gained by integration of the gate driver circuits with the power MOSFETs and by the use of novel electronic packaging approaches plays a key role in the redesign of the charger system that should ultimately result in an overall cost savings for the vehicle manufacturer.

2.5 Cree Silicon Carbide Process

A cross sectional view of one approach to the integrated Cree SiC process is shown in Fig. 5. In the figure, the structure for both the low voltage NMOS process and a typical power MOSFET is shown on the left and right sides of the figure, respectively. Since the power MOSFET is a vertical device and symmetric about the gate, only one half of its structure is shown.

As mentioned previously, there are two ways in which the p-wells can be created in the structure. For this project, both epitaxial and implant versions were fabricated for each run of wafers containing low voltage NMOS devices. Other parameters, such as the amount of p-

doping, were also varied between wafers on the first runs to provide a wider spread for characterization [18]. It is important to note that the Cree power MOSFETs are fabricated using an implant process. This means that the implant process is the only processing option for low voltage circuits that truly allow integration with the power MOSFETs. However, overall experience with the wafers fabricated during the project indicated that the epitaxial process tended to have higher yields. In addition, while these are two separate processes it is possible that process parameters (e.g., threshold voltage) in the epitaxial process could be duplicated in the implant process. Therefore, while circuits fabricated in the epitaxial process cannot be directly integrated with the power MOSFETs, successful demonstration of a circuit in the epitaxial process is sufficient to conclude that it would function in the integration-compatible implant process as well.

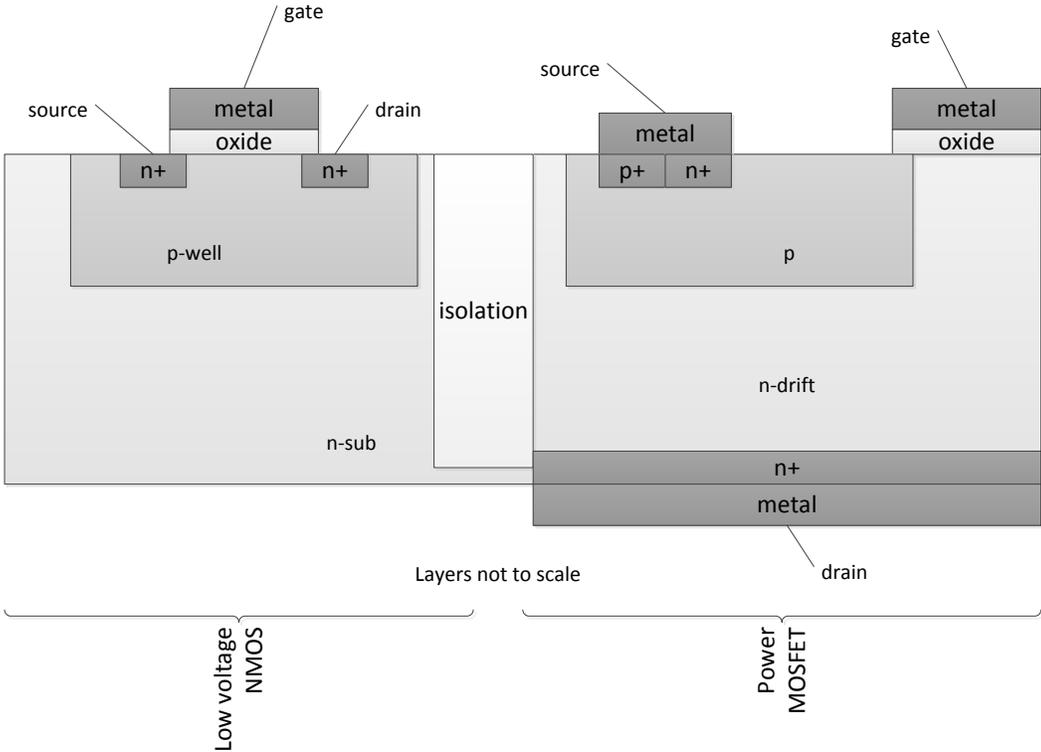


Fig. 5. Cross sectional view of the Cree SiC process.

2.5.1 Overview of Fabrication Runs

There were three fabrication runs made by Cree for this project. A synopsis of these runs can be seen in Table 3. As mentioned previously, wafers were fabricated using both epitaxial and implant processes, although not all circuits were fabricated using both approaches. The first run of wafers (“Characterization Run #1”) was a 7 mm x 7 mm test coupon that contained test structures to allow characterization of the devices and the extraction of parameters so that models could be developed for simulation [18]. Since the second and third runs, labeled here as “Fabrication Run #1” and “Fabrication Run #2”, respectively, were the only ones to contain actual circuits, these will be the focus moving forward.

Since the UVLO was included in the cells used for the latter two runs that were focused on circuit fabrication and testing rather than device characterization, Fabrication Run One will hereafter be referred to as the first fabrication run, while Fabrication Run Two will be referred to as the second fabrication run. Thus, while somewhat confusing, it is important to establish that while there were three *wafers* runs, the latter two will be referred to as the first *fabrication* run one and the second *fabrication* run throughout the remainder of discussion herein.

TABLE 3. WAFER FABRICATION RUNS FOR THE PROJECT

	Tape-out Date	Delivery Date	Description
Characterization Run #1	11/23/2010	March 2011	Test structures for device model development
Fabrication Run #1	11/17/2011	February 2012	First run of devices without full temperature models for resistors available; n-type depletion and enhancement devices available
Fabrication Run #2	9/23/2012	December 2012 / January 2012	Full temperature models used; only n-type enhancement devices available

While not originally on the project schedule, the second fabrication run taped out in September 2012 was deemed necessary in order to prove out new design topologies and to give circuit designers the opportunity to re-spin their designs with the more up-to-date device models and Process Development Kit (PDK) that were developed after Fabrication Run One. It also was intended to allow the design teams to focus on the original task of building a gate buffer circuit in the implant process to allow integration with the power devices. Therefore, it was originally decided to use only implant devices for Fabrication Run Two, since this was the only process compatible with power device integration. However, wafers were ultimately fabricated in Fabrication Run Two using the epitaxial process also, since the epitaxial wafers had proven to be the only wafers that functioned in the first run and the proving of new design topologies was also considered critical by the team, even if the epitaxial version could not be directly integrated with a power MOSFET.

A synopsis of the key differences between the implant and epitaxial processes is shown in Table 4. Resistors made of both polysilicon and diffused SiC were available in the PDK. It was originally assumed that both epitaxial and implant versions of all circuits would need to be delivered for Fabrication Run Two; thus, the size of the resistors in each circuit had to be adjusted as necessary to accommodate the sheet resistance afforded by each process for each type of resistor. Due to concerns with gate-source breakdown, Cree felt it necessary to de-rate the gate-source voltage of the implant devices to 16 V or less. As will be seen in the design section for Fabrication Run Two, these differences between the two processes also meant that the resistors in the UVLO front end had to be adjusted for each version of the design.

TABLE 4. COMPARISON OF IMPLANT AND EPITAXIAL PROCESSES

	Epitaxial Process	Implant Process
Operating voltage	20 V	16 V
Sheet resistance for Diffusion resistor	115 Ω/\square	213 Ω/\square
Sheet resistance for Polysilicon resistor	119 Ω/\square	145 Ω/\square
Temperature coefficient for Diffusion resistor	770 ppm/ $^{\circ}\text{C}$	1460 ppm/ $^{\circ}\text{C}$
Temperature coefficient for Polysilicon resistor	880 ppm/ $^{\circ}\text{C}$	730 ppm/ $^{\circ}\text{C}$

2.5.2 Challenges

The intention to integrate the low voltage circuits and power devices limited the process in many respects. For the first fabrication run, one limitation of the Cree process was that only NMOS enhancement and depletion devices were available; no PMOS devices were available in the process because no isolation wells could be made in the process. A further complication was that there were no diodes available in the process, which meant that it was not possible to implement circuit topologies such as bandgap references or electrostatic discharge (ESD) protection.

Since no wells were available, there was no isolation between the NMOS devices and the substrate. Therefore, the source-body voltage (V_{sb}) could not be assumed to be zero as in many modern processes; this meant that the threshold voltage of devices could vary depending on the voltage present at the source terminal.

The threshold voltage for a MOSFET with $V_{SB}=0$ (V_{t0}) is given by Eq. (2.5), where ϕ_{ms} is the work function difference between the gate metal and the semiconductor in eV, ϕ_f is the energy needed to invert the channel in eV, C_{ox} is the gate oxide capacitance in F/m, and Q_{ss} is the positive charge density at the oxide-silicon interface (caused by defects) in Coulombs.

$$V_{T0} = \phi_{ms} + 2\phi_f + \frac{Q_b}{C_{ox}} - \frac{Q_{ss}}{C_{ox}} \quad (2.5)$$

$$V_T = V_{T0} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}) \quad (2.6)$$

$$\gamma = \frac{1}{C_{ox}} \sqrt{2q\epsilon N_A} \quad (2.7)$$

The more general formula for threshold voltage (V_T) is given in Eq. (2.6), where V_{SB} is the source-body voltage for the MOSFET in volts and the parameter γ is defined as shown in Eq. (2.7), where q is the electron charge in coulombs, ϵ is the permittivity of the substrate, and N_A is the hole concentration of the of the substrate in atoms/cm³ [22]. In a typical CMOS process, devices are fabricated inside wells in order to allow the fabrication of n- and p-channel devices with similar threshold voltages on the same substrate [12]. This also allows the source contact for each device to be tied to the well in which the device is placed, effectively making the source-body voltage (V_{SB}) equal to zero for all devices. For this scenario, the terms on the right side of Eq. (2.6) cancel and the threshold voltage is dependent only on process parameters (which are carefully controlled).

In the process used for this project there were no wells to provide isolation between devices, so the body connection of all devices was effectively tied to ground. Thus, for devices where the source terminal was connected to ground in the circuit, the parameter γ was still effectively zero. However, for devices where the source terminal voltage could vary during circuit operation, the parameter γ was not zero and the threshold voltage increased as the body voltage was increased.

A simplified example of how the body effect impacts a circuit can be shown using the simple inverter structure in Fig. 6. Here, the body connection for M2 is tied internally to the same potential as the source for M2. Therefore, M2 will exhibit no body effect and the threshold voltage for M2 (V_{t2}) will remain constant during operation. For M1, however, the voltage at the output will vary between approximately $V_{DD}-V_{t1}$ (when M2 is turned off) to V_{DSSat2} (when M2 is turned on). Thus, V_{t1} will vary during circuit operation. In the case of this circuit, it is desirable to have V_{OUT} as high as possible so that the signal will not degrade as it passes through subsequent logic gates. However, any circuit changes made to increase V_{OUT} also cause a corresponding increase in V_{t1} , which counteracts the goal of increasing V_{OUT} . While the designer can anticipate the impact that the body effect has on a circuit, it is often desirable to choose circuit topologies that avoid the issue altogether. In this example, if the pull-up device M1 was replaced with an appropriately sized resistor, the issue could be avoided. Based on the characterization of devices in the first run, the threshold voltage (V_T) for a 32 x 2 enhancement mode device at 25 °C was found to vary from approximately 3.4 V ($V_{SB}=0$) to 7.3 V ($V_{SB}=15$ V) [23].

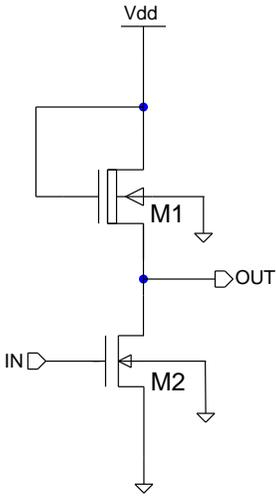


Fig. 6. Simple NMOS-based inverter with active load.

Another process limitation was the availability of only one metal layer available for signal routing in the process. This required the polysilicon layer to be used when it was necessary to cross (under) a metal trace. Unfortunately, the sheet resistance of the polysilicon was anticipated to be relatively high, thus requiring special consideration to minimize parasitic resistance during layout when routing in the polysilicon layer.

During the testing of the initial characterization run, it became clear that there was a process issue when it was discovered that the threshold voltage for devices had shifted lower after the first round of testing. It was later discovered that mobile ion contamination had occurred during fabrication. The impact of these contaminants on semiconductor device reliability and performance was theorized and described in the mid-1960s [24]. One common Mobile Ion Contaminant (MIC) is sodium, which can be introduced into the oxide either from improper handling or via other process materials such as the resist or metal etchant. In the case of improper handling, human body oils or sweat can be the source of contamination.

A diagram that explains the motion of mobile ions within the gate oxide is shown in Fig. 7. Sodium ions are able to easily move through the gate oxide, even at room temperature. Thus, when a positive gate voltage is applied to a device, the cations within the oxide are driven away from the metal gate towards the oxide-substrate interface. Since they are unable to diffuse into the substrate, they collect and form a sheet of positive charge at the interface. This sheet of charge acts like a potential applied to the gate, and tends to push the channel towards inversion. The net result is that the threshold voltage for the device is effectively permanently reduced.

As previously mentioned, organic contamination due to mishandling is only one source of these ions. Other potential sources include the resist used during the photolithography

process and the solution used for wet etching the metal layer. To combat the issue, low-sodium resists and etching techniques have been shown to be effective in reducing contamination [25].

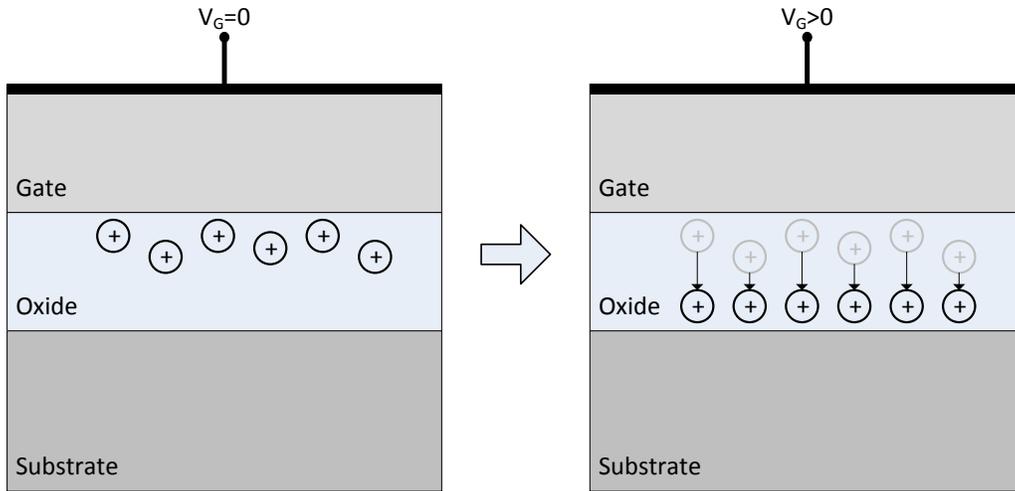


Fig. 7. Mobile ion contamination in MOSFET gate oxide.

Two methods have been used traditionally to control the damage done by mobile ion contaminants. Gettering describes the process used to “get” or trap mobile ion contaminants in the gate oxide of the MOSFET. The first approach uses a layer of phosphosilicate glass (PSG) on the gate oxide to trap the ions. Fig. 8 shows how the PSG is used for this purpose. The PSG layer is relatively thin (on the order of 125 Angstroms), but serves adequately to both getter (i.e., trap) and act as a barrier to Na^+ ions [26]. Another approach to addressing the issue of MICs in the case of silicon-based devices is the use of silicon nitride in the gate, since it acts as a barrier against mobile ions.

For the first fabrication run of the Cree process, the lack of gettering led to enhancement devices that would demonstrate a proper threshold voltage on the first measurement, but would exhibit a threshold near zero for all subsequent measurements. Although Cree agreed to address this issue by introducing gettering in the fabrication run(s) to follow, it presented a challenge for

UA researchers collecting the device data used to generate the simulation models. The impact of this issue and others was worsened further by a compressed project timeline.

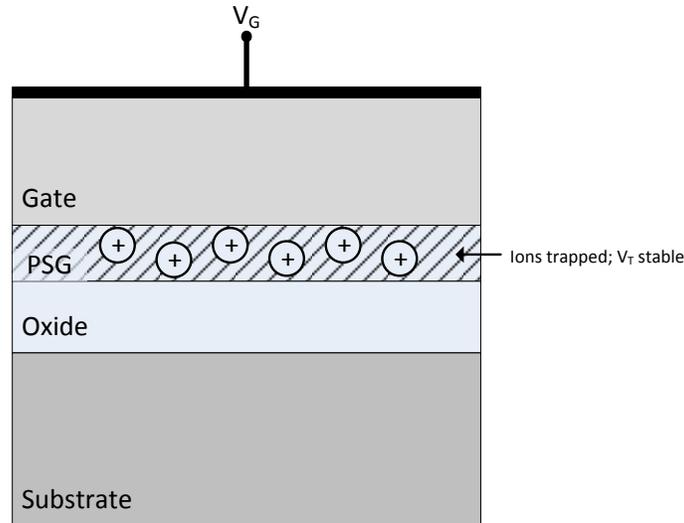


Fig. 8. Phosphosilicate glass (PSG) as a getter.

From a design standpoint, another challenge was the fact that the initial device models created for the process were “binned”, rather than scaled. This meant that devices used for design and simulation had to be chosen from a discrete set of geometries, which limited the selection of devices considerably. The device sizes available in the first fabrication run (for both depletion and enhancement devices) are shown in Table 5.

The number of “fingers” for each device type (effectively, the multiplicity) could be modified to any integer value. It is also important to point out that the device curves for certain devices (the 32x2 devices in particular) were more thoroughly characterized than others, which meant that the simulations for these particular devices were deemed as being more accurate than the others by the team. This fact often played a key role in determining which geometries to use for a given purpose during the design process, and led to a decision to use only 32x2 MOSFETs in the UVLO circuit design included on the second fabrication run.

TABLE 5. DEVICE GEOMETRIES AVAILABLE FOR FABRICATION RUN ONE (W/L)

Device (WxL)
32x2
32x4
8x8
16x8
32x8 (depletion only)

To further complicate time-based pressures, the models that allowed simulation at specific temperatures (25 °C, 125 °C, and 225 °C) were not available until approximately two weeks before the tape out deadline for Fabrication Run One. This meant that a number of last-minute adjustments to the circuits had to be made just before the tape out. In addition, these temperature models did not include temperature coefficients for the resistors used in the process; as will be seen in later discussion, this tended to make the simulated results at elevated temperatures look much better than those actually measured.

When preparing for the second fabrication run, a team decision was initially made to focus only on implant circuits. Since the depletion devices had been demonstrated to exhibit sub-par performance in the implant process and inconsistent performance (leakage) in the epitaxial process, it was decided to use only enhancement-mode devices moving forward. This required all designers to re-spin their designs for Fabrication Run Two to remove all depletion mode devices and replace them (where applicable) with resistor-based pull-ups. Ultimately, however, the collaboration team elected to attempt the fabrication of circuits in both processes.

These process changes were compounded by the fact that the tape out for Fabrication Run Two was previously not planned in the project schedule. In order to yield results in a meaningful time frame, this tape out date was scheduled on an aggressive time scale that left little time for extra exploration of the design space.

Finally, the space available for layout was limited for the second fabrication run because of the number of process variations deemed necessary by the collaboration team. This meant that the circuits for the second fabrication run needed to have a smaller footprint than those in the first run, while at the same time they had to be constructed with the smaller palette of devices available. The consequence of these constraints was the omission of certain circuits that had been on the first tape out in order to provide space for other designs that had risen in priority, one example being the “glue” logic used to tie together the fault logic circuits into one output.

2.6 Under Voltage Lock-Out Description

As previously mentioned, the UVLO asserts a signal to indicate when the supply voltage has fallen below a pre-set threshold and de-asserts this signal when voltage levels have risen sufficiently. As a part of the fault detection system, the UVLO signal was intended to be fed to a series of logic gates that combine the output of the UVLO circuit with that of the over current protection circuit, thus deriving the final FAULT signal. The FAULT signal was then to be monitored by both internal and external circuits to allow action to be taken in the event of a system fault.

The role of a UVLO circuit is to provide a logic-level output that indicates when a monitored voltage has fallen below an acceptable threshold. This output signal is monitored by a system controller, which can then halt activity that could damage other system components or cause other ill effects. UVLO circuits are used in many products, including self-oscillating half-bridge drivers used in lighting ballasts [27], uninterruptable power supplies (UPSs), and within the multiple electrical systems found in hybrid/electric cars [28]. In some commercial products,

such as DC-DC converters, the designer can tailor the switching points of the on-board UVLO circuit to fit the needs of the application at hand [29].

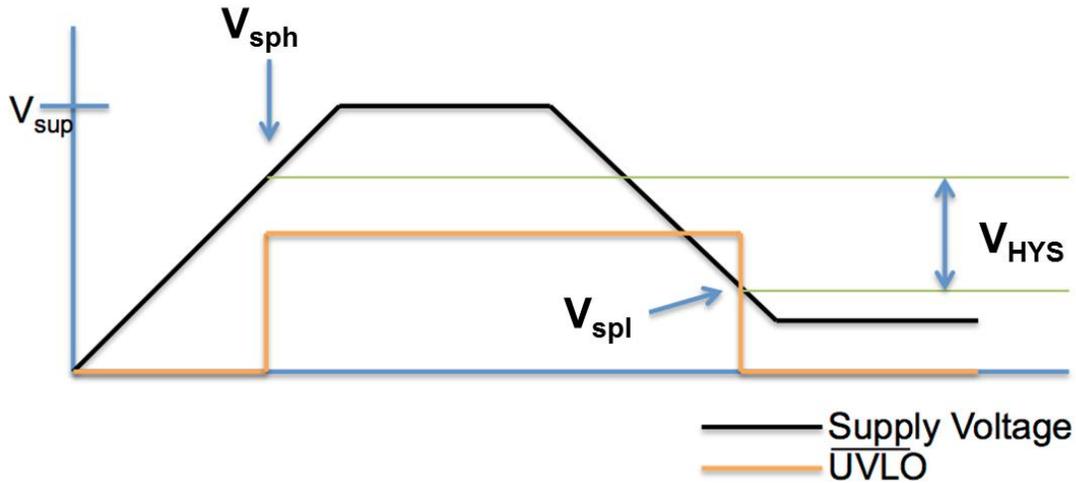


Fig. 9. Simplified UVLO waveform.

A diagram showing a simplified waveform for a UVLO circuit is shown in Fig. 9. In this diagram, the supply is being monitored by the UVLO. While the supply voltage ramps up to the nominal supply voltage (V_{sup}), the active-low UVLO output stays low. Upon reaching the positive-going threshold V_{SPH} (sometimes referred to herein as the upper switch point), the UVLO output is de-asserted to indicate that an under voltage condition no longer exists. After some time, the supply voltage drops to the negative-going threshold V_{SPL} (sometimes referred to herein as the lower switch point), at which point the UVLO output is asserted to indicate that an under voltage condition again exists. Hysteresis in the circuit is represented by the voltage V_{HYS} , which is the difference between V_{SPH} and V_{SPL} . While exaggerated in the diagram for clarity, this hysteresis provides a noise margin to prevent erratic switching behavior (e.g. “jitter”) near the switching points.

CHAPTER 3 – FABRICATION RUN ONE

This chapter provides details on the design and simulation of the UVLO circuit for the first fabrication run. The design workflow for each fabrication run will also be presented.

3.1 Design and Simulation for Fabrication Run One

A simplified block diagram of the UVLO circuit used in the first fabrication run is shown in Fig. 10. A resistor network in the Switching/Hysteresis Control block is used to divide the monitored voltage so that it crosses the switching point of the first inverter whenever it falls below a set threshold. The output from this inverter is fed back to the resistor network such that hysteresis is introduced into the circuit; this allows the UVLO to de-assert only after the monitored voltage rises to some point above the negative-going threshold crossed previously. The output buffer (the second inverter) drives the UVLO signal to external circuits. The voltage regulator is required because the switching point of the inverter is dependent upon the supply voltage. Thus, a suitable stable regulated power supply is necessary in order to maintain the stability of the switch points on the inverter as much as possible and, thus, the switching points of the UVLO. This, of course, implies that the output of the voltage regulator ideally needs to be stable over temperature.

Targeted specifications for the version of the UVLO designed for Fabrication Run One are given in Table 6. The propagation delay of 10 μ s or less was chosen based on the idea that the maximum MOSFET switching speed would be near 50 kHz and that a fault should be asserted within approximately one-half of a clock cycle. It was also indicated by system

designers at APEI at that time that the anticipated slew rate of the power supply that the UVLO would be expected to monitor was a change of 1 V in 50 μ s (or, 20 mV/ μ s).

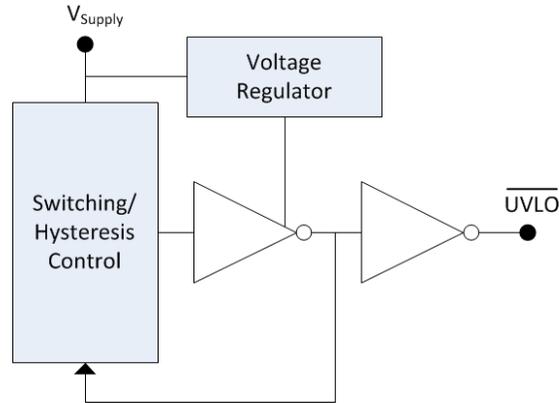


Fig. 10. Simplified block diagram of the UVLO circuit.

TABLE 6. UVLO SPECIFICATIONS FOR FABRICATION RUN ONE

UVLO Specification	Value	Notes
Positive going Threshold	18.5 V	Assumes hysteresis of 0.5 V
Negative-going Threshold	18 V	Lower switch point is 10% V_{DD}
Propagation delay	< 10 μ s	Simulated to be < 700 ns
Maximum DC Bias current	1 mA	Probably optimistic
Valid logic outputs	“0” \rightarrow < 1.5 V “1” \rightarrow > 18 V	
Operating Temperature	0 $^{\circ}$ C \rightarrow 200 $^{\circ}$ C	Tested to 225 $^{\circ}$ C; other specs +/- 5%

The values for the upper and lower switch point were selected based on the idea that a 10% variation in the monitored voltage (assumed to be 20 V) would be reason enough to trigger an assertion of the UVLO output. The only specification for the switch points given by APEI was that the power MOSFETs tend to become far less efficient at voltages near 14 V, and thus

the switch points specified are above this minimum to avoid concerns expressed by the system designers. The amount of targeted hysteresis was arbitrarily chosen to be 2.5% of the supply voltage (0.5 V).

3.1.1 Design Tool Chain

Schematic capture was accomplished in Cadence Virtuoso V6.1.4. The custom models in the Cree PDK developed at the University of Arkansas were imported into the system and updated by other team members under revision control using the Concurrent Versioning System (CVS). This approach allowed the tracking of various PDK features throughout the development process and also allowed a rollback in the event a bug was found that necessitated a return to a previous version.

Simulation was executed in the Cadence Analog Design Environment (ADE). The underlying simulation was performed in HSPICE and visualized using ADE. For certain parameter sweeps, HSPICE was run from the command line using a customized input file. In some cases, the export of waveforms was accomplished using a customized input file and a custom Python script that allowed the export of data to a format that could easily be graphed, such as a Comma-Separated Values (CSV) file.

3.1.2 UVLO Circuit Topology

Various topologies were considered for use in the UVLO; many UVLO or voltage reference topologies in the literature are CMOS-based [30–34] and proved difficult to translate to the process at-hand. Older, NMOS-based designs that used voltage references or current references for biasing typically either did not consider operation over wide temperature ranges [35], used very “long” devices, or exhibited other device characteristics that were not available for consideration in this design [36]. The choice of topology was ultimately driven by the need

to use the simplest approach that would yield satisfactory results given the potential complications that are inevitable when working in an evolving process.

After considering all the issues working against a successful demonstration, team members decided early in the project that simplicity was likely the only approach with a chance for success. Thus, even in cases where more complexity might potentially yield better performance, it was deemed better to go with a simpler approach. This line of thinking, coupled with a compressed timeline for the project, led to the decision to use a topology based on the one used by Hoque and Ang [34].

The circuit topology used by Hoque and Ang is shown in Fig. 11. This CMOS-based design contains a pre-regulator (voltage regulator), resistor-based hysteresis, and inverters that serve to buffer the final output signal. As previously mentioned, the regulated voltage is used to drive the remainder of the circuit so as to minimize the impact on the switch points as the primary supply voltage fluctuates. It is important to point out that the inverters in this CMOS-based design do not require the regulator to deliver a significant current. This differs considerably from the NMOS-based Cree process, in which current would be continuously required during operation when the pull down device was turned on.

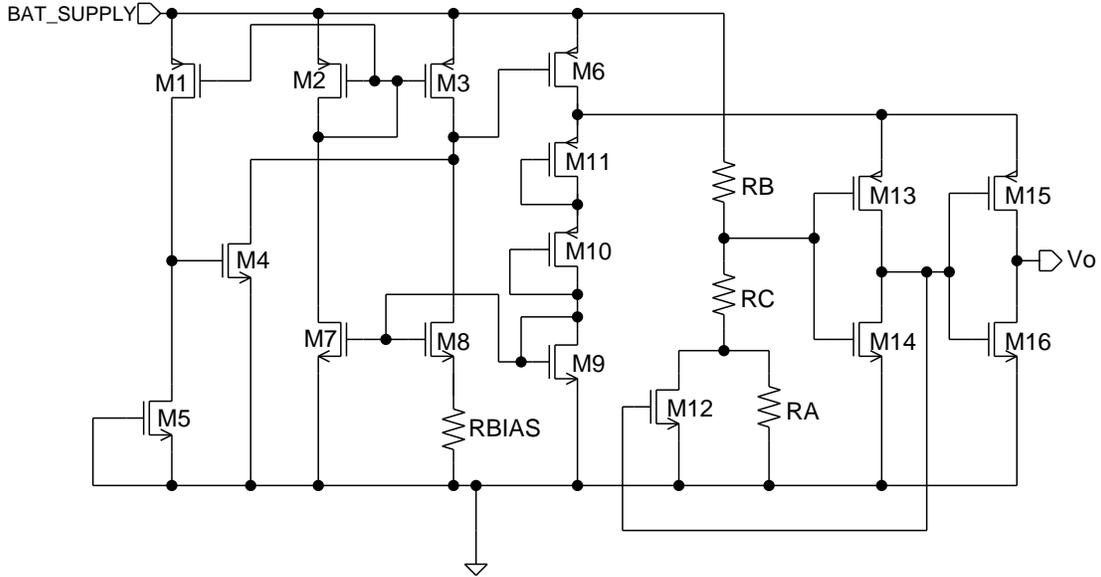


Fig. 11. UVLO topology used by Hoque and Ang [34].

It is also important to note that Hoque and Ang designed the pre-regulator to operate with an output of approximately 2.6 V. This, too, would be an issue in the Cree process, as this would provide insufficient head room for circuit operation (the threshold voltage for the enhancement mode MOSFETs in the Cree process is approximately 3 V). In addition, operation over a wide temperature range was not taken into consideration with the pre-regulator design used by Hoque and Ang, since a variation in the switching point on the order of 8% was deemed sufficient by the authors in their paper. This contrasts starkly with the needs of the SiC-based design, which was required to operate over a wider range from 0 °C to 200 °C.

One way to view the regulator topology used by Hoque and Ang in their voltage reference (formed by M2, M3, M7, M3, and RBIAS, with M9, M10, M11, and M6 in the feedback path) is as a current mirror and a current source back-to-back, where the gain around the loop is less than unity; this description is fitting, in that at the core of the topology used by the authors is a beta multiplier [22]. A block diagram depicting this arrangement of a current

mirror and a current source is shown in Fig. 12(a); for further discussion, a more simplified CMOS beta multiplier circuit is shown in Fig. 12(b).

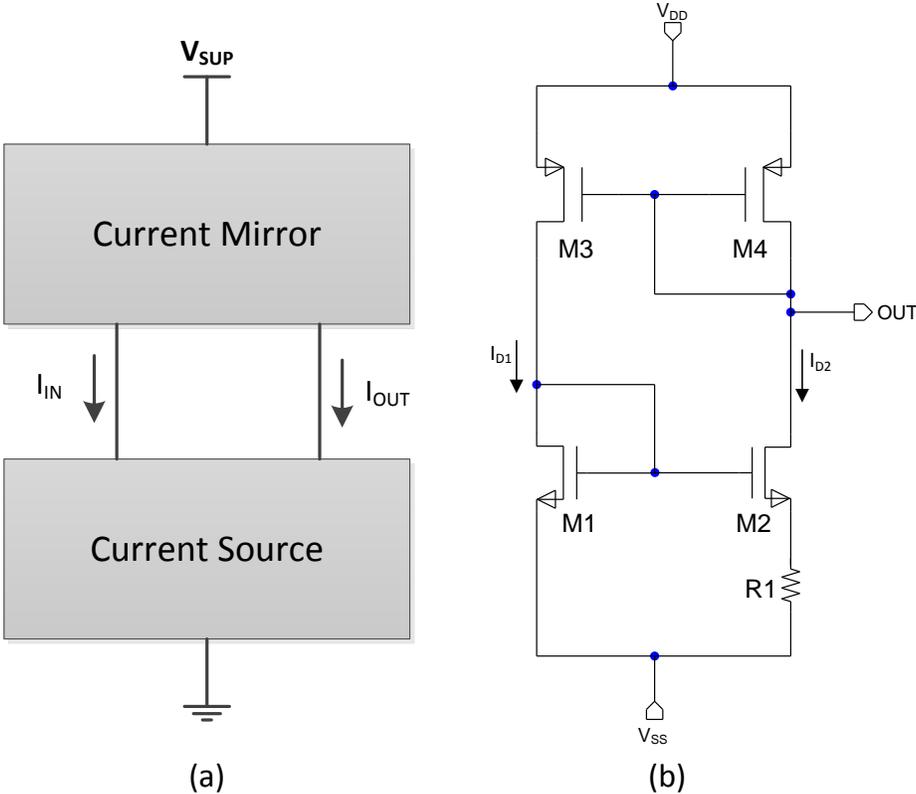


Fig. 12. Block diagram of the beta multiplier.

In Fig. 12(b), the resistor in the source of M2 (R_I) serves to keep the positive feedback gain from the current source below unity to maintain stability. In Fig. 13, a plot of V_{GS1} versus the output currents I_{D1} and I_{D2} for this generic representation is shown. The intersections of the two curves represent the stable operating points of the circuit during operation [22], [37].

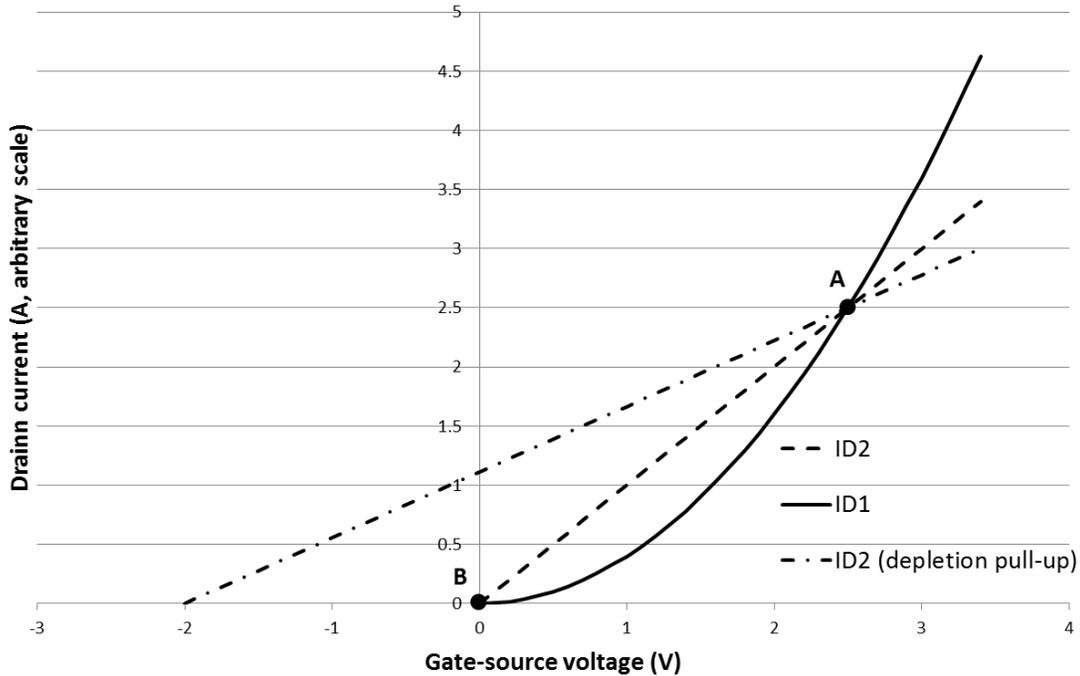


Fig. 13. A plot of current versus gate voltage for the devices in a CMOS beta multiplier.

The topology used by Hoque and Ang, as well as other CMOS-based approaches, require a start-up circuit in order to ensure that the circuit will function properly after power up. This is because there are two stable operating points for these circuits: the desired current/voltage output and zero [22]. These stable operating points are shown in Fig. 13 as points A and B. At point B, no current flows; at point A, a steady-state point is reached at the desired output level. Without some way to “bootstrap” the circuit at power up, it is possible that the circuit would remain at stable operating point B and generate no output.

In Fig. 11, the devices used in the startup sub-circuit are M1, M4, and M5. During startup, M4 (a PMOS transistor) is turned on; this pulls the gate of M6 low and forces current to flow through the output stage. As the level of current in the circuit approaches the stable operating point, the gate of M4 is brought high, which turns it off. The circuit then continues

operation at its stable operating point as if the startup circuit was not present. Startup is not an issue in the NMOS-based version presented here, as the depletion mode devices begin turning on as soon as supply power is applied. In Fig. 13 this effect is approximated by the second sloped line, which represents the load presented by the depletion mode devices. In this case, the two curves in the NMOS-based version do not intersect at zero; therefore, the only stable operating condition is at the desired operating point.

In the new UVLO topology, the regulator used by Hoque and Ang was initially replaced with a beta-multiplier-based design implemented in the Cree NMOS process; the sub-circuit used can be seen in Fig. 14. In a traditional beta multiplier topology, the pull-up devices are PMOS transistors, whereas here the pull-up devices are depletion mode NMOS devices. The name of the beta multiplier is derived from the concept that beta (the transconductance) of M1 is larger than M3 (because M1 is sized larger than M3) and the gate-source voltage difference between these two transistors is ultimately dropped across the resistor. For a typical CMOS process, this means that as temperature increases the resulting increase in the value of R compensates for the decrease of V_T in M1 and maintains a constant voltage at the output [38]. In the absence of statistical data regarding V_T shift over temperature in the Cree process, optimization of R to compensate for the shift of V_T was not attempted; instead, focus was centered on achieving the desired output voltage.

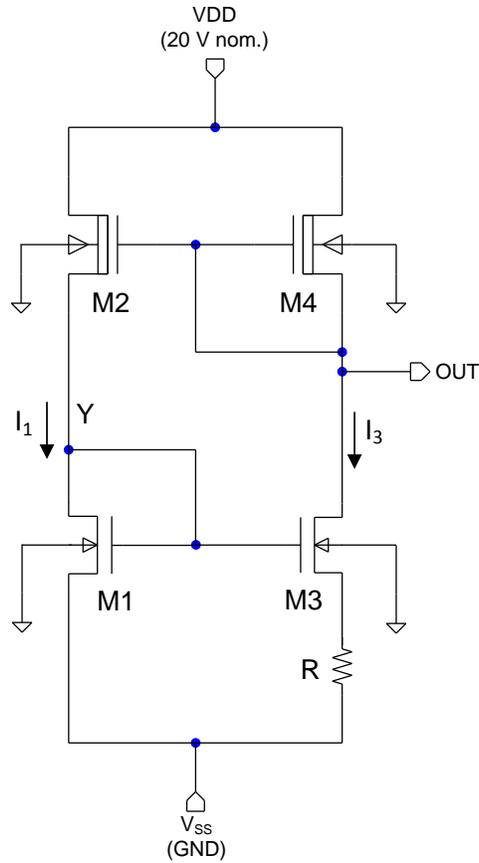


Fig. 14. NMOS derivative of a CMOS Beta-multiplier.

TABLE 7. COMPONENT VALUES AND SIZES FOR THE BETA MULTIPLIER IN FIG. 14

Device	Width / Length / Multiplicity
M4	16 / 8 / 8
M3	32 / 4 / 20
M2	8 / 8 / 10
M1	32 / 4 / 1
R	400 Ω

The circuit in Fig. 14 operates similarly to its CMOS counterpart, with the introduction of depletion mode NMOS devices to replace the PMOS transistors in the CMOS version. This version of the topology produces an output of approximately 5.5 V at 25 °C for a supply voltage between 10 and 20 V. The waveform simulated for this circuit is shown in Fig. 15.

Single-Stage Voltage Reference Output

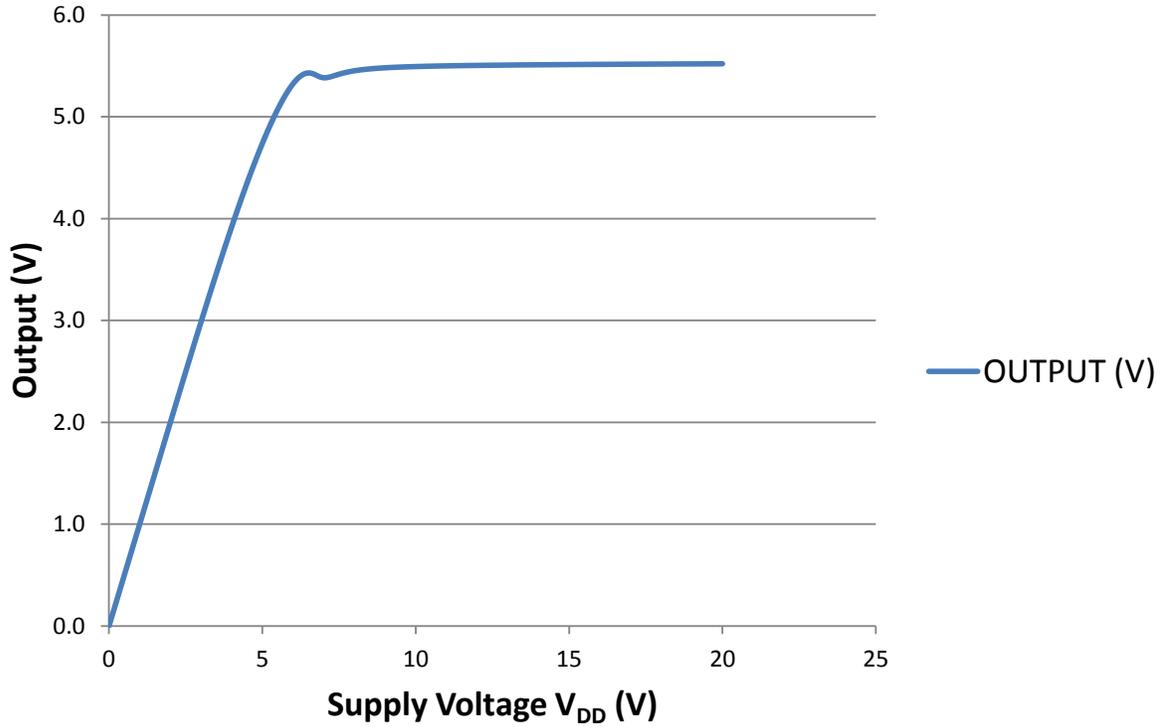


Fig. 15. Simulated single-stage voltage reference output for a swept supply voltage.

For the circuit in Fig. 14, it is assumed that the current I_3 through M3 is related to the current I_1 in M1 by a ratio α , therefore $I_3 = \alpha I_1$. Ignoring body effect and channel modulation, the current is:

$$I_1 = \frac{1}{2} \beta_1 (V_{GS1} - V_{T1})^2 \quad (3.1)$$

Solving for V_{GS1} yields:

$$V_{GS1} = \sqrt{\frac{2I_1}{\beta_1}} + V_{T1} \quad (3.2)$$

A similar expression exists for V_{GS3} . The voltage V_{GS1} can also be expressed as:

$$V_{GS1} = V_{GS3} + I_3 R \quad (3.3)$$

Substituting the expression for V_{GS1} in Eq. (3.2) (and the equivalent expression for V_{GS3}) into Eq. (3.3) yields:

$$\sqrt{\frac{2I_1}{\beta_1}} + V_{T1} = \sqrt{\frac{2I_3}{\beta_3}} + V_{T3} + I_3R \quad (3.4)$$

If it is assumed that $V_{T1}=V_{T3}$, and by using the relationships $I_3 = \alpha I_1$ and $\beta_3 = K\beta_1$, it is possible to solve for I_1 :

$$I_1 = \frac{2}{\alpha^2 R^2 \beta_1} \left(1 - \sqrt{\frac{\alpha}{K}}\right)^2 \quad (3.5)$$

Substituting the expression in Eq. (3.5) into Eq. (3.2), and solving for R yields:

$$R = \frac{2}{\alpha \beta_1 (V_{GS1} - V_{T1})} \left(1 - \sqrt{\frac{\alpha}{K}}\right) \quad (3.6)$$

At this point, it is known that $\beta_1 = K_1'(W/L)$ and that a value for K' of $0.5 \mu\text{A}/\text{V}^2$ can be used for the enhancement mode device based on validation with previous simulation results. V_T is already known to be near 3 V, and the desired value for V_{OUT} is 5.5 V. Knowing that V_{GS1} must be slightly higher, a value for V_{GS1} of 6.5 V is assumed. A value for K of 20 is first chosen, and then a value for α of 18 because it is likely slightly smaller than K . Substituting these values into Eq. (3.6), the value for R is found to be 407 Ω ; this is rounded to 400 Ω for simplicity.

The size of devices can be calculated by first assuming that M1 is a 32x4x1 device. Since the value of K is assumed to be 20, this leads to a 32x4 device with a multiplicity of 20 for M3. In order to calculate W/L for M2, it is necessary to solve for the value of I_1 . This can be done using Eq. (3.5) and the value of parameters already defined or calculated, and yields a calculated current of approximately 24 μA ; a more conservative value of 20 μA is chosen instead. Now knowing I_1 , it is possible to use the current equation for a MOSFET in saturation and a value for $K' = 20 \mu\text{A}/\text{V}^2$ for the depletion devices based on previous simulations to solve for W/L :

$$\frac{W}{L} = \frac{2I_2}{K_2'(V_{GS2} - V_{T2})^2} \quad (3.7)$$

Substituting known values into Eq. (3.7), W/L for M2 is found to be 11; a value of 10 is chosen for simplicity, thus yielding a size for M2 of 8x8x10. A long device was used on the assumption that it would provide better performance as an active load. The same approach is used to solve W/L for M4 using the relationship $I_4 = I_3 = \alpha I_2$; the value of W/L for M4 is calculated to be 22. Iterative simulation was used to achieve a V_{OUT} of 5.5 V; this yielded a final W/L value of 16 for M4 and a final size for M4 of 16x8x8.

As mentioned, the NMOS-based beta multiplier generated an open circuit output voltage of 5.5 V, and it was initially planned to cascade two stages to achieve an output of approximately 10 V. However, it was later decided to use a higher voltage of 15 V instead, in order to accommodate the reduction in output seen at higher temperatures due to threshold voltage drift. In order to address the need for a higher output voltage, four “stages” of the topology were “stacked” to achieve the desired output voltage, a technique that is used elsewhere in the literature [32], [33]. The resulting topology is shown in Fig. 16. Here, the topology has been adjusted to accommodate the additional current that must be handled in the lower stages by increasing the size of the devices. The body effect also plays a role in the devices that are in the upper stages. Therefore, the final topology was derived by cascading the topology in Fig. 14 and then scaling devices in each stage incrementally to achieve stable operation and a final output near 15 V. The final size of devices in Fig. 16 can be compared with those in Table 7.

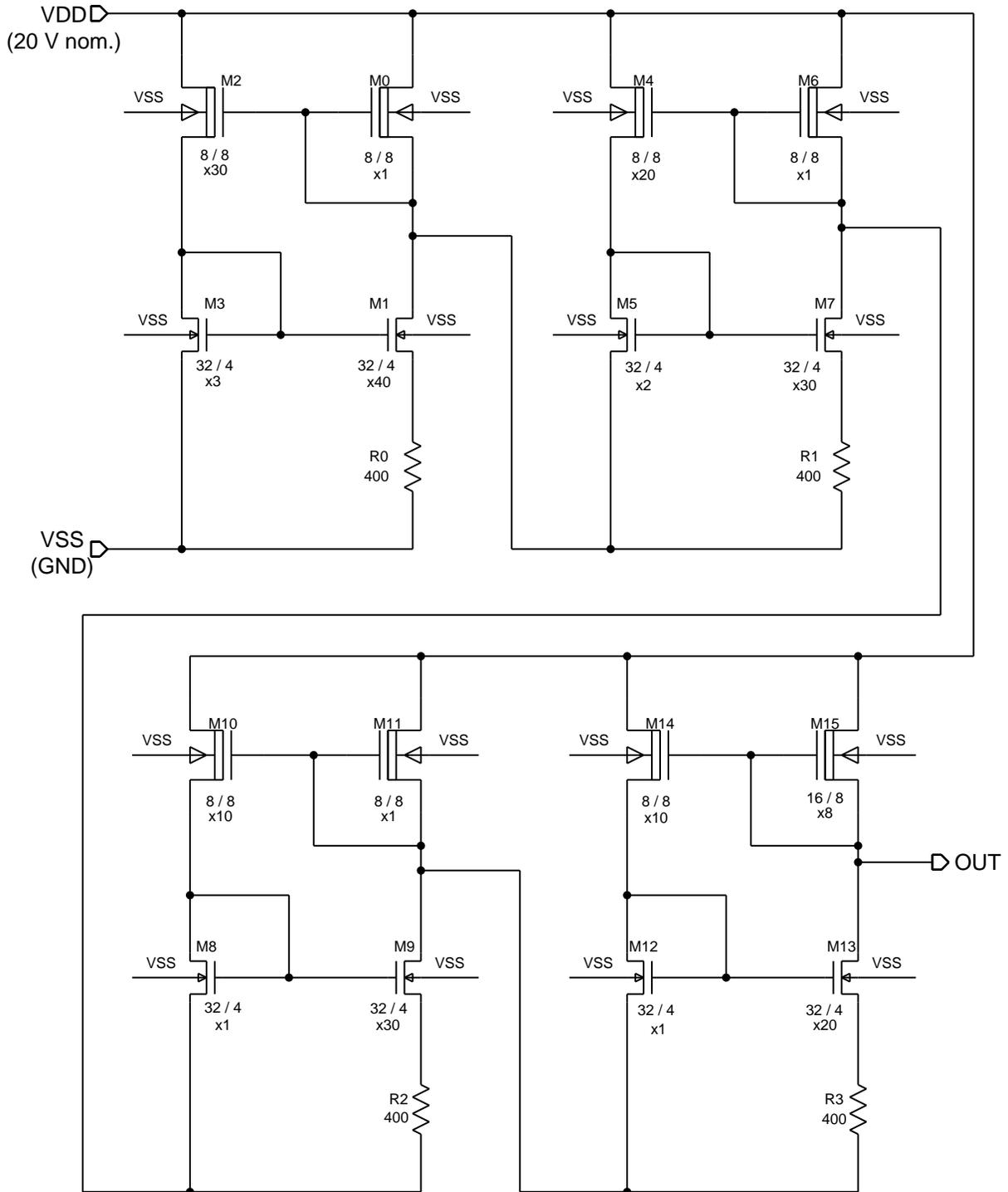


Fig. 16. The final “stacked” version of the UVLO voltage reference.

The open circuit output voltage of the circuit in Fig. 16 is 15.27 V at 25 °C, which is well within the range of voltage that was desired. It is important to point out that the topology shown is more accurately described as a voltage reference than a voltage regulator. A voltage regulator would be expected to regulate the output voltage for relatively wide ranges of current, while a reference is intended to provide a particular voltage with minimal current draw on the output. The repercussion of not using an actual voltage regulator is a sag in the output with increasing amounts of current. The choice to use the reference topology and live with a sagging output voltage was driven by a number of project-level pressures. The primary reason was that a full voltage regulator would have required significantly more layout space, and since there was already a team member working on a voltage regulator [23], the use of significant layout space on the chip to duplicate functionality was less defensible. To minimize voltage drop on the output, it was decided to supply the regulated voltage to only the first inverter in the UVLO, since it was the most critical in terms of determining the overall switch point for the circuit.

Although the output voltage for the reference in the cascaded version after loading with the final UVLO circuit was 5.4 – 3.4 V, it was still possible in simulations to produce the proper output waveforms by adjusting the resistors in the hysteresis section. After some discussion, it was decided that the safest way to test the circuit and to assure the maximum chance of success for the entire gate driver was to provide an external voltage source for the first switching position. Thus, the schematic and layout was amended to provide a bonding option that would allow either the internal voltage reference or an external source to be used.

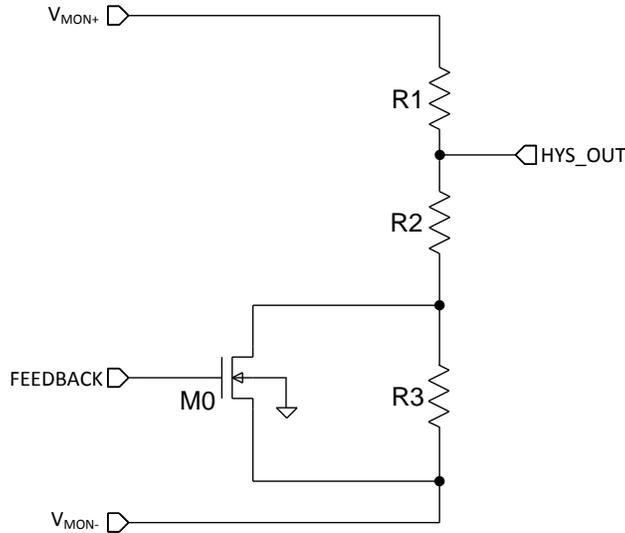


Fig. 17. Hysteresis portion of the UVLO circuit for Fabrication Run One.

The hysteresis portion of the UVLO circuit is shown in Fig. 17. Hysteresis is accomplished in the circuit by applying feedback from the output (equivalent to the inverted logic level of HYS_OUT) to the transistor M0. When HYS_OUT is above the switching threshold, M0 is turned off and R₃ is simply in series with R₂ to form a voltage divider with R₁. When the switching point drops sufficiently, the UVLO switches state and FEEDBACK goes HIGH. This has the effect of shorting out R₃ and effectively sets a new (higher) switching point. This is because the voltage applied at V_{MON+} must now climb higher in order to cross the switching point at HYS_OUT again, since now only R₂ forms the lower leg of the voltage divider. Once this happens, FEEDBACK again returns low, which effectively re-inserts R₃ into the network and resets the switching point to the original value. Assuming no hysteresis in any other portion of the circuit, this allows the amount of hysteresis and the upper and lower switch points to be solely determined by R₁, R₂, and R₃. It is also important to note that the shift in voltage at HYS_OUT that occurs when M0 switches acts as a positive feedback mechanism.

The values for resistors R_1 , R_2 , and R_3 can be calculated by first assuming an approximate overall current drain of $I_{MAX} = 250 \mu\text{A}$ based on the desire to limit total current consumption of the UVLO circuit to approximately 1 mA and the arbitrary choice to let the resistor network consume one-fourth of the total current budget when using a maximum supply voltage of 20 V. Referring to Fig. 17, it would be assumed that the VMON+ connection would be tied to VSUP (the supply voltage being monitored) and that the VMON- connection would be tied to ground. Using KVL:

$$V_{SUP} = I_{MAX}R_1 + I_{MAX}R_2 + I_{MAX}R_3 \quad (3.8)$$

where the value of V_{SUP} and I_{MAX} are known, which allows the total resistance of the network to be calculated as being 80 k Ω . Also, the resistors R_1 , R_2 , and R_3 form a voltage dividing network, so that:

$$V_{HYS_OUT} = V_{SUP} \left(\frac{R_X}{R_1 + R_X} \right) \quad (3.9)$$

Where $R_X = R_2$ or $(R_2 + R_3)$, depending on whether the transistor M0 is turned on or off, respectively.

Since the value of R_3 is assumed to be much smaller than the values of either R_1 or R_2 , and since it is known that the hysteresis voltage (V_{HYS}) is approximately 0.5 V, then:

$$R_3 \approx \frac{V_{HYS}}{I_{MAX}} = \frac{0.5 \text{ V}}{250 \mu\text{A}} = 2 \text{ k}\Omega \quad (3.10)$$

Substituting the result from Eq. (3.10) into Eq. (3.8), it is possible to calculate that $R_1 + R_2 = 78$ k Ω . Based on simulations of the inverter topology in the circuit, the switch point for the inverter is found to be approximately 5 V. Substituting this value into Eq. (3.9) for the case where the input is below the lower switch point where R_3 is not effectively in the circuit so that $R_X = R_2$. Here, it is also found that $V_{SUP} = V_{SPH}$. This gives:

$$R_2 = \frac{V_{SUP}}{V_{SPH}} (R_1 + R_2) = \frac{5V}{18.5V} 78 k\Omega \approx 21 k\Omega \quad (3.11)$$

Now having values for resistors R_2 and R_3 , it is possible to substitute back into Eq. (3.8) to find that $R_1 \approx 57 k\Omega$.

These calculated values do not precisely match the final values used for the circuit, however. Ultimately, the final values used in the design for $R_1 = 56.2 k\Omega$ and $R_2 = 20.5 k\Omega$ were close to calculated values. The final values were derived by making minor adjustments to the calculated values above and were selected because they yielded switch points at 18.41 V and 19.13 V at 125 °C, which was considered the nominal operating temperature for the circuit and still provided for circuit operation at 225 °C, albeit with a reduced hysteresis of 0.15 V. The larger value chosen for R_3 was derived from iterative simulation to set the final size of both R_3 and M0 and will be discussed below.

The switching and output buffer portion of the UVLO circuit is shown in Fig. 19. The buffer consists of four cascaded inverters. The latter three are simple resistor-transistor inverters that were chosen for their simplicity and in an attempt to minimize possible issues seen with depletion devices. V_{DD} for the inverters was tied to the 20 V rail being monitored; this was done to assure the highest possible output voltage for the final stage. Power for the first stage, a Schmitt trigger, was supplied by a separate, dedicated 10 V supply.

A size of 32x2 was chosen for all MOSFETs because it was the earliest device characterized and was considered to be the most consistent model. The resistor for the final output inverter was chosen to be 15 k Ω , based on the conservative assumption of driving a 15 pF load and the choice to limit the rise time to less than 1 μ s to allow sufficient time for the signal to propagate to other logic circuits within the targeted 10 μ s propagation delay specification. With a time constant $\tau = RC$, and making the conservative assumption that the

rise time occurs in three time constants, a rise time of 675 ns was calculated for a 15 k Ω resistor. To simplify layout, the same size of resistor was assumed for the other inverters as well.

It is worth noting that, by the time this part of the circuit was designed, it had been revealed during a review meeting that the 1 mA target for total current consumption was very conservative and that as much as 5 times more current was acceptable from the standpoint of system designers. For the simple inverters, the primary concern was to assure that the pull down device was of a sufficient size to yield a valid logic “0” output (1.5 V or less). Thus, while the size of the 15 k Ω resistor could have been made smaller to facilitate a faster rise time, it would also have meant that more current would be necessary to transition the output low and, therefore, a larger MOSFET would have been required for proper operation. Referring to Fig. 19, the amount of current needed to drop 18.5 V across R_8 (and achieve a minimum pull down of 1.5 V) can be calculated as:

$$I = \frac{V_{DD} - V_{OUT}}{R_8} = \frac{20\text{ V} - 1.5\text{ V}}{15\text{ k}\Omega} = 1.2\text{ mA} \quad (3.12)$$

Knowing the current, it is possible to calculate the size of M18 by using the equation for current for a MOSFET in saturation:

$$I = \frac{1}{2} K'_N \frac{W}{L} (V_{GS} - V_T)^2 \quad (3.13)$$

and then solving for W/L to get:

$$\frac{W}{L} = \frac{2I}{K'_N (V_{GS} - V_T)^2} \quad (3.14)$$

where $K'_N = 0.5\ \mu\text{A}/\text{V}^2$, which was chosen because it gave a good match with previous simulation results, V_{GS} is 10 V (since the first stage was to be powered by an external 10 V supply), and a V_T is 3 V. The calculated result for W/L is 106. Since a 32x2 device is being used, the value of W/L is divided by 16 to find that a minimum multiplicity of about 6 would be

needed to pull down to 1.5 V. However, since it is obviously preferable to pull down lower than the maximum logic “0” level, a recalculation was performed using a V_{OUT} of 0.2 V to yield a multiplicity value of 7. Similar calculations were performed for M19 and M8, and their multiplicity was the same as M18. In simulation, however, M8 had to be increased in size to 30 to give reasonable fall times for the large load expected. In retrospect, this was done rather hastily and could have been more optimized. It was also found during simulation that M19 had to be increased in size to 28 to be able to drive the large feedback transistor used to short a resistor in the feedback network and, after doing this, increasing the size of M8 to 9 was done to drive the larger transistor M19.

The Schmitt trigger on the front end of this circuit, formed by R_{I0} , M15, M7, and M10, was used after having mediocre results with using a simple resistor-transistor inverter. After a new round of model updates in the weeks leading up to tape out, re-simulation of the UVLO showed that the simple resistor-transistor inverter failed to provide operation across the full temperature range. In an effort to address this issue, it was then replaced with the Schmitt configuration. A more proper derivation of a Schmitt trigger will be presented in Chapter 4; here, however it should be pointed out that the focus was on controlling the hysteresis using a resistor network; therefore, the Schmitt trigger was modified through iterative simulation to have minimal hysteresis.

Data from the plot seen in Fig. 18 is used to calculate the size of the transistor needed for M22 used in the hysteresis portion of the circuit (shown in Fig. 20). This plot shows $R_{DS(ON)}$ for a 32x2 device of multiplicity 1. Here, with a V_{GS} near 20 V, it can be seen that a single 32x2 device has an $R_{DS(ON)}$ of about 2.3 k Ω .

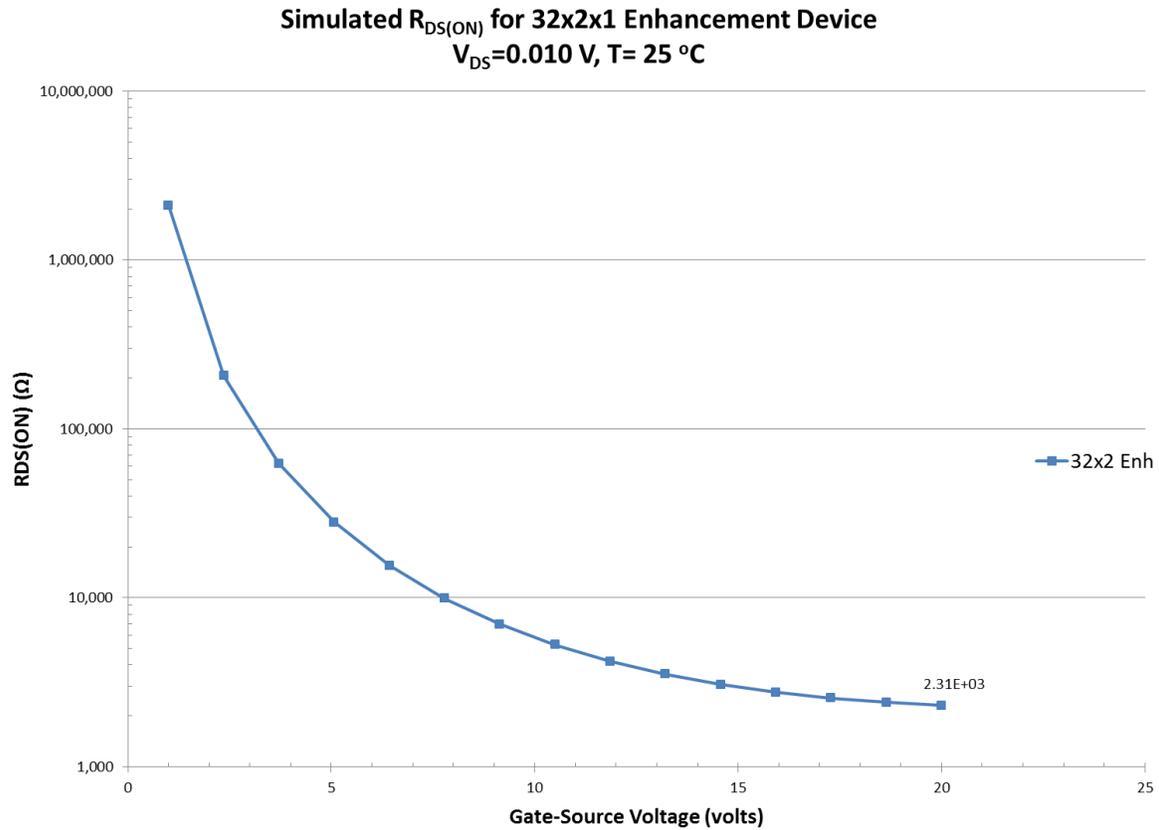


Fig. 18. Simulation showing $R_{DS(ON)}$ for a 32x2 enhancement MOSFET.

Knowing that it is necessary to change the drop across R_3 in the same figure from 0.5 V to 5 mV (a drop of 99%) and that the current is 250 μA , it is possible to calculate the $R_{DS(ON)}$ necessary to reach 5 mV. Since the value of $R_{DS(ON)}$ will be quite small, it is assumed that the larger 2 k Ω resistor with which it is paralleled can be neglected, thus allowing calculation of the necessary $R_{DS(ON)}$ as:

$$R_{DS(ON)} = \frac{0.005\text{ V}}{250\ \mu\text{A}} = 20\ \Omega \quad (3.15)$$

Dividing the $R_{DS(ON)}$ of a single device (2.3 k Ω) by 20 Ω , it is found that a multiplicity of 115 is needed for M22.

Unfortunately, it went unnoticed at the time that the on-the-fly resizing of the Schmitt trigger to minimize hysteresis led to an issue where the pull down for the output of the trigger

was not sufficiently low when simulated at high temperature. This then led to rest of the inverter chain not swinging rail-to-rail, and caused the inverter driving M19 to not be driven fully into cut off. This meant that the gate of transistor M22 used in the hysteresis portion of the circuit (shown in Fig. 20) was not driven fully to 20 V, and was instead driven to near 12 V (as revealed by simulation much later after the tape out). This would lead to a much larger $R_{DS(ON)}$ for M22 and is now understood as the reason why the multiplicity of M22 had to be increased during simulation iterations to 400 in order to get it to pull sufficiently low, even after increasing the size of the resistor it is paralleled with to 3 k Ω . In retrospect, more attention should have been paid to internal node voltages while making adjustments to the circuit, so that the repercussions of each change were fully understood.

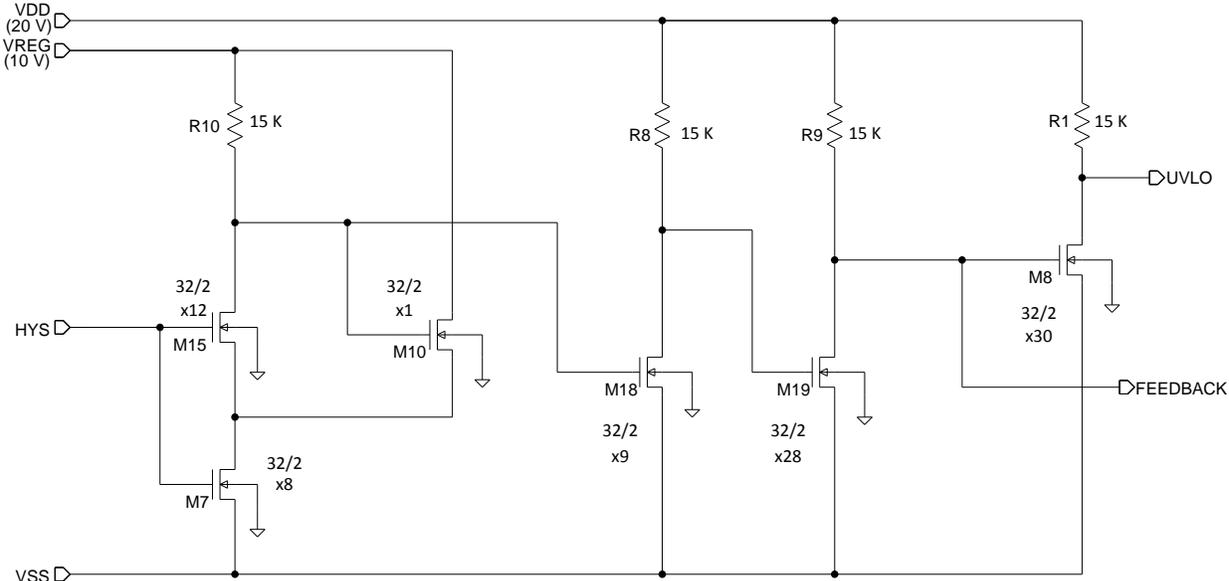


Fig. 19. The switching and buffer portion of the UVLO circuit.

To help assure successful demonstration of the gate driver as a whole and to minimize the layout footprint, the resistors used for dividing down the supply rail in the hysteresis portion were taken off-chip. Doing this allowed for adjustment of the switching threshold to account for

process variation. In addition, a bonding option was added in the final layout to allow either the onboard voltage regulator or an external voltage regulator to be used, thus allowing performance evaluation of the original design while minimizing the risk of failure for the entire gate driver chip. To add further assurance, an overriding ENABLE signal was added to the fault protection logic to allow the gate driver to operate without fault protection in the event the UVLO or overcurrent protection sub-circuits exhibited issues that prevented normal operation.

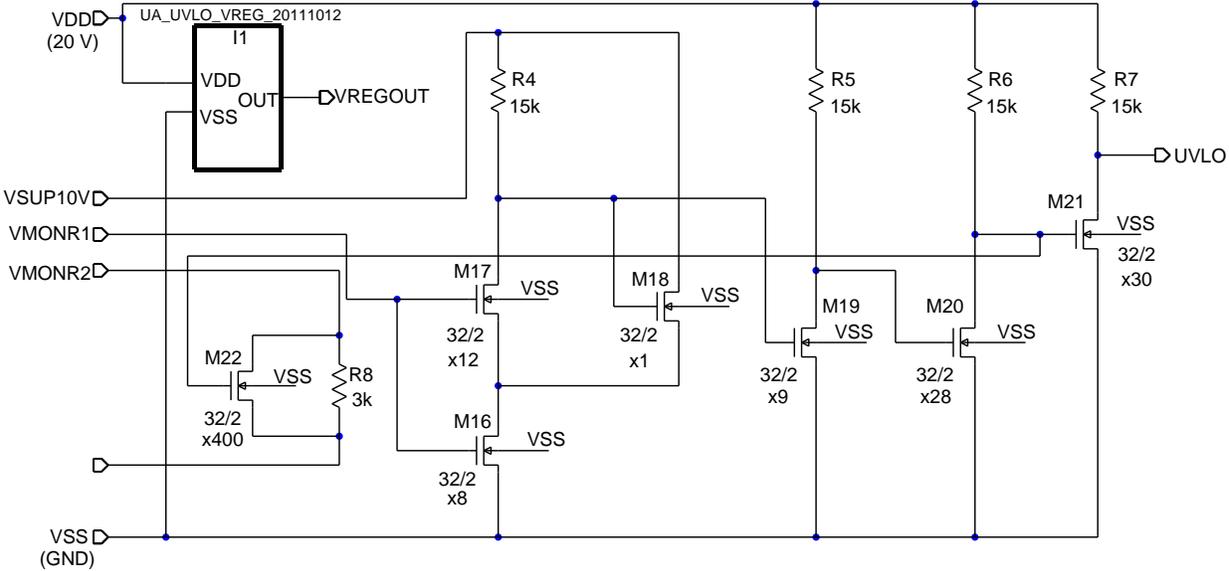


Fig. 20. The final UVLO schematic for Fabrication Run One.

Fig. 20 shows the final UVLO schematic for the first fabrication run, including the hysteresis, switching, and buffer sub-circuits. The underlying schematic for the voltage regulator symbol in the schematic is identical to that seen in Fig. 16. The V_{SS} labels within the schematic indicate that the body connections for all MOSFETs are tied to the V_{SS} power rail.

3.1.3 Other Circuits

Early in the project, the collaboration team had expressed the desire for a temperature sensor that could be placed alongside the gate driver circuit on the die and be used to provide real time temperature readings for the system controller. A temperature sensor was created as

part of a separate effort and included on the tape out. An overview of this circuit is provided in Appendix A.

3.1.4 Design Trade-offs

Considerable time pressures were applied to the design process as a result of device model changes, learning curves for the design tool chain, and last minute changes to the combinational logic for the fault circuits. Several approaches to tackle the problem were considered and partial experimentation was performed on these approaches; however, due to time constraints, the final approach was ultimately chosen because it appeared to have the best chance for success with the least degree of risk. Therefore, it is worth noting that these time pressures inevitably led to trade-offs in the final design.

One key concern during the design process was the need to conserve space whenever possible. The final chip that was taped out for Fabrication Run One was 8.7 mm x 5.8 mm, and contains both the pad rings and circuits. However, leading up to the tape out date, it had been assumed that it would be much smaller. An early estimate for the area needed for the UVLO based on an area requirement of approximately $640 \mu\text{m}^2$ per $32 \times 2 \times 1$ depletion device was $137,148 \mu\text{m}^2$. However, this size estimate did not include space for routing or probe pads, nor did it take into account the larger devices that would be necessary in the design. Ultimately, the size of the layout for the UVLO was just over $620,000 \mu\text{m}^2$. Given the space requirements anticipated for other circuits in the cell, this ultimately meant that there was no space for the large devices that would be necessary to build a robust voltage regulator. Hence, as previously mentioned, the regulator topology used to feed the portion of the circuit most sensitive to voltage variation was a compromise in performance and space, with the bulk of compromise afforded to the former.

One design parameter that did not need to be adjusted for maximum performance was switching speed. Unlike the gate buffer circuit (for instance) where the timing of signals is absolutely critical, the switching speed for assertion of the UVLO output (the most critical parameter) was relatively relaxed. Ultimately, the simulated switching speed of the UVLO circuit was always much faster than the targeted upper limit (on the order of hundreds of nanoseconds), so circuit modifications to speed up the circuit were never considered during the design phase.

3.1.5 Simulations

As previously mentioned, the voltage levels seen in the output of the simple back-to-back current mirror circuit were too low to be of use in the UVLO circuit, so the unit cell was “stacked” to achieve an open circuit voltage of approximately 15 V. The simulated output for this circuit can be seen in Fig. 21. As expected, the output of this version of the voltage reference also demonstrated a notable dependence on temperature, but time constraints prevented any further adjustment to the topology and, much like Hoque and Ang concluded in their paper, some deviation over temperature was deemed acceptable.

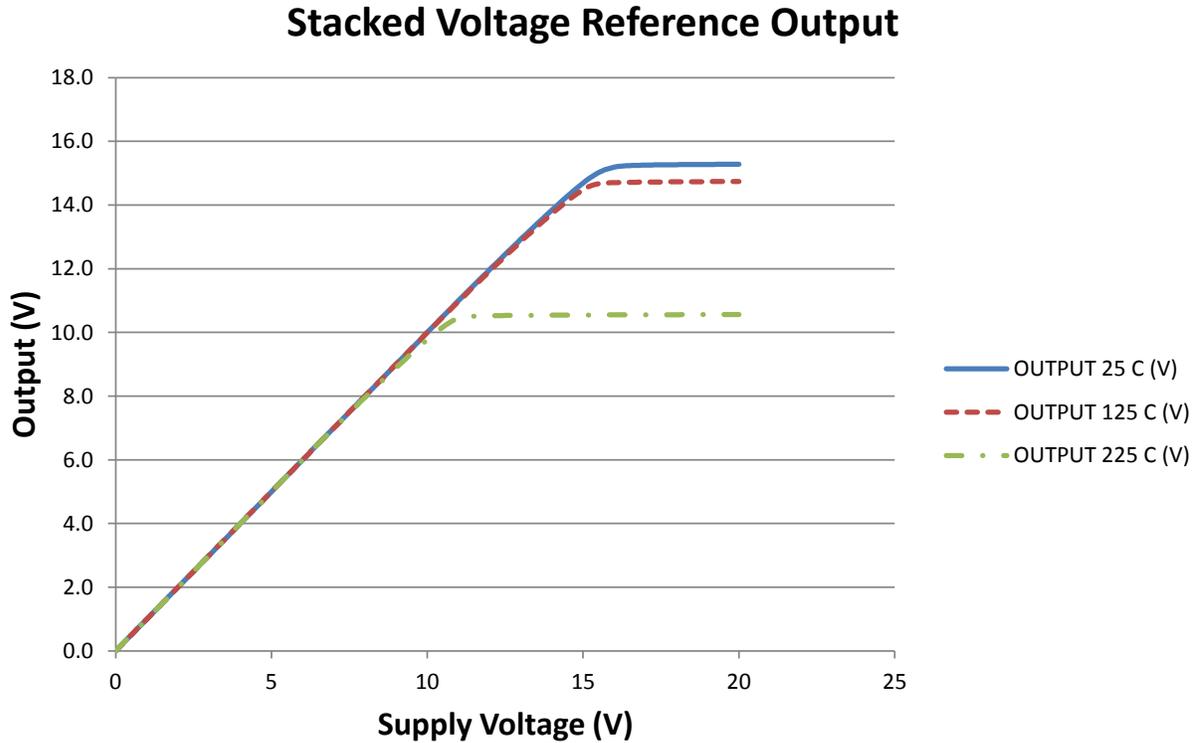


Fig. 21. Simulated output waveform for the stacked voltage reference.

When designing a circuit in which the switching point is critical for circuit operation, it is important to understand how the switching point is determined. In Fig. 22, a simple resistor-transistor inverter is presented. It is intuitive to imagine that if the value of the resistor is decreased while the size of transistor M0 remains the same, the effective switching point of the circuit shifts accordingly higher. This is because as the resistor decreases in value, the transistor must be turned on more strongly to pull down the output to reach a given level. As expected, there are other factors at play. For instance, it is possible to make the resistor so small that M0 is unable to pull down the output below a level that would be considered a valid “0” input for a logic circuit.

Waveforms for this circuit are shown in Fig. 23, where the value of the resistor is swept from 2 k Ω to 22 k Ω and the size of M0 is kept constant at 32x2x3. In the waveform, the input to the inverter is shown transitioning from high-to-low and the resulting output for each resistor value is shown.

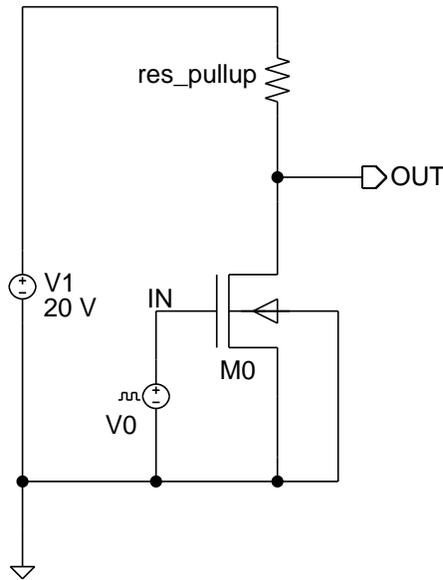


Fig. 22. Simple RTL inverter.

To provide the best noise margin, a reasonable switching target for a circuit using a 20 V supply would be around the midpoint (10 V). From the waveforms shown, it can be seen that a lower valued resistor not only has a higher switching point (near 14 V), but it also prevents the output from dropping below about 9 V at the lowest point; this output would not be sufficient if the signal was driving the input of a similar inverter. At the other end of the spectrum, the largest value (22 k Ω) would have a switching point near 8 V and allows the output to be pulled below 1 V. Based on the curves shown, a reasonable compromise in terms of resistor size (which translates to layout area), switching point, and pull-down level might be 15 k Ω .

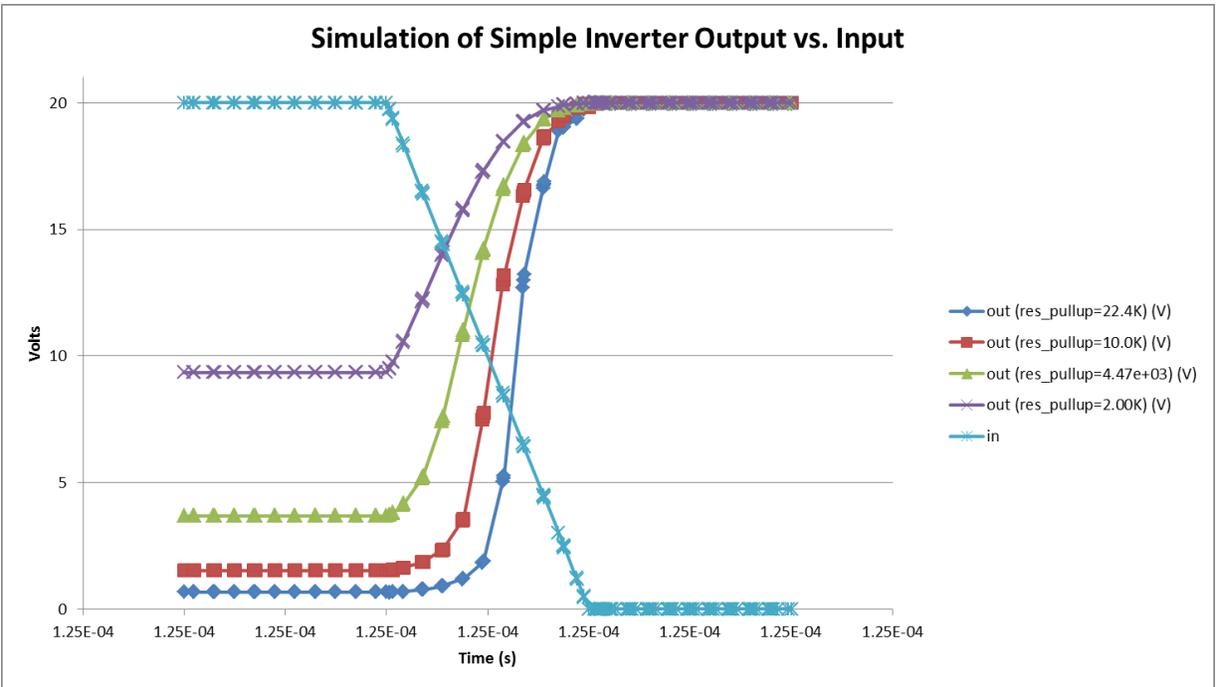


Fig. 23. Simulation of the simple RTL inverter showing one switching point.

During the course of the design process, a number of inverter topologies were considered. Four of these topologies are shown in Fig. 24. In this circuit used to evaluate the performance of each topology, output signals OUT1-4 are the outputs for a simple inverter with an active load pull-up (a depletion device), a simple resistor-transistor inverter, a Schmitt-like configuration with a depletion mode pull-up, and a Schmitt-like inverter with a resistor pull-up, respectively.

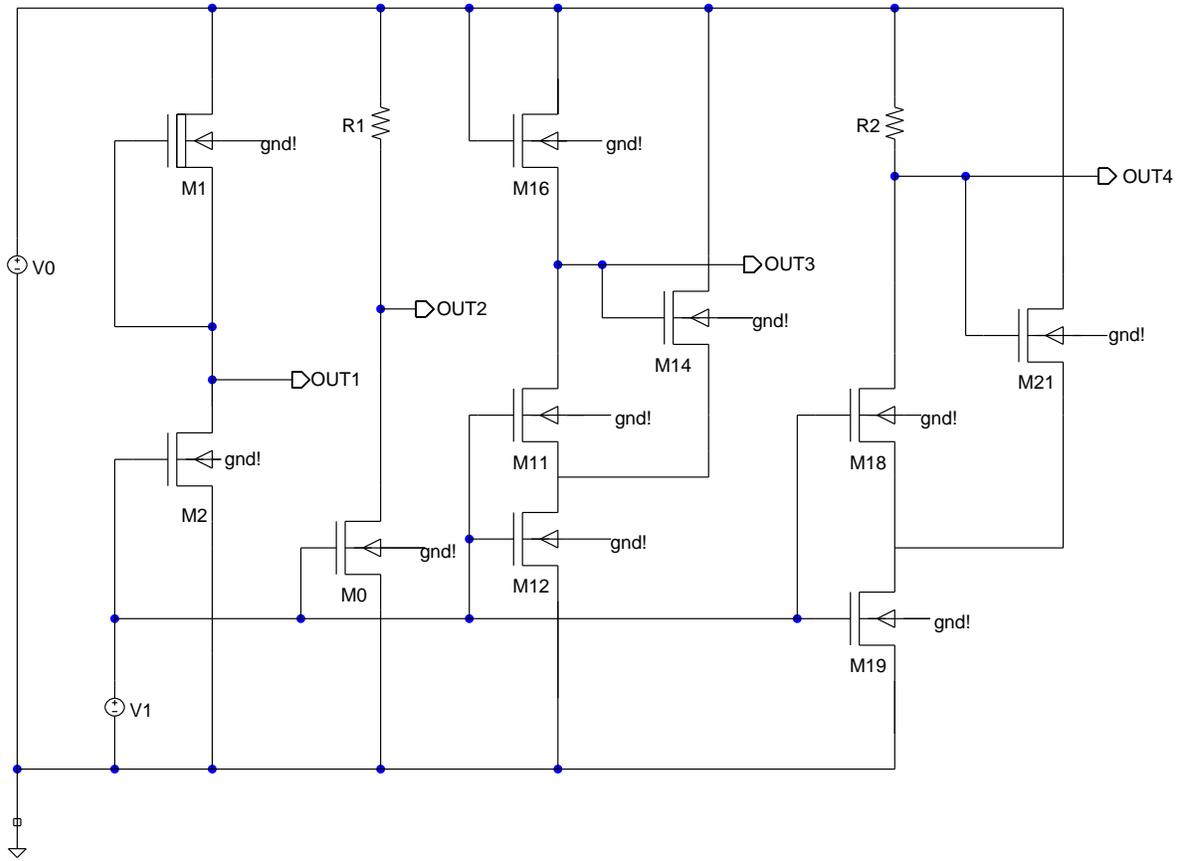


Fig. 24. A circuit to compare various inverter topologies.

Simulated waveforms for each of these outputs are shown in Fig. 25. While each topology may not be fully optimized for performance, it is the general shape and minimum/maximum output levels that are under consideration here. It can be seen that some topologies provide a rather sluggish turn on or turn off, while others exhibit a very sharp (and desirable) transition. Also, some outputs pull very near the power rails, while others do not. Based on experimentation with each topology and the analysis of waveforms such as these, the choice to use the Schmitt-like topology with a resistor pull-up in the UVLO was made, since it demonstrates a rapid transition while still swinging from 20 V down to below 1.5 V.

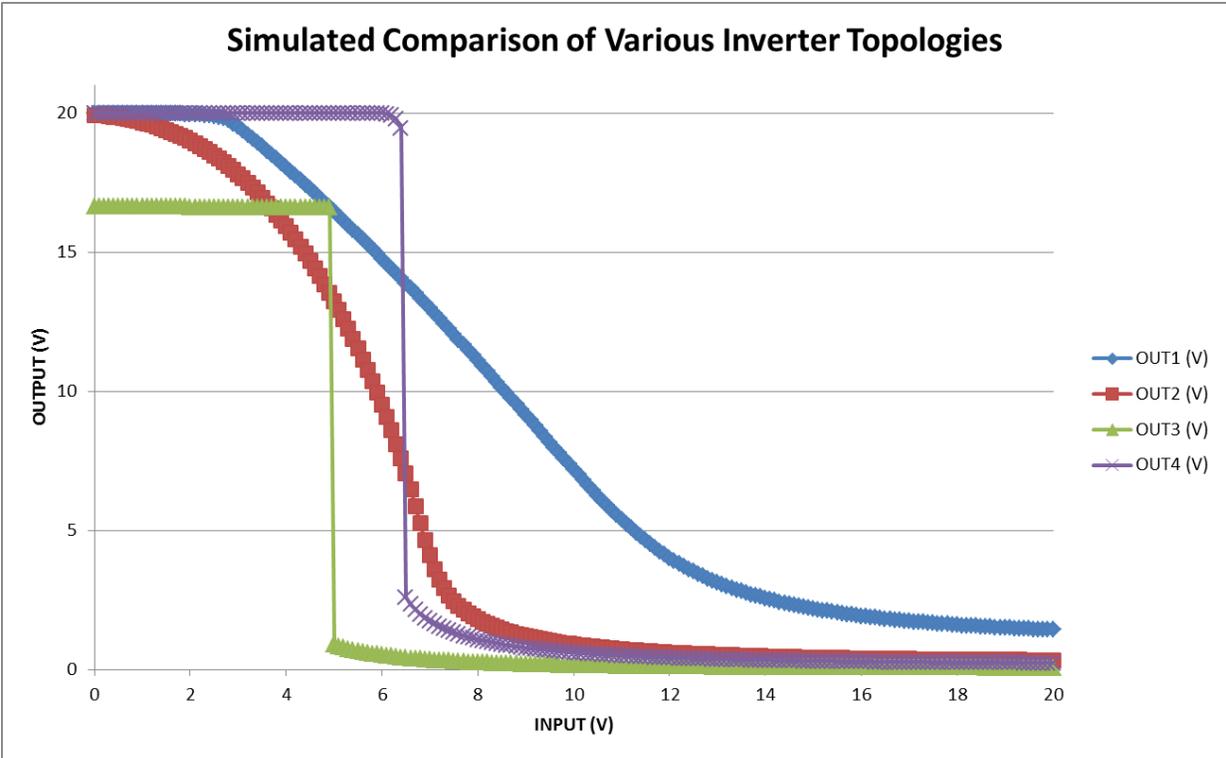


Fig. 25. A simulated comparison of the inverter topologies in Fig. 24.

The simulated waveforms in Fig. 26 represent the output of the UVLO at 25 °C using an external voltage regulator. The solid line in the figure represents the value of VDD (or the monitored supply rail) while the dashed line represents the UVLO (active low) output. Here, the upper and lower switch points are found to be at 19.5 V and 18.7 V, respectively. During circuit power up, there is a slight rise in UVLOBAR until the supply voltage has risen sufficiently to allow the devices in the signal path to turn on and pull the output low. The output then remains low until the monitored rail reaches 19.5 V, at which point it is de-asserted. The output then remains asserted until the rail drops below 18.7 V, at which point it is re-asserted. The output changes state as the monitored rail experiences several excursions through the switching points. It is important to point out that since the final output stages are tied to the rail being monitored,

the output never reaches a higher voltage than the rail itself. However, the outputs are still well above the threshold needed to drive the next stage of logic.

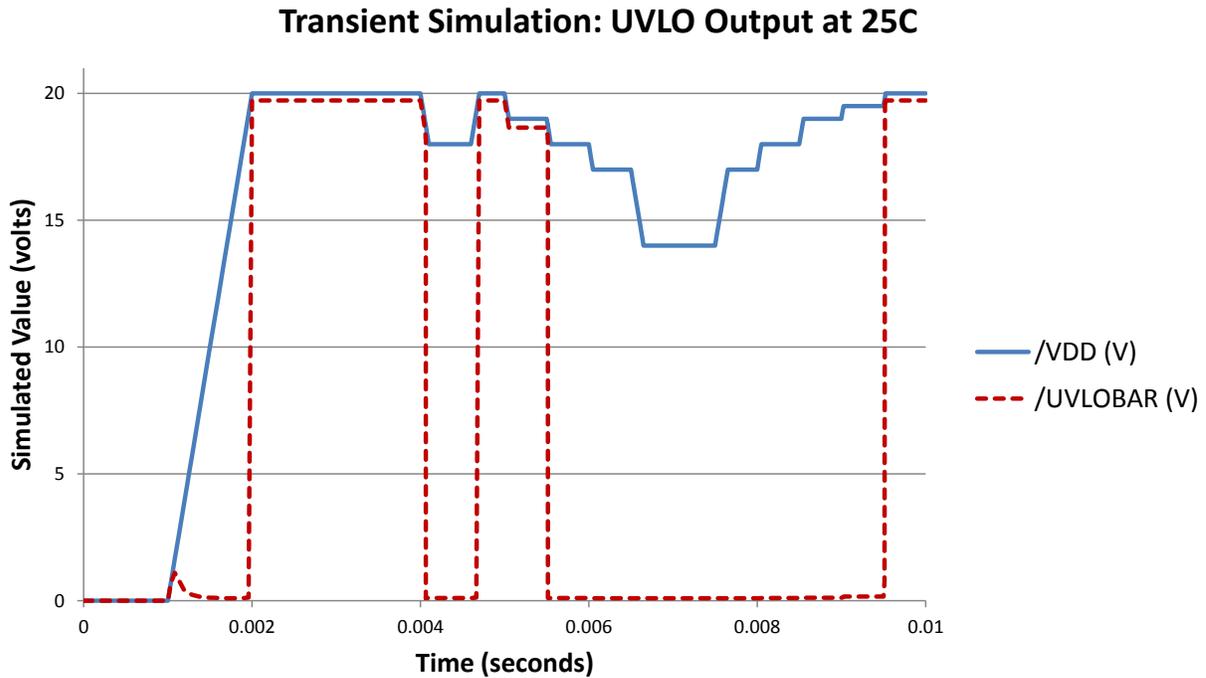


Fig. 26. Transient simulation of the UVLO at 25 °C.

The waveforms shown in Fig. 27 and Fig. 28 represent the output of the UVLO circuit at 125 °C and 225 °C (respectively) using an external voltage regulator. In the first of these waveforms, the switching thresholds are still very near the 18.2 V and 19.5 V as seen in the waveforms simulated for 25 °C. In the waveform for 225 °C, however, the switching points and hysteresis voltage have both gone down with an increase in temperature; here, there are switch points at 18.7 V and 18.2 V. While the upper switch point has shifted down by 1.3 V, the lower switch point has shifted down by only 0.5 V over the 200 °C range.

It is important to note that in all cases the final switch points for indication of a fault condition are still well above the 14 V originally noted as the lowest safe operating voltage. While not ideal behavior, this 2.5% shift seen over temperature in the simulation was deemed acceptable in light of the time pressures leading up to the first tape out.

Unfortunately, as will be seen later, the lack of temperature models for the diffusion resistors leading up to the first tape out would result in considerable differences between the simulation waveforms and the actual circuit waveforms at elevated temperatures.

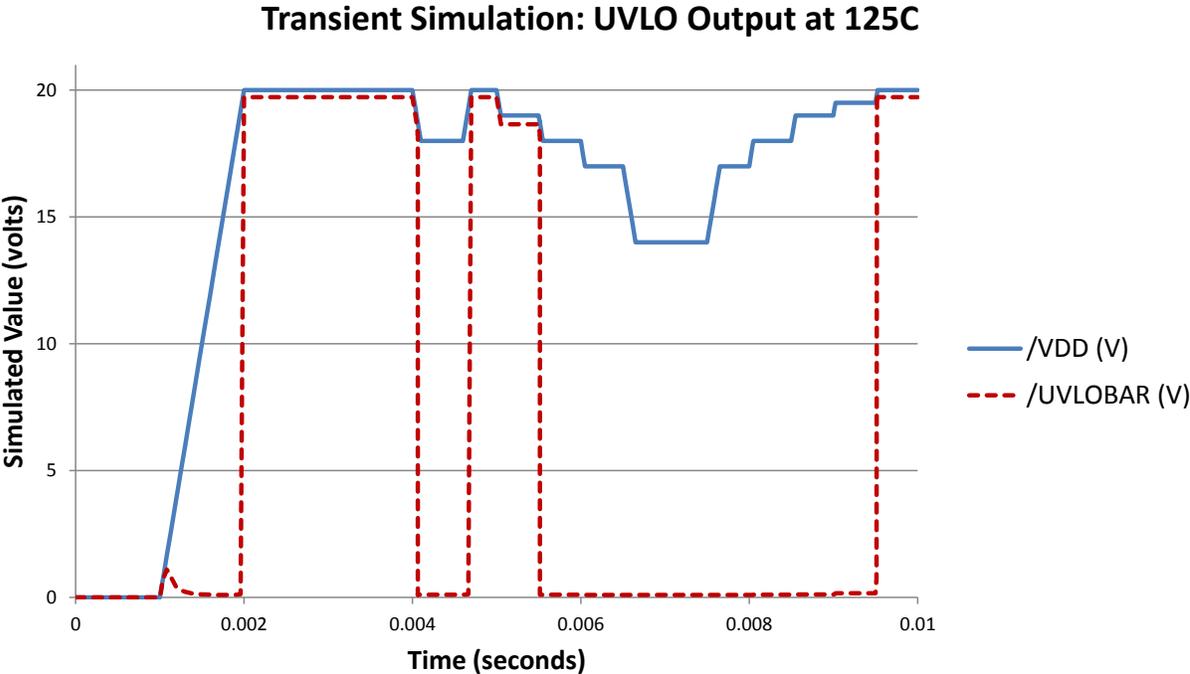


Fig. 27. Transient simulation of the UVLO at 125 °C.

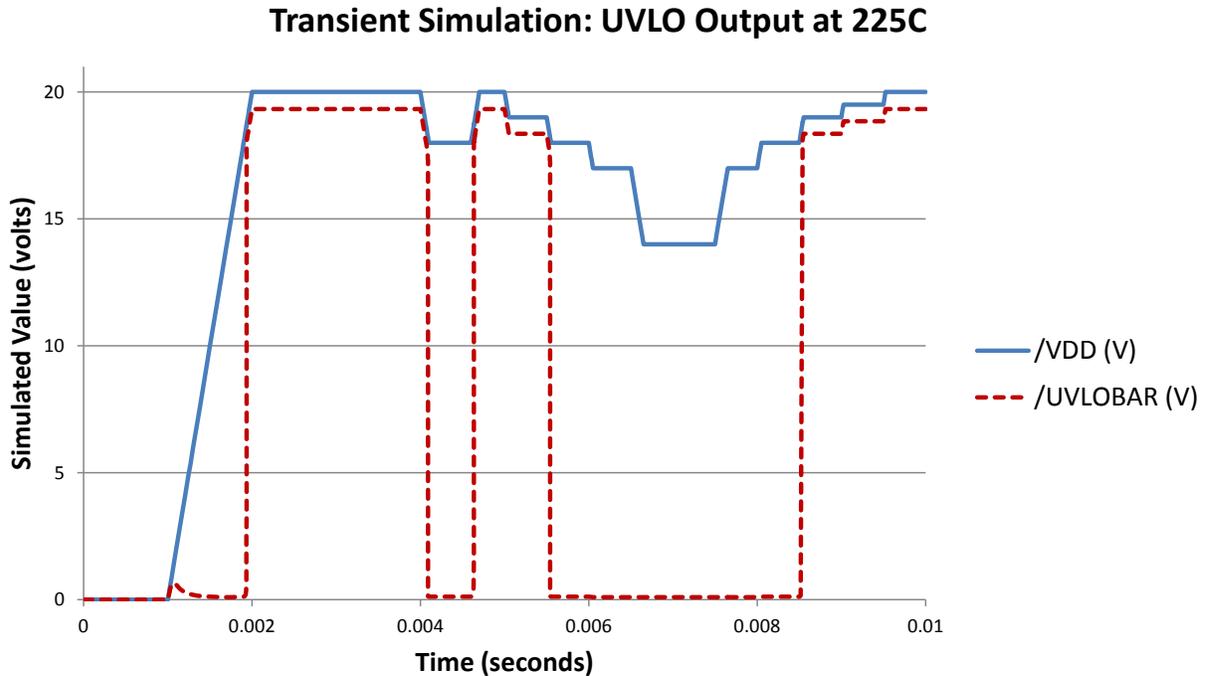


Fig. 28. Transient simulation of the UVLO at 225 °C.

3.2 Layout for Fabrication Run One

Layout of the design was accomplished using Cadence and the Process Development Kit (PDK) designed by UA researchers. This effort was completed in time to meet the tape out deadline in November 2011. A view of the final layout cell containing the full UVLO circuit, including the voltage regulator, the switching circuit, hysteresis control, and the output buffer can be seen in Fig. 29. The scales shown in axes of the figure are in microns, giving an overall layout area of $854.5 \mu\text{m} \times 786.5 \mu\text{m}$ ($672,064 \mu\text{m}^2$). The power supply rail (VDD, 20 V) is located at top, while the ground connection (VSS) is located at bottom. Substrate contacts can be clearly seen in the ground bus and throughout the layout where the ground connection is routed. The connection for the externally regulated supply (10 V) is located in the upper-right. It is connected directly to a small bond pad that allows for use of the external supply or (when

bonded to the other pad nearby) the use of the internal voltage regulator. The remaining connections from top-to-bottom on the right side are VMONR1, UVLOBAR (the output), VMONR2, and VMONNEG.

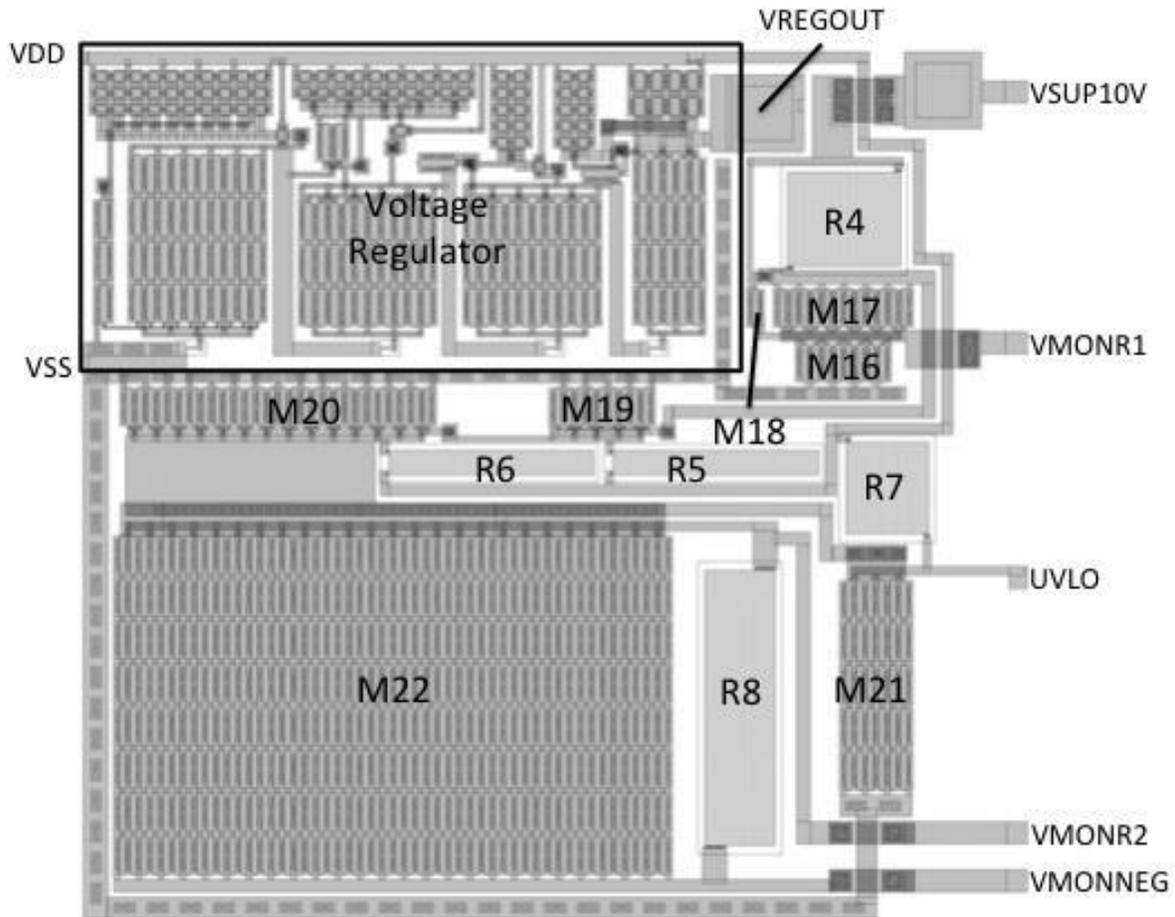


Fig. 29. Layout of the UVLO circuit for Fabrication Run One.

The layer map for the process is shown in Table 8. P-cells (programmable cells) were available in the PDK to generate valid instances of the individual devices and to generate resistors based on the length, width, and line count parameters passed in from the schematic. Therefore, once the necessary devices were generated and placed into the design, much of the

layout effort was centered on tying together devices using the POLY and METAL layers and optimization to minimize the layout footprint.

TABLE 8. LAYER MAP FOR THE CREE PROCESS

Layer name	Description
POLY	Polysilicon
METAL	Metal
ACTIVE	Cut through field ox
NDIFF	n-type diffusion
PDIFF	p-type diffusion
RESISTOR	Virtual; marked resistors for parameter extraction
CAPACITOR	Virtual; marked resistors for parameter extraction
THRESHOLDENH	Threshold adjust enhance (increase V_T)
THRESHOLDDEP	Threshold adjust deplete (decrease V_T)
NPLUS	n+ diffusion
PPLUS	p+ diffusion

Design rules for the process are shown for reference in Table 9. These rules were embedded in the PDK and used for automated Design Rule Checking (DRC). As is readily apparent, the minimum feature sizes used are quite large compared to modern silicon-based processes.

TABLE 9. DESIGN RULES FOR THE CREE PROCESS

	Length / Distance (μm)
Spacings (minimum)	
NPLUS	2
POLY	2
METAL	5
OHMIC_CONTACT	2
ACTIVE	5
VIA (last)	20

PPLUS	2
POLY to NPLUS, ENHANCEMENT, DEPLETION	0.5
Minimum Widths	
POLY	2
NPLUS	2
THRESHOLDENH	2
THRESHOLDDEP	2
ACTIVE	5
OHMIC_CONTACT	2
METAL	5
VIA (last)	10
PPLUS	2
Enclosure (minimum)	
CONTACT by METAL	1
CONTACT by POLY	2
CONTACT by PPLUS	1
CONTACT by NPLUS	1
Overlap	
OHMIC_CONTACT overlaps METAL, POLY, NPLUS, PPLUS, ACTIVE	N/A

3.2.1 Challenges

One challenge presented by the layout was spawned by the fact that only one metal layer was available for routing. For cases such as the one seen in Fig. 30, this meant that a relatively large area was required to transition from metal to polysilicon and then back to metal without incurring a significant penalty in terms of parasitic resistance. This type of constraint applied not only to the metal/polysilicon trace widths, but also to the size of the contacts used to connect to diffusion resistors. It was not learned until after the first fabrication run that the

contact resistance for these was $5 \text{ k}\Omega/\mu\text{m}^2$, which could result in a significant resistance value error if not taken into consideration. Thus, simply using the minimum size contact resulted in $1.25 \text{ k}\Omega$ of series resistance in the trace. Unfortunately, the impact of contact resistance was not known to the design team prior to the tape out for Fabrication Run One; it was, however, given more consideration in the second run.

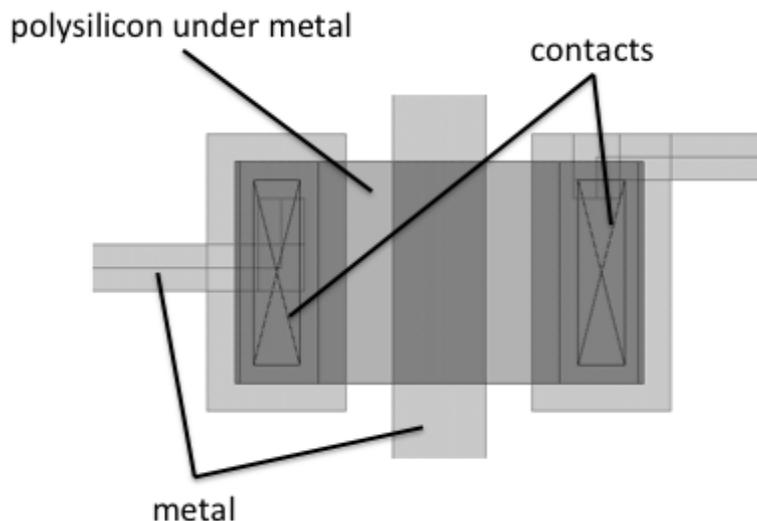


Fig. 30. Example of tunneling under a metal trace using the POLY layer.

Another considerable challenge was to design the circuits for operation across a wide temperature range from $25 \text{ }^\circ\text{C}$ to $225 \text{ }^\circ\text{C}$. Unfortunately, for Fabrication Run One, the PDK did not include temperature coefficients for the resistors in the process, which meant that simulation waveforms at higher temperatures were ultimately misleading. As will be seen in the results section to follow, this led to misplaced confidence in simulation results that resulted in performance issues at higher temperatures.

3.3 Testing for Fabrication Run One

This section provides an overview of the apparatus and procedures used for device testing and experimental results. Due to a lag in the project schedule that was caused by the effort necessary to package the die, some preliminary testing was performed before packaging and more comprehensive testing was performed using the full experimental apparatus after packaged die were available from APEI.

Preliminary testing of the die was accomplished by manually probing the die on the probe station shown in Fig. 31. By probing manually, it was possible to apply power to the temperature sensors and the voltage regulator in order to see if they were operational and to collect some data on device performance. Individual NMOS devices were also placed in the design; thus, curves from these devices captured by the modeling team were compared with simulation results to gauge how closely the modeling approached the actual fabricated devices.

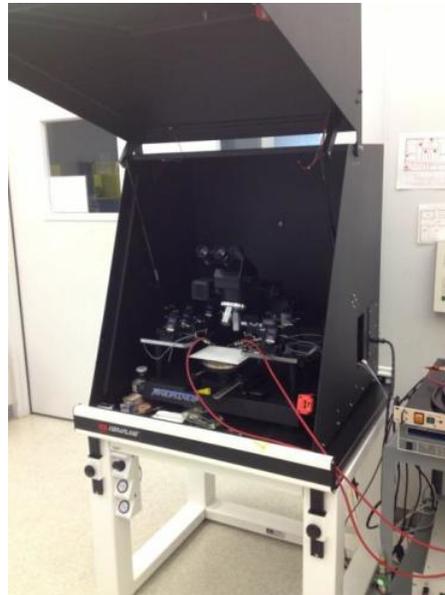


Fig. 31. Photograph of the probe station used in early testing.

Full testing of the UVLO and associated circuits on the die was accomplished by packaging the die in 100-pin, off-the-shelf packages that had sufficient pin count and were tolerable of the temperature range planned for testing (25-225 °C). Initial samples of the packaged die were placed on a Direct-Bond Copper (DBC) board, which acted as an interposer and solved the issue of how to apply heat to the device under test (DUT) without damaging other components required for testing. Connections from the DBC board to other boards or instruments were accomplished via Teflon[®] coated wire capable of withstanding temperatures of 400 °C. The wires were connected to the DBC via screw terminals that were soldered to the traces on the DBC. These wires were then connected to a breadboard and/or instrumentation to facilitate testing. Subsequent testing was conducted using an updated version of the interposer board design realized using printed wiring board technology on Rogers Corporation RO4350B™ board material. The switch to the Rogers material from DBC was made to expedite the fabrication of the boards and to save time that could be spent on other project activities. Previous experiments at APEI had indicated that the Rogers boards could withstand temperatures in excess of 300 °C for short periods, making them suitable for the proposed testing.

A flowchart for the UVLO testing plan is shown in Fig. 32. Shown are the basic steps needed to make the required initial adjustments for the UVLO on a given DUT and capture data over temperature. This flowchart highlights only those steps necessary for testing of the UVLO and temperature sensor. A more complex testing plan was necessary to incorporate the steps needed to test the other fault detection circuitry and gauge overall system performance for other subcircuits, including those for the fault logic and overcurrent protection. For these circuits, certain inputs had to be tied to appropriate voltage levels in order to enable/pass-through signals

to allow the output of the UVLO to be observed. For example, the inputs for the overcurrent protection circuit were tied to ground in order to disable operation of the circuit.

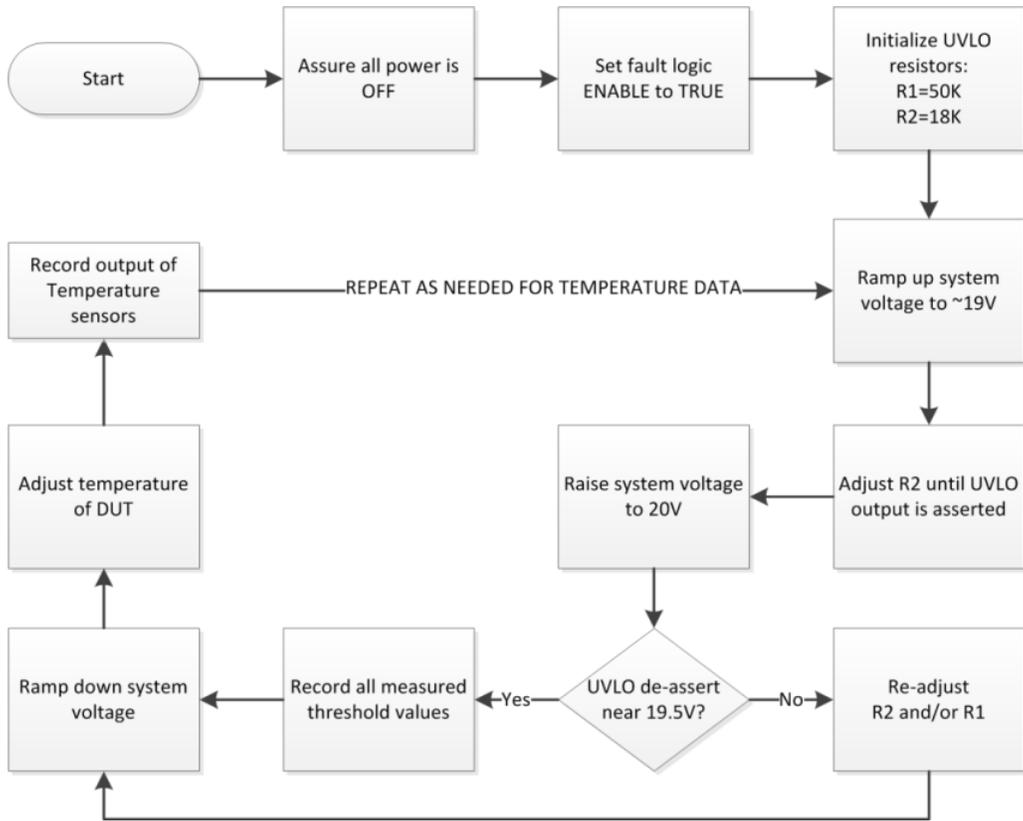


Fig. 32. Flowchart for the UVLO testing plan.

3.3.1 Initial Testing

Initial “heartbeat” testing occurred on the probe station. Since the number of probes was limited to four or less, effort was centered on probing the 15 V regulator and the temperature sensor. Each of these subcircuits required only three probe connections: power, ground, and output. Both epitaxial and implant devices were available, and a number of die were probed from each wafer type. No working circuits were found on the implant device wafer lot, a circumstance which was mirrored in the experimental results for other circuits.

The measured output of the UVLO regulator on epitaxial die 1-4 at room temperature is compared with that of the simulated waveform in Fig. 33. The measured results are a close match with the simulated waveform shown in Fig. 21. The final output voltage for the simulated waveform was ~15.3 V, while the measured value was 15.1 V. These initial results were quite encouraging, since the measurements were close to the anticipated values. Measured data for the temperature sensor was also encouraging, and is presented in Appendix A.

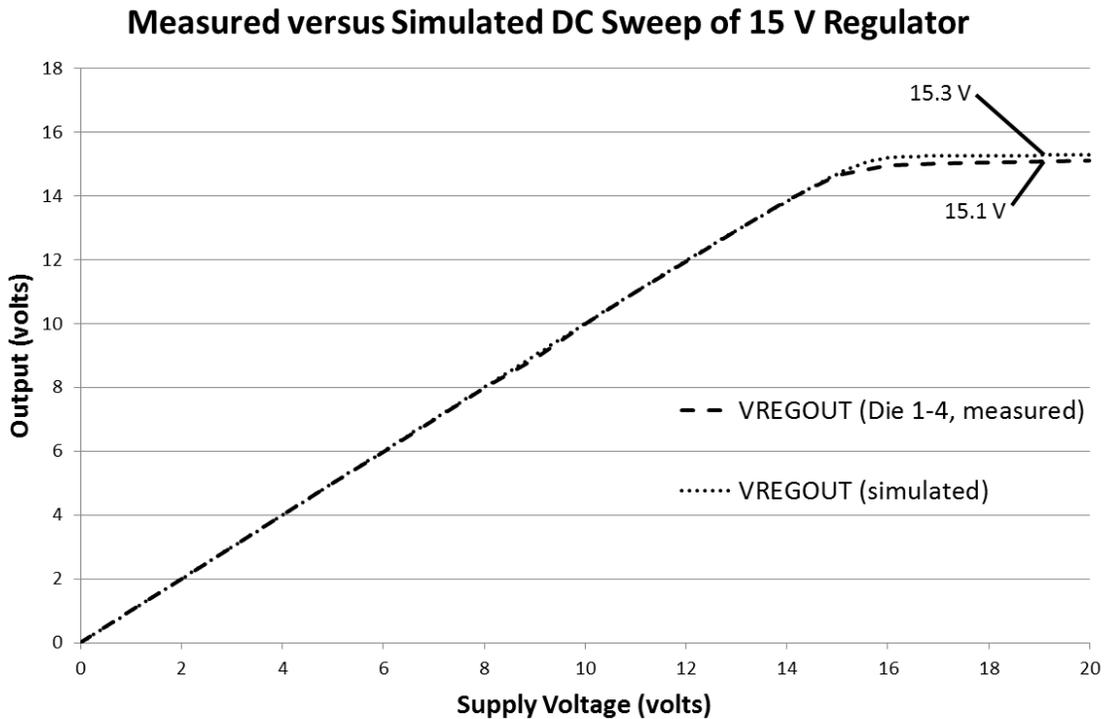


Fig. 33. Measured versus simulated DC sweep of the 15 V regulator.

3.3.2 Packaging for Test

In order to facilitate testing, the die was packaged in an off-the-shelf, 100-pin CQFP package (Kyocera part no. CCF10008) by APEI. This package was chosen because it was ceramic-based (and would thus be able to tolerate the temperatures anticipated during testing), had an adequate pin count, and because its cavity size of 0.355" x 0.355" allowed it to contain the

gate driver die with sufficient clearance for wire bonding. A photo of one of these packages mounted on a Rogers 4350-based PCB is shown in Fig. 34. The wires insulated with Teflon® can be clearly seen terminating at the terminal blocks on the board.

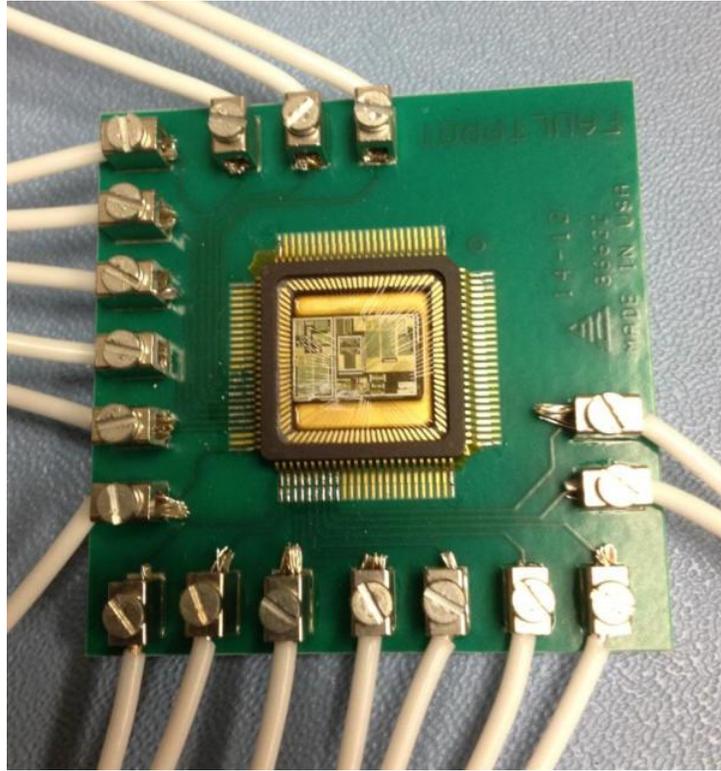


Fig. 34. Photo of the fault protection test board used in Fabrication Run One.

A wire bond diagram for the package configuration tested is shown in Fig. 35 [39]. It is important to note that APEI engineers chose the placement of bond wires to maximize manufacturability by attempting to minimize bond wire length and by avoiding the crossing of wires whenever possible. Even so, the resulting bond pattern was quite complex.

Before the PCBs based on Rogers material were fabricated, the packaged parts were attached to direct bond copper (DBC) boards for testing. This was done primarily to expedite the testing process in order to meet a delivery deadline. A photograph of the patterned DBC substrates used for early testing can be seen in Fig. 36. The panel seen in the image was plated

with nickel using an electroless process and was then diced into individual test substrates. Later, to facilitate testing at higher temperatures using more accurately patterned boards, devices were packaged on the RO4350B™ boards using the same design. One of these boards was used to characterize the temperature sensor over a wider temperature range by enabling it to be put into a thermal cycling chamber.

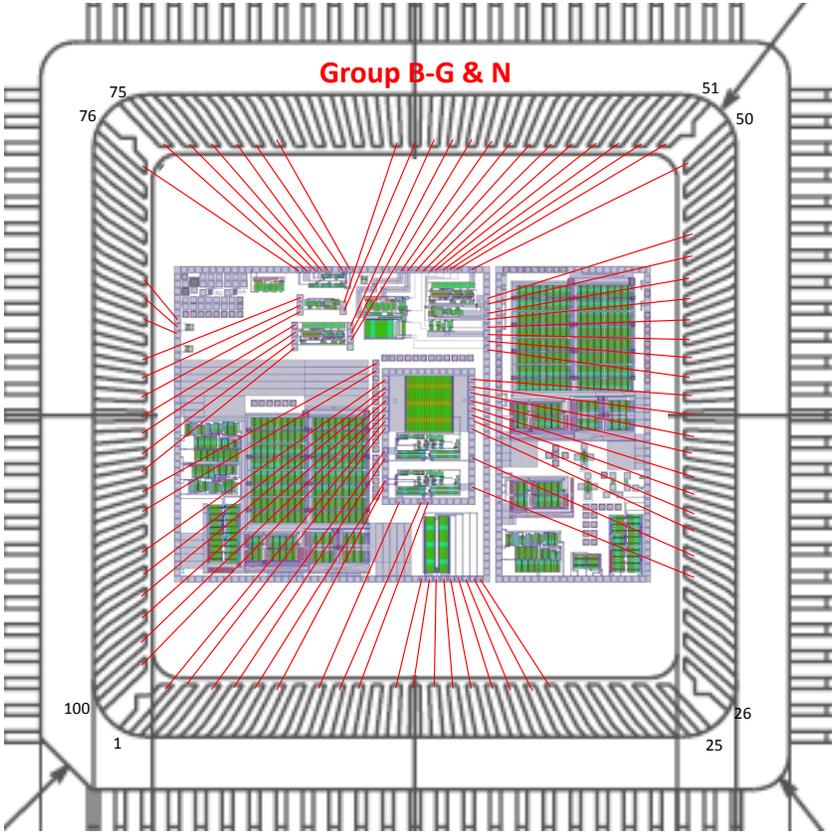


Fig. 35. The wire bond diagram for the packaged die tested. Image courtesy of APEI.

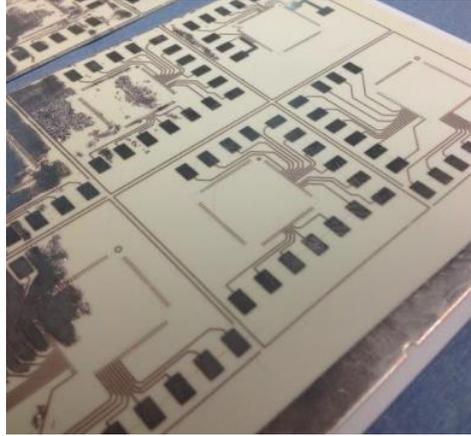


Fig. 36. Patterned DBC substrates used for early testing before dicing.

3.3.3 Testing Apparatus

A block diagram of the apparatus used for testing the die is shown in Fig. 37. In this diagram, the digital multi-meter (DMM) used was a Hewlett Packard 3458A and the power supply was a Hewlett Packard E3631A. These instruments were each controlled via their IEEE-488 port, also known as a General Purpose Interface Bus (GPIB) port. A ProLogix GPIB-to-USB adapter was used to connect the GPIB devices to a laptop PC. The ProLogix adapter was chosen because it auto-translates data to/from the GPIB bus over a Universal Serial Bus (USB) connection using a “virtual” serial port on the PC [40]. Using this adapter, it was possible to communicate and control the GPIB devices using the Python scripting language. Since other students had used other Python scripts to automate testing in the past, this allowed existing code to be leveraged by simply writing an importable Python module that mimics the API used by other Python-based control libraries (e.g., the pyVISA library). Results from each voltage sweep were saved by the software to Comma Separated Value (CSV) files to simplify the process of importing the data into Excel (or other tools) for analysis.

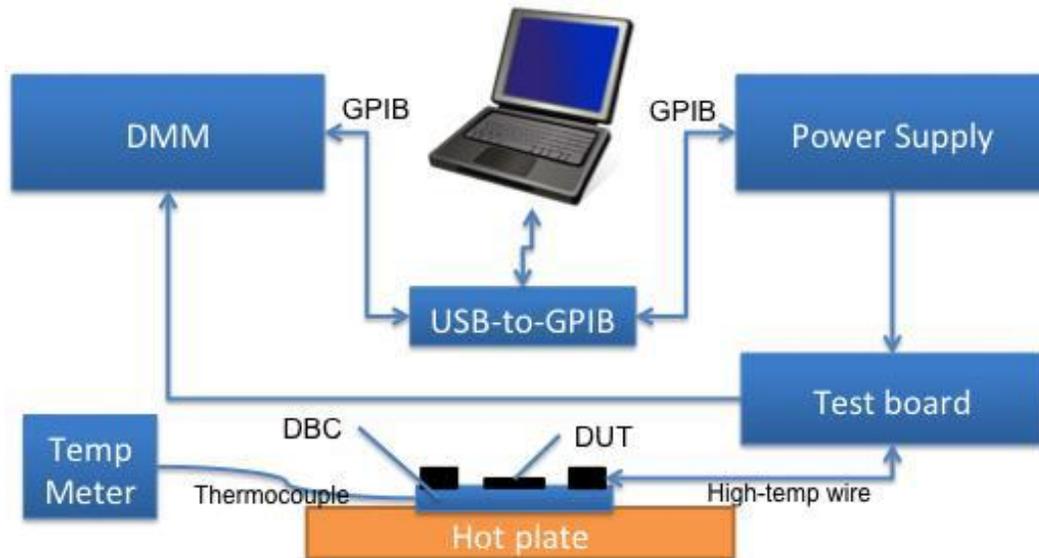


Fig. 37. Block diagram of experimental apparatus.

3.3.4 Results

Capturing data for the UVLO was more difficult than expected due to several factors. First, device yields were relatively low. This meant that as the complexity of any given circuit increased, the probability of finding a working version of that circuit decreased. This alone would not have been cause for concern, since the UVLO circuit itself was relatively small compared to some of the other circuits on the die. However, when the die arrived at UA it was discovered that standalone versions of the UVLO and two of the three standalone temperature sensors had been dropped out of the design data before mask fabrication. After an investigation by the UA team, it was discovered that certain cell names used when generating the final GDSII data had been in excess of 32 characters in length, which caused the tool used by Cree (LASI) to drop out those cells. After confirming this as being the issue, the UA team and Cree created a new workflow to avoid the issue for further tape outs.

Unfortunately, the lack of a standalone version of the UVLO meant that testing could only be performed on the UVLO cell that was connected to the fault logic and overcurrent protection circuits. This presented a considerable problem, since the output for the UVLO cell in this particular circuit block had not been routed to an external pin and was thus not directly observable. Ideally, it would be possible to view the output of the fault current logic to sense switching of the UVLO, but low yields prevented the discovery of a working UVLO where the other fault circuits were also fully functional.

While the UVLO output could not be directly observed, however, the connections for the resistors used for setting the switch points were routed to external pads. This allowed the monitoring of the voltage drop across the internal hysteresis resistor and made it possible to detect when the UVLO was switching without directly measuring the output. A captured waveform for a functional UVLO found using this approach at room temperature is presented in Fig. 38. Here, after the external input resistors have been adjusted for process variation, the voltage measured across the internal resistor is found to be transitioning at switch points occurring near 18.5 V and 19.0 V; the small shift seen can easily be accommodated by adjusting the external resistors. More importantly, however, hysteresis is present, although (at 0.35 V) it is slightly less than the simulated amount of 0.85 V. The choice to set the switch points approximately 0.5 V higher than the original specification was driven by a discussion among team members that using slightly higher switch points than originally chosen might be desirable. Since the switch points could be shifted by adjusting the external resistors, setting the exact point where switching occurred to match a particular target was considered less critical at the time than capturing the switching behavior of the device over temperature. As the next figure illustrates, switching behavior over temperature was indeed a reason for concern.

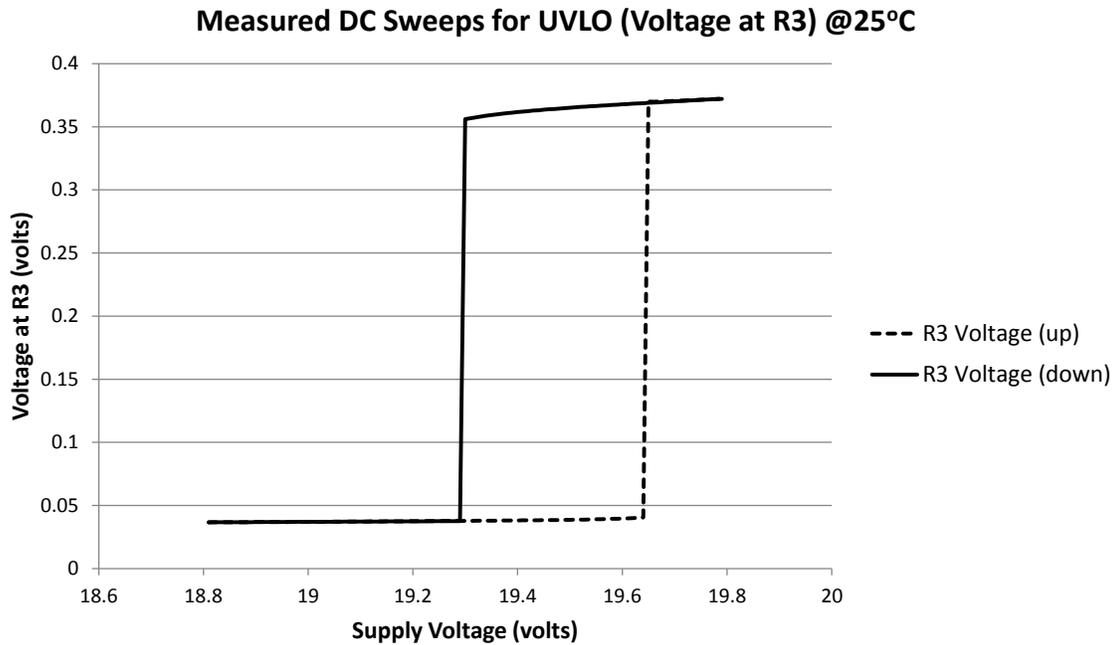


Fig. 38. Measured DC sweep for UVLO (voltage on R_3) at room temperature.

In Fig. 39, the same data has been captured with the circuit at 125 °C. Here the results are less encouraging, as the switch points have shifted downward to near 15.5 V and the amount of hysteresis has collapsed to nearly zero. This data was the first indication that the lack of temperature data for resistors in the PDK had led to a design that was not as stable over temperature as was first thought. Data was not captured at 225 °C since, at 125 °C, hysteresis was nearly absent and the circuit had already failed to meet design requirements.

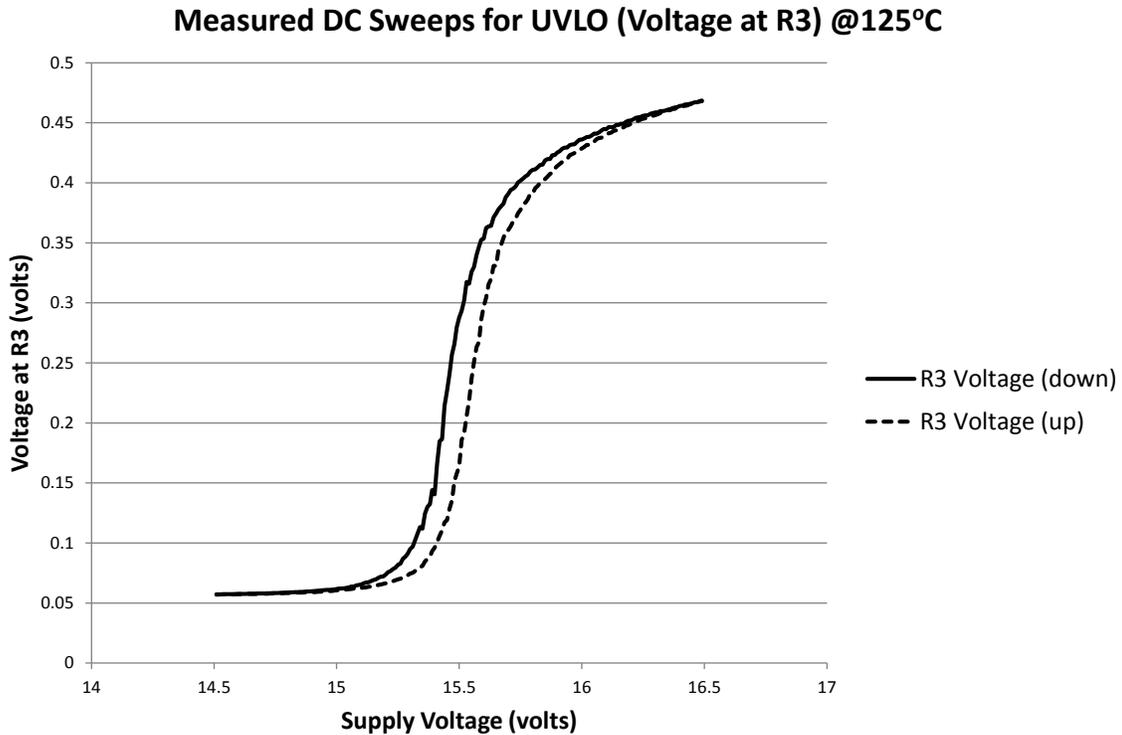


Fig. 39. Measured DC sweep for UVLO (voltage on R_3) at 125 °C.

At this point, testing was halted while new simulations were run. It was at about this time when the resistor models in the PDK were updated to reflect the temperature coefficient present. After re-adjusting component values in the simulation, the resulting waveform exhibited a shape similar to that seen in the measured data in Fig. 39. To some degree, the result was encouraging in that it showed that the simulation matched test bench results. However, it also revealed the shortcomings of the circuit topology when operating over the specified temperature range, making it clear that another circuit approach (and another fabrication run) would be necessary.

While the results garnered from Fabrication Run One were not exactly as desired, they did provide useful insights. It was clear that the behavior of the MOSFETs in the process were

reasonably close to those predicted by the models in the PDK, although better characterization of resistor behavior over temperature was necessary (and was later added). Also, yields were not high, which underscored the importance of minimizing circuit complexity to maximize the probability of producing a working circuit. Finally, a number of workflow issues were uncovered that would be addressed in the next (and future) tape outs.

CHAPTER 4 – FABRICATION RUN TWO

4.1 Design and Simulation for Fabrication Run Two

This chapter provides details on the design, simulation, and layout of the UVLO circuit for the second fabrication run from Cree. Other than using an updated process development kit, the tool chain for the second run was identical to that of the first run. The targeted specifications for the second fabrication run are presented in Table 10. Since it was decided to have both epitaxial and implant versions of the circuits on the tape out, two separate sets of specifications were necessary. This is primarily because Cree recommended staying below 16 V for the gate-source voltage on the implant devices in order to prevent break-down. The epitaxial devices were expected to survive a gate-source voltage of 20 V reliably, and thus the supply voltages and the switch points necessarily had to change.

The amount of hysteresis specified in the table is 0.5 V, although this should be considered the minimal amount desired. While shifting of the switch points would not be preferred, it was more critical that the amount of hysteresis not reduce as temperature increased during operation. This would lead to instability and/or reduced noise margin for the UVLO.

Both epitaxial and implant versions of the UVLO were included in the second fabrication run. Based on early conversations regarding the tape out, it was understood by UA team members that one reticle would be created from all cell designs and then that reticle would be used to fabricate both epitaxial and implant process runs. Following this approach would mean that devices intended for different processes would appear side-by-side on the same cell, although only those devices intended for the process used would be expected to perform as

desired. Versions of the UVLO circuit were ultimately placed on two top-level cells, “UA” and “UA_SPLIT.”

TABLE 10. UVLO TARGET SPECIFICATIONS FOR FABRICATION RUN TWO

UVLO Specification	Value (P-IMP)	Value (P-EPI)	Notes
Positive-going threshold	15.2 V	19.5 V	Updated to higher values as compared to first run
Negative-going threshold	14.5 V	19.0 V	14.5/19 V > Value > 14 V
Propagation delay	< 10 μ s	< 10 μ s	Simulated (w/ parasitics) was: 1.5 μ s (assert) 0.96 μ s (de-assert)
Max. DC current	~1 mA	~1 mA	
Valid logic outputs	“0” \rightarrow < 1.5 V “1” \rightarrow > 8 V	“0” \rightarrow < 1.5 V “1” \rightarrow > 8 V	This was a target. Actual pull-ups were much higher.
Operating temperature	0° \rightarrow 200 °C	0° \rightarrow 200 °C	Nominal temp ~125 °C
Supply voltage (V_{DD})	16 V	20 V	

Since a considerably larger number of die were sent to the UA for evaluation on Fabrication Run Two, UA team members adopted a simple naming scheme to allow tracking of individual die during testing. The die were provided in die trays with a 5 x 5 array of pockets. A convention was adopted whereby the chamfered corner of the tray was located in the upper right and the die were assigned labels based on their location in the tray with the upper left-hand corner used as a reference. For example, the die in the upper-left hand corner (row 1, column 1) became R1C1. The die immediately to the right of R1C1 was R1C2, and so on. Thus, any

particular die could be referenced by appending this label to the name of the wafer lot and cell name. For example, a valid die reference would be “JU0505-29_UA-SPLIT_R1C2”. This naming convention will be used throughout this chapter in order to reference particular die that were tested.

4.1.1 Lessons Learned

Having been through the trials seen in the first fabrication run, the design process for the second run was entered with a number of new points in mind, based on lessons learned from the first run and based on new information learned from Cree since the previous tape out. After the temperature coefficients for the diffusion and polysilicon resistors were added to the PDK, it had been learned during the first fabrication run that the device models were reasonably accurate. This knowledge was based on data captured from discrete devices and on the fact that the outputs for circuits such as the voltage reference were relatively close to simulated values. It was also now known that the impact of temperature on diffusion resistors could not be ignored, so the fact that the temperature coefficients for diffusion- and polysilicon-based resistors had been added to the PDK built considerable confidence in simulation results.

4.1.2 New Constraints

A listing of key changes for the second fabrication run is shown in Table 11. During team discussions, it was decided to omit depletion devices from the second fabrication run due to low device yields and inconsistent device behavior. The lack of depletion devices in the second run meant that circuits such as the temperature sensor and the voltage reference would have to be completely re-designed in order to be included on the new run. Both epitaxial and implant versions of the circuits were to be fabricated and, since the two processes had different maximum gate-source voltages, it was necessary to modify resistor sizes in the design because

sheet resistance in the resistors was expected to be different for each process as well. This meant that the physical size of all the resistors in the design had to be adjusted, depending on which process was to be used for a given design cell.

It is important to reaffirm that the only circuits that were compatible with integration with power devices were those with devices based on the implant process. However, since epitaxial devices yielded better on the previous fabrication run, it was decided by the collaboration team to fabricate circuits using both processes in order to increase the chances of yielding functional circuits so that the effectiveness of new design topologies could still be evaluated.

Finally, it had been uncovered after discussions with Cree subsequent to the first fabrication run that the contact resistance between metal and diffusion resistors was much higher than previously thought. This high contact resistance, on the order of $5 \text{ k}\Omega/\mu\text{m}^2$, meant that contacts to diffusion resistors had to be made as large as was practical and that simply using the minimum contacts automatically generated by the via p-cell in Cadence (as was done in the first fabrication run) would not be acceptable.

TABLE 11. KEY DESIGN CHANGES FOR FABRICATION RUN TWO

Change in Fab Run Two	Impact
No depletion devices	All circuits relying on depletion devices required redesign to use resistors for pull-up
Both implant and epitaxial versions to be fabricated	Two versions of the UVLO were necessary to accommodate differences in resistor sheet resistance
Implant devices could not withstand a gate-source voltage greater than 16 V	UVLO circuits had to be adjusted to accommodate different supply voltages and switching points
Contact resistance from METAL to a diffusion resistor greater than originally thought	Additional space required in all circuits to allow larger contacts and reduce inline parasitic resistance

4.1.3 UVLO Circuit Topology for Fabrication Run Two

A simple inverter with a resistor-based pull up is shown in Fig. 40. As has already been presented through simulation, the switch point for this circuit is dependent on the value of the resistor R_I and the pull down strength (i.e., multiplicity) of M1. For any increase in the voltage at IN, there is a corresponding voltage decrease at OUT. As R_I is made larger for the same input, the voltage at OUT decreases yet further. Ultimately, there is a balance between the minimum voltage that can be achieved at OUT, the amount of current dissipated, and the rise time of the output as the load capacitance is charged through R_I . Thus, there are extreme values of R_I that might be unacceptable due to the minimum output voltage being too high or because the rise time was too long. The point to be taken, however, is that within a certain region of operation, minor fluctuations of R_I due to temperature tend to cause the switch point of the circuit to shift as well. As the temperature increases, the corresponding increase in the value of R_I tends to make the output go low for a lower voltage at the input, i.e., the switch point shifts downward.

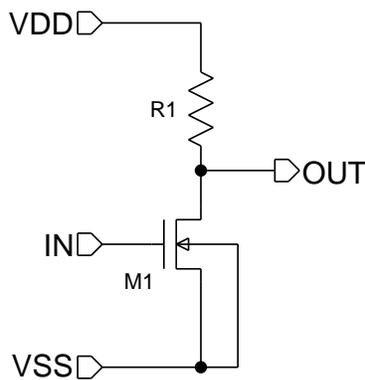


Fig. 40. A simple inverter with resistor-based pull up.

In addition to the downward shift in switch point due to the rising value of R_I , it is also the case that the threshold voltage V_T for M1 would tend to decrease with an increase in temperature [22]. Assuming that the source-body voltage is zero, the formula for charge density in the depletion region is given by:

$$Q_b = \sqrt{2qN_A\epsilon 2\phi_f} \quad (4.1)$$

where q is the charge on an electron in coulombs, N_A is doping density in atoms/cm³, ϵ is the dielectric constant, and ϕ_f is the energy needed to invert the channel in eV. This can be substituted into Eq. (2.5) to yield:

$$V_{t0} = \frac{\sqrt{2qN_A\epsilon(2\phi_f)}}{C_{ox}} + 2\phi_f + \phi_{ms} - \frac{Q_{ss}}{C_{ox}} \quad (4.2)$$

It is assumed that ϕ_{ms} , Q_{ss} , and C_{ox} are temperature independent. Differentiating Eq. (4.2) then yields:

$$\frac{dV_{t0}}{dT} = \frac{\sqrt{2qN_A\epsilon(2)} d\phi_f}{2C_{ox}\sqrt{\phi_f}} + \frac{2d\phi_f}{dT} = \frac{d\phi_f}{dT} \left[2 + \frac{1}{C_{ox}} \sqrt{\frac{qN_A\epsilon}{\phi_f}} \right] \quad (4.3)$$

Also:

$$\phi_f = \frac{kT}{q} \ln \left[\frac{N_A}{n_i} \right] \quad (4.4)$$

where k is Boltzmann's constant, T is temperature in kelvin, q is the charge on an electron in coulombs, N_A is doping density in atoms/cm³, and n_i is the intrinsic carrier concentration. The intrinsic carrier concentration is defined as:

$$n_i = \sqrt{N_c N_v} e^{-\frac{E_g}{2kT}} \quad (4.5)$$

where E_g is bandgap of the semiconductor at $T = 0$ K, N_c is the density of states near the conduction band, and N_v is the density of states near the valence band. Substituting Eq. (4.5) into Eq. (4.4) gives:

$$\phi_f = \frac{kT}{q} \ln \left[\frac{N_A e^{\frac{E_g}{2kT}}}{\sqrt{N_c N_v}} \right] \quad (4.6)$$

Assuming that the density of states at both bands is independent of temperature, Eq. (4.6) is differentiated to yield:

$$\frac{d\phi_f}{dT} = \frac{kT}{q} \left[-\frac{E_g}{2kT^2} \right] + \frac{k}{q} \ln \left[\frac{N_A e^{\frac{E_g}{2kT}}}{\sqrt{N_c N_v}} \right] \quad (4.7)$$

Substituting Eq. (4.6) into Eq. (4.7) gives:

$$\frac{d\phi_f}{dT} = -\frac{E_g}{2qT} + \frac{\phi_f}{T} = -\frac{1}{T} \left[\frac{E_g}{2q} - \phi_f \right] \quad (4.8)$$

Finally, substituting Eqs. (2.7) and (4.7) into Eq. (4.3) produces:

$$\frac{dV_{t0}}{dT} = -\frac{1}{T} \left[\frac{E_g}{2q} - \phi_f \right] \left[2 + \frac{\gamma}{\sqrt{2\phi_f}} \right] \quad (4.9)$$

From Eq. (4.9) it is observed that the change in the threshold voltage is inversely proportional to temperature, which would tend to cause pull down devices to switch on at a lower gate-source voltage as temperature increases.

As already mentioned, the Cree MOSFETs also exhibit an improvement in carrier mobility as temperature increases. This effect means that M1 exhibits a lower $R_{DS(ON)}$ with an increase in temperature, which would tend to cause it to pull down more effectively when turned on.

In Fig. 41, the Schmitt Trigger configuration used in both the first and second fabrication runs is shown. While operation of the circuit is somewhat more complicated than that of the simple inverter, it is still evident that temperature changes would cause shifts in the value of R_I and the threshold voltage, thus causing the output to drop more quickly for a given input, thus shifting the switch points lower.

through the resistor), finding a way to modify the current through the circuit as the temperature changed was considered to be a viable solution.

One approach to implementing this method is presented in Fig. 42. Here, the circuit in the previous figure has been modified so that M1 is now continuously biased. Also, a new resistor R_2 has been added. This new topology effectively steers current between two legs, one containing M2 and another containing M3. Operation is very similar to that of the original topology; however, the addition of R_2 now allows the gate-source voltage for M2 to be manipulated, affording some control of the switch points of M2. The effect of the value of the source resistor R_2 on the circuit at a given temperature is shown in Fig. 43. Here, as the value of R_2 increases, the switch points for the circuit are shifted up as well. This allows finer control of the hysteresis in the circuit and, in combination with the front end resistors, allows placement of the switch points at practically any level.

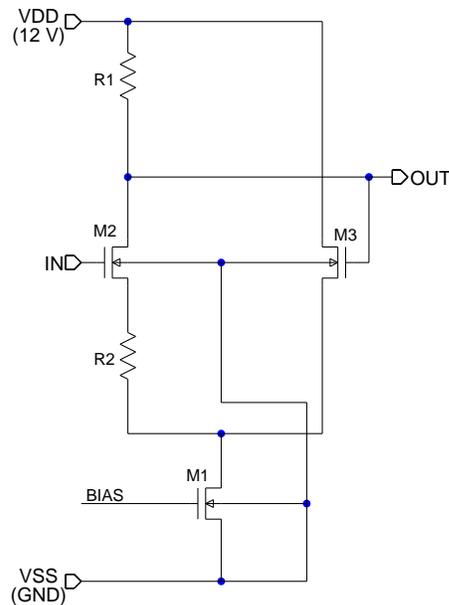


Fig. 42. A modified Schmitt trigger topology.

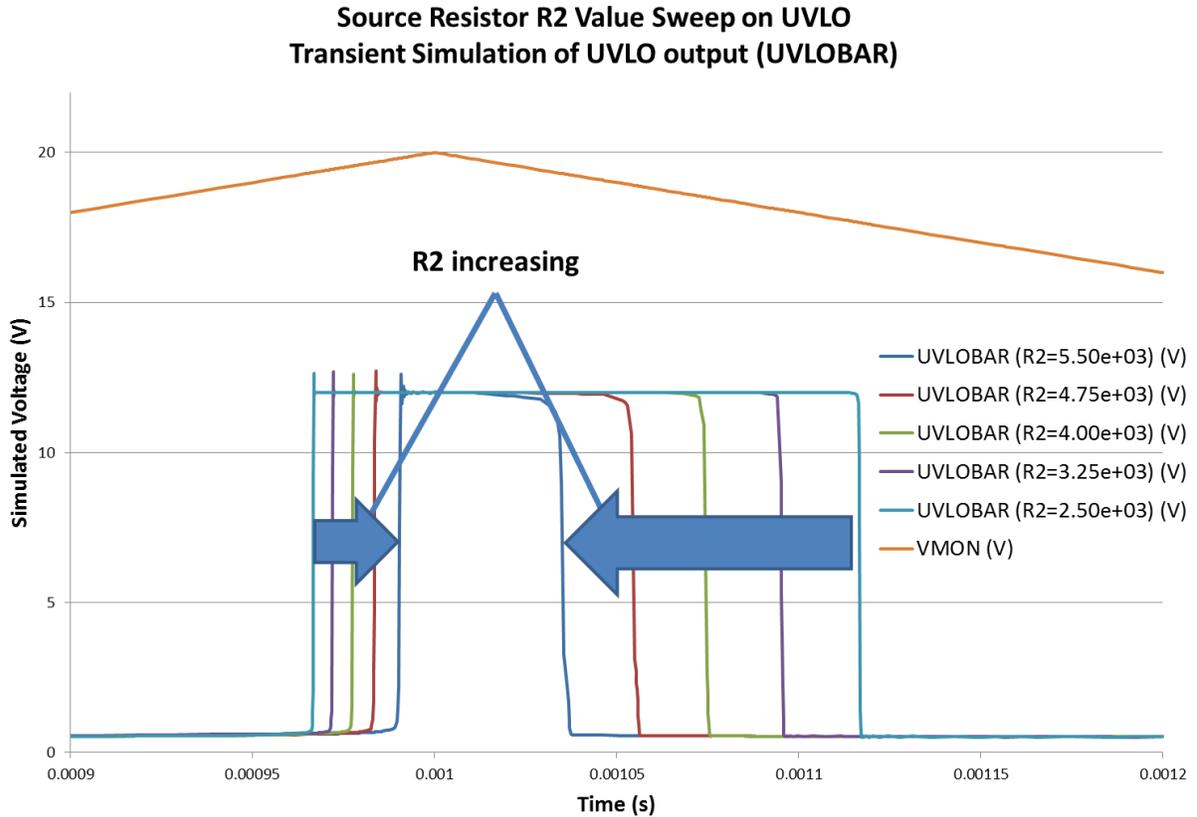


Fig. 43. The effect of changing the value of source resistor R_2 .

For a given current through R_2 , the increase of R_2 with temperature would cause a corresponding voltage rise at the source of M2 that would raise the switch point of the circuit to partially offset the effects mentioned previously. The method used to accomplish this biasing change is shown in Fig. 44. Here, the components R_3 and M4 have been added. R_3 , M4, and M1 form a resistor-biased current source. As the value of R_3 increases with temperature, the current through M4 decreases, ultimately causing the current through M1 to decrease. This offset of current with temperature can be adjusted by sizing R_3 , M4, and M1. Since the equivalent resistance that M1 presents to the circuit increases for a lower V_{GS1} , the voltage at the drain of

M1 increases also. This change in voltage leads to an increase in the voltage at the source of M2, which tends to counteract the drop in V_T that occurs with an increase in temperature.

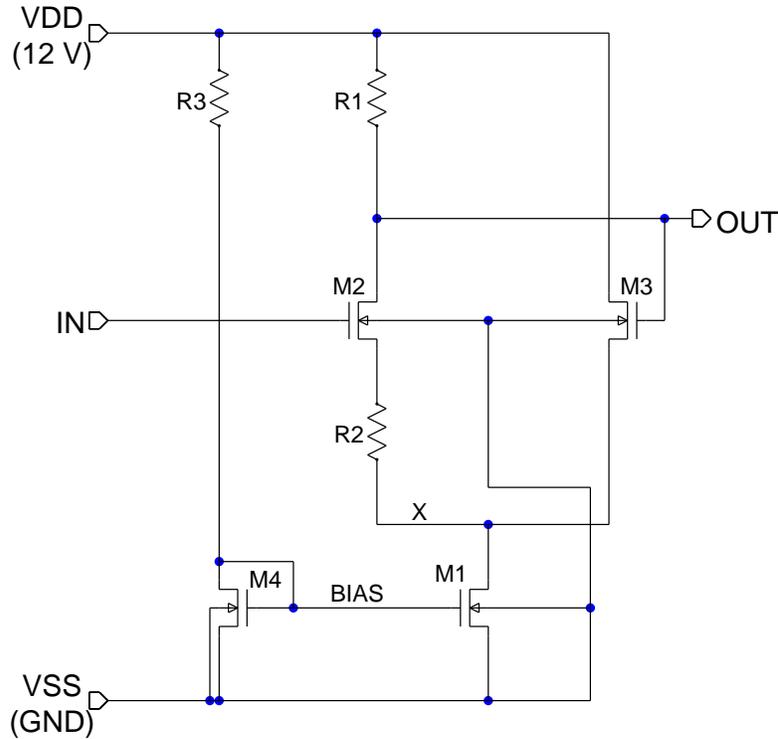


Fig. 44. The modified Schmitt trigger with a resistor-based bias in the current mirror.

The UVLO circuit can be viewed as having three primary functional blocks. The first is a resistor divider block, located on the front end, in which the values of the resistors can be adjusted to set the switch points to the desired level for the monitored rail. Details on the design of the voltage divider will not be discussed, as it is a simple calculation once the desired switch point and the switch point for the next stage is known.

The design of the next two sections can be started by describing their functionality as separate blocks. Before doing this, the problem must be constrained by making reasonable choices for certain key parameters. Some of these initial choices are shown in Table 12.

TABLE 12. INITIAL PARAMETER CHOICES FOR UVLO FABRICATION RUN TWO

Parameter	Value	Justification
Supply voltage (V_{DD})	12 V	Output adequate to drive additional stages; common voltage in automotive applications; readily available at the system level
K'_N	$0.5 \mu\text{A}/\text{V}^2$	Shown to give consistent calculation results based on early simulation work
W/L	32 / 2	These devices were among the earliest devices modeled and were generally considered to be the most proven
V_{TN}	3 V	Based on simulation and device curves

The functionality of the output stage will be considered first and is outlined in Table 13. This block is an inverter and, since it is expected to drive logic elsewhere on chip, it is desirable for the output swing for this stage to be as near the supply rails as possible to assure complete switching. Per the earlier review of inverter topologies, the Schmitt trigger topology shown in Fig. 41 was chosen for switching performance.

TABLE 13. SPECIFICATIONS FOR UVLO OUTPUT STAGE

Parameter	Value	Justification
Output swing (ideal)	0 to 12 V	Assures strong switching in subsequent logic.
Function	Inverter	Generates appropriate logic level output
Topology	Schmitt trigger	Sharp transitions; simplicity.
Switching thresholds	Near 6 V	Chosen because it is $V_{DD}/2$
Hysteresis	1 V	About 10% of V_{DD}
Rise time	$< 2 \mu\text{s}$	Chosen to ~20% 10 μs specification for the UVLO to allow for signal propagation
Output load	15 pF	Chosen because it is ~3x the maximum load actually anticipated

The design for the Schmitt trigger is initiated by choosing a value of R_I based on rise time requirements. Assuming a time constant $\tau = RC$ with $C = 15$ pF, a max rise time of $2 \mu\text{s}$, and the conservative rule that three time constants represent the rise time, a value for R of 44 k Ω is calculated as the upper bound for the pull up resistor. Since a smaller resistor yields a lower rise time and translates to a smaller layout foot print, the choice is made to reduce the size of the resistor by one-third, giving a value for R of 30 k Ω . This translates to a rise time of approximately $1.4 \mu\text{s}$, which is still reasonable and reduces the layout footprint as well.

Referring to Fig. 41, the size of M2 is first determined. Assuming M2 is on, the output voltage is:

$$V_{OUT} = V_{DD} - I_1 R_1 \quad (4.10)$$

where I_1 is the current through M2 and M1. Further, $V_{OUT} = V_{T3} + V_x$, since the circuit is considered to be at the point where M3 begins to turn on and switching occurs (i.e, the point where $V_{IN} = V_{SPL}$). It is also the case that:

$$I_1 = \frac{1}{2} \beta_2 (V_{GS2} - V_{T2})^2 \quad (4.11)$$

$$V_{GS2} = V_{IN} - V_x = V_{SPL} - V_x \quad (4.12)$$

where V_x is the voltage at the source of M2.

It is now possible to solve Eq. (4.10) for I_1 . Substituting this result and Eq. (4.12) into Eq. (4.11), and then solving for β_2 yields:

$$\beta_2 = \frac{2(V_{DD} - V_{T3} - V_x)}{R_1 (V_{SPL} - V_x - V_{T2})^2} \quad (4.13)$$

Upon examination of the circuit, it is noted that V_x will begin floating higher as the switch point of M2 is approached, due to M1 nearing turn off and M3 nearing turn on. To attempt to compensate for this effect, it is assumed for the sake of a starting point that V_x will float to 0.5 V before the switching takes place. Assuming switch points centered at 6 V and with

1 V of hysteresis, this yields a value for V_{SPL} of 5.5 V. Substituting this and other known values into Eq. (4.13), a $W/L=88$ for M2 is calculated. Since 32x2 devices are in use, it is necessary to scale by increments of 16. Therefore, after rounding up, multiplicity for M2 of 6 is chosen.

Per textbook recommendations for a CMOS Schmitt trigger that β_2 be greater or equal to β_3 or β_1 [41], the relationship $\beta_1 = \beta_2$ is assumed. To solve for the multiplicity of M3, it is assumed that the upper switch point occurs when the current through M1 and M3 are equal just before M2 turns on. Setting these currents to be equal yields:

$$\frac{\beta_1}{2}(V_{SPH} - V_T)^2 = \frac{\beta_3}{2}(V_{DD} - V_x - V_{T3})^2 \quad (4.14)$$

It is assumed also that $V_{T2} = V_{T3}$ and also that:

$$V_{SPH} = V_{IN} = V_{T2} + V_x \quad (4.15)$$

It is now possible to substitute Eq. (4.15) into Eq. (4.14), which gives:

$$\frac{\beta_1}{\beta_3} = \frac{(V_{DD} - V_{SPH})^2}{(V_{SPH} - V_{T1})^2} \quad (4.16)$$

Assuming an upper switch point of 6.5 V and using other known values to solve for the ratio of β_1/β_3 , a ratio of 2.5 is derived which leads to a multiplicity for M3 of 15. After using these values for simulation, the upper and lower switch points were found to be at 7.6 V and 6.7 V, respectively, which were both higher than expected.

Taking Eq. (4.16) and solving for V_{SPH} yields:

$$V_{SPH} = \frac{\left(V_{DD} + \sqrt{\frac{\beta_1}{\beta_3}} V_T \right)}{1 + \sqrt{\frac{\beta_1}{\beta_3}}} \quad (4.17)$$

Since it can be assumed that V_{DD} is relatively large compared to the term containing β_3 on top, the lower term will dominate. Therefore, decreasing the multiplicity of M3 will lead to a lower V_{SPH} . In simulation, the multiplicity of M3 was adjusted iteratively downward to 6, which yielded switch points of 6.7 V and 6.4 V. This was deemed close enough to the desired center

point of 6 V, albeit with reduced hysteresis. The reduction in hysteresis was not considered an issue, since 0.3 V was enough to avoid jitter during switching. This equation also indicates that the upper switch point would tend to shift upward if the supply voltage was increased.

The next UVLO block to consider is the input stage. The specifications for this stage are presented in Table 14. Since the topology chosen prevents the output from pulling down fully, an output voltage is targeted here to assure that the last stage can be fully turned off. The switching thresholds are chosen to be centered near 9.5 V, knowing that the anticipated switch points on the monitored rail will be near 19 V. This would require the monitored voltage to be divided by two and translates to front end resistors that are roughly equal in size. Hitting the 9.5 V target was not critical to operation; rather, it was chosen only because of the desire to keep the resistors on the front end approximately the same size to facilitate a more compact layout.

TABLE 14. SPECIFICATIONS FOR UVLO INPUT STAGE

Parameter	Value	Justification
Output swing	5 V to 12 V	Topology prevents full swing; 5 V used because it is 1.5 V less than the switch point for the output stage and should assure turn-off there.
Function	Inverter	Generates appropriate logic level output
Topology	Modified Schmitt trigger	Modified topology used to allow some compensation for temperature
Switching thresholds	Near 9.5 V	Switch points are anticipated to be near 19 V; this value would lead to two approximately equal resistors for the dividing network
Hysteresis	1 V	About 10% of V_{DD}
Rise time	$< 2 \mu\text{s}$	Chosen to ~20% 10 μs specification for the UVLO to allow for signal propagation

To begin the design of the input stage seen in Fig. 44, a value for R_1 of 30 k Ω is first assumed. This is done to improve the compactness of the final layout, knowing that the same

value was used in the output stage and because it is already known that this resistor value led to reasonably sized MOSFET sizes in the output stage.

Since V_{OUT} is planned to swing between 5 V and 12 V, and because a value has been chosen for R_1 , it is now possible to find I_1 , since it is known that:

$$V_{OUT} = V_{DD} - I_1 R_1 \quad (4.18)$$

where I_1 is the current through M1. Substituting in known values yields $I_1 = 230 \mu A$. Since I_1 is actually the sum of the currents through M2 and M3, and since it is known that the output will not drop below 5 V, this means that V_{GS3} will likely not be zero, and it can be assumed that there must be some minimal amount of leakage current through M3. In an attempt to compensate for this leakage, the current is scaled up by approximately 5%, giving a current I_1 of 245 μA .

For the current source, the unknowns are R_3 , V_{BIAS} , the current I_4 through M4, and W/L for M4. In the interest of keeping the layout compact, and since there must be a starting point for calculations, a value of 30 k Ω is assumed for the pull up resistors. For simplicity, it is assumed that W/L for M4 and M1 will be equal, i.e. they will act as a current mirror. It is known that:

$$V_{BIAS} = V_{DD} - I_4 R_3 \quad (4.19)$$

Substituting in values, it is found that $V_{BIAS} = 4.65 V$. The equation for current in a MOSFET in saturation can then be used to calculate W/L , since $\beta_4 = K'_N(W/L)$. This yields a $W/L = 360$, and since 32x2 devices are being used, a multiplicity of 22 for M4 (which is equivalent to a W/L of 352) is chosen. Since it was decided to make the sizes of M1 and M4 equal, the multiplicity for both are now known.

In preparing to calculate values for R_2 , M2, and M3, it is noted that simulation sweeps of R_2 have already demonstrated that increasing R_2 tends to raise both switch points and decrease hysteresis. This is because it introduces negative feedback at the source of M2, which tends to delay the turn on of M2 as the resistance increases, and the same effect accelerates the turn off of M2. As can be seen in Fig. 43, the effect is more pronounced at the lower switch point for the turn off of M2. At the start of this transition, current is flowing through M2, so the effect of voltage at the source of M2 caused by voltage across R_2 is more prominent than that seen at turn on when the currents are very low. Since it is known that R_2 can be used to make minor adjustments in both the switch points and hysteresis, a value of zero is assumed for R_2 for the time being to simplify calculations.

Focusing on the calculation of M2 and M3, it is now possible to derive an equation for the ratio β_1/β_3 , using a procedure similar to that used for Eq. (4.6), resulting in:

$$\frac{\beta_1}{\beta_3} = \frac{(V_{DD} - V_{SPH})^2}{(V_{BIAS} - V_T)^2} \quad (4.20)$$

Solving this yields $\beta_1/\beta_3 = 2.3$. Knowing that the multiplicity of M1 is 22, this result indicates a multiplicity for M3 of 10.

Looking now at the size of M2, a similar derivation to that used for Eq. (4.13) can be used to derive an equation for the case seen here where the effect of R_2 has been added:

$$\beta_2 = \frac{2(V_{DD} - V_{OUT} - V_x)}{R_1(V_{SPL} - V_x - I_2 R_2 - V_T)^2} \quad (4.21)$$

Without a value for V_x , calculating β_2 becomes a challenge. Also, since it is present in the squared term of the expression, minor changes in its value can result in vastly different values for the value of β_2 . It was chosen, therefore, to follow the same path as seen in the derivation of values for the Schmitt trigger in the output stage and set $\beta_2 = \beta_3$, since this led to stable operation in that case. Setting M2 to a multiplicity of 10 to match M3, the upper and

lower switch points were simulated to be 8.5 V and 7.6 V, respectively. Referring back to Eq. (4.17), the multiplicity of M3 and M2 were increased to 16 and re-simulated; as noted in Table 15, the upper switch point was shifted higher to 8.7 V. At this point, the resistor R_2 was introduced into the circuit and simulations were run until the upper switch point was near 8.9 V; this is depicted in the Sim Run #3 column in the table. As expected, this had the effect of also shifting the lower switch point higher, which resulted in less hysteresis.

TABLE 15. COMPONENT VALUES IN THE UVLO INPUT STAGE AS ADJUSTED DURING SIMULATION

Component	Size/Value			
	Sim Run #1	Sim Run #2	Sim Run #3	Sim Run #4
R_1	30 k Ω	30 k Ω	30 k Ω	30 k Ω
R_2	0 Ω	0 Ω	4 k Ω	4 k Ω
R_3	30 k Ω	30 k Ω	30 k Ω	30 k Ω
M1	32 / 2 x22	32 / 2 x22	32 / 2 x22	32 / 2 x20
M2	32 / 2 x10	32 / 2 x16	32 / 2 x16	32 / 2 x16
M3	32 / 2 x10	32 / 2 x16	32 / 2 x16	32 / 2 x16
M4	32 / 2 x22			
V_{SPH}/V_{SPL}	8.5 V / 7.6 V	8.7 V / 7.2 V	8.9 V / 8.4 V	9.1 V / 8.7 V

Following this, simulations were run over temperature while modifying the multiplicity of M1 to attempt to optimize for the shift of the lower switch point over temperature. The data for three of these passes are shown in Table 16. The drift of both switch points became smaller as M1 was decreased; at a multiplicity of 18 the waveforms began to show signs of under biasing, such as slow and “stepped” transitions; insufficient current leads to an insufficient voltage drop across the pull up resistor, which would prevent M3 from turning off. The final

value of M1 was set to 20; the final schematic for the UVLO circuit is shown in Fig. 45 and the final switch points are as indicated in the Sim Run #4 column in Table 16.

TABLE 16. SWITCH POINT SHIFTS OVER TEMPERATURE WHILE VARYING M1 MULTIPLICITY

	V_{SPH}	V_{SPL}
M1 Multiplicity	Shift from 25 °C to 225 °C	Shift from 25 °C to 225 °C
22	-0.250 V	-0.040 V
20	-0.168 V	-0.025 V
18*	-	-
* At a value of 18, under biasing was apparent in the waveforms.		

Some insight into temperature behavior can be gained by solving for V_G of M2 in Fig. 44. This is done by starting with the equation for current in a MOSFET at saturation:

$$I_2 = \frac{1}{2} \beta_2 (V_{GS2} - V_{T2})^2 \quad (4.22)$$

Knowing that $V_{GS2} = V_{G2} - V_{S2}$ and $V_{S2} = I_2 R_2 - V_x$ and substituting these into Eq. (4.22), it is found that:

$$V_{G2} = \sqrt{\frac{2I_2}{\beta_2}} + I_2 R_2 + V_x + V_{T2} \quad (4.23)$$

The convention is now adopted that a subscript 1 or 2 will be added to variables to indicate whether they are applicable at one of two temperatures. A subscript of 1 will indicate operation at a lower temperature, and a subscript of 2 will indicate operation at a higher temperature. Also, $V_{G2} = V_{SPL}$, since this voltage represents the lower switch point.

To examine the effect of the switch point over temperature, the expression $V_{SPL2} - V_{SPL1}$ is found:

$$V_{SPL2} - V_{SPL1} = \left[\sqrt{\frac{2I_{22}}{\beta_2}} - \sqrt{\frac{2I_{21}}{\beta_1}} \right] + [I_{22}R_{22} - I_{21}R_{21}] + [V_{x2} - V_{x1} + V_{T2} - V_{T1}] \quad (4.24)$$

Ideally, the switch point would not change over temperature, so the expression $V_{SPL2} - V_{SPL1}$ would be equal to zero. Thus, it is necessary to examine how each expression is affected by temperature and how each expression can be made to approach zero.

At a higher temperature, mobility increases (β is larger), V_T decreases, and resistor values increase. Referring now to the first bracketed expression as “Expression 1”, the next as “Expression 2”, and so on, it can be seen that Expression 1 will tend to decrease as β increases with temperature. Expression 2 would tend to increase with temperature as the resistor increases in value. Expression 3 tends to decrease as V_T decreases with an increase in temperature. In order to reduce shifting of the switch point over temperature, it is desirable to counteract the behavior seen in each expression.

In the final circuit topology, as temperature increases the current I_2 decreases, while the voltage V_x increases. From 25 °C to 225 °C, simulated current drops from 230 μ A to 196 μ A, a change of about 15%. At the same time, the value of V_x increases from 3.3 V to 3.6 V, a change of about 9%. Measured data suggests that the resistors increase in value by approximately 18% over the same temperature range.

Examining the expressions in Eq. (4.24), it is evident that Expression 1 would tend to become more negative as the current is increased (although it trends with the square root of the current). For Expression 2, the decrease in current would tend to push the switch point somewhat lower with temperature; however the shift in current is not as large as the shift in resistance, so the term would still have a more positive component at a higher temperature. For Expression 3, raising the voltage at V_x tends to counteract the shift in V_T . However, the 0.3 V change in V_x is likely less profound than the change in V_T , so while there is some improvement,

the expression is still negative overall. This matches observations seen in simulation, in that while the shift of lower switch point can be reduced, it can never be completely eliminated using the approach chosen. A more complicated approach, however, would have posed a significant challenge to implementation in the current Cree process.

After examining Eq. (4.24), it is apparent that the presence of the source resistor R_2 tends to improve performance over temperature. Without it, Expression 2 can contribute nothing to counteract the effects of the other two expressions.

In regards to the temperature behavior of the upper switch point, Eq. (4.15) can be used to solve for $V_{SPH2} - V_{SPH1}$ as shown in Eq. (4.25):

$$V_{SPH2} - V_{SPH1} = [V_{x2} - V_{x1} + V_{T2} - V_{T1}] \quad (4.25)$$

Here, the upper switch point tends to shift downward with temperature regardless of changes made to current I_2 or R_2 . This trend was supported by simulation over temperature.

As a contingency, a separate version of UVLO epitaxial layout was created in which the front end resistors were omitted and the input was directly accessible via an external pad. This variation of the circuit, called the epitaxial experimental (or, “epi-X”) version, was created in the event that process variation (or other issues) necessitated that the resistors be externally adjusted in order to achieve the proper switch points. Ultimately, this decision made just before the final tape out turned out to be a particularly good idea.

In order to conserve layout space, the decision was made to not include a separate voltage regulator in the second fabrication run. Instead, it was assumed that an externally regulated voltage source would be provided by the system.

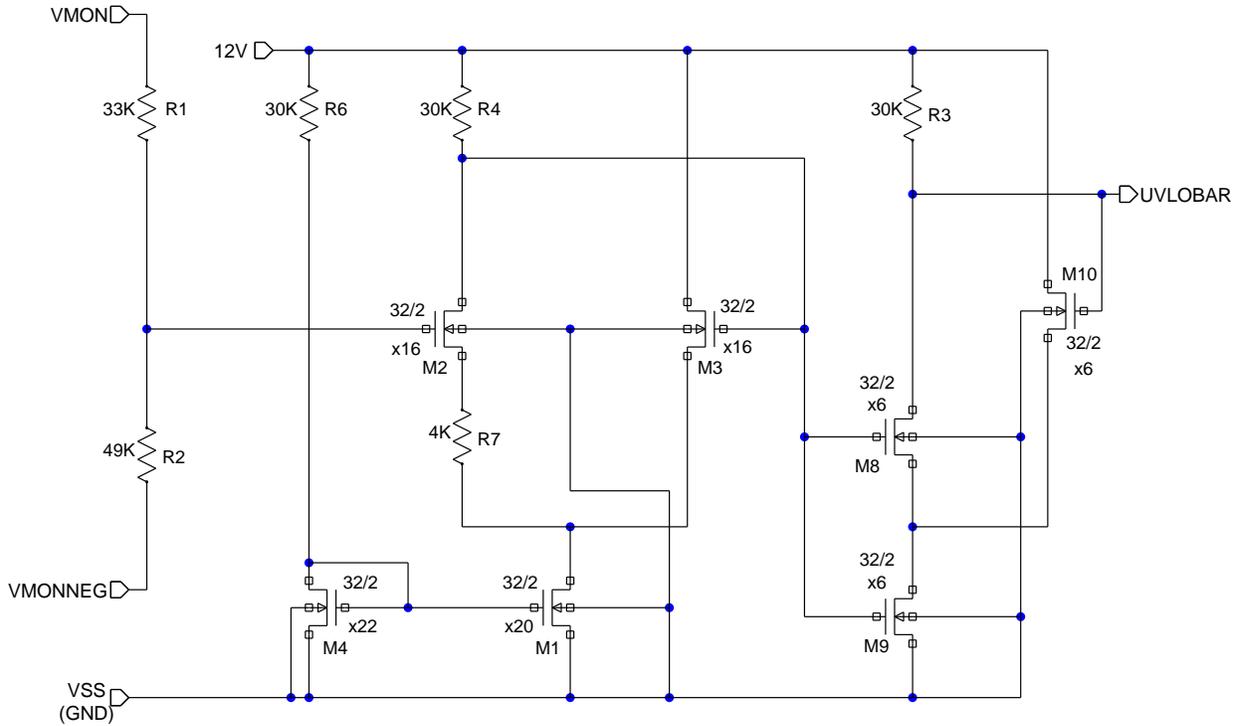


Fig. 45. The final UVLO circuit topology for Fabrication Run Two.

Several changes were made in the second fabrication run to better address issues with testability encountered in the first. Also, as previously mentioned, the UVLO was not tied directly to any other logic circuits, but rather was left in a standalone configuration so that observability was maximized to better facilitate testing. The ability to use only probe pads to perform testing allowed full characterization on a probe station, thereby avoiding the need to design and implement a custom packaging solution for testing.

4.1.4 Other Design Structures in Fabrication Run Two

In addition to the UVLO circuit, two resistor test structures were also designed so that characteristics for both polysilicon and diffusion resistors could be captured. These structures were designed around the Transmission Line Model (TLM) method, which is commonly used

to measure contact resistance [42], [43]. A more detailed overview of these structures is provided in Appendix B.

4.1.5 Simulations

Transient simulation waveforms for the final UVLO circuit shown in Fig. 45 are shown in Fig. 46. The anticipated switch points across temperature are shown in the table inset in the figure. These switch points were determined by examining the input voltage in the simulated data where the output reached $V_{DD}/2$ during each transition. The simulation waveforms indicated that the UVLO switch points would vary by less than 0.5 V over the temperature range between 25 °C and 225 °C. Rise time for the output for a 1pF load was simulated to be approximately 350 ns. Fall time was approximately 1 μ s, and so the speed of the circuit was deemed acceptable in light of the requirement that the transition times be less than 10 μ s. In retrospect, the relative asymmetry of the rise and fall times was an indicator that certain MOSFETs in the circuit were marginal in terms of turn-on with a supply voltage of 12 V. After process variations, this marginality proved to be an issue when the devices were tested. Since the processes used were under development, statistical models were not available that would have allowed “over-process” simulations in the PDK. The simulated switch points indicated that the lower switch point would remain relatively stable, while the upper switch point would vary slightly with temperature.

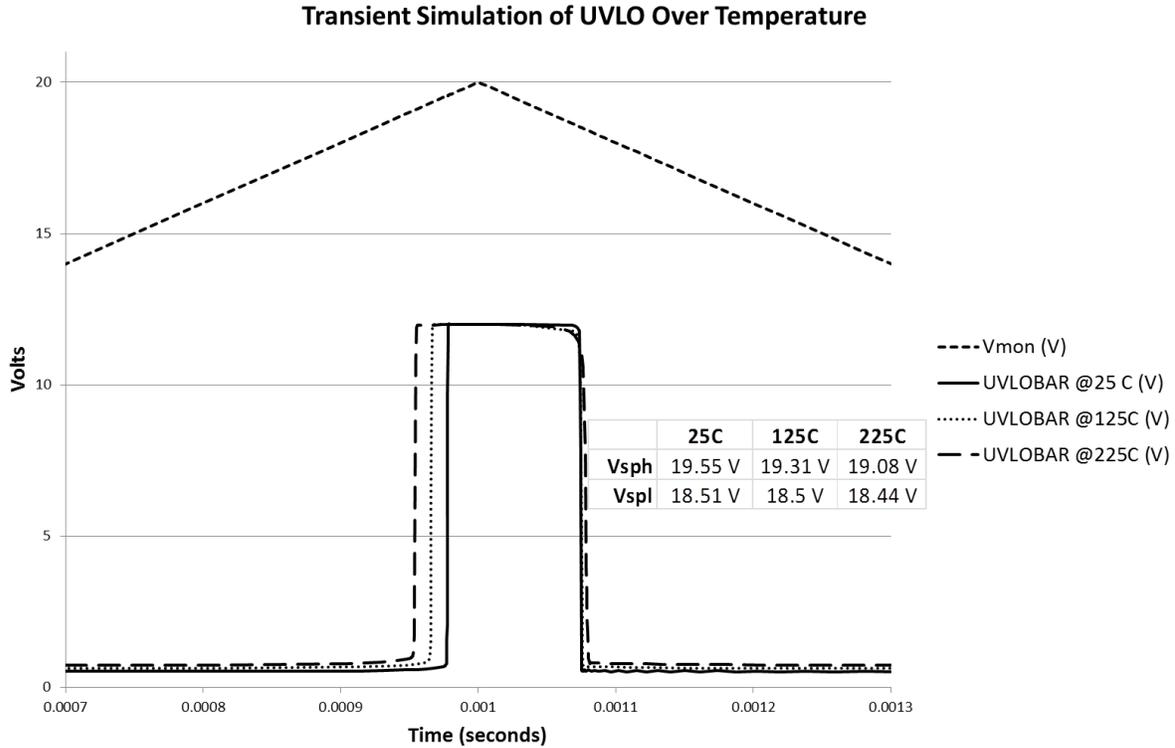


Fig. 46. Transient simulation of the UVLO for Fabrication Run Two over temperature.

It is important to point out that this circuit approach is sensitive to the stability of a number of process parameters. Any process variation that affects the threshold voltage of the devices, the value of the resistors, or other MOSFET parameters could impact the performance of the circuit. In addition, the circuit was designed for operation with a 12 V supply; varying the supply voltage would tend to affect biasing levels and impact performance over temperature as well. The epi-X version was included as a hedge to attempt to address the sensitivity of the circuit to these parameters by allowing the switch points to be adjusted externally if necessary.

4.2 Layout for Fabrication Run Two

The final size for the new UVLO layout was 513 μm x 347 μm , or approximately 178,000 μm^2 . This represents a 3X reduction in size over the layout in the first fabrication run.

While the reduction in size is at least partially due to the omission of the voltage regulator, it was also due in large part to the absence of the large NMOS device used in the feedback path of the first design. In terms of complexity, the circuit used in the second fabrication run was approximately the same as that of the first.

4.2.1 Challenges

The lack of depletion mode devices meant that all circuits had to be designed using resistor-based pull ups. The resistors in the process presented a number of challenges. Although there were two resistor types available (polysilicon- and diffusion-based), the diffusion-based resistors were preferred for design because they had a greater heat dissipation capability due to their embedded nature. However, metal contacts to the diffusion resistors were plagued by the relatively high contact resistance previously mentioned. Modeling of these effects was not implemented in the PDK, which meant that large contacts had to be used to avoid significant parasitic resistance. In addition to this, the tolerance of the resistors was not known.

4.2.2 Final Cell Layouts

The final layout for the implant version of the UVLO is shown in Fig. 47; the epitaxial version of the UVLO is shown in Fig. 48. Both designs attempt to use oversized contacts for connections to the diffusion resistors and, whenever possible, large contacts to connect metal to polysilicon. An example of the latter can be seen in the polysilicon-based bridge that was placed between M2 and the common node between R_1 and R_2 .

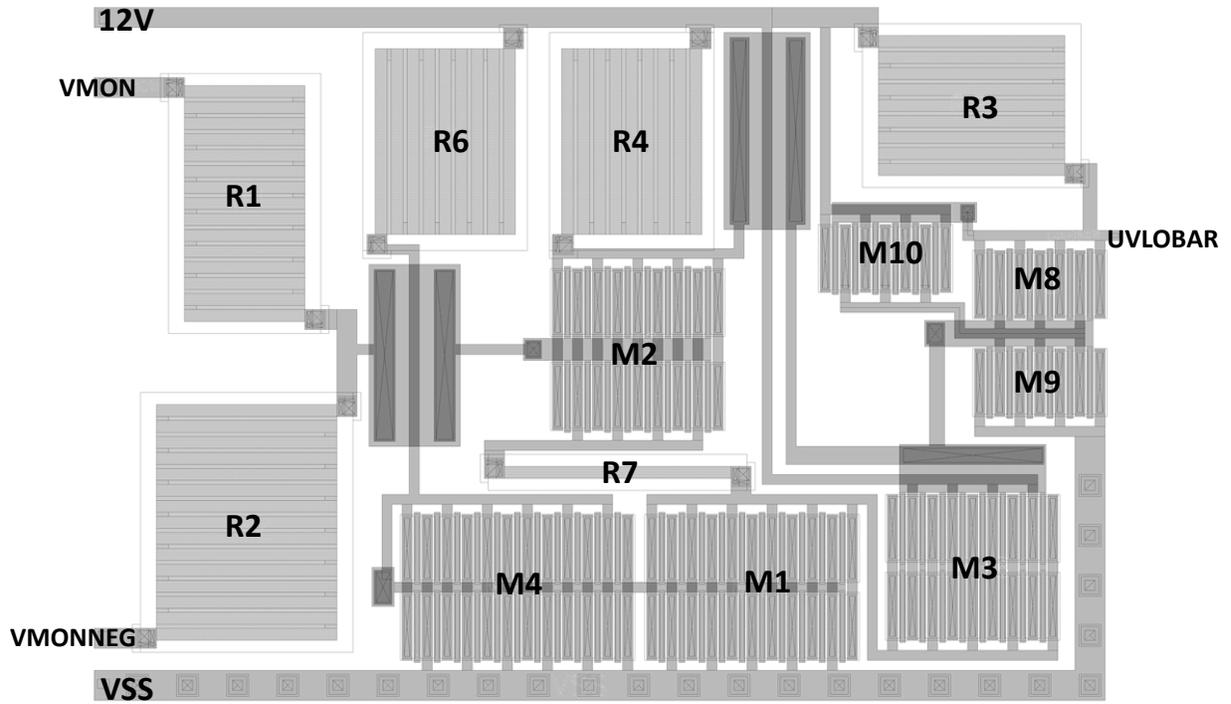


Fig. 47. Final UVLO layout for Fabrication Run Two (implant version).

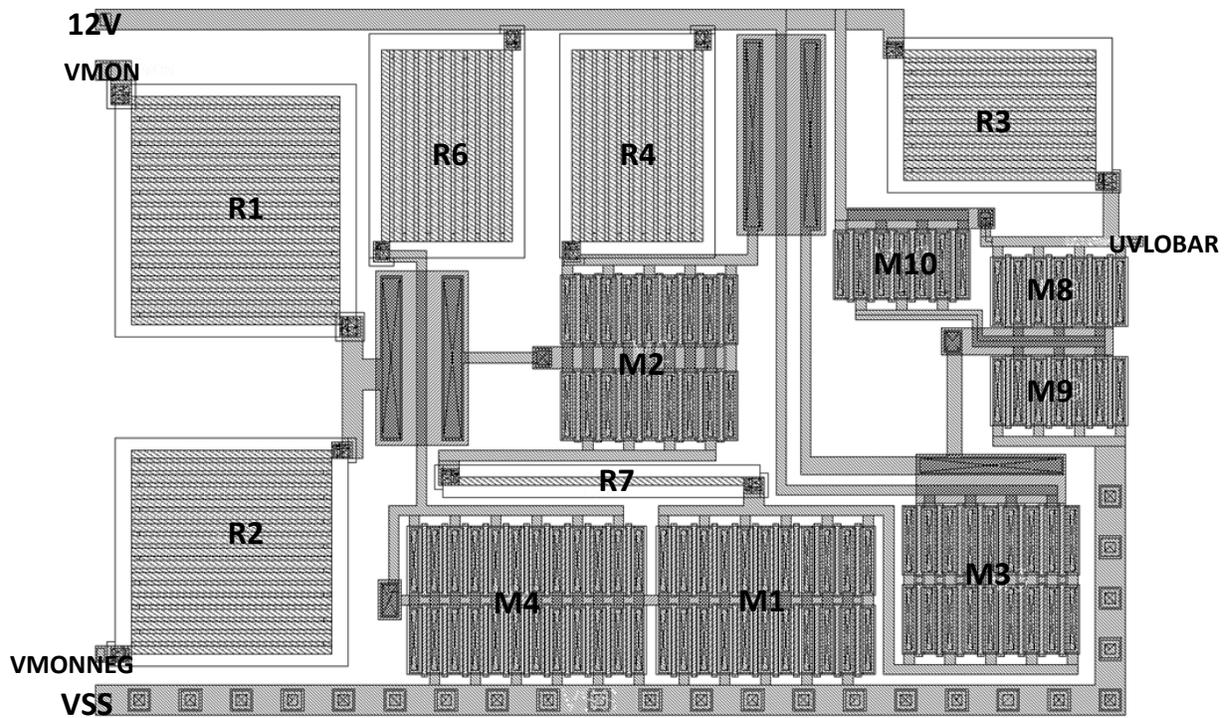


Fig. 48. Final UVLO layout for Fabrication Run Two (epitaxial version).

The epitaxial “experimental” (epi-X) layout is shown in Fig. 49. Here, the resistor voltage-dividing network on the front end has been removed and the input to the first input has been made directly accessible. This input was ultimately routed to an external pad to allow the input from an external resistor network to be directly injected. Since there was some process variation on the final die, this cell was ultimately used for the bulk of data capture during the testing phase of the project.

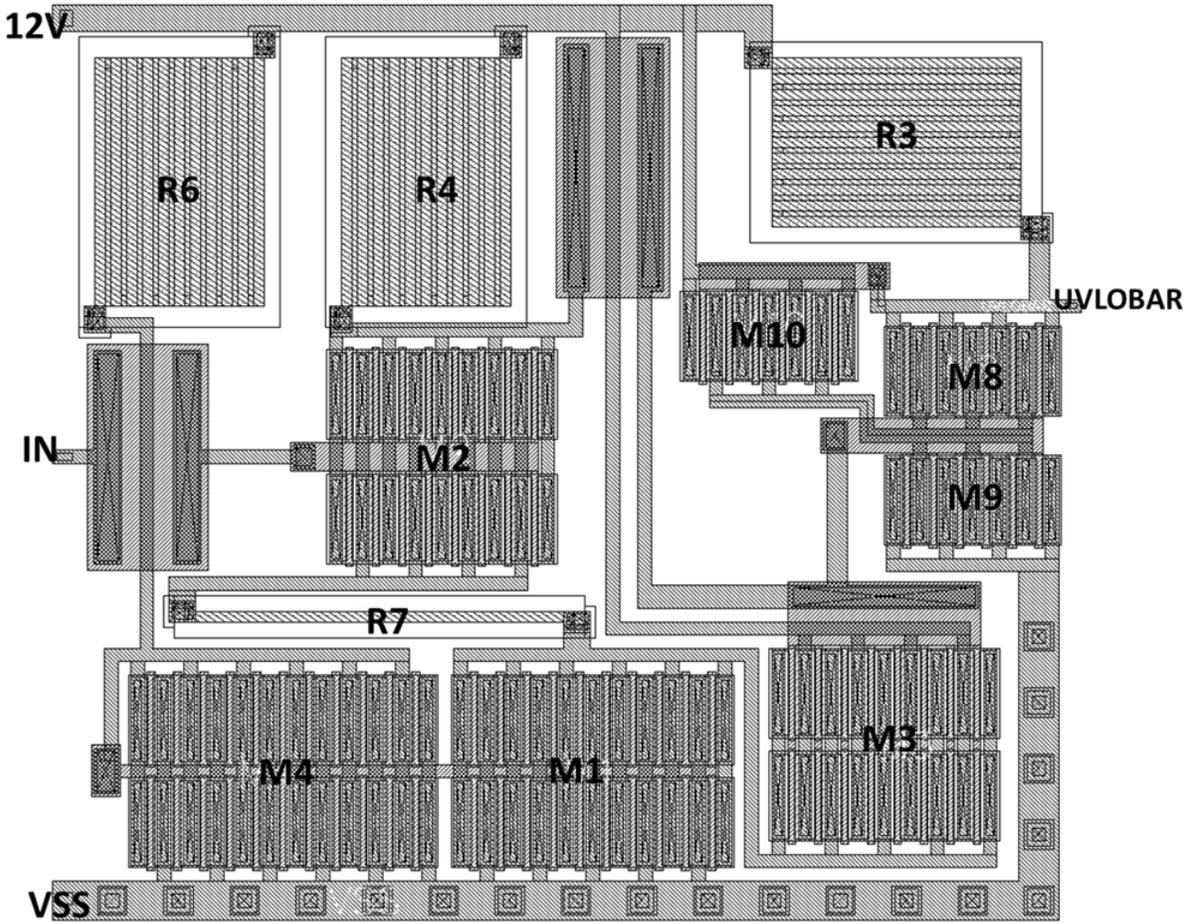


Fig. 49. Final UVLO layout for Fabrication Run Two (epitaxial experimental version).

A view of the final chip layout for the UA_SPLIT reticle is shown in Fig. 50. This reticle contained an implant version of the UVLO, the epi-X version of the UVLO, the TLM resistor test structures, and cells for other UA students participating in the effort. The various cells are labeled in the figure. A photograph of the final chip layout of the UA chip is shown in Fig. 51. On this chip, the epitaxial version of the UVLO was placed, as well as the TLM resistor test structures.

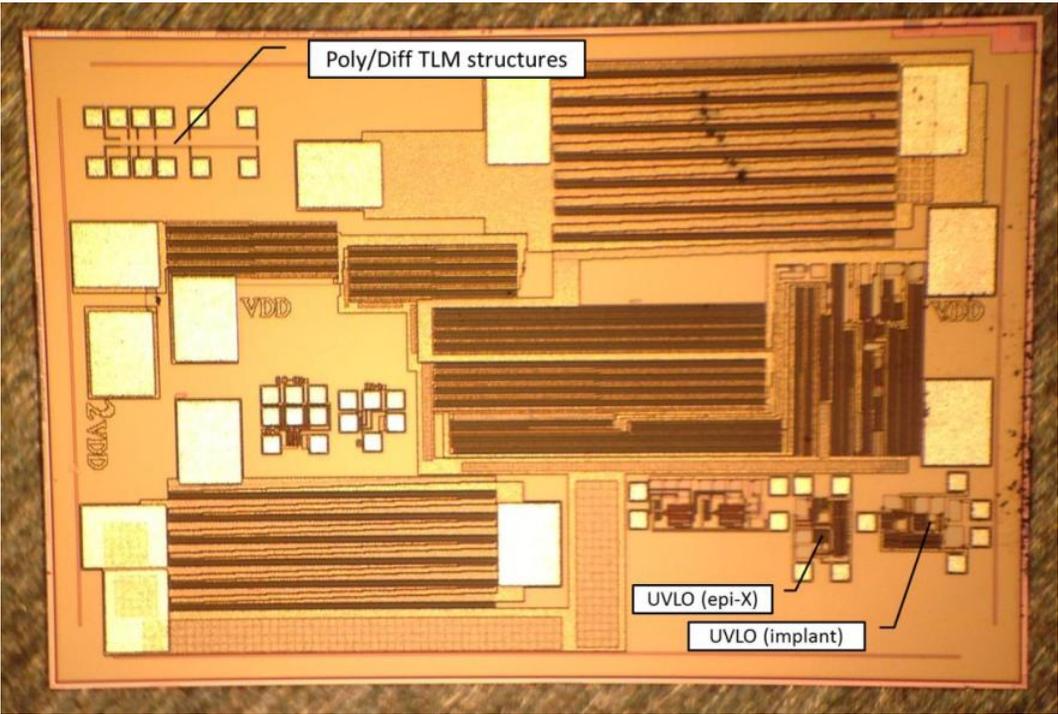


Fig. 50. A photograph of the final chip layout for the UA_SPLIT chip.

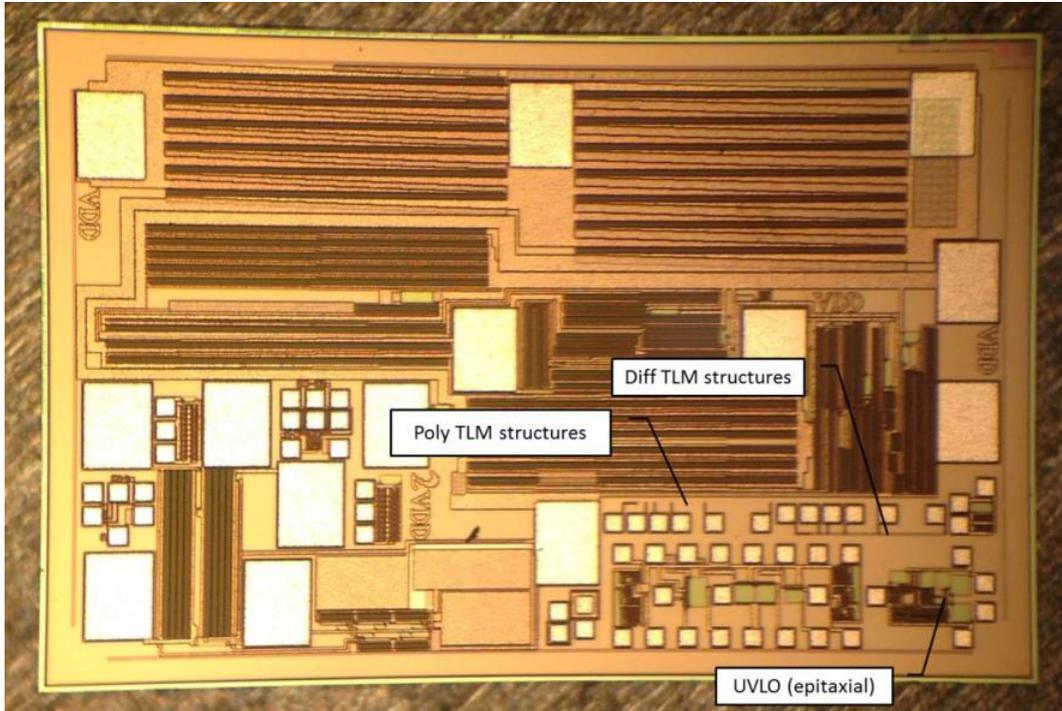


Fig. 51. A photograph of the final chip layout for the UA chip.

4.3 Testing for Fabrication Run Two

No specialized packaging was required for testing the UVLO for the second fabrication run; direct probing was opted for instead, primarily due to the economic and schedule costs associated with packaging the devices for high temperature testing, but also for the ease of testing afforded by using simple prober-based testing.

4.3.1 Experimental Apparatus

For Fabrication Run Two, a new probing system, shown in Fig. 52, was used. Also shown in this figure are the instruments used for DC sweeps of the UVLO. Shown in the figure are (a) the SemiProbe M-6 probing station and (b) the Keithley 4200 series Semiconductor Measurement System and a rack mount PC used for testing. The labeled items in the figure included (1) the probing stage with a heated chuck and (2) temperature controller capable of

reaching 315 °C, (3) the Keithley 4200, and (4) the rack mount PC. Since Microsoft Windows XP was the operating system is used for the Keithley 4200, and since both the Keithley and the rack mount PC were networkable, the open source software *Synergy* was used to provide seamless control of both systems using only one keyboard and mouse. This test setup was used for DC sweep testing by configuring the Keithley 4200 to perform voltage sweeps of the input, running the tests, and saving the resulting output to Microsoft Excel-compatible output files.

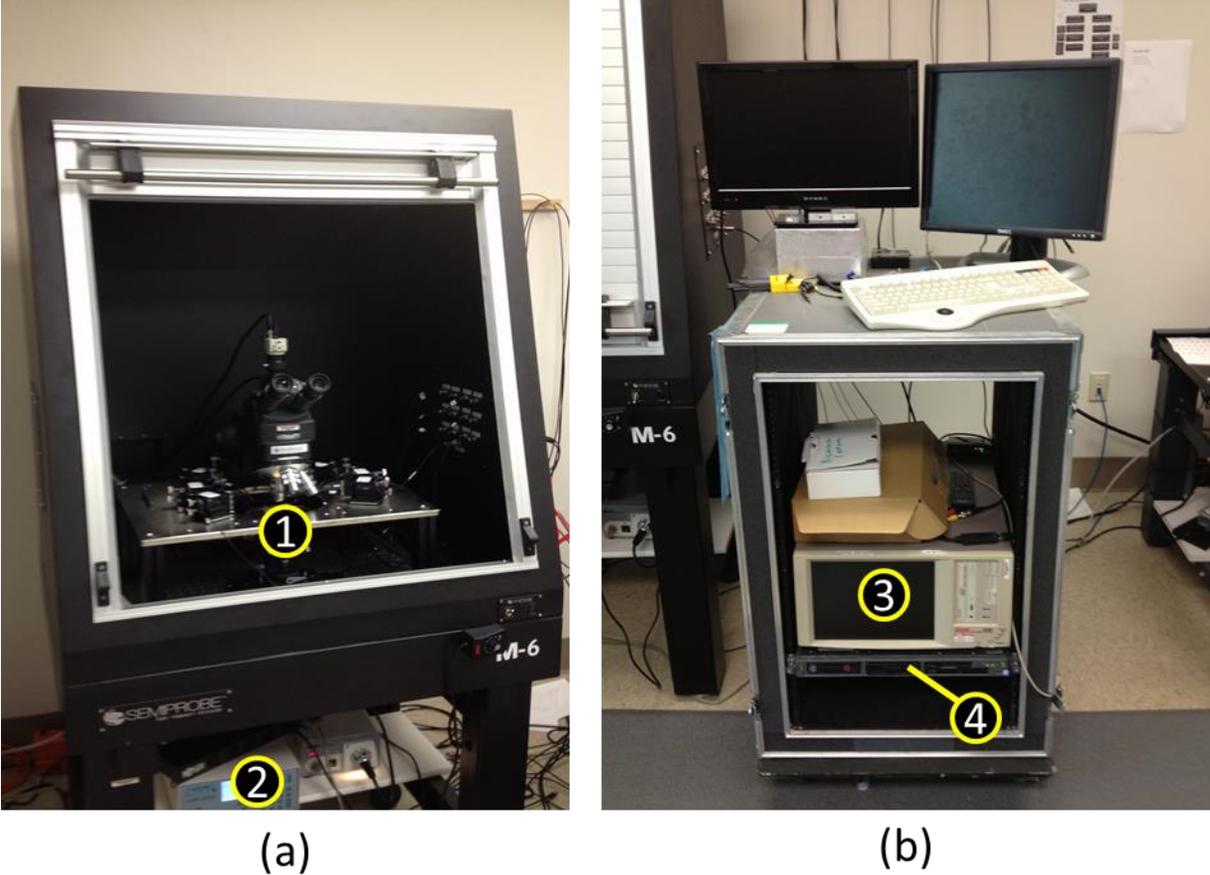


Fig. 52. Photograph of the SemiProbe manual probing system.

A separate test apparatus configuration, shown in Fig. 53, was used for transient measurements. The components shown in the figure include (1) a Tektronix TDS 744A color oscilloscope, (2) a Tektronix AFG 3022B arbitrary function generator, (3) an HP DC power

supply at 16 V used to power the UVLO, (4) a DC power supply at 10 V used to offset the signal from the function generator to achieve a ramp from 0 to 20 V DC, (5) a digital multi meter (DMM) used to confirm power supply output, and (6) a 100 kΩ potentiometer mounted in a bread board to allow convenient adjustment of the voltage divider on the front end of the UVLO. A photograph of a UVLO Epi-X cell being probed can be seen in Fig. 54. The pads shown in the image have multiple probe marks, a result of the multiple probe contacts made while ramping up temperature.

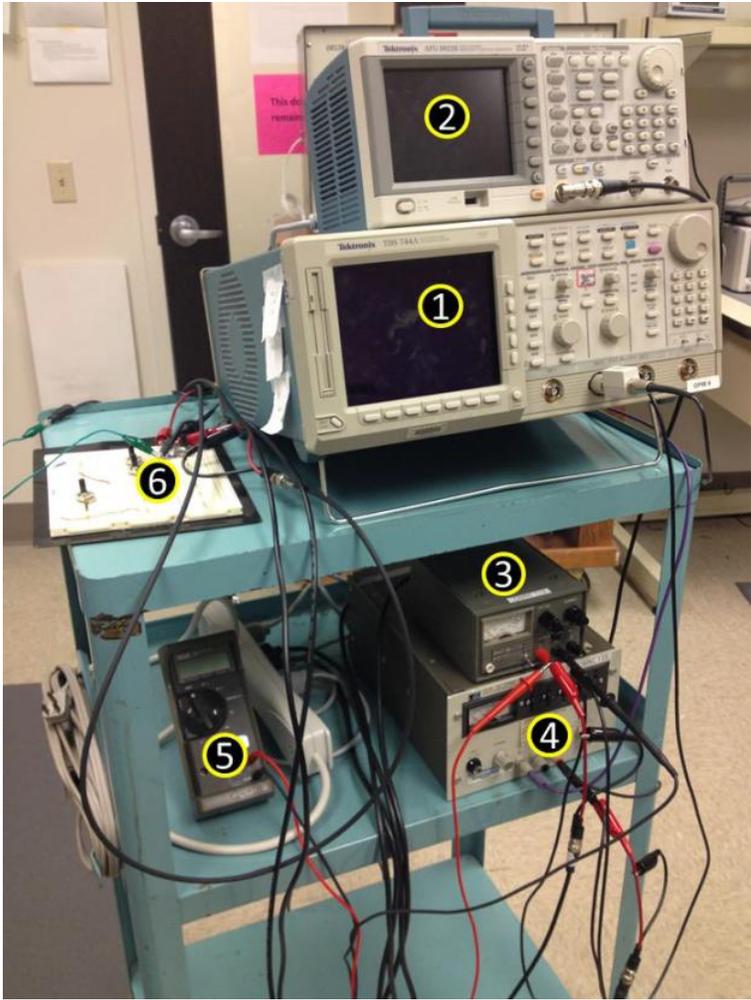


Fig. 53. Test apparatus used for transient testing.

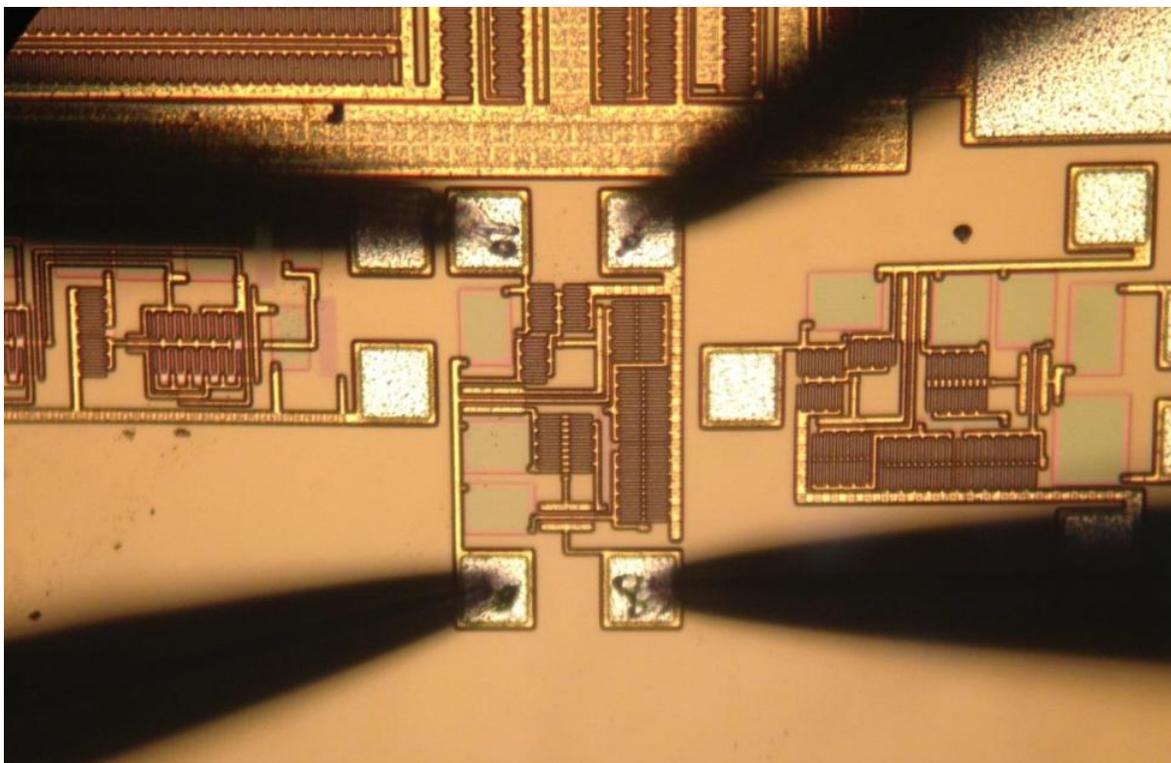


Fig. 54. A photograph of a UVLO Epi-X cell being probed during transient testing.

4.3.2 Results

The initial batch of devices that arrived for testing from Cree was fabricated using the epitaxial process. As in the first fabrication run, a random sample of the 32x2 test structure devices were probed upon initial reception of the die. Results from these tests were reasonable (i.e., no devices were dead), so manual probing of the UVLO was initiated.

Initial results using a 12 V power supply to power the UVLO resulted in no usable output. This issue was likely a result of process variation causing the output Schmitt trigger to not be fully turned on. The waveforms seen during DC sweep testing exhibited very soft switching behavior, to the point that the positive feedback did not seem to be taking place. This suggests that the output of the first Schmitt trigger was not swinging sufficiently to fully turn-off the MOSFET used for positive feedback.

Fig. 55 shows DC sweep data measured for a UVLO using a 12 V supply. The “soft” transitions are evident in the waveform. Hysteresis was slightly negative for this device; other devices tended to show either negative hysteresis as shown here, or slightly positive hysteresis (but very near zero).

After increasing the power supply to 16 V, usable results were obtained and the switching behavior of the circuit was similar to those simulated, albeit with a shift in switch points. Operation was attempted with supply voltages between 12 V and 16 V, but ultimately 16 V was chosen as the new supply voltage simply on the assumption that it might yield a better operating margin over temperature.

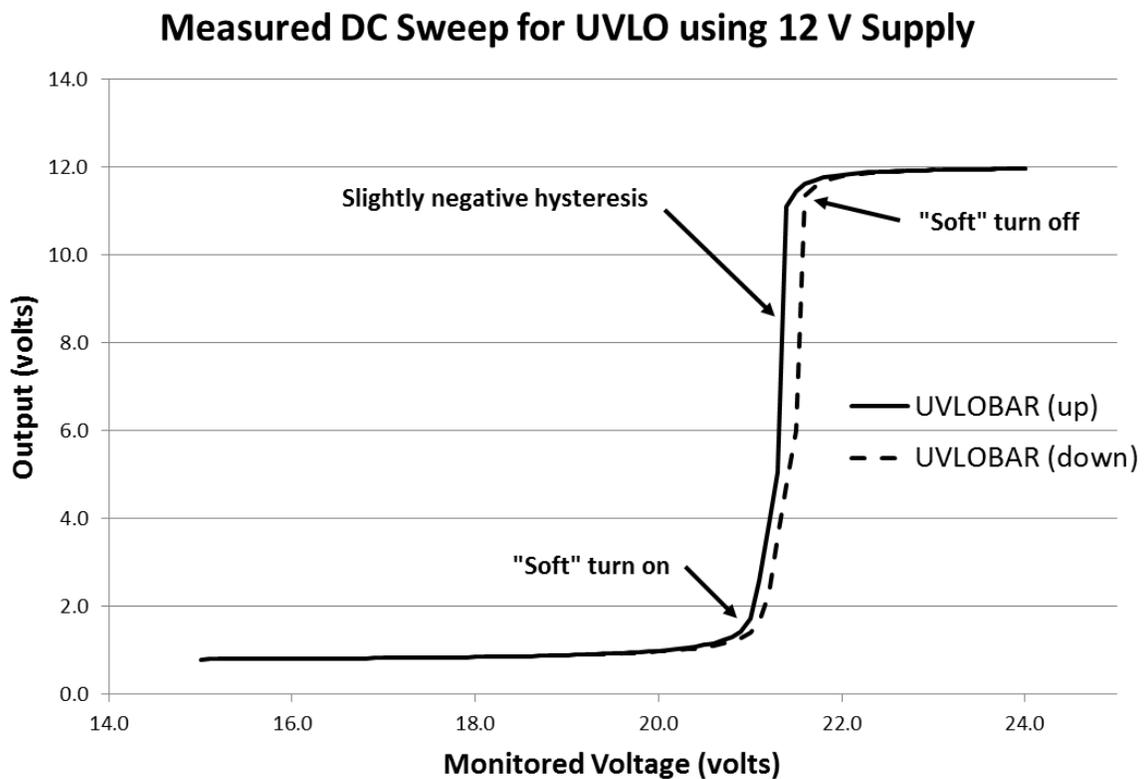


Fig. 55. Measured DC sweep for the UVLO on HW0613-32_UA_R1C2 with a 12 V supply.

One example of a DC sweep measurement for a device on a “UA” wafer cell is shown in Fig. 56. It is important to note that this device was intended for fabrication in the implant

process, so it would not be expected to be switching at the desired points. It was chosen for preliminary testing because it seemed prudent to choose a device that could be considered “safely destructible” for the first probing attempt. The device was found to have upper and lower switch points somewhere near 27.1 V and 26.9 volts, respectively. However, hysteresis was present and the device exhibited operation at 125 °C, as seen in Fig. 57. At the higher temperature, some shift in the switch points was present; however unlike the UVLO in the first fabrication run, a complete collapse of hysteresis did not occur at the higher temperature; in fact, the amount of hysteresis increased. At 125 °C, the upper and lower switch points are near 25.2 V and 23.9 V, respectively. At this point, testing had to be halted on this device due to damage inflicted from electrostatic discharge (ESD). At the time, it was not immediately suspected that ESD was an issue, since a grounding strap was worn at all times while handling the devices and when stepping up to the test bench. During subsequent testing efforts, it was discovered that static charge was being generated when sitting in the laboratory chairs and that a discharge occurred when approaching the test bench to put on the wrist strap. The issue was never encountered again after ESD shoe straps were worn at all times so that charge was continually dissipated through the grounded floor mats inside the laboratory.

As already stated, waveforms on the test bench tended to be softer and exhibit no hysteresis when using a 12 V supply. The measurement of diffusion resistors in the process had revealed that the resistor values were 18% lower than the designed values. However, after updating resistor values in simulation there was no appreciable change in the simulated outputs at 12 V; simulated waveforms still indicated proper operation, although it was apparent that under biasing was occurring when using a 12 V supply on the test bench.

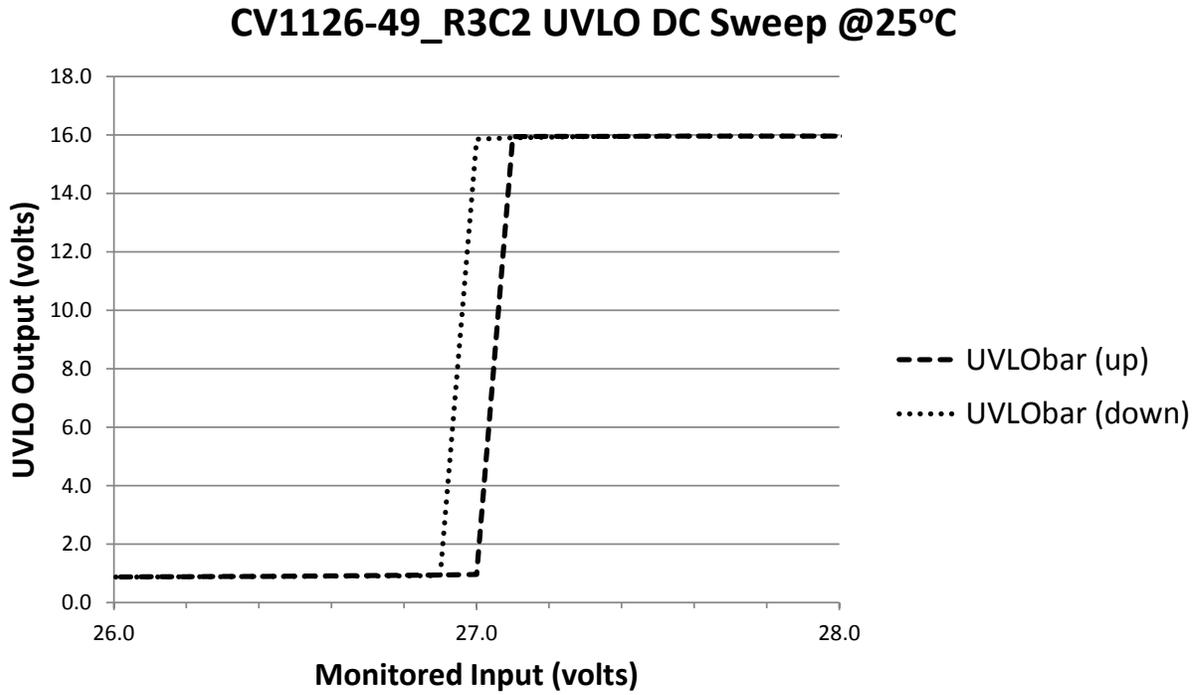


Fig. 56. Measured DC sweep for die R3C2 from wafer CV1126-49 at 25 °C.

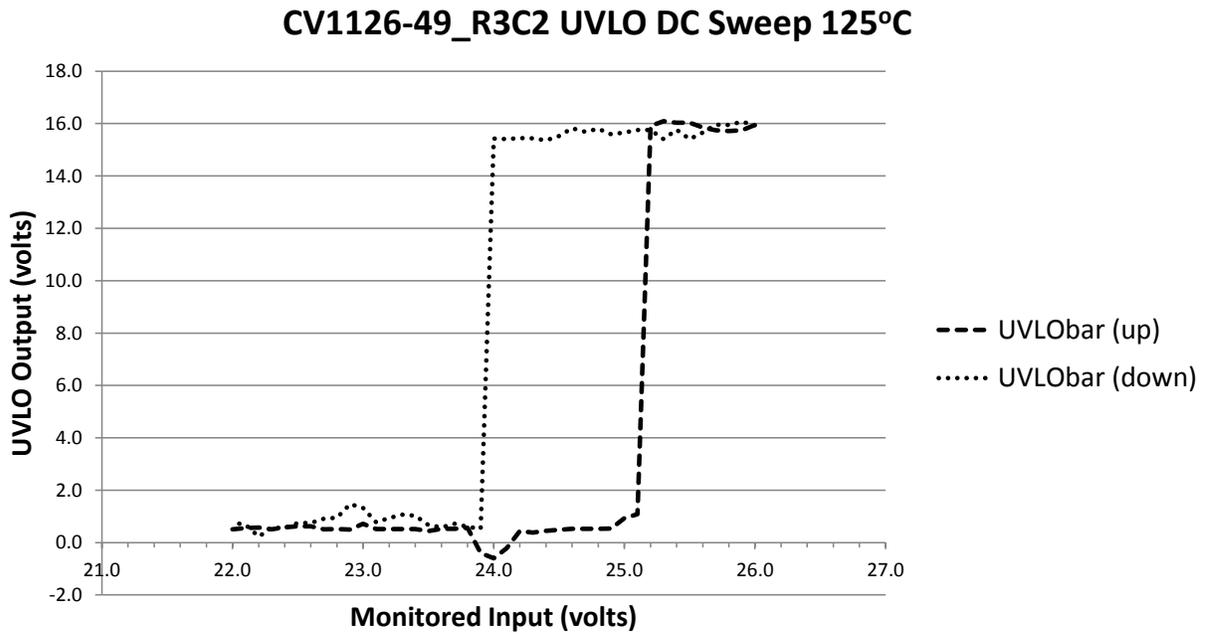


Fig. 57. Measured DC sweep for die R3C2 from wafer CV1126-49 at 125 °C.

Left with only the MOSFETs to investigate, the transconductance curve for a single $32\mu\text{m} \times 2\mu\text{m}$ enhancement device from the same wafer lot as the tested UVLO was compared with the same curve from simulation. A plot of this data is shown in Fig. 58. The data shown in this figure indicates that for gate-source voltages in the range below approximately 6.5 V, the simulated output would tend to assume more current for a given V_{GS} than that seen in the actual device.

Given this observation and a desire to reproduce observed test bench waveforms in simulation, the multiplicity value for each MOSFET in the design was reduced by one-half to approximate the reduction in current predicted by the difference between the curves in Fig. 58. Resistor values remained 18% lower than their original values, as based on measurements. The modified circuit was then simulated using supply voltages of both 12 V and 16 V. The waveforms simulated for a 12 V supply are shown in Fig. 59. Here, the soft turn-ons and lack of hysteresis is evident in the simulation and closely emulates the curves seen on the test bench when using a 12 V supply.

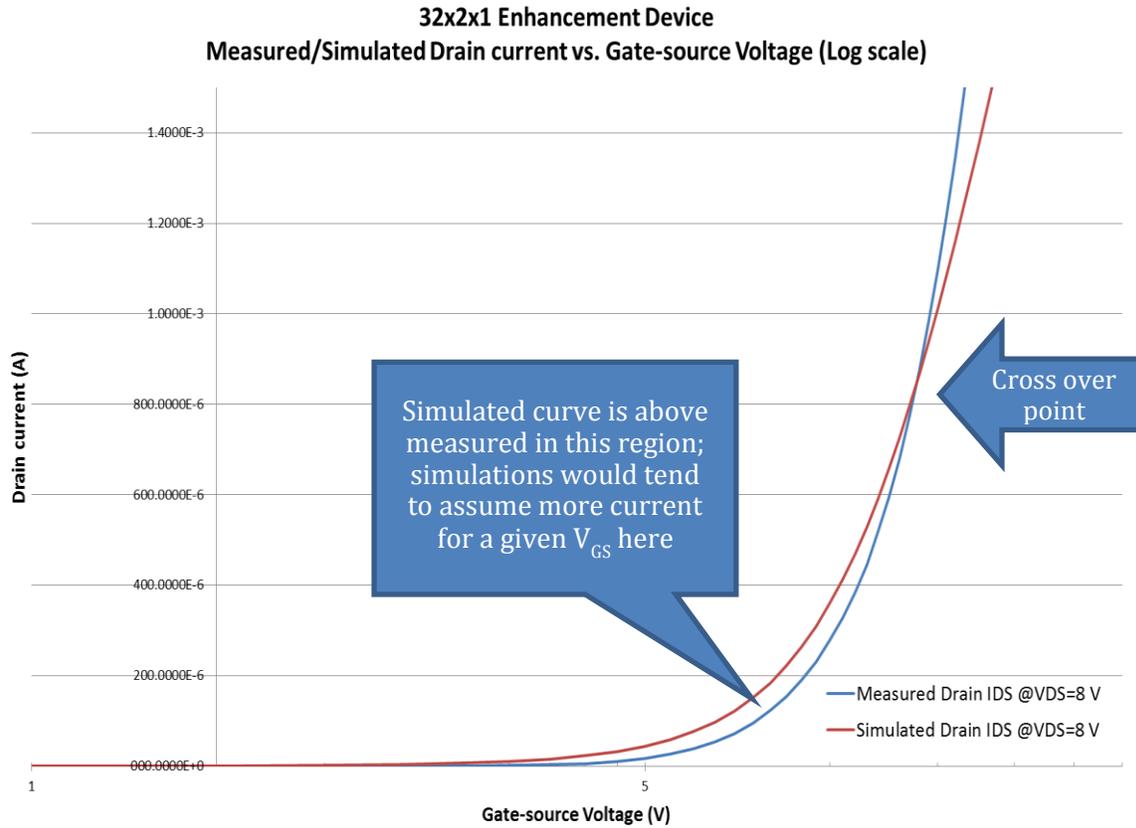


Fig. 58. A comparison of simulated and measured values for drain current vs gate-source voltage in a 32x2 device.

The waveforms for the same circuit after changing the supply voltage to 16 V can be seen in Fig. 60. In this figure, both sharp transitions and hysteresis are present, mirroring the waveforms and general behavior seen in waveforms captured on the test bench with a 16 V supply. This further supports the idea that process shift resulted in under biasing, and explains the necessity to run with a higher supply voltage in order to obtain sharp output transitions and hysteresis.

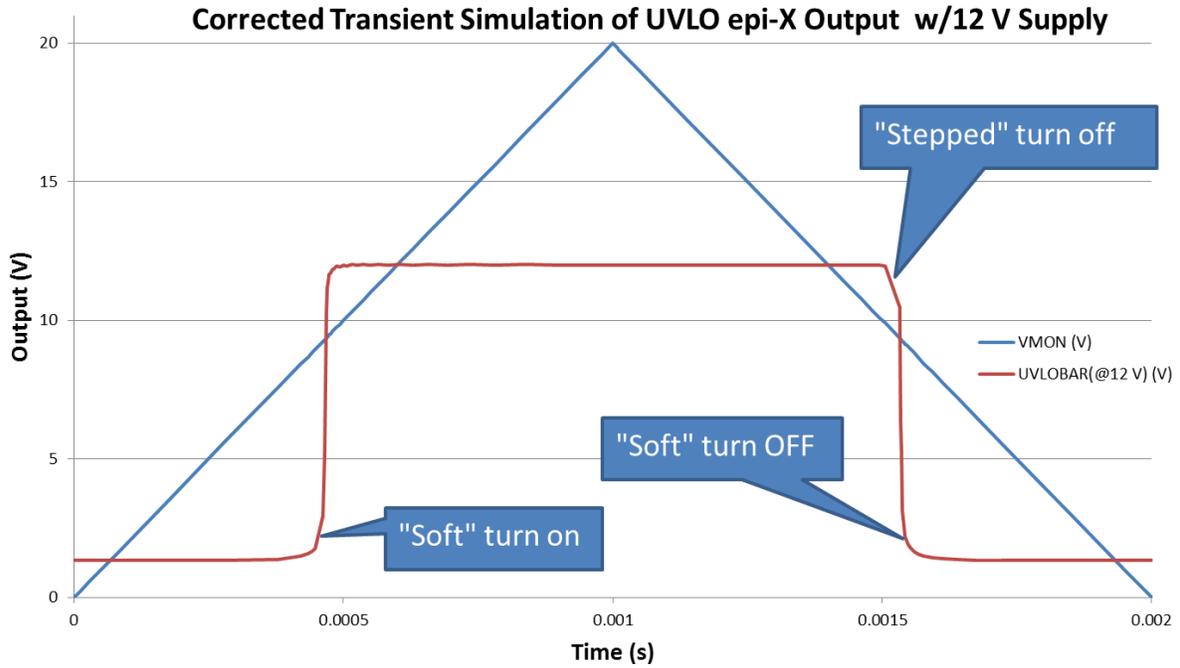


Fig. 59. UVLO simulation with 12 V supply after adjusting MOSFET transconductance due to process shift.

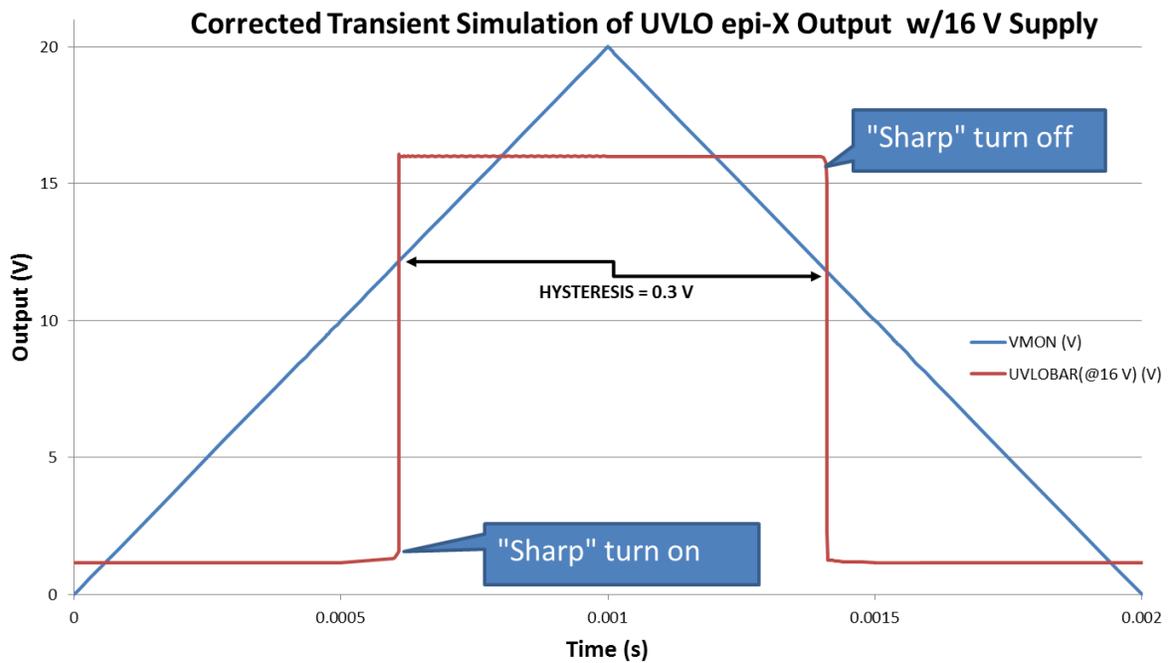


Fig. 60. UVLO simulation with 12 V supply after adjusting MOSFET transconductance due to process shift.

Further testing was focused on measuring UVLO cells intended for use in the epitaxial process. A few data points were captured from epitaxial versions of the UVLO, but the switch points for these were skewed high by about 3 V. Following this result, an “epi-X” cell was probed and found to have switch points that were approximately 3 V higher than simulated as well, a side effect of using the higher supply voltage. Since it had become evident that some process variation was present, and since the necessity to use a higher supply voltage had caused a further shift in the switch points, the focus of all future testing was shifted to the epi-X version of the UVLO.

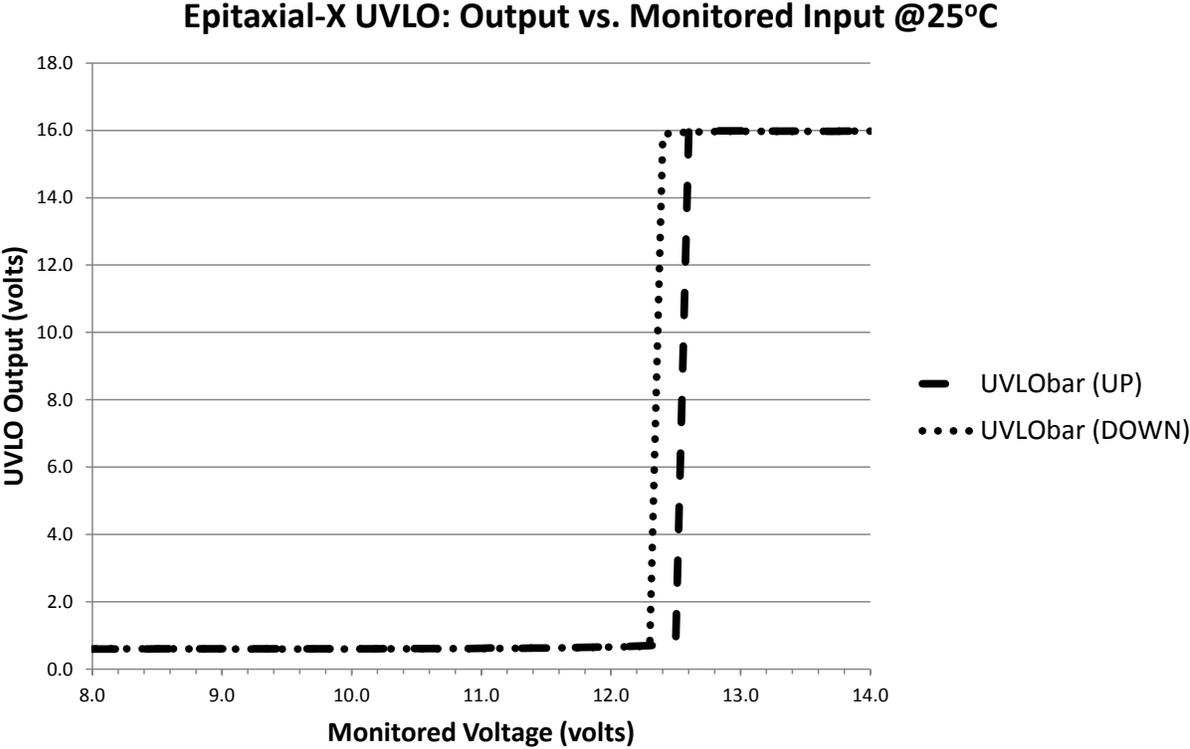


Fig. 61. Measured DC sweep for die R3C3 on wafer JU0505-29 at 25 °C.

The waveforms shown in Fig. 61 were captured from an epi-X version of the cell with no resistor network on the front end. In the figure, the upper and lower switch points are

approximately 12.6 V and 12.3 V, respectively. This can be contrasted with simulation waveforms of the same circuit using both 12 V and 16 V supplies at room temperature, shown in Fig. 62. The consequences of using a higher supply voltage are an overall shift higher in the switch points and an increase in the amount of hysteresis.

Although the switch points for the circuit were anticipated to switch near 9 V, simulation indicated that a shift to a higher switch points was anticipated when running at the higher supply voltage. The measured value for both the higher switch point and the simulated value are shifted up by approximately 3 V.

Referring back to the discussion on Eq. (4.17), it is noted that V_{SPH} is linearly proportional to V_{DD} . Thus, as V_{DD} increases, it is anticipated that the V_{SPH} would increase as well. Taking Eq. (4.13) and solving for V_{SPL} yields:

$$V_{SPL} = \frac{\sqrt{V_{DD} - V_{T3} - V_x}}{\sqrt{\frac{R_1 \beta_2}{2}}} + V_x + V_T + I_2 R_2 \quad (4.22)$$

which indicates that V_{SPL} trends upward with the square root of V_{DD} . Thus, while both switch points trend upward with V_{DD} , the lower switch point trends slower than the upper switch point. Thus, there is both an upward shift in switch points and more hysteresis with an increase in temperature, as indicated in Fig. 62.

While performing DC sweeps of the epi-X version of the UVLO, data was also captured for the current draw of the circuit. For the JU0505-29_R3C3 die, the maximum current draw was 1.66 mA. It had been revealed at a group meeting that the original 1 mA target was conservative and that as much as 5X more current would still allow the system to meet the overall current budget. Therefore, while this measured value was higher than the originally targeted figure of 1 mA, it was not a roadblock to integration of the UVLO with the gate driver system.

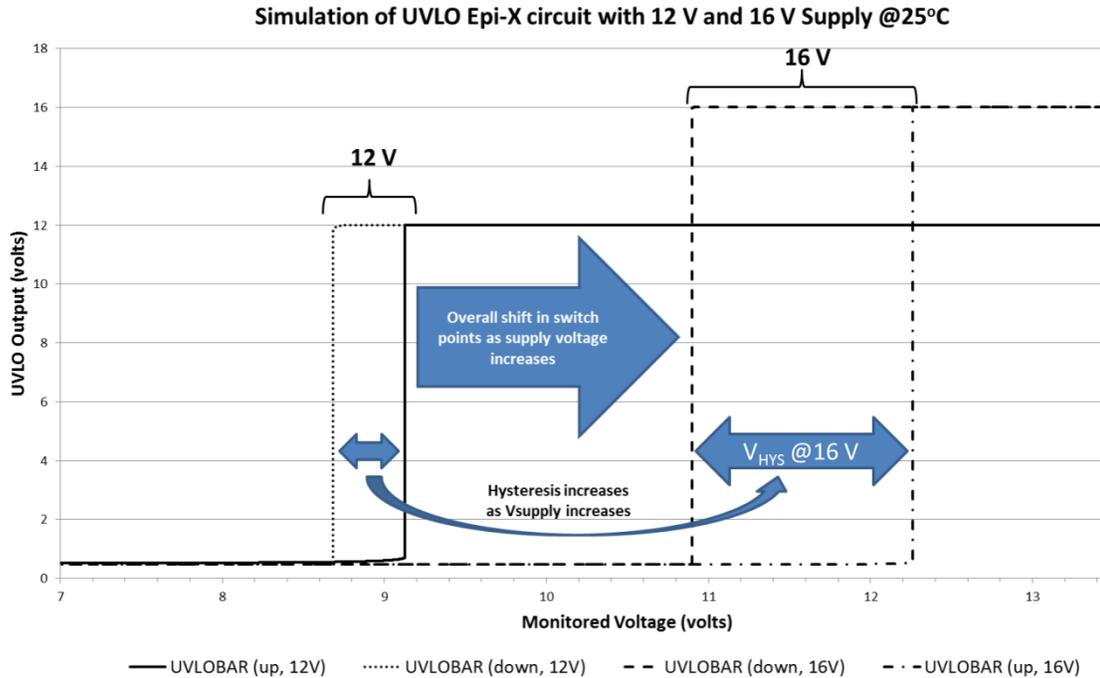


Fig. 62. Simulation of the UVLO epi-X circuit using 12 V and 16 V supplies at room temperature.

Next, in order to more accurately measure the switch points and rise/fall time information over temperature, transient testing was conducted. The front end of the Epi-X version of the UVLO was connected to an external potentiometer so that the switch points could be adjusted in real time. Stimulus for the input of the UVLO was a 0 to 20 V ramp generated using the arbitrary function generator. Based on information acquired during previous project meetings, it was assumed that the voltage being monitored (i.e., the UVLO input) would change at the rate of approximately 1 V for every 50 μ s. Using this as a guideline, the ramp was configured to ramp up to 20 V in 1 ms and back down at the same rate, for an overall signal period of 2 ms. Since the output from the function generator was 20 V_{p-p}, the output was put in series with a second 10 V DC voltage source in order to produce a final waveform output that

ramped from 0 to 20 V. The second DC supply was used to supply 16 V DC power to the UVLO. Rise and fall times were measured from the 10% and 90% points in the signal swing.

Fig. 63 shows the measured rise time for the JU0505-29_UA-SPLIT_R2C5 epi-X die at room temperature. As previously mentioned, the output of the UVLO was not intended to drive large loads and was not buffered to do so; therefore the measured value for rise time of 21.9 μs was not surprising considering the amount of capacitive load. However, it was considerably larger than the desired rise time of 10 μs or smaller set forth in the target specification. The fall time, meanwhile, was measured to be approximately 2 μs . It is worthwhile to understand how much load capacitance the test setup contributes in order to fully appreciate the impact that it has on the measured rise/fall times.

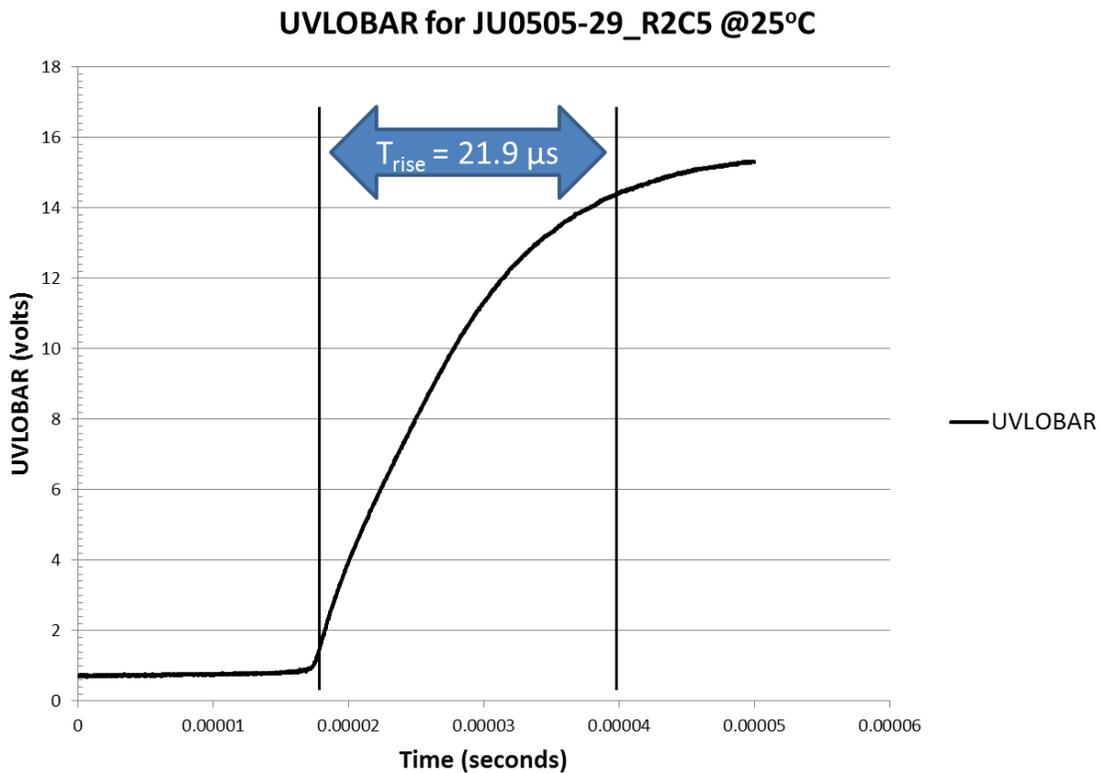


Fig. 63. Measured rise time for the JU0505-29_UA-SPLIT_R2C5 Epi-X die.

The signal path being driven by the UVLO consisted of a needle probe connected to an RG-174 coaxial cable that was 6 ft. in length. That cable connected to a bulkhead connector on the prober chassis, which (for the measured signal in Fig. 63) was connected to another 6 ft. of RG-58 coaxial cable. The RG-58 was then connected to the scope, which would add an additional load on the order of 10-15 pF. Since RG-174 has a nominal capacitance of 30.8 pF/ft. [44] and RG-58 has a maximum capacitance of 26 pF/ft. [45], the capacitive load in the coaxial cable alone is calculated to be near 340 pF. After re-simulating the UVLO with a capacitive load of 340 pF, the simulated rise and fall times were 27 μ s and 1.6 μ s, respectively. Since the manufacturer specifies that the figure of 26 pF for RG-58 is worst case, it is a reasonable assumption that the actual capacitance is somewhat lower than what was calculated, which brings the measured value into reasonable agreement with the simulated value.

To try to minimize the load contributed by the coaxial cables, the oscilloscope was moved closer to the probe station and the RG-174 from the probe was connected directly to the oscilloscope. This reduced the amount of capacitance in the path by one-half and yielded rise and fall times of 10.3 μ s and 960 ns, respectively. This result confirmed that the coaxial lines in the measurement path were contributing significantly as capacitive loads on the output.

The amount of actual capacitance in this case is easy to estimate if it is assumed that there are approximately three time constants between the 10% and 90% signal levels. Since the time constant $\tau = RC$, and since the pull up resistor in the final UVLO output stage is 30 k Ω , this equates to approximately 114 pF of load capacitance. This is slightly less than what the length of the RG-174 would indicate, however the assumed length of 6 ft. was an approximation and there is likely some variation in the capacitance per unit length figure for cables produced by different manufacturers.

Since the UVLO output was intended to drive no more than a few gates of capacitance (on the order of a few pF), the proper way to measure the output would be via the use of an active probe. Since an active probe was not available at the time, a series of measurements were completed over temperature using the RG-174 cable only. These results are presented in Table 17 for the JU0505-29-UA-SPLIT_R2C5 epi-X die and can be used to compare the general effect of temperature on rise and fall times.

TABLE 17. RISE AND FALL TIME DATA FOR JU0505-29-UA-SPLIT_R2C5

	Die Temperature			
	25 °C	125 °C	225 °C	300 °C
Rise Time (μs)	10.3	11.4	12.8	12.9
Fall Time (μs)	0.960	0.510	0.480	0.420

The increase in temperature would also cause an increase in the value of the resistors. This increase in resistor value with temperature was manifested as an increase in the measured rise time. As already mentioned, the devices in this process tend to have a lower $R_{DS(ON)}$ with higher temperature, which is indicated by a shorter fall time as temperature increases.

While collecting data across temperature from 25 °C to 300 °C, data for the upper and lower switch points was collected as well; later, more data was collected for temperatures down to -55 °C. All captured data is presented in Table 18. As expected, the amount of hysteresis is more than originally planned at room temperature, due to the higher supply voltage in use. While the upper switch point (V_{sph}) is relatively stable over temperature, the lower switch point (V_{spl}) trends lower as the temperature increases. One positive aspect of the trend, however, is that the amount of hysteresis does not decrease with an increase in temperature, which would lead to instability. Another noteworthy fact is that the UVLO still continued to function when tested at 300 °C, a temperature that is 50% higher than the specification dictates for the high end

of the operating range. Therefore, even at the higher-than-rated temperature of 300 °C, the UVLO would still be able to assert a fault before the monitored voltage dipped below the absolute allowable minimum of 14 V. At the maximum operating temperature in the specification (200 °C), approximately 3.5 V of hysteresis was measured. While this figure is larger than originally desired, it is still within bounds that allow for proper operation of the UVLO across the targeted temperature range; in fact, data recorded shows the UVLO operational throughout the temperature range from -55 °C to 300 °C. A plot of the data presented in the table is shown in Fig. 64, where the downward trend of the lower switch point is obvious.

TABLE 18. UPPER AND LOWER SWITCH POINT DATA FOR JU0505-29_UA-SPLIT_R2C5

	Die Temperature						
	-55 °C	-25 °C	0 °C	25 °C	125 °C	225 °C	300 °C
V_{sph} (volts)	19.8	19.5	19.4	19.3	19.2	19.1	19.1
V_{spl} (volts)	19.3	18.9	18.5	18.2	16.6	15.3	14.6
V_{HYS} (volts)	0.5	0.6	0.9	1.1	2.6	3.8	4.5

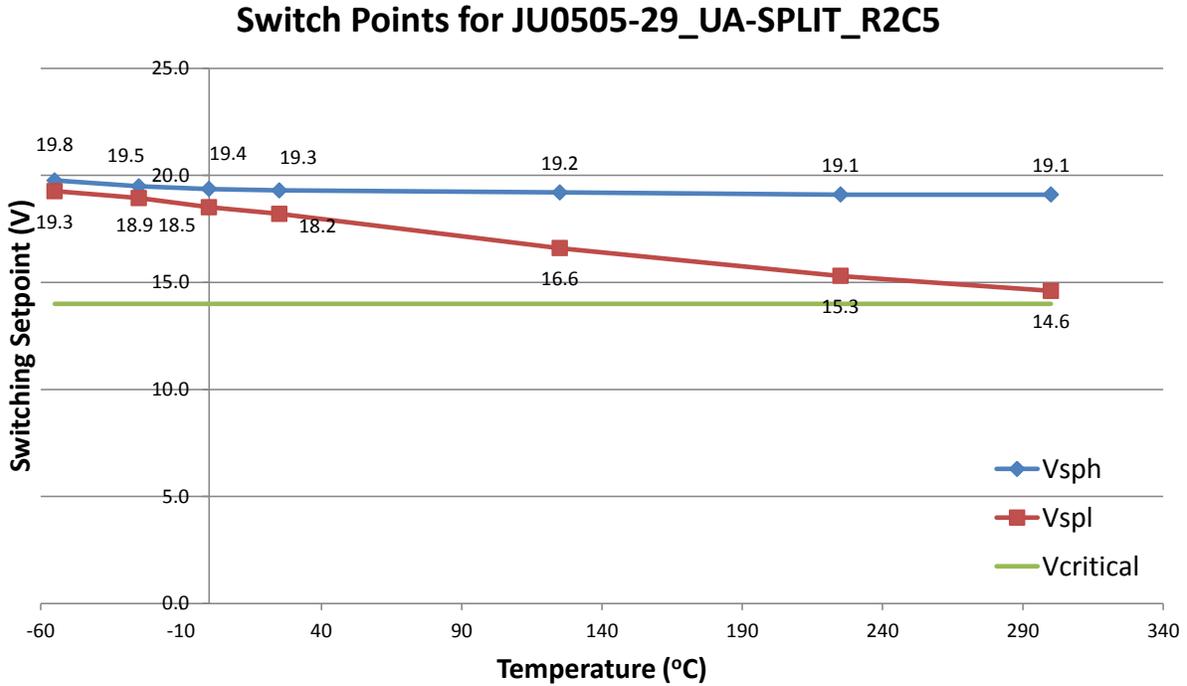


Fig. 64. Switch point plot for JU0505-29_UA-SPLIT_R2C5 from -55 °C to 300 °C.

While it is possible to project the rise and fall times for the case when the circuit is driving onboard logic by using calculations based on the known load at the time of test, an active probe was sought out and used to measure the output of the UVLO in order to attain a direct measurement. According to datasheet for the PicoProbe model 12C active probe, the load presented to the device under test is 0.1 pF. Since the active probe was very close to the heated chuck, measurements were captured at only 25 °C and 125 °C to avoid damaging the probe. The results for these measurements are shown in Table 19, where it can be seen that the rise and fall times are significantly lower and fall well below the 10 μs targeted in the original specification, leaving ample time for the signal to propagate through additional logic and still meet the desired timing specification. The data in the table was captured using a 16 V supply after adjusting the external potentiometer to yield switch points near the targeted values at 25 °C. These results

provide confirmation that the rise and fall times of the UVLO are well within the targeted specifications. As anticipated, the trends seen in the rise and fall times using an active probe mirror those seen in Table 17.

TABLE 19. UVLO RISE/FALL TIMES ON JU0505-29_R2C5 USING AN ACTIVE PROBE

	25 °C	125 °C
Rise time	248 ns	260 ns
Fall time	301 ns	111 ns

After the die for the implant process were delivered, it was discovered that the bulk of the UA-designed circuits (including the UVLO) would not be fabricated in the implant process due to a miscommunication among team members. However, while the data collected on the epitaxial version of the UVLO circuit was therefore the only data available, it provided sufficient evidence to validate the design approach and yielded a functional UVLO circuit that would require minimal modification to function in the process compatible with integration with the power MOSFETs.

CHAPTER 5 – CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

High temperature, low voltage SiC circuits will have a significant impact on future power systems and integration of the logic and gate driver with the power devices has many advantages. Some level of fault protection in the gate driver circuit is necessary to protect the devices in the system and the driver itself. By detecting voltage drops in the system, the UVLO acts as a critical part of the fault protection circuitry in the gate driver. Although a literature search reveals that a number of silicon carbide-based circuits have been realized, including operational amplifiers [6], logic circuits [46], and gate drivers [47], [48], no gate driver or UVLO circuit implemented in silicon carbide process that could potentially be integrated with the power MOSFETs themselves could be found. For those instances where silicon carbide-based CMOS logic could be found, it was fabricated using a process that rendered it incompatible with die-level integration of the power devices.

The work herein has yielded the first UVLO fabricated in silicon carbide that is capable of being integrated with power MOSFETs and operates over a 350 °C range. The challenges faced during the work proposed were unique, because there were considerable process-based constraints encountered that would not be a factor in designs where integration with the power devices was not a primary goal. In addition, the final topology borrows concepts from other design approaches used in other processes to yield a unique topology that achieves the desired effect. This design and derivatives thereof could be used in future silicon carbide designs where under voltage lock out functionality is desired.

Captured waveforms show that the switching behavior of the fabricated device, while not ideal, allows for UVLO operation throughout the targeted temperature range from 25 °C to 200 °C. In addition, the circuit continued to provide a usable output at 300 °C and down to -55 °C. Measured rise and fall times were well below the 10 μ s time originally targeted, and sufficient hysteresis was maintained throughout the operating temperature range to prevent instability. Current draw was somewhat higher than anticipated; however this can partly be blamed on the use of a higher supply voltage for the device tested and the fact that the resistors in the process were nearly 20% lower in value than anticipated.

As discussed, data suggests that integration of the gate driver with the power MOSFETs could lead to reduced cooling system costs, lower assembly costs, and improved electrical performance. While the economic impact for an electric vehicle produced in high volume is theoretically significant, the resulting savings for the manufacturer will likely not be realized for 5-10 years based on current trends in the industry.

5.2 Future Work

While the circuit presented was functional across a wide temperature range, the need for an externally regulated voltage is likely the first limitation that needs to be addressed. The design of a completely autonomous onboard voltage regulator would reduce the integrated circuit pin count and decrease the complexity of external circuitry.

The second limitation of this circuit is that it has not been verified in the implant version of the process. This fact, coupled with the need for a higher supply voltage due to the decrease in transistor transconductance, impresses the need for focus on these aspects of the final designs. PDK revision and design activity that analyzes process variability should lead to a final successful design.

While another student on the project successfully demonstrated a voltage regulator circuit, like the UVLO circuit, it required a stable external voltage reference [23]. Given the current status of the Cree process, it seems that realization of a stable onboard reference will remain a significant challenge until diodes (or diode-connected bipolar junction transistors) are available in the process to provide the devices necessary to construct a bandgap reference.

With maturation of the process, the resulting increase in yield might allow the UVLO (and other circuits) to benefit from a redesign that uses more complex topologies. Along with the addition of a stable voltage reference, this might allow the design of a UVLO based on a more complex circuit such as a comparator. Successful realization of such a topology, however, would require significant changes to the current process, a task that is made particularly challenging by the over-arching requirement to maintain process compatibility so that integration of the low voltage devices with the power MOSFETs remains possible.

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APPENDIX A: TEMPERATURE SENSOR

The specifications for the temperature sensor included on Fabrication Run One are shown in Table 20. In the hours before the tape out date, the circuit in Fig. 65 was put together quickly, iteratively simulated, and put on the chip in hopes it would satisfy the need for a temperature sensor.

TABLE 20. TEMPERATURE SENSOR SPECIFICATIONS

	Value	Comments
Temperature Operating Range	25 °C-200 °C	Wider range preferred
Footprint	N/A	None specified; smallest possible pref.
Output	0 to 3 V	None specified; assumed CTAT output with range of 0-3 V

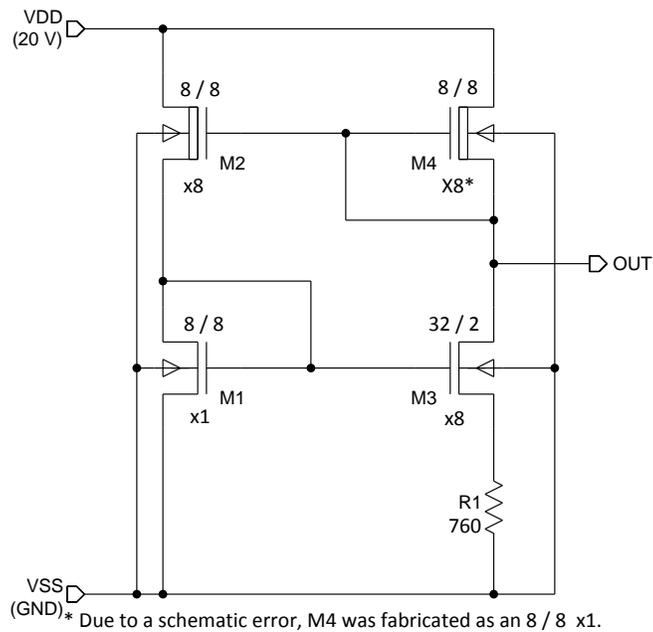


Fig. 65. Temperature sensor for Fabrication Run One.

This design is another example of a simple “beta multiplier”-inspired voltage reference derived from a CMOS-based version found in a popular text [41]. The primary goal was to use devices with a relatively small footprint so that the impact on layout area would be minimal. Just before tape out, this circuit was added to the final cell to allow characterization of the output and (with calibration) allow it to act as a temperature sensor on the die. As hinted in the figure, there was an issue during layout that affected this circuit, which will be discussed below.

Simulated transient waveforms for the topology in Fig. 65 over temperature are shown in Fig. 66. In this waveform, the supply voltage is being ramped over time from 0 to 20 V at each temperature. Since the reference output tends to be constant across a wide range of supply voltages, any difference in output voltage is primarily due to changes in temperature. In the simulation, the output of the temperature sensor was expected to vary from near 3 V at room temperature to approximately 1.5 V at 225 °C. While it was anticipated that process variation might cause the voltage to shift somewhat, the advantage of the approach was that the temperature could still be calculated from the measured voltage if a simple calibration was performed on the device.

As has already been mentioned, however, there was a design error introduced into the schematic which caused M4 in the circuit to be mistakenly replaced with a smaller (8x8x1) device. While this led to a lower output voltage than what was desired, the output still varied with temperature and yielded a usable temperature sensor.

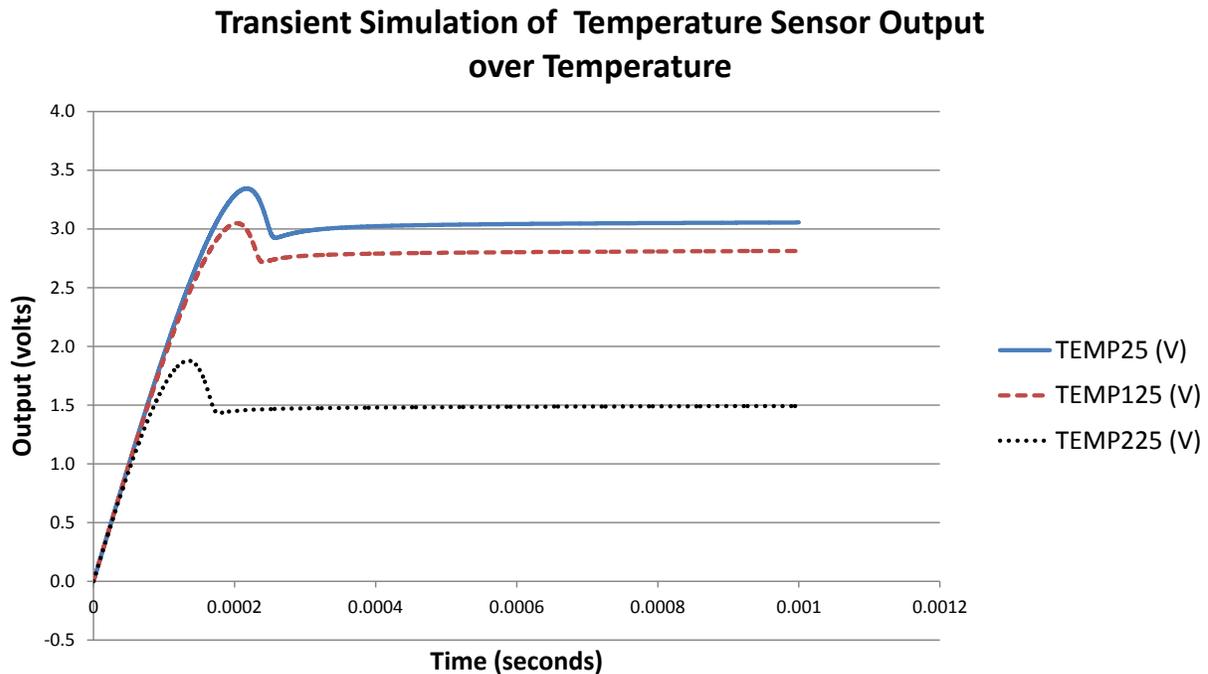


Fig. 66. Transient simulation of temperature sensor in Fig. 65.

Capture data for a working temperature sensor is shown in Fig. 67. Data was collected for six points between 20 °C and 270 °C. The resulting waveform shows a reasonably linear response up to about 125 °C. Using a piecewise linear approach, it would be possible at higher temperatures to translate the output voltage to a temperature reading as well. A number of temperature sensors were measured; due to process variation, the output voltages were found to vary by a few tenths of a volt. However, with proper calibration, any of these devices could be used to measure temperature. Once packaged, the same die was characterized over a wider temperature range, since this allowed it to be safely placed in a temperature cycling oven.

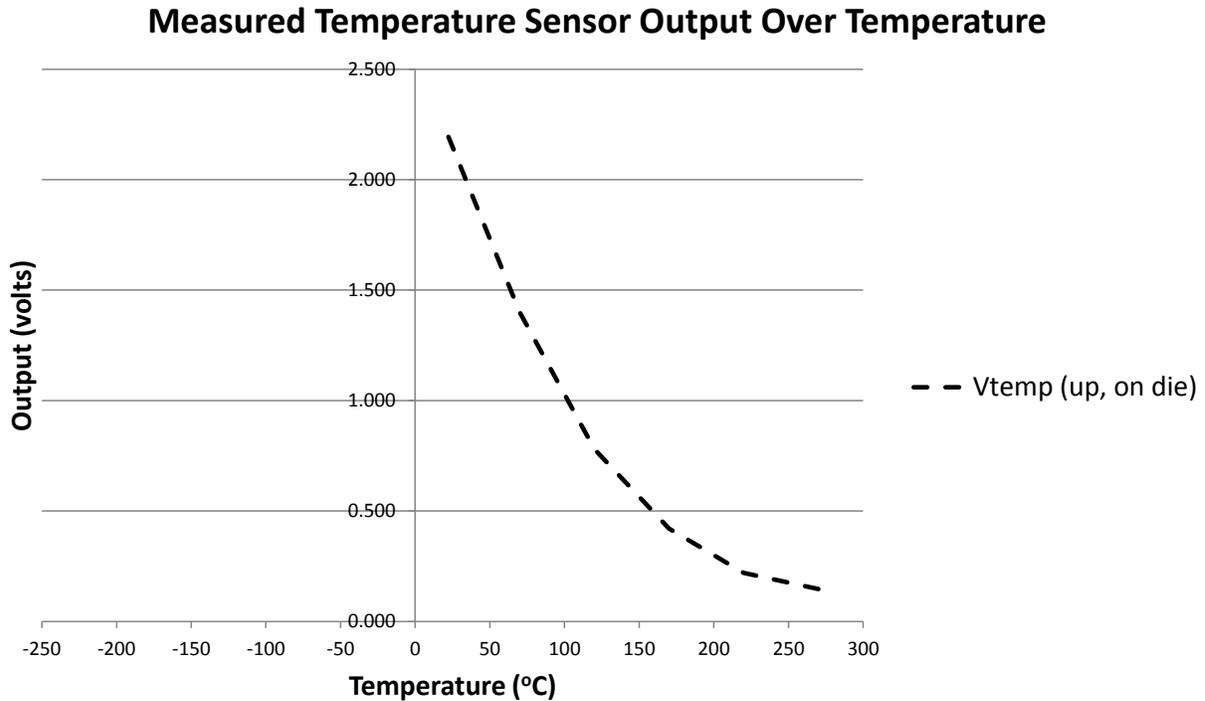


Fig. 67. Measured temperature sensor output over temperature (probe data).

During further testing, liquid nitrogen was used in the oven to fill in the gaps for captured data from -184 °C to 23 °C. Two runs were executed where data was captured with temperature either increasing or decreasing over portions of the aforementioned range. This data was then combined with data previously captured at the probe station for a separate die; the resulting waveform is shown in Fig. 68. In the figure it is found that the previously mentioned linear region of the sensor output extends down to approximately -100 °C. It is also worthwhile to point out that while the data across temperature was collected using two separate die, the variation between these die was not significant.

There was, however, one issue. The output of the temperature sensor at room temperature was approximately 2.2 V. As already mentioned, due to a workflow mistake during layout, one of the transistors in the circuit was 8 times smaller than desired. Subsequent re-

simulation of the circuit indicated that the stable output should have been near 0.7 V, not 2.2 V. Process variation was the assumed culprit for this discrepancy at the time, although in hindsight it is possible that an unexpectedly higher contact resistance for connections made to the diffusion resistors might also be to blame, since all resistor contacts used minimum sized p-cell generated contacts.

Ultimately, however, the measured data indicates that the topology was functional over a wide temperature range from approximately -125 °C to 200 °C and with calibration would satisfy the needs for an onboard temperature sensor.

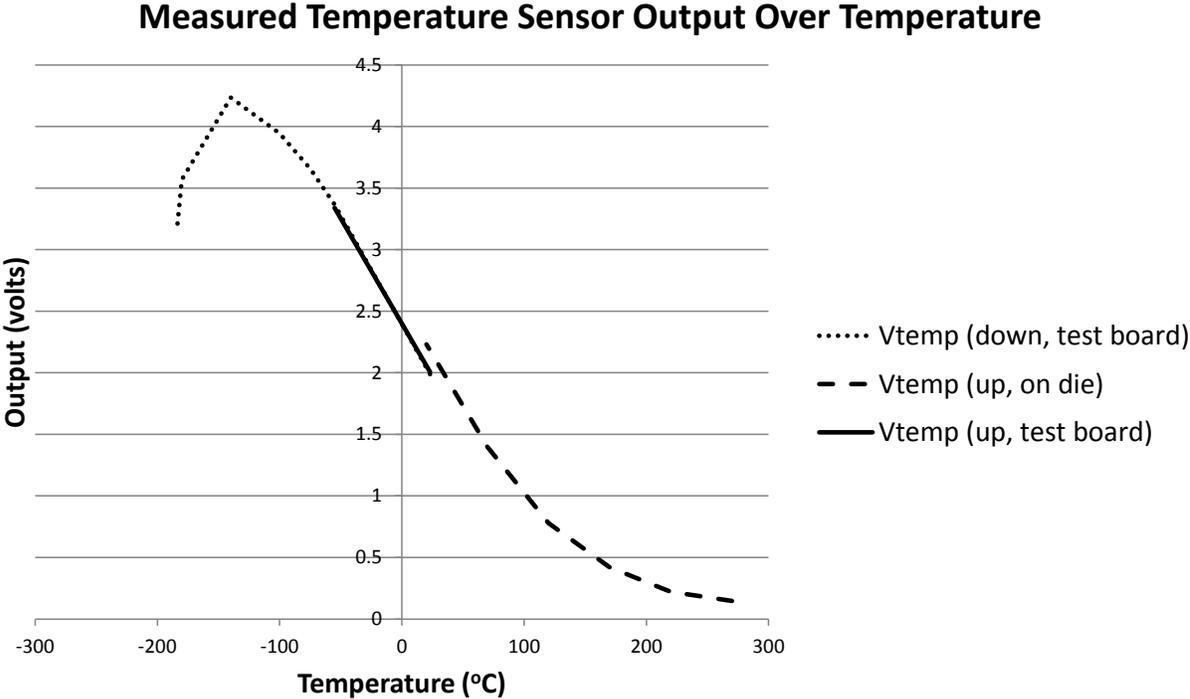


Fig. 68. Measured temperature sensor output over temperature.

APPENDIX B: RESISTOR TEST STRUCTURES

The resistor test structures were based on the Transmission Line Model (TLM) method. Fig. 69 shows the annotated layout for the polysilicon TLM structure. Taps were created along the length of each strip so that the resistors were scaled at 1x, 2x, 4x, 8x, and 16x. The structures allow both measurement of the sheet resistance and extraction of the contact resistance for each resistor type. Contact resistance is extracted by plotting the resistance of each resistor strip, fitting the data to a straight line, and then finding the y-intercept for that line. The amount of resistance at the y-intercept point represents the resistance present for a zero-length resistor and, when divided by two, yields the resistance in one contact. The TLM structure size and layout for the diffusion resistor was identical to that of the polysilicon structure.

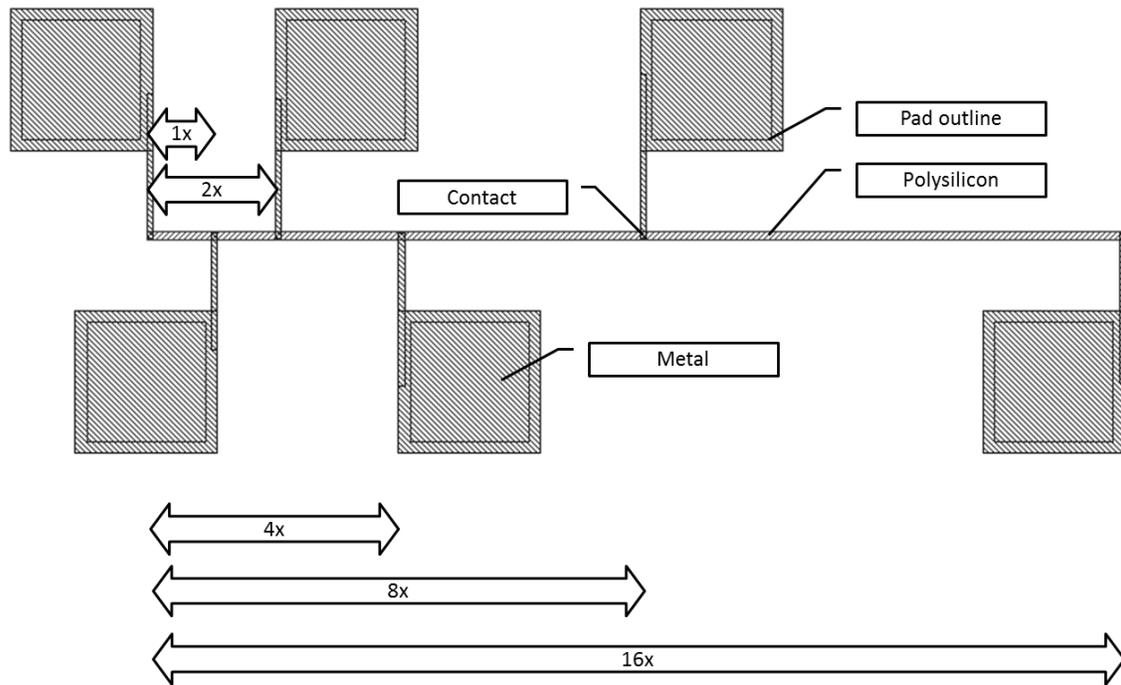


Fig. 69. The polysilicon TLM structure designed to extract contact resistance.

Table 21 shows the anticipated measured resistances of each structure for a 1x line segment (without contact resistance), based on the sheet resistances used in the PDK for each process.

TABLE 21. TLM STRUCTURE ANTICIPATED MEASURED RESISTANCES FOR THE 1X LINE SEGMENT

	Epitaxial	Implant
Polysilicon	918 Ω	1119 Ω
Diffusion	1242 Ω	2300 Ω

Testing results for the resistor test structures took more time to collect than expected, due to apparent issues with the contacts used on the test structures. Initial test measurements tended to produce extremely large resistance values for all diffusion resistors and most polysilicon resistors. The probe tips were inspected and confirmed to be clean and undamaged. Since near-

minimum contacts were used for the TLM structures, it is assumed that the contacts may not have been completely etched.

Eventually, one polysilicon structure on the UA_CV1126-44 die was found where the measurements for all the TLM segments seemed reasonable. Initial results at room temperature for the polysilicon-based resistor test structure on CV1126-44_UA_R1C2 are shown in Table 22. The figures recorded in the first row of the table represent the measured resistance at the test structure pads for each resistor size in the structure. The data in this row is shown plotted in Fig. 70, where a line representing a linear fit for the data is overlaid and the equation for the resulting line is also shown. The y-intercept for the linear fit is 320.32 Ω ; since this should represent the resistance of two contacts, the resulting average contact resistance is 160.2 Ω per contact. In the second row of the table, this contact resistance has been subtracted from the originally measured amount to show the value of each resistive segment. The third row of the table shows the value that was anticipated based on the sheet resistances used in the PDK, while the fourth row expresses the percentage of error between the anticipated and actual values.

TABLE 22. POLYSILICON-BASED RESISTOR TEST RESULTS FOR CV1126-44_UA_R1C2 AT 25 °C

Length	1x	2x	4x	8x	16x
Measured Resistance	1,035 Ω	1,725 Ω	3,130 Ω	5,937 Ω	11,581 Ω
Resistor Value	714 Ω	1,404 Ω	2,809 Ω	5,617 Ω	11,260 Ω
Anticipated Value	918 Ω	1,836 Ω	3,672 Ω	7,344 Ω	14,688 Ω
% Error	22.1%	23.5%	23.5%	23.5%	23.3%

The results seen in Table 22 indicate that the value of polysilicon resistors in the process were about 23.5% less than anticipated. Since the resistors in the UVLO were all diffusion

resistors, this measured value had very little impact on switch point behavior. However, these results do indicate that the sheet resistance of the poly silicon was less than expected, which would tend to bode well for the parasitic resistance introduced by polysilicon in the layout.

In order to capture data for the diffusion resistors, TLM structures on epitaxial die designed by the team members at Oak Ridge National Labs were measured. The results from these measurements across temperature can be seen in Table 23. The ORNL designs used contacts that were larger than those used on the UA design, which provided a more reliable connection to the underlying resistor. The data in the table indicates that the values of the diffusion resistors, much like those based on polysilicon, tended to be lower than the anticipated value, some by as much as 18%.

Resistance by Length for Poly Resistor on CV1126-44/R1C2

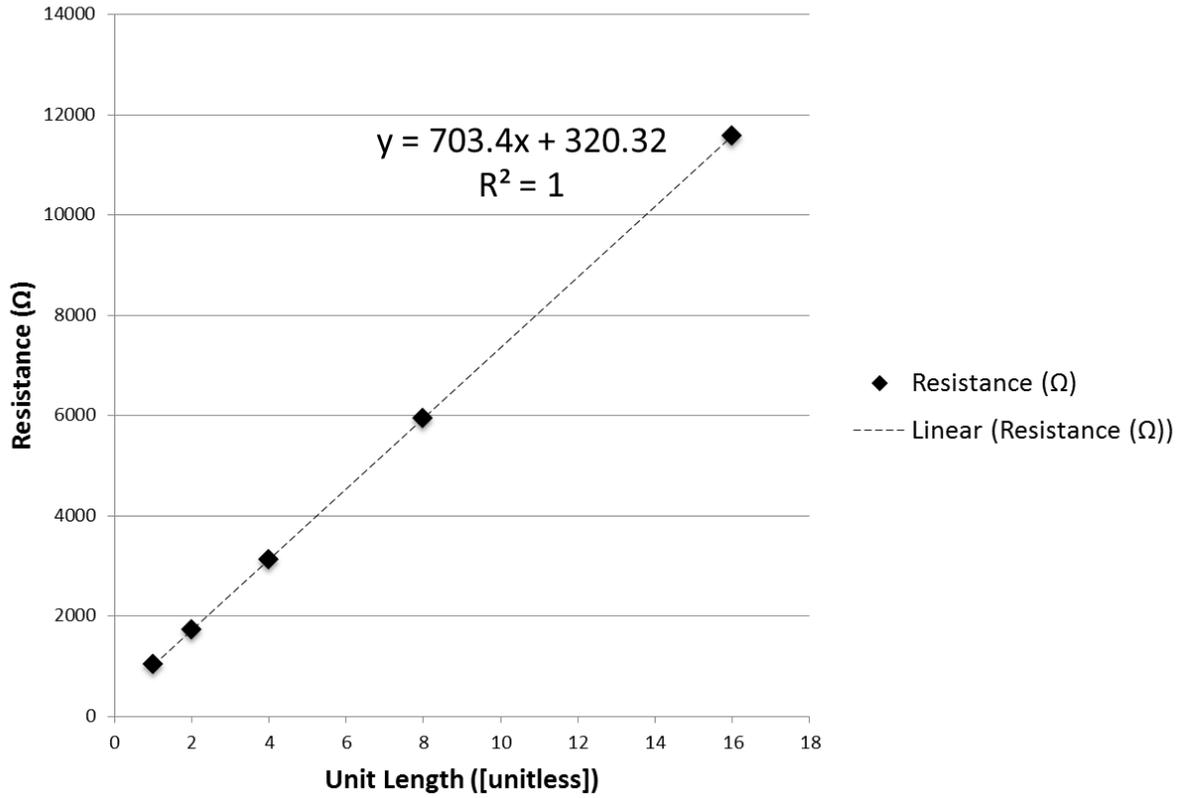


Fig. 70. Resistance vs. length for the polysilicon resistor test structure on CV1126-44/R1C2.

TABLE 23. RESISTOR DATA FOR EPI RESISTORS ON ORNL_PEP1_2.0_JU0505-28 AT 25 °C

Device	Sheet resistance
R3C1	94 Ω/□
R5C3	101 Ω/□
R2C4	109 Ω/□

