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Design and Fabrication of Inverter and Rectifier Modules for Indirect Matrix Converter Applications

Design and Fabrication of Inverter and Rectifier Modules for Indirect Matrix Converter Applications

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

by

SaikishoreTalakokkula
Jawaharlal Nehru Technological University
Bachelor of Technology in Electronics and Communication Engineering, 2010

August 2013
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

_____
Dr. Simon Ang
Thesis Director

_____
Dr. Juan Carlos Balda
Committee Member

_____
Dr. H. Alan Mantooth
Committee Member

Abstract

In power converter applications, silicon carbide (SiC) power semiconductor devices are preferred over their silicon counterparts due to many advantages such as wide bandgap, high junction temperatures and low on-state resistance. The SiC devices provide reduced conduction and switching losses. Due to the above mentioned advantages the power conversion efficiency of SiC devices is better compared to that of silicon (Si) devices.

This thesis studies the implementation of 1200V/17A Normally-off SiC JFETs for an indirect matrix converter (IMC) application. A discussion on the parasitic inductance optimization is presented based on the electromagnetic simulation results extracted from the Ansoft Q3D extractor. The thermal analysis for the modules is performed using Dassault system SolidWorks 3D CAD tool to obtain optimized designs under working conditions. The IMC consists of both Inverter and Rectifier Power modules which are externally connected with a dc link. Each switching path is carefully analyzed and thereby the designs and layouts are minimized to have the least parasitic circuit elements on those IMC modules. A discussion on the conduction losses is described based on Q3D simulations.

The two modules were fabricated using a direct bond copper (DBC) substrate. The procedure for building the modules are explained along with the materials used. The fabrication steps with respect to designing and processing the module are detailed. Finally, tests are conducted for the IMC converter. The results obtained thus demonstrate the operation of IMC modular prototypes.

Acknowledgements

I thank almighty god and my parents, for giving me strength and moral support in my academic and other activities all the years of my life.

I would like to thank my advisor, Dr. Simon Ang for his continuous support throughout my graduate studies. This work could not have been finished without his guidance, support and time, and I will never forget him as he has been my inspiration as I hurdle all the obstacles in the completion of this research work.

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Additional thanks go to my colleagues Shirley, Shilpa, Jinchang, Marwan and Atanu, for their valuable helpand advice in performing fabrication procedures, thermal and electrical simulations.

Last but not the least, I thank all my friends who made my Master's journey a memorable experience.

Abstract

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I. Introduction

1.1 Power Modules:

A power electronic module can be defined as an electronic device integrated with several power semiconductor devices with the required electrical paths and heat flux path. It was in the mid seventies of the past century that the first power module was built [1]. The first system that was built has a combination of two chips on a metalized ceramic substrate under a common housing. In general most of the power modules have tremendous advantages, as before the discrete components are attached to coolers. The major changes that the power modules brought to the power electronic systems are:

- Compact size.
- Cost effectiveness.
- Increased reliability.
- Lower weight.

The major applications of the power electronic modules are found in switching mode power supply, uninterrupted power supplies (UPS), industrial motor drives and HVDC (High Voltage Direct Current) inverters, and AC Motor Controls (VVVF Inverter, Servo Amps, etc) [2]. Over the last decades, power electronic packaging technology has evolved incremental improvements in performance and reliability. The requirements for cost, compact size and less weight require improvement in high power packaging density. To decrease the volume of the converter, the volume of the power electronic components must first be reduced.

The basic functions of power module packaging include connection of power semiconductor chips to external units, removal of generated heat within the module, and protection ofthe module from environmental hazards [3]. Power semiconductor chips generate losses during conduction and switching. Heat sinks and thermal issues are vital to semiconductor packaging as they are one of the limiting factors for packaging. Due to increase in the current requirements in recent years the demand for high thermal conductivity modules is increasing. Currently there is ample research on increasing the thermal ability of module packaging [3].

1.2 Silicon Carbide Devices:

Silicon Carbide (SiC) devices have enhanced performance in most of the aspects when compared to its silicon (Si) counterparts. Switching devices with wide bandgap silicon carbide (SiC) offer a higher performance improvement compared with Si devices. Some of the major advantages of using SiC devices over Si devices are:

- Higher breakdown voltages.
- Low On resistance.
- Higher thermal conductivity.
- Wider bandgaps hence higher operating temperatures.
- Better reverse recovery.

These advantages of SiC devices enable us to design power electronic modules with lower parasitic inductance values and also higher junction temperatures to extend the limits of thermal capability. For low-voltage dc–dc converter the soft-switching conditions can be achieved with very low effort using SiC devices. SiC devices offers the reduction of chip size which could help

to increase the power density. Due to the above mentioned advantages SiC offers low switching losses resulting in a higher efficiency and compact design [4].

In applications, where a high output voltage is required, high-voltage SiC diodes offer a huge advantage as they enable lower voltage drop and thus resulting in lower losses. However, it is also important to keep in mind that the SiC devices are relatively new and will keep improving in the future [4].

1.3 Matrix Converters

Matrix converters (MC) have fully controlled bidirectional switches that work without any dc-link circuit, and hence, they do not require large energy storage elements [5]. When compared to conventional two stages ac/dc/ac converters MC has various advantages: for example due to the absence of energy storage elements MC has a simple and compact power circuit, this allows as increase in system life time or reliability [6]. In MC system the ratio between the input and output power factor can be unity if minimum harmonic distortion is maintained [7], apart from this MC provide sinusoidal input currents and also sinusoidal output voltages [1], [8].

Conventional Matrix converters (CMC) and Indirect Matrix Converters (IMC) are two different types of MCs. CMC performs voltage and current conversion in a single stage from the input to output, whereas IMC carries out it in two power stages [9]. The basic indirect matrix converter topology is shown in Figure 1.1. The input phase of the IMC is a three phase rectifier which has 12 unidirectional devices and the next stage is a conventional three phase inverter with 6 unidirectional devices. The IMC is bidirectional and has low switching losses when compared to CMC.

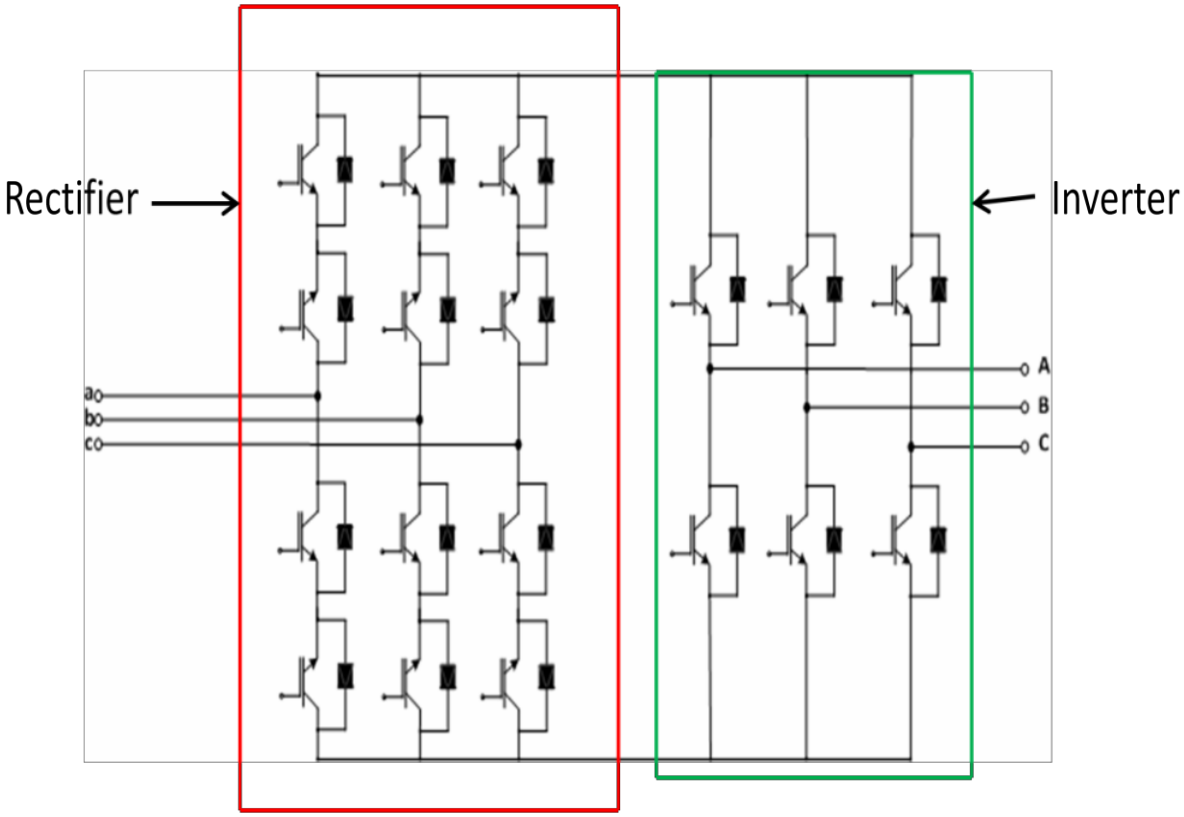

Figure 1.1 IMC Schematic.

SiC devices can achieve higher power densities and increase reliability at higher temperatures. For the packaging of the IMC SiC JFET's are used, as it has some major advantages over conventional Si based IGBT's and MOSFET's such as low on-resistance and high breakdown voltages[7]. The papers [10] & [11] analyze different converter modules that use SiC-JFETs as primary devices where the JFETs provide high frequency switching.

1.4 Project overview

The IMC with its control system is shown in Figure 1.2. Integration of all the device components into a single level of IMC is a major issue, as IMC has a large number of discrete components that makes it bulky and also adds huge parasitic circuit elements. Power module packaging provides a better solution to mitigate this problem. The inverter and rectifier modules will be constructed using power electronic packaging techniques, which can decrease the parasitic circuit elements and provide a compact size to the system.

The first challenge in this project occurs in the design segment, where an optimum design should be made to minimize the parasitic inductances. In the module packaging process the first stage starts with the design layout by exploring the devices that are to be used. In the next stage an optimal layout is designed based on thermal and electrical simulations. Finally the material selection is performed before the module packaging process.

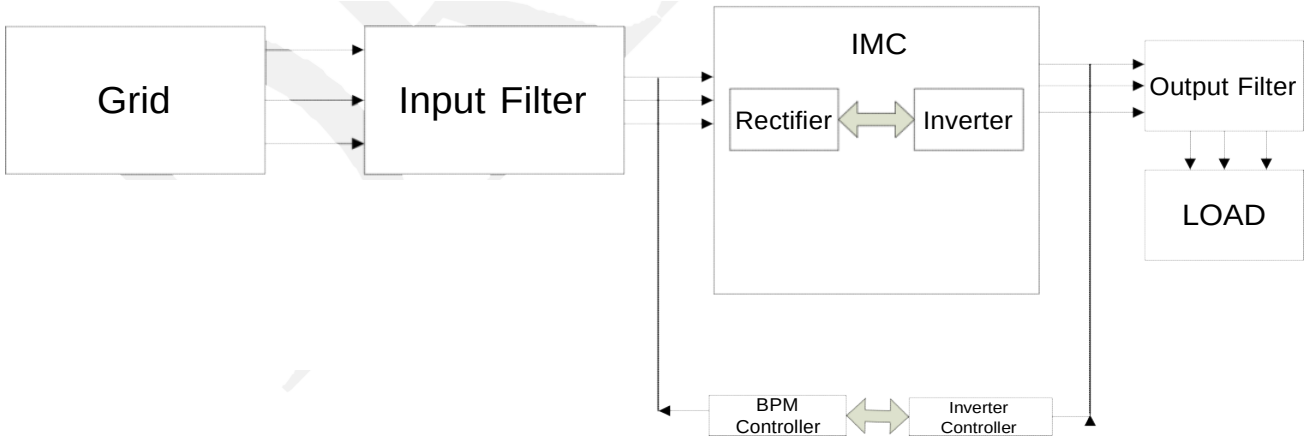

Figure 1.2 IMC Prototype

1.5 Packaging

IMC power modules are divided into two separate modules: inverter and rectifier modules. In general the processes for packaging and fabrication of these modules are similar . In this thesis, the design and packaging for these two modules are presented. Figure 1.3 describes the cross-sectional view of the module construction.

The important stages in module packaging are

- Layout design.
- Preparation of substrate.
- Device attachment using solder alloys.
- Wire bond inter-connection.
- Module protection.

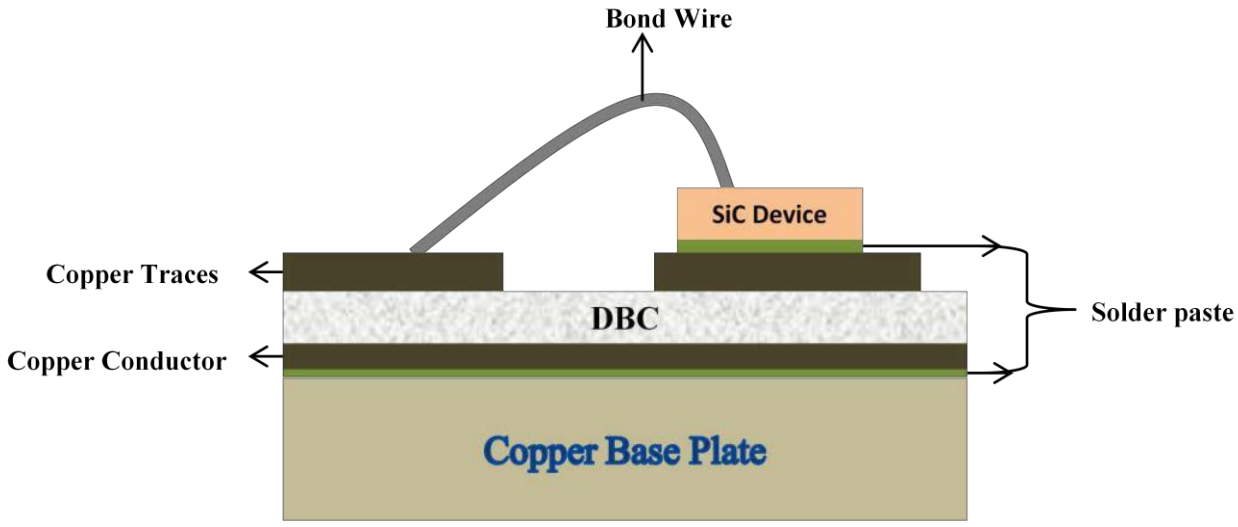

Figure 1.3 A Power Module Cross-Sectional View.

1.6 Organization of Thesis

This thesis is organized into six chapters that describe the important stages of IMC module design and fabrication. The next chapter describes the design aspects to minimize the parasitic inductances and the layouts. Chapter III describes the material selection for the process. The fabrication and packaging processes are presented in Chapter IV. Chapter V presents the test results. Chapter VI concludes and provides some aspects of future work for this thesis project. Finally the process flow steps for different techniques along with the mechanical layouts and travelers are presented in appendices.

II. Parasitic and Thermal Analysis.

2.1 Introduction

This Chapter introduces the important aspects of module layout. The design for both inverter and rectifier modules are critical to the system, since it defines the system performance. High power density and high switching frequency modules have faster switching rates. Due to faster switching, the parasitic inductance components play a critical role in system performance. These parasitic inductance causes different kind of losses such as module de-rating, ringing in the switching waveforms, energy losses, and over voltages [7], [12], [13]. Hence, careful layout and design of the modules are very important.

In this Chapter, various parasitic reduction techniques are used in module design. Based on the reduction techniques the inverter and rectifier module layouts are proposed. Later a discussion on parasitic extraction using ANSYS Q3D is presented where both modules are carefully analyzed. The conduction losses in these modules are studied. Electrical simulations are performed based on the switching positions of the IMC schematic.

To compare the simulation results, a time domain reflectrometry (TDR) technique is used to measure the parasitic inductances in these modules. Thus, both simulation and measured results of parasitic inductances are compared. Finally the finalized designs from the ANSYS Q3D are transferred into AutoCAD software to generate the photo masks.

2.2 Parasitic Inductance Reduction Techniques

The parasitic inductance in a power module mainly comes from the device package structures. A basic half-cell as shown in Figure 2.1 is first considered.

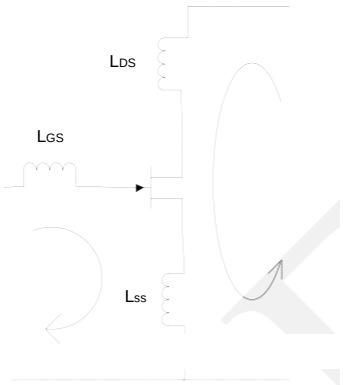

Figure. 2.1 Basic Half-cell

The three primary stray inductances from the current paths in the basic half-cell are [13]:

1. ―The gate loop inductance L_{GS} formed by the gate path‖[13].
2. ―The main switching loop inductance L_{DS} formed by the drain current path‖[13].
3. ―The common source inductance L_{SS} that exists in both loops‖[13].

The main switching loop inductance $L_{DS,}$ rather than the gate loop inductance L_{GS} contribute to ringing in the switching waveform. The gate-driverunit can usually be controlled more easily than the main power loop, which gives a smaller L_{GS}[13]. Switching loop has lower damping than compared to gate loop and similarly the gate resistance. Damping also exists in gate driver output impedance and JFET internal gate resistance. The trace resistances in the drain and source inter connection paths are usually quite small and unable to damp any oscillation. Its unable to decay any oscillations in switching when it has small inter connection resistances [13].

2.3 Important Guidelines:

The important guidelines from the paper [13] are ―for very high speed switching circuits the value of switching loop inductance L_{DS}should be minimized implies the diode and the JFET's are placed close to each other‖[13]. ―Placing the gate driver closer to the power device will minimize the value of gate loop inductance‖. Finally, to ―minimizing the common source inductance L_{SS}can effectivelyreduce the switching loss, which occurs from the results coupling effect of current loop between the gate and drain-source‖[13]. The module layout also plays an important role in parasitic circuit element generation. Careful layout can reduce the parasitic circuit elements significantly. Some of the important wire bond and design improvements are mentioned below.

Wirebond :

- The interconnection of the bonds are as short as possible.
- Increase the number of bondwires
- Increase the bond wire diameter

Substrate:

Large substrate area can make inductance large. Hence the maximum pattern utilization should be done.Widen the pattern width and shorten the pattern length can help to reduce the parasitic inductance.

The effective stray inductance is an important design consideration in a module. Parasitic inductances are present everywhere in a module. However, those parasitic inductances in the conduction path during switching on and off are the most important. In a half bridge switch, the

current conduction is between upper JFET and the lower diode, or between the lower JFET and upper diode [14]. Thus to decrease the parasitic inductance the physical length of the conduction path should be reduced for each leg of the switching positions.

Careful layout of switching leg can reduce the inductance between two switching devices. The stray inductance due to wire bonding, external soldering and package lead are present in packaged modules. When there is current flowing from an active switch to a reverse recovery diode, these parasitic inductances under high *di/dt* condition can cause damage to the devices. The parasitic inductance is also responsible for the electromagnetic interference by causing voltage spikes and oscillations.

2.4 Parasitic Analysis:

The parasitic analysis is very important in the module design segment. This allows controlling the losses associated with the parasitic circuit elements for the module. The IMC has two separate control power stages; they are the inverter and rectifier modules.

Inverter module:

The inverter schematic is shown in Figure 2.2 for the parasitic analysis. It has 6 unidirectional switches with two level motor drive topology and each switch consists of a 20A SiC JFET(J_{1p},J_{2p},J_{3p},J_{1n},J_{2n},J_{3n}) and a 20A anti- parallel SiC Shottky diode(D_{1p},D_{2p},D_{3p},D_{1n},D_{2n},D_{3n}). The main terminals are the two DC terminals X+ and X- and three I/O phase terminals P, Q and R; apart from that there are six gate terminals for the inverter module which are connected to a gate driver board using gate pins. It is also important to locate the gate pins along the outside edges of the package to enable the connections to external gate driver. By using the accurate dimensions of all the components and positioning them based on the module requirement a

layout is proposed. Figure 2.3 shows inverter power module Q3D showing the power devices and terminals.

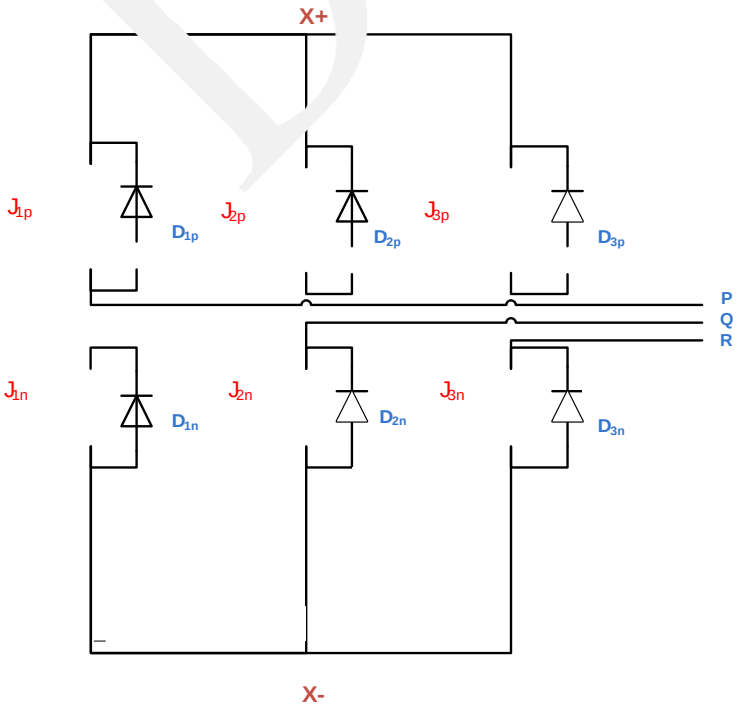

Figure. 2.2 Inverter schematic

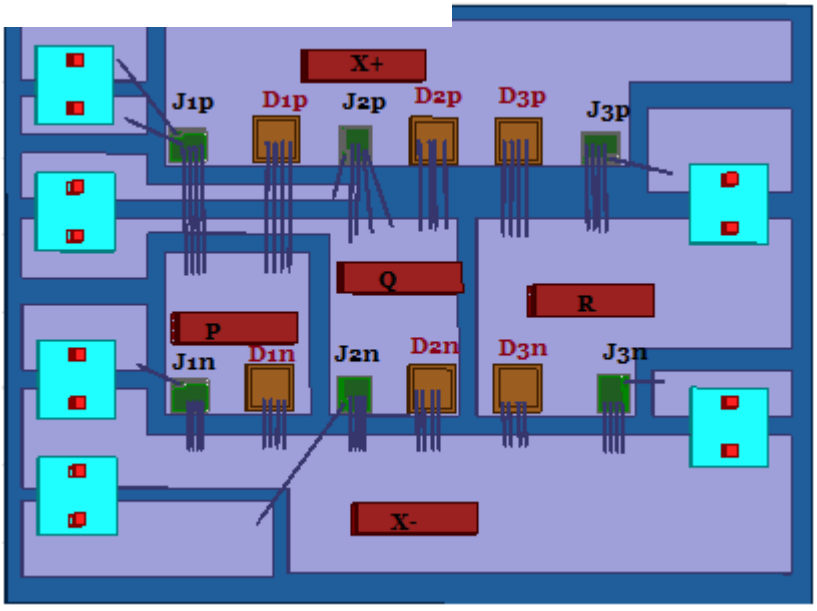

Figure 2.3 Inverter module Q3D layout.

To understand the parasitic inductance a paticular switching combination is considered in Figure 2.4a. The inverter switching operation in this combination starts from the current path at the SiC JFET J_{1A} and to the rectifier circuit through the dc link X+ as shown in the Figure 2.4 . The current then returns through the lower diode J_{3n} to the node R. The current commutates between the JFETs J_{2n} and J_{3n} in response to the input PWM control signals, thereby switching the dc-link

voltage between $v_{\diamond\diamond}$ and$v_{\diamond\diamond}$; and the remaining switches are open in this combination [7].

The
parasitic for this combination comes from the bond wires between the sources of the devices (J_{1p},J_{2n},J_{3n}) the DBC substrate traces, between the conducting traces and the connectors, and the bond wires between the gate pads of the JFETs and the gate connectors of SiC JFET.

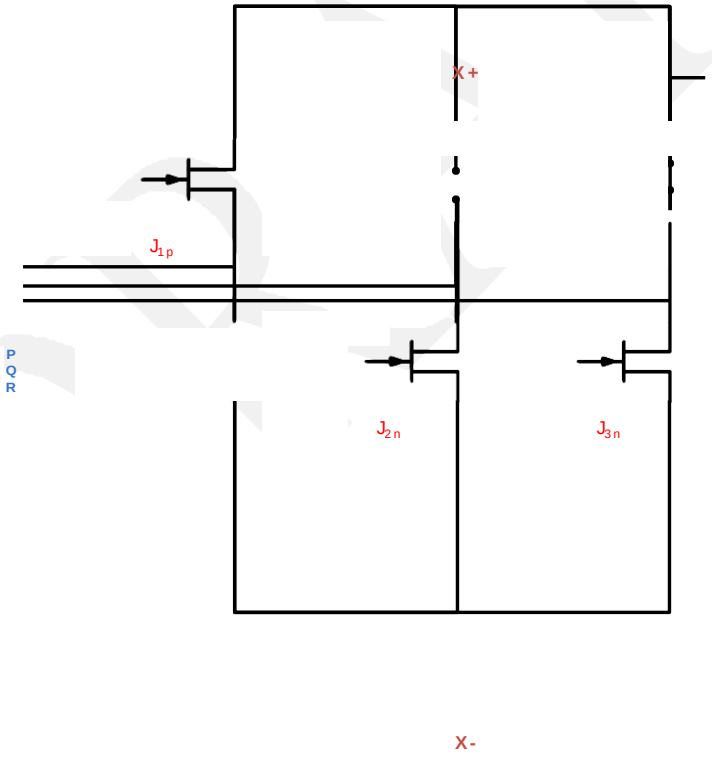

Figure 2.4a Selected switching combination-Inverter

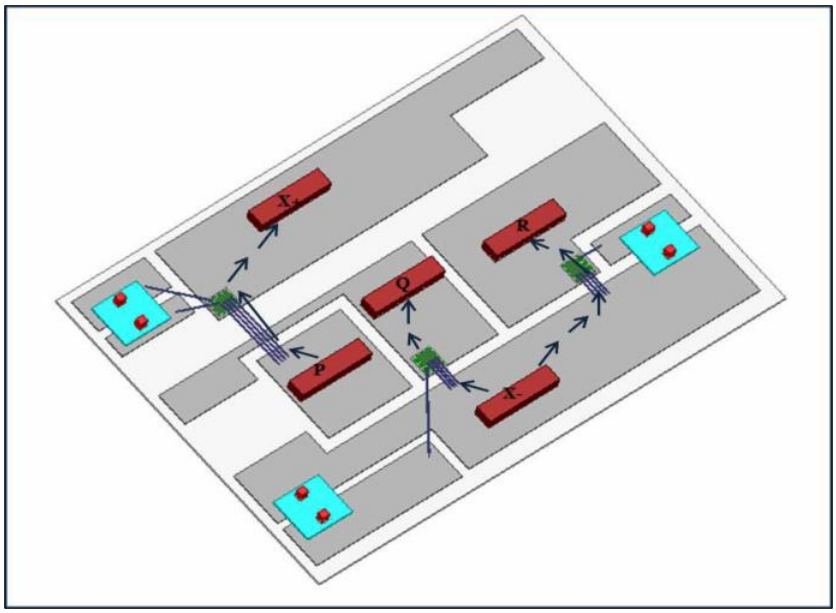

Figure 2.4b Parasitic induction paths on the Inverter module for a selected switching combination.

As the currents paths vary for each switching combination, the values of the parasitic inductances are different. Several layouts were analyzed before finalizing the inverter module layout. The parasitic circuit elements for this particular layout are summarized in Table 2.1. These parasitic circuit elements are extracted using the ANSYS Q3D software and the simulations are performed at 30 KHz frequency for all the switching combinations, where the gate parasitic inductance extraction is carried out at 50MHz. A higher frequency for the gate circuit extraction is due to the rise time of the gate signals. Also, the schematic of the inductance can be better understood with the circuit schematic of inverter along with the parasitic inductances shown in Figure 2.5.

Table 2.1 Inverter Module Parasitc.

Parameter	**J_{1A}**	**J_{3B}**	**J_{5C}**	**J_{2n}**	**J_{4n}**	**J_{6n}**
DC bus to drain stray inductance (nH)	3.4	2.1	3.2	6	2.12	5.7
Drain to input connectors stray inductance (nH)	5	3.4	5.2	2.8	3	2.8
Gate-loop inductance (nH) @ 50 MHz	7.6	16	6.8	5.8	14	5.6
Parasitic resistance (mΩ)	1.8	0.8	2.1	2.3	0.6	0.8
Conduction loss (mW)	0.52	0.23	0.6	0.66	0.2	0.23

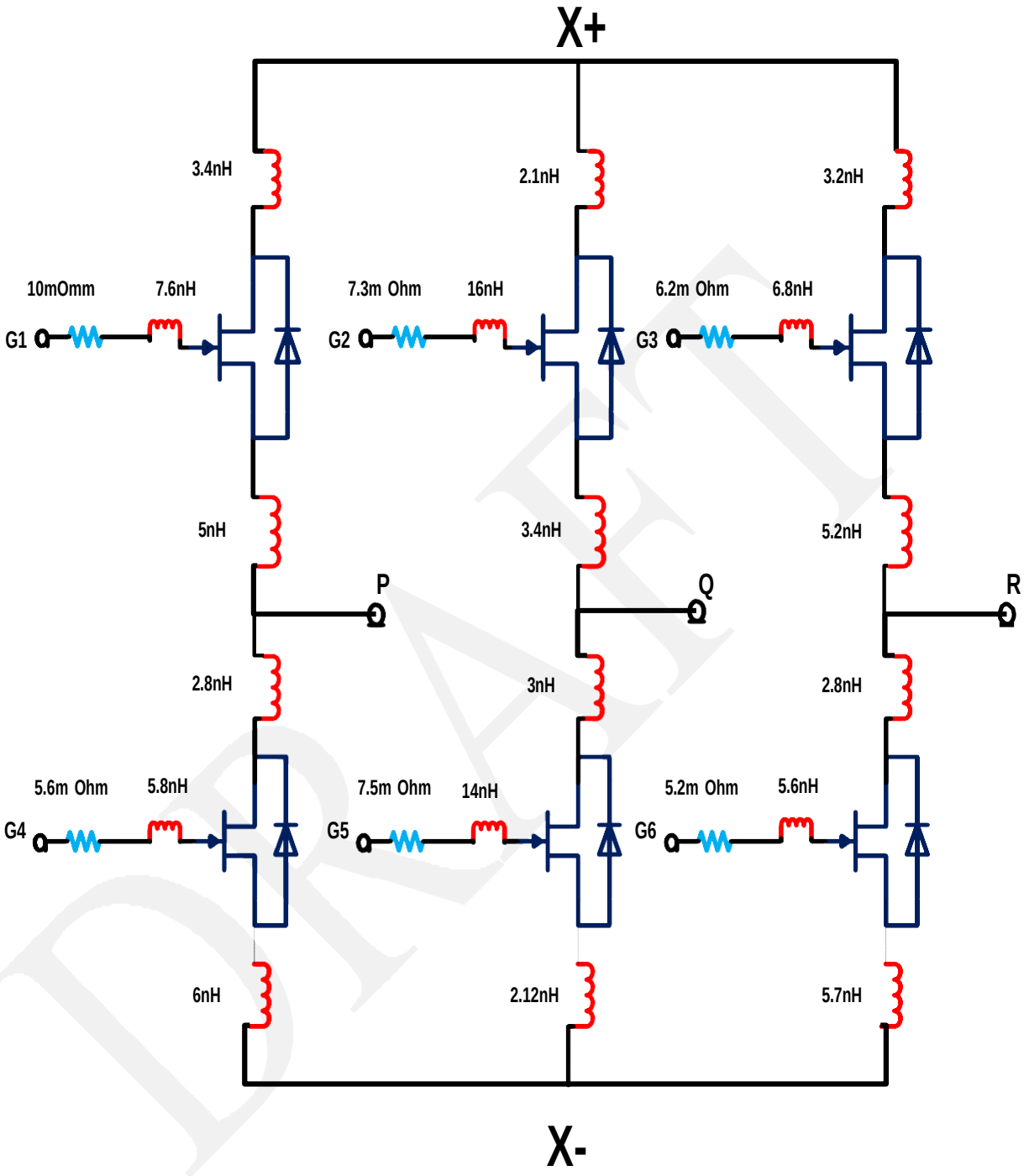

Figure 2.5 Inverter schematic with parasitic values from the Q3D extractor

DRAFT

Rectifier Module:

A similar parasitc extraction technique is performed for the rectifier module. Tehe Rectifier schematic is shown in Figure 2.6 for the parasitic analysis. It has 12 unidirectional switches consists of 20A SiC JFETs and 20A parallel SiC Shottky diodes . The main terminals are two DC terminals X+ and X- and three I/O phase terminals S, T, and U; apart from that there are twelve gate terminals for the rectifier module which are connected to a gate driver board with the help of gate pins. By using accurate dimensions of all the components and positioning them based on the module requirement a layout for the rectifier module is proposed. Figure 2.7 shows the layout for the rectifier module showing the power devices and terminal locations..

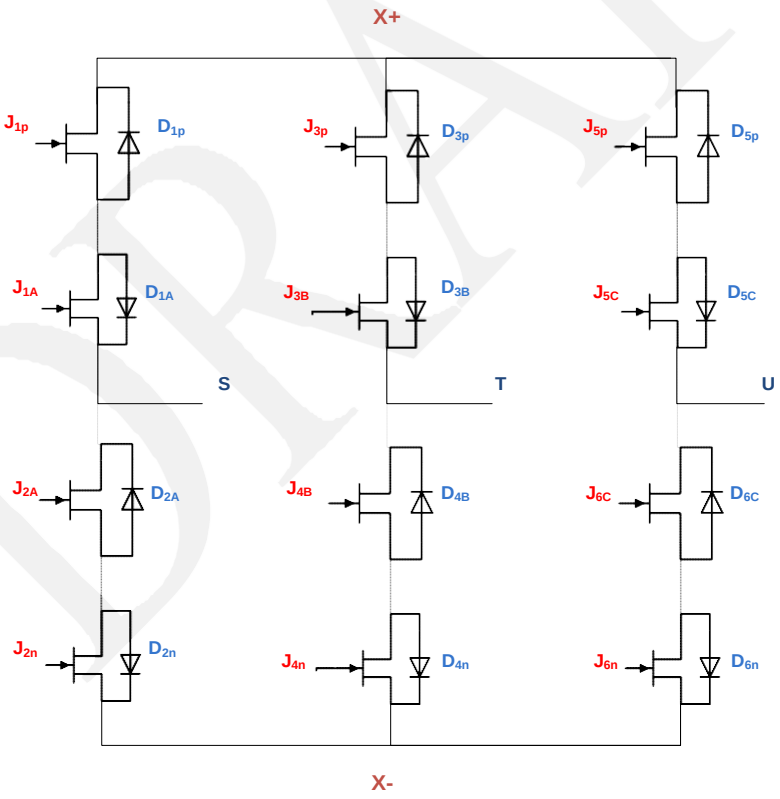

Figure 2.6 Rectifier Schematic

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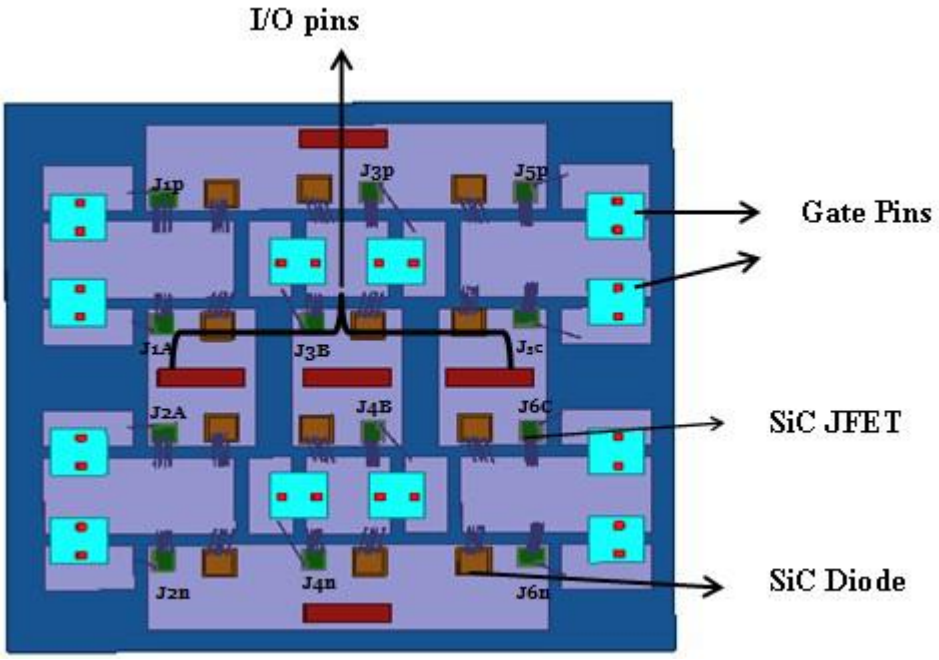


Figure 2.7 Inverter module Q3D layout.

To understand the parasitic inductance, a paticular switching combination is considered in Figure 2.8a. The rectifier switching operation in this combination starts from the current path at the SiC JFET R_{1A} through the diode D_{1p} and through the load as shown in the layout of Figure 2.8b . The current then returns through the lower JFET J_{6n} and, the diode D_{1c} to the node U. The current commutates between the JFETs J_{5n} and J_{3n} in response to the input PWM control signals,

thereby switching the dc-link voltage between $v_{\diamond\diamond}$ and$v_{\diamond\diamond}$; and the remaining switches are

open
in this combination. The parasitic for this combination comes from the bond wires between the sources of the devices ($J_{1A,}$ $J_{5n,}$ J_{6n}) and the diodes (D_{1p}, D_{5b}, D_{6c}) to the DBC substrate traces, between the conducting traces and the connectors, and the bond wires between the gate pads of the JFETs and the gate connectors.

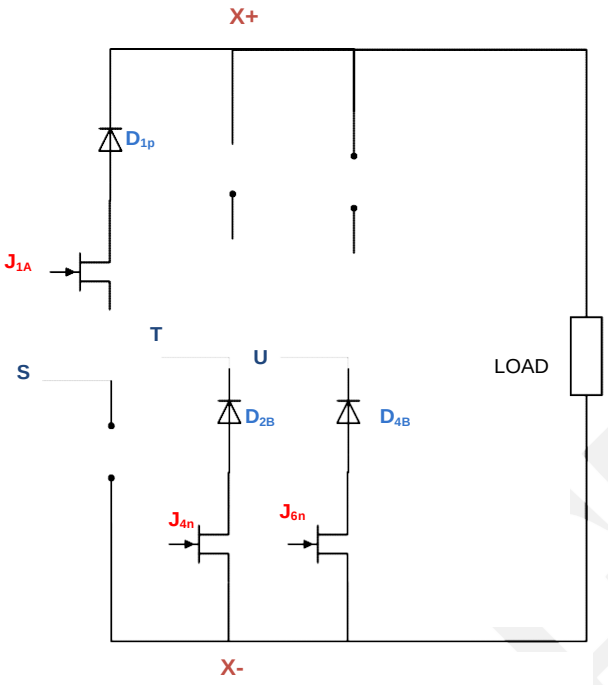


Figure 2.8a Selected switching combination-Rectifier

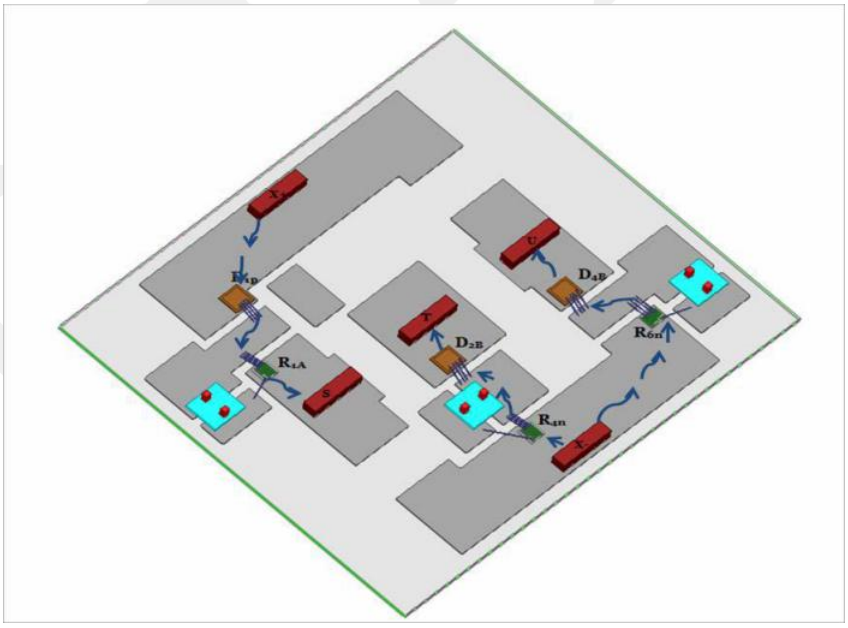


Figure 2. 8b Parasitic induction paths in rectifier for a selected switching combination [7]

Several layouts were analyzed before finalizing the final rectifier module layout. The parasitic circuit elements for this particular layout are summarized in Table 2.2. These parasitic are extracted using the ANSYS Q3D extractor. Simulations are performed at 30KHz frequency for all the switching combinations, where the gate inductance extraction is carried out at 50MHz. Figure 2.9 shows the extracted parasitic circuit elements in schematic form.

Table 2.2 Rectifier Module Parasitc [7].

Parameter	**R_{1A}**	**R_{3B}**	**R_{5C}**	**R_{2n}**	**R_{4n}**	**R_{6n}**
DC bus to drain stray inductance (nH)	6.5	2.3	6.5	6.5	2.3	6.5
Common-Source inductance (nH)	9.6	10.8	9.6	9.6	10.8	9.6
Drain to input connectors stray inductance (nH)	4.5	3.7	4.5	4.5	3.7	4.5
Gate-loop inductance (nH) @ 50 MHz	5.4	5.2	5.4	5.4	5.2	5.4
Parasitic resistance (mΩ)	1.4	0.8	1.4	1.4	0.8	1.4
Conduction loss (mW)	0.4	0.23	0.4	0.4	0.23	0.4

The IMC parasitic resistances are also extracted using Q3D extractor for a current of 17 A, the conduction losses are around 0.5 mW, for practical purposes these values are negligible compared to the device losses. However for a current capability of 450A these values may be in several hundred watts when the devices are connected in parallel [15].

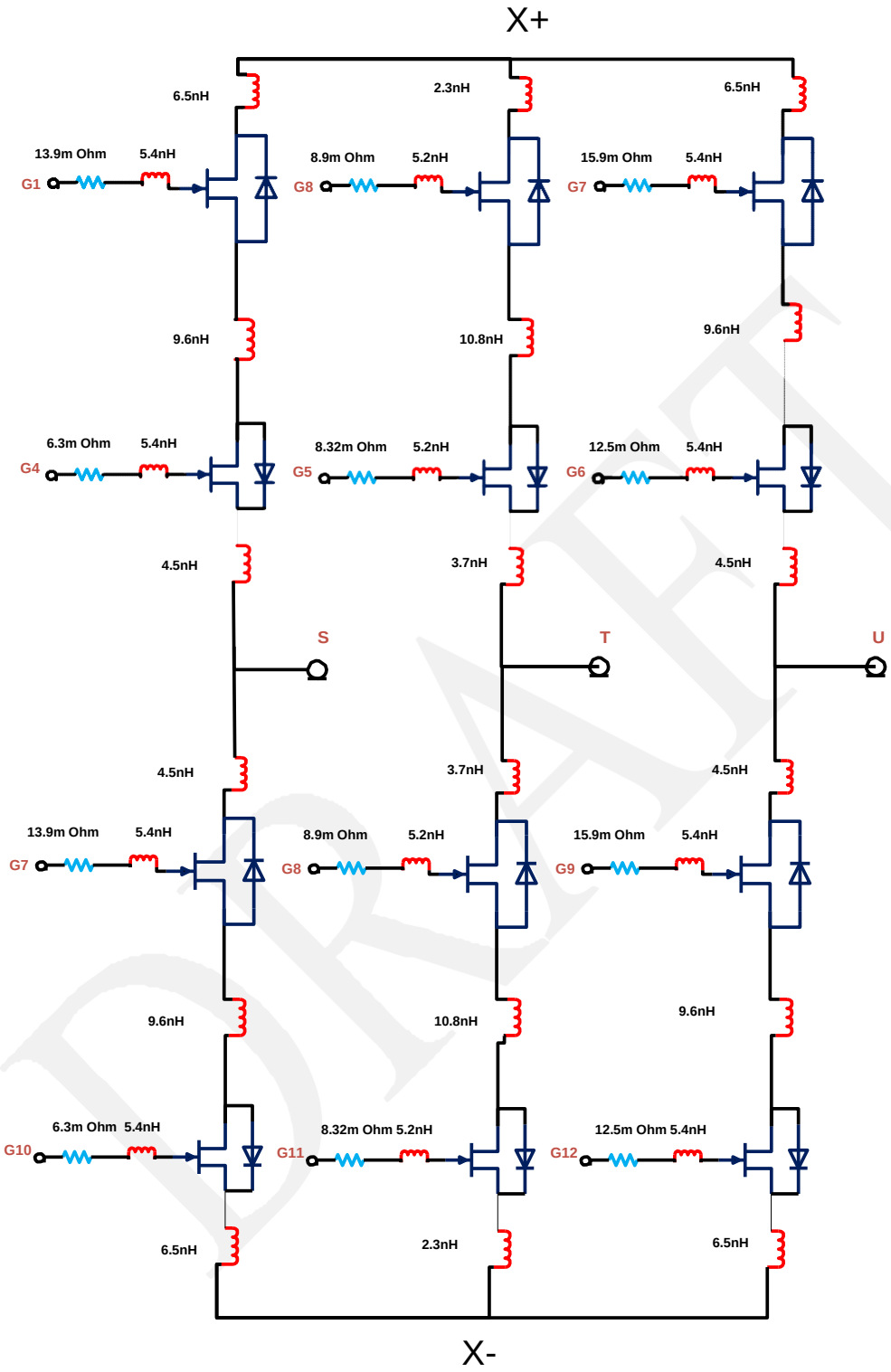


Figure 2.9. Rectifier schematic with parasitic values from Q3D extractor

DRAFT

2.5 Thermal Analysis

Thermal analysis helps to understand the performance of the modules in operating conditions. In a power electronic module one of the important parameters is operating temperature. In general heat transfer mechanism takes place in three various ways conduction, convection and radiation. Conduction is responsible for heat transfer within the body, convection is responsible for heat from outside source to the body and radiation occurs at very high temperature. In the power module heat passes through the solder layer through the DBC substrate and finally heat is removed from the copper base plate. Thermal issues are quiet common in power electronic modules. The use of proper heat sinks and cooling fans should solve some of the thermal problems. Apart from that there should be sufficient airflow within the packaged module[7].

The rate of heat transfer by conduction is defined by $Q_{conduction}$is given by [3]

$$Q_{conduction} = k.A.\frac{\Delta T}{l} \text{ Kelvin .(W/mK)} \quad \text{.....[2.1]}$$

Where,

A - Cross-sectional area of the module substrate.

ΔT - Temperature difference.

K - Thermal conductivity.

l - Separation distance.

The convection is the heat exchange between the surface and its surroundings. The rate of heat transfer by convection is given by $Q_{convection}$

$$Q_{convection} = h.A.\ \Delta T \quad W/m^2K \quad \text{.....[2.2]}$$

Where,

h - Convection coefficient.

ΔT - Temperature difference between surface and ambient temperature.

A - Surface Area.

The value of the convection coefficient (h) for natural convection is in the range 5-25 ($W/m^{2}\cdot K$) and for forced air convection the value of h is 20-300 ($W/m^{2}\cdot K$).

Table 2.3 Material Properties for Thermal Simulations [7].

Material Type	Thermal Conductivity (W/m-K)	Thickness (mm)
SiC devices	358	0.37
Solder paste	622	0.11
DBC copper	405	0.62
Ceramic (Al_2O_3)	36	0.62
Base plate	405	6.4

Thermal simulations are performed using Dassault system SolidWorks 3D CAD tool. The power applied to the JFETs is 18W with 50% duty cycle [7]. The maximum operating temperature of the SiC devices are 150°C which becomes the modules operating temperature.In the thermal analysis each material is designed layer by layer and materials are assigned with their thermal conductivity values as shown in Table 2.3.As with a power of 18W the module and a heat sink of100mm x100mm is considered for heat conduction. A free air convection of convection coefficient of10 ($W/m^{2}.K$) is considered for simulations. Figure 2.10 shows an

solidworksimage of the thermal analysis. The image shows the temperature of the module reaches 56.45°C which is well below the maximum operating temperature [7].

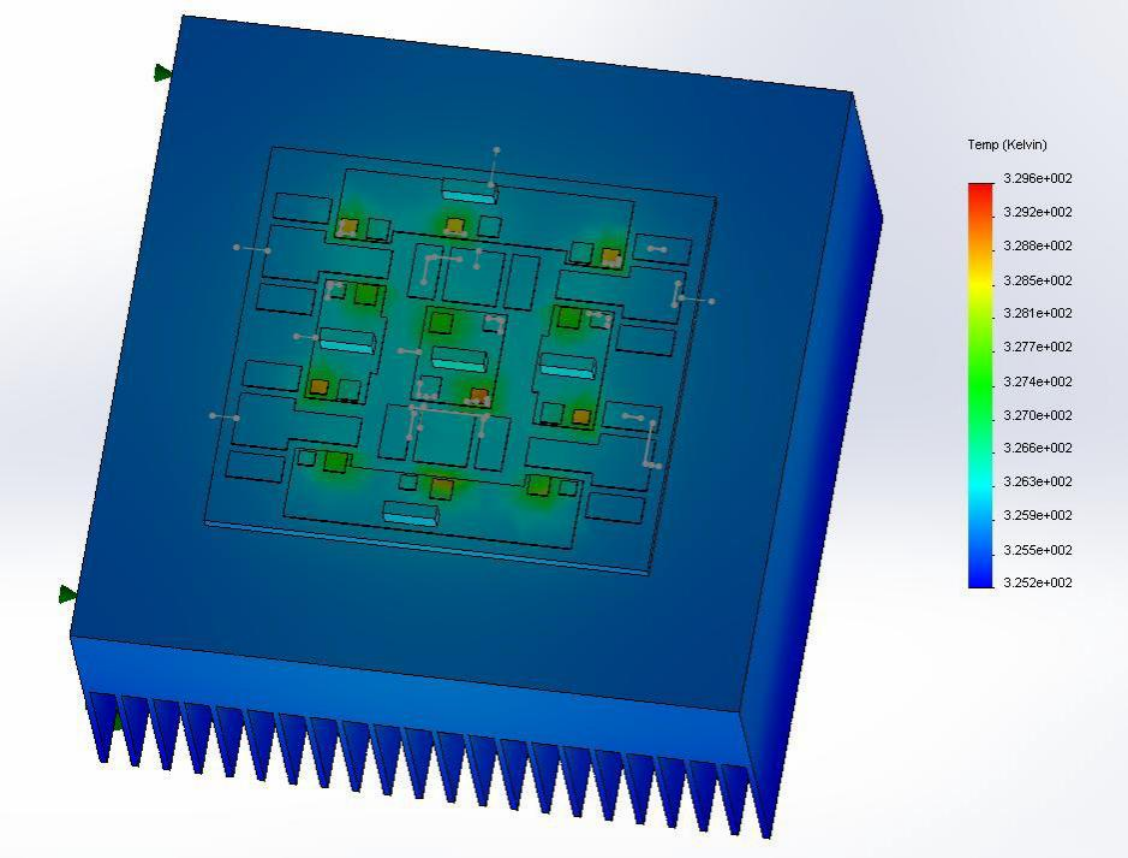


Figure 2.10.SolidWorksThemal Simulation [7].

III. Materials used.

3.1 Introduction

Choosing the right materials for the power module and assembly is very important. These materials can be the power substrate, base plate, bonding materials, bond wires, terminals and encapsulation. The material properties vary differently due to their thermal and electric properties.

3.2 Substrate

Direct Bonded Copper (DBC) is used as the substrate for the module processing [16]. In general there are three layers that make a DBC substrate. The top copper layer is used for the interconnection paths after it is etched; in the middle is the ceramic substrate which can be aluminum nitride (AlN) or alumina (Al_2O_3) material. The bottom layer is the copper layer for thermal conduction path [17].

Major factors that critical in considering the DBC substrate are the thermal conductivity and coefficient of linear expansion (CTE). These properties for a DBC substrate are given in below Table 3.1.

Table 3.1 DBC Properties [18]

Properties/Material	Alumina (Al_2O_3)	Aluminum Nitride (AlN)
Thermal Conductivity W/mK @ 20°C	24	180
Coefficient of Linear Expansion ppm/K @ 20°C - 300°C	6.8	4.7

For the IMC application the alumina (Al_2O_3) substrate was chosen as it is more economical. The layout geometry constraints of the DBC substrate are summarized Table 3.2.

Table 3.2 DBC Dimensions [18]

Dimension/Material	Alumina(Al2O3)
Thickness of Copper/Ceramic	0.3mm/0.63mm
Size	5.50‖ x 7.5‖

3.3 Bonding Material:

There are two different bonding materials used in the entire process of fabrication. The basic objective of these bonding materials is to have a better thermal, mechanical and electric conduction between the bonded components. It plays a vital role in the power module performance as they act as a physical connection between the base plate, DBC, power devices and terminal connectors.

In both of the modules solder alloy is used as the bonding material for the die attachment. Generally a solder alloy is a mixture of two or more elements which has a melting point below that of the individual elements. During the process the solder alloy is placed between the two components and processed in a SST or Sikama furnace.

A tin-silver-copper (SAC 405) solder perform and a lead-tin (Pb-Sn) solder paste are used for the attachment. SAC 405 is used for the base plate and die attachment to the DBC substrate. The Pb-Sn paste is used to attach both the gate and power connectors. Initially the base plate and die attachment is first performed and later the connectors are attached. It is important to

understand the melting points, electrical resistivity and thermal conductivity of these solders which are listed in Table 3.3.

Table 3.3 Solder Properties [19]

Material	Melting point(°C) solidus / liquidus	Electrical Resistivity, μΩ·m	Thermal Conductivity, W/m·K
SAC 405(Sn95.5Ag4.0Cu0.5)	217/220	0.132	62
Sn63Pb37	183	0.145	50

3.4 Devices:

As mentioned earlier the devices that are used for the module are the normally-off SiC JFETs and SiCShottky Diodes as shown in Figure 3.1. The devices are rated at 17A/1200V and 20A/1200V, respectively. The electrical characteristics and the dimensions are documented in the data sheets [20][21]. Table 3.4 summarizes the device parameters.

A **B**

Figure. 3.1.SiCJFET(A) and Diode(B)[20], [21].

Table 3.4 Product Summary

JFET	BV_{DS}=1200V	$R_{DS}(ON)_{max}$ =100 Ohm	2.43mm X 2.16mm
Diode	V_{RRM}= 1200 V	$I_{F(AVG)}$ = 20 A	3.08mm X 3.08mm

3.5 Encapsulation Material:

A GE TSE3051 [22] silicone gel is used as the encapsulation material. This is a low viscosity silicone gel used to provide protection to the modules from environmental factors such as dirt, humidity and vibration [22]. A proper curing process is important for effective encapsulation. The material properties of the silicone gel are listed in Table 3.5.

Table 3.5 Encapsulation Material [22].

Properties	Measurement
Viscosity (23°C) Pa•s	0.7
Density(23°C) g/cm³	0.97
Thermal Conductivity W /m • K	0.17
Dielectric Strength kV/mm	18
Curing time 125°C	2hrs

3.6 Other Materials

Other materials that are used in the module design are base plate, housing and raphite fixture. First, the copper base plate is used to act as a thermal spreader in between the DBC substrate and the heat sink. A 0.125‖ thick copper base plate is machined for both the modules based on the

module dimensions. Polytetrafluoroethylene (PTFE) housing is fastened on top of the substrate using four screws. This housing acts as a sidewall protection for the module. They are machined to the required dimensions as shown in Figure 3.2.

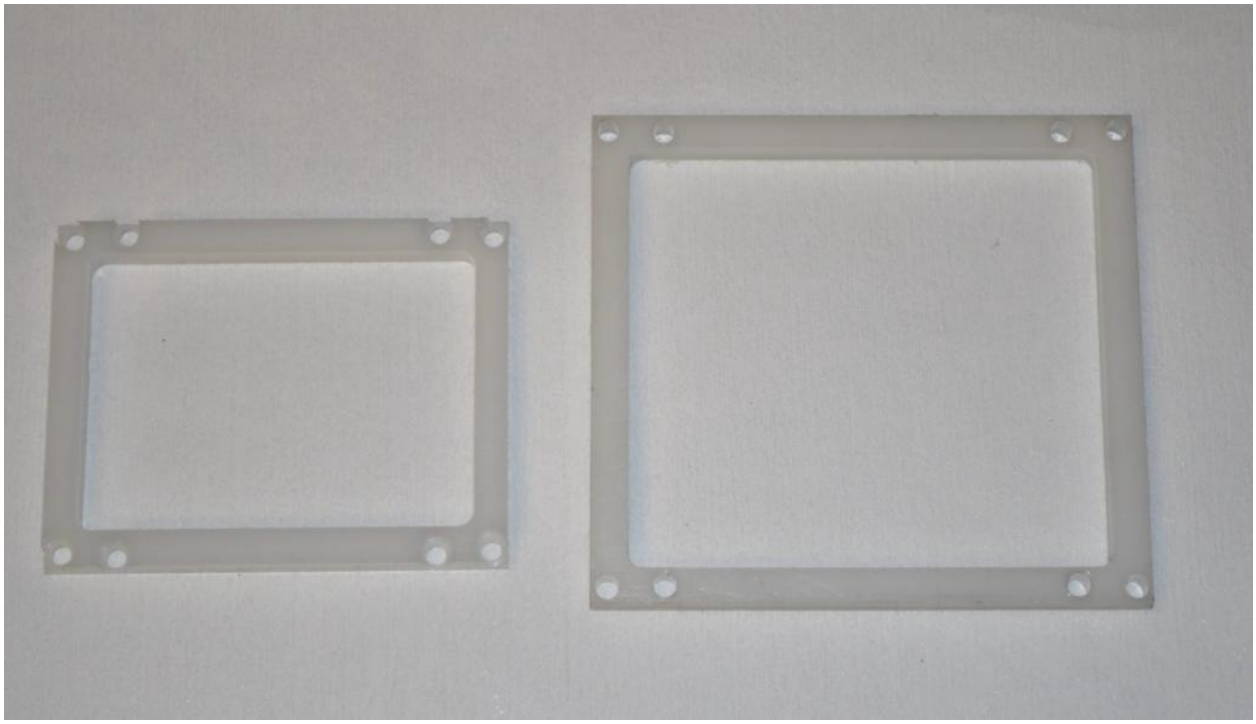


Figure 3.2 PTFE Housing for Inverter and Rectifier[23].

Finally, a graphite fixture is made for both the modules. This fixture helps to position and hold all devices as well as the connectors during the attachment process. Both the fixtures are machined based on the designs from AutoCAD presented in Appendix 2. The graphite fixtures for both the modules are shown in Figure 3.3. The openings in the graphite fixtures are used to place the dices and terminals.

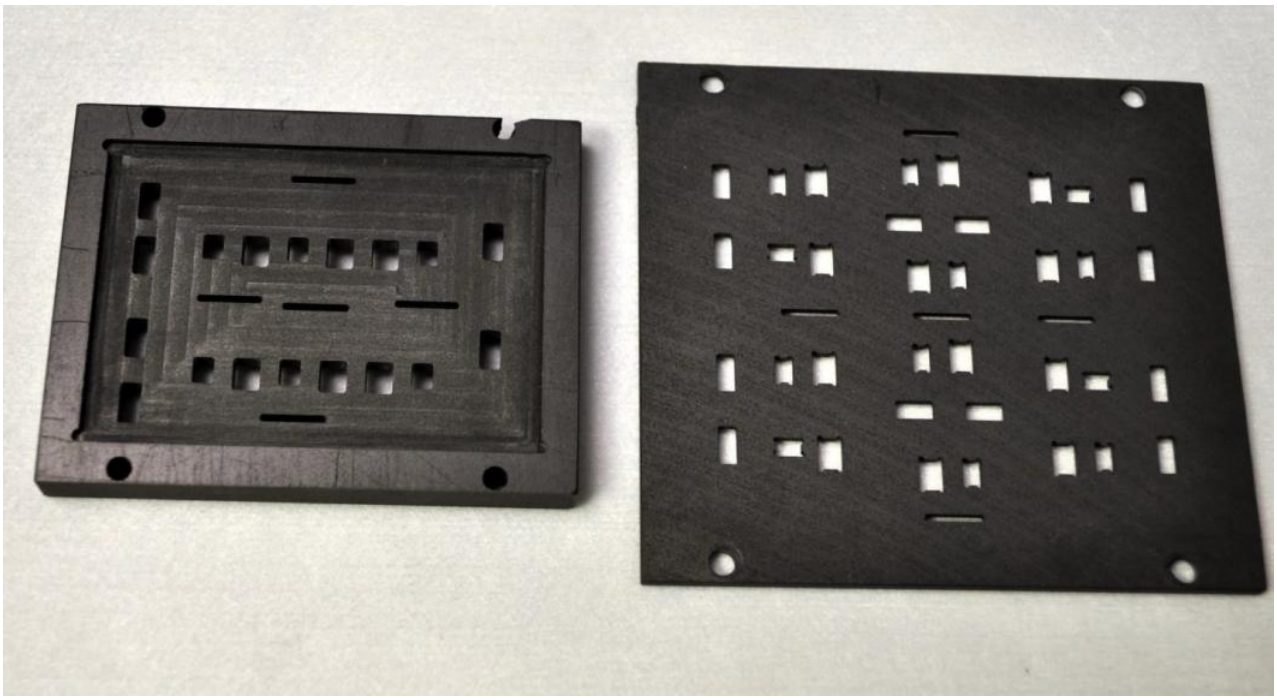


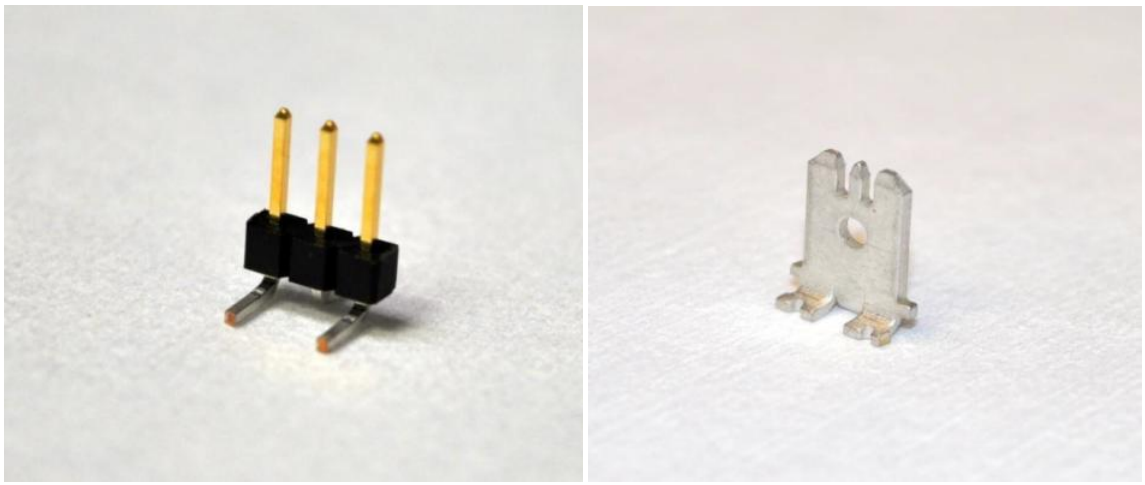
Figure 3.3 Graphite Fixtures for Inverter and Rectifier[23].

3.7 Connector Pins.

The IMC has 18 gate connectors that are connected to a gate driver board. These connectors are the Sullin's male polyester copper alloy headers (SSC02SYAN) [24]. There are 10 aluminum power connectors for both the modules as the input/output and dc connectors. Each pin is attached carefully to the substrate using the lead-tin (Pb-Sn) solder paste. The images of these pins are shown in Figure 3.4.

Table 3.6 Connector pin Dimensions

Gate connector	5.84mm X 5.59mm X 2mm
Power Connector	7.2mm X 5mm X 3mm



(a) (b)

Figure 3.4 (a) Gate connector (b) Power Connector[23].

IV. Fabrication Procedures

4.1 Introduction

In this Chapter we discuss the fabrication procedures for both the IMC modules. The major steps performed are substrate preparation, module assembly, and other component preparation.

Fabrication begins with the substrate preparation to obtain the desired pattern and size. Later the process of building the modules begins. In this process different attachment techniques are used to attach the base plate, power devices and connectors onto the DBC substrate. To support the module base plates, housing and the graphite fixture are machined based on the design requirements. Finally an encapsulation material is used to protect the module from handling and harsh environment. The complete process steps for all the procedures and the travelers for the processing equipment are presented in Appendices.

4.2 Substrate Preparation:

a. Substrate Cleaning:

Initially it is very important to clean the new DBC substrate which helps in removing the dirt and oxidized and organic materials on the DBC surface. The cleaning procedures starts with an ultrasonic cleaning and a 10% HCl clean. This cleaning helps to prepare the substrate for better plating.

In the ultrasonic procedure, the alumina DBC is cleaned with acetone solution. First, a 500mL acetone solution is poured into a clean steel tank shown in Figure 4.1. Later the tank is filled with DI water in the ultrasonic bath. The temperature of the bath is set to 40°C and the

sonics value is set to 60. This procedure is performed for 5 minutes by setting the display time is set to 5 minutes. Once the temperature of the bath reaches this level, the DBC substrate is placed in the acetone solution through in the steel tank. The ultrasonic process is started and the DBC substrate is flipped half way thru the process so that ultrasonic can be performed on both sides. Once the process stops, the DBC substrate is cleaned with DI water.

Figure 4.1 Ultrasonic Bath [23].

The second part of the cleaning is performed using a 10% HCl acid solution. Here the DBC substrate from the ultrasonic process is dipped in the 10% HCl solution for 3 minutes. During the process the DBC should not be exposed in air for a long time to protect it from oxidation. The DBC substrate is then cleaned in water and immediately transferred in water for Ni plating. Improper cleaning methods result in bad a Ni plating.

b. Nickel Plating:

The basic advantage of performing the nickel (Ni) plating is to prevent the copper substrate from oxidation. It is very important to start the Ni plating bath before the process of substrate cleaning in order to perform the plating immediately after cleaning. The plating bath shown in Figure 4.2 should be started ahead of cleaning such that it is preheated to 38°C by the time the DBC substrate cleaning is done.

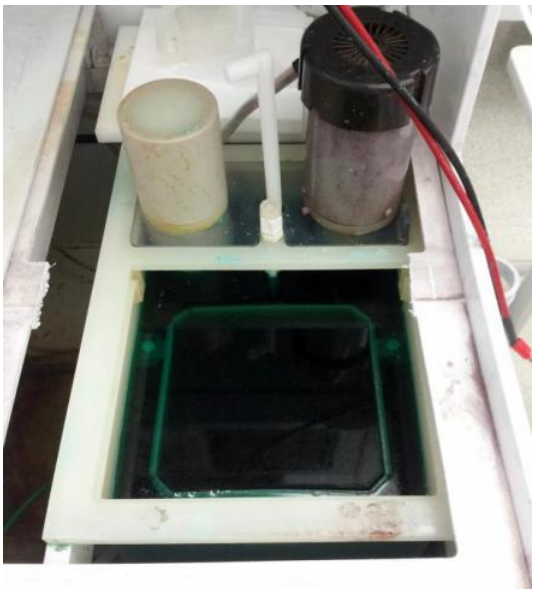


Figure 4.2.Ni Plating Bath[23].

The DBC after the 10% HCl cleaning is placed in a 150mm cassette and submerged into the Ni plating bath. Care must be taken that DBC should be completely immersed into the Ni plating solution. The cathode of the power supply is connected to the DBC and the anode is connected to the Ni plating source. By controlling the current density and plating time, required nickel thickness can be plated on the DBC substrate. Table 4.1 gives the values of the voltage

and current used to obtain the required thickness for this thesis project. It is also found that a current value of 1A gives the best nickel plating results.

Table 4.1. Ni Plating Process

Area	Density	Current	Rate	Thickness	Units	Time
532.257cm^2	0.004A/cm^2	2.13A	0.025mcm/min	3	(um)	120min

Once the nickel plating is done the DBC is rinsed in water and dried. Figure 4.3 shows an image of DBC substrate after good Ni plating.

Figure 4.3 Ni Plated DBC[23].

c. Dry Film Patterning

A photo mask was generated based on the optimized design layout. The mask which is generated in AutoCAD DXF file is shown in the Appendices. This mask is used as a pattern layout on the Ni plated DBC substrate.

Dry film patterning is a dry process where a chemical photo resist is applied onto a DBC substrate in a dark room. To start with, the DBC is initially preheated on one side and then passed through the photo resist laminator. Later the photo mask is attached to one side of the laminated DBC and exposed under an UV light for 2 minutes. The DBC is immersed in a developer solution until the photo resist is completely developed. The photo resist is stripped after the process of etching pattern, the DBC substrate is brought back to the dark room to strip off the resist. A wet etching is used for this purpose.

d. Etching:

Before etching, Chencut etcher is preheated to 35°F temperature. The DBC substrate after developing from the dry film process is placed in the etcher. The conveyor speed is set to 3.2mil/min to etch an 8mil copper. The etching solution that is used for the process is the ferric chloride etchant. Once the process is done, the DBC substrate is rinsed in water and is now ready for the photo resist strip figure 4.4 shows the Chemcut etcher used for the process.

Figure 4.4 ChemcutMachine [23].

e. Dicing:

A dicing saw is used to cut the etched DBC substrate into required parts. The process uses a 10mil diamond blade. The forward cut speed of the dicing saw is set to 40mil/rpm and the speed of rotation is 20,000rpm. Care should be taken while setting the height so that proper cutting is done. The dicing process steps are shown in the Appendices.

4.3. Module Assembly

It is important to clean the DBC substrate parts and the base plates properly before processing. To clean the parts we use a hybrid asher. It helps in proper attachment without defects. During the process the module parts are placed in the chamber and subjected to oxygen exposure for 5 minutes to remove any organic compounds on both sides. Later they are exposed in argon for 5 minutes to remove any oxide materials. Figure 4.5 shows the hybrid asher instrument used for the process.

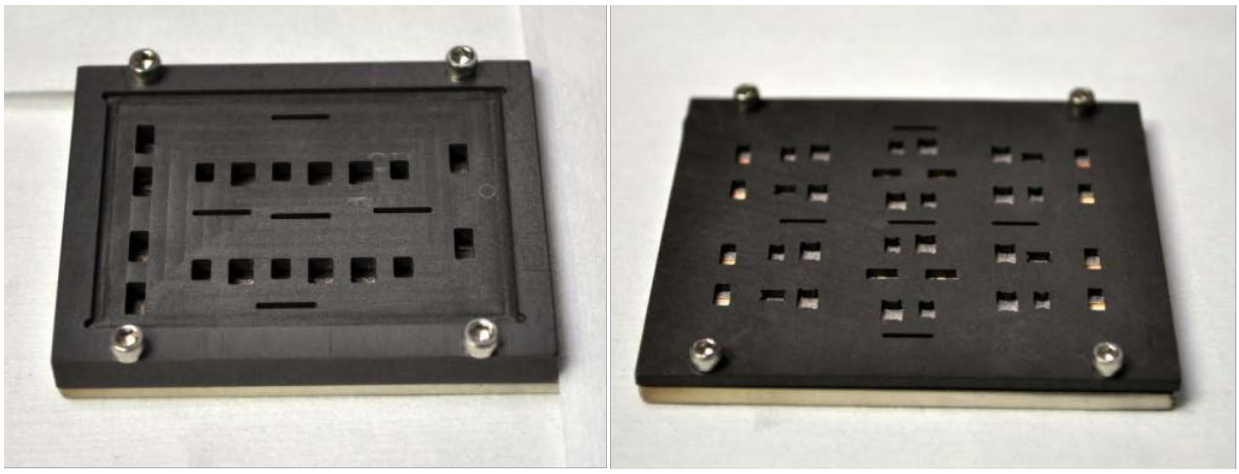
Figure 4.5 Hybrid Asher [23].

The module assembly process has two different steps. First, the base plate and the devices are attached in an SST vacuum reflow oven using the solder preforms. The second step includes connector attachment with the lead-tin solder paste in a Sikama furnace shown in Figure 4.6.

Figure 4.6 Sikama Hotplate[23].

a. SST Attachment:

The devices and the base plate are attached to the DBC substrates in this process. Here all the attachments are performed in one step. Initially the SAC 405 preform is cut into required size for the devices and the base plate for attachment. Later a layer of this perform is placed between the base plate and the substrate. The graphite fixture which is designed with pockets is placed on the substrate. This assembly is fixed tightly with four ¼ inch screws. The solder performs for the devices are carefully placed in the pockets with the help of a vacuum wand. In the similar way the devices are positioned. The entire assembly shown in Figure 4.7 is now placed in the SST vacuum furnace for attachment and to prevent oxidation.



(a) (b)

Figure 4.7 SST Process Inverter and Rectifier [23].

The SST profile is shown in Figure 4.8.The reflow procedure is presented in the Appendices. The vacuum level is set at 10 psig. Nitrogen is used to create air pressure and fill the solder voids. Heat ramps up to 180°C in 5 minutes, for the next 2 minutes the heat ramps to 265°C

which is about 50°C higher than solder perform melting point. The temperature graphs are shown in Figures 4.8 show the reflow temperature and pressure to yield void free attachment.

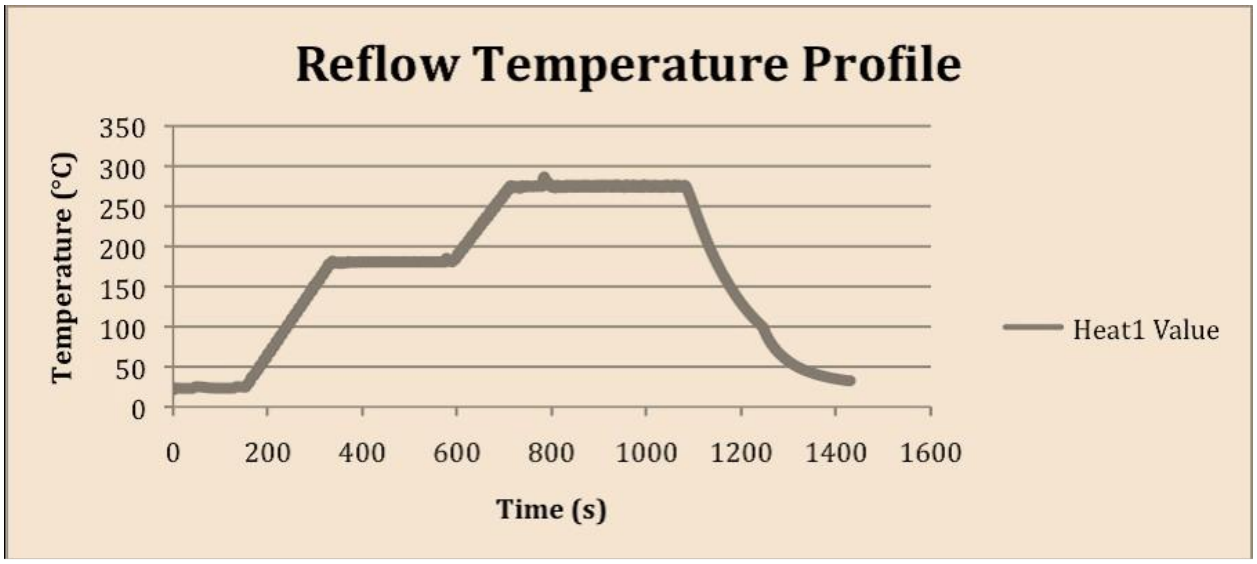


Figure 4.8 (a) Reflow temperature profile SST

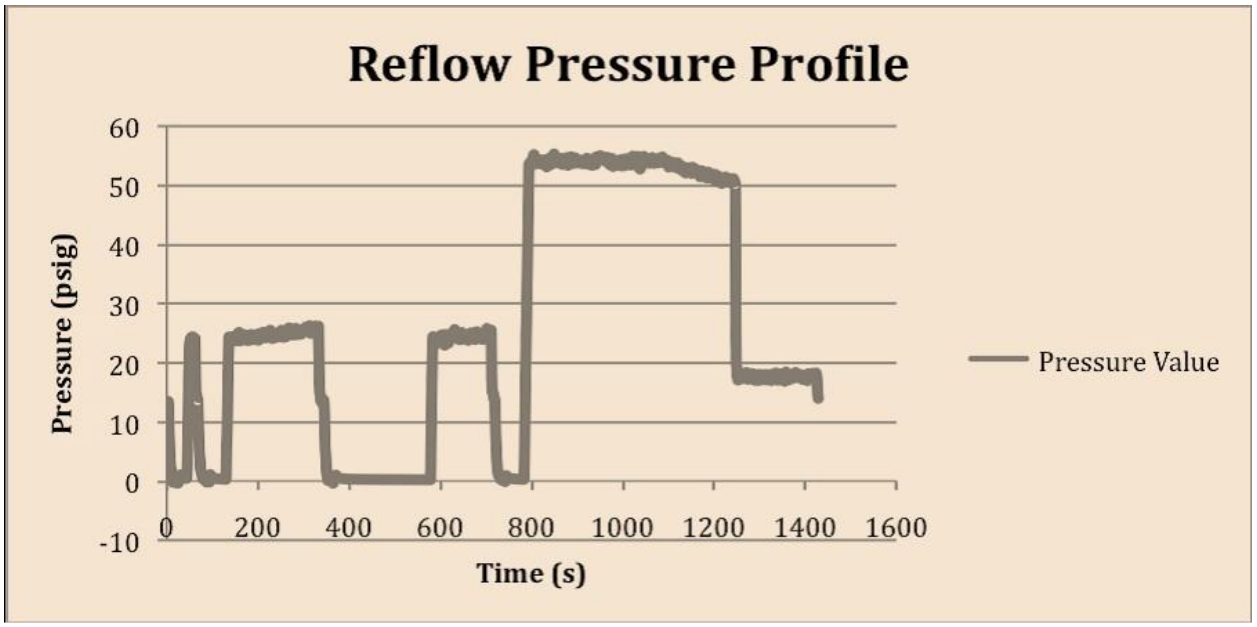


Figure 4.8(b) Reflow Pressure Profile SST.

Figure 4.9 shows the inverter module after the die attachment process. As can be seen, the power devices are attached to their intended locations.

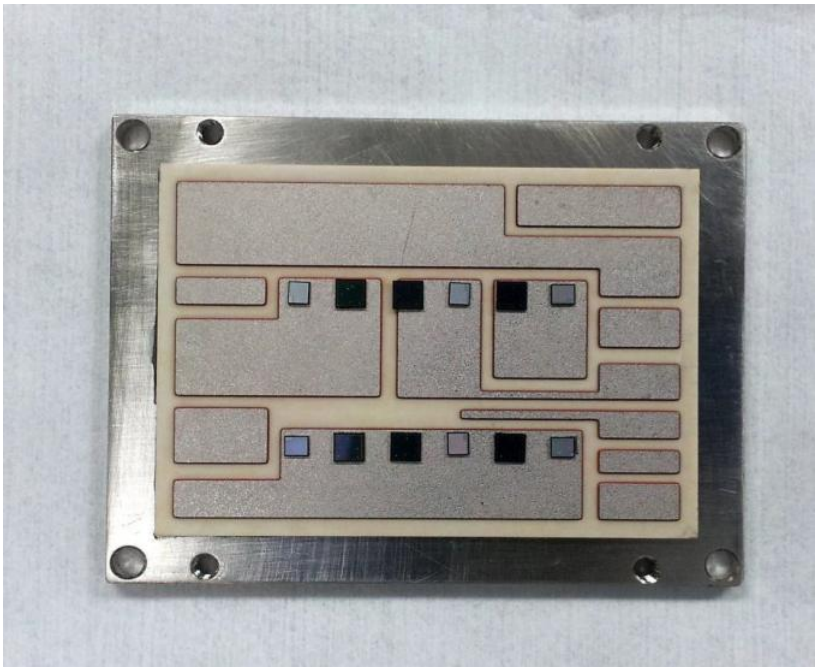


Figure 4.9 Inverter Module after Die Attachment [23].

b. Wire Bonding:

The immediate process after die attachment is the wire bonding. To connect the top-side electrodes of the die, a 5-mil aluminum bond wire is used to connect the SiC devices to the copper interconnection metallization on the DBC substrate. Sources of the JFETs are connected to the copper traces using four bond wires and the anodes of the diodes are connected to the copper traces with five bond wires [7]. A wire bond machine is used for the bonding. Figure 4.10 shows the inverter module after wire bonding.

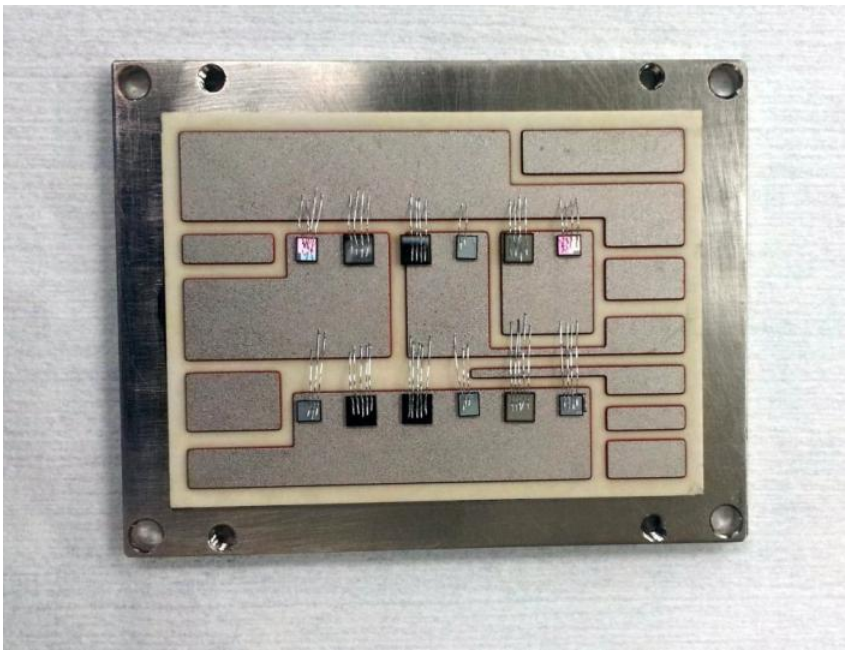


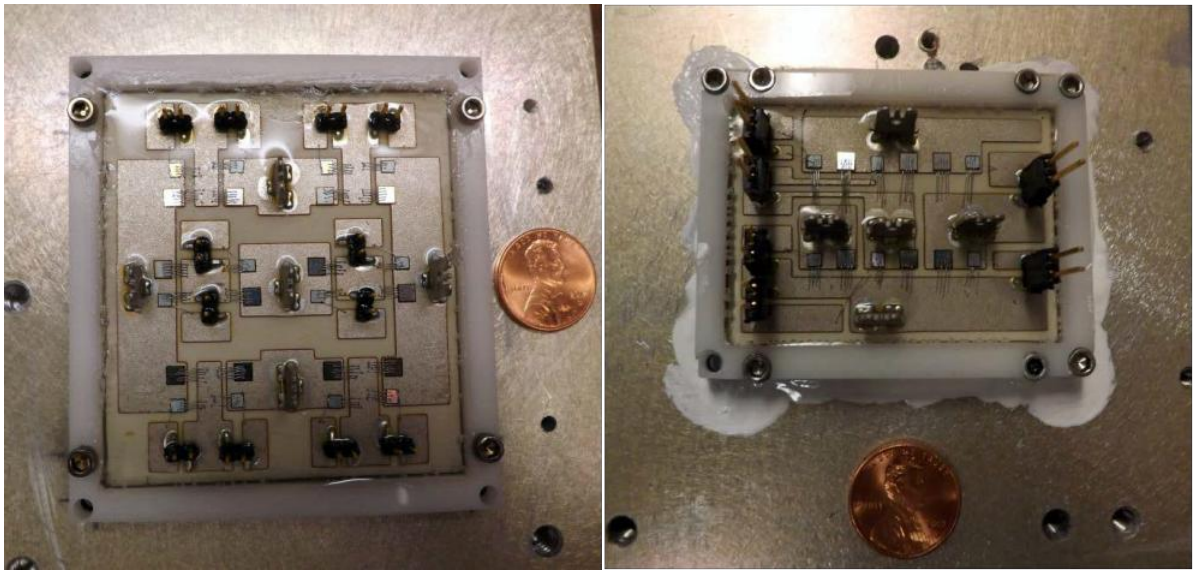
Figure 4.10 Inverter Module after wire bonding[23].

c. Connector Attachment:

The power and gate connectors are attached onto the DBC substrates in a Sikama chain oven using gate connector pins (Sullin's male polyester copper alloy headers) and aluminum power connectors. Initially the connector parts are cleaned in isopropyl alcohol (IPA) solution. The module after wire bonding is carefully brought under a microscope. The positions of the connectors are marked using graphite fixture. Next, the connectors are attached using the lead-tin (Pb-Sn) solder paste. The entire module is run through the Sikama chain furnace. The temperature is ramped to 175^{o}C for 2 minutes. This is followed by a reflow temperature of 225 ^{o}C. The process steps to operate the Sikama chain furnace are presented in the Appendices.

d. Housing and Encapsulation:

The PTFE sidewall is fixed to the base plate around the module using four ¼ inch steel screws. The design and dimensions for the sidewall are described in the Appendices. To protect the module from bad handling and other environmental issues the module is filled with an encapsulation material (GE TSE3051). In this process the encapsulation material is slowly dispensed from one corner of the module until it fills the entire module. This silicone gel requires an elevated temperature to cure. Curing process is done in two main steps. Initially the temperature is raised slowly until it reaches 125°C. Later the modules are cured at the same temperature for 2 hours. The modules did not have any significant damages after all the fabrication process. The final assembled rectifier and inverter modules are presented in Figure 4.11.



A. Rectifier Module **B. Inverter Module**

Figure 4.11 Final Assembled Modules[23].

V. Testing Analysis & Conclusions

5.1 Introduction

In this Chapter, the results related to TDR testing which verify the parasitic inductances of the modules are presented. Later, to demonstrate the functionality of the IMC prototype the IMC system is tested with the devices operating at a switching frequency of 30KHz and connected to a RL load. The electrical testing of the IMC system was performed by my colleagues in the Arkansas Renewable Energy System Laboratory [25].

5.2 TDR measurements:

It is important to have experimental measurements of the parasitic inductances of the power module designs. Accurate measurements of these values play a major role in predicting these parasitics [26].

The extraction of parasitic that is generated by high speed switching can cause electromagnetic issues and other losses. The simulation of parasitic circuit elements using Q3D extractor is purely a mathematical analysis that helps in the design phase [28]. Apart from this we need physical measurements to verify the designs..

To measure the parasitic inductances of the modules, a time domain reflectrometry (TDR) is used. TDR has an open circuit transmission with the material/subject under test and contains a pulse generator connected to it [29]. The probe of the TDR is designed to have minimum impedance that yields a mismatch at the feed. TDR works on the principle of signal reflection. Figure 5.1 shows a TDR measurement instrument setup with the probe and an oscilloscope.

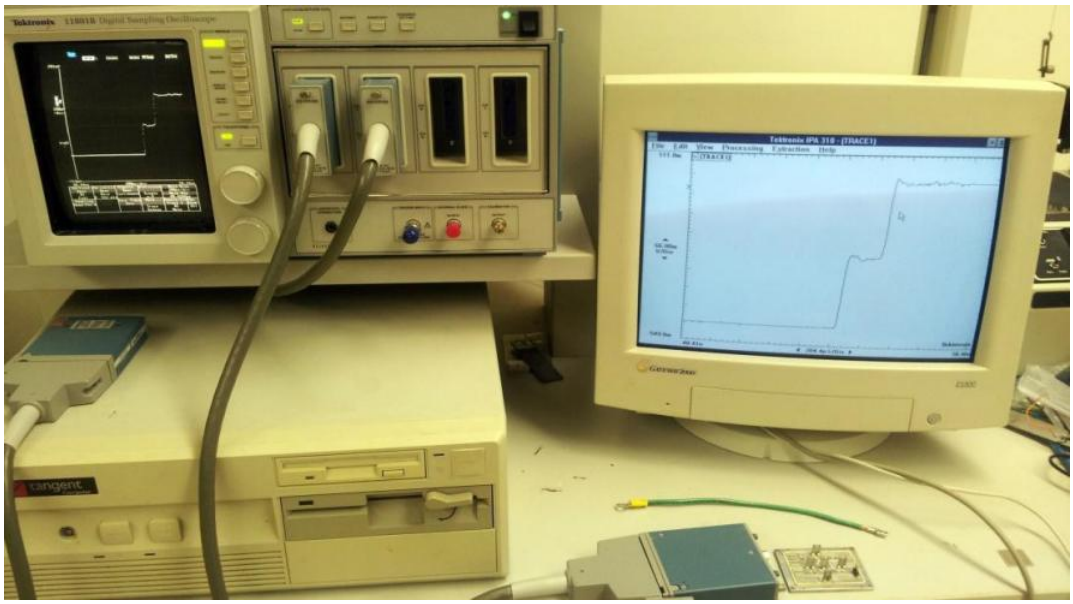


Figure 5.1 Time domain Reflectrometrysetup[23].

The DBC for the modules are properly analyzed for both the inverter and rectifier modules. TDR measurements are performed on the current switching paths. To compare the Q3D parameters to TDR measurements, the measurements are made exactly on the same path. Table 5.1 lists the inverter module parasitic inductances and Table 5.2 lists the inverter module parasitics extracted from TDR.

Table 5.1 TDR results for Rectifier Module.

Parameter	**R_{1A}**	**R_{3B}**	**R_{5C}**	**R_{2n}**	**R_{4n}**	**R_{6n}**
DC bus to drain stray inductance (nH)	6.25	—	6.25	6.25	—	6.25
Common-Source inductance (nH)	11.06	12.26	11.06	11.06	12.26	11.06
Drain to input connectors stray inductance (nH)	6.55	3.82	6.55	6.55	3.82	6.55
Gate-loop inductance (nH)	9.72	9.47	9.72	9.72	9.47	9.72

Table 5.2 TDR results for Inverter Module.

Parameter	I_{1A}	I_{3B}	I_{5C}	I_{2n}	I_{4n}	I_{6n}
DC bus to drain stray inductance (nH)	2.73	2.02	2.84	2.79	2.3	2.87
Drain to input connectors stray inductance (nH)	6.97	4.6	6.2	3.6	3.2	3.97
Gate-loop inductance (nH)	8.2	17.9	7.92	7.62	13.97	6.7

To summarize, the parasitic inductance measurements from TDR and the Q3D extracted values are almost similar. The largest parasitic inductances are found in the gate loop inductance as there is a single wire bond connected to gate of the device to the gate pin, whereas multiple wire bonds are used to connect the source of the devices to the DBC.

5.3 IMC Electrical Characterization Results:

The electrical characterization of IMC prototype is shown in Figure 5.2 with the control board, gate driver board, filters and the IMC modules included. Input filters of 70 µH and 20 µF are used in series with a 10 Ω resistor, and an output filter of 2 mH and 10 µF with a resistor of 1 kΩ is used. The total power density of the system is calculated to be 72 KVA/Liter [7], out of which the IMC power module volume is 7.9% of the total volume. The test results imply the use of power electronic packaging has reduced the volume of the IMC system and made it compact.

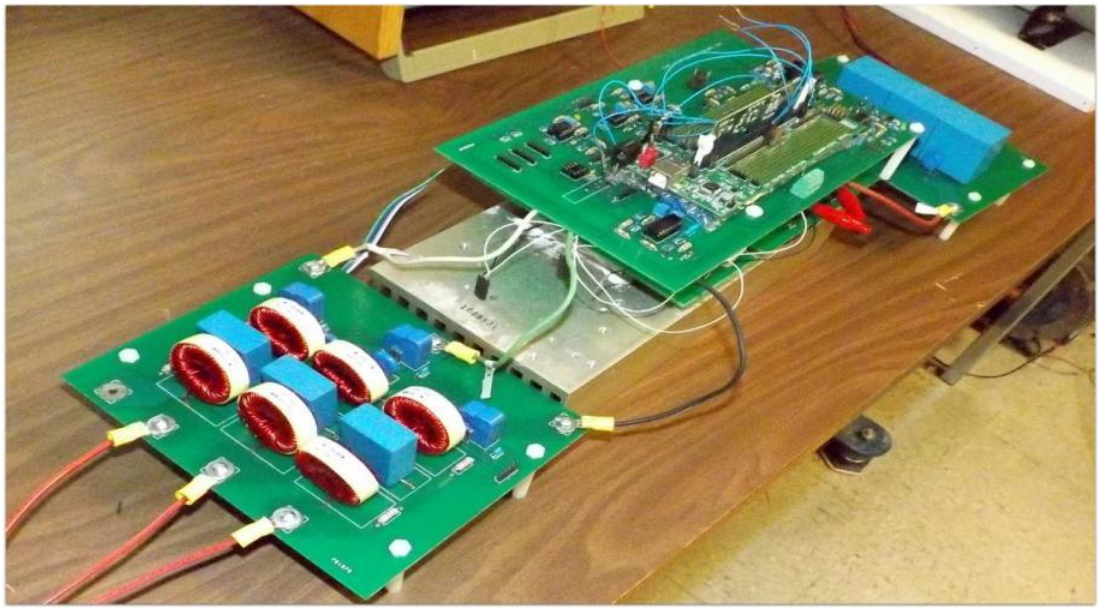


Figure 5.2 IMC Prototype experimental setup [27].

In the experimental setup the input is supplied with a three phase and a RL load of 1.5mH in series of a 15 Ω resistor is connected to each phase. The SiC JFETs used for both the modules switch at 15nS. The system is run at a power supply frequency of 60 Hz and a voltage of 200Vrms. The graph of the dc-link along with the input voltages and the filtered input currents are obtained and shown in the Figure 5.3. The virtual dc link voltage at the switching frequency is shown in first graph of Figure 5.3 at 200V/div, next a line-to-line input voltage and the input phase current are represented in the graph.

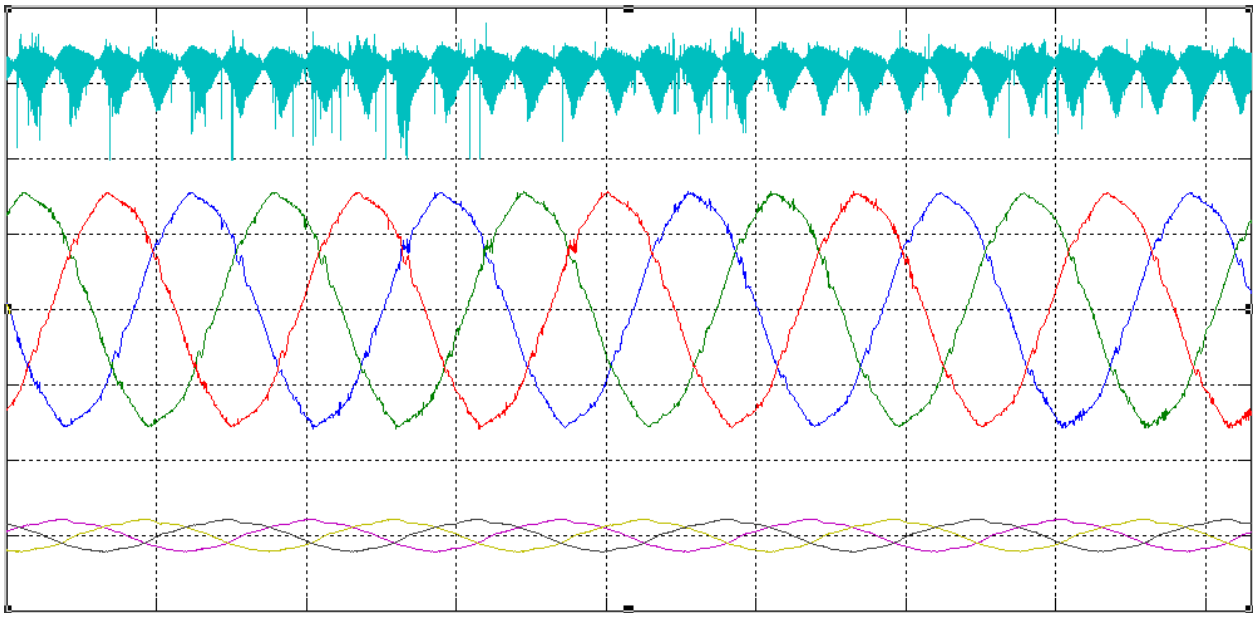


Figure 5.3 Virtual dc link voltage at (top), input line-to-line voltage at (middle), and input phase current at (bottom) [27].

VI. Conclusion and Future work

This thesis focuses on the design and packaging of the IMC power modules using SiC devices, along with analysis on parasitic inductances. Functional inverter and rectifier modules were successfully designed, fabricated and tested.

In Chapter 2, parasitic analysis based on different reduction methods was used to achieve optimum layouts. In Chapters 3 and 4, analysis for various materials and the process for the fabrication of both inverter and rectifier modules are presented. The main goal of the project is to decrease the volume for both the modules using 18 SiC JFETs and 18 SiC diodes and to reduce the parasitic circuit elements to achieve improved performance. Finally a brief version for the experimental results was presented in Chapter 5.

Future work is mainly concentrated on integration of both the inverter and rectifier modules into a single package. This will reduce the parasitic circuit elements in the dc-link connection between the modules. In our fabricated modules a large amount of parasitic circuit elements are present between the interconnection of the inverter and rectifier modules. An inter layer integration scheme will be employed to integrate the rectifier and the inverter modules.

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Appendices.

1. **Process Travellers:**

Ultrasonic Cleaning (DBC, Base plate)

Prechecks

- Chase
- Air
- Nitrogen
- Reset dump rinse
- Rinse tank

Powerups

- Connect power
- Turn on
- Retrieve Acetone and Waste bottles
- Fill water(4cm below operating level level)

Prechecks

- Set sonics (Highlight)
- clear display (Press C-clear)
- set display(Press up key to set for 5 mins)
- Install 6L stainless steel tank
- Pour Acetone in steel tank (500 ml)
- I/O (turn ultrasonic on)

- Rinse Beaker
- Install DBC
- Flip DBC halfway through.
- Fill 5L plastic beaker with 4L water
- Turn off ultrasonic
- Rinse DBC with DI water gun and place it in 5L beaker for storage and transfer
- Dump Acetone in waste bottle then place the bottles in chem cart
- Rinse the steel ultrasonic tank
- Open foset and dump water
- Clean Acetone waste Funnel

Cleaning (DBC, Base Plate)

- N2 + Air(chase)
- Retrive 6L tank
- Turn On bench
- Apron
- Flap out
- Face Sheild
- Gloves(Check for pin holes)
- HCl
- saftey Bucket
- Use 4L Glass beaker
- Rinse

- water(740ml)
- HCl(260ml)
- Rinse Dishware with water
- Place DBC(3mins)
- Flip Halfway through
- Water in plastic beaker 4liters
- Return DBC to water beaker
- Pour HCl in HCl waste bottle placed in empty dump rinse tank
- place conc. HCl in acid closet
- Rinse 6L Tank and beakers
- turn off bench.

PLASMA Cleaning/ Ashing (DBC, Base Plate)

- Asher on
- Check Argon pump in chase (13.9Psi)
- Check Oxygen Pump in chase (49.6Psi)
- Press ventilation
- Open the cover (Hold it)
- Place your parts in the asher and put them in
- Close the cover and hold it
- Press ventilation off
- Press pump on

- When pressure reaches <0.2 turn on the channel
- Put the channel in oxygen (dial 3)
- Wait for the timer to be on (5min)
- Turn on generator
- Wait for 5 minutes (times "0")
- Deactivate oxygen
- Change channel to Argon (dial 2)
- Press Argon
- Timer on (5min)
- Press generator
- Timer "0"
- Turn of Argon
- Turn of Pump
- Turn on ventilation (hold the cover)
- Pull out your parts and reverse them
- Repeate the process
- Ventilation off
- Close the lid
- Pump on
- Power of asher
- Power off channel
- Close the Argon valve in the chase.

Ni Plating

- Turn ON bench power
- Pump(Green button)
- Temp controller
- Power
- Hold(Wait till it reaches 35C)
- Check liquid level(fill 1" from top)
- Retrieve 150mm Cassette
- Install DBC
- Connect cables
- Anode
- Cathode
- Install cassette holder
- Set time
- Press set up
- Under CS Press up key to desired time then SAVE,RETURN,STOP/ RESET
- Power on
- Voltage-7.9
- Current-2.13
- Enter
- Output On

Area	Density	Current	Rate	Thickness	Units	Time
532.257	0.004	2.13	0.025	3	(um)	120

- Press start Timer
- When complete out put Off
- Press Stop/Reset
- Pumpoff
- Rinse the DBC in water
- Power off bench

Dry Film

- Turn on UV for 30 mins
- Turn on hot plate and set to 120 degree C
- Preheat the laminator
- Preheat on side of the DBC placing it on the hot plate
- Go through the laminator to apply dry film on DBC
- one side of DBC
- Preheat the other side of DBC
- Go through the laminator to apply dru film on the other side
- Put DBC in air for 15 mins to get better adhesion between the DBC and dry film
- Attach/ align mask on DBC
- Expose under UV for 2.5 mins
- Put in air for 15 mins

- Peel of the marla
- Put in developer for 2-3 mins
- agitate the developer solution
- Check the pattern, if not developed increase the developing time by 10 seconds increment untill the DBC is fully developed
- Wash the DBC with de-ionized water
- Dry the DBC
- Ready for Chem Cut

Chem Cut

- Fill process log(Note the thickness of DBC)
- Check level(at the black mark)
- Etch Pump on
- Etch heat on
- Wait untill temp is 125C
- Push rinse water inlet.
- Push Oscillation
- Turn switch ON
- Runout Off/On fron Off to On
- Set conveyor speed (to 3.2 on LCD conveyor)
- Load sample(use table)
- unload sample
- Inspect DBC for proper Etch else increase the speed

- Turn Runout Off/On to Off
- Turn off oscillation,Rinse,Etch heat ,Etch pump.
- Press Stop
- Set Speed/Etch
    - Thickness Speed 1
    - 12mil 3.2

Stripping

- Strip of the blue film from the DBC in the fixer solution for 5 minutes, agitate the solution.
- Wash/Rinse with water untill the resedue of thew blue film goes away.
- Hang the DBC to dry

Dicing

- Prechecks
- Metal blade for Silicon
- Diamond blade for glass/ceramic
- Process log
- Measure sample dimensions
- Package
- Power Up
- Tape mounter
- set to 7
- Demounter

- Saw
- Edit Recipe
- Program 1 for Silicon
- Program 6 for glass/ceramic
- 30,000 RPM for silicon
- 20,000 RPM for glass/ceramic
- Zero Chuck
- No wafer/ frame installed
- Spindle on
- Mount Wafer
- Install wafer
- Install metal frame
- Pull tape
- Wait untill tape bonds to wafer
- Table up
- Table down
- Uninstall metal frame
- Install frame on saw
- Wafer lock
- Spindle on
- Align
- Establish Index
- Pre cut

- Single cut
- Auto cut
- Home
- Uninstall frame on saw
- Spindle off
- Wafer release
- Shut down

Die Attachment (SST Vaccum Furnace)

- Open the Nitrogen valve in the chase
- Turn on the SST power (Green switch)
- Turn on chiller
- Turn on the vaccum pump
- Open the lid
- Put the fixture in the SST
- Run the " SST 405" (Approx 83min. Profile)
- After done open lid and take out the fixture
- Place fixture, DBC, preforms
- Run the "Cleaning" profile (Approx 12min. Profile)
- After done open lid and take out the fixture, DBC, and preforms
- Arrange the Devices using fixture, DBC and preforms
- Put the part back in the SST

- Close the lid
- Run the "SST 405" Profile (Approx 42min. Profile)
- After done open the lib and take out the part
- Turn off vaccum pump
- Click "Power Down the Machine"
- Turn of SST
- Turn off chiller,
- Close the Nitrogen valve in the chase.

Wire bonding:

1. Power on
2. Parts on bonding machine holder
3. Vacuum on
4. Adjust height of first
5. Adjust height of second
6. Adjust loop
7. Bonding
8. Power off
9. Remove cacumme
10. Remove sample from holder.

Attach Connectors in Housing (Using Sikama)

- Press exhaust- start
- Water on (left side, above black mark)
- Gas on (Nitrogen)
- Power on.
- Temperature set
    - 125 200 275 135
    - 125 200 275 135
- Controller set (Set it to 3min. 20sec.)
- Conveyor set (10"/second)
- Press start
- Set hood height.

Encapsulation:

- Use syringe to inject TSE 3521 inside power module side wall
- Leave the module and encapsulate in the room temperature for half an hour
- Move module inside oven and apply vacumme 19 in. of Hg
- Increase the temperature to 150°c and cure it in oven for 1 hour

SST Vacuum Reflow

1.“SAC405” Profile:

00:01 vacuum on
00:02 heat propband 26
00:03 heat rate 5
00:04 heat reset 14
00:05 heat maxpower 25
00:30 VACUUM CHECK SET 100 TORR
00:31 VACUUM CHECK ON
00:34 VACUUM CHECK OFF
00:40 vacuum off
00:41 pressure set 10 psig
00:42 gas3 on
00:59 gas3 off
01:00 exhaust on
01:04 exhaust off
01:06 vacuum on
02:06 vacuum off
02:07 pressure set 10 psig
02:08 gas3 on
02:28 gas3 off
02:29 heat on
02:30 heat ramp 180 c
05:30 heat set 180 c
05:31 exhaust on
05:42 exhaust off
05:43 vacuum on
09:31 heat set 180 c
09:33 vacuum off
09:35 pressure set 10 psig
09:36 gas3 on
09:48 HEAT MAXPOWER 30
09:49 heat ramp 275 c
09:56 gas3 off
11:49 heat set 275 c
11:50 exhaust on
11:57 exhaust off
11:58 vacuum on
13:00 vacuum off

13:01 pressure set 40 psig
13:02 gas3 on
13:22 gas3 off
18:00 heat set 275 c
18:02 heat off
20:46 exhaust on
20:48 gas2 on
23:45 gas2 off
23:48 exhaust off
23:50 beep on
23:53 beep off.

Cleaning (DBC, Fixture, preforms):

1. 0.01 vacuum on
2. 0.02 heat prop band 26
3. 0.03 heat rate 5
4. 0.04 heat reset 14
5. 0.25 heat max power 25
6. 0.3 vacuum chuck set 100 torr
7. 0.31 vacuum chuck on
8. 0.34 vacuum chuck off
9. 0.4 vacuum off
10. 0.41 pressure set 10psig
11. 0.42 gas3 on
12. 0.59 gas3 off
13. 1 exhaust on
14. 1.04 exhaust off
15. 1.06 vacuum on
16. 2.06 vacuum off
17. 2.07 pressure set to 10psig
18. 2.08 gas3 on
19. 2.28 gas3 off
20. 2.29 heat on
21. 2.3 heat ramp 225 C
22. 3.1 heat set 225 C
23. 7.1 exhaust on
24. 7.12 exhaust off
25. 7.15 vacuum on
26. 8.01 heat set 225 C
27. 8.02 heat off
28. 8.1 vacuum off
29. 9.24 exhaust off

30. 9.25 gas2 on
31. 12.5 gas2 off
32. 12.51 exhaust off
33. 12.52 beep on
34. 12.53 beep off

Module Drawings:

Scale- units: Inches.

Base Plate:

The base plate is made of copper with a quarter inch thickness. Figure I.a and Figure I.b shows the measurements of the inverter and rectifier base plates in inches respectively.

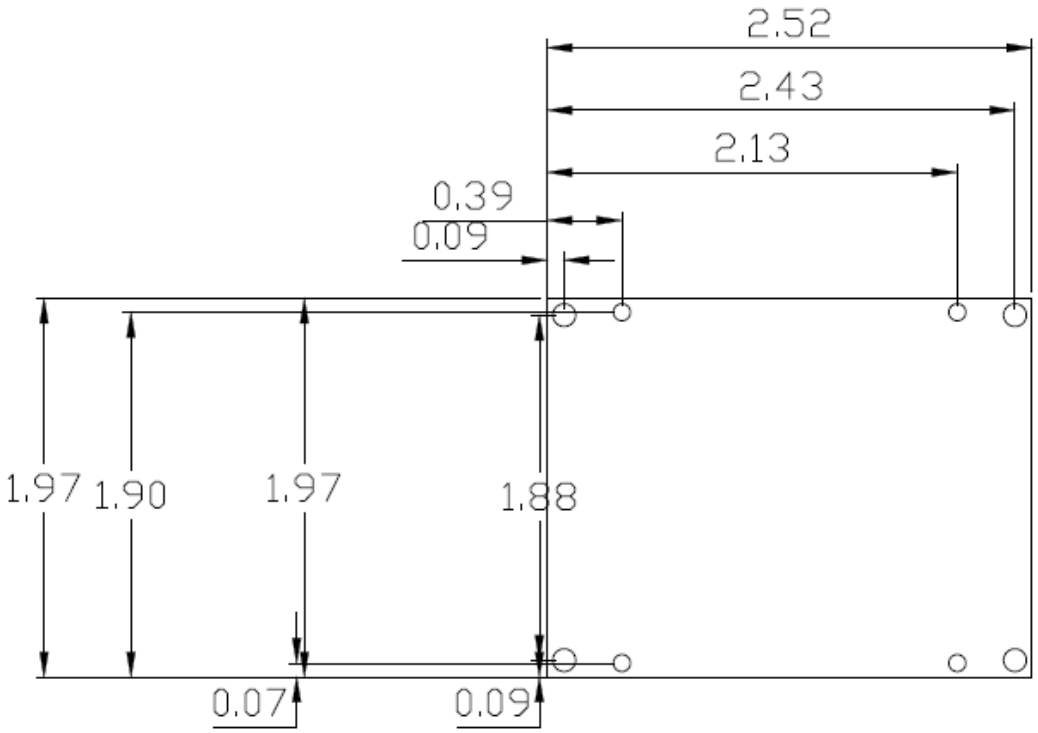

Figure I.a Inverter base plate

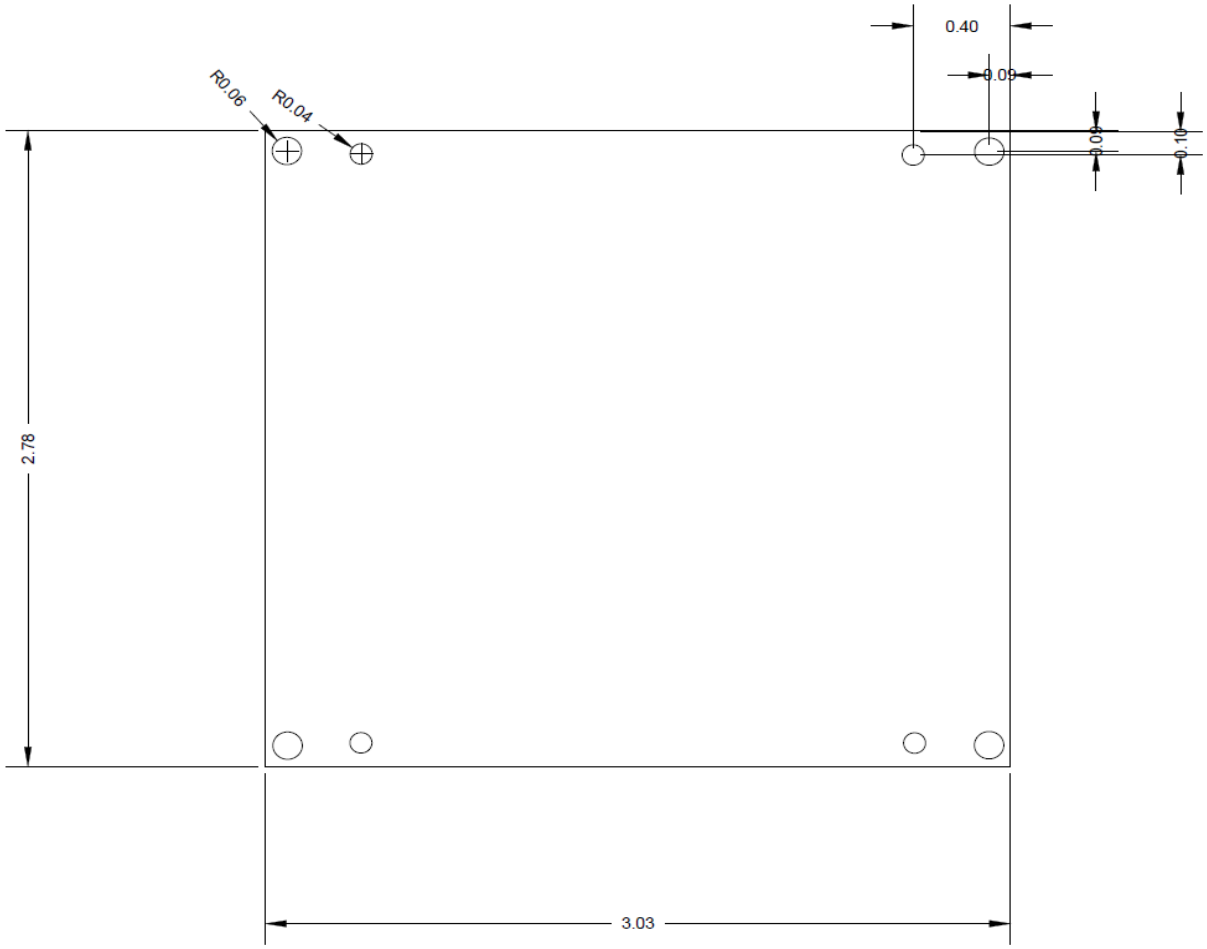

Figure I.b Rectifier Base plate

Housing:

A Polytetrafluoroethylene (PTFE) housing is machined with the below measurements for both inverter and rectifier modules.

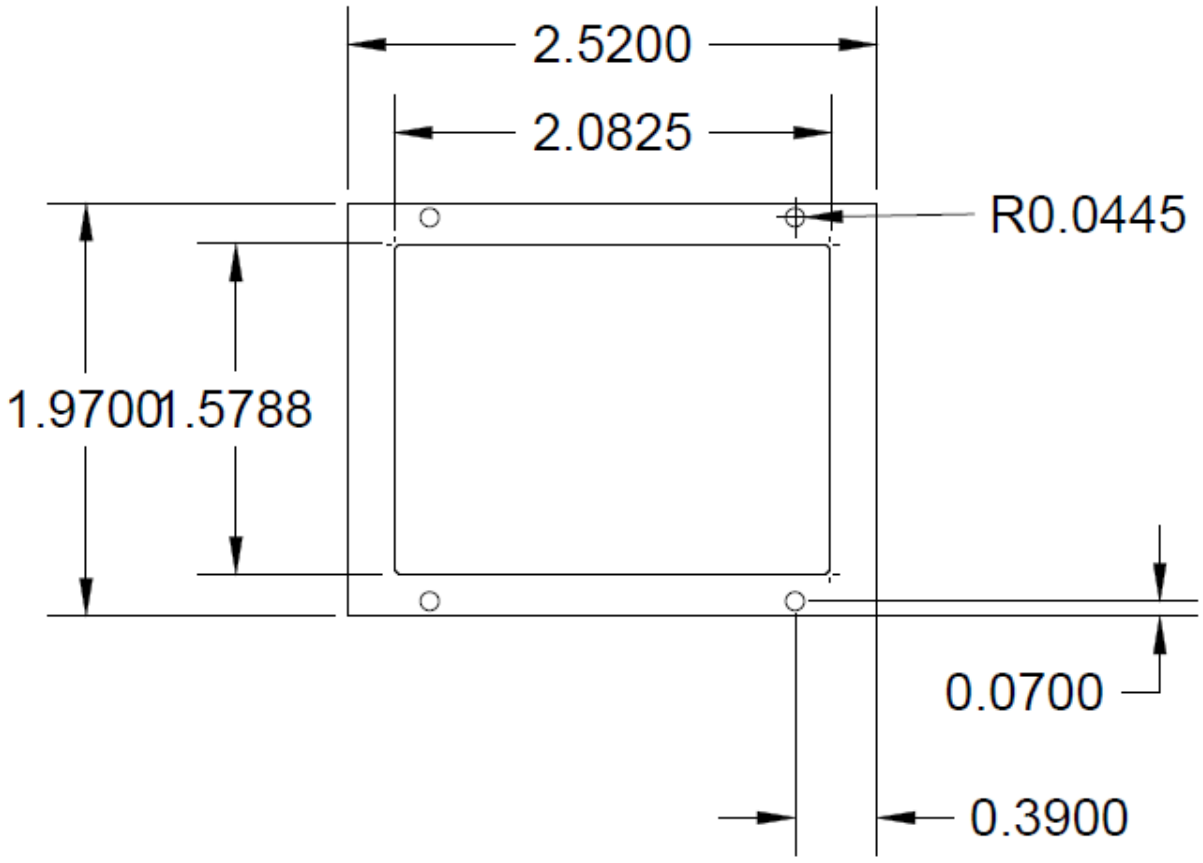

Figure II.a Inverter housing

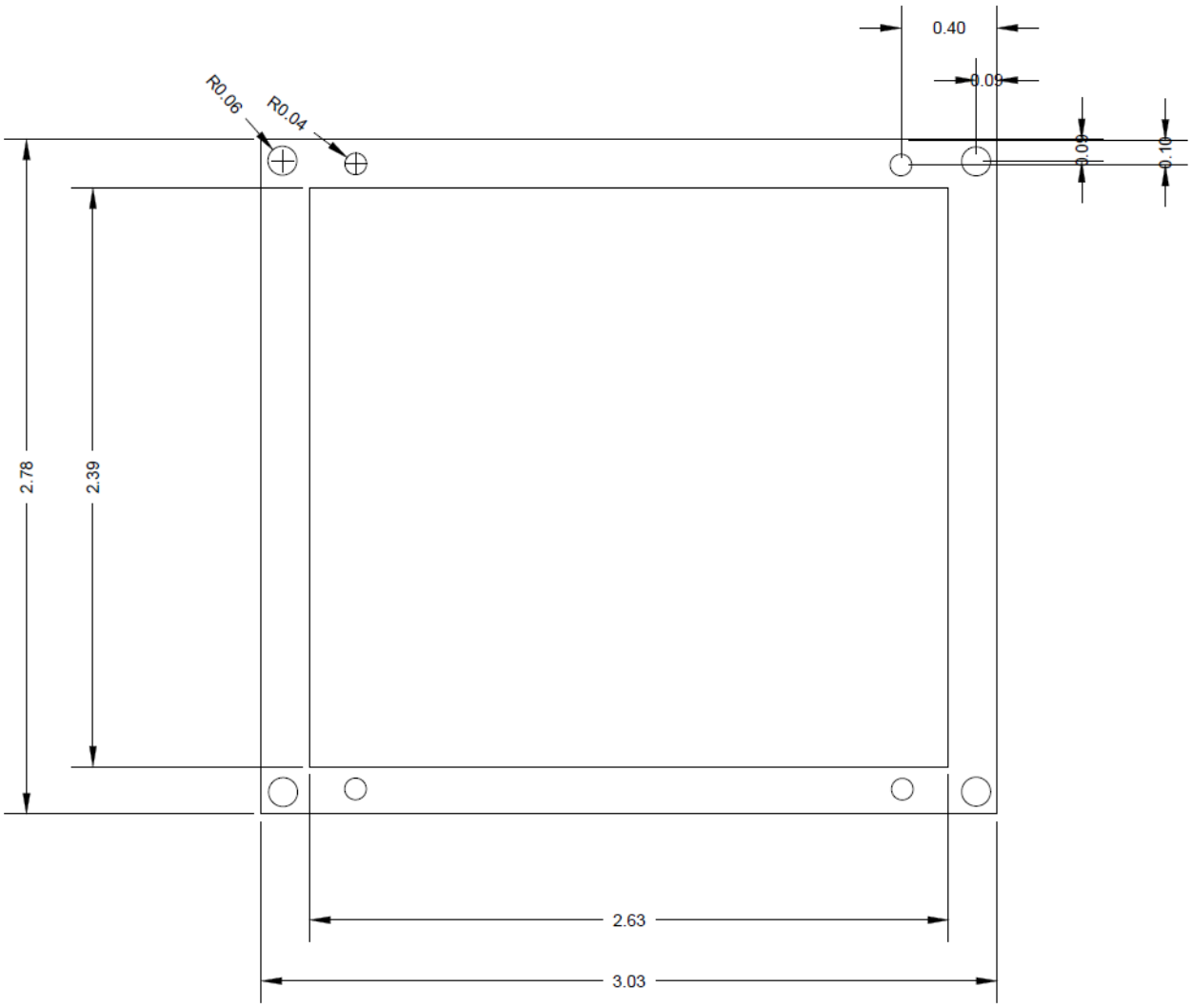

Figure II.b Rectifier Housing.

Graphite Fixture:

The graphite fixtures are designed based on the positions of the devices and the connectors in the module. The drawings for the inverter and rectifier fixtures are shown in figures III.a and III.b, respectively.

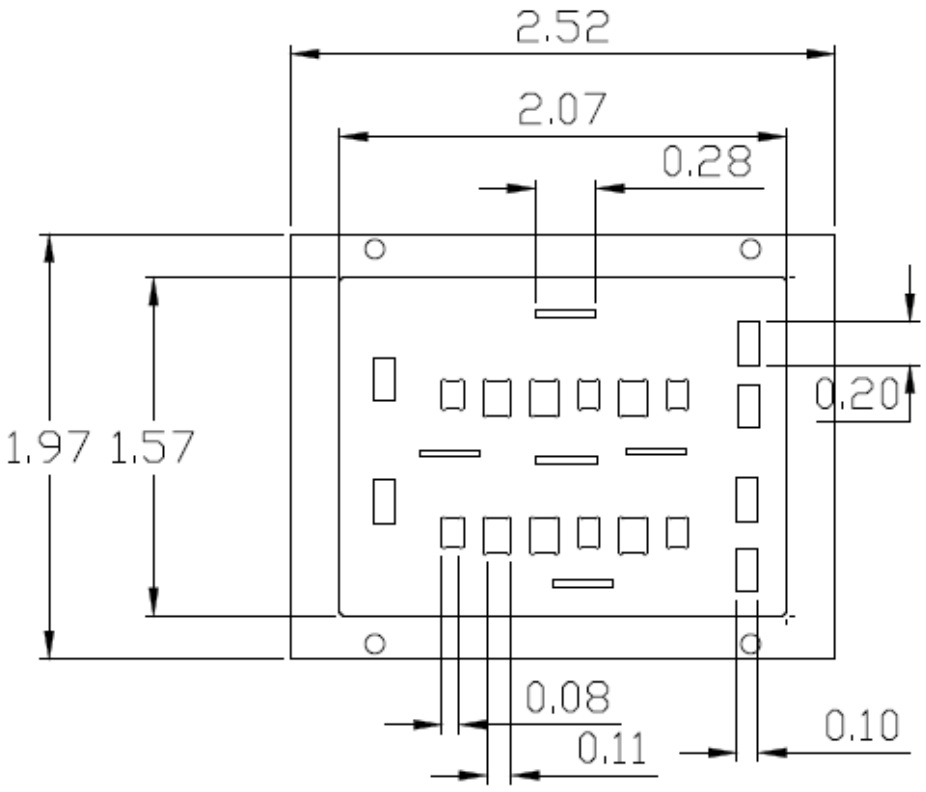

Figure III.a Inverter Fixture.

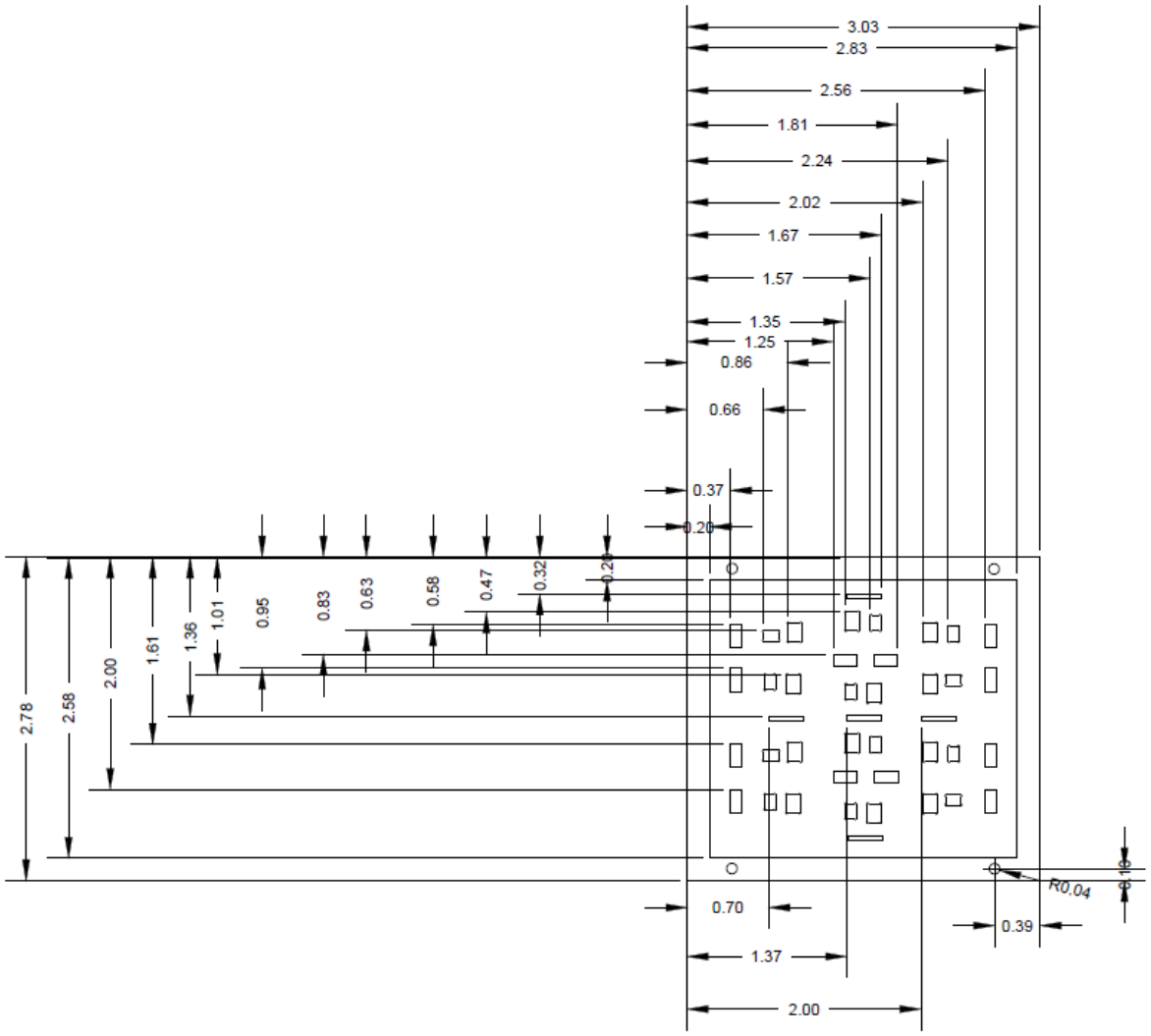

Figure III.b Rectifier Fixture

Photo Mask:

The photo mask used in the dry film is designed in AutoCAD. Figures IV.a and IV.b show the drawings of the inverter and rectifier photo, plots respectively.

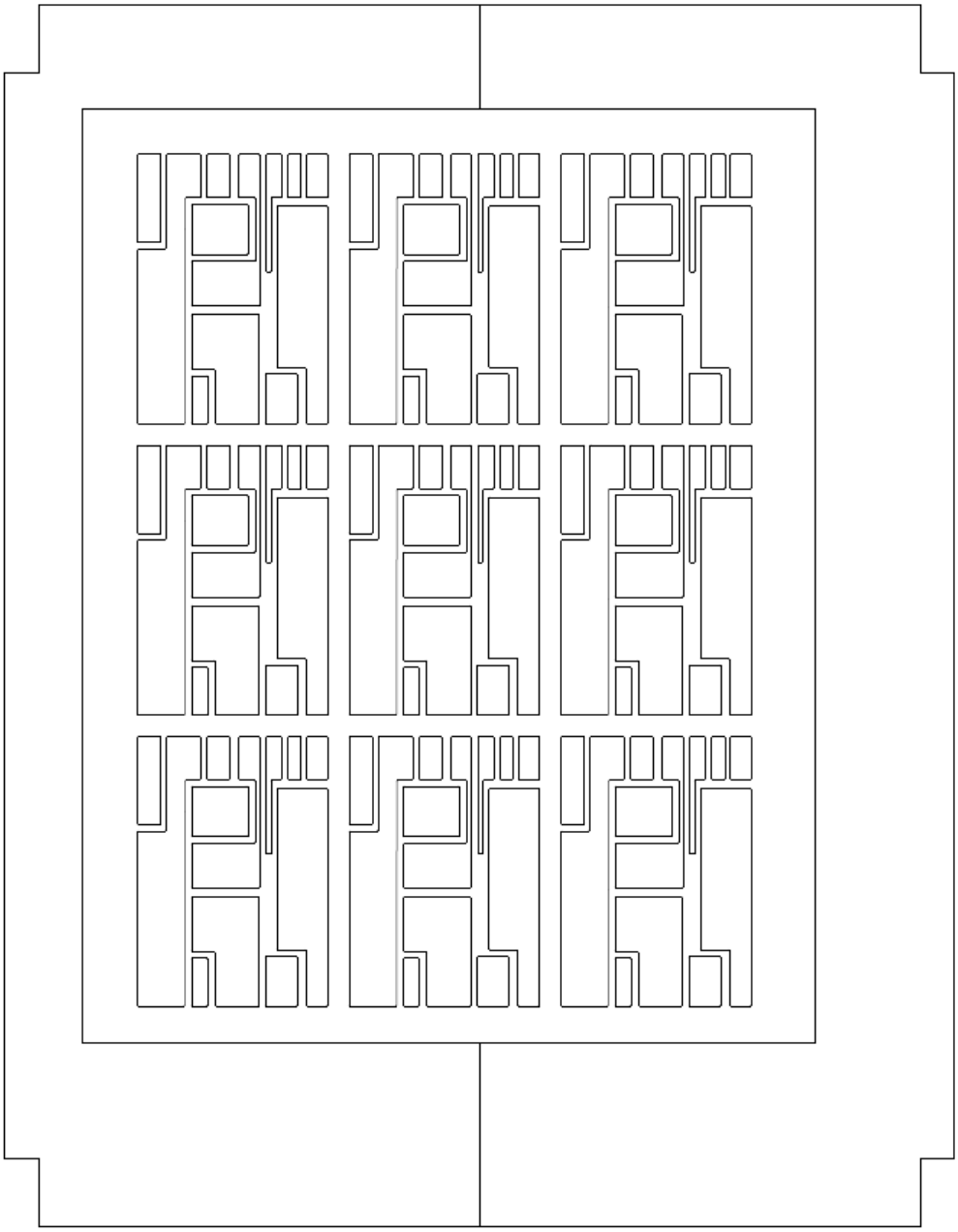

Figure IV.a Inverter Photo Mask

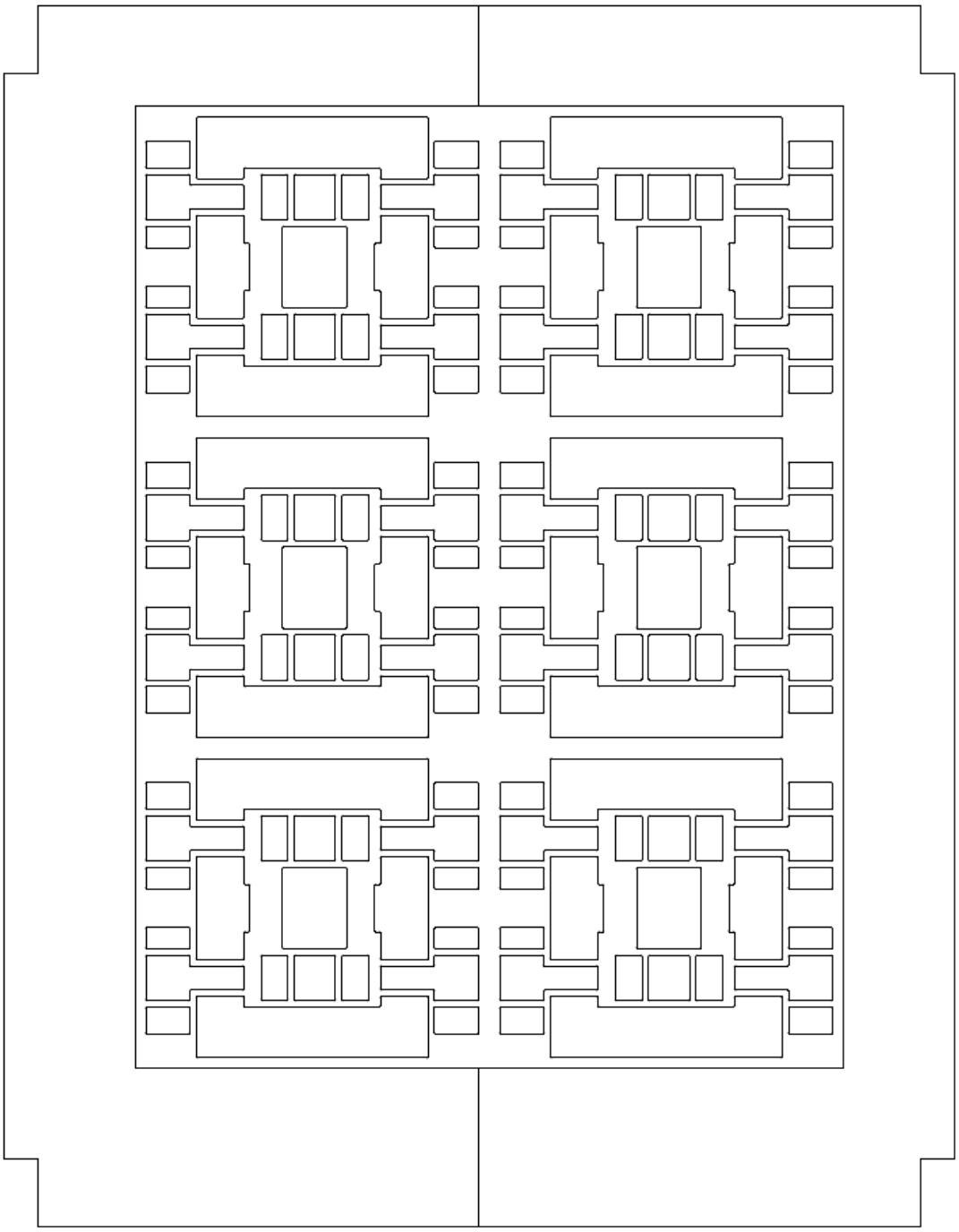

Figure IV.b Rectifier Photo Mask.