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Fabrication of Horizontal Silicon Nanowires Using a Thin Aluminum Film as a Catalyst

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By

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ABSTRACT

Silicon nanowires have been the topic of research in recent years for their significant attention from the electronics industry to grow even smaller electronic devices. The semiconductor industry is built on silicon. Silicon nanowires can be the building blocks for future nanoelectronic devices. Various techniques have also been reported in fabricating the silicon nanowires. But most of the techniques reported, grow vertical silicon nanowires. In the semiconductor industry, integrated circuits are designed and fabricated in a horizontal architecture i.e. the device layout is flat compared to the substrate. When vertical silicon nanowires are introduced in the semiconductor industry, a whole new architecture is needed to fabricate an electronic device. If the silicon nanowires can be grown horizontally, it will be much easier to incorporate these nanowires in the current architecture.

In this thesis, horizontal silicon nanowires were grown on top of a silicon substrate in a bottom up approach. A thin layer of pure aluminum was used as a catalyst to grow the silicon nanowires. In this process, silicon from the substrate itself acts as a source to grow the nanowires. A device cannot be fabricated if the silicon nanowires are in full contact with the underlying silicon substrate. Therefore, in the later part, these silicon nanowires were grown on top of an oxide layer using the same conditions. Several windows were etched in the oxide layer with variable oxide widths to observe the growth of these nanowires.

This thesis is approved for recommendation
to the Graduate Council.

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CHAPTER 1: INTRODUCTION

1.1 Overview of nanowires

An integrated circuit is a piece of semiconductor material, on which a number of electronic devices are connected. Every integrated circuit performs a specific function. Integrated circuits are used in almost all electronic equipment in use today and have revolutionized the world of electronics. The first integrated circuit was created by Jack Kilby in 1959 [41]. Jack Kilby demonstrated the practicality of resistors, capacitors and transistors based on the semiconductor technology. In the year 1964, Gordon E. Moore made an important observation on the rate of improvement of electronic components on a single integrated circuit chip. According to Moore's Law, the number of electronic components on a single integrated circuit chip doubles every 18 months [42]. Figure 1.1 shows the rate of growth of number of components on a single IC chip on Intel Microprocessors. For the past half century, the IC industry has evolved exponentially following the Moore's Law. IC industries make their future planning on the number of components and the size of an integrated circuit based on the Moore's Law.

As the number of components increase, the density of components in a single integrated circuit also increases. Today, major semiconductor companies continue to lead the industry, driving Moore's Law to increase functionality and performance and decrease costs and size, bringing growth to industries worldwide. In the current technology, most of the devices are fabricated in the nanometer regime. Intel is now working on the processors built by 22 nanometer technologies, which is expected to contain more than 3 billion transistors in an area of the size of a fingernail [43].

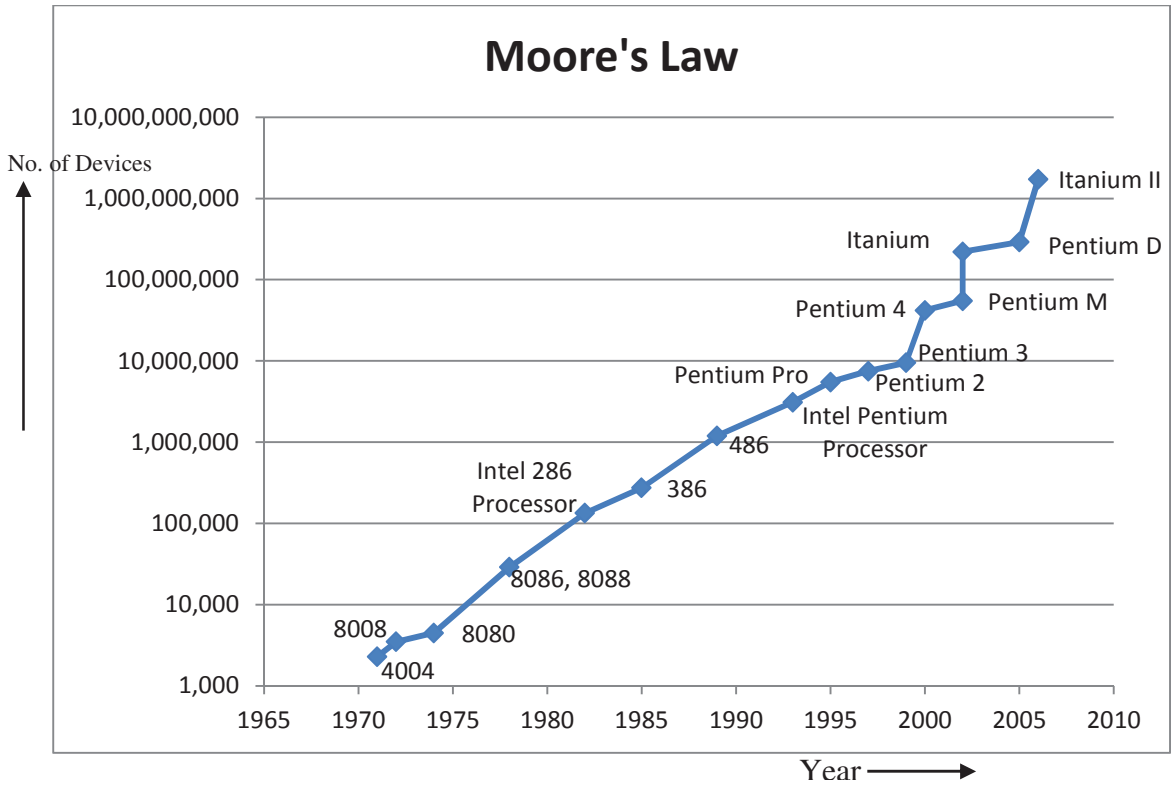

Figure 1 - 1: Growth of number of components on a single IC chip from Intel Microprocessors.

A nanowire is a nanostructure whose diameter is of the order of 10^{-9} meters. There are different types of nanowires, for example metallic (Ni, Pt, Au), semiconducting (Si, Ge, GaN) and insulating (SiO_2, TiO_2) nanowires. These nanowires are often referred to as one dimensional structures because the atoms are confined to grow in a single dimension. Usually the aspect ratio of these one dimensional nanowires (length to width ratio) can be 1000 or more. The incorporation of these nanowires into the integrated circuits proved the continuity of Moore's Law. For example, Itanium II 9000 series chips from Intel has a device count of around 1,720,000,000 is made using the 90 nanometer process technology.

Silicon nanowires are the most important nanostructures which can be used in the manufacturing of nano-semiconductor integrated circuits. Since silicon is the most common material used in the semiconductor industry, silicon nanowires can be easily incorporated into

the current technology. These silicon nanowires can be synthesized by many processes. Much success has been achieved in growing vertical silicon nanowires on a substrate. The first vertical silicon nanowire was identified in the year 1964, by R. S. Wagner and W. C. Ellis using the Vapor-Liquid-Solid method. This process was later on explained in detail by E. I. Givargizov in the year 1975.

The silicon nanowires can also be fabricated by photolithography process. But the cost of manufacturing of these nanowires is very high. In the photolithography process, the material is made into the desired shape in such a way that it can be incorporated into the components. This process is referred as a top down approach. The Vapor-Liquid-Solid process is considered as a bottom up approach. In this approach, the natural behavior of atoms, depending on the growth parameters, leads to the construction of the nanostructures. In general the bottom up approach is a cost effective process when compared to the top down approach.

1.2 Motivation

The motivation for this work is to fabricate a network of horizontal silicon nanowires on top of an insulating layer using aluminum as a catalyst.

In the semiconductor industry, aluminum is one of the most common materials used for metallic interconnects in the semiconductor industry. Aluminum is an excellent conductor and forms an ohmic contact with silicon. An ohmic contact is a region on semiconductor device that has been prepared so that the current-voltage (I-V) curve is linear. In this type of contact, current is not rectified by the metal–semiconductor junction. Rectifying properties depend on the metal's work function, the band gap of the intrinsic semiconductor, the type

and concentration of dopants in the semiconductor, and other factors. If the metal-semiconductor junction has rectifying properties, a potential barrier is formed near the junction, which can have characteristics just like a diode.

Aluminum can easily be deposited on a substrate by evaporation or sputtering techniques. Though aluminum has many advantages, it also has some disadvantages, for example, interdiffusion of silicon and aluminum at high temperatures. This is because of the high diffusivity of silicon in aluminum at high temperatures. When pure aluminum is deposited on a silicon substrate as a contact and when the substrate is heated to high temperatures, silicon diffuses into the pure aluminum from the point of contact, which in turn makes pits in the silicon substrate. To cover the void, aluminum diffuses into the silicon substrate. This effect is referred to as 'aluminum spiking'. This spiking can largely affect the quality of the electronic components because of the increased leakage current.

If the diffusion of silicon through the aluminum layer can be controlled by varying the parameters, to self-assemble the silicon atoms along the grain boundaries of aluminum, a network of horizontal silicon nanowires can be fabricated.

1.3 Goals

In this effort, the goal is to control the growth of a network of horizontal silicon nanowires on top of an oxide layer using a thin aluminum film as the catalyst. The concept of high diffusivity of silicon in aluminum films will be used to fabricate a network of horizontal silicon nanowires. The role of the silicon dioxide layer, acting as a barrier layer between the silicon and the aluminum will be investigated to get a good network of horizontal silicon

nanowires. An attempt to produce a model for a junctionless horizontal silicon nanowire back gate field effect transistor is made.

In order to accomplish the goals of this research, several experiments were designed with different patterns and different thicknesses of silicon dioxide layer. The outcome of the work was a network of horizontally grown silicon nanowires on top of an oxide layer. The diameter of the silicon nanowires was measured to be from 60 nm to 100 nm.

1.4 Thesis Organization

Chapter two introduces the reader to the interaction between aluminum and silicon materials. The properties of aluminum and silicon are highlighted to discuss the phenomenon of the high diffusivity of silicon in an aluminum film. The material of this chapter is closely related to the results presented in chapter four. Most of the discussion on the results of this work depends on the information presented in this chapter.

Chapter three describes the experimental methods used in this research. Some of the analytical methods used in this research are briefly explained in order to better understand the results.

Chapter four describes the results and discusses the implication on this research. Analytical results are shown in this chapter to explain the growth of horizontal silicon nanowires.

Chapter five includes the conclusion and future work.

CHAPTER 2: LITERATURE SEARCH

2.1 Introduction to Silicon Nanowire Growth Techniques

In the recent years, many efforts have been made to fabricate silicon nanowires by employing different methods such as nano-photolithography method, laser ablation method, Vapor-Liquid-Solid method, thermal evaporation method etc. These methods can be classified into two approaches – Top-down approach and Bottom-up approach.

2.1.1 Top-Down Approach

In top – down approach, the nanostructures are defined on a substrate by the combination of photolithography, etching and deposition. This approach uses the nano or micro fabrication methods, where external tools are used to cut, mill, and shape materials into a desired shape. In the conventional photolithography, the features are transferred from a mask onto a substrate coated with a thin layer of photoresist by shining the ultraviolet light. However, the feature size in this process is limited to only several microns depending of the wavelength of light. The feature size can be decreased in the photolithography process by implementing the recent technologies. But the cost of the equipment goes exponentially high [1].

Dr. J. A. Rogers's group from University of Illinois at Urbana-Champaign has been doing research on fabricating high performance flexible thin film transistors by transferring a network of thin silicon nanowires onto a plastic substrate [2]. In their process, silicon-on-insulator wafers were used as the substrates. On these wafers, the thickness of silicon on the insulator is 100 nm. The native oxide was stripped off from the surface using a dilute HF acid. Then a thin layer of 20 nm Al, followed by a 100 nm Au was evaporated on the substrate. The metallic layer was then

patterned into desired geometries using photolithography or micro-contact printing and etching. The exposed silicon was anisotropically etched using TMAH, followed by a lift-off process of the underlying oxide layer which was etched using a concentrated HF acid and free the silicon nanowires. Figure 2.1(a) shows the fabrication process used by the group and (b) shows a bunch of nanowires fabricated using the process.

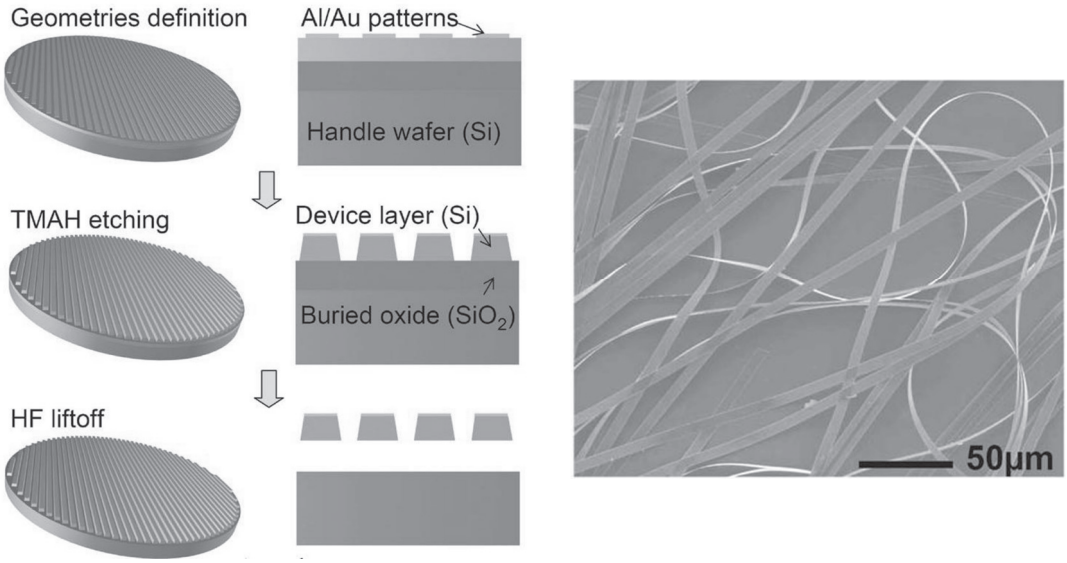

Figure 2 - 1: (a) Top-Down process of silicon nanowire fabrication, (b) set of silicon nanowires fabricated using the process [2].

2.1.2 Bottom-Up Approach

In the bottom – up approach, silicon nanowires are grown or synthesized instead of patterning or etching. In this approach, atoms are selectively added to create the structures. It uses the chemical properties of the materials to self-organize itself into a desired structure. Self-assembly is an important aspect in this approach. This approach is a very cost effective process when compared to a top-down approach.

There are many processes to grow silicon nanowires using bottom-up approach, such as laser ablation method [8], thermal evaporation method [7], plasma enhanced chemical vapor

deposition method [9], and the most common vapor-liquid-solid (VLS) method. This method was first introduced by R. S. Wagner and W. C. Ellis in 1964 [3] [4] and later on in the year 1975, it was described in detail by E. I. Givargizov [5].

2.1.2.1 VLS Process

The discovery of the VLS technique occurred by accident [3]. Liquid metallic spheres were observed to form on the tips of growing whiskers because of the presence of impurities. Impurities were concentrated at the tip of the whiskers where they formed low-melting eutectic phases. The metallic sphere was termed as a "catalyst" because of its role in accelerating the growth process. The VLS technique is now the preferred technique for growing whiskers and the catalyst is intentionally added to system. A metallic catalyst is applied to a growth substrate that is heated in a controlled atmosphere furnace.

The catalyst melts and beads to form nanodots. Process gases, like silane, are then passed in the furnace and the catalyst becomes supersaturated and begins to precipitate a nanowire. The nanowire grows in a preferred orientation and continues growing as long as the process gases are supplied. The metallic catalyst nanodot at the tip of the nanowire has a complex function. In addition to being a catalyst for gas-phase reactions, it also serves as a medium for nanowire precipitation. The size of the catalyst nanodot determines the diameter of the nanowire grown [10]. Figure 2.2 shows the VLS growth mechanism.

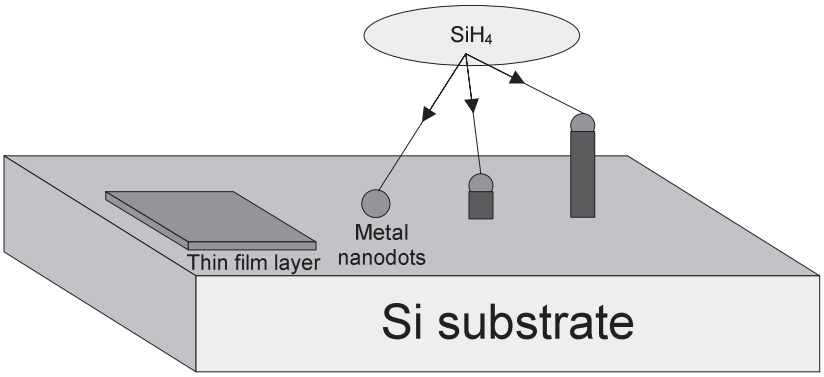

Figure 2 - 2: VLS process mechanism

2.1.2.2 Evaporation Process

In the evaporation process [7], a mixed powder of silicon and metal (as a catalyst) is heated in a silica boat, inside a quartz tube at high temperatures like 1200ºC. At this temperature, the silicon powder will be vaporized. There is a constant flow of an inert gas like argon inside the quartz tube, directed towards the substrate. The vapor is carried by the flowing argon onto the silicon substrate to grow the silicon nanowires. This process is very simple and direct, but the only problem is the elevated temperatures. At high temperatures, the metal catalyst might contaminate the silicon nanowires and the silicon substrate. Also the position and the diameter of these nanowires cannot be controlled by this process.

2.1.2.3 Laser ablation method

In this method [8], the apparatus consists of a laser source, lens, target, furnace, cold finger (for collecting nanowires) and inert gas inlet/outlet. Inside the quartz furnace, a laser beam is focused onto the target to create a hot dense vapor of silicon and the metal catalyst. Usually the target is an alloy of silicon and a metal catalyst. The quartz furnace should be maintained at the eutectic temperature of silicon and the metal catalyst to keep the clusters in liquid state.

Silicon nanowires begin to grow after the metal catalyst and silicon liquid balls become supersaturated in silicon and continue to grow as more silicon saturates in the balls. The grown nanowires are carried by the inert gas to the cold finger. When they reach the cold finger, the nanowires solidify and the growth terminates. The diameter of the nanowires depends on the size of the clusters. However the diameter of these nanowires cannot the controlled because the clusters are formed in the vapor instead of a pre-patterned catalyst. The position of the nanowires also cannot be controlled because they solidify randomly on the cold finger.

2.2 Challenges in vertical silicon nanowire growth and device fabrication

So far, making nano-devices from silicon nanowires involves a two-step process: fabricating and then positioning the nanowire in the desired position to fabricate an electronic device [25]. For silicon nanowires, precise control of the size, diameter, position and orientation have been practical problems. After the silicon nanowires are grown, there are still many problems in the post-growth steps to make nanodevices, such as handling, positioning, aligning and assembling. Because of their extremely small size, latest technology is required to handle these tasks.

The problem with each of the growth method is that it is not compatible with the current silicon thin film industry [26]. For example, for the vertical nano electronic devices, the device architecture is not yet implemented in the industry. The device architecture is more suitable for the horizontal electronic devices. Semiconductor device fabrication is a multi-step process of photographic and chemical processing steps during which electronic circuits are created on a semiconducting wafer made of silicon [27]. After the devices are fabricated on a wafer, several layers of interconnecting metal contacts are processed that are separated by dielectric layers [28].

The insulating layer can be a form of silicon dioxide or a silicate glass, but recently low dielectric constant materials are being used.

Our objective is to grow a horizontal network of silicon nanowires on top of an insulating layer (silicon dioxide) on a silicon substrate. Aluminum is used as a catalyst to grow the horizontal silicon nanowires. The position of the horizontal silicon nanowire depends on the position and geometric attributes of the oxide layer. The length and alignment of the horizontal silicon nanowires can be controlled well in this process and can be easily used for device fabrication.

2.3 Aluminum – Silicon:

In the silicon industry, aluminum is one of the most preferred metals used for the interconnections. It has many advantages over other metals, for example copper or gold. Gold traps the electrons and holes in silicon killing the lifetime of the electrons [29] and also poses a serious contamination problem for silicon in the CMOS technology. Copper has a high contact resistance with silicon [30]. From an electrical point of view, aluminum is less conductive compared to copper and gold but aluminum has a low resistivity and a good current carrying density. Aluminum is also available in its purest form and is easy to pattern with the conventional photolithography process.

2.3.1 Aluminum – Silicon Phase Diagram

Phase diagrams are used to represent the state relationships between materials as a function of temperature. Figure 2.3 shows the phase diagram of aluminum and silicon. A phase diagram is a graphical representation of the equilibrium states of an alloy for various

temperatures. The states may be solid, liquid or gases and the materials take a variety of forms depending on interactions between them. The most common form is used to show the interactions between two materials and is called a binary phase diagram. The phase diagram is drawn from the phase rule of Williard Gibbs [11]. The phase rule states that sum of the number of degrees of freedom of a system must equal the sum of the components plus two when in equilibrium, and is given by:

$$P + F = C + 2$$

P is the number of phases, F is the degree of freedom and, C is the number of pure elemental components. The degrees of freedom are the number of intensive variables, such as temperature and, pressure, that can be altered without bringing about the disappearance of a phase or the formation of a new phase.

The free energy concept can be used to explain the phase behavior of an alloy system. According to the second law of thermodynamics, in a system in which the temperature and pressure are fixed, the thermodynamic potential or Gibbs free energy, G, must be a minimum. The thermodynamic potential is given by:

$$G = U - TS + PV$$

U is the internal energy, T the temperature, S the entropy, P the pressure, and V the volume. For the alloy systems, the PV term is small and can be neglected. The condition of equilibrium is that the free energy F = U – TS should be minimized. This quantity, F, is known as the Helmholtz Free Energy.

2.3.2 Eutectic System

A eutectic system is a mixture of elements that has a single chemical composition that solidifies at a lower temperature than any other composition. This composition is known as the eutectic composition and the temperature is known as the eutectic temperature [32]. On a phase diagram the intersection of the eutectic temperature and the eutectic composition gives the eutectic point. For aluminum and silicon, the eutectic temperature is 577ºC at 12.6% weight of silicon. The melting points of aluminum and silicon are 660ºC and 1414ºC. At the eutectic point, the liquid of the two solid solutions coexist at the same time and are in chemical equilibrium. The eutectic temperatures of some other alloys of silicon are shown in table 2.1 [12].

Aluminum and silicon solidify in different structures, respectively Face Centered Cubic (FCC) and diamond cubic. In figure 2 – 3, these two solid phases are shown as α and β regions. At high temperatures, the hypoeutectic alloy forms a rich aluminum α-phase solid. The hypereutectic alloy forms almost pure β-phase silicon. Very little silicon dissolves in the α-phase and very little aluminum dissolves in the β-phase.

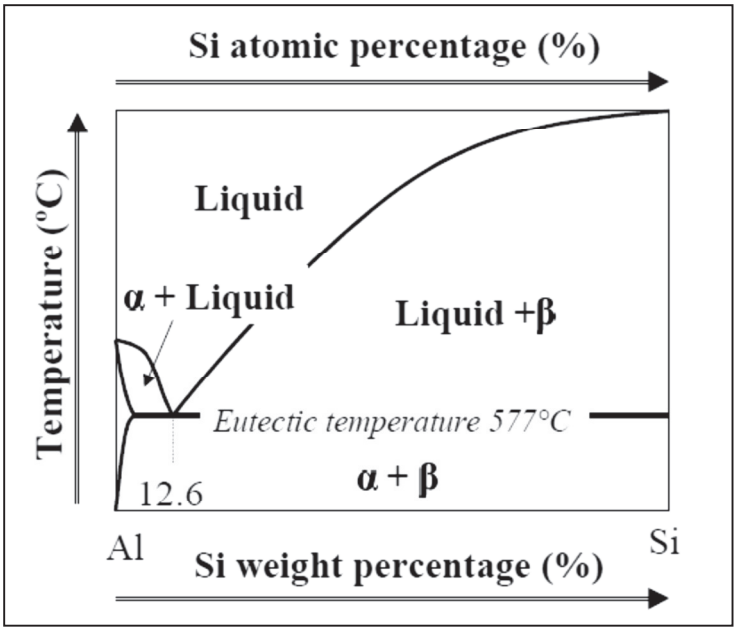

Figure 2 - 3: Phase diagram of Aluminum and Silicon

Alloys	Eutectic Temperature
Au-Si	360ºC
Al-Si	577ºC
Ag-Si	837ºC
Fe-Si	>1200ºC

Table 2 - 1: Eutectic temperatures of different silicon alloys

2.4 Aluminum interaction with silicon

The thermal expansion coefficients of aluminum and silicon are 24 x 10^{-6} /K and 2.6 x 10^{-6} /K respectively. When a silicon substrate is annealed in contact with aluminum, there will be significant amount of compressive stress build up on the aluminum film. In some cases, the stress causes the aluminum film to peel and become discontinuous.

Other major problem with aluminum and silicon is the aluminum spiking. Aluminum is very reactive with silicon. The diffusion constant, D, can be calculated from the equation:

$$D = D_0.e^{(-Ea/kT)}$$

where D_0 is the pre-exponential term (D_0 = 4.8 cm^2/sec) and E_a is the activation energy (Ea = 3.36 eV) [34]. Pure aluminum is highly unstable on silicon when the contact is annealed at 450°C. Silicon has a high diffusivity (10^{-8} cm^2/sec primarily along aluminum grain boundaries) and a high solubility (0.5 wt. %) in aluminum. Therefore, the contact failure mechanism is silicon dissolving in aluminum and aluminum spiking in silicon [33]. Sometimes this process causes shorting between the metallic multilayers or the active layers of silicon, damaging the device [13].

Electromigration is another problem where metal ions are transported by momentum exchange between electrons moving under the influence of an electric field. To solve the problem of spiking, a diffusion barrier is used to prevent the direct interaction of aluminum and silicon. Another method is also used, where a small percentage of silicon is mixed in the aluminum layer, which is deposited on top of the silicon layer. This prevents the diffusion of silicon from the substrate into the aluminum layer [33].

One more reason for aluminum is chosen as a metal contact in MOSFET is because of its good adherence to silicon dioxide. At high temperatures, aluminum interacts with silicon dioxide layer and forms aluminum oxide (Al_2O_3). This reaction is an exothermic reaction. Aluminum breaks the silicon-oxygen bonds and forms a more stable aluminum oxide releasing 176.4kcal/mole energy [32]. The reaction is as follows:

$$3SiO_2 + 4Al \longrightarrow 2Al_2O_3 + 3Si + 176.4 \text{ kcal/mole}$$

This process is self-limiting. When aluminum oxide reaches a certain thickness, it acts as a barrier and prevents further oxidation of aluminum.

CHAPTER 3: EXPERIMENTAL METHODS

3.1 Introduction

The first part of this chapter describes the techniques, materials, and procedures used in this research. In the present study, silicon wafers and corning 7059 glass samples are used as the substrates. The silicon samples are cleaned with a three stage wet chemical cleaning process. Silicon dioxide is grown on the silicon samples by thermal oxidation. The oxide is patterned using photolithography process. Aluminum is deposited on the samples using two ways: sputtering and thermal evaporation. After the thin film deposition, the samples are annealed in a high vacuum annealing chamber. Focused Ion Beam (FIB) is used to deposit platinum as drain and source contacts on a nano electronic device. After the deposition and annealing, the surface morphology of samples is studied using Scanning Electron Microscopy (SEM). Energy Dispersive X-ray spectroscopy is used to determine the distribution of different elements on the samples. In this chapter, a brief description of these tools will be presented.

3.2 Sample preparation

3.2.1 Silicon substrate cleaning

In this research, (100) oriented 5 inch silicon wafers are used to prepare the samples. 1 inch x 1 inch square silicon samples are cut from the 5 inch wafers using a dicing saw. After dicing the wafer, the samples are cleaned with deionized water jet and dried using a nitrogen gun. The samples are then carried in a closed container to a “class 100” clean room to do a three step wet chemical cleaning process.

In the first step, organic residues on the substrates are cleaned using a piranha solution (1:1 H_2SO_4:H_2O_2) at 120°C [35]. The reaction with these two chemicals is exothermic; therefore no external heating is required to heat the solution. The mixture is a strong oxidizer. It will remove most organic matter, but hydroxylates the surface, making them extremely hydrophilic. The samples are immersed in the piranha solution for 10 minutes and are rinsed with deionized water. To remove the oxide layer, the samples are dipped in a diluted hydrofluoric acid (1:100 HF:H_2O) for 30 seconds. The samples should be hydrophobic after this step. The samples are then rinsed with deionized water to remove the droplets of diluted hydrofluoric acid.

The substrates are then subjected to Baker Clean process. For this step, JTB-100 (diluted Alkyl-Ammonium Hydroxide) from J. T. Baker is used instead of the two step RCA chemical cleaning method [36]. Statistics from the J. T. Baker Company shows that the particle count after using the JTB – 100 is below the original or virgin wafer particle count. This step removes all the inorganic contaminants from the substrates. The substrates are transferred to a mixture of (1:0.2:5 JTB-100:H_2O_2:H_2O) solution heated to 70°C for 10 minutes. An external heater is used to heat the solution since there is no exothermic reaction in this mixture. The substrates are then rinsed with deionized water. This step is followed with a quick dip in diluted hydrofluoric acid (1:100 HF:H_2O) for 30 seconds to remove the oxide formed during the cleaning. The samples are again rinsed with deionized water to remove any remaining hydrofluoric acid droplets.

The final step is to remove the native oxide layer from the substrates. The easiest way is to immerse the substrates for a few seconds in diluted hydrofluoric acid. For this purpose, the substrates are dipped in diluted hydrofluoric acid (1:10 HF:H_2O) for about 30 seconds [14]. Together with the removal of the native oxide layer, the surface becomes hydrogen terminated

and hydrophobic. Finally the substrates are dried in a stream of nitrogen gas to remove any traces of hydrofluoric acid.

3.2.2 Deposition of Aluminum

3.2.2.1 Sputtering

Thin aluminum films are sputter deposited on the samples in a chamber of a multi chamber cluster tool. Figure 3.1 shows the schematic diagram of the multi-chamber cluster tool that is used in the present study. The multi-chamber system has five chambers. Main Processing Zone (MPZ) 1 is a PECVD chamber for intrinsic silicon deposition, MPZ 2 is also a PECVD chamber for phosphorous or boron doped silicon deposition, MPZ 3 is a sputter deposition chamber for amorphous silicon, MPZ 4 is a sputter chamber for aluminum, and MPZ 5 is used for annealing. Home is a chamber through which samples are placed in the tool. The multi-chamber system has an Internal Transfer Zone (ITZ), which is a connecting chamber from home to any of the other chambers. A mechanical pump is connected to the ITZ that can reach 100 mTorr. The ITZ has a mechanical arm controlled by a computer through a stepper motor. The robotic arm can be programmed to place a substrate in the five MPZ's. MPZ1 and MPZ2 are connected to one turbo molecular pump; MPZ3 and MPZ4 are connected to another turbo molecular pump. Every chamber has its own throttle valve that isolates it from its turbo pump. The turbo molecular pump can pump the MPZ's to a pressure below 10^{-8} Torr. Figure 3.2 shows the front view of the multi-chamber system.

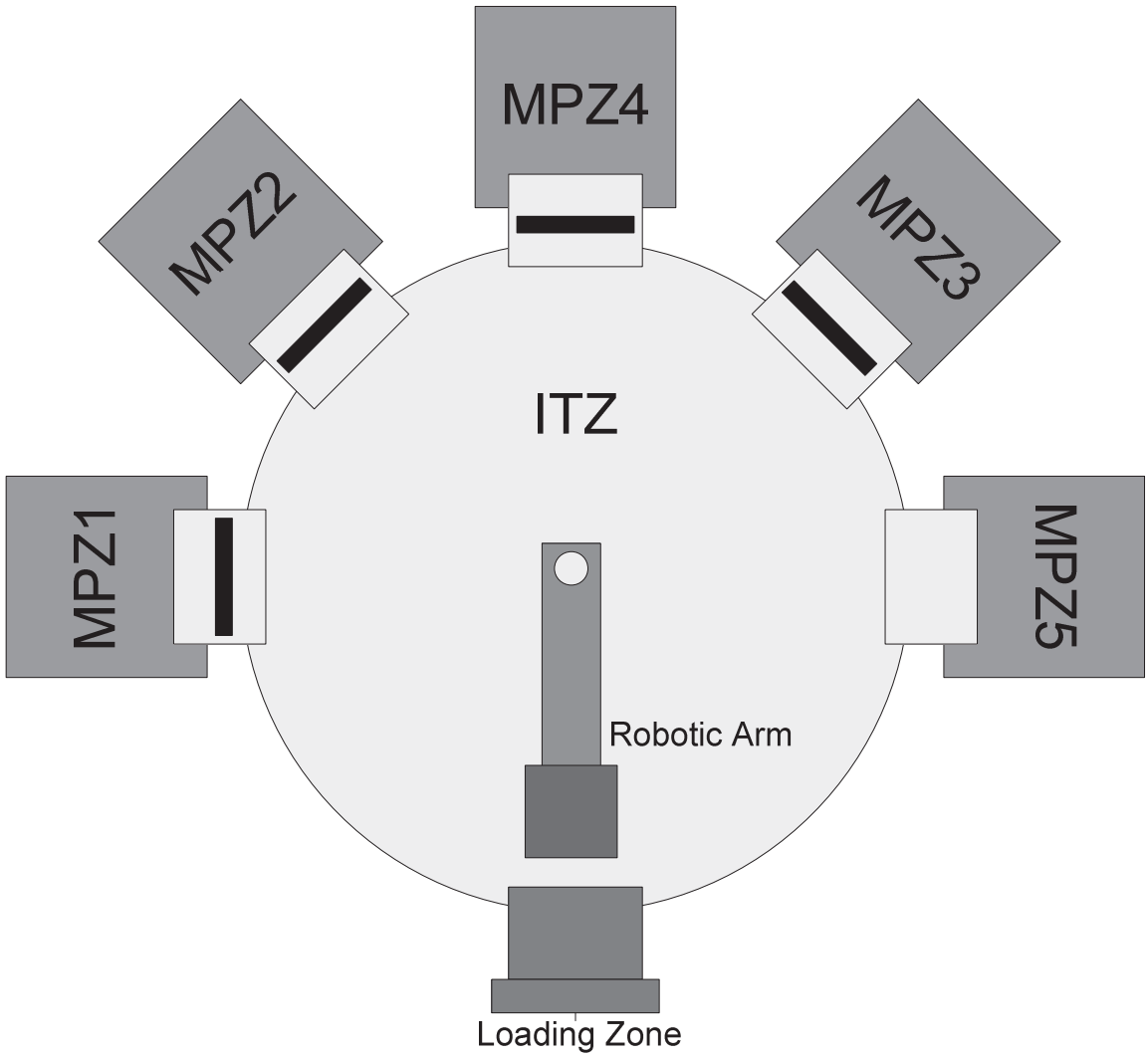

Figure 3 - 1: Schematic view of the Multi-chamber System

Aluminum sputtering is done in MPZ4. Before placing the samples in MPZ4, all the gate valves for the MPZ's are checked to ensure that they are closed. Then ITZ is vented to atmospheric pressure. The sample is placed in the home chamber and the robotic arm is programmed to pick up the sample holder from home. During this time, the home gate is closed manually and the roughing valve is opened to pump the ITZ. After the pressure inside ITZ reaches 100 mTorr, the roughing valve is closed and the gate valve for MPZ4 is opened. The robotic arm is then programmed to transfer the sample

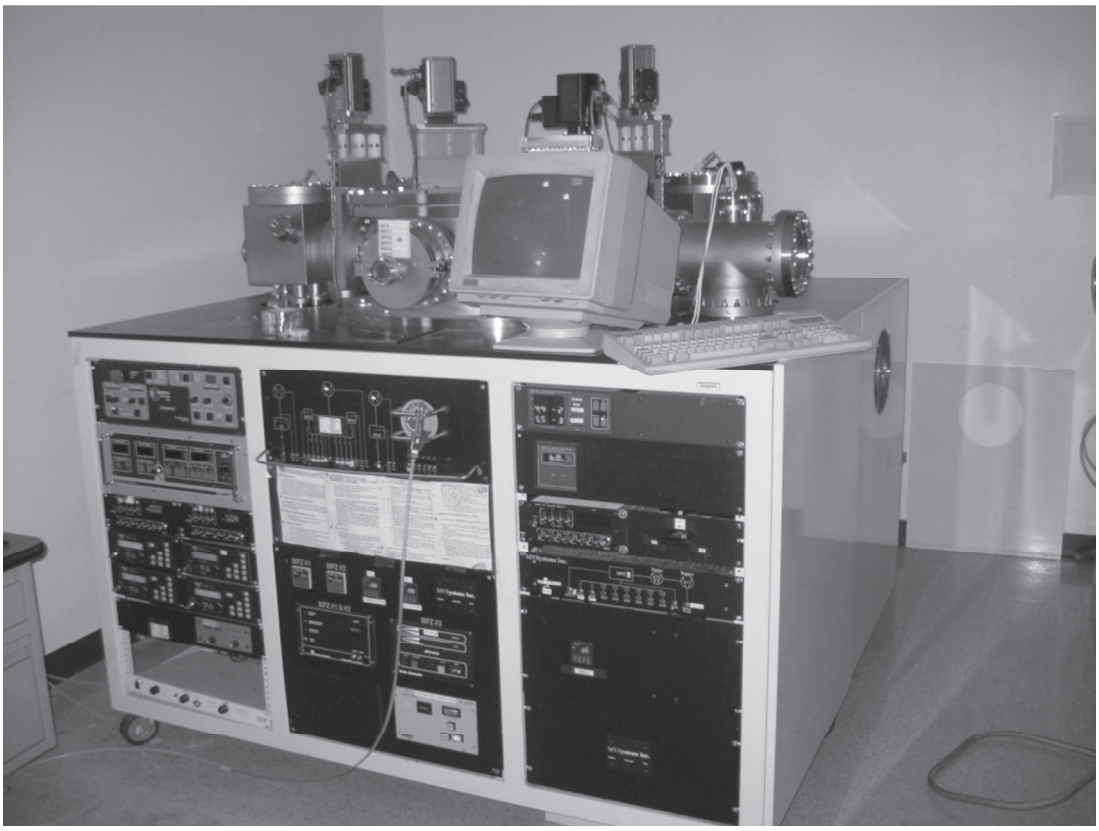

Figure 3 - 2: Front view of the Multi-Chamber System

holder to MPZ4. The gate valve is then closed and the throttle valve is opened full to pump the chamber using turbo molecular pump. The sputtering chamber uses a 3 inch diameter magnetron sputter gun. The chamber is pumped down to a very high vacuum in the order of 10^{-8} Torr before any gas is introduced. Argon gas is used as a precursor in the sputtering chamber. Argon gas is flown in the chamber at a rate of 20 sccm. The plasma dissociates the argon gas into ionized Ar^{+} ions. These argon ions are accelerated towards the negative electrode, which is the aluminum target. The Ar^{+} ions bombarded the aluminum target, knocking off the aluminum atoms. The knocked off aluminum atoms are deposited on the substrate forming the aluminum film. The chamber is maintained at a pressure of 5 mTorr using the throttle valve and the temperature is maintained at 40ºC.

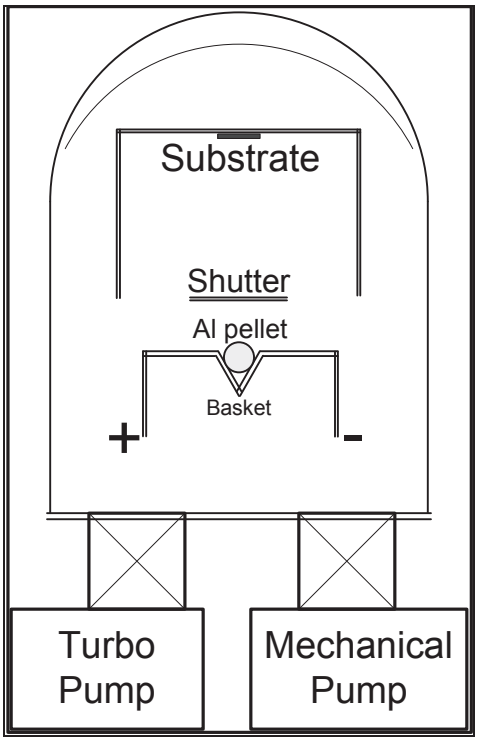

Figure 3 - 3: Schematic diagram of the Edwards Auto 306thermal evaporation system

The deposition process is timed to get the desired thickness of aluminum. The deposition rate has been previously measured to be 13 nm/minute when the RF power is set to 150 Watts.

3.2.2.2 Thermal Evaporation

Edwards Auto 306 thermal evaporation system is used for thermally evaporating aluminum. Figure 3.3 shows the schematic diagram of the system. A mechanical pump and a turbo molecular pump are connected to the system to pump the chamber to a high vacuum of about 10^{-6} mTorr. The samples are attached to the substrate holder with screws to hold the samples facing down in the chamber. The bell jar is closed and the valves are opened to pump the chamber to the desired vacuum. Liquid nitrogen can be used to pump the chamber down quickly to reach the high vacuum. . The substrates are maintained at room temperature. The

aluminum source, which is 99.99% pure, is placed in a tungsten filament connected to two electrodes. A current of 0.6 amps to 0.8 amps is passed through the filament. This causes the filament to heat up and melt the aluminum pellet. At some point the aluminum starts to evaporate from the molten pellet and is deposited on the substrate in the form of a layer. A crystal thickness monitor is used to measure the thickness of the deposited aluminum films.

3.3 Annealing

Samples are then annealed in a thermal annealing system MPZ5. MPZ5 doesn't have a gate valve. It is open to the ITZ. Two tungsten filament lamps are used to heat the substrate. The temperature set in the temperature controller is not the actual temperature of the substrate. The calibration of temperature controller was done by Dr. Husam Abu-Safe for his research. Figure 3.4 shows the relation between the temperature controller value and the actual temperature of the substrate. The samples are transferred to MPZ5 with the robotic arm from ITZ. To maintain high vacuum, the roughing valve for ITZ is closed and gate valve of MPZ4 is opened to use the turbo molecular pump connected to MPZ4. It takes around 20 to 30 minutes for the substrate temperature to stabilize at 600ºC. The samples in this study have been annealed at 600ºC at high vacuum for 8 hours. After the temperature of the substrate drops down to the room temperature, the substrate holder is programmed to deliver the substrate to home chamber.

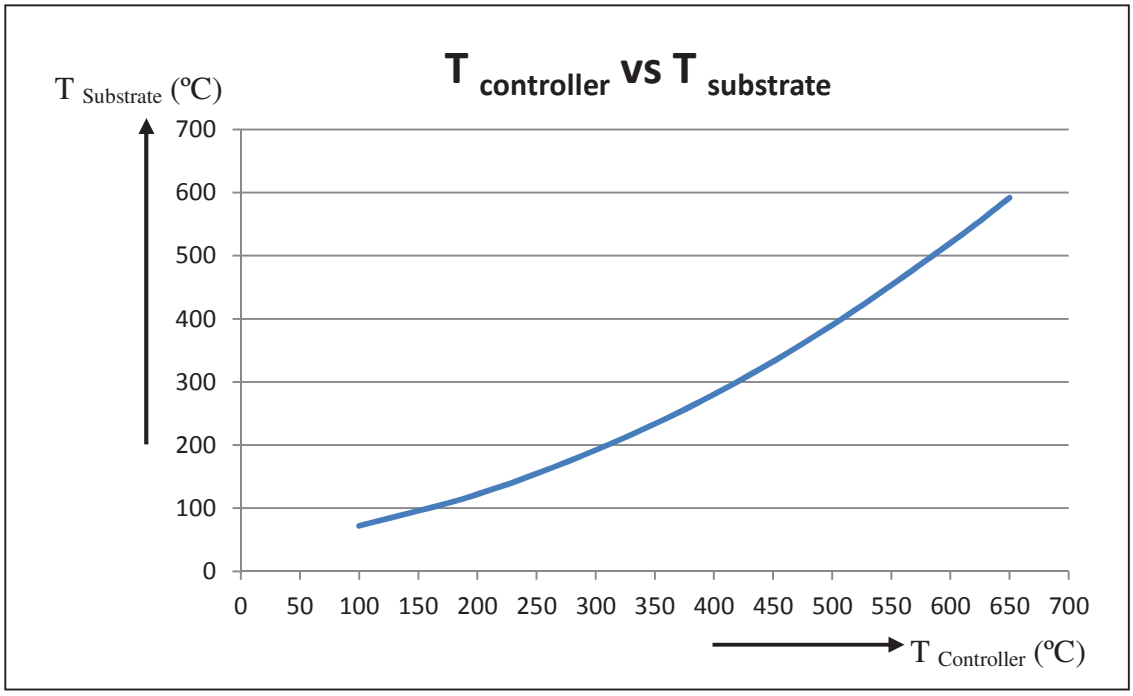

Figure 3 - 4: Graph showing the relation between the controller setting and the actual substrate temperature.

3.4 Thermal Oxidation

The silicon dioxide (SiO_2) is one of the most common insulators used in the semiconductor technology [37]. The thin layer of native oxide always grows on a silicon surface even at room temperature, as long as there is an oxidizing ambient. The thickness of the native oxide is very small and the native oxide formation is a self-limiting process [38]. Thick silicon dioxide layer is grown on a silicon wafer through a process called thermal oxidation. Thermal oxidation is a technique that uses high temperatures to promote the growth rate of oxide layers. In the thermal oxidation process, the silicon substrate is exposed to an oxidizing agent like oxygen or steam at high temperatures, producing thick oxide films.

Thermal oxidation is done in a high temperature oxidation furnace or a diffusion furnace. Figure 3.5 shows a sketch of a thermal oxidation furnace. Silicon wafers are heated to a high temperature in a long furnace in an oxidizing ambient. A furnace typically consists of a cabinet, a quartz process tube, a heating system, a temperature measurement and control system, a loading system for loading and unloading wafers, a system for introducing the process gases in and out of the quartz tubes.

The wafers are placed in a quartz boat, which is loaded into the heated quartz process tube. The oxidizing gas then enters the process tube from the source end, subsequently oxidizing the wafers. Depending on which oxidizing gas, the thermal oxidation may either be in the form of dry oxidation (with oxygen gas) or wet oxidation (with steam). The reactions for dry and wet oxidation are given by the following equations: [39]

1. For dry oxidation: $Si + O_2 \longrightarrow SiO_2$
2. For wet oxidation: $Si + 2H_2O \longrightarrow SiO_2 + 2H_2$

During dry oxidation, the silicon wafer reacts with the ambient oxygen, forming a thin layer of silicon dioxide on its surface. In wet oxidation, steam is introduced into the chamber where it reacts with the silicon to produce the oxide and hydrogen gas. These oxidation reactions occur at the $Si\text{-}SiO_2$ interface. Silicon at the interface is consumed as oxidation takes place. As the process continues the $Si\text{-}SiO_2$ interface moves into the silicon substrate. Oxide growth rate depends on temperature, pressure and time of the process. Oxide growth rate is directly proportional to the oxidation time, temperature and pressure.

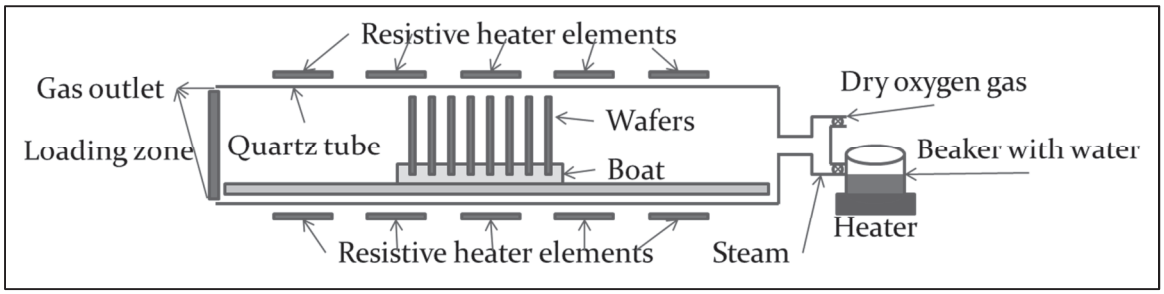

Figure 3 - 5: Model of a thermal oxidation furnace

3.5 Analytical Techniques

3.5.1 Scanning Electron Microscopy

A Scanning Electron Microscopy (SEM) is a microscope that uses electrons instead of light to form an image. An electron gun produces an electron beam and accelerates it to energies between 2 keV to 40 keV. Two or three electromagnetic lenses de-magnify the electron beam until it reaches a diameter of 2-10 nm before it hits the specimen. When this beam of electrons hits the surface of the film, secondary electrons are ejected which are then collected and analyzed to obtain information and an image of the surface. The electron beam is scanned across the specimen by the scan coils, while a detector counts the number of low energy secondary electrons. Fig 3.6 shows a schematic view of a standard scanning electron microscope.

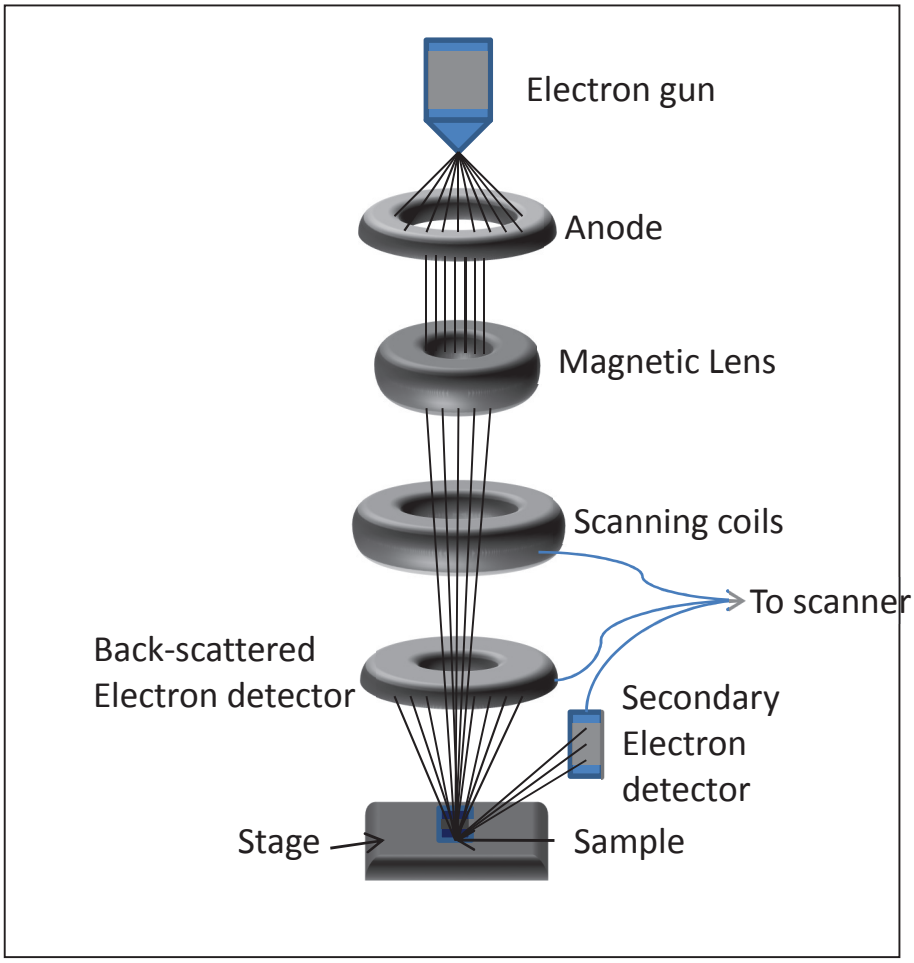

Figure 3 - 6: Schematic view of a standard SEM

3.5.2 Energy Dispersive X-ray spectroscopy (EDX)

When the primary electrons, sent by the electron gun in the SEM, interact with the specimen, the energy of these electrons can be transferred to the specimen by several processes. One of these processes is the emission of X-rays. Each element emits X-rays of a certain wavelength that is characteristic of the material of the specimen. Collection and analysis of these rays can help in determining the elemental composition of the specimen.

The characteristic X-ray of an element is produced when a vacancy in the inner shells of an atom is filled by an electron falling from one of the outer shells. The vacancy in the inner

shell can be created by a high energy beam electron or secondary electrons that can knock one of the inner shell electrons out of its orbit. All elements, except for few of the small atomic number elements, produce characteristic X-rays that have energies proportional to their atomic number, Z. An element may have characteristic X-rays of different energies, depending on how they are emitted. X-rays may be emitted by an electron falling from L shell to the K shell or from M shell to the L shell. They can also be emitted by the falling of an electron from M shell to K shell. Therefore physics adopted the nomenclature K_α, K_β etc. to denote the different characteristic X-rays of an element. K_α is the X-ray emitted when an electron from the L shell falls into a vacancy in the K shell. K_β is the X-ray emitted when an electron from the M shell falls into a vacancy in the K shell. K_α X-rays are more probable to be emitted that K_β especially in low atomic number atoms. In the current work we will be only interested in the characteristic K_α X-rays of silicon, aluminum and oxygen.

Although EDX is generally known to be a technique to analyze and examine specimen surfaces, the X-rays produced during the specimen-electron beam interaction do not quite come from the surface region. When the electron beam falls onto the specimen surface, it penetrates to regions deep inside the specimen. The depth of penetration depends on two major factors; 1) the atomic number (Z) of the element (lower the Z, deeper the penetration) and 2) the energy of the primary electrons (higher the energy, deeper the penetration. The penetrating electrons create a bulb-shaped interaction volume that may extend to several microns inside the specimen. Figure 3.7 shows the volume of interaction of the EDX in a sample.

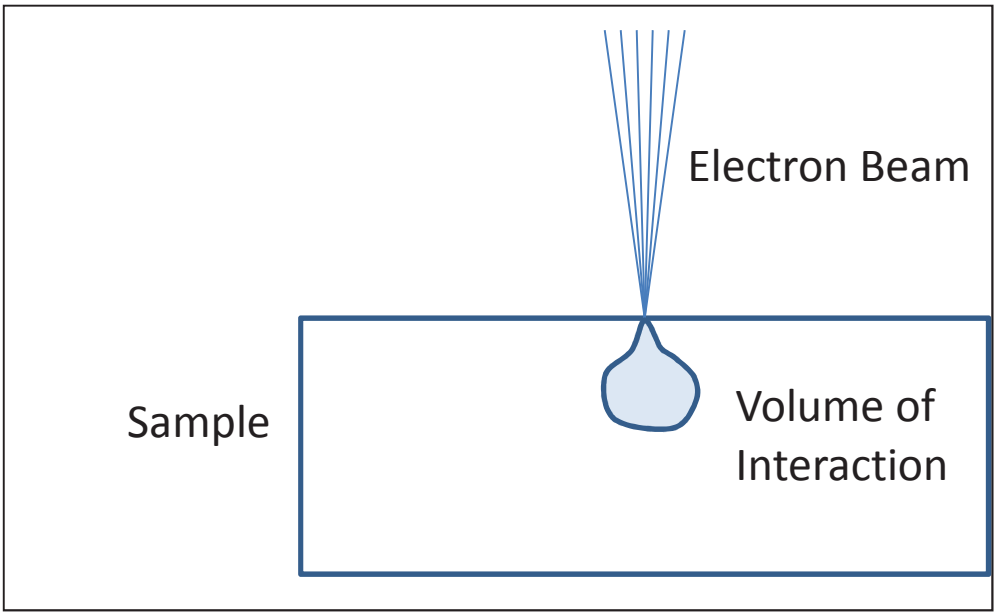

Figure 3 - 7: Figure showing the volume of interaction of the EDX in a sample

3.5.3 Focused Ion Beam (FIB)

Focused ion beam systems operate in a similar fashion to a scanning electron microscope. FIB systems use a finely focused beam of gallium ions. These ions can be operated either at low beam currents or high beam currents depending on the purpose. Low beam currents are generally used for imaging purposes, while high beam currents are used for sputtering or milling [40]. When gallium (Ga^{+}) primary ion beam hits the sample surface, a small amount of material is sputtered. Because of this, secondary ions are released from the surface. The primary beam also produces secondary electrons. These sputtered ions are collected to form an image as the primary beam scans the sample surface. At low primary beam currents, very little material from the sample surface is sputtered. At higher primary beam currents, a large amount of material can be removed from the surface, allowing precision milling of the sample down to a sub-micron scale. Figure 3.8 shows a schematic view of the FIB process.

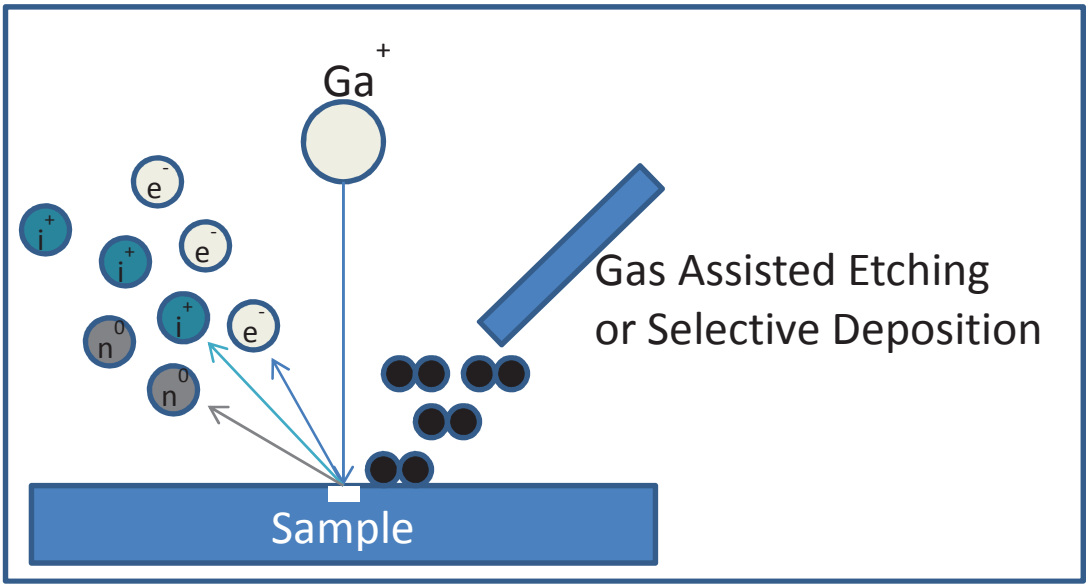

Figure 3 - 8: Figure showing the volume of interaction of the EDX in a sample

If the sample is non-conductive, a low energy electron flood gun is used to provide charge neutralization. Unlike SEM, where a thin conductive surface coating is required to scan an insulating region, in a FIB positive secondary ions can be analyzed to get a clear image of highly insulating samples. In addition to primary ion beam sputtering, FIB can also be used to deposit metals on the samples with a variety of gases. These gases can either interact with the primary beam to provide selective gas assisted chemical etching or selective deposition.

CHAPTER 4: RESULTS AND DISCUSSION

4.1: Introduction

In this chapter, results on the fabrication of horizontal silicon nanowires using aluminum as a catalyst are presented. The interaction between aluminum and silicon results in different kinds of structures like nano-platelets, nanorods and nanowires, depending of the growth parameters. In this research, main emphasis was given to the growth of horizontal silicon nanowires on a silicon substrate using a thin aluminum film as a catalyst. In the course of experiments, different nano structures were observed by changing the parameters. For example, a jungle of vertical nanowires can be grown by annealing a thin layer of aluminum deposited by sputtering system on a silicon substrate. Similarly, a network of horizontal silicon nanowires can be grown by annealing a thin layer of aluminum deposited by evaporation system on a silicon substrate.

A (100) oriented silicon wafer was used as the substrate. The nominal thickness of the aluminum layer used was 40 nm. The source of silicon to grow the nanowires is the substrate itself. Samples were annealed at different annealing times to study the growth process of the horizontal silicon nanowires. The experiments were carried out in two phases. In the first phase, silicon nanowires were grown on a clean silicon substrate. In the second phase, silicon nanowires were grown on an insulating layer. A model of a nano device has also been introduced based on the results.

The main goal in doing this research was to build a nanodevice with an array of horizontally grown silicon nanowires across an insulator connecting two regions: source and drain. Figure 4.1 shows the basic model of a nanodevice. If a gate metal is introduced to induce a conducting channel between source and drain regions, a simple switch can be fabricated from the nanodevice.

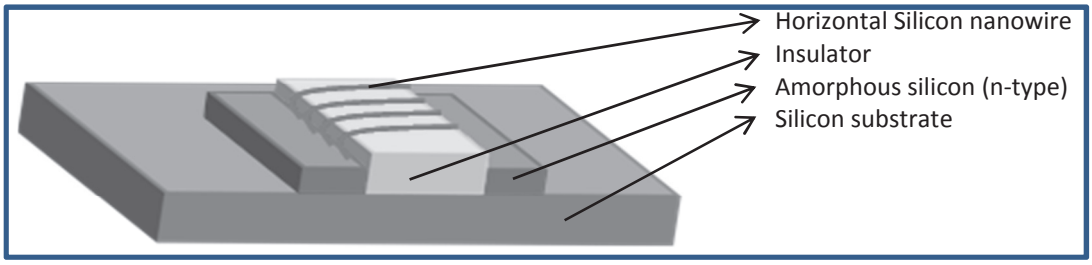

Figure 4 - 1: Model of a nanodevice with an array of horizontal silicon nanowires connecting two regions

In the past decade of integrated circuit device fabrication, aluminum was considered as the most common metal for the interconnections in the semiconductor technology. Aluminum is the third most abundant element on Earth. There are many advantages of aluminum. It is relatively cheaper, it has good conductivity and it is relatively inert. Because of this dependency on aluminum, it becomes difficult to form an ohmic contact to moderately doped n type silicon. Aluminum forms an ohmic contact easily on p type silicon and heavily doped n type region. Even then aluminum has many problems. One of the most severe problems is the “junction spiking”. This problem becomes severe as the device dimensions are reduced, i.e. if the contacts become smaller and junction depth is too shallow.

Let us consider a simple p-n junction. Figure 4.2 shows a cross sectional view of a simple p-n junction. Let's suppose aluminum is in contact with the p-type region.

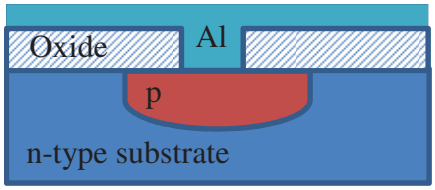

Figure 4 - 2: Cross sectional view of a simple pn junction

In order to form a good ohmic contact, the substrate should be annealed at a high temperature. Usually 450°C is chosen to be the most common annealing temperature to form a good ohmic contact. From the aluminum – silicon phase diagram, at 450°C, aluminum dissolves 0.5 weight % of silicon. If the aluminum deposited is in its purest form, then it dissolves the silicon from the substrate. If the junction is too shallow, there is more risk of spiking. If the contact window is too small, aluminum goes vertically down, shorting the p-type and the n-type regions.

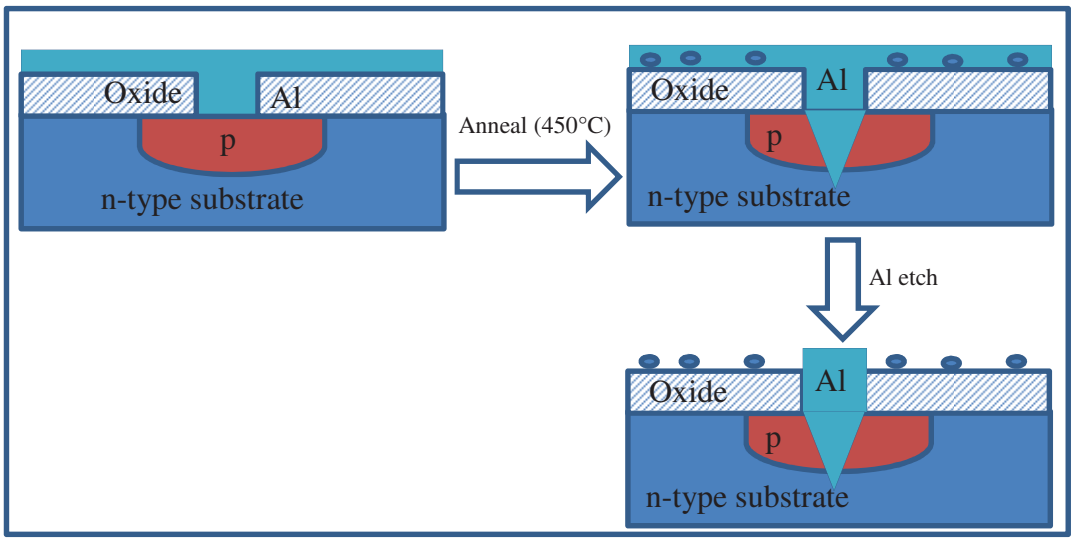

Figure 4 - 3: Cross section view of the annealing process and the aluminum spiking in silicon

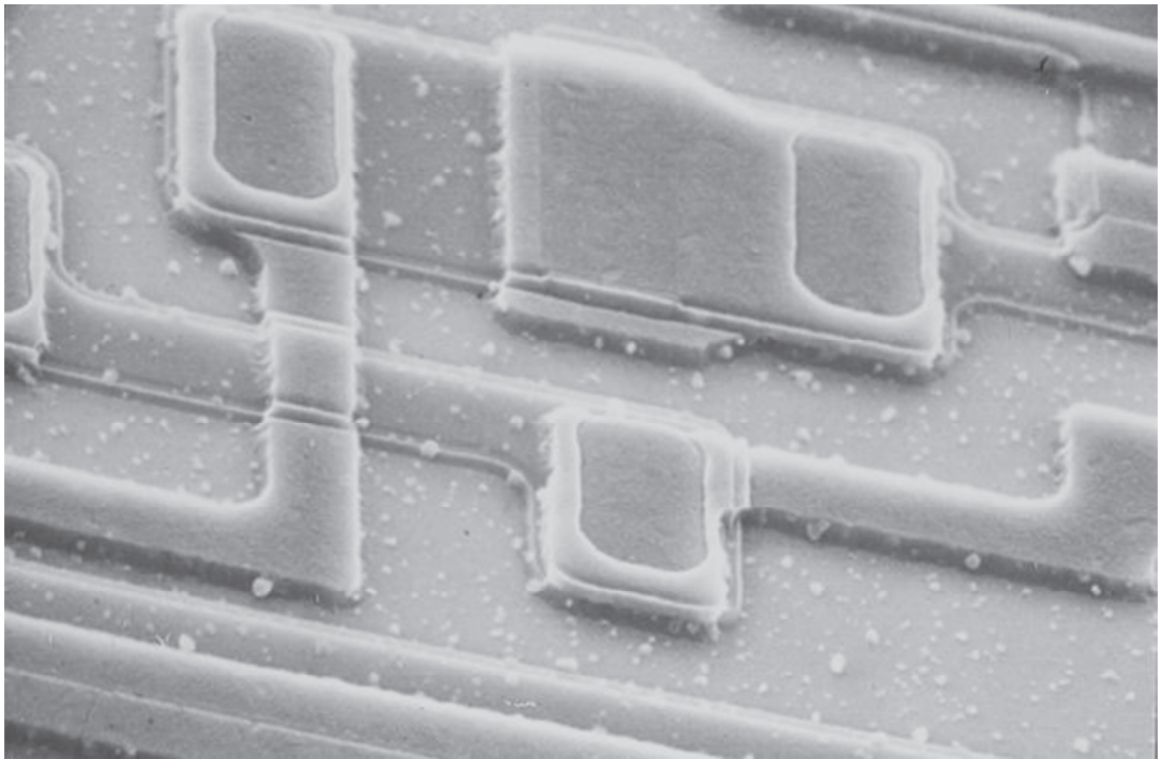

Figure 4 - 4: Photo courtesy HP. SEM image showing the silicon crystals on the surface when the unwanted aluminum is etched away.

When aluminum diffuses into the substrate, silicon diffuses through the aluminum and precipitates in the aluminum layer. There will be a two way diffusion of aluminum and silicon through the annealing process. As the aluminum gets deeper and deeper into the substrate, an equal amount of silicon diffuses through the aluminum layer. When the unwanted aluminum is etched away, silicon crystal precipitates are left on the substrate. Figure 4.4 shows a SEM image of a sample from HP, showing the silicon crystal precipitates on the substrates after the unwanted aluminum was etched from the substrate.

Because of the high diffusivity of silicon in aluminum, the silicon is picked from one place and is deposited at another place. This happens when the thickness of aluminum is in the order of several microns. If we can use this concept of picking up the silicon from one place and

depositing at a desired place to form a nanowire or an array of nanowires, we can easily fabricate nanodevices. In order to achieve the goal, this research is categorized into two phases.

- Phase 1: To grow a network of horizontal silicon nanowires on a bare clean silicon substrate, using aluminum as a catalyst.
- Phase 2: To grow a network of horizontal silicon nanowires on an insulator region connecting two regions on the substrate, using aluminum as a catalyst.

4.1.1 Phase 1: Horizontal silicon nanowires on a silicon substrate

When the thickness of deposited aluminum layer is of several microns, silicon diffuses through the aluminum layer and precipitates likes balls on the substrate. If the thickness of aluminum layer is reduced to the order of several nanometers, let us say less than 100 nm,silicon can easily diffuse all over the aluminum layer. As the thickness of aluminum layer is reduced, the grain size also reduces. This is because the grain size of aluminum is directly proportional to the thickness of aluminum layer. Diego Chaverri from University National, Costa Rica, found that the grain size of aluminum is dependent on the thickness of the film above 25 nm. According to the results, the relation between average grain size and thickness (in nm) of aluminum is given by:

$$D_g = 0.1267D + 22.308 \text{ [15]}$$

Where D_g is the average grain size of aluminum and D is the thickness of the aluminum film. The grain size of the aluminum is almost equal to the thickness of the aluminum layer below 25 nm. If the thickness of aluminum is more than 25 nm, then the grain size will be less than the film thickness.

When a silicon substrate with a thin layer of aluminum film is annealed, the grains coalesce with each other and form larger grains [9]. This is called the grain boundary diffusion [8]. The aluminum grains arrange themselves such that the grain boundaries form tripoints. A tripoint is a point at which the boundaries of three grains meet. Because of the rise in temperature, there will be a thermal coefficient mismatch between aluminum and silicon. The coefficient of thermal expansions of aluminum and silicon are $24x10^{-6}$/K and $2.6x10^{-6}$/K [11], respectively. So basically when the temperature rises, aluminum layer tries to spread out more as compared to the silicon substrate. As the annealing continues, the silicon from the substrate diffuses into the thin aluminum layer. The diffusion usually occurs from all over the substrate. But the diffusion occurs a lot faster from the tripoints. This is because of the stress build up at these tripoints, where the three grain boundaries meet. At these tripoints, since the diffusion is a lot faster, excess amounts of silicon is deposited at these tripoints. The excess silicon forms a shape of a mound.

As the temperature ramps up, a concentration gradient occurs near the aluminum-silicon interface. From the phase diagram of aluminum and silicon, at 450°C, 0.5wt% of silicon is soluble in aluminum. At this temperature, silicon starts diffusing into the aluminum layer, creating a void in the substrate. Consequently, aluminum diffuses into the substrate filling the voids. Moreover, the diffusion rate of silicon through the aluminum grain boundaries is more than the diffusion rate of silicon through the aluminum grains itself. This is because the aluminum grain boundaries are like defects between the grains. The resistance for the diffusion of silicon through the grain boundaries is less. When the diffusion starts, the silicon quickly diffuses through the aluminum grain boundaries, “decorating” the aluminum grain boundaries.

When sufficient silicon diffuses through the aluminum layer, it precipitates along the aluminum grain boundaries in the form of a silicon nanowire.

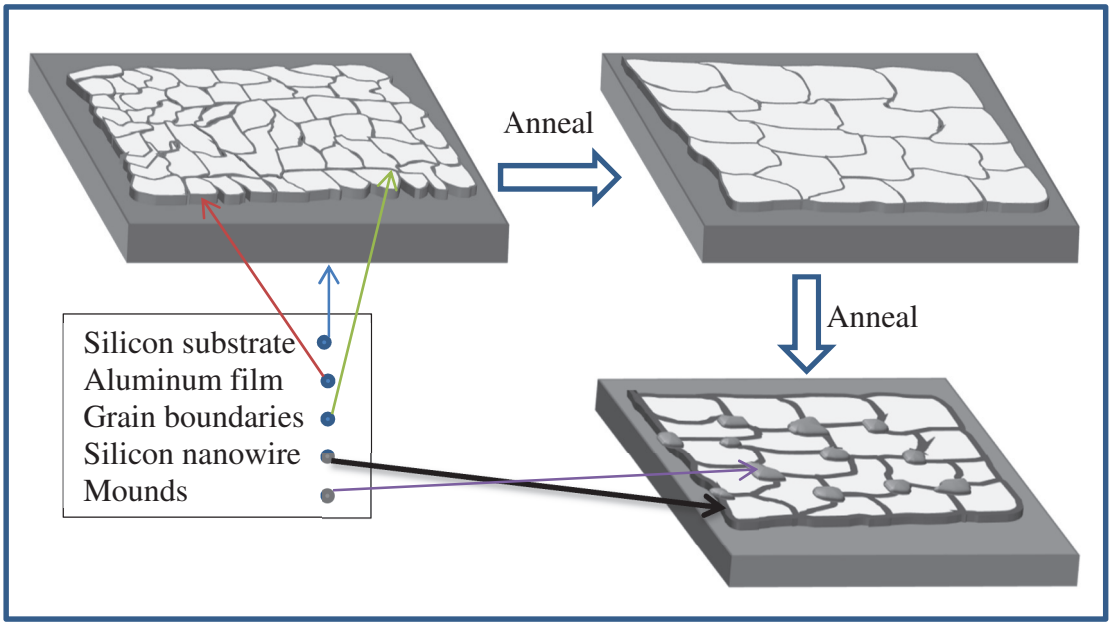

Figure 4 - 5: Process showing the fabrication of horizontal silicon nanowires on a silicon substrate

4.1.2 Phase 2: Horizontal silicon nanowires on an insulator

With phase 1, horizontal silicon nanowires can be grown on top of a silicon substrate. But all the silicon nanowires are in a closed network attached to the substrate. In short, all the horizontal silicon nanowires are shorted. A nanodevice cannot be fabricated in such process. To fabricate a nanodevice, the silicon nanowires have to be fabricated on an insulator with the two ends connected to the substrate. In that manner, the silicon nanowire is no more shorted to the substrate. The one possible way is to use the process in phase 1 to grow an array of horizontal silicon nanowires on top of an insulator.

During the aluminum grain boundary diffusion, the grain size of aluminum can increase from several nanometers to several micrometers. Let us suppose the average grain diameter of aluminum after the annealing increases to 5 µm. If the width of the insulator layer is maintained less the average grain diameter, then we can grow an array of horizontal silicon nanowires across the insulator connecting the two regions on either side of the insulator. Figure 4-6 shows the process flow for phase 2.

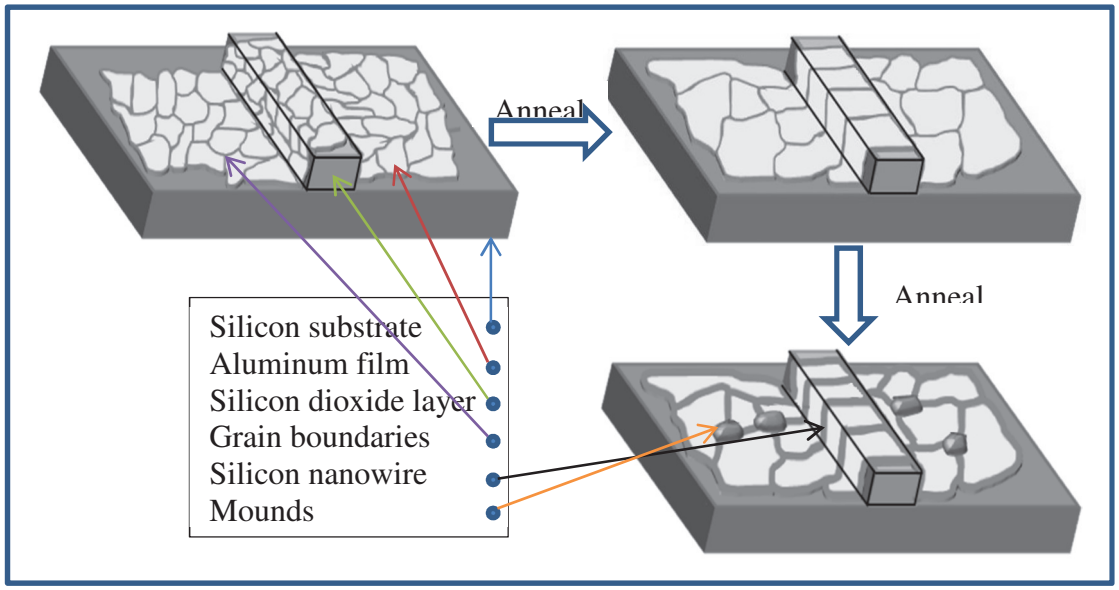

Figure 4 - 6: Process showing the fabrication of horizontal silicon nanowires on an insulator

From the figure 4-6, if the width of the oxide layer is less than the average grain size diameter, nanowires can be grown across the insulator layer.

The insulator can be either silicon dioxide or silicon nitride. Photolithography techniques can be used to pattern the oxide layer. The coefficient of thermal expansions of aluminum, silicon and silicon dioxide are 24×10^{-6}/K, 2.6×10^{-6}/K and 0.5×10^{-6}/K [11], respectively. When the temperature rises, aluminum layer tries to expand when compared to the silicon substrate and the silicon dioxide. Because of this coefficient mismatch, there exists a lot of stress near the edge of

the oxide layer. This site serves as the main source of silicon from the substrate. Most of the silicon that diffuses on top of the oxide layer is taken from the edge of the oxide layer.

As the temperature rises, there will be concentration gradient of silicon in the aluminum layer. So silicon starts diffusing from the substrate on top of the oxide layer through the thin aluminum layer. Consequently, many spikes will be observed around the edge of the oxide layer. Since it is a two way process, i.e. as the silicon diffuses on top of the oxide layer, aluminum diffuses into the substrate. On the silicon substrate where aluminum is in contact, similar results can be expected as in phase 1.

4.2 Horizontal Silicon Nanowires on a silicon substrate

To study the growth of horizontal silicon nanowires on a silicon substrate, a series of experiments were designed to optimize the growth the nanowires. In the first set of experiments, pure aluminum is deposited on silicon substrates with the sputtering system and annealed at 600ºC for 8 hours. This way no horizontal silicon nanowires were observed on the substrates. Instead vertical silicon nanowires and platelets were observed. In the following experiments, aluminum was deposited using evaporation system. After annealing the substrate, horizontal silicon nanowires were observed on the substrate. Different thicknesses of aluminum were evaporated on the samples to find an optimum thickness of aluminum layer sufficient to grow a network of horizontal silicon nanowires. Time study was conducted to examine the growth of horizontal silicon nanowires as the annealing time progresses. The annealing of the substrates was stopped at certain intervals and observed to study the growth of horizontal silicon nanowires.

In the first two experiments, a silicon sample is cut from a (100) oriented five inch silicon wafer. All the samples were cleaned to remove the native oxide from these substrates. A Corning 7059 glass substrate is also included in these experiments, along with the silicon substrates. A thin layer of 40 nm aluminum is sputtered on the samples at 192ºC. Film deposition on heated substrates reduces the intrinsic tensile stress. Also the deposition onto heated substrates increases the film density, hardness and adherence [12]. The samples were then annealed in a high vacuum annealing system at 600ºC for 8 hours. Figures 4 – 7 shows the SEM images of the sample after annealing.

The samples from the first experiment were wiped with acetone before taking the SEM images. Normally this step is not suitable for these samples, because it will damage the features on the sample. From the figure 7, we can see broken wire like structures protruding from the mound kind of structures.

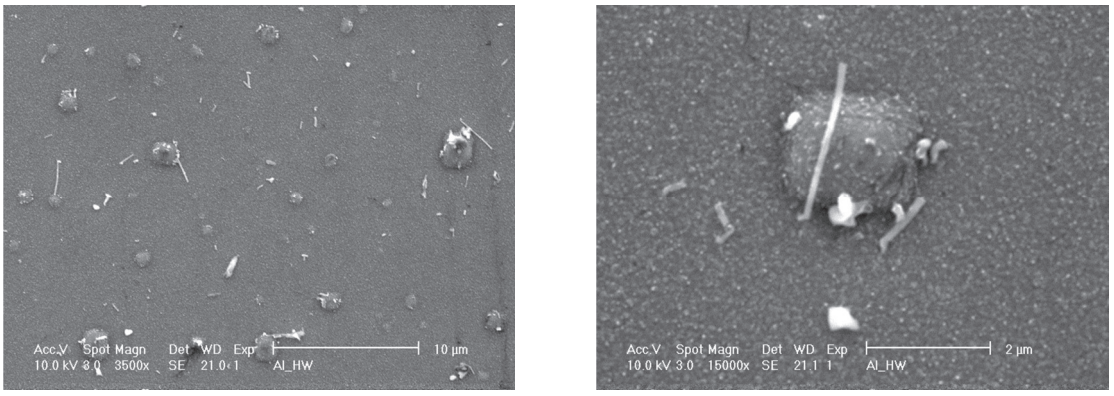

Figure 4 - 7: SEM images of the sample after 8 hours of annealing. The samples were wiped with acetone before taking the images.

The same experiment is repeated with another sample, following the same process as in the first experiment, except the substrate temperature was maintained at 40ºC. Figures 8 and 9

represent the SEM images of the silicon substrate and a corning 7059 glass substrate from experiment 2.

In the figures 8a and 8b, we can clearly see the formation of silicon nanowires. Unlike the VLS process to grow the vertical silicon nanowires, where silicon is introduced into the system in vapor phase (e.g. silane), no gas is introduced in these experiments. Instead the samples were maintained at a high vacuum pressure (10^{-7} Torr). From figure 8b, many nanodots were observed on the substrate. The nanowires are observed to be growing from these nanodots. When the length of the nanowire exceeds a certain limit, it breaks off and drops horizontal on the substrate. These nanowires were only observed in some patches on the silicon substrate (figures 8c and 8d). Figures 9a and 9b show the SEM images of a glass substrate from experiment 2. The glass substrate is included in this experiment to observe the behavior of aluminum with the temperature, assuming no interaction between the aluminum and the glass substrate.

From figure 9a we can observe that the aluminum is balling up to form a mound. This phenomenon was observed all over the glass substrate. The diameter of these mounds was measured to be ranging from hundreds of nanometers to 2 μm. The same mounds were observed on the silicon substrate as well. The silicon nanowire growth was only observed at some places (white patches) on the silicon substrate but not on the glass substrates as expected. Since the sputtering and annealing of the substrates were done under high vacuum, the substrates are free of any oxide formation.

The diffusivity of silicon in aluminum is very high at high temperatures. When the annealing temperature slowly rises to the eutectic temperature (577ºC), the silicon starts diffusing into the aluminum layer at much lower temperatures.

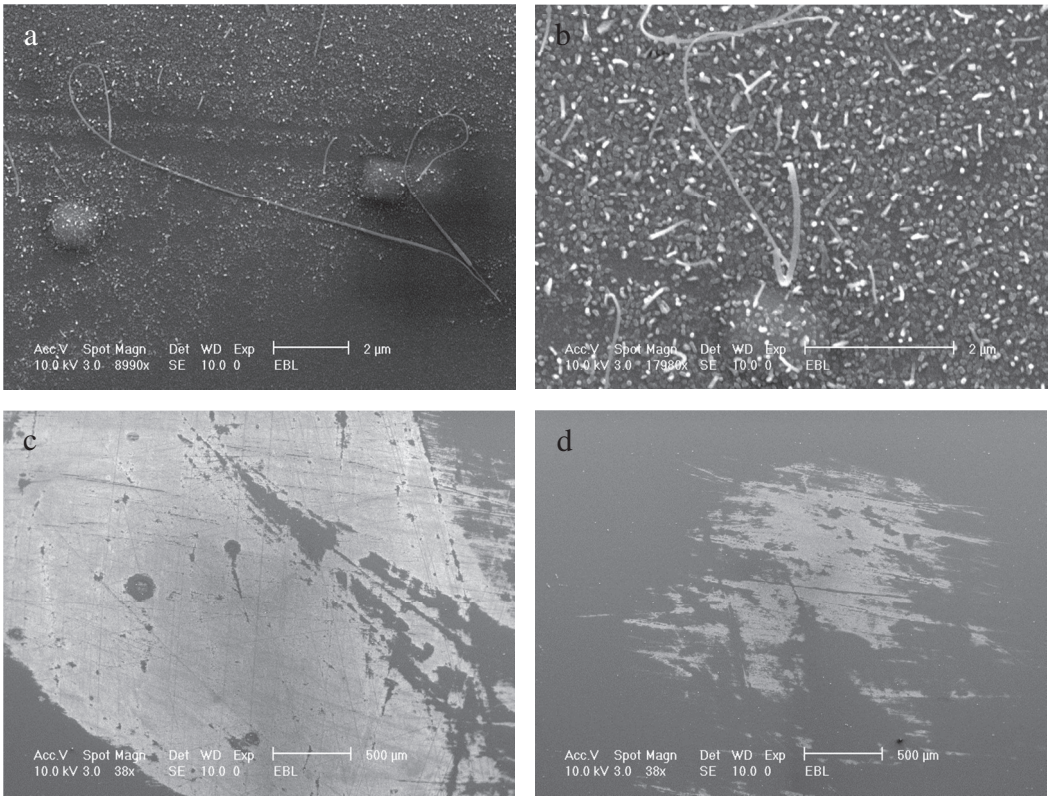

Figure 4 - 8: SEM images of a silicon substrate from experiment 2 after annealing

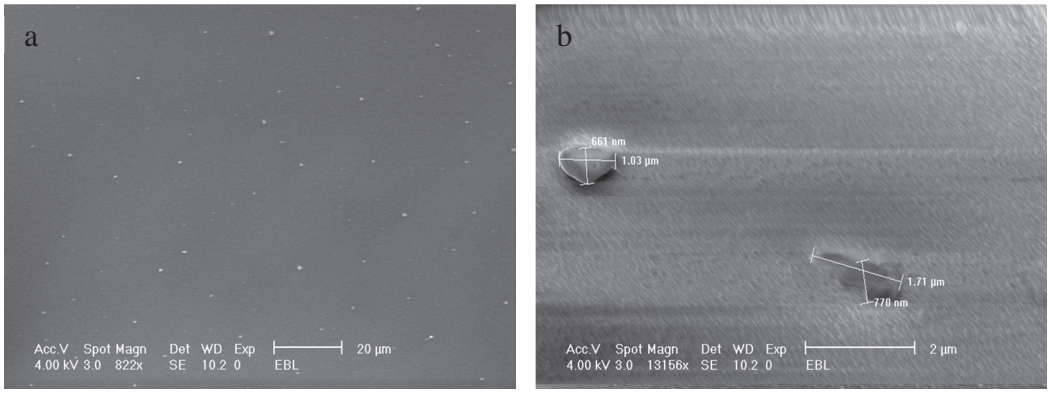

Figure 4 - 9: SEM images of a glass substrate from experiment 2 after annealing

During the diffusion, silicon leaves a void in the substrate. To fill the void, the aluminum gets deeper and deeper into the substrate. These sites act as a major source of silicon to diffuse into the aluminum layer.

The third experiment was concentrated on observing the effects of different native oxide thickness on the silicon substrates to the growth of silicon nanowires. In this experiment, five silicon samples were cut from a five inch silicon wafer. All the samples were treated with the three step chemical cleaning process described earlier in section 3.3.1, HF dip being the last step. The samples were not rinsed with DI water. Because of the HF dip, the samples are free from any native oxide.

When the hydrogen terminated (passivated) surface of crystalline silicon is exposed to atmosphere at room temperature, it reacts with oxygen to form a very thin silicon dioxide film. This film is called native oxide. This oxide film is essentially amorphous. On a crystalline silicon sample, thickness of the native oxide approaches approximately 5 nm after one year of exposure to atmosphere [20]. Some work done earlier at University of Arkansas by Marwan Albarghouti has shed light on the measurement of thickness of native oxide using a Fourier Transform Infrared Spectroscopy (FTIR) on a hydrogenated amorphous silicon layer. The thickness values were measured to be around 0 nm after 1 day, 0.5 nm after 5 days, and 0.9 nm after 9 days. Hydrogenated amorphous silicon layer is known to have its surface dangling bonds terminated by hydrogen atoms. This is why oxide growth on the hydrogenated amorphous silicon surface is slower than on a crystalline silicon surface. The growth of the native oxide layer is self-limiting because in order for the growth to continue, oxidizing radical atoms must penetrate through the oxide layer and reach the silicon surface to grow more oxide. So, as the thickness grows the rate of penetration of the oxidant molecules decreases and so does the growth of oxide layer [21].

The samples were treated with an HF dip to remove any native oxide and the first sample was labeled as “0 day”. The rest of the samples were left exposed to the ambient atmosphere.

Four samples were taken, one by one after 3, 5, 6 and 7 days respectively and were labeled as such. The number on each sample represents the number of days left exposed to the atmosphere to grow the native oxide layer. Each sample was introduced in the multi chamber PECVD system after the ambient atmosphere exposure. Figure 10 shows the SEM images of all the five samples. Thin hexagonal platelets were observed on all the samples. Similar research done by Richard F. Hill and Robert Danzer [22] explains that the formation of well-defined hexagonal shaped platelets is made of α-alumina. It was reported that after the calcination of an aqueous mixture of boehmite and hydrofluoric acid at temperatures as low as 1000ºC results in the formation of hexagonal shaped α-alumina platelets and the formation of aluminum fluoride promotes the growth of these platelets. In this experiment, the HF dip during the wafer cleaning process could be the possible reason for the growth of these hexagonal platelets. The reaction of aluminum layer with the remnants of HF acid on the substrate might have led to the formation of aluminum fluoride, which acts as a catalyst for the growth of these hexagonal alumina platelets.

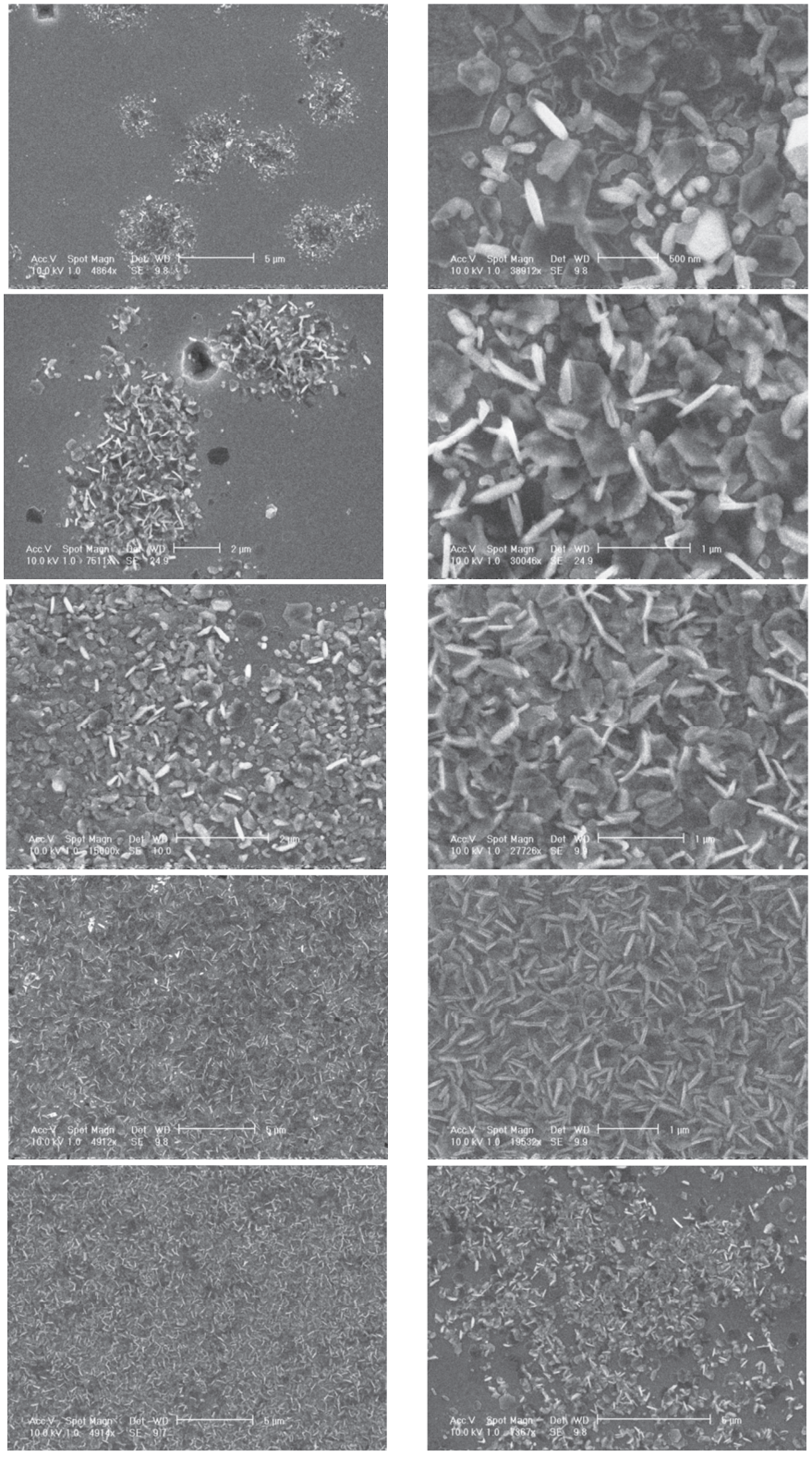

Figure 4 - 10: SEM images of the samples showing the platelet formation on the surfaces. (a, b)-0 days, (c, d)-3 days, (e, f)-5 days, (g, h)-6 days, (i, j)-7days.

4.2.1 Varying the thickness of aluminum layer

So far aluminum was deposited on the substrates using sputtering system. With this method, horizontal silicon nanowires were not observed on the substrate. In the following experiments, pure aluminum was evaporated on the substrates using an evaporation system. Three samples were cut from the same substrate and different thicknesses of aluminum (10 nm, 20 nm and 40 nm) were evaporated on each sample. The samples were annealed for 8 hours at 600°C. The samples were cooled to room temperature and the surface morphology was examined by SEM.

Figures 11(a) and 11(b) show the SEM images of a sample with 10 nm of aluminum layer. As we can observe after the annealing, not many mounds were observed on the surface of the substrate. Also the mounds were less than a micron diameter in size. On top of these mounds, we can observe some dendrite formations. These dendrites must be the silicon coming from the substrate. The formation of mounds can be explained from the pitting phenomenon. But due to the insufficient amount of aluminum, limited silicon can only diffuse from the substrate into the mounds. Many nanodots were also observed on the substrate. These nanodots can be the silicon diffusing through the aluminum layer. Apart from the mounds and the nanodots, many dark patches were also observed on the surface. These patches are the pits in the silicon substrate. Because of the insufficient amount of aluminum, the silicon just diffuses from the pits into the aluminum instead of forming a mound around the pit. Horizontal silicon nanowires were not observed on this substrate. The reason is due to the insufficient amount of aluminum present on the substrate.

Figures 11(c) and 11(d) show the SEM images of a sample with 20 nm of aluminum layer. As we can observe after the annealing, many mounds were observed on the surface of the substrate. These mounds were interconnected by a layer of crystalline silicon film diffused from the substrate on the surface. In this case, the thickness of aluminum film was sufficient enough for silicon from the substrate to diffuse into the aluminum layer. After the mounds are formed around the pitting region, the silicon diffuses through the aluminum layer to deposit along the grain boundaries. Because of the excess amount of silicon diffusing through the aluminum layer, it is deposited as a continuous film all over the surface. Only a limited number of horizontal silicon nanowires were observed on the substrate. Most of the silicon from the substrate is spread out on the surface, interconnecting the mounds.

Figures 11(e) and 11(f) show the SEM images of a sample with 40 nm of aluminum layer. As we can observe after the annealing, many mounds were observed on the substrate. Also, the silicon diffusing from the substrate is mostly confined around the dark aluminum spots. The excess silicon diffusing through the aluminum layer gets deposited along the aluminum grain boundaries in the form of a nanowire. This thickness of aluminum is optimum to grow the horizontal silicon nanowires on top of the substrate. From figure 11(f), we can observe the mounds interconnected by the horizontal silicon nanowires.

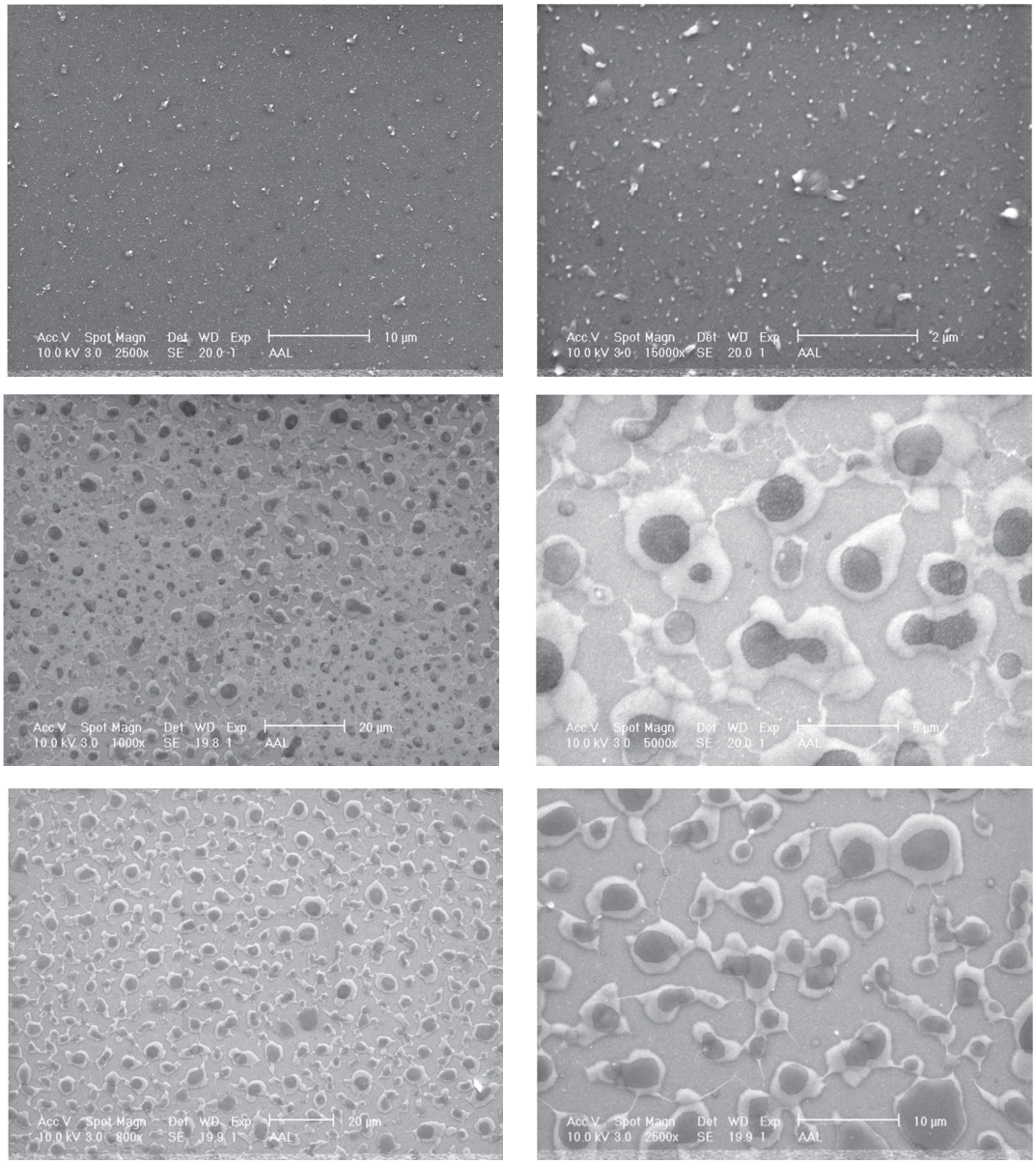

Figure 4 - 11: SEM images of the samples with different thicknesses of aluminum (a, b) – 10nm, (c, d) – 20nm, (e, f) – 40 nm.

4.2.2 Time Study of the nanowire growth

In order to better understand the growth mechanism of the horizontal silicon nanowires, the growth of nanowires was monitored as a function of time. Three samples were cut from the same substrate and 40 nm of aluminum was evaporated on each sample. The samples were then

annealed at 600ºC for 2, 4, 6, 8 and 10 hours. The samples were cooled to room temperature and then the surface morphology was examined by SEM.

4.2.2.1 Experiment 1:

Figure 12 shows the temperature profile for each sample. The samples were annealed for 2 hours, after which the annealing system was turned off and the samples were left to cool down to room temperature. After the samples reach the room temperature, one sample is taken out and stored in a storage box and labeled as "2hr". The other samples were transferred to the annealing system and heated to 600ºC for another 2 hours. The samples are again cooled down to the room temperature and a second sample is taken out and stored in a storage box, labeled as "2+2hr". The last sample is transferred into the UHV annealing system and heated to 600ºC for another 2 hours. This sample was cooled down to room temperature and stored in a storage box, labeled as "2+2+2hr". The samples were also dipped in an aluminum etchant, to remove the thin aluminum layer from the surface. All the three samples were examined with a SEM to study the surface morphology.

In this experiment, the growth of the nanowires was not observed. But instead, we can observe the formation of the mounds. These mounds are the sites where the silicon starts to diffuse from the substrate into the aluminum layer. These sites correspond to the tripoints in the aluminum layer. During the annealing process, aluminum film expands. This results in a compressional stress at the tripoints. In figure 13(a), after 2 hours of annealing, we can observe several mounds of sizes ranging from 1 μm to 5 μm. Figure 13(b) shows the SEM image of the same sample after the aluminum is etched from the surface.

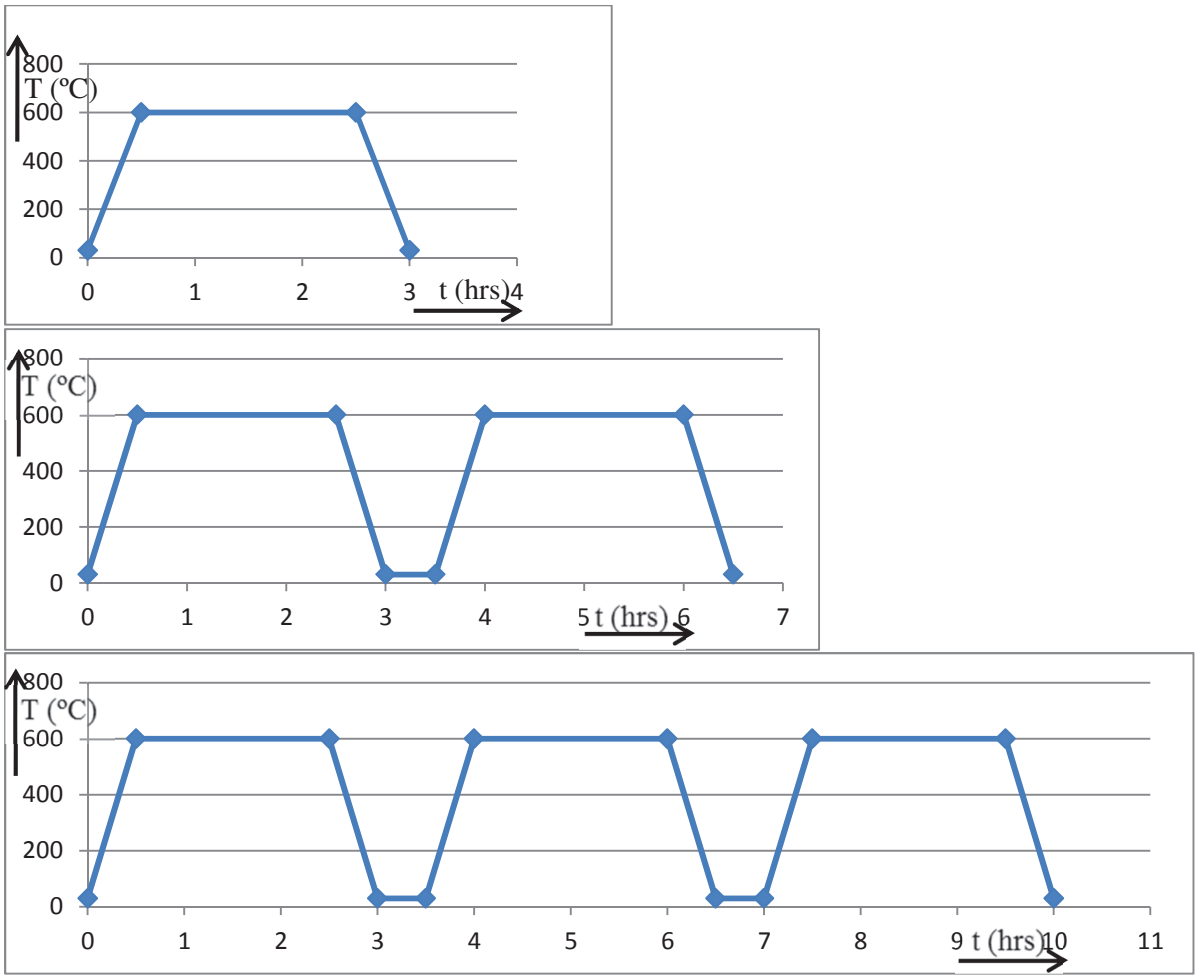

Figure 4 - 12: Temperature profiles for each sample annealed for 2, 4 and 6 hours

In this image, we can observe pits on the surface at the same sites where we had observed the mounds. The pits were also the same size as that of the mounds, ranging from 1 µm to 5 µm. At this point, the silicon starts to diffuse into the aluminum layer. As the annealing continues, the silicon diffuses through the aluminum layer starting from these points. Figure 13(c) shows the SEM image of a sample which is annealed for another 2 hours after the sample is cooled down. The top view of this sample with the aluminum layer is almost the same as the sample from figure 13(a).

When the aluminum layer is etched from the surface of the sample, we can observe many smaller pits on the surface apart from the big pits observed in figure 13(b). This can be explained based on the nature of aluminum. When the aluminum was evaporated on the substrate, it was 99.99% pure. But after 2 hours of annealing, silicon from the substrate diffuses into the aluminum layer. After the substrate is cooled down, a small percentage of silicon settles in the aluminum layer.

When annealing starts, the silicon diffusing into the aluminum layer will be less, because of the small percentage of silicon which has already diffused into aluminum, during the first 2 hours of annealing. This creates the small pits on the substrate. The samples are cooled again to the room temperature and annealed for another 2 hours. Figures 13(e) and 13(f) show the SEM images of the samples (with aluminum and without aluminum) labeled as “2+2+2 hours”. We can observe here that figure 13(e) is almost the same as the figures 13(a) and 13(c). After the first 2 hours of annealing, the top surface seems to be not affected. The only change is occurring at the interface of the aluminum layer and the substrate. From figure 13(f), we can observe many smaller pits on the substrate. The number of these smaller pits is more that the number observed in the figure 13(d). The same explanation as in the previous sample goes for this sample also.

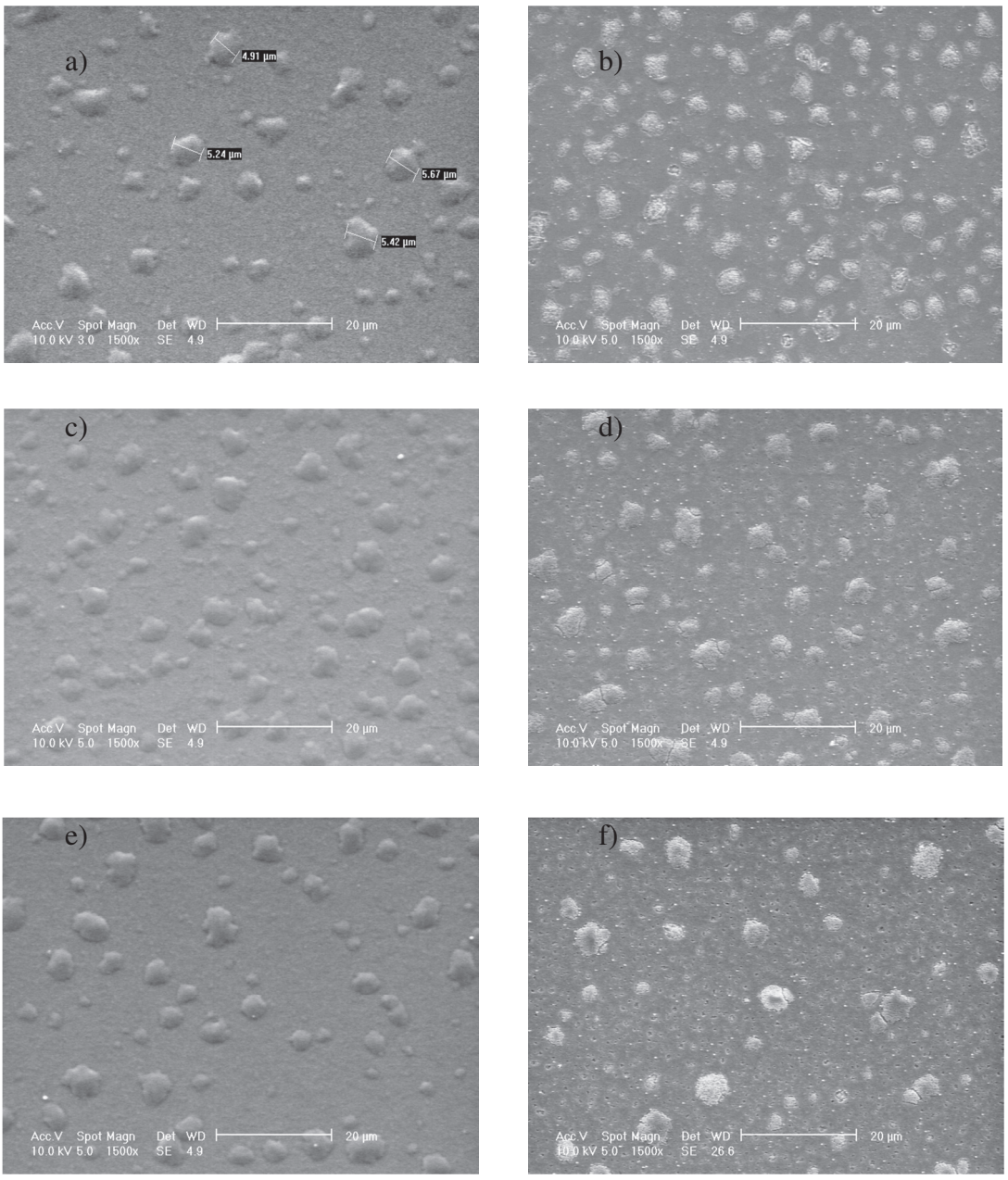

Figure 4 - 13: SEM images of the samples (a, b) annealed for 2 hours, (c, d) annealed for 2 hours, cooled and then annealed for another 2 hours, (e, f) annealed for 2 hours, cooled and annealed for 2 hours, cooled and annealed for another 2 hours.

4.2.2.2 Experiment 2:

In this experiment, three samples were diced from a single silicon wafer. These samples were cleaned with piranha etch, followed by a RCA clean and a HF dip. This ensures that the surfaces of the samples are hydrogen terminated and are free of any native oxide. Forty nanometers of aluminum is thermally evaporated on the samples at the same time. These samples were introduced into the Ultra High Vacuum (UHV) annealing system, which is already maintained at 600ºC. Each sample was introduced in the annealing system one at a time. The first sample was annealed for 2 hours, second sample for 4 hours, and the third sample for 6 hours. After the annealing, the samples were cooled down to room temperature. Half of each sample is dipped in aluminum etchant until the aluminum layer dissolves.

In figure 14(a), some mounds were observed on top of the substrate after 2 hours of annealing. The same results were observed in the first part of the previous experiment. Figure 14(b) shows the same sample after the aluminum was etched from the surface. After the aluminum was etched away, many pits were observed on the surface. The pits were observed in the same locations where the mounds were observed. These are the sites where the silicon starts to diffuse from the substrate into the aluminum layer.

Figure 14(c) shows the SEM image of a sample after 4 hours of annealing at 600°C. Figure 14(d) shows the SEM image of the same sample after the aluminum is etched from the surface. From figure 14(c), it is observed that the mound size is increased when compared to the mounds from figure 14(a). This shows that the silicon was etched from the substrate continuously such that an island of silicon is formed around the etch

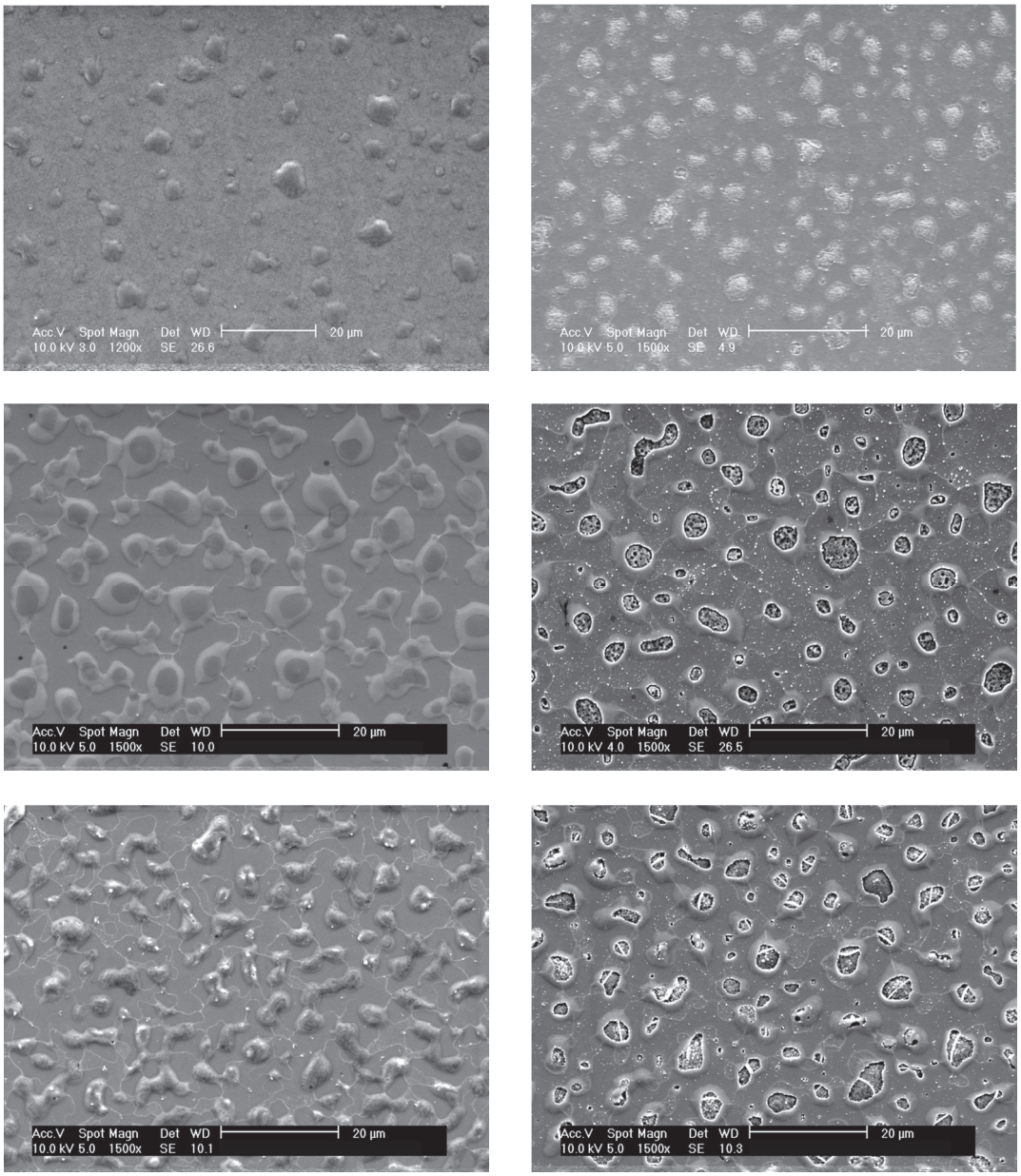

Figure 4 - 14: SEM images of the samples (a, b) annealed for 2 hours, (c, d) annealed for 4 hours, (e, f) annealed for 6 hours.

site. This is very clear from figure 14(d), which shows a crater formation in the center of the islands. The dark regions from the figure 14(c) are rich in aluminum. Therefore only the darker regions were etched away after the aluminum etching. Apart from the islands, nanowire structures were observed on the substrate. The regions on the substrate show a little roughness

which implies that as the aluminum was etched from the surface, some silicon crystallites were left on the substrate. This implies that the silicon was diffusing through the aluminum layer.

Figure 14(e) shows the SEM image of a sample annealed at 600 °C for 6 hours. Figure 14(e) shows the same island formation that was observed from sample after annealing for 4 hours. Web like nanowire structures were also observed on the substrate interconnecting the islands. The aluminum gets deeper and deeper into the substrate and the silicon diffuses out of the substrate, diffusing through the aluminum layer and depositing along the grain boundaries of aluminum. Figure 14(f) shows the SEM image of the same sample after the aluminum is etched from the surface. This shows the same crater formation as observed in the figure 14(d). Also the nanowire formation in the figure 14(f) is very prominent as compared with figure 14(d).

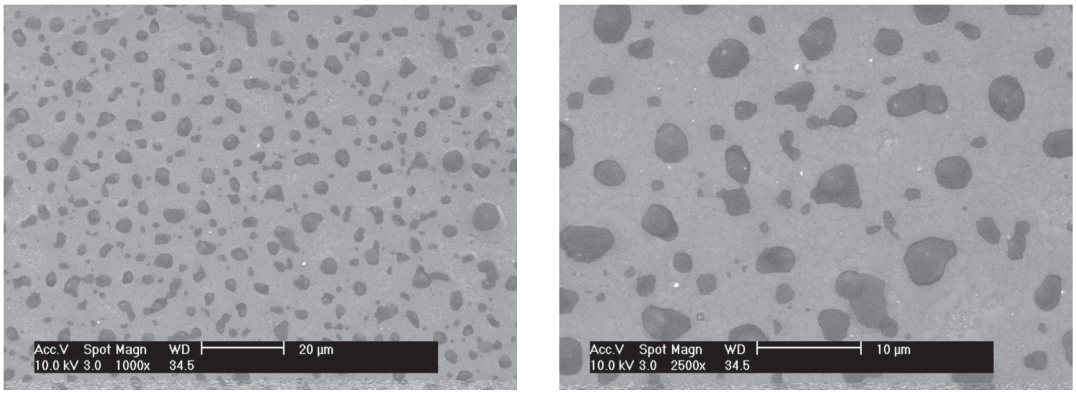

Figure 4 - 15: SEM image of a sample annealed for 10 hours

Figure 15(a, b) shows the SEM image of a sample annealed at 600ºC for 10 hours. In this figure, we can observe black spots distributed all over the surface. These black spots bear a resemblance to the same black spots that were observed in figure 14(c) and 14(e). From these figures we can also observe that the mounds observed in figure 15, coalesced with each other to form a continuous layer like structure. This is because of the excess amount of silicon being diffused into the aluminum layer. These black spots are rich in aluminum and are the sites where

silicon is continuously digged from the substrate and traverses through the aluminum layer. When excess amount of silicon diffuses into the aluminum layer, the mounds observed in figure 15 increases in diameter until they merge with their adjacent mounds, thus forming a continuous layer of crystalline silicon.

4.3 Horizontal Silicon Nanowires on top of an oxide layer:

In phase 1, horizontal silicon nanowires were successfully grown on top of a silicon substrate. Moving on to phase 2, an oxide layer is grown on silicon substrates by thermal oxidation. The oxide layer is patterned by the photolithography process to define various features by gradually increasing the width of the oxide layer and also the window size on the substrates. By varying the oxide width, we can estimate the maximum length of silicon nanowires that can be grown across the oxide layer. By varying the window size, we can observe the demand of silicon that is needed from the substrate to grow the silicon nanowires. A thin layer of aluminum is then evaporated on the substrates and annealed to grow the horizontal silicon nanowires.

4.3.1 Thickness of the oxide layer vs. the silicon nanowire growth

In this experiment, a 450 nm of silicon dioxide layer is grown in a thermal oxidation furnace on a five inch silicon wafer. The oxide layer is patterned with the photolithography process to define various features on the substrates. The silicon wafer is then diced into 1”x1” substrates by a dicing saw. Each substrate is then subjected to an oxide etching process with a buffered oxide etchant (BOE). The substrates are dipped in the BOE solution for 2, 3 and 4 minutes. The oxide thickness was measured by Nanospec. The resulting thickness of oxide layer was measured to be 250 nm, 100 nm and 10 nm. The four substrates with different oxide thicknesses were loaded in an aluminum evaporator system. Forty nanometers of aluminum was

thermally evaporated on these samples. The samples were quickly transferred into the MPZ 5 of the multi chamber PECVD system and annealed for 8 hours at 600°C.

Figures 16(a) and (b) show the SEM images of a sample with 10 nm of oxide layer, before and after etching aluminum. In figure 16(a), we can observe three windows on the substrate. Each window is of 10 µm x 80 µm in dimension. After the annealing, we observe the same characteristics on the oxide layer as seen on the silicon substrate. Some silicon nanowires were observed on the silicon substrate as well as on the oxide layer. Along with the silicon nanowires, the mounds were also similar on both the layers. Since the oxide layer was etched to get only 10 nm, there is a possibility of getting many pinholes on the oxide layer. From these pinholes, aluminum can easily get in contact with the silicon substrate underneath the oxide layer and the diffusion of silicon from the substrate into the aluminum layer can cause the mound formation on top of the oxide layer.

Figures 16(c) and (d) show the SEM images of a sample with 100 nm of oxide layer, before and after etching aluminum. In figure 16(c), we can observe the three windows on either side of the oxide layer. On the silicon substrate, the horizontal silicon nanowire growth was normal as expected. When we observe the oxide layer, networks of nanowires were grown on the oxide layer without any mound structures. Each nanowire was measured to be around 80 nm to 100 nm in diameter. Also many pits were observed to be along the edge of the oxide layer, which acts as a major source of silicon diffusing to the top of the oxide where it gets deposited along the aluminum grain boundaries. These networks of nanowires were observed to be running parallel to the oxide layer, which means the length of the nanowire is parallel to the length of the oxide layer. Also there were many tripoints observed in the network on top of the oxide. This

clearly shows the grain boundary sketch of the aluminum layer. Figure 16 (d) shows the SEM image of the sample after etching the aluminum. The nanowires were still intact on the oxide layer, which proves that these nanowires are made of silicon.

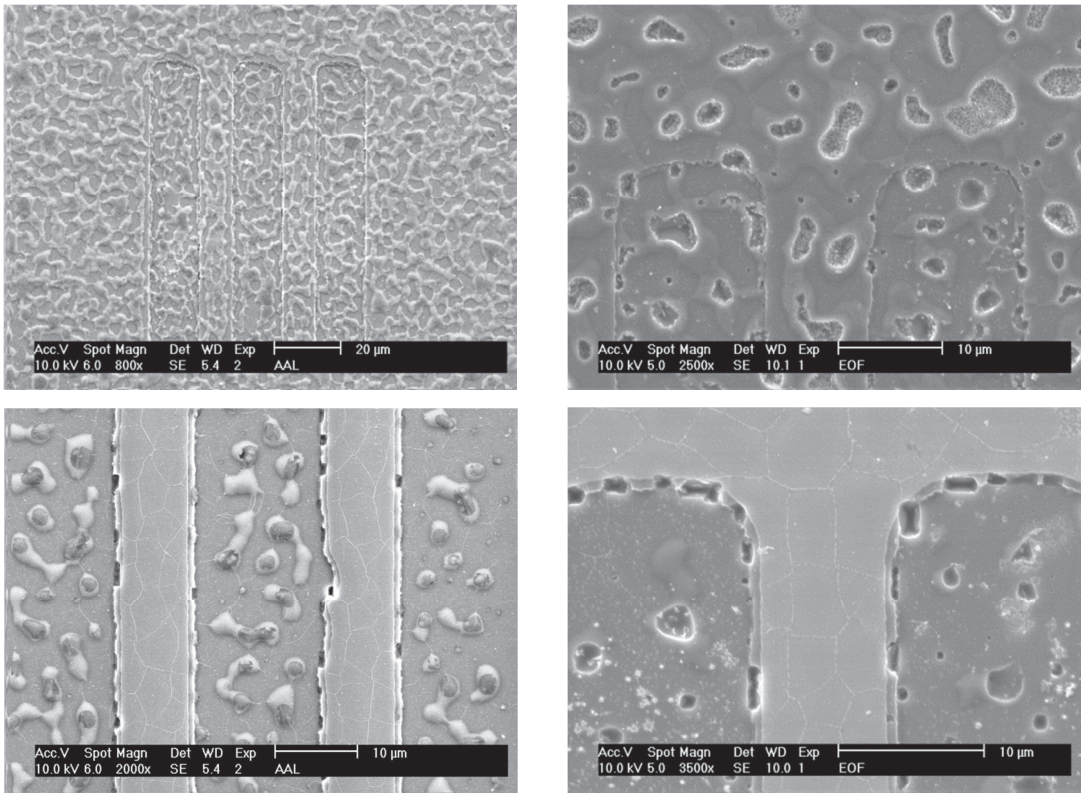

Figure 4 - 16: SEM images of the sample with patterned oxide and 40 nm of thin aluminum layer annealed at 600ºC for 8 hours. (a, b) – 10 nm oxide; (c, d) – 100 nm oxide.

Figures 17(a) and (b) show the SEM images of a sample with 250 nm of oxide layer, before and after etching aluminum. In figure 17(a), we can observe a network of nanowires on the substrate as well as on top of the oxide layer. The network of silicon nanowires on top of the oxide layer are interconnected with mounds like structures. When silicon diffuses through the aluminum layer, it forms mound like structures all over the oxide layer because of its high diffusivity constant. Usually these mounds are formed at the tripoints of the aluminum grain boundaries. When silicon diffuses through the aluminum layer, aluminum diffuses into the

substrate to fill the voids created in the substrate. As the two-way diffusion occurs, aluminum layer near the pits gets thinner and thinner gradually. At some point, the thickness of aluminum will be so reduced that the diffusion of silicon stops from the substrate. Because of the concentration gradient of silicon on the oxide, silicon from the mounds starts diffusing into the aluminum layer, forming the silicon nanowires.

Figures 17(c) and (d) show the SEM images of a sample with 450 nm of oxide layer, before and after aluminum etching. In figure 17(c), the mounds did not grow on the substrate. Instead, the pits were visible on the substrate as dark spots. Around the dark spots, there is a discontinuous network of silicon nanowires observed on the substrate. Also on the oxide layer, a discontinuous network of silicon nanowires was observed. It had the same hollow mounds kind of structures spread out on the oxide layer. The network of nanowires was not continuous instead the tripoints looked as if they were a little elevated from the surface, showing the initial stages of the mound formation on the oxide layer. This is because of the inefficient amount of silicon diffusing on top of the oxide layer. The thickness of the oxide layer is 450 nm and the diffusion of silicon depends on the thickness of the oxide layer and also the edge profile of the aluminum layer evaporated on the surface. If the step coverage is not perfect, then the diffusion of silicon may be slower or may not even happen. From this experiment, it is observed that if the oxide thickness is maintained around 100 nm, it is good enough to grow a network of silicon nanowires on top of an oxide layer.

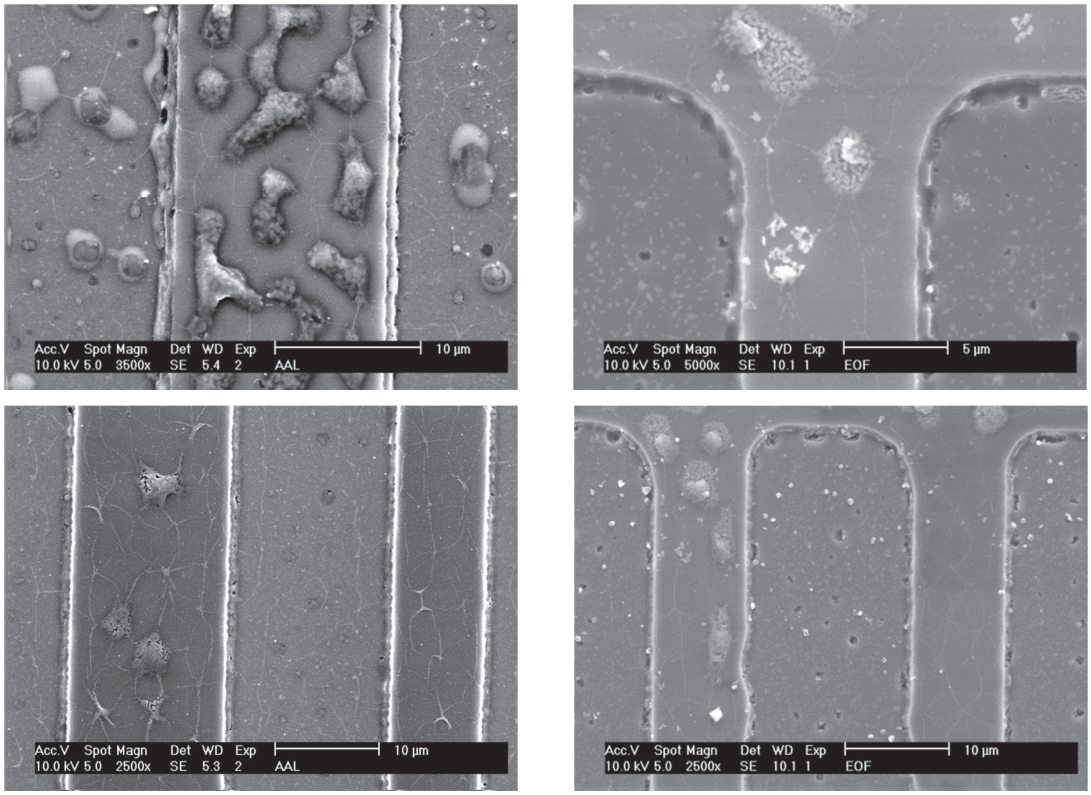

Figure 4 - 17: SEM images of the sample with patterned oxide and 40 nm of thin aluminum layer annealed at 600ºC for 8 hours. (a, b) – 250 nm oxide; (c, d) – 450 nm oxide.

4.3.2 Study of Oxide layer width and Window size

From the previous experiment, it is clear that to get a good network of silicon nanowires on top of an oxide layer, the thickness of the oxide layer should be maintained around 100 nm. So for the future experiments, the thickness of the oxide layer was fixed to 150 nm. Now the question is how far the silicon nanowires can travel on top of an oxide layer? Also what happens if we restrict the amount of silicon for diffusion? For this reason, a mask was designed to vary the width of the oxide layer and also the area of the windows. The width of the oxide layer is varied from 2 µm, 20 µm, 50 µm, 100 µm and 200 µm. Similarly, the edge of the window's square is varied from 10 µm, 50 µm, 100 µm and 200 µm. A schematic drawing of the mask used in this process is shown below.

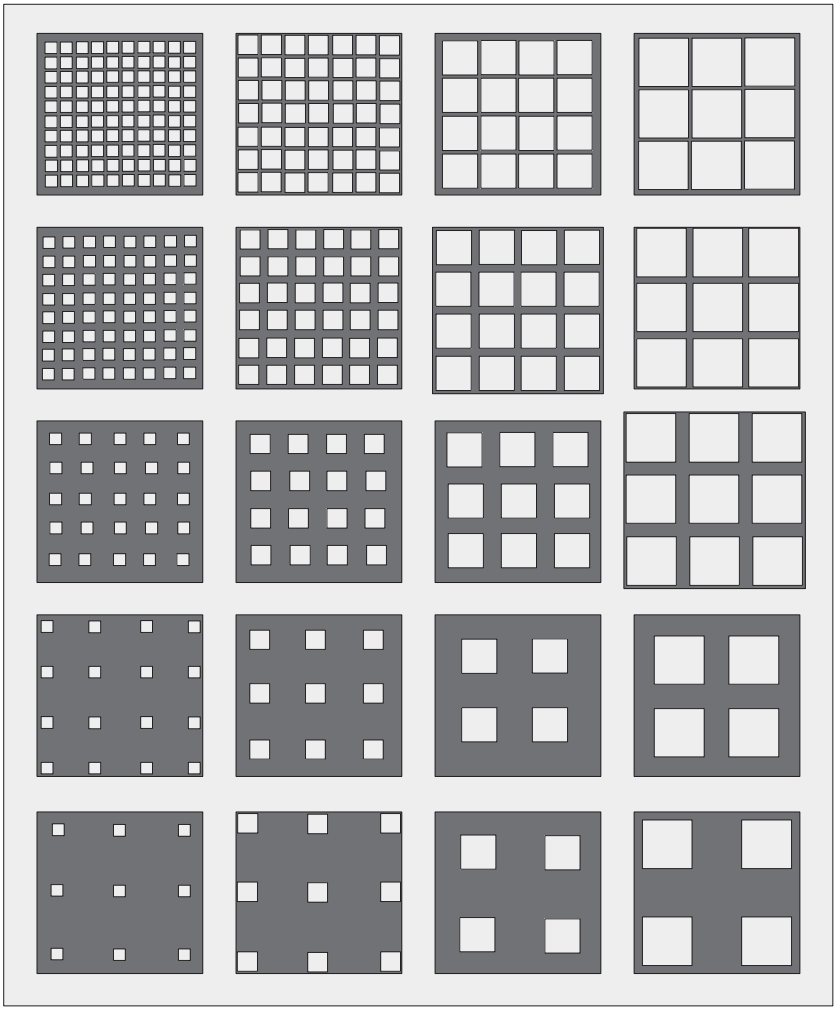

Figure 4 - 18: Schematic diagram of the top view of the mask used in the experiments. The dark and light regions show the oxide layer and the silicon substrate respectively.

4.3.2.1 Experiment 1:

40 nm of aluminum was thermally evaporated on the sample. A silicon substrate fully covered with 150 nm of oxide is also introduced in the system along with the patterned oxide sample. The oxide sample shows the interaction of aluminum with the oxide layer in the absence of the diffused silicon. The annealing temperature was set at 580°C. The samples were then annealed for 8 hours.

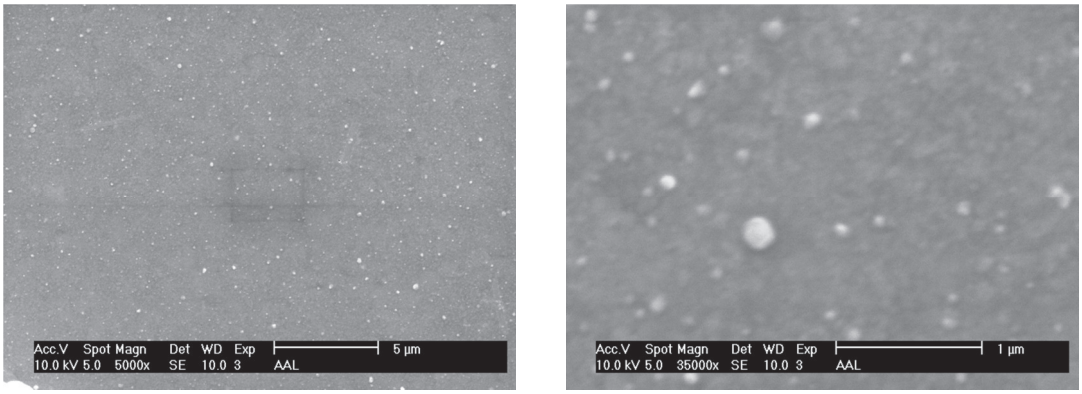

Figure 4 - 19**:** SEM images of a sample fully covered with oxide and 40 nm aluminum, and annealed at 580ºC for 8 hours.

Figures 19(a) and (b) show the SEM images of a sample fully covered with oxide and 40 nm aluminum, after it is annealed at 580ºC for 8 hours. It is observed that there seems to be no major interaction between the aluminum and the oxide layer. From the top view, we can observe many nanodots formed on the surface of the sample. These can be the aluminum nanodots. But after the evaporation of aluminum, for the sample to be loaded in the annealing chamber, the sample is exposed to the ambient atmosphere. There is a high chance to form of alumina on the top layer of aluminum. When the annealing starts, the aluminum reacts with the silicon dioxide layer to form Al_2O_3. The formation of Al_2O_3 may hinder the inter-diffusion of silicon and aluminum.

Figures 20(a) and (b) show the SEM images of the sample with the patterned oxide layer. The nanowire growth was observed over the substrate depending on the oxide width and the amount of silicon source. But after the sample was dipped in an aluminum etchant, the nanowires observed on the sample were wiped out as seen in figures 20(c) and (d). This may have happened because the mounds and the other features may have more percentage of aluminum content. So when the sample is dipped in the etchant solution, it had also removed the nanowire features.

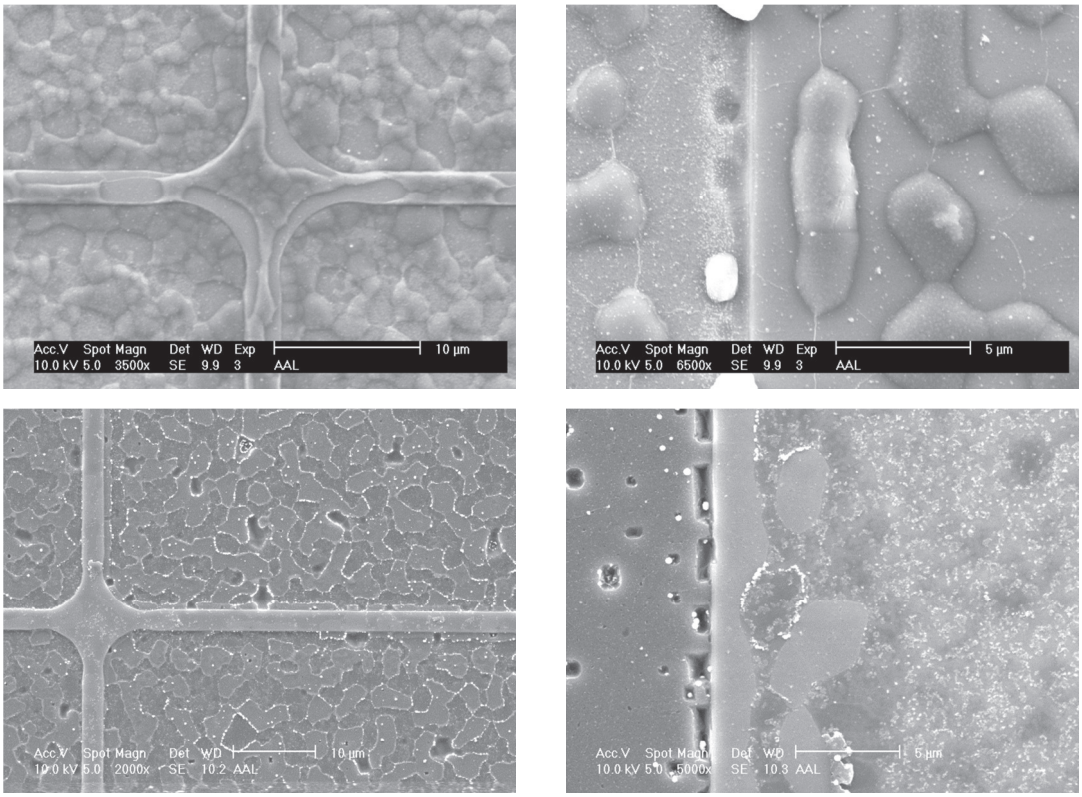

Figure 4 - 20: SEM images of a sample with patterned oxide layer after annealing at 580ºC for 8 hours, (a, b) – before aluminum etching, (c, d) – after aluminum etching.

4.3.2.2 Experiment 2:

The same experiment is repeated by changing the annealing temperature to 600ºC. The rest of the parameters were maintained the same.

Figures 21 (a, b), (c, d), (e, f), (g, h) and (i, j) show the SEM images of the sample with at 10 µm x 10 µm square window and oxide width varying from 200 µm, 100 µm, 50 µm, 20 µm and 2 µm before and after etching aluminum respectively. The circle that is visible in all the images is the actual window. That is the site where the oxide is etched from the substrate. These windows were supposed to be perfect squares. But during the photolithography process, the oxide layer was under-etched resulting in the curved corners. Figures 21 (b), (d), (f), (h) and (j) are the SEM images of the samples after etching the aluminum from the samples in figures 21

(a), (c), (e), (g) and (i) respectively. Comparing the samples before etching the aluminum, we can observe the pits very clearly in the sites where the oxide width is 200 µm and 100 µm. The pits in the later images are not visible before etching the aluminum, because they are covered with mounds of aluminum. After the aluminum is etched from these samples, these pits are clearly visible. In these images, the window size, oxide thickness and the aluminum thickness are all the same. The only variable in these sites is the oxide width. When the oxide width is 200 µm, the only source of silicon is the 100 μm^2 window (ignoring the adjacent windows). When annealing starts, silicon starts diffusing into the aluminum inside the windows. At this point there will be a silicon concentration gradient in the aluminum. Since there is a thin continuous film of aluminum extending on the oxide layer, silicon diffuses on top of the oxide layer through the aluminum layer.

Figures 22 (a) and (b) show a schematic model of the silicon concentration change on the oxide layer over time for 200 µm and 20 µm oxide widths. The edges of the oxide layer are the starting points for the diffusion of silicon. The large width of the oxide layer demands a lot of silicon when compared to the 20 µm oxide width. Since there is a lot of area for the silicon to diffuse, the diffusion from the substrate is very extreme that the spiking doesn't stop during the annealing period. This is very prominent from the figures 21 (a), (c), (e) and (g).

For the 20 µm oxide width, the diffusion happens from both the edges of the oxide layer and silicon can easily diffuse through the 20 µm width in no time. Once enough silicon is diffused on the oxide, silicon from one edge diffuses to the other edge covering up pits. This is the reason why we cannot observe any pits in the figures 21 (e), (g) and (i). From figure 22 (b),

the concentration of silicon across the oxide layer stays almost constant because of the sufficient amount of silicon diffusing from the substrate.

Also from figure 21 (a), we can observe a bright ring around the window, on the oxide layer. This ring forms because of the depletion of aluminum in that region. When silicon diffuses into the aluminum layer, aluminum diffuses into the silicon substrate. This phenomenon was previously mentioned as spiking. During the diffusion process, there is a limit for the amount of aluminum to diffuse. As the diffusion continues, the aluminum layer gradually thins down. Slowly, the area around the windows gets depleted of the aluminum. At this point the diffusion of silicon and aluminum stops on top of the oxide layer, because there is no medium for silicon to diffuse. In the same figure 21 (a), we can observe that the most of the silicon nanowires are not continuous. There are many breaks in the nanowire formation. This is because most of the silicon diffuses to the center of the oxide layer to maintain the silicon concentration of 12.6 wt.% of aluminum. These observations support the silicon concentration model depicted in the figures 22 (a) and (b).

It has already been mentioned that the diffusion of silicon is faster through the grain boundaries of aluminum when compared to the bulk of aluminum grains itself. When the diffusion starts, silicon quickly diffuses through the grain boundaries, “decorating” the aluminum grain boundaries and diffuses further on the oxide layer. The grain boundaries of aluminum form a pattern with many tripoints in the grain structure. A tripoint is a point where three grains meet each other. At these tripoints, most of the silicon diffusing through the aluminum layer precipitates like mounds or globules. That is the reason why we see many mounds formed on the oxide layer, interconnected by the silicon nanowires, in figures 21 (a, c, e, g and i).

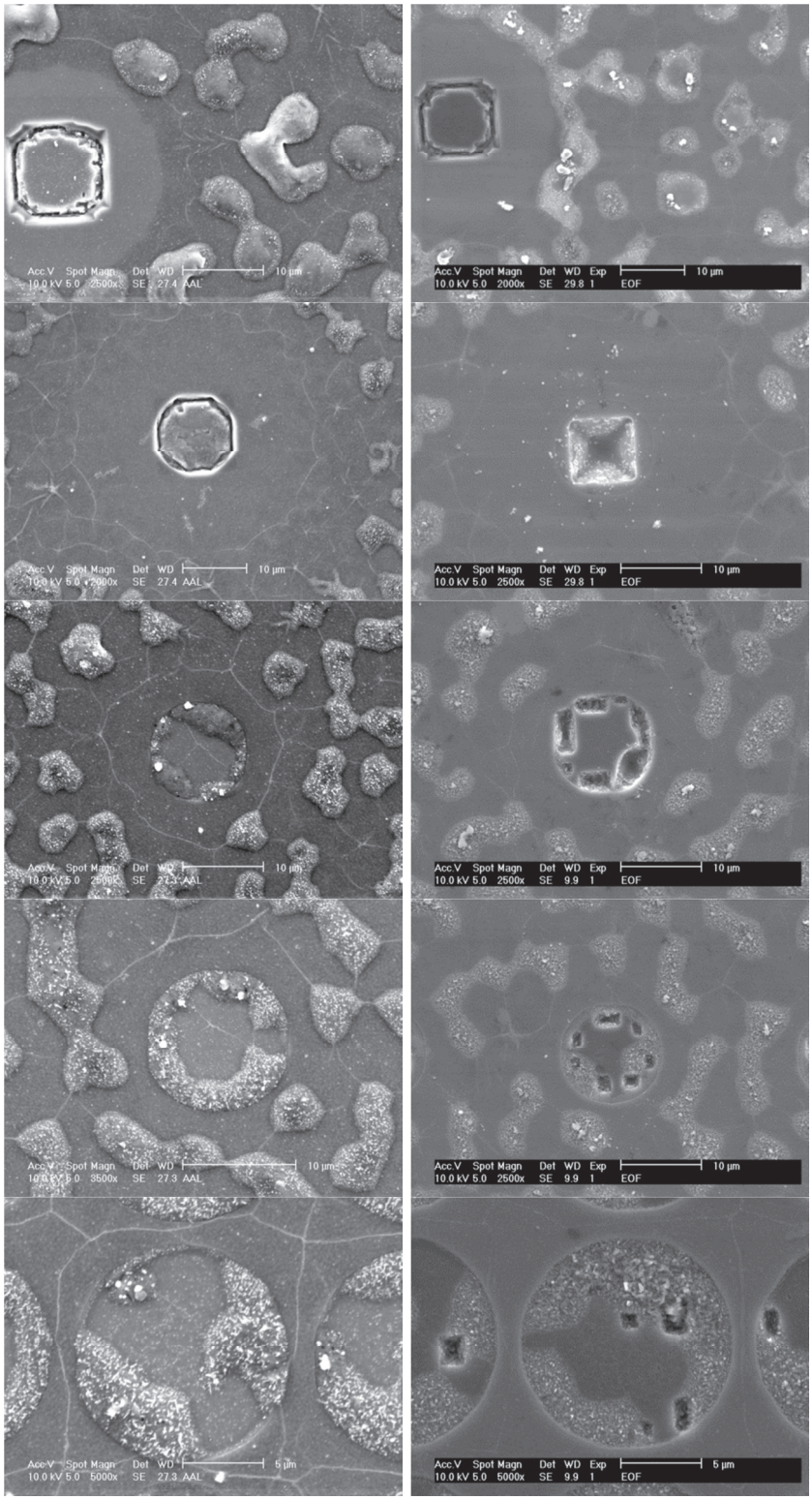

Figure 4 - 21: SEM image of a sample with 10 µm x 10 µm window size and oxide width of (a, b) 200 µm, (c, d) 100 µm, (e, f) 50 µm, (g, h) 20 µm and (i, j) 2 µm before and after etching aluminum respectively.

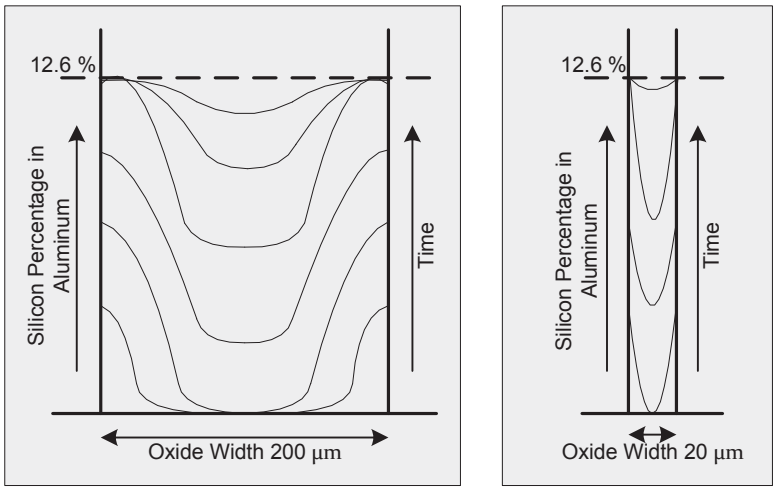

Figure 4 - 22: Silicon concentration over time on top of the oxide layer

Figure 23 shows a model of an island on top of a substrate, with the direction of the free energies. If γ_s is the free energy associated with the substrate surface, γ_i is the free energy of the island-substrate interface, and γ_f is the free energy of the surface of the island, then the island surface will contact the substrate surface at an angle θ, where

$$\gamma_s = \gamma_i + \gamma_f.\cos(\theta) \qquad [18]$$

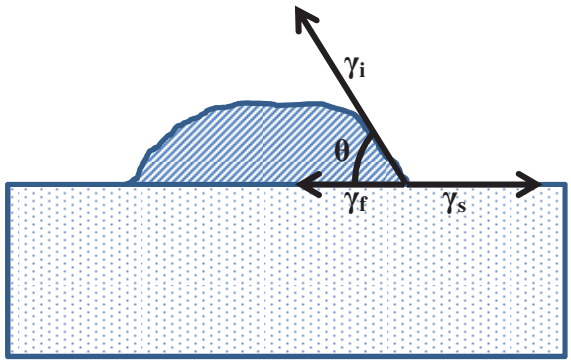

Figure 4 - 23: Contact angle of an island to a substrate

In the figure 21, many bright nanodots were observed all over the substrate and also on the oxide as well as the windows. These are the silicon granules precipitated on the surface while diffusing through the thin aluminum layer. When the mounds of silicon are formed at the

tripoints, there is still a layer of aluminum around the mounds. A small percentage of aluminum-silicon diffusion also happens within these mounds. The mounds themselves act as a secondary source of silicon on top of the oxide layer. Because of the high silicon concentration gradient with aluminum, the texture of the mounds also changes. When we compare figures 21 (a) and (i), the texture of the mounds near the edges is little different. This is because of the difference in the silicon percentage. Most of the silicon near the edge of the oxide diffuses to the farther sites in figure 21 (a), because of the large oxide width. But in figure 21 (i), the oxide width is only 2 µm. Silicon diffusing from one edge of the oxide can quickly diffuse to the opposite edge of the oxide, thereby precipitating as mounds and covering the pits. Because of the high concentration of silicon, the texture of these mounds becomes rough and small particulates of silicon show up on the surface.

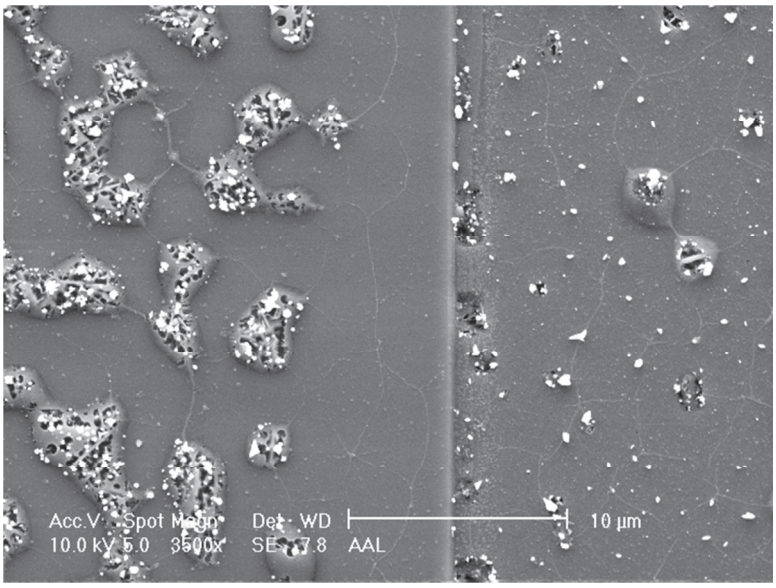

Figure 4 - 24: SEM image of the sample where aluminum is wet-etched from the surface

Figure 24 shows the SEM image of a site after the aluminum was wet etched from the surface. From the figure, we can observe pits on the edge of the oxide, on the mounds inside the

windows (right side) and also on the mounds on top of the oxide (left side). The silicon nanowires were intact on the surface of the substrate and also on the oxide layer. Along with the silicon nanowires, we can also observe the bright particulates (silicon) left on the surface.

Another interesting observation from this experiment was the network of nanowires observed in figure 21 (i) and (j). The circles from the top view are the windows and the horizontal and vertical stripes are the oxide layer. After annealing the substrate at 600ºC for 8 hours with 40 nm of thin aluminum layer, network silicon nanowires was observed to be almost aligned along the oxide layer. During the annealing process, the diameter of aluminum grains grows from several nanometers to several micrometers (~ 10 μm). In all the previous sites, the width of the oxide layer was more than the diameter of aluminum grains. That is the reason why a group of silicon nanowires were observed on the oxide layer instead of a single nanowire growing along or across the oxide layer. The aluminum grains aligned along the oxide layer such that the grain boundary of two adjacent grains was laid along the oxide layer instead of growing across the oxide. The nanowires were still intact on the sample even after the aluminum was etched from the substrate, proving that these are silicon nanowires.

This result does not satisfy the motivation behind this research of growing an array of horizontal silicon nanowires across the oxide layer, but the growth of silicon nanowires on top of the oxide was controlled in one way or the other. Similar results were also observed in various sites of the sample where the window size was increased to 2500 μm^2, 10000 μm^2 and 40000 μm^2. Figures 25, 26 and 27 show the SEM images of these sites with different oxide widths.

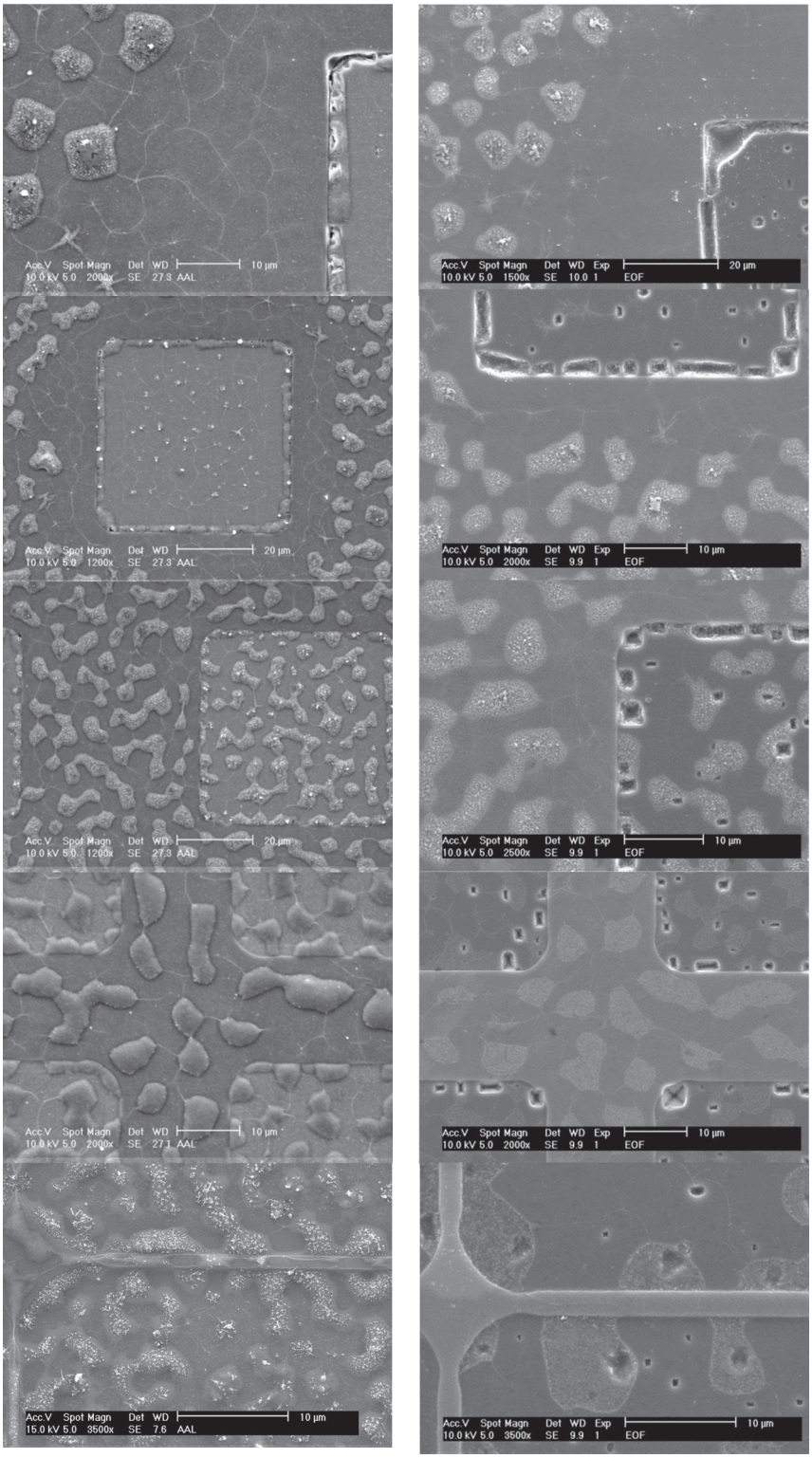

Figure 4 - 25: SEM image of a sample with 50 µm x 50 µm window size and oxide width of (a, b) 200 µm, (c, d) 100 µm, (e, f) 50 µm, (g, h) 20 µm and (i, j) 2 µm before and after etching aluminum respectively.

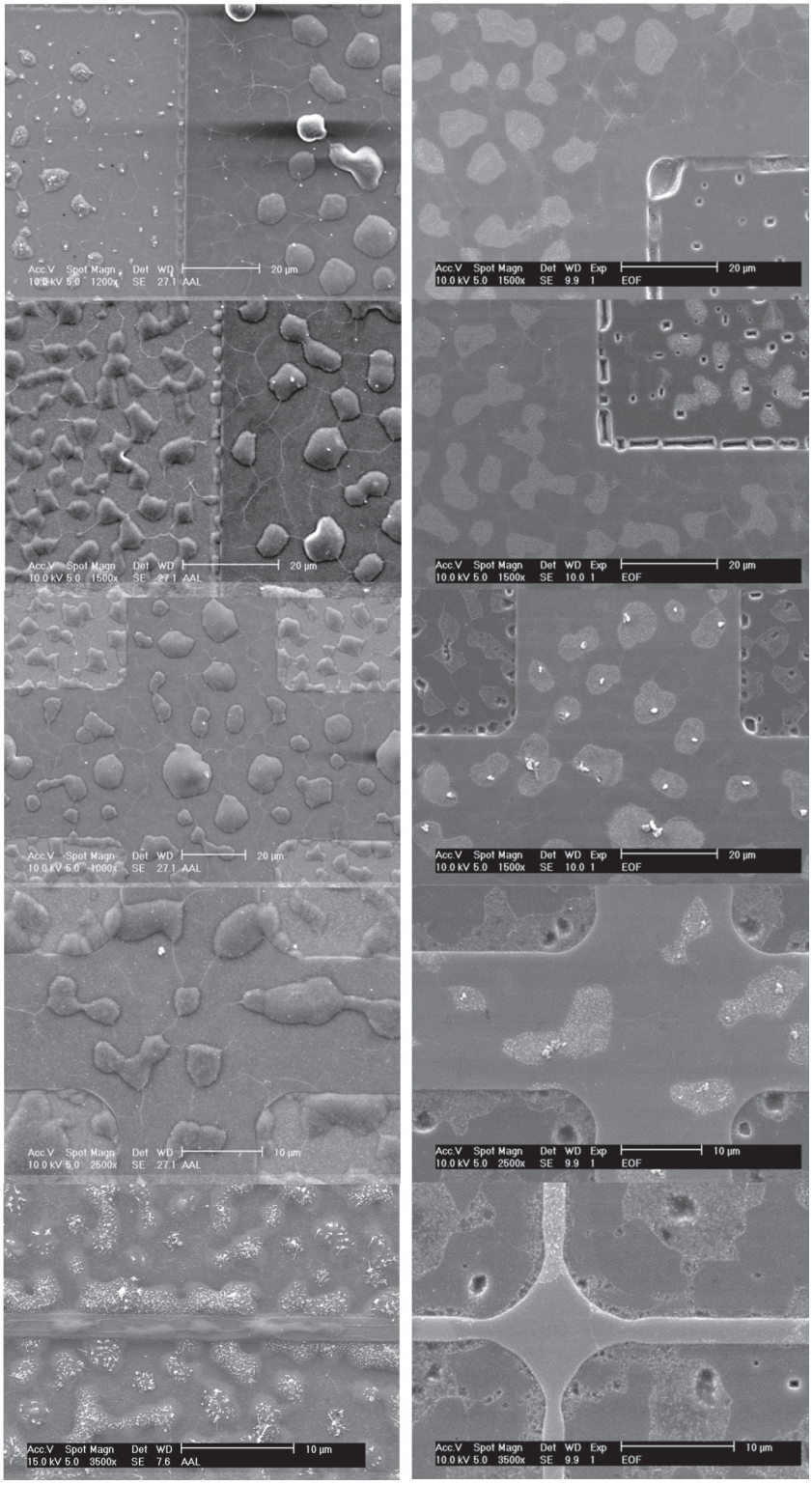

Figure 4 - 26: SEM image of a sample with 100 µm x 100 µm window size and oxide width of (a, b) 200 µm, (c, d) 100 µm, (e, f) 50 µm, (g, h) 20 µm and (i, j) 2 µm before and after etching aluminum respectively.

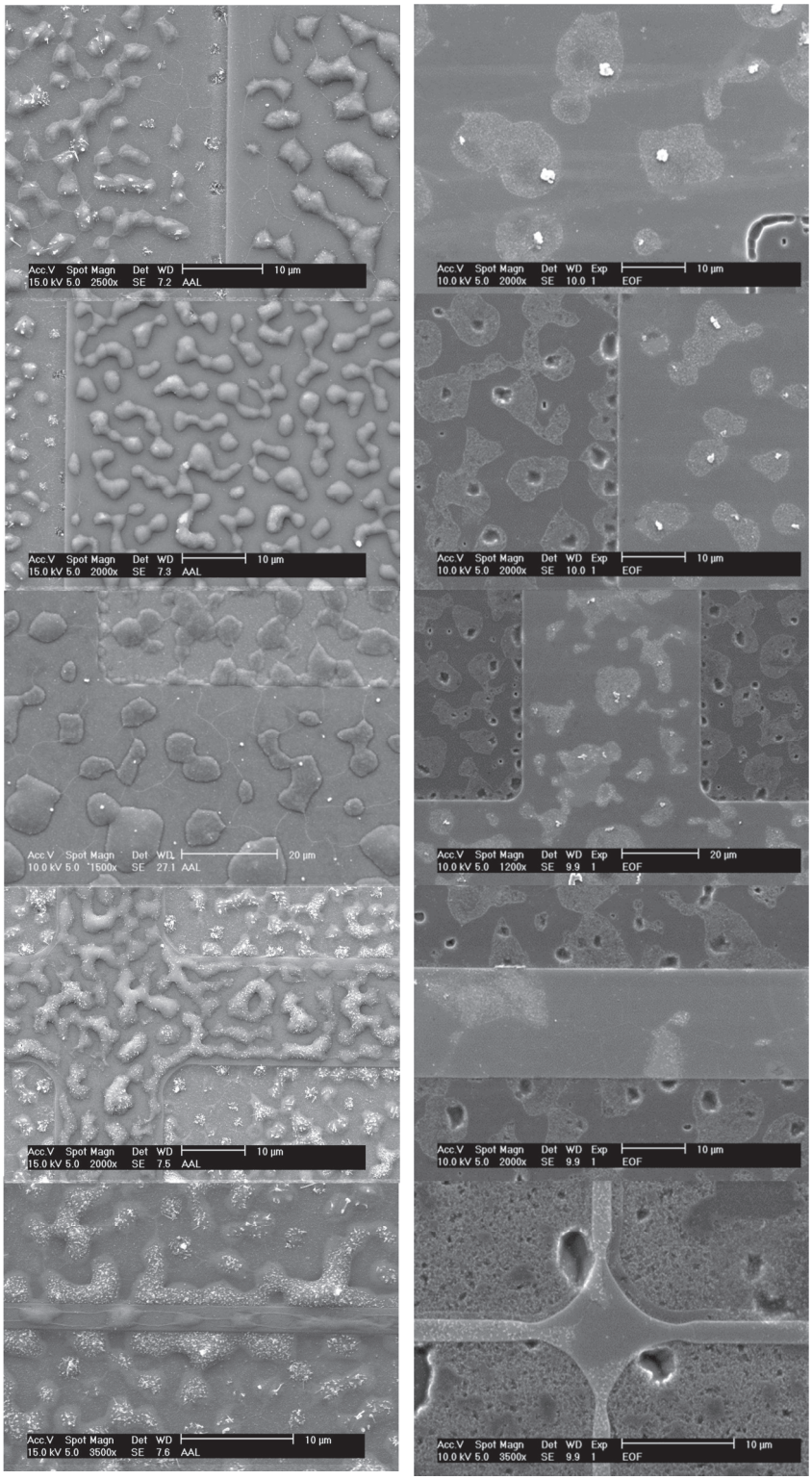

Figure 4 - 27: SEM image of a sample with 200 µm x 200 µm window size and oxide width of (a, b) 200 µm, (c, d) 100 µm, (e, f) 50 µm, (g, h) 20 µm and (i, j) 2 µm before and after etching aluminum.

The EDX patterns from figure 28 show that the mounds are made of aluminum and silicon. The pits observed on these islands show a relatively higher concentration of aluminum when compared to the mounds. Figure 28(a) shows the EDX pattern on top of the silicon dioxide layer. From the pattern it is clear that the layer is mainly made of silicon and oxygen. Figure 28(c) shows the EDX pattern on top of a mound on the oxide layer. This shows that the mound is made up of an alloy of aluminum and silicon. Figure 28(e) shows the EDX pattern of a pit on the island on the oxide layer. The aluminum content in this pit is observed to be higher than the aluminum content in the mound itself. Figure 28(g) shows the EDX pattern on top of a silicon nanowire on the oxide layer. In this pattern, it can be observed that the nanowire is mainly made up of silicon. The oxygen content showing in this pattern is expected to be from the oxide layer beneath it.

Figure 28(b) shows the EDX pattern on top of the bare silicon. The pattern shows that it is pure silicon with little trace of aluminum. Figure 28(d) shows the EDX pattern on a mound on the substrate. This pattern shows significant amount of aluminum present in the mounds. Figure 28(f) shows the EDX pattern in the pits of the islands on the substrate. From the pattern it is clear that the amount of aluminum present in these pits is higher than the aluminum present in the mounds. These pits are also the main source of silicon coming from the substrate. The higher concentration of aluminum shows that the aluminum is going deeper into the substrate pushing the silicon out of the substrate. Figure 28(h) shows the EDX pattern observed on the nanowire on the substrate. This shows that the nanowire is mainly comprised of silicon.

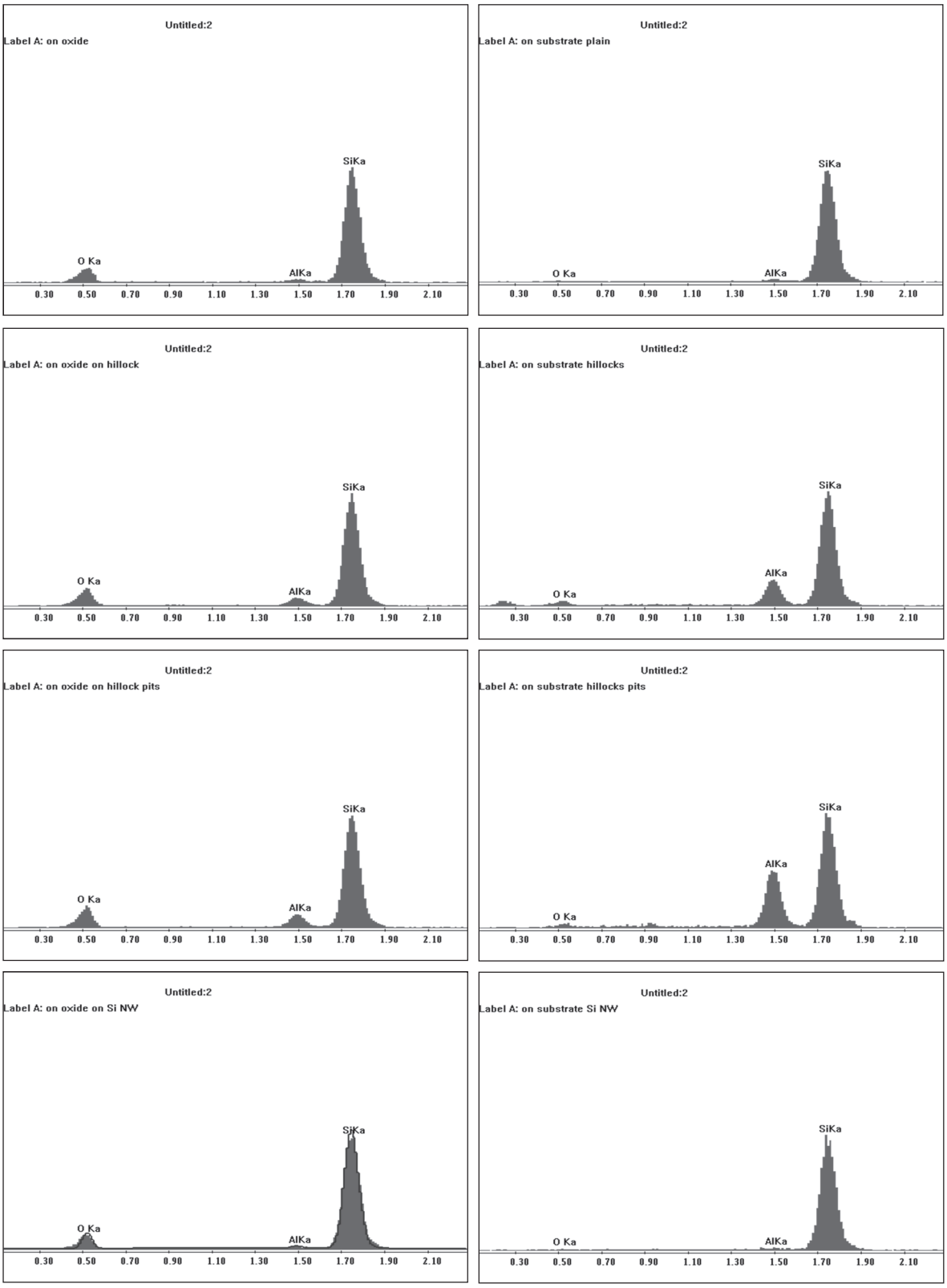

Figure 4 - 28: EDX patterns of the sample at various sites

Based on these results, a nano-electronic device was designed and fabricated. Figure 29 shows a schematic of a junctionless silicon nanowire field effect transistor. Because of the aluminum, the nanowire is doped p-type. In this transistor, the entire length of the nanowire acts as a channel. Figure 30 shows the top view of the junctionless field effect transistor after etching the aluminum. The drain and source contacts on the silicon nanowire are formed by depositing platinum using focused-ion beam (FIB). Platinum is chosen as the contacts because it forms a good ohmic contact with silicon. The other silicon nanowires in contact with the platinum are cut by using the FIB. Figure 31 shows the EDX results of the junctionless silicon nanowire field effect transistor. Figure 31 (b) shows all the elements found on the substrate. Each element is given a color code, for example, silicon is red, aluminum is purple, oxygen is sky blue and, platinum is blue. The software has the capability to select each element and highlight its position on the substrate. Figures 31 (c-f) shows the composition of each element found on the substrate.

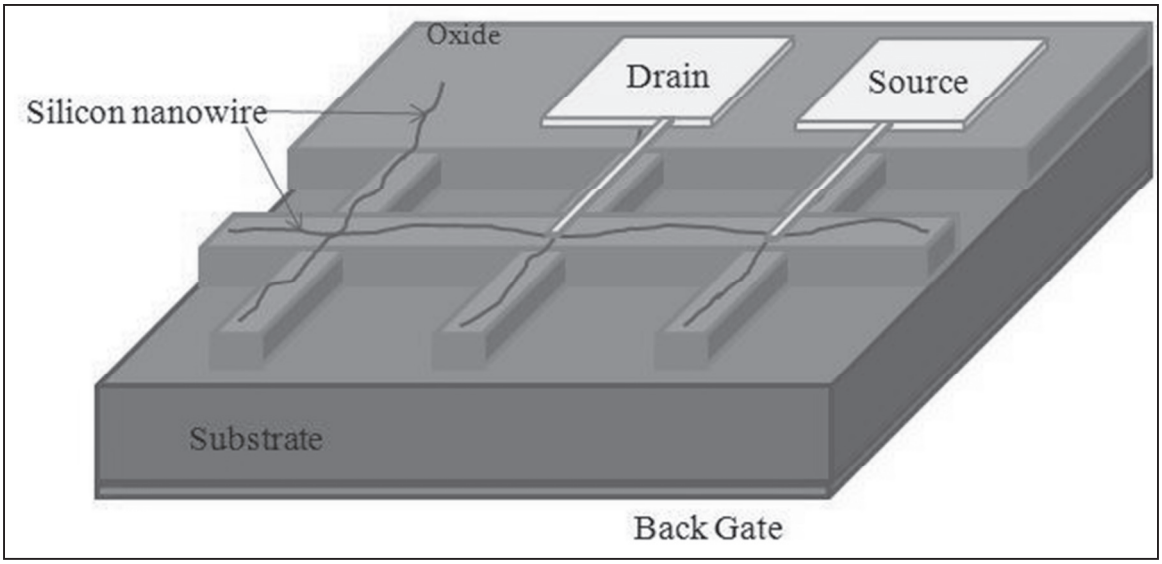

Figure 4 - 29: Schematic of a nano-electronic device

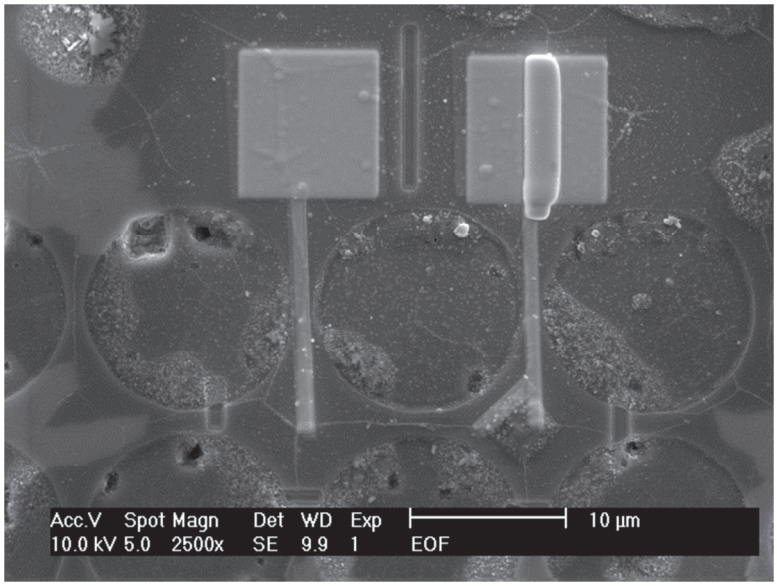

Figure 4 - 30: Top view of a junctionless silicon nanowire field effect transistor

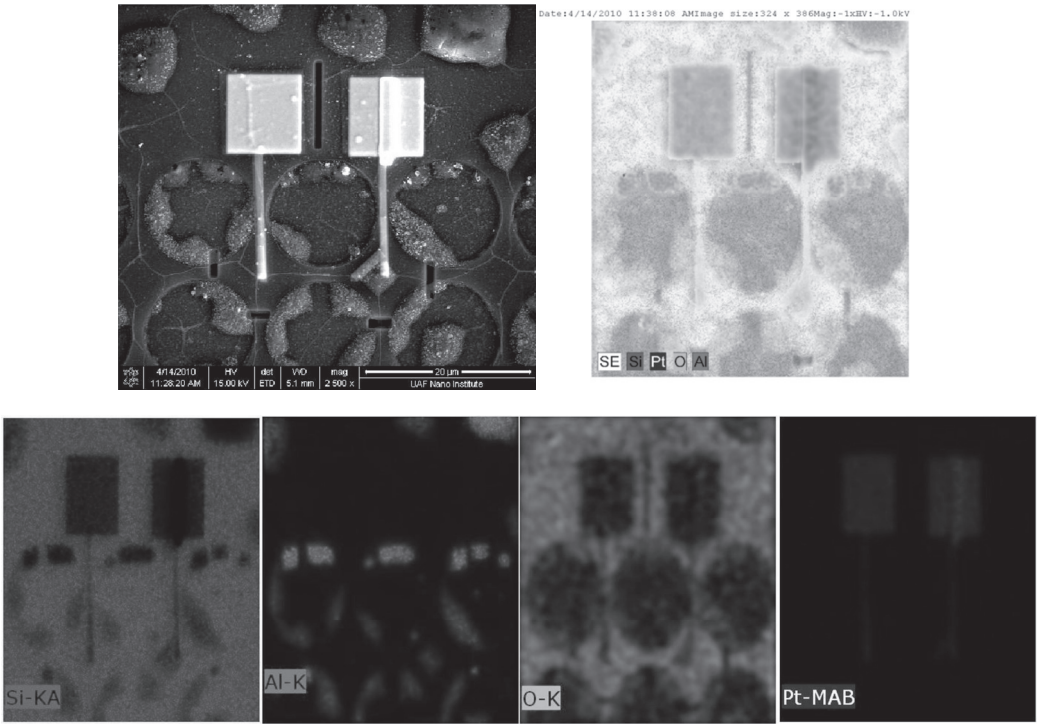

Figure 4 - 31: EDX report of the junctionless silicon nanowire field effect transistor

CHAPTER 5: CONCLUSION AND FUTURE WORK

5.1 Conclusion

This research work was directed towards the fabrication of horizontal silicon nanowires on a substrate using aluminum as a catalyst. A new mechanism was proposed in which the crystalline silicon from the substrate diffuses through the aluminum layer and deposits along its grain boundaries to form a network of nanowires. The thickness of aluminum is optimized to grow a network of horizontal silicon nanowires. It was shown that 40 nm of thin aluminum layer is needed to fabricate the horizontal silicon nanowires. A time study experiment is conducted to clearly understand the growth process. The substrate should be annealed for 8 hours at 600ºC to grow the horizontal silicon nanowires. If the annealing time exceeds 8 hours, silicon diffusing from the substrate forms a continuous crystalline layer on the substrate.

A continuation of this work was to fabricate a network of horizontal silicon nanowires on an insulating layer. Silicon dioxide was chosen as the insulator because it can be easily grown using a thermal furnace and oxide patterning was done using photolithography. The thickness of the oxide layer was optimized to grow a network of horizontal silicon nanowires. Growth parameters were maintained the same in order to achieve the network of nanowires.

To optimize the growth properties of the silicon nanowires, the width and the window size of the oxide layer were varied. It was discovered that the width of the oxide layer plays a major role in controlling the growth of horizontal silicon nanowires. A schematic of a simple silicon nanowire field effect transistor was designed and fabricated using platinum as the drain and source contacts.

5.2 Future Works

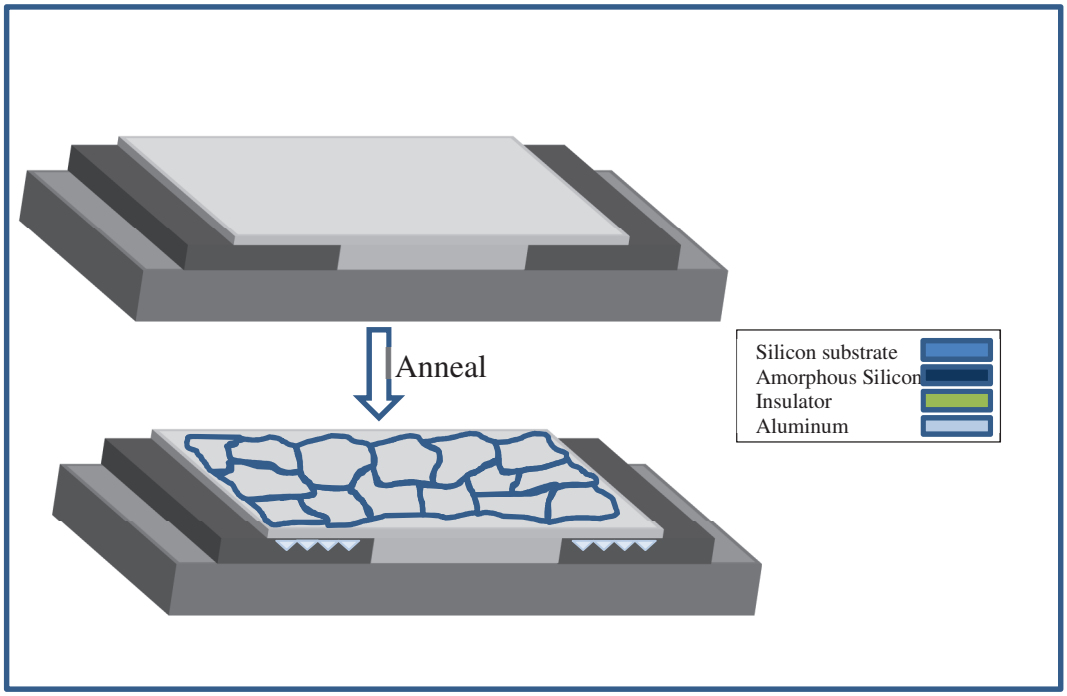

Figure 5 - 1: Process showing the formation of silicon nanowires using amorphous silicon as the source of silicon

So far crystalline silicon substrate was used as a source of silicon to grow a network of horizontal silicon nanowires. But the silicon substrate is being destroyed or used by forming aluminum pits in the bulk of the substrate. This is highly undesirable in forming devices on the substrate. So a layer of amorphous silicon can be deposited on top of the silicon substrate as the source of silicon. Aluminum diffusion in amorphous silicon is believed to be faster than aluminum diffusion in crystalline silicon. So the diffusion of silicon into the aluminum layer can start at lower temperatures.

Figure 5-1 shows a schematic of a process in growing the horizontal silicon nanowires using amorphous silicon. Let's suppose there is an insulator layer separating two layers of amorphous silicon on a crystalline silicon substrate as shown in the figure 5-1. A thin layer of

aluminum is deposited on top of the layers. The two amorphous silicon layers act as a source of silicon and the aluminum layer on top of the insulator acts as a sink. Silicon diffusion in this case starts at a lower temperature instead of the high diffusion temperatures for crystalline silicon substrates. The diffused silicon decorates the aluminum grain boundaries in the thin aluminum film, growing a network of horizontal silicon nanowires on top of the insulator. Because of aluminum layer, the nanowires formed will be doped p-type. If the amorphous silicon layers are doped n-type, then by depositing a floating gate on the silicon nanowires, a simple p-MOSFET can be fabricated.

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