8-2012

A Silicon Carbide Linear Voltage Regulator for High Temperature Applications

Javier Antonio Valle Mayorga
University of Arkansas, Fayetteville

A SILICON CARBIDE LINEAR VOLTAGE REGULATOR FOR HIGH TEMPERATURE APPLICATIONS

A SILICON CARBIDE LINEAR VOLTAGE REGULATOR FOR HIGH TEMPERATURE APPLICATIONS

A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Engineering

By

Javier Antonio Valle Mayorga
John Brown University
Bachelor of Engineering, 2003
Aichi Institute of Technology
Masters of Science in Electrical Engineering, 2008

August 2012
University of Arkansas

Abstract

Current market demands have pushed the capabilities of silicon to the edge. High temperature and high power applications require a semiconductor device to operate reliably in very harsh environments. This situation has awakened interests in other types of semiconductors, usually with a higher bandgap than silicon's, as the next venue for the fabrication of integrated circuits (IC) and power devices. Silicon Carbide (SiC) has so far proven to be one of the best options in the power devices field.

This dissertation presents the first attempt to fabricate a SiC linear voltage regulator. This circuit would provide a power management option for developing SiC processes due to its relatively simple implementation and yet, a performance acceptable to today's systems applications. This document details the challenges faced and methods needed to design and fabricate the circuit as well as measured data corroborating design simulation results.

This dissertation is approved for recommendation
to the Graduate Council.

Dissertation Director:

_____

Dr. H. Alan Mantooth

Dissertation Committee:

_____

Dr. Randy Brown

_____

Dr. Juan C. Balda

_____

Dr. Scott Smith

_____

Dr. Jia Di

Dissertation Duplication Release

I hereby authorize the University of Arkansas Libraries to duplicate this dissertation when needed for research and/or scholarship.

Agreed _____

Javier Antonio Valle Mayorga

Refused _____

Javier Antonio Valle Mayorga

Acknowledgements

It was during my elementary school years that I decided to get a doctorate. At that point and with a mind full of utopic thoughts, I wanted to get a doctorate in politics. It took a couple months in high school to grow fond of science. Since then, it has been a long journey from Leon, Nicaragua - the little town that Ruben Dario would call *his* Paris.

I would have never been able to make it up to this point without the invaluable and blind support from my parents and brothers. My mom, that with the broken heart of a mother letting her boy go to another country, never tried to stop me. My dad, with his very strong and manly figure, gave me at that time one of the best gifts of my life, a single tear while he dropped me at the airport. From the bottom of my heart, thanks to both of you. I am proud to be your son. I will always remember where I come from, to make sure I know where I am going. Dad, it breaks my heart that you could not witness this accomplishment but I am finishing up in your name, I love you and you have no idea how much I miss you. Sergio and Ricardo, thanks for always being there.

From a boy to a man, I married my complement, literally. Our marriage does not follow the typical “alike” story. But somehow, deep in the mysteries of life and love, God has put us together and has created an amazing bond that will never die. Thanks Enma for your love and support. It is not easy to be the wife of a student, but now all our efforts are finally paying off. I love you and I am eternally thankful for the two little angels God has given us. They are the strength that pushes me forward and I cannot see my life without them. Fernanda and J. Isaac, this is for you too.

I also want to thank Dr. Mantooth for this achievement. But not the professor that supported me financially all these years. Nor the advisor that has taught me to be a better engineer, to work hard and to always do my best. I want to thank the person that has supported me during some personal bad times. I certainly appreciate the time you spent talking to me about the things in life that we as humans never seem to understand. You did in fact help me to face these bad times and I am eternally thankful for that.

Finally, I thank to the amazing group of friends that made the endless nights at the lab easier. I have learned a lot from each one of you and I certainly hope that I had an impact in your lives as large as the one you had in mine. Special thanks to Ashfaqur Rahman for the technical discussions we had for this project. You have been blessed with a terrific mind but beyond that, with the gift of being a good friend.

Por una Nicaragua libre de tiranos

Javier A. Valle Mayorga

Table of Contents

CHAPTER 1: INTRODUCTION

1.1 Motivation

After the invention and revolution of portable devices such as cell phones and cameras, power management has become a critical factor in the proper operation and efficiency of such devices. Power management, in these cases, is responsible for supplying and conditioning power to the different circuits in the device. These circuits could be analog or digital in nature and are all usually powered by batteries which incur substantial voltage and current variations across time and over a wide range of operating conditions [1]. Power management in such cases is achieved by a regulator which minimizes these variations and provides stable and constant power to the circuits in the system under different loads and environmental settings.

While it is true that regulation is very important in high performance applications, ideally any type of system should have some regulation. It is a common practice for Integrated Circuit (IC) designers to account for power supply variations whenever the specifications of a circuit are being determined. Ideally, if these variations in the supply could be reduced by a regulator, it would provide more flexibility to the design process and robustness to the circuit. It is important to notice that power management implies supplying a constant voltage regardless of current variations. Hence, a voltage reference differs from a voltage regulator by the fact that the former does not provide large currents. An ideal regulator should also protect the circuits it is powering up using features such as over-current protection, thermal shutdowns and open/short loads detection.

As mentioned before, regulation should also exist under the wide range of operating conditions the circuits are designed to operate in. In this context, applications in high temperature environments such as automotive and oil drilling exploration are now being enhanced due to recent developments in wide bandgap semiconductor materials such as Gallium Nitride (GaN) and Silicon Carbide (SiC). Prior to these developments, considerable heat sinking requirements and/or placing the circuits away from the heat source were some of the solutions used for high power and/or high temperature operation when Silicon (Si) was used. Silicon-on-Insulator (SOI) also provides an option for circuitry operating up to 225 °C in these kinds of applications [2]. However, the wide bandgap of GaN and SiC (about 3 times the 1.1 eV bandgap of Si) allows, in theory, the placement of these new devices or circuitry close to the heat source without any temperature risks (theoretically up to 600 °C) or breakdown voltage issues.

The problem with these new materials is that they are not mature enough and are still being studied. While it is true that discrete devices are commercially available, the circuitry concept as in Si is still not adequate. Out of these wide bandgap semicondutors, SiC has proven to be the most suitable for the applications previously mentioned [3]. SiC Schottky diodes and power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are now being used in power electronic systems due to the large number of benefits such as low on-resistance, faster switching and temperature range of operation [4]. With these discrete devices being commercially available, the next logical step is to fabricate SiC ICs. Different Boolean gates and conventional operational amplifiers operating at temperatures of 300 °C and above have been fabricated in SiC and will be discussed in Section 2.3.2 However, the literature does not report any complex circuit fabricated in SiC, and there is currently no option for regulation in this field either.

1.2 The need for a SiC voltage regulator

The research project under which this SiC voltage regulator is being fabricated is one of the first steps into fabricating SiC ICs. The project's goal is to integrate an existing 4H-SiC power MOSFET from Cree Semiconductor with low voltage 4H-SiC depletion and enhancement NMOS in order to develop a prototype battery charger system for the next generation of Toyota Prius. Cree Semiconductor is fabricating both the high voltage and the low voltage 4H-SiC MOSFETs.

Due to the importance of power management and the steps being taken towards fabricating SiC ICs, all the different features that we currently employ from Si circuitry should be explored with this new semiconductor. As argued before, power management is nowadays one of the most critical aspects in the design process, and this dissertation presents the first attempt to provide an option in that field. This dissertation presents the design process and experimental data of a SiC linear voltage regulator for high temperature applications.

1.3 Dissertation structure

This dissertation is arranged the following way:

- Chapter 1: Introduction – A brief overview of the motivation behind this work.
- Chapter 2: Silicon Carbide – This chapter presents an overview of the different properties of SiC and its advantages when compared to Si. It also presents where the state-of-the-art is in respect to fabricating devices and circuits using this semiconductor material.
- Chapter 3: Cree SiC Process – Details of the process used to fabricate the transistors are presented. The challenges of the process and the repercussions in the design process are discussed as well.

- Chapter 4: Voltage Regulators – A detailed explanation of the classification and operation of voltage regulators is discussed. The state-of-the-art in Si voltage regulators is presented.
- Chapter 5: SiC Voltage Regulator Design – In this chapter, a step by step explanation of the transistor level design process of the voltage regulator is presented. Simulations and performance are discussed in detail.
- Chapter 6: SiC Voltage Regulator Testing and Characterization – The results of testing the SiC voltage regulator are summarized here. A performance comparison with Si voltage regulators is included.
- Chapter 7: Conclusions and Future Work – This chapter presents the conclusions from the work presented in this dissertation. Recommendations for future work based on the work presented here are presented as well.

CHAPTER 2: SILICON CARBIDE

2.1 SiC Properties

SiC is positioned to be the semiconductor that will advance the state-of-the-art for high temperature electronics applications. SiC power devices offer tremendous advantages over conventional switch technology, including the possibility for 10× the power density, 10× the breakdown voltage, 1/10th the switching losses, higher switching frequencies, and operation at considerably higher temperatures [4], [5].

Depending on its polytype structure, SiC can be mainly classified as 3C, 4H and 6H poly type. 4H-SiC however, is preferred for power device structures due to its higher band gap (3.26 eV for 4H-SiC and 3.0 eV for 6H-SiC). Simple circuits such as operational amplifiers and Boolean logic gates have been fabricated in 6H-SiC [6]-[9]; although new research is being oriented toward 4H-SiC due to its advantages in power electronics applications. As mentioned before, this project will integrate 4H-SiC power devices with 4H-SiC low voltage devices and hence we will refer to 4H-SiC only as SiC from now on.

The literature shows the focus on SiC devices has been limited to power electronics applications and not extended to low voltage electronics due to the challenges faced with the fabrication process. These challenges are mainly due to the interface and oxide traps that degrade the performance of the devices by reducing mobility and causing threshold voltage instability [10]-[13]. This project, however, attempts to explore the SiC IC field to investigate the numerous benefits that could be obtained from it. These benefits are due mainly to the SiC properties described in this chapter.

2.1.1 Energy Band Gap

Energy band gap is the property that allows SiC to be classified as a wide band gap semiconductor. The band gap for Si is 1.1 eV, while the band gap for 4H-SiC is 3.26 eV. The larger band gap results in lesser thermal generation of carriers in the depletion region of devices. This situation is favorable for reducing the leakage current of devices which utilize P-N junctions to support voltages [14].

The lesser generation of carriers is related to the intrinsic carrier concentration which is temperature dependent. For silicon, the intrinsic carrier concentration is given by:

$$n_i = 3.87 \times 10^{16} T^{3/2} e^{-(7.02\times10^3)/T} \quad (2.1)$$

and for 4H-SiC, it is given by:

$$n_i = 1.70 \times 10^{16} T^{3/2} e^{-(2.08\times10^4)/T} \quad (2.2)$$

Plotting these two equations, as shown in Fig. 1, allows the grasping of their practical meaning. For example at room temperature Si's intrinsic carrier concentration is 1.4 x 10^{10} cm^{-3}, but at a temperature of about 550 °K (277 °C), it increases to about 1 x 10^{15} cm^{-3}, matching a typical light doping concentration used to fabricate devices. This situation makes the doped areas useless and hence, the device unsuitable for high temperature. 4H-SiC on the other hand, has an intrinsic carrier concentration of 6.7 x 10^{-11} cm^{-3} at room temperature and only 3.9x10^{7} cm^{-3} at 700 °K (427 °C), making it, in theory, able to operate at such high temperatures.

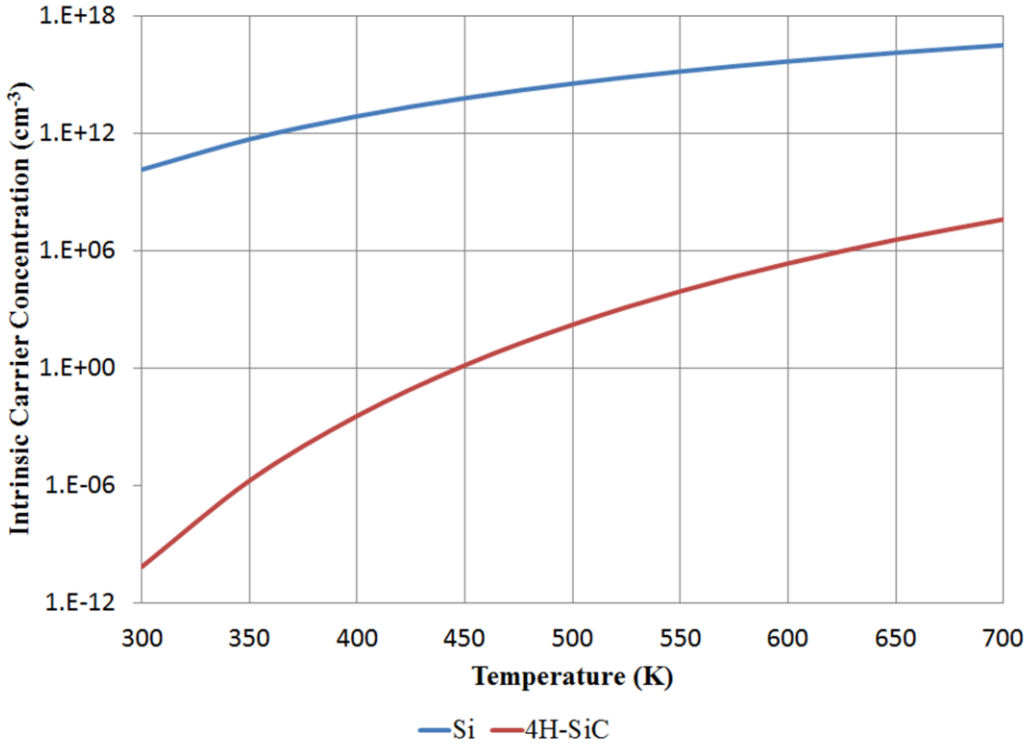


Fig. 2.1 – Intrinsic carrier concentration of Si and 4H-SiC across temperature.

2.1.2 Impact Ionization Coefficients

Reduced impact ionization coefficients are related to the higher breakdown voltages that wide band gap semiconductors offer when compared to Si. This is one of the main attributes of SiC for power device applications. Impact ionization is an avalanche process created by an electric field. In this case, a carrier is accelerated to a high enough kinetic energy to cause an ionization collision with the lattice. This single event results in carrier multiplication (generation of electron-hole pairs) which can become very high due to its avalanche nature [15]. The impact ionization coefficients for semiconductors are dictated by Chynoweth's Law [16], [17]:

$$\propto = ae^{-b/E} \tag{2.3}$$

where E is the electric field component in the direction of the current flow. The parameters *a* and *b* depend on the semiconductor material and temperature.

The extracted impact ionization coefficients for Si and 4H-SiC are shown in Fig. 2.2. From there, it can be observed that the generation of carriers due to impact ionization in 4H-SiC occurs at an electric field an order of magnitude larger than in Si.

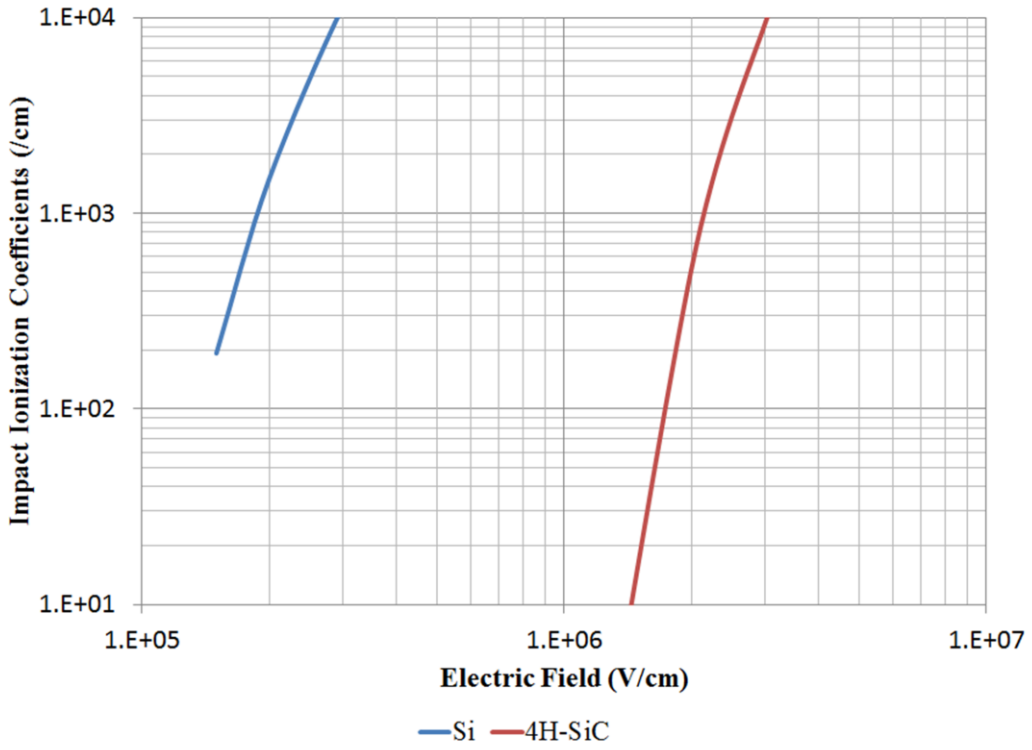


Fig. 2.2 – Impact ionization coefficients in Si and 4H-SiC.

2.1.3 Electron Mobility

This property is particularly important for SiC power devices since the conductivity of the drift region (the region designed to withhold the blocking voltage of the device) depends on it. The conductivity is defined as:

$$\rho_n = \frac{1}{q\mu_n N_D} \tag{2.4}$$

where μ_n is the mobility of electrons which are a function of doping concentration N_D and temperature. The electron mobility in Si and SiC as a function of the doping concentration is given by:

$$\mu_n(Si) = \frac{5.1x10^{18} + 92N_D^{0.91}}{3.75x10^{15} + N_D^{0.91}} \tag{2.5}$$

$$\mu_n(4H - SiC) = \frac{4.05x10^{13} + 20N_D^{0.61}}{3.55x10^{10} + N_D^{0.61}} \tag{2.6}$$

The electron mobility at room temperature as a function of the doping concentration is plotted in Fig. 2.3.

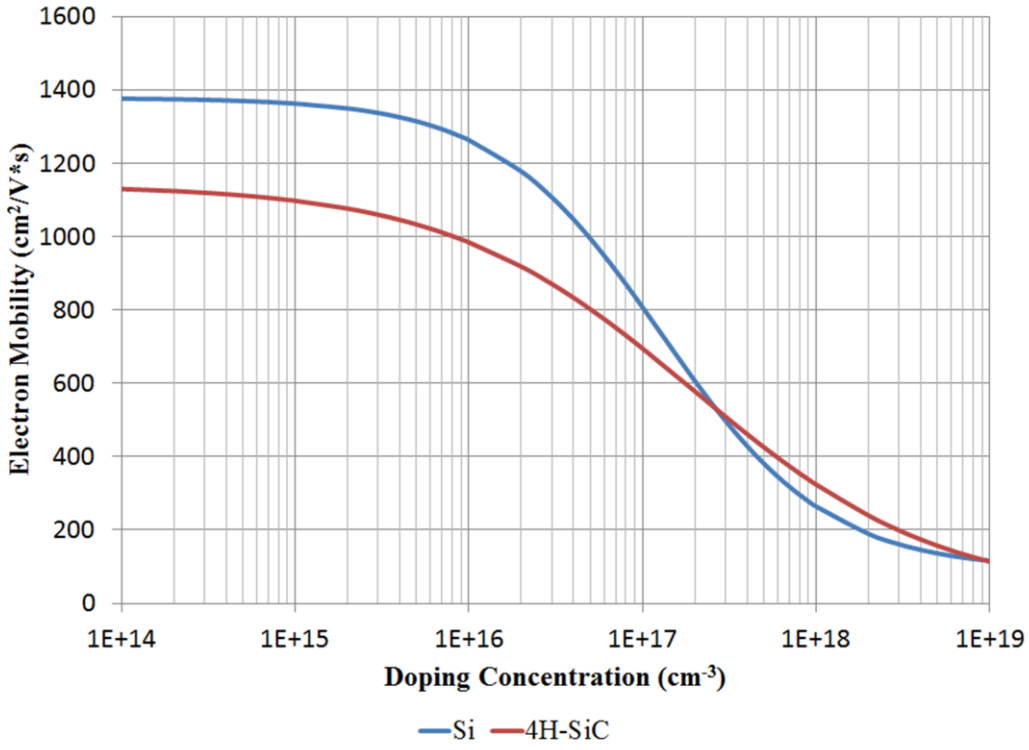


Fig. 2.3 – Electron mobility for electrons in Si and 4H-SiC.

As a function of temperature and at low doping concentrations, the electron mobility in Si and SiC is given by:

$$\mu_n(Si) = 1360\left(\frac{T}{300}\right)^{-2.42} \tag{2.7}$$

$$\mu_n(4H-SiC) = 1140\left(\frac{T}{300}\right)^{-2.70} \tag{2.8}$$

The mobility decreases in semiconductors as temperature increases due to enhanced phonon scattering [14]. This can be observed in the electron mobility for Si and SiC as a function of temperature shown in Fig. 2.4.

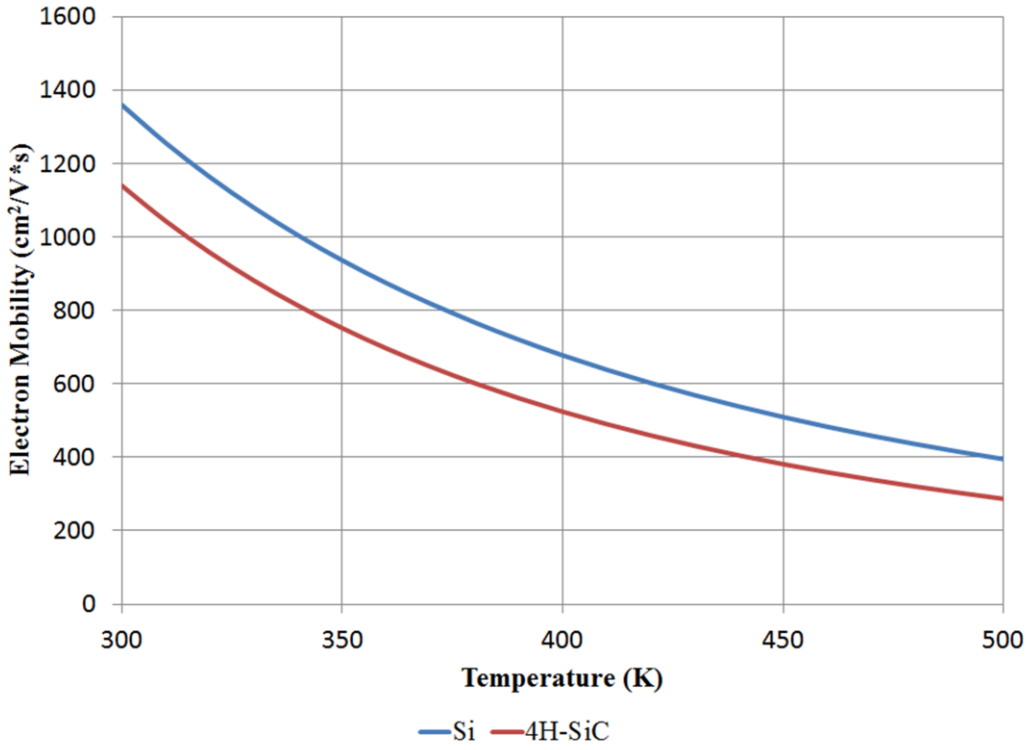


Fig. 2.4 – Electron mobility for electrons in Si and 4H-SiC.

2.2 Challenges in SiC

Even though SiC devices present great advantages over their Si counterparts, their fabrication still presents difficulties. The wide band gap of SiC is definitely one of its most attractive features since it allows high breakdown voltages, but it also causes a low intrinsic carrier concentration. This low concentration presents challenges with the inversion layer mobility and reliability in passivating dielectric layers [18].

The inversion layer mobility challenges are explained by the large band gap of SiC which requires that the energy bands must bend three times more than Si in order to reach inversion. This results in a larger depletion width and hence in a larger surface electric field. At the same time, the surface roughness mobility decreases since it is inversely proportional to the square of the electric field [19]. The high density of traps in the SiC/SiO_2 interface also plays a role in the inversion layer mobility. The traps reduce channel mobility because the trapped electrons cannot contribute to the current flow, and this reduces the inversion-layer charge density at a given bias voltage. These electrons also act as Coulomb scattering sites that reduce the inversion layer mobility at low fields.

Since the surface field of SiC is larger than that of Si, the gate oxide layer must also be able to withstand this electric field. In addition to that, SiC is more sensitive to electrons being injected into the oxide since the barrier height for electron injection into the oxide is larger for Si than it is for SiC [18]. Overall, the SiC/SiO_2 interface is one of the more challenging areas in SiC device fabrication due to all the different problems that arise from it.

The literature reports improvements to some of the previously described challenges. The use of gate oxide processes based on Nitrogen (N) ion implantation and reduced thermal-budget

wet oxidation has shown improvement in the electron channel mobility [20]. In a similar manner, reducing the surface roughness by capped activation anneal with graphitized resist has also resulted in better mobility [21].

2.3 State-of-the-art in SiC Device Fabrication

In the last couple of decades, many high voltage diodes, transistors and even integrated circuits have been experimentally demonstrated in SiC. Most of the research effort, however, has been to fabricate SiC devices to improve the performance and temperature capability of power electronics systems to a point that devices, such as 4H-SiC Schottky diodes, JFETs and MOSFETs, are now commercially available [22]-[24]. This section summarizes key features about the state-of-the-art devices in SiC.

2.3.1 Power devices

Schottky Barrier Diodes (SBD) were the first SiC devices introduced in 2001 [25]. These unipolar devices (only one type of electrical carrier) are used mainly for rectifying purposes and they are currently available with blocking voltages up to 1700 V. These diodes can withstand a 10x blocking voltage as their Si counterparts with the same SiC drift layer thickness [26]. They are commercially offered by a variety of vendors such as Cree and Infineon.

PiN diodes, although not commercially available, have been fabricated and tested at the research level. These bipolar devices have been reported to withstand up to 16 kV and surprisingly handle up to a hundred amps of current [27]. For these devices, forward voltage drop and reverse recovery current are the main features under investigation and improvement.

In addition to SBDs and PiN diodes, power switches are of great interest because of the benefits in different switching applications such as Hybrid Electric Vehicle (HEV) circuitry and

grid applications [27]-[30], where the low on-resistance of a SiC power switch, mixed with the abilities to operate at very high temperatures and block high voltages, make them ideal. SiC Commutated Gate Turn-Off Thyristor (SiC GTO) and Insulated Gate Bipolar Transistors (IGBT) have been reported [27] although focus seems to be on unipolar devices such as MOSFETs and Junction FETs (JFETs) in the 1200 V regime. This is mainly due to the minority carrier lifetime control issues associated with bipolar devices [26].

Currently, 1200 V normally-on and normally-off SiC JFETs are commercially available from SemiSouth [24] and Cree offers the only commercial N-channel SiC MOSFET with a breakdown voltage of 1200 V. As described in the previous section, the SiC/SiO_2 interface issues make SiC MOSFETs still very complicated to fabricate at a production level. Since JFETs do not need an oxide layer they are more commercially available.

There are currently a significant number of publications about power modules using SiC devices such as inverters and chargers [31] [32] where the main benefits of SiC, such as breakdown voltage and temperature capability, are fully exploited.

2.3.2 Integrated Circuits

The literature reports some integrated circuits fabricated either in 6H-SiC or 4H-SiC. Some of these circuits are from times even before the SiC SBDs became commercially available in 2001. Since the development of SiC has been closely related to power electronic modules (due to the breakdown voltage and temperature capabilities) and as SiC fabrication still presents many challenges, most of the reported integrated circuits have been simple digital logic, such as inverters, ring oscillators and flip-flops. The exception has been that of operational amplifiers.

The intent of the digital logic circuitry is usually to use it in a form of a gate driver buffer or in a similar manner to control the power devices in a power module.

One of the most elaborate SiC ICs published is an intelligent gate driver fabricated in a 5 μm, 6H-SiC CMOS process in 1999 [33]. This gate driver consists of digital logic, charge pump and protection circuitry along with a few others. However, even though different circuits were fabricated, only "some of the subcircuits have been measured and operated at temperatures up to 300 °C" [33] defeating the goal of an integrated circuit. Other SiC ICs reported in the 6H poly-type include NAND, NOR and XNOR gates, latches, flip-flops and adders among others [6], [8], and [9], and they have all been individually tested up to 300 °C. 6H-SiC MESFET operational amplifiers have also been reported [34] with operation up to 350 °C, and some others fabricated using 6H-SiC JFET with operation up to 600 °C [7].

More recent literature indicates an apparent shift towards 4H-SiC ICs but still reports the presence of the same fabrication challenges discussed before. The trend in the circuits has remained the same: simple digital circuits, gate driver buffers and operational amplifiers but most of them are fabricated using BJT or JFET (avoiding the oxide layer issues) [35], [36]. This tendency to avoid oxide layers has even been practiced with 6H-SiC devices in digital logic and operational amplifiers fabricated recently by the NASA Glenn Research Center and tested up to 500 °C [37], as opposed to the 6H-SiC CMOS processes from the decade before. The exception in this case is a recently reported NMOS-based enhancement SiC operational amplifier fabricated in a 4H-SiC substrate by General Electric and tested up to 350 °C [38]. At the end, even though SiC processes are still developing and being explored, there has been no attempt to design and fabricate circuits other than digital logic and operational amplifiers, making this SiC voltage regulator truly an advance of the state-of-the-art in the field.

CHAPTER 3: CREE SILICON CARBIDE PROCESS

3.1 Overview

As mentioned before, the main objective of this project is to integrate, in the same 4H-SiC wafer, an existing Cree power MOSFET with low voltage devices used to drive the power device. Since the existing power MOSFET is already fabricated in an n-type substrate, the low voltage devices must be fabricated in the same substrate. Fig. 3.1 shows a cross-section of the integrated substrate as previously described.

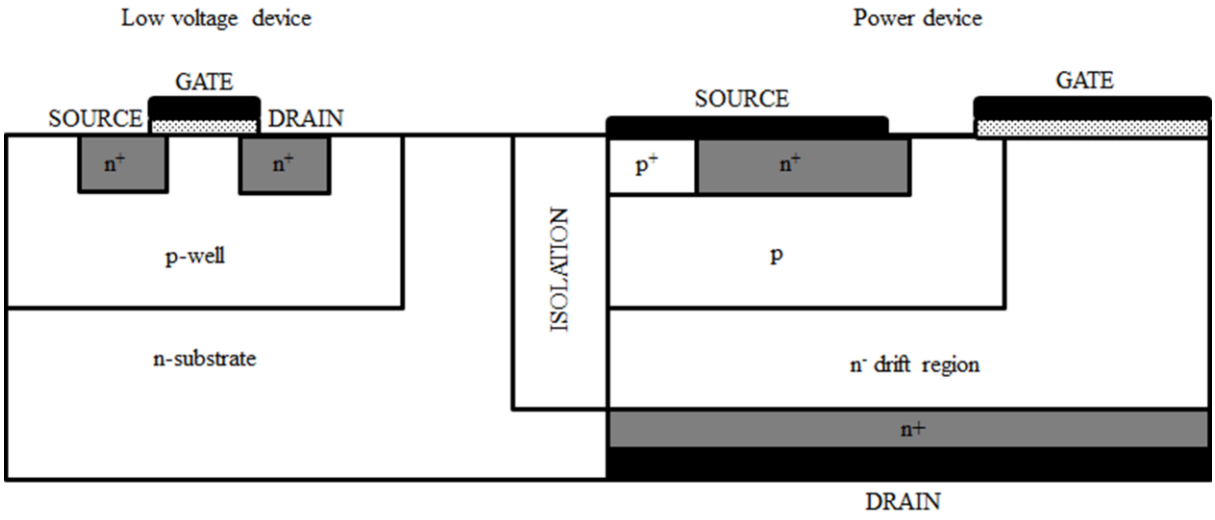


Fig. 3.1 – Substrate integration of power devices with low voltage devices.

The low voltage process is a high risk attempt from Cree to fabricate complete functional integrated circuits in 4H-SiC. It is a 2 μm, all NMOS (depletion and enhancement) process with one metal layer and one poly layer. This latter detail becomes a challenge for designers since the layouts of the circuits will be larger than usual in order to avoid adding parasitic capacitances (due to high resistivity of poly) to the already high risk circuits. The gate oxide thickness in the

process is specified as 40 nm. The enhancement devices are intended to have a positive threshold voltage V_T and the depletion devices (normally-on devices) are intended to have a negative V_T.

Since this process is being built from the ground up, models had to be generated for the circuit designers. For this purpose, a 7 mm x 7 mm test chip with a large variety of transistor sizes, resistors, capacitors and other test structures was fabricated. The smallest transistor used was 8 μm x 2 μm and the largest transistor was 32 μm x 8 μm. Separate 120 μm x 120 μm pads were connected to each device terminal with each pad having an opening of 100 μm x 100 μm for proper probing.

The integration approach shown in Fig. 3.1 indicated the need for a p-well where the low voltage devices would be fabricated. This p-well can be obtained in two different ways [39]:

- Selective ion implantation of the p-well with B or Al ions followed by high temperature annealing – This process is already part of the fabrication process of the power MOSFET, which makes this process easy to implement. The problem with this option is that the diffusion coefficients for SiC are very small even at high temperatures [14]. Therefore, the ion implantation process would aggravate the SiC/SiO2 interface issues previously presented.
- Growth of a p-type epitaxial layer - A p-epi layer can be grown on top of the n-type substrate. This process allows a very well controlled p-doping concentration without aggravating the interface issues inherent to SiC. The disadvantage of this option is that a p-epi layer is not part of the standard fabrication process for the power MOSFET which could result in the increase of the cost of integration.

The test chip was fabricated in three different doping profiles for each type of the p-well (p-epi and p-implant) options in order to determine the best option to proceed with the fabrication of the actual circuitry for the electric charger in this project. In addition to different doping profiles, there were two types of p-epi substrates, one with a threshold voltage adjust feature (to obtain a larger threshold voltage) and one without it. This additional classification in the p-epi susbstrate only concerns the enhancement devices. This was done in order to have better control of the threshold voltage of the devices at high temperatures. The depletion devices in both p-epi substrates have the same doping profile. Fig. 3.2 shows the different types of wafers used for the test chip.

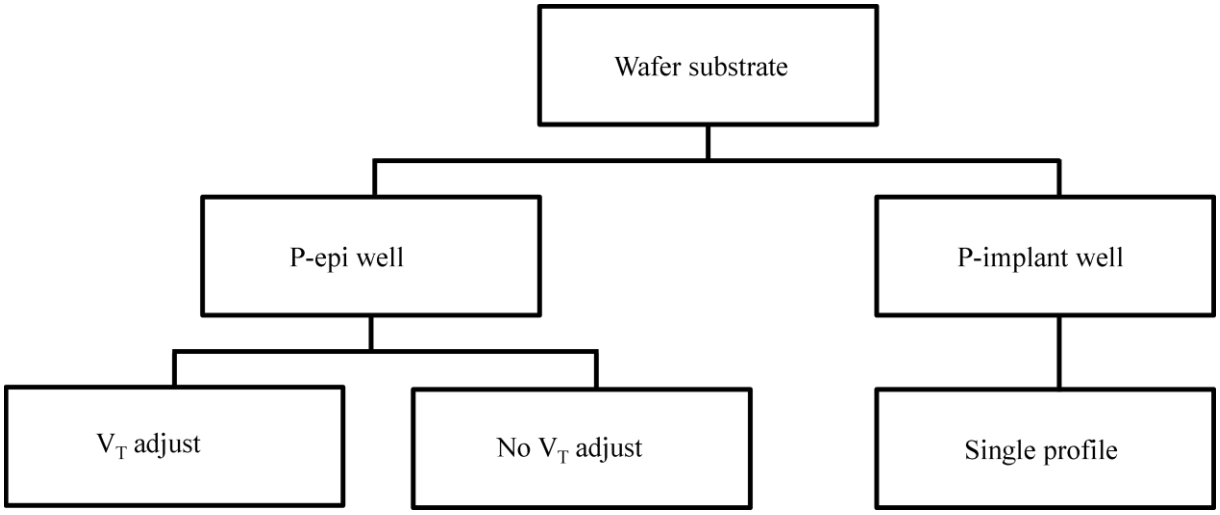


Fig. 3.2 – Different types of wafer used for the low voltage devices test chip.

After characterization of the test chip, the wafers from one of the doping profiles of the p-epi well option with V_T adjustment were selected for the circuits fabrication and hence, to generate the models. More details about threshold voltage and small-signal parameters, such as transconductance and output resistance, will be discussed in the regulator design chapter.

3.2 Limitations

The most obvious limitation with this process is the lack of PMOS devices. PMOS devices, besides being normally-off devices, allow for very low on-resistance when used as pull-up devices. The NMOS depletion devices (normally-on) were the option in this process for these kind of devices, forcing designers to forgo the benefits of complementary MOSFET processes and go back to the first stages of Si circuit design when NMOS-only processes were the norm [40]-[42].

Another important limitation in the process is inherent in the fabrication process of the low voltage devices. Since the goal of this project is to fabricate these devices on a p-well located on top of the n-type substrate (shared with the power MOSFET), the p-well will always have to be at the same potential as the n-substrate in order to reverse bias that junction. At the current stage of the project when integration with the power MOSFET has not yet taken place, the substrate will be connected to the lowest potential in the circuit (commonly ground) and hence, so will the p-well, which could be considered the "substrate" of the low voltage devices. The limitation imposed by this latter fact is that the bulk or body of the NMOS devices must always be connected to the lowest potential of the circuit (ground) rather than the source of the device, as it is usually done to avoid substrate bias voltage (V_{SB}) issues in stacked devices. The equation for the threshold voltage of a MOSFET V_T is given by [43]:

$$V_T = V_{TO} + \gamma[(2\phi_F + V_{SB})^{\frac{1}{2}} - 2\phi_F{}^{\frac{1}{2}}] \tag{3.1}$$

where V_{TO} is the threshold voltage for $V_{SB} = 0$ V, ϕ_F is a physical parameter and γ is a fabrication parameter dependent on the doping concentration of the substrate, the permittivity of the bulk material and the oxide capacitance.

From the previous equation it can be concluded that for stacked devices (where the source is above the lowest potential), there will always be a substrate bias voltage V_{SB} which will result in an increase in threshold voltage. This increase could be quite significant depending on the value for V_{SB} (further details in Chapter 5) and hence, could aggravate the already risky process with considerable limitations in terms of circuit design.

Capacitors also present a challenge in this process. While it is true that capacitors can be external (especially if they are large) to avoid the expense of adding parasitic capacitances and resistances to the circuit, ideally they should be integrated in the circuit. In this process, capacitors are formed using silicon dioxide as a dielectric between a poly layer and a metal layer as shown in Fig. 3.3. An additional gettering layer is added between the oxide and the metal in order to reduce mobile ion contamination as described in the next section. The issues with the capacitor formation process are the thickness of the dielectric, the distance between the poly layer and the substrate, and the high resistivity of the poly layer. This 119 Ω/□ resistivity adds an Equivalent Series Resistance (ESR) to the capacitor, a very important detail to be taken into account by designers, which, as in the case of a voltage regulator, could drastically affect the circuit performance. The effect of the distance between the layers can be explained using the equation for the capacitance of a capacitor C, defined as [44]:

$$C = \varepsilon_r \varepsilon_o \frac{A}{d} \tag{3.2}$$

where ε_r is the relative permittivity of material between the plates, ε_o is the dielectric constant (8.85×10^{-12} F/m), A is the area of overlap of the two plates and d is the distance between them. From the measurements shown in Fig. 3.3 it can be seen that even though the process is not a sub-micron process, large areas would still be needed to obtain small capacitors due to the large

distance between the plates, i.e. a 1 pF capacitor would need an area of about 26,000 μm^2. In addition to the area constraint, the fact that the distance between the poly layer and the substrate is also quite large would create a parasitic capacitor in series of similar value with the intended capacitor in the circuit. Due to all these reasons, if capacitors are integrated in the circuits, it will likely add risks and constraints to the already existing limitations of the process.

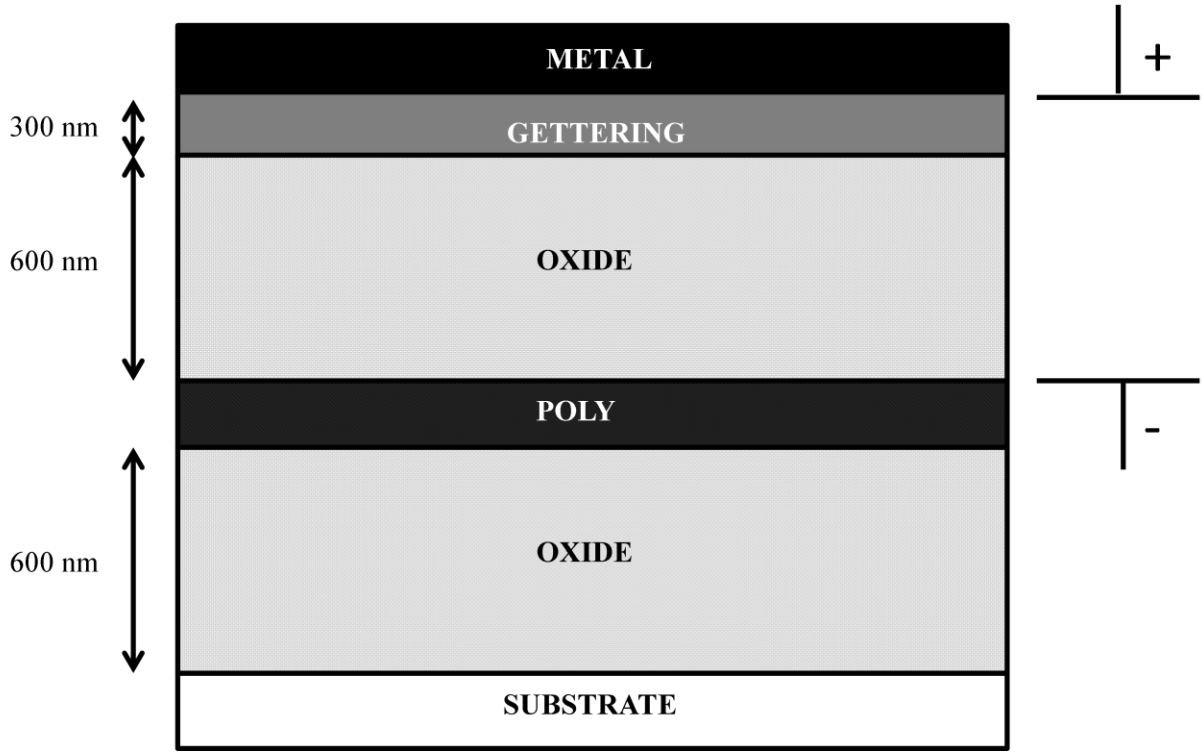


Fig. 3.3 – Layers stack to obtain a capacitor in the Cree SiC process.

3.2.1 Mobile Ion Contamination

Besides the previously foreseen limitations of the process, an unexpected event took place while characterizing the enhancement devices from the test chip. It was observed that the threshold voltage of the devices changed after the first measurement. After numerous measurements the threshold voltage remained the same, but it was already altered from the first measurement. As an example, Fig. 3.4 shows the input characteristics at room temperature on a

32 µm x 2 µm enhancement device which were used to generate device models [39]. It can be observed how, after the first measurement, the threshold voltage decreased. This behavior is explained by mobile positive ion contamination in the field oxide [45]. Due to the presence of alkali metal ions, such as sodium (Na) and potassium (K), in the silicon dioxide, a reduction in the threshold voltage occurs when an electric field is applied to the gate. This is because the ions drift to the Si/SiO_2 interface due to the electric field and hence, they attract electrons making the device to turn on with a lesser gate voltage.

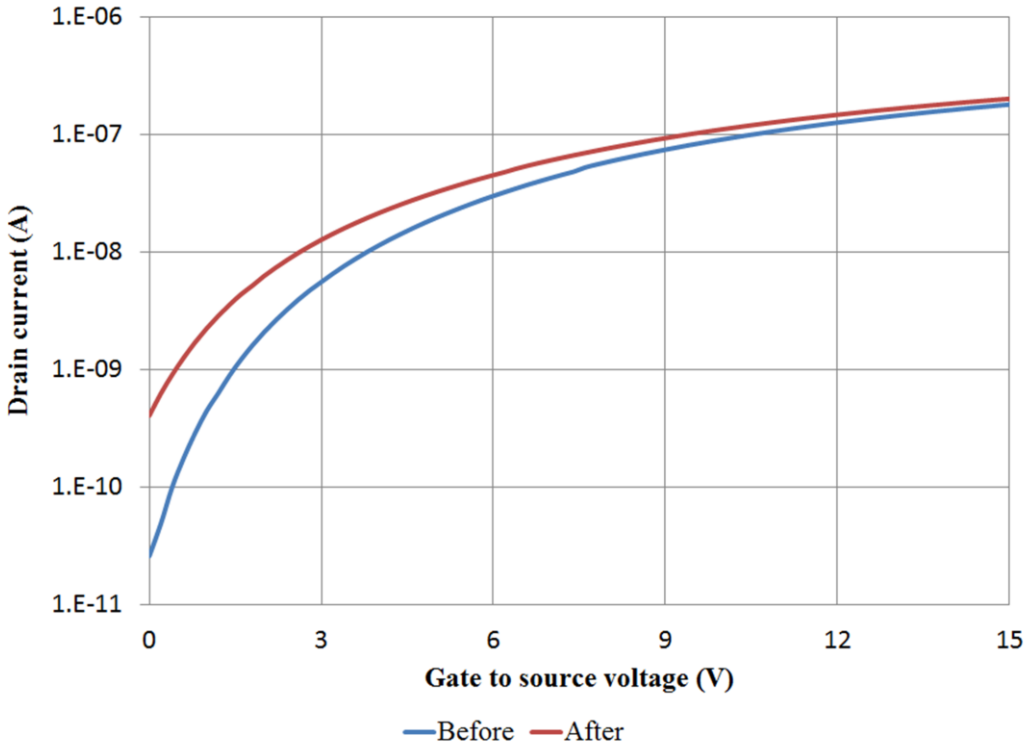


Fig. 3.4 – Shift in threshold voltage after the first measurement due to mobile ion contamination in a 32 µm x 2 µm enhancement device at room temperature.

This phenomenon occurred during testing and created problems decades ago when the manufacturing process was in development. Nowadays there are different techniques [46]-[48],

such as the use of phosphorus doped oxides (known as Phosphosilicate glass, PSG) or silicon nitride (Si_3N_4) top layers to trap the mobile ions and avoid their interference with the device performance. Such a gettering layer, as the one shown in Fig. 3.3, is the one Cree decided to implement in the fabrication of the voltage regulator (and the rest of the circuits for the charger project) in order to avoid any further effect of the mobile ions in the SiC devices.

In order to characterize the devices used to generate the models and minimize the risk of mobile ion contamination, different dies had to be used for different device sizes in such a way that only one measurement was performed on each die for a specific device. The same procedure was repeated for measurements over temperature. There is, of course, the uncertainty of knowing the extent to which these measurements were accurate enough, and therefore it has a significant impact on the generation of the models. For a designer, reliability on the device models is critical since that (aside from process variation) predicts the performance of the circuit after fabrication. This mobile ion contamination and its unknown effects on the models is probably the riskiest factor in the design of this voltage regulator. Unexpected shifts in threshold voltage not accounted for by the models could drastically affect the performance of any circuit regardless of the process used.

3.3 Low voltage models

As mentioned before, the low voltage process developed by Cree consists of enhancement and depletion n-type MOSFETs. The breakdown voltage specified by Cree for these devices is 20 V. Due to the problems faced during the characterization stage of the test chip devices, SiC PSP models for the 32 μm x 2 μm enhancement and depletion type were the first ones to be developed at room temperature in order to meet the schedule for the project. Therefore, the initial design activities were performed using these models. After some issues with the SiC

PSP models were discovered, a Si PSP model for the same type of devices was developed only for room temperature. Eventually, the same model was scaled for the different device sizes, and finally, a discrete temperature model for 125 °C and 225 °C for each size was developed a couple of weeks before the circuits were sent to Cree for fabrication. Figs. 3.5, 3.6, 3.7 and 3.8 show the measured data compared to the model data for the input and output characteristics of the 32 μm x 2 μm enhancement and depletion devices at 25 °C, respectively [39]. From these figures it can be observed how the input characteristics measured data (blue) fit well with the model (red curves) for the enhancement devices, but not so well for the depletion devices. This is due to limitations in the PSP model used for the project [39]. The output characteristics for both devices also suffer from some deficiency, mainly that the drain current never quite follows the measured data. This notorious discrepancy between the model and measured data represents a challenge for designers since the circuits have to be designed with a large range of operating conditions in order to ensure functionality. Designing for very precise analog performance has to be avoided due to the nature of the process and the models.

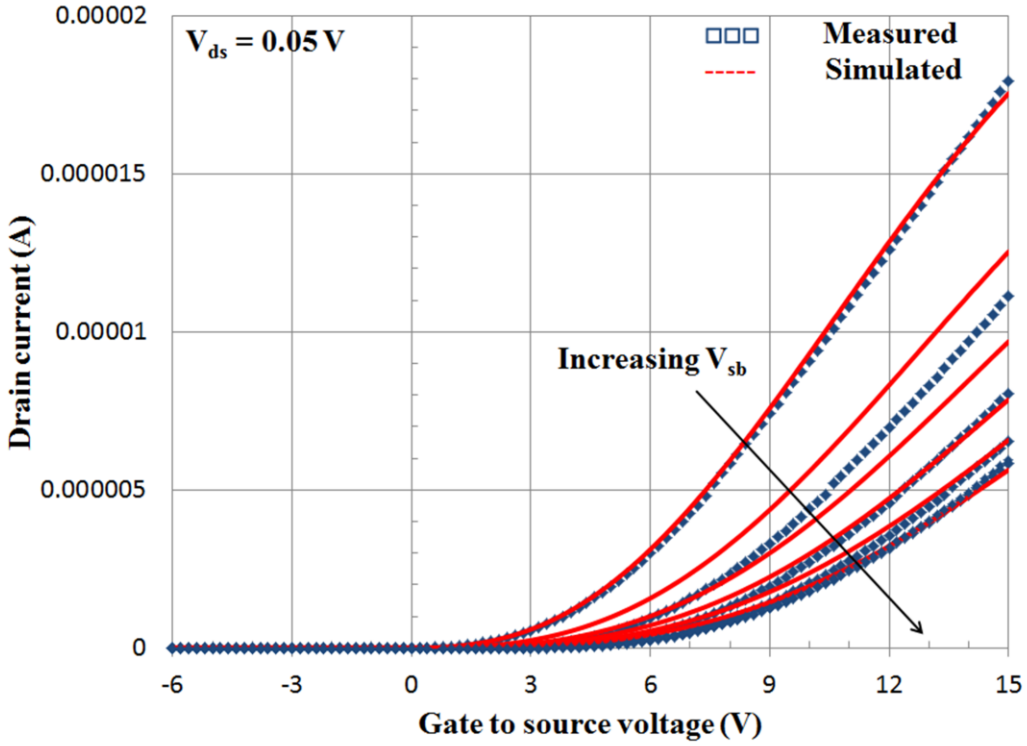


Fig. 3.5 – Input characteristics of a 32 µm x 2 µm enhancement device at 25 °C.

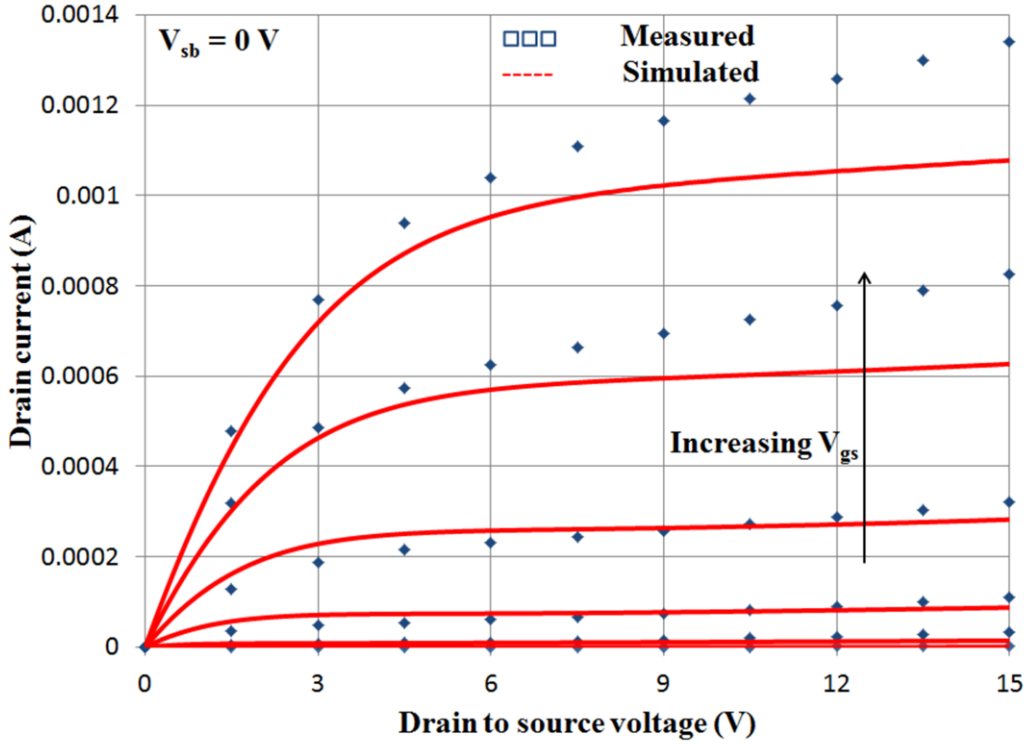


Fig. 3.6 - Output characteristics of a 32 µm x 2 µm enhancement device at 25 °C.

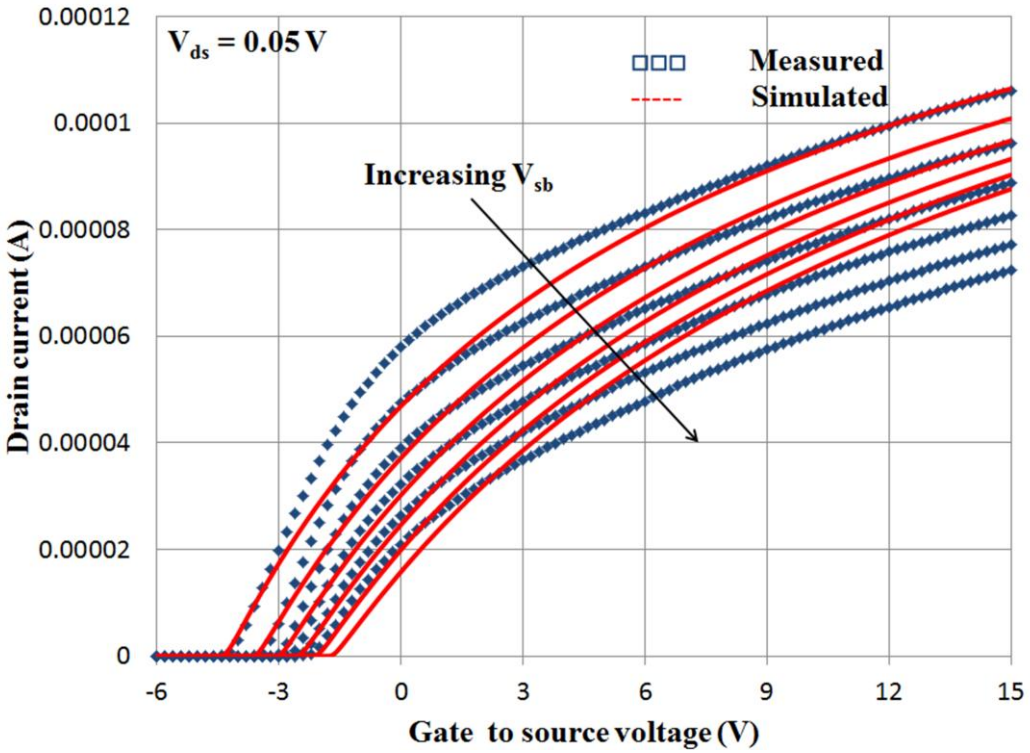


Fig. 3.7 – Input characteristics of a 32 µm x 2 µm depletion device at 25 °C.

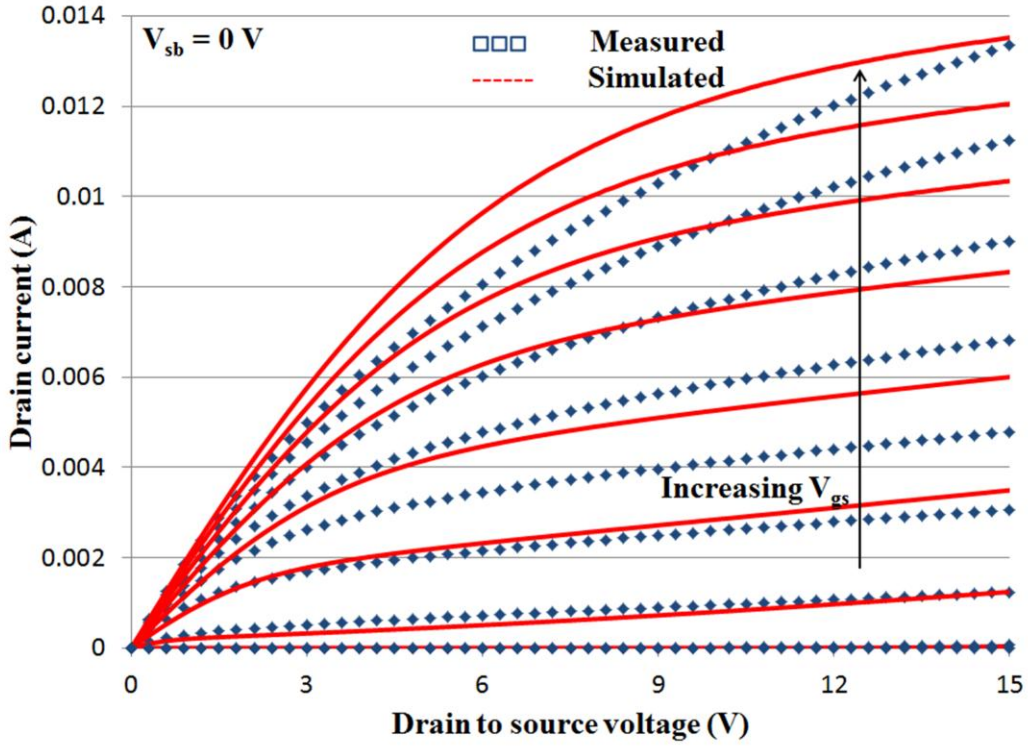


Fig. 3.8 - Output characteristics of a 32 µm x 2 µm depletion device at 25 °C.

Due to the risk factor related to this project, since its beginning, it was required to make decisions related to the voltage regulator design that would maximize the chances of fabricating a working circuit. One of these decisions was to employ only the 32 μm x 2 μm devices in the design of the voltage regulator since the modeling efforts were focused on them since the very beginning, and they were in fact, the first models available. This in addition to the fact that since they have the largest W/L ratio of all the available devices, they would provide the largest current, a factor that was critical in the design of the pass device of the regulator. This section therefore, intends to present the performance details of these devices and how they impacted the design of the voltage regulator. Table 3.1 shows the approximated threshold voltage values for the 32 μm x 2 μm devices obtained from Figs. 3.5 and 3.7.

Table 3.1 Approximated Threshold Voltage Values for the 32 μm x 2 μm Devices at 25 °C using the Low-voltage SiC Models.

$\|V_{SB}\|$ (V)	V_T – Depletion (V)	V_T – Enhancement (V)
0	-4.5	3.4
3	-3.7	4.6
6	-3.1	5.5
9	-2.4	6.2
12	-2.1	6.8
15	-2.0	7.3

The two main small-signal parameters of interest from these devices are the transconductance, g_m, and the output resistance, r_o, of the transistors since they will be used for

the small-signal model of the voltage regulator. Fig. 3.9 shows the input characteristics of a 32 μm x 2 μm enhancement device at 25 °C, 125 °C and 225 °C (right) and the transconductance plot (left) obtained by taking the derivative of the drain current. Fig. 3.10 shows the output characteristics of the same device at 25 °C, 125 °C and 225 °C (right) and the output resistance plot (left) obtained by taking the inverse of the derivative of the drain current. Figs. 3.11 and 3.12 show the same characteristics for a 32 μm x 2 μm depletion device. For simulation purposes, $V_{DS} = V_{SB} = 5$ V for the input characteristics and $V_{GS} = V_{SB} = 5$ V for the output characteristics.

From the input characteristics graphs, it can be seen that the depletion devices have a poor performance at 225 °C resulting in a poor transconductance value. Also, the increase in current with temperature in the enhancement devices is worth noting. In standard Si technology, drain current and threshold voltage decrease as temperature increases. In the current SiC technology, the drain current is strongly influenced by the presence of interface traps at the SiC/SiO_2 interface as discussed in Section 2.2. It has been shown that as temperature increases, the occupancy of interface traps decreases, making more electrons available for conduction [49]. As a result, despite reduction in channel mobility, the overall current in enhancement MOSFETs increases.

From the output characteristics graphs, it can be observed how significant the effects of the body-channel modulation are in this process. The slope of the transistors in saturation is quite large, almost resembling the behavior of a resistor more than that of a transistor. As a result, the output resistance varies continuously, and it is not as stable as in a well-defined Si process. This indicates that for design calculations, approximate numbers for transconductance and output resistance for both - enhancement and depletion devices- will have to be used.

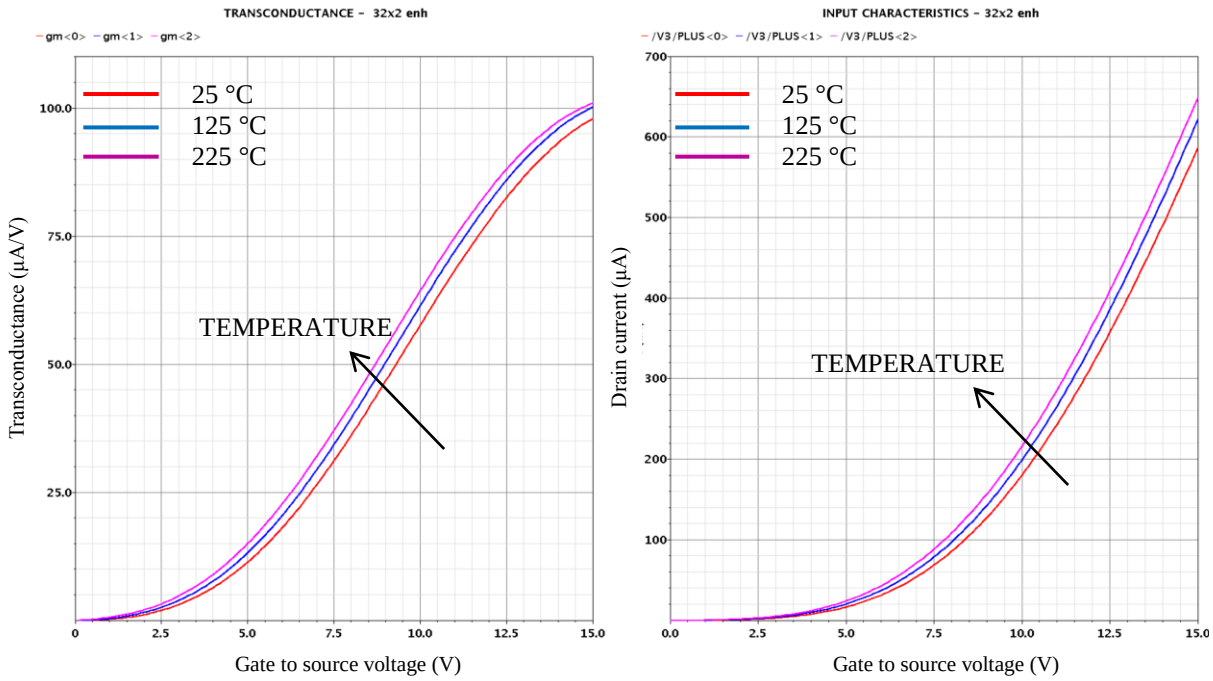


Fig. 3.9 – Transconductance (left) and input characteristics (right) for a 32 µm x 2 µm enhancement device with $V_{DS} = V_{SB} = 5$ V at 25 °C, 125 °C and 225 °C.

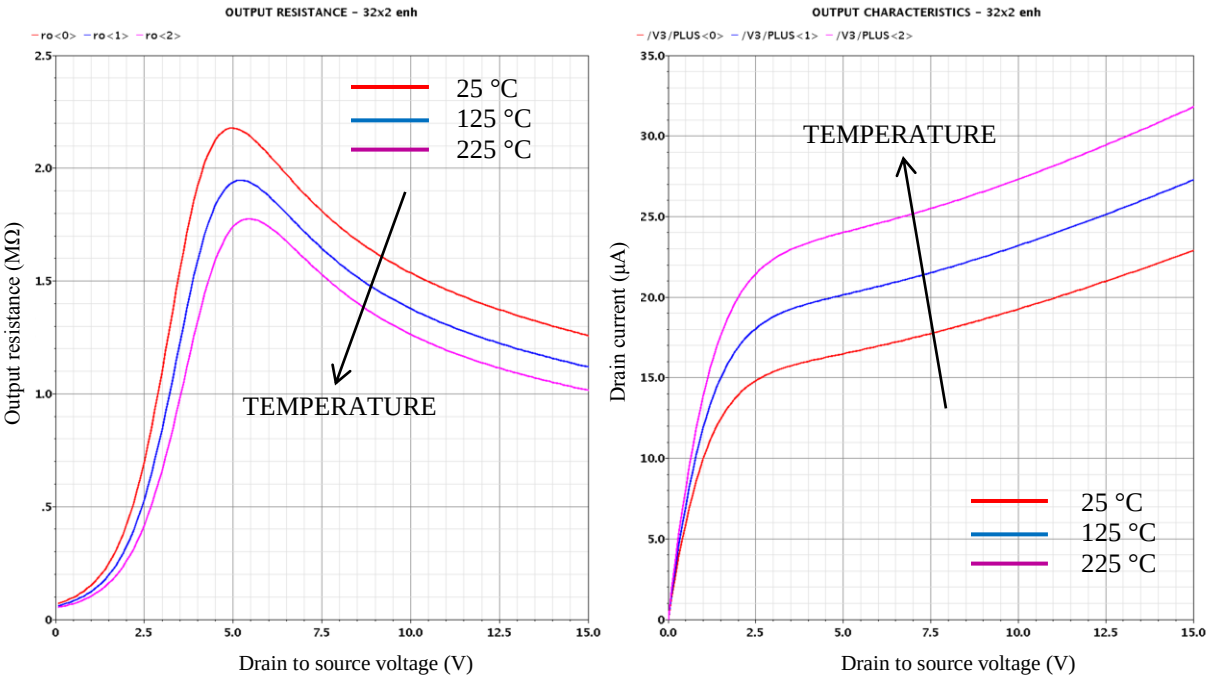


Fig. 3.10 – Output resistance (left) and output characteristics (right) for a 32 µm x 2 µm enhancement device with $V_{GS} = V_{SB} = 5$ V at 25 °C, 125 °C and 225 °C.

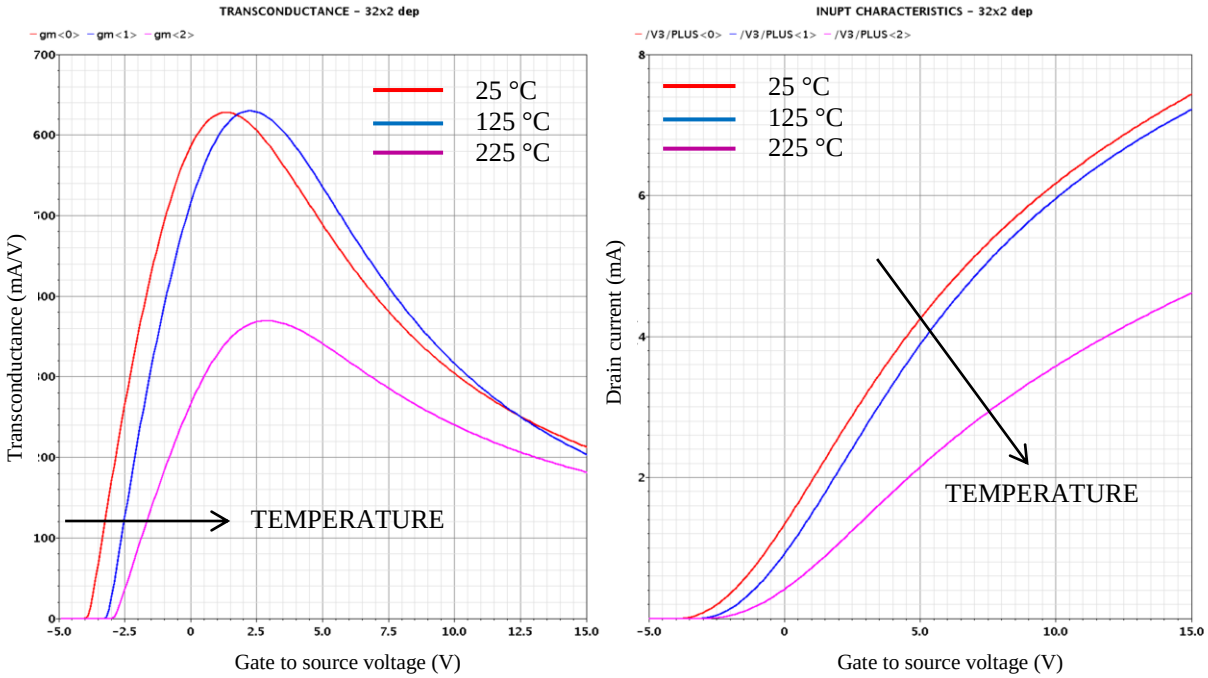


Fig. 3.11 – Transconductance (left) and input characteristics (right) for a 32 µm x 2 µm depletion device with $V_{DS} = V_{SB} = 5$ V at 25 °C, 125 °C and 225 °C.

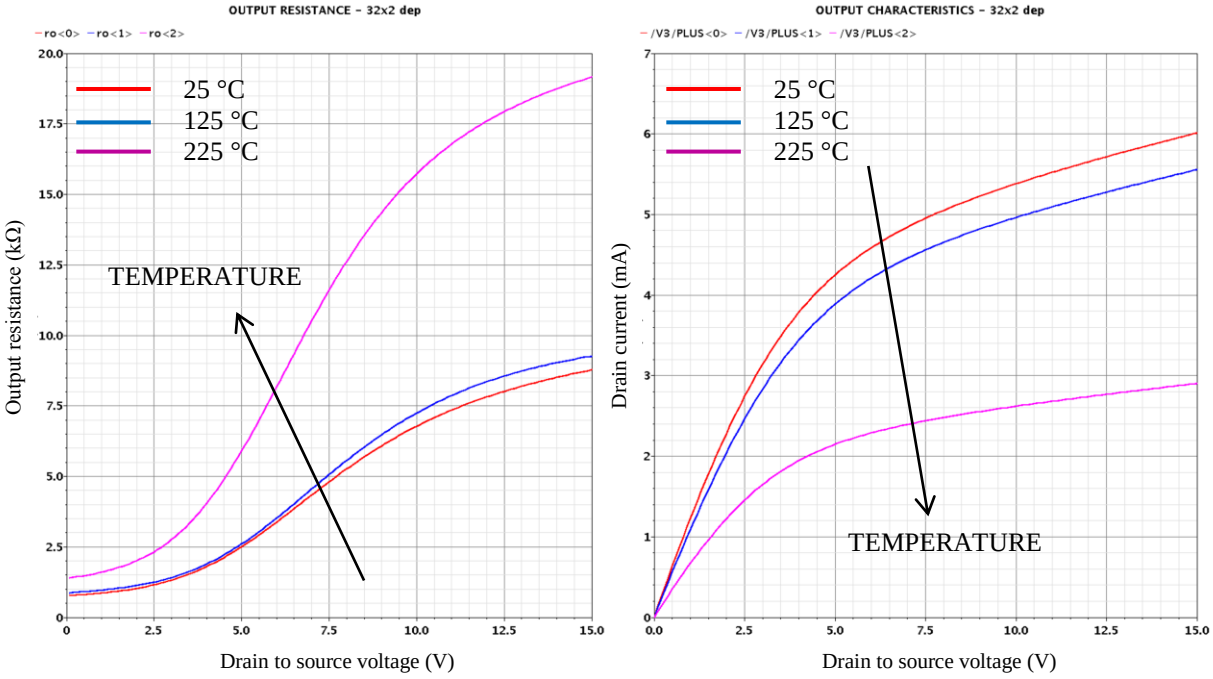
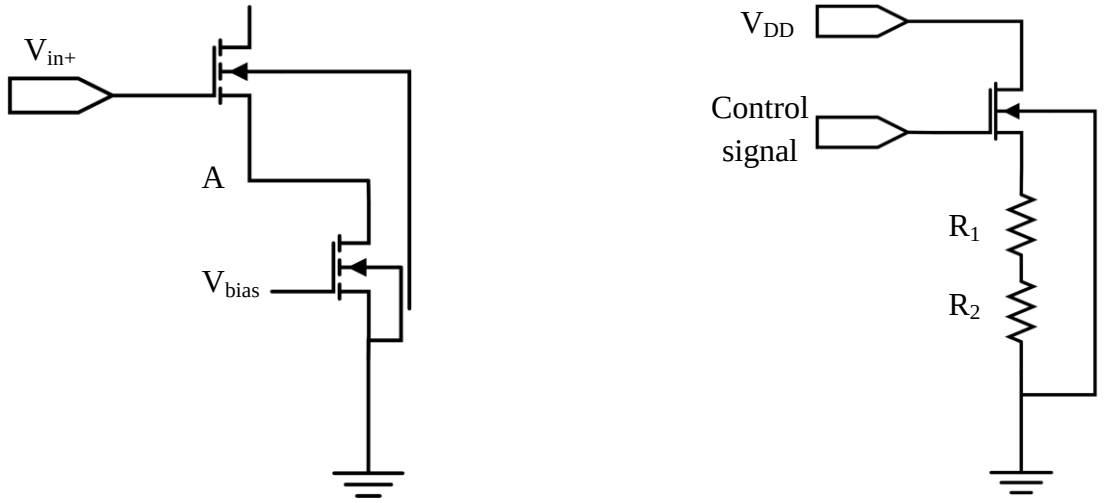


Fig. 3.12 – Output resistance (left) and output characteristics (right) for a 32 µm x 2 µm depletion device with $V_{GS} = V_{SB} = 5$ V at 25 °C, 125 °C and 225 °C.

In addition to temperature, the substrate bias voltage also plays an important role in the performance of the devices as shown in Figs. 3.5 and 3.7. As explained in the previous section, since the substrate connection must always be connected to the lowest potential in the circuit, there will be a substrate bias voltage for stacked devices. More specific examples are the circuits shown in Fig. 3.13. Circuit (a) is a generic tail current circuit for an amplifier with NMOS input devices (only one input is shown). In this case, the input devices will have a substrate bias voltage and hence, their performance will be different to the bottom devices which have the same gate biasing voltage but have their source connected to ground. Circuit (b) is the NMOS depletion pass device of a generic linear regulator in series with resistors used as a feedback network. In this case, the pass device will have a substrate bias voltage equal to the output of the linear regulator, a detail that will seriously impact the design of the regulator in this dissertation.

In the case of the amplifier, assuming a bias voltage for the tail current transistor of about 7 V would result in a V_{SB} of about 5 V for the transistors in the input stage. The difference in drain current and threshold voltage for an enhancement transistor in this input stage with 3 different V_{SB} values compared to the same device with V_{SB} = 0 V can be observed in Fig. 3.14. In the case of the regulator, the difference is more noticeable since VDD is 20 V and the devices in this process are all NMOS. This implies that the highest output voltage of the regulator (measured at the source of the pass device transistor) is VDD-V_T in order to allow the pass device to turn on. For the sake of argument, it is assumed that the output is set to 15 V and that a depletion transistor is used as the pass device in order to take advantage of its negative threshold voltage. This would result in V_{SB} = 15 V and V_{DS} = 5 V. The difference in threshold voltage and current is quite noticeable as shown in Fig. 3.15. It can be noticed that when V_{SB} = 15 V, V_T is about half of its normal value.



(a) (b)

Fig. 3.13 – Examples of stacked devices in a) an n-type input stage amplifier and b) NMOS depletion pass device in a generic linear voltage regulator.

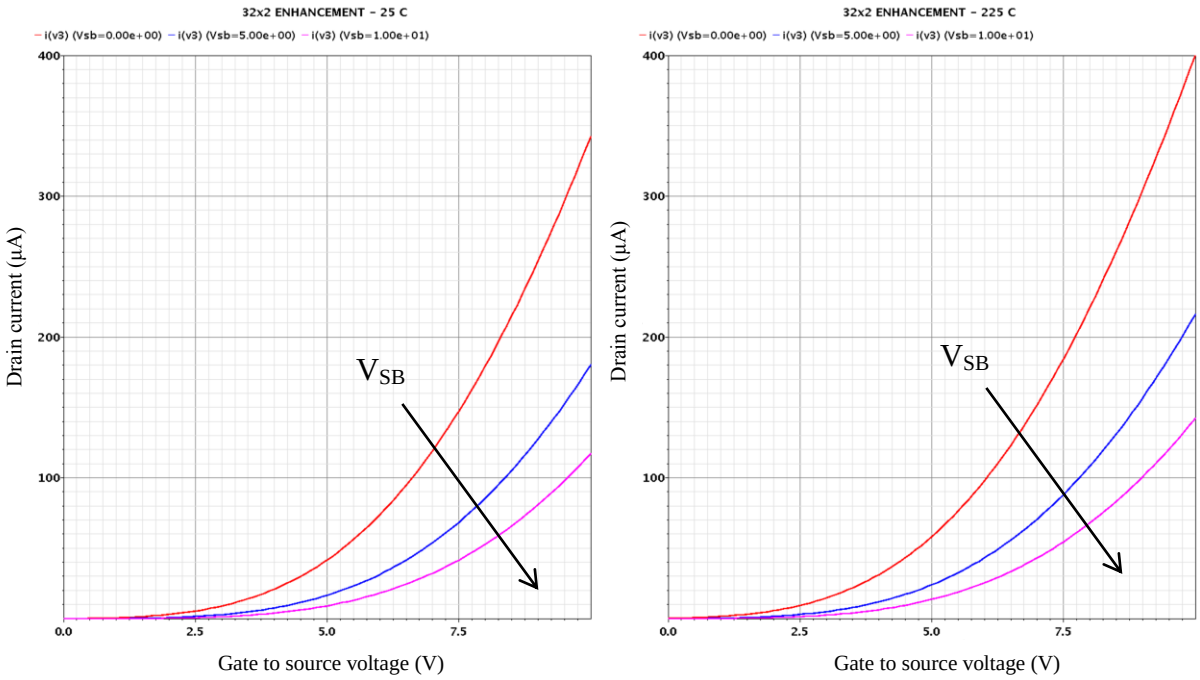


Fig. 3.14 – Input characteristics for a 32 µm x 2 µm enhancement device with V_{DS} = 5 V for V_{SB} = 0, 5 and 10 V at 25 °C (left) and 225 °C (right). The increase in threshold voltage due to the increase in V_{SB} can be observed. The threshold however, decreases, as temperature increases as it occurs in Si.

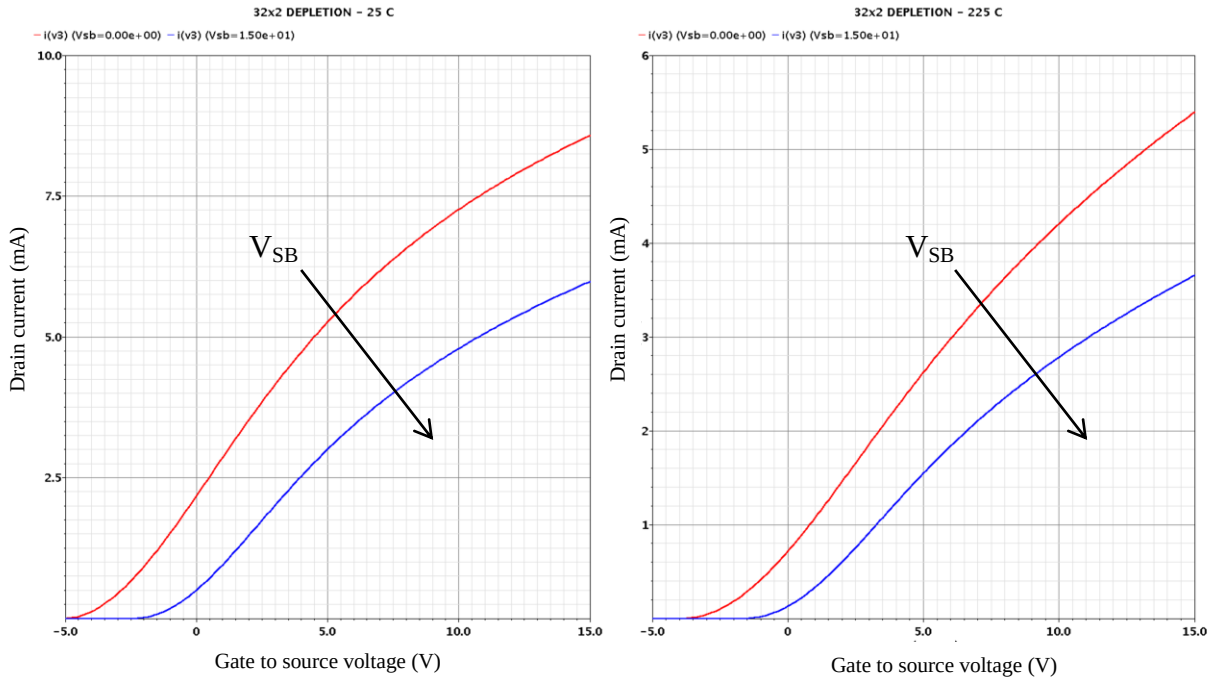


Fig. 3.15 – Input characteristics for a 32 µm x 2 µm depletion device with V_{DS} = 5 V for V_{SB} = 0 and 15 V at 25 °C (left) and 225 °C (right). The increase in threshold voltage due to the increase in V_{SB} can be observed.

The gate capacitance is another parameter of interest - particularly for the design of a linear regulator. As will be discussed later on, the gate capacitance of a pass device in a generic linear regulator is a key component in its frequency response and stability. In this process, the total gate capacitance C_{GG}, seen at the gate of the device was measured for the 32 µm x 8 µm devices [39]. The actual measurement though, was taken on a much larger 20 x 50 µm x 50 µm C-V test structure and then scaled down for each specific device. Figs. 3.16 and 3.17 show the measured and model data for the gate capacitance of a 32 µm x 8 µm enhancement and depletion device respectively. The C-V characteristic of the enhancement device shows a “hook and ledge” behavior due to the large density of interface states in the device [50].

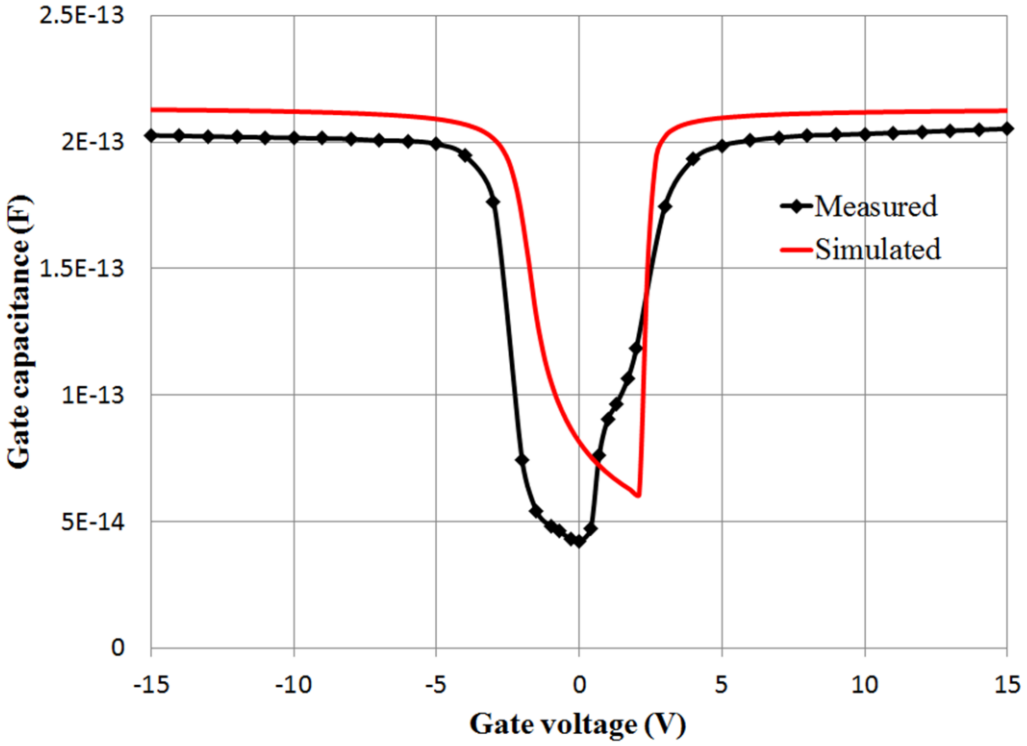


Fig. 3.16 – Gate capacitance measurements of a 32 µm x 8 µm enhancement device.

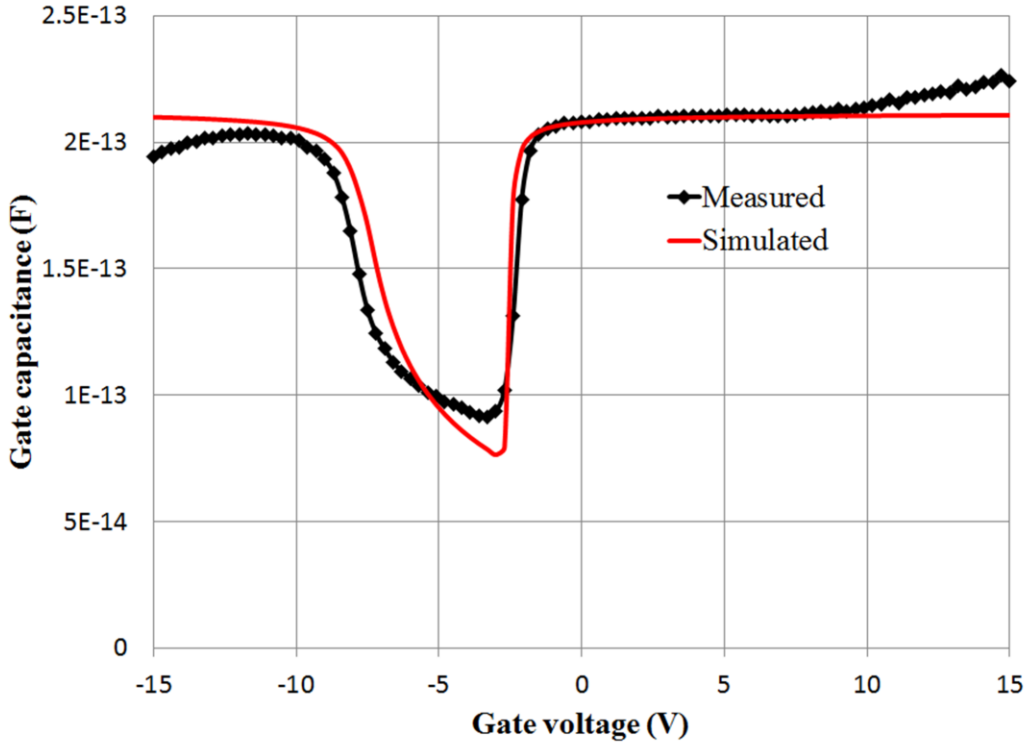


Fig. 3.17 – Gate capacitance measurements of a 32 µm x 8 µm depletion device.

As mentioned earlier, the gate capacitance value of the pass device is critical in the design of a linear regulator. Since the pass device will be in a configuration like the one shown in Fig. 3.13 (b), there will a substrate bias voltage V_{SB} affecting the device. The increase in substrate bias voltage will actually decrease the value of the gate capacitance C_{GG}. Since the source and drain regions of the devices are small compared to the bulk region, C_{GG} is mostly dominated by the gate to bulk capacitance C_{GB}. Then, as V_{SB} increases, the depletion width under the gate of the device will increase as well. This depletion width, in terms of capacitance, is the separation between the layers (gate and bulk) of the parasitic capacitor C_{GB}. Hence, based on (3.2), as the distance increases, the capacitance will decrease. Fig. 3.18 shows how the increase in V_{SB} affects the total gate capacitance.

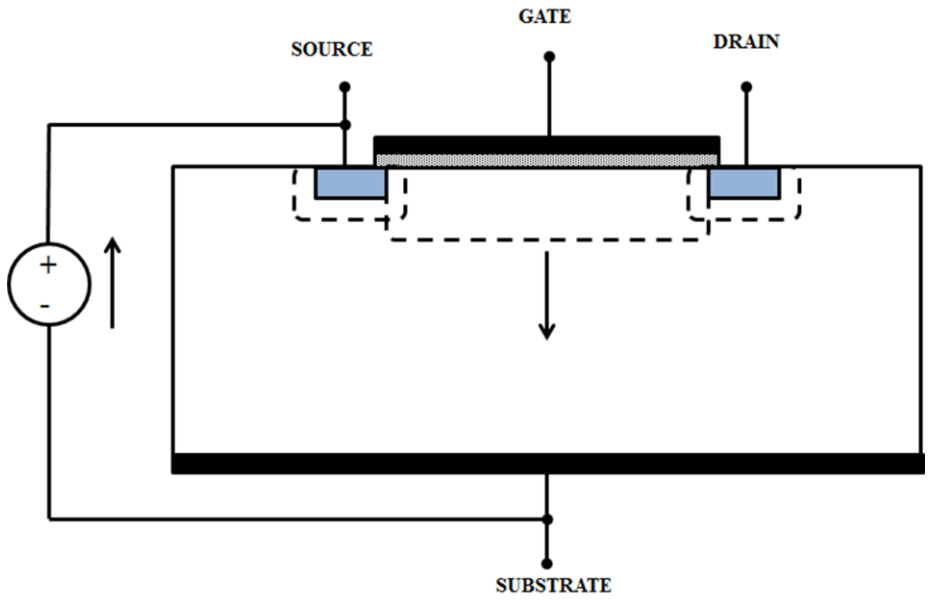


Fig. 3.18 – Effect of the substrate bias voltage in the total gate capacitance.

In order to quantify this effect, an RC circuit using the gate capacitance of a 32 μm x 2 μm depletion device with multiplicity of 2000 was simulated. The multiplicity is necessary in

order to account for the large load current typically delivered by linear regulators. The drain of the device was left floating in order to make sure that only the gate capacitance of the device was the only capacitance seen by the input signal. A 10 MΩ resistor was used in order to maximize the time constant τ=RC of the circuit. A 1 Hz, 0-20 V_{p-p}, 50% duty cycle and $t_{rise} = t_{fall} = 100$ ns square signal was used as input signal. The delay between the input signal and the output signal (measured at the gate of the device) will provide the value for the gate capacitance, taking into account that one time constant is what takes for the gate capacitance to charge to 63.2% of the input signal value [44]. Fig. 3.19 shows a schematic of the RC circuit and Fig. 3.20 shows the results with $V_{SB} = 0$ V and $V_{SB} = 15$ V. Table 3.2 summarizes the results.

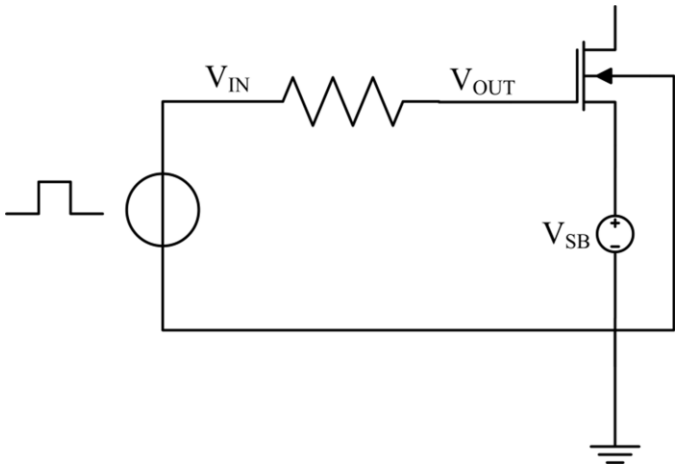


Fig. 3.19 – Test circuit to measure the effect of the substrate bias voltage in the gate capacitance. The depletion device has a multiplicity of 2000.

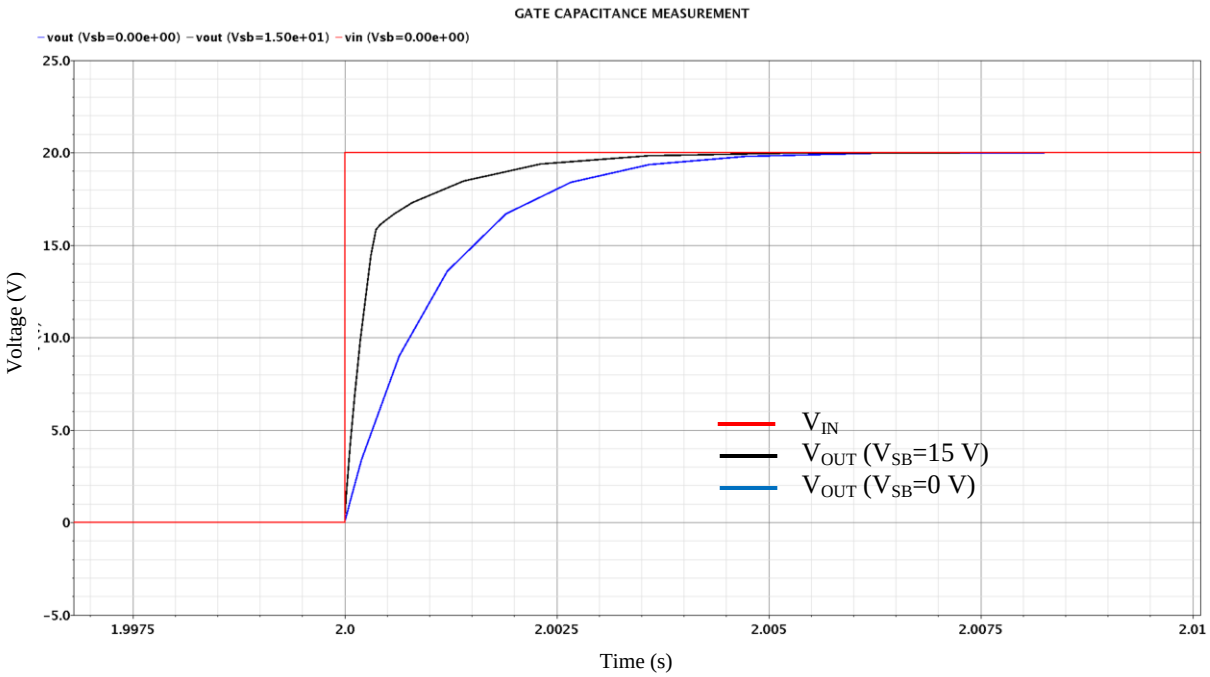


Fig. 3.20 – Effect of substrate bias voltage on the gate capacitance using a 32 µm x 2 µm depletion device at 25 °C. The red curve is the input signal, the blue curve is the output signal at V_{SB} = 0 V and the black curve is the output signal at V_{SB} = 15 V.

Table 3.2 – Gate Capacitance Measurements of a 32 µm x 2 µm, M=2000 Depletion Device.

$\|V_{SB}\|$ (V)	τ (µs)	R (MΩ)	C (pF)
0	1098	10	109.8
15	265	10	26.5

From Table 3.2 it can be seen that the substrate bias voltage affects the gate capacitance by a factor of approximately 4. This detail was taken into account when analyzing the frequency response of the regulator. A similar, but lesser, effect in the gate capacitance should be expected in other transistors in the regulator with a non-zero substrate bias voltage.

This section has presented the issues associated with the models used to design the linear voltage regulator. These issues are related to the limitations in the current SiC technology as well as the limitations in the process specifically used to design the circuit. These risks, and the uncertainty level of the process and the models, were considered when the regulator was designed. Relaxed specifications and simplified techniques were adopted in order to minimize the risks.

CHAPTER 4: VOLTAGE REGULATORS

Power management is highly important in any electrical circuit. From the IC point of view, the designer tries to foresee any changes in the power supply for the circuit and designs accordingly. However, there could be significant variations in the power supply depending on loading or other conditions that could be very difficult to predict but which could drastically affect the performance of any circuit. Voltage regulators prevent this from happening by providing a very well defined steady voltage for a specific maximum load. Depending on the application, a properly selected voltage regulator can avoid any failure due to power supply variations.

Voltage regulators could be generally classified as linear or switching. Linear regulators are also called series regulators due to the fact that the pass element is in "series" between the input (the supply that is being regulated) and the load (the regulated output). The term "linear" refers to the fact that the current flow (from the pass device) and the control (the signal driving its gate) are continuous in time [1]. Due to the same reason, the output of a linear regulator cannot exceed its input. Switching regulators, on the other hand, can accommodate AC and DC inputs and outputs. From this, it can also be concluded that their circuits tend to be more complex. They are also larger due to the need of inductors. However, depending on the topology, switching regulators can deliver an output larger (boost converter) or smaller (buck converter) than its input. This allows a wide range of options for the switching regulator outputs. The voltage regulator discussed in this document is a linear type but a brief discussion about switching regulators will be presented for reference and comparison purposes.

4.1 Switching regulators

These types of regulators can handle Alternating Current (AC) and Direct Current (DC) input and output voltages. These types of conversions require, in many cases, the use of inductors, transformers, capacitors and diodes that, besides the actual switching devices and depending on the type of regulator and application, make the circuits bulkier and more complicated than linear regulators. From the IC point of view, as it pertains to this research, DC-DC converters are then the most relevant types of switching regulators.

There is a large variety of switching regulators but generally, they can be classified into the following main types:

- Buck – when the output produced is smaller in magnitude than the input.
- Boost – when the output produced is larger in magnitude than the input.
- Buck-boost – when the output produced is of opposite polarity of the input.
- Flyback – when multiple outputs, larger and smaller in magnitude than the input, are produced.

A Pulse Width Modulated (PWM) conditioner is a typical block of a switching regulator. The PWM controller is a combination of an analog signal from an error amplifier with a PWM Analog-to-Digital converter (ADC) that is used to control the “on” time of the switching devices in the regulator [1]. These switching devices usually need to be driven at high frequencies since this reduces the size and weight of the passive components in the circuit [2]. However, as a result of this fast switching, noise is introduced in the circuit. A positive feature of the switching devices is that their voltage drop is smaller than the voltage drop of a pass transistor of a linear regulator resulting in a reduction of dissipated power [1]. This links directly to the fact that switching regulators are more power efficient than linear regulators.

Efficiency η is defined as the ratio of the output power to the input power. The input power includes the power consumed by the regulator as well as the power delivered to the load.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{REG+}P_{OUT}} \tag{4.1}$$

This equation indicates that the quiescent current in a linear regulator I_Q (the current not flowing to the load) and the difference between the input and output voltage makes the circuit less efficient. An expanded version of the efficiency equation helps visualize this relationship.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_{OUT\times}V_{OUT}}{(I_Q + I_{OUT})V_{IN}} \tag{4.2}$$

This implies that minimizing the quiescent current will improve efficiency, but it will still be limited by the ratio of the output voltage V_{OUT} to the input voltage V_{IN}. As mentioned previously, the voltage drop across the pass device of a linear regulator is larger than for the switching device in a switching regulator, and as a result, the efficiency of linear regulators is lower. Decreasing the difference between the input and output voltage will obviously increase the efficiency if the quiescent current is kept small compared to the output (load) current.

4.2 Linear regulators

The voltage regulator in this investigation is a linear regulator. This allows for a simpler and more IC oriented design with a broader range of applications. A basic linear regulator consists of five main blocks shown in Fig. 4.1:

- Error amplifier – This circuit monitors the output for any changes in the load condition and generates an error signal that is sent to the gate of the pass device in order to compensate for the change.
- Pass device – This device is in charge of delivering the current to the load. This is usually a very large transistor (BJT or MOSFET) with a very large gate capacitance that plays an

important role in the stability of the regulator. The size of the device depends on the load rating of the regulator. The pass device could be better explained as a load-variant resistance adjusted by the error amplifier.

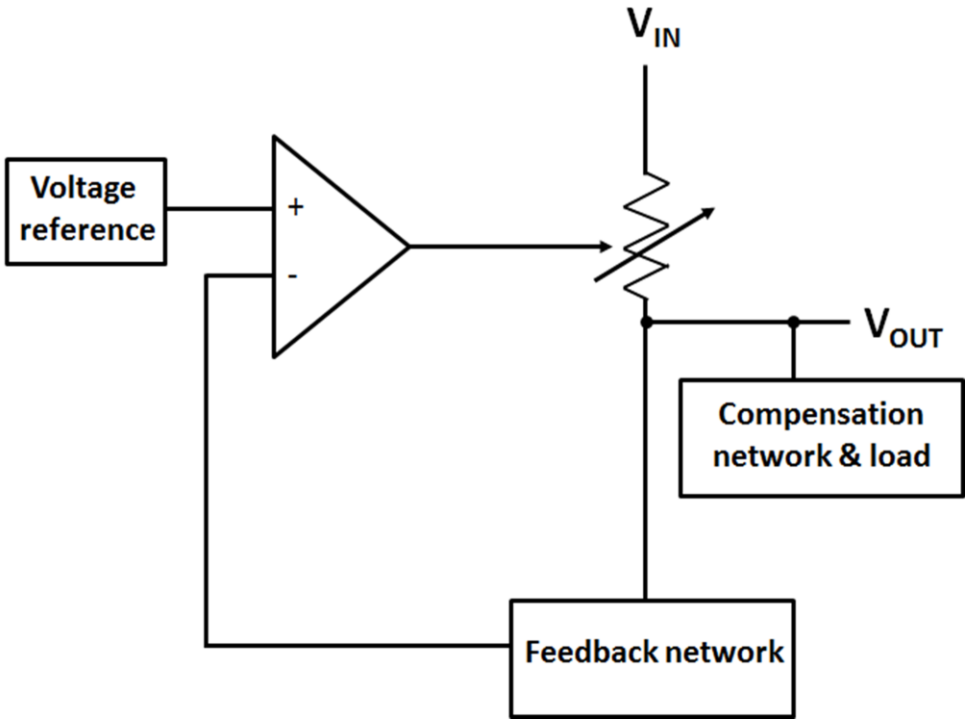


Fig. 4.1 – Block diagram of a linear voltage regulator.

- Voltage reference – This constant voltage reference is constantly being compared by the error amplifier to the signal from the feedback network. This is a very critical block of the regulator since variations in this voltage reference, due to temperature or any other environmental effects, will directly impact the output of the regulator and hence its performance. These voltage references are usually designed around Si bandgap references due to their stability over temperature and other events.
- Feedback network – This is mainly composed of two resistors in series with the pass device. The output of the regulator is located between the top resistor and the pass device

and the connection point between the two resistors provides the feedback signal monitored by the error amplifier. Regulators employ a negative feedback loop meaning that a decrease in magnitude in the feedback signal will result in a change in signal from the error amplifier to the pass device to increase the output voltage.

- Compensation network – In order for the regulator to be stable over frequency, either an external or an internal network (mainly composed of a large capacitor) is needed. The key role in the selection of the capacitor is its ESR which will also play an important role in the frequency response of the regulator.

In addition to these blocks, there are a number of features added to voltage regulators in order to enhance their performance. Some of these include, but are not limited to, overcurrent protection, startup circuitry, thermal shutdown and open/short load detection and will be discussed in Section 4.3. These features are implemented by cleverly designed, sensitive and precise circuits which have been possible due to the maturity, reliability and technological advances of Si manufacturing process.

Linear regulators could generally be classified based on the amount of power they are able to deliver to the load, the type of frequency compensation implemented and the pass device dropout voltage. Table 4.1 shows this classification [1].

Table 4.1 – Generic Linear Regulators Classification

FEATURE	CLASSIFICATION	
Power	High if $I_{LOAD} > 1$ A	Low if $I_{LOAD} < 1$ A
Compensation	External	Internal
Dropout	High if > 0.6 V	Low if < 0.6 V

Power

The amount of power needed from a voltage regulator depends on the application. The literature indicates that the maximum output current for linear regulators range from 50 – 300 mA. Most commercial linear regulators also fall within that range; although, there are also a few available in the 1 – 3 A range [51]. As mentioned before, the issue with linear regulators is that they are considered less efficient than switching regulators and at high power applications, this disadvantage worsens. A common technique, to take advantage of both types of regulators in a system, is to use one master switching regulator and then make use of linear regulators at the load locations. This technique is called point of load (PoL) regulation [1] and it is widely used in complex systems.

Compensation technique

This compensation has to do with the location of the dominant pole in the frequency response of the regulator (more details in Section 4.2.2), but not necessarily the location of the capacitor used to stabilize the regulator. If the dominant pole is located at the output of the regulator, then it is considered externally compensated. If the dominant pole is located in an internal node, then it is internally compensated. The confusion here arises from the fact that the external capacitor located at the output of the regulator is commonly the one used to stabilize the system, that is, to generate the dominant pole. This capacitor, however, even if it is connected to the output of the regulator, can be part of the IC using additional techniques to ensure frequency compensation. In that case, the regulator is still considered to be externally compensated. The literature also reports numerous capacitor-less linear regulators [52]-[54]. In these cases, the dominant pole is generated by an internal capacitor but still connected to the output of the regulator.

Dropout voltage

This is defined as the minimum difference between the unregulated input supply and the regulated output supply that guarantees proper voltage regulation. Dropout voltage increases dissipated power which is an undesired situation. Current commercial low-dropout voltage regulators (LDO) offer dropout voltages as low as 30 mV [51] which minimizes drastically the amount of dissipated power. This is effectively achieved by the use of PMOS transistors as the pass device (unavailable in the Cree SiC process) or by the use of NMOS transistors as pass devices in conjunction with charge pumps. This latter technique, however, usually makes use of capacitors and clock signals in order to achieve the performance and features needed to drive the NMOS pass device. Such requirements would worsen the risks already presented in this process.

4.2.1 Specifications

The performance of a linear regulator is determined mainly by its response to changes in its input and load. Even though these specifications are DC parameters, the overall AC response of the regulator is of particular interest since it reflects its stability. This section intends to provide a description of both DC and AC specifications for linear regulators.

Load regulation

Load regulation (LDR) is defined as the change in DC output voltage as a response to changes in the DC load current. It is, in other words, the output resistance of the regulator ($R_{o\text{-}reg}$) [55],

$$LDR = R_{o-reg} = \frac{\Delta V_{OUT}}{\Delta I_{LOAD}} = \frac{R_{o-pass}}{1 + A_{OL}\beta} \tag{4.3}$$

where $R_{o\text{-}pass}$ is the output resistance of the pass device, A_{OL} is the open-loop gain of the regulator and β is the feedback gain. An ideal linear regulator should show no change in its output voltage when there are changes in the load for which it is designed. In reality, this is not

true since the output of the voltage regulator will need a finite amount of time to respond to changes in the load. During this time, its output will change until the regulator starts to respond. In a system level, the parasitic resistance, inductance and capacitance introduced by wires and board connections will affect the load regulation performance since they will increase the time for the regulator to respond.

Line regulation

Line regulation (LNR) is defined as the change in DC output voltage with respect to changes in the DC input voltage. Power Supply Rejection (PSR), often mistaken with line regulation, includes the entire frequency spectrum. It is usually specified for specific frequencies, i.e. 30 dB at 1 kHz.

The effects of power supply variation in a linear regulator come from the supply for the regulator itself as well as from variations in the voltage reference, V_{REF}, used by the error amplifier (see Fig. 4.1). Since the regulator is a negative feedback loop, where the difference between the variations of V_{OUT} and V_{REF} are constantly amplified, changes in V_{REF} due to power supply variation become significant in the performance of the regulator. In the same manner, any other factors, such as temperature variations, that affect V_{REF} will affect the performance of the regulator. The voltage regulator in this dissertation will make use of an external reference in order to mitigate additional risks that could affect the performance of the regulator. More details about this are discussed in the regulator design chapter.

Quiescent current

Quiescent current, I_Q, is defined as the DC current flowing through the feedback network. It is important for power dissipation calculations since it is constantly flowing regardless of the

load. Ideally, I_Q should not change with variations in the load although in practice it varies due to the changes in resistance of the pass device and the load.

Phase margin

Phase margin is used to measure the stability of the regulator. An unstable regulator will present undesired oscillation in the output voltage. Literature indicates acceptable phase margins are usually at least 60 degrees [56]. More detailed information about stability and phase margin is discussed in Section 4.2.2.

Transient response

Typically, the transient response of a regulator is the behavior of the circuit to noise either from a switching load or a switching supply. The worst case scenario (and the most commonly tested) is when the load current suddenly changes from its lowest rated value to its highest one. Fig. 4.2 shows the typical transient response of a 15 V linear regulator to a load-current step of 3 A.

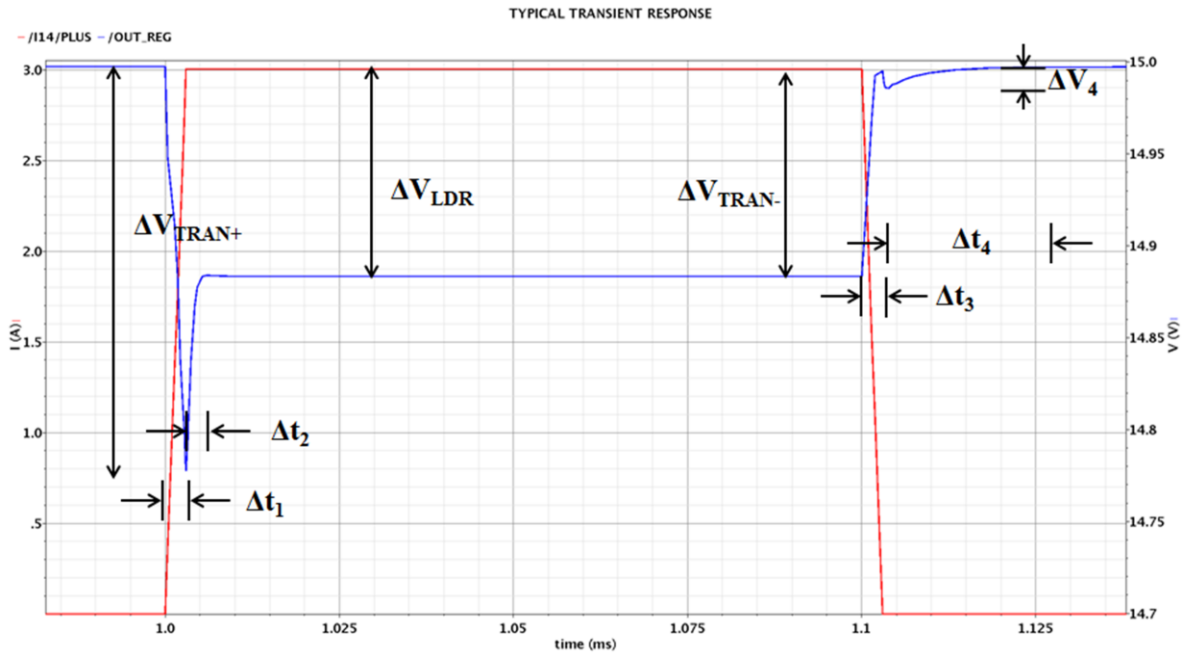


Fig. 4.2 – Typical response of a linear regulator (blue) to a sudden load current change (red).

In order to better understand the different transitions shown in Fig. 4.2, a more detailed schematic of a linear regulator is shown in Fig. 4.3. In this case, the feedback (R_1 and R_2) and compensation networks (C_{OUT} and R_{ESR}) are clearly indicated. Also, since a regulator provides power to different circuits, such circuits usually make use of decoupling capacitors. This capacitance is represented as C_b, and depending on its value, could play an important role in the AC performance of the regulator.

The transient response to a load-current step as the one shown in Fig. 4.2 starts with the time Δt_1 that it takes the regulator (the feedback loop to be more specific) to start responding to the sudden change in load current. From this statement, it can be inferred that the closed-loop bandwidth of the regulator plays a crucial role, since the larger the bandwidth, the faster the regulator will respond.

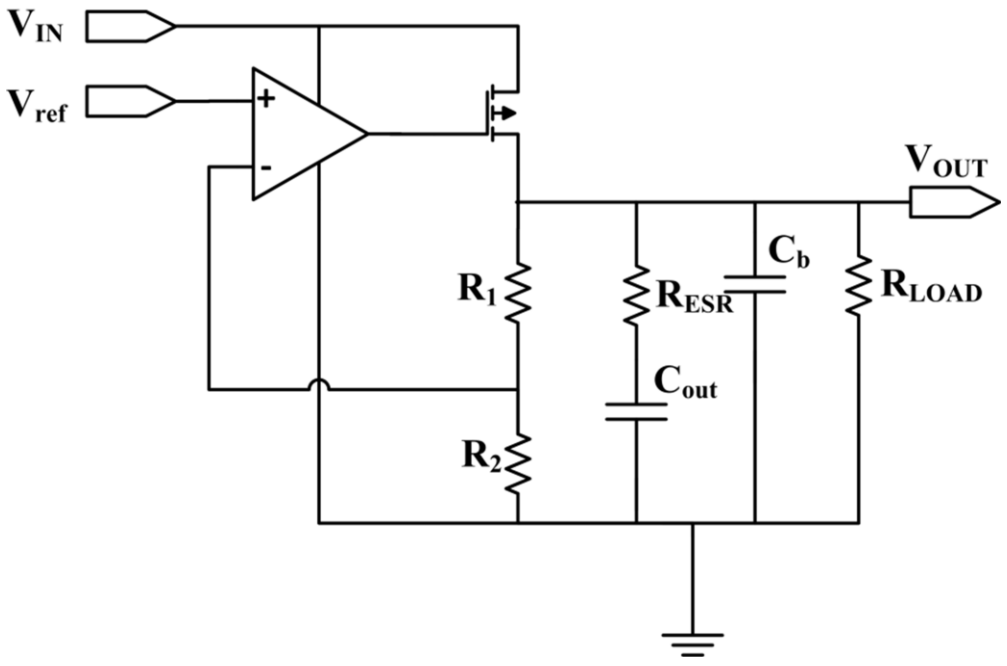


Fig. 4.3 – Schematic of a generic linear regulator.

Δt_1 will also be affected by how large the parasitic capacitance of the pass device (C_{par}) is because depending on the slew-rate (SR) of the error amplifier, the response time will be slower or faster [57]. Therefore,

$$\Delta t_1 \approx \frac{1}{BW_{CL}} + SR_{time}, \text{ from } i = C\frac{dV}{dt} \tag{4.4}$$

$$\Delta t_1 \approx \frac{1}{BW_{CL}} + C_{par}\frac{\Delta V}{I_{SR}} \tag{4.5}$$

where ΔV is the voltage variation in the parasitic capacitance of the pass device, and I_{SR} is the slew rate current applied to that capacitance. Δt_1 is also the time it takes the regulator to reach the lowest permissible undershoot voltage ΔV_{TRAN+}, which will be a function of the output capacitor C_{OUT}, the voltage drop across R_{ESR}, the load current ΔI_{LOAD} momentarily supplied to the output by C_{OUT}, and the bypass capacitor C_b. Using the same basic capacitance equation as before,

$$\Delta V_{TRAN+} = \frac{\Delta I_{LOAD}}{C_{OUT} + C_B}\Delta t_1 + \Delta V_{ESR} \tag{4.6}$$

After the lowest voltage has been reached, the feedback of the regulator starts to respond, and Δt_2 is the time it takes for the pass device to charge the load capacitors [57] and reach its final V_{LDR} value. From (4.3) it can be seen that $V_{OUT} = V_{LDR}$ and therefore,

$$\Delta V_{LDR} = I_{LOAD}R_{o-reg} \tag{4.7}$$

In a similar manner to when the current steps up, it takes some finite amount of time Δt_3 for the regulator to respond when the current steps down. The feedback loop needs to respond to the load current change by "less" turning on the pass device. Once this time has elapsed, ΔV_{TRAN-} has been reached and it is defined by a very similar equation to ΔV_{TRAN+}.

$$\Delta V_{TRAN-} = \frac{\Delta I_{LOAD}}{C_{OUT} + C_B}\Delta t_3 + \Delta V_{ESR} \tag{4.8}$$

Finally, the voltage on the output capacitors settle down to its final value after some time Δt_4 which can be expressed in terms of the quiescent current I_Q,

$$\Delta t_4 \approx \frac{C_{OUT} + C_B}{I_Q} \Delta V_4 \tag{4.9}$$

One important fact to notice from Fig. 4.2 is that the response of the regulator is not symmetrical. This is due to the slew rate unidirectional limitation of the error amplifier that mainly affects the load-current step-up event.

4.2.2 Stability in linear regulators

A stable regulator is defined as having a considerable phase margin open-loop response in order to avoid oscillations in its output voltage. In other words, the open-loop gain response of the regulator needs to be similar to a single pole system, that is, to cross the 0 dB axis with a slope of 20 dB/decade [58]. The issue with regulators is that due to their compensation network, capacitive loads and internal capacitances, there will be more than one pole in the system. The key is to spread them out in order to obtain a good phase margin (at least 60 dB) by inserting a zero in the system. The simplest form to insert a zero in the open-loop response is to make use of the ESR of the output capacitor. Fig. 4.4 shows the ideal open-loop response of a stable linear regulator.

The AC schematic shown in Fig. 4.5 is used to determine the open-loop response of the regulator. For the purpose of analysis, the loop is broken in the feedback path. The open-loop response has an easily identifiable pole at the output of the error amplifier and a real component formed by the feedback resistors. The pass transistor with the entire output impedance (Z_{out}) of the regulator provides the rest of the response.

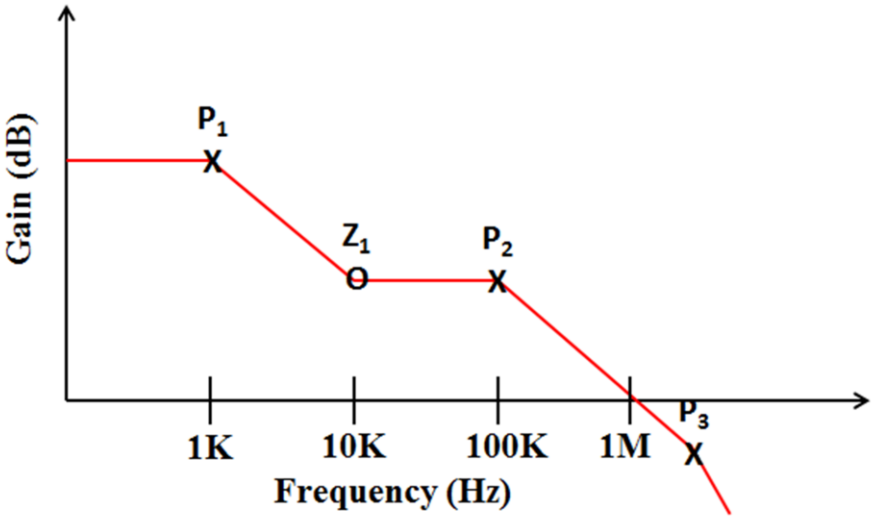


Fig. 4.4 – Ideal open-loop response of a linear regulator.

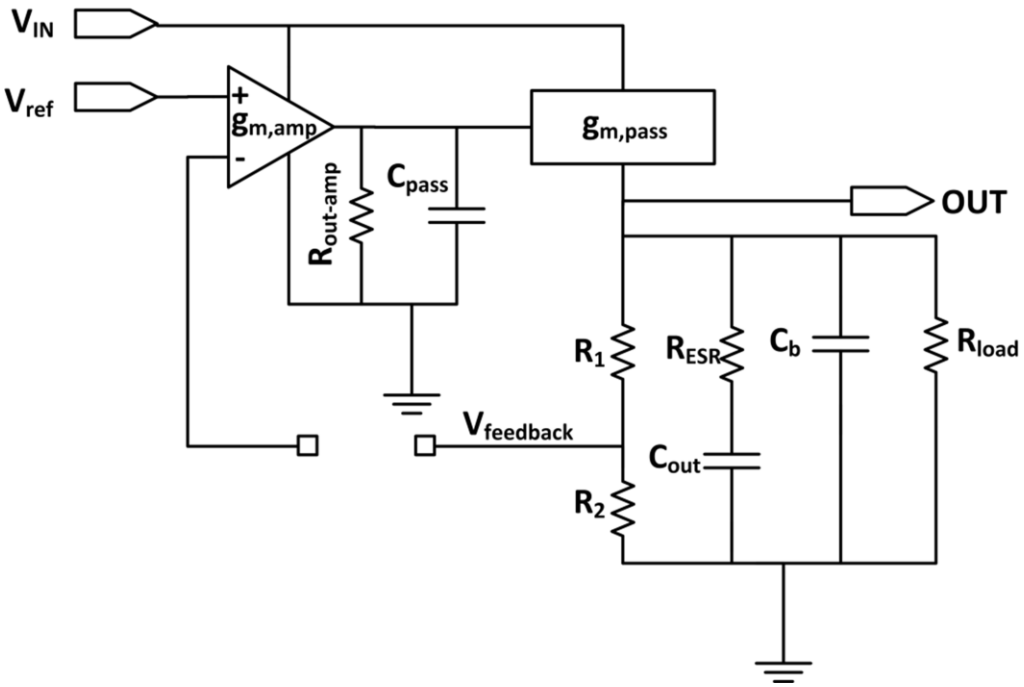


Fig. 4.5 – AC schematic used for open-loop response analysis.

The overall response can be expressed as

$$\frac{V_{feedback}}{V_{ref}} = \left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{g_{m,amp} r_{out,amp}}{1 + s r_{out,amp} C_{pass}}\right)(g_{m,pass} Z_{out}) \tag{4.10}$$

where $g_{m,amp}$ and $g_{m,pass}$ are the transconductances of the error amplifier and the pass device, respectively. $R_{out,amp}$ is the output resistance of the error amplifier, C_{pass} is the parasitic capacitance of the pass device and Z_{out} is the impedance of the regulator seen from the output. Z_{out} can then be expressed as

$$Z_{out} = (r_{out,pass} || R_1 + R_2 || R_{load}) || \left(\frac{1}{sC_b}\right) || \left(\frac{1 + sR_{ESR}C_{out}}{sC_{out}}\right) \tag{4.11}$$

where the first term is approximately equal to $r_{out,pass}$ and this term will be denoted as R_{out} from now on.

Then Z_{out} becomes,

$$Z_{out} = \left(\frac{\frac{R_{out}}{sC_b}}{R_{out} + \frac{1}{sC_b}}\right) || \left(\frac{1 + sR_{ESR}C_{out}}{sC_{out}}\right) = \left(\frac{R_{out}}{1 + sR_{out}C_b}\right) || \left(\frac{1 + sR_{ESR}C_{out}}{sC_{out}}\right) \tag{4.12}$$

$$Z_{out} = \frac{\left(\frac{R_{out}}{1 + sR_{out}C_b}\right)\left(\frac{1 + sR_{ESR}C_{out}}{sC_{out}}\right)}{\frac{R_{out}}{1 + sR_{out}C_b} + \frac{1 + sR_{ESR}C_{out}}{sC_{out}}} \tag{4.13}$$

$$= \frac{R_{out}(1 + sR_{ESR}C_{out})}{sR_{out}C_{out} + (1 + sR_{out}C_b)(1 + sR_{ESR}C_{out})}$$

$$Z_{out} = \frac{R_{out}(1 + sR_{ESR}C_{out})}{sR_{out}C_{out} + 1 + sR_{ESR}C_{out} + sR_{out}C_b + s^2 R_{out}R_{ESR}C_{out}C_b} \tag{4.14}$$

and after rearranging the terms in the denominator

$$Z_{out} = \frac{R_{out}(1 + sR_{ESR}C_{out})}{s^2 R_{out}R_{ESR}C_{out}C_b + s(R_{out}C_{out} + R_{ESR}C_{out} + R_{out}C_b) + 1} \tag{4.15}$$

$$Z_{out} = \frac{\frac{R_{out}(1+sR_{ESR}C_{out})}{R_{out}R_{ESR}C_{out}C_b}}{s^2 + \frac{s(R_{out}C_{out}+R_{ESR}C_{out}+R_{out}C_b)}{R_{out}R_{ESR}C_{out}C_b} + \frac{1}{R_{out}R_{ESR}C_{out}C_b}} \tag{4.16}$$

$$Z_{out} = \frac{\frac{R_{out}(1+sR_{ESR}C_{out})}{R_{out}R_{ESR}C_{out}C_b}}{s^2 + s[\frac{(R_{out}+R_{ESR})C_{out}+R_{out}C_b}{R_{out}R_{ESR}C_{out}C_b}] + \frac{1}{R_{out}R_{ESR}C_{out}C_b}} \tag{4.17}$$

However $C_{out}>>C_b$ and therefore,

$$Z_{out} = \frac{\frac{R_{out}(1+sR_{ESR}C_{out})}{R_{out}R_{ESR}C_{out}C_b}}{s^2 + s[\frac{(R_{out}+R_{ESR})C_{out}}{R_{out}R_{ESR}C_{out}C_b}] + \frac{1}{R_{out}R_{ESR}C_{out}C_b}} \tag{4.18}$$

$$= \frac{\frac{R_{out}(1+sR_{ESR}C_{out})}{R_{out}R_{ESR}C_{out}C_b}}{[s + \frac{R_{out}+R_{ESR}}{R_{out}R_{ESR}C_b}][s + \frac{1}{C_{out}(R_{out}+R_{ESR})}]}$$

$$Z_{out} = \frac{[\frac{R_{out}\ 1+sR_{ESR}C_{out}}{R_{out}R_{ESR}C_{out}C_b}](\frac{R_{out}R_{ESR}C_b}{R_{out}+R_{ESR}})C_{out}(R_{out}+R_{ESR})}{[1+s(\frac{R_{out}R_{ESR}}{R_{out}+R_{ESR}})C_b][1+s(R_{out}+R_{ESR})C_{out}]} \tag{4.19}$$

Finally Z_{out} becomes

$$Z_{out} = \frac{R_{out}(1+sR_{ESR}C_{out})}{[1+s(R_{out}||R_{ESR})C_b][1+s(R_{out}+R_{ESR})C_{out}]} \tag{4.20}$$

Inserting this equation for Z_{out} into the original open-loop response equation

$$\frac{V_{feedback}}{V_{ref}} = (\frac{R_2}{R_1+R_2})(\frac{g_{m,amp}r_{out,amp}}{1+sr_{out,amp}C_{pass}})\frac{g_{m,pass}R_{out}(1+sR_{ESR}C_{out})}{[1+s(R_{out}||R_{ESR})C_b][1+s(R_{out}+R_{ESR})C_{out}]} \tag{4.21}$$

$$\frac{V_{feedback}}{V_{ref}} = \left(\frac{R_2}{R_1 + R_2}\right)(g_{m,amp} r_{out,amp})(g_{m,pass} R_{out}) \frac{(1 + sR_{ESR}C_{out})}{(1 + sr_{out,amp}C_{pass})[1 + s(R_{out}||R_{ESR})C_b][1 + s(R_{out}+R_{ESR})C_{out}]} \quad (4.22)$$

From this equation it can be observed that the open-loop response is determined at the DC level by the feedback resistors ratio and by the gain of the error amplifier and the pass device. The response consists of three poles and one zero that can be simplified by noticing that the ESR values are typically (and intended to be) very small even when compared with R_{out} which is very close to $r_{out,pass}$. As a result,

$$p_1 \approx \frac{1}{2\pi r_{out,pass} C_{out}} \quad (4.23)$$

$$z_1 \approx \frac{1}{2\pi R_{ESR} C_{out}} \quad (4.24)$$

$$p_2 \approx \frac{1}{2\pi r_{out,amp} C_{pass}} \quad (4.25)$$

$$p_3 \approx \frac{1}{2\pi R_{ESR} C_b} \quad (4.26)$$

Ideally, the locations of the poles and zeroes should be as above in order to ensure the stability of the regulator as shown in Fig. 4.4. Proper selection of the output capacitor and its ESR value are critical for this purpose. Another important detail in the open-loop response of the regulator is to be aware that the output resistance of the pass device $r_{out,pass}$ will decrease as the load current increases displacing the pole to a higher frequency. Figs. 4.6 and 4.7 show the gain and phase response of a linear regulator, at no load and full load, respectively. The change in location of the dominant pole can be observed and as a result of this pole moves close to the zero making the gain and phase responses seem different. Also, mainly as a result of the decrease in $r_{out,pass}$, a decrease in the gain is always expected at full load. Overall, this regulator is stable since the phase margin is larger than 60 degrees even at full load. This response was obtained

using a C_{out} = 10 µF, ESR = 0.5 Ω, C_b = 0.3 µF, R_1 = 1 kΩ and R_2 = 2 kΩ. The maximum load current was 3 A.

Given the importance of the output capacitor and its ESR, commercial linear regulators usually provide a recommended capacitor size with its minimum and maximum value for ESR such that stability of the regulator is insured. In addition, plots for different ESR values versus load current for a specific capacitor size are usually included in the datasheets [59]. In real practice, ceramic capacitors can be used in series with a resistor in order to satisfy the ESR requirements for stability. Another option is to use tantalum capacitors although they tend to be larger and more expensive than ceramic capacitors [59].

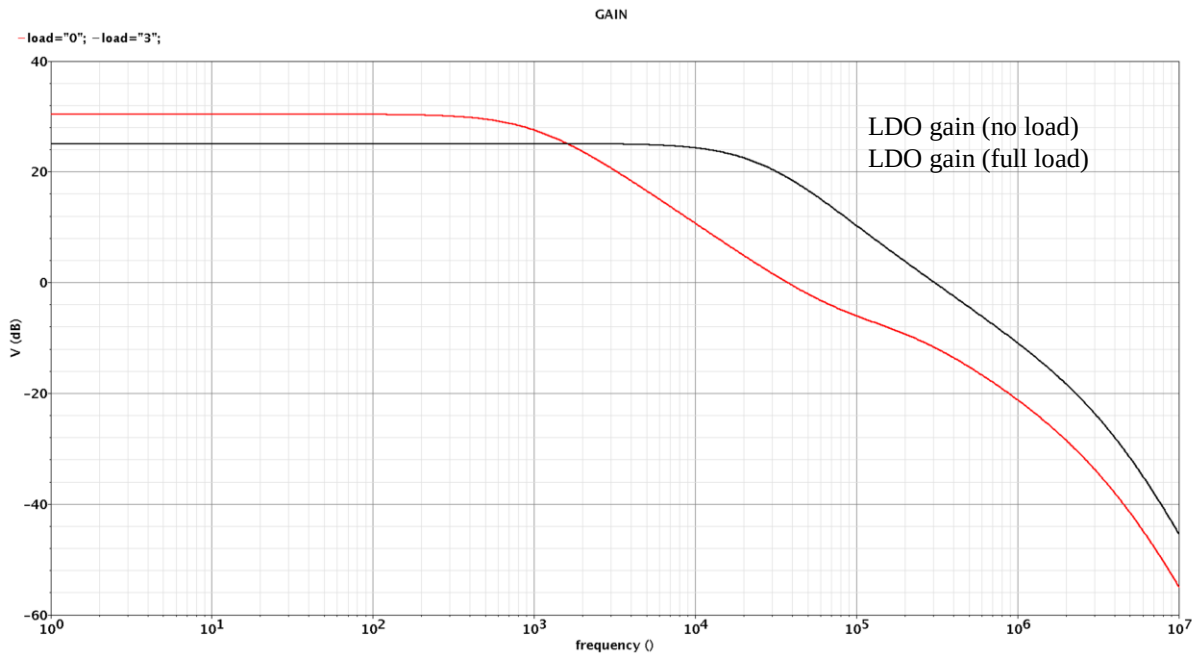


Fig. 4.6 – Gain response of a stable linear regulator without load and at a full 3 A load. The displacement of the dominant pole can be observed as a result of a decrease in the output resistance of the pass device. This also results in a gain loss at full load.

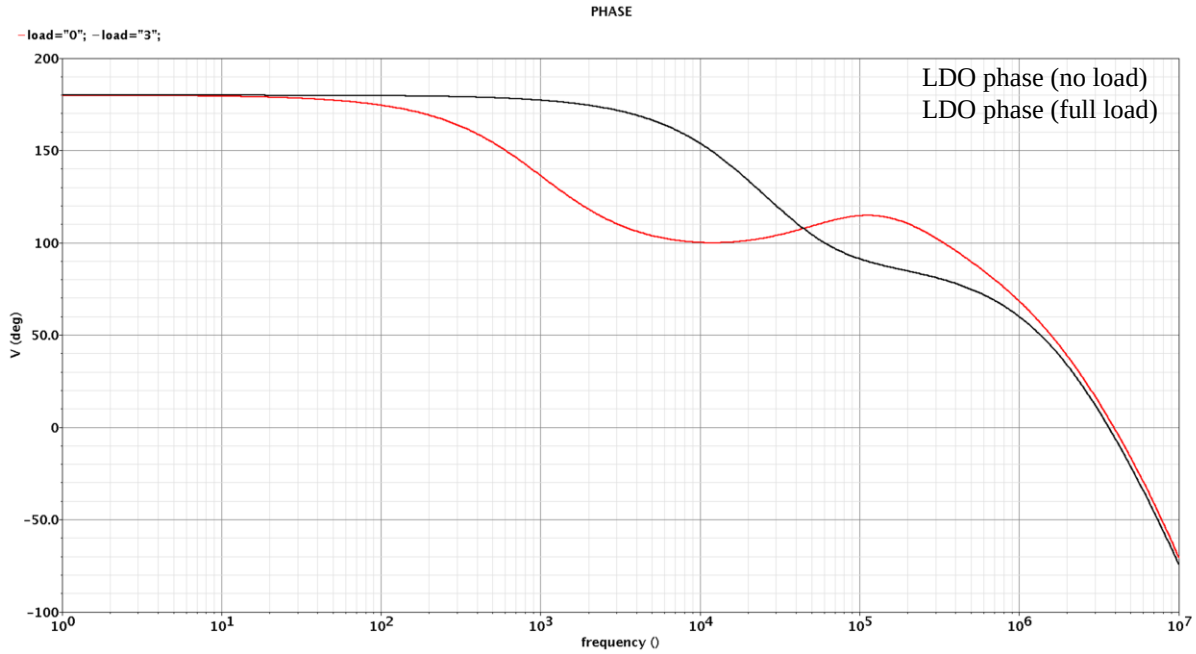


Fig. 4.7 – Phase response of a stable linear regulator without load (red) and at a full 3 A load (black). The displacement of the dominant pole can be observed as a result of a decrease in the output resistance of the pass device. The zero at no load condition cancels out as a result of this displacement.

4.3 State-of-the-art in Si linear regulators

Due to the significant advances in Si manufacturing processes, a very large number of features are now part of the current Si linear regulators reported by the literature. As fabrication processes have moved into the sub-micron region, most linear regulators available are classified as LDOs. This section focuses on these types of regulators, and their most advanced features and topologies are presented.

One of the most significant features is the low-quiescent current and low dropout voltage since they both reduce the amount of dissipated power. This reduction is particularly interesting for mobile electronics applications where power becomes a major constraint, especially due to the reduction in power supply voltages as manufacturing technologies have advanced. A low-quiescent current, I_Q, improves the efficiency of the regulator as shown in (4.2). This is true

when there is no load current and the equation is dominated by I_Q. At large load currents, the quiescent current is negligible and therefore, it can be used to improve the transient response of the regulator. Fig. 4.8 shows the three different scenarios of how the quiescent current behaves respect to the load current.

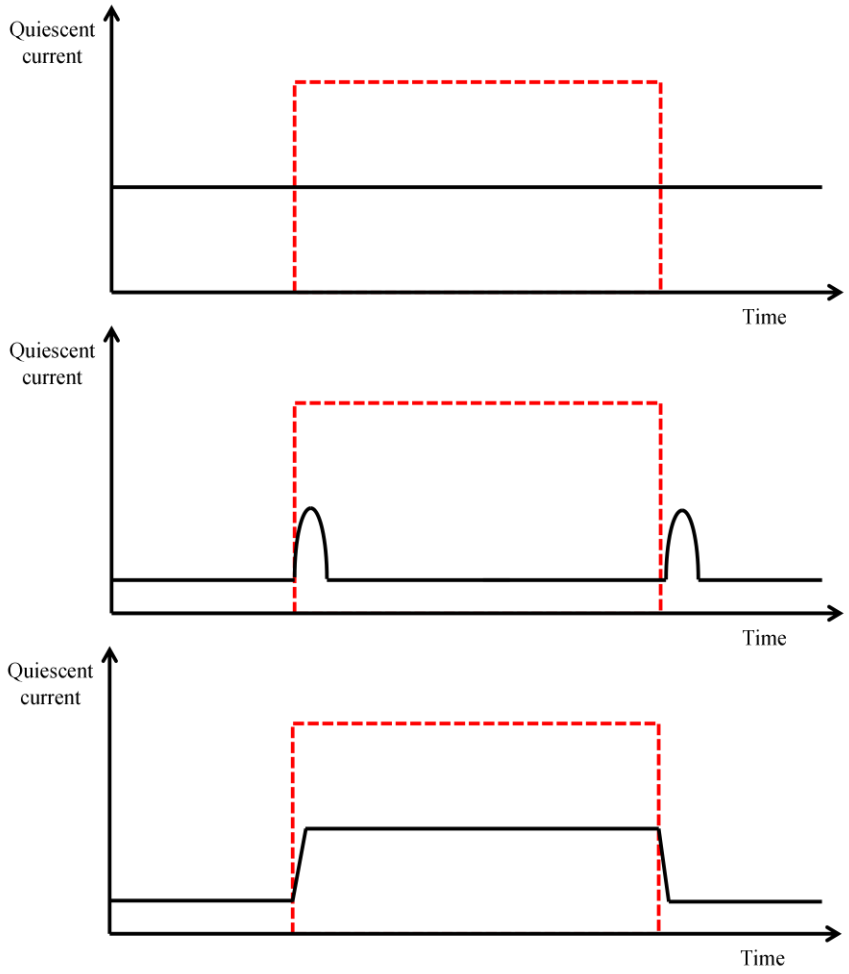


Fig 4.8 – Quiescent current (black) behavior respect to load current changes (red) in a linear regulator.

The first scenario is when the quiescent current is maintained at a constant value regardless of the load current. This is obviously not a very efficient system but it could be suitable for certain applications where power dissipation is not critical. The second scenario, also

called dynamic biasing, is when the quiescent current is increased only during the large transient current changes in the load. In the third scenario, the quiescent current increases to a higher value for the duration of the entire time the load is at its peak current value. This makes it less efficient than the second case but in both cases, the quiescent current is small compared to the load current. Therefore, with some additional circuitry, this quiescent current can be used to speed up the regulator response to changes in the load current. This is mainly achieved by improving the slew rate at the node where the parasitic gate capacitance of the pass device is located.

Following this trend, Rincon-Mora [60] presents a 1.2 V / 0.9 V input/output voltages, 230 μA quiescent current at its 50 mA maximum output current, externally compensated LDO with two particular features, a current efficient buffer and a current boosting technique. The LDO was fabricated in a CMOS, 2 μm process, but with the ability to fabricate vertical NPN transistors through the addition of a p-base layer. The current efficient buffer senses the current through the pass device and a ratio of this current is fed back into the node charging up the parasitic capacitance of the pass device (C_{pass} in Fig. 4.5). At no load current, the current fed back is negligible (current efficient) but at full load, the current helps charge the parasitic capacitance and it displaces the parasitic pole associated with this node to higher frequencies, improving the frequency stability of the regulator. The current boosting technique makes use of the threshold voltage change due to the substrate bias voltage condition described in section 3.2. This substrate bias voltage change is achieved using a Schottky diode in a similar circuit and concept to the current efficient buffer. Since the pass device threshold is decreased at full load (due to the substrate bias voltage applied by the diode), then the pass device is driven harder, boosting its current as needed by the load. Fig. 4.9 shows a transistor-level schematic of the main features of this LDO [60].

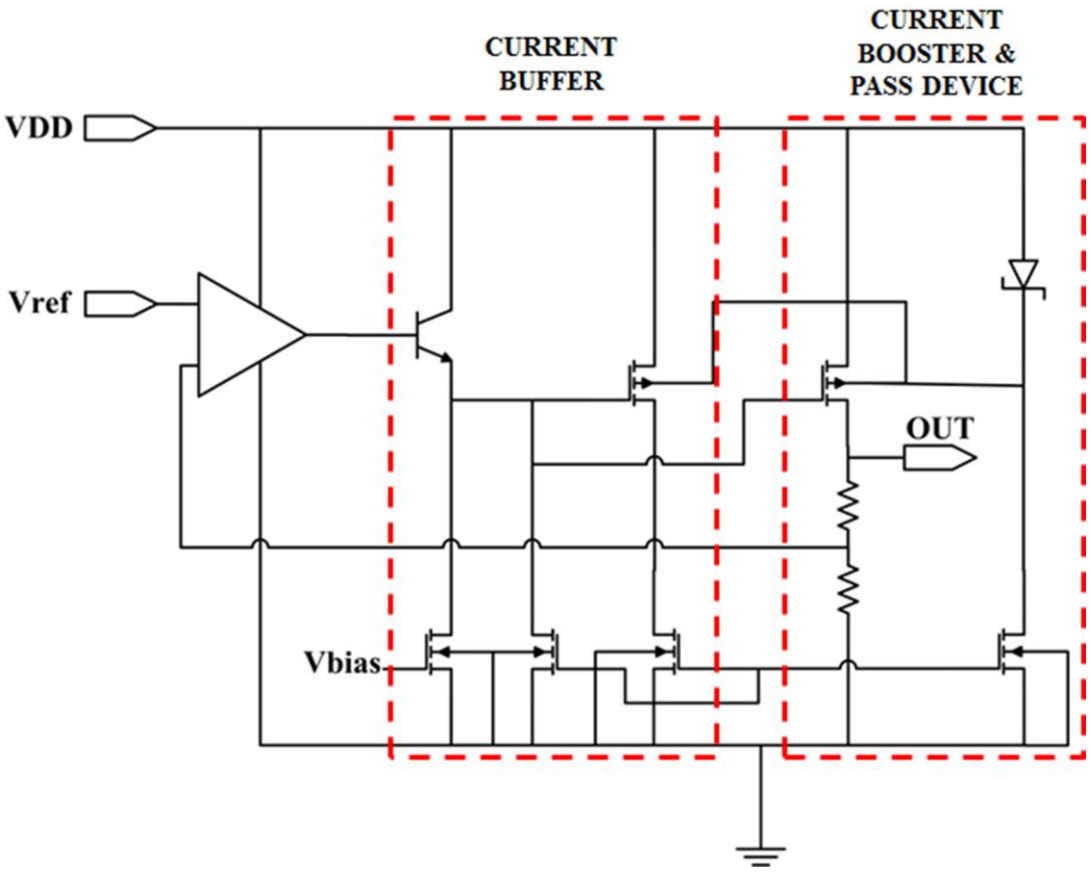


Fig. 4.9 – The current efficient buffer and current boosting technique described in [60].

Different circuit techniques have been presented for low-voltage linear regulators attempting to improve the transient response. A high slew rate push-pull output amplifier is reported in [61]. The amplifier consists of two cross-couple connected common-gate differential input transconductance cells and a current summation circuit. This configuration allows for fast charging and discharging of the gate capacitance of the pass device. The LDO using this amplifier does not need any external or internal capacitors for frequency compensation due to the small input resistance of the differential cells. This LDO is fabricated in a 0.35 μm CMOS process with a quiescent current of 1.2 μA and a maximum load current of 50 mA. The same topology reported in [61] but with a Slew Rate Enhancement (SRE) circuit is reported in [62]. In

this case, the SRE is only active during the transient changes in the load current (dynamic biasing) and it is placed in parallel with the amplifier reported in [61]. The SRE provides the dynamic current to charge and discharge the gate capacitance of the pass device even faster and hence, improving the transient response of the LDO type regulator. This LDO is capacitor-less, fabricated in a 0.35 μm CMOS process with a quiescent current of 8 μA and a maximum load current of 100 mA. The load regulation is indeed improved when compared to [61].

Another idea on how to improve the slew rate at the gate capacitance of the pass device is presented in [63]. In this case, a voltage spike detection circuit at the output of the regulator is used to improve the slew rate only when large transient changes occur in the load (dynamic biasing), making the system current efficient. The detection circuit makes use of coupling capacitors to detect the voltage spikes at the output and hence, adjustments can be made to the biasing currents in the circuitry. The LDO is capacitor-less, fabricated in a 0.35 μm CMOS process with a quiescent current of 19 μA, an output of 0.8 V and a maximum load current of 66.7 mA. [61] - [63] make use of a non-traditional regulator topology to avoid the need for external or internal capacitors for frequency compensation of the regulator. This LDO topology is based on the flipped voltage follower (FVF) structure for low-voltage applications [64]. This structure is able to source large amounts of current due to its low output impedance. The FVF is a modified version of the super source follower (SSF) configuration. The SFF is intended to lower the output resistance of a standard source follower circuit by making use of a negative feedback loop [55]. Figs 4.10 and 4.11 show the FVF based LDO topology and the FVF configuration, respectively.

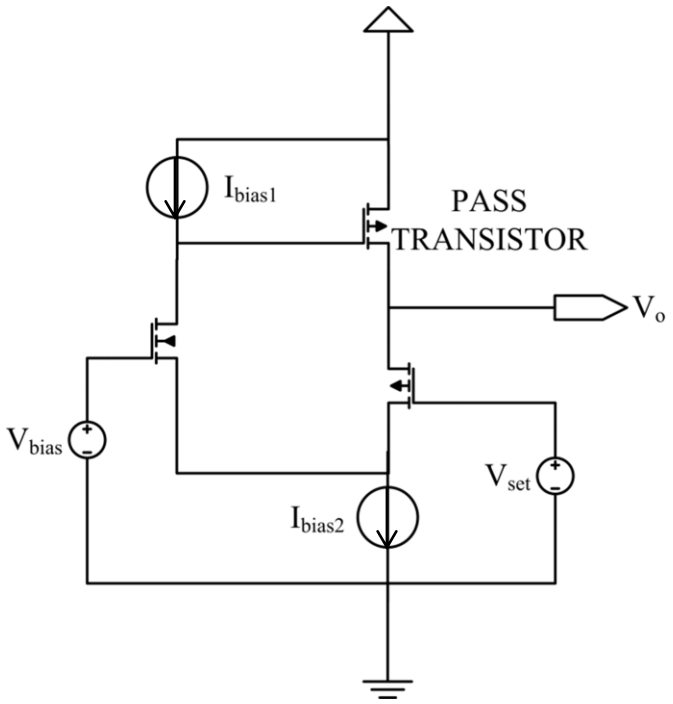


Fig. 4.10 – FVF based LDO topology used in [55]-[57].

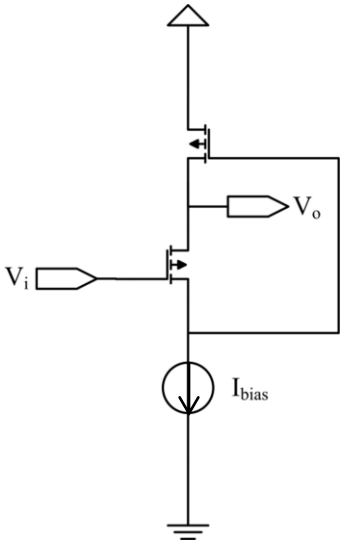


Fig. 4.11 – FVF configuration.

The elimination of compensation capacitors using the FVF topology favors integration and allows improving regulators to better suit the current low-voltage mobile applications.

However, FVF based LDOs using external capacitors are still possible as reported in [65]. This LDO makes use of the original FVF configuration where the source of the bottom transistor is connected to the gate of the pass device of the LDO. Since the voltage changes in the output are detected and adjusted only by the bottom transistor, the system is called a Single Transistor Control (STC) LDO. In order to avoid changes in the output due to temperature or process variation, the gate control signal for the bottom transistor is generated using a bandgap reference. Fig. 4.12 shows a schematic of this LDO. The LDO is stable over frequency with and without external capacitors proving the feasibility of the FVF based LDO topology to reduce the output impedance of the system. This LDO was fabricated in a 0.35 μm CMOS process, with a quiescent current of 95 μA, and a maximum load current of 50 mA. Fig. 4.12 shows a schematic of this FVF based LDO with external compensation.

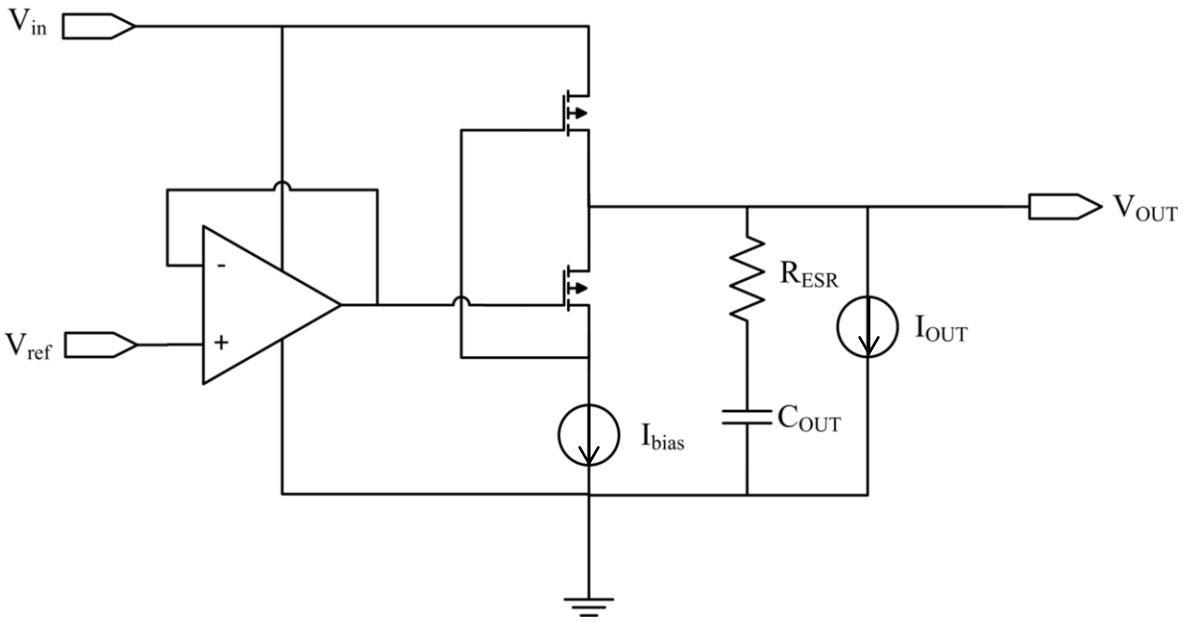


Fig. 4.12 – FVF based LDO with external frequency compensation.

Most error amplifiers used in a generic linear regulator (Fig. 4.3) incorporate an output stage, also referred to as buffer. The buffer allows driving the large pass device quickly. This is accomplished by having low output impedance and also providing sourcing and sinking current to charge and discharge the parasitic capacitance of the pass device quickly [1]. Current efficient buffers, like the one reported in [60], are examples of this technique used to enhance the transient response of a regulator. A more recent LDO presented in [66] focuses on an impedance attenuated buffer to achieve a better performance. The LDO was fabricated in a 0.35 μm, twin well CMOS process, has a quiescent current of 20 μA, a maximum load current of 200 mA and makes use of a 1 μF external capacitor. This LDO follows the standard topology of a generic linear regulator shown in Fig. 4.3 but it places a buffer between the error amplifier and the pass device. The error amplifier in this LDO consists of a single stage folded cascode structure. The buffer allows for output resistance reduction at the gate of the pass device and current enhancement under different load conditions. The buffer makes use of an NPN transistor acting as a feedback device to achieve this goal. In addition, the frequency response of this LDO consists of only one pole before reaching its Unity Gain Frequency (UGF). This is due to the output resistance reduction technique which pushes the pole at the gate of the pass device to a higher frequency. A zero cancellation scheme is also implemented by using a very small internal compensation capacitor making the LDO stable over the entire load current range.

Finally, in the field of low power transient enhanced linear regulators, there is a simple but interesting structure that follows the generic linear regulator topology. The LDO reported in [67] makes use of multiple small-gain stages to enhance the transient response of the regulator. The LDO is fabricated in a 90 nm CMOS process, has a 1 V output, a maximum load current of 50 mA, a quiescent current of 9.3 μA and makes use of a 1 μF capacitor with an ESR of 0.35 Ω.

The main technique in this regulator is to increase the loop gain and by doing so, the bandwidth of the regulator is also increased. This results in a load regulation improvement as indicated in (4.3). The problem in this design is frequency stability since poles and zeroes are being created by every single stage. The regulator, however, is frequency stable since the poles and zeroes from each stage are located beyond the UGF. This was possible because the gain factor of each individual stage was reduced; hence the parasitic gate capacitance at each stage input is small enough to push the poles and zeroes to high frequencies. At the end, the frequency response of the regulator is very similar to the one described in Section 4.2.2 since no additional poles and zeroes are part of the analysis. Fig. 4.13 shows a schematic of this linear regulator.

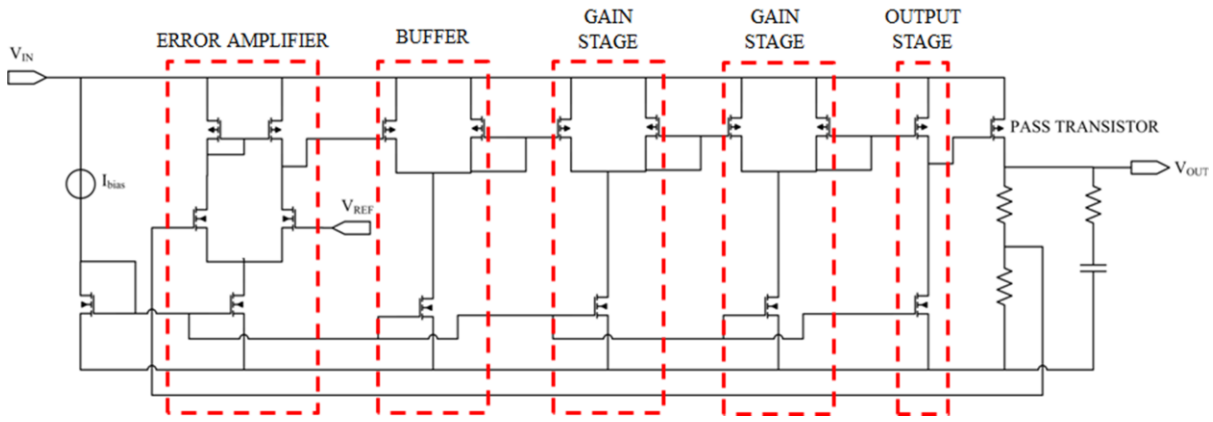


Fig. 4.13 – A multiple gain stages, transient enhanced LDO.

All the regulators presented up to this point have PMOS transistors as pass devices. This is because all of them are fabricated using low-voltage sub-micron technologies where low dropout is critical. The literature, however, reports linear regulators that make use of NMOS transistors as pass devices [68]-[71]. These regulators are usually focused on improving its PSR since they are used in System-on-Chip (SoC) applications for typical noisy environments [72]. Another focus of interest for these regulators is the very low output impedance obtained from the

source follower configuration [73]. The limitation of this topology is that the output voltage needs to be lower than the gate voltage by at least V_T. The common technique to overcome this problem, and still have a low dropout feature, is the use of a charge pump that allows the gate voltage of the pass device to be larger than the input voltage of the regulator. The tradeoff with charge pumps or similar circuits is the need for on-chip capacitors and clock signals. A common topology to improve PSR, and hence noise performance, in regulators with PMOS and NMOS pass devices is to cascode the devices. [70], [74] report this particular topology in order to isolate the pass device from noise from the input supply or from voltage stress.

The use of NMOS transistors as pass devices could also be determined by the features of the process used for fabrication. Su et al. report a high temperature, high voltage, linear regulator using a high voltage n-type DMOS as a pass device [75]. The regulator will be used in gate driver ICs for power converters inside the HEV. This linear regulator is fabricated in a 0.8 μm BJT-CMOS-DMOS (BCD) SOI process, has an output of 5.3 V and a maximum load current of 200 mA. Because of the high voltage DMOS devices in this process, the input voltage for this regulator is 10-30 V and since its output is 5.3 V, there is no concern about low dropout performance, thus eliminating the need for a charge pump. The regulator follows a standard topology and it makes use of Proportional To Absolute Temperature (PTAT) and Complimentary To Absolute Temperature (CTAT) techniques to generate temperature independent current sources used in the error amplifier. The literature does not report many high temperature linear regulators. Honeywell, a well-known high temperature electronics company, reports another SOI linear regulator with output voltages between 5 V-15 V, maximum load current of 500 mA and external pass device [76]. Holter et al. also report a high temperature linear regulator fabricated in a 1.2 μm BiCMOS process with output voltages between 5 V -12 V and maximum load

current of 250 mA [77]. Nowadays, there are high temperature commercial linear regulators offered by Honeywell [78] and Texas Instruments [51], rated up to 225 °C and 210 °C, respectively. The maximum load current for these types of linear regulators is still in the hundreds of mA range.

This section intended to present the latest Si linear regulators reported by the literature. Due to the current advanced Si manufacturing capabilities in the sub-micron range, these latest regulators are usually all low-power and current efficient. In addition, since BJTs are current-driven devices, they are not suitable for the current efficient and low power performance expected from the current regulators. This is why almost all of these designs are CMOS based.

Furthermore, since the operation of a system depends on the power delivered by the linear regulators, it is not uncommon to add protection circuits to the regulator. Some of them include, but are not limited to, overcurrent protection, thermal shutdown, under-voltage lockout, and soft start circuitry [51], [57]. Most of these features are to complement the performance at the system level without enhancing the core functionality of the regulator. Due to this reason, they were not discussed in this section.

CHAPTER 5: SiC VOLTAGE REGULATOR DESIGN

At this point, it should be apparent that the limitations in the Cree SiC process will be the major constraint for the design of the linear voltage regulator. The lack of PMOS devices in the process does not allow fabricating an LDO but rather a linear voltage regulator where the output will have to be no greater than $V_{IN} - V_{T,NMOS}$. In addition to this, the poor capability of the process to fabricate on-chip capacitors as described in Section 3.2, does not allow designing a charge pump for low dropout while using a NMOS transistor as a pass device. However, using a depletion NMOS transistor as a pass device provides a reasonable solution to this problem. Even though the dropout will still be larger than an LDO, it will be less than using an enhancement NMOS. As described in Section 3.2, the substrate bias voltage has a considerable effect in this process, and using the standard topology for a linear regulator, the effect on the threshold voltage would be an increase in the same way as in the circuit in Fig. 3.12 (b). Since the threshold voltage for a depletion device is negative, the maximum output of the voltage regulator with a depletion NMOS as a pass device will be larger than a regulator with an enhancement NMOS as a pass device. The delicate part of this design technique will be to quantify the actual effect in the threshold voltage as accurate as possible in order to properly drive the pass device.

In the rest of the circuitry, i.e. the error amplifier, where depletion NMOS devices could be used as the loads of each stage, the substrate bias voltage might have a deeper effect. Depletion devices are generally used as loads and therefore, they will always have a substrate bias voltage different from 0 V. When these devices are used as loads, their gate is connected to their source [41] [42], and since their threshold voltage is negative, the devices are always on ($V_{GS} = 0$ V and $V_{GS} > V_T$). When the substrate bias voltage effect is taken into consideration, the increase in the threshold voltage might reach a point where it becomes larger than 0 V and as a

result, the device will turn off. Therefore, depending on the operation of the circuit and the parameters of the device (W/L ratio, number of fingers, etc.), there can be different substrate bias voltages for each device in the same circuit, increasing the level of complexity in an already very sensitive and developing process. For this reason, the use of depletion NMOS as loads will be avoided in this design. n^+ implant resistors will be used as pull-up devices to ensure the proper operation of the circuit and reduce the risks associated with the process.

All the previous reasons, and the fact that the process does not offer any diodes, also make it virtually impossible to design and fabricate a stable voltage reference for the error amplifier. As was discussed in Section 4.2, the stability of the voltage reference propagates throughout the entire regulator and it could have a severe impact in its performance. An external voltage reference will eliminate these risks and will still demonstrate the feasibility of a SiC linear regulator.

Finally, as mentioned at the beginning of this chapter, the limitation in fabricating only very small on-chip capacitors forces the regulator to be externally compensated, e.g. C_{OUT} in Fig. 4.3 will be external. The feedback network will also be external in order to allow regulating at different voltages by using different values for R_1 in the feedback network. As a general rule, circuits will need to be simple in order to ensure proper operation of the regulator despite the different limitations of the process, and risks will be reduced by using external components and reference voltages that require very precise and predictable operations that, at this point, only Si can provide.

In summary, it was decided to design the 15 V output, 3 A maximum load current SiC linear regulator with the following constraints:

- Use a depletion NMOS transistor as a pass device.

- Use resistors as loads where needed.
- Use an external voltage reference for the error amplifier.
- Use an external capacitor for frequency compensation.
- Use external resistors for the feedback network.
- Design circuits that are simple in nature to ensure full functionality.

5.1 Pass device

In order for linear regulators to deliver large amounts of current as requested by the load, the pass device is usually a very large transistor. Besides the current, the size of the transistor (W/L ratio) depends also on the output voltage of the regulator. As mentioned earlier, the large size of the transistor implies also a very large parasitic capacitance which plays an important role in the performance of the regulator.

In a very well defined process, a very good first order approximation of the pass device could be obtained from the standard saturation equation of a transistor [43]:

$$I_D = \frac{1}{2} k'(\frac{W}{L})(V_{DS,SAT})^2 \tag{5.1}$$

where W/L is the width to length ratio of the transistor and k' is a process dependent parameter defined as

$$k' = \mu_N C_{OX} \tag{5.2}$$

where μ_n is the electron mobility and C_{OX} is the oxide capacitance.

From the relationships, the very first unknown is the electron mobility. In Section 2.1.3, the electron mobility for 4H-SiC was defined by (2.6), which depends only on the doping concentration. The doping concentration profile of the wafer selected to develop these models peaked at about $5x10^{16}$ cm^{-3} [39]. From this, the electron mobility is about 802 cm^2/Vs. The gate

oxide thickness for the process is about 40 nm, and using 3.97 as the dielectric for silicon dioxide, results in an oxide capacitance of 0.878 fF/μm^2. Setting the maximum current for the linear regulator at 3 A, V_T = -2V, $V_{DS,SAT}$ = 5 V and solving for W/L in (5.1) yields a value of 3262. Table 5.1 summarizes the calculations.

Table 5.1 – First-order Approximation of the W/L Ratio for the Pass Device.

Doping concentration N_D	$5x10^{16}cm^{-3}$
Electron mobility μ_n	802 cm^2/Vs
Oxide capacitance C_{OX}	0.878 fF/μm^2
V_T @ V_{SB}=15 V	-2 V
$V_{DS,SAT}$	5 V
I_{MAX}	3 A
W/L	3262

The W/L ratio above means that only 204 - 32 μm x 2 μm depletion devices (a W/L = 16) would be needed. However, this result only takes into account the effect of the substrate bias voltage on the threshold voltage, not on the reduction in the drain current. From Fig. 3.14, the actual amount of current delivered by one 32 μm x 2 μm depletion device with a V_{SB} = 15 V and V_{GS} = 5 V (the maximum allowable V_{GS} for an output of 15 V) at both corner temperatures can be determined. From these values, the total number of devices needed to deliver 3 A can be calculated since multiplicity is simply a scale factor in the models. The values and results are shown in Table 5.2.

Table 5.2 – Amount of 32 µm x 2 µm Depletion Devices Needed to Deliver 3 A Taking into Account the Drain Current Reduction due to the Substrate Bias Voltage.

Temperature (°C)	25	225
Drain current (mA)	3	1.75
Devices needed	1000	1715

The results in Table 5.2 include all the known limitations to the process. In order to make the design flexible and minimize the risk, the number of devices was decided to be 2000. This implies a W/L total ratio of 16*x*2000 = 32,000. While it is true that setting the number of devices at 2000 implies a larger layout area and larger parasitic capacitance than needed, this decision intends to prevent unexpected limitations caused in the drain current of the devices due to the nature of this process or for any other reason. The parasitic capacitance for a 32 µm x 2 µm depletion device with M = 2000 and V_{SB} = 15 V was already calculated to be 26.5 pF as shown in Table 3.2.

A very important detail to notice for this specific regulator is the use of an NMOS depletion device. Most regulators use PMOS devices for this purpose in order to achieve low dropout and improved efficiency. Since the source of the PMOS transistor is connected to the input voltage V_{IN}, and the regulator output is measured at its drain, the transistor is in a common source configuration. A small-signal analysis of this kind of configuration as part of a linear regulator is shown in Fig. 5.1. The resistors R_1 and R_2 are the feedback network as shown in Fig. 4.3.

As a result of this standard configuration, the pass device by itself has a gain which contributes to the overall gain of the regulator. This gain A_{PASS} is defined as

$$A_{PASS} = \frac{V_{OUT}}{V_G} = g_m[r_o||(R_1 + R_2)] \tag{5.3}$$

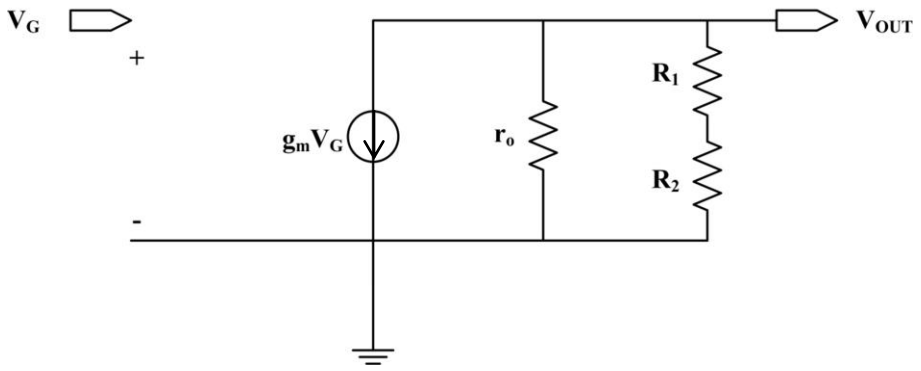


Fig. 5.1 – Small signal analysis of a linear regulator with a PMOS pass device.

However, since the output resistance of the pass device is very low compared to the feedback resistors, the gain of the pass device is positive and can be approximated as

$$A_{PASS} \approx g_m r_o \tag{5.4}$$

The difference arising from using a NMOS depletion device is that the transistor will be in a common-drain, also called source-follower, configuration. In this case, the output of the regulator is taken from the source of the pass device and as a result, the gain A_{PASS} is different from (5.4). Fig. 5.2 shows a small-signal analysis of the common-drain configuration as part of a linear regulator.

From Fig. 5.2, the gain A_{PASS} can be defined as,

$$A_{PASS} = \frac{V_{OUT}}{V_I} = \frac{V_{SOURCE}}{V_{GATE}} \tag{5.5}$$

$$V_{SOURCE} = g_m V_{GS}[r_o||(R_1 + R_2)] \tag{5.6}$$

$$V_{SOURCE} = g_m(V_{GATE} - V_{SOURCE})[r_o||(R_1 + R_2)] \tag{5.7}$$

$$V_{SOURCE} = g_m V_{GATE}[r_o||(R_1 + R_2)] - g_m V_{SOURCE}[r_o||(R_1 + R_2)] \tag{5.8}$$

$$V_{SOURCE} + g_m V_{SOURCE}[r_o||(R_1 + R_2)] = g_m V_{GATE}[r_o||(R_1 + R_2)] \tag{5.9}$$

$$V_{SOURCE}(1 + g_m[r_o||(R_1 + R_2)]) = g_m V_{GATE}[r_o||(R_1 + R_2)] \tag{5.10}$$

$$A_{PASS} = \frac{V_{OUT}}{V_I} = \frac{V_{SOURCE}}{V_{GATE}} = \frac{g_m[r_o||(R_1 + R_2)]}{1 + g_m[r_o||(R_1 + R_2)]} \tag{5.11}$$

$$A_{PASS} \approx \frac{g_m r_o}{1 + g_m r_o} \tag{5.12}$$

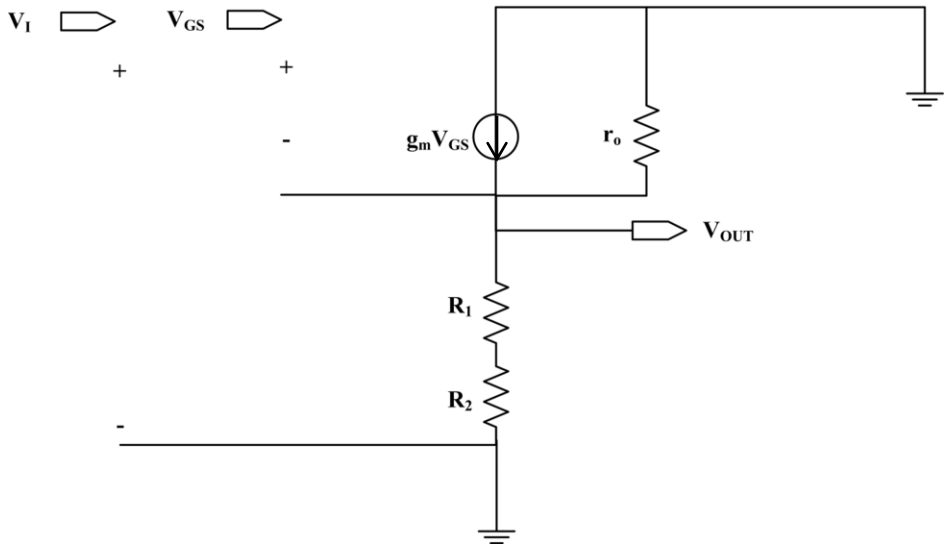


Fig. 5.2 – Small signal analysis of a linear regulator with a NMOS pass device.

The result in (5.12) indicates that using an NMOS transistor as the pass device (a limitation inherent to the process) will result in not obtaining a gain contribution from the pass device to the overall gain of the regulator , as it would occur if a PMOS transistor in a common-source configuration was to be used. Standard linear regulators do benefit from the gain provided as a result of using a PMOS transistor as a pass device. This gain, in addition to the gain of the error amplifier, improves the transient response of the regulator and its overall performance.

In the case of this specific SiC regulator, the gain in the frequency response will come only from the error amplifier, from which (5.12) will be subtracted. This decrease in gain due to

the common-drain configuration is larger at high currents given that r_o is inversely proportional to the drain current of the pass device as shown in (5.13).

$$r_o = \frac{V_A}{I_D} \tag{5.13}$$

where V_A is a process parameter called the Early voltage [43]. It is important to recall that the linear regulator will provide large amounts of current (in the Amps range) and therefore, the r_o variation from no load to full load condition is significant.

5.2 Feedback network

The feedback network consists of two resistors in series, R_1 and R_2, as shown in Fig. 4.3. These resistors are sized depending on the desired output voltage V_{OUT}, quiescent current I_Q, and the reference voltage V_{REF} used for the regulator based on the following equations.

$$R_1 + R_2 = \frac{V_{OUT}}{I_Q} \tag{5.14}$$

$$R_2 = \frac{V_{REF}}{V_{OUT}}(R_1 + R_2) \tag{5.15}$$

The efficiency of the regulator, as defined in (4.2), plays a key role in determining I_Q. However, given that this is not a low-dropout regulator; the efficiency will mostly be determined by the V_{OUT} to V_{IN} ratio which equals 0.75. Therefore, the quiescent current needs to be small enough compared to the maximum load current of 3 A, so that it does not worsen the default 75% efficiency. A quiescent current on the order of milliamps should be able to do this.

The other issue to take into account is that due to the large multiplicity of the pass device, providing such a small quiescent current during the no load condition implies that the pass device will be very close to being turned off. Such precise performance is to be avoided in this process as discussed before, although since the feedback network is external, the quiescent

current and feedback resistors could be adjusted if needed. For the sake of argument and simulation purposes, the quiescent current was set to I_Q = 5 mA. As a result,

$$R_1 + R_2 = \frac{15\ V}{5\ mA} = 3\ k\Omega \tag{5.16}$$

The feedback network is part of the DC overall gain of the regulator as shown in (4.10), although its contribution can be better understood in terms of V_{REF} and V_{OUT} as described next.

5.3 Voltage reference

The ideal voltage reference should be a voltage insensitive to changes in temperature, supply voltage and process variations. Because of these constraints and the limitations of the Cree SiC process it was decided to use an external voltage reference. V_{REF} has an impact on the gain of the feedback network $\beta_{feedback}$ based on the following equation.

$$\beta_{feedback} = \frac{V_{REF}}{V_{OUT}} = \frac{R_2}{R_1 + R_2} \tag{5.17}$$

Since the reference voltage is one of the inputs of the error amplifier, its value should be one that properly drives the gate of the input stage of the amplifier. Given that the supply for this process is 20 V and V_T, based on Table 3.1 is at least 3.4 V, a mid-rail value of 10 V was chosen for V_{REF}. This will ensure that the transistor at the input stage connected to V_{REF} will be fully on and there will still be a 10 V margin for amplification from the error amplifier. With V_{REF} defined, R_1 and R_2 can be calculated using (5.17).

$$R_2 = \frac{10\ V}{15\ V}(3\ k\Omega) = 2\ k\Omega \tag{5.18}$$

$$R_1 = 1\ k\Omega \tag{5.19}$$

Using also (5.17), the contribution of the feedback network to the overall DC gain of the regulator can be calculated as,

$$\beta_{feedback} = \frac{V_{REF}}{V_{OUT}} = \frac{10\ V}{15\ V} = -3.52\ dB \tag{5.20}$$

5.4 Compensation network

The compensation network consists of a large capacitor C_{OUT} and its ESR. Since this compensation capacitor is usually large (in the μF range), due to the limitation of this process in fabricating large on-chip capacitors, C_{OUT}, was decided to be external.

The output capacitor plays a crucial role in providing large transient currents to the load while the pass device starts responding. It also plays a role in generating the dominant pole in the frequency response as shown in (4.23). Both of these constraints determine the size of the capacitor and its ESR.

When the load current suddenly increases, it takes a finite amount of time, Δt_1 for the regulator to respond. As described in (4.5), this time depends on the bandwidth of the regulator and the time taken to charge up the parasitic capacitance of the pass device. During this time, C_{OUT} and any bypass load capacitors C_b (refer to Fig. 4.3) supply a certain amount of current, ΔI_{LOAD}, to the load. Since C_{OUT} is usually a very large capacitor when compared to C_b, most of the current will flow from C_{OUT}. There will be then, a voltage drop, ΔV_{ESR}, across the ESR defined by [1] as:

$$\Delta V_{ESR} = \left(\frac{C_{OUT}}{C_{OUT} + C_b}\right)\Delta I_{LOAD} R_{ESR} \tag{5.21}$$

This voltage drop will be proportional to the current provided by C_{OUT} and it will stay at a steady value until the regulator responds [79]. Once the regulator responds, the entire load current will be provided by the pass device and hence, the voltage drop across ESR will return to zero. From all this, it can be concluded that the voltage drop across ESR is an undesired one from the point of view of the transient response. However, the ESR of C_{OUT} is still needed since

it contributes with the capacitance to provide a zero that helps obtaining a stable frequency response for the regulator as shown in (4.24).

The aim here is to obtain a range of values for C_{OUT} and ESR that will satisfy the conditions just described. From (4.5), an approximate value for the response time of the regulator can be obtained. For the sake of argument and specifications definition, the closed loop bandwidth of this regulator is assumed to be 1 MHz. Then Δt_1 is greater than 1 μs. The load transient responses of regulators with large current capability are usually tested at a rate of 1 A/μs [51]. This implies that at least 1 A of current must be provided by C_{OUT} before the regulator responds. Assuming that the voltage drop across C_{OUT} is desired to be not larger than 150 mV during Δt_1 (1% of the desired 15 V output voltage) requires C_{OUT} to be larger than 6.67 μF. For simulation purposes, C_{OUT} was then set to 10 μF. This large value for C_{OUT} should also allow having a low frequency dominant pole to ensure the stability of the regulator.

The value for ESR will have to be decided through simulations. It is only known at this point that it needs to be very small to improve the transient response of the regulator, but it has to be a value that still creates a zero at the right frequency to ensure stability. In addition, it is reported that capacitors usually have less than 2 Ω of ESR [58]. Based on these constraints and for initial simulation purposes, ESR was set equal to 0.5 Ω.

An additional detail regarding the output capacitor for regulators is its Equivalent Series Inductance (ESL). The ESL of a capacitor is aggravated by the parasitic inductance associated with layout and packaging. The effect of the ESL is directly proportional to the load current rate change. As mentioned before a 1 A/μs rate is typical of large load current regulators. Typical values for ESL are less than 5 nH [1] which implies a voltage drop of 5 mV. This is about

0.033% of the desired output voltage of the regulator. As a result, even though ESL could create an undesired voltage drop, the current capacitor technologies avoid such situations.

5.5 Error amplifier

The error amplifier needs to magnify the difference between the change in the regulator output voltage detected by the feedback network, and the reference voltage. The error signal will drive the gate of the pass device accordingly and therefore, the gain of this signal is the most critical feature of the amplifier. The amplifier by itself does not need to be frequency stable; its only function is the amplification of the error. However, special attention has to be placed to the poles generated by the amplifier. As long as these poles are located at frequencies larger than the unity gain frequency of the regulator, they will have no effect in the regulator performance.

Based on the decisions at the beginning of this chapter concerning the design of this linear regulator, the error amplifier will not employ NMOS depletion devices as loads. Resistors will be used as loads in order to minimize risks. In addition to this, due to the same reasons why the depletion devices are avoided as loads, all the transistors in the error amplifier will be enhancement devices.

The first decision to be made is what topology to use. Based on the previous discussion, NMOS enhancement devices will be the input stage with resistors as loads. The tail current will also be an enhancement device biased by another enhancement device. Due to the lack of PMOS devices and to avoid substrate bias voltage conditions on the transistors, the error amplifier will be differential ended. Fig. 5.3 shows a schematic of the input stage of the error amplifier. Since only one output of the differential ended error amplifier is needed to drive the gate of the pass device, only half of the voltage gain from the error amplifier will be used by the regulator. This implies a 6 dB gain loss that will have to be taken into account for gain calculations.

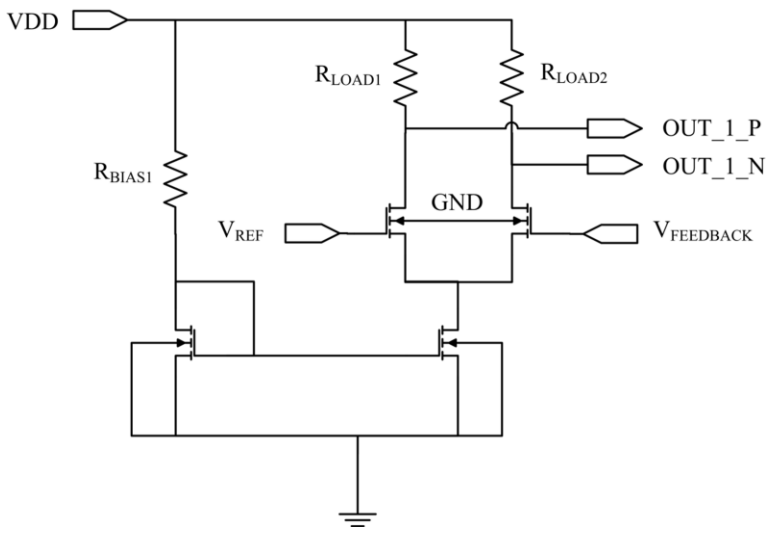


Fig. 5.3 – Input stage of the error amplifier.

In order to ensure functionality of this linear regulator, a simple approach similar to the one presented in [67] was selected for the error amplifier. The goal is to obtain as much gain as possible while keeping the regulator stable. Therefore, a large gain input stage followed by two medium gain stages was decided to be used for the error amplifier. All stages will have the same topology. Fig. 5.4 shows a schematic of the error amplifier topology decided for this linear regulator. Since there are 3 stages, OUT_3_N is the signal used to drive the gate of the pass device.

The reason for the intermediate stages to not have the same gain as the input stage is to make sure that the poles from those stages are located at higher frequencies. From the small-signal circuit for the input stage, the gain and pole for each stage can be obtained. Fig. 5.5 shows the circuit used for this analysis. From Fig. 5.5, it can be determined that the total gain A_G for each stage, and the pole P_{error} associated with it, will be equal to,

$$A_G = g_m(r_o||R_{LOAD}) \tag{5.22}$$

$$P_{error} = \frac{1}{2\pi(r_o||R_{LOAD})C_{in}} \tag{5.23}$$

where C_{in} is the gate capacitance of the transistor in the following gain stage. For the last stage, C_{in} will be equal to the gate capacitance of the pass device.

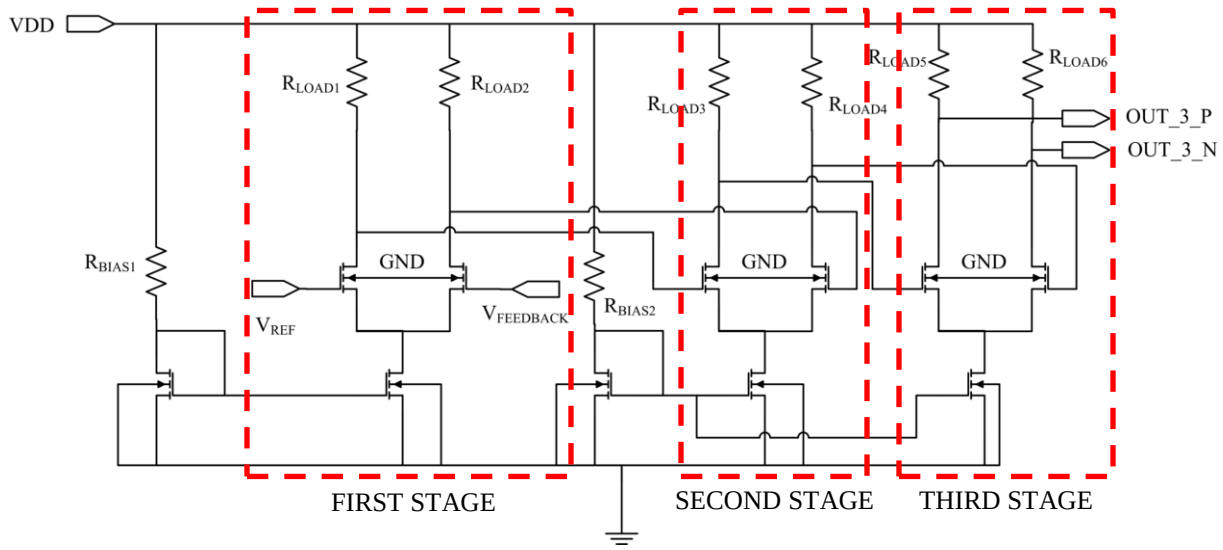


Fig. 5.4 – Differential ended error amplifier schematic. The input stage is followed by two medium gain stages.

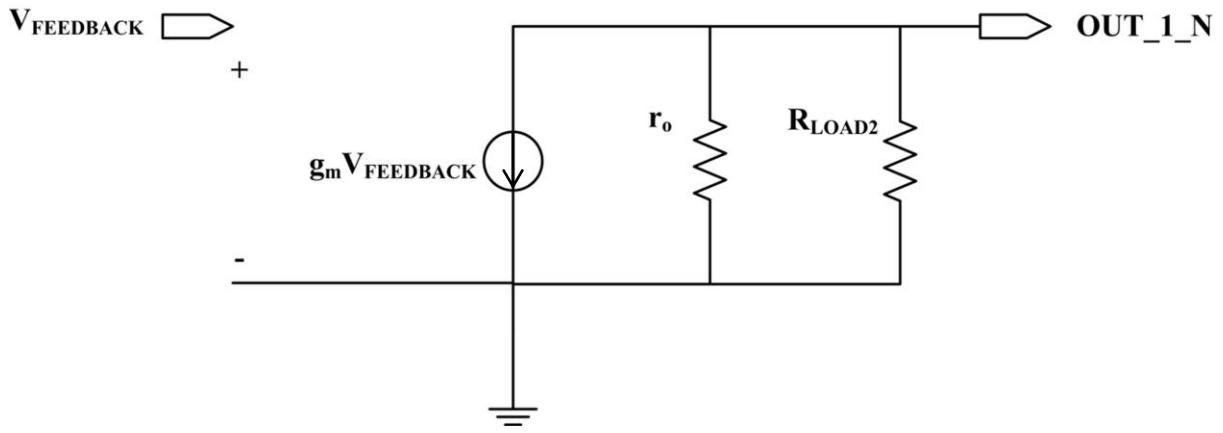


Fig. 5.5 – Small-signal circuit of the input stage of the error amplifier.

From (5.22) it can be seen that specific values for the transconductance g_m and the output resistance r_o of the transistors used in each stage are needed in order to calculate the gain from

each stage. A larger transconductance and a large output resistance will maximize the gain. A tradeoff however, will be needed since a larger drain current I_D in a transistor implies a reduction in the output resistance as given in (5.13), but it also means a larger transconductance as given in (5.24),

$$g_m = [2I_D k'(\frac{W}{L})]^{\frac{1}{2}} \tag{5.24}$$

From (5.23) it can be concluded that since the poles for each stage will be the product between the output resistance of the stage and the gate capacitance of the following stage, decreasing the transistor W/L ratio of the following stage will decrease the gate capacitance and hence, will move the pole to higher frequencies. It should be evident that by doing this, the drain current of the following stage will decrease, which as mentioned before, will imply a reduction in gain. The difference in drain current (and for that matter, tail current) among the stages is the reason why the second and third stage of the error amplifier in Fig. 5.4 do not use the same bias voltage for the tail current transistor. The reason why the bias current for the input stage was not scaled for the second and third stage is because the models did not reflect accurate current mirrors for this process. Similar to other situations, it was decided to minimize the risks by simply using an independent bias current for the second and third stage.

The next step before choosing the final values for the transistors and resistors shown in Fig. 5.4 is to determine the DC bias point needed from the error amplifier to properly drive the pass device. The most sensitive bias point is when the load current is zero since the pass device is almost turned off. An inaccurate bias point in this situation will imply that:

- Either the pass device would be off, making the regulator output 0 V.

- Or, the pass device would be delivering unnecessary current to the load or that the quiescent current would be larger than designed for. In either case, the efficiency of the regulator would be affected.

  The bias point at no load V_G, can be approximated by using (5.1) where

$$V_{DS,SAT} = V_{GS} - V_T \tag{5.25}$$

The rest of the unknowns in (5.1) have been already determined and are summarized in Table 5.3. It should be noticed that the value for V_T used in these calculations is -2.5 V rather than -2 V as shown in Table 3.1. This is due to the large number of transistors in parallel used for the pass device. At a specific gate voltage, the drain current for a single transistor will be multiplied by the number of transistors in parallel. Therefore, in order to meet the 5 mA requirement for the quiescent current, the transistors need to be even "less" turned-on so that the total current in the pass device does not exceed the specification. In addition, it was decided to use 2000, 32 μm x 2 μm depletion devices in parallel, which is a larger number than the 1715 transistors shown in Table 5.2. As explained then, the intention is to minimize the risk by foreseeing limitations in the drain current due to the substrate bias voltage. However, the 285 additional transistors for the pass device play a role in the calculation for the gate bias voltage at no load since their current is being added up with the rest of the devices.

The result for V_G was approximately 12.57 V for the linear regulator with no load current. This implies that in order to obtain this DC voltage in OUT_3_N, compromises among the drain current, load resistors and DC output values for each stage have to take place. In order to allow enough room for the DC swing of each stage due to the changes in the load current, it was decided to have a 10 VDC output from the input stage and about 11 VDC from the second stage. The DC output for the third stage is equal to the V_G value just determined. Table 5.4 shows the

final values for parts of the error amplifier used for this linear regulator (Fig. 5.4). All transistors are 32 μm x 2 μm enhancement devices.

Table 5.3 – Parameters used to Determine the Gate Bias Voltage for the Pass Device with No Load.

W/L	32000
I_Q	5 mA
V_S	15 V
V_T	-2.5 V
k’	70.44 μA/V^2

Table 5.4 – Final Values for the Parts of the Error Amplifier Shown in Fig. 5.4.

INPUT STAGE		**CONSTRAINT**
Input transistors multiplicity	100	Input characteristics simulations.
R_{LOAD1}=R_{LOAD2}	24.3 kΩ	DC output ~ 10 V
R_{BIAS1}	15.1 kΩ	V_{GS} for trail transistor
Tail transistor multiplicity	5	Input characteristics simulations.
Tail current	~0.8 mA	Largest gain
SECOND STAGE		**CONSTRAINT**
Input transistors multiplicity	10	Low gate capacitance
R_{LOAD3}=R_{LOAD4}	43.7 kΩ	DC output ~ 11 V
R_{BIAS2}	32.7 kΩ	V_{GS} for trail transistor
Tail transistor multiplicity	5	Input characteristics simulations.
Tail current	~0.4 mA	Medium gain
THIRD STAGE		**CONSTRAINT**
Input transistors multiplicity	10	Low gate capacitance
R_{LOAD5}=R_{LOAD6}	35.3 kΩ	DC output ~ 12.6 V
Tail transistor multiplicity	5	V_{GS} for trail transistor
Tail current	~0.4 mA	Input characteristics simulations.

In order to calculate the gain from each stage using (5.23), approximated values for the transconductance and output resistance of the input transistors for each stage need to be

determined. As shown in Section 3.3, these parameters vary a lot in this process depending on the voltages at the terminals of the transistors. After initial simulations of the entire regulator were run, the input transistors for each stage of the error amplifier had an average value for V_{DS} and V_{SB} of about 5 V under no load conditions for the regulator. With this information and using Figs. 3.8 and 3.9, approximated values for g_m and r_o can be obtained. Table 5.5 shows the results. It should be noted that Figs. 3.8 and 3.9 are for a 32 μm x 2 μm enhancement device with a multiplicity of 1. Table 5.5 accounts for the multiplicity of the transistors in each stage.

Table 5.5 – Approximated g_m and r_o Values for the Transistors in the Different Stages in the Error Amplifier During No Load Conditions.

FIRST STAGE		
Temperature (°C)	**g_m (mA/V)**	**r_o (kΩ)**
25 (~V_{GS}=4 V)	0.639	32.24
125 (~V_{GS}=3.5 V)	0.557	35.37
225 (~V_{GS}=3.3 V)	0.583	34.22
SECOND AND THIRD STAGE		
Temperature (°C)	**g_m (mA/V)**	**r_o (kΩ)**
25(~V_{GS}=5.3 V)	0.129	194.3
125 (~V_{GS}=5 V)	0.132	193.8
225 (~V_{GS}=4.7 V)	0.113	196.1

Using the values from Table 5.5 and (5.23), the gain for the error amplifier can be calculated. The results are summarized in Table 5.6. The output resistance for each stage has to be calculated using the load resistor values from Table 5.4. In addition, the multiplicity of the

transistors for each stage has to be taken into account, noticing that for r_o, the relationship is inversely proportional.

Table 5.6 – Voltage Gain for the Error Amplifier Across Temperature.

Temperature (°C)	Output resistance (kΩ)			Gain (dB)			
	Stage 1	Stage 2	Stage 3	Stage 1	Stage 2	Stage 3	Error amplifier
25	13.86	35.68	29.87	18.94	13.24	11.70	43.88
125	14.40	35.66	29.86	18.08	13.44	11.89	43.41
225	14.21	35.74	29.92	18.36	12.15	10.60	41.11

It can be observed that the gain of the error amplifier remains fairly constant over the temperature range. This is due to the changes in the current through the devices across temperature which forces the error amplifier to adjust the output from each stage accordingly, hence there are different V_{GS} values for each stage in Table 5.5. It is also important to remember that the total gain for the error amplifier in Table 5.6 is the differential gain. Since only one output from the error amplifier is being used, the gain from the error amplifier as part of the regulator is decreased by 6 dB. This results in an average gain contribution across temperature of about 36.8 dB to the whole regulator gain. This gain is not final since the losses from the pass device and feedback network have to be taken into account. These details will be discussed in the next section.

It should be noted that the gain values in Table 5.6 are under no load condition. These values are expected to change under full load conditions since the error amplifier will respond to the changes in the load. These changes will directly impact the transconductance and output resistance values used to calculate the gain.

5.6 Linear voltage regulator

The design of the error amplifier concluded the design of the linear voltage regulator. Fig. 5.6 shows a schematic of the entire regulator. For simulation purposes and in compliance with the fact that $C_b << C_{OUT}$, C_b was set to 0.3 µF for simulation purposes. This value for C_b assumes three, 0.1 µF decoupling capacitors in parallel used for three different circuits powered by this linear regulator. The 0.1 µF value for a decoupling capacitor is a common value found in many datasheets and application manuals, but mainly, it is a value smaller enough than C_{OUT} (by a factor of 100) so that it will not interfere with the dominant pole created by C_{OUT} in the frequency response of the regulator. R_{LOAD} represents the load current and assuming a 15 V constant output voltage across temperature, R_{LOAD} will range from about 5 Ω (3 A load) to an infinite impedance (no load). The frequency response of the linear regulator was then simulated under all conditions to verify stability.

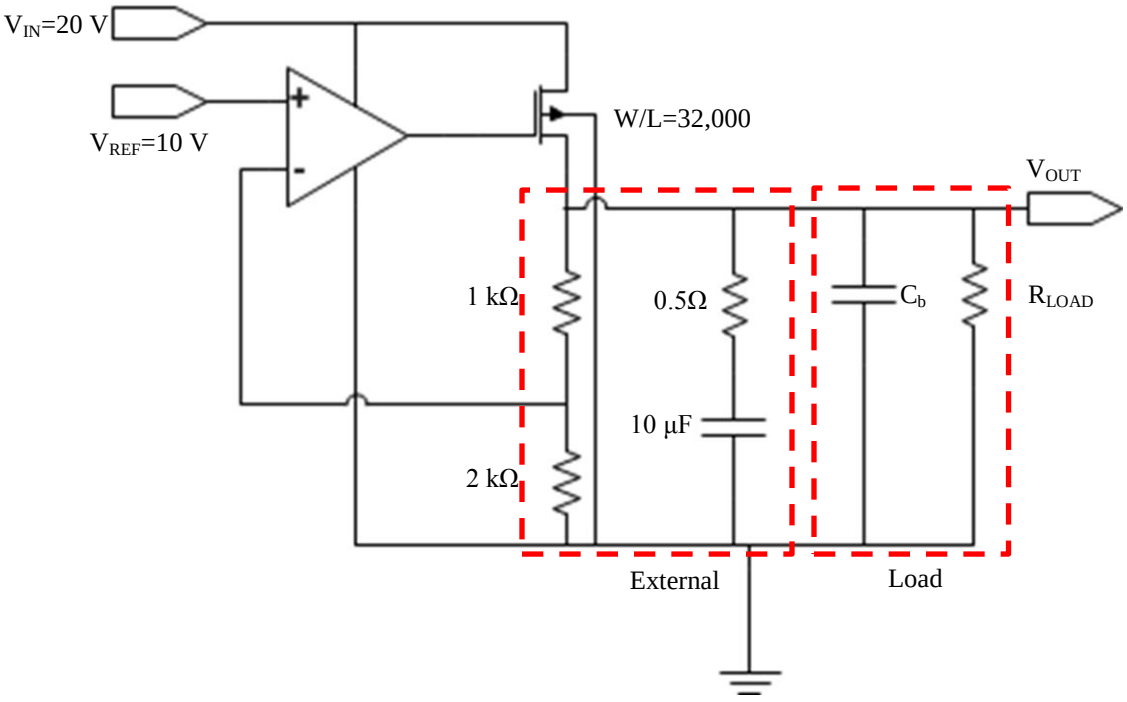


Fig. 5.6 – Final linear regulator design.

5.7 Frequency response

An important value to determine before simulation is the DC gain of the common-drain configuration of the pass device as shown in (5.13). As was mentioned in Section 5.5, the DC voltage needed at the gate of the pass device under no load conditions is 12.57 V. Since the source of the pass device will be 15 V, V_{GS} = -2.43 V, V_{DS} = 5 V and V_{SB} = 15 V. Under these conditions, the transconductance, output resistance and gain of the pass device under no load conditions can be approximated to be the values shown in Table 5.7.

Table 5.7 – Gain Calculations of the Pass Device Under No Load Conditions.

g_m (mA/V)	r_o (kΩ)	Gain (dB)
5.347	0.774	-1.88

With this last stage gain known, the overall gain response under no load conditions for the regulator can be approximated using the values shown in Table 5.8.

Table 5.8 – Linear Regulator Gain Calculations Under No Load Conditions.

Element	Gain (dB)
Pass device	-1.88
Feedback network	-3.52
Error amplifier	36.8
Total	31.4

The total gain under no load conditions is not expected to change over temperature since most of this gain comes from the error amplifier and it was shown to be fairly constant across the entire temperature range in Table 5.6. The gain is, however, expected to change at full load since the small-signal parameters of every transistor in the circuit will vary and the error amplifier will have to respond to the changes in the load. This might imply that, at full load, the voltage needed at the gate of the pass device might be very high and hence the current will be reduced in the stages of the error amplifier. As has been discussed before, reducing the current affects the transconductance and output resistance values of the devices.

The linear regulator was simulated using the approach shown in Fig. 4.5. The frequency response at 25 °C under no load conditions is shown in Fig 5.7. These simulation results contain important information about the linear regulator design. First of all, the overall gain of the regulator is 30.42 dB, very close value to the calculated gain of 31.4 dB presented in Table 5.8.

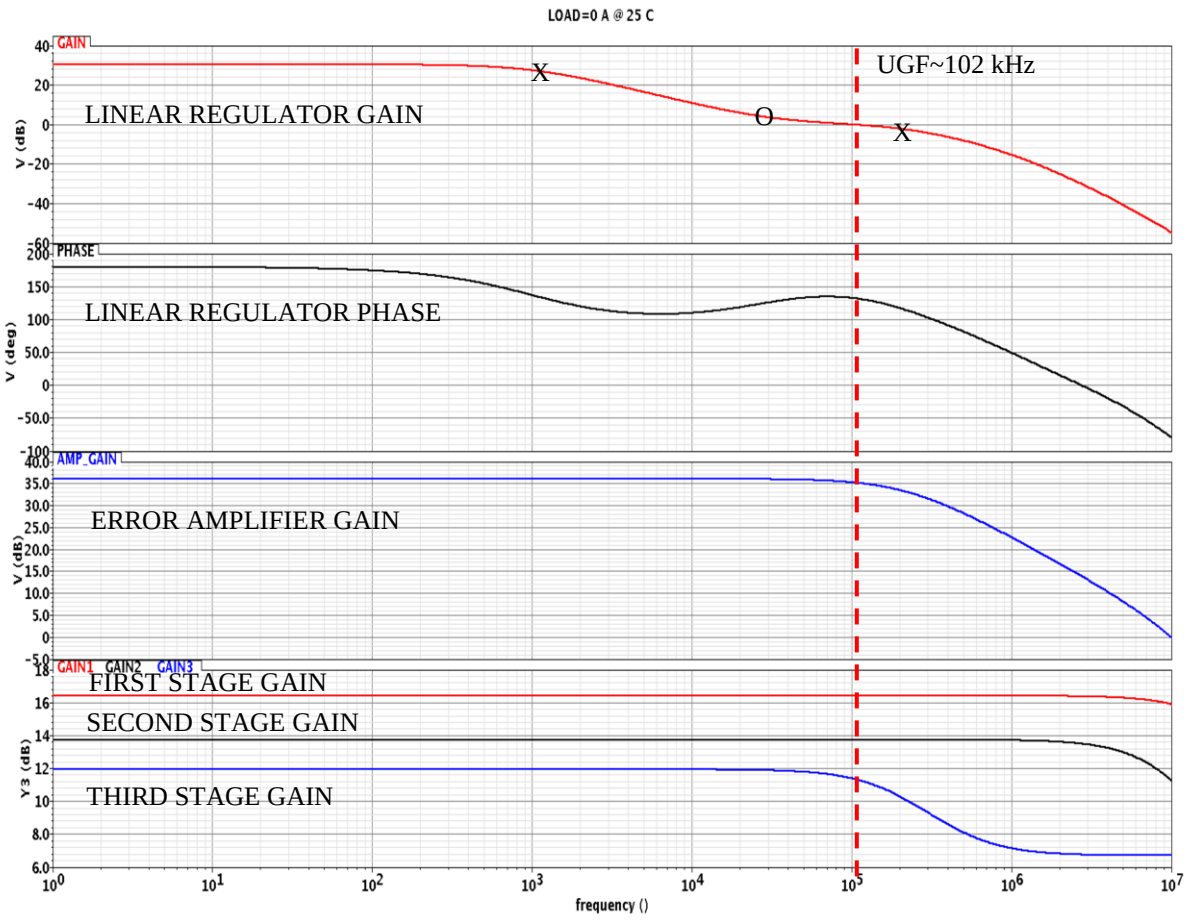


Fig. 5.7 – Frequency response of the linear regulator at 25 °C under no load conditions. From the error amplifier stages gain, it can be seen that the poles from the first and second stage (black and red curves respectively) are beyond the unity gain frequency of the regulator. The third gain stage (blue) generates the pole from the pass device gate capacitance right before crossing the 0 dB line.

From the phase response, a pole and a zero occur before crossing the 0 dB at a frequency of approximately 102 kHz. A second pole occurs right after the 0 dB crossing which is not the ideal response for a stable regulator. The goal is to cross the 0 dB line with a -20 dB/decade slope, achieved by creating a pole-zero-pole sequence before the crossing in the frequency response. In this case, since the gate capacitance of the pass device (second pole) is decreased by the 15 V substrate bias voltage condition, this pole is located at a frequency slightly larger than

the 0 dB crossing frequency. This situation would normally not occur in a process where the substrate bias voltage would not have such a significant effect. Nonetheless, the regulator is stable with a phase margin of 132 degrees and the flattening at the 0 dB crossing point is due to the proximity of the zero and the second pole.

The simulated error amplifier gain is 36.09 dB, which is very close to the calculated gain of 36.8 dB presented in Table 5.8. Furthermore, the simulated gains from each stage are respectively 16.42, 13.75 and 11.94 dB, close to the calculated gains of 18.94, 13.24 and 11.70 dB presented in Table 5.6.

In addition, the poles from the second and third stage are located after the unity gain frequency of the regulator as intended. This validates the approach of using lesser gain in these stages by reducing the multiplicity and drain current of their transistors. The poles and zero from the frequency response in Fig. 5.7 can be calculated using (4.23) to (4.26). It should be noted that due to the common-drain configuration of the pass device in this design, the overall open-loop gain equation varies from (4.22). This variation is explained in the following calculations.

$$p_1 \approx \frac{1}{2\pi r_{out,pass} C_{out}} = \frac{1}{2\pi(774)(10x10^{-6})} = 20.6\ Hz \tag{5.26}$$

$$z_1 \approx \frac{1}{2\pi R_{ESR} C_{out}} = \frac{1}{2\pi(0.5)(10x10^{-6})} = 31.8\ kHz \tag{5.27}$$

$$p_2 \approx \frac{1}{2\pi r_{out,amp} C_{pass}} = \frac{1}{2\pi(29870)(26.5x10^{-12})} = 201.1\ kHz \tag{5.28}$$

$$p_3 \approx \frac{1}{2\pi R_{ESR} C_b} = \frac{1}{2\pi(0.5)(0.3x10^{-6})} = 1.06\ MHz \tag{5.29}$$

As expected, the dominant pole (p_1) does not seem to agree with the frequency response shown in Fig. 5.7 where it seems to be located around 1 kHz. The reason behind this discrepancy

is the common drain configuration of the pass device in the regulator. The behavior of the devices in this process also has a toll in this discrepancy, since the values for g_m and r_o are very sensitive to slight changes in the bias conditions for a specific situation.

In Section 4.2.2, the open-loop response equation for a regulator with a pass device in common source configuration was derived. The common source configuration was selected since most of the regulators nowadays use PMOS transistors as pass device. Due to lack of these devices in this process, this regulator was forced to have a pass device in the common drain configuration. The implications affect only the last term, $g_{m,pass}Z_{out}$, in (4.10) which is related to the gain and pole of the amplifier with the pass device. As indicated in (5.13), the gain of the common drain amplifier is slightly less than unity due to the configuration. Fig. 5.8 shows a more detailed small-signal model of the pass device for this specific regulator. The actual dominant pole location can be derived from analysis of this circuit.

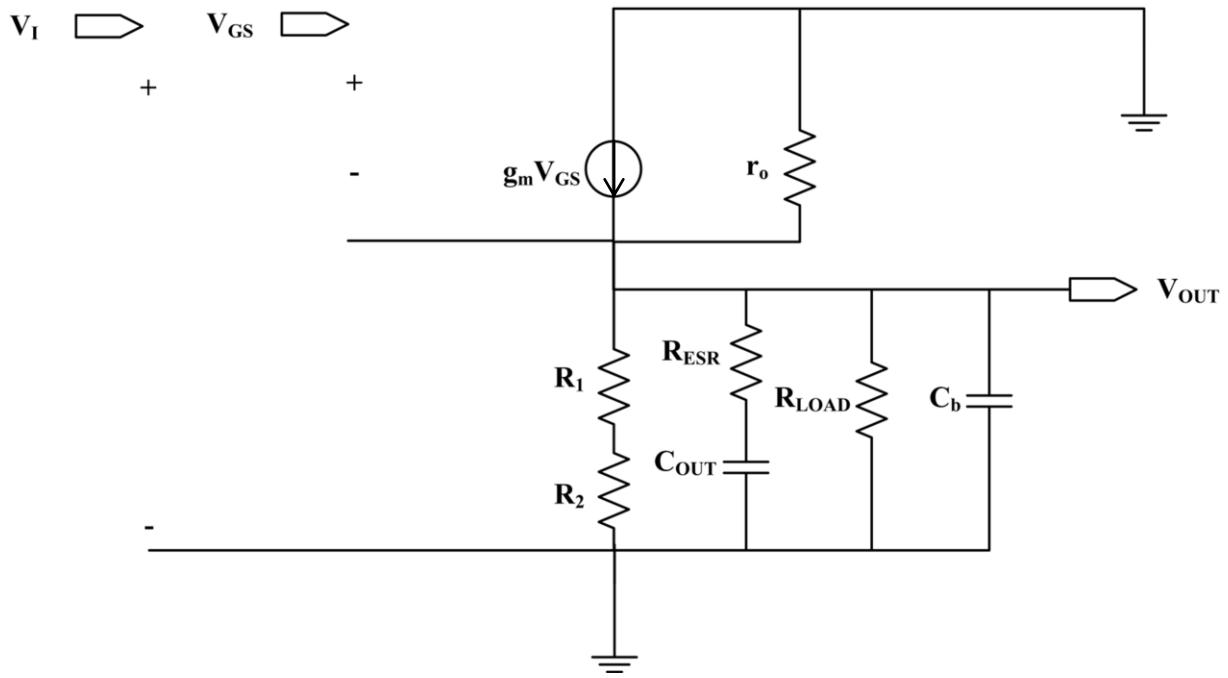


Fig. 5.8 – Complete small signal analysis of the pass device in the designed regulator.

Following a similar analysis to the one leading to (5.12), the gain of the pass device is defined as follows. For a more simple algebra, the ESR of the output capacitor (too small to be of significance) and the bypass capacitor C_b (small compared to C_{OUT}) will not be included. The C_{OUT} and r_o are the main contributors to the dominant pole. A detailed derivation of the gain of the pass device, including these terms, shows no conflict with the results of the following analysis.

$$A_{PASS} = \frac{V_{OUT}}{V_I} = \frac{V_{SOURCE}}{V_{GATE}} \tag{5.30}$$

$$V_{SOURCE} = g_m V_{GS}[r_{out,pass}||(R_1 + R_2)||R_{LOAD}||\frac{1}{sC_{OUT}}] \tag{5.31}$$

$$V_{SOURCE} = g_m(V_{GATE} - V_{SOURCE})[r_{out,pass}||(R_1 + R_2)||R_{LOAD}||\frac{1}{sC_{OUT}}] \tag{5.32}$$

$$\begin{aligned} V_{SOURCE} &= g_m V_{GATE}[r_{out,pass}||(R_1 + R_2)||R_{LOAD}||\frac{1}{sC_{OUT}}] \\ &- g_m V_{SOURCE}[r_{out,pass}||(R_1 + R_2)||R_{LOAD}||\frac{1}{sC_{OUT}}] \end{aligned} \tag{5.33}$$

$$\begin{aligned} V_{SOURCE} + g_m V_{SOURCE}[r_{out,pass}||(R_1 + R_2)||R_{LOAD}||\frac{1}{sC_{OUT}}] \\ = g_m V_{GATE}[r_{out,pass}||(R_1 + R_2)||R_{LOAD}||\frac{1}{sC_{OUT}}] \end{aligned} \tag{5.34}$$

$$\begin{aligned} V_{SOURCE}(1 + g_m[r_{out,pass}||(R_1 + R_2)||R_{LOAD}||\frac{1}{sC_{OUT}}]) \\ = g_m V_{GATE}[r_{out,pass}||(R_1 + R_2)||R_{LOAD}||\frac{1}{sC_{OUT}}] \end{aligned} \tag{5.35}$$

$$A_{PASS} = \frac{V_{OUT}}{V_I} = \frac{V_{SOURCE}}{V_{GATE}} = \frac{g_m[r_{out,pass}||(R_1 + R_2)||R_{LOAD}||\frac{1}{sC_{OUT}}]}{1 + g_m[r_{out,pass}||(R_1 + R_2)||R_{LOAD}||\frac{1}{sC_{OUT}}]} \tag{5.36}$$

Since $r_{out,pass} < R_1+R_2$ and also less than R_{LOAD} (specially at no load conditions), the gain of the pass device A_{PASS} can be simplified as

$$A_{PASS} \approx \frac{g_m(r_{out,pass} || \frac{1}{sC_{OUT}})}{1 + g_m(r_{out,pass} || \frac{1}{sC_{OUT}})} \tag{5.37}$$

$$A_{PASS} \approx \frac{g_m r_{out,pass}}{1 + g_m r_{out,pass} + s r_{out,pass} C_{OUT}} \tag{5.38}$$

$$A_{PASS} \approx \frac{\frac{g_m r_{out,pass}}{1 + g_m r_{out,pass}}}{1 + s\frac{r_{out,pass} C_{OUT}}{1 + g_m r_{out,pass}}} \tag{5.39}$$

The result in (5.39) indicates that the dominant pole p_1 is located at

$$p_1 \approx \frac{1}{2\pi \frac{r_{out,pass} C_{OUT}}{1 + g_m r_{out,pass}}} \tag{5.40}$$

As mentioned earlier, the sensitivity of the devices in this process to slight changes in the bias conditions also affected the calculated value for the dominant pole. As will be shown in Section 5.8, the actual DC voltages of the pass device under no load condition are a little bit different from the values used to calculate the small-signal parameters shown in Table 5.7. As a result, using (5.40) and the new values for g_m and r_o yields a more accurate calculated value for the dominant pole. Table 5.9 summarizes the results. It should also be remembered that since the body and source in this process are not connected, the value for g_m is affected. A more accurate calculation would include g_{mb} in the analysis.

Table 5.9 – Accurate Dominant Pole Calculations Under No Load Conditions.

DC bias values	g_m (mA/V)	r_o (kΩ)	Gain (dB)	Pole (Hz)
V_{GS}= -2.43 V, V_{DS}=5 V, V_{SB}=15 V (calculated)	5.347	0.774	-1.88	20.6
V_{GS}= -2.28 V, V_{DS}=5 V, V_{SB}=15 V (simulated)	34.2	0.136	-1.69	661

As it can be seen in Table 5.9, using both the values for g_m and r_o at the simulated DC bias conditions and the more specific equation for the dominant pole location, yield a result more in agreement with the 1 kHz location of the dominant pole shown in Fig. 5.7. The fact that the gain of the pass device did not change much validates these results. The reason for the slight change in the gain is that the changes in the DC bias condition affect g_m and r_o in different directions (g_m is proportional to $\sqrt{I_D}$ while r_o is inversely proportional to I_D). In addition, the gain of the pass device is a ratio involving both parameters and as a result, the errors in the parameters cancel out.

The simulated frequency responses under no load conditions at 25 °C, 125 °C and 225 °C are shown in Fig. 5.8. The simulation results shown in Fig. 5.8 corroborate the results shown in Table 5.6 for the calculated error amplifier gain across temperature. Since most of the gain of the regulator comes from the error amplifier and this gain stays fairly constant, the overall response of the regulator stays constant as well.

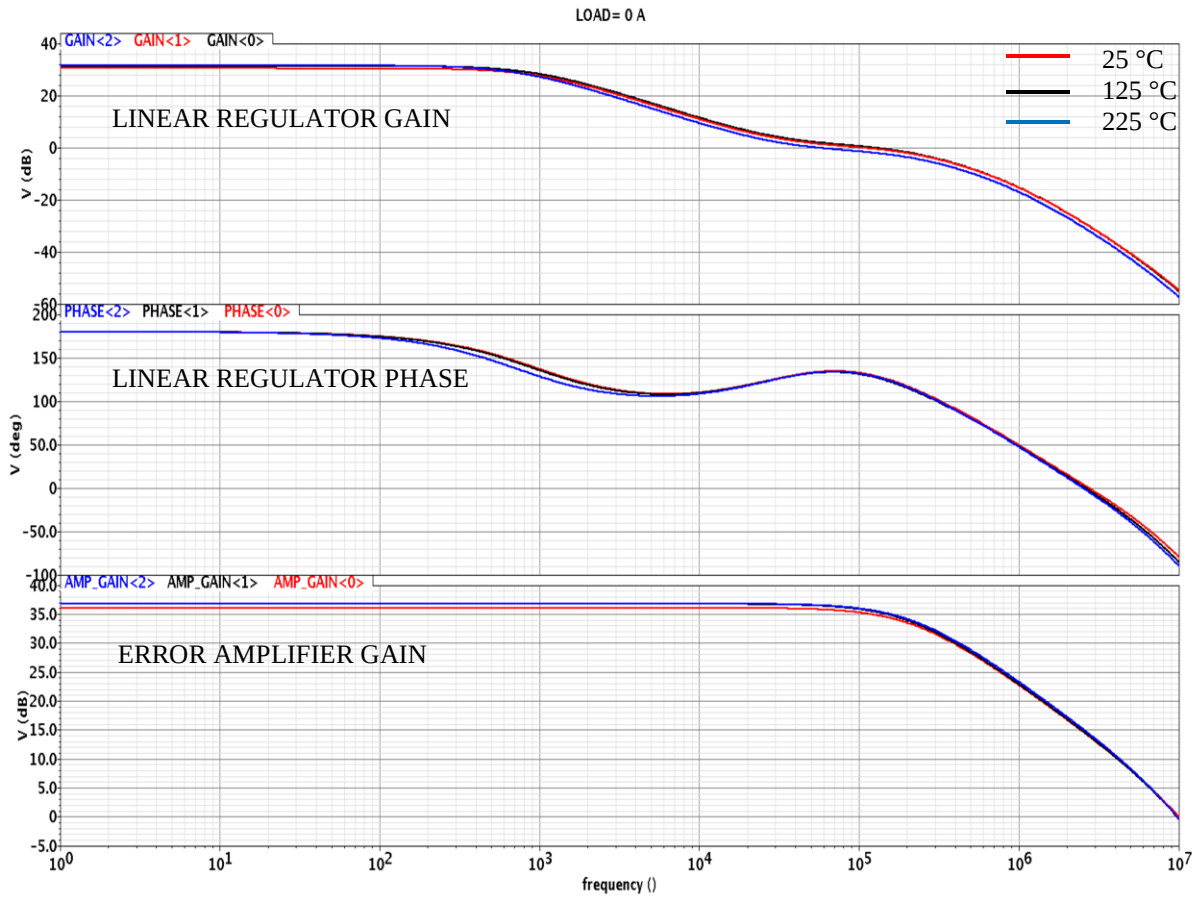


Fig. 5.8 - Frequency response of the linear regulator at 25 °C, 125 °C and 225 °C under no load conditions. The response varies vary little with temperature as expected.

The frequency response of the linear regulator at full load at 25 °C is shown in Fig. 5.9. This simulation shows a regulation gain of about 25.12 dB which represents a decrease of 5.3 dB when compared to the no load response. The error amplifier gain of 31.31 dB also shows a decrease of about 4.8 dB. From the gain in each stage, it can be seen that this overall gain loss is due to the gain loss in the third stage mainly. The reason is quite simple. The error amplifier responds to the change in load current by increasing the gate voltage applied to the pass device from 12.57 to 16.9 V. This means that the voltage drop across the load resistor in the third stage needs to be smaller. As a result, the current is reduced which translates to a smaller gain in this

stage. Table 5.10 shows a quantified analysis of the gain decrease in the third stage of the error amplifier at 25 °C.

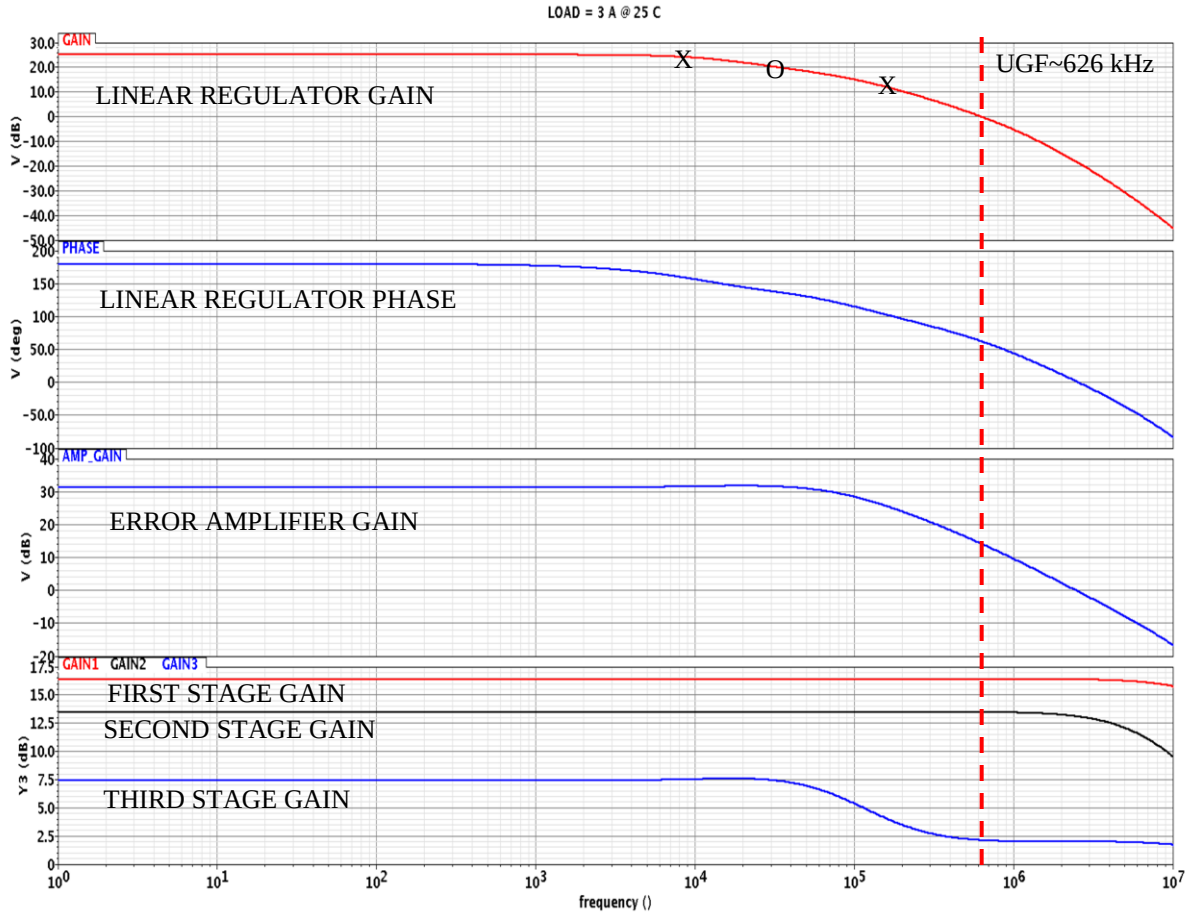


Fig. 5.9 – Frequency response of the linear regulator at 25 °C and full load (3 A). A decrease in gain is observed as well as displacement of the dominant pole to a region nearby the zero. The regulator is still stable with a phase margin of about 62 degrees and a UGF of 626 kHz.

Table 5.10 – Small-signal Parameters for the Third Stage of the Error Amplifier Under Full Load Conditions.

THIRD STAGE @V_{DS}= 11.23 V, V_{GS}=3.97 V, V_{SB}=5.67 V	
Output DC voltage (V)	16.90
g_m (μA/V)	68.73
r_o (kΩ)	245.76
R_{OUT} (kΩ)	30.88
Gain (dB)	6.54

The new 6.54 dB gain for the third stage at full load represents a loss of 5.16 dB of gain for this stage when compared to the no load condition. This result explains the overall lower gain of the regulator in Fig. 5.9. The dominant pole movement is also explained by a change in the current, except that in this case, this is due to an increase in the drain current of the pass device. The increase, based on (5.12), decreases the output resistance of the pass device and as a result, the pole moves to a higher frequency. A new calculation for this dominant pole requires simulating the pass device using the new gate voltage value of 16.9 V (from Table 5.10). From the simulation, the small-signal parameters will be used together with (5.40) to calculate the new pole location. The results are shown in Table 5.11. The values from Table 5.11 can also be used to corroborate that the pass device gain at full load is not responsible for the overall gain loss shown in Fig. 5.9. The gain of the pass device at a full load is -1.66 dB compared to the -1.69 dB gain at no load. As showed before, the overall gain loss is mainly due to the third stage of the error amplifier.

Table 5.11 – Small-signal Parameters of the Pass Device Under Full Load Conditions at 25 °C.

PASS DEVICE @V_{DS}= 5.12 V, V_{GS}=2.02 V, V_{SB}=14.88 V	
Source voltage (V)	14.88
g_m (A/V)	1.08
r_o (Ω)	4.40
Pole location (kHz)	20.81

The new calculated location for this dominant pole under full load condition agrees with the simulated location shown in Fig. 5.9 with about the same margin of error as under the no load condition. In this occasion, the gain response crosses the 0 dB line at a -20 dB/decade slope as expected due to an increase in the UGF and a small movement of the third pole to the left. This third pole, located at the gate capacitance of the pass device, moved slightly to the left due to a small increase in the output resistance of the third stage from 29.87 kΩ (shown in Table 5.6) to 30.88 kΩ (shown in Table 5.10). This changes the location of this pole to a frequency of about 139.4 kHz under full load conditions, compared to 201.1 kHz under no load conditions. The zero formed by the ESR and the output capacitor does not change its location since the resistance and the capacitance are not dependent on load current changes or temperature. The simulated frequency responses under full load conditions at 25 °C, 125 °C and 225 °C are shown in Fig. 5.10.

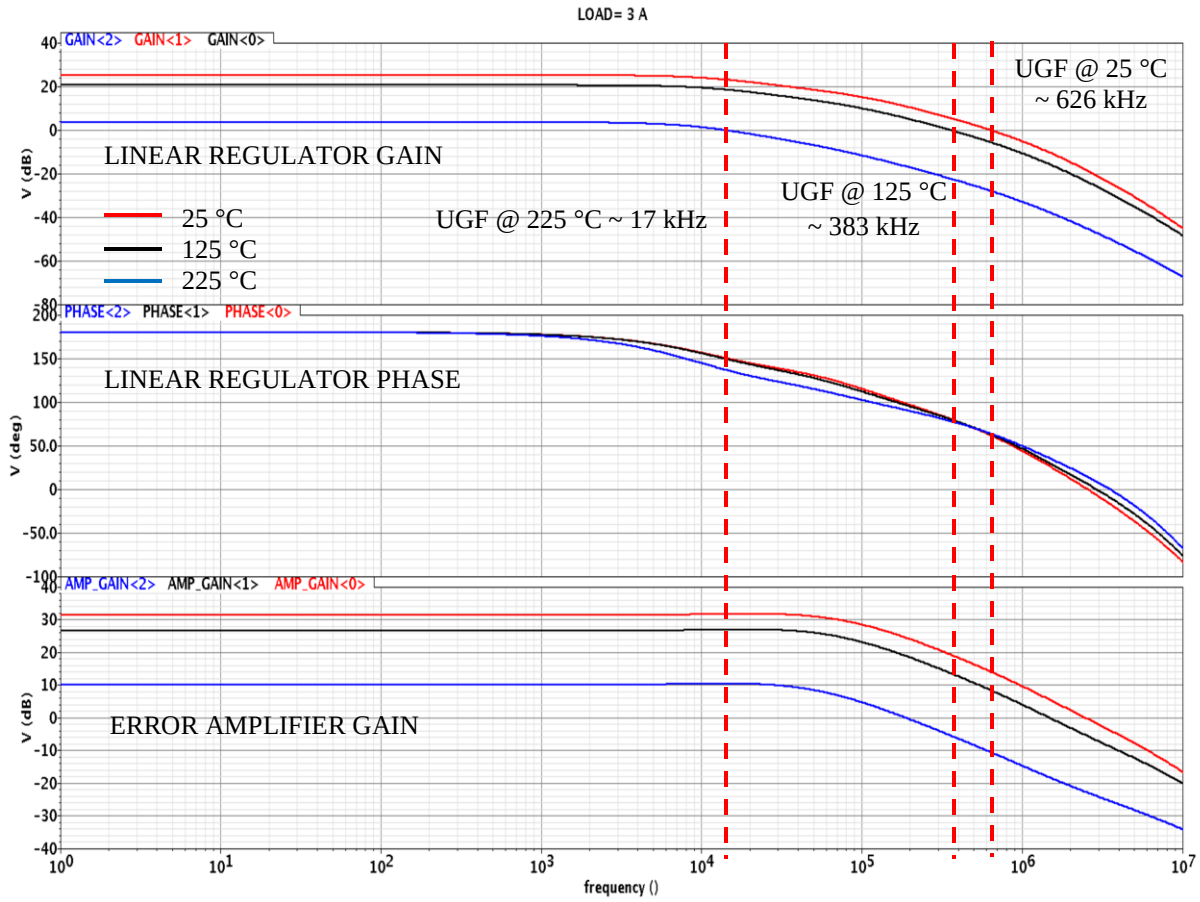


Fig. 5.10 - Frequency response of the linear regulator at 25 °C, 125 °C and 225 °C under full load conditions. From the phase response it can be seen that the poles and zero barely move with temperature. The main issue with temperature variation is the decrease in the overall gain of the regulator which tracks the same behavior as the error amplifier gain.

The decrease in the overall gain from 30.42 to 25.12 dB due to the change in load current at 25 °C is explained by the reduction in the gain of the third stage of the error amplifier. In the same manner, the reduction in the overall gain at full load when the temperature is increased to 125 °C and 225 °C can be explained by recalculating the gain using the new biasing conditions in the transistors of the third stage of the error amplifier. Table 5.12 shows these biasing voltages at the two temperatures and the small-signal parameters under those conditions.

Table 5.12 - Small-signal Parameters for the Third Stage of the Error Amplifier Under Full Load Conditions at 125 °C and 225 °C.

Temperature	Output (V)	g_m (μA/V)	r_o (kΩ)	R_{OUT} (kΩ)	Gain (dB)
125 °C (V_{DS} = 11.99 V, V_{GS} = 3.30 V, V_{SB} = 5.65 V)	17.64	56.11	292.63	31.50	4.95
225 °C (V_{DS} = 14.21 V, V_{GS} = 1.74 V, V_{SB} = 4.98 V)	19.19	26.61	599.14	33.34	-1.04

From Table 5.12 it can be seen that the decrease in the overall gain of the regulator at high temperatures is again mainly due to the error amplifier. In the third stage of the error amplifier, the 4.95 and -1.04 dB gain at 125 °C and 225 °C, respectively, imply a loss of gain of 1.59 and 7.58 dB, respectively, from the gain at full load condition at 25 °C for this stage. However, under full load conditions, the first and second stages also suffer from gain reduction at high temperatures. A similar analysis reveals that the sum of all these gain reductions does in fact agree with the overall gain reduction of the regulator across temperature as observed in Fig. 5.10.

At 225 °C the gain loss is considerable and therefore, a negative impact in the transient response of the regulator should be expected. The gain loss is, however, an expected effect of regulation. The error amplifier is providing a feedback and therefore adjusting its output accordingly. The first reaction to improve this situation would be to decrease the voltage reference in order to allow for a larger output swing of the error amplifier when large load

current changes occur. The problem with this is that by decreasing the voltage reference, the constant negative gain from the feedback network is increased as described in (5.20). Table 5.13 summarizes the simulated frequency response results of the linear regulator. From the table, a decrease in the UGF under full load conditions can be observed as temperature increases. This change is also due to the gain reduction previously described. As the DC gain decreases, the curve will cross the 0 dB sooner and this will also result in an increase in phase margin.

Table 5.13 – Simulated Results from the Frequency Response of the Linear Regulator.

Temperature (°C)	Load (A)	Dominant pole (kHz)	UGF (kHz)	DC gain (dB)	Phase margin (deg)	Error amp gain (dB)
25	0	1.03(0.66)	102	30.42	132	36.09
	3	10(20.81)	626	25.12	62	31.31
125	0	1.03(0.66)	102	31.00	132	36.09
	3	10(20.81)	383	20.64	79	26.61
225	0	1.03(0.66)	46	30.42	132	36.09
	3	10(20.81)	17	4.58	135	11.03

Simulated(Calculated)

In addition to showing the change in UGF, the results in Table 5.12 indicate a temperature insensitive linear voltage regulator under no load conditions. Temperature comes into play under full load conditions by reducing the gain of the regulator. The palpable effect will be noticeable in the transient response discussed in the following section.

5.8 Transient response

After the frequency response of the linear regulator indicated stability, the regulator was then simulated with large load dumps. Fig. 5.11 shows the load regulation capabilities of the linear regulator at 25 °C, 125 °C and 225 °C to a sudden 3 A load current change at a rate of 1 A/μs. The results are summarized in Table 5.14.

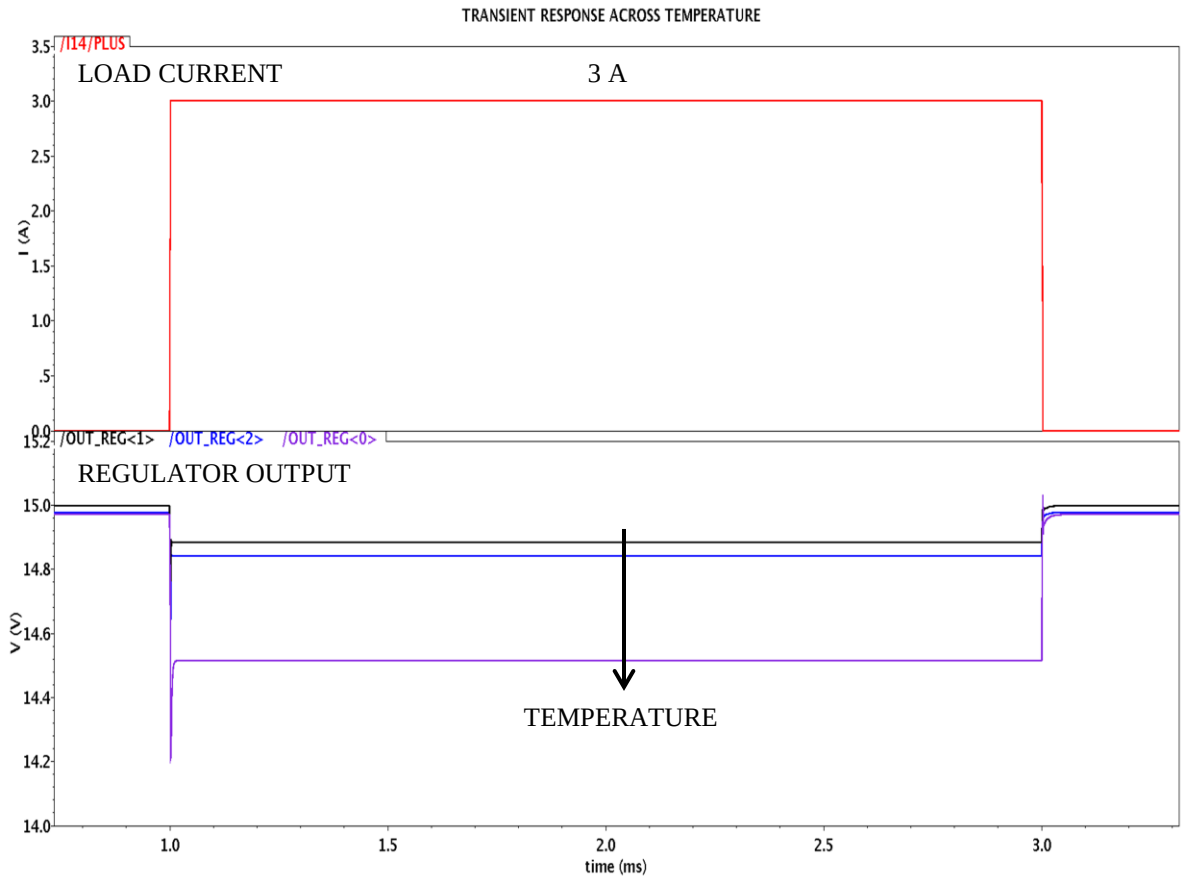


Fig. 5.11 – Load regulation across temperature

Table 5.14 – Load Regulation Simulated Results Across Temperature.

Temperature (°C)	Load (A)	V_{OUT} (V)	Load regulation (mV/A)	Load regulation (%)
25	0	14.99	36.67	0.73
	3	14.88		
125	0	14.98	46.67	0.93
	3	14.84		
225	0	14.97	143.33	2.87
	3	14.54		

As expected, the load regulation worsens at 225 °C due to a decrease in the overall gain of the regulator as described in (4.3). The load regulation is still less than 3% (or 0.96 %/A) across the entire temperature range. This value is about 10 times larger than a Si, 3A LDO with a supply voltage of 0.8 to 5.5 V and rated up to 125 °C [80].

Undershoot and overshoot voltages of the transient response (ΔV_{TRAN+} and ΔV_{TRAN-} in Fig. 4.2) are also of interest. Zoomed in pictures of the areas of interest are shown in Fig. 5.12 and 5.13. The results are summarized in Table 5.15.

The undershoot voltage is a very important parameter for the proper operation of the circuits powered by the regulator. A very low undershoot voltage could force these circuits to stop operating. This parameter can be calculated using (4.6) and then compared to the simulated value. In order to calculate the undershoot voltage; the voltage drop across ESR and the momentary current supplied by C_{OUT} (while the regulator responds) need to be known. Table 5.16 shows the simulated ΔV_{ESR} values and the comparison between the simulated and

calculated values for the undershoot voltage ΔV_{TRAN+}. The current supplied by C_{OUT} can be calculated using ΔV_{ESR} and ESR = 0.5 Ω.

Table 5.15 – Undershoot and Overshoot Values due to a 3 A Load Current Change.

Temperature (°C)	Undershoot (V)	ΔV_{TRAN+} (mV)	Overshoot (V)	ΔV_{TRAN-} (mV)
25	14.76	230	15.01	130
125	14.66	320	14.99	150
225	14.27	700	15.02	480

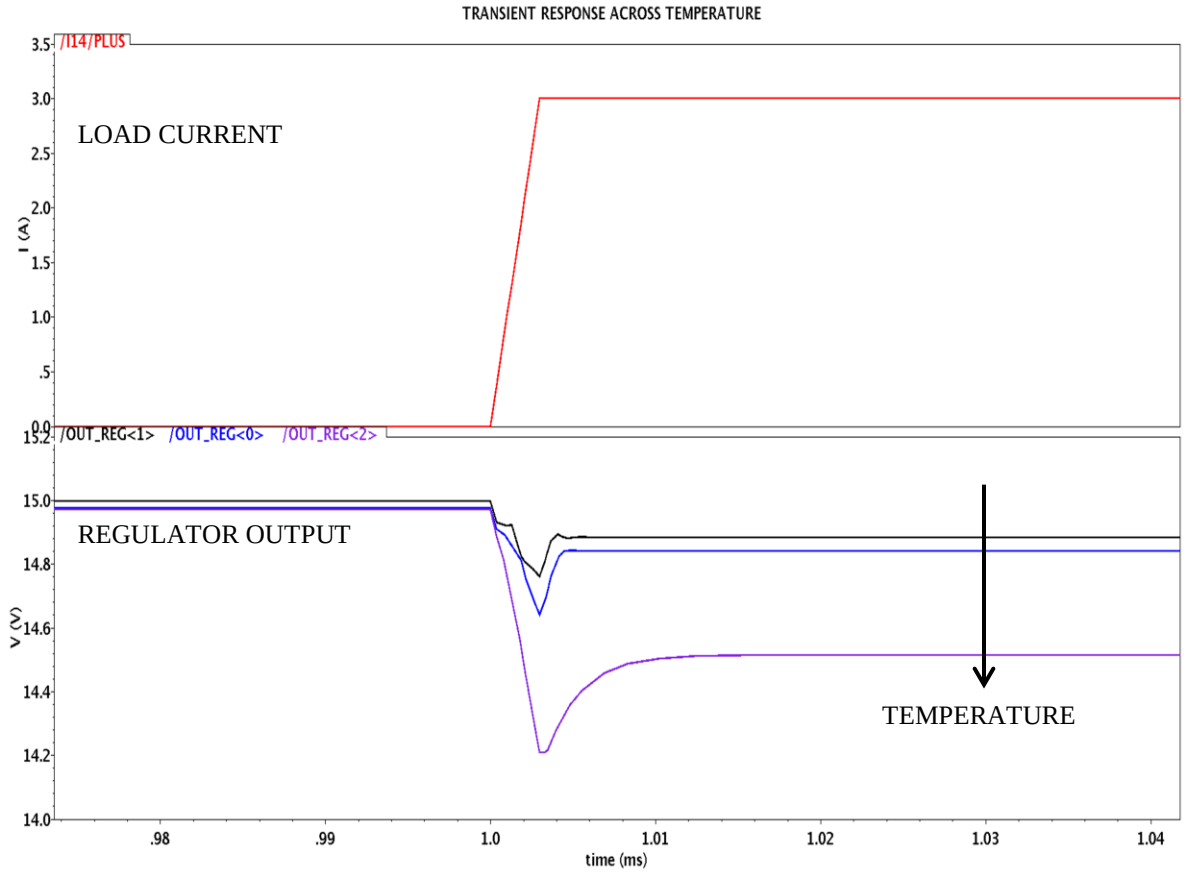


Fig. 5.12 – Transient undershoot voltage due to a 3 A load current change.

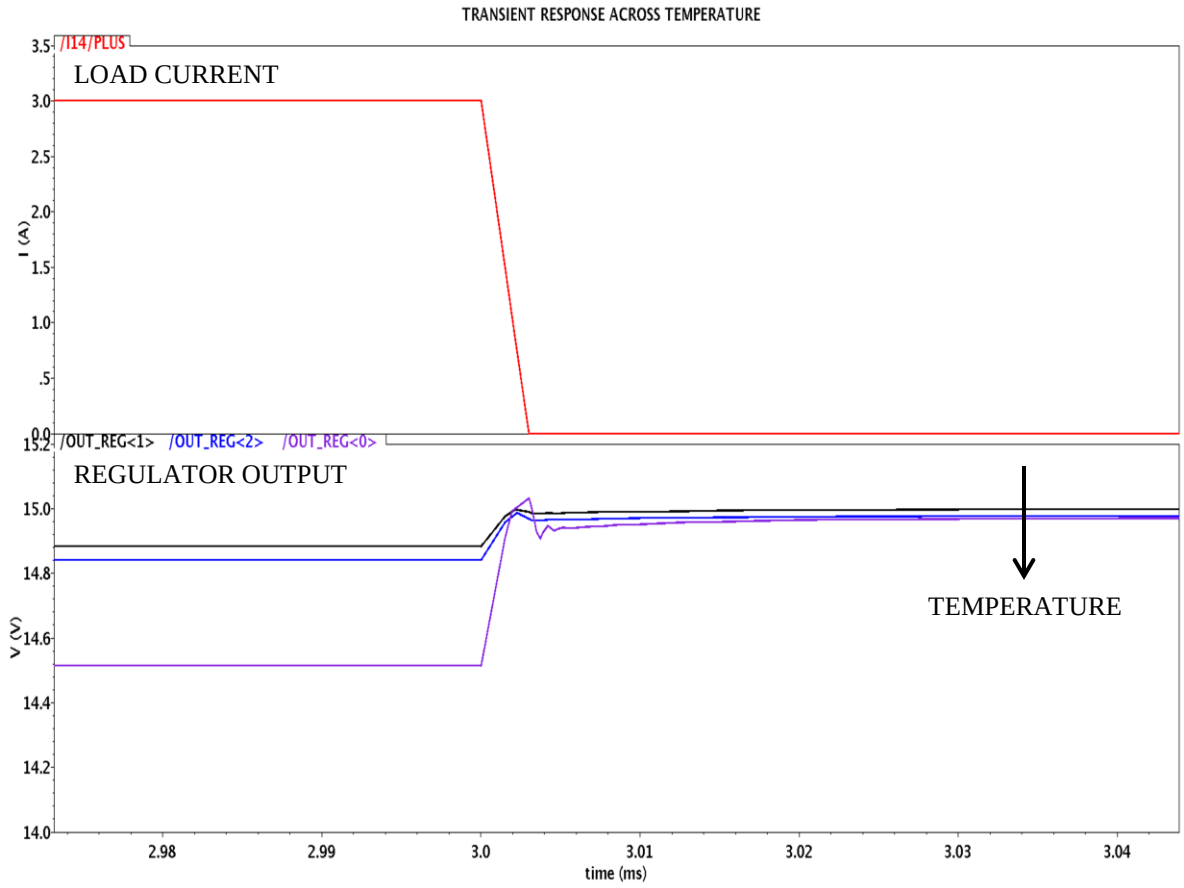


Fig. 5.13 – Transient overshoot voltage due to a 3 A load current change.

Table 5.16 – Simulated and Calculated Values Comparison for the Undershoot Voltage.

Temperature (°C)	**ΔV_{ESR} (mV)**	**ΔV_{TRAN+} simulated (V)**	**ΔV_{TRAN+} calculated (V)**
25	174	0.23	0.27
125	240	0.32	0.38
225	527	0.70	0.83

The response time of the linear regulator (Δt_1 in Fig. 4.2) is another parameter of interest. The response time as described in (4.5) depends on the closed loop bandwidth BW_{CL}, the gate capacitance of the pass device C_{PAR}, the voltage variation at the gate of the pass device ΔV, and the current applied to this capacitance I_{SR}. Since the regulator is a closed loop system, the values for BW_{CL} are the same as the UGF values shown in Table 5.13. The simulated values for the remaining parameters across temperature are shown in Table 5.17.

Table 5.17 – Simulated Parameter Values Affecting the Regulator Response Time.

Temperature (°C)	Δt1 (µs)	ΔV (V)	ISR (µA)
25	2.97	4.17	68.2
125	2.99	4.21	63.2
225	2.99	5.65	80.3

Using Table 5.17, values for the response time can be calculated using (4.5). C_{PAR} is the gate capacitance of the pass device equal to 26.5 pF as described in Section 3.3. Table 5.18 shows the comparison between the measured and the calculated values for the response time.

Table 5.18 – Simulated and Calculated Values Comparison for the Regulator Response Time.

Temperature (°C)	Δt1 simulated (µs)	Δt1 calculated (µs)
25	2.97	3.22
125	2.99	4.37
225	2.99	60.69

The very large difference between the measured and calculated value for the response time of the regulator at 225 °C is due to the very low bandwidth of the regulator at that temperature. Since the response time in (4.5) is inversely proportional to the bandwidth, the response time increases. As discussed before, the low bandwidth is the result of a very drastic reduction in the gain of the regulator. A better calculated value for the response time can be obtained by using a more accurate equation for (4.5) defined as [1]:

$$\Delta t_1 \approx \frac{0.37}{BW_{CL}} + C_{par}\frac{\Delta V}{I_{SR}} \tag{5.41}$$

Using this equation, the value Δt_1 at 225 °C reduces to 23.6 µs. Even though this result is about 8 times larger than the simulated value, both (4.5) and (5.41) are intended to provide approximate values for the time response of the regulator. In addition to this, the largest discrepancy occurs at high temperatures, when the interface traps present in the SiC/SiO_2 interface of the enhancement devices alter the behavior of the devices as discussed in Section 3.3.

An additional important feature to notice from Fig. 5.12 and 5.13 is the lack of ringing in the output of the regulator when the sudden load current change occurs. Typically, four rings or less are a sign of enough phase margin for a stable regulator [58]. As shown in Table 5.12, the phase margin across temperature is never less than 60 degrees.

As discussed in Section 5.2, one of the benefits of having an external feedback network is the ability to obtain different regulated output voltages by simply changing the value of R_1. Fig. 5.14 shows the different output voltages, with a 3 A maximum load current, by sweeping R_1 from 0 to 1.5 kΩ.

From Fig. 5.14, it can be observed how at 225 °C, the regulated output voltage starts to saturate after about a 1 kΩ value for R_1. This is due to the restriction on the maximum output voltage possible which results from using an enhancement NMOS device in the common drain configuration. From the graph it can be concluded that, if the regulator were to be used across temperature, the maximum output voltage will be about 15 V which is obtained by setting R_1 = 1 kΩ. This conclusion can be better understood by calculating the load regulation from the data contained in Fig. 5.14. Fig 5.15 shows the load regulation for different output voltages.

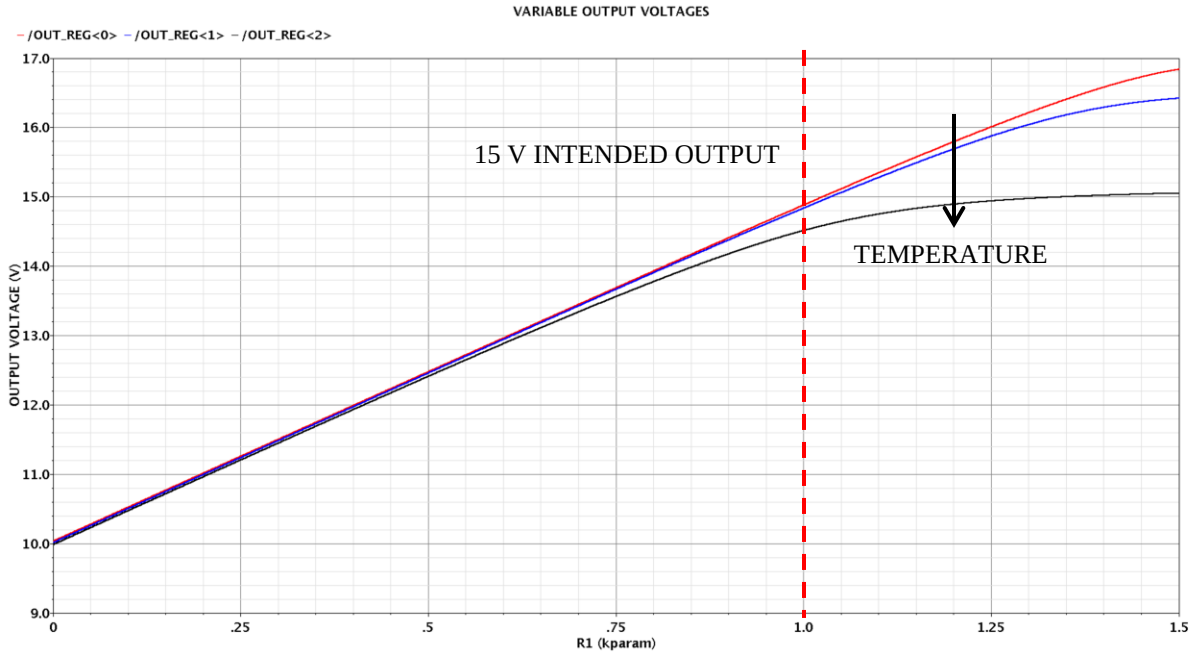


Fig. 5.14 – Different output voltages (y-axis), at a 3 A load current, obtained by increasing the value of R_1 (x-axis) from 0 Ω to 1.5 kΩ at 25 °C, 125 °C and 225 °C.

From Fig. 5.15 it can be seen that the load regulation at 225 °C stays below 2% up to an output voltage of about 14.5 V. After that, the regulation increases drastically making it difficult to find an application where such regulation would be acceptable. The load regulation at different output voltages improves as the maximum load current decreases. Fig. 5.16 shows the

load regulation obtained for different output voltages at maximum load currents of 1 and 2 A. The requirements on output voltage, maximum load current and load regulation will depend on the application and the system specifications.

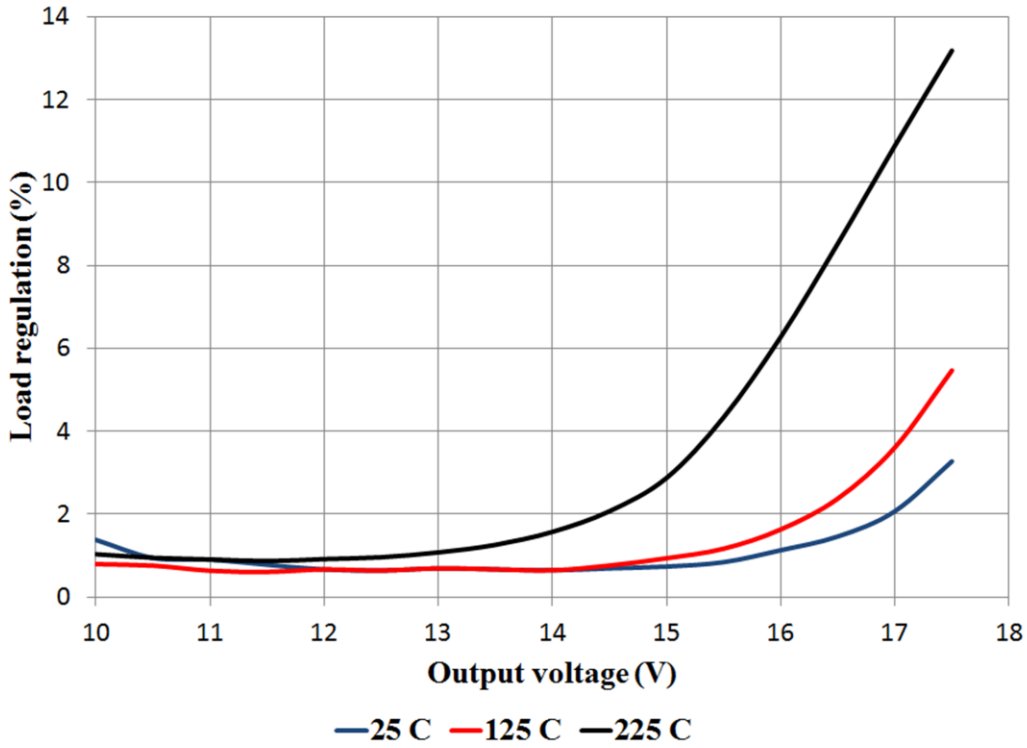


Fig. 5.15 – 3 A load regulation for different output voltages at 25 °C, 125 °C and 225 °C.

As expected, load regulation is improved by decreasing the maximum load current from the regulator (Fig. 5.16). The maximum output voltage from the regulator also increases while still keeping a very low load regulation. For example, at 1 A load current, the maximum output voltage can be set to 17 V and the regulator will still have less than 2% load regulation even at 225 °C. At 2 A load current though, in order to keep the same load regulation, the output voltage can only be a maximum of about 15.5 V. Table 5.19 shows a comparison for a 15 V output voltage for different load currents at 25 °C, 125 °C and 225 °C. The load regulation expressed in mV/A might give the appearance, for a specific temperature, of improving as the load current

increases as opposed to the load regulation expressed as a percentage that worsens. The interpretation of the results is that an increase in the load current by a factor of 2 or 3 does not imply an increase by the same factor in the load regulation in mV/A. The change in the load regulation indicates in fact, a factor of less than 1.

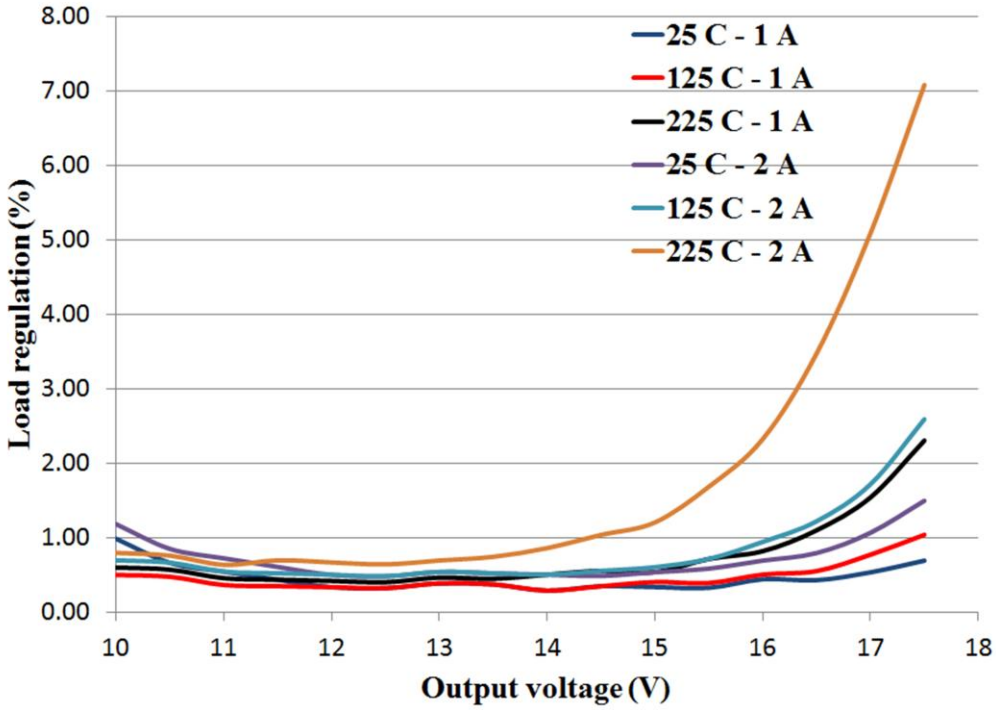


Fig. 5.16 – Load regulation at 1 and 2 A for different output voltages at 25, 125 and 225 °C.

The next important transient parameter for a linear regulator is line regulation. As described in Section 4.2.1, the DC line regulation is the variation in the DC output voltage of the regulator due to the changes in the DC input voltage. Fig. 5.17 shows the simulated line regulation performance of the regulator for a 15 V output voltage and a load current of 3 A. Fig. 5.18 shows the line regulation for a 15 V output voltage and a load current of 1 A and Fig. 5.19 shows the line regulation for a 10 V output and a load current of 3 A.

Table 5.19 – Load Regulation Simulated Results Across Temperature for Different Load Currents.

Temperature (°C)	Load (A)	Load regulation (mV/A)	Load regulation (%)
25	1	50.00	0.33
	2	40.00	0.53
	3	36.67	0.73
125	1	60.00	0.40
	2	45.00	0.60
	3	46.67	0.93
225	1	80.00	0.53
	2	90.00	1.20
	3	143.33	2.87

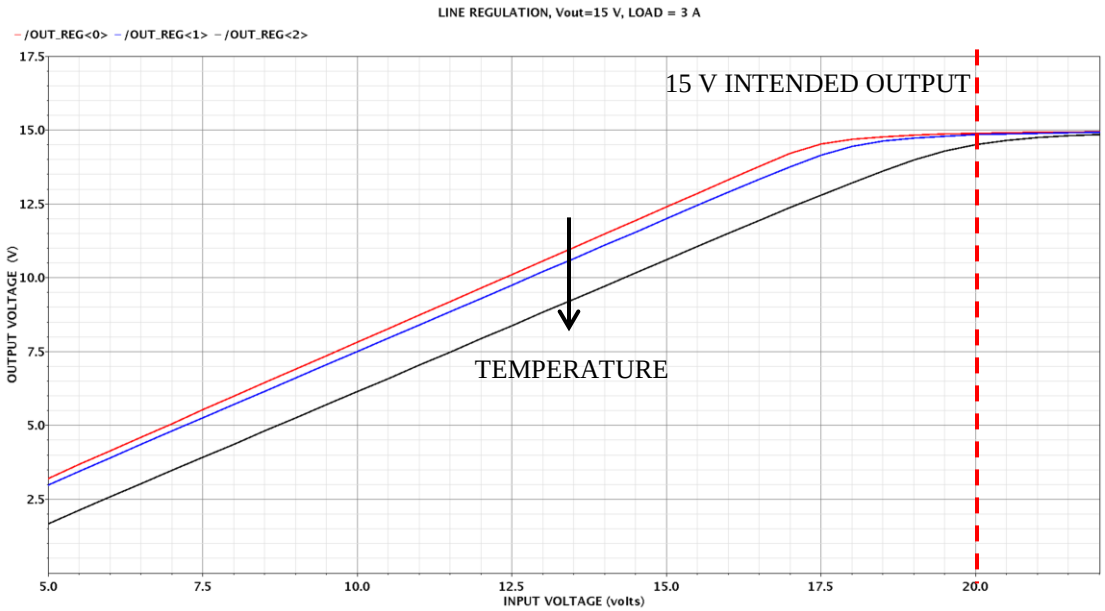


Fig. 5.17 – Regulator output voltage (y-axis) as a function of the input voltage (x-axis) for a 3 A load at 25 °C, 125 °C and 225 °C.

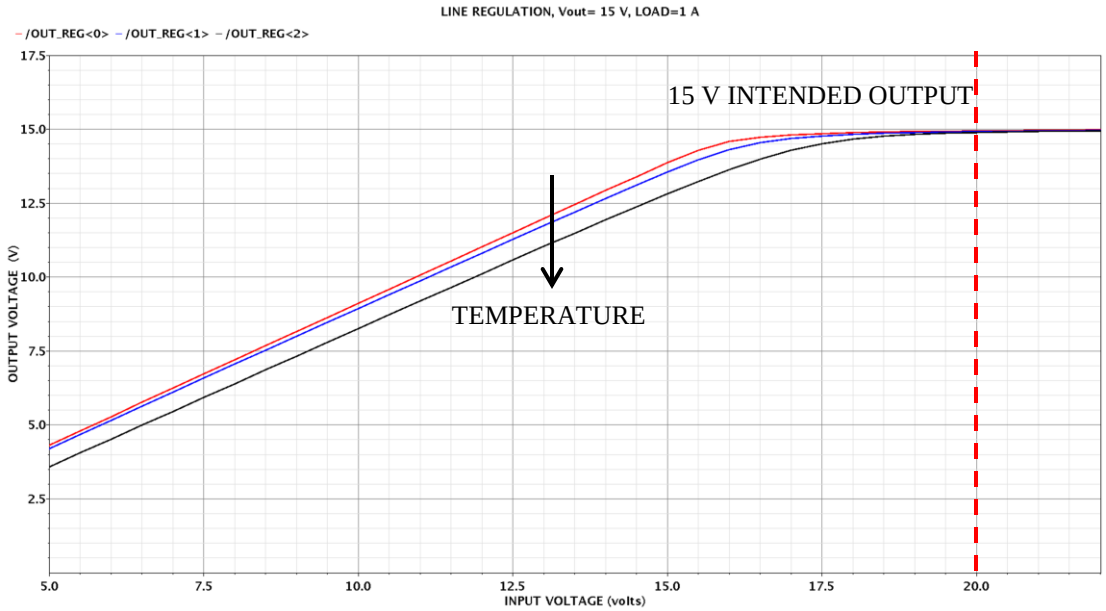


Fig. 5.18 – Regulator output voltage (y-axis) as a function of the input voltage (x-axis) for a 1 A load at 25 °C, 125 °C and 225 °C.

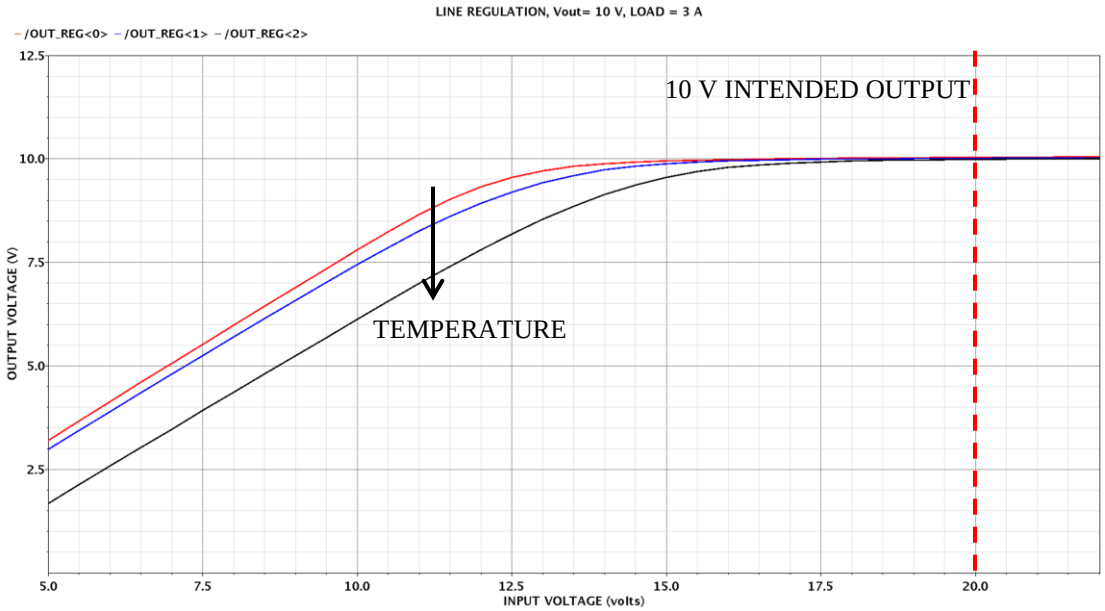


Fig. 5.19 – Regulator output voltage (y-axis) as a function of the input voltage (x-axis) for a 3 A load at 25 °C, 125 °C and 225 °C.

As in the case of load regulation, line regulation improves as the output voltage of the regulator is decreased or the load current is decreased. For the purpose of comparison, the data in

the previous figures will be analyzed for an input voltage of 18-22 V which represents a ±10 % variation from the nominal 20 V. In the case of a 15 V output, at 3 A load current (Fig. 5.17), the output to input voltage relationship for the 18-22 V input voltage range is not as linear as in Figs. 5.18 and 5.19. A linear relationship between the input and output voltages for this case is calculated and presented, along with the other cases, in Table 5.20. From the figures and the data in Table 5.20, it can also be concluded that reducing the output voltage of the regulator has a larger noticeable effect than reducing the load current. For the 10 V output, at 3 A load current, an input voltage starting at about 16 V will probably provide a fairly constant output voltage. However, for the 15 V output, 1 A load current this starting voltage is about 17.5 V.

Table 5.20 – Line Regulation Simulated Results Across Temperature for Different Load Currents and Output Voltages.

Temperature (°C)	Output (V)	Load (A)	Line regulation (mV/V)
25	15	3	57.3
	10	3	8.0
	15	1	23.7
125	15	3	102.3
	10	3	8.5
	15	1	30.3
225	15	3	385.3
	10	3	12.2
	15	1	57.0

A final aspect to explore in the transient response is the effect of the ESL of the output capacitor. This simulation is just to quantify the maximum ESL value (if any) present in C_{OUT}. As discussed in Section 5.4, the current capacitor technologies enable capacitors to have ESL values less than 5 nH which should not be of any concern for this regulator. Fig. 5.20 shows the effect of ESL at 25 °C in the output of the 15 V, 3 A linear regulator. The values used for ESL were 0, 50 and 100 nH. ESL does not seem to affect the DC output voltage of the regulator but it does have an effect during the sudden load current changes. Ringing in the output voltage can be observed as ESL is increased. Needless to say, this is an undesired behavior for any linear regulator. Based on Fig. 5.20 and [58], an ESL=50 nH is the maximum allowable value for C_{OUT} since with this inductance ringing is not as notorious as with ESL=100 nH.

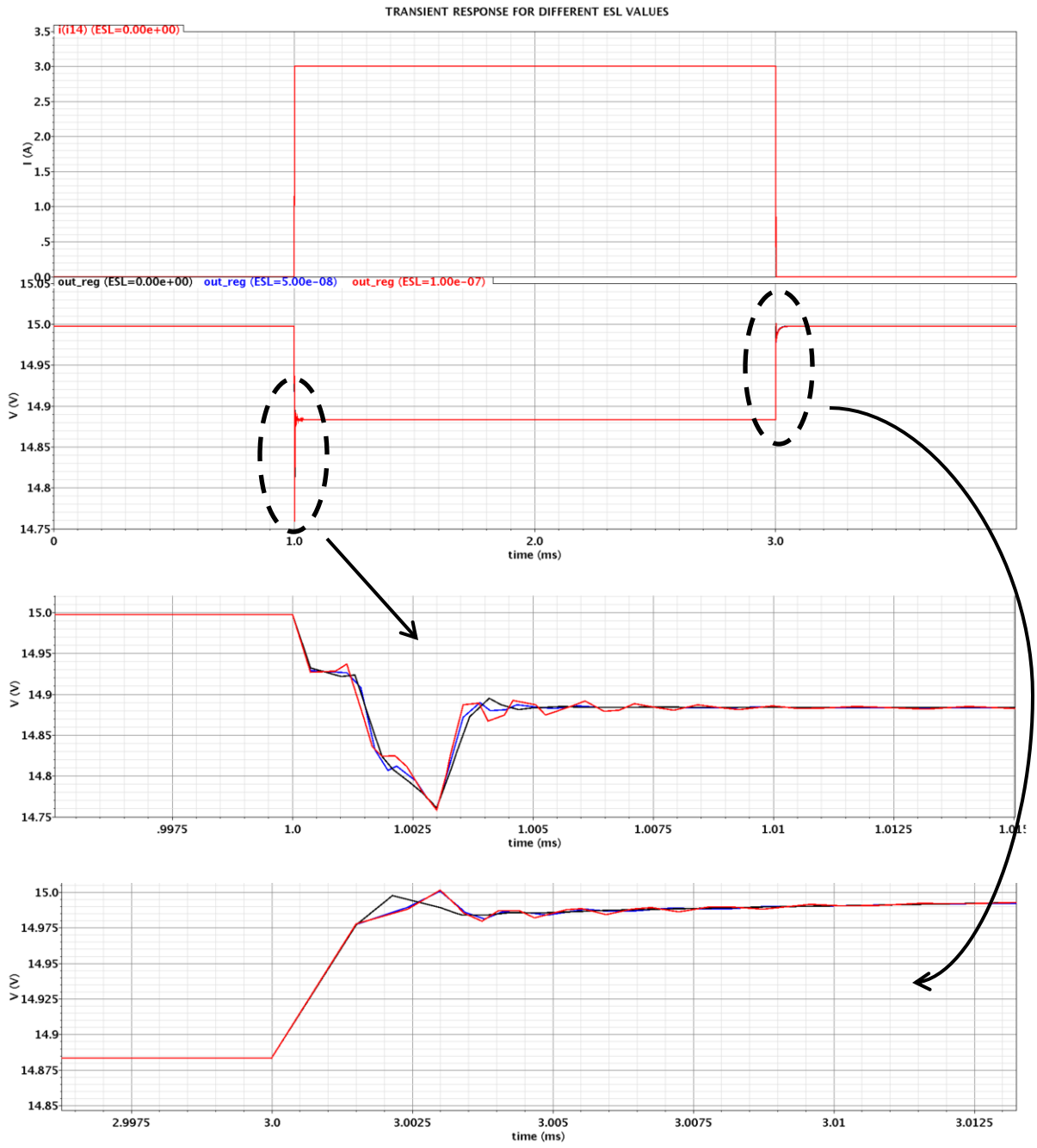


Fig. 5.20 – Transient response (top) at 25 °C of a 15 V output linear regulator to a sudden 3 A load current change using a 10 µF output capacitor with ESL=0 nH (black), 50 nH (blue) and 100 nH (red). The circled areas are enlarged to show the ringing effect of ESL in the output voltage of the regulator.

5.9 Layout

The layout of the linear regulator as it was sent for fabrication is shown in Fig. 5.21. The dimensions are 2460 μm x 1680 μm. A standalone error amplifier was included in the run to measure the output biasing voltages for debugging purposes. The dimensions of the regulator by itself are 1539 μm x 1440 μm without pads. This standalone error amplifier and the linear regulator were placed inside an individual pad ring, isolated from the rest of the circuits in the run. The location of this pad ring inside the entire die sent for fabrication is shown in Fig. 5.22. In the entire die, additional substrate contacts were placed on the top and left side of the linear regulator pad ring to ensure a good ground connection to the substrate close to the output of the regulator.

Due to only one metal layer and one very resistive poly layer, the layout of the circuits was not a trivial matter. In order to avoid crossing over metal with poly, the layout had to be expanded. Even though this technique did not minimize the layout area, it did prove to be effective in reducing the parasitic resistance of the poly overlap connections. These resistances in some cases turned out to be in the range of kΩ. After the initial post-layout simulations, it was decided to completely avoid poly overlap connections since they were creating 1-2 V offsets in the output of the regulator and the error amplifier.

Since the input and output terminals of the regulator will handle up to 3 A of DC current, a total of 8 pads were used for each of them. In addition, thick metal traces were used to connect to these pads based on a specification from Cree that a 5 μm wide metal trace should handle at least 20 mA of DC current. Therefore, at its maximum load, the regulator will provide 3 A of DC current, needing at least 750 μm wide metal traces to handle this amount of current. Since each pad is 120 μm x 120 μm, using 8 pads suffice the metal thickness requirement.

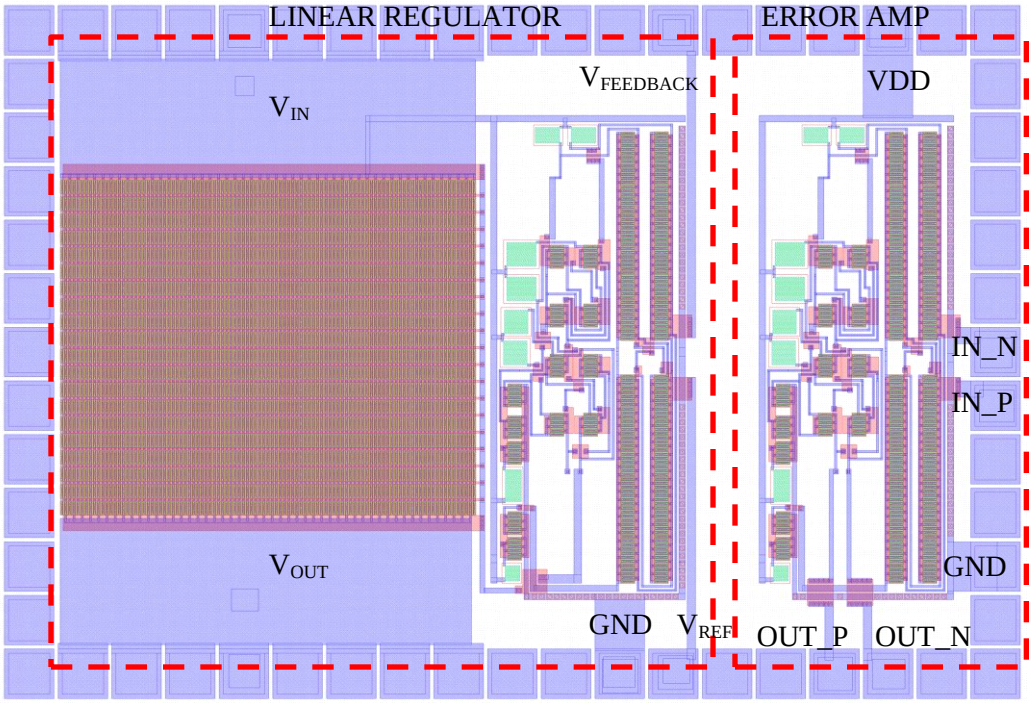


Fig. 5.21 – Layout of the linear regulator and a standalone error amplifier.

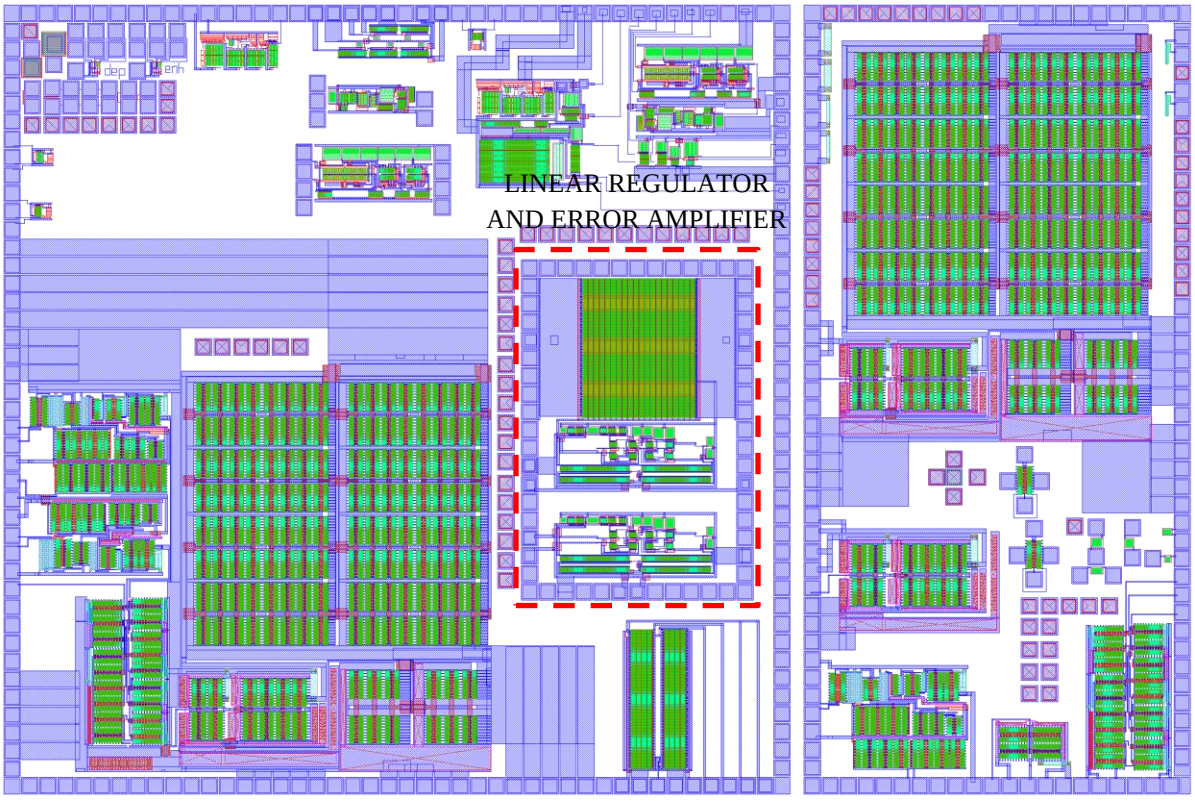


Fig. 5.22 – Layout of the entire 8.7 mm x 5.8 mm SiC die sent for fabrication.

The layout of the pass device also took into consideration the current limitation of the metal traces. The area of the pass device accounts for about 67% of the total area of the linear regulator. The 2000 transistors needed to compose the pass device were arranged in 20 rows, each with 100 transistors. This way, at a maximum load of 3 A, each transistor in the first row (drain), would see a maximum current of 30 mA. This 30 mA will then be distributed across the 20 transistors in each column until the source of the pass device is reached. The ground terminal of the linear regulator in the layout is the ground reference for the error amplifier. Hence, it will never handle the large amounts of load current since the current will flow from the source of the pass device directly into the load.

5.10 Post-layout simulations

The sole purpose of post-layout simulations is to ensure that the final layout of the circuits does not introduce parasitic elements (resistance and capacitance) that will impact their performance. As discussed in the previous section, the layout of the linear regulator was not trivial and it had to be done a few times before the parasitic elements did not affect the performance drastically. This section presents the comparison between the pre- and post-layout simulations of the linear regulator. The post-layout simulations include the connection to the pads providing the closest available resemblance of how the circuit will perform after fabrication. Satisfactory frequency and transient (load) responses at the corner temperatures should validate the final layout. Fig. 5.23 shows the frequency response of the regulator at 25 °C for the no load and full load conditions. Fig. 5.24 shows the same frequency response at 225 °C. Fig. 5.25 shows the load regulation performance at 25 °C and 225 °C and Fig. 5.26 shows an enlarged area of the undershoot and overshoot voltages for both temperatures. Tables 5.21 and 5.22 summarize the results for the frequency and transient responses, respectively.

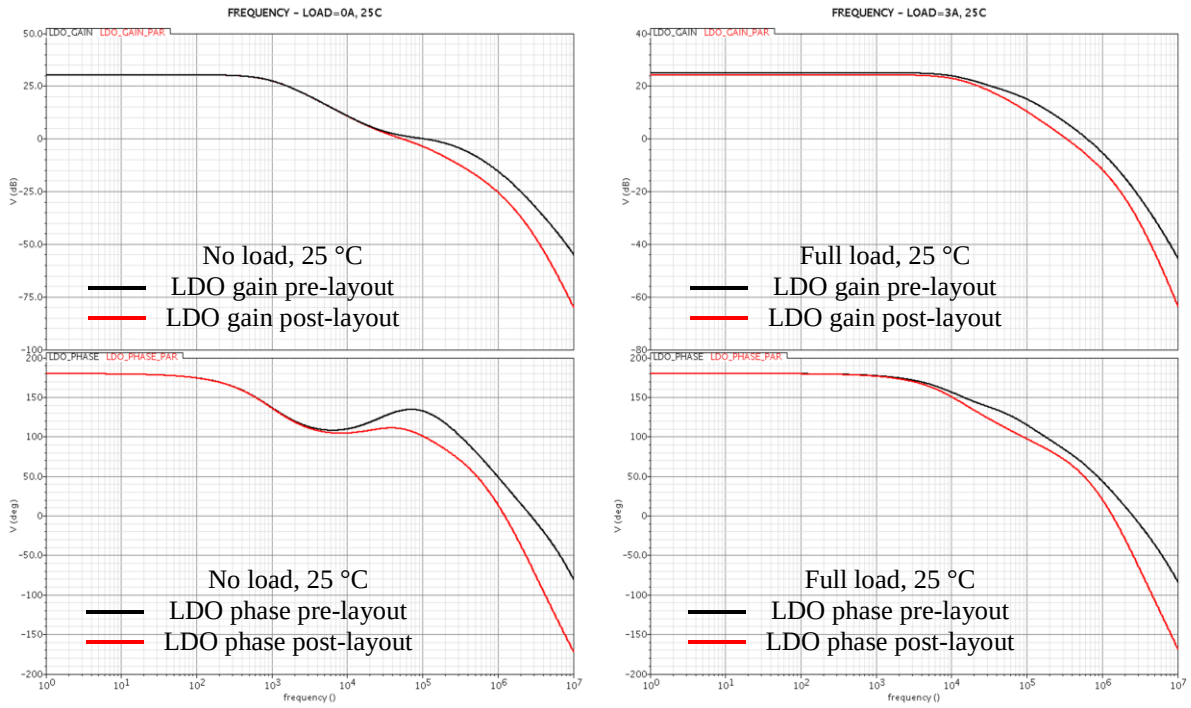


Fig. 5.23 – Frequency response of the regulator at 25 °C for no load (left) and full load (right) condition. A displacement of the third pole can be observed.

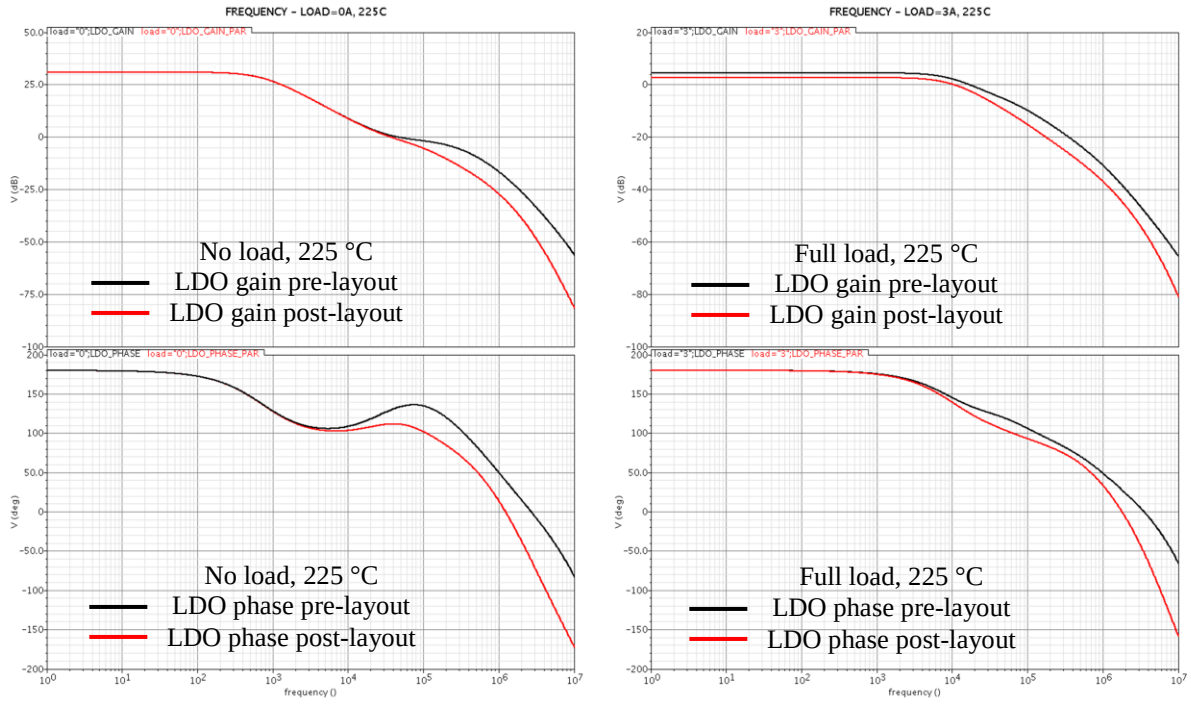


Fig. 5.24 – Frequency response of the regulator at 225 °C for no load (left) and full load (right) condition.

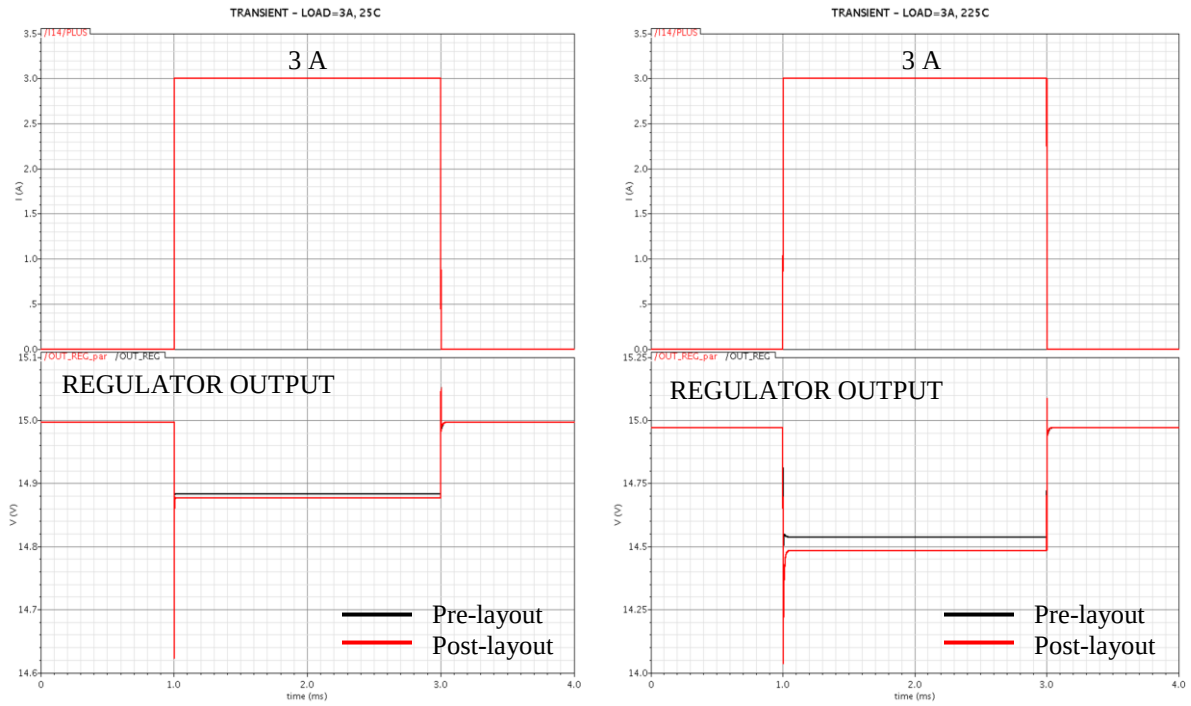


Fig. 5.25 – Transient response to a 3 A load current change at 25 °C (left) and 225 °C (right). The red and black curves are the post and pre layout simulations, respectively.

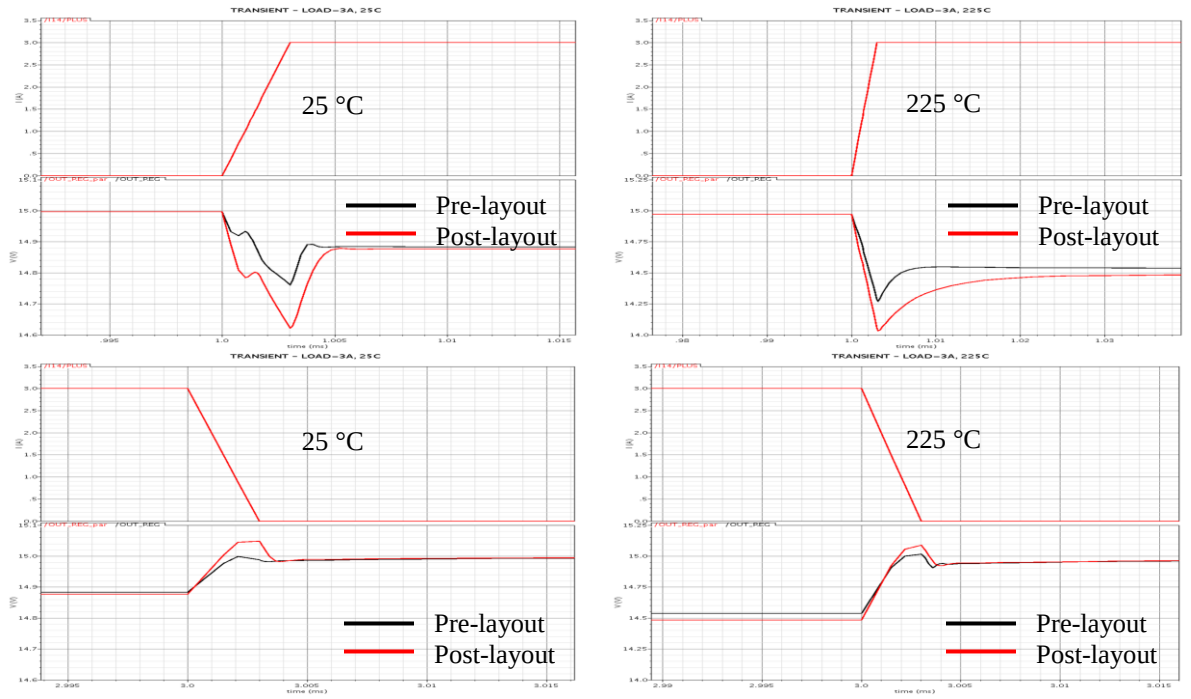


Fig. 5.26 – Undershoot (top) and overshoot (bottom) regions for the 3 A load current change in Fig. 5.25. The red and black curves are the post and pre layout simulations respectively.

Table 5.21 – Comparison Between the Pre and Post Layout Simulation Results for the Frequency Response of the Regulator at the Corner Temperatures.

Temperature (°C)	Load (A)	DC gain (dB)	UGF (kHz)	Phase margin (deg)
25	0	30.42(30.42)	102(53)	132(110)
	3	25.12(24.32)	626(336)	62(69)
225	0	31.00(31.00)	46(37)	132(112)
	3	4.58(2.74)	17(11)	135(138)

Pre-layout/(Post-layout)

Table 5.22 – Comparison Between the Pre and Post Layout Simulation Results for the Transient Response of the Regulator at the Corner Temperatures.

Temperature (°C)	Load (A)	Output (V)	Load regulation (%)	Undershoot (mV)	Overshoot (mV)
25	0	14.99(14.99)	0.73(0.80)	230(370)	130(180)
	3	14.88(14.87)			
225	0	14.97(14.97)	2.87(3.27)	700(930)	480(610)
	3	14.54(14.48)			

Pre-layout(Post-layout)

Looking at Figs. 5.23 and 5.24 and Table 5.21, the results for the frequency response before and after layout are very similar. There is a very small minimal difference in the DC gain of the responses. The largest difference occurs at 225 °C and that is due to the already deteriorated behavior of the error amplifier trying to keep up with the change in load current. This behavior is worsened by the parasitic elements as a result of the layout. The phase margin

stays always larger than 60 degrees, ensuring stability of the regulator. The decrease in UGF is related to the displacement of the second pole (C_{pass} and $R_{OUT,amp}$) observed in Figs. 5.23 and 5.24. This is due to the parasitic resistance of the routing layers that add up to $R_{OUT,amp}$ moving the pole slightly closer to the zero. The zero does not move under any condition since it is formed by ESR and C_{OUT}, both of which are external and not dependent on the layout of the regulator. The dominant pole (C_{OUT} and $R_{OUT,pass}$) does not seem to move mainly also because C_{OUT} is external.

The post-layout transient response does not show enough of a change in the load regulation to create any concern as well. The worst DC output voltage variation due to the layout is less than 0.5%. The increase in undershoot and overshoot voltages was expected due to the parasitic resistance associated with the routing layers that ends up in series with the ESR of the output capacitor.

Overall, the post-layout simulation results are satisfactory. As mentioned before, this was achieved by a constant iterative process in the layouts of the pass device and the error amplifier. The results in Tables 5.21 and 5.22 indicate the present of parasitic elements but these do not compromise the performance of the linear regulator. Such parasitic elements were expected due to the lack of more than 1 metal layer for routing and a very resistive poly layer.

CHAPTER 6: SiC VOLTAGE REGULATOR TESTING AND CHARACTERIZATION

After the regulator was fabricated, it was packaged in a Kyocera 100-pin quad package. Fig. 6.1, 6.2 and 6.3 show, respectively, a picture of the fabricated die, the packaged die and its corresponding bonding diagram. Table 6.1 shows the respective pin names and numbers.

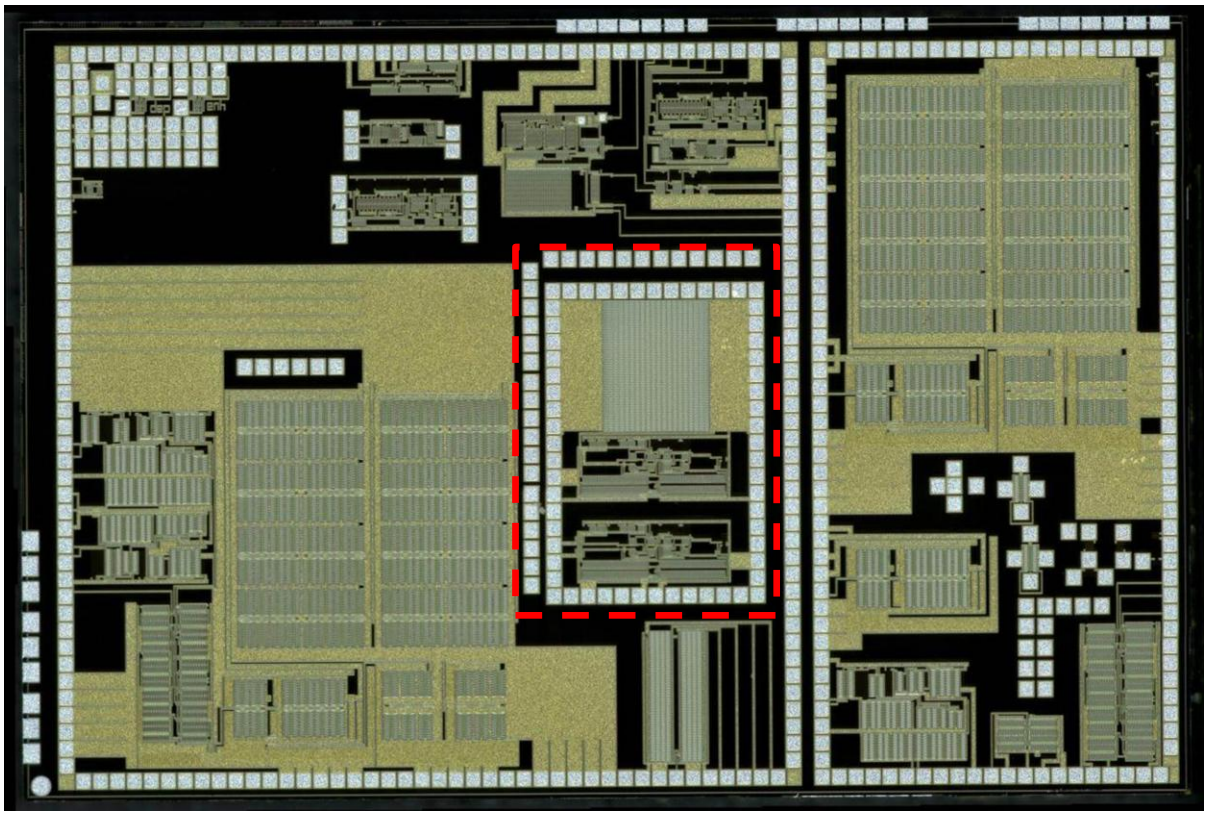


Fig. 6.1 – Picture of the 8.7 mm x 5.8 mm fabricated die indicating the location of the linear regulator and the standalone error amplifier.

After the die were received, a quick measurement on some test devices in the die was performed. This was done in order to validate the accuracy of the models available for this process and the results were quite satisfactory for the enhancement devices. The depletion devices showed a leakage current of about 20-30 μA at small V_{SB} values, but it disappeared as V_{SB} was increased. The decision to not use depletion devices in the error amplifier and the fact

that the pass device (depletion type) has a constant V_{SB} = 15 V, make this leakage effect irrelevant to the regulator performance. However, it should be pointed out that the models actually used in the design process before the linear regulator was sent for fabrication were not the same models used in this validation process. The reason for this is that before the model development process was complete, the modeling engineer was compelled to deliver a working version of the models to the designers to speed up the design process. After tapeout, the modeling engineer continued working on improving the models and it is that final version of the models that is used to validate them by comparing them to measured data from test structures in the die. Therefore, since the final models are more accurate than the models used for tapeout, some discrepancy between the measured and simulated data should already be expected. Fig. 6.4, 6.5, 6.6 and 6.7 show the comparison between the models used for tapeout and the final version for the input and output characteristics of the enhancement and depletion devices, respectively.

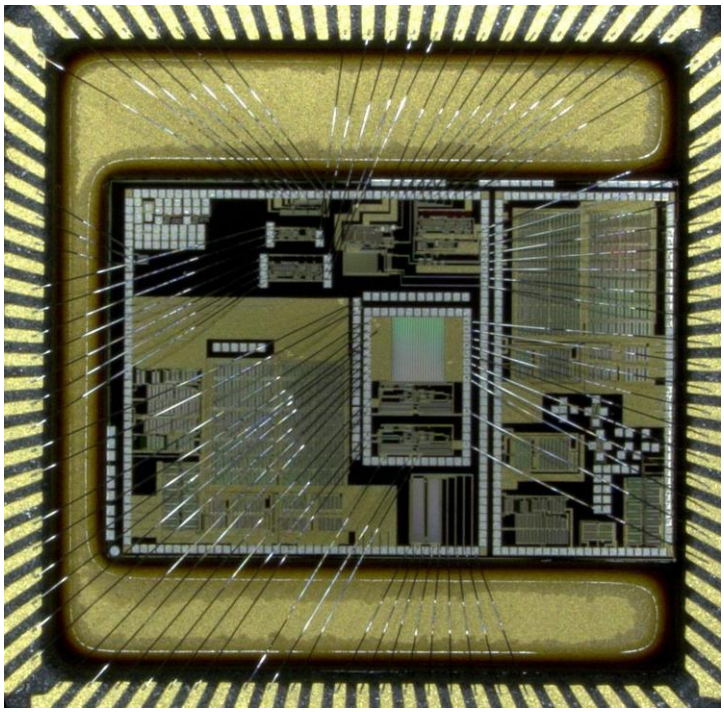


Fig. 6.2 – Picture of the die with wire bonds inside the 100 pin Kyocera package.

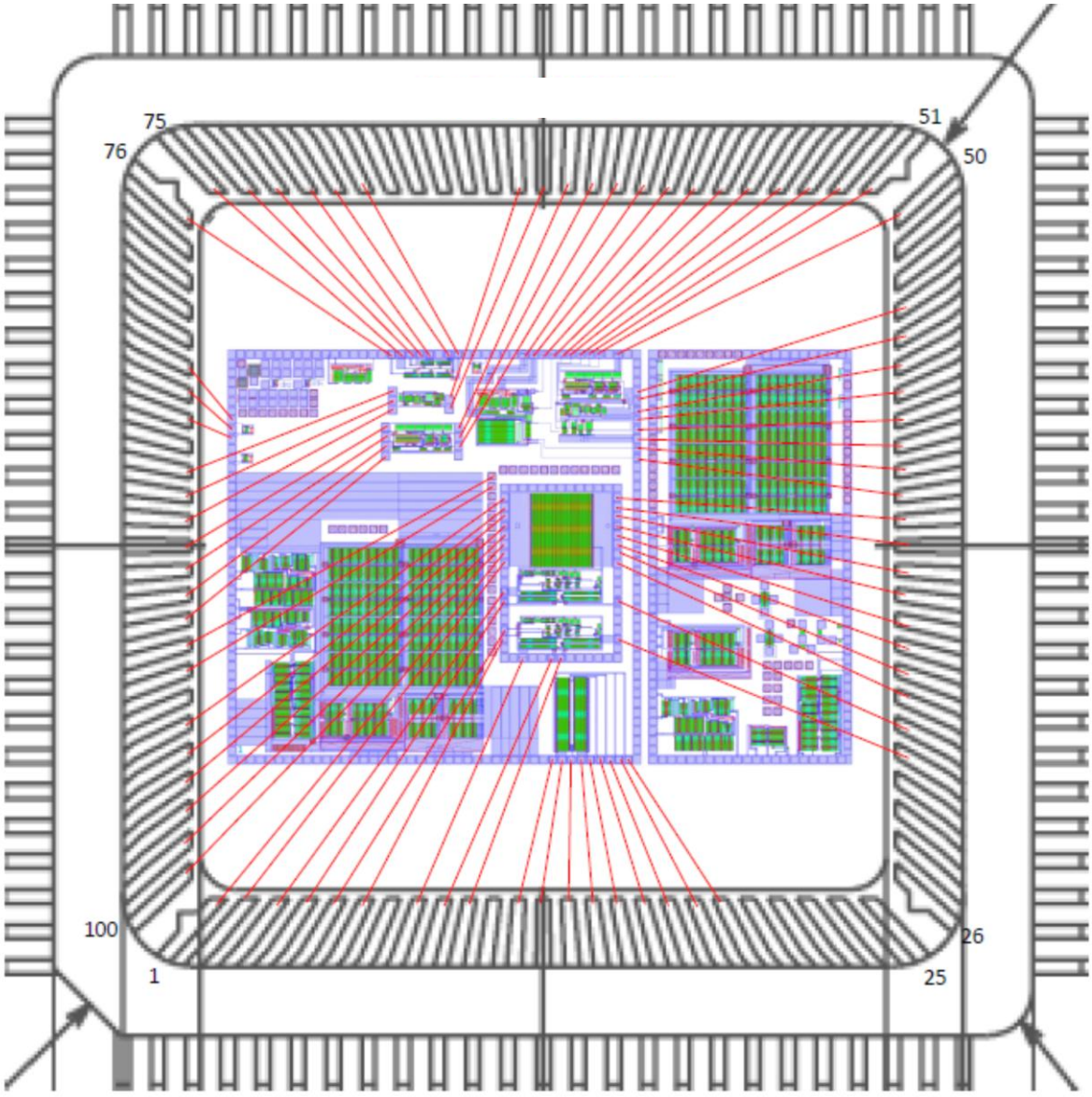


Fig. 6.3 – Bonding diagram for the linear regulator and the standalone error amplifier.

Table 6.1 – Pin Names and Numbers for the Linear Regulator Bonding Diagram.

LINEAR REGULATOR		ERROR AMPLIFIER	
Pin number	**Pin name**	**Pin number**	**Pin name**
1-2, 95-100	VOUT	5	OUT_P
3	GND_REG	6	OUT_N
4	VREF_REG	8	GND
31	VFEEDBACK_REG	9	IN_P
32-39	VDD_REG	10	IN_N
		30	VDD

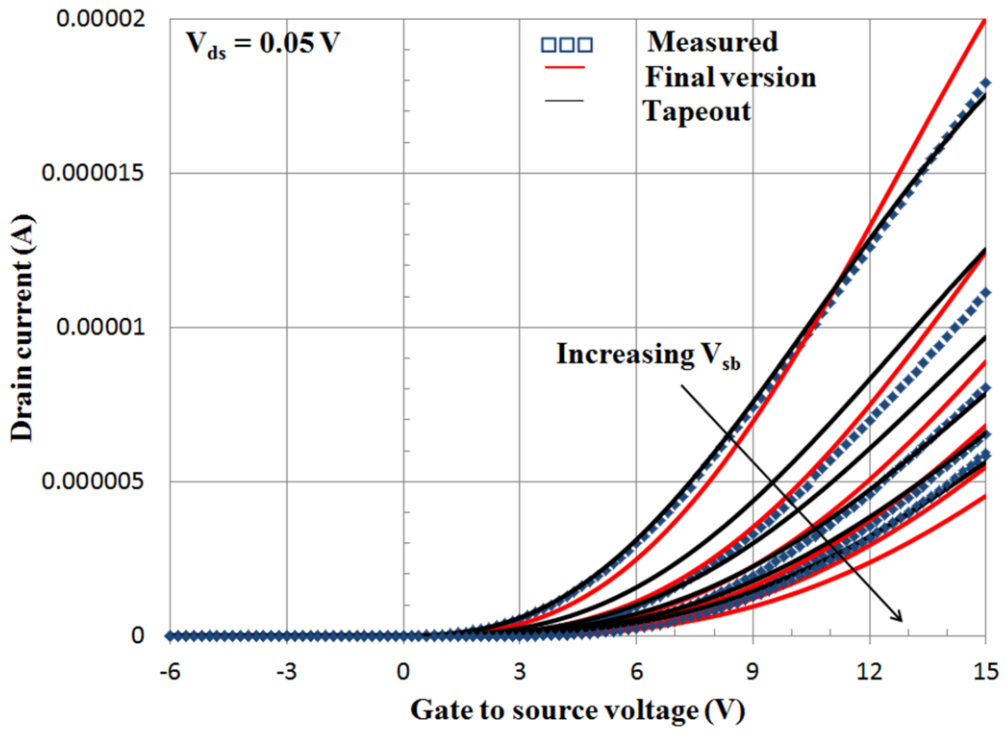


Fig. 6.4 – Input characteristics model comparison for a 32 µm x 2 µm enhancement device.

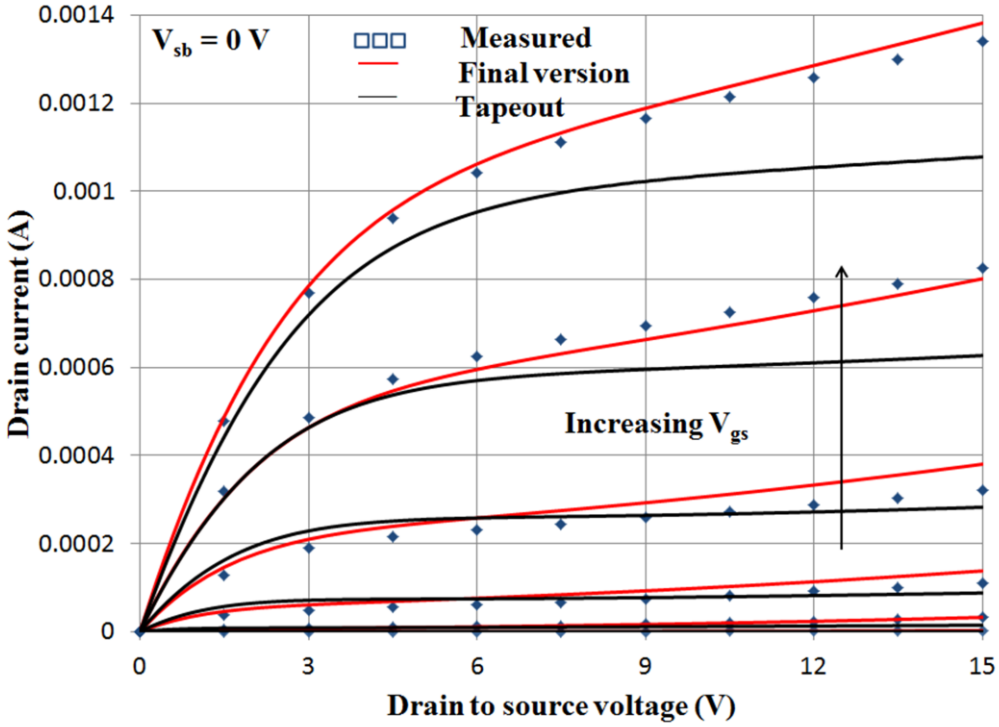


Fig. 6.5 – Output characteristics model comparison for a 32 µm x 2 µm enhancement device.

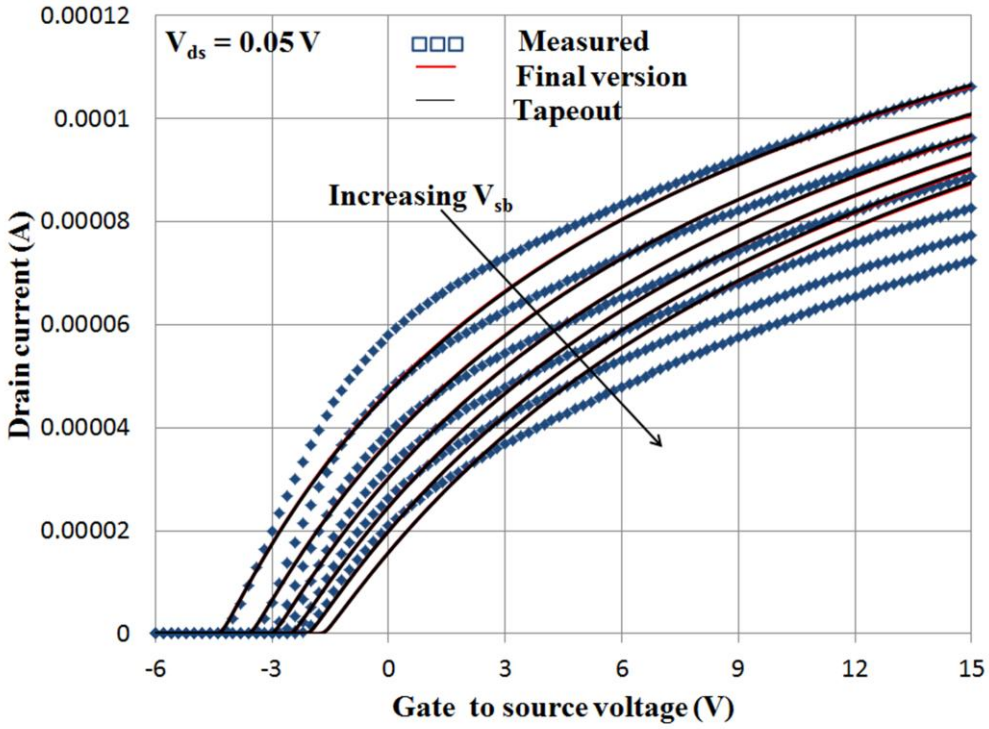


Fig. 6.6 – Input characteristics model comparison for a 32 µm x 2 µm depletion device.

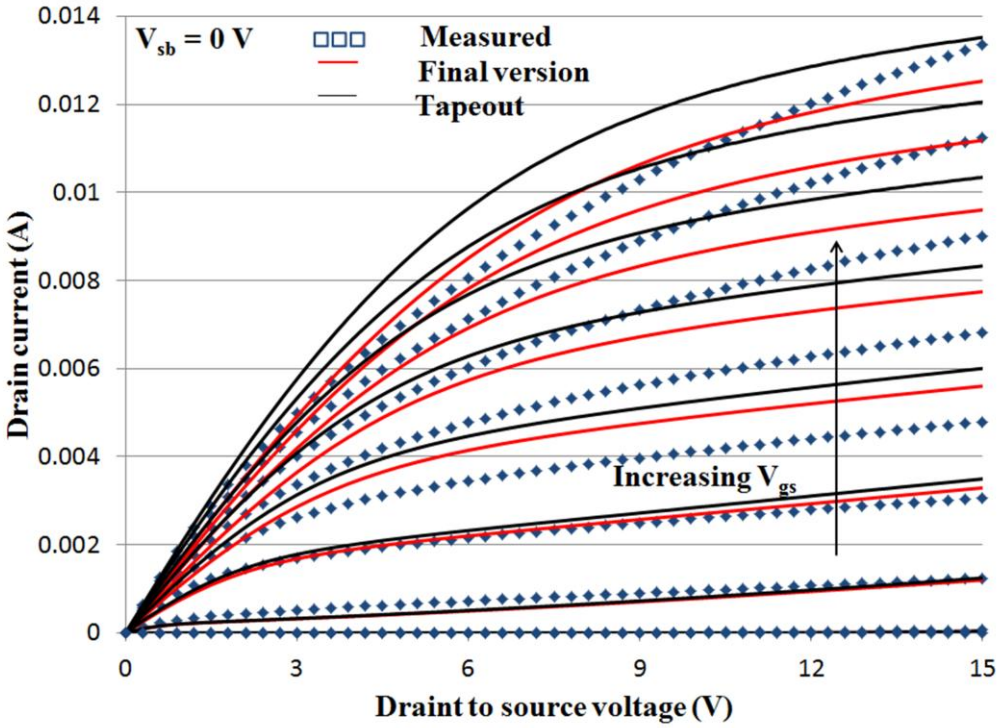


Fig. 6.7 – Output characteristics model comparison for a 32 µm x 2 µm depletion device.

From the previous figures it can be seen that the models used for tapeout (black curves) and the final version (red curves) are actually different. In general, simulations with the final version of the models match the measured data better. Only the input characteristics of the depletion MOSFET are the same for both versions of the models. As expected, the discrepancy between the measured and modeled characteristics will propagate into all the stages of the design and will create an unavoidable variation between the collected and the simulated data.

After the linear regulator was packaged, Direct Bonded Copper (DBC) boards were fabricated. DBC boards are able to withstand very high temperatures and are therefore suitable for this specific application. Fig. 6.8 shows the packaged die mounted on the DBC board fabricated for the linear regulator. A Rogers 4350 PCB rated up to 288 °C [81] was also used to mount a different packaged die. Fig. 6.9 shows the packaged die mounted on the Rogers 4350

board. In addition, a simple 1 layer Printed Circuit Board (PCB) was sent for fabrication to be used as a daughter board. This will allow using surface mount parts for the external feedback and compensation networks as well as the load used to test the linear regulator, reducing parasitic elements associated with bread boards and through-hole components. Fig. 6.10 shows a picture of the PCB used for testing.

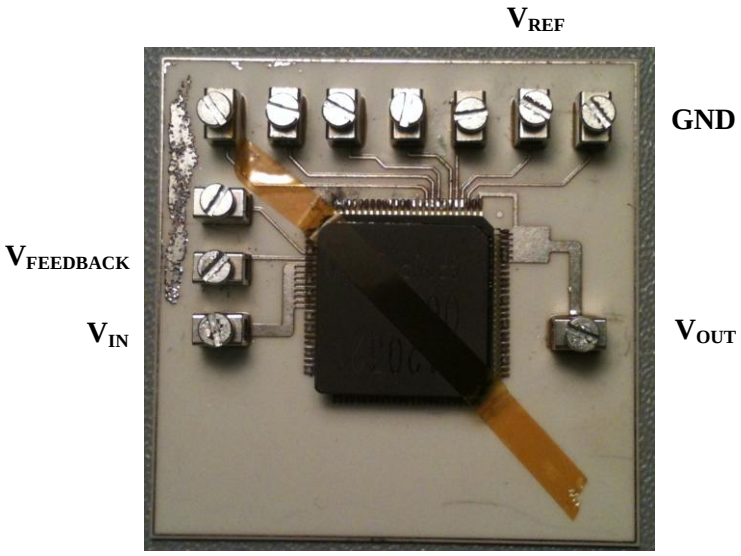


Fig. 6.8 – Packaged die mounted on DBC board used for testing.

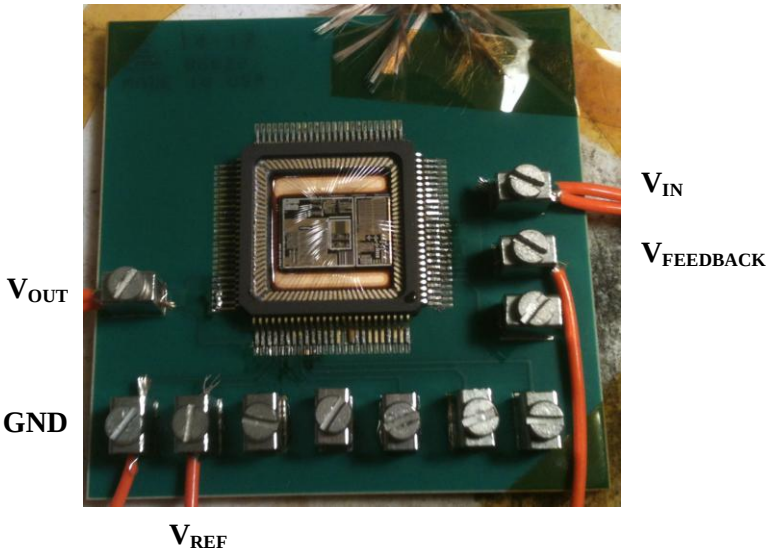


Fig. 6.9 – Packaged die mounted on Rogers 4350 PCB used for testing.

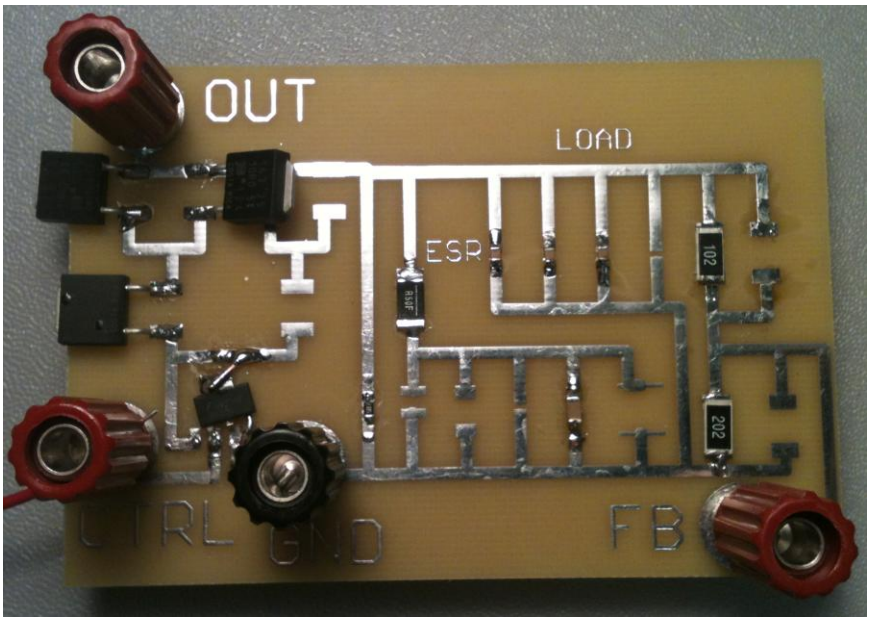


Fig. 6.10 – Daughter board used for testing.

There are large amounts of data collected from three different die for this linear regulator. This chapter however, intends to consolidate this data and present the most relevant results that demonstrate the full functionality of the circuit under different conditions. All the data presented in this chapter is from the DC response of the regulator since the frequency response cannot be physically tested. Simulation data is the only source of information for that performance. This is mainly because in a linear regulator, the negative input of the error amplifier is connected to the output through one of the resistors of the feedback network and hence, any applied signal would be fed directly to the output. This would not allow performing an AC analysis, like the one shown in Fig. 4.5, where the feedback loop needs to be broken.

DC testing of the linear regulator focused on its line and load regulation, and the transient response. These characteristics were evaluated primarily for the intended 15 V output voltage across temperature. However, in order to demonstrate functionality of the regulator at different

output voltages, some line and load regulation data was also collected for output voltages of 10 and 12.5 V. The 10, 12.5 and 15 V output voltages were obtained using values of 0, 0.5 kΩ and 1 kΩ, respectively, for R_1 in the feedback network. In addition, ceramic and tantalum types of output capacitors were used for each test in order to observe, if any, differences in the performance of the regulator. The differences were almost negligible and therefore, only data using a ceramic output capacitor with a series ESR is included.

The initial data obtained from the transient response test at 1 and 2 A showed some small signs of oscillation in the output of the regulator. While these signs of oscillation were still not critical (four rings or less), more detailed and extensive simulation at these load conditions indicated that reducing the value of ESR from 0.5 to 0.2 Ω guaranteed a larger phase margin across the entire load range (0 to 3 A). As discussed in the previous chapters, a phase margin larger than 60 degrees ensures frequency stability of a linear regulator. Therefore, a 10 μF ceramic capacitor in series with a 0.2 Ω resistor was used as compensation network to collect all the DC data presented in this chapter.

Another important fact concluded from the initial transient response of the regulator is that the overshoot and undershoot voltages are about ±10% of the output when the I_{LOAD} = 3 A at 25 °C. This means for example, that for V_{OUT} = 15 V, the overshoot and undershoot peak voltages reach about 13.5 and 16.5 V, respectively. Needless to say, this behavior is undesired since it could cause unexpected behavior in the circuits being powered by the linear regulator. In addition, if these circuits have some kind of protection circuitry, such as an UVLO, it could turn the circuits off. The fact that these large overshoot and undershoot voltages were observed at room temperature indicates that they would simply aggravate as temperature is increased. The explanation for this behavior is mainly due to the parasitic inductances associated with the test

setup and the process itself. **Due to this situation, it was decided to focus the testing of the regulator with load currents up to 2 A (some data is still presented for I_{LOAD} = 3 A). The capacitive load of the regulator was set to 0.3 µF as discussed in the design chapter.**

Due to the lack of any kind of ESD protection in the die, handling of the chips had to be done with extreme care and with proper grounding of the test bench and the person handling the chips.

6.1 High temperature testing

The high temperature testing was performed using a hot plate and the temperature was monitored using a thermocouple attached to the board. As expected, there was heat loss due to the entire test setup and therefore, a thermal camera was used to determine the actual junction temperature of the die under no load conditions. In addition, to ensure that the thermal camera readings were also accurate, the exposed die was sprayed with a painting of known emissivity. This allowed finding a reliable correlation between the thermocouple reading, the hot plate reading and the actual junction temperature of the die. Fig. 6.11 and 6.12 shows the thermal camera pictures at 125 and 225 °C, respectively. Table 6.2 shows the temperature readings from the hot plate, the thermocouple and the thermal camera.

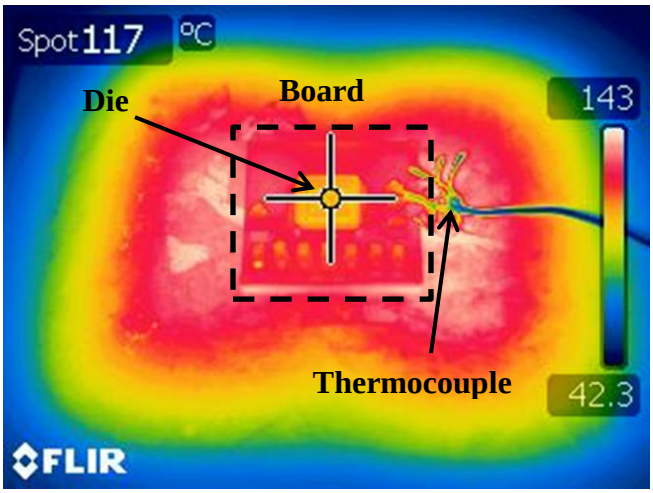


Fig. 6.11 – Thermal camera picture of Rogers 4350 PCB for testing at 125 °C

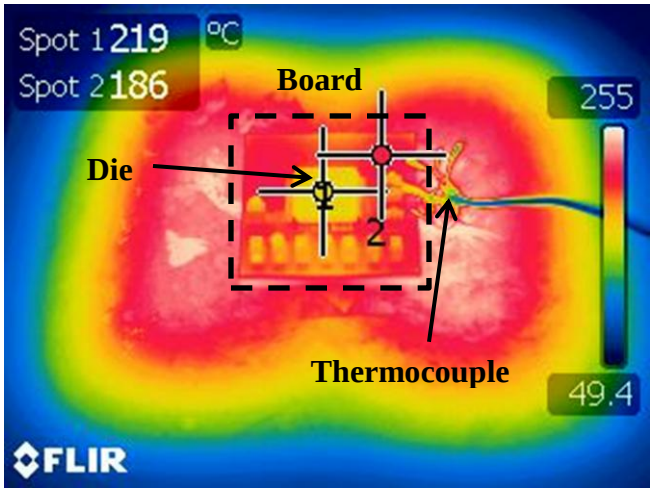


Fig. 6.12 – Thermal camera picture of Rogers 4350 PCB for testing at 225 °C

Table 6.2 - Temperature readings comparison

Hot plate (°C)	Thermocouple (°C)	Thermal camera (°C)
150	120	117
260	225	219

From Table 6.2, it can be seen that the thermocouple and thermal camera readings are very close to the actual desired testing temperatures (125 and 225 °C). However, since the load currents for this regulator are in the order of 1, 2 and 3 A, their effect on the temperature of the die is not negligible and it is a factor that must be taken into account when testing over temperature. Fig. 6.13 and 6.14 show the thermal camera pictures at 225 °C (based on Table 6.2) for 1 and 2 A of load current, respectively.

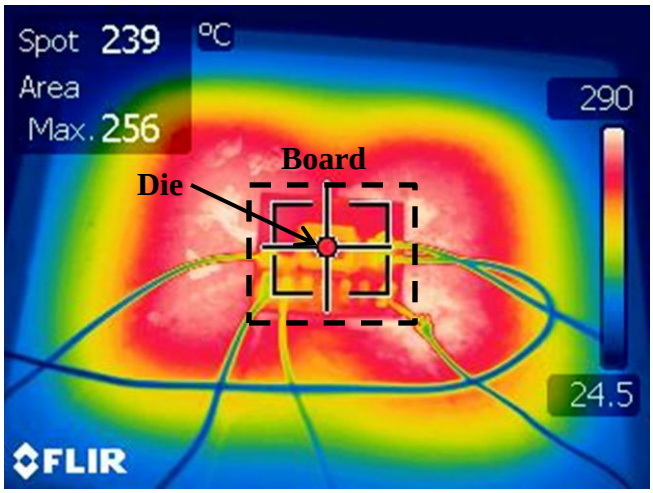


Fig. 6.13 – Thermal camera picture of Rogers 4350 PCB at 225 °C at 1 A of load current

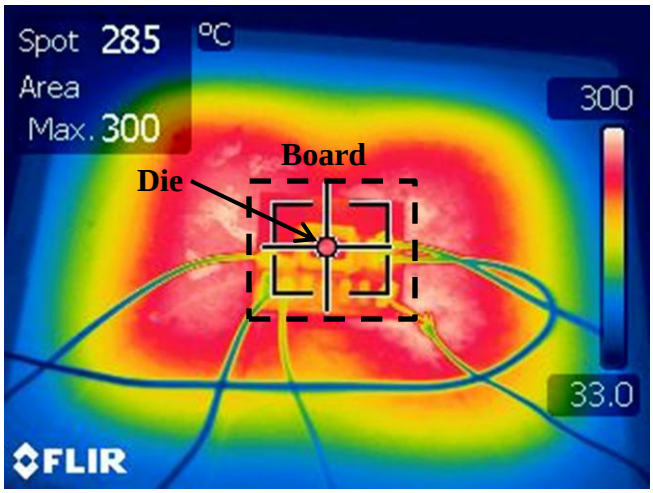


Fig. 6.14 – Thermal camera picture of Rogers 4350 PCB at 225 °C at 2 A of load current

As expected, the temperature under large load currents increases drastically from the desired testing temperature. At 2 A, the change in temperature is about 60 °C from the claimed temperature of operation. Therefore, testing under these conditions was performed for very short periods of time and allowing time in between the tests to avoid overheating the die.

6.2 Load regulation

The load regulation test consisted of measuring the output voltage of the regulator for different load currents across temperature. For this purpose, the daughter board and some external power resistors were used as resistive loads to obtain the different discrete data points. Fig. 6.15 shows the load regulation measured data for the three different output voltages across temperature. Table 6.3 shows a comparison between measured and simulated load regulation percentage at 225 °C (worst case condition). This data corroborates the simulated data by indicating an improvement in load regulation at lower output voltages.

The measured data differs slightly from the simulated data. However, as it was extensively discussed in this dissertation, differences between the simulated and measured data were expected due to the sensitivity of the process and the version of the models used to design the regulator. The packaging of the die and wire connection of the circuit are also expected to add some discrepancy as well.

Even with the unaccounted parasitic element from the test setup of the process itself, load regulation is still less than 4.5% under the worst case condition. It is up to the systems designer and the intended application to determine the acceptable load regulation for the system and limit the maximum load current accordingly.

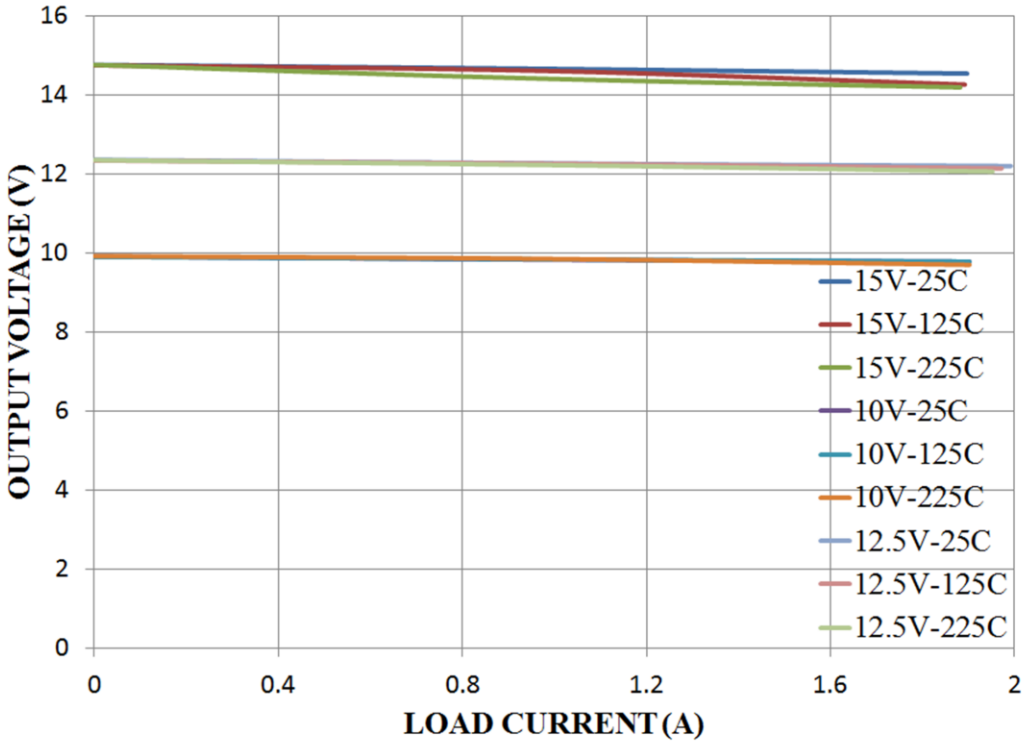


Fig. 6.15 – Load regulation for a 10, 12.5 and 15 V output voltage at 25, 125 and 225 °C.

Table 6.3 – Load Regulation Percentage Measured Data at 225 °C.

		Measured		Simulated	
Output (V)	**Load (A)**	**V_{OUT} (V)**	**Load reg (%)**	**V_{OUT} (V)**	**Load reg (%)**
10	0	9.92	--	10.09	--
	1	9.85	0.71	10.03	0.59
	2	9.70	2.22	10.01	0.79
12.5	0	12.35	--	12.53	--
	1	12.21	1.13	12.48	0.39
	2	12.06	2.35	12.45	0.64
15	0	14.76	--	14.97	--
	1	14.41	2.37	14.89	0.53
	2	14.19	3.86	14.79	1.20

6.3 Line regulation

The line regulation test consisted of measuring the output voltage of the regulator for different DC input voltages. The region of most interest is for a ±10% variation from the nominal input 20 V supply. Fig. 6.16 shows the line regulation measured data for the three different output voltages at 25 °C under no load, 1 and 2 A conditions.

A quantified value of the DC line regulation for a ±10% variation in the input voltage is presented in Table 6.4. Similar to load regulation, line regulation improves at lower output voltages. The DC line regulation for V_{OUT} = 15 V across temperature under different load

conditions is shown in Fig. 6.17. Table 6.5 shows a comparison between measured and simulated line regulation data at 225 °C for V_{OUT} = 15 V (worst case condition).

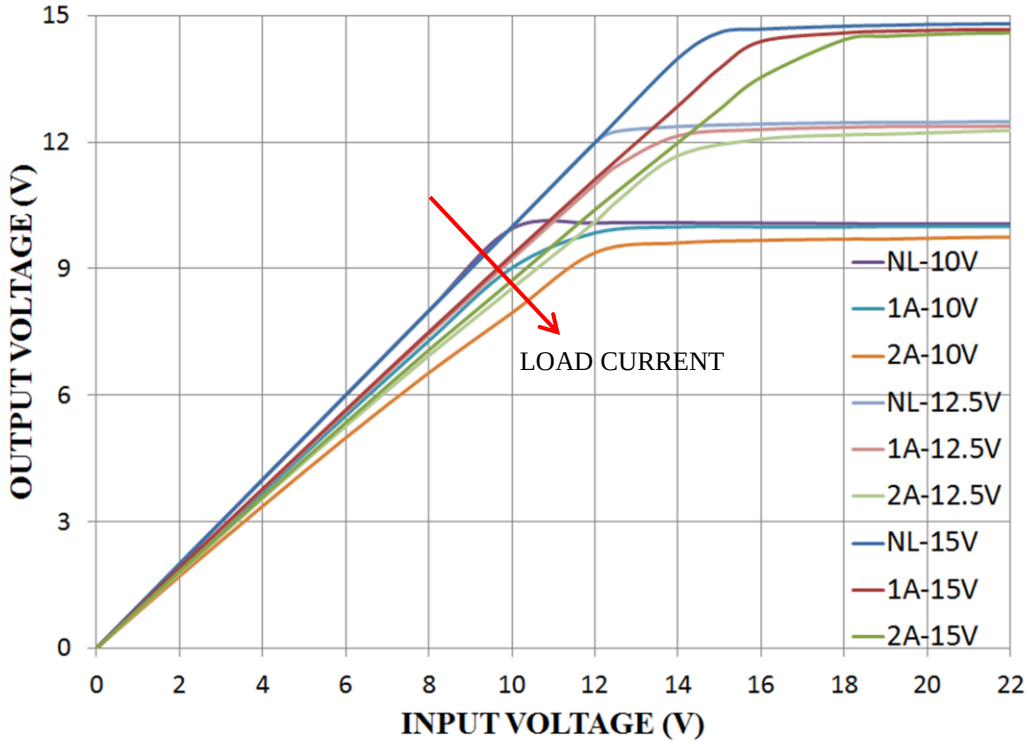


Fig. 6.16 – Line regulation at 25 °C for different output voltages under different load conditions.

Table 6.4 – DC Line Regulation at 25 °C for Different Output Voltages Under Different Load Conditions.

V_{OUT} (V)	Load (A)	Line regulation (mV/V)
10	0	0
	1	2
	2	14
12.5	0	5
	1	6
	2	28
15	0	15
	1	20
	2	39

Table 6.5 – DC Line Regulation for V_{OUT} = 15 V at 225 °C for Different Load Currents.

I_{LOAD} (A)	Measured line reg. (mV/V)	Simulated line reg. (mV/V)
0	31	20
1	112	59
2	192	168

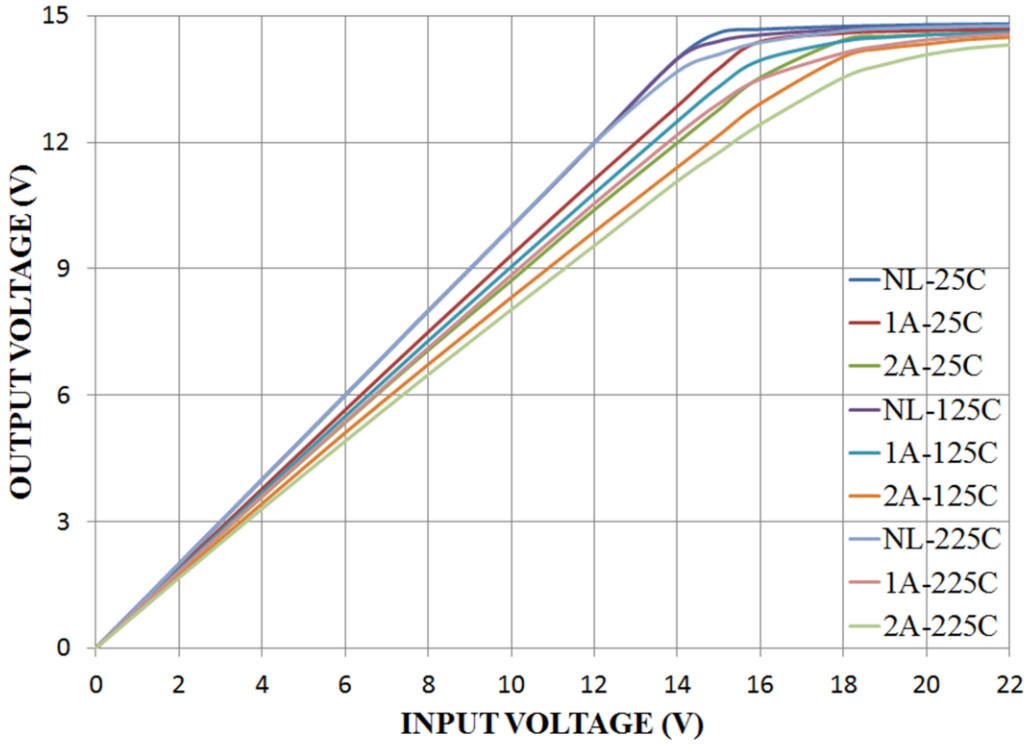


Fig. 6.17 – Line regulation for V_{OUT} = 15 V across temperature under different load conditions.

The trend in Tables 6.4 and 6.5 is the same as in the load regulation data, that is, line regulation improves as the output voltage is decreased or as the load current is decreased for a specific output voltage. From the line regulation test, it can be concluded that the line regulation under worst case condition is 192 mV/V.

6.4 Transient response

The transient response test consisted of applying sudden load current steps to the regulator like the one shown in Fig. 4.2. For this purpose, the daughter board had series and parallel arrangements of 25 W power resistors in series with a Fairchild Semiconductor MOSFET, N-channel 60 V, 4 A power transistor with a maximum R_{DSON} = 0.1 Ω [82]. The

source of the power MOSFET was connected to ground. The gate of the power MOSFET was driven by a 0-5 V pulse signal generated by an Agilent 81101A, 50 MHz waveform generator. The pulse signal width was set to 1 second so that the transient response would not be the response to a spike load current but rather to a continuous event. The response was captured by an Agilent 54622D, 100 MHz mixed-signal oscilloscope. The rise and fall times of the pulse signal were set to 1, 2 and 3 μs for the respective 1, 2 and 3 A transient load current tests in order to match the 1 A/μs current rate change used in simulations. Due to the time scale needed to observe the change in the output voltage of the regulator, the load current rise and fall had to be captured using separate pulses. Fig. 6.18 shows the transient response for V_{OUT} = 15 V to a 3 A load current change at 25 °C. The large undershoot and overshoot voltages can be observed to be about ±10% of the desired output voltage.

Due to these large undershoot and overshoot voltages it was decided to concentrate the testing of the linear regulator to a maximum load current of 2 A as it was mentioned at the beginning of this chapter. As discussed before, the unaccounted parasitic elements take a toll on the performance on the regulator. It should be noted also, that these parasitic elements and the discrepancy between the models used for the design of this regulator also probably affect the DC biasing of the error amplifier. This situation would result in an unaccounted gain reduction in the error amplifier that is also evident in the larger than simulated values for the load and line regulation data.

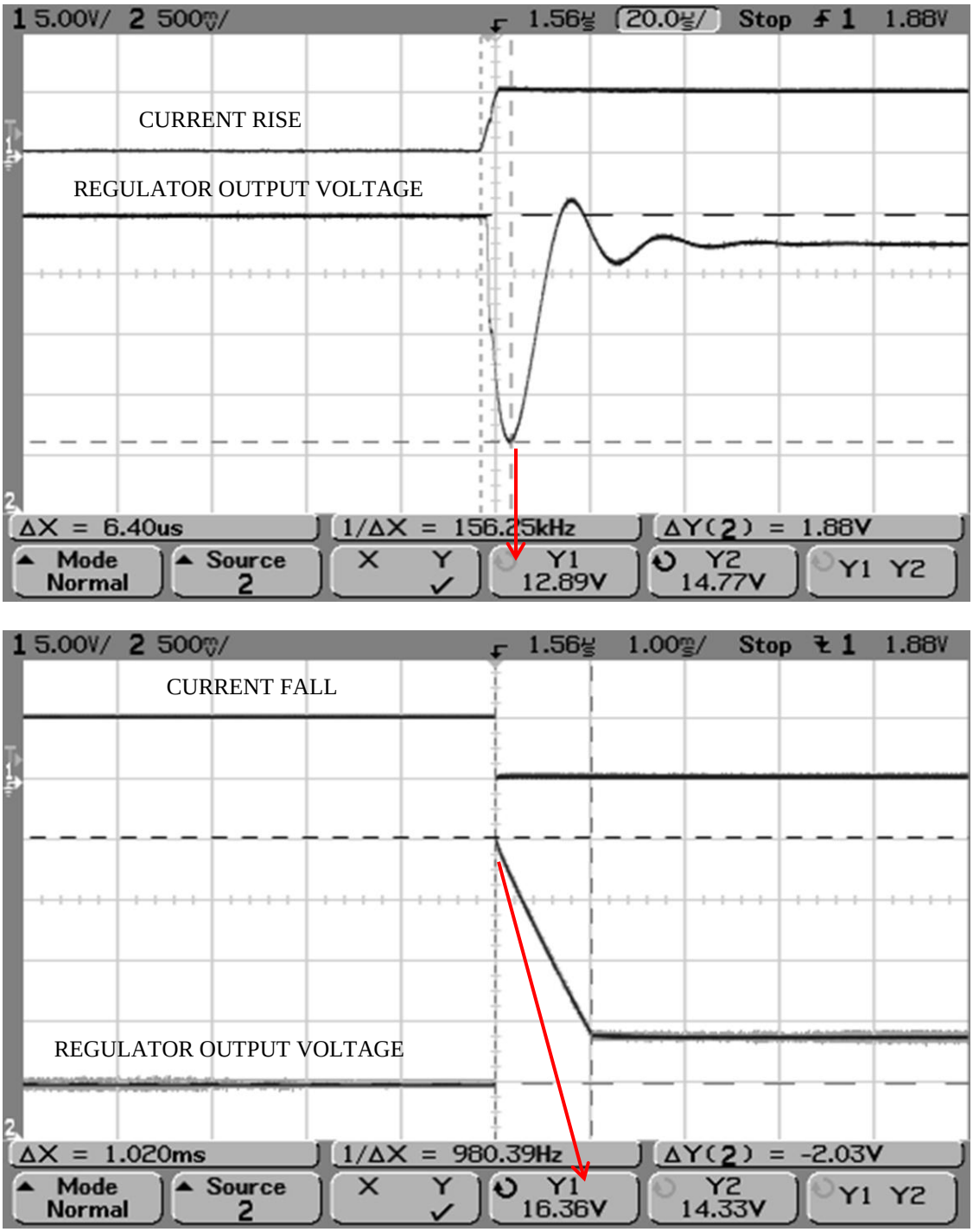


Fig. 6.18 – Transient response to a 3 A load current change at 25 °C for V_{OUT} = 15 V. The top curve in each figure is the control signal applied to the gate of the power MOSFET. The output of the regulator in each figure is the bottom curve.

Screenshots from the oscilloscope as the ones shown in Fig. 6.18 were taken for 10, 12.5 and 15 V output voltages at 25, 125 and 225 °C for different load conditions. However, for brevity, only the waveforms for the worst case condition (225 °C and 2 A) for a 10 and a 15 V output voltage is presented here. Fig. 6.19 and 6.20 shows the transient response to a 2 A load current change for the conditions previously mentioned. Table 6.6 shows a summary of the complete transient test for V_{OUT} = 15 V and a comparison between the measured and simulated values as well.

Table 6.6 – Measured and Simulated Transient Performance of the Linear Regulator at 25, 125 and 225 °C for V_{OUT}=15 V.

Temperature (°C)	Load (A)	V_{OUT} (V)	Undershoot (V)	Overshoot (V)
25	0	14.76 (14.99)	--	--
	1	14.66 (14.94)	14.14 (14.92)	15.34 (15)
	2	14.54 (14.91)	13.63 (14.87)	15.75 (14.99)
125	0	14.75 (14.98)	--	--
	1	14.61 (14.92)	14.05 (14.89)	15.3 (14.98)
	2	14.26 (14.89)	13.48 (14.83)	15.72 (14.98)
225	0	14.76 (14.97)	--	--
	1	14.41 (14.89)	13.95 (14.85)	15.3 (15.01)
	2	14.19 (14.79)	13.30 (14.67)	15.63 (15.02)

Measured (Simulated)

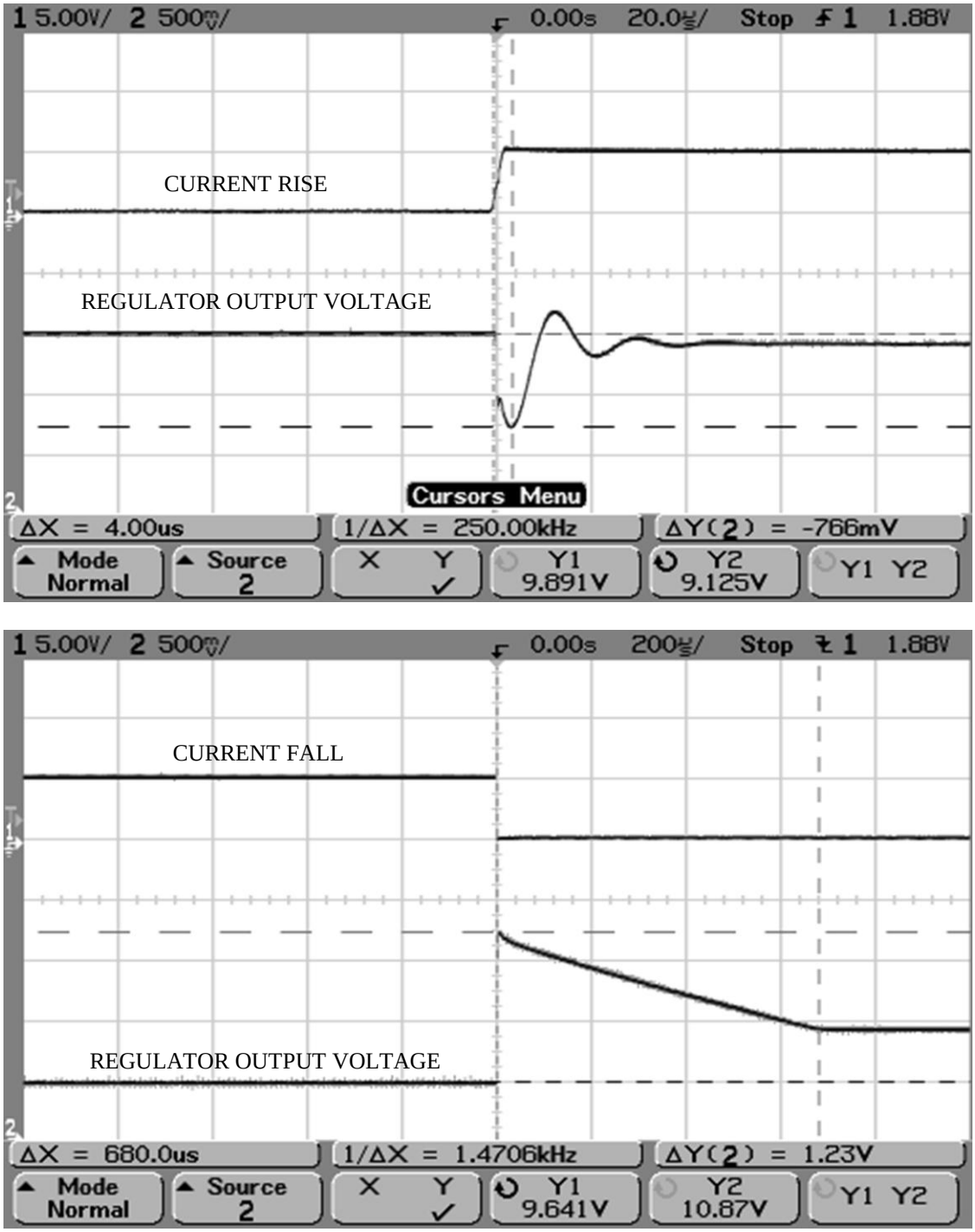


Fig. 6.19 – Transient response to a 2 A load current change at 225 °C for V_{OUT} = 10 V. The top curve in each figure is the control signal applied to the gate of the power MOSFET. The output of the regulator in each figure is the bottom curve.

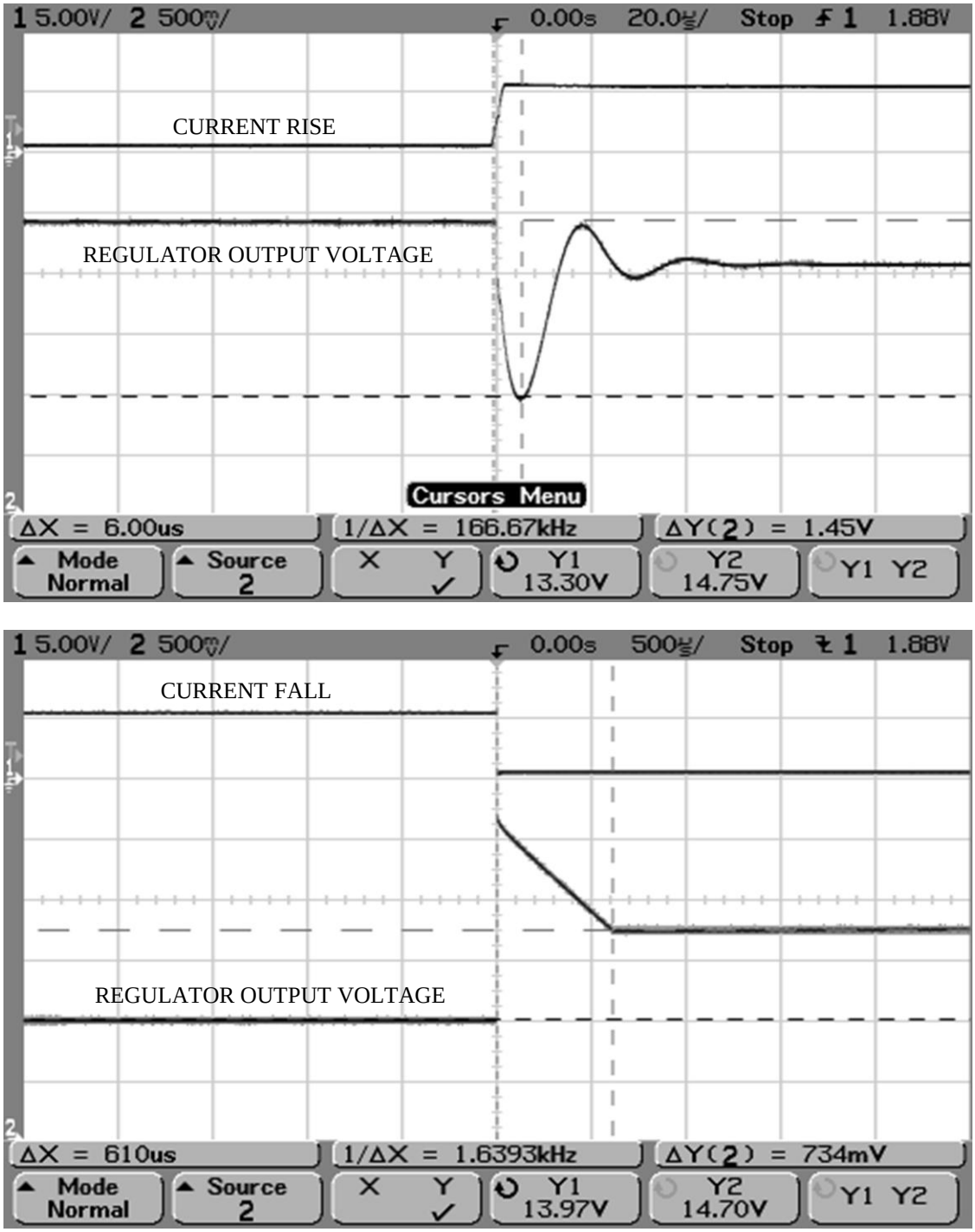


Fig. 6.20 – Transient response to a 2 A load current change at 225 °C for V_{OUT} = 15 V. The top curve in each figure is the control signal applied to the gate of the power MOSFET. The output of the regulator in each figure is the bottom curve.

The previous figures might seem to differ in the DC output voltages of the regulator. The main reason for this is the nature of the regulator itself. The output voltage of the regulator is constantly adjusted based on changes detected by the feedback network. Every time a test was performed on the regulator, the conditions were intended to be the same but it is likely that minimum variations in the test setup would be detected by the feedback network.

Also, at large loads (>1 A), the solder used for the power resistors in the daughter board started to melt after a couple of seconds. Even though these resistors were rated for this amount of power, the large amount of current had that effect on the solder material which translated into fluctuations in the resistive load (connections deteriorating). As a result, the transient and load regulation tests had to be performed quickly but, small fluctuations in the output voltage and current were still observed in the power supplies and in the oscilloscope.

An important point to notice from all the transient response figures is the particular overshoot magnitude and discharging behavior when the load current suddenly goes back to zero (negative current dump). Undershoot voltages are also large in magnitude although they do not present the long discharging behavior that overshoot voltages experience. This is the result of large parasitic capacitances and the large output capacitor, resulting in a time constant associated with the discharging of the capacitor. The capacitor needs to discharge the excess current being dumped to it while the pass device is still on, waiting to be turned off by the feedback network. The magnitude of undershoot and overshoot voltages is due mainly to inductive kicks associated with the test setup and the regulator itself. As expected, as the load current is increased, this behavior at the output voltage of the regulator worsens. These inductive kicks and other type of undesired responses due to parasitic elements should be replicated in simulations for further development of the regulator as discussed in the next chapter.

Undershoot and overshoot voltages can be improved by using a larger output capacitor. This of course, comes at the expense of a bulkier capacitor and a larger discharging time during the negative current dump. Fig. 6.20 shows the transient response to a 2 A load current change at 25 °C for V_{OUT} = 15 V using C_{OUT}=15 μF (ESR=0.2 Ω). Table 6.7 shows a comparison between these test results and the same test results from Table 6.6 when C_{OUT} = 10 μF. While these values were only taken at 25 °C, the trend will remain the same across temperature.

Table 6.7 – Measured Transient Performance of the Linear Regulator at 25 °C for V_{OUT} = 15 V with C_{OUT} = 10 μF and C_{OUT} = 15 μF.

C_{OUT} (μF)	Load (A)	V_{OUT} (V)	Undershoot (V)	Overshoot (V)
10	0	14.76	--	--
	1	14.66	14.14	15.34
	2	14.54	13.63	15.75
15	0	14.73	--	--
	1	14.66	14.42	14.97
	2	14.59	14.13	15.12

While Table 6.7 validates that using a larger output capacitor does in fact improve undershoot and overshoot voltages, Table 6.6 shows a completely functional SiC linear voltage regulator for V_{OUT} = 15 V up to a 2 A load current . The reason for which this regulator might not be feasible at a 3 A load current, as it was originally designed for, are the large undershoot and overshoot voltages mainly due to parasitic elements as previously discussed.

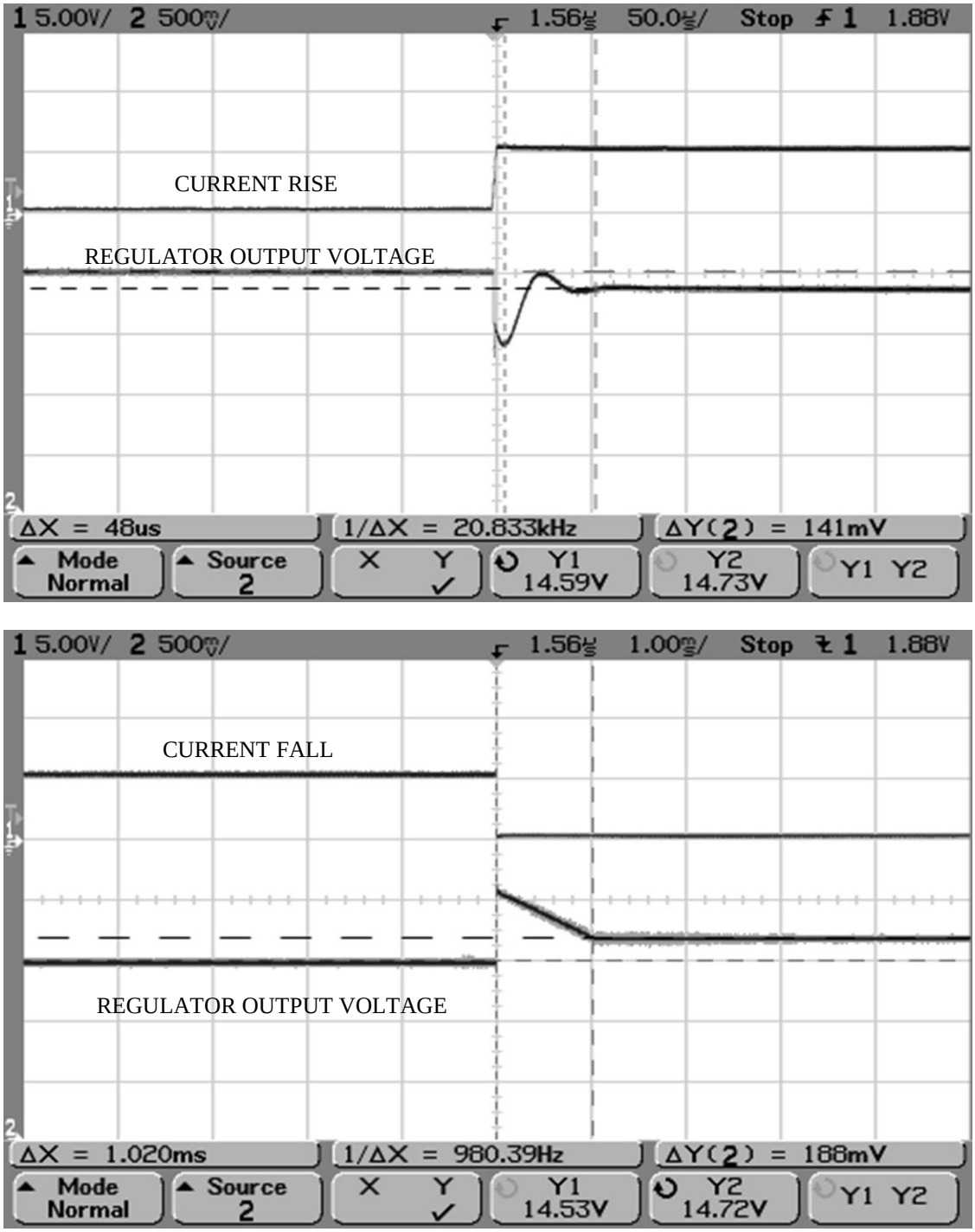


Fig. 6.20 – Transient response to a 2 A load current change at 25 °C for V_{OUT} = 15 V with C_{OUT}=15 µF. The top curve in each figure is the control signal applied to the gate of the power MOSFET. The output of the regulator in each figure is the bottom curve.

6.5 Overall performance

All the data presented so far corroborates that the regulator designed and fabricated for this dissertation is in fact, a fully functional one, with the limitation of the 2 A maximum load current. The expected differences between the measured and simulated data are explained by parasitic elements involved in the test setup and the different version of models used for the design of the circuit. The 3 A maximum load current originally designed for, can be achieved by initially replicating the undesired transient responses obtained in the experimental data so that the parasitic elements can be quantified. With this information, then make the necessary changes to the regulator to counteract these undesired effects. The overall measured performance of the linear regulator for the nominal V_{OUT} = 15 V and C_{OUT} = 10 μF is summarized in Table 6.8.

All the data presented in this chapter comes from a single die mounted on a Rogers 4350 PCB. However, data was also taken from two additional die in order to quantify the process variation. One of the die was mounted on a DBC board and the other die in a Rogers 4350 PCB. Table 6.9 shows a comparison of the DC output voltages and load regulation among the 3 die. *PCB 2* denotes the board used to collect all the data presented up to this point.

Table 6.9 indicates that there is less than 5% variation from the average value for the DC output voltages across temperature and different loads. In addition, the largest sample standard deviation for the DC output voltages is about 100 mV.

Table 6.8- Specifications of the SiC Linear Voltage Regulator for V_{OUT} = 15 V.

Temp (°C)	Load (A)	VOUT (V)	Load reg (%)	Line reg (mV/V)	Undershoot (V)	Overshoot (V)
25	0	14.76	--	15	--	--
	1	14.66	0.68	24	14.14	15.34
	2	14.54	1.49	36	13.63	15.75
125	0	14.75	--	17	--	--
	1	14.61	0.95	31	14.05	15.3
	2	14.26	3.32	55	13.48	15.72
225	0	14.76	--	20	--	--
	1	14.41	2.37	59	13.95	15.3
	2	14.19	3.86	168	13.30	15.63

Table 6.9- Process Variation Data for V_{OUT}=15 V.

		DBC		PCB 1		PCB 2		Average
Temp (°C)	**Load (A)**	**V_{OUT} (V)**	**Load reg (%)**	**V_{OUT} (V)**	**Load reg (%)**	**V_{OUT} (V)**	**Load reg (%)**	**V_{OUT} (V)**
25	0	14.79	--	14.84	--	14.76	--	14.80
	1	14.63	1.08	14.74	0.67	14.66	0.68	14.68
	2	14.47	2.16	14.57	1.82	14.54	1.49	14.53
125	0	14.69	--	14.83	--	14.75	--	14.76
	1	14.57	0.82	14.63	1.35	14.61	0.95	14.60
	2	14.3	2.65	14.45	2.56	14.26	3.32	14.34
225	0	14.83	--	14.82	--	14.76	--	14.80
	1	14.56	1.82	14.48	2.29	14.41	2.37	14.48
	2	14.26	3.84	14.11	4.79	14.19	3.86	14.19

CHAPTER 7: CONCLUSIONS AND FUTURE WORK

7.1 Summary

The first reported SiC linear voltage regulator has been presented in this dissertation. Since the feedback and compensation networks are external, the feasibility of regulating at different voltages and load currents allows a large range of applications for this regulator. In general, any system should always include some type of regulation to allow proper operation of all the circuits in the system. This regulator provides the first option in voltage regulation for the developing SiC IC processes reported in the literature.

The developing nature of the SiC process used to fabricate this regulator limited the options available for topologies and features that could be used to design the regulator. The lack of a PMOS device is a particular limitation that simply allowed neither fabricating an LDO nor increasing the gain of the regulator. Overall, all the limitations discussed in Chapter 3 impacted every area of the design process - from the models used to simulate the circuit to the layout used to fabricate it. In addition to this, while the last version of the models for this process was very satisfactory when compared to the measured data, these were not the models used to simulate the regulator. As a result, this implied, from the beginning, that measured and simulated data were going to differ. In addition, the effect of parasitic capacitances and inductances observed during testing took a toll on the performance of the regulator limiting the maximum load current to 2 A in order for the undershoot and overshot voltages to stay within ±10% of the regulated output voltage. A solution to this issue is discussed in the future work section.

At the end however, the approach of implementing a simple but working topology for the linear regulator proved to be correct. The simple fact that the depletion devices showed leakage

current at small V_{SB} values validated the approach to use resistors as pull-up devices in the error amplifier. This leakage current did not affect the pass device (the only depletion type device in the regulator) because the leakage current disappears completely as V_{SB} is increased. This is supported by pointing out that the DC current in the power supplies used for testing under no load conditions was always 6 to 7 mA, a result of adding the 5 mA quiescent current from the regulator with the ~1 mA quiescent current in the error amplifier. The use of an external voltage reference also proved to be correct for all the reasons previously discussed.

7.2 Future work

There are still areas of improvement for the linear voltage regulator presented in this dissertation. Some of them require further development of the process used to fabricate it, while others are needed to improve the performance of the regulator as it was originally designed. The main areas of improvement that would benefit this regulator are:

Experimental testbench simulations

The effects of parasitic elements in the performance of the regulator need to be replicated in simulations. This would allow quantifying the amount of resistance, inductance and capacitance associated with the test setup and the process itself. The simulations would consist of the same schematics but adding elements, mainly resistors and inductors, almost at every pin of the chip so that cables, daughter board, wire bonds and any other type of external connection can be properly represented in the simulation.

Once this process is complete, the total amount of resistance, inductance and capacitance would allow the evaluation of their effects on the performance of the regulator. Series resistance between the output and feedback network for example, would shift the DC output voltage down.

Inductance would be responsible for the large undershoot and overshoot voltages observed during transient and any capacitance in series with the output capacitor would affect this response as well. Finally, the regulator can be altered to counteract these parasitic elements either by adjusting the external parts used to test the regulator (feedback resistors and output capacitor) or by internal changes to the design itself. It is important to recall however, that the current capability of the pass device as it is sized currently meets the 3 A maximum load current. In fact, Section 6.4 shows the regulator delivering a 3 A maximum load current. The issues here, as it has been described, were the large undershoot and overshoot voltages. Hence, the changes needed in the design to reach this specification satisfactorily are mostly related to the effect of parasitic elements observed during testing rather than the circuit not being able to deliver that amount of current.

Regardless of these simulations however, a PoL application type for this regulator (as discussed in Section 4.2) would alleviate some of these parasitic elements effects. Using the regulator in a system level application where the regulator is placed in proximity to the load (without the need of wires and with very short solder connections) would certainly reduce the parasitic elements and an improvement in performance would be observed.

Larger gain from the error amplifier

As discussed previously, all the gain in the regulator comes from the error amplifier. Therefore, increasing this gain will directly result in an improvement in performance of the regulator. Subject to improvement in the performance of the depletion devices in this process, different topologies making use of these devices as loads could be explored so that the gain increases. The efficiency of the regulator would not change in this case, since depletion devices

used as loads are normally on, equivalent to a resistor as it was used in this design. However, the larger output resistance of the transistors would possibly benefit the gain of the error amplifier.

On-chip voltage reference

This option depends directly on the maturity of the process used so that performance variations related to the fabrication process and temperature are very controlled. Assuming this is achieved, an on-chip voltage reference would make the linear regulator more suitable for IC applications. However, given the importance of this voltage reference in the performance of the regulator, detailed attention has to be put into the topology and design used for the voltage reference.

Common-source configuration

This option also depends directly on the process used to fabricate the regulator. As of now, the Cree SiC process used only offers NMOS devices. As a result, the common-drain configuration of the pass device does not contribute to the gain of the regulator (gain less than unity). While it is true that a common-source configuration would require a PMOS device, it would contribute to the gain of the regulator and as a result, its performance would be improved. Having a PMOS device would also benefit the gain of the error amplifier and it would also allow exploring a large number of topologies available for amplifiers in CMOS processes.

Under Voltage Lockout (UVLO) and Over-Current Protection (OCP)

Most of today's voltage regulators offer some kind of protection again current spikes and low input voltages. Therefore, once the fabrication process allows it, the addition of these protection features would certainly enhance the performance of the linear voltage regulator as a

system. These features, besides providing protection for the devices in the regulator, also ensure protection for the circuits powered by the regulator.

7.3 Conclusion

The market's demand for more robust systems in terms of voltage blocking capabilities and temperature of operation have led to explore new semiconductor devices. SiC has proven to be a solution to these demands due mainly to its wide band gap properties. However, the fabrication of SiC devices had been focused until now, on discrete devices such as diodes and transistors. This implied for example, having a mixture of SiC and Si IC in a power electronic system. As expected, the next logical step was to attempt to fabricate SiC IC that would allow designing an entire SiC system, exploiting at its maximum the benefits of this material.

In a similar logical step, once SiC ICs start maturing, power management options will be needed to ensure proper operation of a system. This SiC linear voltage regulator addresses this need and pushes forward the state-of-the-art in SiC so that one day, not that far ahead, there will be complete and sophisticated SiC systems as analogous to the ones available in Si presently.

REFERENCES

[1] G. A. Rincon-Mora, *Analog IC design with low-dropout regulators*, The McGraw-Hill Companies, 2009.

[2] J. Valle-Mayorga, C. Gutshall, K. Phan, I. Escorcia, H. A. Mantooth, B. Reese, M. Schupbach, and A. Lostetter, "High Temperature Silicon-on-Insulator Gate Driver for SiC-FET Power Modules," IMAPS *International Conference and Exhibition on High Temperature Electronics Network (HiTEN)*, 7 pgs., Oxford, England, July 18-20, 2011.

[3] A. Elasser, and T. P. Chow, "Silicon Carbide Benefits and Advantages for Power Electronics Circuits and Systems," *Proceedings of the IEEE*, vol. 90, No. 6, pp. 969-986, Jun. 2002.

[4] B. McPherson, J. Hornberger, J. Bourne, A. Lostetter, R. Schupbach, R. Shaw, B. Reese, B. Rowden, K. Okumura, T. Otsuka, A. Mantooth, S. Ang, and J. Balda, "Packaging of High Temperature 50 kW SiC Motor Drive Modules for Hybrid-Electric Vehicles," *IMAPS*, San Jose, CA, pp. 663-670, Nov. 2009.

[5] A. B. Lostetter, J. Hornberger, B. McPherson, B. Reese, R. Shaw, M. Schupbach, B. Rowden, A. Mantooth, J. Balda, T. Otsuka, K. Okumura, and M. Miura, "High-Temperature Silicon Carbide and Silicon on Insulator Based Integrated Power Modules," *2009 IEEE Vehicle Power and Propulsion Conference*, Dearborn, Michigan, Sept. 7-11, 2009.

[6] U. Schmid, S. T. Sheppard, and W. Wondrak, "High Temperature Performance of NMOS Integrated Inverters and Ring Oscillators in 6H-SiC," *IEEE Transactions on Electron Devices*, vol. 47, no. 4, pp. 687-691, Apr. 2000.

[7] A. Patil, X. Fu, M. Mehregany, and S. Garverick, "Fully-Monolithic, 600 °C Differential Amplifiers in 6H-SiC JFET IC Technology," *IEEE 2009 Custom Integrated Circuits Conference*, Cleveland, Ohio, Sept. 13-16, 2009.

[8] W. Xie, J. A. Cooper, Jr., and M. R. Melloch, "Monolithic NMOS Digital Integrated Circuits in 6H-SiC," *IEEE Electron Device Letters*, vol. 15, no. 11, pp. 455-457. Nov. 1994.

[9] D.B. Slater, Jr., L.A. Lipkin, G.M. Johnson, A.V. Suvorov, and J.W. Palmour, "High Temperature Enhancement-Mode NMOS and PMOS Devices and Circuits in 6H-SiC," *Device Research Conference*, pp. 100-101, 1995.

[10] M. Gurfinkel, J. Suehle, J. B. Bernstein, Y. Shapira, A. J. Lelis, D. Habersat, and N. Goldsman, "Ultra-fast characterization of transient gate oxide trapping in SiC MOSFETs," *Proc. 45th Annual IEEE Int. Rel. Phys. Symp*., pp. 462–466, 2007.

[11] A. J. Lelis, D. Habersat, G. Lopez, J. M. McGarrity, F. B. McLean, and N. Goldsman, "Bias stress-induced threshold-voltage instability of SiC MOSFETs," *Materials Science Forum*, vol. 527–529, p. 1317-1320, 2006.

[12] A. J. Lelis, D. Habersat, F. Olaniran, B. Simons, J. M. McGarrity, F. B. McLean, and N. Goldsman, "Time-dependent bias stress-induced instability of SiCMOS devices," *Proc. Mater. Res. Symp.*, vol. 911, pp. 335–340, 2006.

[13] S. Suzuki, S. Harada, R. Kosugi, J. Senzaki, W. Cho, and K. Fukuda, "Correlation between channel mobility and shallow interface traps in SiC metal–oxide–semiconductor field-effect-transistors," *Journal of Applied Physics*, vol. 92, no. 10, pp. 6230–6234, Nov. 2002.

[14] B. J. Baliga, *Silicon Carbide Power Devices*, World Scientific, 2005.

[15] B. G. Streetman, and S. Banerjee, *Solid State Electronic Devices*, 6th ed., Prentice Hall, 2000.

[16] A. G. Chynoweth, "Ionization Rates for Electrons and Holes in Silicon," *Physical Review*, Vol. 109, pp. 1537-1545, 1958.

[17] A. G. Chynoweth, "Uniform Silicon P-N Junctions II. Ionization Rates for Electrons," *Journal of Applied Physics*, vol. 31, pp. 1161-1165, 1960.

[18] K. Matocha, "Challenges in SiC Power MOSFET Design," *ISDRS 2007*, College Park, MD, December 12-14, 2007.

[19] S. Potbhare, N. Goldsman, A. Akturk, and M. Gurfinkel, "Energy-and Time-Dependent Dynamics of Trap Occupation in 4H-SiC MOSFETs," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, Aug. 2008.

[20] A. Poggi, F. Moscatelli, S. Solmi, and R. Nipoti, "Investigation on the Use of Nitrogen Implantation to Improve the Performance of N-Channel Enhancement 4H-SiC MOSFETs," *IEEE Transaction on Electron Devices*, vol. 55, no. 8, Aug. 2008.

[21] A. Agarwal, M. Das, B. Hull, S. Krishnaswami, J. Palmour, J. Richmond, S. H. Ryu, and J. Zhang, "Progress in Silicon Carbide Power Devices," *Device Research Conference*, pp. 155-158, 2006.

[22] Datasheets available online at: http://www.cree.com

[23] Datasheets available online at: http://www.infineon.com

[24] Datasheets available online at: http://www.semisouth.com

[25] P. Friedrichs, "Unipolar SiC Devices – Latest Achievements on the Way to a New Generation of High Voltage Power Semiconductors", *CES/IEEE 5th International Power Electronics and Motion Control Conference*, Shanghai, China, pp. 1-5, 14-16 Aug. 2006.

[26] J. Millan, P. Godignon, and D. Tournier, "Recent Development in SiC Power Devices and Related Technology," *Proc. 24th International Conference on Microelectronics*, Vol. 1, Serbia and Montenegro, May 16-19, 2004.

[27] L. Cheng, et. al., "Development of Low RON,Diff, 12 kV 4H-SiC GTOs for High-Power and High-Temperature Applications," presented at the *IMAPS High Temperature Electronics Conference (HiTEC),* Albuquerque, NM, May 8-10, 2012.

[28] H. Zhang, L. M. Tolbert, and B. Ozpineci, "Impact of SiC Devices on Hybrid Electric and Plug-In Hybrid Electric Vehicles," *IEEE Transactions on Industry Applications*, vol. 47, no. 2, Mar-Apr. 2011.

[29] G. Majumdar, and T. Oomori, "Some Key Researches on SiC Device Technologies and their Predicted Advantages," *Power Electronics Europe*, Issue 6, pp. 18-22, 2009.

[30] P. Roussel, "SiC power devices: if we only had a switch…," *Semiconductor Today, Compounds & Advanced Silicon,* vol. 2, Issue 5, pp. 40-42, Jun. 2007.

[31] B. McPherson, J. Hornberger, J. Bourne, A. Lostetter, R. Schupbach, R. Shaw, B. Reese, B. Rowden, A. Mantooth, S. Ang, J. Balda, K. Okumura, and T. Otsuka, " Packaging of High Temperature 50 kW SiC Motor Drive Modules For Hybrid-Electric Vehicles", *IMAPS 42nd International Symposium on Microelectronics*, San Jose, CA, Nov. 1-5, 2009.

[32] B. Reese, B. McPherson, R. Shaw, J. Hornberger, R. Schupbach, A. Lostetter, B. Rowden, A. Mantooth, S. Ang, J. Balda, K. Okumura, and T. Otsuka, " High Temperature (250 °C) Silicon Carbide Power Modules With Integrated Gate Driver Boards", *IMAPS International Conference on High Temperature Electronics HiTEC*, Albuquerque, NM, May 11-13, 2010.

[33] J. S. Chen, K. T. Kornegay, and S. H. Ryu, "A Silicon Carbide CMOS Intelligent Gate Driver Circuit with Stable Operation over a Wide Temperature Range," *IEEE Journal of Solid State Circuits,* vol. 34, no. 2, pp. 192-204, Feb. 1999.

[34] M. Tomana, R. W. Johnson, R. C. Jaeger, and W. C. Dillard, "A Hybrid Silicon Carbide Differential Amplifier for 350 °C Operation," *IEEE Transactions on Components, Hybrids and Manufacturing Technology*, vol. 16, no. 5, pp. 536-542, Aug. 1993.

[35] S. Singh, and J. A. Cooper, "Bipolar Integrated Circuits in 4H-SiC," *IEEE Transactions on Electron Devices*, vol. 58, no. 4, pp. 1084-1090, Apr. 2011.

[36] Y. Zhang, K. Sheng, M. Su, J. Zhao, P. Alexandrov, X. Li, L. Fursin, and M. Weiner, "Development of 4H-SiC LJFET-Based Power IC," *IEEE Transactions on Electron Devices*, vol. 55, no. 8, pp. 1934-1945, Aug. 2008.

[37] P. G. Neudeck, D. J. Spry, L. Y. Chen, C. W. Chang, G. M. Beheim, R. S. Okojie, L. J. Evans, R. Meredith, T. Ferrier, M. J. Krasowski, and N. F. Prokop, "6H-SiC Transistor Integrated Circuits Demonstrating Prolonged Operation at 500 °C," *IMAPS HiTEC*, 2008.

[38] A. Vert, et. al., "SiC High Temperature Operational Amplifier," *IMAPS International Conference and Exhibition on High Temperature Electronics HiTEC*, Albuquerque, NM, May 8-10, 2012.

[39] M. Mudholkar, "Characterization and Modeling of 4H-SiC Low Voltage MOSFETs and Power MOSFETs," PhD dissertation, Dept. Elect. Eng., University of Arkansas, Fayetteville, AR, May 2012.

[40] I. A. Young, "A High-Performance All-Enhancement NMOS Operational Amplifier," *IEEE Journal of Solid State Circuits*, vol. SC-14, no. 6, pp. 1070-1077, Dec. 1979.

[41] D. Senderowicz, D. A. Hodges, and P. R. Gray, "High-Performance NMOS Operational Amplifier," *IEEE Journal of Solid State Circuits*, vol. SC-13, no. 6, pp. 760-766, Dec. 1978.

[42] D. Senderowicz, and J. H. Huggins, "A Low-Noise NMOS Operational Amplifier," *IEEE Journal of Solid State Circuits*, vol. SC-17, no. 6, pp. 999-1008, Dec. 1982.

[43] A. S. Sedra, and K. C. Smith, *Microelectronic Circuits*, 5th ed., Oxford University Press, New York, 2004.

[44] J. W. Nilsson and S. A. Riedel, *Electric circuits*, 6th ed., Prentice Hall, 2000.

[45] E. H. Snow, A. S. Grove, B. E. Deal, C. and T. Sah, "Ion Transport Phenomena in Insulating Films," *Journal of Applied Physics*, vol. 36, no.5, pp.1664-1673, May 1965.

[46] P. Balk and J. M. Eldridge, "Phosphosilicate Glass Stabilization of FET Devices," *Proceedings of the IEEE*, vol. 57, no. 9, pp. 1558-1563, 1969.

[47] J. W. Osenbach, and S. S. Voris, "Sodium diffusion in plasma-deposted amorphous oxygen-doped silicon nitride (a-SiON:H) films," *Journal of Applied Physics*, vol. 63, no.9, pp. 4494-4500, May 1988.

[48] C. W. Pearce, J. L. Moore, and F. A. Stevie, “Removal of Alkaline Impurities in a Polysilicon Gate Structure by Phosphorus Diffusion,” *Journal Electrochemical Society*, vol. 140, no. 5, pp. 1409-1413, May 1993.

[49] S. Potbhare, N. Goldsman, G. Pennington, L. Aivars, and M. James, “A physical model of high temperature 4H-SiC MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 100, pp. 2029-2040, 2006.

[50] A. Goetzberger and J. C. Irvin, “Low-temperature hysteresis effects in metal-oxide-silicon capacitances caused by surface state trapping,” *IEEE Transactions on Electron Devices*, vol. ED-15, pp. 1009–1014, 1968.

[51] Datasheets available online at: http://www.ti.com/ldo

[52] R. J. Milliken, “A capacitor-less low drop-out voltage regulator with fast transient response,” MS thesis, Dept. Elect. Eng., Texas A&M University, College Station, TX, Dec. 2005.

[53] Kim, Y.-I., and Lee, S.-S., "Fast transient capacitor-less LDO regulator using low-power output voltage detector," *Electronics Letters*, vol.48, no.3, pp.175-177, Feb. 2, 2012.

[54] E.N.Y. Ho, and P.K.T. Mok, "A Capacitor-Less CMOS Active Feedback Low-Dropout Regulator With Slew-Rate Enhancement for Portable On-Chip Application," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol.57, no.2, pp.80-84, Feb. 2010.

[55] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed., John Wiley & Sons, Inc., New York, 2001.

[56] E. Rogers, “Stability Analysis of Low-Dropout Linear Regulators with a PMOS Pass Element,” Power Management Division, Texas Instruments, Inc., August 1999.

[57] G. A. Rincon-Mora, “Current Efficient, Low Voltage, Low Drop-Out Regulators”, Ph.D. dissertation, Dept. Elect. Eng., Georgia Inst. of Technology, Atlanta, GA, Nov. 1996.

[58] J. Falin, “ESR, Stability, and the LDO Regulator”, Application Report, Texas Instruments, Inc., May 2002.

[59] J. Falin, “Ceramic Capacitors Replace Tantalum Capacitors in LDOs”, Application Report, Texas Instruments, Inc., Oct. 2006.

[60] G. A. Rincon-Mora, and P. E. Allen, “A Low-voltage, Low Quiescent Current, Low Drop-Out Regulator”, *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 36-44, Jan. 1998.

[61] T. Y. Man, P. K. T. Mok, and M. Chan, "A High Slew-Rate Push-Pull Output Amplifier for Low-Quiescent Current Low-Dropout Regulators with Transient-Response Improvement," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 54, no. 9, pp. 755-759, Sep. 2007.

[62] X. Ming, Z. Zhou, and B. Zhang, "A Low-Power Ultra-Fast Capacitor-Less LDO with Advanced Dynamic Push-Pull Techniques," *IEEE/IFIP 19th International Conference on VLSI and System-on-Chip*, 2011.

[63] P. Y. Or, and K. N. Leung, "An Output-Capacitorless Low-Dropout Regulator with Direct Voltage-Spike Detection," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 458-466, Feb. 2010.

[64] R. Gonzalez Carvajal, J. Ramirez-Angulo, A. J. Lopez-Martin, A. Torralba, J. A. Gomez Galan, A. Carlosena, and F. Munoz Chavero, "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design." *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 52, no. 7, pp. 1276-1291, Jul. 2005.

[65] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok, and M. Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 55, no. 5, pp. 1392-1401, Jun. 2008.

[66] M. Al-Shyoukh, H. Lee, and R. Perez, "A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator with Buffer Impedance Attenuation," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 8, pp. 1732-1742, Aug. 2007.

[67] M. Ho, K. N. Leung, and K. L. Mak, "A Low-Power Fast-Transient 90nm Low-Dropout Regulator With Multiple Small-Gain Stages," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 11, pp. 2466-2475, Nov. 2010.

[68] G. Giustolisi, and G. Palumbo, "Dynamic-biased capacitor-free NMOS LDO voltage regulator," *IEEE Electronic Letters*, Vol. 45, No. 22, Oct. 2009.

[69] D. Camacho, P. Gui, and P. Moreira, "An NMOS Low Dropout Voltage Regulator with Switched Floating Capacitor Gate Overdrive," *52nd IEEE Intl. Midwest Symposium on Circuits and Systems*, pp. 808-811, 2009.

[70] V. Gupta, and G. A. Rincon-Mora, "A 5mA 0.6μm CMOS Miller-Compensated LDO Regulator with -27dB Worst-Case Power-Supply Rejection Using 60pF of On-Chip Capacitance," *IEEE Intl. Solid-State Circuits Conference*, pp. 520-521, 2007.

[71] G. W. den Besten, and B. Nauta, "Embedded 5 V-to-3.3 V Voltage Regulator for Supplying Digital IC's in 3.3 V CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 7, pp. 956-962, Jul. 1998.

[72] V. Gupta, G. A. Rincon-Mora, and P. Raha, "Analysis and Design of Monolithic, High PSR, Linear Regulators for SoC Applications," *IEEE Intl. SoC Conference*, pp. 311-315, 2004.

[73] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-Efficient Linear Regulator with Ultra-Fast Load Regulation," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 933-940, Apr. 2005.

[74] K. Wong, and D. Evans, "A 150mA Low Noise, High PSRR Low-Dropout Linear Regulator in 0.13 μm Technology for RF SoC Applications," *Proceedings of the 32nd European Solid-State Circuits Conference*, pp. 532-535, 2006.

[75] C. Su, M. A. Huque, B. J. Blalock, S. K. Islam, L. M. Tolbert, and R. L. Greenwell, "A High Temperature, High-Voltage Linear Regulator in 0.8 μm BCD-on-SOI," *Intl. Symposium on Microelectronics*, pp. 207-214, 2009.

[76] B. W. Ohme, and M. R. Larson, "Control Circuit Design for High Temperature Linear Regulators," *Fourth Intl. High Temperature Electronics Conference HITEC*, pp. 45-50, 1998.

[77] B. Holter, T. Fallet, G. Forre, and S. D. Moen, "High Temperature Integrated Voltage Regulator System Design," *Proceedings of the 40th Midwest Symposium on Circuits and Systems*, vol. 2, pp. 1465-1468, 1997.

[78] Datasheets available online at: http://www.honeywell.com

[79] B. King, "Understanding the load-transient response of LDOs", *Texas Instruments Analog Applications Journal*, pp. 19-23, Nov. 2000.

[80] Texas Instruments, "3.0A Low Dropout Linear Regulator with Programmable Soft-Start," TPS 749xx datasheet, Jun. 2007 [Revised Nov. 2010].

[81] Datasheet available online at: http://www.rogerscorp.com/documents/726/acm/RO4000-Laminates---Data-sheet.aspx

[82] Datasheet available online at: http://www.fairchildsemi.com/ds/ND/NDT3055L.pdf