12-2011

Design of a Low Noise Amplifier for Wireless Sensor Networks

Ting Liu
University of Arkansas, Fayetteville

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Design of a Low Noise Amplifier for Wireless Sensor Networks

A thesis submitted in partial fulfillment
of the requirements for the degree of
Masters of Science in Electrical Engineering

By

Ting Liu
University of Arkansas
Bachelor of Science in Electrical Engineering, 2009

December 2011
University of Arkansas

ABSTRACT

CMOS technology becomes important in Radio Frequency (RF) communication systems which include both a receiver and a transmitter. In a high performance radio receiver, the Low Noise Amplifier (LNA) is the first circuit, and its noise performance dominates the entire receiver. Depending upon the system in which they are used, LNAs can be designed according to various topologies and structures. The LNA needs to have matched input impedance, and at the same time it should amplify the small amplitude input signal without adding too much noise and still have the minimal power consumption. It also needs a good interface with external filters for input and output matching networks; usually the input impedance is matched to a 50 Ω source resistor. Low noise figure, reasonable gain, stability and linearity are important properties for the LNA. This thesis will present a technique for implementing a CMOS Low Noise Amplifier with inductive source degeneration, compare this approach with other topologies, analyze the source of noise, and match the input and output impedance. The design requirements for the LNA are operation at 433 MHz, achieving noise figure smaller than 2 dB, and voltage gain around 15 dB. The circuit was implemented in the IBM 130 nm CMOS process.

This thesis is approved for
Recommendation to the
Graduate Council

Thesis Director:

_____

Dr. H. Alan Mantooth

Thesis Committee:

_____

Dr. Randy Brown

_____

Dr. Scott Smith

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ACKNOWLEDGEMENTS

I would like to thank many people who made my life at Arkansas memorable. First, I wish to acknowledge my advisor, Professor Dr. H. Alan Mantooth. He gave me this great opportunity to participate in the wireless sensor network project. And I am really thankful for his support, courage and guidance throughout the pursuit of my Master's degree. I would also like to thank Dr. Randy Brown and Dr. Scott Smith for being part of my thesis committee.

I also wish to acknowledge all my team members in the project for their constant support and help during the research. I have learned a lot from each one of them, and am really thankful for all their help. I especially want to thank Dr. Matt Francis and Kacie Woodmansee for their careful review of my thesis.

All my work is dedicated to my God. I am thankful that my Lord Jesus Christ brought me to the United States, let me get to know Him, led me to find the meaning of my life and for being my savior. Thanks to God that for blessing me with the wisdom to accomplish all of the work I have done in US.

DEDICATION

I dedicate this thesis to my family and friends, especially…

to Dad and Mom for instilling the importance of hard work and higher education, and financial support for the five years of oversea study;

to Li Zhenhua for his understanding and patience, encouraging me to reach my dream;

to Hong Tan for being such a good friend and roommate, and taking good care of me;

to all the brothers and sisters in Chinese Church for their encouragement and support.

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CHAPTER 1

Introduction

Wireless communication has experienced a rapid development in the past two decades. There has been great growth in many high performance systems, such as cellular systems (AMPS, GSM, TDMA, CDMA, W-CDMA), global positioning system (GPS) and wireless local area network (WLAN) systems [1].

1.1 Overall Wireless Communication System

The digital revolution in the wireless market has brought many changes in analog transceivers today. The wireless transceiver has to detect a very weak and high frequency (almost always gigahertz) signal, and at the same time transmit it at high frequency and high power. This characteristic requires high performance from RF and baseband analog circuits, such as filters, amplifiers, voltage control oscillators (VCOs) and mixers. The required high performance of the RF circuit working at high frequencies brings a big challenge to the circuit design as well. With the consideration of the price and power consumption, many groups are doing research into the use of Complementary Metal-Oxide Semiconductor (CMOS) technologies for Radio Frequency (RF) applications. CMOS Integrated Circuits (ICs) have low cost, low power consumption and better integration with DSP chips, and they also allow a large amount of digital functions on a single die. They do, however, have limitations for noise and linearity compared to other processes, such as SiGe and GaAs processes.

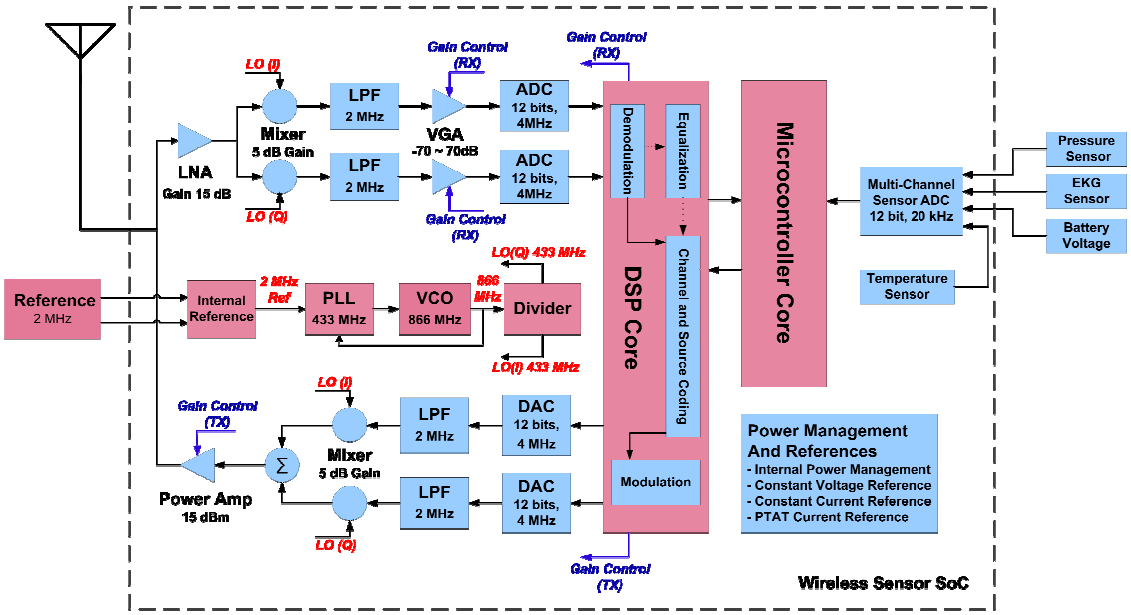

Figure 1.1. Wireless communication system

In Figure 1.1, the wireless sensor system can be seen, where the LNA receives a signal from the antenna, and outputs RF signals that are then mixed with the local oscillator signals through the down convert mixer. After the signal receives a large gain from (the programmable Gain Amplifier) PGA, it is converted by the Analog to Digital Converter (ADC) and processed by the digital core. The signal that coming from the digital core can then be retransmitted, by travelling through the Digital to Analog Converter (DAC), the up converting mixer and through the Power Amplifier (PA) which in turn drives the antenna.

1.2 Definition of Low Noise Amplifier

In a high performance radio receiver, the first block is usually the low noise amplifier, and its noise performance sets a limit on that of the entire receiver. The main function of an LNA is to minimize noise as much as possible while amplifying the small-signal from the antenna with a reasonable gain. In earlier research, LNAs have been developed to reach more stringent goals, such as using lower DC power supply, and the

reduction of the overall current and hence less power in the circuit. All the tradeoffs between size, cost, and performance have made the design of the LNA more complicated [2]. Most of the tradeoffs are between maximizing gain and minimizing noise figure, and much effort has been placed on optimizing both of these [2].

1.2.1 Friis' Formula

In a multi-stage communication system, every stage contributes noise to the entire system. According to Friis' Formula, the total noise factor, which is a scale used to measure the total noise in a circuit, can be calculated as:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \ldots \tag{1.1}$$

In this equation, the noise factor and gain of the first stage are significant contributions to the total noise factor, and the noise factor components of the following stages are reduced by the gain of the first stage. A reasonable large gain and a small noise factor for the first stage in a system should be important considerations for good signal processing. Using Friis' Formula for noise, and the fact that the LNA is typically the first block of the receiver, it is clear that the noise figure (NF) of the LNA is a key component for the entire front-end radio receiver circuit.

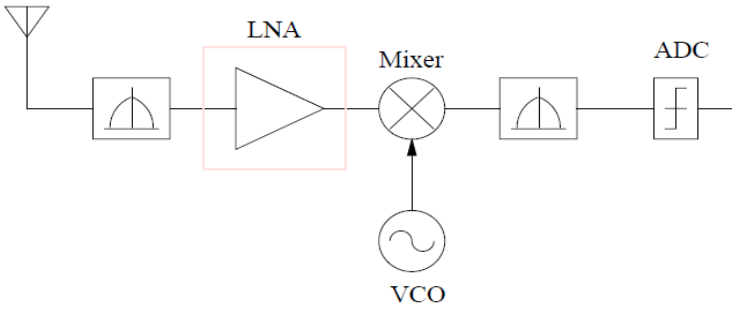

Figure 1.2. Typical architecture of a radio receiver [6]

The noise in the subsequent stages of the receiver chain is reduced by the gain of the LNA; so Friis' Formula can be expressed as:

$$F_{receiver} = F_{LNA} + \frac{(F_{rest} - 1)}{G_{LNA}} \tag{1.2}$$

From equation (1.2), it is clear that the role of an LNA is amplification of the input signal without addition of too much noise to the whole system.

1.3 Noise

Any communication system is sensitive to noise. In electronics, "everything except the desired signal [3]" is the general definition for noise. Artificial noise, such as power supply noise and signal cross talk can be avoided by good shielding. But some types of noise, classified as fundamental noises, are irreducible in the signal processing, and can be heard as continuous hissing in an audio system and seen as snow in a TV set. The fundamental noise is random but can still be characterized by statistical analysis. In an LNA, the major types of fundamental noise are thermal noise and quantum noise. Since this project is dealing with relatively low radio frequencies around 433 MHz, thermal noise is the main noise source.

1.3.1 Thermal Noise

The kinetic energy of particles generates thermal noise under their finite temperature. According to the discovery of Johnson, noise properties are determined by the temperature and electrical resistance of a given conductor rather than conductor's material and the measurement frequency [4] [5]. The thermal equilibriums are:

$$\overline{v_n^2} = s_{v_n}\Delta f = 4kT\Delta fR \tag{1.3}$$

$$\overline{i_n^2} = s_{i_n}\Delta f = 4kT\Delta f/R \tag{1.4}$$

where k is Boltzmann's constant (about $1.38 \times 10^{-23} J/K$), T is the absolute temperature in Kelvin, Δf is the noise bandwidth in Hertz over which the measurement is made, and R is the conductor's resistance. The models of the thermal noise are represented as follows:

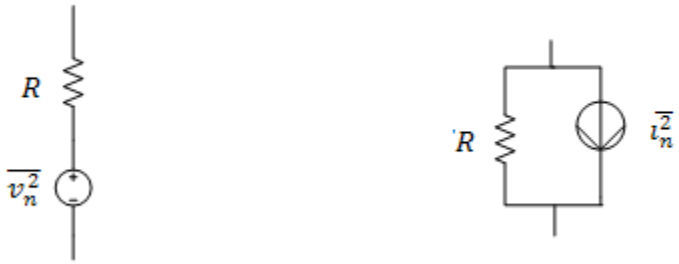

Figure 1.3. Resistor thermal noise models

When the random thermal agitation in the conductor gives rise to noise, the way to reduce the noise in the resistance is to keep the temperature as low as possible.

1.3.2 Thermal Noise in MOSFETs

In a high performance and high frequency analog RF circuit, the thermal noise behavior is important for a MOS transistor in saturation. According to van der Ziel's research, a thermal noise model for MOSFETs consists of drain current noise, induced gate current noise and their cross-correlation coefficient and is derived in [6]:

$$\overline{i_d^2} \triangleq 4kT\Delta f \gamma g_{d0} \tag{1.5}$$

$$\overline{i_g^2} \triangleq 4kT\Delta f \delta g_g \tag{1.6}$$

$$g_g \triangleq \zeta \frac{\omega^2 C_{gs}^2}{g_{d0}} \tag{1.7}$$

where $\gamma, \delta, and\ \zeta$ are bias-dependent factors; $g_{d0}$is the drain output conductance under zero drain bias, g_g is the real part of the gate-to-source admittance. For long-channel MOSFETs, the value of γ is $\frac{2}{3} \leq \gamma \leq 1$. These values keep the MOSFET in saturation.

Since the induced gate noise and drain current noise share the same origin, it can be assumed that δ is twice as large as γ [7].

1.3.2.1 Drain Current Noise

Substrate resistance especially contributes to drain current noise in long channel MOSFETs. Moreover, the drain current noise is frequency dependent, as seen from the inspection of the physical structure and the corresponding frequency-dependent expression for the substrate noise contribution [3]:

$$\overline{i_d^2} \triangleq \frac{4kTR_{sub}g_{mb}^2}{1+(\omega R_{sub}C_{cb})^2}\Delta f \tag{1.8}$$

This noise can be ignored as long as the operating frequency is below 1 GHz. Since the operating frequency is 433 MHz in this project, the drain current noise can be ignored in the total noise for a low noise amplifier.

1.3.2.2 Induced Gate Current Noise

At high frequency (beyond 10 MHz), there will be capacitive noise flow to the gate because of the high capacitive coupling between the channel and the gate. The resistive material between the gate and the channel can also produce a thermal noise current. The following picture shows the induced gate noise in a MOSFET:

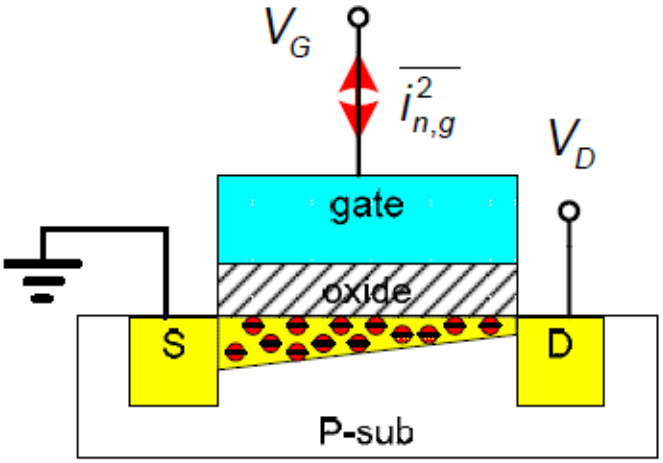

Figure 1.4. Induced gate noise model [8]

The following equations can be derived:

$$\overline{i_g^2} \triangleq 4kT\Delta f \delta g_g \tag{1.9}$$

$$g_g \triangleq \zeta \frac{\omega^2 C_{gs}^2}{g_{do}} \tag{1.10}$$

The spectral density of the induced gate noise, $\overline{i_g^2}$, is not a constant, and it is proportional to ω^2. As the noise will increase according to ω, the noise is not a white noise but a “blue noise”.

1.4 Noise Factor and Noise Figure

As the noise can be modeled by mathematical equations, the signal to noise ratio (SNR) can be used as a measurement of the presence of noise in a signal.

$$SNR = \frac{Signal\ Power}{Noise\ power} \tag{1.11}$$

The noise factor indicates the degradation of SNR by a circuit. Noise figure is an important measurement of the system noise performance. In realistic amplifiers, the components will add extra noise as the signal propagates through the network. “An ideal

noiseless two-port network contributes no noise, and the noise factor is equal to one" [7].If the circuit does have noise, the noise factor will be larger than 1.

$$F = \frac{Total\_noise\_power\_at\_output}{Noise\_power\_at\_output\_due\_to\_input\_source} \quad (1.12)$$

$$F = \frac{SNR_{IN}}{SNR_{OUT}} \quad \text{(Noise Factor)} \quad (1.13)$$

Noise figure (NF) is the noise factor expressed in dB unit:

$$NF = 10\log\left(\frac{SNR_{IN}}{SNR_{OUT}}\right) \quad \text{(Noise Figure)} \quad (1.14)$$

The Noise Figure is a major parameter for an LNA; the smaller the value, the better the noise performance; conversely, the larger the value, the more extra noise has been introduced into the whole system.

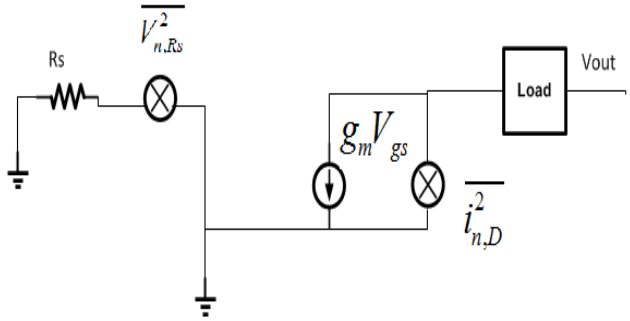

Figure 1.5. Noise sources in an LNA

For any kind of resistor, a noise will be generated due to the irregular movement of the current carrier. Thermal noise is modeled as a current source. In Figure 1.5, $\overline{V_{n,Rs}^2}$ is the noise from the source resistor; and $\overline{i_{n,D}^2}$ is the typical noise from the transistor, which is the thermal noise. More details about the LNA noises will be discussed in the design in Chapter 4.

CHAPTER 2

Two Port Network and Impedance Matching

2.1 Impedance Matching Network

It is desired for the circuit to transfer as much of the power as possible. Therefore, the transferred power will depend not only on the input and output resistance values, but also on the reactance values.

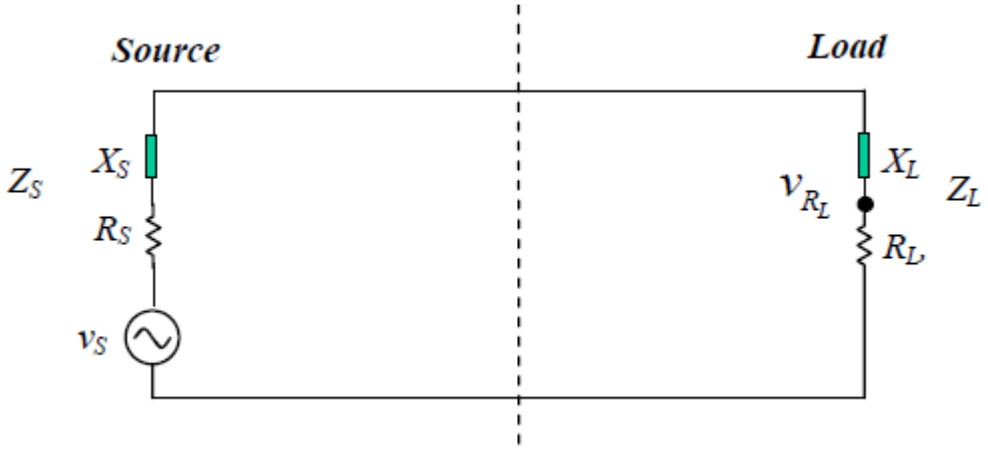

Figure 2.1. Voltage and power transferred from a source to a load [9]

From Figure 2.1, the load power equation can be derived as the following [9]:

$$P_{R_L} = v_S^2 \frac{R_L}{(R_S+R_L)^2+(X_S+X_L)^2} \tag{2.1}$$

where P_{R_L} is transferred power, R_S is the source resistor, R_L is the load resistor, v_S is the source voltage, X_S is the source reactance, and X_L is the load reactance.

In order to maximize the power transferred from the source to the load resistor, the reactance must have equal magnitude but opposite sign due to the following equations [9]:

$$X_S = -X_L \tag{2.2}$$

$$P_{R_L} = v_S^2 \frac{R_L}{(R_S+R_L)^2} \tag{2.3}$$

An impedance matching network is inserted between the source and the load to maximize power transfer without any phase shift [2]. The “impedance matching network in fact is an impedance-conversion network. It can be constructed by passive parts or both active and passive parts. The input and output matching networks of an LNA are a kind of matching network which usually consists of only passive parts. There would be no power consumption in the matching network if a matching network consists of only ideal inductors and capacitors” [9].

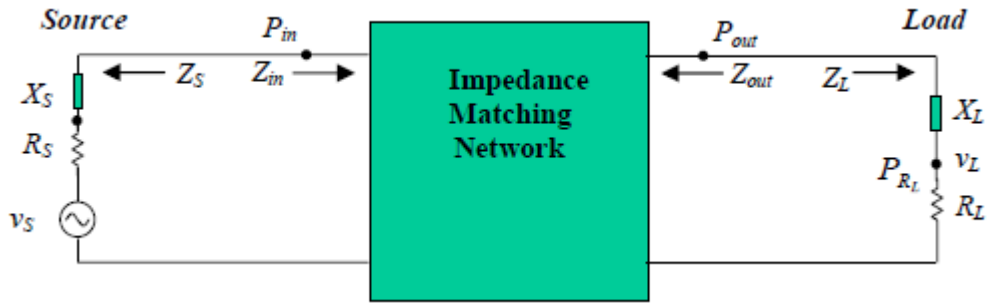

Figure 2.2. An impedance matching network inserted between source and load [9]

In Figure 2.2, P_{R_S} is the power in the source, P_{in} is the power delivered to the matching network from the source, P_{out} is the power at the output of impedance matching network, and P_{R_L} is the power delivered into the load resistor from the source [9]. However, for an LNA, the source resistor is considered to be 50 Ω for a load antenna, and most of the testing equipment is designed to match to 50 Ω as well; both the input and output impedances need to match 50 Ω so the circuit which will have the least power loss for the signal received from and the signal transferred to the next block.

As a conclusion, the real part of input impedance Z_{in} should be equal to 50 Ω; the same applies to the output impedance Z_{out}. And the imaginary parts should be cancelled by the impedance matching network.

2.2 Two Port S-Parameter

In the design of analog LNA circuits, work begins with the two-port network. The two-port network is used to determine figures such as gain, noise, linearity, and stability all of which are important for designing a Low Noise Amplifier. This method is most commonly used for radio frequency circuits which require low signal power consumption. In Figure 2.3, a two-port network with four terminals is shown, and the input and output of the circuit were defined by the two ports. “Two terminals define a port if the current flowing into one terminal is the same as the current flowing out of the other terminal” [6]. Two-port S-parameters are also an index used for evaluating how well the impedances match for the circuit.

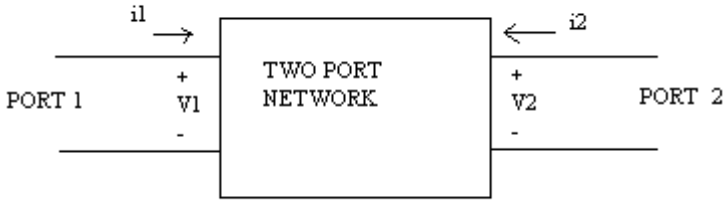

Figure 2.3. Two-port network diagram

In Figure 2.4, to simplify a two-port network, the circuit can be treated as a “black box” with a set of distinctive properties, so the physical performance of the circuit becomes less important during the analysis. S-parameters are defined in terms of traveling waves on transmission lines attached to each of the ports of the network. Individual elements are determined by measuring the forward and backward traveling waves with matched loads at both the input and output ports. The incoming and outgoing signal waves at the ports of a circuit are:

$$V_1^- = S_{11}V_1^+ + S_{12}V_2^+ \tag{2.4}$$

$$V_2^- = S_{21}V_1^+ + S_{22}V_2^+ \tag{2.5}$$

For S_{11}, if the output line is matched, $Z_L = Z_0$, then the load will not reflect power, so $V_2^+ = 0$,

$$S_{11} = \frac{V_1^-}{V_1^+}|_{V_2^+=0} \tag{2.6}$$

$$S_{21} = \frac{V_2^-}{V_1^+}|_{V_2^+=0} \tag{2.7}$$

S_{11} and S_{21} are measured at the terminals of the output cables in a matched impedance network.

$$S_{12} = \frac{V_1^-}{V_2^+}|_{V_1^+=0} \tag{2.8}$$

$$S_{22} = \frac{V_2^-}{V_2^+}|_{V_1^+=0} \tag{2.9}$$

S_{12} and S_{22} are measured at the terminals of the input cables in a matched impedance network.

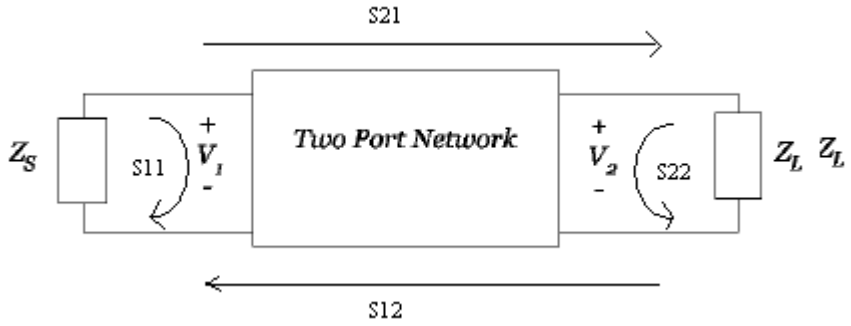

Figure 2.4. S Parameter representation of a two-port network [7]

In this LNA design, the input impedance requires matching the 50 Ω antenna, and the output impedance is required to match the impedance of the next block. S_{21} is the forward voltage gain and S_{12} is the reverse voltage gain, S_{11} is the input port voltage reflection coefficient, and S_{22} is the output port voltage reflection coefficient. The input return loss is the logarithmic magnitude of S_{11}, which is a scalar measurement of how

close the actual input impedance matches to the system; the S_{22} is similar to S_{11}, but it is measurement of the output port impedance matching.

CHAPTER 3

Design Topology

3.1 Topology Comparison

Many researchers have investigated different designs and implementations of LNA architectures using CMOS. There are three common CMOS LNA topologies that are analyzed and compared for an identical frequency operation in this chapter. Since the induced gate noise is the major contribution in an LNA, and is also a major characteristic; these three configurations are described according to the noise effects for an LNA.

3.1.1 Topology 1: Shunt Resistor

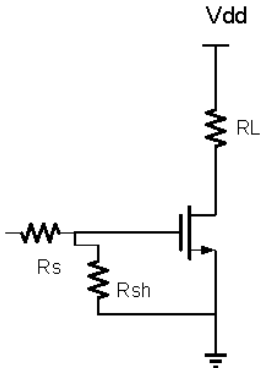

Figure 3.1. Shunt resistor topology [10]

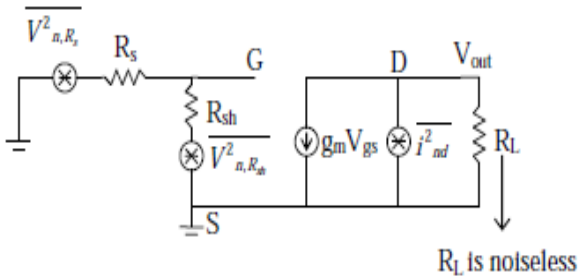

Figure 3.2. Small-signal model of shunt resistor topology [10]

In Figure 3.2, it is obvious that the R_{sh} term introduces extra noise $\overline{V^2_{n,Rsh}}$, so the shunt resistor structure will have poor noise figure; also the input signal is attenuated by

the voltage divider. However, it greatly simplifies impedance matching design. In Table 3.1, the values of Z_{in} are only dependent on the R_{sh}. So if R_{sh} equals 50 Ω, the input impedance matches 50 Ω.

3.1.2 Topology 2: Shunt Feedback Topology

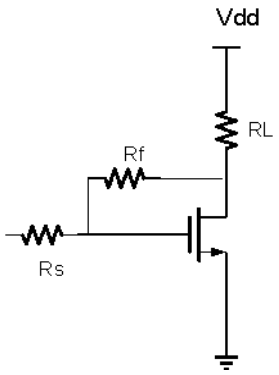

Figure 3.3. Shunt feedback topology [10]

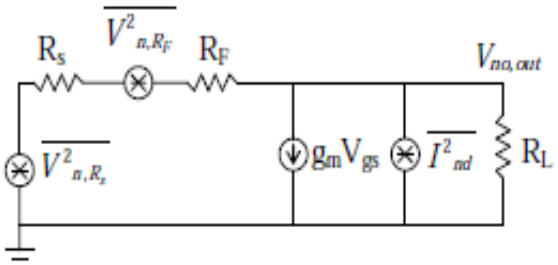

Figure 3.4. Small-signal model of shunt feedback topology [10]

In the shunt feedback topology (Figure 3.3), the R_F term again adds extra noise, $\overline{V^2_{n,Rf}}$ in the circuit. Although R_F could be selected to be larger than R_s to decrease the noise figure, it requires a shunt inductor when the operating frequency goes high. At relatively low radio frequency, this topology will have a broad band. And it is also easy for impedance match to 50 Ω. From Table 3.1, the input impedance is dependent on the values of g_m, R_F and R_L; as long as the value of g_m is defined, varying the values of R_F and R_L will easy match to 50 Ω.

3.1.3 Topology 3: Source Degenerated Topology

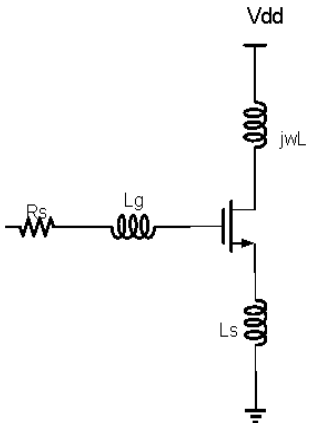

Figure 3.5. Source degenerated structure [10]

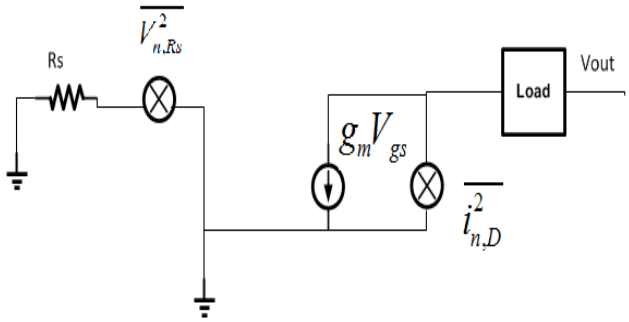

Figure 3.6. Small-signal model of source degenerated topology [10]

The source degenerated topology (Figure 3.5) has a very good noise figure, since it only has the noise source from the transistor itself and the source resistor; in addition, the inductors are all noiseless for an ideal one[10]. For this reason, this topology is chosen for the design of the LNA for the target application. Using equations in Table 3.1 it can be seen that the impedance is dependent on frequency so the circuit is only matched for a narrow frequency band. More discussion of the performances of this topology will be discussed in Chapter 4.

Table 3.1. Comparison of different topologies for the LNA [10]

Type of Topology	Zin	Noise Factor	Gain
Shunt Resistor	Rsh	$2+\frac{4\gamma}{g_m R_s}$	$\frac{-g_m R_L}{2}$
Shunt feedback	$\frac{R_F+R_L}{1+g_m R_L}$	$1+\frac{R_S}{R_F}(1+\frac{1}{g_m R_s})^2+\frac{\gamma}{g_m R_S}$	$-g_m R_L$
Source Degenerated	$j\omega(L_g+L_s)$ $+\frac{1}{j\omega C_{gs}}$ $+\frac{g_m L_s}{C_{gs}}$	$1+\frac{\gamma}{g_m R_S Q_{in}^2}$ $(note: Q_{in}=\frac{1}{2\omega_0 R_S C_{gs}})$	$Q_{in} g_m$

3.2 Cascode Amplifier

Due to the other major characteristic of LNAs, voltage gain, a large g_m is needed. A large g_m can also reduce LNA noise figure. Moreover, input-output isolation is important to reduce the LO leakage and for self-mixing. Applying the cascode input stage structure will not only improve g_m, but also provide a good input-output isolation and reduce the Miller effect.

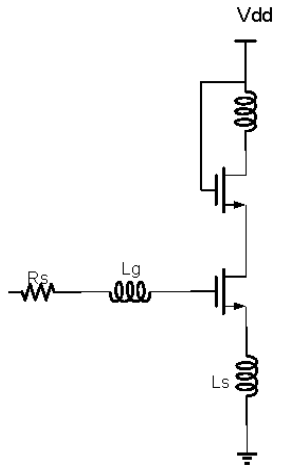

Figure 3.7. Cascode source degenerated LNA topology

3.3 Fully Differential LNA

In Chapter 1, it was seen in the interrelated circuit (Figure 1.1) that the Gilbert mixer requires differential inputs from LNA. A fully differential structure provides better performances for the circuit than the single-ended LNA. The substrate noise, which may arise from other components of the integrated circuit receiver, will be blocked by the differential structure of the LNA; this is one of the major advantages of the differential LNA. There are other advantages of a differential LNA: firstly, it decreases the sensitivity of the parasitic inductance which connects to ground (Ls); and secondly, the differential amplifier attenuates the common-mode signal. Since the LNA is receiving a small signal from the antenna which is a single-ended input, an off-chip balun transformer is needed to convert a small-single input to differential inputs feeding to the fully differential LNA. Note that this also introduces noise figure degradation.

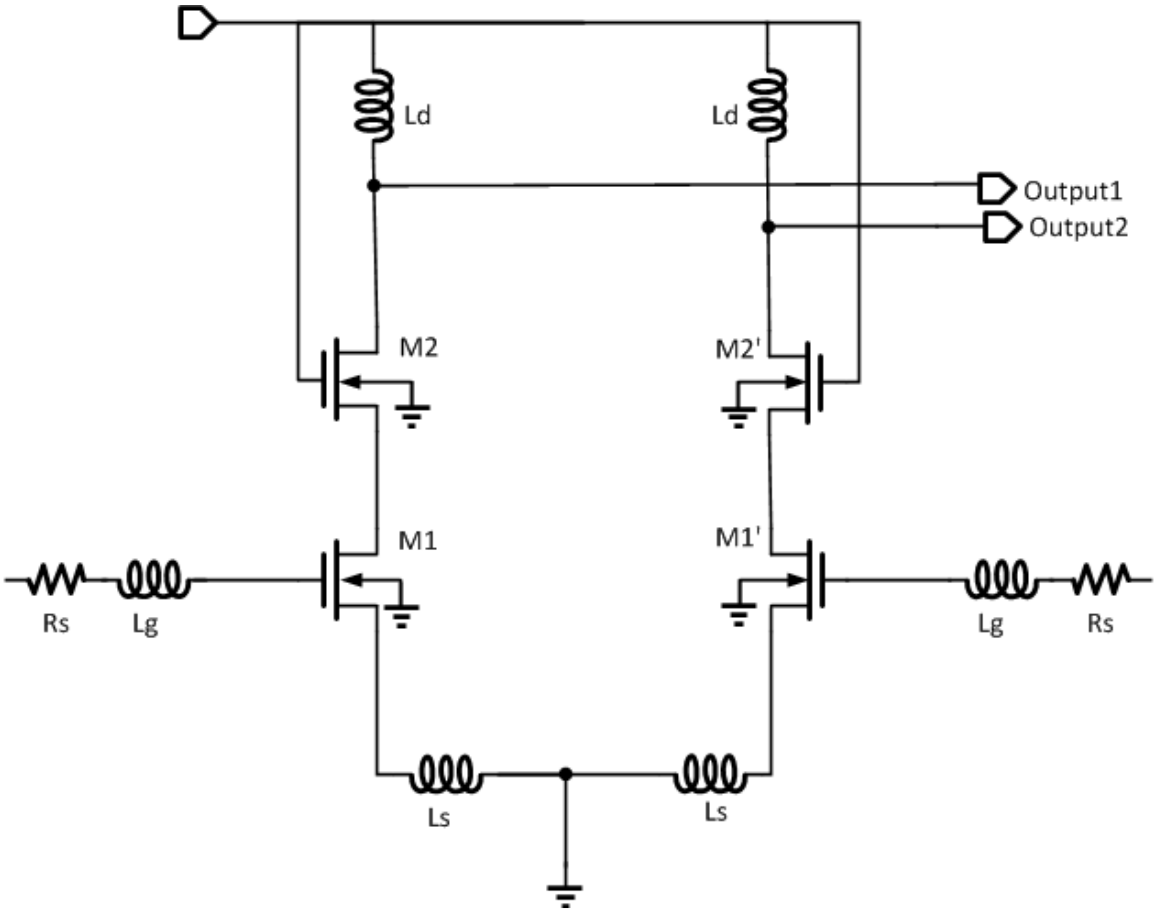

Figure 3.8. Fully differential LNA structure

CHAPTER 4

Design Process

As described in the previous chapters, the source degenerated topology is shown to have the best performances for a realistic LNA. In this chapter, the design of the size of the transistors and selection of the values for the inductors is described using the source degenerated topology. The LNA design is a tradeoff process, which means specifications such as noise figure, linearity, voltage gain, input and output matching and power consumption must be traded with each other to reach the optimal solution.

4.1 Characteristic Analysis

Consider the source degenerated topology and the small-signal model of an LNA (Figure 4.1):

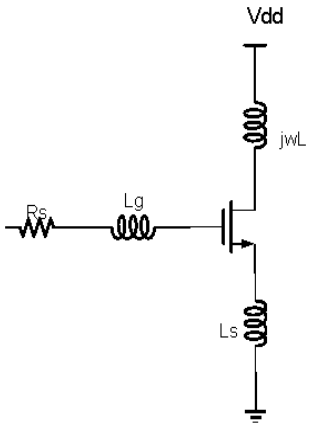

Figure 4.1. Source degenerated topology

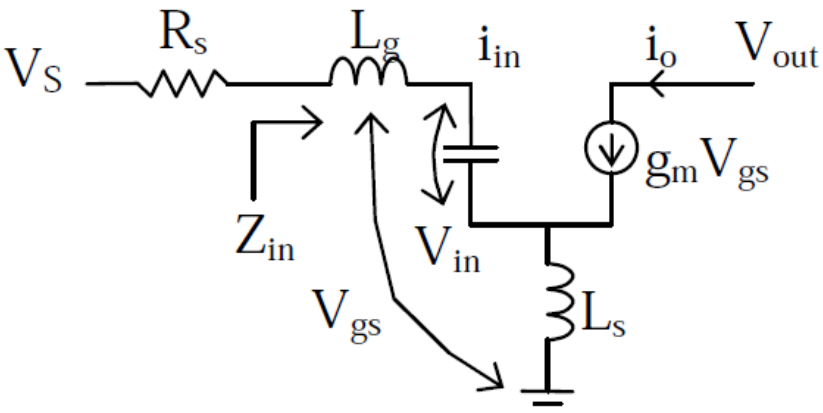

Figure 4.2. Small-signal model of LNA [10]

In Figure 4.1, Lg is the input inductor, Ls is the source inductor, and jwL represents the inductive load. Then considering the small-signal model of the LNA (in Figure 4.2), i_{in} is the input current of the transistor, and i_o is the output current of the transistor, g_m is the transconductance of the input transistor and C_{gs} is the gate to source capacitance; so, according to the KVL rule, the voltage can be derived from the small-signal model as following:

$$V_{in} = i_{in}(j\omega L_g + j\omega L_s) + i_{in}(\frac{1}{j\omega C}) + i_o j\omega L_s \tag{4.1}$$

The output current is:

$$i_o = g_m V_{gs} = g_m i_{in} \times \frac{1}{j\omega C_{gs}} \tag{4.2}$$

So,

$$V_{in} = i_{in}[j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}}] \tag{4.3}$$

The impedance at the input port is then derived as:

$$Z_{in} = \frac{V_{in}}{i_{in}} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{4.4}$$

To be matched with the parasitic capacitor, the following equality should be used:

$$\omega_o(L_g + L_s) = \frac{1}{\omega_o C_{gs}} \tag{4.5}$$

Since the antenna has a resistance equal to 50 Ω, the value of the inductor can be calculated from:

$$R_s = \frac{g_m}{C_{gs}} L_s = 50\Omega \tag{4.6}$$

Next, according to a series RLC circuit, the voltage ratio (Q) is given as:

$$Q = \frac{V_c}{V_{in}} = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 RL} \tag{4.7}$$

where V_c is the voltage on the capacitor.

For this series RLC circuit,

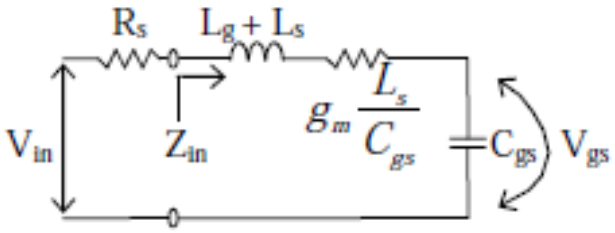

Figure 4.3. LNA series RLC circuit [10]

the voltage ratio (Q factor) will have the following expression:

$$Q_{in} = \frac{\omega_0(L_G + L_S)}{R_S + \frac{g_m L_S}{C_{gs}}} = \frac{1}{\omega_0(R_S + \frac{g_m L_S}{C_{gs}})C_{gs}} \tag{4.8}$$

So, the gain is:

$$V_{gs} = Q_{in} V_{in} \tag{4.9}$$

The transconductance can be derived from the previous equations:

$$G_m = \frac{I_{out}}{V_{in}} = \frac{V_{gs} g_m}{V_{in}} = Q_{in} g_m \tag{4.10}$$

So the voltage gain in the source degenerated circuit can be calculated as,

$$\frac{V_{out}}{V_{in}} = -G_m R_L \tag{4.11}$$

where R_L is the load resistance.

The noise model of this circuit is:

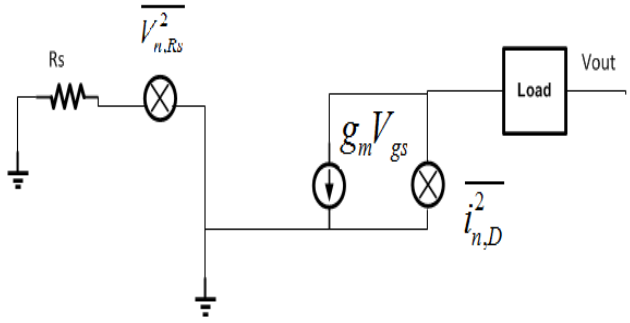

Figure 4.4. Noise model of source degenerated LNA[10]

From Chapter 1, the noise figure of this circuit can be expressed as:

$$F = \frac{Total\_noise\_power\_at\_output}{Noise\_power\_at\_output\_due\_to\_input\_source} = \frac{\overline{V_{n,Rs,out}^2} + \overline{V_{n,D,out}^2}}{\overline{V_{n,Rs,out}^2}} \tag{4.12}$$

where $\overline{V_{n,Rs}^2}$ is the noise from source resistor, and $\overline{i_{n,D}^2}$ is the thermal noise from the transistor. According to the thermal noise definition in Chapter 1, both of these can be expressed as follows [3] :

$$\overline{V_{n,R_s,out}^2} = \overline{V_{n,R_s}^2} G_m^2 R_L^2 = 4kTR_s \Delta f G_m^2 R_L^2 = 4kTR_s \Delta f Q_{in}^2 g_m^2 R_L^2 \tag{4.13}$$

$$\overline{V_{n,D,out}^2} = \overline{i_{n,D}^2} R_L^2 = 4kT\gamma g_m \Delta f R_L^2 \tag{4.14}$$

where k is Boltzmann's constant (about $1.38 \times 10^{-23}\ J/K$), T is the absolute temperature in Kelvin, and Δf is the noise bandwidth in Hertz over which the measurement is made,

R_L is the load resistor, R_S is the source resistor, G_m is the transconductance, and Q_{in} is the voltage ratio of the series RLC circuit.

Thus the noise factor given as:

$$F = 1 + \frac{\overline{i_{n,D}^2} R_L^2}{\overline{V_{n,Rs}^2} Q_{in}^2 g_m^2 R_L^2} = 1 + \frac{\gamma}{g_m R_s Q_{in}^2} \tag{4.15}$$

where γ is a bias-dependent factor.

4.2 Design of the Transistors

In order to calculate the size of the transistors, the gate-oxide thickness T_{OX} must be known, and the following parameters should be calculated: ε_0 is the permittivity of free space, ε_S is the relative permittivity of the material, and ε_{OX} is the permittivity of the silicon oxide.

$$\varepsilon_{ox} = \varepsilon_s \varepsilon_o \tag{4.16}$$

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} \tag{4.17}$$

where C_{OX} is the gate oxide capacitance, μ_n is the carrier mobility.

The calculation of the width of the input transistor W_{M1}, where ω_0 is the resonant frequency, C_{gs} is the gate to source capacitance, L is the gate length of the transistor, C_{ox} is the oxide capacitance per unit area, and R_s is the source resistance is given as:

$$W_{M1} = \frac{1}{3\omega_0 L C_{ox} R_s} \tag{4.18}$$

So the gate to source capacitance can be calculated by:

$$C_{gs} = \frac{2}{3} W_{M1} L C_{ox} \tag{4.19}$$

where g_m is the transconductance of the input transistor, and to calculate it we should assume a drain current value I_{DM1},

$$g_m = \sqrt{2 \times \mu_n C_{ox} \frac{W_{M1}}{L} I_{DM1}} \tag{4.20}$$

Finally the transition frequency is defined as:

$$\omega_T = \frac{g_m}{C_{gs}} \tag{4.21}$$

Using the equations in Chapter 3, the noise factor can be determined as following, where the noise figure is the noise factor in dB unit:

$$F = 1 + 2.4 \frac{\gamma}{\alpha} \frac{\omega}{\omega_T} \tag{4.21}$$

In order to match a pure resistance of 50 Ω, the parasitic capacitance from the transistor should be cancelled by inductive components in the circuit. The design of matching inductors is illustrated with the following equations. Normally for CMOS: $\gamma = 2$ and $\alpha = 0.9$, the unit of resonant frequency and transition frequency should be in radians/sec. In Figure 4.2, the source inductor Ls and the gate inductor Lg both can be calculated by the equations:

$$L_S = \frac{R_S}{\omega_T} \tag{4.22}$$

$$L_g + L_s = \frac{1}{(\omega)^2 \times C_{gs}} \tag{4.23}$$

Assuming a value for the load capacitor C_L, the load inductor can calculated from:

$$L_d = \frac{1}{\omega_0^2 C_L} \tag{4.24}$$

At 433MHz frequency, L_d and the output transistor width should be large enough to resonate with the C_{db} the drain-to-body capacitance of the output transistor at the

designed frequency. L_g and L_s are used to provided inductance to counteract the capacitance of C_{gs}, in order to form the necessary purely resistive input. “It is narrow band because the impedance matching is only established within a very narrow frequency range due to the resonant nature of the reactive matching network. [11]” Due to the large width of the transistors, the impedance matching network becomes challenging.

The overall design of the fully differential LNA is shown in Figure 4.5:

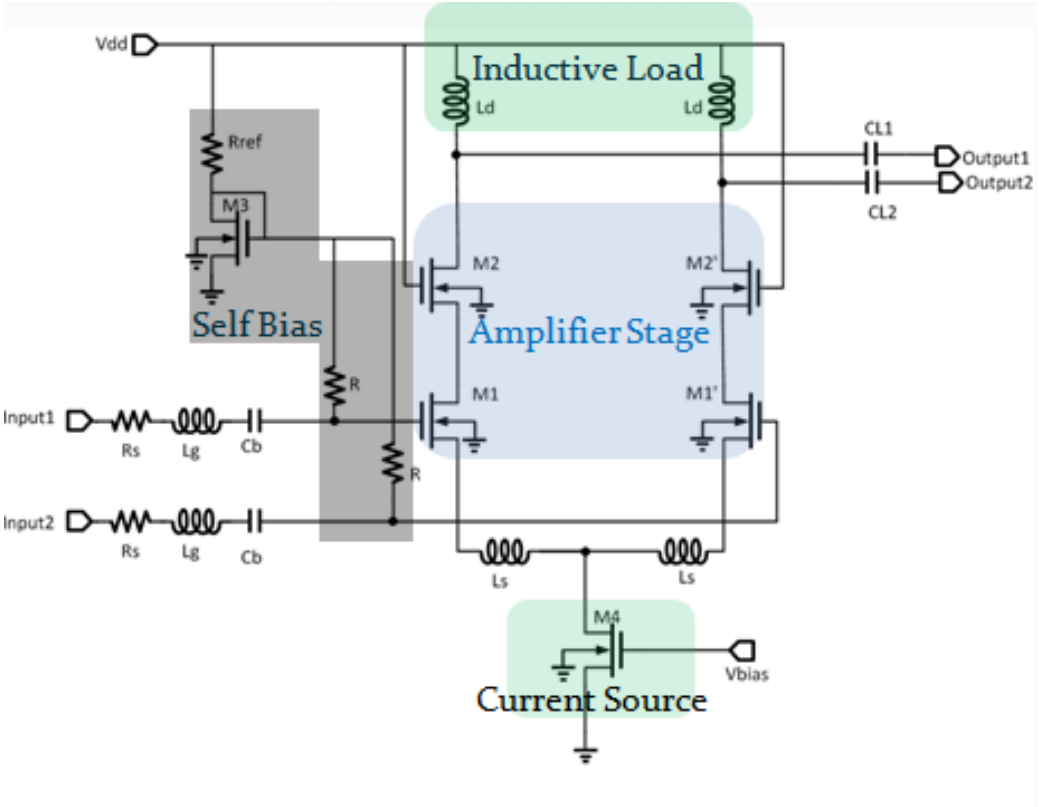

Figure 4.5. Fully differential LNA

To summarize, M1 and M1’ are the differential input transistors which have the same size, cascade transistors M2 and M2’ are “used to reduce the interaction of the tuned output with the tuned input” [3] and also to reduce the effect of M1’s C_{gd}, and improve the gain. M3 forms a current mirror with M1 and M1’ (M1=M1’), and its width is a “small fraction of M1’s width to minimize the power overhead of the bias circuit”

[3]. “The current through M3 is set by the supply voltage and R_{ref} in conjunction with V_{gs} of M3. The resistance R_{ref} needs to be large enough so that the equivalent noise current is small enough to be ignored” [3]. In this system, R_{ref} is slightly larger than 1 kΩ. M4 is used as a current source in the circuit, and it provides enough current for each branch. L_s is the source inductor used for impedance matching to a pure resistance at 50 Ω. L_d is the noiseless inductive load. An on-chip matching network would require a large inductor which would take more than 50% size of the chip. So in this design, off-chip inductor matching is properly designed to counteract the transistor parasitic capacitance. C_b is the DC blocking capacitor to complete the biasing and prevent the gate-to-source bias of M1 from getting upset.

It was assumed that the total current through the current source is 12 mA, so 6 mA for I_{DM1} is used in the calculation. For the impedance inductors calculation, C_b is assumed at 10 pF, so that the reactance can be ignored at the signal frequency.

Using all given information to calculate the values from the equations, all the component values for the LNA are recorded in the Table 4.1.

Table 4.1. Components calculation and simulation values

Components	Symbols	Calculated Values	Simulated Values
Transistor M1,M1', M2,M2'	W/L	1.716 m / 240 n	1.8 m / 240 n
Transistor M3	W/L	-	10 u / 240 n
Transistor M4	W/L	-	70 u / 240 n
Inductor	Ld	31.3 nH	11.932 nH
Inductor	Ls	0.51 nH	1.632 nH
Capacitor	CL1, CL2	10 pF	10 pF
DC block capacitor	Cb	10 pF	10 pF
Resistance	Rref	-	1.455 kΩ
Resistance	R	-	3.094 kΩ
Off-chip inductor	Lg	81.22 nH	43 nH
Off-chip capacitor	C1,C2	10 pF	10 pF

All inductor and capacitor values are fine tuned in simulation to achieve the lowest possible noise figure at the target frequency of 433MHz, which sacrificed the peak gain to be at a lower frequency.

CHAPTER 5

Simulations and Results

The design has been simulated with Cadence in spectreRF to verify the performances of the fully differential LNA. The main characteristics are simulated over the temperature range of -55 ºC to 125 ºC. The simulation test bench was designed to test the main characteristics of an LNA, such as noise figure, voltage gain, impedance match, stability and linearity. This design used RF type components for the main LNA circuit, such as RF transistors, RF inductors and RF capacitors. The RF transistors in the layout have guard rings which make a good shielding for the transistors. The RF inductors also have guard rings shielding to avoid the signal cross-talk. All the RF components have parasitic inductance, capacitance and resistance modeled. In spectreRF, analyses such as Periodic Steady State Analysis (PSS), Periodic Noise Analysis (Pnoise), and Periodic S-Parameter Analysis (PSP) are used to simulate the main characteristics. Transient Analysis (trans) was used to view the waveforms, and DC Analysis (dc) to check the transistor's quiescent state. All the simulations were performed using parasitic extracted layout including bonding pads. All characteristics and simulation results will be explained in this chapter.

5.1 Test Bench Setup

In Figure 5.1, the test bench in Cadence has the package bond wires modeled to imitate the parasitic capacitance, inductance and resistance in the real circuit. The power supply, bias voltage, ground, and differential input signals are applied to the circuit, and the differential output signals are observed. The power supply for VDD is 1.2 V, and Vbias is 0.6 V. The LNA chip symbol includes all the internal pad connections. The

input balun and output balun are used from the “rflib” library to convert from balanced to unbalanced signals, and vice versa. Impedance matching networks are inserted in the circuit, which uses ideal inductors and capacitors from the cadence “analogLib” library. The input port simulated with a sinusoidal waveform with -22 dBm amplitude (around 50 mVpp) at 433 MHz. Both input and output ports are set to have a 50 Ω resistance which act as source resistor and load resistor.

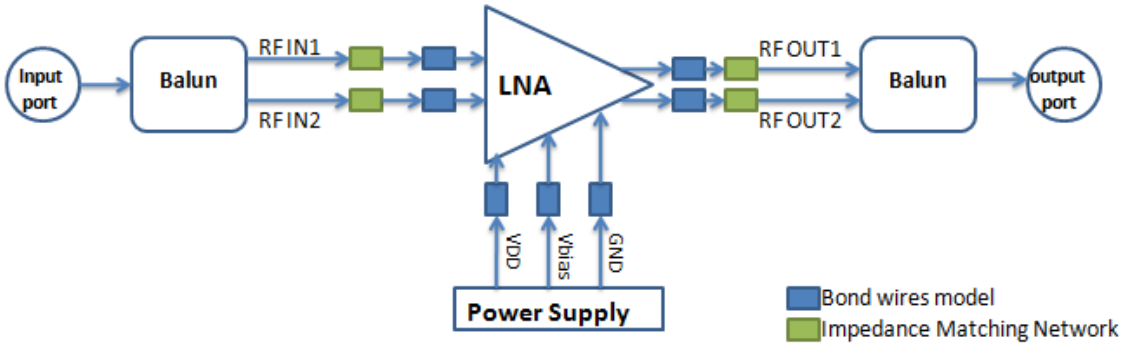

Figure 5.1. Test bench for LNA in Cadence

All the main characteristics’ simulation results below are explained at room temperature (25 ℃) specifically. In this RF design circuit, most of the circuits need acceptable performances throughout a temperature range. So the temperature variation becomes a key issue in the design of integrated circuits, and the temperature sweeps are recorded and analyzed in this chapter as well.

5.2 Voltage Gain Simulations

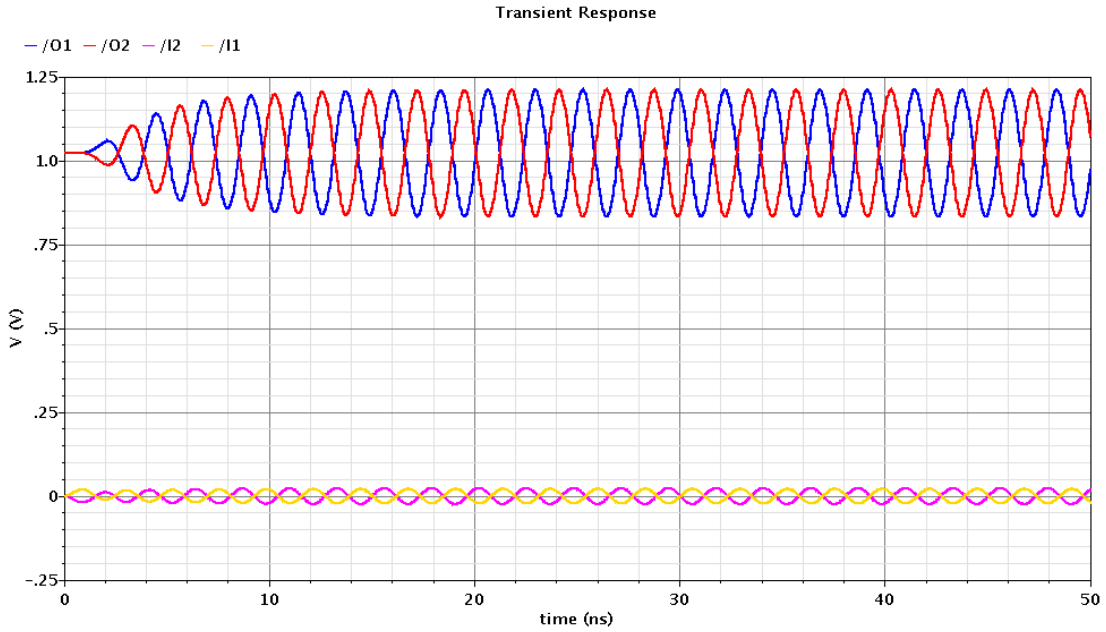

Figure 5.2. Differential inputs and differential output waveforms

In Figure 5.2, the two output signals are 180 degrees out of phase with each other, and the observed offset of the output signals is around 1.05 V.

The voltage gain simulation uses the PSS analysis. Auto calculation for the beat frequency is used with, ten output harmonics to be simulated. Accuracy defaults are set at moderate. The simulation is run and voltage gain is plotted from direct plot −>main form −> pss.

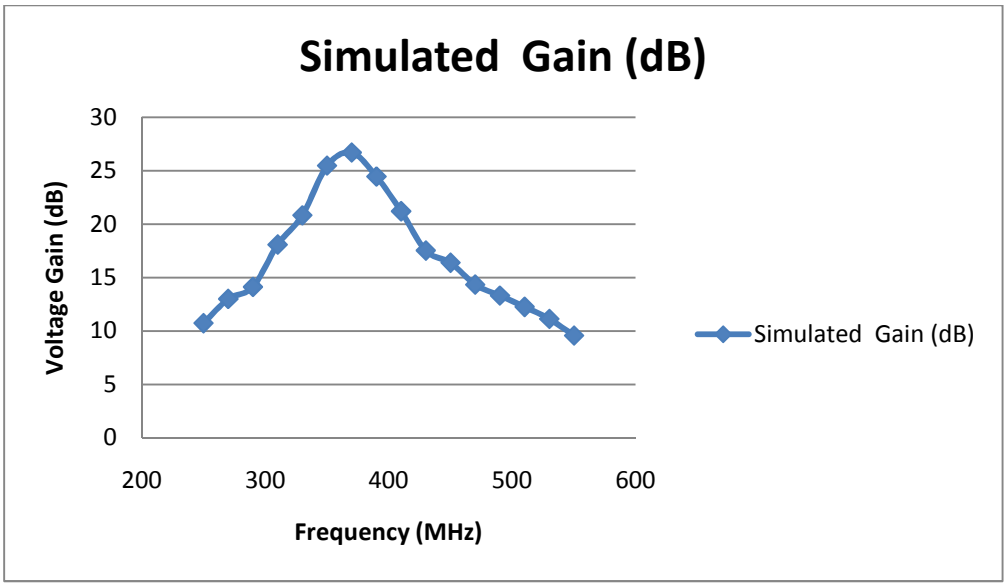

Figure 5.3. Voltage gain vs. frequency in band of interest (250MHz to 550MHz)

In Figure 5.3, the voltage gain has the maximum value equal 27dB at 370 MHz, as tradeoffs have been made to achieve the lowest noise figure at 433MHz, but also has a voltage gain equal 18.45dB which is still above the desired gain of 15 dB. More discussions of the tradeoffs between voltage gain and noise figure can be found in Chapter 8.

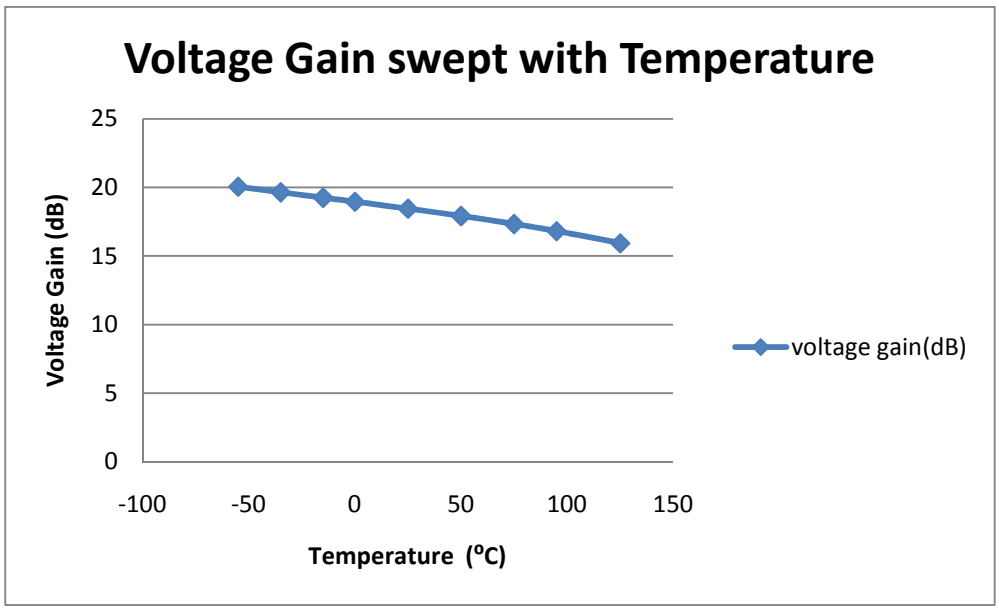

Figure 5.4. Voltage gain swept with temperature

Figure 5.4 is the simulation result of the voltage gain over temperature swept from -55 ºC to 125 ºC. The voltage gain decreases by as much as 5 dB as the temperature goes high. Temperature increases will lead the drain current (I_D) decreases [12]. In addition, as the temperature is increasing, both of the important parameters related to the temperature in MOSFET, threshold voltage (V_T) and mobility (μ_n) are decreasing according to the following expressions [13]:

$$V_T(T) = V_T(T_0) - \alpha_{V_T}\Delta T \tag{5.1}$$

$$\mu_n(T) = \mu_n(T_0)\left(\frac{T}{T_0}\right)^{\alpha_\mu} \tag{5.2}$$

where $\Delta T = T - T_0$, T_0 is the reference temperature. α_{V_T} lies in the range 0.5-4 mV/K, and α_μ lies in the range 1.5-2.

It can then be seen that the transconductance g_m of the transistor is decreasing with temperature from its expression:

$$g_m = \sqrt{2\mu_n C_{ox}}\sqrt{\frac{W}{L}}\sqrt{I_D} \tag{5.3}$$

As the voltage gain is proportional to transconductance of the transistor, it can be concluded that increasing temperature will decrease the transconductance, which means decreasing the voltage gain.

5.3 Noise Figure Simulations

The noise figure simulations are performed using Pnoise analysis. The selected beat frequency is at 433 MHz. The sweep range has been chosen from 100 MHz to 800 MHz. Automatic and absolute sweep types are used with 20 maximum sidebands. Voltage is chosen to be the output section, and the output net was selected as the positive output node, and GND was selected for the negative output node. The noise type was

chosen for sources, and then the enable box is checked. A simulation is run with PSS together, and Noise Figure is plotted from direct plot −>main form −> pnoise.

Figure 5.5 gives the simulated noise figure at 25 ºC. The results show the noise figure over the frequency range of 100 MHz to 800 MHz. The lowest peak value seen in figure is 1.48844 dB at 433.96 MHz. From noise factor calculations in Chapter 1, the noise factor thus is equal to 1.40878, which is the ratio of total noise power at the output and noise power only due to the input source. With 1.48844 dB noise figure at the required frequency, this LNA has a low noise figure at 25 ºC. Moreover, the LNA also has good noise performance at the frequency range from 400 MHz to 450 MHz.

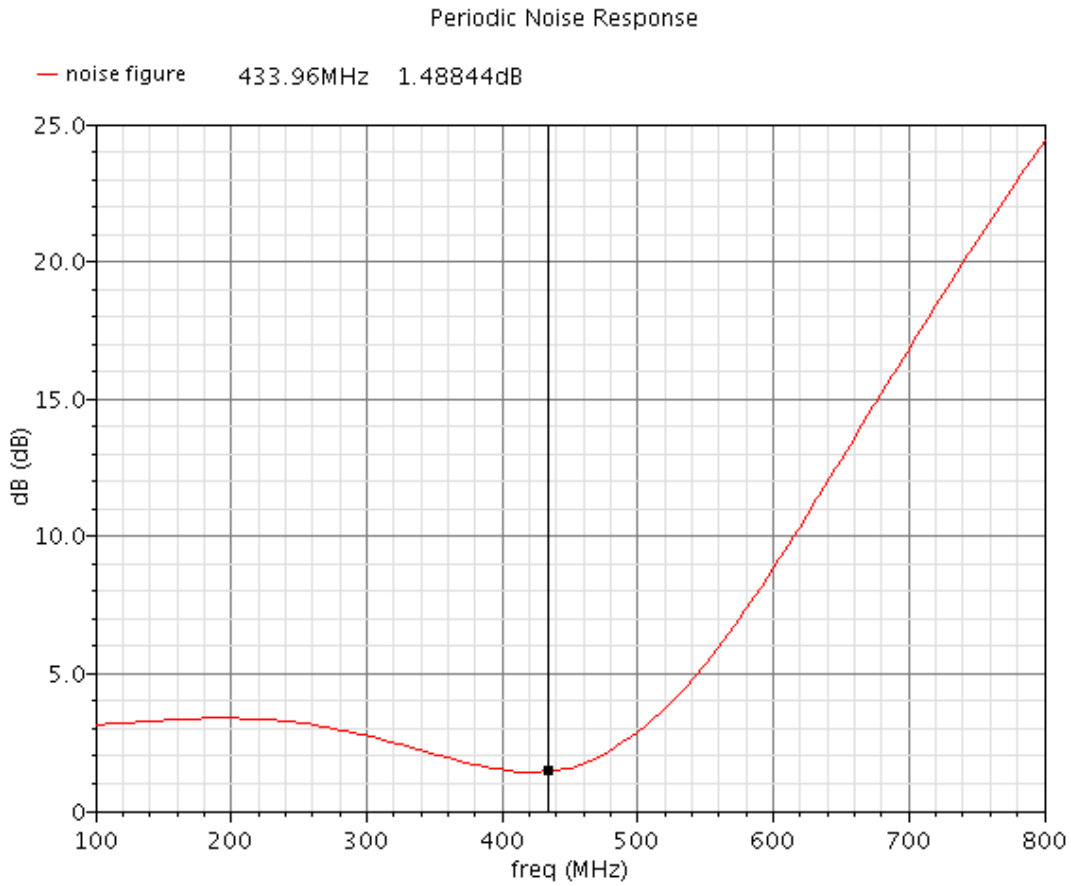

Figure 5.5. Noise figure at 25 ºC

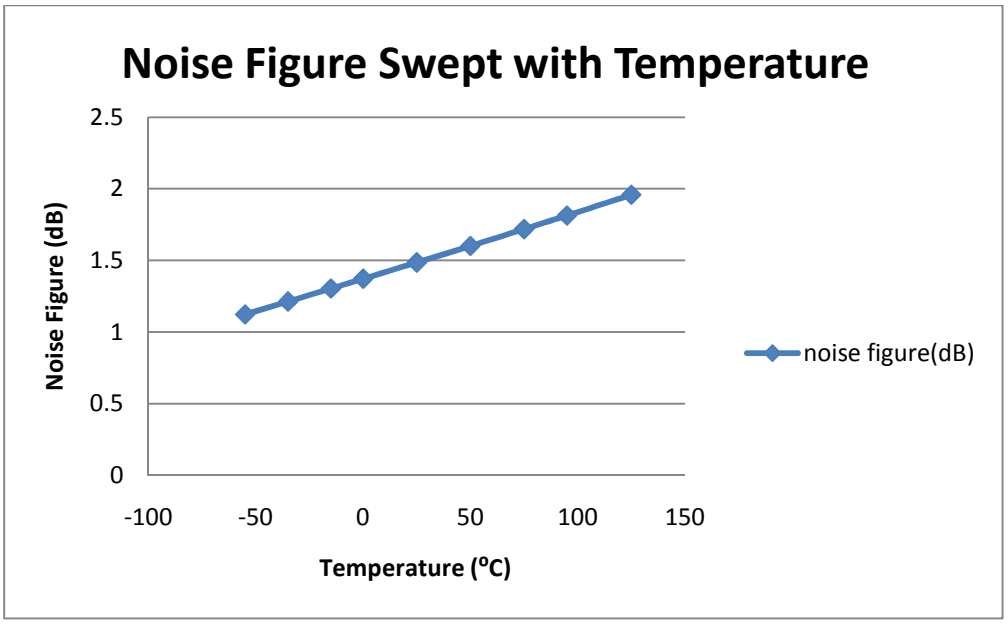

Figure 5.6. Noise figure swept with temperature

Figure 5.6 gives the simulation results of the noise figure with the temperature swept from -55 ºC to 125 ºC. The noise figure varies almost 1 dB inside the temperature range. From Chapter 1, it was shown that the dominant noise, thermal noise, is directly related to the temperature. As the temperature goes high, the noise figure increases. However, this LNA still operates with a low noise figure at the highest temperature required by system specifications.

5.4 S-Parameter Simulations

The s-parameter simulations use both PSP and PSS analysis together. Automatic sweep type is chosen with a frequency range of 100 MHz to 800 MHz. Noises have been checked for both input and output ports. The enable box is checked. The simulation is run and S-Parameters is plotted from direct plot −>main form −> pss.

According to Chapter 2, S21 should be equal to 17.2 dB (the gain of the amplifier), and the S11 and S22 measurement should be small enough (below -10 dB) to verify that the impedances have matched well. From Figure 5.7, S11 is observed to be -

20.35 dB. It can be concluded that the input impedance is matching pretty well; moreover, the input impedance matching is still acceptable from 420 MHz to 450 MHz. But the output impedance matching, where S22 equals -7.01 dB, could be better if improvement is made in the output matching network. S12 is small enough at -41.09 dB to maintain reverse signal isolation for the LNA.

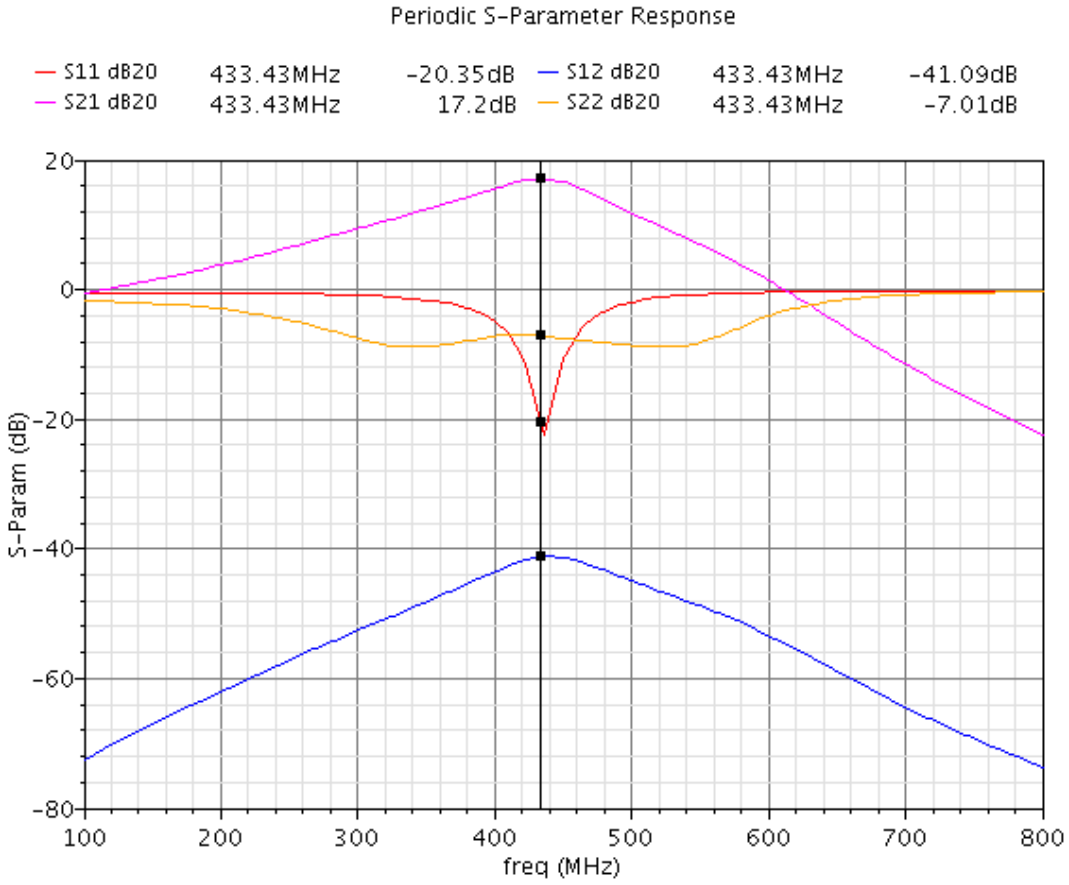

Figure 5.7. S-Parameters at 25 °C

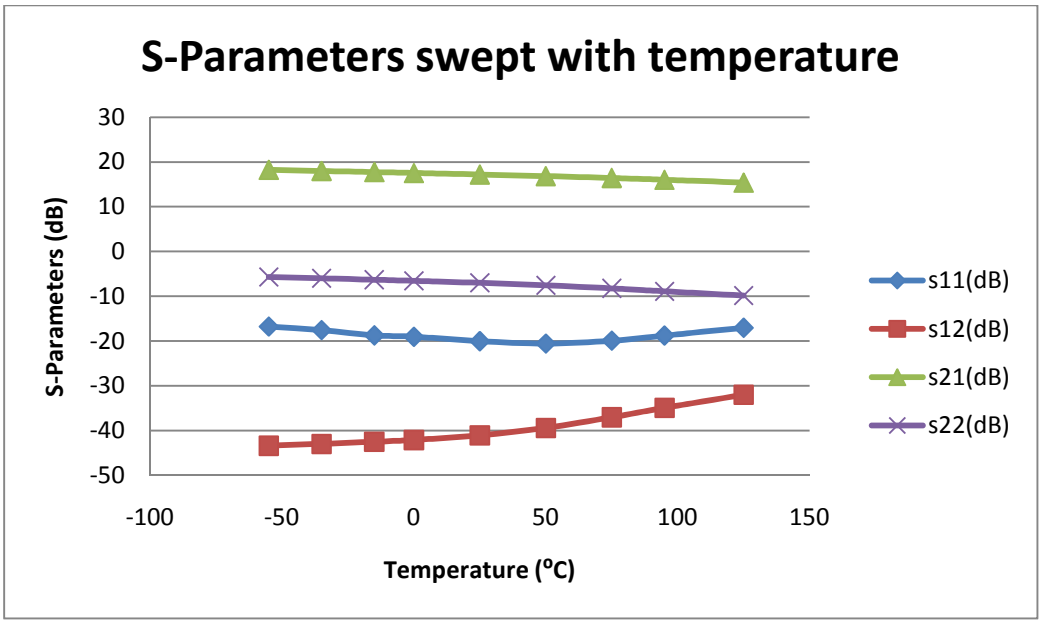

Figure 5.8. S-Parameters swept with temperature

In Figure 5.8, S-Parameters observed over a swept temperature range of -55 ºC to 125 ºC are given. The value of S21 is the LNA gain; from the voltage gain simulation, it was seen that the gain is decreasing as the temperature is increased. S11 is more flat with only a slight change over the large temperature range, so the temperature does not affect S11 a lot. Throughout the temperature range, S12 has increased by almost 10 dB, which means the reverse isolation is becoming worse, but still within the acceptable range (below -30 dB). S22 has decreased by 5 dB, which means the output impedance improves with the temperature.

5.5 Stability Simulations

The stability is measured by using both PSP and PSS analysis together as with S-Parameters simulation. The K factor and Delta (Δ) are plotted from direct plot −>main form −> pss.

Rollett's stability factor (K) is the main method used to determine the stability of an LNA. It is calculated by a set of S-Parameters for the device at the operating

frequency. The following equations about stability parameters K and $|\Delta|$ indicate the device will not oscillate and be unconditionally stable [14],

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1 \tag{5.4}$$

$$K = \frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}S_{21}|} > 1 \tag{5.5}$$

In Figure 5.9, Kf is the K factor, and is equal to 6.205 at 433MHz. B1f is Δ, and its value is 0.8104 which is smaller than 1. According to equation (5.4) and (5.5), the simulation results show that this LNA is unconditionally stable.

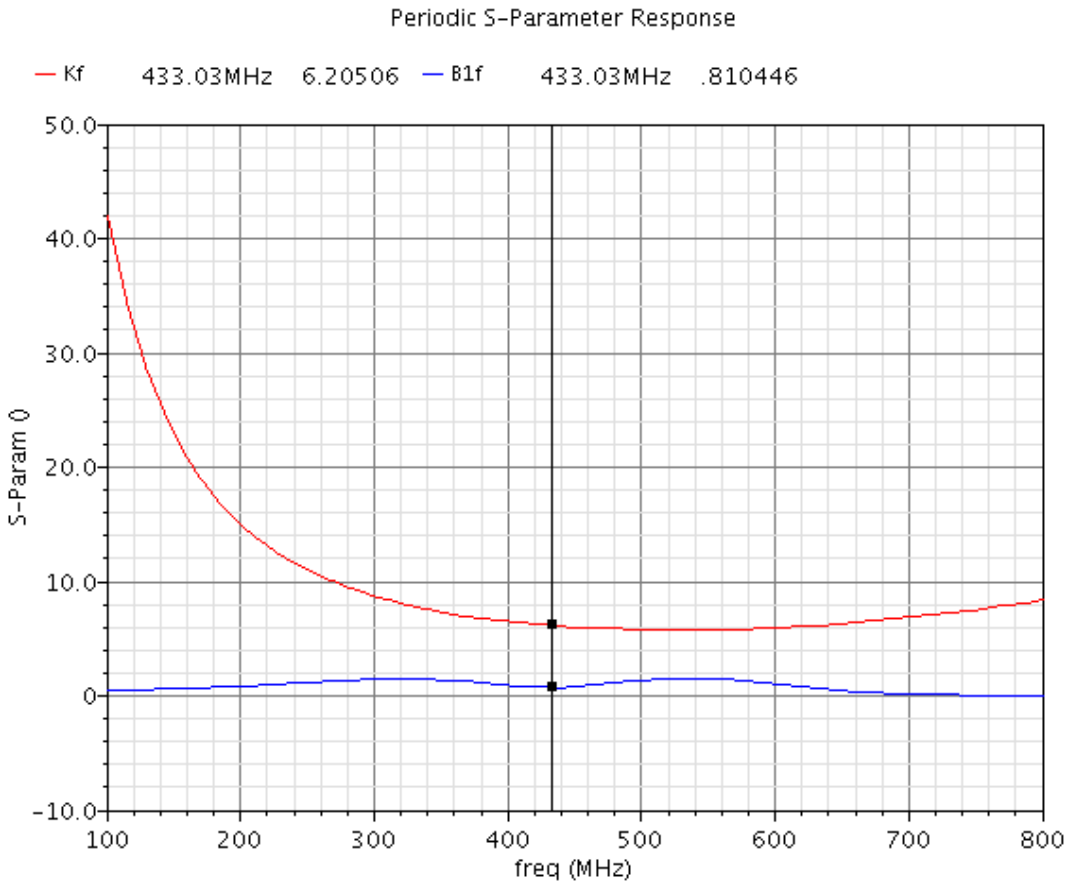

Figure 5.9. Stability at 25 °C

5.6 Linearity Simulations

The linearity of the LNA can be measured by the IP1, which is performed PSS analysis. Auto calculation for the beat frequency is used, output harmonics are chosen to be 10, and accuracy defaults are set at moderate. The amplitude was swept from -40dBm to 0 dBm, with a linear sweep type for 10 steps. The enable box is then checked. Simulation is run and the Compression Point (CP) at the first harmonic (433 MHz) with an extrapolation point at -40 dBm is plotted from direct plot −>main form −> pss.

In an amplifier, the gain will remain constant for low level input signals. But the amplifier will begin to go into saturation and its gain will decrease when a higher level input signal is applied. The IP1 (1 dB compression point) gives the power level due to a 1dB gain drop from the input small-signal value. The IP1 can be seen in Figure 5.10 is -16.8205 dB.

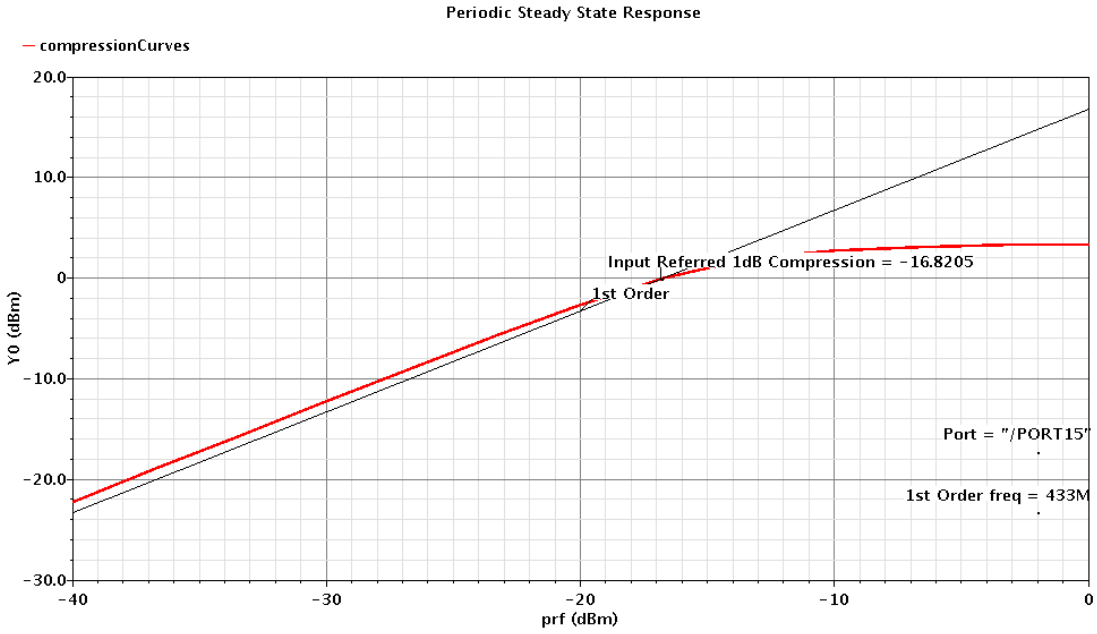

Figure 5.10. S-Parameters at 25 °C

5.7 Comparison with Other Designs

Much research has been done into CMOS LNA design. Table 5.1 gives a comparison between the major characteristics of this work with other LNA designs. All the designs operate at different frequencies and use different power supplies. In these four designs, the noise figure has a range from 2.463 dB to 1.25 dB. The design of this particular work predicts a noise figure of 1.48 dB, which is in the range of the compared designs. The voltage gain has a range from 18.36 dB to 13.5 dB. The simulated voltage gain of this work is 18.45 dB, which can be observed as a good gain for an LNA. The S-parameters show the input and output impedance matching; S21 is the same as voltage gain. Recall that if all of the S11, S22, S12 have small values, the input and output ports have been matched close to the required impedance.

Table 5.1. Comparing with other designs

Parameters		Design 1 [15]	Design 2 [16]	Design 3 [17]	Design 4 [18]	This Work	Unit
Frequency	F	5.4 G	2.4 G	881 M	433 M	433 M	Hz
Supply Power	Vdd	1	1	3	2.2-5.5	1.2	V
Process	CMOS process	0.18	0.18	-	-	0.13	Um
Noise Figure	NF	2.463	1.986	1.6	1.25	1.48	dB
Voltage Gain	VG	11.57	-	-	13.5	18.45	dB
Input Port Voltage Reflection	S11	-15.35	-22.34	-10	-	-20.35	dB
Reverse Voltage Gain	S12	-19.56	-34.34	-20	-	-41.09	dB
Forward Voltage Gain	S21	-	18.36	11.5	-	17.2	dB
Output Port Voltage Reflection	S22	-16.26	-12.92	-10	-	-7.01	dB

CHAPTER 6

Layout and Considerations

The layout of a circuit is very important for RF circuits. It will directly affect the real RF circuit performances. The fully differential LNA was laid out using Virtuoso layout editor inside the Cadence design kit.

6.1 Chip Layout

In an RF circuit, the signal traces can be more important than designed capacitors, inductors, or resistors if the traces are long. A good design of the traces will guarantee a successful RF circuit design [9]. In RF circuits, the traces should be kept much shorter than the wavelength of the input signals. In this specific design, the nominal frequency is 433 MHz and using the velocity of light, which is 3×10^8 m/s , the signal wavelength is calculated to be approximately 0.69 m. Therefore, the lengths of the traces are not a big issue in the layout design but should still be kept as short as possible.

A good trace style avoids bad performance, such as cross-talk between traces, along with mutual capacitance and inductance. The main rule of the trace is to keep it as short as possible rather than being aesthetically pleasing. The bias traces should be perpendicular to the RF signal traces. They must not be placed in parallel if at all possible. If two traces have to be parallel with each other, the distance between them should be greater than three times the width of the traces. This will greatly reduce the cross talk between them. If a trace needs to go from a large width to a small width or vice versa, the trace width should be changed smoothly in order to keep impedance variation smooth. Overall, the trace should be “as short as possible, as smooth as possible, and as perpendicular from each other as possible” [9]. It is highly recommended to use higher

level metal for the bias and signal runners, because the higher metal is thicker to reduce the resistive loss. A sufficient number of vias should be placed to connect the different metal traces, to make sure that the connection vias can carry the required current through them.

From Chapter 4, as the ratio of the transistors was relatively large and the length of the transistor was chosen to be .24 µm, multiple fingers were needed to achieve the large ratio of the transistors. For better performances, the width of a single finger should as small as possible. RF inductors need guard rings around them in order to have a good shielding, and the ground plane of the inductor was connected to metal M1. The distance between the traces and the inductor was kept at least 10 µm in order to meet DRC requirements.

Table 6.1. Fully differential LNA Pin Map

I/O	Access Layer	Pad Location
VDD	E1	Bottom-right
Vbias	E1	Bottom-middle
GND	E1	Bottom-left
GND	MA	Right-top
GND	E1/MG	Right-middle
RF OUTPUT1	MA	Right-top
RF OUTPUT2	MA	Right-top
RF INPUT1	MA	Right-middle
RF INPUT2	MA	Right-middle

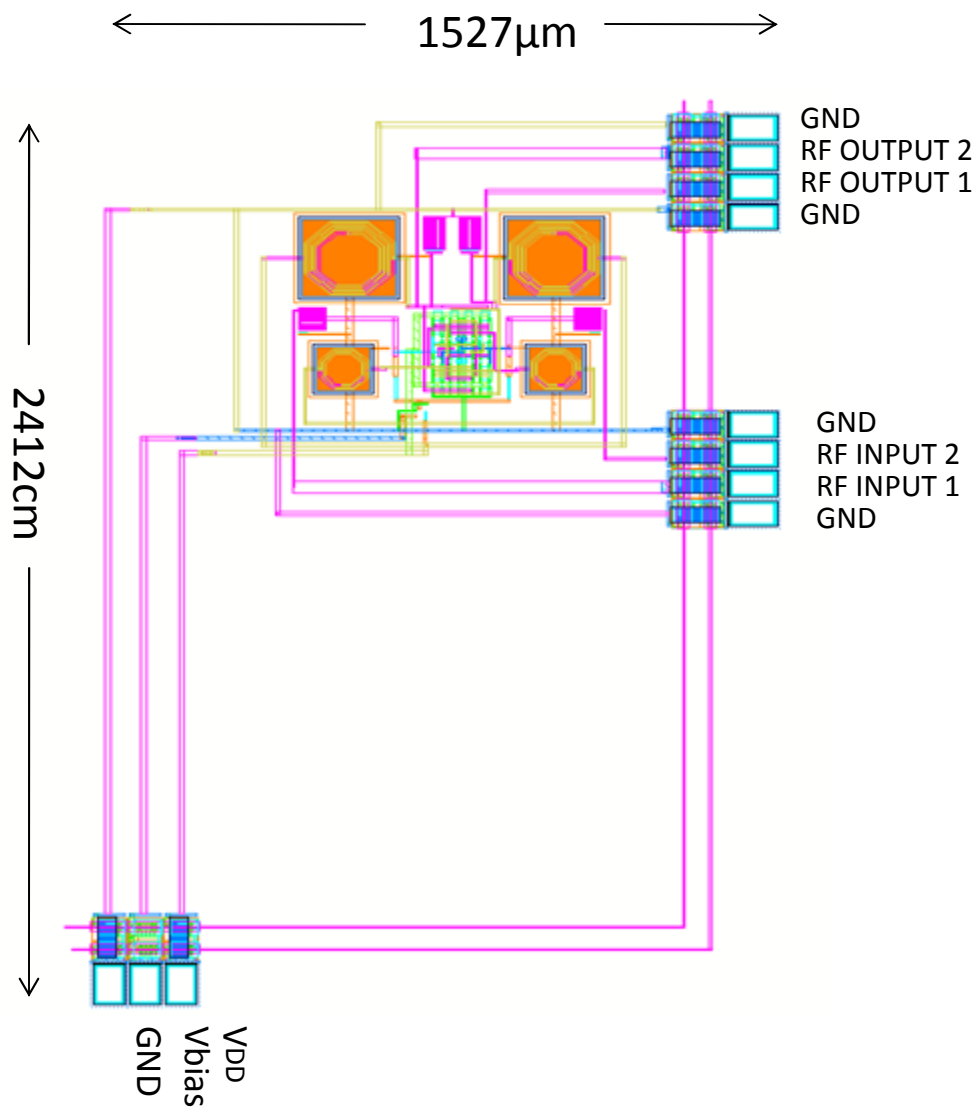

Figure 6.1. Fully differential LNA layout with pads

Due to limitation of chip space and the length of the traces to the pads of the other circuits, Figure 6.1 shows the best pads possible connection to fit the LNA in this chip. The blank corner was occupied by a circuit which required shorter path to pads. However, the RF traces are shorter than the DC biasing.

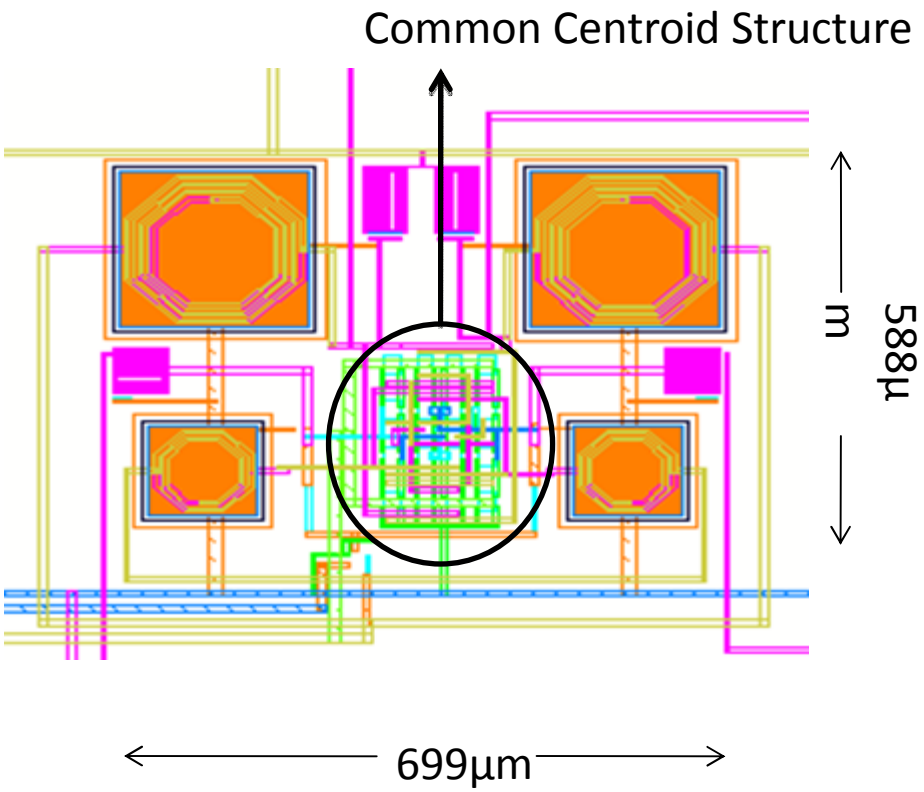

Figure 6.2. Fully differential LNA without pads

According to the equations in Chapter 4, it can be seen that the higher frequency the smaller the W/L ratio. As 433 MHz frequency is a relatively low frequency in the RF range, the W/L ratio of the transistors are large. The common centroid method was implemented in this layout design [19]. It was used to make the circuit immune to the cross-chip gradient effect that occurs when current goes through the transistors. However, it requires take more space in the circuit layout.

The transistor common centroid layout was completed with the following rules [19]:

1. Coincidence: The centroids with matched devices such as transistors should be coinciding as much as possible.
2. Symmetry: The array should be symmetric in the X axes and Y axes.

3. Dispersion: The segments of each device should be distributed uniformly through the layout.
4. Compactness: The array should be placed as compact as possible, and it is better to have the shape of the structure like square.

Since M1, M1', M2 and M2' are identical to each other in the circuit, each of them has been divided by four as in the shading part of Figure 6.3. The common centroid structure applied to these four transistors in the amplifier stage in order to fulfill the rules above is given in Figure 6.4 below.

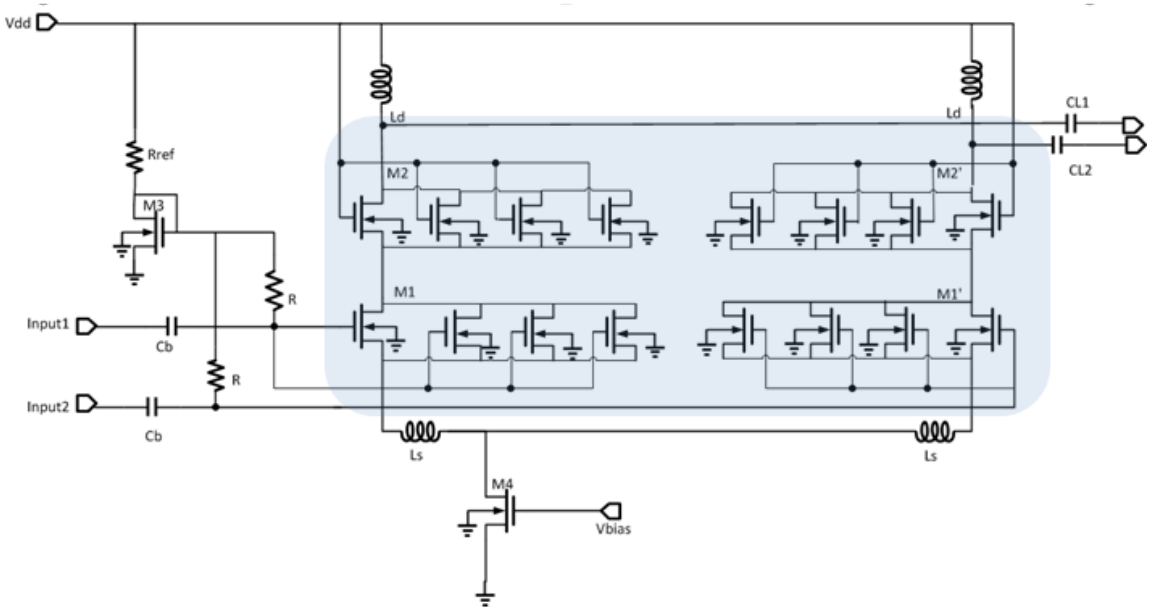

Figure 6.3. Fully differential LNA with transistors split

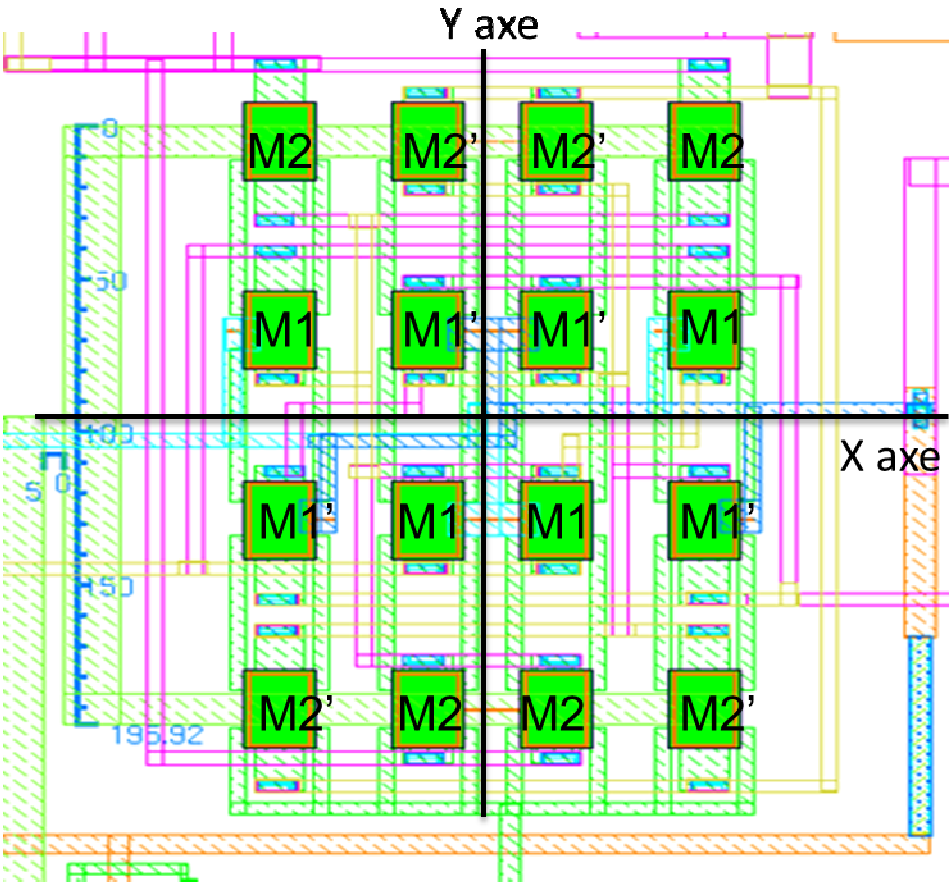

Figure 6.4. Common centroid structure layout for transistors

Figure 6.4 shows the uniform distribution of the split transistors. All of the transistors are symmetric with both X and Y. The arrays have been placed as close as possible within the consideration of the trace's metal width and the distance between the traces. Offset voltage can be introduced in the differential LNA due to the mismatching of the transistors, and the ratio of the feeding drain current and the bias voltage to the amplifier will be affected by the mismatching as well. Using common centroid techniques should minimize these effects.

CHAPTER 7

PCB Design and Testing Plan

This chapter will present the design of the testing board and test plan for an LNA, including planning ahead for the bonding diagram, and setting up the measuring equipment and the connection cables.

7.1 Package Information

The fully differential LNA was bonded and packaged at Metal Oxide Semiconductor Implementation Service (MOSIS). The proper package was chosen according to the cavity capacity, number of pins and temperature range. A 48 pin QFN package was selected for minimal parasitics, capable of handling temperatures up to 125 ℃. The selected package cavity size was 5200 µm×5200 µm, the die size was 4110 µm×4110 µm, the minimum pad size was 100 µm×62 µm, and the minimum pad pitch was 80 µm. The bonding diagram is shown in Figure 7.1. The LNA circuit was placed in the right bottom corner. Table 7.1 gives the detailed package connections.

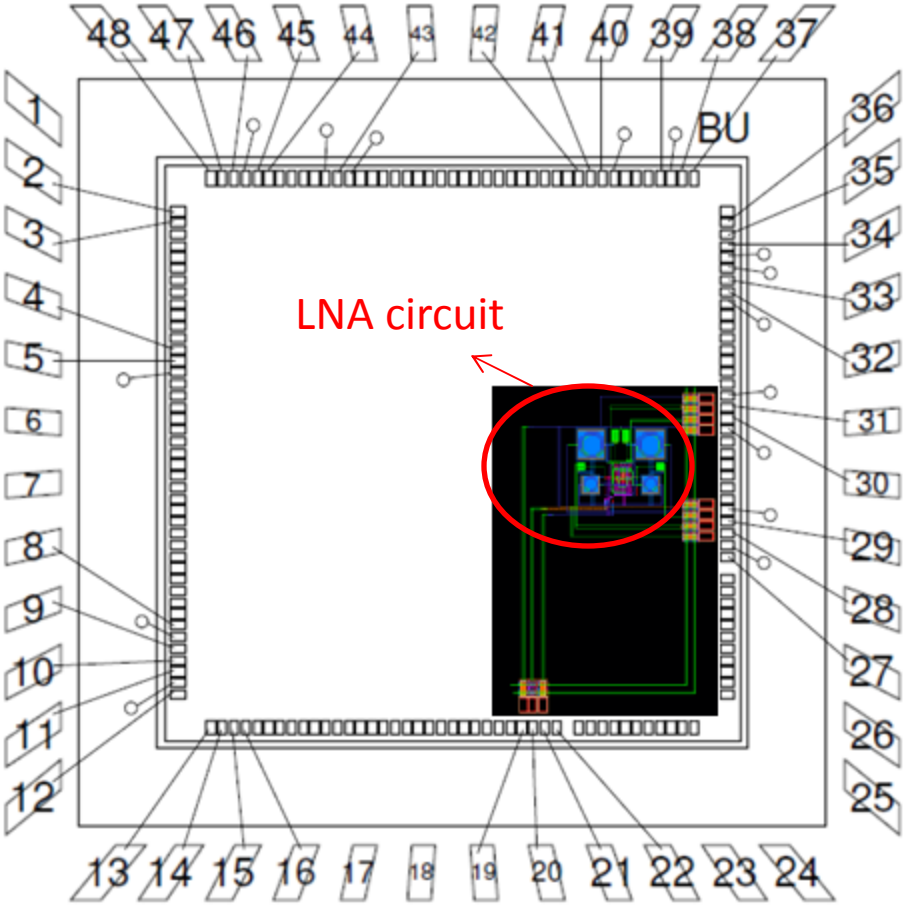

Figure 7.1. Bonding diagram of the chip

Table 7.1. Bonding diagram pin out information

Pin number	Corresponding signal
31	RF OUTPUT2
30	RF OUTPUT1
29	RF INPUT2
28	RF INPUT1
27	PADS POWER SUPPLY
22	PADS GND
21	VDD
20	Vbias
19	GND

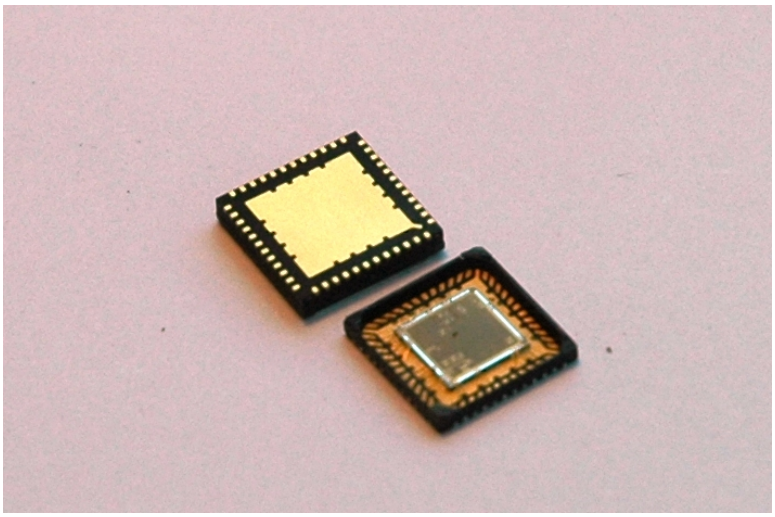

Figure 7.2. The manufactured chip in QFN package

7.2 PCB Design for RF Circuit

Since the PCB was operating at Radio Frequency, a 4-layer board design was used that "allows distributed RF decoupling of a DC power plane sandwiched between two layers of predominantly ground plane [20]" and maintains a continuous ground plane. On an RF circuit board, all the RF signals, either from the input port or output port, need a common RF ground to be the reference point. The common ground makes sure all the points are equipotential [9]. Using a 4-layer board allows the dimensions of a microstrip line matched to 50 Ω to be a more manageable size.

In this design, the PCB has two ground plane layers, one power plane layer and one circuit trace layer. "The metallic runner with high conductivity either on the IC substrate or on the PCB in the RF range is a micro strip line" [9]. In order to reduce the distributed capacitance, inductance and resistance, the metallic trace's width and shape should be well designed. By using all the information such as standard layer stack, copper weights, dielectric constant, material data, and thickness of core from the board

manufacture, the width of a microstrip line matched to 50 Ω can be achieved easily. The bias traces should be wide enough to decrease the resistance from the path.

For an RF signal path, a 45˚ arc is used if a bend is needed; this will decrease the losses and spurious emissions due to the impedance mismatch. Since this is a fully differential circuit, it is important to make the differential pair traces as identical as possible. Otherwise, there will be voltage offset between the differential signals. The RF trace and bias trace should be perpendicular to each other or far away from each other. The differential input signals should be perpendicular with the differential output signals in order to avoid the over cross signals between them.

The connection between an RF component to ground should be as short as possible, and in many cases two or three parallel vias were needed to the ground plane in order to decrease the impedance.

Almost all of the components selected were surface mount type, because for an RF circuit, the smaller size and shorter trace will decrease the parasitic capacitance and resistance. The components were selected to operate within the temperature range from -55 ºC to 125 ºC, since this LNA will be tested over that range.

Banana jacks were used to connect to the power supply, bias voltage and ground.

50 Ω impedance SMA connectors were used in this design for RF signals interfaces, due to their small size, wide frequency range and high reliability.

7.2.1 Regulator Setup for Bias Voltage

For this PCB, a 1.2 V power supply and 0.6 V bias voltage were needed. Regulators are used to main the constant voltage level in this PCB design. The TPS71701

voltage regulator was used to implement 1.2 V VDD. The LT3021 was used to implement the 0.6 V bias voltage, which has a similar structure as Figure 7.3.

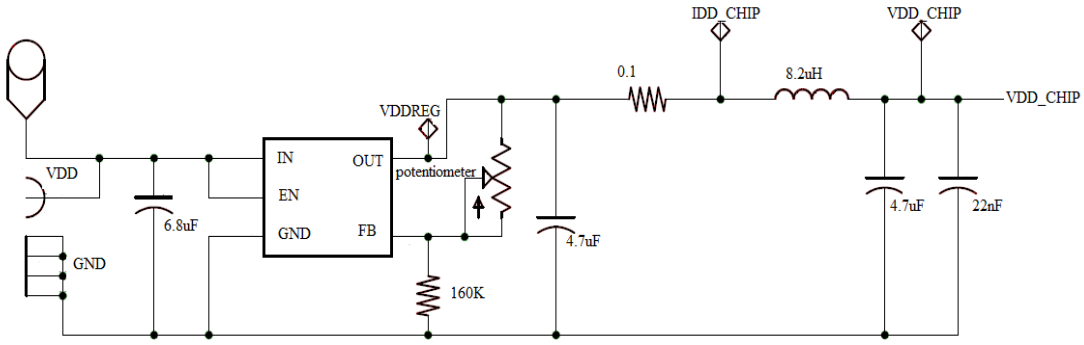

Figure 7.3. Using TPS71701 to setup for 0.6 bias voltage

A 100 kΩ potentiometer was used to adjust to the required voltage. Using the equation on the datasheet of the TPS71701 regulator, the resistor was chosen as 160 kΩ to make sure the regulator was stable. The 6.8 µF input capacitor improved the source impedance and further ensured the stability. The 0.1 Ω shunt resistor was included so the current going into the chip can be calculated by the voltage drop on the 0.1 Ω resistor using a multimeter.

7.2.2 Impedance Matching Network

According to Chapter 2 (impedance matching) and Chapter 4 (calculation of the matching inductor) the sizes of the on-chip inductors were too large to be implemented on the chip. With all the considerations of the chip size and flexibility of adjustability, off-chip impedance matching was implemented in this design.

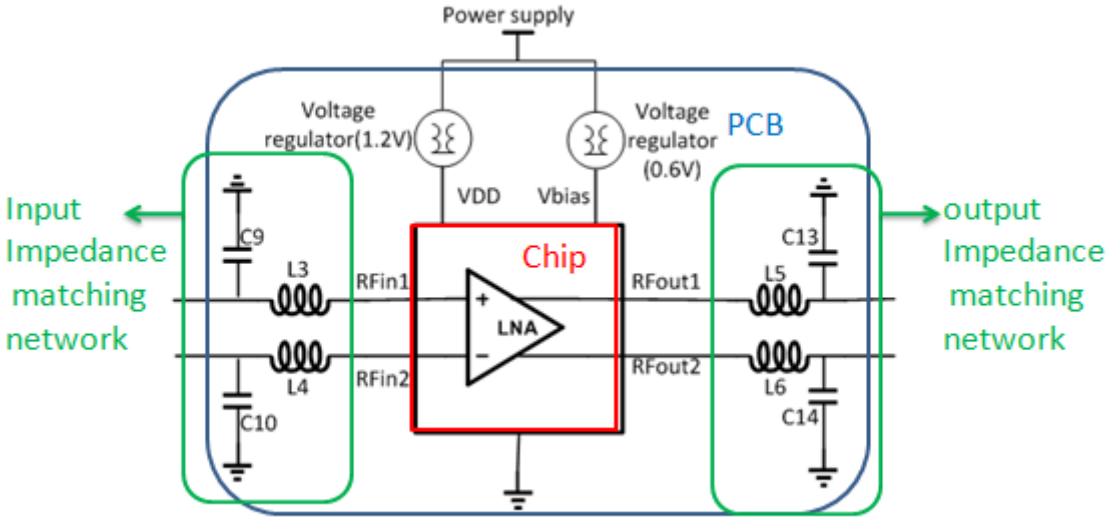

Figure 7.4. Impedance matching networks

Following all the manufacturers' design rules, the schematic of the LNA testing board was designed in the EAGLE tool as shown in Figure 7.5 and Table 7.2.

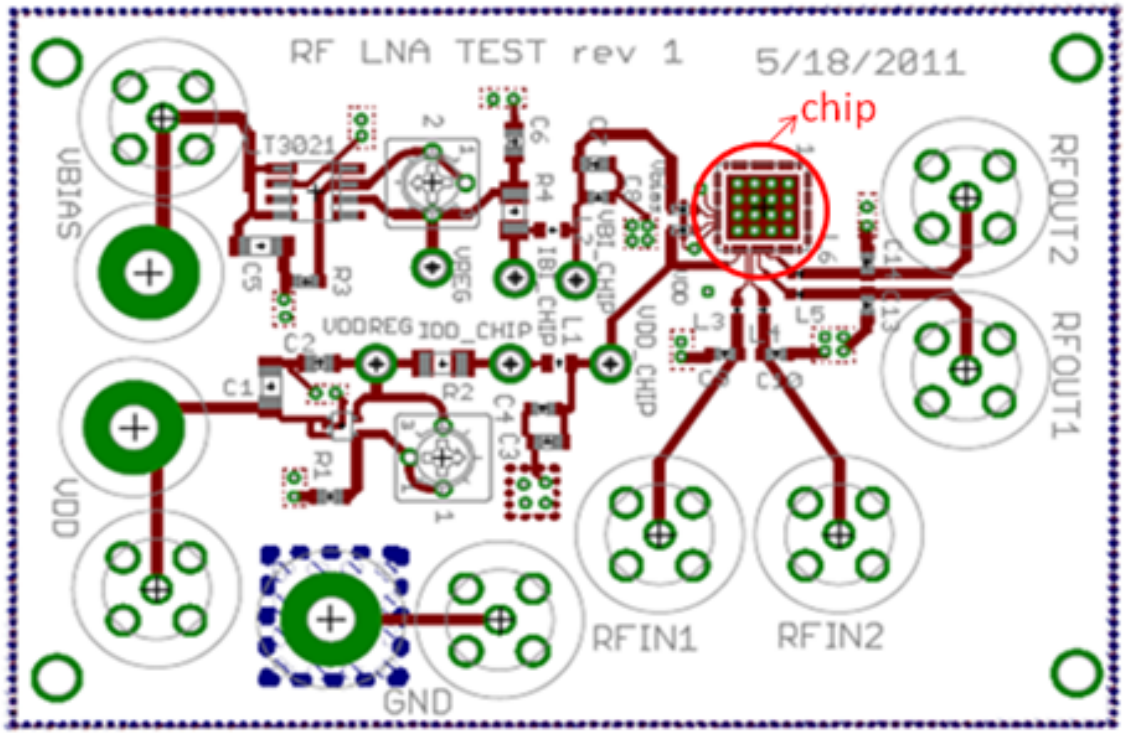

Figure 7.5. PCB for RF LNA testing

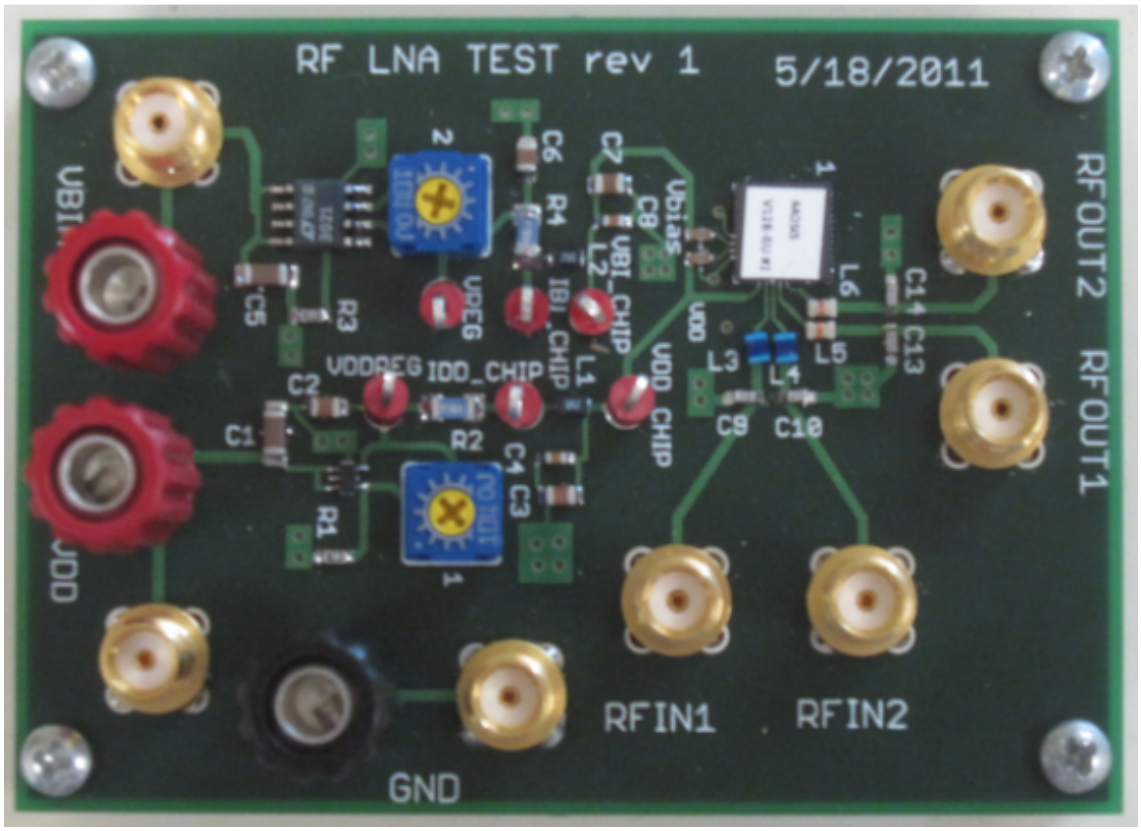

Figure 7.6. Test board for LNA

Table 7.2. Components names and values

Name	Components	Value
C1,C5	Capacitor	6.8 µF
C2,C3,C6,C7	Capacitor	4.7 µF
C4,C8	Capacitor	22 nF
C9,C10	Capacitor	10 pF
CAPTH C11, CAPTH C12	Capacitor	470 nF
C13,C14	Capacitor	4.7 pF
L1,L2	Inductor	8.2 nH
L3,L4	Inductor	43 nH
L5,L6	Inductor	22 nH
R1	Resistor	160 kΩ
R3	Resistor	20 kΩ
R2,R4	Resistor	0.1 Ω

7.3 Balun Board

Baluns are transformers which can convert single input (unbalanced signal) to differential outputs (balanced signals) with the same amplitude but 180˚ phase shift from each other. A balun can also combine a differential signal into a single ended signal. There are three terminals on the balun. Looking into the three terminals, all three terminals' impedance should be equal to 50 Ω. Since the baluns chosen did not have the desired temperature range from -55 ºC to 125 ºC, they were designed on a separate PCB. In this way, the LNA circuit can be tested in the chamber throughout the temperature range. Because the baluns were directly connected to the RF signals, SMA connectors were necessary for all the inputs and outputs on the balun board [3].

Figure 7.7. Separate balun board

In Figure 7.7, the left balun was used since this one had better observed performances than the smaller one, such as less intersection loss.

Table 7.3. Balun board connections

PORT	NAME
UNBALANCED	RF_LNA
BALANCED	RF_LNA+
BALANCED	RF_LNA-

7.4 Test Setup

7.4.1 Test Equipment

The following table includes all the test equipment that was used in the testing of the design. The operational frequency range for all RF source and measurement equipment must include 433 MHz.

Table 7.4. Testing equipment

Equipment Model	Equipment description
Tektronix AWG7102	Arbitrary Waveform Generator 10GS/s
Tektronix MSO4104	Mixed Signal Oscilloscope 1GHz 5GS/s
Fluke 45	Dual Display Multimeter
Hewlett Packard 8563A	Spectrum Analyzer 9KHz-22GHz
Hewlett Packard E3631A	Triple output DC power supply 0-6V, 5A/0 ±25V,1A
Agilent E8361A	Two-Port Network Analyzer 10MHz to 67GHz
Delta 9039	Chamber for Temperature testing
NC346 Series	Noise source less than 1.15:1 from 10MHz- 5GHz for units with 5-7 dB or 14-17 dB ENR
Connection Cables	Male SMA to male SMA cables, male SMA to BNC cables, and the connector's resistance matched to 50 Ω

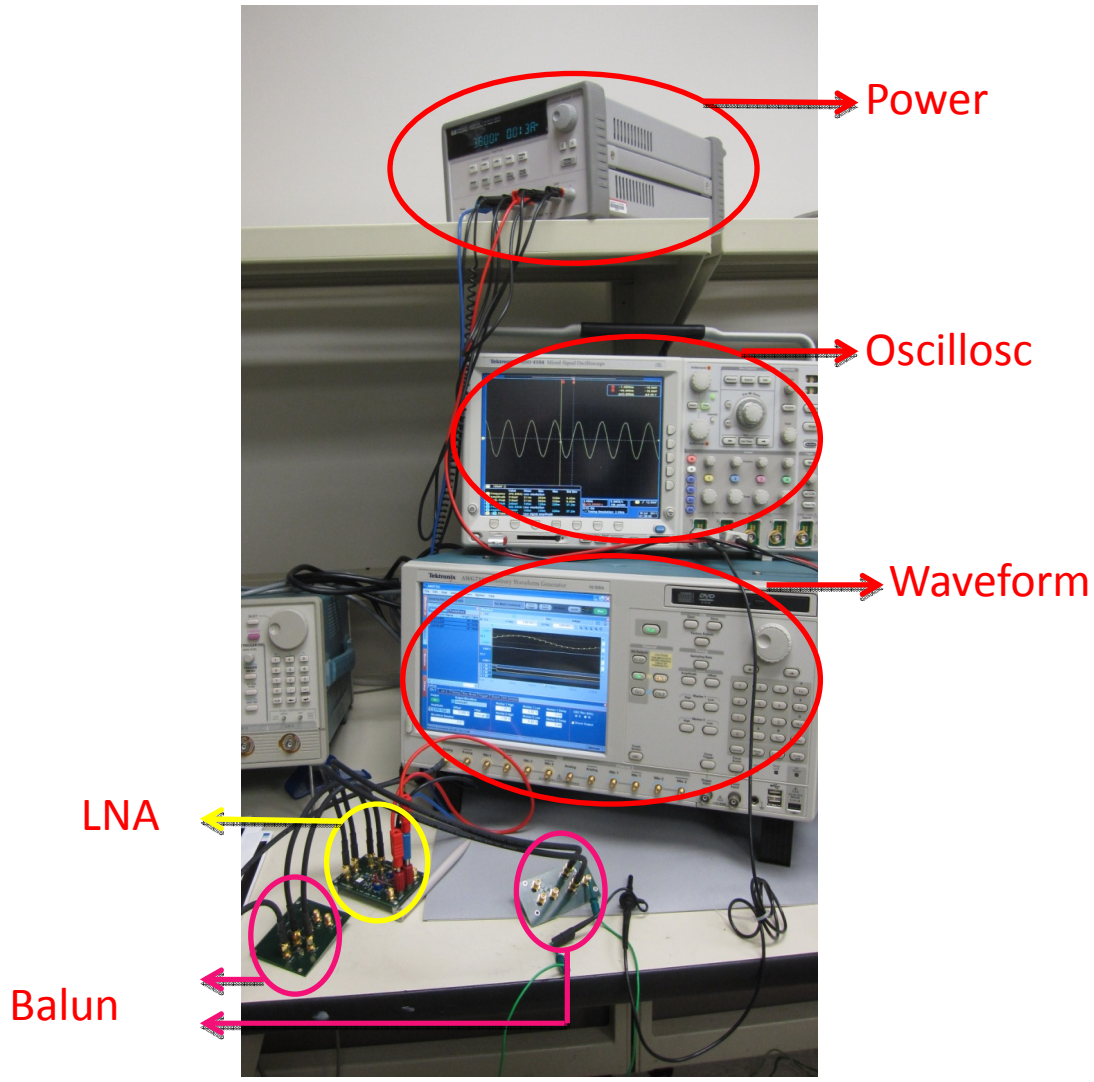

Figure 7.8. Testing setup for differential LNA

7.4.2 Baluns Setup

Because a network analyzer was very sensitive to a small DC level voltage, baluns were used to block the DC level voltage. In order to test the s-parameters of a fully differential LNA, a single input and a single output were needed to connect to the Network Analyzer, so the balun boards were needed for the differential pair to a single-ended conversion as in Figure 7.9.

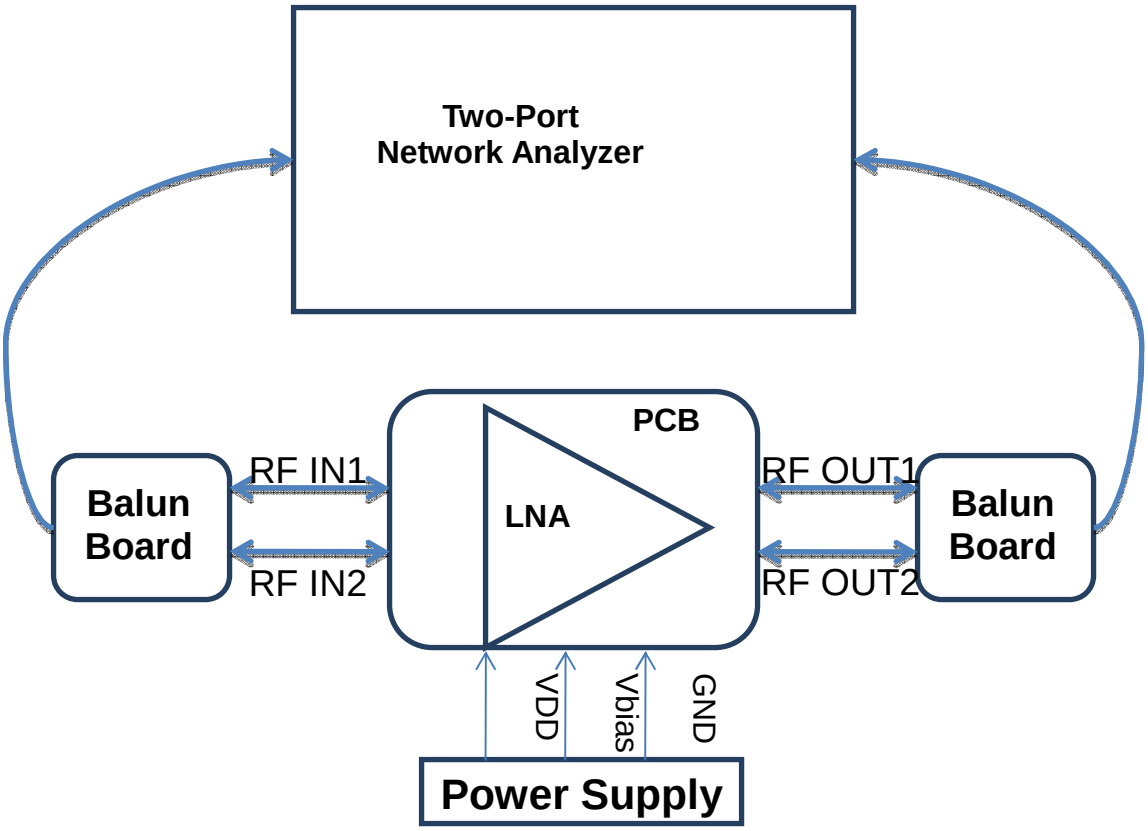

Figure 7.9. Testing setup using network analyzer

7.5 Test Results

7.5.1 Balun Performance

The baluns were connected as in Figure 7.10:

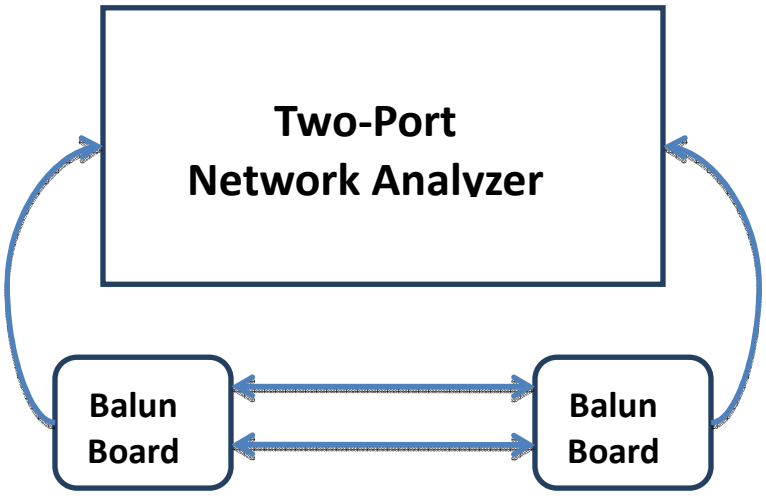

Figure 7.10. Balun board connection to network analyzer

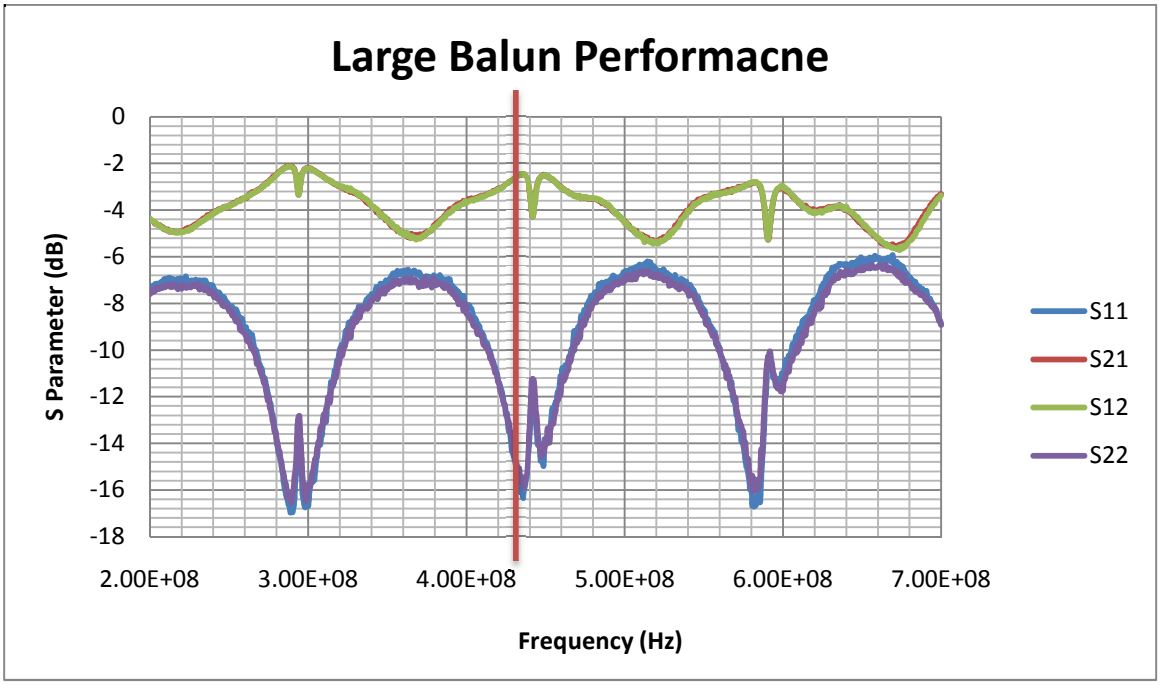

Figure 7.11. S-Parameter measurement for two balun boards

In Figure 7.11, the red line in the graph is 433 MHz. It can be seen that the observed S11 overlaps with S22, and S21 overlaps S12. For ideal baluns, there is no reverse gain and very good isolation between input and output signals, which means that S12 and S21 should be equal to 0 dB, and S11 and S22 equal to infinity. The real baluns, used in this design are not ideal, and the two measured baluns had S12 and S21 equal to -2.54dB, and S11, S22 equal to -15.1dB. More simulations with modeled baluns, which are used to match the real balun performance, have been performed in Chapter 8.

7.5.2 LNA S-Parameter Measurements

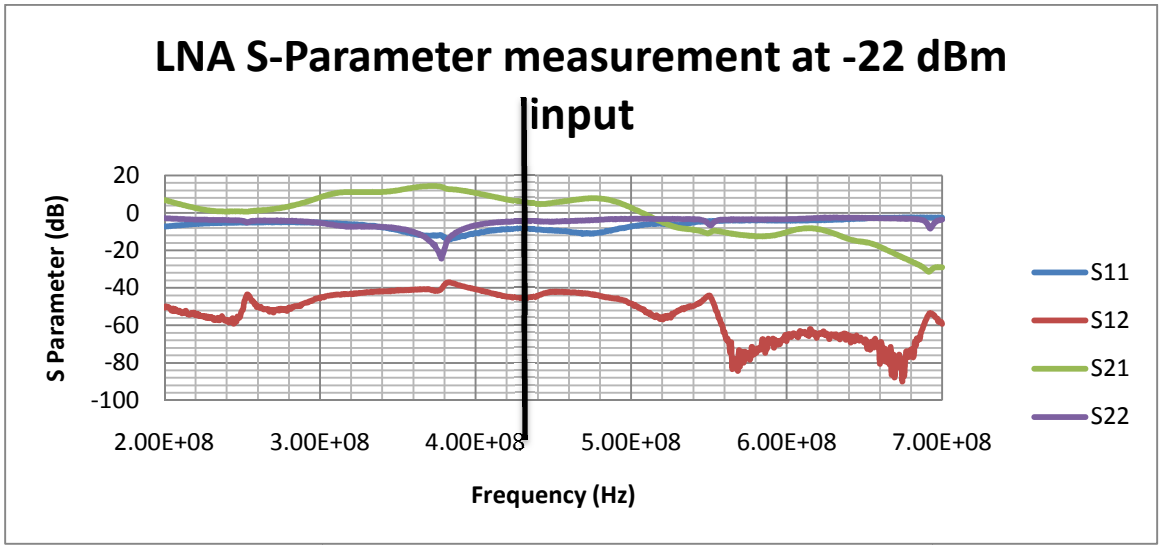

Figure 7.12. S-Parameter measurement at -22 dBm input

In Figure 7.12, S11 and S22 show that the impedance of the LNA matches well around 370 MHz; from the data analysis, S21 has a gain of 14.255 dB at 373 MHz, and S12 is observed to be small enough to keep the reverse signal isolation for the LNA. The black line in the figure marks the frequency of 433 MHz. Overall, the impedance does not match well at 433 MHz. This may be caused by the solder used, which may have a parasitic capacitance that affect the impedance matching. Decreasing the capacitor value at the output impedance network might improve the performance. More investigation and illustration of the observed shift in S21 (LNA voltage gain), is included in Chapter 8.

7.5.3 Voltage Gain Measurements

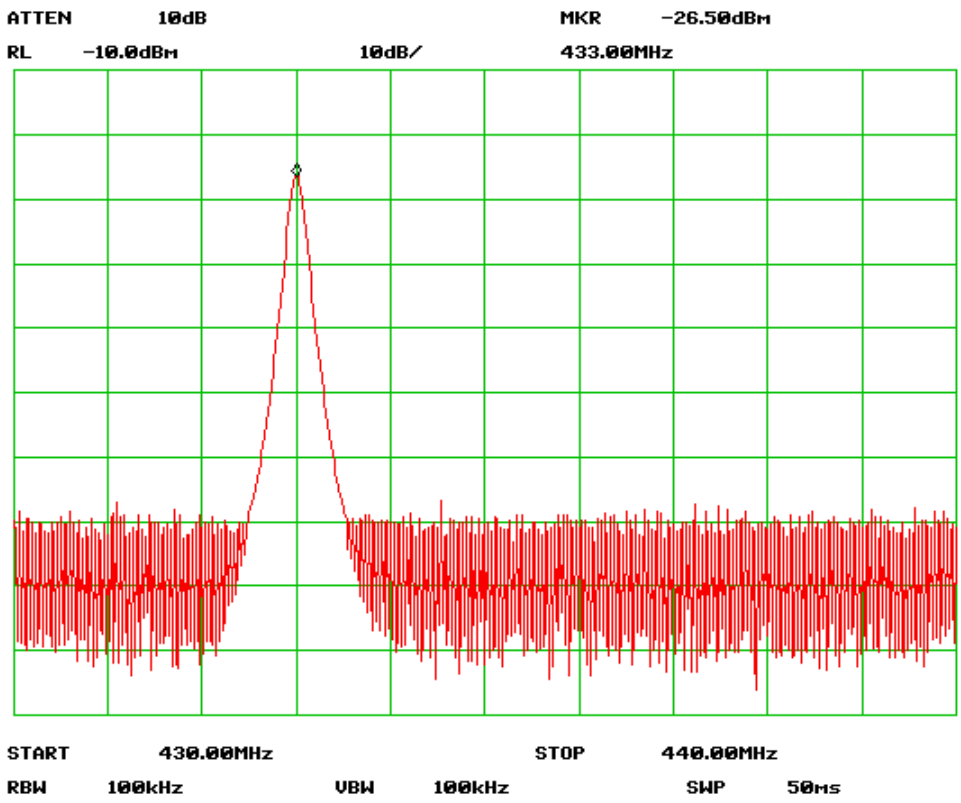

Figure 7.13. Output from two baluns at 433 MHz

Voltage gain measurements of the balun boards were performed using an RF signal generator providing an input signal with a magnitude of 50 mVpp (which is -22 dBm). To characterize the balun loss, the input balun was directly connected to the output balun, and the single-ended output from the output balun connected to the Spectrum Analyzer. The captured image shows the balun boards have a 4.5 dB gain loss at 433MHz.

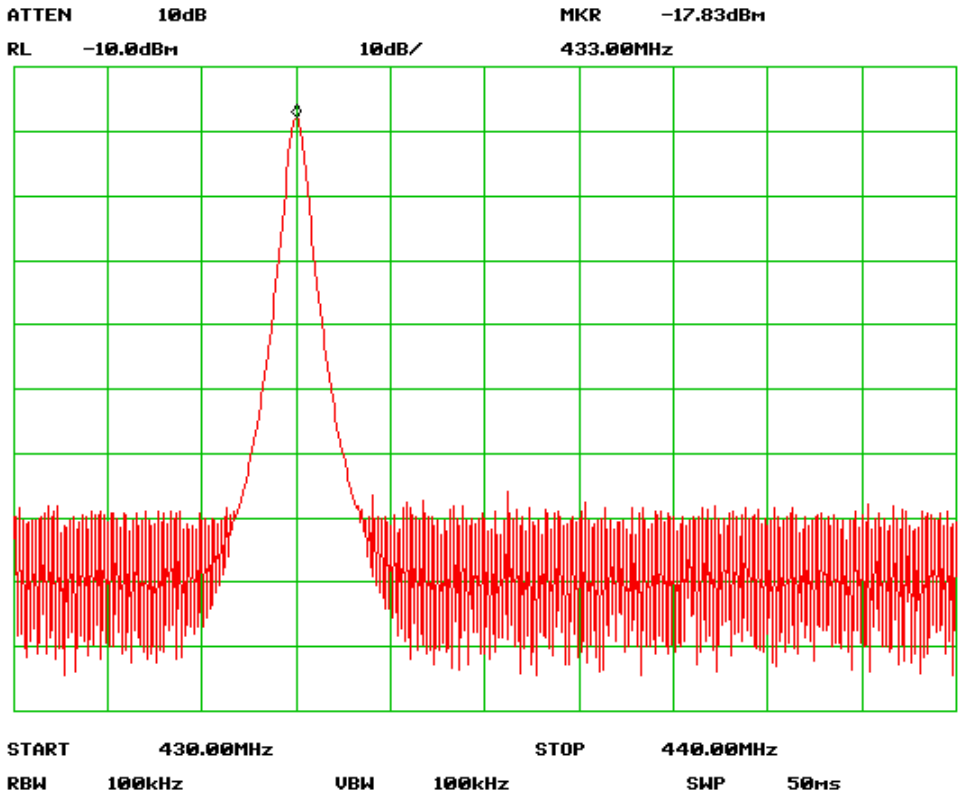

Figure 7.14. LNA testing with two baluns at 433 MHz

Again using a 50 mVpp (-22 dBm) input signal at 433MHz, voltage gain measurement of the LNA was performed using both the input balun board and the output balun board connecting to the LNA PCB. The observed output was -17.93 dBm (81.2 mVpp) (Figure 7.14). If the 4.5 dBm loss from the two balun boards is accounted for, the actual output power can be calculated to -13.33 dBm (136.3 mVpp).

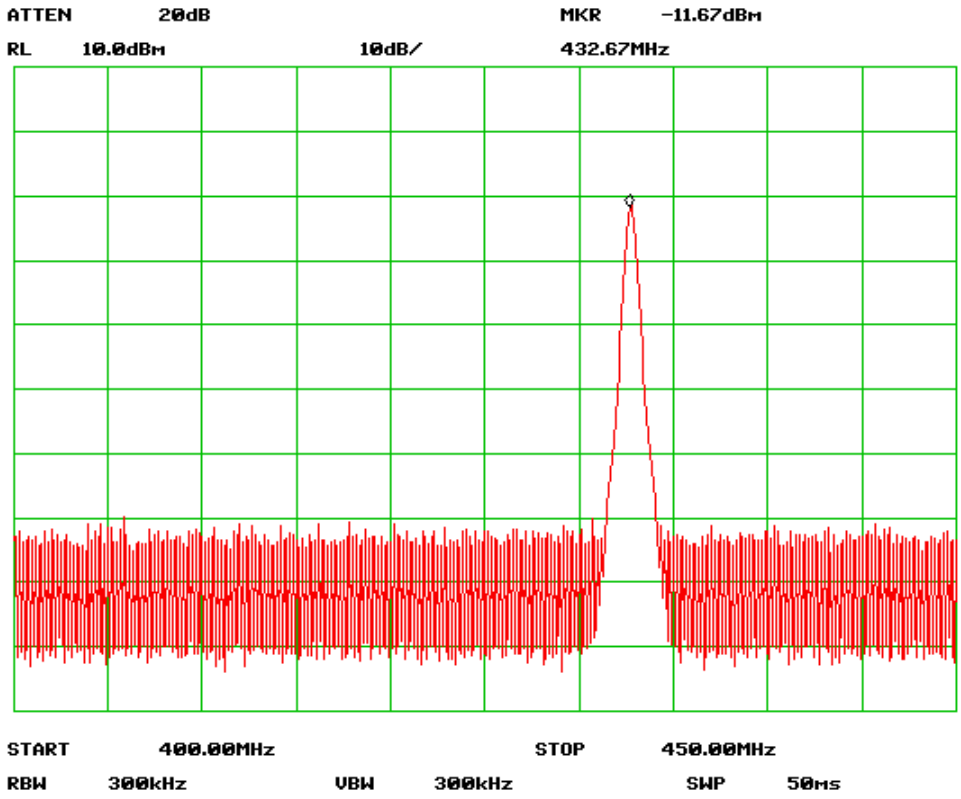

Figure 7.15. LNA testing with only output balun at 433MHz

Next, a differential source with 50 mVpp (two outputs 180˚ out phase with each other) was used. In this configuration, only the output balun was used to combine the differential signals to single-ended for connection to the spectrum analyzer. The observed output in this configuration was -11.67 dBm (165 mVpp). The two signal sources from the generator give out the exact 50 mVpp differential signals to the LNA, and there is no balun board loss during the testing, which made the output power higher than Figure 7.14.

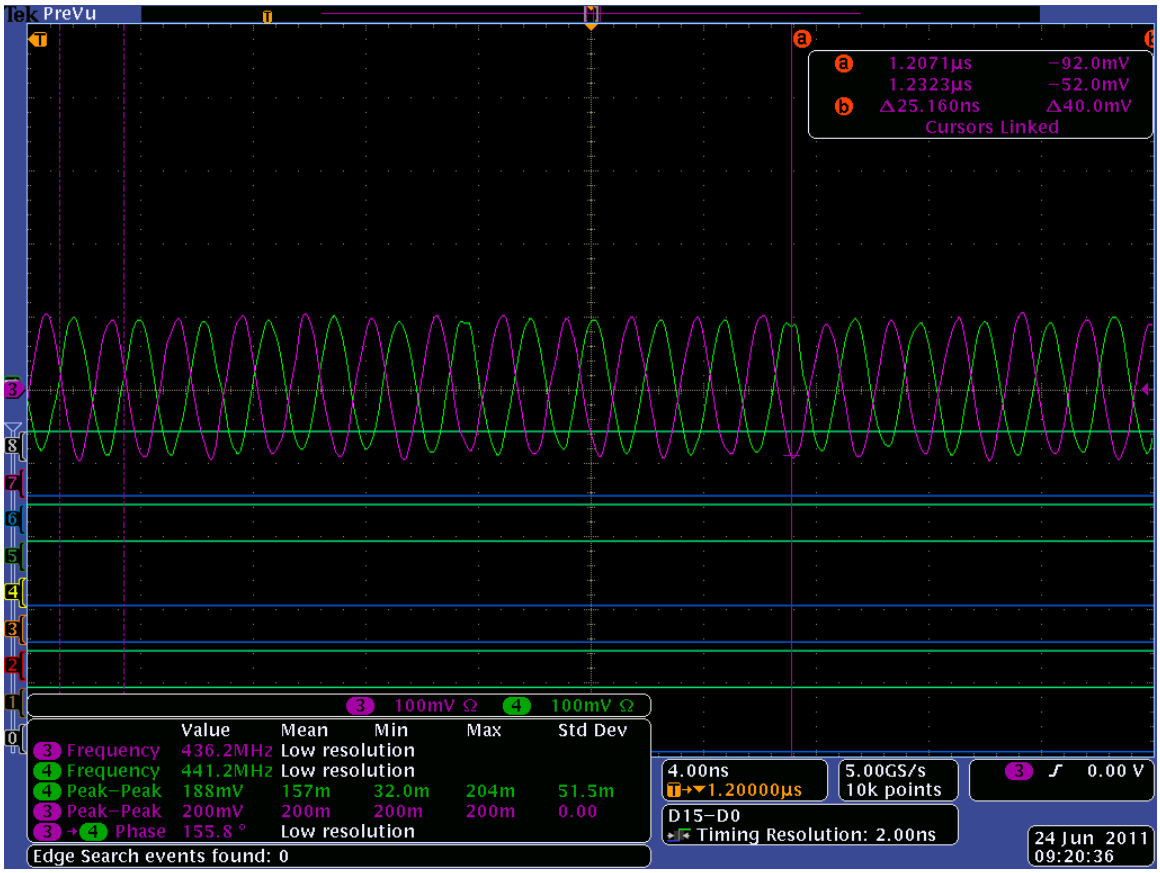

Figure 7.16. Differential outputs of LNA with 50mVpp input at 433MHz

Figure 7.16 gives the measured output signals of the LNA from the Oscilloscope. By using only output baluns during the test, the differential output signals were observed to be 155.8˚ out of phase with each other, with a peak-to-peak value of around 200 mV. Therefore, the observed gain was approximately 20log(200 mV/50 mV) = 12.04 dB.

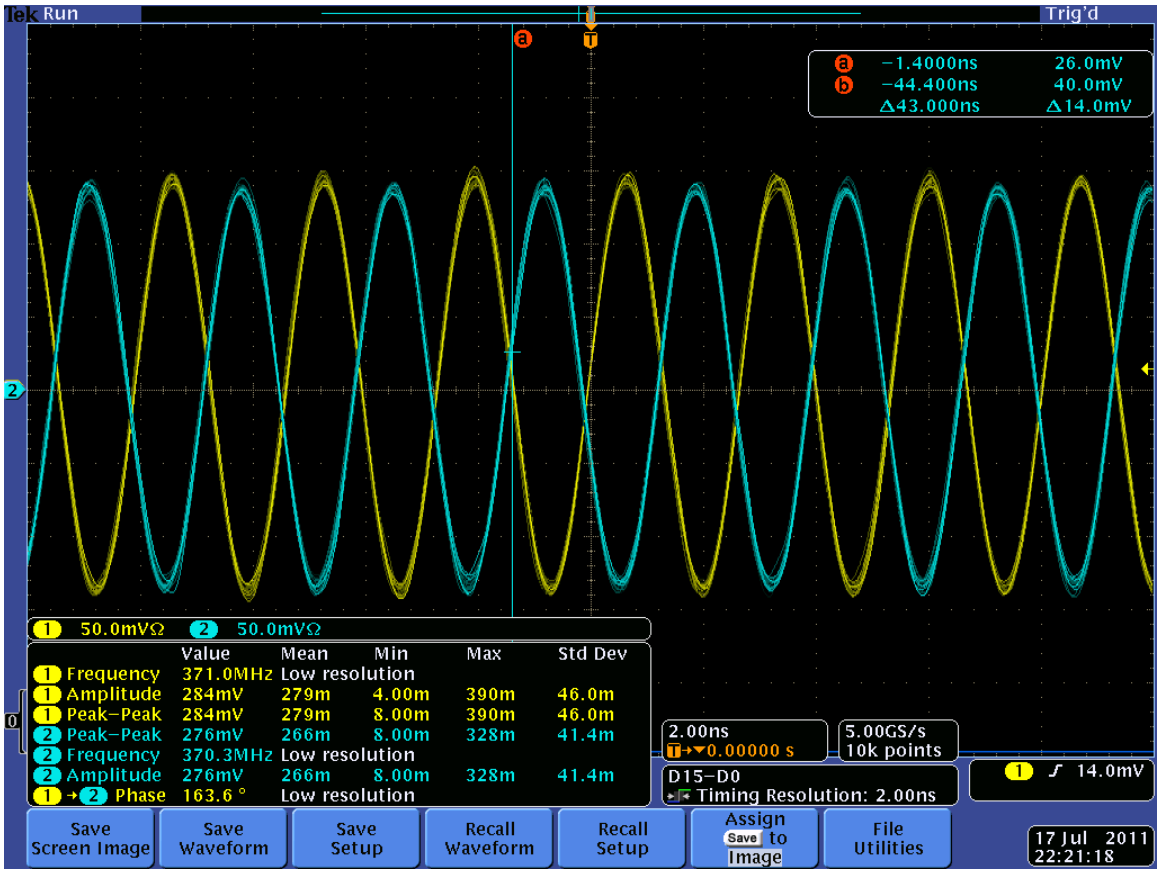

Figure 7.17. Differential outputs of LNA with 50mVpp input at 371MHz

According to the measurement from the s-parameters and simulation, the maximum gain frequency of the LNA was observed at ~370 MHz. In Figure 7.17, we can see the Vpp of the differential outputs observed at 280 mV at this frequency, and they are ~163.6˚ out phase with each other. Therefore, the measured gain was around 20log(280 mV/50 mV) = 14.96 dB. It can be seen that this LNA has a larger gain at 370MHz than 433MHz just as was observed in simulation.

7.5.4 Linearity Measurements

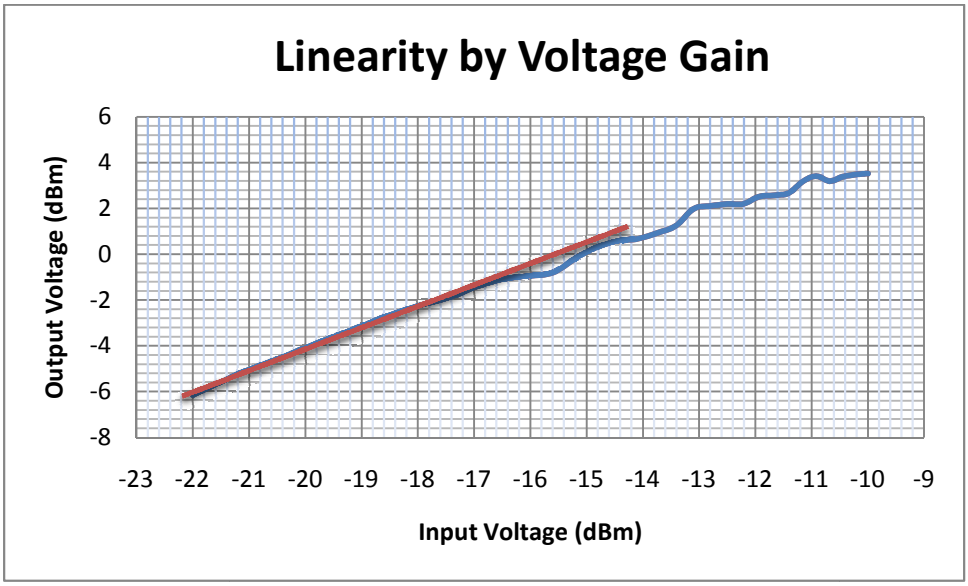

Figure 7.18. Linearity measurement with voltage gain at 370 MHz

In Figure 7.18, output voltages were recorded according to the different input voltages at 370 MHz; the measurement was being done with both input and output baluns connected in the circuit. The red line is the linear trend line of the measurements. From this figure, the LNA has good linearity if the input voltages are smaller than -16.5 dBm. And the IP1 simulation results matched the experimental results.

7.5.5 Noise Figure Measurement

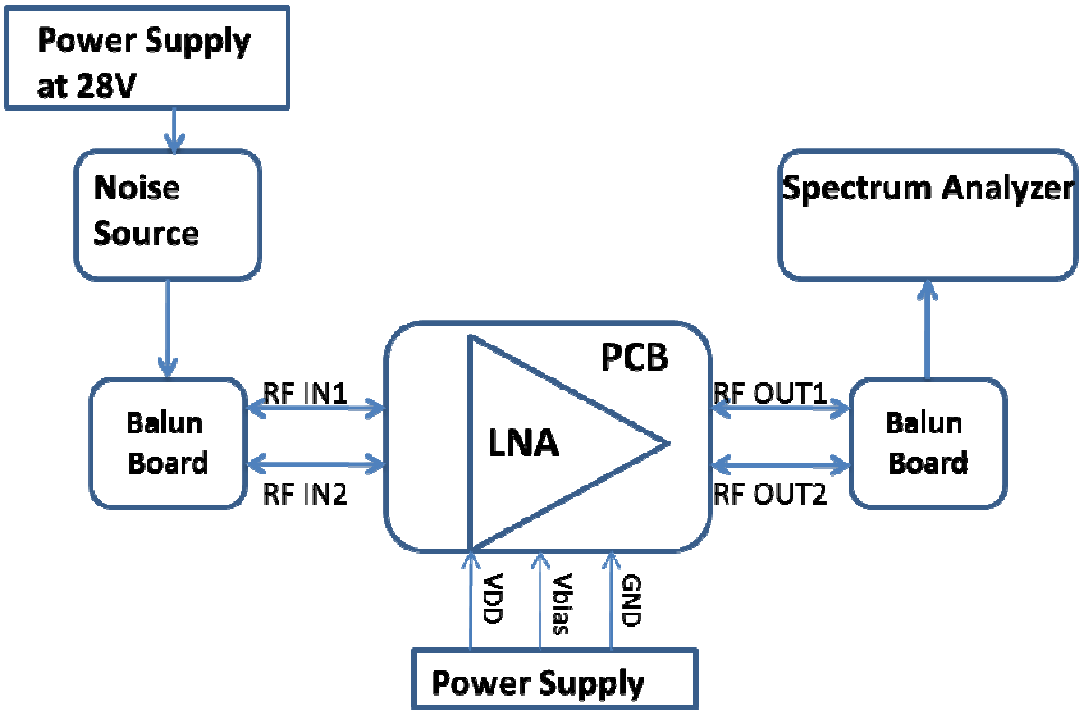

Figure 7.19 Set up for noise figure measurement

Figure 7.19 shows the set up for noise figure measurement which used the Y Factor method. In order to use Y Factor method, an ENR (Excess Noise Ratio) noise source is needed for the testing [21]. The noise source requires a high DC power supply up to 28V, and its operating frequency is up to 5GHz. Turning the power supply to the noise source on and off, the spectrum analyzer measured the change in the output noise power density. The equation for calculating the NF is [21]:

$$\frac{\quad}{\quad} \qquad (7.1)$$

The ENR values are on the noise source, and different noise source will have different ENR values. The smaller the ENR, the lower noise figure can be measured by this method.

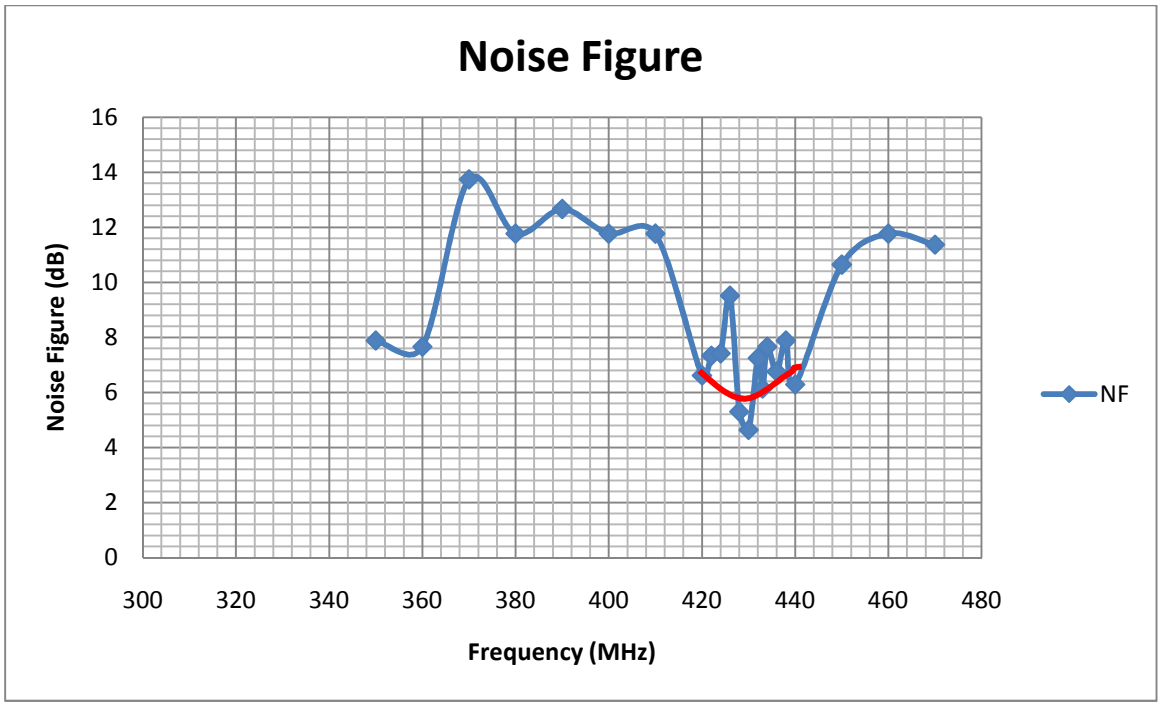

Figure 7.20. Measured noise figure

From Figure 7.20, the lowest value of the noise figure is around 433 MHz. And the noise figure at 433 MHz is around 6 dB. The red curve in Figure 7.20 shows the trend of the noise figure around 433 MHz. Comparing with Figure 5.5 which is noise figure from simulation, the lowest noise figure at 433 MHz for both. Because the output of the noise source used in the testing produced output noise measurements close to the noise floor of the spectrum analyzer, the results for the noise figure are fluctuating. But it shows a general trend of low noise figure around 430 MHz, the range of interest which is consistent with simulated values. Also due to the loss associated with balun boards, environmental noises and the limitation of the equipment, the noise figure is higher than the simulation value. Better results could be obtained using a Faraday cage.

CHAPTER 8

Conclusions and Future Work

The presented thesis explains the design flow of a fully differential LNA as the first block in a wireless communication system. An LNA amplifies the small-signal from the antenna without adding excessive noise into the system.

The LNA design started with an explanation of the noise and the noise sources. By understanding the LNA and potential source of noise, a suitable topology could be chosen to achieve the design requirements. Since the source degenerated topology had the lowest noise contribution this topology was chosen, and transistor sizes, impedance matching networks, DC blocking capacitors, and bias circuits all needed to be well designed at a 433 MHz operation frequency to ensure a quality design. After Cadence simulations verified all the designed values and corroborated its function in a schematic and layout level, the low noise amplifier was sent for fabrication to MOSIS using a 0.13 μm technology process. A test plan was prepared during the fabrication time, and the PCB design was finished before the chip returned.

According to the experimental results, the LNA as designed with a low noise figure at 433 MHz, has a peak value of voltage gain at 372 MHz. This is because of the tradeoffs that were made between voltage gain and noise figure. The gain was even lower than simulated because the board manufacturer cannot guarantee the impedances for the microstrip lines for the designed board, so gain loss resulted from impedance mismatch. Also, on the balun boards, parasitic resistance from soldering and mismatching impedance from both the input and output ports during measurement degraded the voltage gain as well. Overall, this LNA has higher gain and better linearity at 373 MHz

than 433 MHz but sacrifices noise figure to achieve that lowest observed noise figure (measured and simulated) at the target 433MHz.

More measurements and simulations have been performed to trouble shoot the difference between simulated and measured gain vs. frequency characteristics.

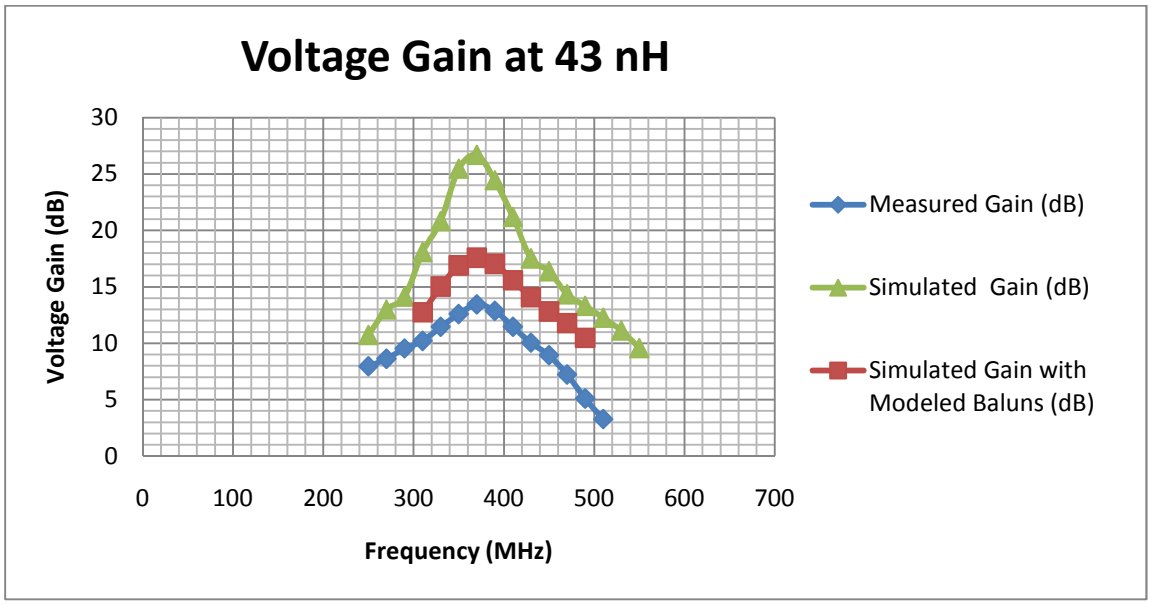

Figure 8.1. Measured voltage gain vs. simulated voltage gain

With 43 nH in the impedance matching network, all of the simulated voltage gains have peak frequencies at around 370 MHz. The measured voltage gain is lower than the simulated voltage gain. However, the gain with more accurately modeled baluns, which have the same performances as the real baluns, decreases the gain by almost 8 dB in the simulation. And also due to the board's loss and the parasitic resistance, the gain still decreases by 4 dB for the measurement.

Table 8.1. The Comparison of simulation with the modeled baluns and measurement with balun boards

Parameters	Simulated with Modeled Baluns	Measured with Balun Boards
S11 = S22	-15.1 dB	-15.15 dB
S12 = S21	-1.68 dB	-2.54 dB
Voltage Gain	13.91 dB	12.04 dB
Noise Figure	2.19 dB	6 dB

In Table 8.1, the modeled baluns have been made in the simulation to be as close as possible to the measured balun boards; there is 1.87 dB difference of the voltage gain between the simulation and measurement. These balun models were used to replicate the test setup in the simulation.

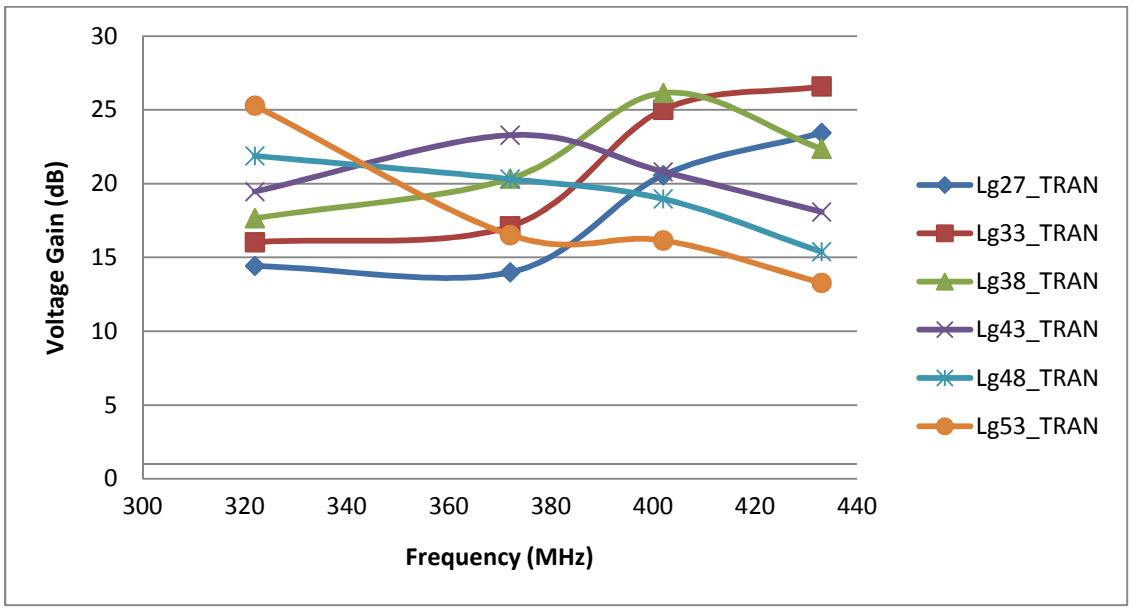

Figure 8.2. Different input impedance vary the voltage gain

Varying the inductor value in the impedance matching network in simulation, the maximum gain frequency changes as well. The gain changes when the input impedance varies. But either increasing the input inductor in the matching network to 53 nH or decreasing it to 27 nH, will increase the noise figure by more than 1 dB compared to the noise figure at 43 nH.

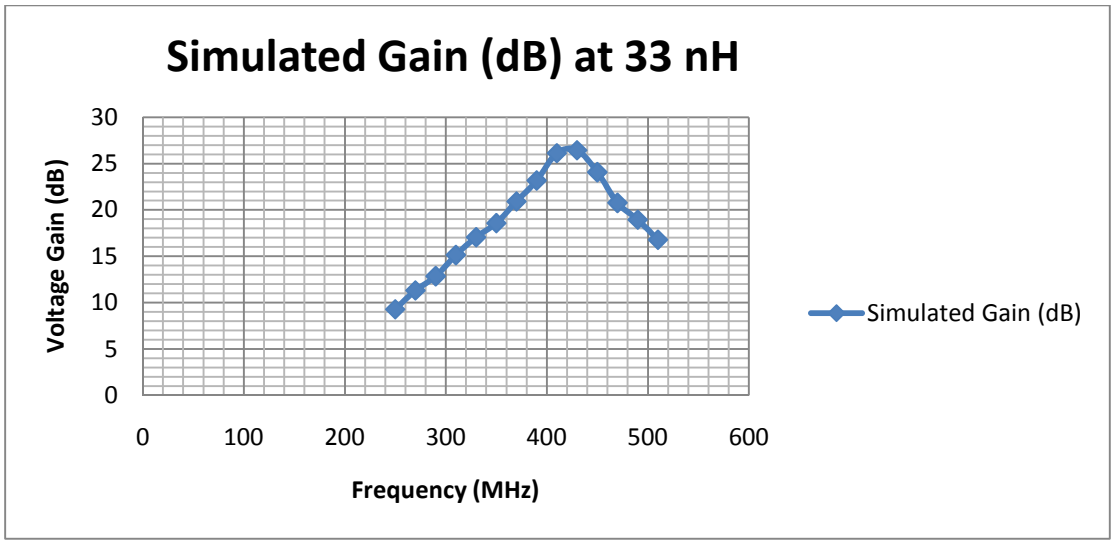

Figure 8.3. Voltage gain with 33 nH input impedance match

Concluding from Figure 8.3, by replacing the 43 nH with a smaller inductor of 33 nH, the maximum gain frequency shifted to 433 MHz. The smaller inductor in the impedance matching network shifts the peak value of the voltage gain. But the noise figure at 33nH is increased to 1.84 dB in the simulation.

Tradeoffs have to be made between voltage gain and noise figure:

From the equations of the thermal noise in MOSFET:

The thermal noise power from the source resistor is:

$$\overline{V_{n,R_s,out}^2} = \overline{V_{n,R_s}^2} G_m^2 R_L^2 = 4kTR_s\Delta f G_m^2 R_L^2 = 4kTR_s\Delta f Q_{in}^2 g_m^2 R_L^2 \qquad (4.13)$$

And the thermal noise power from the transistor is:

$$\overline{V_{n,D,out}^2} = \overline{i_{n,D}^2} R_L^2 = 4kT\gamma g_m \Delta f R_L^2 \quad (4.14)$$

Thermal noise is directly related to the transconductance g_m , and the equations for transconductance is :

$$g_m = \sqrt{2\mu_n C_{ox}} \sqrt{\frac{W}{L}} \sqrt{I_D} \quad (5.3)$$

It can be seen that the gain increase is because of the transconductance increase. So as long as the transconductance increases, the gain will increase and the circuit will be introduced to more thermal noise, which will lead to an increase to the noise figure. Thus the lowest point of noise figure will not match with the highest value of the voltage gain. So the tradeoff must be made for an LNA in order to reach the lowest noise figure and still have a sufficiently large gain.

Referring to the voltage gain measurement in Figure 8.1 and noise figure measurement in Figure 7.20, the gain has been sacrificed to reach the lowest noise figure.

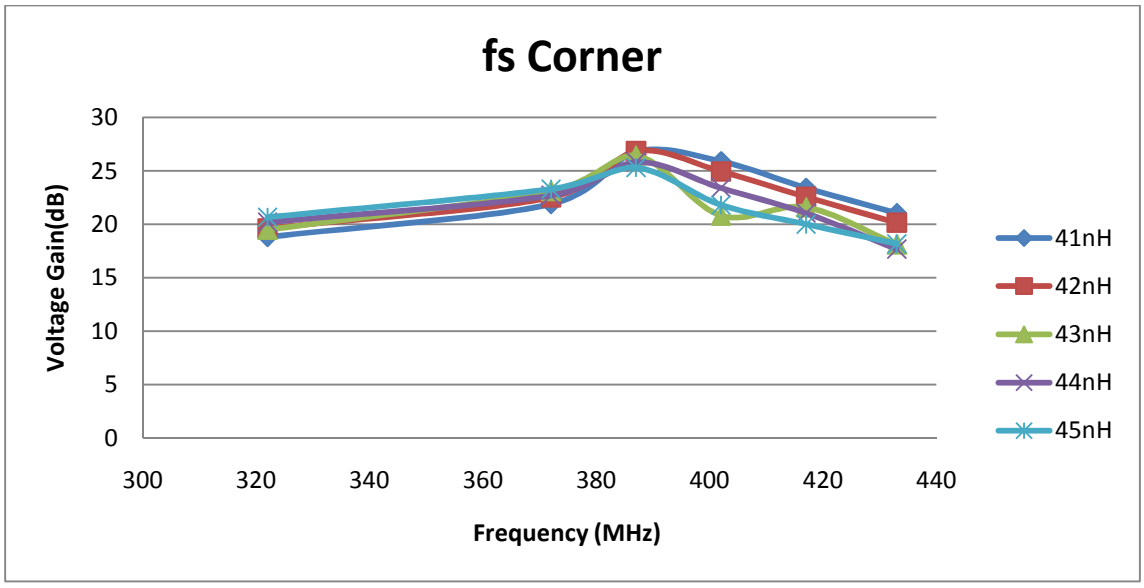

Figure 8.4. fs corner simulations with different input impedance match values

The Figure 8.4 is the voltage gain under process skewed “fs” (fast NMOS, slow PMOS) simulation varied with different impedance matching network. The fs corner simulation results are close to the “tt” (nominal) simulations.

Overall, the tradeoffs between noise figure and voltage gain have to be made to achieve the optimum performance for an LNA. Although the input impedance matching network is shifting the peak values of the gain, this LNA provides a sufficient voltage gain at 433 MHz. Also, the noise figure will increase by changing the inductance in the impedance matching network to a value other than 43nH. Hence, though the design shows the highest gain around 370 MHz, the fact that its noise figure is lowest at 433 MHz, led to this design.

In future work, noise figure should be measured with more accurate equipment including the use of a Faraday cage and batteries for the power supply to remove excess noise. The integration of the fully differential low noise amplifier in the wireless communication system level design is the main future work. The impedance match between the LNA and the mixer (the next block), as well as the linearity range for the mixer should be considered.

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