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Study of Current Optocoupler Techniques and Applications for Isolation of Sensing and Control Signals in DC-DC Converters

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STUDY OF CURRENT OPTOCOUPLER TECHNIQUES AND APPLICATIONS FOR ISOLATION OF SENSING AND CONTROL SIGNALS IN DC-DC CONVERTERS

STUDY OF CURRENT OPTOCOUPLER TECHNIQUES AND APPLICATIONS FOR ISOLATION OF SENSING AND CONTROL SIGNALS IN DC-DC CONVERTERS

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ABSTRACT

There is a need for power switches that can operate at high voltage, high temperature, and high switching frequencies with low losses. Power switches fabricated from wide bandgap materials such as silicon carbide (SiC) or gallium nitride (GaN) can outperform conventional silicon switches due to material property advantages. Another common problem in grid-connected applications is the need for high voltage-isolation of gate drivers and control circuitry while operating efficiently at the high switching frequencies, high power density, and high temperatures made possible by wide bandgap devices. Transformers cannot operate at the temperatures of these wide bandgap devices and a new solution needs to be determined to operate at higher temperatures with smaller footprints. The purpose of this research is to determine the baseline performance of the current technologies used to isolate gate driver and control signals from high voltage power electronics. Research was conducted to determine the characteristics of current optical isolation technologies and implementation techniques in the specific areas of propagation delay, linearity, power consumption, and voltage isolation to determine the baseline performance that future devices could improve upon. The techniques employed to operate the current optocoupler technology were looked at individually and implemented in a Buck converter to determine the performance characteristics with respect to the figures of merit above. The results of the research were that although optocouplers can be used in many different functions the current technology benchmark lacks the robustness of speed, noise immunity, and easy implementation to compete with current workhorse technologies like transformers. The linearity of transmitted analog signals, transmission speed of digital control signals, and the maximum allowable voltage between power stage and control circuitry will need to be improved by future optocoupler technologies like GaN to compete with current isolation techniques.

This thesis is approved for recommendation
to the Graduate Council.

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DEDICATION

To Jesus, my friend and Hero

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1 INTRODUCTION

Power electronics are increasing in power level and switching frequencies while decreasing in size because of increased power density, operating temperature, and breakdown voltage due to the innovation of power semiconductor devices like SiC MOSFET's and IGBT's [1]. Power electronics, no matter how simple or complex, need control circuitry of some form to control how the power system reacts to line and load changes. The controller uses system variables from the power electronics system, like input current or output voltage, to analyze the condition of the power electronic circuitry so that control signals can be produced to regulate and stabilize the behavior of the power circuitry to keep the system stable in a dynamic environment. These control circuits work at relatively low voltages while the power electronic circuits can operate at increasingly high voltages due to the aforementioned innovations in semiconductor technology. If direct connections are made between the power circuitry and control circuitry via the network that senses the control variable (i.e., a voltage divider sensing an output voltage) the large noise associated with power circuitry will influence the operation and distort the control circuitry – possibly destroying it. The control circuitry needs to be electrically isolated from the power circuitry. This is done by isolating the two circuits' grounds from each other and removing any electrical connections between the two. Figure 1.1 shows this concept.

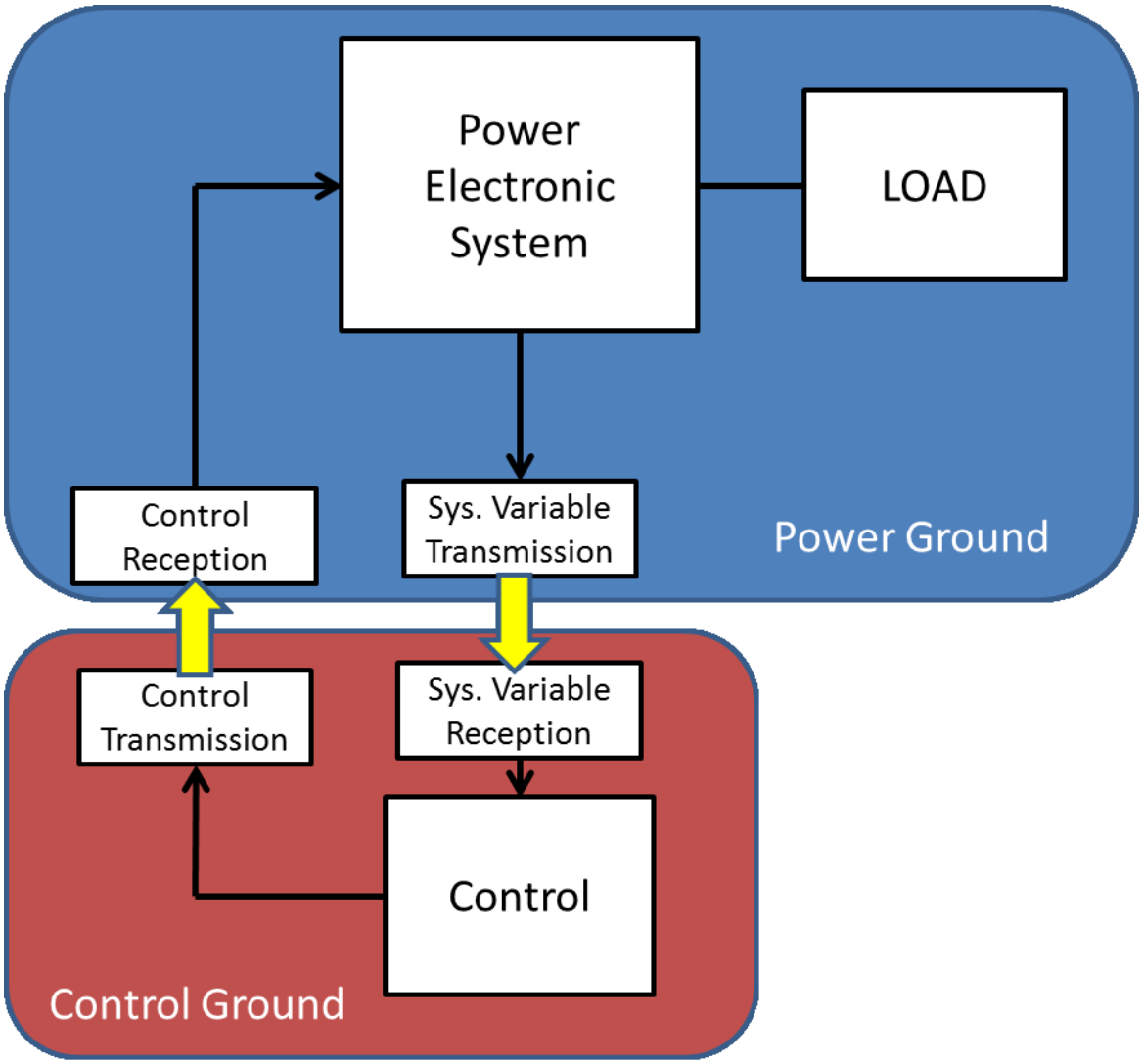


Figure 1.1 Concept of isolated grounds for control and power circuit

The first role for isolation is isolating power supplies from each other. The two isolated grounds (represented as the red control ground and blue power ground) would require two separate power supplies to power their respective circuitry. The power ground is established by the power input to the power electronics system and no connection is made to the power input to the control circuitry so that the grounds are electrically separate from each other. This means that all the signals in the power circuit will be referenced to a different potential than the signals in the control circuit. This potential difference between the two separate grounds can be large. How can the sensed system variables and control

signals be sent between separately referenced circuits without electrical connections (shown as the yellow arrows in Figure 1.1)? This question is answered by special devices that can transmit through the isolation barriers without electrically coupling the two circuits. These devices operate by converting the electrical signals into other forms (i.e. magnetic or optical) to be transmitted through the isolation barrier and then converted back to an electrical signal referenced to the correct ground potential. Three common techniques have been developed to implement both types of isolation: transformers, optical devices, and capacitors. Research is being done in these three areas to follow the trend in power electronic systems to have greater switching frequencies and higher power with smaller footprints, which in isolation technology means faster transmitting speeds and greater voltage isolation in a smaller package.

1.1 Purpose of the Thesis

The purpose of this thesis is conveying the results of research into only one of the different isolation devices, the optocoupler. The principal objective is to determine the state of commercially available optocoupler technology. A benchmark will be created to determine the baseline performance of these optical isolation devices. This benchmark can be used to compare new optical isolation technology with future technologies like gallium nitride (GaN) optical devices. GaN is expected to be the improvement in optical isolation that will allow optical isolation to be implemented within the higher power and higher frequencies of current and future power electronics. This means isolation is needed between a larger voltage difference, but with the very fast transmitting speeds needed for faster switching frequencies. A parallel purpose is to create an all-optical control loop for a specific power electronic design. The design of the power electronic system is included to show the current optical limitations on a power electronics system. The application context power electronic system is chosen to be a current-mode optically-controlled Buck converter with an isolated resonant energy recovery

MOSFET gate driver as presented in [2]. The reasons for choosing this specific design are to display the many uses for optical isolation and these reasons are elaborated on in the following chapters. To understand the need for optocoupler technology and the improvements possible with GaN the other two isolation techniques, capacitive and transformer isolation will be briefly discussed.

1.2 Broader Context of Thesis

1.2.1 Capacitive Isolation

Isolation with capacitors is used to isolate a voltage potential from earth ground and reference it to a floating node within the circuit, and to transmit information through an isolation barrier between two different references. In the former application the energy transfer is done through the charging of the capacitor which is a limiting factor in that the capacitor will need a time when it is not used and recharged. The first example of capacitive isolation is a bootstrapping circuit which allows a power source to keep its voltage potential (in relationship to its actual reference node) even when it is referenced to a floating node [3]. Switches are always present in capacitive isolation because there must be a time when the bootstrap capacitor is recharged through a switch connected to actual ground potential. This is isolation between the actual ground of a power supply and a floating node within the circuit with a few extra, small components. Figure 1.2 shows a bootstrap circuit [3]. The disadvantage is that this circuitry only allows a floating reference point and does not isolate voltages. In Figure 1.2, when Q_1 is on, the bootstrap diode D_B and the high-side driver are subjected to V_{DD} which can be very large in a power electronics circuit. With optical isolation the optocoupler is the only component that must withstand this voltage so the other circuitry can be rated much lower.

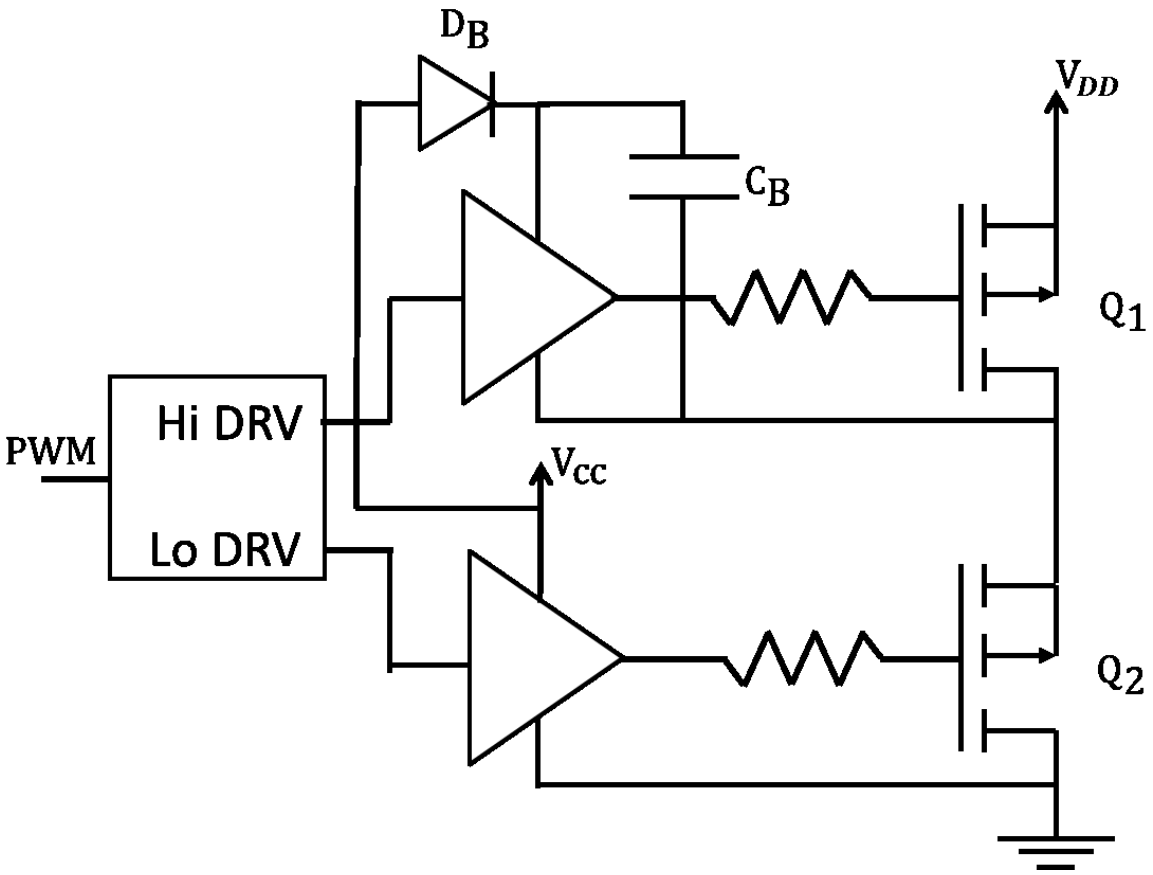


Figure 1.2 Bootstrap circuit [3]

Another circuit employing capacitive isolation is a charge pump [4]. A fully isolated voltage potential can be generated from a grounded source voltage using a square wave, diodes, and capacitors as shown in Figure 1.3 [4]. The components (IC's and external diodes) are subjected to the full system voltage so they have to withstand large voltages as in the bootstrap topology. Also, capacitors can be used to transmit through isolation barriers as shown in [5]. Optocouplers cannot reach the transmission speeds of capacitive isolation with the current technology, but it can transmit signals across its entire bandwidth without the use of pulse width modulation and it is a much smaller footprint [5].

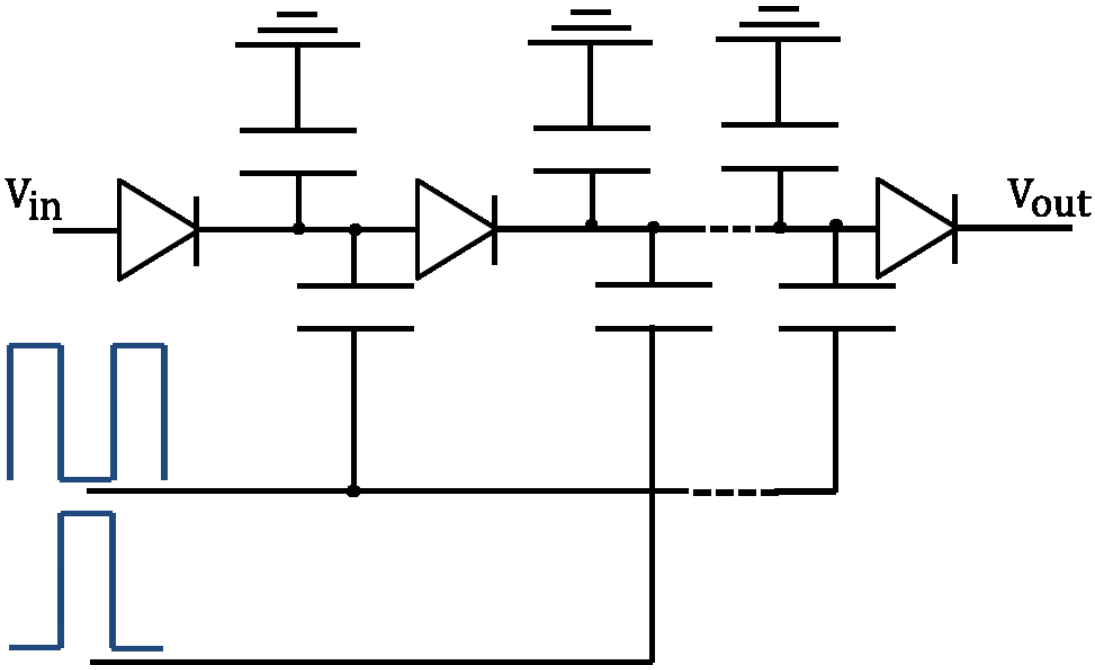


Figure 1.3 Dickson charge pump [4]

1.2.2 Transformer Isolation

Transformers are the current workhorse for isolation. The secondary windings are electrically isolated from the primary windings. The magnetic field produced by the primary winding induces a current on the secondary winding determined by the ratio of the number of turns. In a transformer the power is transferred by the use of this magnetic field so there is no direct electrical connection. Transformers are also very efficient, but their footprint is larger than the capacitive isolation schemes. The size of the transformer is dependent on the number of windings and the frequency at which it is operating. The size decreases as the frequency increases, but it remains a larger footprint than the circuitry necessary for capacitive isolation. Transformers can be used for both isolation purposes, creating isolated power supplies as shown in Figure 1.4a and transmitting signals in Figure 1.4b [1].

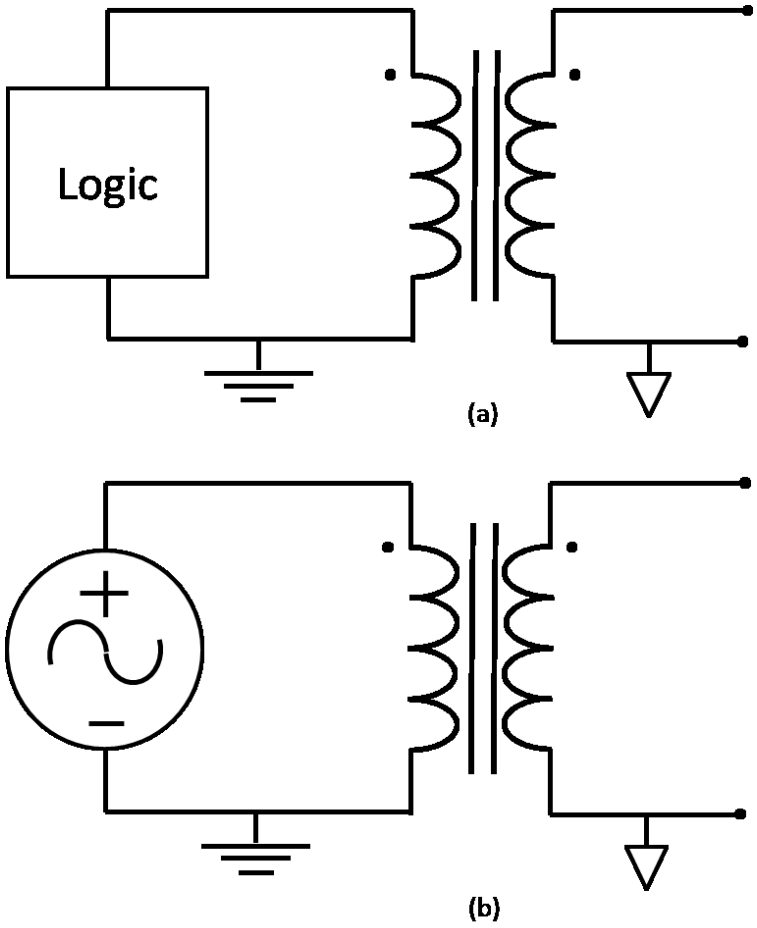


Figure 1.4 Transformer isolation for logic signals (a) and power (b)

The scope of this thesis is the transmission of signals through isolation and in this application the duty cycle is limited to less than 50%, so the transformer will not saturate. The size of the transformer limits it to large circuits that do not need to save space. With optical isolation the optocoupler is very small and can be implemented on chip [1]. It can be used to transmit digital information with large voltage isolation and an analog current signal without the limiting duty cycle.

1.3 Optocoupler Introduction

1.3.1 Optocoupler's Basic Structure and Isolation Applications

Now that the other two isolation technologies are understood the use of optocouplers can be appreciated. Optocouplers, most simply put, are a combination of a diode, that emits light when current flows through it, and a diode that absorbs the light and produces a proportional current (like a solar cell) [6]. Figure 1.5 shows a simple schematic of an optocoupler.

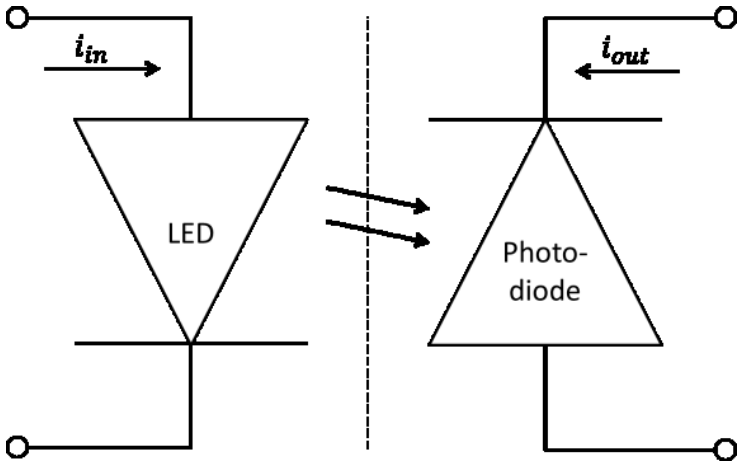


Figure 1.5 Basic structure of optocoupler

Just like a solar cell, the optocoupler can be used to generate isolated power from a ground referenced power supply by sending the power via light. This is an extremely important application of the optocoupler because of its very small size and large operating range (compared to transformer saturation).[1] The optocoupler is most useful transmitting sensed information measured from the power circuitry that is needed by the control circuitry. As seen in Figure 1.5, the output signal is isolated from

[1] Research into improving this power isolation technique is being done in collaboration with the University of South Carolina and will not be covered in this thesis.

the input, where the transmission medium is light so there is no electrical connection between the input and output.

There are many different types of optocouplers available commercially (operating with digital signals or analog signals as inputs), and this thesis defines an application context to test these optocouplers in a high speed, high power, and high temperature environment to determine a benchmark for current technologies to be compared to future technologies like GaN. This is important to find the areas that GaN can improve upon with its inherent higher temperature, lower power consumption, shorter propagation delays, and higher voltage isolation capabilities. It is important in order to determine the current limitations of commercially available technologies in the four areas that GaN optocouplers are supposed to improve upon because when GaN devices can be fully tested there will be a benchmark to quantitatively compare GaN's improvements or trade-offs to the developed technologies in the market.

1.3.2 Determining the Benchmark

There are two main components to determining the benchmark set by commercially available optocouplers. Because optocouplers do not operate independently, the first is to separately test the different kinds of optocouplers with an application specific circuit that will employ different types of optocouplers and determine the limiting characteristics of each kind of optocoupler application. The two types of applications are analog and digital transmission. The analog optocouplers transmit information accurately with the use of op amp circuitry around the optocoupler. In this optocoupler application the accuracy and propagation delay from input to output are the important figures of merit. They will be measured in the presence of temperature and input changes to determine the baseline performance of these types of optocouplers. The importance is maintaining an output that tracks the input linearly over a large range of temperature and inputs. This range will be quantified and recorded as the benchmark

that future analog optocouplers will improve upon. The digital optocouplers only transmit ones and zeros by employing an output stage that swings from on to off very quickly. The figures of merit for these circuits are their propagation delay, minimum pulse width, and power consumption. Just like the analog transmission optocouplers these parameters will be analyzed in the presence of temperature and biasing changes to determine the digital benchmark.

The second component is implementing an all-optical closed loop power converter with the commercially available optocouplers. The power converter application context will be used to display the same limits (propagation delay, temperature, accuracy, power consumption, etc.) in a practical power electronics system with very specific requirements for the optocouplers operation. The design process will be parallel to the first component. This will create a viewpoint into the functionality of the optocouplers in the presence of noise and timing constraints compared to the ideal bench top testing of the optocouplers with ideal inputs and biasing. The future work will be to implement the GaN optocouplers into the same application context to determine the benefits.

1.4 Thesis Organization

The Background chapter presents a foundational understanding of the optocoupler technologies available and their different uses. It also defines the application context for the first component of experimentation that will be implemented to find the speed and temperature limits of the available optocouplers independent from the full system implementation. In the next chapter, Optocoupler Characterization Experiments, experiments are conducted on the individual topologies to determine the benchmark for each of the topologies and to understand the design decisions that have to be made to implement the optocouplers into the Buck converter. The second component of experimentation is determined to be a current-mode optically-controlled Buck converter. This is chosen because it needs isolated current and voltage sensing and gate drive control. These reasons are elaborated upon in the

Background chapter. The Implementation of Optocouplers in a Closed-Loop Buck Converter Chapter shows the design procedure of the current-mode optically-controlled Buck. The Buck converter implements the best of the analog and digital design to determine their performance in an application context with real power, noise, and stability requirements. Simulation results are recorded for the design in this chapter. The final PCB implementation and experimental results are recorded as well. The Conclusions chapter records the final benchmark for each of the individual optocoupler topologies. The final chapter will also describe conclusions on the overall advantages and disadvantages of optocouplers in the Buck converter. Future work will also be discussed in the Conclusions chapter.

2 BACKGROUND

This chapter describes the information needed to understand the basic concepts of the technology that is analyzed in this thesis. The foundations that are laid in this chapter are broken down into three sections. The first section reveals the needed information to understand what an optocoupler is, how it works, and the different devices available. The next section defines the Buck converter, the application context for testing the optocouplers functions in a real world circuit. It discusses why the Buck converter was chosen, its basic operation principles, where the optocoupler is an integral part to its operation and the control methods that need to be implemented. Finally, the gate driver options for the isolated, wide bandgap switch are introduced and its need and operation are outlined. These three foundations are needed so that the experiments that determine the benchmark performance of the current optocouplers can be understood. Once the optocoupler is understood the optimal topology can be chosen to implement in optical Buck converter and the final conclusions about the optocoupler's use in a DC-DC converter system can be drawn.

2.1 Optocouplers

The conventional technique to transmit electrical information without direct electrical connections is transformers, as discussed in the introduction. Because of the inherent advantages of an optocoupler, for instance its smaller size and possible monolithic integration onto a power electronics chip, it is desirable to improve the current technology to eliminate their inherent disadvantages like long propagation delays so they can compete with transformers in the isolation market.

Optocouplers are the key component of research in this thesis. All the circuitry around it, from the application context to the auxiliary circuits that optimize the optocouplers is there to test and enhance its operation and performance. To fully understand the design process of testing, enhancing, and finally

characterizing a benchmark for the optocouplers, the basic operation of the fundamental optocoupler structure and operation must be understood.

2.1.1 Optocoupler Basics

Optocouplers are used, similarly to transformers, to transmit electrical information without electrically coupling the transmitter and receiver. Optocouplers use light generated by current flowing through a light emitting diode (LED) to transmit signals and that light needs to be converted back to voltage signals at the output to be useful. A photodiode (or phototransistor) is the second half of an optocoupler, which creates an electrical potential when light impinges on its p-n junction. Figure 2.1 shows a simple schematic representation of an optocoupler, it can be seen that no electrical connection is made between the input LED and output photodiode. The photodiode has a single PN junction that generates electrical power from the impinged light [6].

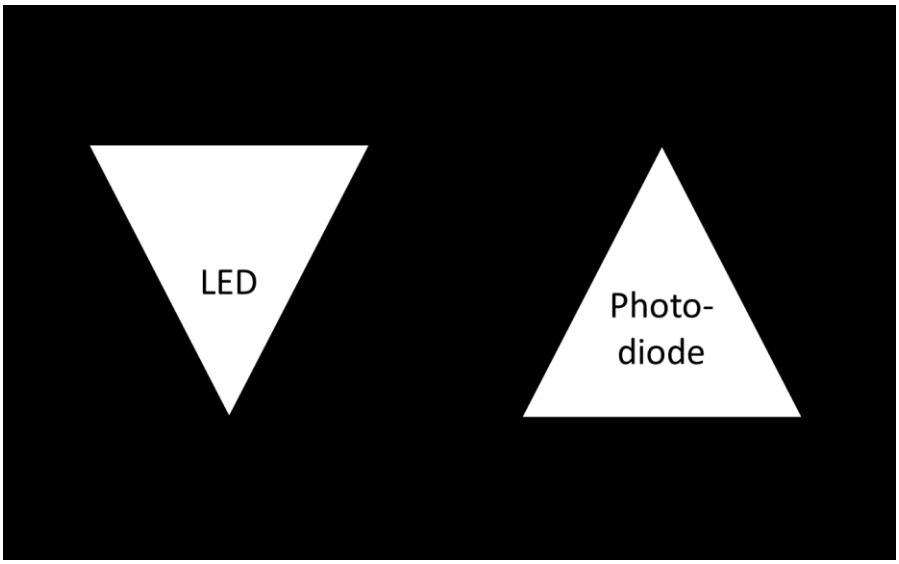


Figure 2.1 Basic structure of optocoupler

Since the photodiode is basically a diode that has enhanced light sensitivity the I-V relationship is inspected to determine its operating characteristics. For the operation of transmitting signals through

an isolation barrier the photodiode will act as a receiver. To operate as a receiver the PN junction needs to be reverse-biased. Ideally, if the junction is uniformly illuminated with photons with an energy greater than the energy of the bandgap $\left(hv>E_g\right)$ then electron hole pairs (EHPs) are generated at a rate of g_{op} (EHP/cm^3-s) and swept out of the depletion region participating in current flow [6]. This current is defined by:

$$I_{op}=qAg_{op}\left(L_p+L_n+W\right) \quad \textbf{(2-1)}$$

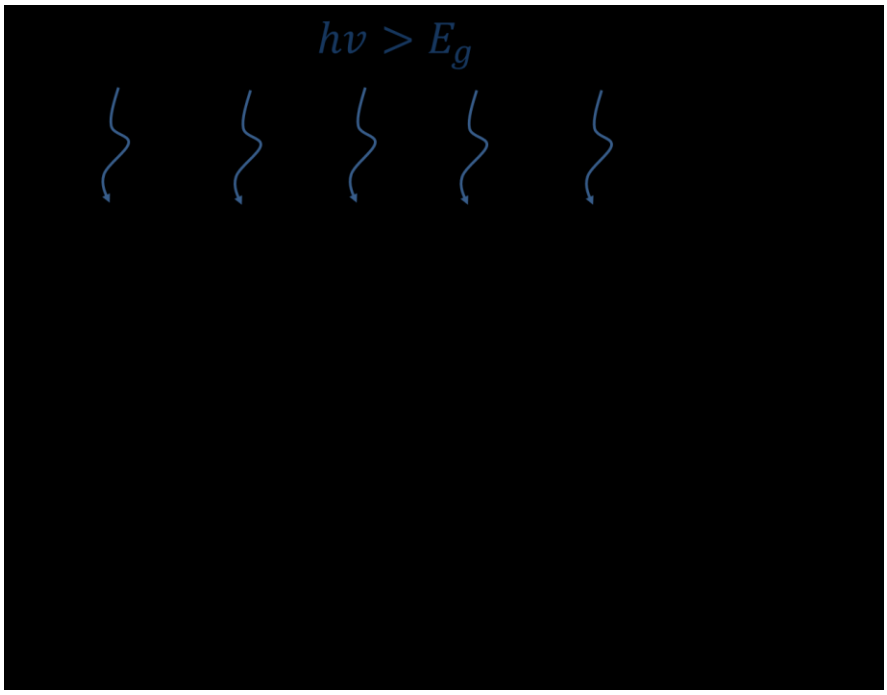


Figure 2.2 Structure of photodiode [6]

This equation states that the current is determined by the rate at which the EHPs are created in the depletion region $\left(Ag_{op}W\right)$, holes created per second within a diffusion length on the *n*-side $\left(Ag_{op}L_n\right)$, and electrons created per second within a diffusion length on the *p*-side $\left(Ag_{op}L_p\right)$. This current is directed from the *n*-region in Figure 2.2 to the *p*-region, so it subtracts from the diodes fundamental current to become [6]:

$$I=I_{th}\left(e^{\frac{qV}{kT}}-1\right)-I_{op} \quad \textbf{(2-2)}$$

The I-V curve shifts downward (increasing current in the negative direction) by increasing values of g_{op}. Figure 2.3 shows the I-V curve for increasing g_{op}. Through investigation of the I-V curve the photodiode has three quadrants of operation while light is impinged on the junction.

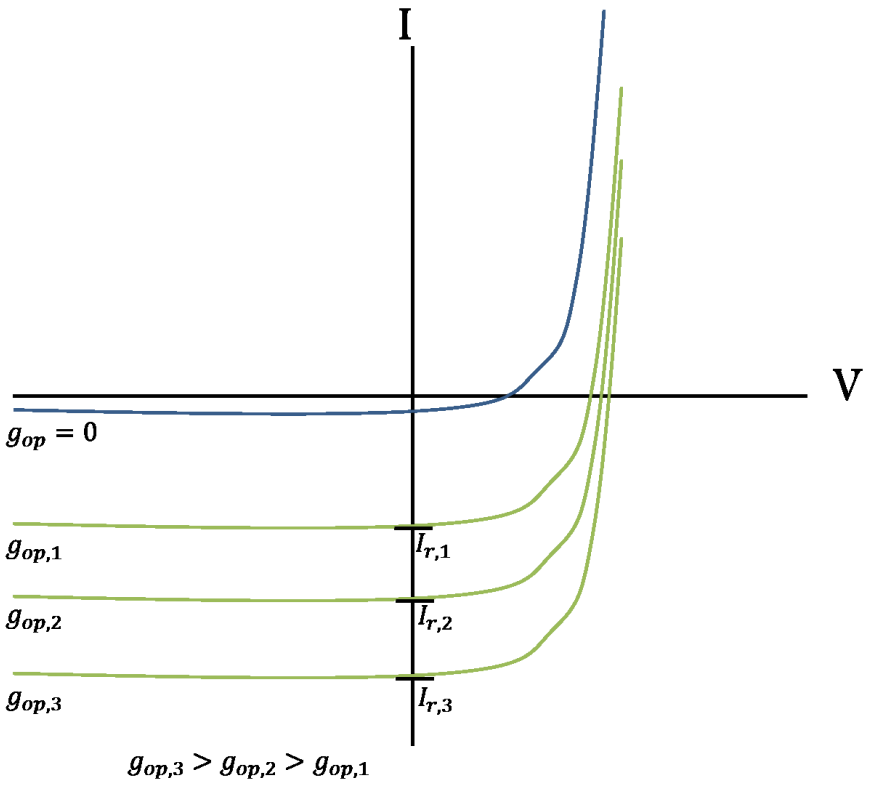


Figure 2.3 I-V curve for photodiode [6]

The three different quadrants of operation each have different desirable characteristics. In the first quadrant the photodiode characteristics follow that of a normal diode with an increased cut-in voltage. This quadrant is avoided in optocoupler applications because current will flow independent of the operation of the LED. In quadrant three the diode is reversed biased and without any added optical energy the reverse current equals the leakage current of the diode. As the optical energy increases

(increasing g_{op}) the current increases from $I_{r,1}$ to $I_{r,3}$. This current flows from the *n*-region to the *p*-region as shown in Figure 2.4a and consumes energy [6]. This is called the photoconductive mode of operation [7]. In the fourth quadrant the photodiode is forward biased but the current is still negative. In this case, the photodiode delivers energy [6], [7]. This is the photovoltaic mode (same operation of a solar cell), and it is shown in Figure 2.4b.

Figure 2.4 Two quadrants of operation, photoconductive (a) and photovoltaic (b)

Photovoltaic mode is not discussed further in this thesis. This regime is fully investigated by the University of South Carolina in a collaborative project. As stated, the photoconductive mode is used to transmit signals through an isolation barrier because the LED controls the output current by impinging light on a reverse biased junction of a PN Photodiode. All the current created is due to the input LED current. Now that the basic operation is understood the specific parameters of the optocoupler can be discussed. These parameters are important to the benchmark to be set because they are the factors that

affect the key merits of performance like speed, propagation delay, operation over temperature, and power consumption.

2.1.2 Optocoupler Parameters

The LED emits light depending on the amount of current flowing through it. This light impinges on the photosensitive part of a reverse biased photodiode and, as can be seen above, causing a current to flow through the photodiode. This is the basic building block of an optocoupler. There are important parameters to notice when discussing optocouplers as a whole that will determine the baseline performance in the areas that have been described. The first parameter is the ratio between the forward current of the LED and the photodiode current it induces through the mechanism explained above. This ratio is called the current transfer ratio (CTR). The CTR is around 0.2% [8] naturally. Meaning if there is 10 mA flowing through the LED there will be 20 μA flowing in the photodiode. This is obviously a very small current gain. Another problem with the CTR of an optocoupler is its non-linearity. It will be shown in later sections that as temperature or even forward LED current increases the CTR will change. This nonlinearity needs to be reduced for analog transmission. Topologies will be discussed that can employ a feedback scheme to overcome some of these issues.

Two other important figures of merit that specifically affect the maximum speed of the optocoupler are the propagation delay and the minimum pulse width due to the turn on and off times of the device (the rise and fall times). The propagation delay is the amount of time it takes to see a response in the output photodiode current due to a change in the input LED current. This can be due to the time it takes the light radiating from the LED to reach the threshold at which the photodiode begins to produce current. Another aspect of propagation delay that will directly affect the minimum pulse width is the turn on and off times of the device. These are determined by the process of injecting and dissipating the minority carriers to turn on or off the device. The overall effect of longer turn on and turn

off times is that the minimum pulse width will increase. In the next section it will be shown that these parameters will be more disadvantages depending on the application context in which the optocoupler is used.

Something to note here is that temperature and biasing are very important in the discussion of optocouplers because temperature will affect the CTR, propagation delay, and minimum pulse width due to how it affects the semiconductor devices. The individual optocoupler experiments defined in the Optocoupler Characterization Experiments chapter will be conducted over temperature to find how it affects these parameters and the overall benchmark. All these characteristics are not well defined in datasheets, they are given at one or two operating points and in this thesis these will be exhaustively tested over the entire range of biasing and temperature. Because future devices will be made from GaN, which is a wide bandgap device, they will be able to operate over a larger temperature range and this data will need to be compared to the current technologies.

Other important features of any optocoupler are withstanding voltage and a secondary parameter, transient common-mode immunity. These characteristics are not specifically tested in the experiments to determine a benchmark because they are well defined in datasheets, but they will be described here. The transient common-mode immunity is the maximum rate of rise or fall time of a common-mode voltage on the input and output of the optocoupler that causes the output to change states [9]. This output state change is due to the common-mode noise coupling through the parasitic capacitances of the LED or the coupling capacitance from the LED to the photodiode [9]. The rate of rise or fall is around 10 $\frac{\text{kV}}{\text{us}}$ with a minimum common-mode voltage potential of 1 kV in the current technologies [9]. The withstanding voltage is simply the voltage potential that the optocoupler can isolate from one side of isolation to the other. Currently, this is on average 5 kV for 60 seconds and 1.4 kV for dc voltages [7], [10], [11], [12].

2.1.3 Optocoupler Application Topologies

Thus far the optocoupler has been presented as a stand-alone device, but it is always implemented within a specific application with auxiliary circuitry to compensate for its disadvantages. Because of the parameters discussed in the previous section, circuitry needs to be implemented around the optocoupler to negate the disadvantages of CTR, propagation delay, minimum pulse width, and optimize the device, so that the maximum speed can be achieved in a variety of roles in which the optocoupler is placed. Two general categories can be made for all the functions of the optocoupler in an application. The first category is the optocoupler implemented in an analog role and the second is a digital role.

For the analog role, small changes to the input current cause even smaller changes to the output current. The optocoupler, in this sense, can be classified as a current amplifier or current-controlled current source. It is desired that the output tracks the input accurately and linearly over a desired range. In the digital role, the optocoupler is a switch. In this digital role, an input over a certain threshold causes the output state to change to a high or low state. In both roles the basic optocoupler operates in the same way that has been described up to this point, the difference is the circuitry around the optocoupler. So, to use these devices within a specific application (i.e. transmitting analog or digital information) they will not operate independently from the circuitry that implements the optocoupler in the two different roles described. The different topologies for each role are introduced here and the Optocoupler Characterization Experiments chapter determines the experiments that are used to determine which topology is optimal for the application context and the overall benchmark for the current optocouplers. The future GaN devices will also be used within these two different roles, so a standard benchmark of these circuits is important because the GaN optocouplers should enhance these

circuits so they can operate with less propagation delay, high linearity at greater temperatures, and with larger voltage isolation.

2.1.3.1 Role One: Analog Transmission

The important characteristics of the analog transmission role are linearity and propagation delay. The parameters that affect the important characteristics of the first role are the CTR, temperature, and biasing. The CTR is not linear over a particular bias point and temperature, so the output will not track the input linearly over a very large range, see Figure 2.5. Also, the propagation delay will determine the maximum frequency at which the analog optocouplers can be operated. One reason analog topologies used to transmit analog signals need auxiliary circuitry is to compensate for this nonlinear CTR parameter; generally this is done by employing feedback so that the output can accurately track the input. Another reason is that the CTR is naturally low from LED current to photodiode current. Increasing this low gain is done by adding gain into the topology with the same feedback. In some situations an open loop circuit can be used if the input LED is maintained within a small biasing range and the output stage has enough gain to overcome the low CTR gain, and this topology will be discussed later. To understand how each circuit topology effects the natural transmission of data from the input to output the natural transfer function of the most simplistic optocoupler topology method is shown in Eq. (2-6) and the schematic and waveforms in Figure 2.5.

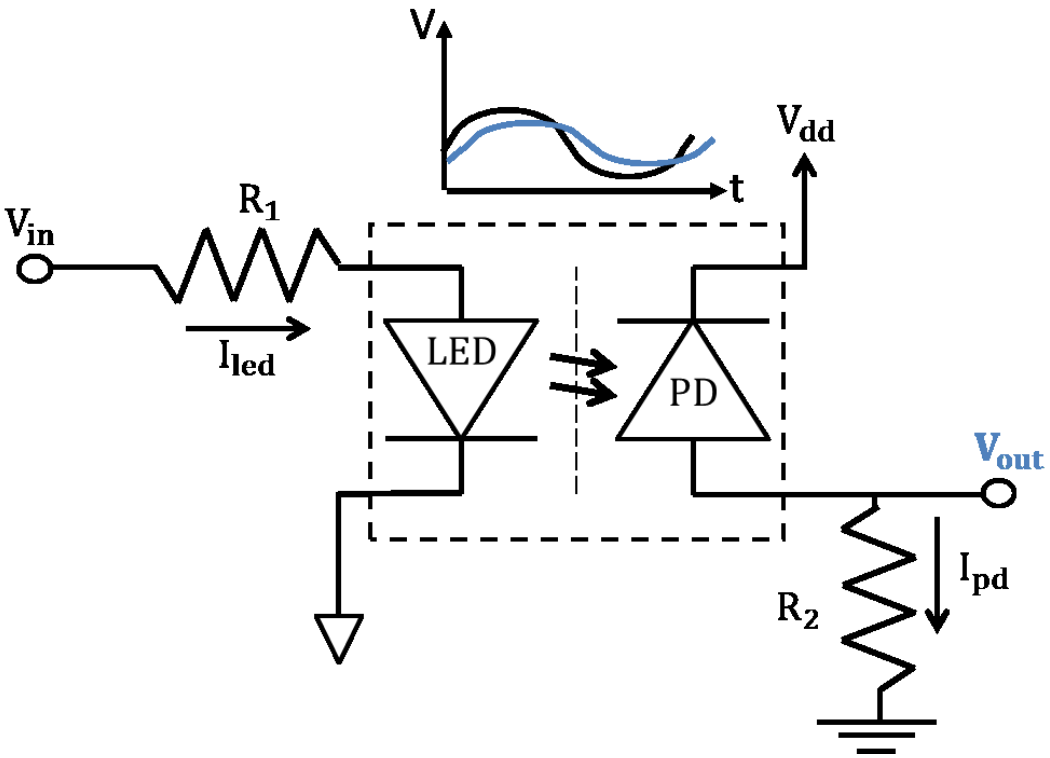


Figure 2.5 Basic transmission topology with waveform for input and output voltage

$$\frac{V_{in}}{R_1} = I_{led} \quad \textbf{(2-3)}$$

$$V_{out} = I_{pd} * R_2 \quad \textbf{(2-4)}$$

$$I_{pd} = I_{led} * CTR \quad \textbf{(2-5)}$$

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1} CTR \quad \textbf{(2-6)}$$

The input resistance R_1 is used to convert the input voltage to a current I_{led}. The photodiode current I_{pd} is generated by I_{led} at a gain equal to the current transfer parameter, CTR. I_{pd} is then converted to a voltage by the resistor R_2. The final transfer function is shown in Eq. (2-6) and Figure 2.5 shows a waveform of the input and output to illustrate the nonlinearity of the CTR parameter over a range of I_{led} and the propagation delay. Along with the nonlinearity, the output current is so small that a very large resistance would have to be chosen for R_2 to have unity gain. Even in the case that a large

resistance is chosen, the amount of current this topology could provide to an output load (usually a capacitance) is miniscule. Topologies have been defined to circumvent these issues [7], [12].

The next analog transmission topology, shown in Figure 2.6, shows the same method of converting an input voltage and transferring it to an output photodiode current where it is then converted back to a voltage with an amplifier that can drive a load more realistically [7]. This topology also employs feedback to cancel the CTR parameter out of the transfer gain.

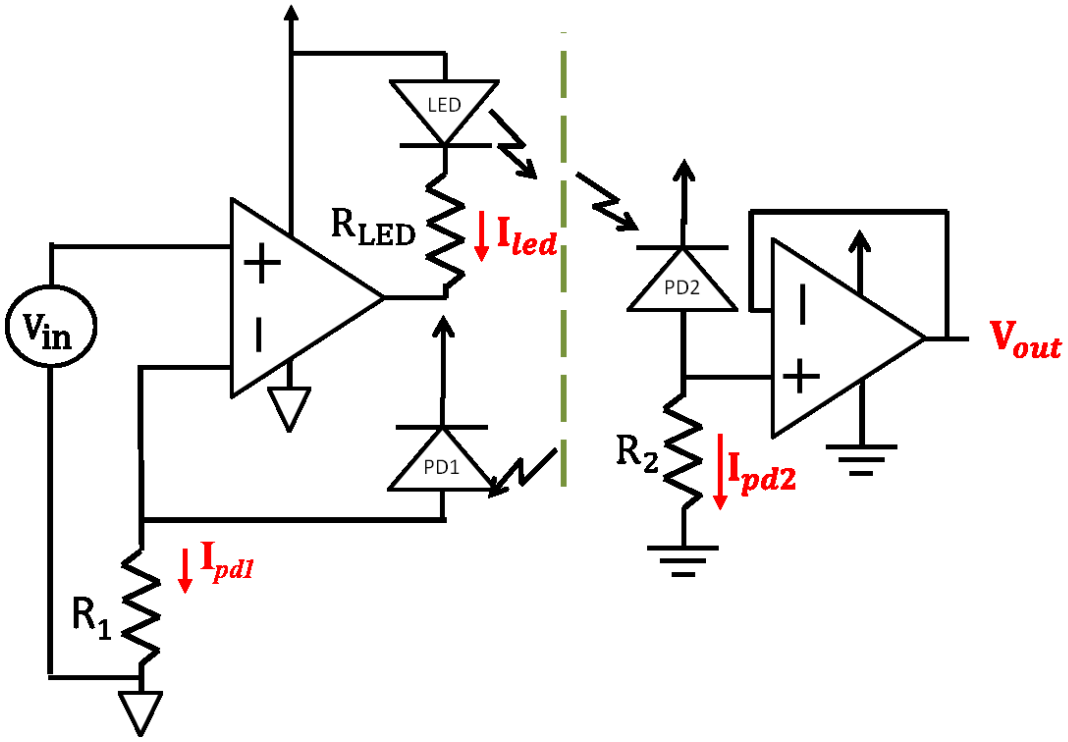


Figure 2.6 Analog transmission topology from [7]

The working principles start at an input applied to the positive node which causes the same voltage potential on the negative node (because of the virtual short of an op amp). The voltage on the negative node causes a current to flow called I_{pd1} that satisfies $\frac{V_{in}}{R_1}$. This current flows through the first photodiode as well, called the servo diode. Because this servo diode is reversed biased the current has

to be produced by light radiating onto its PN junction from the LED. So, for the op amp to reach a steady-state (where the input terminals are at an equal voltage potential) it has to sink current equal to $\frac{I_{pd1}}{CTR}$ through the LED. This relationship is summarized in the equations below [7].

$$I_{pd1}=\frac{V_{in}}{R_1}=CTR*I_{led} \quad \textbf{(2-7)}$$

The light that impinges on the servo diode also impinges on the second photodiode. This current generates an output voltage by a current-to-voltage conversion through the resistor, R_2, connected to voltage follower configured op amp. A voltage follower is used because the voltage will have a unity gain but the op amp will be able to supply much more than the micro-amps of current that the photodiode can supply to a load [7].

$$V_{out}=I_{pd2}*R_2 \quad \textbf{(2-8)}$$

$$I_{pd2}=I_{pd1}=CTR*I_{led}=\frac{V_{in}}{R_1} \quad \textbf{(2-9)}$$

$$\frac{V_{out}}{V_{in}}=\frac{R_2}{R_1} \quad \textbf{(2-10)}$$

The transfer function shows that the feedback on the LED side of the isolation, caused by the servo diode, eliminates CTR from the transfer function. This is extremely powerful for operating the optocoupler in an analog regime over a wide range of temperatures. This means that the input voltage can be a very wide range of voltages without distorting the output because the nonlinear CTR will not affect the output voltage. Conceptually, this works because the photodiode is forced to change exactly as the input voltage changes. The LED provides the correct amount of light to bias the photodiode to satisfy the op amp's virtual short on the input. The photodiode currents will be linear in respect to the input voltage while the LED current will be non-linear, which is the opposite of normal operation. This is why this is an important topology for linear analog transmission optocouplers.

There are a couple of problems to be analyzed in this circuit. One is that the optocouplers in this topology need to optimize propagation delays from the input to output so that the aggregate propagation delay from the op amps and optocoupler will be minimized. Also, the light that is radiated from the LED must impinge equally on the servo diode and output photodiode. A ratio, K_3, is determined to define the difference in the light shining on the two photodiodes from the LED. If this ratio is implemented into the transfer function it shows that there can still be variations, or nonlinearities, in the transfer gain if the amount of light is not the same [7]. Another trade-off is that the addition of the op amps has added more power consumption into the circuit.

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_1} K_3 \qquad \textbf{(2-11)}$$

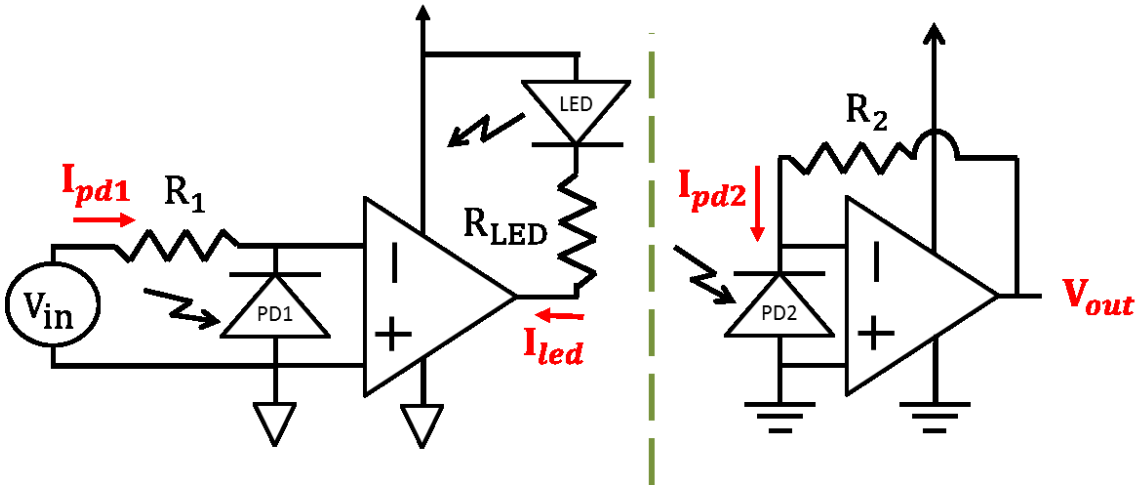


Figure 2.7 Analog transmission topology from [12]

The topology shown in Figure 2.7 is a little bit different than the previous topology but it employs the same optocoupler with a feedback photodiode. The servo diode is now connected between the positive and negative input nodes of the op amp. At a first level approximation the photocurrent, I_{pd1}, is equal to $\frac{V_{in}}{R_1}$ because the negative input is virtually grounded, since the negative and positive nodes are held equal to each other by the virtual short circuit of the op amp. The photodiode is reversed

biased so the current must be generated by light radiating from the LED. The op amp sinks the correct amount of current through the LED (equal to $\frac{Ipd1}{CTR}$ where the actual I_{pd1} is equal to $\frac{V_{in}-V_{pd1}}{R_1}$ due to the voltage drop over the photodiode) that satisfies the small voltage difference across the inputs due to the reverse biased photodiode. The same concept is used on the output as the input, by generating the output voltage with the photodiode current, I_{pd2}, flowing through the feedback resistor R_2 [12].

$$I_{pd1}=\frac{V_{in}}{R_1}=CTR*I_{led} \quad \textbf{(2-12)}$$

$$I_{pd2}=I_{pd1}*K_3=\frac{V_{in}}{R_1}K_3 \quad \textbf{(2-13)}$$

$$\frac{V_{out}}{V_{in}}=\frac{R_2}{R_1}K_3 \quad \textbf{(2-14)}$$

The same transfer function is derived in this topology as on the previous topology. The Implementation of Optocouplers in the Buck Converter chapter will propose methods to determine to implement this linear analog transmission optocoupler into the Buck converter's feedback and the test setup to determine the benchmark for this topology.

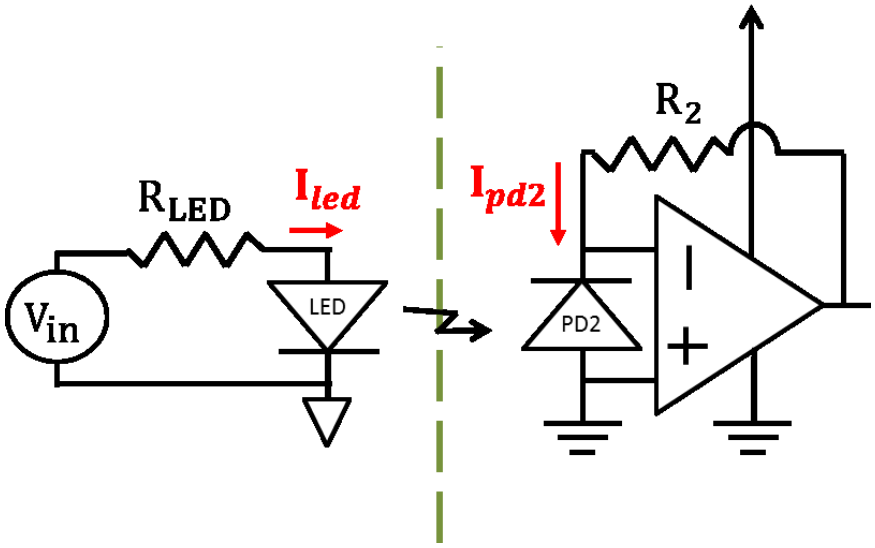


Figure 2.8 Open-loop analog transmission topology

The topology in Figure 2.8 does not have feedback like the previous two circuits so the CTR will appear in the transfer function. It employs the same output concept as the previous topology so it is a simple derivation of the transfer gain.

$$\frac{V_{out}}{V_{in}} = \frac{R_2}{R_{LED}} * CTR \qquad \textbf{(2-15)}$$

The reason this circuit would be used, even with the presence of the CTR term, would be because the input does not use a power supply. The previous two topologies utilized isolated power supplies for the input and output. Depending on where they are used in the circuit this could mean a dedicated power supply just for one op amp. The topology in Figure 2.8 is useful in these applications where an isolated power supply would have to be used to power an op amp. If the input is very well understood and kept within a small range then the CTR term can be considered constant with very small variations on the input bias of the LED. This will minimize the effect of biasing on the CTR so it will be more predictable. Temperature will cause a problem in this circuit, especially if there is a constant current flowing through the LED, not allowing the optocoupler to cool over a period of time which will create more non-linearities in the output. The Optocoupler Characterization Experiments Chapter will define experiments to test this topology over temperature and biasing to understand the benchmark performance of this application circuit that can be implemented in the Buck converter.

2.1.3.2 Role Two: Digital Transmission

The digital transmission role of optocouplers is accomplished by using circuitry around the optocoupler that allows for a voltage to be applied to the input above a threshold and a corresponding rail to rail change on the output. A digital one will be represented by the upper rail of the output and a zero by the grounded rail of the output. There are many different configurations in this category but they all use some mechanism to first, greatly amplify the overall CTR and second, use a device that is

either on or off. This can be done using a BJT, Darlington pair, or even dedicated amplifiers. The most common and simple is a BJT configured with the photodiode supplying current to the base to turn the BJT on. The output current will have a gain of β in this case. Another common configuration is to have an amplifier with hysteresis as the output stage. The Darlington pair will not be analyzed because speed is one of the parameters that need to be optimized and Darlington pairs have very long reverse recoveries because of minority carriers in both transistors that must be swept out.

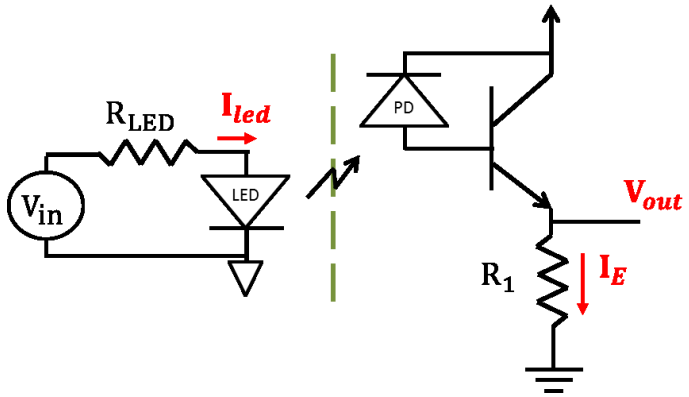


Figure 2.9 Emitter follower digital transmission topology

Figure 2.9 shows the emitter follower configuration. When there is not any current flow in the device the output BJT is off and the output on the emitter is connected to ground. When a voltage is applied to the input that causes enough current to flow in the output photodiode the BJT will turn on and the output will be connected to the supply rail. R_1 is used to bias the BJT so it does not reach saturation and can be switched on and off faster. Most data sheets will record the CTR as the ratio between the LED current and the collector current which causes the CTR term to be very large.

$$I_C=I_{led}*CTR*\beta \quad \textbf{(2-16)}$$

$$V_{CE}>1.4>V_{DD}-I_C*R_1 \quad \textbf{(2-17)}$$

$$CTR_2 = \frac{I_C}{I_{led}} = CTR * \beta \qquad \textbf{(2-18)}$$

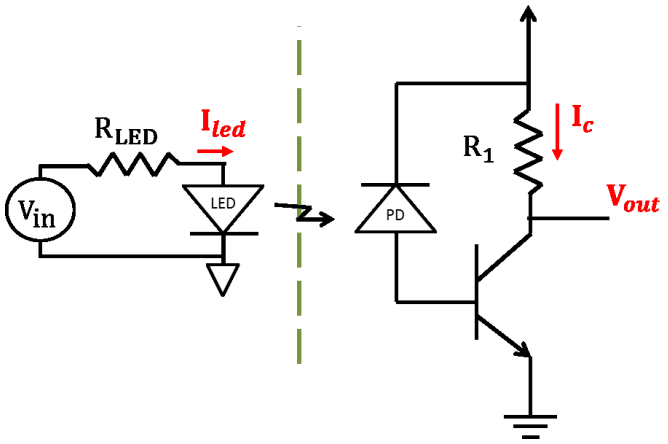


Figure 2.10 Common emitter digital transmission topology

The common emitter configuration shown in Figure 2.10 is very similar but the output is inverted from the input [13]. When there is no voltage applied on the input the output is connected to the supply rail and vice versa when a voltage is applied to the input. Most optocouplers in the digital realm operate better as common emitters because they are much faster, and because speed is important the emitter follower will not be analyzed to determine its benchmark. The figures of merit that will determine the benchmark is propagation delay, the minimum pulse width, and the power consumption. These are chosen because in an isolated transmission circuit speed is the limiting factor for the rest of the system and the power consumption determines the type of isolated supply is needed. GaN will be able to improve mostly the propagation delay because the other two are due to the technology of the BJT, but this topology will be analyzed as well so that the best digital scheme can be chosen for the all optical Buck converter design.

Something to note is the power consumption when the output is on. Both of these circuits draw power through the BJT to ground the entire duration they are on even if they supply a capacitive load.

$$P_{out} \cong I_C^2 * R_1 \quad \textbf{(2-19)}$$

This is where the amplifier output configuration can be useful. There are various different kinds of amplifier schemes used but they all operate in the same way. The photodiode is connected to some kind of drive circuit (usually through a Schmitt trigger) that drives a totem pole configuration. Another difference is the input. It can be either a bare LED or an amplifier controlling the LED biasing as seen in Figure 2.11 [11], [10].

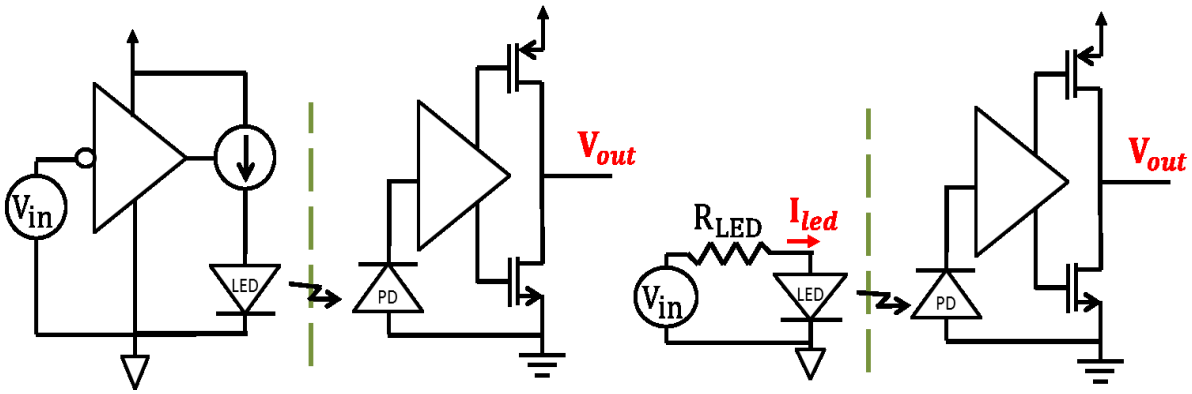


Figure 2.11 Two different digital optocouplers with different input stages and output amplifier configuration [11], [10]

The Optocoupler Characterization Experiments chapter will analyze the differences between these three types (LED and BJT pair), LED and amplifier pair, and amp-LED and amplifier pair) to determine the fastest and shortest pulse width available. There is no need to analyze the transfer functions because these devices are truly on and off devices.

It can be seen that the parameters of the overall transfer gain, propagation delay from input to output, bandwidth, fall and rise time, and isolation voltage are an aggregate of the components within the circuit. Op amp selection, along with passive component selection will affect the circuit's operation. The importance of defining these circuits is twofold: to determine the benchmarks of the overall circuits

with various optocouplers – seen in the Optocoupler Characterization Experiments Chapter – and to design an optical Buck converter that operates to its maximum switching frequencies and temperatures determined by current optocoupler technologies and circuit schemes. Now that all the application topologies for the two different categories are understood the Buck converter will be analyzed.

2.2 Buck Converter

The current-mode optically-controlled Buck converter can now be analyzed since the basic operation of the optocoupler and its applications that will be tested to determine a benchmark for current optocoupler technologies is understood. This section will break down the application system in which the optocouplers will be applied. The basic Buck converter's operation will be presented along with the current-mode control scheme.

The choices to apply the optocouplers in this specific system have to do with the needs that this system will create that can be satisfied by the optocoupler. The Buck converter has a switch that is not connected to ground. Since an *n*-type MOSFET will be used the gate will have to be 10 to 15 V above the source potential. Since the source is floating, the gate driver (to be presented in much greater detail in the next section) will have to be isolated from any other ground reference in either the Buck circuit or the control circuit. This will be called the high-side because the power supplied to the gate driver will be referenced to the source node of the MOSFET. Current-mode control will be explained in greater detail, but the overall reason for choosing it as the control scheme is because there are two feedback loops. The reason two feedback loops are desirable is because this thesis is not trying to determine the best Buck converter, but to determine how optocouplers affect a dc-dc converter when they are used to transmit information to the control circuitry. Current-mode control has two feedback loops that need to transmit a floating referenced current signal, and a ground referenced voltage signal. Using the optocoupler in these two completely different signal paths will give a better insight into its overall

capabilities. The first loop measures the output voltage and this sensed signal must be transmitted across the isolation barrier between the Buck converter circuitry to the control circuitry. The second loop is also referenced to the source node of the MOSFET and this loop will measure the inductor current and transmit it to the control circuitry through the isolation barrier. Figure 2.12 is a very basic graphical representation of all the different isolation barriers and blocks in the overall system. With this system in place the Buck converter can operate with an input voltage up to the withstanding voltage of the optocouplers and still have very low voltage, isolated control circuitry.

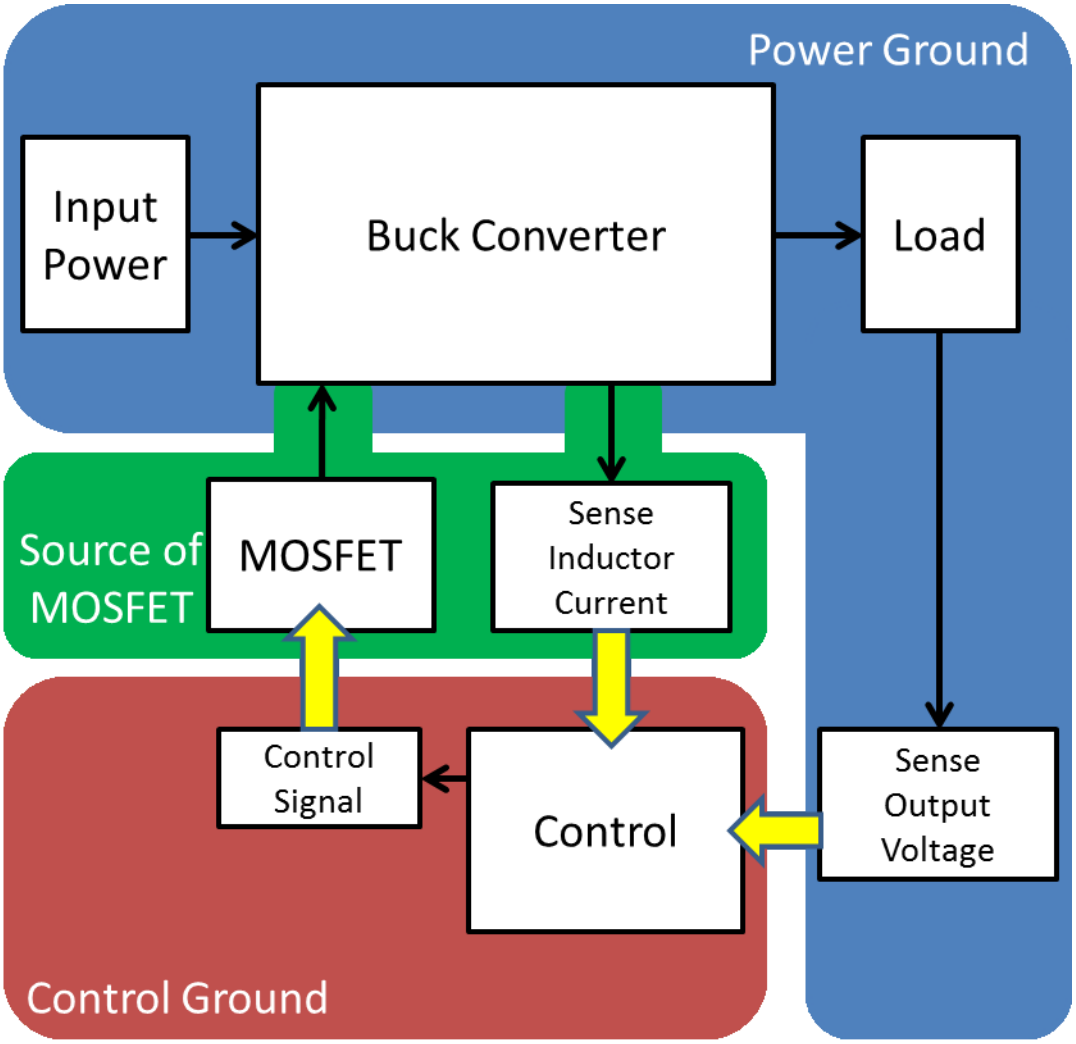


Figure 2.12 Graphical representation showing the control reference's isolation from 1) power ground (Buck converter and output load and voltage sensing), and 2) source of the MOSFET (gate driver and inductor current sensing reference) – yellow arrows are signals transmitted through the isolation barrier between the control circuitry and the rest of the circuitry

2.2.1 Buck Converter Operation

The Buck converter is a specific topology in the class of dc to dc converters. It is one of the building blocks for other, more complicated, converters. Figure 2.13 shows the schematic representation of an open-loop Buck converter. At steady-state the output voltage is held at a fraction

of the input voltage. When the loop is closed by feeding back the output voltage state to control circuitry the output voltage can stay at a specified value with varying input voltage and load conditions (this is called voltage mode control). The key component of the circuit is the switch. It turns on and off at a specific frequency, and the ratio of the on time to the period of the switching time determines the output voltage.

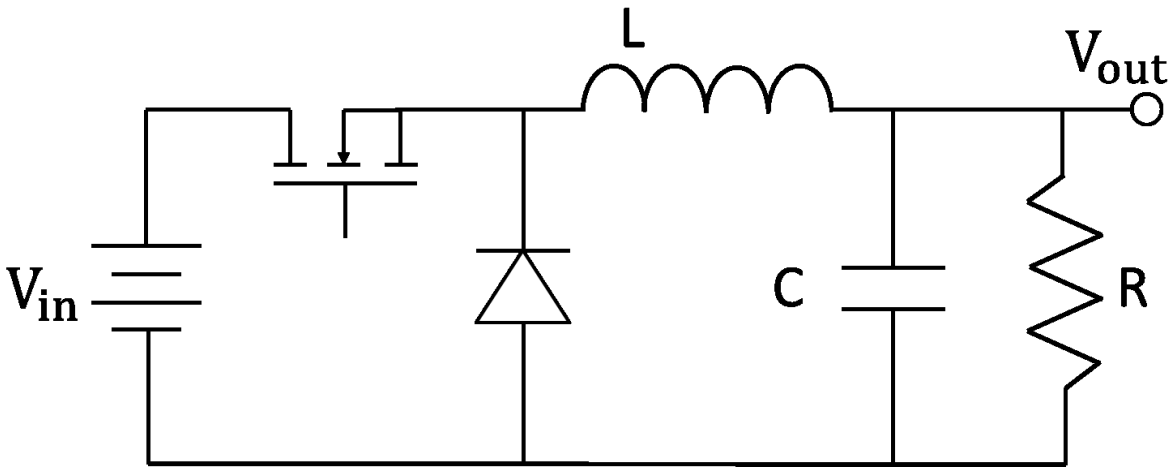


Figure 2.13 Open-loop Buck converter schematic

$$V_{out}=\left(\frac{t_{on}}{T}\right)V_{in}=D*V_{in} \qquad \textbf{(2-20)}$$

This ratio is called the duty cycle (D) and its relationship with the output voltage will be quantified thoroughly later. To understand the operation of the Buck converter the converter must be analyzed during the two different switching events, while the switch is on, which is mode one, and while it is off, called mode two [14]. There are also two different operating regimes of a Buck converter, continuous and discontinuous. This relates to the current in the inductor. In the continuous regime the current of the inductor is always positive and in the discontinuous regime the current in the inductor becomes zero before the end of the switching cycle [14]. The continuous regime is analyzed below and is used in the final system.

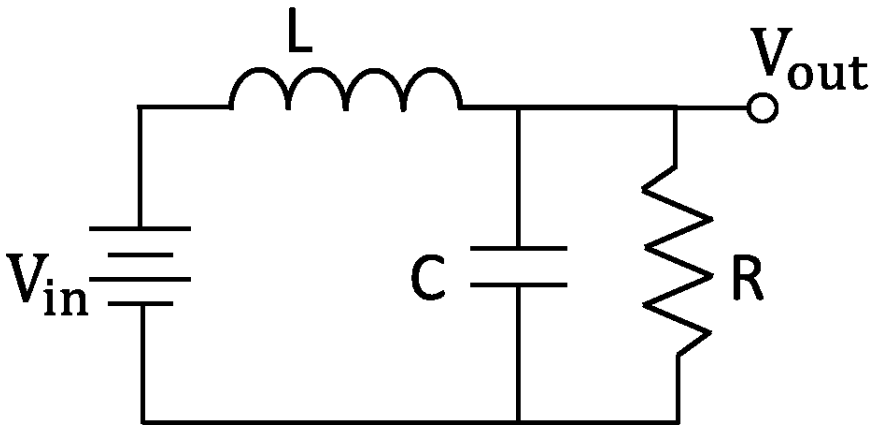


Figure 2.14 Equivalent circuit when switch is closed (mode one)

The beginning of mode one happens when the switch is closed. The equivalent circuit is shown in Figure 2.14. The input voltage is larger than the output voltage so the current through the inductor (L) ramps up and energy is stored in the inductor and capacitor. If the inductor is large enough the rise in inductor current is approximately linear [14].

$$V_{in}-V_{out}=L\frac{di_L}{dt}=L\frac{I_2-I_1}{t_{on}}=L\frac{\Delta I}{t_{on}} \qquad \textbf{(2-21)}$$

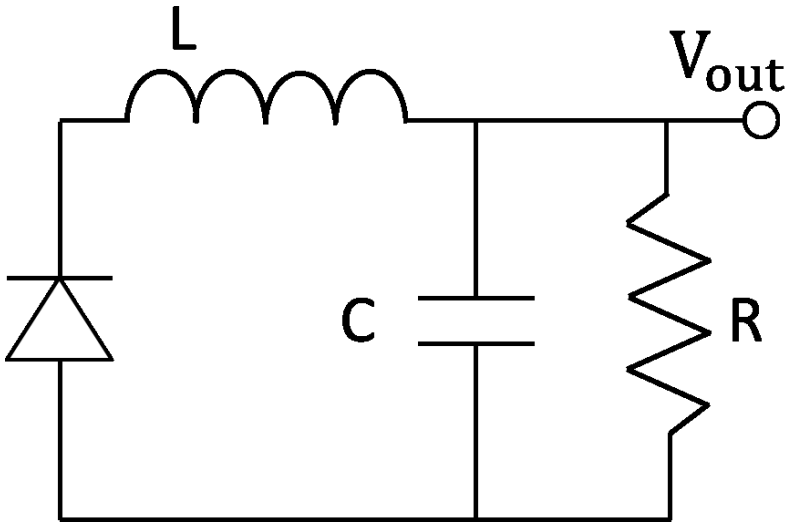


Figure 2.15 Equivalent circuit when switch opens (mode two)

When the switch opens mode two begins. The equivalent circuit is shown in Figure 2.15, it can be seen that this mode is characterized by the stored energy in the inductor and capacitor discharging through the resistor. The diode allows the current in the inductor to flow continuously when the switch is turned off, since it is not possible for the current in the inductor to change instantaneously. To maintain this current the voltage polarity across the inductor reverses. The inductor current decays (approximately linearly if L is large enough) from I_2 to I_1 in this mode [14].

$$-V_{out}=L\frac{di_L}{dt}=L\frac{I_1-I_2}{t_{off}} \quad \textbf{(2-22)}$$

$$V_{out}=L\frac{I_2-I_1}{t_{off}}=L\frac{\Delta I}{t_{off}} \quad \textbf{(2-23)}$$

Now the average output voltage can be found by solving the equation for mode one and two for ΔI and setting them equal to each other. The duty cycle (D) is the ratio of the on-time to the period of the switching time determines the output voltage, $D=\frac{t_{on}}{T}$, and the period is the sum of the on- and off-time, $T=t_{on}+t_{off}$ [14].

$$\Delta I=\frac{(V_{in}-V_{out})t_{on}}{L}=\frac{V_{out}t_{off}}{L} \quad \textbf{(2-24)}$$

$$(V_{in}-V_{out})DT=V_{out}(1-D)T \quad \textbf{(2-25)}$$

$$V_{out}=D*V_{in} \quad \textbf{(2-26)}$$

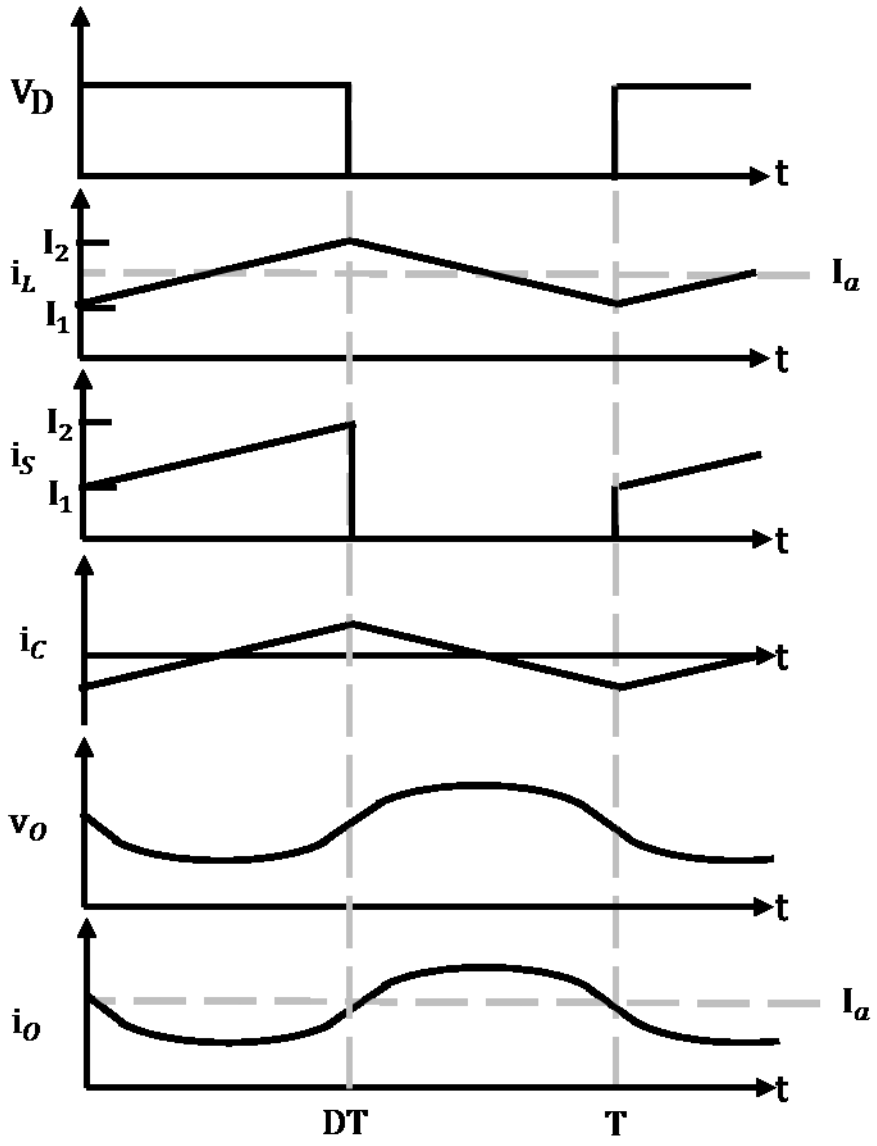


Figure 2.16 Waveforms for Buck converter [14]

The waveforms of the duty cycle, load current (i_o), and output voltage (v_O), are shown in Figure 2.16. The output voltage is related directly to the duty cycle and the input voltage. If the on-time of the switch is half of the off-time then the output voltage will be half of the input voltage at steady state. This is just the average value; there are also ripples in the current (ΔI) and voltage (Δv_c) because of the charge and discharge actions of the inductor and capacitor.

$$T=\frac{L\Delta I}{V_{in}-V_{out}}+\frac{L\Delta I}{V_{out}}=\frac{LV_{in}\Delta I}{V_{out}(V_{in}-V_{out})} \quad \textbf{(2-27)}$$

$$\Delta I=\frac{DV_{in}(1-D)}{f_s L} \quad \textbf{(2-28)}$$

$$\Delta v_c=\frac{1}{c}\int_0^{\frac{T}{2}}\frac{\Delta I}{4}dt=\frac{\Delta I}{8f_s C}=\frac{V_{in}D(1-D)}{8f_s^2 LC} \quad \textbf{(2-29)}$$

Eq.'s (2-27) – (2-29) show that as the inductor and capacitor increase the current and voltage ripple will decrease. These are important design equations that will be used to determine the ripples of the final system. All of these equations are correct for steady-state operation, but how does the effect of line or load changes and start-up affect the open-loop Buck converter? Without controlling the duty cycle this circuit will be unstable in open-loop. The loop is closed by using system variables, in this case inductor current and output, or capacitor, voltage to control the duty cycle. This technique is called current-mode control [1].

2.2.2 Peak Current-Mode Control Feedback

It is desired to hold the output voltage constant even if the input voltage has a transient or changes to a different voltage level indefinitely. Following Eq. (2-20), without controlling the duty cycle of the converter the output voltage will follow the changes in the input voltage directly. Also, if the load changes and starts to draw more or less current the output voltage would change if the duty cycle in Eq. (2-20) was not controlled for that transient. It is possible that the open-loop Buck converter would reach its steady-state output voltage again, but it might also go unstable and stop functioning properly. The goal of any control system for a Buck converter is to control the on- and off-time of the switch at a given frequency to maintain a constant output voltage in lieu of line or load changes. Pulse width modulation (PWM) is used to vary the duty cycle by controlling the on- and off-time of the switching transistor. This is a square wave signal that can be a fixed or variable frequency signal. A fixed frequency signal is generated by changing the on- and off-time of the switch while maintaining a constant period. To do this

the switch is turned on at a fixed period so the duration of the on-time determines the amount of off-time. A variable frequency is generated by keeping the on-time fixed and varying the off-time [14].

Generally there are numerous schemes to do this broken up into two main categories, voltage- and current-mode control. Within the two categories there is a variety of more specific schemes. To simplify this background section only current-mode control will be discussed because it is the only scheme that is used. This is not the procedure for designing the optimal Buck converter, but because this design's purpose is to create an application to demonstrate an all optical control scheme, current-mode control is better because of its multiple feedback loops.

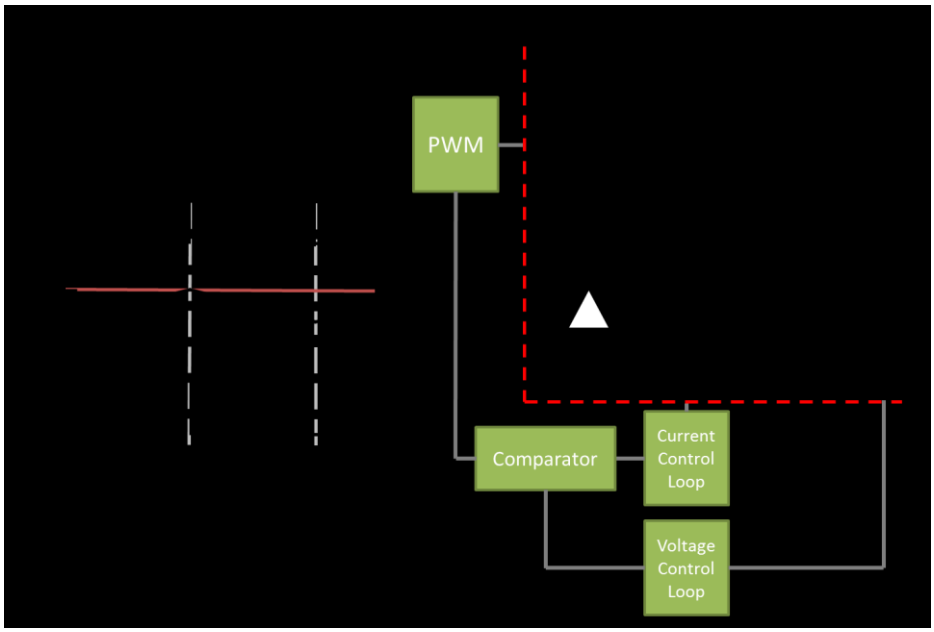


Figure 2.17 Block diagram showing two loop feedback system of the peak current mode control scheme

Current-mode control basically senses the inductor current and compares it to the output voltage to generate a PWM that controls the switches duty cycle. The comparator commands a square wave to turn off and an external oscillator commands the square wave to turn on, thus creating a PWM.

The inner current loop senses the inductor current, scales, adds compensation (discussed later), and compares it to the error voltage generated in the outer voltage loop. Figure 2.17 shows a simple schematic for current-mode control and the waveforms that go along with it. The error voltage generated in the voltage loops becomes the upper limit to the inductor current. When the inductor current intersects the error voltage the PWM signals the switching transistor to turn off. This function's obvious advantage is that it allows for cycle to cycle overcurrent protection. The switch is then turned on again by an external clock to set a fixed period. So the duty cycle is controlled by how fast the current intersects the error voltage [1]. One additional element that current-mode control needs is slope compensation. This compensates for the sub-harmonic oscillations that are present in the current of the inductor when the duty cycle is greater than 50% [15].

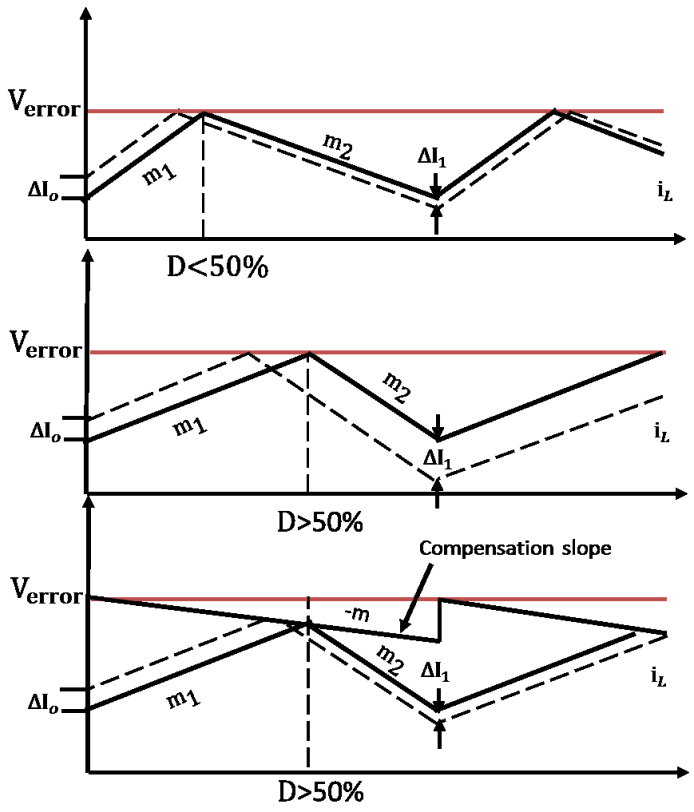


Figure 2.18 Waveforms showing the problem of sub-harmonic oscillations [15]

In Figure 2.18 the waveforms of the inductor current signal being compared to an error voltage are shown. In the top graph the duty cycle is less than 50% so any oscillation (shown as ΔI_o) in the current will die out over multiple cycles quantified in Eq. (2-30) [15].

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right); m_1 > m_2 \quad \textbf{(2-30)}$$

If the duty cycle increases beyond 50% the oscillations will grow each cycle, as shown in the middle graph of Figure 2.18. The equation below quantifies this behavior [15].

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right); m_1 < m_2 \quad \textbf{(2-31)}$$

With the same duty cycle an additional slope (slope compensation) is added to the current signal (or subtracted from the error voltage, depending on the implementation method), and the bottom graph shows that with even a duty cycle greater than 50% the oscillations are attenuated each cycle. Eq. (2-32) shows this quantitatively by adding slope to the current signal [15].

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2+m}{m_1+m}\right); \text{solving for m at 100\% duty cycle} \quad \textbf{(2-32)}$$

$$m > -\frac{1}{2} m_2 \quad \textbf{(2-33)}$$

Implementing slope compensation will be discussed with the design of the current-mode optically-controlled Buck converter because there are various methods depending on configuration of the current sensing network and the external clock. The main reason current-mode control is chosen over voltage mode control is because of the need for high-side current sensing. At high voltages this becomes a problem because the reference node for sensing the current is at a high, floating, voltage. Optocouplers with high speed transmission of analog signals are needed to overcome this problem.

2.2.3 Optocoupler's Role in the Buck Converter

Understanding the application topologies of the optocouplers and how current-mode control is implemented in a Buck converter the need for optocouplers can now be seen. The current-mode control needs the inductor current and output voltage information. But as in Figure 2.12 (the overall block diagram) it is seen that both of these signals are referenced to different potentials in the power stage part of the circuit. This information needs to be transmitted through the isolation barrier to the control part of the circuit. Once there the information is processed to determine the correct duty cycle to apply to the Buck converter to maintain a stable output voltage. Now that the duty cycle is determined the switching commands need to be sent back across the isolation barrier to the isolated gate driver on the power stage side of the circuit. The different application topologies of the optocoupler will be implemented to transmit both the inductor current and output voltage along with sending the switching commands to the gate driver. Figure 2.19 shows a block diagram of the optocoupler's location in the Buck converter closed loop system as blue arrows pointing in the direction of signal flow through the isolation barrier. The only missing block in this diagram is the gate driver. Another section is needed to fully describe the gate driver.

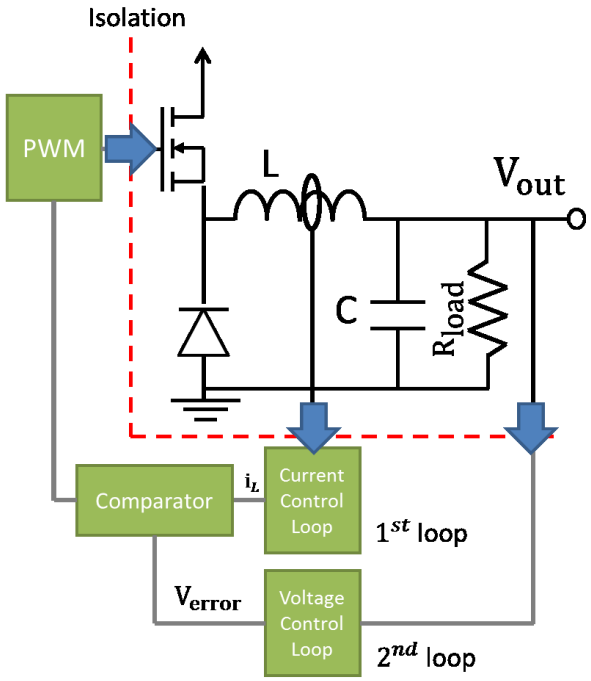


Figure 2.19 Current mode optically controlled Buck converter with blue arrows showing placement of optocouplers. Take note of the type of signals transmitted for each optocoupler (digital gate signal and two analog system variables).

2.3 Gate Drivers

The gate driver is important for multiple reasons; the first of which is to the Buck converter. The MOSFET must be turned on and off with a device that can buffer the low power PWM signal to the power level needed to turn on a MOSFET quickly. Another reason is to expose the digital optocouplers minimum pulse width. The optocoupler will need to transmit the PWM information through the isolation barrier to the isolated power supply with a minimum pulse width. Two gate drivers that need two separate on and off commands (requiring two separate optocouplers) with small pulse widths will be compared (with a conventional gate driver as a control) to determine which one is applicable to this design. A tertiary reason is to determine the lowest power consuming gate driver in the collaborative research with South Carolina.

As stated earlier the switch in the Buck converter does not have a source referenced to ground. A PWM signal referenced to the control circuitry ground is used to tell the switching transistor in a switch-mode power supply when to turn off and on, but there is a problem. The MOSFET needs about a 15 V difference between the gate and source terminals for it to turn completely on and the voltage to keep the gate off will have to be equal to and typically below the source voltage while it is floating. The optocoupler will allow for a control ground referenced PWM signal to be transmitted through the isolation barrier so that on the output it is referenced to the source's reference point, but there is another problem. The PWM signal on the output of the optocoupler can usually only source or sink milliamps of current and for a power MOSFET to be turned on and off in the nanosecond range it will needs Amps of current. This is where the isolated gate driver will occupy. It will be a buffer between the low power PWM signal and high power needed to turn the gate of a MOSFET on quickly. To better understand the gate driver's purpose of buffering the PWM signal the turn on and off of a gate driver must be understood, the next section discusses the way a MOSFET turns on in more depth.

2.3.1 MOSFET Turn-On Analysis

The turn on procedure of a MOSFET needs to be understood to realize the need and purpose of a gate driver. Figure 2.20 shows the schematic used to describe the switching transient of a power MOSFET. The load inductance charges to the drain current of the power MOSFET while it is on and the current discharges through the freewheeling diode when the MOSFET is off. The change in the inductor current during charge and discharge is very small during one switching cycle [7].

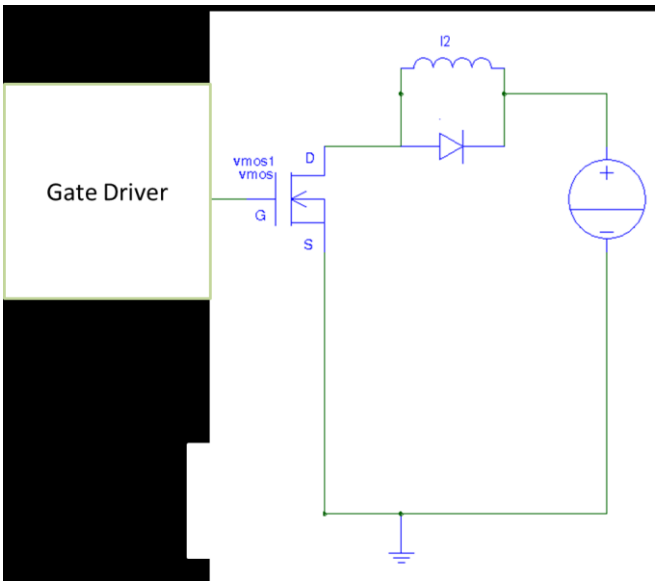


Figure 2.20 Clamped inductive load test setup

The switch is initially off and the load current flows through the diode. The gate voltage (v_G) and drain current (i_D) equals zero while the drain voltage (v_D) equals the input voltage (V_{DD}). The gate driver is also turned on and starts to charge the capacitances (C_{GD} and C_{GS}) of the power MOSFET. No drain current can flow until the gate-source voltage (v_{GS}) exceeds the threshold voltage of the device so the drain voltage stays at V_{DD}. Because the drain voltage is constant this means that C_{GD} stays constant. So until drain current begins to flow only C_{GS} is charging. The gate voltage reaches the threshold voltage at t_1 in Figure 2.21. At this point drain current starts to flow but the drain voltage remains constant because, until the MOSFET can accept the entire load current, the freewheeling diode cannot sustain a voltage other than its forward voltage [16].

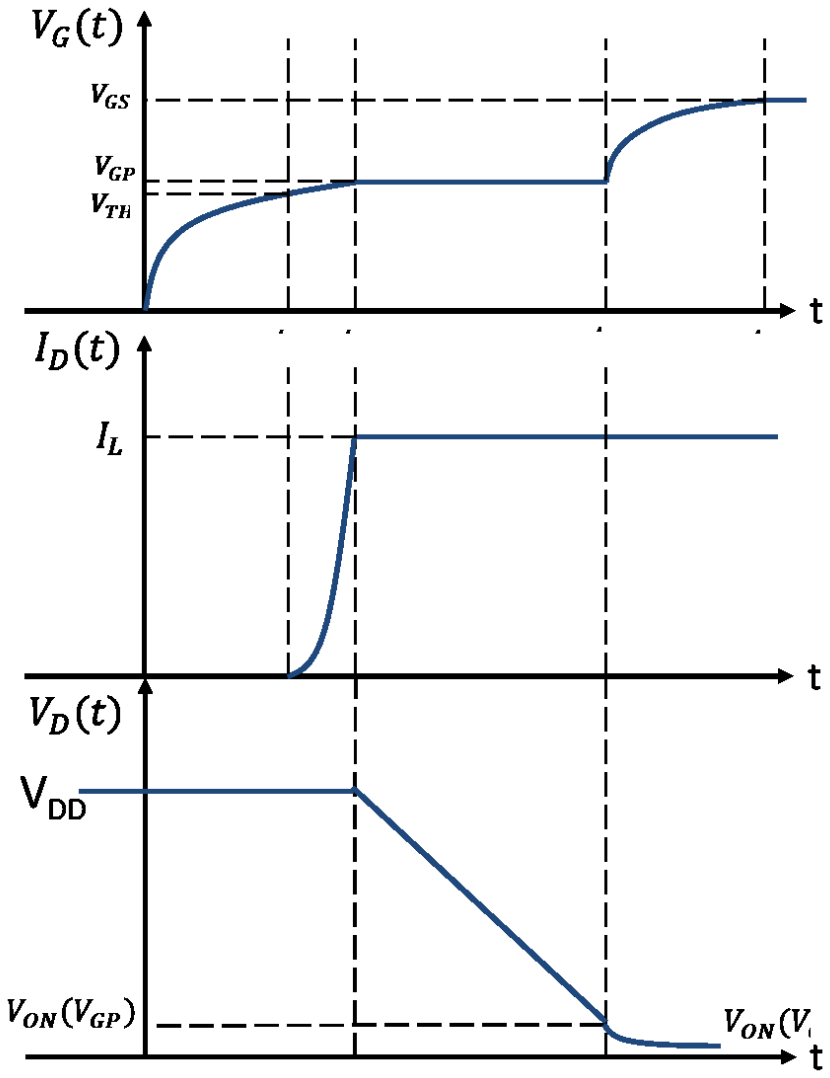


Figure 2.21 Turn-on waveforms for MOSFET [16]

At t_2 in Figure 2.21 the drain current equals the load current and now the drain voltage starts to decrease toward the forward voltage of the MOSFET ($V_{ON}(V_{GP})$). It can be seen that the gate voltage flattens out while the drain voltage decreases to the on-state voltage between t_2 and t_3. This is due to all of the gate current charging the gate-drain capacitance; this is called the Miller capacitance. The drain voltage becomes equal to the on-state voltage of the MOSFET with a gate voltage of V_{GP} at t_3 where the gate voltage, again, increases to the voltage applied by the gate driver, V_{GS} [16]. The turn-off

transient is similar enough in operation to the turn-on operation that it will not be described in full detail here but the reader is directed to [16] for an in-depth analysis. The gate driver is the main focus in this section and in the circuits that will be analyzed the turn-off procedure is symmetrical to turn-on, even in the presence of slightly different phenomena that occur in the turn-off transient of the MOSFET.

It can be seen that the gate voltage increases in a finite amount of time determined by the time it takes to charge C_{GS} and C_{GD}. Three different gate drivers are presented below that will control this charge time, the conventional gate driver, a resonant switching gate driver, and finally a resonant switching gate driver with an energy recovery function [2], [17]. The first gate driver is the most basic gate driver and it is presented to get a basic understanding of the procedure a gate driver goes through to turn on and off a MOSFET and to be a control to compare the other two more exotic gate drivers to. The next gate driver is presented in [17] uses resonance to charge the gate capacitances. This is analyzed because with resonant switching the peak current can be shaved and the input power decreased [17]. The final gate driver uses resonance and then a freewheeling diode scheme to return energy stored in the inductor back to the source and is presented in [2]. Power consumption is important because the power supply to the gate driver is a separate isolated power supply referenced to the source of the MOSFET and must be supplied through means of the isolation techniques that have been discussed. This technique to use optocouplers for sending isolated power will not be analyzed further in this thesis because this is another component of research being done by the University of South Carolina. The gate driver selection is important in the research presented here because either one chosen needs the small pulse width pulses that will help determine the baseline performance of the digital transmission optocouplers.

2.3.2 Specific Gate Drivers Examined

In these three gate drivers the operation will be analyzed. What is not shown is how the switches in the gate driver are turned on and off. This will be discussed further in a different section because it is a topic in itself and has to do with the overall design of the full system.

2.3.2.1 Conventional Gate Driver

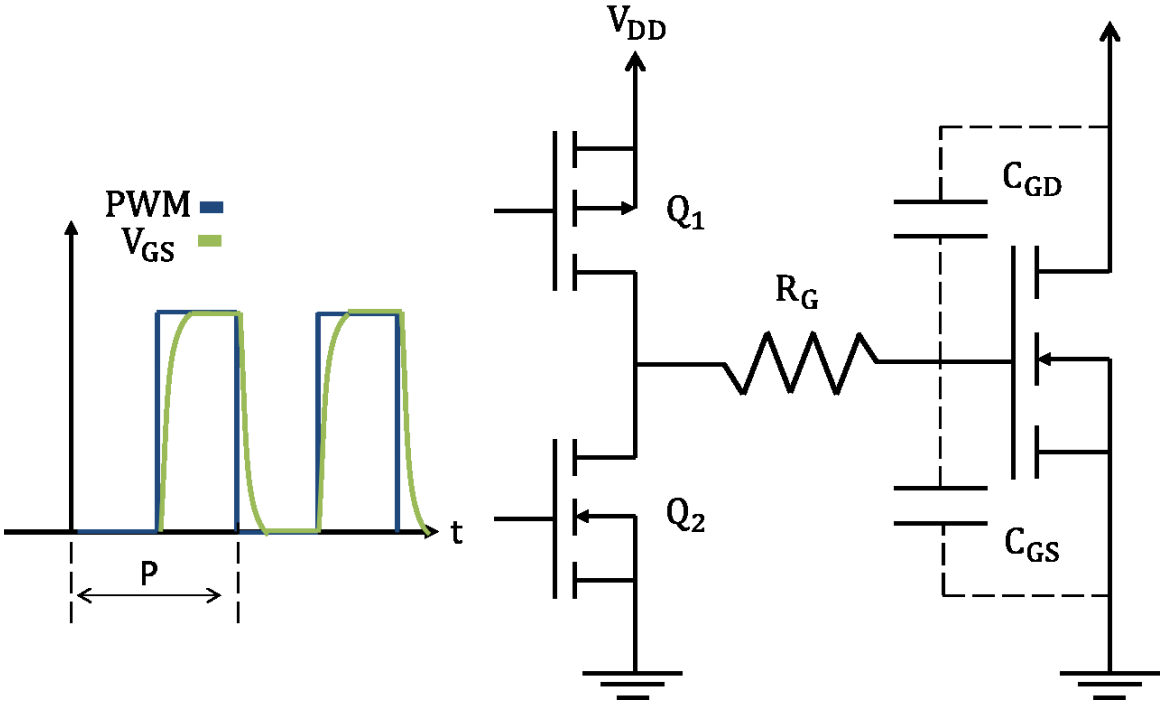


Figure 2.22 Conventional gate driver with basic waveforms

The conventional gate driver is a well-known, fundamental topology with a half-bridge (or totem pole) configuration of two complimentary switching transistors, Q_1 and Q_2. The PWM signal turns on and off Q_1 and Q_2 to control the switching event of the MOSFET shown in Figure 2.22. When the PWM is high the top MOSFET is on and when the PWM is low the bottom MOSFET is on. The MOSFETS are never allowed to be on at the same time. The circuit operates by sourcing current through the gate resistor to charge the gate source capacitance of the MOSFET to V_{DD} when Q_1 is on. The high-side transistor must

stay on to maintain the MOSFET in its on-state. To turn the MOSFET off the high-side transistor turns off and the low-side transistor turns on, connecting the gate terminal of the power FET to the source terminal of Q_2 and discharging the gate source capacitance to the source potential of Q_2, so that V_{GS} is zero.

2.3.2.2 Resonant Gate Driver

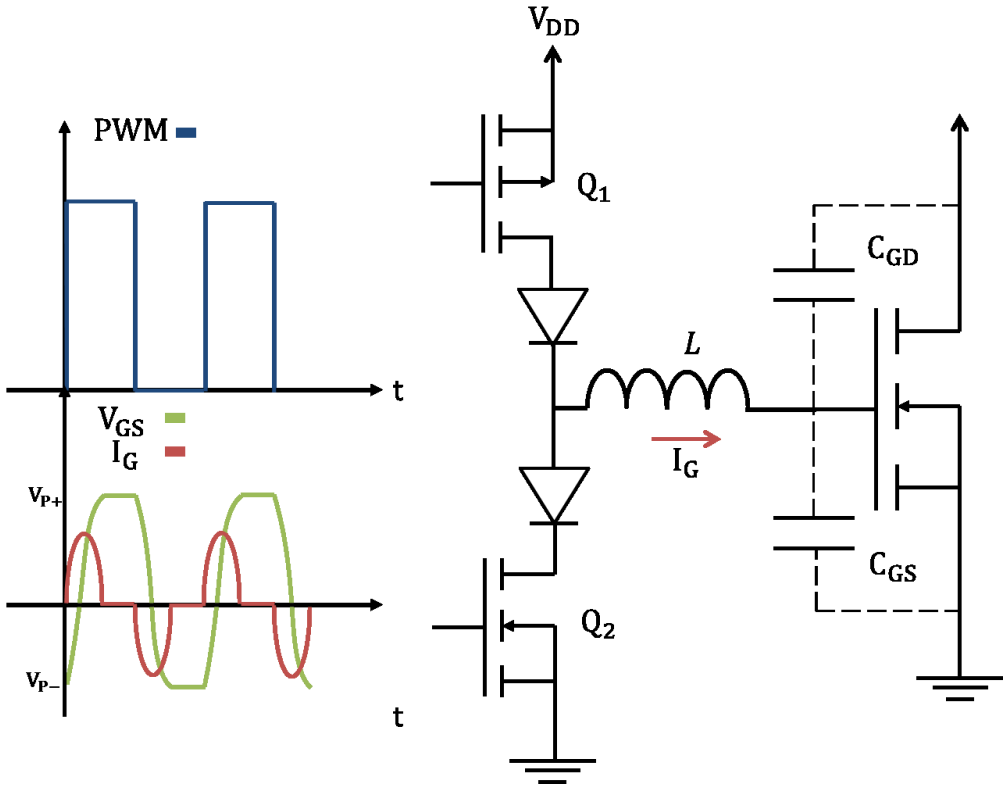


Figure 2.23 Resonant gate driver with basic waveforms [17]

This gate driver adds two diodes and an inductor into the path of the current shown in Figure 2.23. The turn on and off action of this gate driver is characterized by a resonant transition. "Initially Q_1 is on and Q_2 is off, and V_{GS} is at a negative peak (V_{p-} in Figure 2.23)" [17]. The transistors change switching positions and current flows through Q_1 and into the negatively charged C_{GS} storing energy in the inductor. The current flowing through the inductor peaks as V_{GS} reaches zero. The energy stored in

the inductor begins to discharge into C_{GS} causing V_{GS} to rise above zero as current decreases. V_{P+} is reached when the current in the inductor is fully dissipated and will be greater than V_{DD}. This is allowed because the diode will block any possible discharge path. The turn off operation is the same with current flowing in the reverse direction. Again the gate voltage is charged to a voltage less than the ground reference due to the resonant action and the diode [17].

2.3.2.3 Energy Recovery Resonant Gate Driver

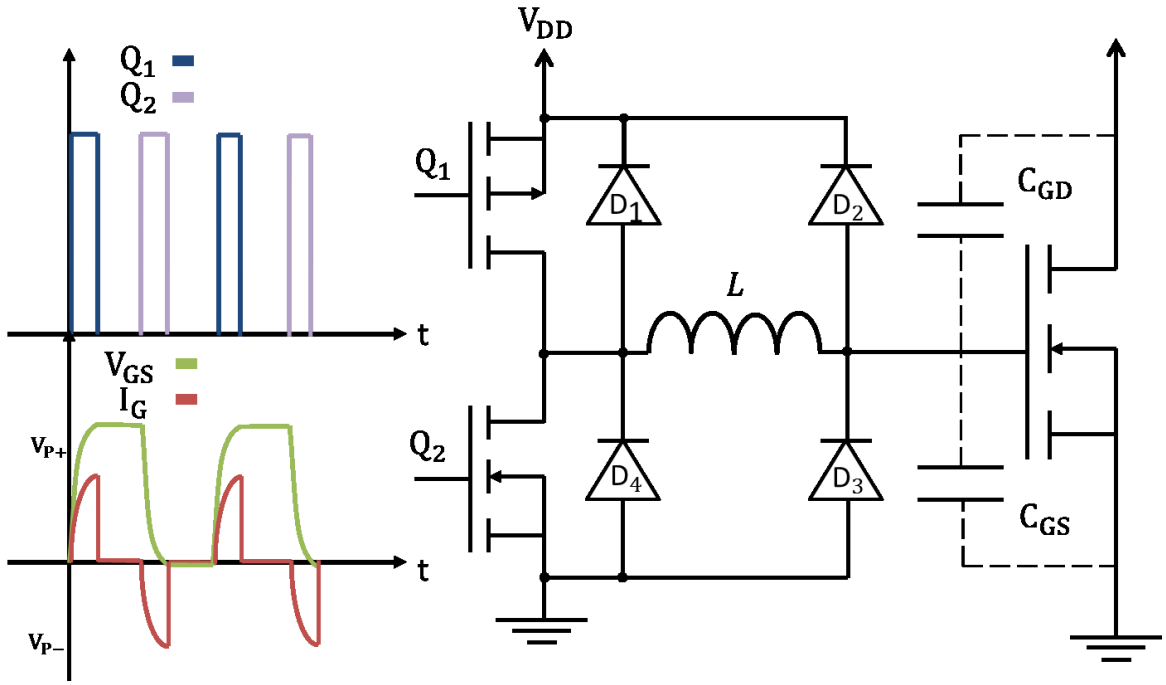


Figure 2.24 Energy recovery gate driver with basic waveforms [2]

The difference in resonant gate driver in Figure 2.24 is its ability to capture energy in the resonant transition and recover it using two added freewheeling diodes. While Q_1 is on the gate capacitances resonate with the inductor charging the gate to V_{DD}. When the gate reaches this voltage the current is at a peak and the D_2 diode clamps the gate from be charged any higher than V_{DD}. When Q_1 is turned off the current in the inductor cannot change direction and causes the freewheeling diodes (D_2,D_4) to conduct which returns the energy stored in the inductor back to the source. This is the energy

recovery action of the circuit. It is important to note that to return the energy the MOSFET must be turned off; otherwise the energy will circulate between the inductor, D_2, and the MOSFET, being dissipated by the stray resistances. The turn off event is exactly the same but with Q_2 and D_1,D_3 acting in the discharge and energy recovery paths [2].

Also, the control scheme for the two resonant gate drivers needs to be described because it differs largely from the control scheme of the conventional gate driver topology. This is due to the need to have a single pulse for the on command and another, separate pulse, for the off command. By comparison the conventional topology only needs one signal to drive both the *p*-type and *n*-type MOSFETs.

Specifically for the energy recovery gate driver the energy recovery action cannot occur until the circulating current is directed back to the source by turning off all MOSFET's as talked about above, so the MOSFET is only pulsed the duration of the on or off time [2]. Adding the separate pulse control scheme adds some complexity in controlling this gate driver.

2.3.3 Controlling Gate Driver Switching Events

A half-bridge is the control action of the gate driver's above, a simple cascade of MOSFETs with the common connection between the two as the output. It is a simple topology that controls the flow of power to the output. If the high-side (HS) MOSFET is on power flows to the output and if the low-side (LS) MOSFET is on the output is connected to ground. An avoided event is when both MOSFETs are on. This short circuits the supply to ground through the on-resistances of the two MOSFETs producing large currents that can damage the switches and the power supply depending on the duration of the event. The half-bridge is a useful topology to charge and discharge the gate of a MOSFET. The MOSFETS can either be CMOS (LS NMOS and HS PMOS) or a fully NMOS configuration.

The CMOS configuration is simpler to control because it takes advantage of the fact that the PMOS gate must be at a lower potential than the source to conduct and the NMOS gate needs a higher potential on the gate relative to the source. Even though control is simplified there are many disadvantages. PMOS has a slower turn on time and their conduction resistance is higher. The solution is using an NMOSFET in place of the PMOSFET. The disadvantage to this scheme is the voltage of the gate on the HS MOSFET needs to float above the source node to be turned on. A simple solution is using a method called boot-strapping, Figure 2.25 shows the schematic for a simple boot-strapping network [3].

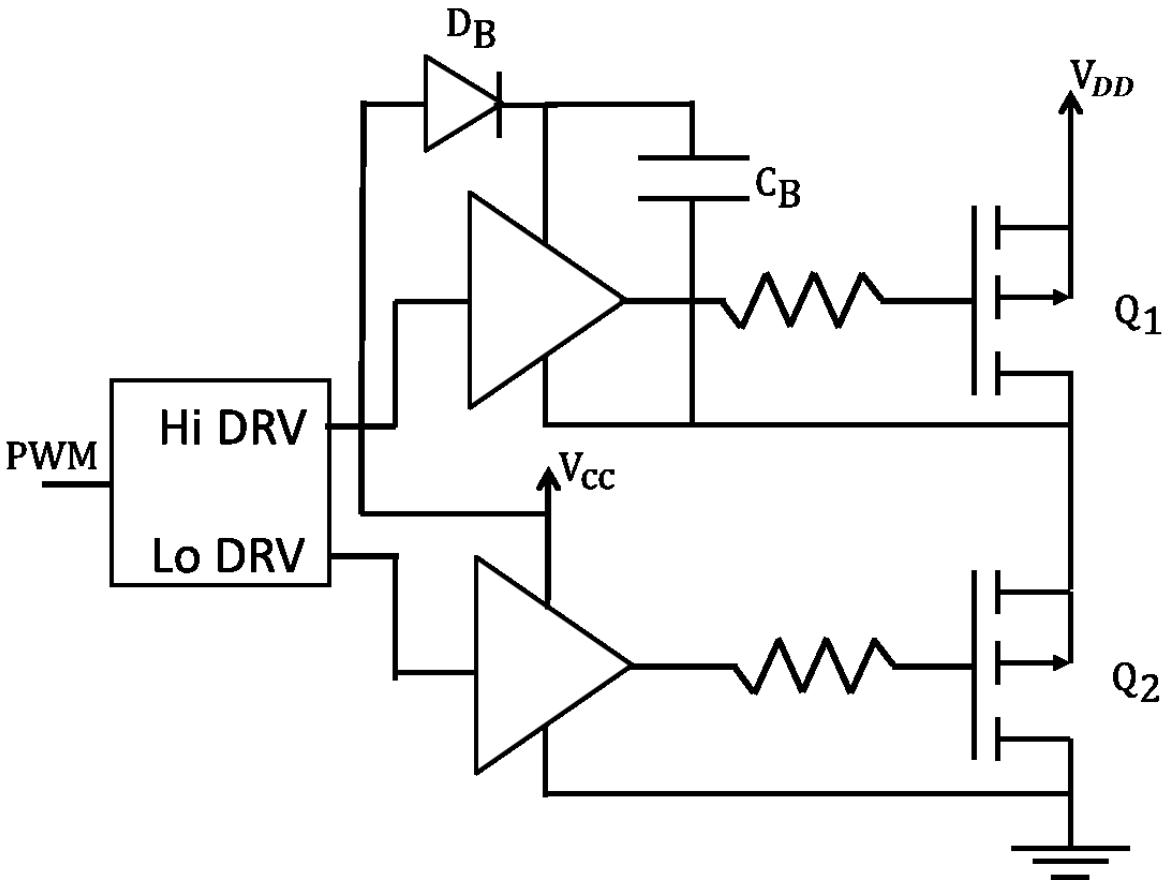


Figure 2.25 Bootstrap circuit for half-bridge topology [3]

Bootstrapping works by using the rule of a capacitor that its voltage cannot change instantaneously. First, Q_2 is on and the output is pulled to ground through this transistor. Q_2 being on

first is important because it also allows the bootstrap capacitor C_B to charge to V_{cc} through the diode. When Q_2 turns off and Q_1 is commanded to turn on the bootstrap diode D_B stops C_B from discharging and the voltage potential V_{cc} is across the source of the HS NMOS and its gate. If C_B has much greater charge than is needed for the HS NMOS C_{GS} then the gate will be charged to $V_{cc}+V_{source}$, thus turning it on. Any charge that was lost on C_B will be replaced when Q_2 turns on again [3].

This chapter discussed the theory behind the functionality, control, and operation of three gate drivers that will be used to operate the MOSFET in the Buck converter. The basic operation of the Buck converter was analyzed along with the control method and the value optocouplers will add to the overall design. The optocouplers natural parameters where analyzed along with the two different categories, analog and digital transmission, and the topologies that allow that operation. The next chapter will evaluate the gate driver that consumes the least amount of power in simulation and the design choices made in its PCB construction to be used in the final system. Another chapter, Optocoupler Characterization Experiments, is dedicated to the experimental setups that are used to determine the benchmark of the currently available optocouplers operating in the most fundamental topologies and discussing the results from these experiments. Once the individual optocoupler topologies are understood the Buck converter with optocouplers implemented in the full system will then be designed. The design procedure will be analyzed and presented to choose both the needed parts for the open-loop Buck converter, its feedback and control circuitry, and the optocoupler topologies that will be used to implement the isolation. Finally, in the Conclusions Chapter, the impact of optocouplers on the Buck converter system is discussed and the final benchmark for the optocouplers is presented.

3 GATE DRIVER DESIGN

The goal of this chapter is to determine the gate driver with the least power consumption and determine the most stable two pulse gate driver. As stated in the previous chapter, it is important to minimize the power that is needed for the isolated power supply that powers the gate driver because it will need to be generated independently from the power supply for the control circuitry or Buck converter. Also, stability is important to the operation of the system with non-ideal components that introduce noise through parasitics that can disrupt the operation of the gate driver.

3.1 Stage One: Validation of Gate Driver Designs

The gate driver design goes through three different stages: from the initial simulation tests to evaluating the best gate driver for the system with a non-ideal simulation, and finally, a gate driver on a printed circuit board (PCB). The first stage is validating with a simulator that the resonant designs presented in the two papers cited will work.

The next stage is implementing a more realistic model in the simulator with more non-ideal components focused on obtaining the total power consumption. This will include using a fully modeled MOSFET for the load of the gate driver. The SiC MOSFET is chosen for the final design because of its commercial availability and the in house model designed by Mihir Mudholkar at the University of Arkansas. This SiC MOSFET will be the switch that needs to be controlled in the Buck converter. Table 3.1 shows its notable parameters [18].

Table 3.1 SiC MOSFET Parameters [18]

SiC MOSFET Parameters	
Irated	20 A
Breakdown Voltage	1200 V
Nominal On Gate Voltage	18 V
Total Gate Charge	90.1 nC
C_{iss}	1.9 nF

With the non-ideal implementation the two resonant designs will be compared with the conventional design to see if they truly improve over hard switching in the simulations. The design with the best performance will be implemented in hardware, and the final stage will be designing and testing the best gate driver on a PCB. This section will give simulation results so that a choice on the best gate driver can be made for the design of the Buck converter, and the following sections will display the results of the gate driver implemented on a PCB.

Something to notice initially is the desired turn on voltage of the SiC MOSFET. A graph, shown in Figure 3.1, is made of the on-resistance of the SiC MOSFET on the y-axis, and the on-voltage on the x-axis to determine the lowest on-voltage that can be utilized. The purpose of this is to decrease the requirements of the gate driver's power supply at the smallest cost to conduction losses. The gate voltage is optimized at 15 V because between 15 and 20 V the on-resistance changes from 150 mΩ to 100 mΩ. Also, increasing to 16 V only provides a 16% decrease in the on resistance while decreasing the gate voltage to 14 V there is about a 25% increase. Because of the test setup for the full Buck converter system a compromise had to be made and the final gate voltage selected is 10 V. This is due to the upper limit of the voltage supplies that will drive the gate of the power FET is 10 V. The drain current is only going to be 5 A so the on-resistance will still be less than 1 Ω. If this thesis was to determine the optimum Buck converter this compromise would not be possible. But, the 1 Ω on-resistance that a 10 V gate voltage will cause is not a hindrance in this system because the power of the Buck converter will not be analyzed. The only important aspect is that the power FET can operate at the voltages levels that are needed to fully test the optocouplers, and that it doesn't impede the switching frequency of the Buck converter before the optocoupler transmission circuitry does.

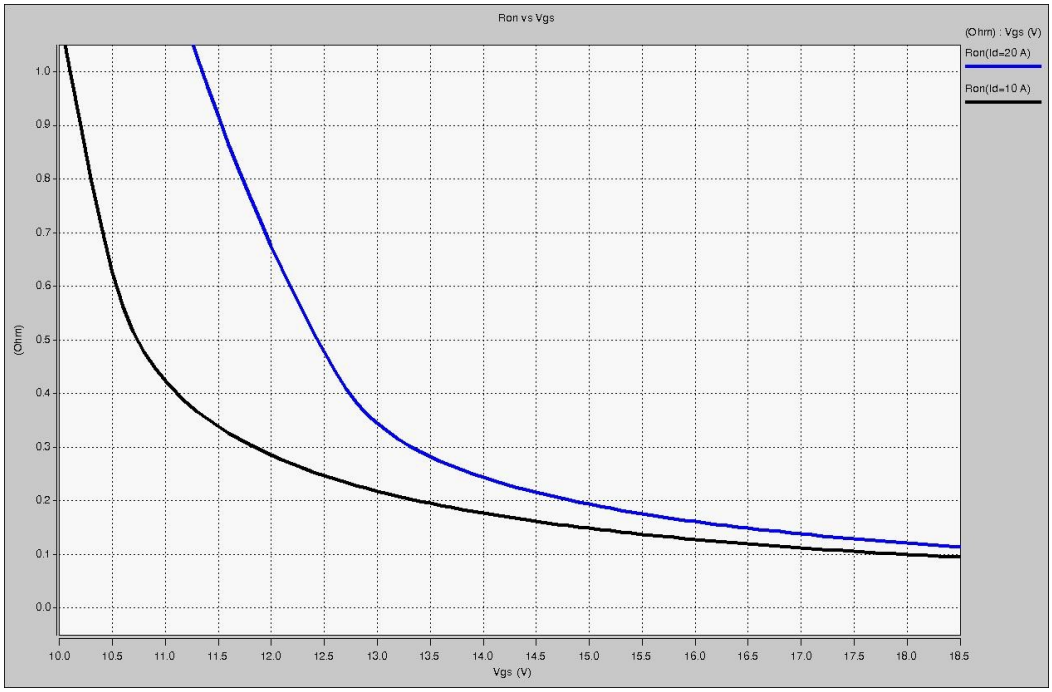


Figure 3.1 On-resistance vs. gate voltage derived from SiC MOSFET model

Some simplifications are made to the circuits to quickly validate the gate driver designs. A capacitor is put in place of the gate of the MOSFET to represent the C_{gs} of the SiC MOSFET. The total input capacitance is 1915 pF [18].This simplification takes away the Miller capacitance effect discussed in Chapter 2. Voltage-controlled switches are put in place of the half-bridge MOSFET configuration. The voltage-controlled switches are used because for validation a full MOSFET model is not needed and too complex to troubleshoot the main function of the gate driver, charging and discharging the gate to source capacitance.

3.1.1 Conventional Gate Driver

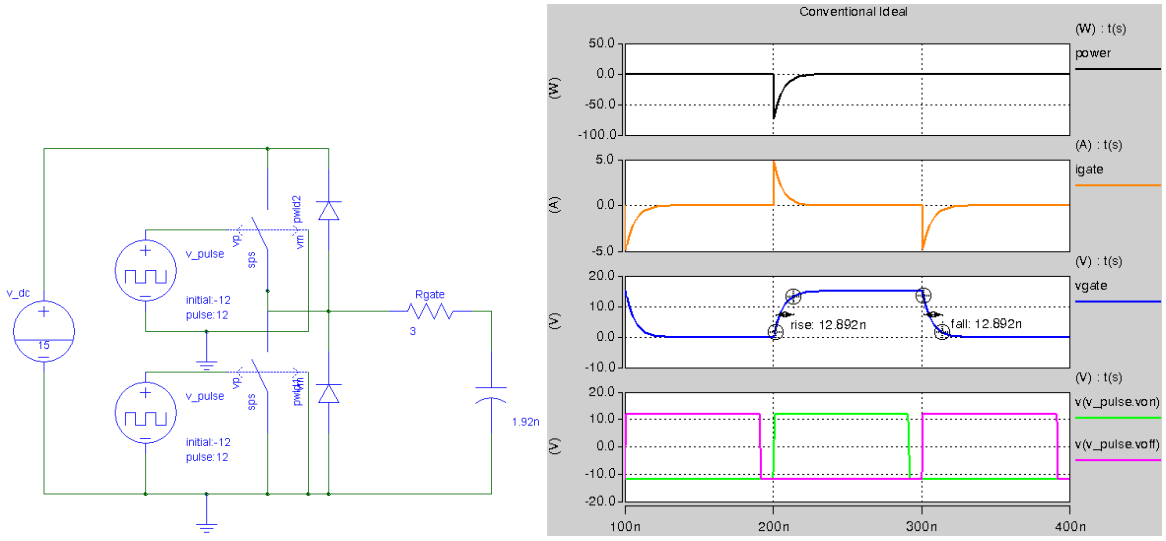


Figure 3.2 Conventional gate driver simulation schematic and waveforms

The conventional gate driver is easily verified in Figure 3.2, where the schematic of the simulated circuit and the respective waveforms are shown. The gate voltage at turn-on is equivalent to a figure shown in the previous chapter of the gate voltage of a power FET turning on. The gate current spikes initially and then exponentially decays, as expected for a capacitor charging. The turn on and off times are determined by the gate resistance and voltage supply. The equations below give a good approximation of turn on time while neglecting the miller capacitance, C_{GD}.

$$C_{GS}\frac{dV_{GS}}{dt}=\frac{(V_{DD}-V_{GS})}{R_G} \qquad \textbf{(3-1)}$$

$$V_{GS}(t_{90\%})=V_{DD}-\frac{V_{DD}}{e^{\frac{t_{90\%}}{R_G C_{GS}}}} \qquad \textbf{(3-2)}$$

$$t_{90\%}=2.3*R_G C_{GS}=13.2\text{ ns} \qquad \textbf{(3-3)}$$

This equation says that V_{GS} reaches 90% of its final value in about two time-constants, which is a good estimation for turn-on time. The waveforms show this estimation is correct. Another thing to note

is the shape and magnitude of the current, or more specifically the power. This is what will need to be decreased by the resonant designs if they are to be implemented.

3.1.2 Resonant Gate Driver

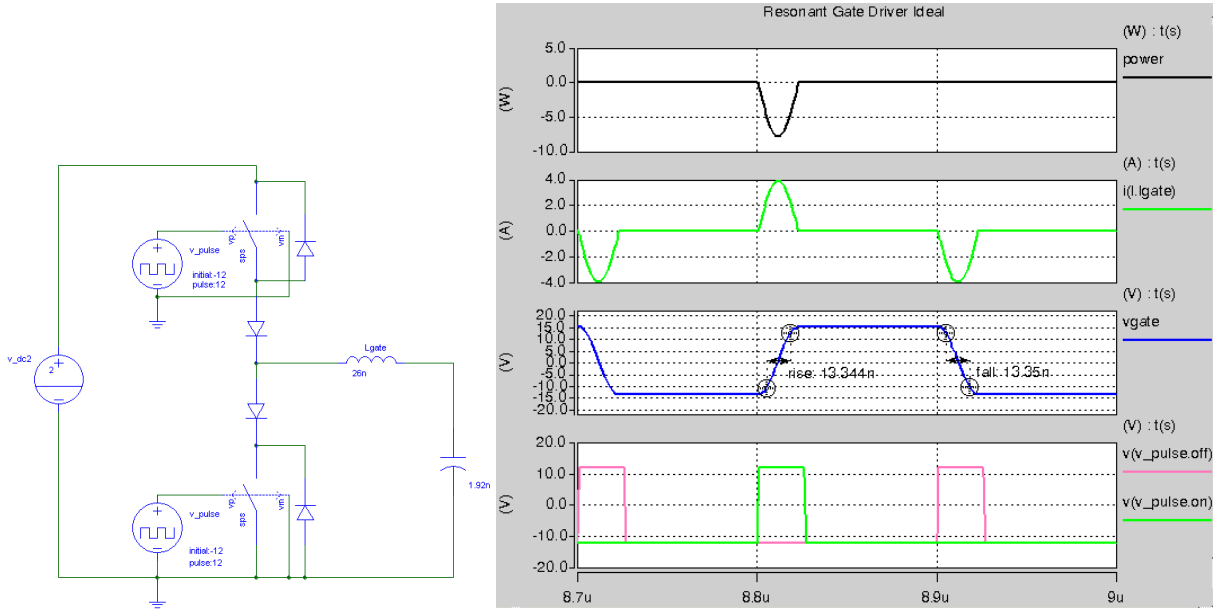


Figure 3.3 Resonant gate driver simulation schematic and switching waveforms

Figure 3.3 shows the resonant gate driver's schematic and waveforms. The gate voltage profile is very similar to the conventional gate driver waveforms except that it swings from -15 to 15 V. The difference is in the current waveform (green). Because of the inductor the current is initially zero. The current peak corresponds with 0 V, thus minimizing turn-on power consumption. The natural resonance frequency is used to approximate the turn-on time [17]. The inductor and capacitor are allowed to resonate for only one half of a resonance frequency of $\frac{1}{2\pi\sqrt{LC}}$.

$$t_{90\%}=0.9\pi\sqrt{LC}=19 \text{ ns} \quad \textbf{(3-4)}$$

The input source only needs to be 2 V in order to achieve the 15 V on-voltage because the resonance of the circuit allows the gate voltage to increase much larger than the input voltage and the diode clamps that increased gate voltage so it won't dissipate back to 2 V [17]. This is very desirable

because it effectively decreases the power consumption by 87% (assuming the same magnitude of the charging current). It can also be seen that the switches do not need to stay on to maintain the gate potential because the added diodes prevent the gate from discharging to the 2 V source through the body diode.

3.1.3 Energy Recovery Resonant Gate Driver

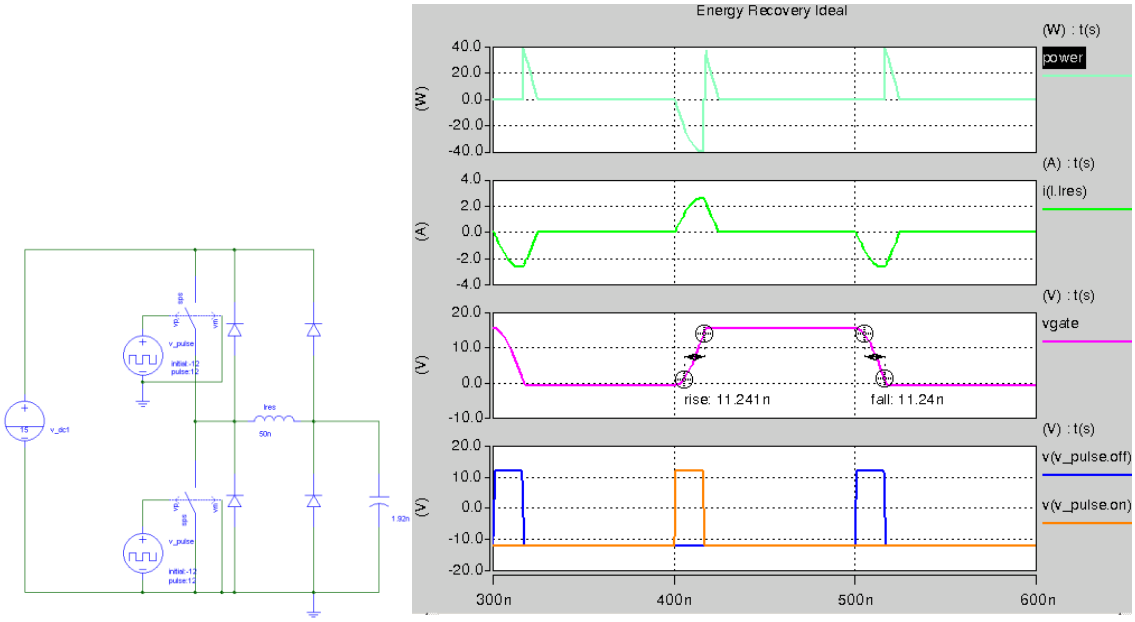


Figure 3.4 Energy recovery resonant gate driver simulation schematic with waveforms

Figure 3.4 shows the schematic and waveforms of the energy recovery resonant gate driver. The profiles of the gate current and voltage are identical to the previous resonant gate driver except that the gate voltage is initially 0 V and is charged to 15 V. The greatest difference in this design is in the power waveform (light green). When the gate voltage reaches the input voltage the high-side MOSFET is turned off (shown as the orange control signal). The power waveform then becomes positive as the current is directed back to the source. In this resonant gate driver the gate voltage is equal to the power supply when the gate is fully charged. The on-time is now only one-fourth of a resonant period.

$$t_{90\%}=0.9*\frac{\pi\sqrt{LC}}{2}=13.8\text{ ns}$$

The energy consumption is larger than the simple resonant gate driver but this gate driver returns energy to the source whenever the high-side switch turns off and during the discharge period. It is seen here that in order to get the energy recovery, like it is stated in the background chapter, the switches must be turned off at the right time. If they stay on too long the energy in the inductor will be discharged through the conduction resistances and not transferred back to the source.

3.2 Stage Two: Non-ideal Implementation and Evaluation Setup

Now that the gate drivers are validated the non-ideal elements replace all the simplifications made in the previous section. The SiC MOSFET model replaces the capacitor so now a simple circuit is designed to allow for the Miller capacitance effect to factor into the power consumption of the gate driver. A simple test circuit is used to bias the SiC MOSFET, and the setup is shown in Figure 3.5. It is designed to set the drain current to 10 A (within the 20 A current range), and the blocking voltage to 100V (The maximum voltage the MOSFET will block in the Buck converter). Each gate driver is implemented in the same design so that the results are consistent with each gate driver so power consumption comparisons can be made.

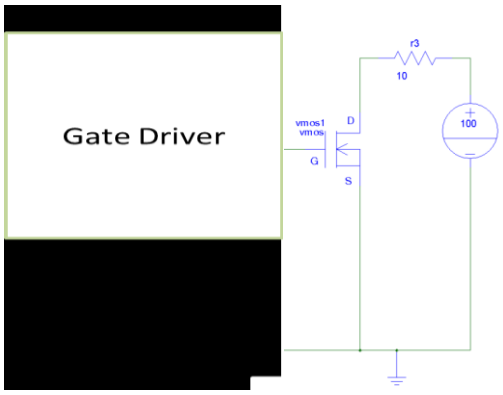


Figure 3.5 Clamped Inductive load test for evaluation purposes

The voltage-controlled switches are not replaced with models of the MOSFET's that will be used in the final hardware implementation because the losses due to the MOSFET will be consistent across all three devices and thus can be eliminated. In the final circuit the IRLM2030 is chosen for the MOSFET's because they have very fast turn-on times and they can easily conduct enough current [19]. They will be placed on the low-side and high-side of the totem pole in an NMOS half-bridge configuration. When implemented this will use the bootstrapping circuit discussed in the background section to control the turn-on and turn-off of the high-side NMOS because the source node is floating. Because this driving scheme is used in all of the gate drivers and the power consumed by charging the bootstrap capacitor is common among all three, it will be excluded from the simulation evaluation.

The final selection will keep the turn-on time of the SiC MOSFET constant while analyzing the average power consumption over a period. Another aspect that will determine selection will be the stability of the gate voltage while it is turned on. Because the resonant gate drivers have short duration command pulses, the gate driver will float between switching events. If there are large transients in application circuit in which the SiC MOSFET is placed, the gate drain capacitance could cause a false switching event. The simulation results and evaluation will be presented in the following section along with the PCB implementation and validation.

The three gate drivers to be compared were presented and validated in the previous section. Now the validation goes one step further by simulating a non-ideal version of the gate driver to determine the least power consuming, and most stable, gate driver. This one will be implemented in a PCB to be used with the full system.

Figure 3.6 through Figure 3.8 show the waveform comparisons of the final test over an entire period, turn-on, and turn-off time, respectively.

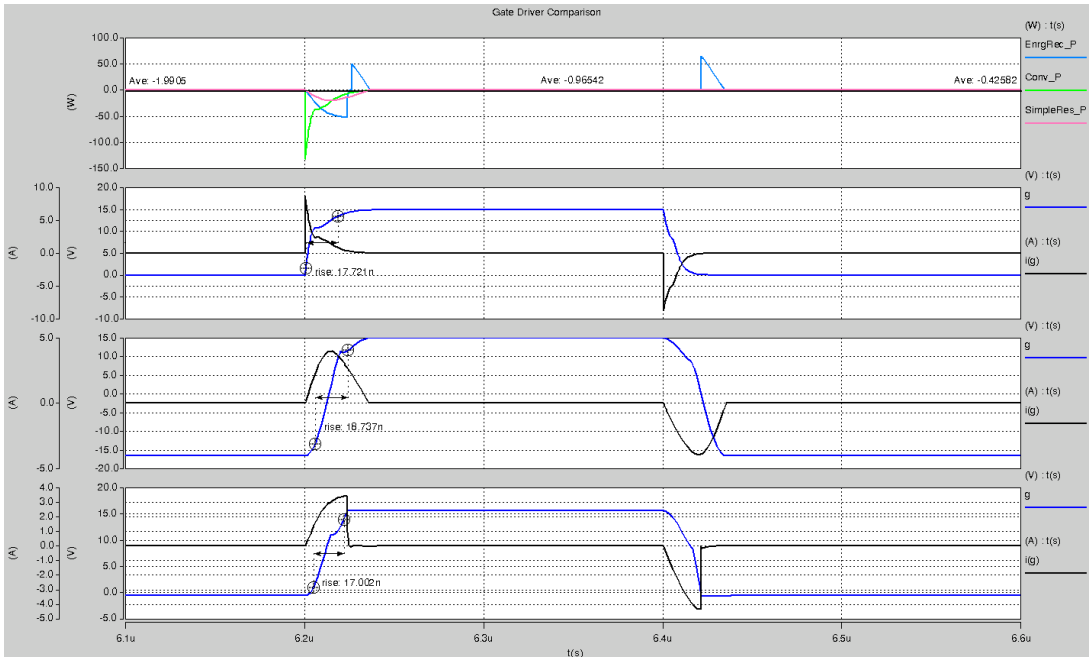


Figure 3.6 Full period comparison of three gate drivers, (top) power comparison, gate current and voltage for conventional, resonant, and energy recovery gate drivers are shown in descending order

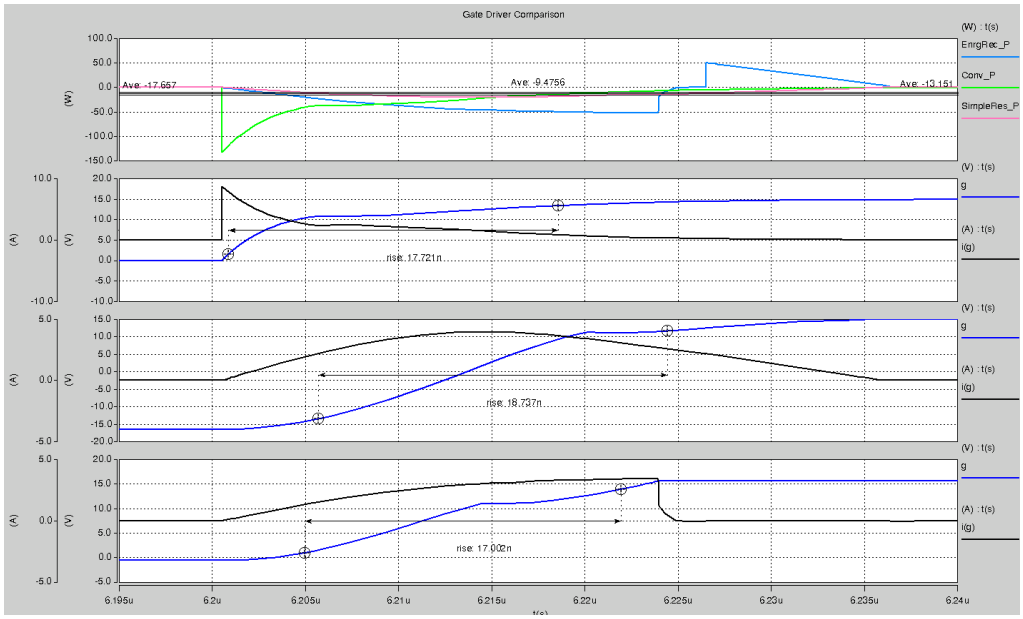


Figure 3.7 Turn-on comparison of three gate drivers, (top) power comparison, gate current and voltage for conventional, resonant, and energy recovery gate drivers are shown in descending order

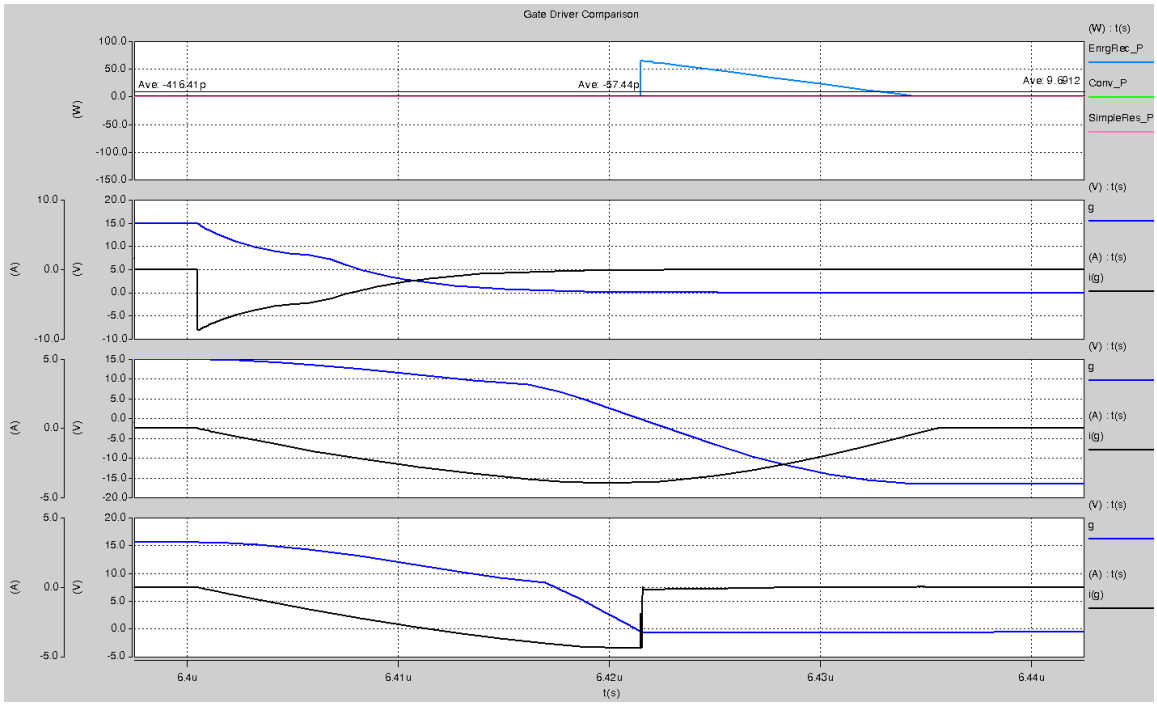


Figure 3.8 Turn-off comparison of three gate drivers, (top) power comparison, gate current and voltage for conventional, resonant, and energy recovery gate drivers are shown in descending order

The waveforms are very similar to the simulation results with the gate represented by a capacitance. The greatest difference in the waveforms is the Miller effect that causes a plateau in the turn-on and –off. The current is the same when compared with the previous simulations except for the energy recovery resonant gate driver. The current decays sharply when the gate voltage reaches its final value. This is due to the current in the gate terminal being reduced to zero and the current in the inductor being redirected to the source through the diode configuration. The top signals show the power consumption. The important characteristic is the average power; this is compared between the three in Table 3.2. The energy recovery resonant gate driver has the least power consumption. This gate driver was also the most stable. The simple resonant gate driver needed multiple cycles to get to the steady-state voltage of the on-voltage because the resonance was used to charge up the gate to 15 V

while the input voltage was 2 V. These reasons determine the energy recovery resonant gate driver to be selected as the gate driver to be implemented on a printed circuit board (PCB).

Table 3.2 Summary of Power Consumption Comparison

	Turn-on	Turn-off	Total
Conventional (W)	-17.67	0	-17.67
Resonant (W)	-9.48	0	-9.48
Energy Recovery (W)	-13.15	9.69	-3.46

3.3 Stage Three: PCB Implementation of Selected Gate Driver

The energy recovery resonant gate driver is chosen for implementation on a PCB. Parts are chosen to implement the functions needed for the full gate driver. The important things to note are control of the two switches, current rating and the desired turn-on time of the MOSFET. The MAX15018a is used as the control IC for the totem pole because it can handle the two different on-pulses needed to turn on the high-side and low-side NMOSFETs [20]. This IC also implements the bootstrapping function with an external bootstrap capacitor. This capacitor is chosen to be 10 nF because it needs to be large enough to supply the charge to the IRLM2030 gates and small enough to be charged up every time the low-side NMOS is on. This is only the turn-off time of the MOSFET. There are two inductor components on the PCB, one surface mount and the other through hole, so that the inductor can easily be changed to modify the turn-on time. The inductor is first chosen to be 22 nH so the charge time can be calculated as follows.

$$t_{charge\text{-}time}=5*R_{on}*C_B=\frac{\pi\sqrt{LC}}{2}=10\text{ ns} \quad \textbf{(3-5)}$$

$$C_{Bootstrap}=\frac{\pi\sqrt{LC}}{10*R_{on}}\cong 20\text{ nF} \quad \textbf{(3-6)}$$

A 10 nF capacitor is under this limit and will decrease the power consumption and still have enough charge to turn on the high-side MOSFET. The diodes used are ZLLS2000 Schottky diodes [21].

The final schematic with all of the chosen parts implemented is shown in Figure 3.9 along with the PCB layout in Figure 3.10. Much time was taken to implement very tight traces and a ground well is used to minimize noise and implement ground distribution. Figure 3.11 shows a picture of the populated board in the lab.

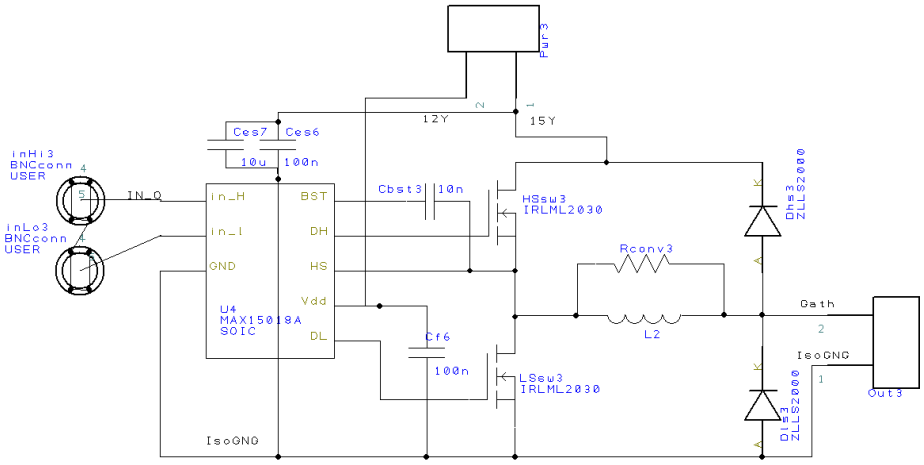


Figure 3.9 Schematic for energy resonant gate driver to be laid out on a PCB

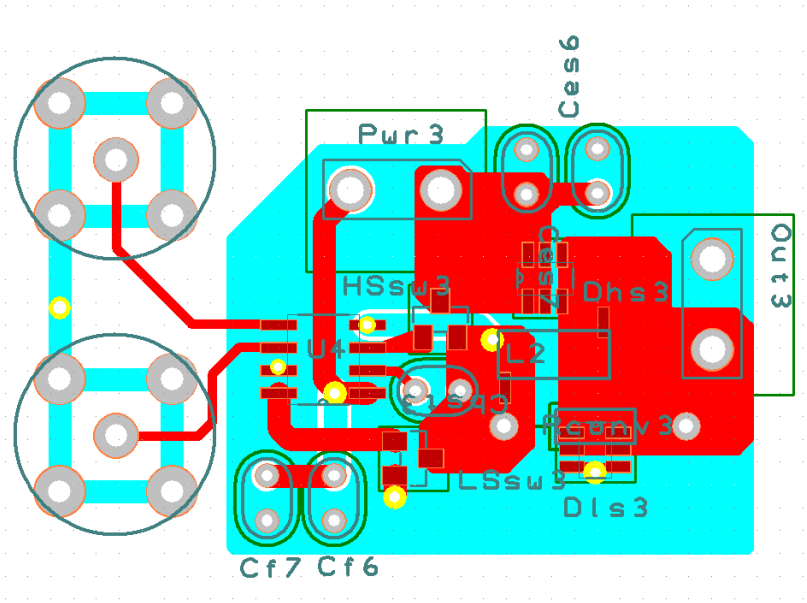


Figure 3.10 PCB layout of energy recovery resonant gate driver

Figure 3.11 PCB populated in the lab (same orientation of previous schematic and layout pictures)

Figure 3.12 shows the energy recovery gate driver waveforms when it is charging a capacitor representing the gate of a MOSFET. This waveform verifies the operation of the gate driver PCB. The on- and off-pulses are very wide because of the waveform generators minimum pulse width (shown in blue for the on-pulse, and orange for the off-pulse).

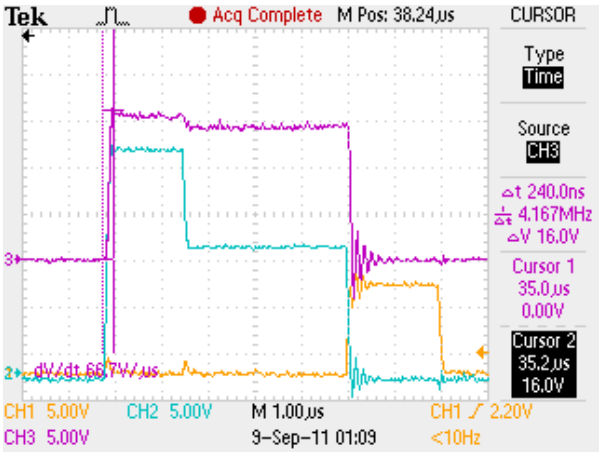


Figure 3.12 100kHz results with a capacitive load, gate (purple), off-pulse (yellow), on-pulse (blue)

The drop in voltage when the high-side NMOS turns off is due to the unclamped gate voltage charging up stray capacitances in the circuit and loosing charge. The solution for this will not be shown because the University of South Carolina is proposing a new gate driver to solve this problem along with the unclamped gate voltage problem in the collaborative research.

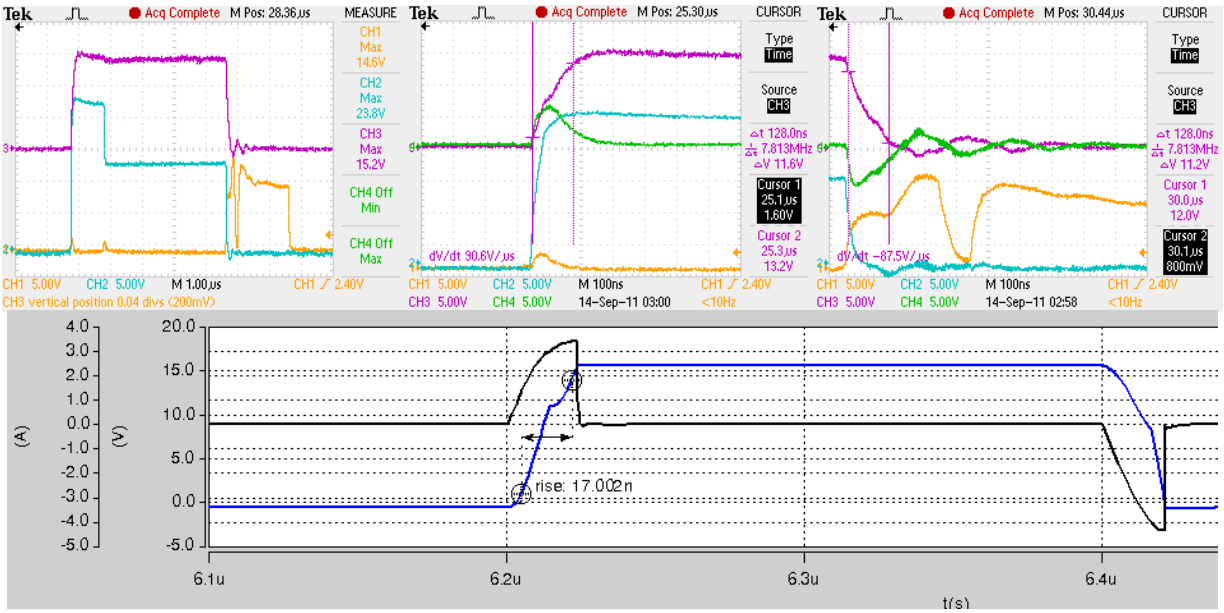


Figure 3.13 100kHz results with SiCMOS load, gate (purple), off-pulse (yellow), on-pulse (blue), gate current (green)

Figure 3.13 compares the waveforms of the simulated gate driver with the PCB gate driver. The waveforms are very similar other than oscillations due to parasitic caused by the tracks and wire connections. Also, the pulse widths for the experimental results are so long that the current during turn-on dissipates before the turn-on time is complete. The current during turn-off matches the simulated value very well. It is not expected to be needed, but the gate driver can switch at 700 kHz with the only limiting factor from going higher is the bootstrap capacitor not being charged fully every off cycle. The gate driver is now fully designed and verified and will be implemented in the final Buck converter system described in Chapter 5.

4 OPTOCOUPLER CHARACTERIZATION EXPERIMENTS

The Buck converter needs to have isolation between the system variables and the control circuit that will use them to control the overall operation of the converter. This isolation is created via optocouplers and the different functions of the optocoupler need to be used to transmit the different kinds of data between the circuits, i.e. voltage, current, and digital signals. This requires optimizing different aspects of the optocouplers. As shown in the Background chapter there are different topologies to use that will enhance certain functions of the optocoupler. There are two primary roles of the optocoupler, to accurately transmit analog voltage and current signals to the control circuitry and to transmit the on and off control signals to the gate driver. Although the optocoupler device might be the same in each of the two different roles, the topology, or circuitry around the optocoupler device, will be different between the optocoupler used in either role as presented in the Background chapter. The analog transmission topologies will allow the output to copy the input levels, while adding desired gain to the signal. The digital transmission topologies cause the output of the optocoupler to reproduce the digital signal applied to the input.

There is another reason to analyze each topology in this section -- to determine the benchmarks for the optocoupler whether analog or digital. Speed, power consumption, and operation over temperature are the important benchmarks for optocouplers to be compared to the other isolation techniques. These are important to be able to understand how optocouplers could be implemented in other power systems and the characteristics that need to be improved to surpass the comparable solutions. The endeavors of the experiments in this section determine the best topology and optocoupler commercially available to use in the two different roles for the Buck converter and the final benchmark for the optocouplers available today. The experiments in this section will pursue both objectives in the same experiments because the parameters that need to be determined and enhanced

for the benchmark are the same key parameters that need to be optimized for use in the Buck converter system.

4.1 Introduction of Commercially Available Optocouplers and Defining the Optimum Application Topology

Each topology will be analyzed based on power consumption, propagation delay, temperature, linearity, minimum pulse width (rise and fall time), and optimum biasing. This design section will define the procedures of determining which topologies will be applicable to this research, and understanding the best possible optocoupler circuit for optimizing the aforementioned parameters and determining the final benchmarks for that topology. The first step in finalizing the design and implementation of the optocoupler topologies is to select the basic building block of all the topologies, the optocoupler. They must be analyzed to select the technology that inherently has the best performance with respect to the key parameters, power consumption, propagation delay, temperature, linearity, etc. The optocouplers that do not meet that standard will not even be tested within the topologies that are defined because they will inherently impede the optimization of the important characteristics.

The currently available optocouplers are broken into three different materials, gallium arsenide (GaAs), gallium arsenide phosphorus (GaAsP), and aluminum gallium arsenide (AlGaAs). The material refers to the type of LED and determines the types of properties like optimum wavelength of light, heat dissipation, and mobility. Also, the different materials can each be packaged in three different ways. One way is as an LED and photodiode pair (applied in analog topologies), as an LED and photodiode with transistor (or phototransistor) pair (basic package for digital topologies), or as an LED and photodiode connected to an amplifier stage. These three types of packages were described in the Background chapter and the type of package is important because the correct one must be selected for the correct topology. Typically, each package is available in any of the three materials so the different materials can

all be implemented in any of the topologies, thus there is the ability to compare between the materials for the same application.

In the graph below the three materials are compared to each other, but the different types of packages have not been broken apart in this comparison. This is due to the fact that propagation delay, power consumption, and isolation voltage are common characteristics that need to be analyzed no matter which output stage is used. If this were a graph comparing CTR then the materials would have to be broken out by package type because the CTR's would be very different. This is due to the different standards for measuring CTR for each output stage.

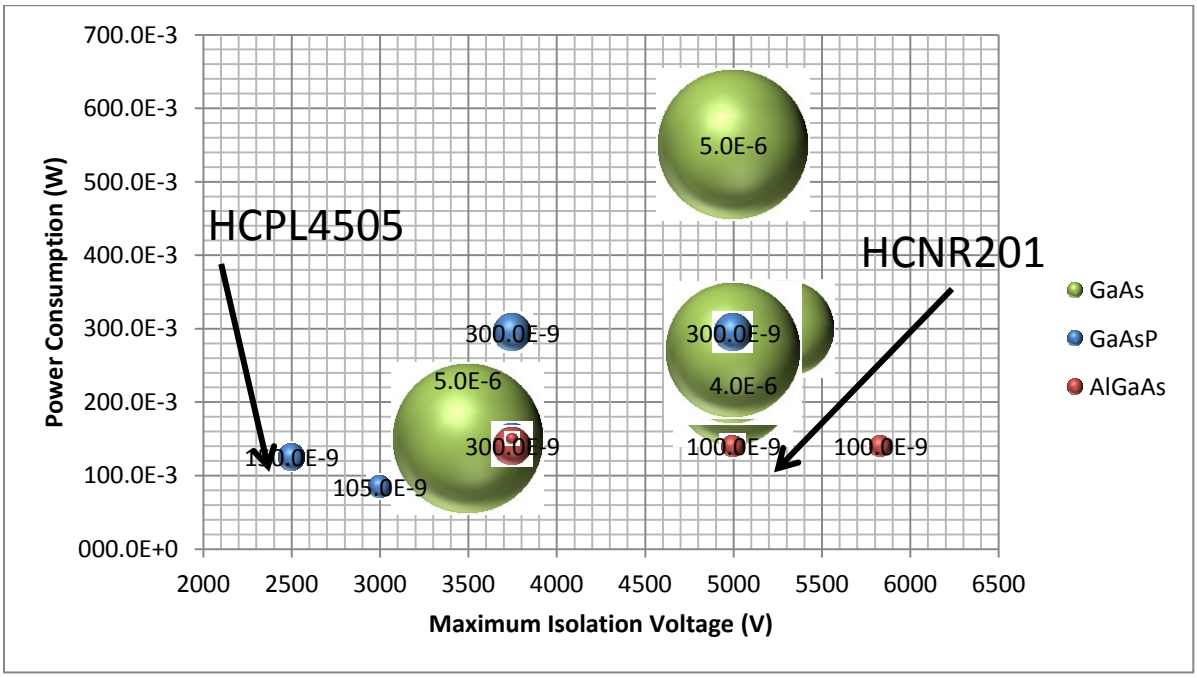


Figure 4.1 Technology versus specification chart comparing power consumption, max isolation voltage (60 s duration), and propagation delay of three different materials

Figure 4.1 compares optocouplers of the three different materials. They are compared on the x- and y-axes by their power consumption and maximum isolation voltage (for 60 s duration). The size of

the bubble indicates the propagation delay, the bigger the bubble the longer the propagation delay. The GaAs devices are quickly ruled out because the propagation delays are as large as the period of a 200 kHz switching frequency which is not uncommon in many dc-dc converter systems. The GaAsP and AlGaAs devices show minimal propagation delays and lower power consumption. The only difference between the two is the maximum isolation voltage. This is not a large hindrance because the SiC MOSFET switch is only rated at 1.2 kV and all these materials are above that. For a final benchmark for determining the possible applications for these optocouplers this plays a larger role. The AlGaAs would be the best choice in this respect because a device is possible with an isolation voltage larger than 5.5 kV. There are some problems relying solely on this graph to make any design decisions. The data is from the datasheets referenced above and the experiments to find them do not necessarily use the same application circuits that will be used to determine the final benchmarks, and the ranges of values are too large to fully understand the benchmark when just analyzing this data. Also, to complete the two objectives, the topologies from the Background section need to be analyzed to determine the final benchmarks and to select the optimized topology for the Buck converter. These topologies are not analyzed in the datasheets. The next sections define the bench top experiments that are used to analyze the different topologies and the results will determine a final benchmark and the topologies that will be used in the Buck converter system. Table 4.1 lists the part names of the chosen optocouplers, broken out by material and role (digital or analog), that will be used in the following experiments. The digital topologies will implement GaAsP and AlGaAs optocouplers and comparisons between the materials will be made. The analog topologies can only implement the AlGaAs material because the GaAsP optocouplers were not available with a servo-diode packaged with the optocoupler (needed for linear analog transmission). Further explanation of the decisions made for the particular parts are presented in their respective experimental section to follow. All of the results from these experiments will be cataloged and discussed in the following sections.

Table 4.1 Optocouplers Experimented to Determine Benchmark

Role	Part	Material
Analog (w/servo-diode)	HCNR201	AlGaAs
Digital (LED/BJT)	HCPL4505	GaAsP
Digital (LED/BJT)	HCNW4505	AlGaAs
Digital (LED/Amp)	ACPL-071L	GaAsP
Digital (Amp-LED/Amp)	HCPL7723	AlGaAs

4.2 Benchmark Experiments for Analog Application Topologies

This section defines experiments and presents the results for the analog transmission topologies. The Background Chapter shows the different topologies used to transmit analog. Experiments are designed with the objective of collecting raw data to understand the key parameters of propagation delay, biasing point, accuracy, power consumption, and temperature for each topology and optocoupler material. A benchmark will be determined based on these results and in the Implementation of Optocouplers in the Buck Converter Chapter the results will be used to determine the topology used in the Buck converter. Only two analog transmission topologies out of the three presented in the Background chapter were chosen for experimentation. The topology shown in Figure 4.2 is not experimented with any further because it has the same working principle of the other feedback analog topology and it would be repetitious to investigate this topology. Also, when implemented on a bread board this topology not only consumed more power with equivalent components, it adds more complexity because the photodiodes are connected to the power supply and the use of an uncompensated voltage follower op amp. The other topology improves upon these weak points by eliminating the output stage's photodiode connection to the supply and a stable feedback network for the output op amp.

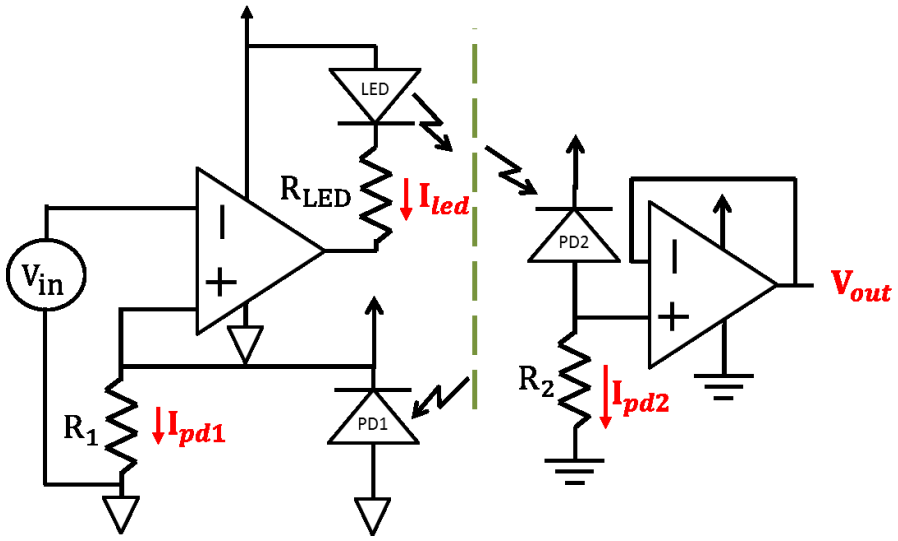


Figure 4.2 Second analog feedback transmission topology not tested further [7]

The remaining analog topologies analyzed are the feedback topology that uses a servo-diode to linearize the transfer function and the open-loop topology that does not need an isolated supply for the input stage. These analog optocoupler topologies each undergo three experiments. The first experiment is defined to understand how biasing affects the circuit. The following section will discuss the test setup and procedure for the experiment. In this experiment a dc voltage is applied at the input to bias the circuit at one operating point and then the response of the output and various other system variables are recorded to determine the key characteristics of the circuit. Then the dc operating point is swept between a minimum and maximum allowable operation range. In the next experiment the biasing results are used to create a sinusoidal waveform, which is applied to the input, with a peak-to-peak voltage of all the reasonable biasing points found in the first test. The final experiment sweeps the temperature of the optocoupler in the same test setup as the second experiment. A conclusion is drawn for the final benchmark for the analog transmission scheme in the Conclusions Chapter using the results from these experiments and Chapter 5 determines the optimal topology based on these results.

Now that the experiments and objectives have been presented the specific device selections need to be understood. The analog topologies only need the optocoupler (packaged with a servo-diode) and an op amp with some external, tunable resistors. The two different topologies will utilize equivalent devices so that comparisons can be drawn. For the optocoupler selection there are two to choose from: Avago's HCNR201 and Vishay's IL300. The HCNR201 is selected for all analog transmission topologies because it has the best raw propagation delay, linear CTR, and temperature operation as seen in the datasheet compared to any other analog optocoupler [12]. The IL300 was another analog optocoupler that is of similar quality of the HCNR201, but is not analyzed because the switching characteristics are a factor of 10 less than the HCNR201 [7]. Table 4.2 presents the data that determined this decision.

Table 4.2 Comparison of IL300 and HCNR201

	HCNR201 (AlGaAs)	**IL300 (AlGaAs)**
Input Current	1 – 20 mA	1 – 60 mA
Peak Input Current	35 mA	250 mA
LED Forward Voltage I_F=10 mA	1.3 – 1.85 V	1.25 – 1.5 V
Max Reverse Voltage	15 V	50 V
Transfer Gain K_3	0.95 – 1.05	0.75 – 1.25
CTR	0.36 – 0.72%	0.4 – 0.8%
PD Leakage Current	0.5 – 25 nA	1 – 25 nA
Bandwidth	1.5 MHz	200 kHz
Withstand Voltage	5000rms	5300rms

The op amp used is the MAX4450 [22]. This op amp was selected based on the criteria to have a maximum output slew rate an order of magnitude larger than the speed of the optocoupler. Also a single supply op amp was chosen. A final note is that the experiments to determine the benchmark presented below is for the design with circuit parameters and component selections shown above. They were chosen to optimize the circuit as much as possible. For example, choosing an op amp with a limited

slew rate would limit the slew rate of the overall topology to the value of the op amp and thus skew the gain of the voltage transfer. The final benchmark that is found through the experiments below is a representation of the advantages and limitations of optocouplers. For any design implementing these optocoupler topologies this benchmark should be considered as the general baseline performance in which these devices should operate when optimized for speed and linearity. Other topologies that optimize other key parameters will have different benchmarks.

4.2.1 Feedback Analog Transmission Topology Bias Experiment Setup

The first experiment, the biasing test, is performed on the topology shown in Figure 4.3. As stated and justified earlier, the HCNR201 and MAX4450 are the optocoupler and op amp, respectively. Figure 4.3 also shows the test setup that is used to measure the key system variables. It can be seen that the system variables measured are V_{in}, V_{out}, I_{pd1}, I_{pd2}, I_{LED}, I_{src1}, and I_{src2}. There are also important calculated parameters that are measured to determine the impact biasing has on the performance of this analog transmission topology. The propagation delay, t_{prop}, is measured from the positive edge of the input to the positive edge of the output. The values of I_{src1} and I_{src2} are used to measure the power consumption on the input and output, respectively. The HCRN201 is biased when the photodiode on the input has tens of micro-amps flowing through it. The input resistor is set to 100 kΩ while the input voltage is swept from 0.5 to 6 V which corresponds to 0.5 µA to 60 µA through the photodiode. The value of R_2 is selected to be 100 kΩ to attain unity gain. The CTR is calculated ($\frac{I_{pd1}}{I_{led}}$) along with the gain ($\frac{V_{out}}{V_{in}}$). If the gain is not unity, then the K_3 factor discussed in the Background chapter is not unity, and would denote there is an unequal amount of light impinging on PD1 and PD2. The final calculated values are the rise and fall times of the output voltage. The input is applied ten times via a pulse at 50 kHz with a positive width of 10 µs to bias the circuit with a dc voltage. There are multiple cycles to make sure the topology is operating in steady-state. This is done at each input voltage level from 0.5 V to 6 V. The

response of the circuit is measured and calculated to determine how the PD1 current affects the performance of the circuit. This experiment is completed for three iterations, one for each R_{LED} value; 110 Ω, 310 Ω, and 510 Ω. This does not bias the LED current differently since the PD1 current sets the LED current, but this does show the impact of the voltage drop across R_{LED} on the LED response.

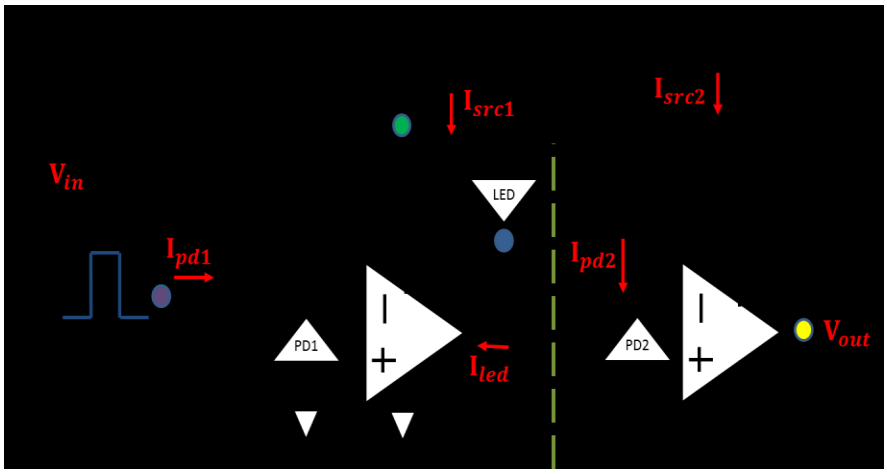


Figure 4.3 Biasing test setup schematic for HCNR201 feedback analog topology (colored nodes show the probe placement (further discussed in following section)

4.2.1.1 Feedback Topology Bias Experimental Results

Before the results can be presented an important comment needs to be made about how the measurements are taken with the oscilloscope probes; circuit placement has an effect on the measurement. The measuring scheme for this experiment and all following analog transmission experiments had to be altered so that the probe capacitance would not skew the results. Although the scope allows for floating measurements, some floating measurements could not be taken because of the 16 pF capacitance of the probe. When the probe is placed across the feedback path of the op amp, which is used for the I_{pd2} measurements, a pole is introduced at 99 kHz $\left(=\frac{1}{2\pi*16p*100k}\right)$. This pole decreases the response time of the output voltage by more than 750%. This difference is shown in

Figure 4.4. Because the probe cannot be used, I_{pd1} and I_{pd2} had to be calculated from the measured values of V_{in} and V_{out} as can be done via the transfer function. This has little impact on the accuracy of the measurements because the calculation only neglects the 10 to 20 mV across the photodiodes during operation and the 1 to 5 µA op amp input current. This introduces a ±4% error for a 500 mV signal which decreases quickly to 1% as the magnitude increases.

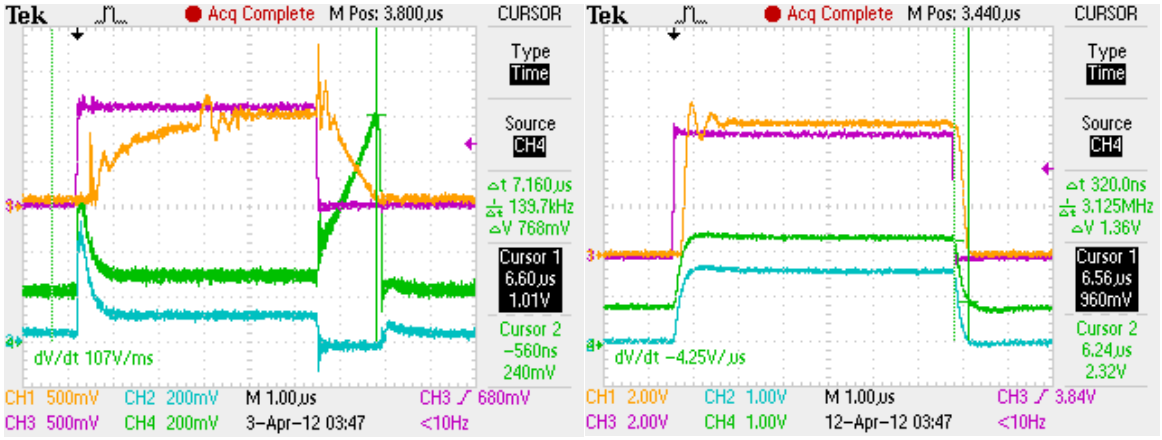


Figure 4.4 Old measurements (left) , new measurements (right); input (purple), output (yellow), LED current (blue), source current (green)

While there is no input applied the LED branch draws 0.7 mA and the op amp draws 6.5 mA for all values of R_{LED}. A figure of merit is created to show the trend of the key parameters as the LED resistance is changed. The trends are created by averaging each respective parameter across all biasing points. These values are only showing trends to introduce the circuit's characteristics. In-depth graphs for each biasing point will be shown in the following sections. Table 4.3 shows the trends of the propagation delay and power consumption as the LED resistance is increased.

Table 4.3 Power Consumption and Propagation Delay Trend as R_{LED} Increases

R_{LED}(Ω)	110	310	510
$t_{prop,avg}$ (ns)	225	390	550
$P_{input,avg}$(mW)	446	258	200

The trend is that for increasing value of R_{LED} the propagation delay decreases while the power consumption also decreases, when the LED resistance is increased 450% (from 110 Ω to 510 Ω), the propagation delay increases by 250% and the power decreases by 220%. The mechanism for the delay in optocouplers is not well understood. The delay is seen to have a dependence on LED resistor values and as the value increases the delay increases. This could be due to the larger voltage transition the output of the op amp must swing through. Also, the input power is based on the forward current of the LED, and as this increases, the propagation delay decreases. But these are simple explanations for a complex phenomenon, as seen in [23], the delay can also be a minimum at the middle of the range of LED currents for other optocoupler devices. Further research in this area, to determine the mechanism of the propagation delay, is required. What is understood is that the bandwidth of the circuit is determined by the propagation delay and desired linearity as corroborated in [23]. Another possible reason for the changing propagation delay in this circuit could be, although the output gain stage is not changed, the input stage's feedback gain and bandwidth is determined by the value of R_{LED} and I_{LED}, when these increase the bandwidth decreases. The important note is that the trend is predictable and the mechanism does not need to be fully understood to conclude a benchmark for the propagation delay.

The next sets of figures are broken out for each value of R_{LED} that the experiment was conducted. The graphs show the different key parameters compared between the ranges of the value of R_{LED}. The propagation delay versus power consumption is defined by normalizing the power consumption by subtracting the $I_{LED}^2 * R_{LED}$ from the total input stage power consumption, which

compensates for the LED resistance component of the measured total power consumption. This is done to look at the power consumed by the op amp, LED, and filter capacitor, since these are the components that will increase or decrease propagation delay. But it is noted that the overall power consumption of the input stage does increase as the photodiode current increases, but not as the R_{LED} decreases, because as R_{LED} increases the current decreases enough to keep the overall power consumption equal even though the op amp is consuming more power.

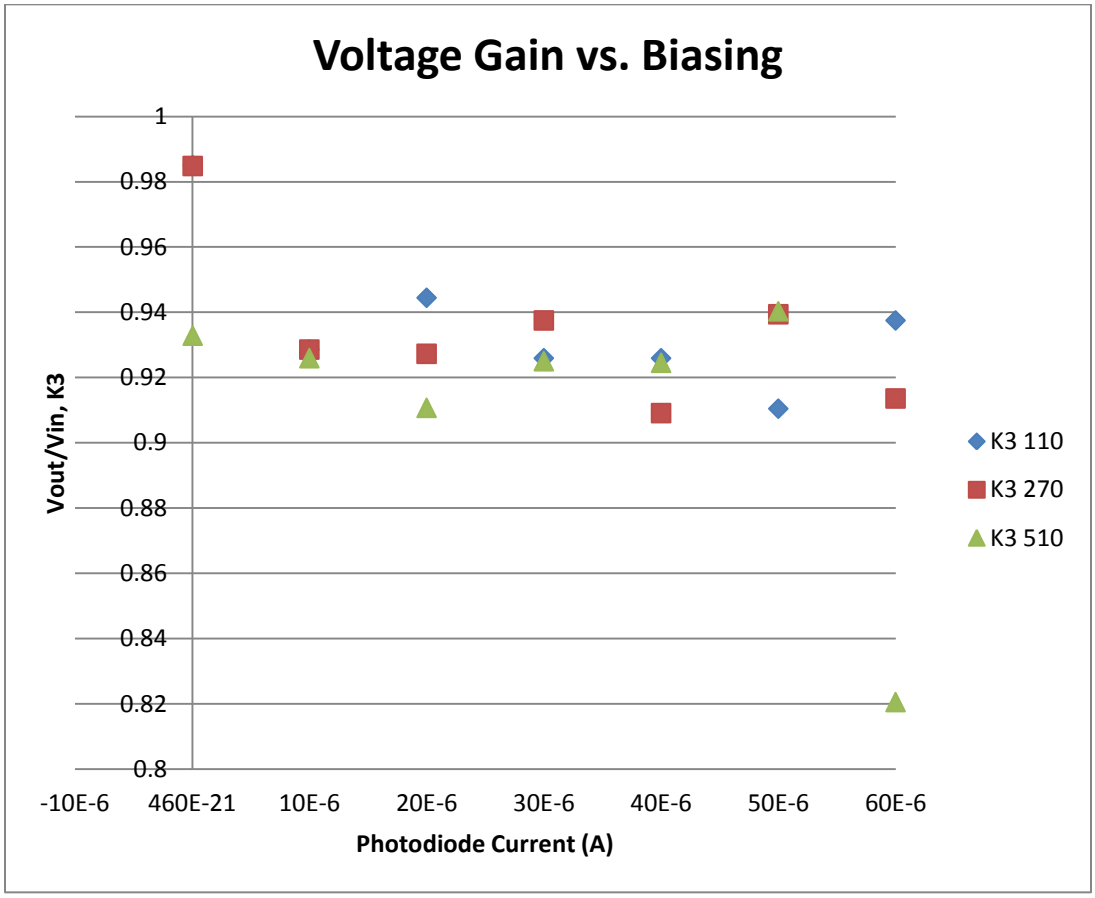


Figure 4.5 Voltage gain versus biasing for different values of R_{LED}

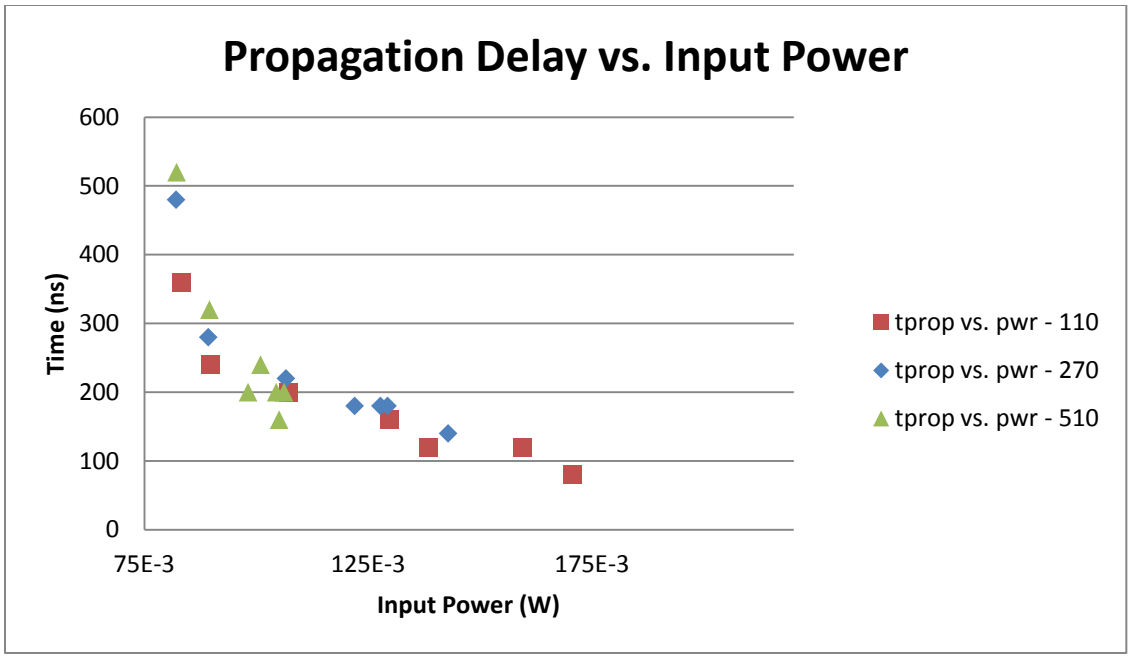


Figure 4.6 Propagation delay versus input power for different values of R_{LED}

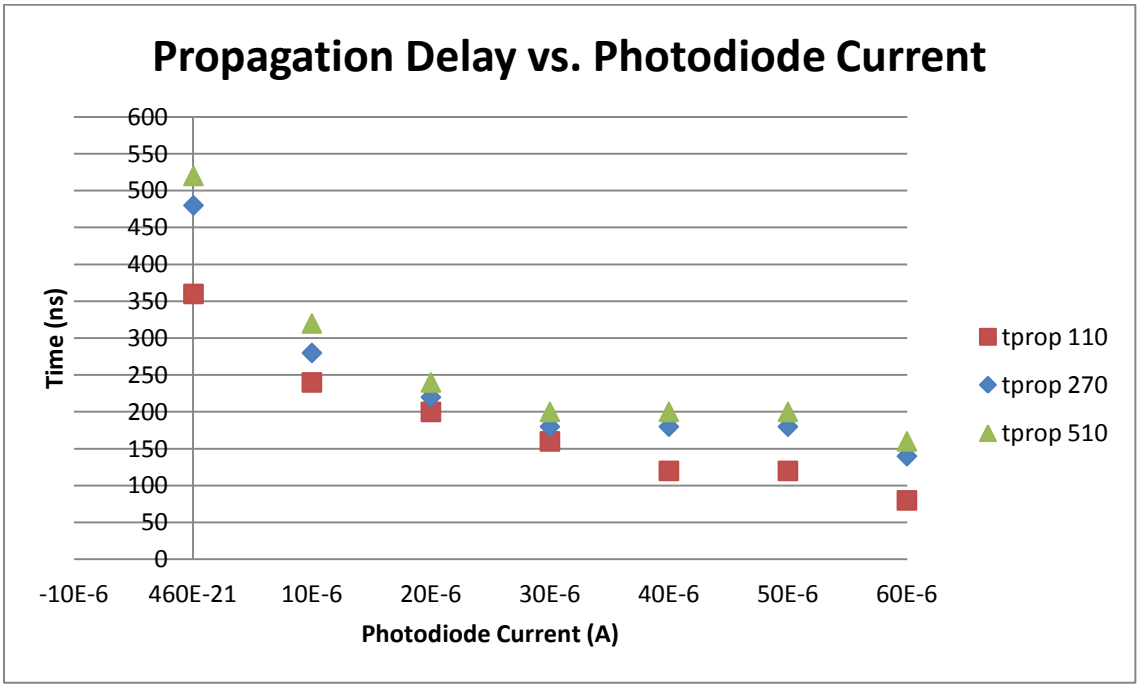


Figure 4.7 Propagation delay versus photodiode current for different values of R_{LED}

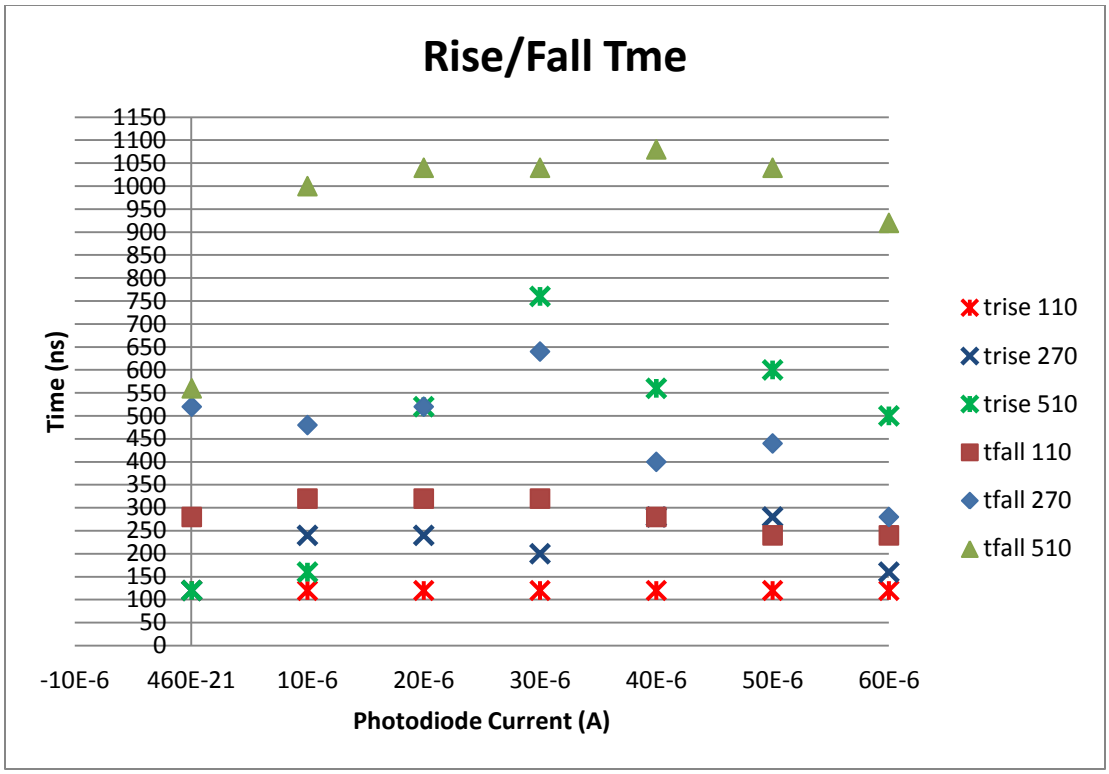


Figure 4.8 Rise and fall times versus photodiode currents for different values of R_{LED}

These figures show the effect of R_{LED} on the response of the circuit. Also, it is seen that as the input photodiode current increases from 0.5 µA to 60 µA the circuit parameters respond in the following ways. The propagation delay decreases by 66% while rise and fall time and voltage gain stay constant. The decrease in the propagation delay cannot be improved further by changing the biasing because 60 µA is the absolute maximum current. The range where the voltage gain is constant is important for the next experiment, the linearity experiment. The voltage gain needs to be constant across a range of biasing so that an input voltage within that range can be expected to cause a linear response in the output. This is shown more in-depth in the next section. The propagation delay has already been discussed, and the affect of the value of R_{LED} is shown more completely in Figure 4.6 and 4.7. Also, the value of R_{LED} impacts the rise and fall time of the output response; an 80% reduction in resistance causes and 80% and 60% decrease in the rise and fall time, respectively. This information is important to

determine the final benchmark, and to determine which topology will be implemented in the Buck converter and how the different values are selected to obtain the optimum performance of the analog transmission circuitry. The next section applies a sinusoidal input to measure the linearity and propagation delay of this feedback analog transmission optocoupler topology.

4.2.2 Feedback Analog Transmission Topology Linearity and Temperature Experimental Setup

Now that the different biasing points are understood independently, a sinusoidal input is applied and the temperature scaled to see what those changes do to the parameters analyzed in the previous experiment. This experiment will completely determine the benchmark for this topology, because it shows the full operation of the circuit while the previous experiment only discovered the correct operating point. The values of R_1 and R_2 are set to 100 kΩ to create a unity gain at nominal operation. The experiment is repeated for the value of the LED resistor from 110 Ω to 270 Ω, and finally 510 Ω, like the previous experiment. The temperature sweep is applied over all values of R_{LED} to determine the best operating point in terms of propagation delay, linearity, and rise and fall times. In each of these experiments the input will be an 80 kHz sinusoidal waveform with 0 V minimum and 6.5 V maximum. Each of these tests will be repeated at 25 °C, 50 °C, and 70 °C. This range is chosen because it stays well below the maximum temperature of 85 °C. The output voltage and LED current are measured while the propagation delay, voltage gain, and K_3 term are calculated via the transfer function. Because CTR is not in the transfer function for this topology the K_3 term is the only thing that will affect the gain during temperature operation. Figure 4.9 shows the experimental setup for the linearity and temperature experiment. The optocoupler is isolated and its temperature is increased. This procedure is included in the experiment so that the effect of temperature on the propagation delay, voltage gain, and K_3 parameter is only caused by the response of the optocoupler to the temperature increase. The

auxiliary circuit is removed from the equation so that the results are only dependent on the optocoupler.

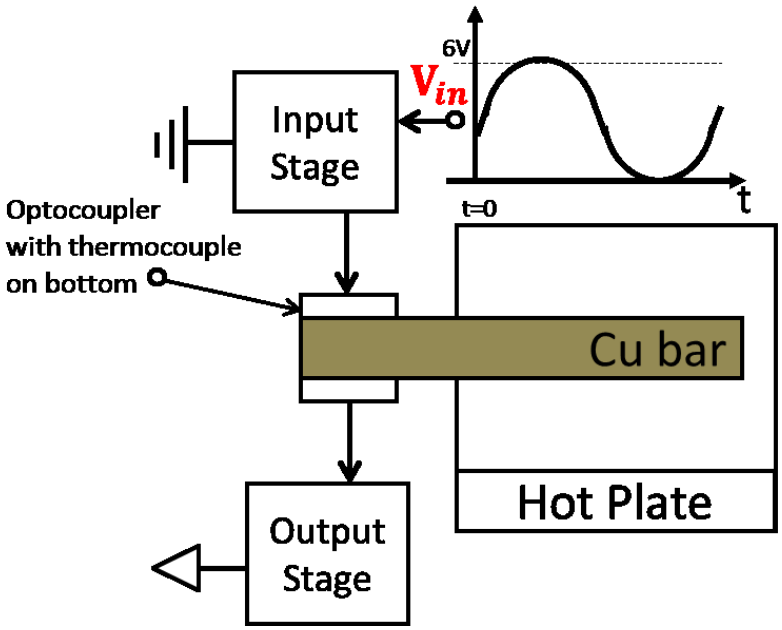


Figure 4.9 Temperature and linearity experimental setup for feedback topology, the probe measurements are the same while the input waveform changes as seen

4.2.2.1 Feedback Topology Linearity Experimental Results

This section shows the linearity and temperature experimental results for the analog transmission feedback topology described above. Figure 4.10 shows the input voltage waveform and the output voltage and LED current waveform measured in this experiment.

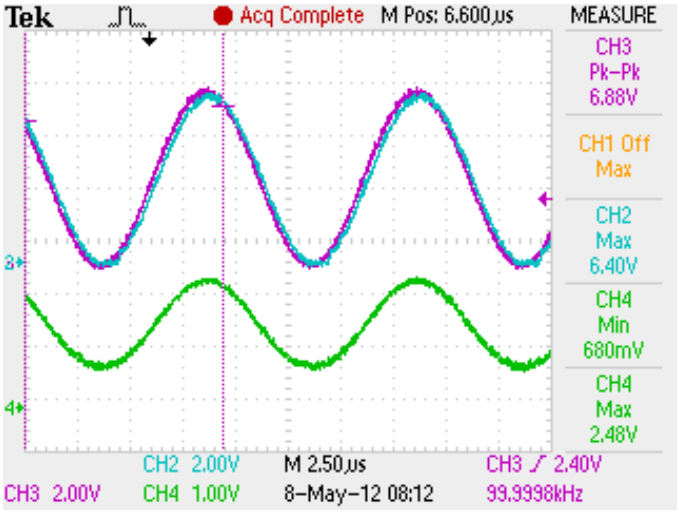


Figure 4.10 Waveform of test, R_{LED} 110 Ω at 70 °C input (purple), output (blue), I_{LED} (green)

The waveforms are extracted to Excel to calculate the propagation delay, voltage gain, and K_3. The first step is to define the propagation delay for each value of the LED resistance at every temperature. Table 4.4 shows these results.

Table 4.4 Propagation Delay Over Temperature for Different R_{LED}'s

	t_{prop}(ns)		
	25°C	**50°C**	**70°C**
110Ω	100	110	180
270Ω	200	230	300
510Ω	300	400	520

While the optocoupler's temperature increases to 70 °C the LED resistance is increased and the propagation delay increases with the same trend as the previous experiment. The temperature causes, on average, a 50% increase in the propagation delay. The next step is to analyze the voltage gain over the entire input range to determine the linearity of this design at various LED resistances. The nominal voltage gain should be unity because both R_1 and R_2 are 100 kΩ.

To analyze the voltage gain ($\frac{V_{out}}{V_{in}}$), an important comment needs to be made. The output is shifted by the propagation delay. This affects the voltage gain measurements because if the input voltage and output voltage are compared at one moment in time an input voltage at t_1 would be compared to an output voltage corresponding to the input voltage at t_1-t_{prop}. To get an accurate value for the voltage gain the output waveform data is shifted by a time step equal to the propagation delay. Figure 4.11 through Figure 4.13 show the voltage gain for each temperature set versus the input voltage plotted on the x-axis. At each temperature each value of R_{LED} is plotted to show the effect of the LED resistance over temperature.

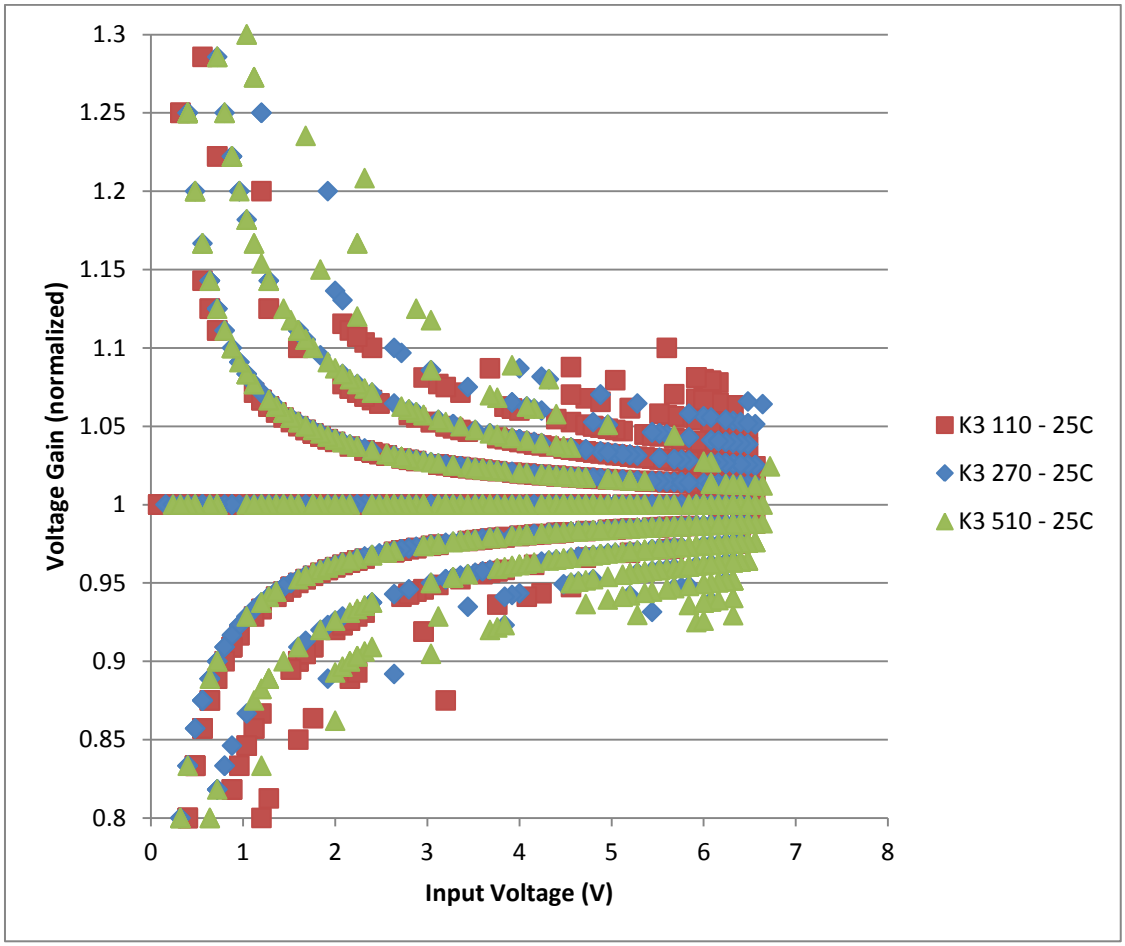


Figure 4.11 Voltage gain versus input voltage over entire biasing range and R_{LED}'s at 25 °C

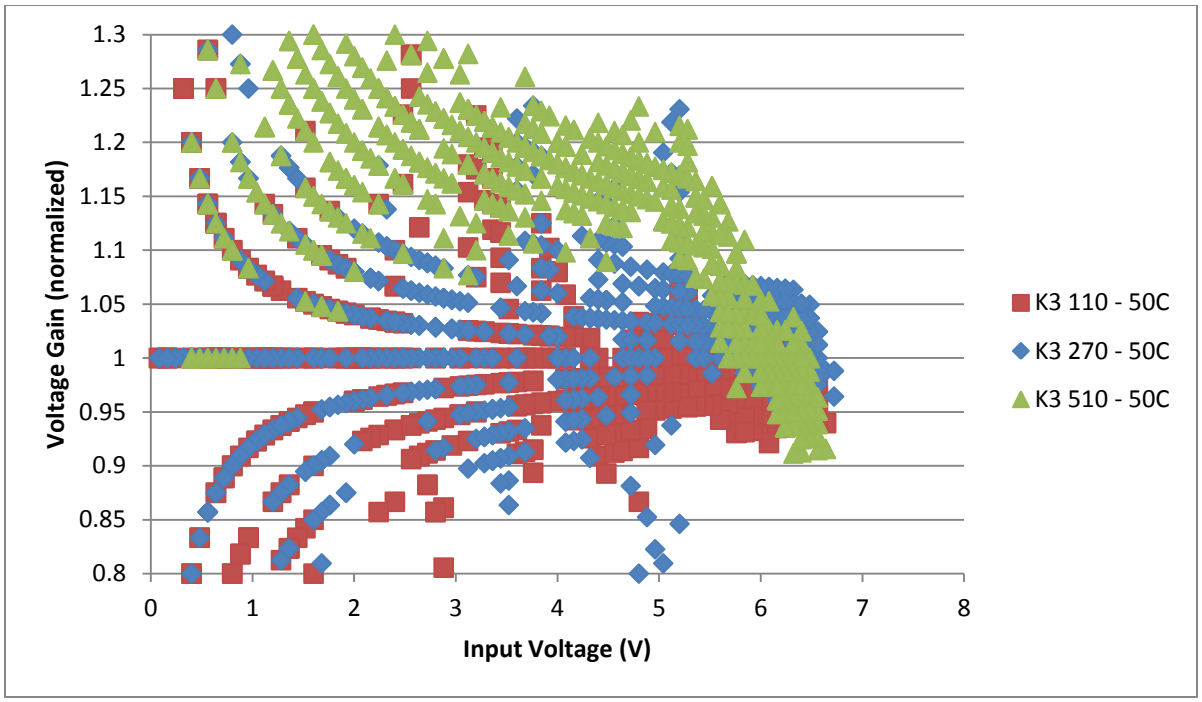


Figure 4.12 Voltage gain versus input voltage over entire biasing range and R_{LED}'s at 50 °C

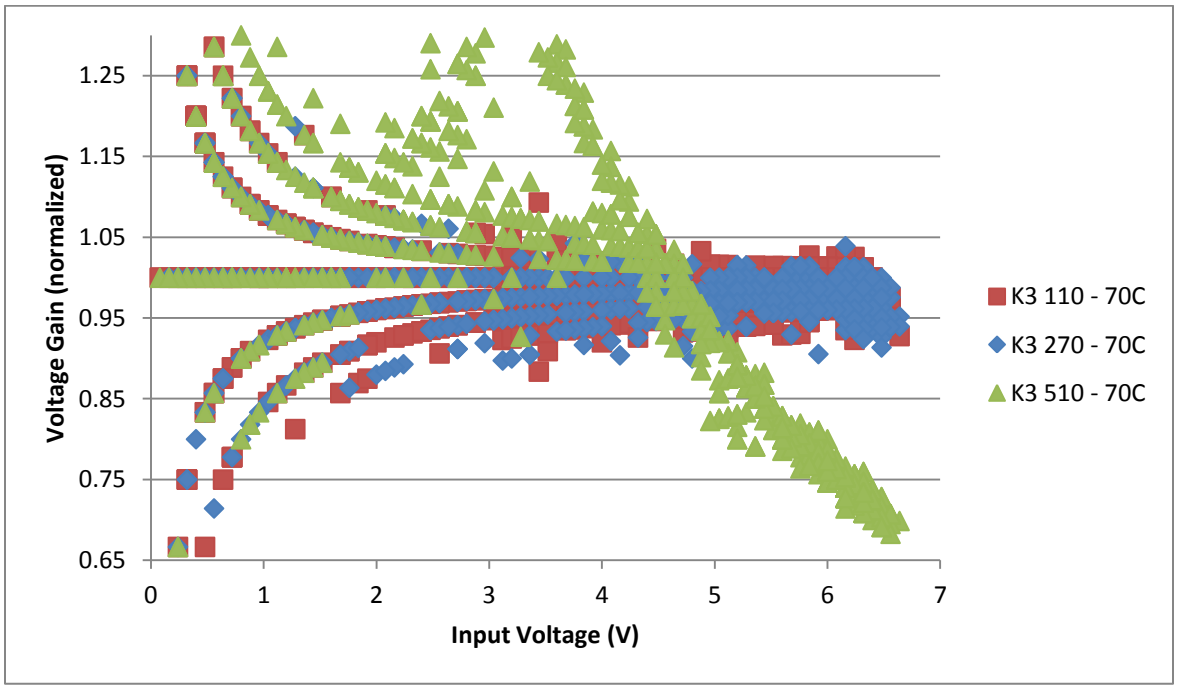


Figure 4.13 Voltage gain versus input voltage over entire biasing range and R_{LED}'s at 70 °C

In this breakout the difference the LED resistance makes can truly be seen by the change in the voltage gain versus the input voltage for each temperature and LED resistance. A perfect optocoupler system would have a straight line at 1 $\frac{V}{V}$ for every temperature. This experiment shows that the voltage gain is not constant across temperatures, LED resistances, and input voltage. The voltage gain starts to spread out from unity as the input voltage decreases below 2 V for 25 °C and below 4 V for 70 °C (excluding the 510 Ω case for now). This non-linear spreading can be avoided by operating above the input voltage thresholds. In this region the voltage gain kept within ±5% of unity.

A note about these graphs on the number of data points needs to be made. The Excel manipulation allowed for every data point taken by the oscilloscope to be used in the calculations. Over two cycles of an 80 kHz signal (25 µs) allowed for over two thousand data points to be used in the calculations. The artifacts in the graphs are due to small voltage variations in the waveforms being measured. All of the data points are left in because it shows two things. First, the trend is shown very well with the mass of data points on the graph, and any shift from the temperature and LED resistance in the response can be seen very well. Second, the data points show that even as the input voltage is decreased below the point of unity gain, there are still data points that show unity gain.

Another note is on the 510 Ω R_{LED} results. The sharp decrease in the voltage gain is due to the large voltage drop over the LED resistance causing the output voltage to clip because it increases above the supply rail. The voltage drop is large because the LED current is created independent of the LED resistance (by the current flowing through the photodiode), and the voltage drop caused by the LED current adds with the LED forward voltage and causes the clipping affect. This shows up as a decrease in the voltage gain at 5 V input for the 50 °C and 4 V for the 70 °C data. The reason why this phenomenon is present at decreasing voltages as temperature increases is explained later.

Figure 4.14 through Figure 4.16 show the same results as before but with the voltage gain versus input voltage broken out for each set of LED resistances compared with the same resistances as temperature increases.

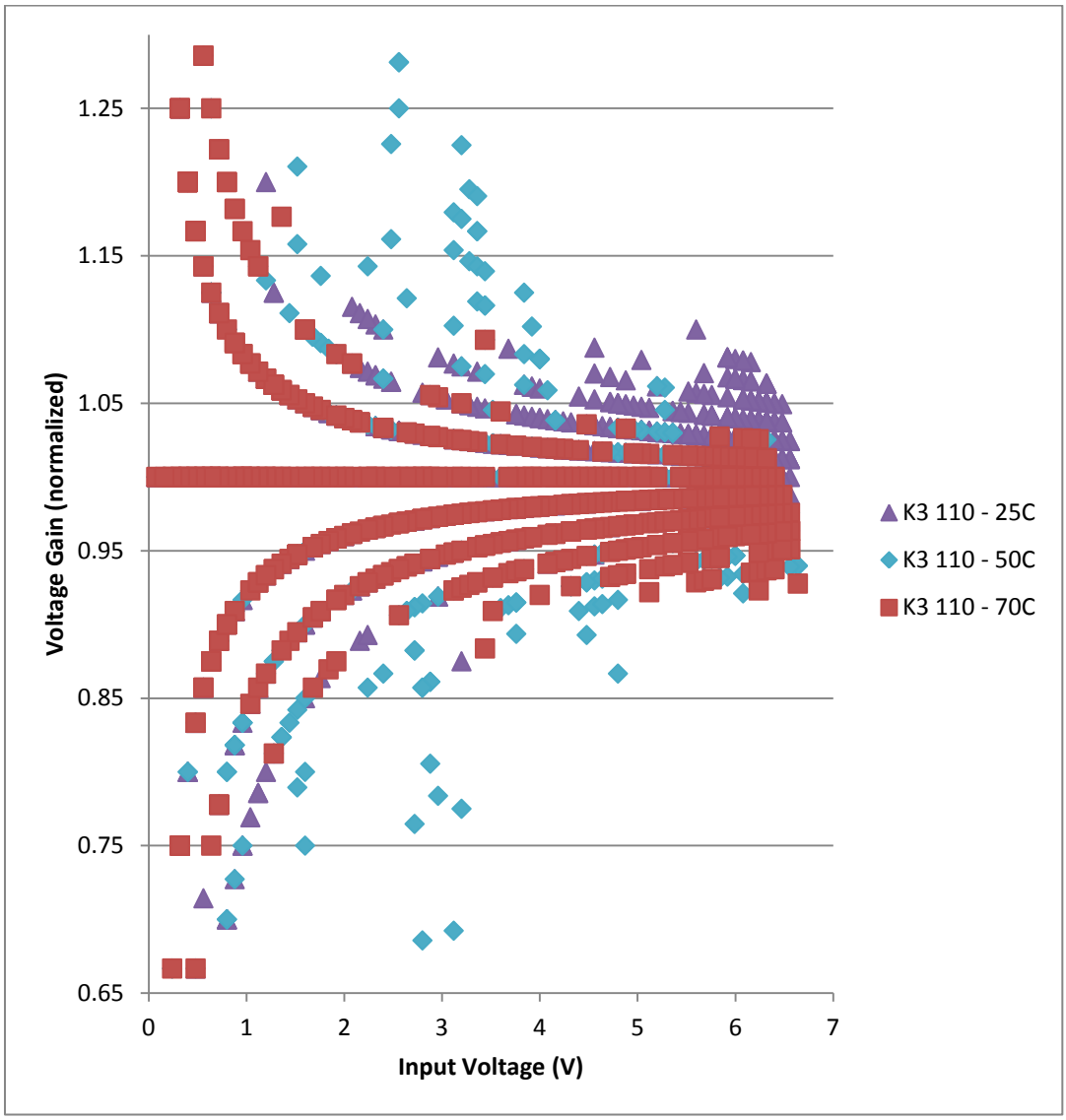


Figure 4.14 Comparison of voltage gain versus input voltage over entire biasing and temperature range for R_{LED} equal to 110 Ω

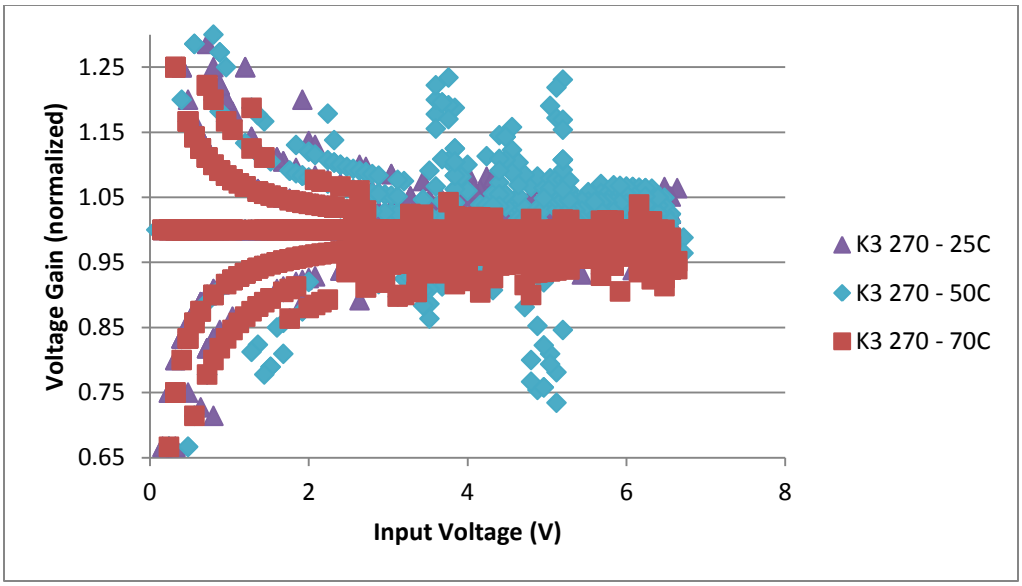


Figure 4.15 Comparison of voltage gain versus input voltage over entire biasing and temperature range for R_{LED} equal to 270 Ω

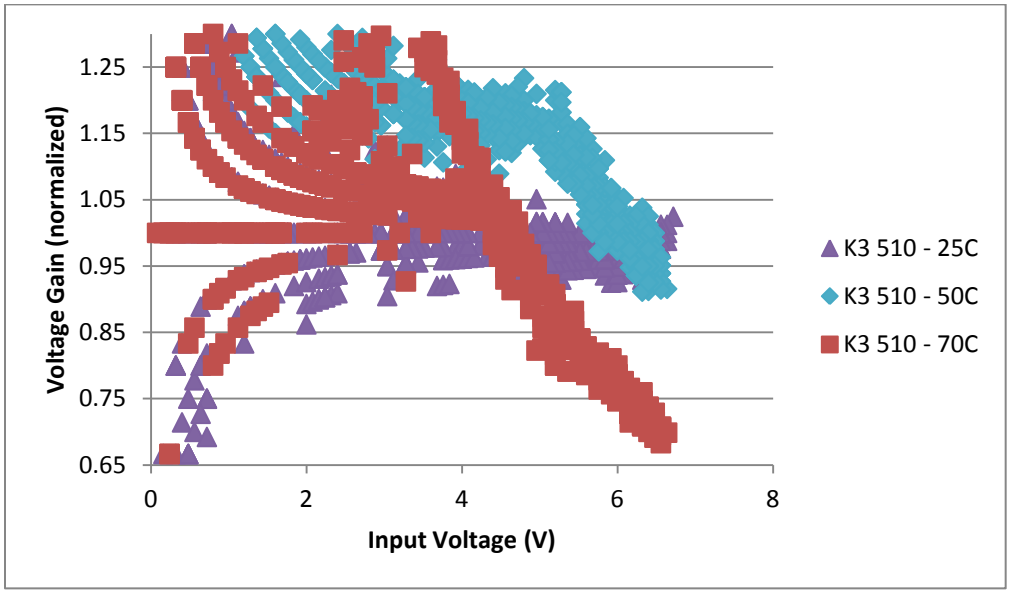


Figure 4.16 Comparison of voltage gain versus input voltage over entire biasing and temperature range for R_{LED} equal to 510 Ω

The 110 Ω and 270 Ω graph are relatively stable as temperature increases. The average gain should be unity gain when the circuit stabilizes above 2 V input but the average gain decreases from unity as temperature increases. This is consistent with the datasheet of the HCNR201, where the K3 decreases with temperature, which would cause a decrease in the voltage gain [12]. There is an approximate 6% decrease in overall voltage gain with temperature. In the 510 Ω graph the temperature affects are more prevalent. The cause of this change can be better seen in the LED current which is formed by the input voltage causing a current to flow in the photodiode. Because the LED needs at least 1.55 V when it is correctly biased the voltage across R_{LED} has to be less than V_{DD}-V_{LED}. In the 510 Ω case the voltage gets above this whenever 16.5 mA flows through the LED. This is the reason for the voltage gain decreasing as the input voltage increases above this threshold. As the temperature increases the LED transfers less energy to the servo diode (6% decrease in CTR over temperature), this means that at the same input voltage for the 70 °C operation there is more current flowing through the diode which causes the voltage across R_{LED} to be greater than V_{DD}-V_{LED} sooner. This causes the decrease in voltage gain much sooner as the temperature increases.

These results will be compared with the voltage gain from the open-loop analog transmission topology seen in the next section in the Conclusions Chapter and it will describe the benchmark for this analog transmission topology. Next, the benchmark experimental results for the analog transmission topology without feedback are discussed.

4.2.3 Open-Loop Analog Transmission Topology Bias Experimental Setup

The open-loop topology is analyzed with experiments in the same way as the previous optocoupler topology. The first, a biasing experiment, determines the output's response to different biasing points of the input LED with the test setup in Figure 4.17 using the MAX4450 and HCNR201 as described previously. The input is a 4 V pulse at 30 kHz with a 50% duty cycle. The value of R_2 is set to

100 kΩ and R_{LED} is swept from 8 kΩ to 110 Ω so that the LED current is biased from 0.5 mA to 18 mA, which covers the entire safe operating range [14]. Data is taken when the topology reaches a steady-state. The values of V_{in}, V_{out}, I_{pd2}, I_{LED}, and I_{src2} are measured while the power consumption, the propagation delay from the input positive edge to the output positive edge, the CTR, and the voltage gain are calculated. The biasing experiment is repeated with R_{LED} set to 510 Ω while the value of R_2 is swept from 22 kΩ to 200 Ω. The propagation delay and the voltage gain is measured and calculated, respectively. This second phase of the experiment is an important step because it will determine if the propagation delay of the op amp is affecting the overall propagation delay for this analog transmission topology. If the propagation delay changes while R_2 changes then the op amp is adding to the overall delay. The following section presents the results from the described experiments.

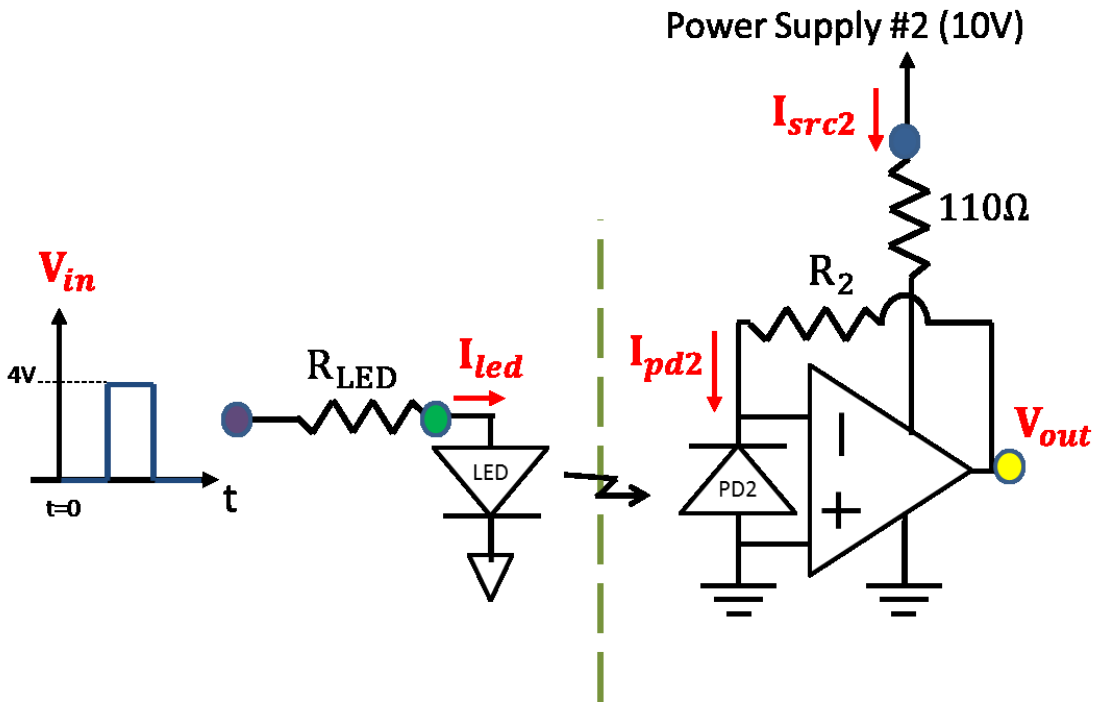


Figure 4.17 Biasing test setup schematic for HCNR201 open-loop analog topology showing the probe placements (the input LED current is measured using the MATH command)

4.2.3.1 Open-Loop Topology Bias Experimental Results

The result of the basing experiment of the open-loop analog transmission topology is shown below. The waveforms in Figure 4.18 show the type of results that were obtained from this experiment. The yellow signal is the input, purple is the output, green is the output stage power consumption, and the red is the input LED current. To measure this topology without skewing the results with the probe capacitance, the output photodiode current is calculated with the output voltage instead of being directly measured like the experimental measurements for the previous topology.

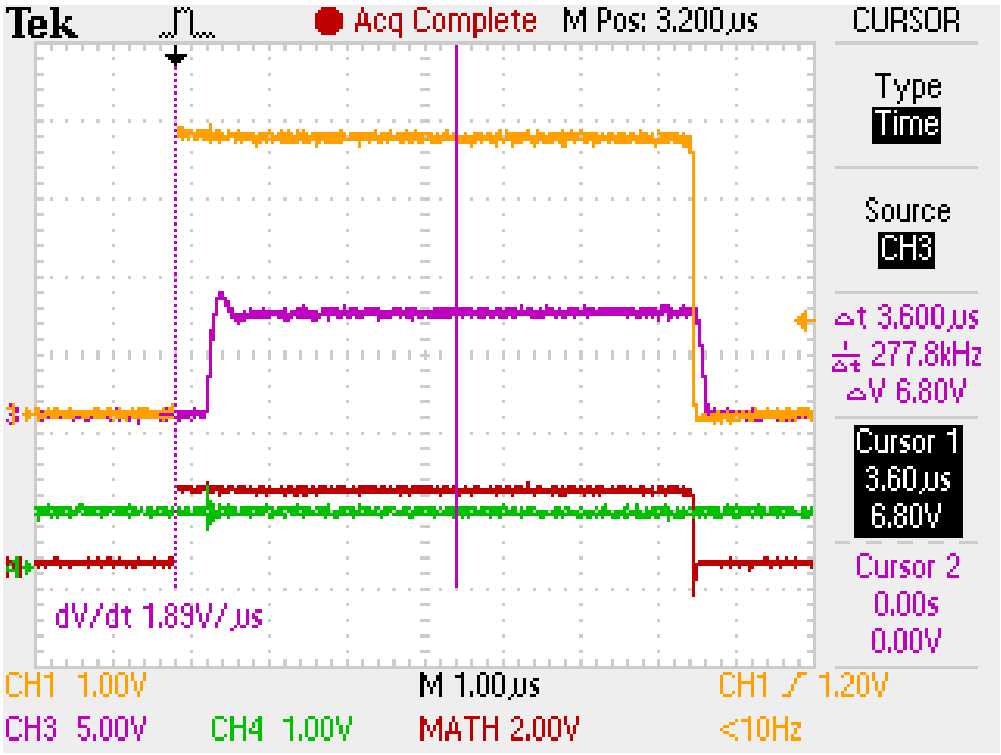


Figure 4.18 Biasing test waveforms for open-loop analog transmission topology, yellow (input), output (purple), output supply current (green), LED current (red)

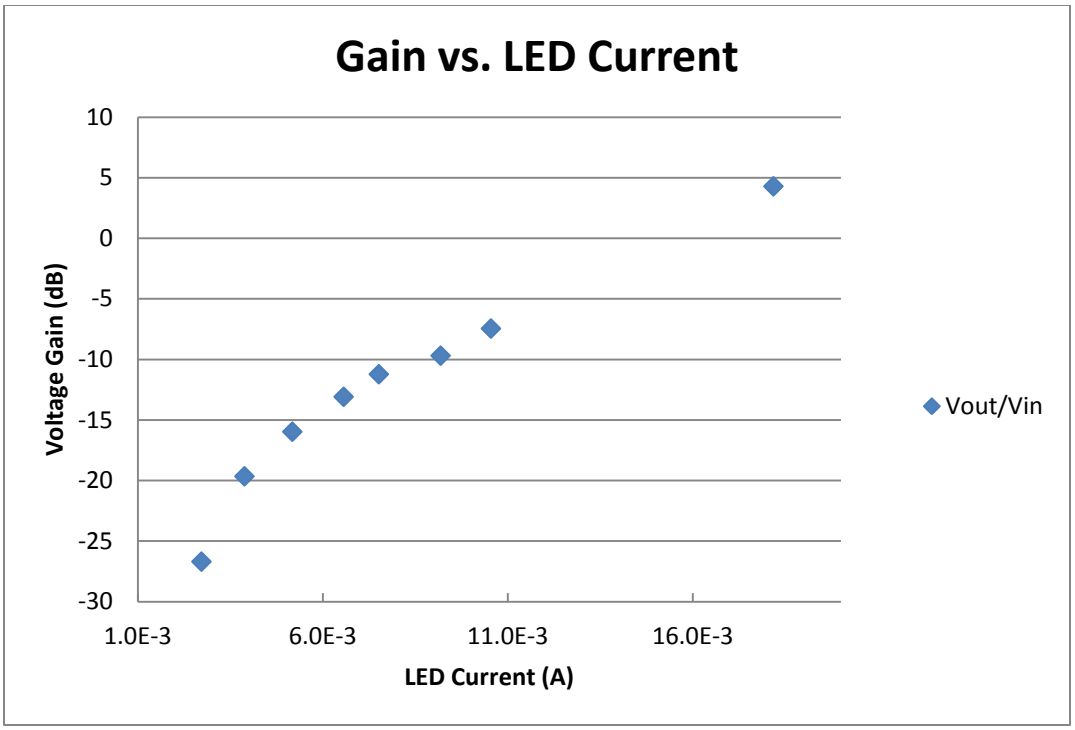


Figure 4.19 Voltage gain versus LED current

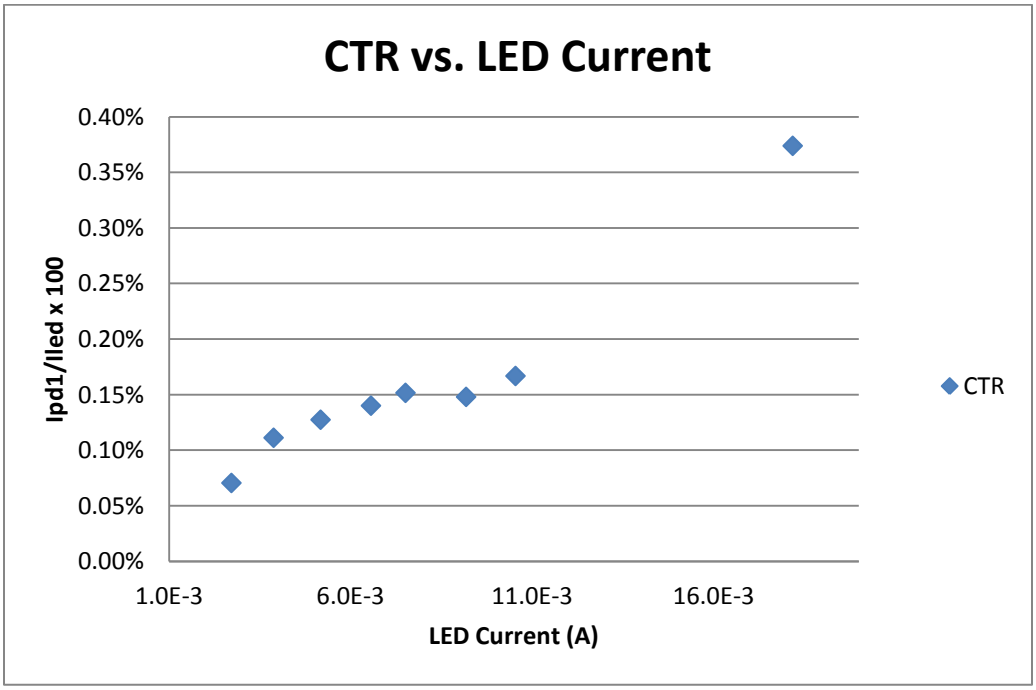


Figure 4.20 CTR versus LED current

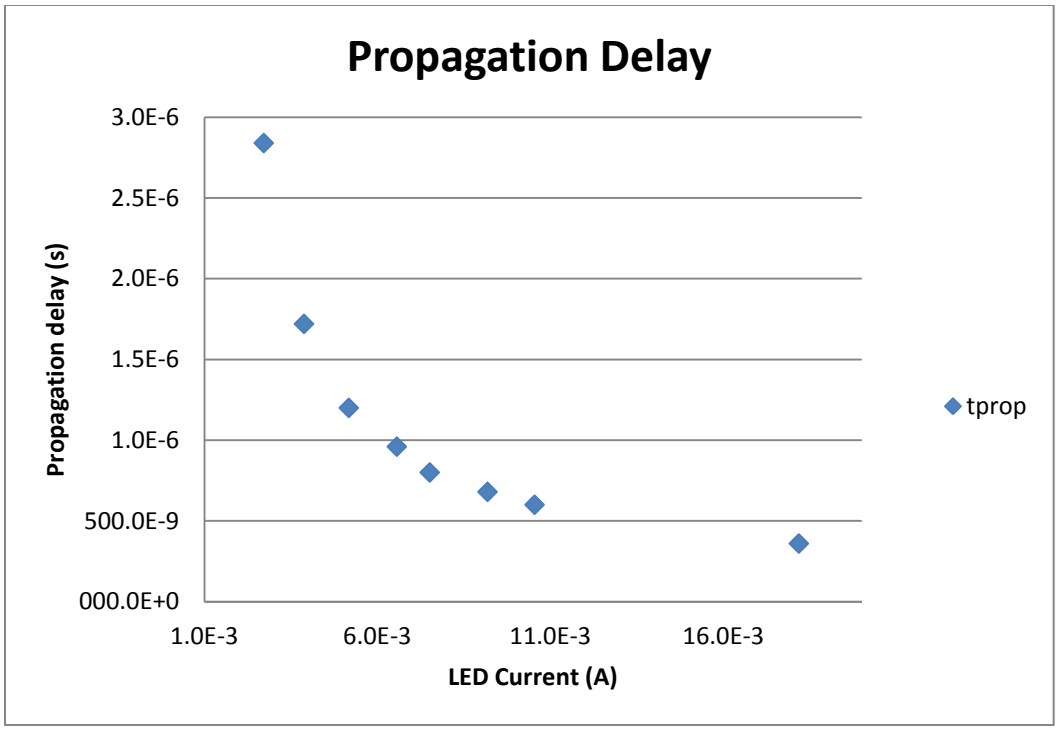


Figure 4.21 Propagation delay versus LED current

Figure 4.19 shows the voltage gain over the changing input bias currents. Also, the change in the CTR can be seen in Figure 4.20 to be non-linear as it increases from 0.10% to just under 0.20% as the input LED current increases. Note that the 0.40% outlier is not an artifact but obtained with a biasing point that is at the extreme edge of the safe operating area so it is not taken into account, but it can be seen to cause another 10 dB increase in the voltage gain. So, a tenth of a percent change in the CTR is seen as a 30 dB change in the voltage gain. This is due to the value of R_2 being so large. It has to be so large to get a voltage at the output that is of a comparable magnitude of the input. To achieve that, R_2 must compensate for the inherent low gain of the optocoupler due to the very small CTR value (about 0.2%). In the previous topology it was seen that the circuit removed the effect of CTR so it had a much more stable gain. This will affect both the outcome of the final benchmark, and the selection and design of the specific topologies for implementation in the Buck converter.

The rise and fall times are not recorded because they do not change with each biasing point (the slope increases as the output voltage increases). The effects of LED current on the propagation delay are shown in Figure 4.21. The propagation delay of the input voltage triggering the output voltage to change decreases as the LED is biased with more current, from 3 μs to 500 ns. The propagation delay could not be decreased any further because the LED cannot be operated with more current. Recall that in the second part of the biasing experiment the value of R_{LED} is held constant (I_{LED}=5.2 mA) and R2 is swept from 22 kΩ to 200 kΩ. The results are shown in Figure 4.22. This shows that the propagation delay of the op amp is affecting the overall propagation delay for this analog transmission optocoupler. The larger the resistance in the feedback path of the output op amp the larger the effect on the propagation delay the op amp has. The 200 kΩ resistor increases the delay by 1 μs. This is difficult to overcome because the CTR is so low a very high gain needs to be added by the output op amp which decreases its bandwidth and thus adds to the delay of the positive edge of the input voltage causing a reaction by the output. This will be a very important design trade-off between the correct voltage gain and the needed propagation delay. These results will be used to determine the benchmark in the Conclusions Chapter and the selection of the specific topologies to be used in the Buck converter. The next section also describes an experiment that will use the biasing information from this experiment to determine more dynamic characteristics of the open-loop analog transmission topology.

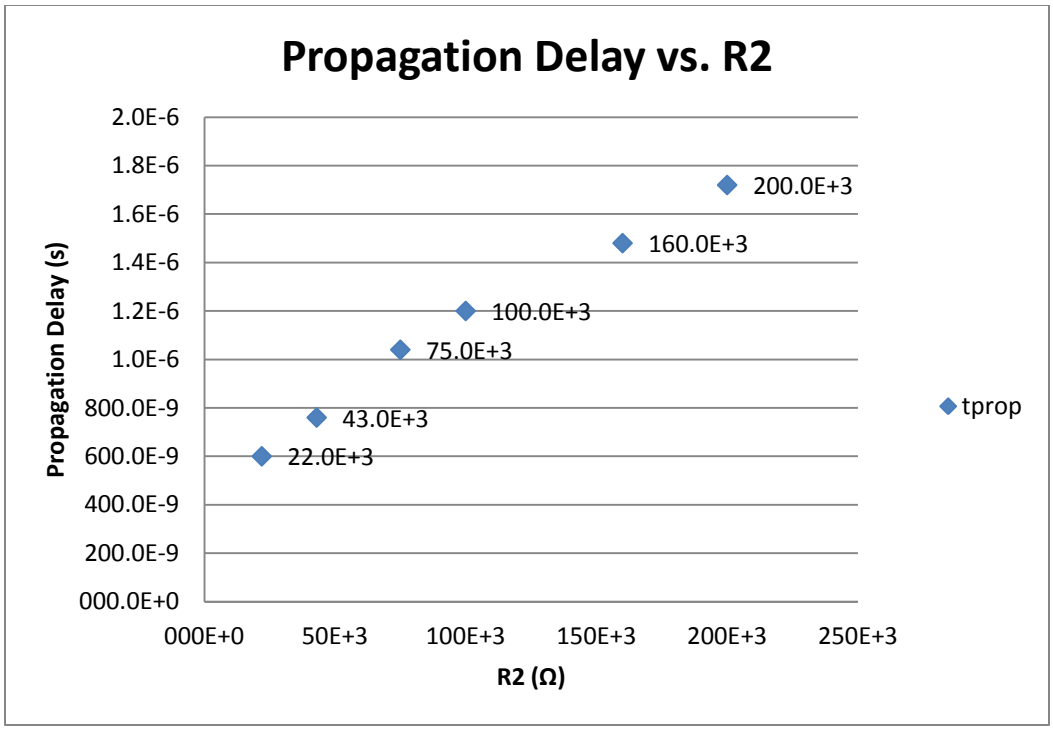


Figure 4.22 Propagation delay versus changes in R_2

4.2.4 Open-Loop Analog Transmission Topology Linearity and Temperature Experimental Setup

Now that the biasing is understood for this topology, a sinusoidal input with a peak-to-peak voltage that spans the entire biasing range is applied and the experiment described below is repeated while the optocoupler is at 25 °C, 50 °C, and 70 °C. This range of temperatures is chosen because it stays well below the maximum temperature of 85 °C. The experiment is repeated for different values of R_{LED}; 110 Ω, 270 Ω, and finally 510 Ω. These are chosen as a good range of biasing from the previous experiment. The experiment is also repeated at each R_{LED} for different values of R_2; 100 kΩ, 75 kΩ, and 45 kΩ. This is performed to understand the impact the op amp's propagation delay on the dynamics of the system while operating with a sinusoidal input. The temperature experiments are not repeated for all the other values of R_{LED} and R_2 from the previous experiment because it was already shown that the biasing points chosen above are the best for this topology in terms of propagation delay, voltage gain, and power consumption. This decision is made because it is the purpose of this research to optimize

these key parameters for the final benchmark and the implementation into the dc-dc converter system. The experimental results at the other non-optimal biasing points would be extraneous.

There are two different input voltages applied over the course of this experiment. Both of them are applied as an 80 kHz sinusoidal waveform. The first input voltage is from 0 to 3.8 V. This is chosen because the input voltage needs to be above a threshold voltage to bias the LED. This threshold is different for each value of R_{LED} since it will decrease the voltage potential at the anode of the LED. This threshold is discovered using the 0 to 3.8 V input waveform. There is also a ceiling because of the variable voltage gain while changing the LED resistance. This maximum input voltage changes for each resistor because the voltage gain will cause the output to increase above the supply rail which clips the output voltage. Once these considerations are determined a second input voltage is applied that changes for each $\mathrm{R_{LED}}$ used in the experiment. The input voltage peak-to-peak differs for each value of $\mathrm{R_{LED}}$ but the circuit is biased consistently so comparisons can still be made. The output peak-to-peak voltage is measured along with the LED current. The CTR is calculated and will be analyzed over the whole input biasing range. This is important because an analysis of CTR will show how it changes over temperature. Also, the voltage gain will be measured and recorded in this same way. Figure 4.23 shows the test setup. To summarize this complex experiment, two main experiments are repeated for different resistor values. The first determines the minimum and maximum input voltage that can be applied for each resistor. The second applies the correct input voltage waveform at 80 kHz for each biasing point and is repeated at each temperature. This experiment will determine the benchmark for this topology and aid in the future selection of the correct topology for the Buck converter.

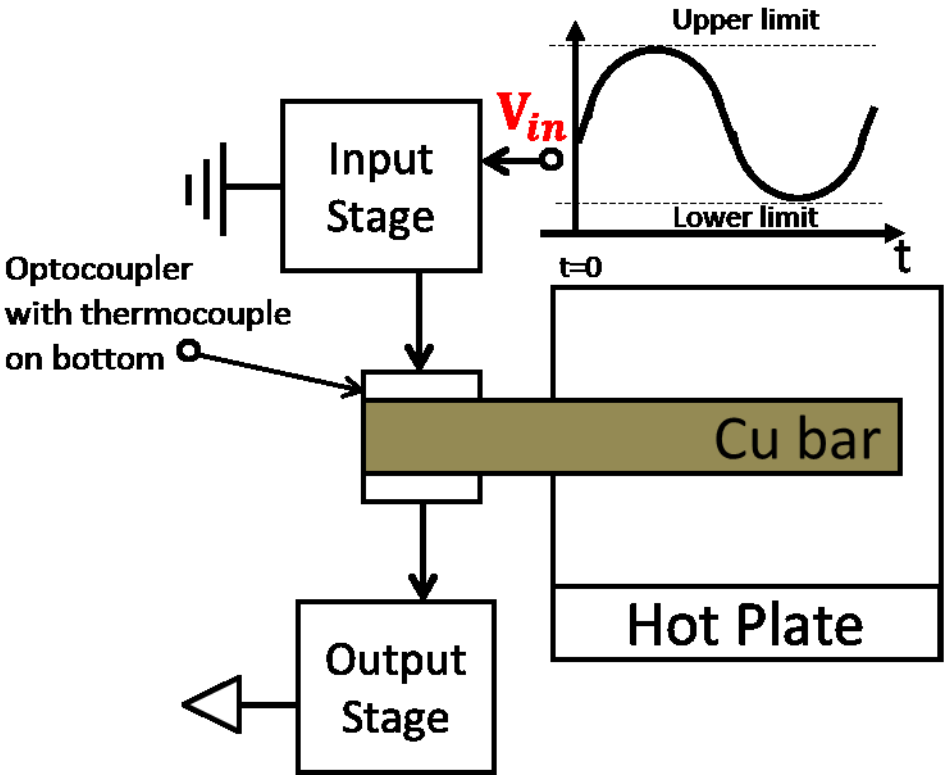


Figure 4.23 Temperature and linearity test setup, probe placement is the same as in the bias test but the input waveform is changed based on discussion above

4.2.4.1 Open-loop Linearity and Temperature Experimental Results

The first results recorded are for the first input voltage applied at 25 °C to show the threshold that the input has to be to initially bias the circuit enough to achieve an output voltage. Figure 4.24 shows the waveforms that present threshold on the input voltage and current. The LED current threshold will be the same at every input LED resistance, but the voltage drop over the resistor causes a larger voltage drop at the same current so more voltage needs to be applied to overcome the larger voltage drop. The thresholds are shown for the different input LED resistances in Table 4.5.

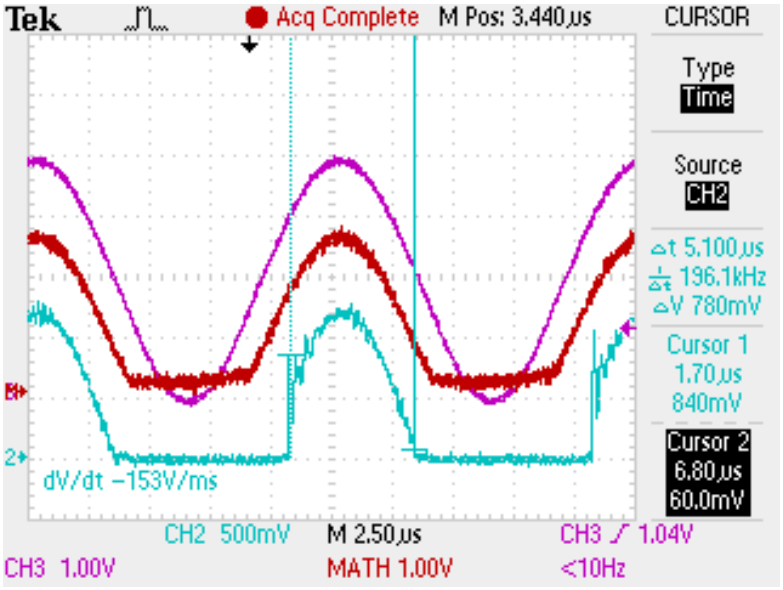


Figure 4.24 Waveform showing input threshold that must be overcome before output has voltage, input (purple), output (blue), I_{LED} (red)

Table 4.5 Input Threshold for Different Values of R_{LED}

R_{LED} (Ω)	Input Threshold (V)
110	1.6
270	1.9
510	2.5

The second part of the experiment applies the correct input voltages repeated for the different resistances and temperatures. This will provide understanding for how CTR changes with respect to input LED resistance, output resistance, and temperature in the open-loop analog transmission topology. The CTR is recorded over the entire range of the input voltage applied by using Excel to calculate the results point by point (the same propagation delay shifts are made on the output as in the previous experiment). The x-axis in the following graphs displays the time the input voltage is applied for one cycle and the y-axis is the CTR as a percentage. The time is arbitrary but it represents one cycle of

the 80 kHz input voltage. In following sections the data will be broken out with the input voltage as the x-axis.

The CTR in these graphs can only be seen as a trend since it is not directly measured against the input voltage, but this will be done more concisely following the explanation of the CTR trends over biasing. The graphs in Figure 4.25 through Figure 4.27 show that with changing output resistances (R_2) the CTR is held constant, which is expected, but showing it verifies the results are accurate with the understood concepts, the output resistor should not have an effect on the current transfer ratio of LED current to photodiode current. Also, the CTR is very non-linear for regions outside of what will be defined as the plateau region. The plateau region is defined by a region where the CTR is within ±5% of a flat value. The non-linear region is located on either side of the plateau region and is seen by a sharp decrease from the value of the plateau region to 0% where the LED current reaches 0 A.

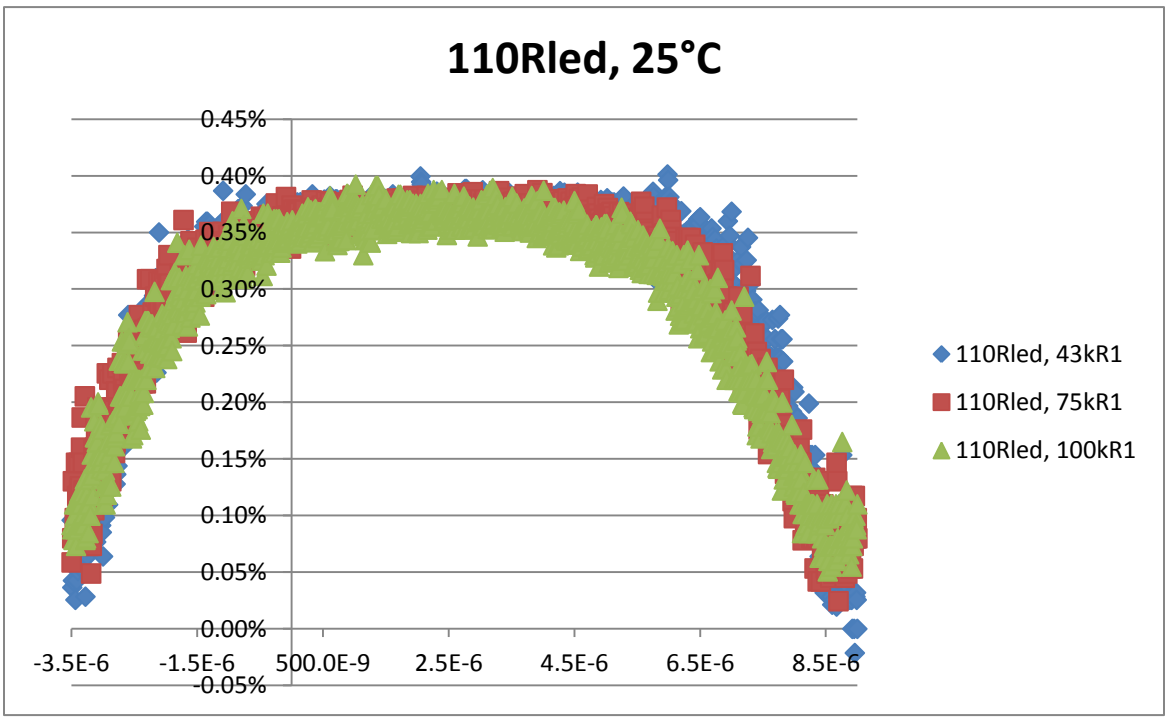


Figure 4.25 CTR over entire time of input voltage range for different R2's with R_{LED} equal to 110 Ω

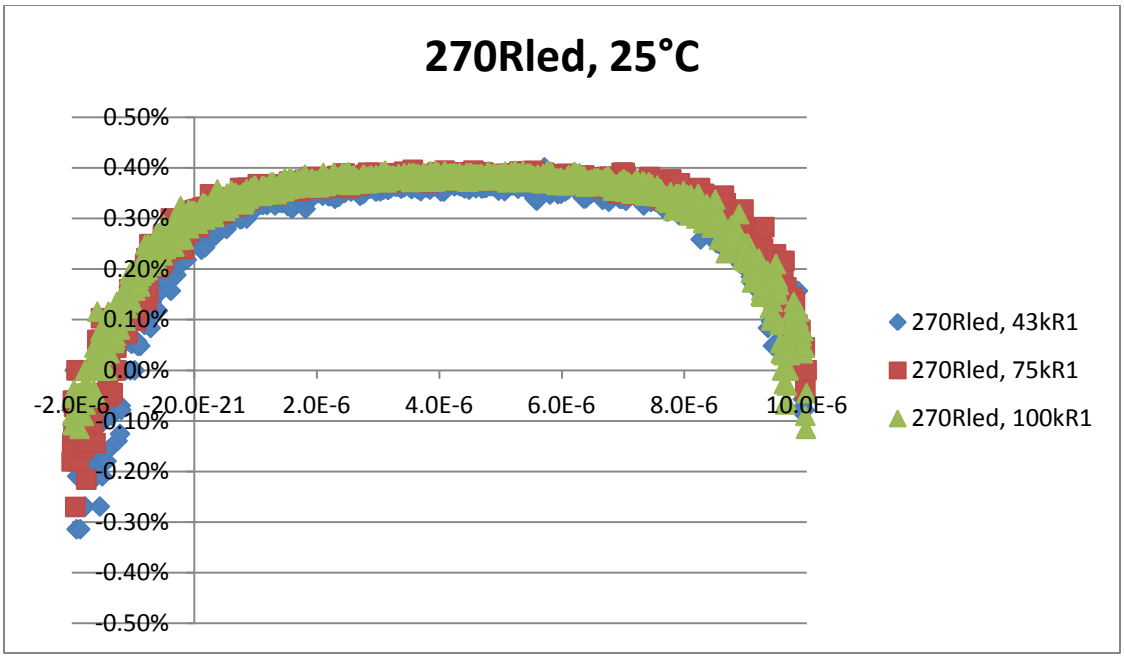


Figure 4.26 CTR over entire time of input voltage range for different R2's with R_{LED} equal to 270 Ω

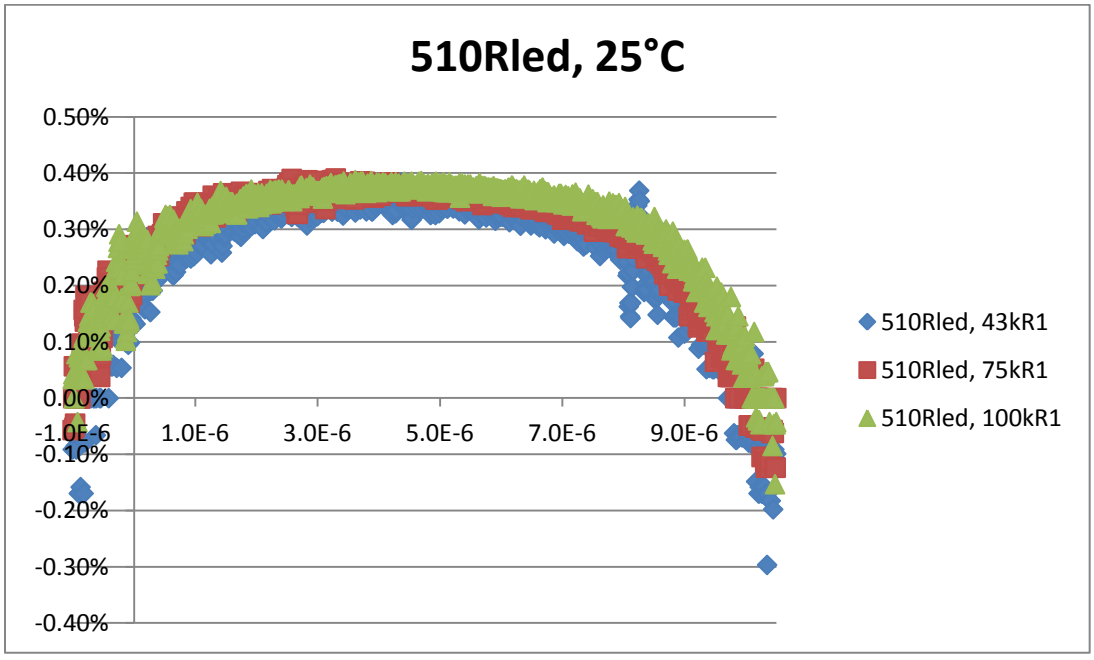


Figure 4.27 CTR over entire time of input voltage range for different R2's with R_{LED}equal to 510 Ω

The relationship between the plateau region, the input voltage, and current is better presented when the x-axis is in terms of the input voltage and the input LED current. This is shown in Figure 4.28 and Figure 4.29, respectively, at 25 °C. Because there is not a noticeable change when the different output resistances are used (as seen in the trends in the previous figures), the 43 kΩ resistor experimental results are arbitrarily chosen to be displayed to simplify the presentation. The threshold voltages can also be seen in these figures at the point the CTR starts to increase representing the LED current being above 0 A. The graph in Figure 4.29 shows that the CTR trend with respect to LED current is the same for all of the different LED resistors; this verifies the results are consistent. It also shows that the plateau region starts at the same current value of 16 mA. The input current in the 270 Ω and the 510 Ω plots do not go as far as the 110 Ω plot because the input voltage is limited to a smaller voltage maximum due to the voltage gain increasing with decreasing resistance, but the trend is still shown to be consistent. The plateau region is defined in Table 4.6.

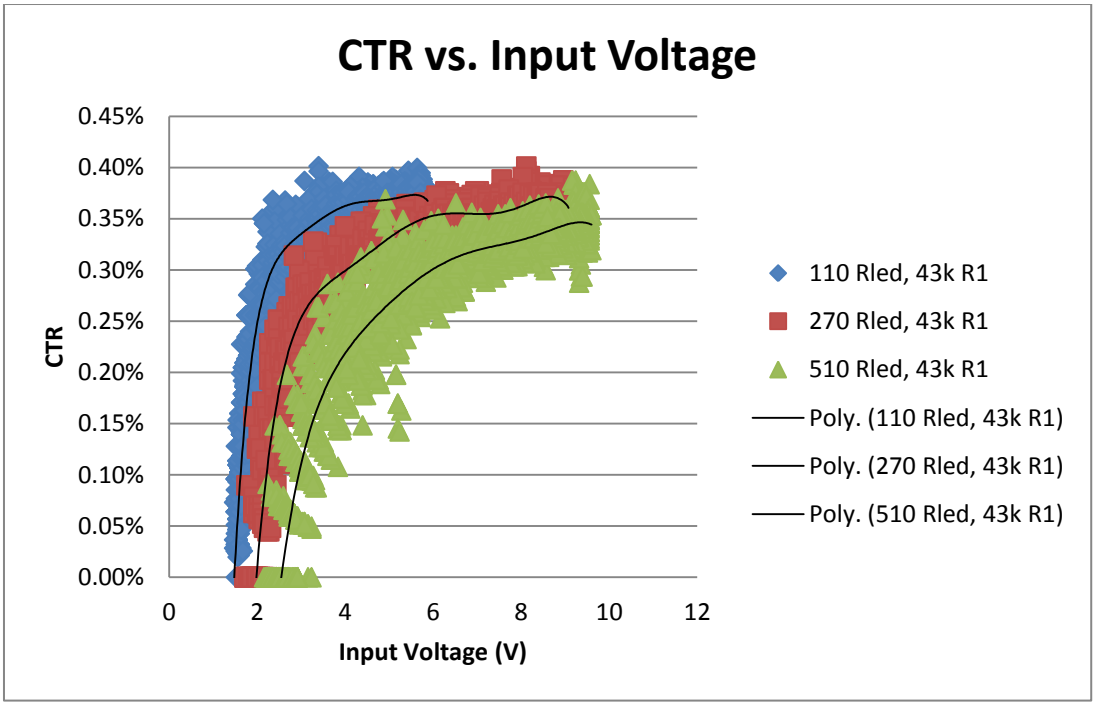


Figure 4.28 Relationship between CTR and input voltage for different R_{LED}s

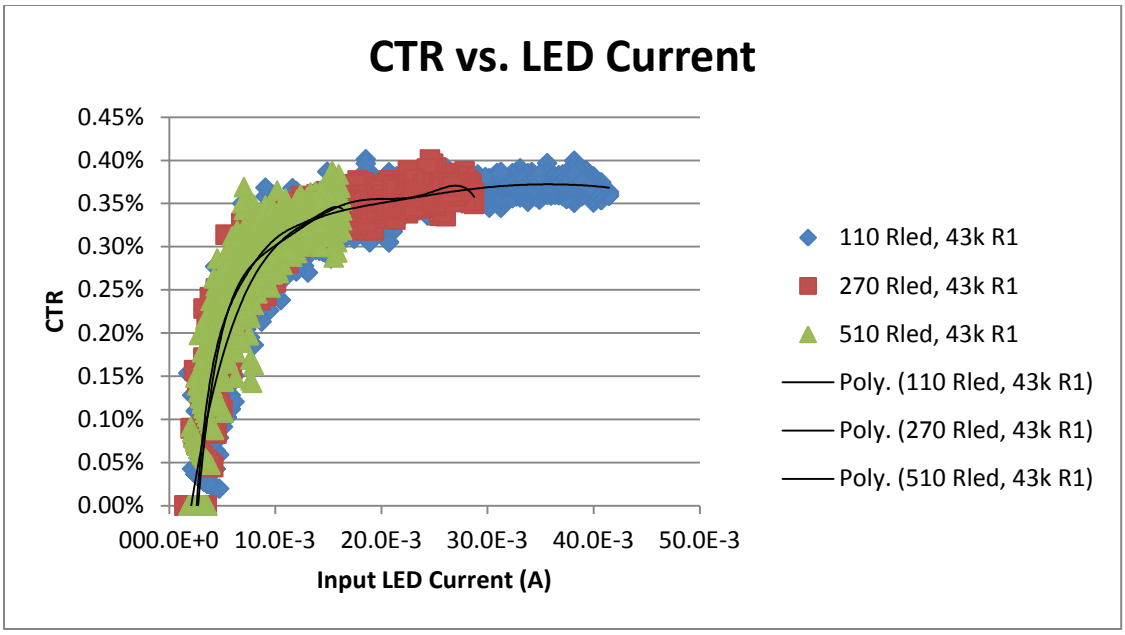


Figure 4.29 Relationship between CTR and LED current for different R_{LED}'s

Table 4.6 Plateau Region for Different R_{LED}'s

	Plateau Region (V)	
R_{LED} (Ω)	Input Voltage (V)	LED Current (mA)
110	3	16
270	5	16
510	7	16

Table 4.7 Propagation Delay for Different R_{LED}'s

		Propagation Delay (ns)		
R_{LED} (Ω)	R_2 (Ω)	25°C	50°C	70°C
110	43k	120	90	100
	75k	140	130	120
	100k	190	210	140
270	43k	120	110	160
	75k	130	150	180
	100k	140	130	180
510	43k	210	150	140
	75k	240	210	180
	100k	180	200	180

The data in

Table 4.7 shows the propagation delay with respect to temperature and LED resistor. The trend for the propagation delay for this topology is to stay within ±20% of 200 ns for all ranges of temperature and output resistance. This continues the trend of the mechanism of propagation delay to be complex. This topology does have a more stable propagation delay over a sinusoidal input than when a dc value is applied. Figure 4.30 through Figure 4.32 show the CTR change over temperature for each LED resistor plotted against the input voltage. The output resistor is held constant but arbitrary to the results as stated earlier, it does not affect CTR.

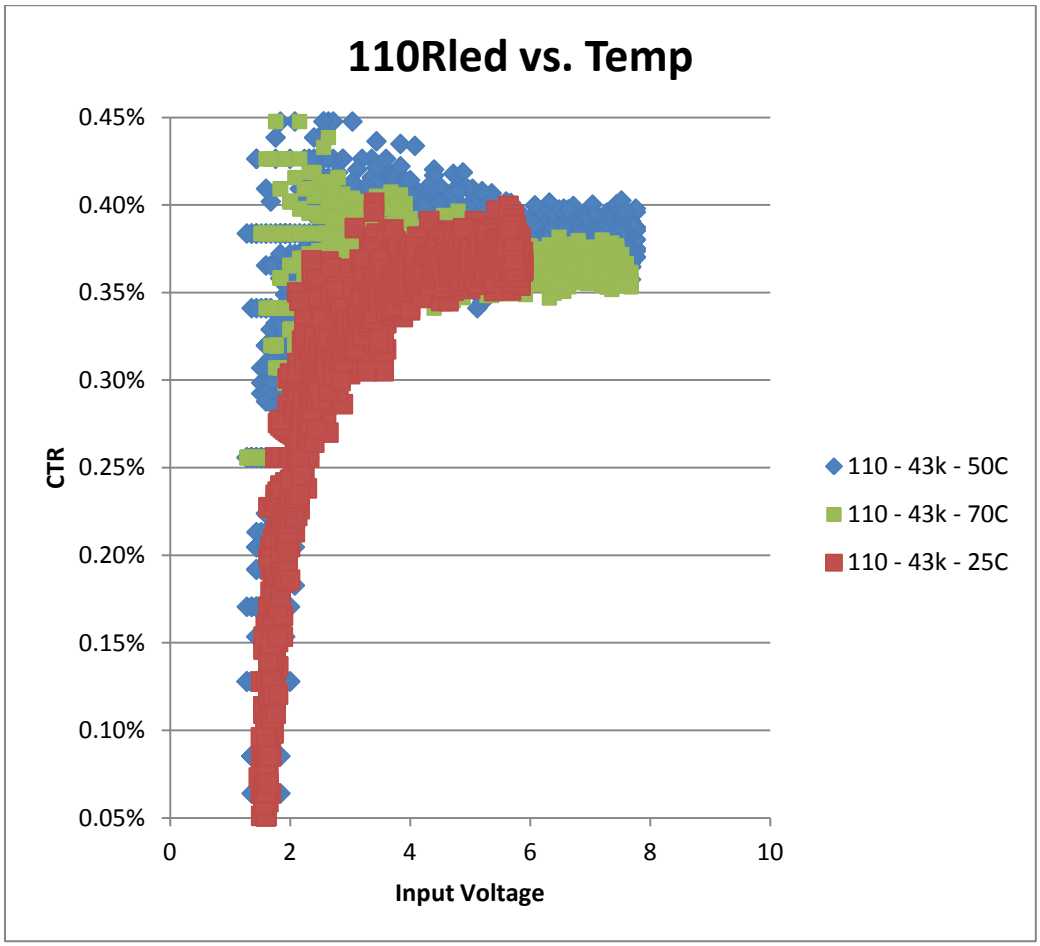


Figure 4.30 Comparison of CTR versus input voltage over temperature range for R_{LED} equal to 110 Ω

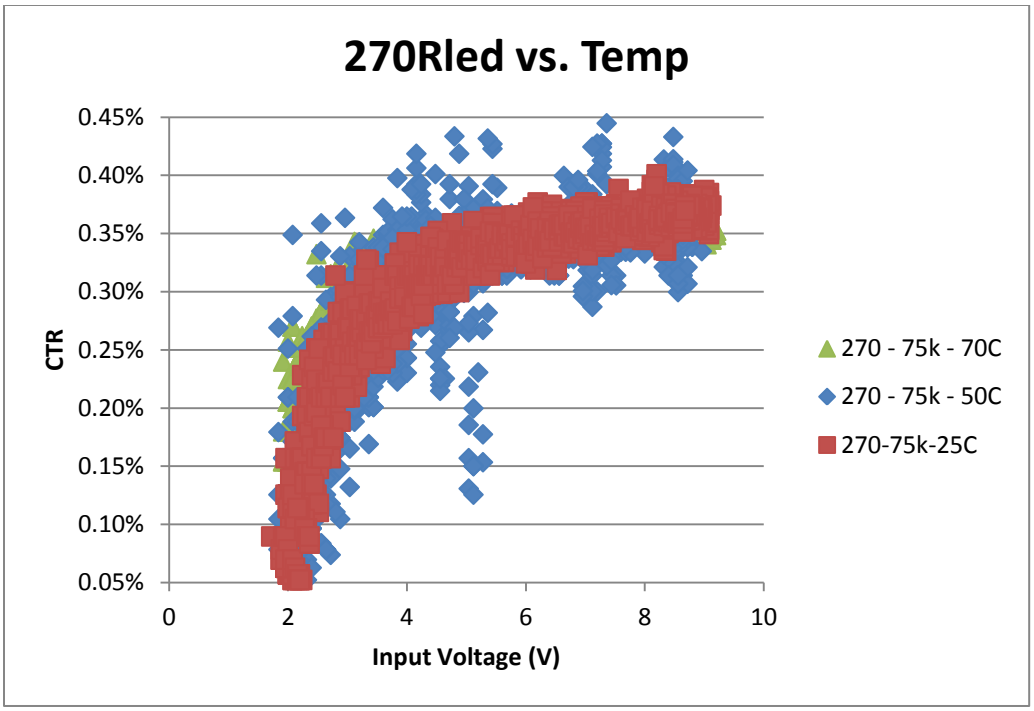


Figure 4.31 Comparison of CTR versus input voltage over temperature range for R_{LED} equal to 270 Ω

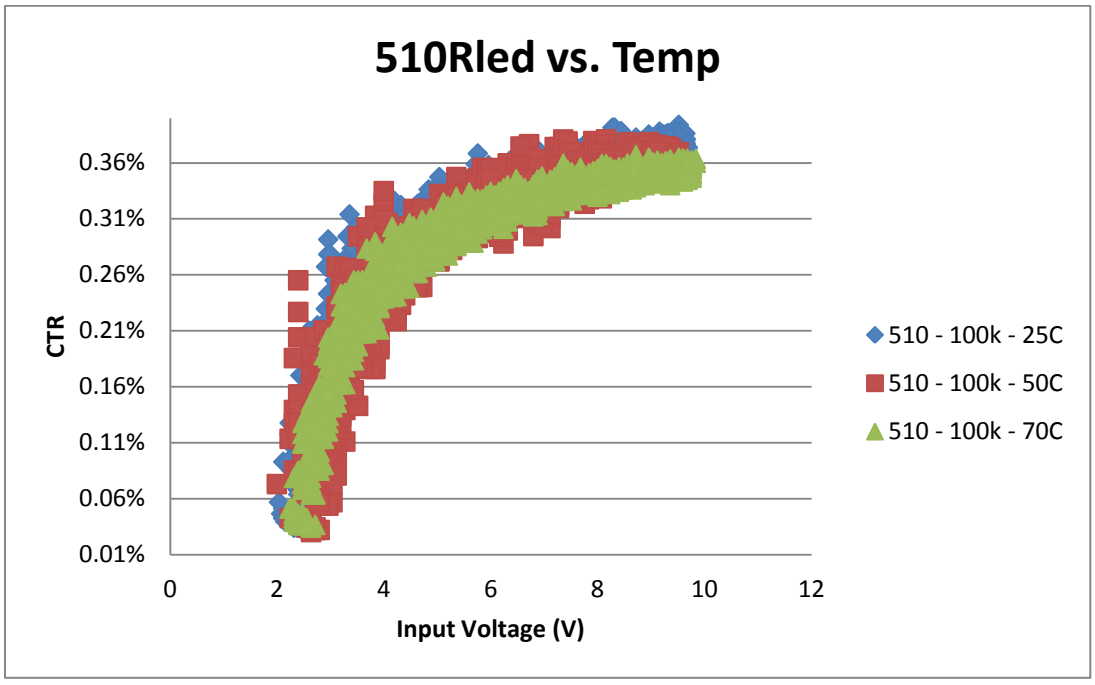


Figure 4.32 Comparison of CTR versus input voltage over temperature range for R_{LED} equal to 510 Ω

The CTR decreases by 4% on average as temperature increases. As shown in the biasing experiment this is represented by a much larger voltage gain decrease. This introduces very large non-linearities and will be summarized in the Conclusions Chapter in the final benchmark.

This concludes the discussion of the results from both of the analog transmission topologies. The design decisions for the implementing the correct topology is made in the Optocoupler and Buck Converter Chapter. The next section describes the experiments to determine which digital transmission approach will be implemented in the Buck converter and the final digital optocoupler benchmark.

4.3 Benchmark Experiments for Digital Transmission Topologies

The optocouplers in this section were shown in Table 4.1 and were chosen because a comparison between GaAsP and AlGaAs needs to be made. The optocouplers have the auxiliary circuitry internal to the package except for the topology with the LED and photodiode base BJT pair. The latter type needs an external pull-up resistor that affects power consumption and minimum pulse width. The analysis of these topologies is to find the best one for the Buck converter and determine the benchmark of the digital optocoupler topology. The analysis is broken down into five distinct experiments. The first four experiments are used to analyze the two different optocoupler topologies. Note that there are two different optocouplers representing the two materials in each topology – the two material types in the NPN BJT category and the two for the totem pole amplifiers. The fifth experiment takes the best topologies (ranked by the key parameters that have been discussed -- power consumption, propagation delay, and minimum pulse width) and implements the same experiments at the best operating point of the devices over temperature. The CTR is not an important parameter in these tests because the output stage is forced to switch fully on, or off, depending on the input. The optocoupler in each category was specifically chosen because it was the fastest and least power consuming of the optocouplers analyzed in the chart at the beginning of this chapter, Figure 4.1.

4.3.1 LED BJT Pair Digital Transmission Optocoupler Experimental Setup

The first topology to be analyzed is the LED and BJT pair. The two optocouplers in this category are the GaAsP HCPL4505 and the AlGaAs HCNW4505 [13]. These optocouplers will be put through the same experiments and compared to each other to find the one that has the best power consumption, propagation delay, and rise and fall times. The values of V_{in}, V_{out}, I_{LED}, I_C, and I_{src} are measured while the power consumption, rise and fall time, and the propagation delay are calculated. The input is a ten cycle pulse of 10 V and the steady-state values are recorded. To find the best biasing point R_2 is held at a constant 1 kΩ while R_{LED} is swept from 16 kΩ to 400 Ω corresponding to an LED current of 0.5 mA to 20 mA, which is within the safe operating range for both optocouplers. This part of the experiment will discover which operating point optimizes the key parameters. The best biasing point then selected and an experiment is repeated with the same input waveform and the LED resistance held constant while the output resistance R_2 is changed from 510 Ω to 16 kΩ to find the minimum rise and fall times for each optocoupler. The experimental setup is shown in Figure 4.33.

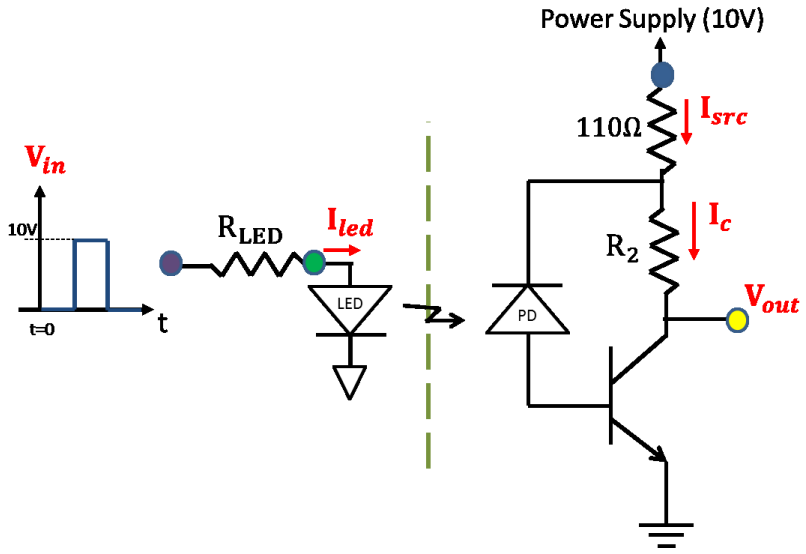


Figure 4.33 Experimental setup schematic for HCPL4505 and HCNW4505 LED/BJT pair digital topology with probe locations shown (LED current is measured with MATH)

The first results represent the data recorded for both the HCNW4505 and the HCPL4505 when the output resistance R_1 is set to 1 kΩ and the experiment is repeated for different values of the input LED resistance. Note that the output is inverted from the input signal. With an output resistance of 1.5 kΩ the HCNW output BJT is in the active mode and the output can only be as low as 0.2 V, but at 1 kΩ the output voltage is only 1.2 V, in saturation mode. The HCPL output BJT never falls below 0.8 V. The trade-off between saturation and active mode is that the fall time is much slower because of minority carriers having to be swept out of the base region. Figure 4.34 presents the raw waveforms for the experiment before the data is extracted and presented. Note that as it has been defined, the rise time is when the output changes to the low-state, and the fall time is when the output changes to the high-state. This is to be consistent when compared to the analog transmission rise and fall time corresponding to the input being applied and removed, respectively.

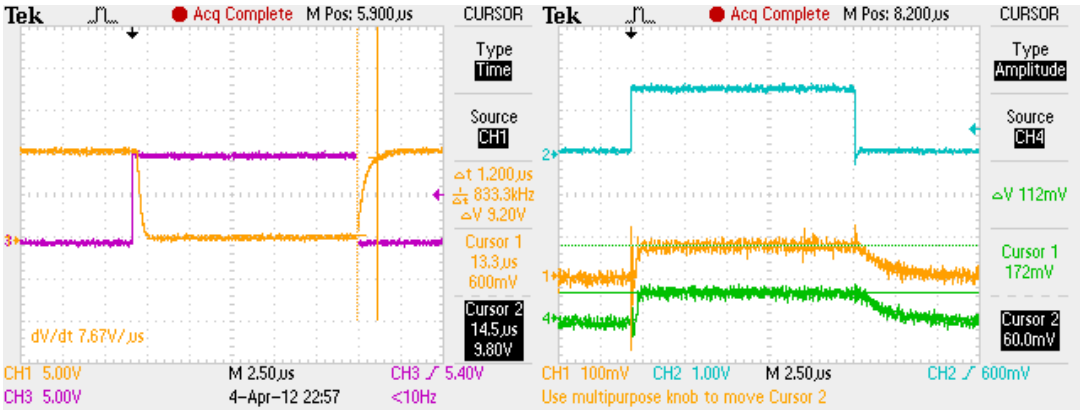


Figure 4.34 Waveform from test; (left) input (purple), output (yellow); (right) LED current (blue), power supply current (yellow), collector current (green)

Figure 4.35 shows the comparison of the propagation delay and the rise and fall time compared across all of the different biasing points showing off the differences between the HCNW4505 and the HCPL4505.

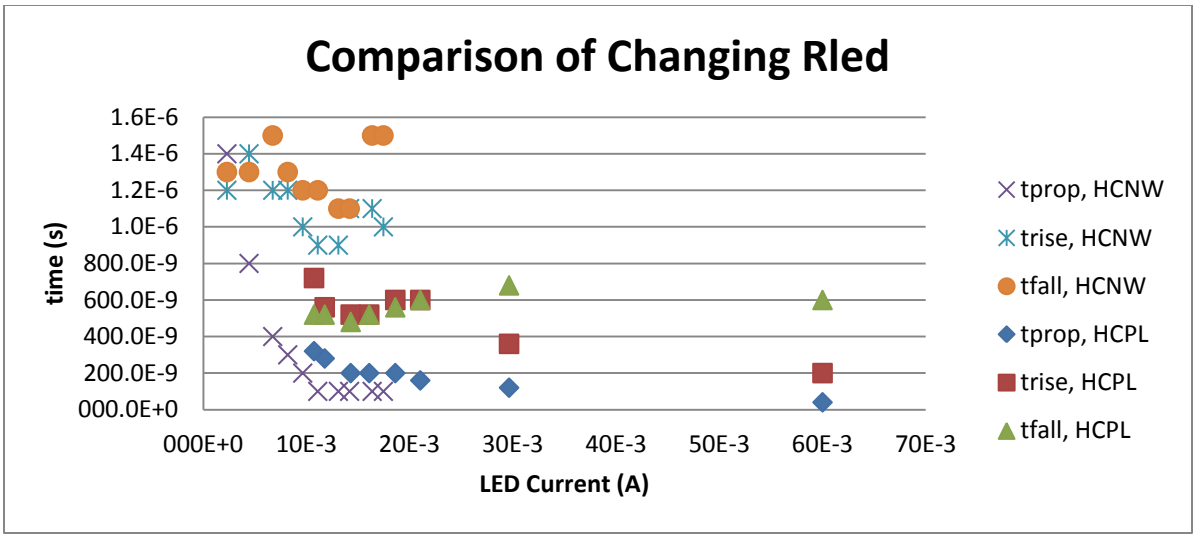


Figure 4.35 Comparison between HCNW4505 and HCPL4505 of rise/fall and propagation times versus LED current and changing R_{LED}

In the initial parts of the biasing experiment (when the input LED resistor is a large value) the output of either of the optocouplers does not fully switch to the low-state. For the output to completely switch the LED needs to be biased with at least 10 mA for the HCNW4505 and 21 mA for the HCPL4505. The HCNW4505 requires 20 mA less current to be at the same propagation delay, but its fall and rise times are 50% to 100% larger. The 400 Ω LED resistance is chosen as the optimal biasing point for the HCNW because the output response is the fastest. Following the same analysis for the HCPL, the LED resistance is chosen to be 270 Ω.

Now that the nominal R_{LED} is chosen, the second part of the experiment can be performed. Figure 4.36 shows the propagation delay and rise and fall times with changing output resistances. The x-axis is shown as power dissipation of the output stage to show the relationship between power consumption and turn-off time (fall time). Because the LED is biased properly the propagation delay stays constant.

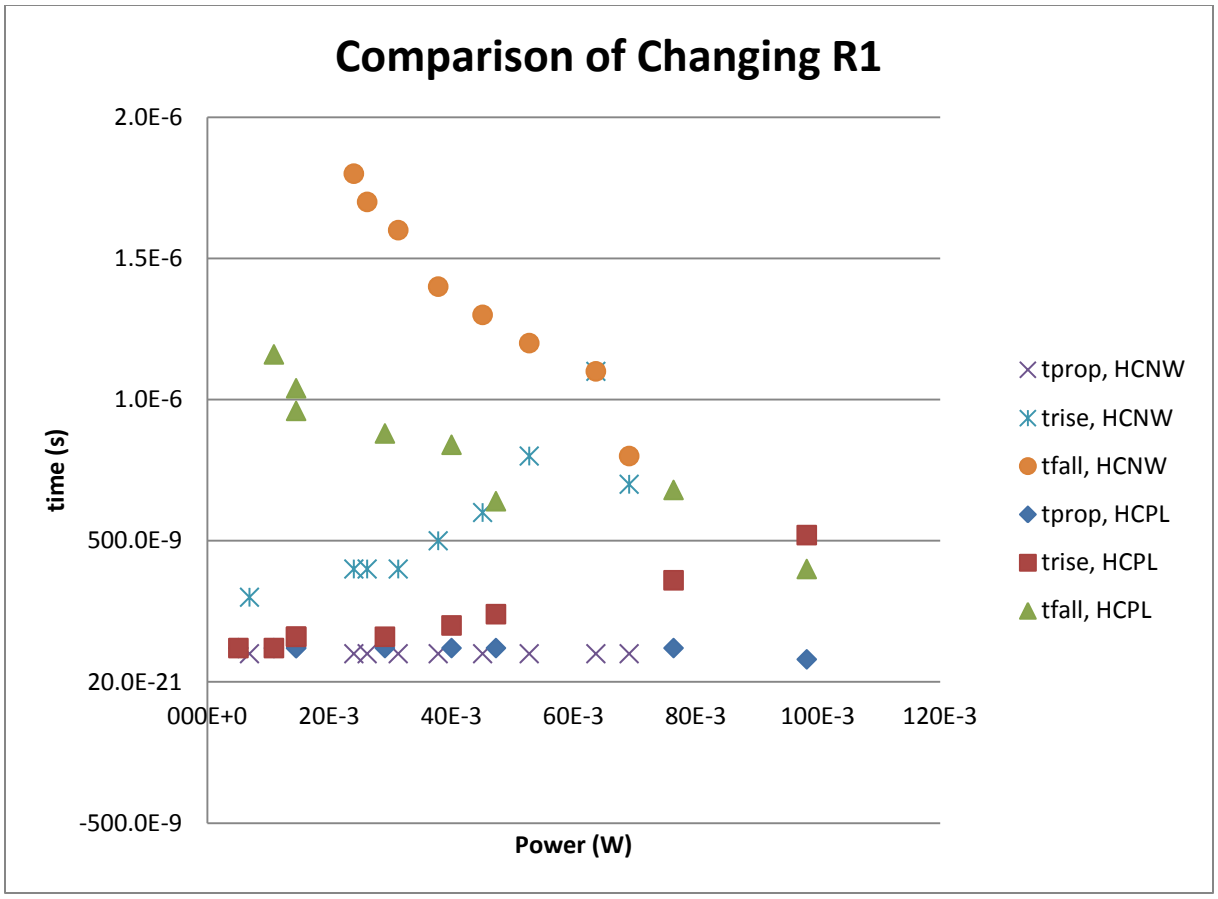


Figure 4.36 Comparison between HCNW4505 and HCPL4505 of rise/fall and propagation times versus power consumption for changing R_2

As the output power increases from 20 mW to 100 mW (representing decreasing output resistances) two things happen. First, the fall time for the HCPL decreases from 1.2 µs to 400 ns and the HCNW from 1.8 µs to 750 ns. Secondly, the rise time for the HCPL increases from 100 ns to 500 ns and the HCNW from 250 ns to 750 ns The HCPL4505 has the same propagation delay and smaller fall and rise times with the same power dissipation on the output. Because of this and the fact that the topology selection for the Buck converter and benchmark are determined by the optimal values for propagation delay, rise and fall times, and power consumption, the HCPL4505 is chosen for the final experiment that repeats the previous procedures at varying temperatures.

4.3.2 Amplifier Digital Optocoupler Benchmark Experimental Setup

The two optocouplers in this category are the GaAsP ACPL-071L and AlGaAs HCPL-7723 [11], [10]. These two optocouplers have output amplifiers internal to the package that magnify the photodiode current with a CMOS totem pole output stage. The HCPL-7723 also has an input amplifier internal to the package. These optocouplers can only utilize a maximum of 5 V on output stage power supply. The only thing that can be changed about the biasing is the input LED current. The input voltage is pulsed to 4 V (the maximum input voltage) for the ACPL-071L, and the value of R_{LED} is changed from 820 Ω to 270 Ω corresponding to an LED current of 4 mA to 9 mA [11]. The system variables V_{in}, I_{led}, I_{src}, and V_{out} are measured and the power consumption of the output, the propagation delay, and the rise and fall time are calculated. Figure 4.37 shows the experimental setup for the ACPL-071L.

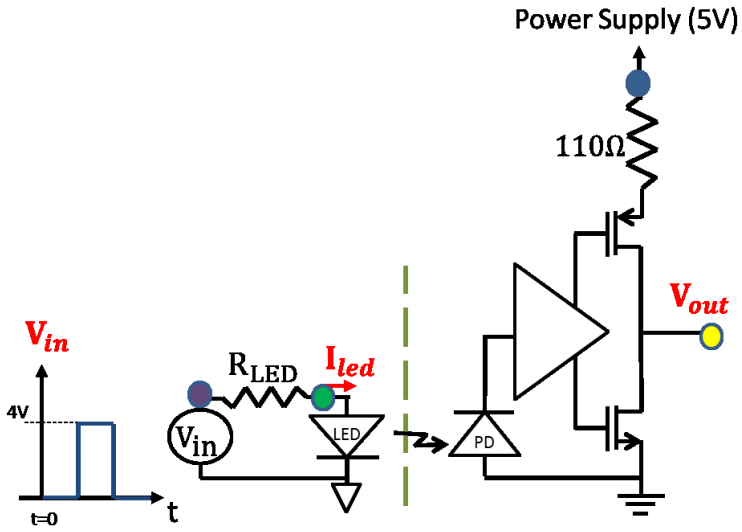


Figure 4.37 Experimental setup for the ACPL-071L LED/amp digital topology with probe locations

The HCPL-7723 has to have a slightly different experimental setup. The input does not need an LED resistance to bias the LED. Figure 4.38 shows the experimental setup, which shows the input stage is a buffer that biases the LED internally. The input voltage is pulsed to 2 V which is the maximum while

the input power supply is at 5 V [10]. V_{in}, I_{src1}, I_{src2}, and V_{out} are measured so that the power consumption, the propagation delay, and the rise and fall times can be calculated.

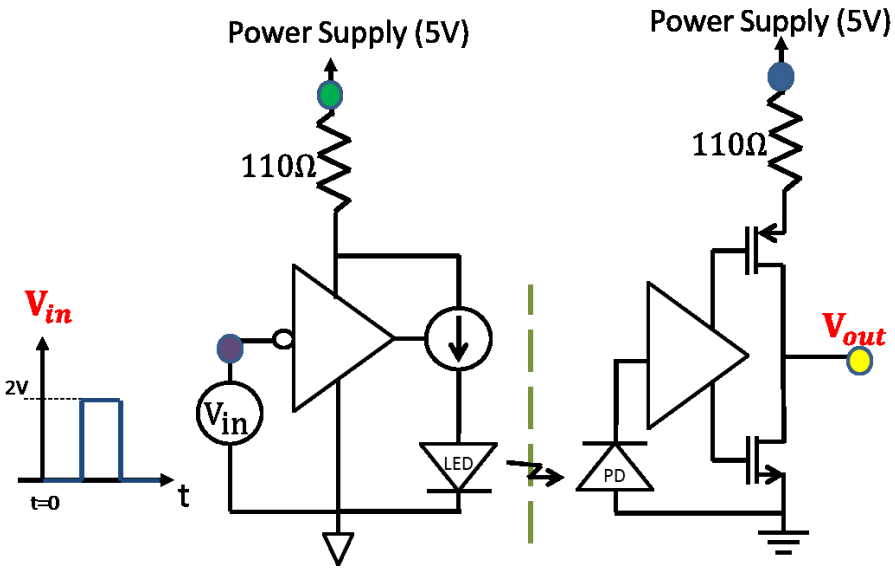


Figure 4.38 Experimental setup for the HCPL7723 amp-LED/amp digital topology with probe locations

The amplifier digital topologies are discovered to be very stiff systems; the measured parameters stay very consistent throughout the experiments. The ACPL-071L experimental results are presented below. This optocoupler uses a complete system in a package. The input LED is biased with a resistor that can be anywhere from 680 Ω to 110 Ω without changing the output characteristics. The maximum input voltage and output supply voltage is 5 V, so the power calculations cannot be compared with the other digital transmission topologies unless they are scaled by a factor of 2. Also, because these devices utilize an optimized output stage the propagation delay and rise and fall times are so short that the input pulse had to be increased to 1 MHz. At this speed the parameters can be more easily measured and Table 4.8 shows the recorded data and Figure 4.39 show the corresponding waveforms.

Table 4.8 Results for Two Different Operating Points

Recorded at 1 MHz		
R_{LED} (Ω)	**270**	**110**
V_{in} (V)	4	3.52
V_{out} (V)	0.32	0.32
I_{LED} (mA)	9.2	18.2
P_{out} (mW)	22.5	22.5
t_{prop} (ns)	50	48
t_{rise} (ns)	20	12
t_{fall} (ns)	30	16

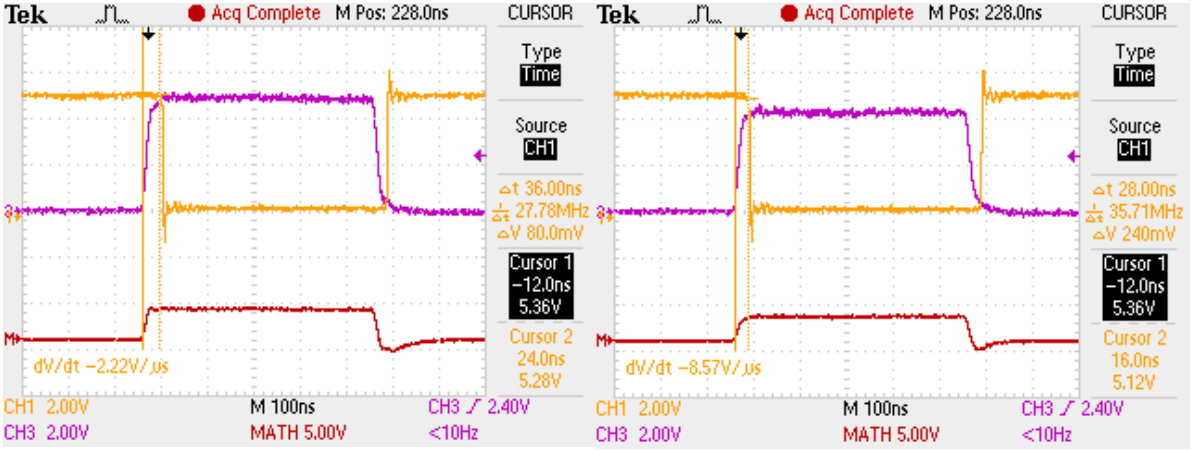


Figure 4.39 Waveforms for data points shown in Table 4.8 (left) 270 Ω, (right)) 110 Ω; output (yellow), input (purple), LED current (red)

The HCPL7723 is an even more all-in-one package with an amplifier biasing the LED and an output stage consisting of another amplifier. The experimental results are recorded below. Because of the all-in-one package, there is no need for an input LED resistor. The input voltage can be a maximum of 2 V to change the output and the input and output supply voltages must be 5 V, and there is not anything to do to bias it differently. Figure 4.40 and Table 4.9 show the only needed data point.

Table 4.9 Results for HCPL7723

V_{in} (V)	2
V_{out} (V)	4.08
P_{in} (W)	0.06
P_{out} (W)	0.013
t_{prop} (ns)	24
t_{rise} (ns)	20
t_{fall} (ns)	44

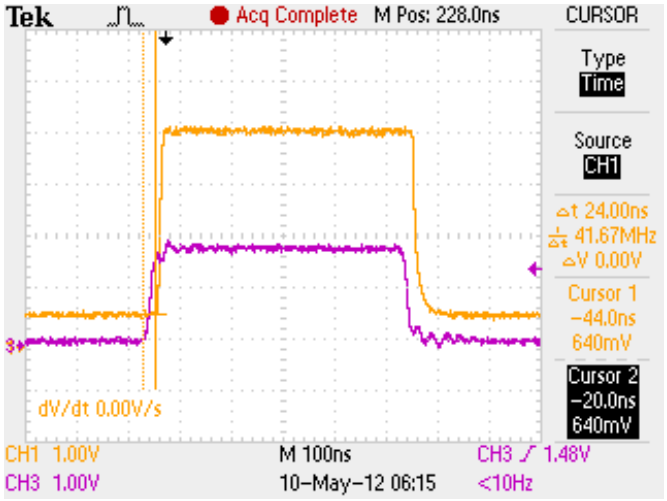


Figure 4.40 Waveforms for data points shown in Table 4.9, input (yellow), output (purple)

4.3.3 Digital Optocoupler Temperature Experimental Setup

The temperature experiments use the best of the previous digital schemes and scales their temperatures to 50 °C and 70 °C, at their best operating points, to find the benchmark for the digital optocouplers currently available. This final test will not have as many data points as the previous tests because each optocoupler will be biased at the optimized point so that the benchmark is found at these different temperatures. The test setup is the same hot plate setup as shown earlier and the input voltage does not change for each respective topology since linearity is not an aspect of these optocouplers.

The temperature experiment for the HCPL4505, ACPL071L and the HCPL7723 are repeated at 25 °C, 50 °C, and 70 °C. The results are shown in Table 4.10 through Table 4.12.

Table 4.10 HCPL4505 Temperature Results

R_{LED} (Ω)	270			390		
Temp (°C)	**25**	**50**	**70**	**25**	**50**	**70**
V_{in} (V)	10	10	10	10	10	10
V_{out} (V)	1.2	1.2	1.8	1.6	1.8	2.2
I_{LED} (A)	29.6E-3	30.4E-3	28.1E-3	21.5E-3	21.5E-3	22.1E-3
I_{src} (A)	4.7E-3	5.1E-3	5.1E-3	4.4E-3	4.6E-3	5.1E-3
P_{out} (W)	47.3E-3	50.9E-3	50.9E-3	43.6E-3	46.4E-3	50.9E-3
t_{prop} (s)	120.0E-9	80.0E-9	120.0E-9	160.0E-9	160.0E-9	160.0E-9
t_{rise} (s)	240.0E-9	360.0E-9	360.0E-9	400.0E-9	440.0E-9	480.0E-9
t_{fall} (s)	640.0E-9	920.0E-9	1.0E-6	840.0E-9	880.0E-9	1.0E-6

As the temperature is increased the rise time increases by 50% and the fall time increases by about 50% as well when the LED is biased at 30 mA. When the biasing is decreases to 20 mA the rise and fall times only increase by 20%. The low-logic output voltage also increases with temperature to a maximum of 2.2 V due to the increased BJT saturation voltage.

Table 4.11 ACPL-071L Temperature Results

R_{LED} (Ω)	110		
Temp (°C)	**25**	**50**	**70**
V_{in} (V)	4	4	4
V_{out} (V)	0.32	0.32	0.4
I_{LED} (A)	2.4	2.6	2.4
I_{src} (A)	0.003	0.003	0.003
t_{prop} (ns)	28	28	28
t_{rise} (ns)	8	8	12
t_{fall} (ns)	8	8	12

Table 4.12 HCPL7723 Temperature Results

Temp (°C)	25	50
Vin (V)	2	2
Vout (V)	4.08	4.08
Isrc1,avg (A)	0.006	0.006
Isrc2,avg (A)	0.013	0.14
t_{prop} (ns)	24	24
t_{rise} (ns)	20	16
t_{fall} (ns)	44	52

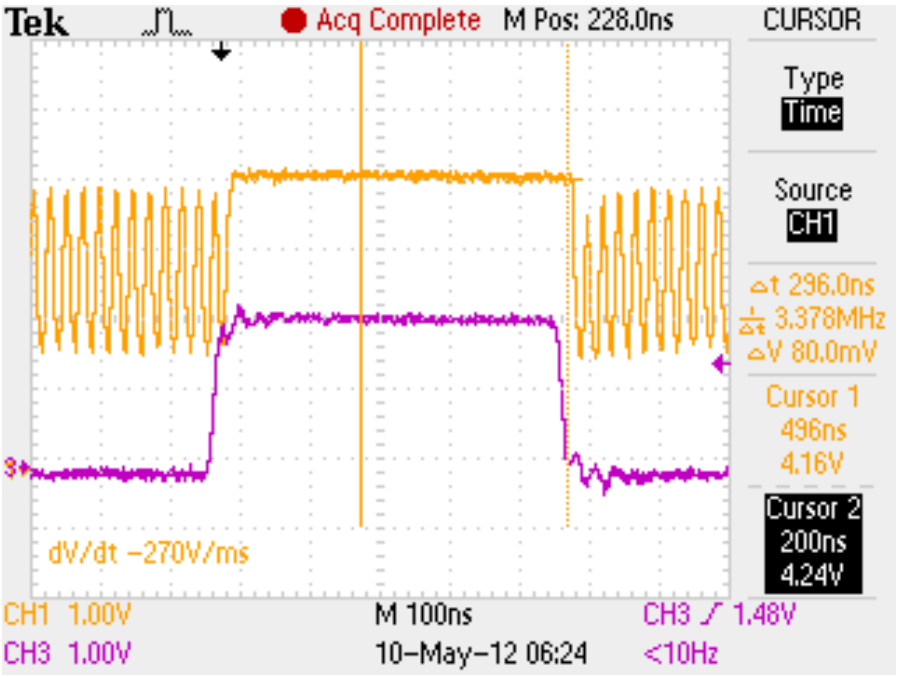


Figure 4.41 Oscillations in HCPL7723 at 70°C, input (yellow), output (purple)

The ACPL071L was stable across the temperatures except for the rise and fall times which began to increase at 70 °C by 100%. The final value was still only 12 ns which is two orders of magnitude below the BJT topology of the HCPL4505. The HCPL7723 was unstable with temperatures over 50 °C as seen in Figure 4.41. This oscillation was present when the optocoupler had no input applied at 70 °C. Nothing was changed between the low temperature experiments and the 70 °C testing of this circuit. A filter

capacitor of 10 nF was applied and the experiment was repeated at all temperatures and the oscillations were still present at 70 °C.

Now that the optocoupler topologies are well understood, because of the experiments in this chapter, selections will be made in the next chapter of the correct topology for the Buck converter. Finally, in the Conclusions Chapter, the benchmark for the analog and digital topologies will be discussed and presented.

5 IMPLEMENTATION OF OPTOCOUPLERS IN CLOSED-LOOP BUCK CONVERTER

Now that the gate driver that controls the main switch and the optocoupler schemes to transmit information between the actual Buck converter and its control circuitry have been defined, the closed-loop optically controlled Buck converter can be designed and implemented. The Buck converter's operation, and reason for choosing it as the application context to demonstrate the optocoupler's qualities, is generally discussed in the Background section. Now the goal is to design a working, closed-loop, current-mode optically-controlled Buck converter. This is accomplished in steps; the first is to present the final goal. That is, to have a Buck converter with a 100 V nominal input and an output of 5 A and 50 V (representing a 250 W load). This is the first and most important design choice. It is the operating point of the Buck converter that ultimately determines all the other selections, excluding the operating frequency. The switching frequency is chosen below but will just be a starting point because the final experiment to determine the impact of the optocouplers on the Buck converter system will increase the switching frequency until the circuit cannot operate any further.

The reason for choosing a 100 V input and a 250 W load is due to multiple reasons. This value is centered on the maximum voltage and power ratings of the different dc sources that are available in the lab, more specifically the input dc supply and floating dc supply. There are facilities that can implement up to 750 kW loads with a range of input dc levels. If that is possible then why choose the 100 V, 250 W design? Why not increase the input voltage to that of the withstanding voltage of the optocouplers at 1 kV? Firstly, the floating supplies can only float to 250 Vdc, so that is the maximum input voltage. Also the withstanding voltages of the optocouplers are very well determined and future optocoupler technologies will also have well determined withstanding voltages because the withstanding voltage is determined by the material properties and not the dynamics of the circuit. Also the design of a 1 kV system would be greatly complicated because the SiC MOSFET switch is only safe switching a dc link, or

input voltage of 600 to 800 V to stay well below its 1.2 kV blocking voltage rating due to the inevitable transients that occur. What truly needs to be tested is not the power of a Buck converter (that can be scaled relatively easily), nor the voltage isolation of the optocouplers (determined already), but a test that determines a benchmark for the speed at which the optocouplers will allow the Buck converter to operate correctly. Frequency is practically independent of power between 100 V and 1 kV so there is no need to complicate the design to determine the impact of the optocouplers.

This design will be presented in two steps. First, the procedures, reasons, and design equations for the various circuits and their components and IC's will be presented. Secondly, these procedures will be followed and design equations used to select the final circuitry and specific component values needed for this design. Finally, after the design is complete the procedures to implement the full Buck converter system on a PCB and the experimental procedures and results are presented.

One note before the design is presented, simulation results will be presented with the appropriate circuit topologies presented in the design and a final full system simulation will be presented to verify the overall design. Circuits that will not be simulated are circuits that are too simple to require simulation to verify their operation, or the optocoupler topologies chosen. The optocouplers are not simulated for two reasons. First, the optocoupler topologies have been extensively verified in the experiments presented in the previous chapter. Second, the optocoupler is not dynamically modeled in any simulation environment. Simple models based on current controlled current sources can be implemented to verify static effects but, as stated in the previous chapter, this is not useful for this design because the optocouplers are used in a dynamic state to transmit constantly changing signals. A static model will not properly validate this functionality. But the purpose of the previous chapter was to not only determine the benchmark for these topologies, but to understand their implementation of the

optocouplers into the Buck converter. With the results of the previous chapter as a guide the correct design decisions for selecting the right topology and the component values can be made.

5.1 Design Method and Implementation

As stated above, another important choice in the initial operating point of the design is the switching frequency. The integrated circuit chosen to close the loop and generate a PWM signal using current-mode control (comparing the inductor current and output voltage) has a minimum switching frequency of 80 kHz, so the initial frequency is set to 85 kHz to operate the PWM within a safe margin [24]. This is still relatively fast since some available optocouplers were shown to have a propagation delay between the order of microseconds and hundreds of nanoseconds depending on the biasing point. The on-time at a 50% duty cycle is only about 6 μs which shows that the optocoupler propagation delay is a very important characteristic to minimize. This propagation delay determines how long it takes for the system variables of the Buck converter to be transmitted to the controller. The benchmark frequency will be limited to the minimum propagation delay that can be achieved by the optocouplers. For example, if the propagation delay of the optocoupler is 500 ns then any on-time for the Buck converter that is less than 1 μs will cause the system variables to distort the PWM generation because the PWM will be comparing old current and voltage data to calculate the new duty cycle. This will introduce large instabilities into the circuit. The other impact the optocouplers will have will be on the accuracy of the system variables that they transmit to the control circuitry. With the linearity described in the Optocoupler Characterization Experiment Chapter, the data transmitted can be skewed by the non-linearities of the optocoupler transmission scheme. This will also cause incorrect duty cycles to be calculated and therefore cause instabilities in the Buck converter system.

Now that a conceptual understanding of the impact of the optocouplers on the converter system, the design procedures can be presented for the Buck converter system shown in Figure 5.1.

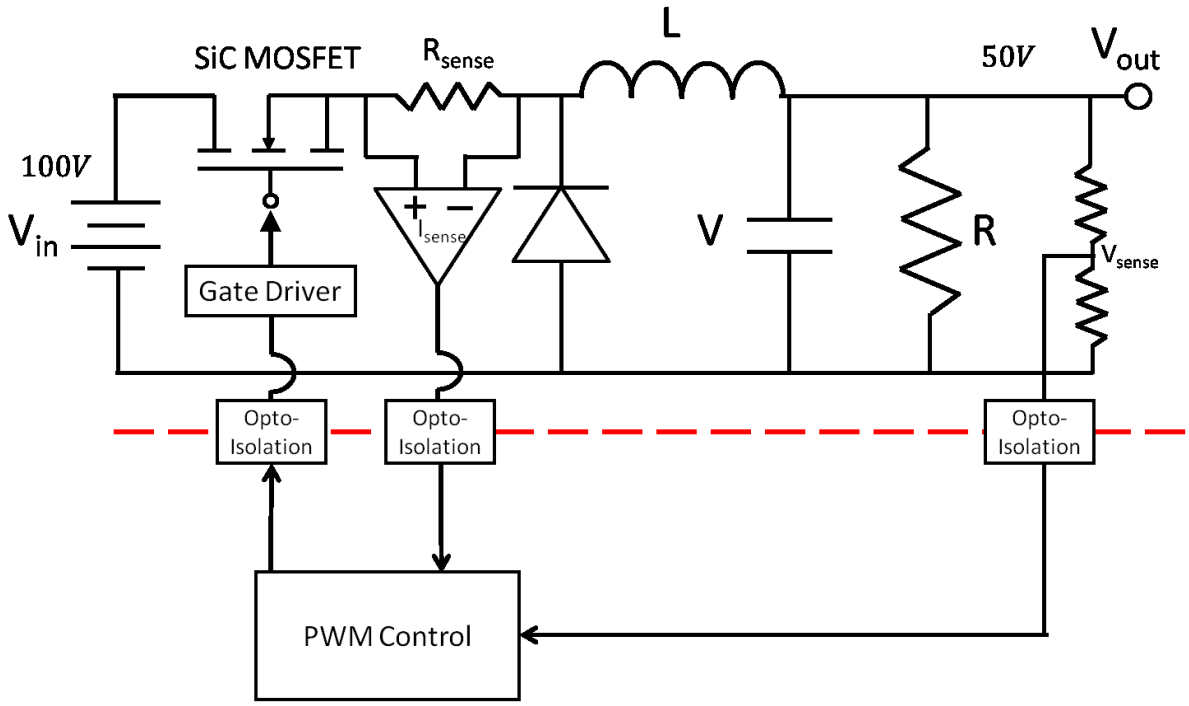


Figure 5.1 Block diagram of Buck converter system

The first part of the design method is to determine the Buck converter inductor and capacitor component values at the operating point that has been selected (100 V input, 250 W load at 50 V, and 85 kHz switching) and at steady-state (50% duty cycle with continuous current). The next step is to determine the steady-state values and waveforms of the inductor current and output voltage so that the sensing network for those system variables can be better defined. The sensing networks are determined next and then the transmission of these analog values through the isolation barrier with the correct optocoupler topology and optocoupler is described and the correct topology selected. The gain of the sensing networks needs to be set so that the PWM IC will generate a 50% duty cycle (allowing 50 V at this steady-state operating point) when the selected PWM IC compares the current and voltage. The final step is determining the digital transmission optocoupler topology to be used to send this PWM information to the gate driver to implement the calculated duty cycle by turning on and off the MOSFET with the correct timing.

5.1.1 Open-Loop Buck Converter

The switch selection is the first step in determining the open-loop Buck converter. The switching transistor was chosen before the Buck converter was chosen as the application context to determine the impact of the optocouplers. The SiC MOSFET became commercially available with a rated blocking voltage of 1.2 kV and drain current of 20 A, and this is the switch that the gate driver is designed around [18]. The diode will also be a SiC device, a SiC Schottky diode rated at 1.2 kV and 20 A [25]. Also, since wide bandgap GaN optocouplers could be prototyped in this application context in future research, it is useful to have a fully wide bandgap system to take advantage of the wider temperature ranges these devices can handle compared to silicon and the other current optocoupler technologies.

The output filter is the combination of an inductor and capacitor. Since the steady-state operating point is known, these values are chosen based on the desired voltage, current ripple, and mode of operation. If the inductance chosen is lower than the critical inductance then the Buck converter will operate in discontinuous mode. The main factor for theoretical design is limiting the voltage and current ripple. A practical design also needs to consider the rated current and voltages as well as the equivalent series resistances (ESR). The two design equations for the current and voltage ripple are shown below.

$$\text{current ripple: } \Delta I = \frac{DV_{in}(1\text{-}D)}{f_s L} \quad \textbf{(5-1)}$$

$$\text{voltage ripple: } \Delta v_c = \frac{V_{in}D(1\text{-}D)}{8f_s^2 LC} \quad \textbf{(5-2)}$$

Table 5.1 Available Inductor Values at Specific Current Ratings [26]

Current rating (A)	L (µH)
20	33
15	68
10	150
6.7	390

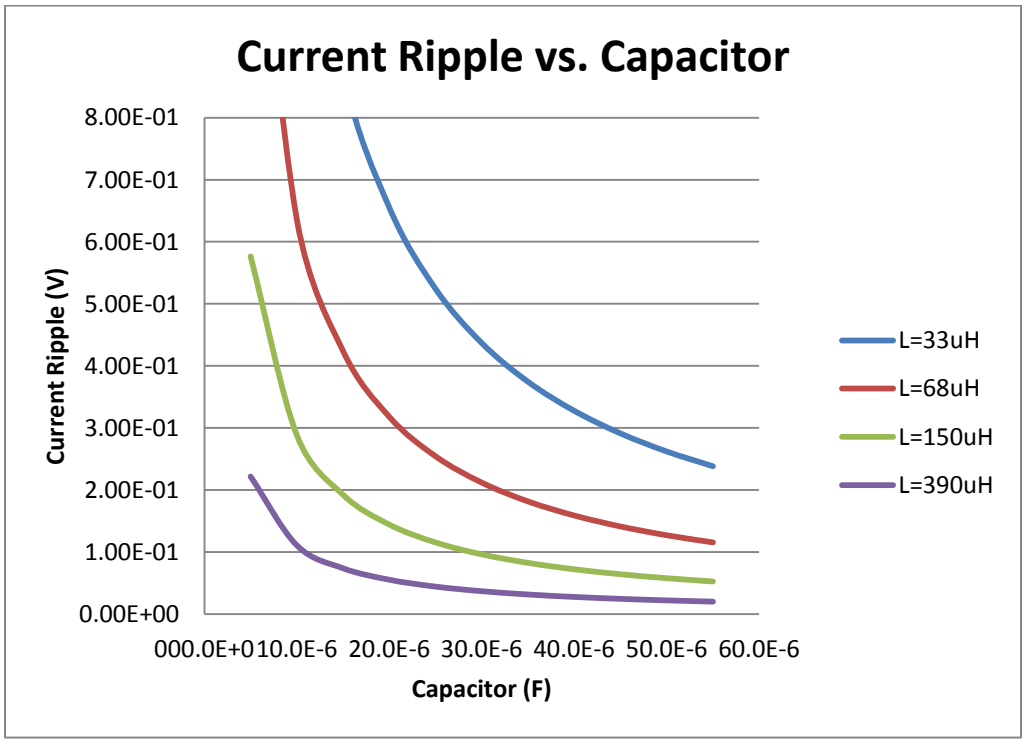


Figure 5.2 Current ripple vs. capacitor values for the different inductors available

Since the load current will be 5 A and the voltage will be 50 V, a desirable current ripple would be less than 100 mA (2%) and a voltage ripple less than 1 V (2%). Figure 5.2 shows a graph of the L and C values that correspond to a range of ripple currents.

Table 5.1 shows the rated amperage of available inductances. The correct choice is an inductance value of 390 µH because there will be 5 A flowing. The only available inductors range from 390 µH and smaller; and the smaller the inductance the larger the current and voltage ripple as seen in

Figure 5.2. With the inductor selected a capacitor value of 10 µF is chosen which is equivalent to a 100 mV voltage ripple and 750 mA current ripple. The current ripple is larger than desired but as seen in

Table 5.1 a larger inductor cannot be used, and a larger capacitance would increase the footprint of the final PCB. An electrolytic capacitor is used because of its size at a 100 V rating. Figure 5.3 shows the simulation validating the calculations. The current ripple is seen to be from 4.76 A to 5.51 A, which corresponds to the 750 mA that was calculated. The voltage ripple cannot be seen because at 50 V the scale is too large to see 100 mV ripple. Note that as the frequency is increased the output filter will not be changed, so the ripples will decrease.

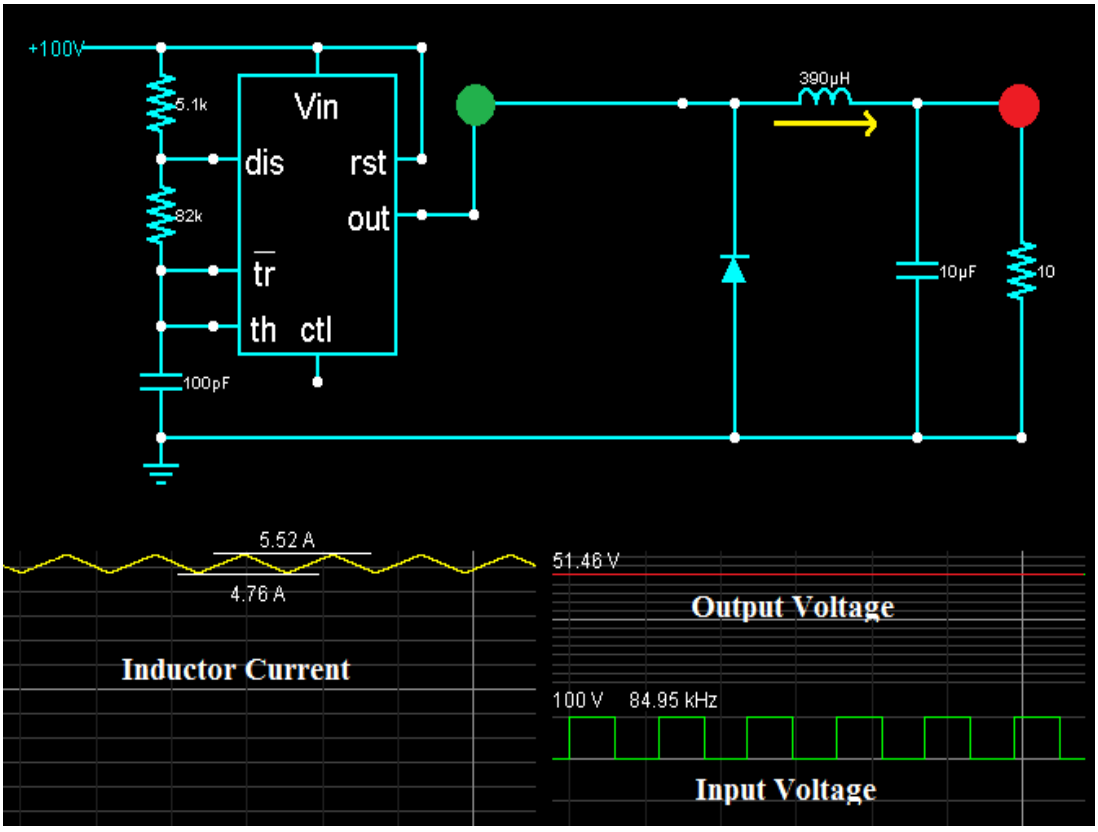


Figure 5.3 Open-loop Buck converter simulation verification, inductor current (yellow), output voltage (red), input voltage (green)

Now that the open-loop Buck converter components have been chosen, the sensing networks implemented in the system can be discussed and designed. For this design to be current-mode control the inductor current and output voltage need to be sensed, scaled, and sent to the controller [15]. For the design to be optically isolated these sensed system variables need to be transmitted through optocouplers from the Buck converter side to the controller side of the circuit. The first step in the design will be to break apart the current sensing network, design it, and then focus on the output voltage sensing network.

5.1.2 Current Sensing Inner Feedback Loop

The current feedback design first determines how to sense the current, then to transmit the signal through the isolation barrier and, finally add slope compensation. There are multiple current feedback sensing schemes, and for current-mode control it depends on what type of current measurement is needed. A simple method is to measure the current in the inductor when the switch is off. This configuration is shown in Figure 5.4 and is called valley current-mode control [27].

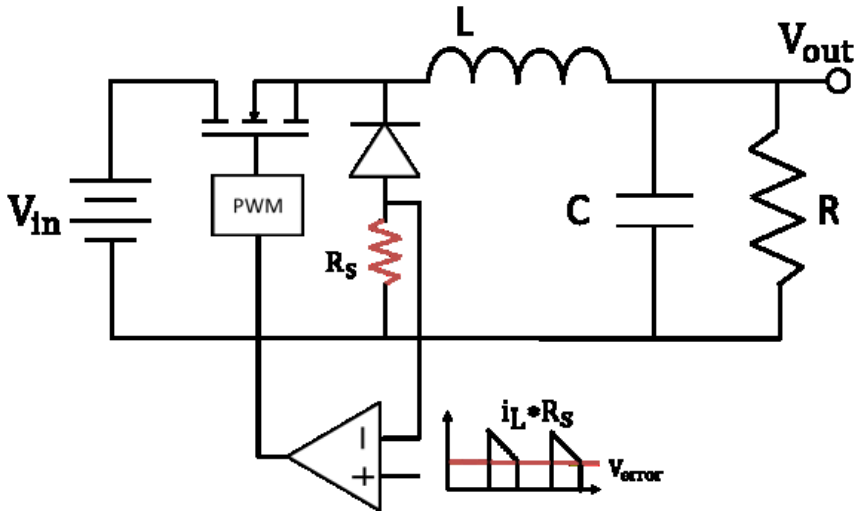


Figure 5.4 Valley current mode (sense resistor placement emphasized) [27]

A small sense resistor is placed between the diode and ground and the sensing network can be referenced to the Buck converter's ground, and a specific current sensing differential amplifier measures the small voltage difference between the two terminals of the resistor. This is not desired for this design because this type of sensing network could be developed without optocouplers since the reference of the sensing circuitry would not be floating at a high voltage. This method controls the on-event of the high-side MOSFET by the sending of an on-control signal to the gate driver when the sensed current signal crosses the error voltage signal as shown in Figure 5.4. This sensing method only captures the downward slope of the current, it cannot protect against overcurrent because of too heavy of a load being driven [27].

Peak current-mode control is chosen for the two reasons valley current-mode control could not be used. It requires high-side current sensing with a floating ground reference and it has inherent overcurrent protection. The same type of sensing resistor in the valley current-mode is placed between the source of the MOSFET and the inductor as shown in Figure 5.5. This sensing method uses a current sense amplifier referenced to the source of the MOSFET to measure the voltage difference the output current will cause over the sense resistor. This method captures the upward current slope and controls the off-event of the MOSFET by sending an off control signal to the gate driver whenever the current intersects the error voltage [27].

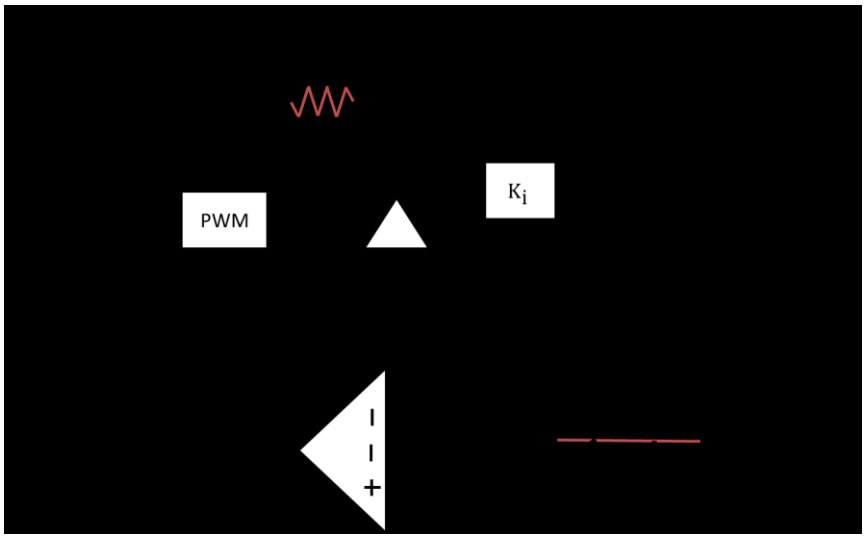


Figure 5.5 Peak current mode control (sense resistor placement emphasized) [27]

The addition of an optocoupler allows signals to be sensed and transmitted to the low voltage control circuitry even if the floating, high-side, reference of the sensed signal is much greater than the ground of the control circuitry[28]. This is defined as the isolation that the optocoupler can provide. For this design, the sensed signal is referenced to a signal that floats between the 100 V input voltage and 50 V output voltage. The control circuitry is at zero volts. If these two circuit grounds were directly connected the control circuitry would be destroyed. Now that an optocoupler is used the input voltage could be as high as the withstanding voltage of the optocoupler.

Now a current sensing network needs to be designed to measure the voltage drop across the sense resistor and send it to the analog transmission optocoupler topology to be sent to the controller circuitry through the isolation barrier. Two key things need to be kept in mind while designing the current sensing network, the gain of the sense network and the slope of the sensed signal. The slope information needs to be known to calculate the amount of slope compensation (as discussed in the background section) needed, and the gain will be factored in because it changes the original slope of the current signal.

5.1.3 High-Side Current Sensing Design and Analog Current Transmission Optocoupler Topology Selection

The actual method of obtaining and transmitting the current sensed signal to the control circuitry follows. Figure 5.6 shows the overall design for completeness, while each subsection's design and selection will be discussed individually [28]. The first step for sensing the peak current is sensing the current as an analogous voltage signal that is obtained from the sense resistor.

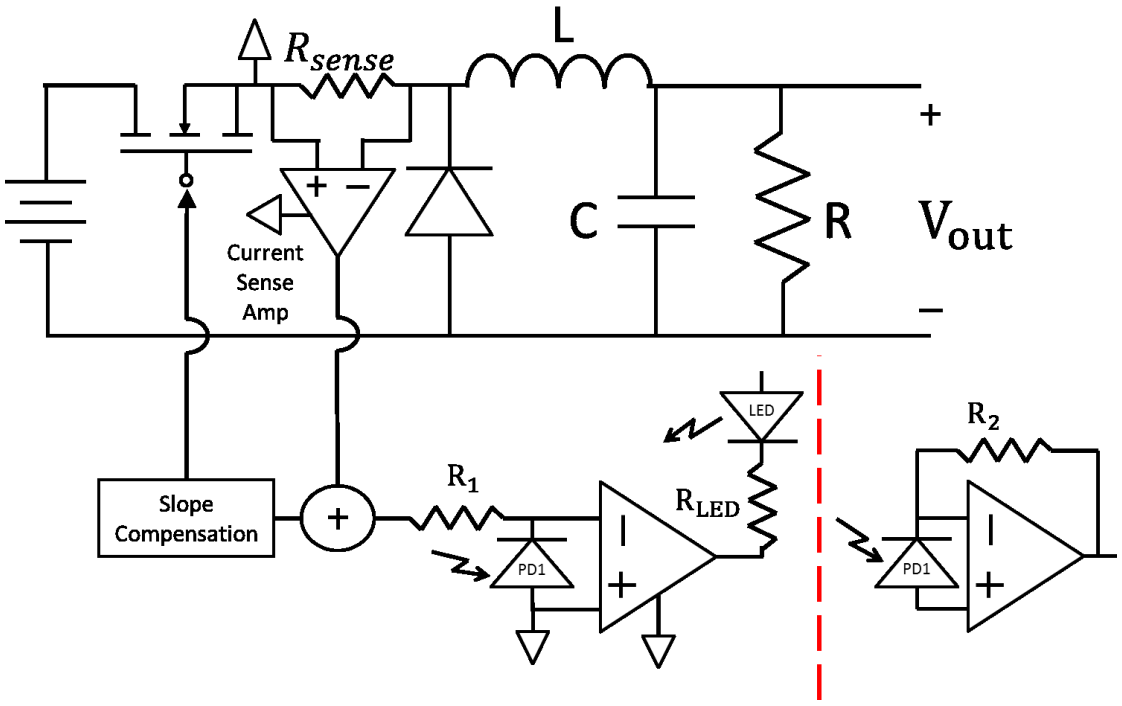


Figure 5.6 Current sense scheme implementing peak current mode scheme with analog transmission optocoupler [28]

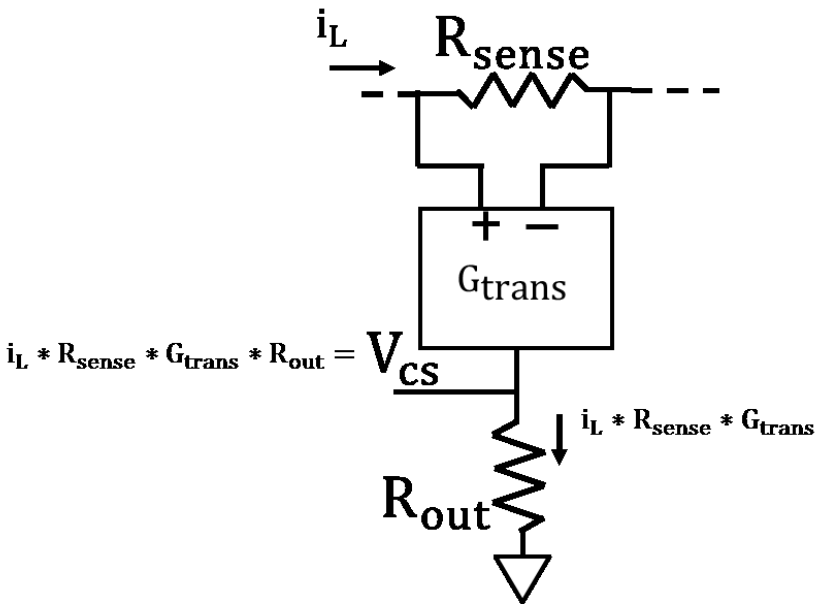


Figure 5.7 Simple block diagram of current sense amplifier [29]

The current sense amplifier block diagram is shown in more detail in Figure 5.7 [29]. It senses the voltage drop over the sense resistor and multiplies it by a transconductance gain parameter, G_{trans}, to produce a current through the output. The output is connected to the floating ground reference through a resistor (R_{out}) which converts the output current of the sense amplifier into a voltage again [28]. Keeping account of the key parameters, overall gain and slope, the gain from the current flowing through the sensed resistor to the voltage at the output of the current sense amp is shown below.

$$\frac{V_{cs}}{i_L} = G_{csamp} = R_{sense} * G_{trans} * R_{out} \quad \textbf{(5-3)}$$

$$\text{Slope: } S_n = \frac{G_{csamp} * (I_{L2} - I_{L1})}{t_{on}} \quad \textbf{(5-4)}$$

I_{L2} and I_{L1} are the minimum and maximum currents due to the current ripple around the 5 A steady state value. S_n is the slope of the current signal after the gain of the sensing network. This will be used in the next section to calculate the slope compensation requirements.

The next step is adding slope compensation to the sensed current signal, as discussed in the background chapter for current-mode control, to compensate for the sub-harmonic oscillations. There are numerous ways to generate a ramp signal to add to the current sense signals. Some methods use the oscillator in the PWM IC to generate a triangle wave with the correct slope and sum the current sense signal together with it. This method has been proven to load the oscillator pin enough to cause the oscillator frequency to shift [30]. Another inherent oscillator in the system is the gate driver output. Since this output drives a large amount of current a small amount (micro-amp range) can be used to charge a specifically sized capacitor to generate a ramp signal [31]. Another advantage to this is that this signal is on the high-side so it can be directly summed with the voltage output of the current sense amp since they are referenced to the same high-side floating ground. This solution is shown in Figure 5.8.

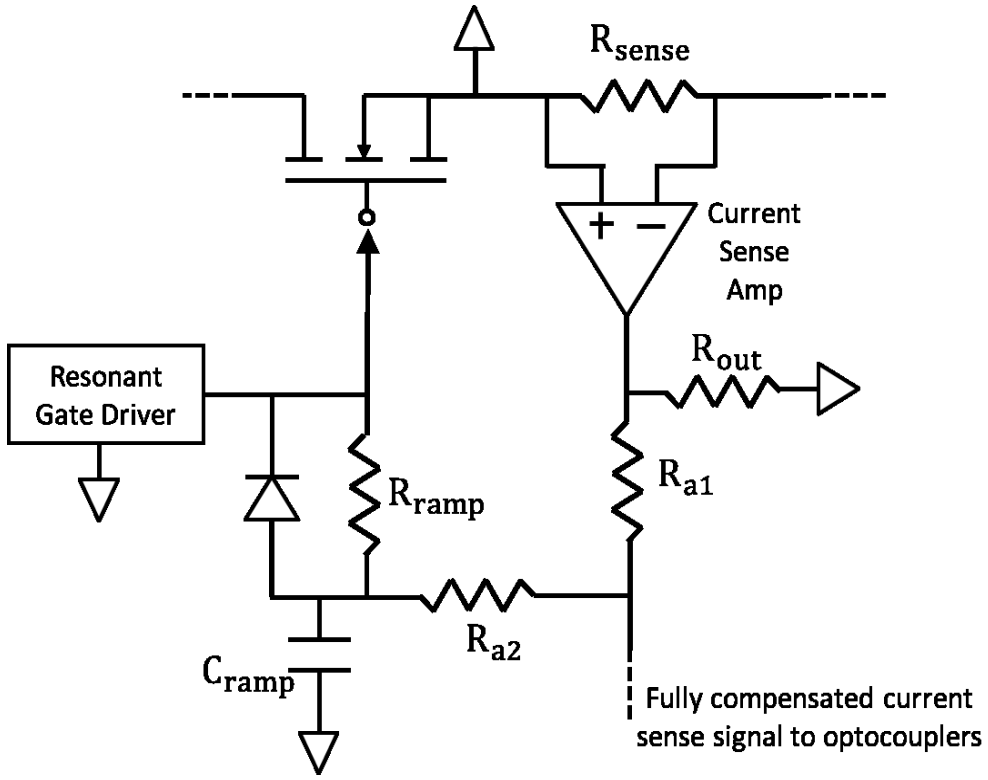


Figure 5.8 Adding ramp compensation on high-side of isolation barrier [31]

The gate signal output goes high turning on the MOSFET, and current flows through R_{ramp} which charges C_{ramp} to a specific voltage V_{ramp}. These two components are chosen for a desired slope and minimal loading of the gate driver. R_{a1} and R_{a2} form a voltage divider to resistively add the output of the current sense amplifier with the slope compensation generated by C_{ramp} (S_{ramp}). R_{a1} and R_{a2} are determined by the desired amount of slope (S_{comp}) needed to stabilize the current signal. This amount is determined by a value titled m_c, which represents how much slope compensation is supplied [31].

$$m_c=1+\frac{S_{comp}}{S_n} \quad \textbf{(5-5)}$$

With an m_c of one there is no external ramp supplied. The factor that determines the amount of external ramp to be added is the value of Q, the quality factor [31].

$$Q=\frac{1}{\pi\left(m_c*D'-0.5\right)} \;\; ; \;\; D'=(1-D) \quad \textbf{(5-6)}$$

When there is no external slope and the duty cycle is 50% (0.5) the Q will become infinite, representing the sub-harmonic oscillations of the current-mode controlled Buck converter [31], [32]. For a stable system, slope compensation corresponding to a value of m_c greater than one needs to be added to keep Q below one. This corresponds to the design equations for R_{ramp}, S_{ramp}, C_{ramp}, m_c, and S_{comp} [31].

$$\text{For minimal loading: } R_{ramp}=\frac{V_{gate,supply}}{I_{ramp}};50\ \mu A<I_{ramp}<200\ \mu A \quad \textbf{(5-7)}$$

$$C=I\frac{dt}{dv}=\frac{I_{ramp}*t_{on}}{V_{ramp}} \quad \textbf{(5-8)}$$

$$S_{ramp}=\frac{V_{ramp}}{t_{on}} \quad \textbf{(5-9)}$$

$$m_c = \left(\frac{1}{\pi} + 0.5\right)\left(\frac{1}{D'}\right) \quad \textbf{(5-10)}$$

$$S_{comp} = (m_c - 1)S_n; \text{ remember } S_n = \frac{G_{csamp} * (I_{L2} - I_{L1})}{t_{on}} \quad \textbf{(5-11)}$$

Once the desired amount of compensation slope is calculated, the values of R_{a1} and R_{a2} can be calculated to add the right amount of the slope from the ramp to the current sense information [31].

$$\text{division ratio, } d_r = \frac{S_{comp}}{S_{ramp}} = \frac{r_{a1}}{r_{a1} + r_{a2}} \quad \textbf{(5-12)}$$

Something to note is that not only is the ratio of R_{a1} and R_{a2} important, but their respective size is too, because if they are two small they will draw more current than the ramp circuit or current sense amplifier will be able to supply. Also, if they are too large they will not be able to supply the correct amount of current for the next stage, the analog transmission optocoupler topology. Figure 5.9 shows the behavioral model of the current sensing circuit that is simulated to validate the design approach chosen. The simulation applies a signal to the current sensing resistor that emulates a 5A current signal. The result shows that the slope of the output signal can be correctly compensated with the correct values of the addition circuit chosen.

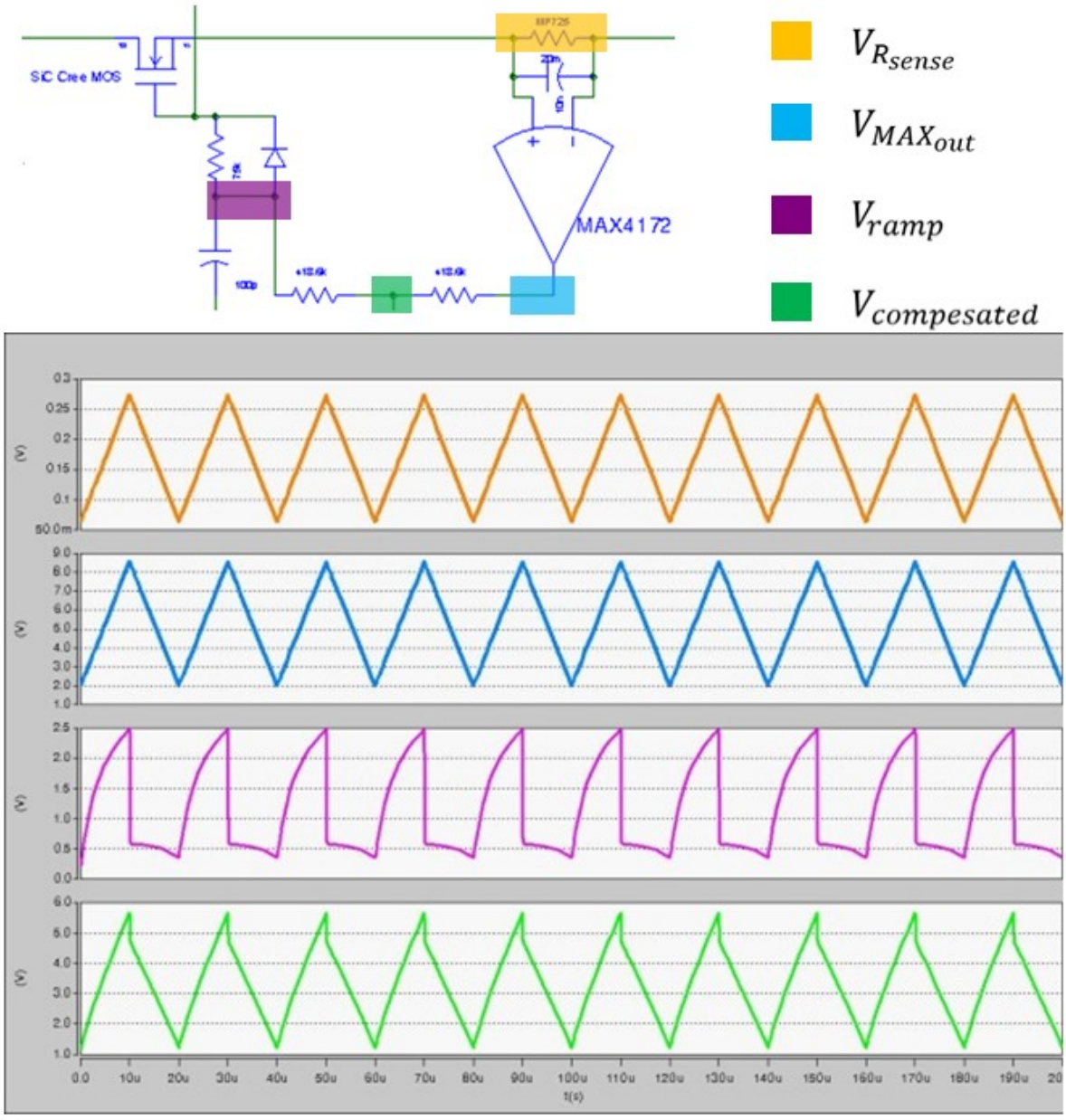


Figure 5.9 Simulation results of the current sensing network; input (yellow), output of differential sensing amplifier (blue), slope generation (purple) compensated signal consisting of output of sense amp added with compensation slope (green)

The fully compensated current signal on the high voltage isolated side of the circuit now needs to be transmitted to the low voltage control circuitry with the optocoupler. Choosing which analog

topology and which optocoupler to use depends on which topology and optocoupler are the fastest and most accurate for transmitting the sensed current signal, which is determined in the Optocoupler Characterization Experiments Chapter to be the topology with a feedback servo-diode that removes the non-linear CTR parameter from the transfer function. This optocoupler topology is chosen because it can linearly track the input voltage (analogous to the sensed current) applied to the photodiode input. This means that small changes of light intensity radiating from the LED due to the sinusoidal sensed signals must be amplified by the photodiode and output scheme linearly and without added propagation delay. Linearly transmitting the signal with a very small propagation delay between the input and the output are the two restricting parameters that helped determine the optocoupler topology that will be used. Although the open-loop analog transmission topology had a smaller propagation delay by 100 ns, this small value would increase because the output voltage of the current sensing network would require a large output resistance. This was seen to increase the propagation delay by as much as 1 μs in the Optocoupler Experimental Chapter. This effect disqualifies the open-loop topology. How the propagation delay will affect the Buck converter and the maximum switching frequency has already been discussed and the final results will be presented when the full Buck converter system has been designed and implemented. With a final decision made for the current sensing optocoupler scheme, the design equations for transmission are described below [12], [28].

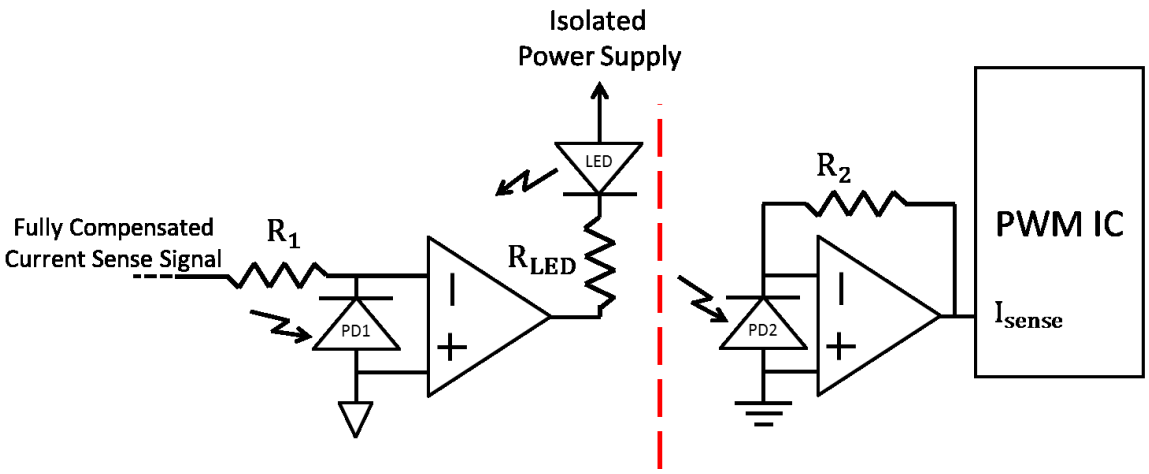


Figure 5.10 Analog transmission optocoupler scheme for current sensing transmission to control IC [12]

The topology shown in Figure 5.10 is discussed in the background section and the design equation is just the transfer function presented in Eq. (2-14) and rewritten in Eq. (5-13). The design decision for the value of R_{LED} is a little more complex because it does not determine any current in the circuit. It will affect the power consumption and also if it is too large the output voltage of the first op amp will not be able to swing far enough and will not provide the correct LED biasing voltage, as shown in Chapter 4.

$$G_{opto} = \frac{V_{out}}{V_{in}} = \frac{R_2}{R1} \qquad \textbf{(5-13)}$$

It is also imperative to bias the LED, PD1, and PD2 correctly. This will be done for the specific parameters of the optocoupler selected. The final value selections for the current sensing network can now be discussed. The current sense amplifier is chosen to be the MAX4172 which allows all the variables in Eq. (5-3) for G_{csamp} to be determined [29]. It can handle a maximum input voltage of 175 mV. So R_{sense} is chosen to be 20 mΩ so that at 5 A the voltage drop will be 100 mV. This leaves the selection of R_{out}. The gain of this transconductance amplifier is 10 $\frac{mA}{V}$, so at 100 mV the current through

the sense resistor is 5 A and the output current of the sense amplifier is 1 mA. The selection of the value of R_{out} is a very big decision. If the optocoupler's transmission gain is set to one, then the value of R_{out} will set the voltage that is seen by the comparator. This is where scaling the sensed current plays a crucial role. For this design the switch needs to be turned off at 5 A (the maximum allowed current), the value of the analogous voltage of the sensed current that will cause the PWM to generate an off-command to the gate driver at this current level needs to be understood. Once this is known the parameters can be chosen to produce this output when 5 A is present on the input to the sensing network. This voltage value is determined by the PWM IC that is chosen; for this design a HV9123 will be optimal because it has simple implementation and allows for a fully analog control system which simplifies the design of the control circuitry interface to the optocouplers [24]. This PWM IC will turn off the switch whenever 1.3 V is seen at the current sense pin. Finally, R_{out} is determined to be 1.3 kΩ so that at 5 A of current flowing through R_{sense}, 1.3 V will be at the output of the current sense amplifier. Now G_{csamp} can be found.

$$G_{csamp}=R_{sense}*G_{trans}*R_{out}=20m*10m*1.3k=0.26 \quad \textbf{(5-14)}$$

So the slope of the inductor reflected to the output of the amplifier can now be calculated along with the rest of the current sensing network. The values of I_{ramp} and V_{ramp} are chosen to be 100 µA and 1.3 V, respectively, and R_{a1} is chosen to be 10 kΩ.

$$S_n=\frac{G_{csamp}*(I_{L2}-I_{L1})}{t_{on}}=\frac{0.26*(5-4.75)}{5.88\mu}=11\ \frac{mV}{\mu s} \quad \textbf{(5-15)}$$

$$m_c=\left(\frac{1}{\pi}+0.5\right)\left(\frac{1}{D'}\right)=\left(\frac{1}{\pi}+0.5\right)\left(\frac{1}{0.5}\right)=1.64 \quad \textbf{(5-16)}$$

$$S_{comp}=(m_c-1)S_n=(1.64-1)*11\ \frac{mV}{\mu s}=7\ \frac{mV}{\mu s} \quad \textbf{(5-17)}$$

$$R_{ramp}=\frac{V_{ramp}}{I_{ramp}}=\frac{1.3}{100\mu}=150\ k\Omega \quad \textbf{(5-18)}$$

$$C=\frac{I_{ramp}*t_{on}}{V_{ramp}}=\frac{100\mu*5.88\mu}{1.3}=440\text{ pF} \quad \textbf{(5-19)}$$

$$S_{ramp}=\frac{V_{ramp}}{t_{on}}=\frac{1.3}{5.88\mu}=227\frac{mV}{\mu s} \quad \textbf{(5-20)}$$

$$d_r=\frac{S_{comp}}{S_{ramp}}=0.466 \quad \textbf{(5-21)}$$

$$r_{a2}=\frac{r_{a1}-r_{a1}d_r}{d_r}=11.5k\Omega \quad \textbf{(5-22)}$$

Now the input to the analog transmission optocoupler is known to be 1.3 V when the current through the sense resistor is 5 A. We want this current to be sent across the isolation barrier with unity gain. The optocoupler chosen in the Optocoupler Experimental Chapter is the HCNR201 [12]. It has a nominal CTR of 0.2%. The nominal current through the LED is about 10 mA, but for this design the operating point will be set around 8.5 mA because of the increase performance seen in the Experimental Chapter without increasing the power consumption too much. This means the photodiode current will need to be about 40 µA when the input is at 1.3 V. This operating points sets R_1 and R_2 [12].

$$R_1=R_2=\frac{V_{in}}{I_{pd1}}=\frac{1.3}{40\mu}=32.5\text{ k}\Omega \quad \textbf{(5-23)}$$

Now that the analogous voltage of the sensed current is on the control side of the system at the current sense pin of the PWM IC, the corresponding sensed output voltage must be found and the voltage sense network must be designed.

5.1.4 Voltage Sensing Outer Feedback Loop

The voltage pin of the PWM IC needs to be at 4 V when the output voltage is at its nominal value of 50 V in order to be compared correctly with the sensed current signal and produce the nominal 50% duty cycle [24]. This criterion determines that the overall gain of the voltage sensing system needs to be 0.08. The voltage on the output is sensed with a simple voltage divider, shown in the design scheme for

the voltage sensing network in Figure 5.11, using two resistors chosen to output a voltage equal to the voltage required by the PWM IC referenced above which will be called V_{th} in the design equations.

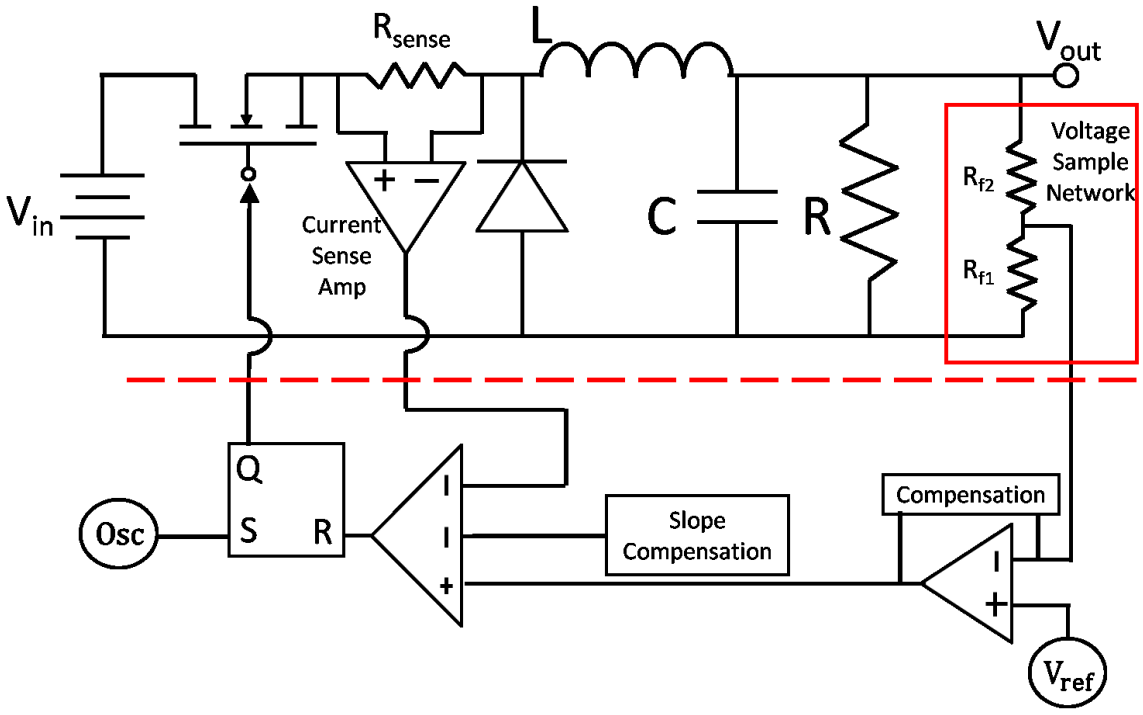


Figure 5.11 Full design scheme for voltage sense network and placement within overall current-mode control scheme

If the load changes then the output voltage will start to change. This will cause an error voltage to change (positive for smaller output voltages and negative for larger output voltages) which in turn changes the duty cycle (compensating the amount of energy transferred from the inductor to the output) until the error voltage is zero again and V_{th} is back to its nominal value of 4 V [14]. The voltage divider design equation can now be determined.

$$\frac{R_{f1}}{R_{f2}+R_{f1}}=0.08 \qquad \textbf{(5-24)}$$

The output of this voltage divider is the input to the analog transmission topology. Obviously the feedback analog topology presented in Chapter 4 will be the best design because of its accuracy and speed. This is the first assumption, but would be an incorrect design decision for a couple reasons. First, the voltage signal does not change as much as the current signal; it is very well defined and stays within a small range of voltage levels because the voltage divider causes a very small fraction of the output voltage to be applied to the input of the transmission circuitry. Also, the current sensing feedback topology needs a dedicated isolated supply for the input stage. This is okay for the current transmission because one is already available due to the need of the high-side gate driver. The voltage sensing network cannot use this isolated supply. If the same supply is used for the current sensing signal the voltage sense scheme will be referenced to a floating ground (specifically, the source node of the switch), but the voltage sampling network is referenced to the Buck converter ground. If the current sense network configuration is used the LED will be biased completely incorrectly, more easily seen in Figure 5.12.

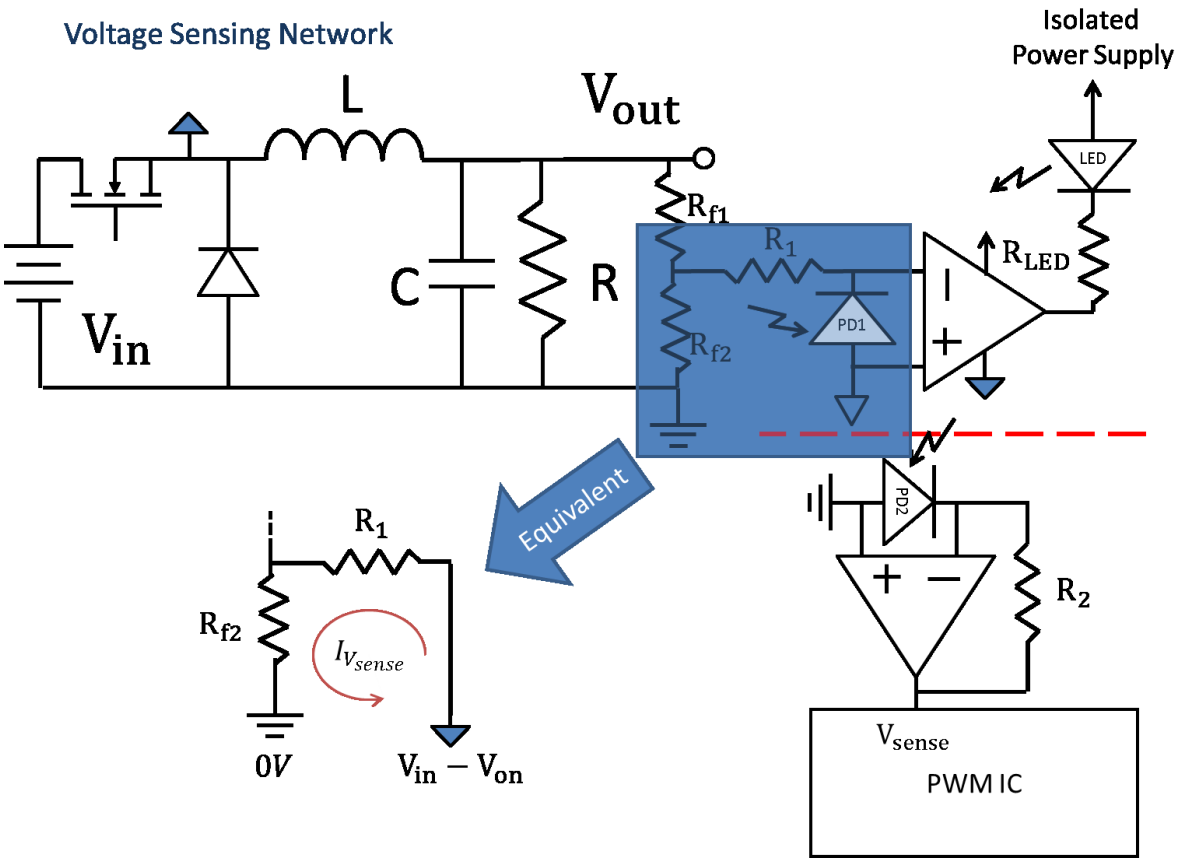


Figure 5.12 Incorrect grounding of voltage sensing network optocoupler

Because the voltage sensing circuit will mostly be a dc value that only fluctuates during transients, an open-loop analog transmission topology can be used by operating in the plateau region described in the experimental results of this topology in Chapter 4. This is a benefit so that another isolated voltage supply does not have to be implemented. Another thing to note is that the different optocouplers are used between the two sensing networks will not have a matched propagation delay (reference the propagation delay results from the two topologies). There will be mismatch of propagation delays because of processing differences and topology selection. With different propagation delays the information at the PWM IC would not accurately represent the actual circuit conditions. . Two facts allow for this mismatch to be present in the system without impeding the

operation of the Buck converter. The first is that the output voltage does not change unless the load changes, and other than the initial transient the time scale is orders of magnitude slower than the current signal cycle to cycle change. This difference in time scale is much larger than a 100 to 200 ns mismatch in propagation delay. The second fact is better explained qualitatively Figure 5.13. During any transient change that takes place on the same time scale as the current signal the instability in the duty cycle introduced by the mismatch will be quickly compensated over a short amount of cycles. One final note, it is still possible for the mismatch to affect the operation. If the mismatch does cause a problem in the operation of the Buck converter then it will become another aspect of the optocouplers impact on the full system.

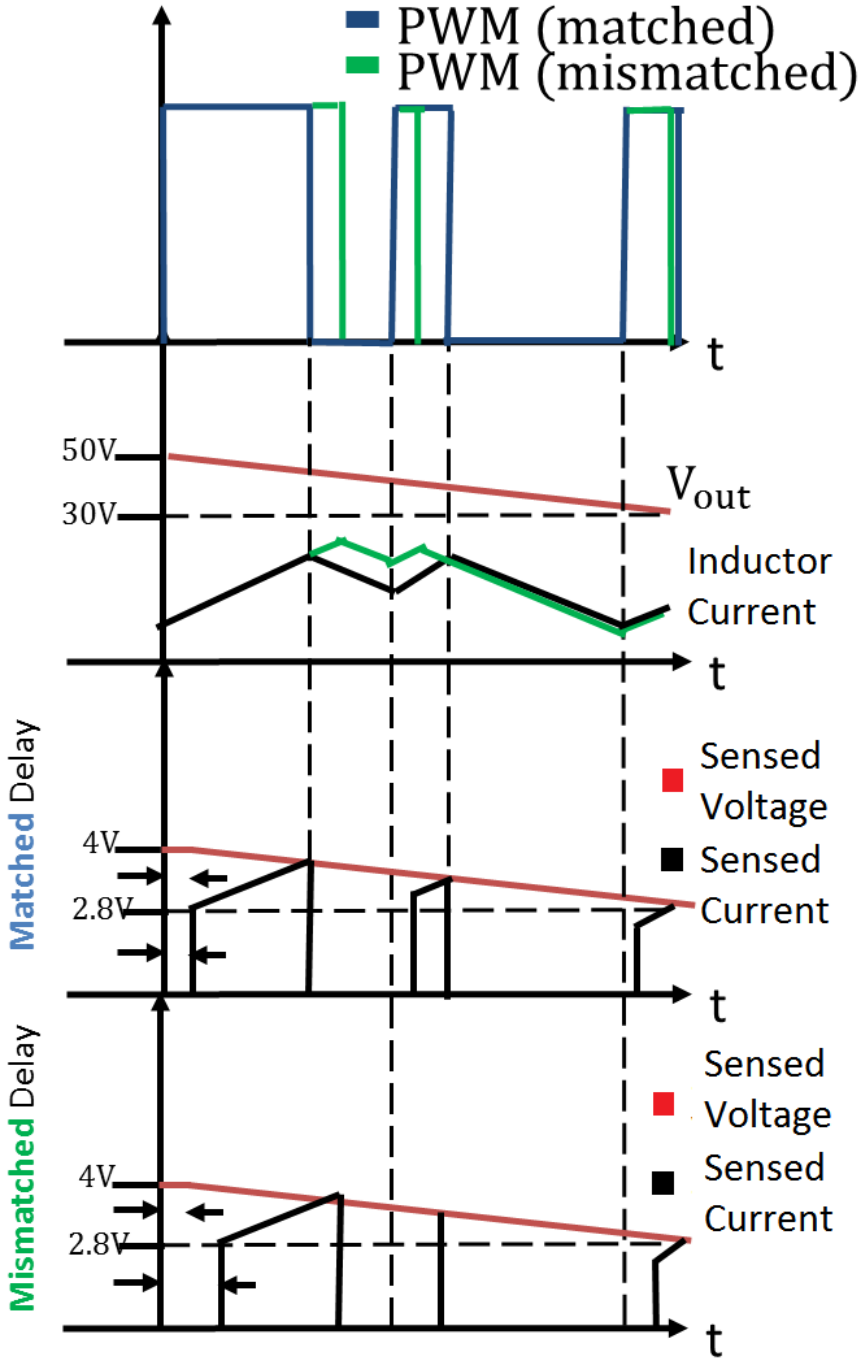


Figure 5.13 Graphical representation of mismatched delay causing different results over multiple cycles (assumed transient causing steady decrease in output voltage)

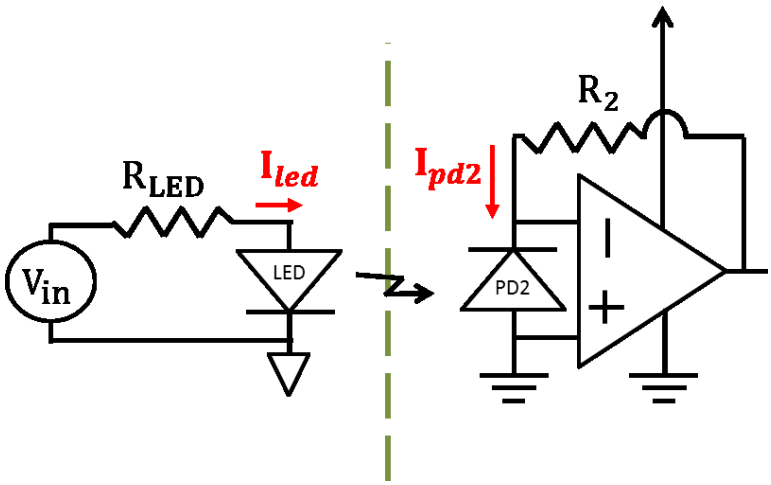


Figure 5.14 Open-loop analog transmission used so the side referenenced to power gound does not need isolated supply

Figure 5.14 shows the open-loop analog transmission topology to be used with the HCNR201. The new steady state design equations will now change for the correct topology, shown in Figure 5.15.

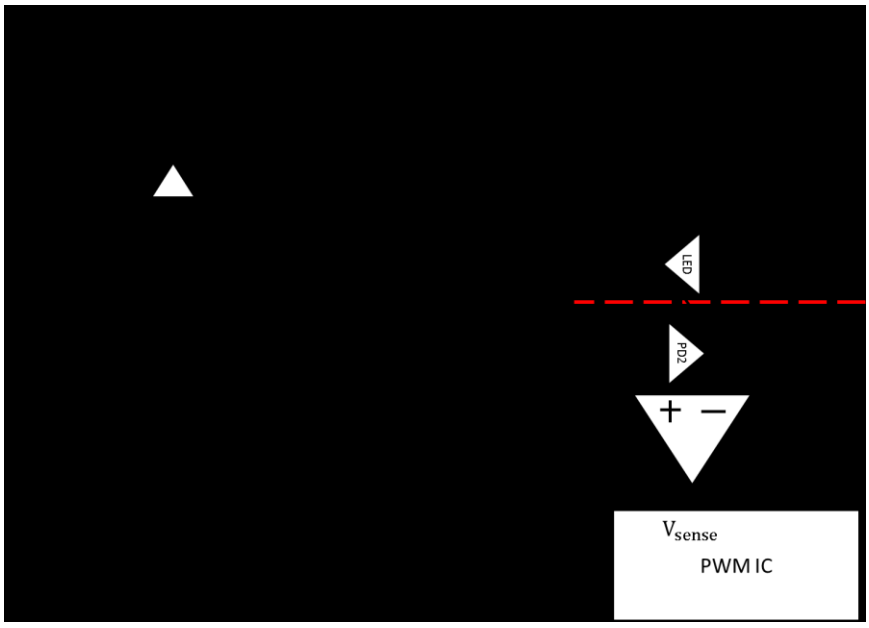


Figure 5.15 Final voltage sensing network detailed schematic

The voltage divider in the original circuit is now no longer a voltage divider because R_{f2} is in parallel with the equivalent resistance of the LED and R_{LED}. Also, the transfer function of the optocoupler topology has CTR in it. So the new design equations need to be defined. Since the solution must be found for the point at which the output is at 4 V a biasing point for the optocoupler is chosen to be the nominal value of 10 mA which is 1.55 V drop across the LED [14]. With an operating point set, the LED is converted to an equivalent resistance. The LED resistance and the biasing resistor R_{LED} are in series and both are in parallel with R_{f2}. Now the design equation can be found for the nominal output of 4 V, which is what the voltage sense pin of the HV9123 needs when the output voltage is at its nominal value of 50 V.

$$I_{V_{sense}}=\frac{V_{out}}{R_{f1}+R_{f2}\,||\left(R_{LED}+\left(\frac{V_{LED}}{I_{LED}}\right)\right)}=I_{LED}+\frac{V_{in}}{R_{f2}} \quad \textbf{(5-25)}$$

$$V_{out}=50V,\ V_{in}=4V,\ V_{LED}=1.55V,\ I_{LED}=10\ mA \quad \textbf{(5-26)}$$

$$R_{led}=\frac{V_{in}-V_{led}}{I_{LED}}=245\ \Omega \quad \textbf{(5-27)}$$

$$\frac{50}{R_{f1}+\frac{400*R_{f2}}{R_{f2}+400}}=10m+\frac{4}{R_{f2}} \quad \textbf{(5-28)}$$

This system is easier if it is solved graphically. The best solution for this design equation is found when both R_{f1} and R_{f2} are equal to 4.2 kΩ. Once this is set the transfer function for the open-loop analog transmission optocoupler can be determined when a nominal CTR is 0.2%.

$$R_2=\frac{R_{LED}}{CTR}*\frac{V_{out}}{V_{in}}=\frac{245}{0.002}\left(\frac{4}{4}\right)=122.5\ k\Omega \quad \textbf{(5-29)}$$

This size of an output resistance increases the propagation delay as seen in the Optocoupler Experimental Chapter. This is an acceptable design trade-off for two reasons. The value of R_{LED} is small enough to compensate some of that propagation delay increase, and the speed of the voltage signal

transmission is not as important as the current sensed signal. Cycle to cycle it stays constant at steady state and is regulated more so by the inductor current. Also, a large output resistance is needed to get the required gain which is the most important for accurately transmitting the output voltage information.

The biasing limits of this circuit need to be determined. This will determine how much the output voltage can change before this sampling network and transmission network will not be biased correctly. Figure 5.16 shows a graph with output voltage of the Buck converter as the x-axis and the output voltage of the transmission network (input voltage to the PWM voltage sense pin) and the LED current plotted as the y-axis. R_{LED}, R_{f1} and R_{f2} are constant while the equivalent resistance of the LED changes with the changing I_{LED} (CTR is held constant).

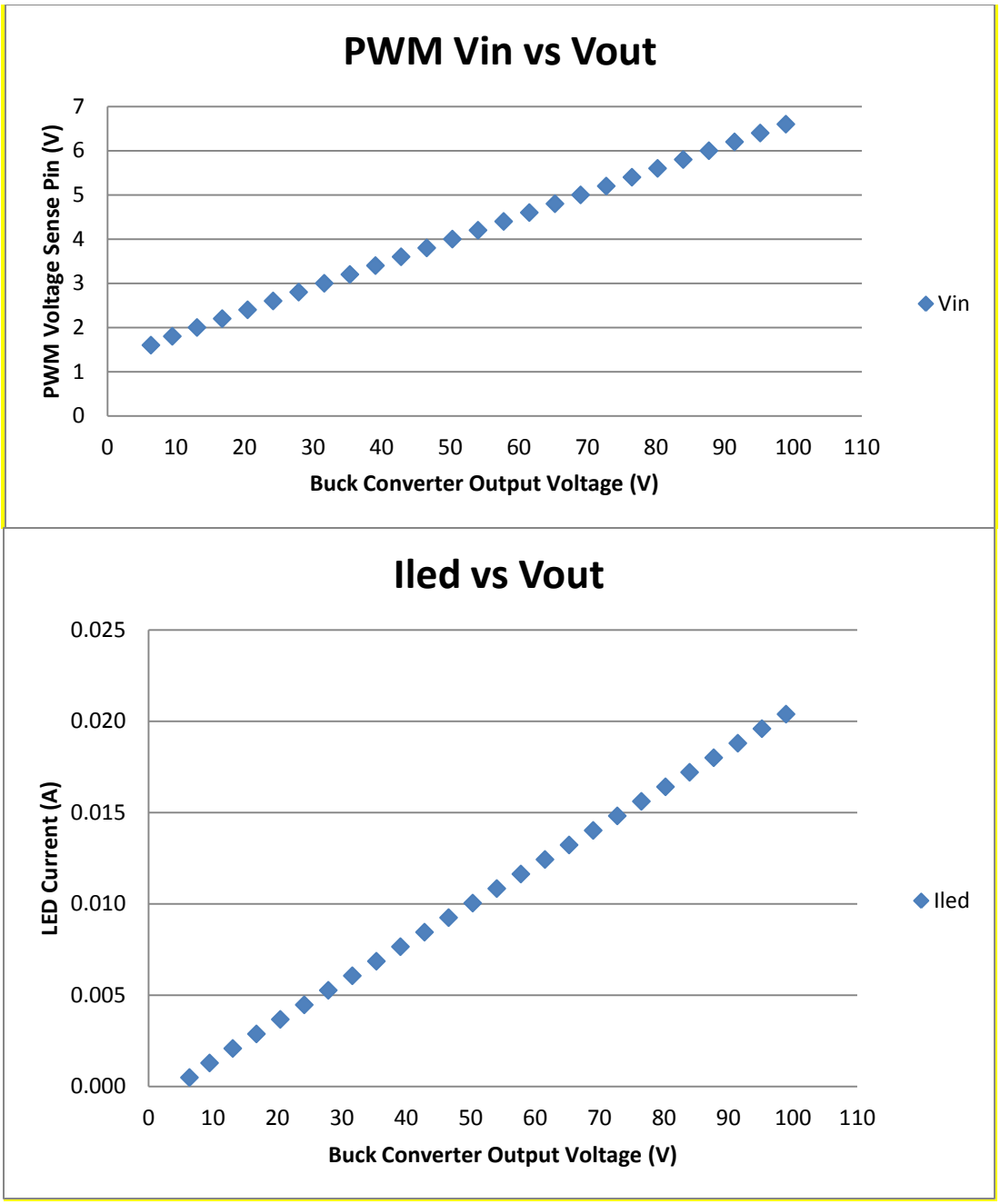


Figure 5.16 PWM voltage sense pin and input LED current versus Buck converter output voltage

The graphs above show that the range of operation for this circuit is from 9 V of the output voltage of the Buck converter to 100 V and greater. The LED current stays within a range of 3 mA to 20 mA which will cause some non-linear responses on the output of the open-loop analog transmission

topology (operation outside of the plateau region). With an R_{LED} value of 275 Ω this region starts at an LED current of 16 mA which corresponds to an 80 V output. This shows that the inabilities of this optocoupler topology to have a constant voltage gain over a range of inputs will affect any transient voltages below 80 V. This trade-off for a decreased propagation delay with this value of R_{LED} is acceptable though. At the nominal 50 V output the open-loop topology will transmit 4 V to the PWM correctly. If the output voltage droops the CTR will decrease causing the voltage gain to decrease but still reflect a decreasing output voltage. This is not a desired effect for a transient drop in the output voltage, but for an output voltage spike the CTR will increase and increase the voltage gain. This will actually increase the response of the control circuitry to dampen the output voltage by decreasing the duty cycle.

Now system variables, the inductor current and output voltage, have been sensed and scaled to the correct values needed by the PWM IC to set the steady-state parameters for the current (5 A) and output voltage (50 V). Now the PWM IC needs to be analyzed more in-depth. The biasing of the IC must be correctly implemented, along with determining how to send the PWM output to the gate driver through the isolation barrier.

5.1.5 Control Circuitry

The PWM IC has been determined to be the HV9123 [24], and now it must be set up properly. This includes biasing the chip, setting the internal oscillator to the correct frequency, using the start-up function correctly, and correctly connecting the compensation pin. The pin diagram is shown in Table 5.2.

Table 5.2 Pin Diagram for HV9123 [24]

Pin #	Description	Pin #	Description
1	+VIN	9	Oscillator In
-		10	Discharge
-		11	VREF
4	Current Sense	12	$\overline{\text{Shutdown}}$
5	Output	13	Reset
6	-VIN	14	Compensation
7	VDD	15	Voltage Sense
8	Oscillator Out	16	Bias

The values for the different external components are shown in Figure 5.17 [26]. The start-up functionality is generated by setting the PWM to a maximum duty cycle of 95% when there is no input applied to the Buck converter. At start up this will allow current to flow limited to the 5 A setting until the circuit is in steady state where it will operate at 50% duty cycle. The compensation is not added to stabilize the poles created by the output filter of the Buck converter because only steady state operation will be analyzed. Also, unlike most systems, the response time will not be determined by the compensation network but by the optocouplers propagation delay.

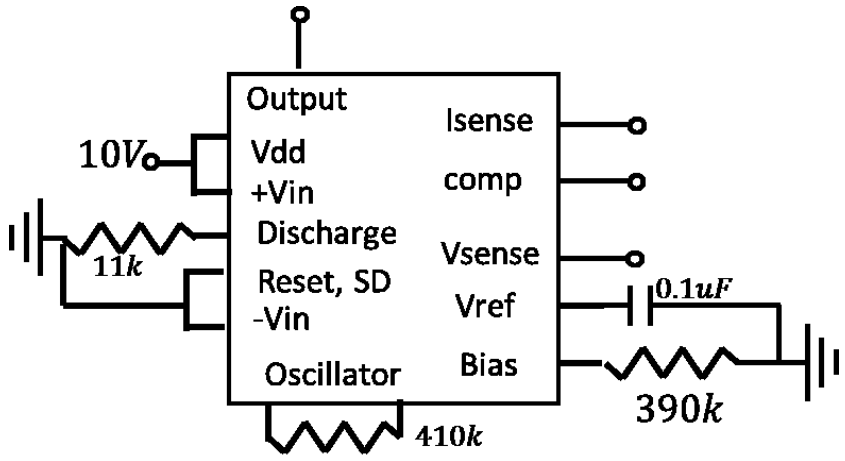


Figure 5.17 External components for HV9123 operation at 85 kHz and 95% maximum duty cycle [24]

The output of the PWM IC is a PWM signal. This signal can only source ±10 mA and is a single square wave which needs to be converted into a separate on- and off-pulse as shown in Figure 5.18. These pulses are then buffered and sent to the digital transmission optocouplers to be sent to the high-side gate driver.

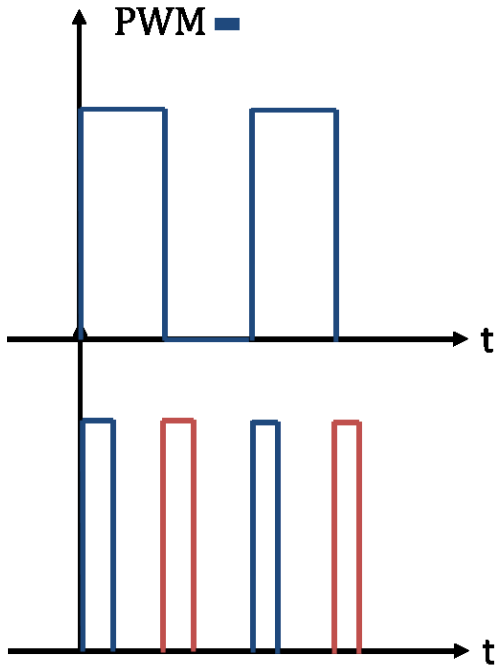


Figure 5.18 Converting PWM signal on top to two separate on- and off-pulses on the bottom

The pulse circuitry is best explained when focusing on one pulse. The design will focus on the on-pulse. First of all, the on-pulse needs to be an exact duration which depends on the rise time of the gate driven by the high-side gate driver. This precise pulse duration is created by a switched capacitor scheme and a comparator. Figure 5.19 shows this topology.

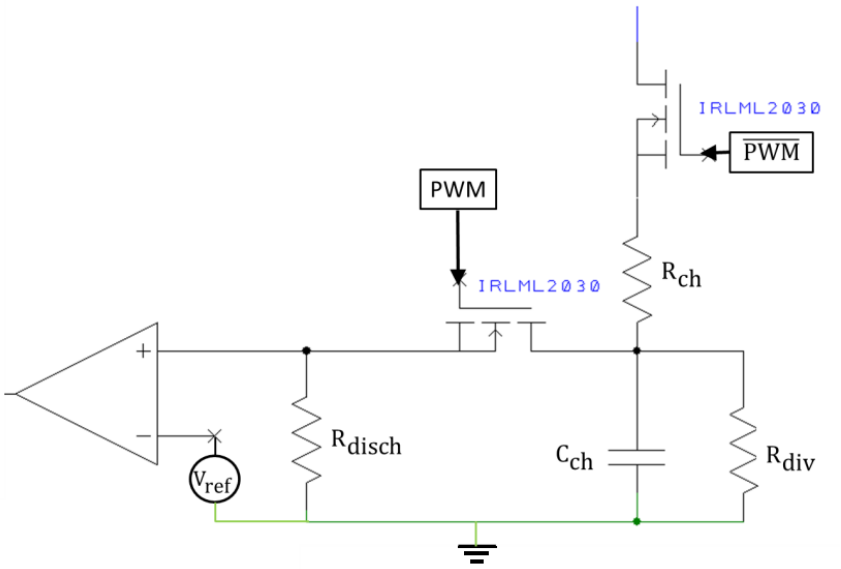


Figure 5.19 Pulse circuitry for on-pulse generation (off-pulse generation is the same with control signals from PWM inverted)

When the PWM signal is low the charging branch is on, causing the capacitor to charge to a final value set by R_{ch} and R_{div}. This value must be reached before the PWM signal goes high in a worst case scenario, which would be the minimum duty cycle of 5%. When the PWM signal goes high the charge switch turns off while the discharge switch is turned on and the capacitor discharges through R_{disch} from its peak value past the negative terminal reference value of V_{ref}. The amount of time that this takes depends on the design equation below.

$$V_{final}=V_{dd}*\frac{R_{div}}{R_{div}+R_{ch}} \quad \textbf{(5-30)}$$

$$t_{ch\text{-}V_{final}}=2.3*C_{ch}(R_{div}||R_{ch})<0.1*T_s \quad \textbf{(5-31)}$$

$$V(t_{pulse})=V_{ref}=V_{final}*e^{\frac{-t_{pulse}}{(R_{div}||R_{disch})C_{ch}}} \quad \textbf{(5-32)}$$

$$-(R_{div}||R_{disch})C_{ch}*\ln\left(\frac{V_{ref}}{V_{final}}\right)=t_{pulse} \quad \textbf{(5-33)}$$

The value of V_{ref} is decided first to be 2.5 V and the final charge voltage for the capacitor will be 5 V. The desired t_{pulse} is the rise time of the MOSFET which will be around 100 ns. With the initial period used of 11 µs, the minimum charge time is 550 ns. The final values are chosen with the design equations above.

$$\frac{5}{10}=\frac{R_{div}}{R_{div}+R_{ch}} \quad \textbf{(5-34)}$$

$$550n=2.3*10n(50||50) \quad \textbf{(5-35)}$$

Because of all the capacitance in the pulse circuitry, if the charge capacitor is chosen less than 10 nF it will discharge too much when the discharge switch is turning on and there will be no pulse on the output of the comparator. This is shown in Figure 5.20 with experimental and simulated data. The capacitor in this experiment and simulation is below 1 nF.

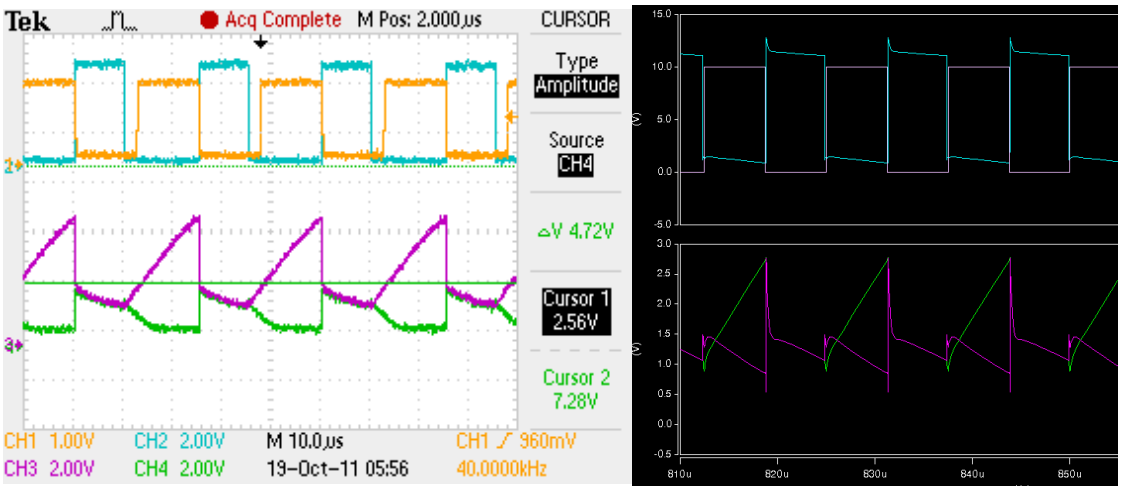


Figure 5.20 Cap discharge below Vref (2.5 V) due to parasitics eliminates pulses; (left) PWM signal (top), cap voltage (purple), Rdisch voltage (green); (right) PWM signals (top), cap voltage (green), Rdisch voltage (purple)

With the capacitor chosen at 10 nF, the resistors are chosen to be 50 Ω. Now the discharge resistor can be determined to give the 100 ns pulse duration, which is determined as 30 Ω in the equation below.

$$-(50||30)10n* \ln\left(\frac{2.5}{5}\right)=130n \qquad \textbf{(5-36)}$$

The waveforms of the pulse circuitry are shown in Figure 5.21. The output of the comparator is what will be sent to the digital transmission optocoupler.

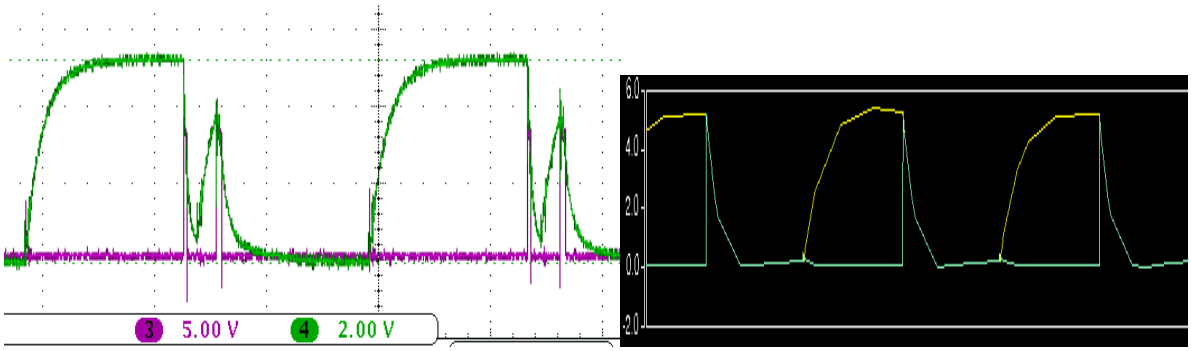


Figure 5.21 Pulse circuitry waveforms (experimental and simulated); (left) output pulse (purple), capacitor voltage (green); (right) capacitor voltage (yelow), Rdisch voltage (green)

5.1.6 Digital Transmission Optocoupler Selection

The selection of the digital transmission optocoupler is determined by the characteristics of the digital optocouplers presented in Chapter 4. The optocouplers must operate at the 10 V supply of the control circuitry unless and level shifter is used. Also, because the MAX15018A is chosen to relay the on- and off-pulses to control the half-bridge topology of the gate driver the digital optocouplers output voltage must be below 3.3 V to register an off-signal and above 6.7 V to register an on-signal to turn on the high-side MOSFET or low-side MOSFET of the gate driver [20]. The optocoupler to transmit the digital signals is chosen to be the LED and BJT pair. This is due to the ability to operate with a 10 V supply unlike the digital optocouplers with an amplifier output stage and the output voltage can swing from a

minimum of 2.2 V at 70 °C to 10 V which is within the thresholds to control the gate driver correctly. The key parameters of pulse width and output voltage range for this circuitry was shown in Chapter 4. Pulse width is important because the energy recovery gate driver is shown to need very short turn-on and turn-off pulses to enable the energy recovery function, fully explained in the Background Chapter and Gate Driver Design Chapter. The pulse width from the input is maintained at the output if the rise and fall times of the output are fast enough to track the input's rise and fall times. The rise and fall times are a restricting parameter of the control signal optocouplers (also spoken as the minimum pulse widths). The rise and fall times and amplitude of the output are the restricting parameters for the control signal optocouplers. With the two key restricting parameters of the LED and BJT digital transmission scheme are determined to be the only applicable optocouplers from the previous chapter because their pulse width, amplitude, and rise and fall times are the best with outputs that are compatible with the thresholds needed by the gate driver inputs. However, the outputs obtained are inverted so a small inverter is used on the high-side before the control signals are sent to the gate driver inputs. To bias these circuits correctly, a buffer stage is needed to drive the LED on the input because the comparator cannot supply the correct amount of current. The buffer and optocoupler scheme is shown in Figure 5.22.

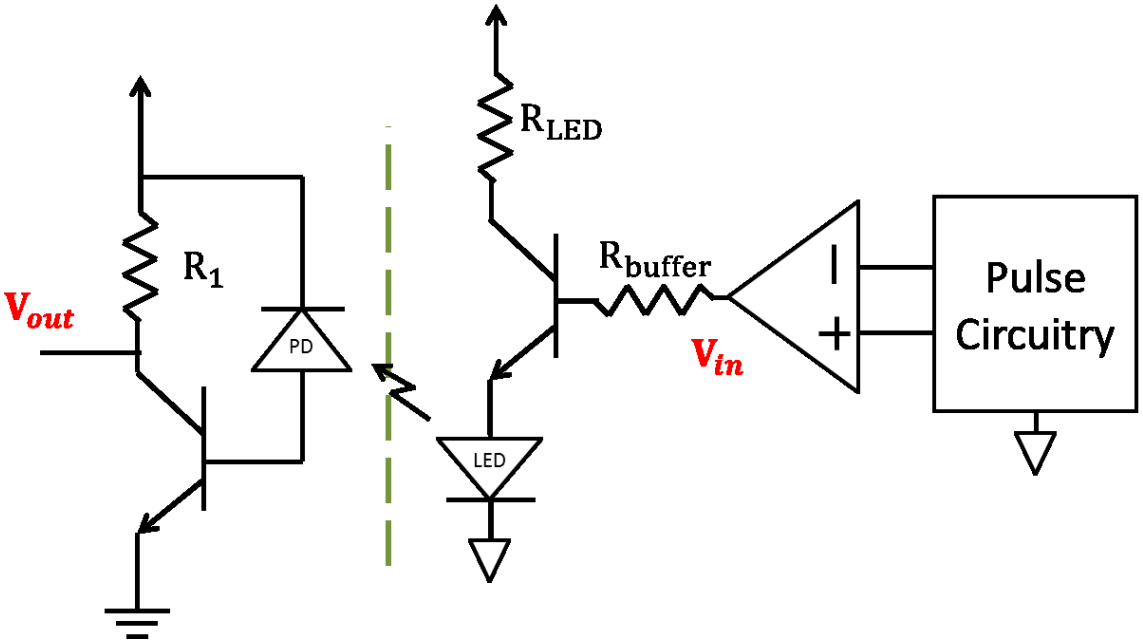


Figure 5.22 Buffer stage from pulse circuitry to digital transmission optocoupler

The comparator's current is buffered through an emitter follower that uses the design equation below to set the buffer resistor so that the proper current for the pulse is sent to the optocoupler. The important parameter is the LED current, which is equivalent to the emitter current.

$$I_{LED}=\beta\frac{(V_{in}-V_{BE}-V_{LED})}{R_{buffer}} \qquad \textbf{(5-37)}$$

With all of the components of the Buck converter designed, the next step is to validate the full system with a simulation and define the tests that determine the optocouplers used in this current-mode optically-controlled Buck converter.

5.2 Closed-Loop Buck Converter Simulation Verification

The Buck converter system validated with a simulation of the schematic shown in Figure 5.23. This simulation implements a simplified current-mode controlled buck converter. There is not any isolation modeled in this simulation because of the absence of a dynamic optocoupler model.

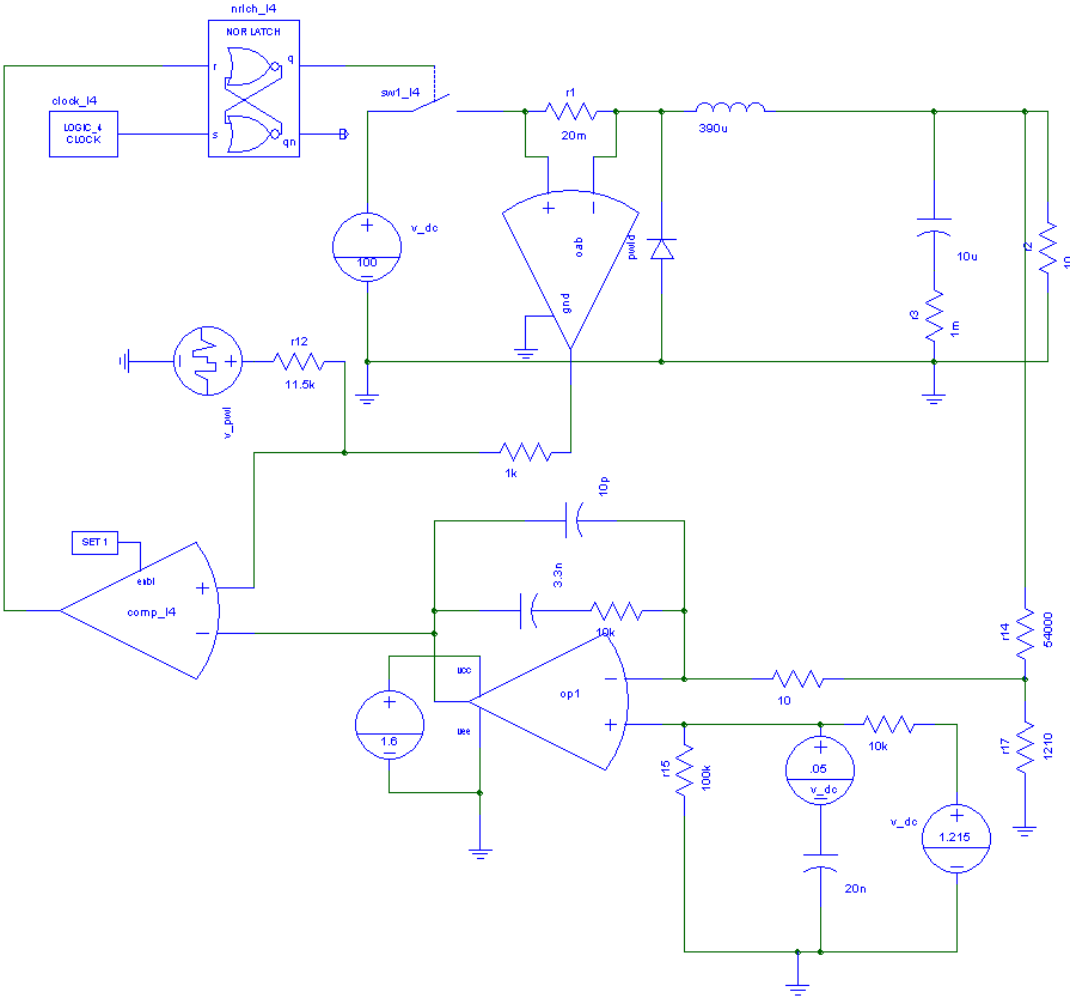


Figure 5.23 Schematic of current-mode Buck converter to validate the design above

This simulation takes into account the current and voltage sensing loop with a Buck converter operating with all of the open-loop parameters defined above (85 kHz, 100 Vin, 50 Vout, 5 A, and correct output filter). The current sensing scheme takes into account the sensing resistor, current sensing amplifier with correct gain, and slope compensation. The analogous voltage of the current sensing signal is then compared to an error voltage that is set to around 1 V (what the HV9123 scales the 4 V voltage sense pin voltage to) to allow for a nominal output voltage of 50 V at 5 A [24]. The compensation network has to be added so that this simulation will mirror the characteristics of the HV9123. The system is simulated over 5 ms with a soft-start of the entire circuit shown in Figure 5.24.

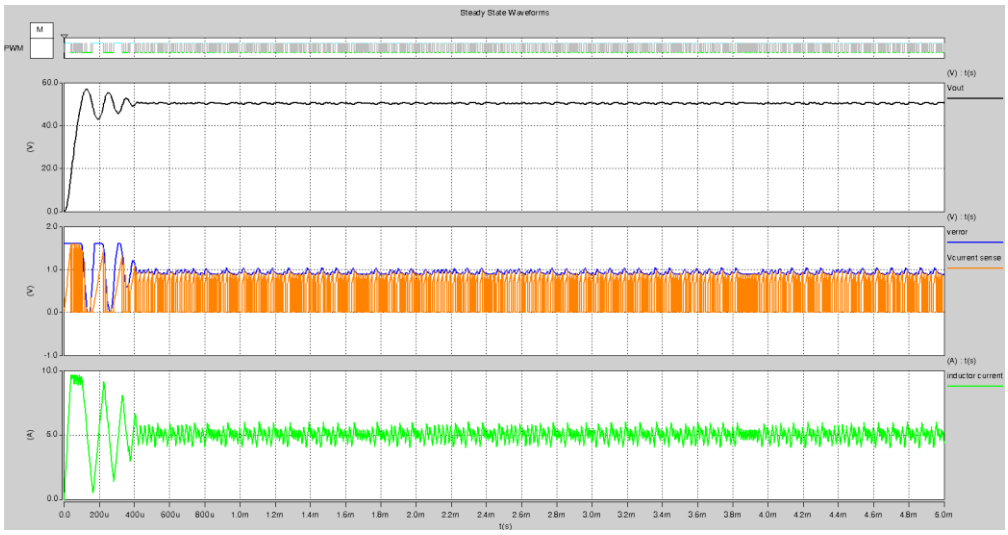


Figure 5.24 Full system simulation, output voltage (black), error voltage (blue), current sense (orange), inductor current (green)

Overall this simulation validates the design chosen above, albeit for oscillations in the inductor current. The output voltage is very stable and Figure 5.25 shows a zoomed in view of a very stable region of this simulation that represents what will be desired in the final design.

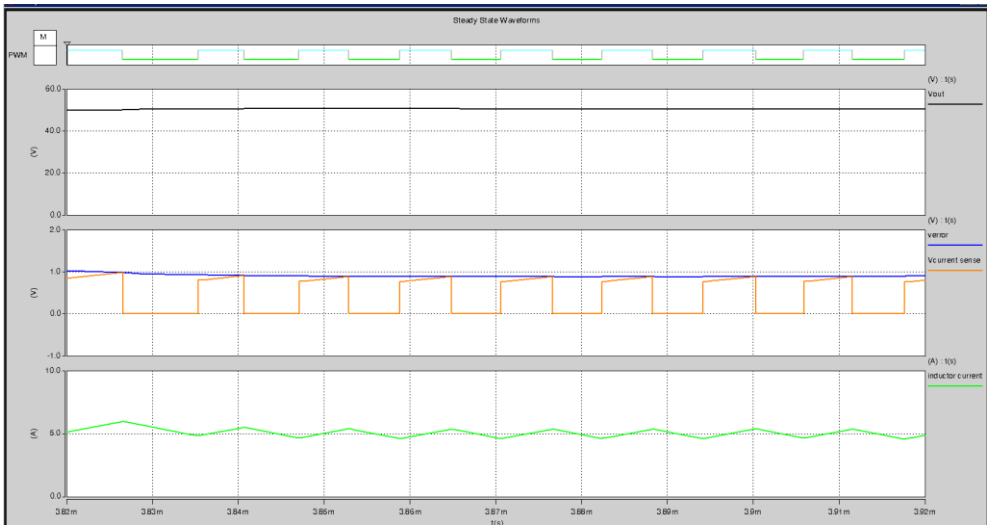


Figure 5.25-Waveforms zoomed in (current and voltage ripple well within design criteria), output voltage (black), error voltage (blue), current sense (orange), inductor current (green)

5.3 Current-Mode Optically-Controlled Buck Converter

With all the full system components designed the current-mode optically-controlled Buck converter can be implemented and a PCB may be designed and populated. The first section will discuss the implementation and initial testing that is done to verify the design fulfills the results from the simulation presented in the Buck design section. Once the operation is verified the final experimentation can begin. The objective for these final experiments of the entire system is to determine the impact of the optocoupler feedback and control networks. Because the weakest link for the optocouplers is the propagation delay the impact on the full system is determined by increasing the frequency of operation of the Buck converter system until the optocouplers impede the proper operation. The respective topologies chosen have been analyzed in depth individually and the benchmark for the current optocoupler technologies is presented and discussed in the Conclusions Chapter to follow.

5.3.1 PCB Implementation of Current Mode Optically Controlled Buck Converter

The first step to testing the full system and determining how the optocouplers affect the operation is designing a PCB for the system. The PCB layout is designed to have all three isolated sections on one board with the optocouplers in between the Buck converter and high-side sensing section and the control circuitry section. Short routing tracks were integral because of the frequencies of the signals. The optimized layout is shown in Figure 5.26 with the sections labeled and the full schematic is shown in Figure 5.27.

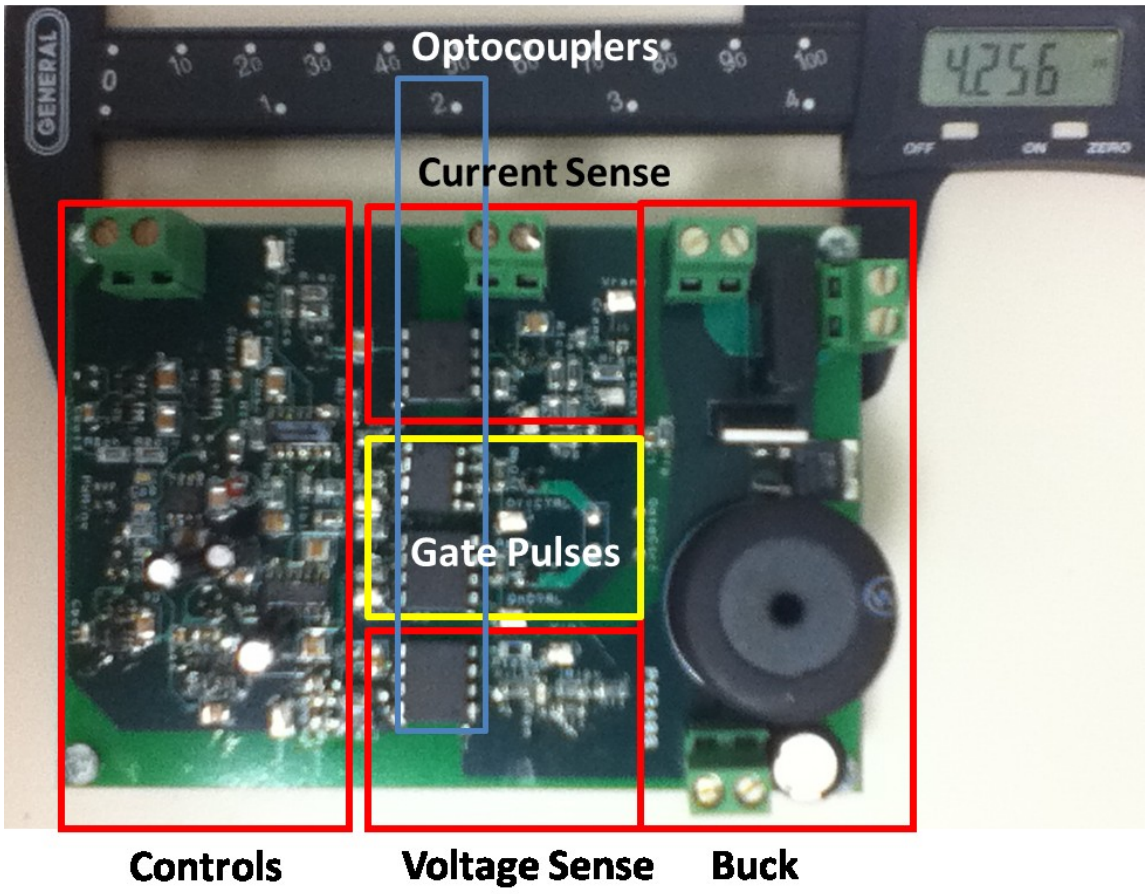


Figure 5.26 Full system PCB in the lab fully populated with sections marked

Once the system is designed a PCB, tests were conducted to verify the physically implemented design. The PCB needs to be verified at the initial values of 85 kHz switching and 100 V input voltage. The test setup is shown in Figure 5.28.

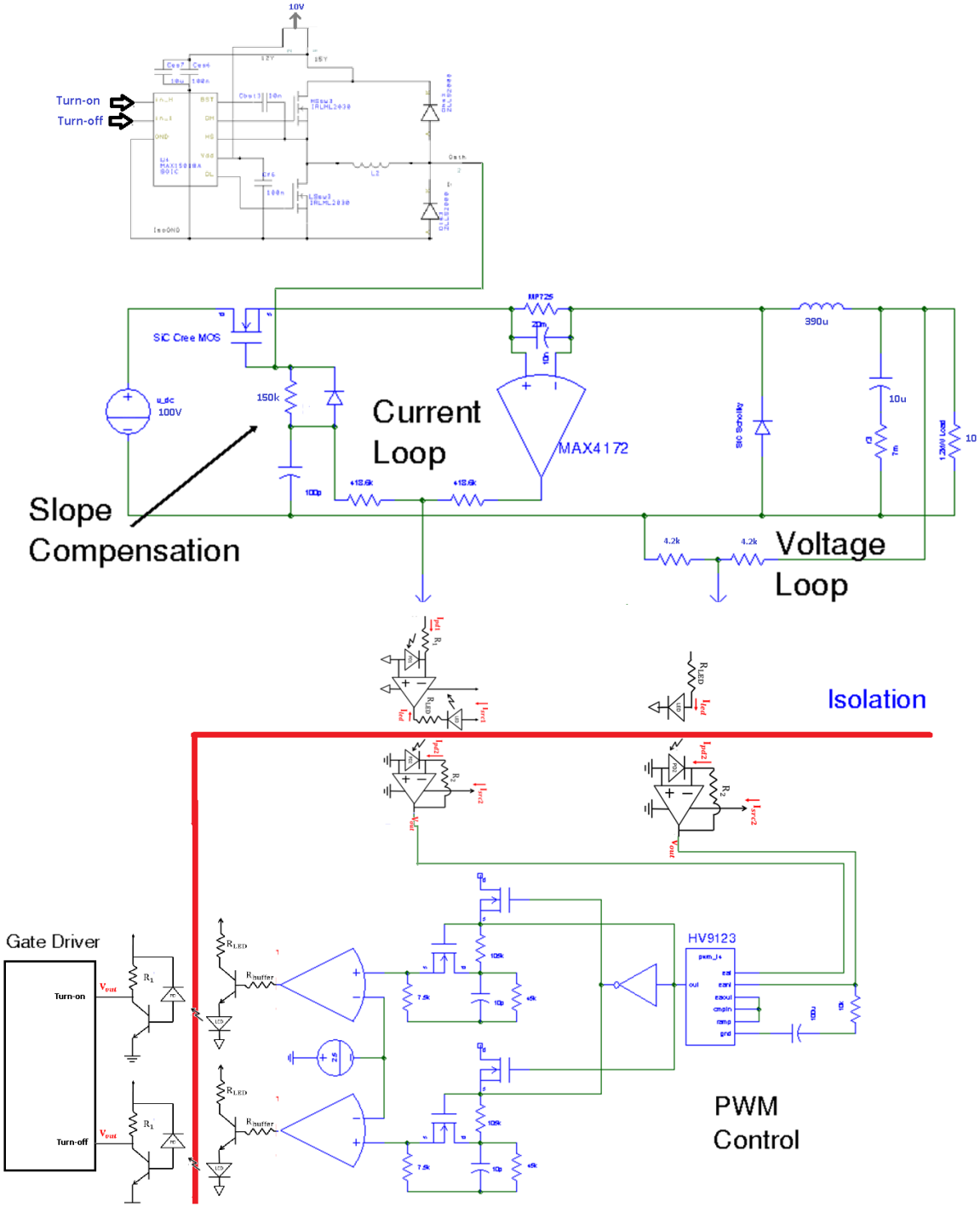


Figure 5.27 Full schematic

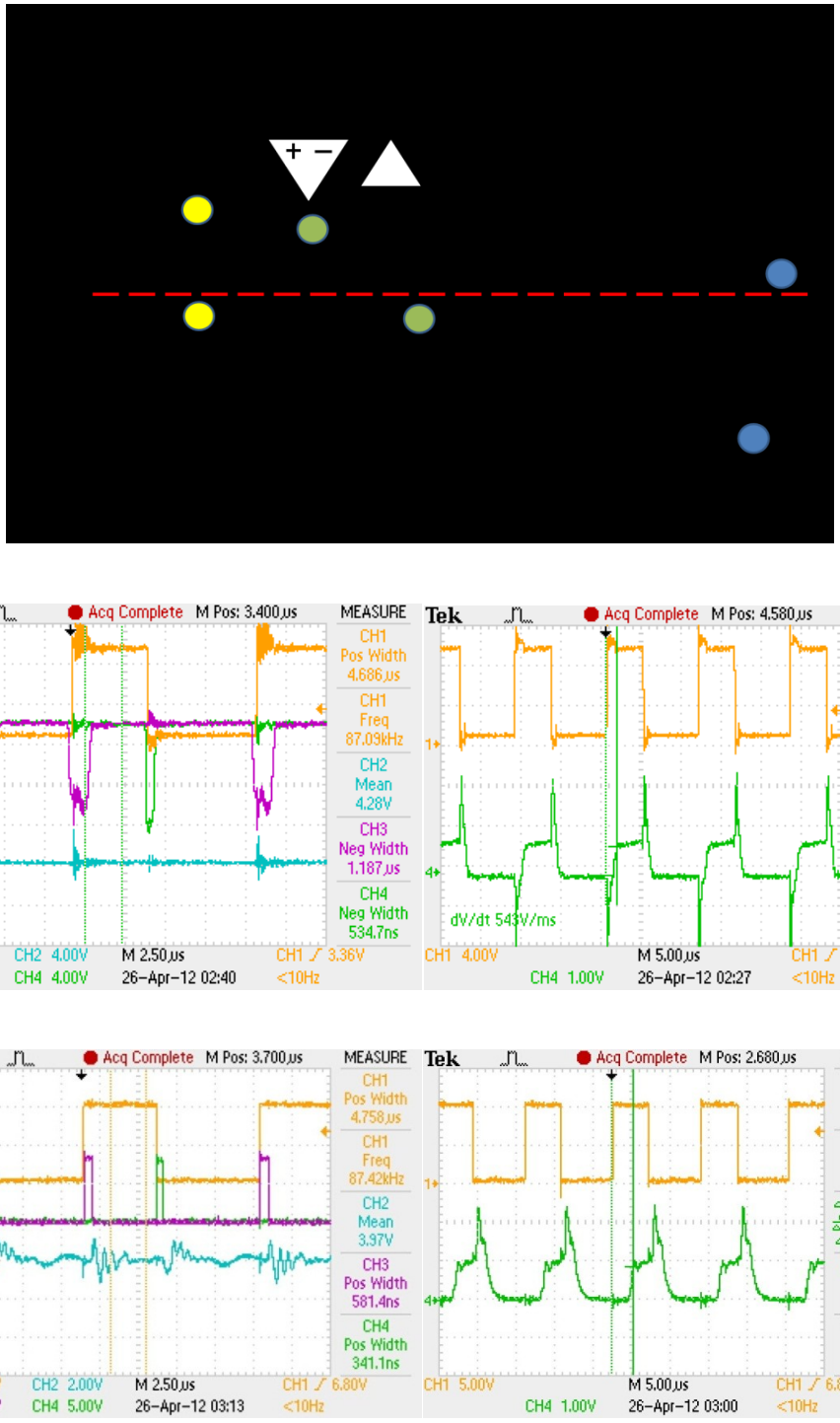


Figure 5.28 Row one: schematic shows the signals measured and their colors; row two: Gate voltage (yellow), on/off-pulses (green and purple), voltage sense (blue), current sense (green); row three: PWM output (Yellow), on/off-pulses (green and purple), voltage sense (blue), current sense (green)

As the initial verification tests began, troubleshooting of different sections of the board took place. Many things like noise and parasitics affected the ideal design described in the Buck converter design section. There are important changes to the design that were decided upon during the verification phase. There were other troubleshooting difficulties, but they are skipped because the problem and solution do not add to or change the benchmark of the optocouplers or the final Buck converter design. The difference in the following troubleshooting discussion is that these changes affect the operation and benchmark of the current-mode optically-controlled Buck converter. The first changes have to do with the noise of the switching MOSFET. Figure 5.29 shows the noise on the gate and drain of the MOSFET while switching, this noise is reflected into the sensing network which causes issues.

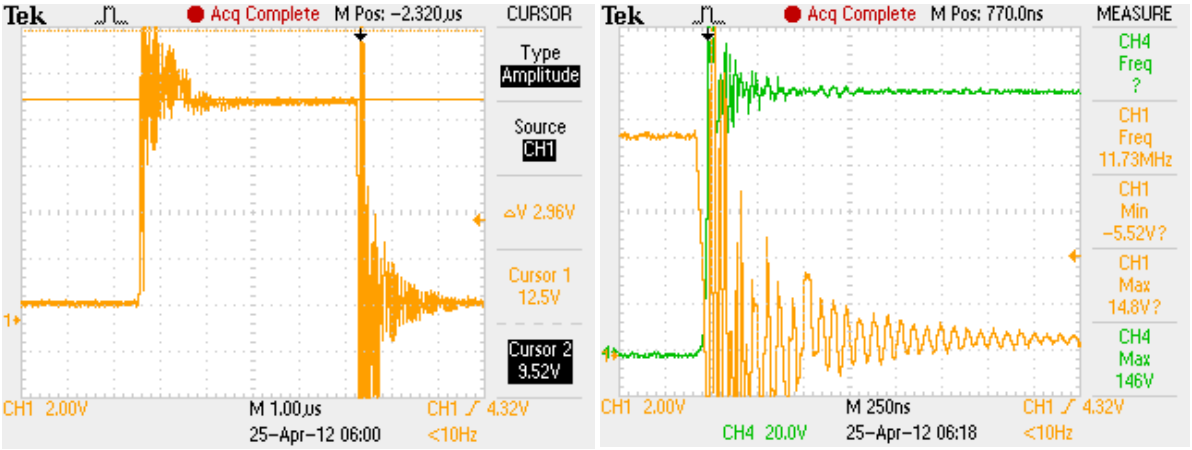


Figure 5.29 Oscillations present in gate (yellow) and drain (green)

The SiC MOSFET is switching 100 V at 85 kHz. The energy being switched is not the problem here. The problem is the rise and fall time of the MOSFET's gate voltage, which is only 8 ns. With any parasitics in the system that will cause a very large spike. The first step is to slow down the rise time by adding inductance into the gate driver path. Adding inductance decreases the resonance frequency, and as described in the gate driver chapter the turn-on time decreases. This is done to decrease the $\frac{di}{dt}$ which, due to inductance being the main component of the parasitics in the circuit, will decrease the

voltage spikes. The original inductance was 22 nH, which is changed to 1 µH in which increases the rise time to 80 ns so that the change in current decreases. A lot of the noise is still present. Figure 5.30 shows that the noise is actually on the turn-off signal coming from the digital optocoupler that transmits this control signal.

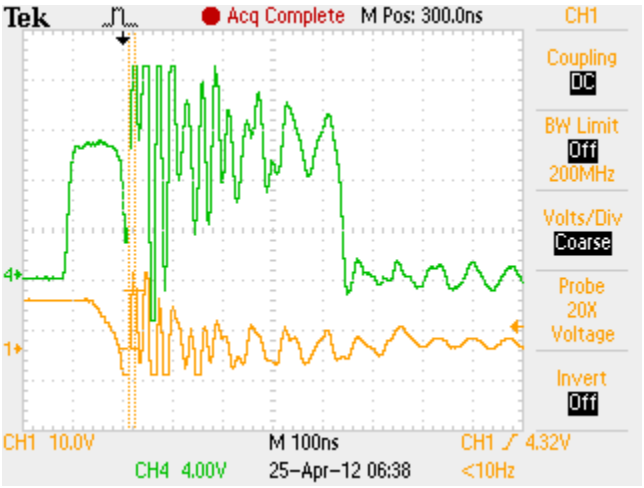


Figure 5.30 Noise in off-pulse (green) and gate voltage (yellow) (spike at 14V+)

The solution was to braid the signal line in the same ground line so that any noise from EMI would appear as common-mode noise and the potential difference would still be the same. The noise shows up in both signal and ground because the tightly braided lines will allow the two signals to share the same space and any electromagnetic signals will affect both wires. Figure 5.31 shows the gate and drain with a smaller and shorter duration noise. The rest of the noise is due to the pulse being on too long because of the limitations of the digital optocoupler. Because of the slow response times of the digital transmission optocoupler pulse width is added to the original signal which causes the energy recovery feature to be disrupted. This response time is further illustrated in the following sections.

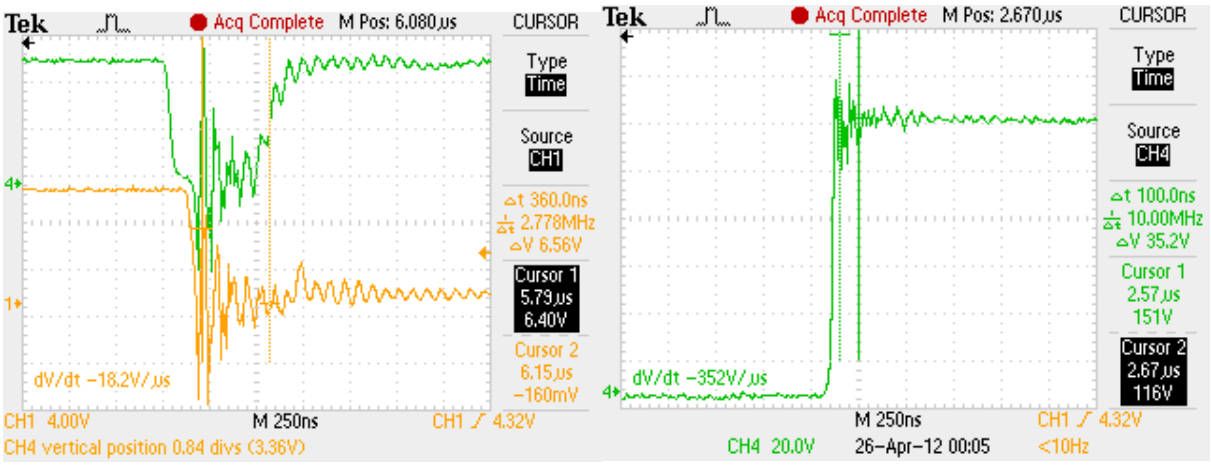


Figure 5.31 After ground wrapped control signal; (left) on-pulse (green), gate voltage (yellow) (spike reduced to 6 V); (right) drain voltage (green)

The next design changes have to do with the optocoupler application topologies. The first change is the resistors that set the gain in the circuitry. Initially the optimal test setup is used of 33 kΩ for both resistors, but the parasitics caused two problems -- an oscillation in the current sensing network and gain differences that needed to be compensated. The gains in the circuit were compensated by increasing the current sense analog transmission topology's R_2 to 43 kΩ and the voltage sense network's sampling resistors were changed to 3.9 kΩ and the LED resistor to 390 Ω. The LED resistor for the current sensing network was a different problem. There were oscillations at a high frequency present in the power supply which is shown in Figure 5.32.

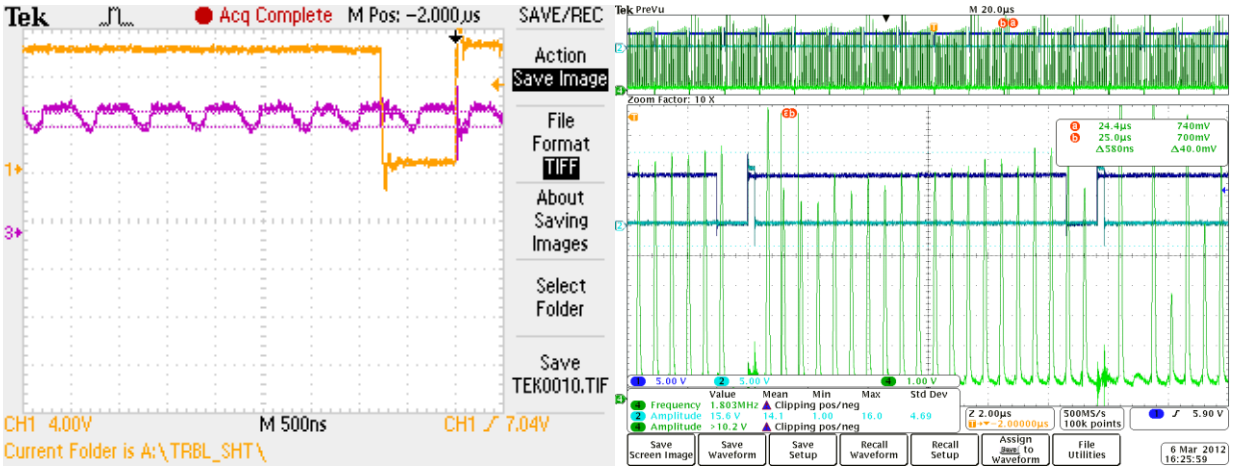


Figure 5.32 Oscillations showing in LED voltage of optocoupler (right-purple) and in output of analog transmission topology (right-green); yellow and blue are gate and PWM voltages, respectively

These were dampened by increasing the LED resistance to 900 Ω shown in Figure 5.33. The increased resistance increases the dampening of any ringing present in the circuit. It had to be increased because the ringing in the circuit needed to be dampened to not falsely trigger the Buck converter's switch. The trade-off is that the propagation delay of the optocoupler decreases as was shown in the application topology test. Figure 5.33 shows the current sensing in green working as predicted. The delay and turn-on spikes are due to the large noise present in the system when it is switching 100 V at 100 kHz and more. These need to be filtered out as best as possible to optimize the operation of the circuit.

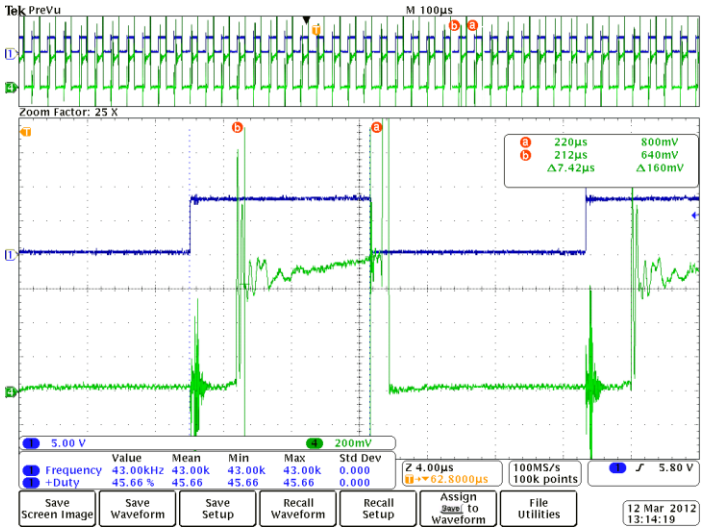


Figure 5.33 Current sense working (green), blue signal is PWM

The next step is the use of low pass filters at the current sensing op amp, voltage sensing input and output, and at the current sensing output. This changes the current signal from the figure above to Figure 5.34. The turn-on spikes are completely gone, while the turn-off spikes (larger due to energy stored in the Buck converter inductor being switched to a different branch of the circuit) were decreased to 2 V.

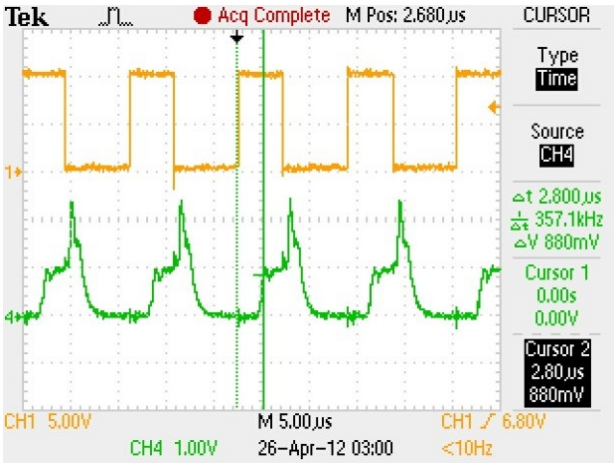


Figure 5.34 Oscillations gone, spike still exists at turn-off due to energy stored in inductor of Buck converter output filter

5.3.2 Benchmark for Current Mode Optically Controlled Buck Converter

Now that the important design changes have been made the initial verification is complete. The initial operation of the Buck converter working at the initial frequency is shown previously. It works with a 100 V input and a 50 V output limited to 5 A. The final test can now be proposed. The system's operating frequency will be changed from 85 kHz to the maximum frequency that the optocouplers will allow. The change in the system will be recorded and a final benchmark can be concluded. The test setup measures many different parameters. Figure 5.35 highlights each system variable that is measured.

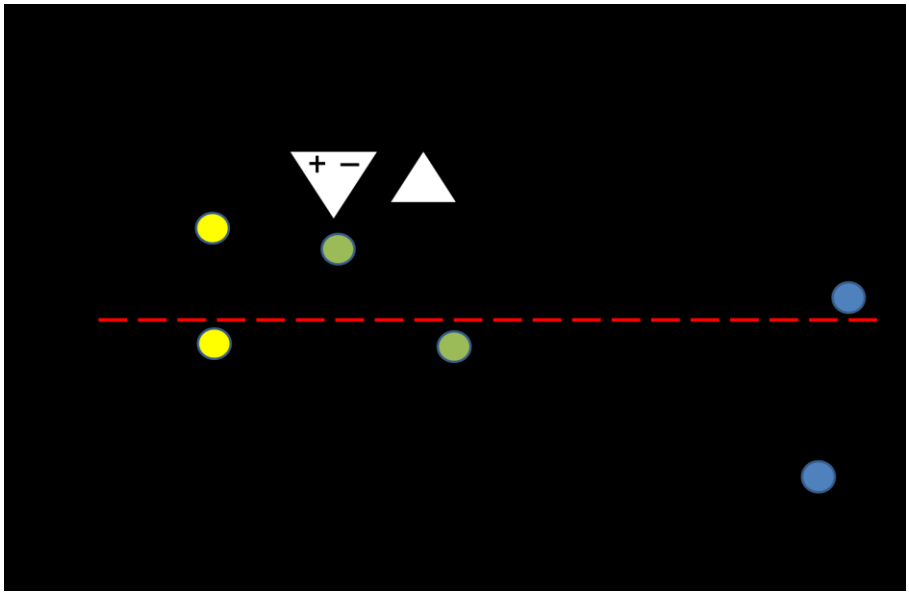
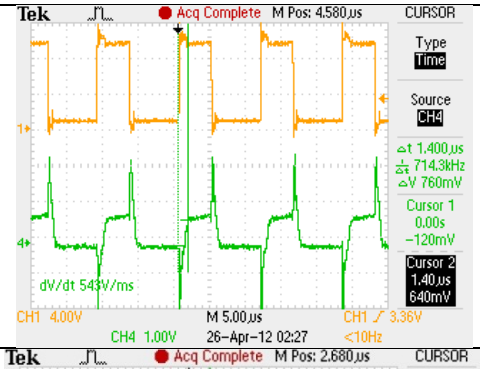
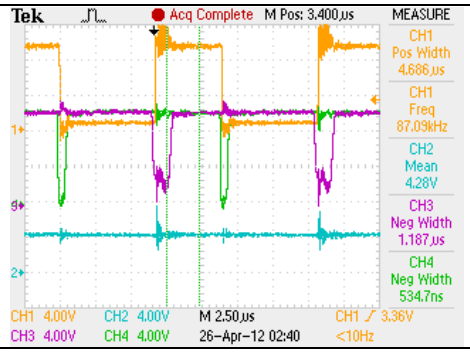
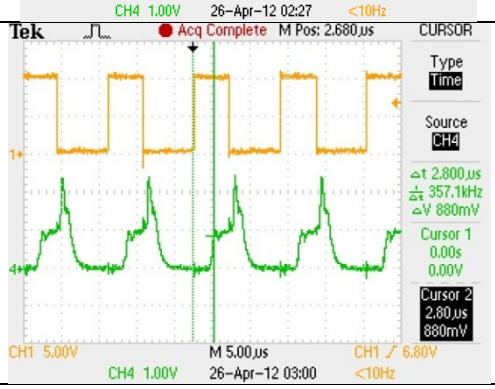
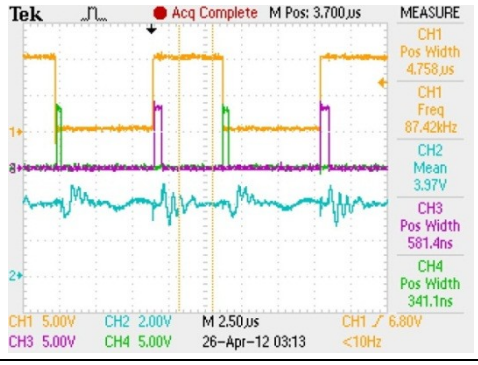
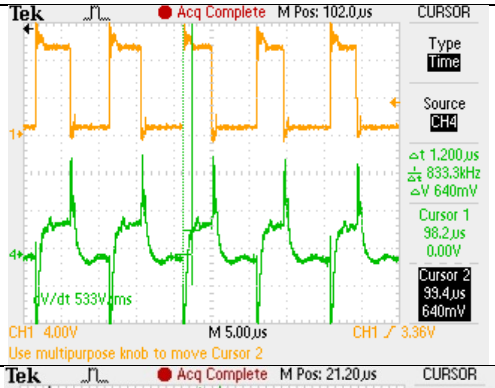
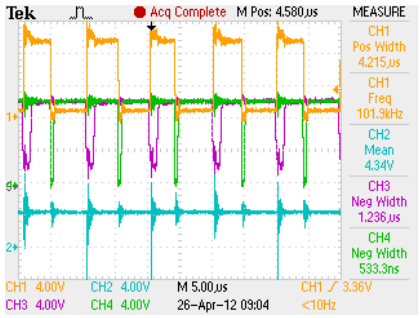
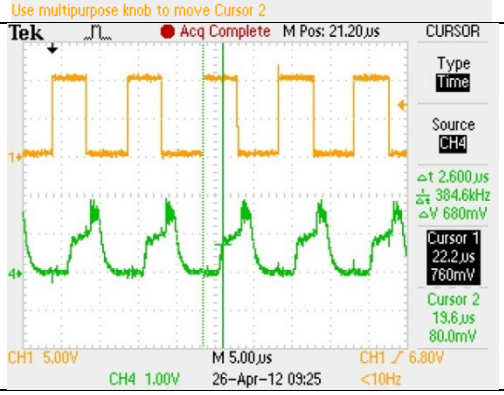
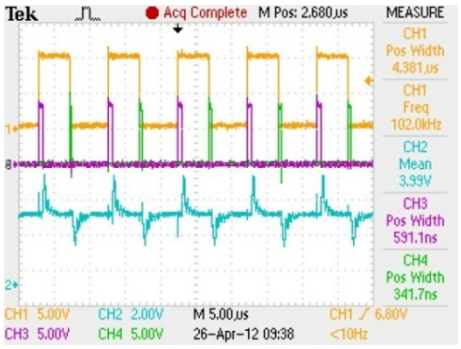
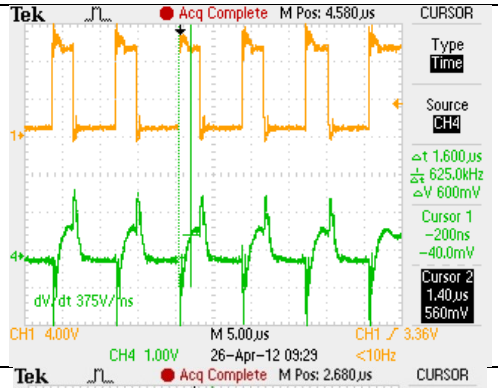
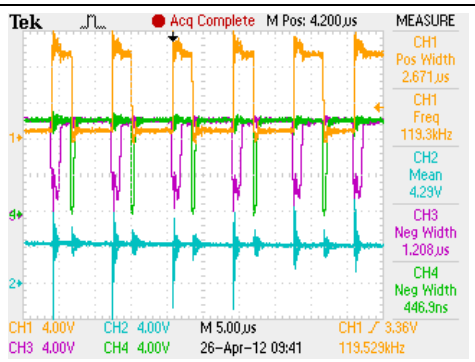
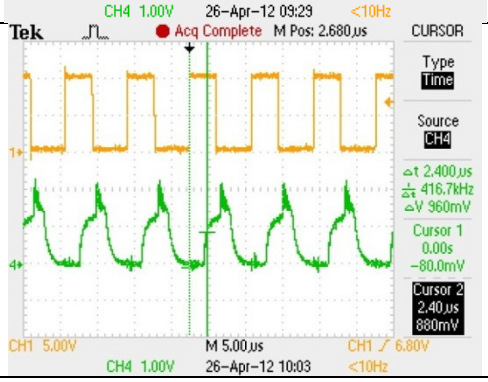
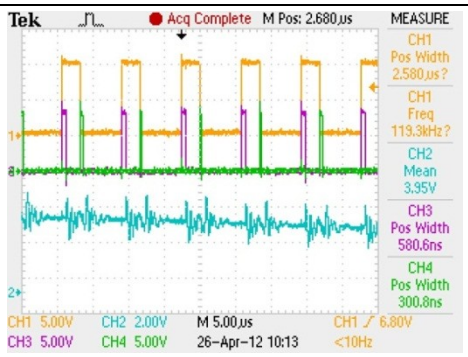
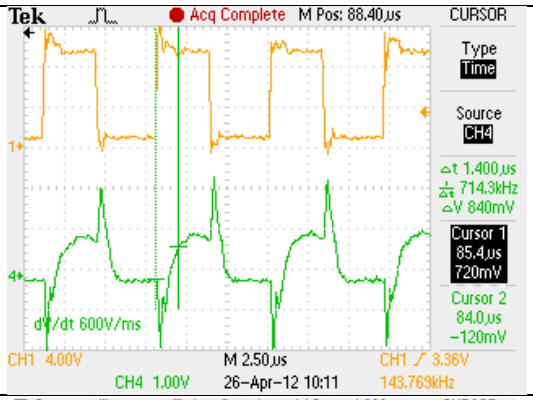
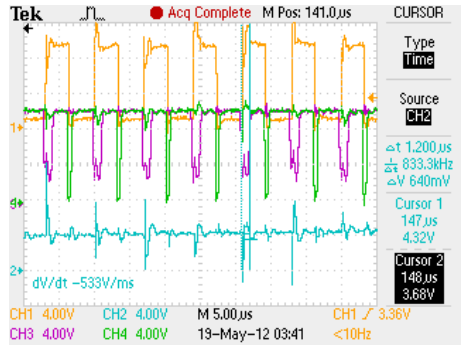
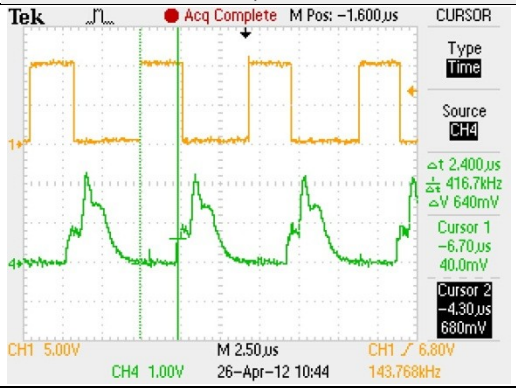
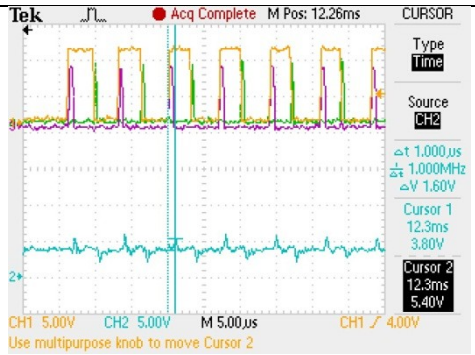


Figure 5.35 Measurements emphasized with colored circles where the dotted line represents the isolation barrier (note that the PWM and Gate signal also show the on- and off-pulses)

Table 5.3 shows the results from increasing the frequency until a maximum frequency was reached due to either the propagation delay of the analog transmission optocouplers or an overlap in the command signals because of the minimum pulse width of the digital optocouplers. The Conclusions Chapter will discuss these results specifically.

Table 5.3 Results for Buck Converter Tests with Increasing Switching Frequencies

	85 kHz	
Power		
Control		
	100 kHz	
Power		
Control		

	120 kHz	
Power		
Control		
	140 kHz	
Power		 *Off-pulse width= 700ns
Control		 *Off-pulse width = 400ns

The propagation delay from the current sensing analog transmission circuitry is a total of 2.4 µs due to the noise present in the system and the increased propagation delay of the optocoupler topology. Also the digital pulses are as large as 1.2 µs on the output of the digital transmission optocoupler due to the minimum pulse widths of that circuitry. This is not the first failure mode in the circuit, but if the operating frequency was able to reach 250 kHz the digital propagation delay would impede correct operation of the Buck converter. The next chapter summarizes the experimental results from the Optocoupler Experimental Chapter to determine the benchmarks and the final implication of the optocoupler on the Buck converter system.

6 CONCLUSIONS

The objective of this thesis is to determine the benchmark performance of the current optocoupler technologies and to design a real-world application for the optocoupler to operate in and display the benchmark within the context of a system. The information presented started with the specific concerns of this thesis. The first concern is the performance of commercially available optocouplers, and to create a benchmark of these optocouplers operating in the specific schemes defined to be analog and digital transmission. This benchmark is determined by experimenting with the two different roles that the optocouplers are applied in (analog and digital transmission) with respect to the important characteristics. These characteristics were defined as propagation delay, linearity, and temperature operation for the analog topologies, and propagation delay, minimum pulse width, and temperature operation, for the digital topologies. Different experiments were conducted in the Optocoupler Experimental Chapter to determine the characteristics of the optocoupler transmission topologies. Below, the final benchmark for the two different optocouplers schemes will be presented.

A parallel concern is to implement these optocoupler topologies that are defined, and test them to determine a benchmark in a specific power electronics system design. The design chosen was a current-mode controlled Buck converter. This system allows for the optocoupler to be shown off in two ways. First, is in the sensing networks that sense and transmit the key system variables (inductor current and output voltage) through the isolation barrier to the low voltage control of the system. The second part is to digitally transmit the control commands through the isolation barrier to the floating, high-voltage, gate driver to control the switch's state. This system determined and explored the limiting factors that the Buck converter had when the optocouplers were placed in the feedback and control path. This is a desired area of research because of the innovations sought in power electronics are

increasing power density, operating temperature, and breakdown voltage, which cannot be achieved with current transformer isolation technologies.

6.1 Benchmarks

The experimental setup and results in the Optocoupler Chapter determined the benchmark for the two optocoupler schemes, digital and analog. This section will synthesize the results to draw conclusions on the final benchmark for each scheme. The benchmark will be defined in each subsection because they are different for each scheme since the information that is being transmitted has unique characteristics.

6.1.1 Analog Topology Benchmarks

The benchmark for the analog topologies is determined by several factors: propagation delay, linearity from input to output, operation over temperature, and power consumption. To conclude this thesis this benchmark needs to be determined from the results presented in an earlier chapter. Something that needs to be noted is the subjectivity of this benchmark. For this thesis some figures of merit outweigh others. Here there is an interest in finding the benchmark with respect to the fastest, most linear analog topology. It is seen from the trend presented in the Optocoupler Characterization Experiments chapter that the power consumption increases as the propagation delay is decreased. If the power consumption figure of merit outweighed the importance of the propagation delay then the final benchmark will look different, thus the subjectivity of this benchmark. The final benchmark that is presented below is a great starting point for any design implementing these optocoupler topologies, but it should not be interpreted as the ultimate performance of these devices, but rather, the optimum performance in which these devices should operate when optimizing for the key parameters that have been chosen.

For the feedback analog topology using the chosen HCNR201 optocoupler the benchmark for the propagation delay for the analog optocouplers is shown right below 100 ns when the photodiode is biased to the maximum amount of about 60 µA and a voltage gain that is easily set by the two system resistors. This biasing corresponds to an input power consumption of 200 mW and an output consumption of 100 mW. This amount includes the power consumption of the op amp that is used in the design.

If the open-loop topology is used with the same optocoupler as in the feedback topology the propagation delay can be found to be below 280 ns but the transfer gain must be decreased to $0.6\,\frac{V}{V}$. The key here is LED current. Increasing this current by increasing the input voltage or decreasing the input LED resistance will decrease the propagation delay. A maximum of about 20 mA is achievable within the safe operating range of the optocoupler. At this point the propagation delay can be expected to be the same as the feedback topology, but it was shown that the output stage has to implement a larger feedback resistor than the feedback topology to have a comparable gain so the overall propagation delay is increased due to the op amp and overcoming the input threshold. The trade-off is a smaller power consumption of 65 mW on the output and zero on the input (excluding the input voltage biasing). In the linearity tests where the input is biased with a voltage that stays above the input threshold, the propagation delay is decreased to 100 ns or less when the smaller LED resistor is used – allowing for larger LED currents. This decrease in the propagation delay is due to the optocoupler operating in a properly biased regime. When the threshold has to be overcome the propagation delay is increased (as seen in the initial biasing test). The feedback analog topology does not have this problem because the input op amp forces the LED to be biased properly to allow the correct amount of current to flow through the input servo diode.

It will be seen in the digital optocoupler topology benchmark that the propagation delay is much smaller than the analog topologies. The speed is affected by the material and packaging of the optocoupler and the input and output stage. The optocoupler material is held constant but the input and output stage is changed dramatically with respect to propagation delays. This is what hurts the propagation delay, or speed at which these devices can operate. The fundamental optocoupler structure that is within the analog topologies is capable of having the same propagation delays and rise and fall times as the digital topologies because it is the same technology, but to have any linearity there must be circuitry around. Also, the low natural gains have to be boosted with large op amp gains causing issues with noise injection. If future technologies like GaN can increase the CTR the high gain in the op amps could be decreased.

The linearity is an important part of the benchmark because if it is bad the optocoupler topology will distort the transmission of the analog data. The output of the analog feedback circuit with the fast propagation delay of around 100 ns is linear between ±5% of nominal gain (unity) while the input servo diode current is around 20 μA. There is no limit on the input voltage to this circuit as long as the input current is kept below about 60 μA. When the input is below the 20 μA region the output starts to decrease to 75% of the input. This is still a decent linearity when compared with the non-feedback topology. The linearity of the non-feedback topology is first seen in the biasing tests as the CTR changes across different LED currents. The CTR is relatively stable within a 5% range until the LED current is increased past the nominal range where the CTR quickly doubles. As seen in the section discussing the propagation delay benchmark, the propagation delay is decreased when operating the LED at this high current level. When a sinusoidal input is applied it can be seen that operating in the region where the CTR doubles from its nominal value allows for the output to be linear to a ±5% region of the CTR value. This happens when the LED is biased above 16 mA. If the 110 Ω R_{LED} is used the propagation delay will

be around 100 ns, but the linear range is only 3 to 6 V. At 6 V the input current is up to around 50 mA, this is not a reasonable area to operate for long periods of time. With the 510 Ω R_{LED} the propagation delay decreases to around 200 ns but the input voltage range increases to an 18 V swing, from 7 V to 25 V. The CTR decreases all the way to 0.05% (an 83% decrease from the nominal gain in the linear region) at a slope of $0.1\frac{\%}{V}$ when the input bias is between 2.5 V to 7 V.

After defining the baseline performance of the propagation delay and linearity the operation over temperature must be identified to finalize the benchmark. For the feedback topology the temperature increases the propagation delay of the benchmark to 180 ns. The linearity is not changed due to temperature unless a larger R_{LED} is used. With a large R_{LED} the output voltage is cut off whenever the current through the LED causes the voltage across R_{LED} to cut-off the voltage across the LED, thus clamping the current even if the input voltage increases. The temperature affects the non-feedback topology by decreasing the overall CTR by about 8%. The linear range does not change because the CTR at each biasing point is shifted down. The propagation delay is generally increased with increased temperature, but not by as large as an amount as the feedback topology. Why is the effect of temperature on propagation delay different between the two topologies when, in both, only the optocoupler is heated? A possible reason is that in the feedback topology the optocoupler parameters change with temperature which effect the propagation delay of the input op amp because it is the feedback for that op amp, and in the non-feedback topology the changing parameters do not change the overall feedback of the op amp. Table 6.1 summarizes the benchmark for the different optocoupler topologies

Table 6.1 Summary of Analog Transmission Optocoupler Benchmark

	Feedback	Effect of Temp	Non-feedback	Effect of Temp
Propagation delay	100 ns	Increased about 100 ns	200 ns (R_{LED} needs to be larger to allow for larger region of linearity)	Increases are only around 20-40 ns
Linearity (±5% of nominal gain)	2 to 6 V (20 µA-60 µA photodiode current)	None (big effect if large R_{LED} is chosen)	7 to 25 V (16 mA-45 mA LED current)	None
Linearity below biasing range	25% of nominal value	None	83% of nominal value	None
Input Power consumption	200 mW	Increased by at least 6-8% (less CTR)	n/a	n/a
Output Power consumption	100 mW	Same	65 mW	Same

A conclusion can be drawn that if a proper supply is available the feedback analog topology has the best baseline performance. Not only is the propagation delay faster overall even when the temperature increases, the linear operating region is stiffer. The biasing might look like a wider region in the non-feedback when the input voltage is focused on, but the feedback topology input voltage can be increased if the input biasing resistor is increased. The best part about the feedback topology is that out of the ±5% region the linearity only changes by ±25%. This still allows the circuit to be useful while the non-feedback topology becomes completely useless outside of the linear region.

6.1.2 Digital Topology Benchmarks

The digital topology benchmark is slightly different than the analog topologies'. Propagation delay and power consumption, along with temperature operation play a large role, but linearity is not needed since this is digital device. Minimum pulse width replaces this which will determine, along with propagation delay, the baud rate these devices can achieve. The minimum pulse width is determined by

the minimum rise and fall time of the digital optocoupler output in response to an input change. It mostly has to do with proper biasing and output stage. A Schmitt trigger with hysteresis on the LED transistor pair could enhance the pulse width by decreasing the output voltage swing needed by the optocoupler output stage. This is done in the amplifier optocouplers and the effect can be seen to improve rise and fall times. The rails that the output must swing to for the LED and BJT pair optocoupler topology is to 10 V, the amplifier topologies only go to 5 V because that is the maximum operating power supply. The power consumption will be compared by simply doubling the amplifier topologies and the rise and fall times (ultimately the minimum pulse width) will be slightly compared by looking at slopes.

Because the output stage only needs to be turned on and off, it can be optimized to have extremely fast rise and fall times so the digital optocouplers have a propagation delay due only to the material of the optocoupler. The LED and BJT topology is not as optimized as a topology as the other ones so it will still have a good biasing range and propagation delay. The digital optocoupler temperature characteristics will determine the how the benchmark changes over increasing temperatures. Table 6.2 summarizes the benchmark for the different devices.

Table 6.2 Summary of Digital Optocoupler Transmission Benchmark

	LED BJT Pair		LED Amplifier Pair	
	HCPL4505 (GaAsP)	**HCNW4505 (AlGaAs)**	**ACPL071L (GaAsP)**	**HCPL7723 (AlGaAs)**
Operating Point	V_{in}=10 V R_{LED}=100 Ω R_{out}=1.5 kΩ	V_{in}=10 V R_{LED}=400 Ω R_{out}=1.5 kΩ	V_{in}=4 V R_{LED}=110 Ω	V_{in}=2 V
Propagation Delay	40 ns	100 ns	28 ns	24 ns
Rise Time	120 ns (83 $\frac{V}{\mu s}$)	700 ns (14 $\frac{V}{\mu s}$)	8 ns (625 $\frac{V}{\mu s}$)	20 ns (250 $\frac{V}{\mu s}$)
Fall Time	580 ns (17 $\frac{V}{\mu s}$)	1700 ns (6 $\frac{V}{\mu s}$)	8 ns (625 $\frac{V}{\mu s}$)	44 ns (114 $\frac{V}{\mu s}$)
Minimum Pulse Width	740 ns	2500 ns	44 ns	88 ns
Max Data Transmission	1.35 MBd	0.4 MBd	22.7 MBd	11.3 MBd
Input Power Consumption	n/a	n/a	n/a	30 (60 mW)
Output Power Consumption	35 mW	58 mW	15 (30 mW)	65 (130 mW)
Effect of Temp	Decreases speed by 35% at 70 °C	n/a	Decreases speed by 15% at 70 °C	Increases fall time and unstable at 70 °C

The first thing seen above is the GaAsP optocouplers have better baseline performance than the other material used, AlGaAs, with its smaller rise and fall times, and correspondingly smaller minimum pulse widths and max data transmission. The amplifier outputs obviously create the benchmark of 22.7 MBd and 15 mW of power consumption. Even when the power is scaled it is less than the LED and BJT pair. Even in the temperature operation the speed only decreases by 15%. Another thing to note is the easy implementation of these devices. The output just needs a 5 V supply and the input needs one input resistor to bias the input LED at about 20 mA.

The next step is to determine the benchmark for the current-mode optically-controlled Buck converter. What will the optocouplers limiting factors like linearity and minimum pulse widths have on

the overall system? The main factor for this is the maximum switching frequency allowed for the full system.

6.1.3 Current Mode Optically Controlled Buck Converter

The last section of the Current-mode optically controlled Buck converter chapter shows the waveforms of the experimental results that determine the maximum frequency of operation. As has been discussed and analyzed the maximum frequency is limited by the operation of the optocouplers. 140 kHz is the highest frequency that can be achieved. Although this frequency was easily accomplishable by the gate command circuitry with a 740 ns pulse width, the current sensing information has a much larger delay. There are two problems at play here. First of all noise injected in the circuit have caused a large propagation delay in the beginning due to a spike lasting 1 μs due to the switching MOSFET which the sensing circuitry and optocoupler transmission cannot respond too. As it has been stated before noise filtering was entered into the design at the point of measurement and then again at the output of the analog transmission circuitry, but this has not been good enough to filter noise over the very sensitive sensing circuitry. Also the optocoupler itself presents another 1 μs delay due to the propagation delay of the analog topology. This is larger than the benchmark set at 100 ns due to the introduction of a larger R_{LED} to dampen the oscillations in the circuitry at steady state.

The biggest lesson learned from implementing these optocouplers into a real circuit is their sensitivity. It can be seen the length at which the design process took to characterize the different optocouplers and determine how they can used stably in the Buck converter system compared to the poor results of a switching frequency of 140 kHz. A lot of this is due to the complexity of designing around the naturally low gains of the optocoupler. Because of these low natural gains, due to the small CTR parameter, the topologies have to introduce high gains with large resistors in the feedback of optocouplers. This has two main problems. One problem is that large resistors are very susceptible to

EMI which generate voltage drops by inducing small amounts of current (tens of micro-amps) through the resistor. The other problem is that the biasing current is only tens of micro-amps so it is also very easy to distort. For the benchmark to be reached in a real system very good noise filtering needs to be applied. This would be very complex and possible future research into optocoupler analog applications.

6.2 Future Work

The future work can be broken down into two parts, research into other ways to implement optocouplers into power systems and ways to enhance the fundamental optocoupler and the circuits around them.

There are many other areas optocouplers can be implemented into power systems. One is in the actual gate control of MOSFET's in a half- or full-bridge topology. If enough gate voltage potential could be directly transmitted to the gates of the MOSFET's then there would not be a need for bootstrapping because the potential could be referenced to any node in the circuit, and unlike bootstrapping there would be isolation created as large as the withstanding voltage of the optocoupler. The area for research in this topic would be increasing rise and fall times because of how much that adds to the pulse width of a signal being transmitted. As seen in the benchmark conclusion, it can be upwards of 50% more pulse width.

This idea of transmitting information along with energy (charging the gate of a MOSFET) leads into a second area of research for implementing optocouplers into other areas of power systems, to create isolated power supplies in small footprints with high efficiency. Something not looked at in this thesis was the photovoltaic mode of operation for an optocoupler. This mode operates the output so that it supplies energy. This is the same concept as modern solar cells. The main problem for this topic of study is efficiency of energy transfer. Since CTR is so incredibly low the power on the output will be a factor of CTR less than the input. And in this case a BJT cannot be used to increase this CTR by a factor of

β. There have been vast improvements in efficiency of commercial solar cells but to scale that down into the footprint of an optocoupler package is not a small task.

As stated earlier the dynamic characteristics of the optocoupler are not modeled in any simulation environment. This owes itself to the small uses the optocoupler has played thus far in the critical path of transmitting system variables to control a particular system. A simple static model with a current controlled current source can be used to simply model digital transmission, but for the analog transmission the CTR non-linearity and propagation delays present have large impacts on the overall system. For continued research on the subject of the optocoupler transmitting information on a critical path this needs to be remedied. Future work in this area could apply the dynamic characteristics derived by the experiments conducted in this thesis into a comprehensive model for the optocoupler.

Another area of future work is in the optocoupler material. GaN has been discussed multiple times in this thesis. There is obviously a need for optocouplers that can operate with more linearity and speed. GaN can be bring the improvements needed in increased CTR parameter in better matched and efficient LED and photodiode pairs and the rise and fall times needed to increase the overall baud rate. Something to continue researching is topologies to increase certain aspects of the key parameters presented in this thesis. With more circuitry can there be enhanced linearity and shorter propagation delays over temperature and biasing?

There is much more room in this area of research to innovate optocouplers enough so that they can replace the current transformer and increase power density by decreasing size, increase operating temperature, and increase switching speeds. This thesis has been a study into where the technology is at now and how it can be improved for future use.

7 REFERENCES

[1] Ned Mohan, Tore M. Undeland, and William P. Robbins, *Power Electronics*, 3rd ed., Bill Zobrist, Ed. Hoboken, NJ: John Wiley & Sons, Inc., 2003.

[2] Yuhui Chen, F.C. Lee, L. Amoroso, and Ho-Pu Wu, "A resonant MOSFET gate driver with complete energy recovery," in *Power Electronics and Motion Control Conference, 2000. Proceedings. IPEMC 2000. The Third International*, vol. 1, 2000, pp. 402- 406.

[3] Jonathan Adams, "Bootsrap Component Selection For Control IC's," International Rectifier, El Segundo, Design Tip DT 98-2a 2001.

[4] John F. Dickson, "On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 3, pp. 374-378, June 1976.

[5] Texas Instruments, Inc., "Digital Isolator Design Guide," Texas Instruments, Inc., Dallas, Design Guide 2009.

[6] Ben G. Streetman, *Solid State Electronic Devices*, 4th ed., Alan Apt and Jow Scordato, Eds. Englewood Cliffs, NJ: Prentice-Hall, Inc., 1995.

[7] Vishay Intertechnology, Inc., "IL300 Linear Optocoupler," Vishay Semiconductor, Datasheet 2011.

[8] P. Vettiger, "Linear Signal Transmission with Optocouplers," *Solid-State Circuits, IEEE Jounral of*, vol. 12, no. 3, pp. 298-302, June 1977.

[9] Vishay Intertechnology, Inc., "Optocoupler Common Mode Transient Immunity (CMTI) - Theory and Practical Solutions," Vishay Semiconductor, Application Note 83 2003.

[10] Agilent Technologies, "Agilent HCPL-7723 and HCPL-0723 High Speed CMOS Optocoupler," Agilent Technologies, Datasheet 2005.

[11] Avago Technologies, "ACPL-071L and ACPL-074L Single-channel and Dual-channel High Speed CMOS Optocoupler," Avago Technologies, Datasheet 2011.

[12] Avago Technologies, "HCNR200 and HCNR201 High-Linearity Analog Optocouplers," Avago Technologies, Datasheet 2008.

[13] Hewlett Packard, "HCPL-4504 and HCNW4504 High CMR, High Speed Optocouplers," Hewlett Packard, Datasheet.

[14] Simon Ang and Alejandro Oliva, *Power-Switching Converter*, 2nd ed. Boca Raton, FL: CRC Press

Talyor and Francis Group, 2005.

[15] Unitrode Corporation, "Modelling, Analysis, and Compensation of the Current-Mode Converter," Texas Instruments, Inc., Application Note U-97 1999.

[16] B. Jayant Baliga, *Fundementals of Power Semiconductor Devices*. New York, NY: Springer, 2008.

[17] I.D. de Vries, "A resonant power MOSFET/IGBT gate driver," in *Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE*, 2002, pp. 179-185.

[18] Cree, Inc., "CMF20120D-Silicon Carbide Power MOSFET (Z-FET MOSFET)," Cree, Inc., Durham, Datasheet 2011.

[19] International Rectifier, "IRLML2030TRPbF HEXFET Power MOSFET," International Rectifier, El Segundo, Datasheet 2009.

[20] Maxim Integrated Products, "MAX15018A Half-Bridge MOSFET Driver," Maxim Integrated Products, Sunnyvale, Datasheet 2008.

[21] Diodes Incorporated, "ZLLS2000 40V High Current Low Leakage Schottky Diode," Diodes Incorporated, Datasheet 2010.

[22] Maxim Integrated Products, "MAX4450 Single Supply Op Amp with Rail-to-Rail Outputs," Maxim Integrated Products, Sunnyvale, Datasheet 2000.

[23] D.A. Williams, "Optocoupler selection for high frequency power supplies," in *Applied Power Electronics Conference and Exposition, 1995*, 1995, pp. 90-95.

[24] Supertex, Inc., "HV9123 High-Voltage, Current-Mode PWM Controller," Supertex, Inc., Sunnyvale, Datasheet 2008.

[25] Cree, Inc., "C3D10060A–Silicon Carbide Schottky Diode Z-REC Rectifier," Cree, Inc., Durham, Datasheet 2009.

[26] Abracon Corporation, "Thru-Hole Drum Core Power Inductors AIRD-03," Abracon Corporation, Rancho Santa Margarita, Datasheet.

[27] Song Liu, "Selection of Three Locations of Current Sense Resistor in Buck Converter," Alpha and Omega Semiconductor, Shanghai, Application Note PIC-007 2008.

[28] Maxim Integrated Products, "Optocoupler Extends High-Side Current Sensor to 1kV," Maxim Integrated Products, Application Note 1867 2003.

[29] Maxim Integrated Products, "MAX4172 High-Side Current-Sense Amplifier," Maxim Integrated Products, Datasheet 2010.

[30] Unitrode Corporation, "Practical Considerations in Current Mode Power Supplies," Texas Instruments, Inc., Application Note U-111 (SLUA110) 1999.

[31] Christophe Basso, "Ramp Compensation for the NCP1200," Semiconductor Components Industries, LLC, Application Note 8029/D 2001.

[32] Ridley Engineering, Inc., "An Accurate and Practical Small-Signal Model for Current-Mode Control," Ridley Engineering, Inc., Current Mode Control Modeling Application Note 1999.