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Design of an 866 MHz On-chip Frequency Synthesizer

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DESIGN OF AN 866 MHz ON-CHIP FREQUENCY SYNTHESIZER

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A thesis submitted in partial fulfillment
of the requirements for the degree of
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By

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Abstract

There is a strong need for stable frequency references with large tuning ranges in today's communication systems. While the crystal oscillators assure good frequency stability, it is not possible to achieve a large frequency range by tuning the passive components attached to them. Frequency synthesizers are usually used for this purpose because of their ability to produce a variety of output frequencies. The Phase Locked Loop (PLL) based frequency synthesizer is the most preferred of all types of synthesizers available because of its additional features like programmability, low noise and low cost as well as high accuracy and stability. The main idea of this PLL-based synthesizer is to phase-lock its output signal with an input reference signal and to produce a synchronous output. It does this by generating an error signal to correct the oscillator frequency. This functionality is achieved by integrating a phase detector, charge pump, loop filter and voltage controlled oscillator block in series with a frequency divider in feedback.

This thesis presents, in detail, the design of all the individual PLL blocks, the strategies employed in the design, issues faced in testing and the test data from simulation and measurement. All the above mentioned PLL blocks are designed in the 130 nm IBM-CMOS cmrf8sf process and optimized for low power consumption. PLLs are used in almost all kinds of communication systems, transmitters and receivers for applications such as carrier recovery, carrier generation, clock slew correction, frequency modulation and demodulation.

This thesis is approved for
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Graduate Council

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Finally, this work would not have been possible without the constant support and help of my beloved parents and my family members who always believed in my ability. I owe them big time for inculcating in me the qualities required to be successful in my career.

Dedication

I dedicate this work to my beloved parents Sri. Achuta Bhat Joshi and Smt. Krishnaveni. You both are my source of inspiration since my childhood. You are the very reason behind where I stand today. Thanks for all your love, affection and support. Love you maa and papa.

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Chapter 1

Introduction

In earlier days LC based tuned oscillators were used as the main source of frequency generation. This LC tank circuit resonates at a particular point generating a fixed frequency. These tuned oscillators had to be adjusted manually to change the resonating frequency of the LC circuit. The main drawback of these tuned oscillators is that they are very susceptible to frequency drifts with change in temperature and aging. As such, they could not be used in frequency sensitive applications such as military and satellite systems [1].

Crystals were the next generation of oscillators, which operate by converting mechanical vibrations to oscillation frequency. These use quartz crystals as the main element. Because of the nature of their frequency generation these oscillators are very immune to thermal noise. Hence, they can produce a very stable output frequency. But, the disadvantage of using these oscillators is each crystal can only produce a single output frequency. Therefore, multiple crystals would be required for varying frequency, which is not a viable option in integrated circuit applications. Also, this is impractical in applications like coherent detection which require a large range of frequencies. In coherent detection, the incoming carrier acts as the reference frequency to the internal oscillator and the oscillator generates the output signal in phase with the incoming input reference. Therefore, it would be required to use multiple crystals to tune to different input frequencies making the crystal oscillators unfit in these kinds of variable frequency applications [1].

The frequency synthesizer is a general solution to all of the above mentioned issues. The frequency synthesizer, as the name implies, is capable of generating a variable output frequency

by synthesizing its inputs. Although there exist a variety of synthesizers, the phase locked loop based frequency synthesizer is widely used for on-chip applications because of its low power consumption and very low phase noise. The phase locked loop (PLL) helps in synchronizing the phase of the oscillator-generated signal with the input reference signal. The PLL internally generates an error signal which is fed to the Voltage Controlled Oscillator (VCO) to fine tune its phase and frequency to be in sync with the input reference. Hence, the PLL-based synthesizer tunes itself to any incoming input frequency thus functioning as a variable frequency generator. The synthesizers used in tuned radio receiver circuits and almost all the communication systems are based on this PLL logic.

This thesis presents an 866 MHz on-chip PLL-based frequency synthesizer block design consisting of a phase frequency detector, charge pump, loop filter and frequency divider. It also shows integration with the voltage controlled oscillator (VCO) designed by Kacie Woodmansee, a fellow MSCAD lab student. It is designed to be part of a future 12 channel wireless transceiver network in the 433 MHz frequency band and serves the purpose of providing a stable reference oscillator signal to the rest of the circuitry. This wireless transceiver has been designed for medical, mobile and sensor network applications and is implemented in the 130 nm IBM-CMOS process. It consumes very low power, i.e. measured to be about 2.89 mW from simulations, and it is capable of running over the temperature range of -55 ˚C to 125 ˚C.

The wireless transceiver acts as a communication interface between an external base station and the on-chip digital data processor. In detail, the transceiver has a transmitter and receiver on-chip with an antenna attached on one of its ends. The receiver acquires the data wirelessly from the base station and it processes and converts this data into a digital format and hands it over to the digital portion of the chip for further processing. Likewise, the transmitter

receives the data or commands from the digital portion of the chip, converts it into analog form and does signal conditioning so that it can be transmitted wirelessly to the base station. The DSP core and microcontroller compute the received digital converted data inputs from the various sensor interfaces such as pressure sensor, EKG sensor and batter voltage sensor.

The following block schematic in Figure 1.1 shows the architecture of the wireless transceiver chip in this context.

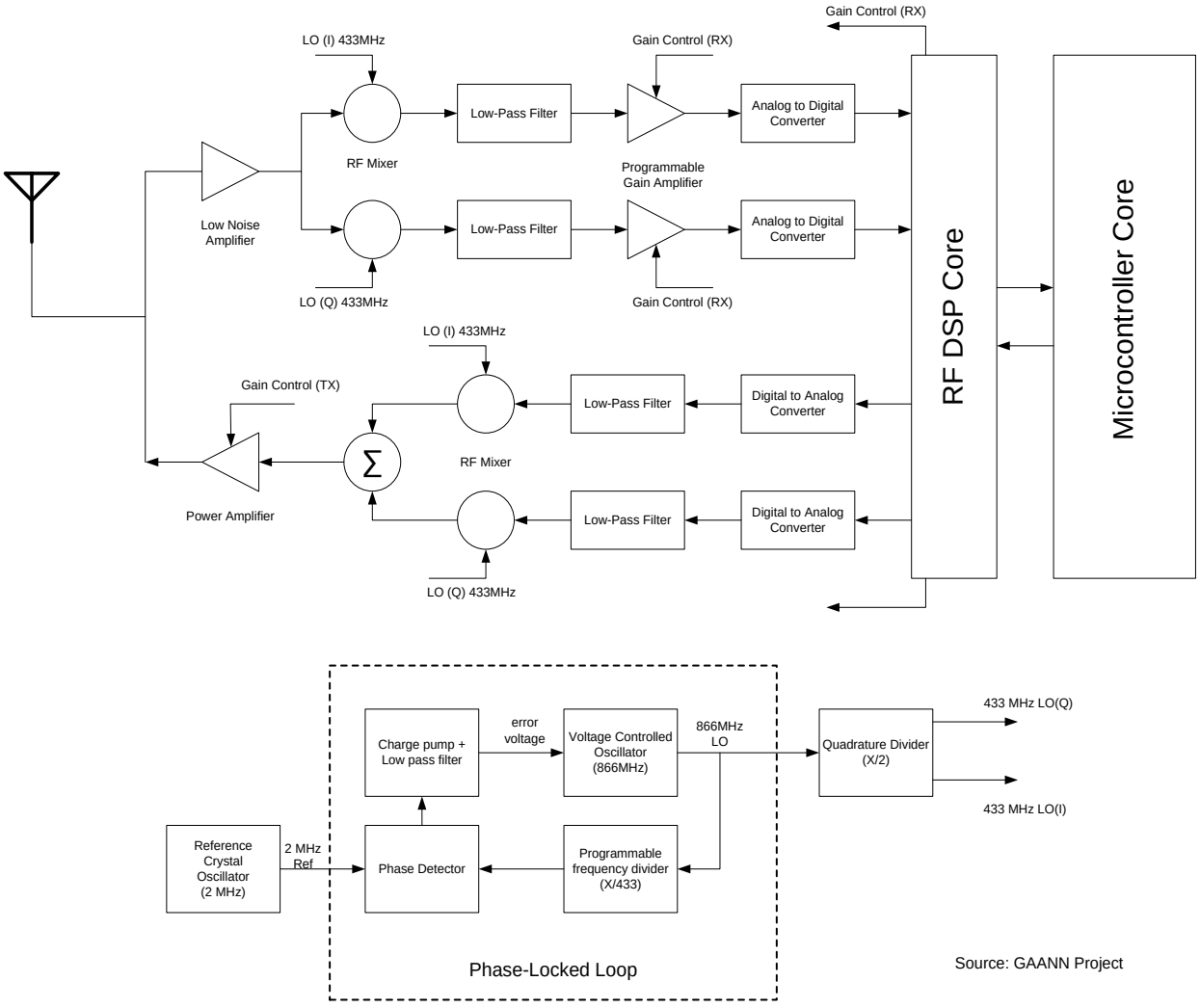

Figure 1.1. GAANN wireless transceiver architecture diagram

The rest of the thesis is organized in the regular systematic way of circuit design, simulation results obtained in the Cadence design system, followed by bench testing results. Chapter 2 discusses the overview of frequency synthesizers, different synthesizer architectures and a working logic of the PLL-based synthesizers. Then Chapter 3 introduces the topologies used for design and strategies employed for the synthesizer blocks designed in this context. Also, it presents a detailed circuit working logic description along with the simulation data gathered. Chapter 4 talks about integration of all of the PLL blocks, simulation data of the integrated PLL and the integration issues addressed. In addition, it presents the layout design considerations of each of the blocks and the integrated PLL. Finally, Chapter 5 discusses PCB test board design and the results obtained from bench testing. The thesis concludes with future work that needs to be done in Chapter 6.

Chapter 2

Frequency Synthesizers Overview

The frequency synthesizer is a variable oscillator which can generate a variety of frequency combinations. Frequency synthesis is the process of mixing two frequencies. The synthesizer utilizes division, multiplication and mixing operations to generate the desired output.

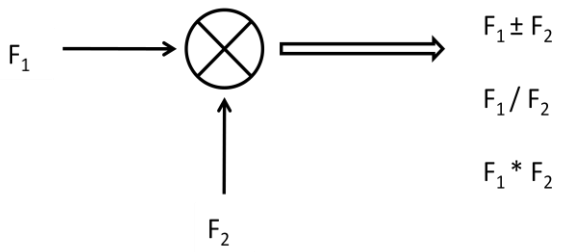

Figure 2.1. Synthesizer Block Diagram

In high frequency applications, it is very difficult to generate multiples of GHz frequencies using a standalone oscillator but, the synthesizers are able to generate high frequencies using the low frequency inputs by frequency multiplication or frequency mixing. Therefore, they are of great use in these kinds of applications [1].

2.1 Overview of Frequency Synthesizers

Synthesizers are broadly categorized into three types. The architecture details of these three categories are as mentioned below [2].

2.1.1 Direct Frequency Synthesizers: These types of frequency synthesizers use a set of standard stable input reference frequencies as the inputs. To generate higher frequency outputs from the given set of discrete frequencies a multiplier is used. The filter then separates out the

unwanted frequencies from the multiplier output leaving the required output frequency. The general block diagram of direct frequency synthesizer is as shown in Figure 2.2 [2]. The main advantages of this architecture are its fast frequency switching and very low phase noise. Also, it maintains the stability of the input references in the generated output signal. Usually it is used in applications which require higher frequencies than the input reference. But, it quickly gets large by requiring too many input references for a range of frequencies. So these are obsolete in the present day synthesizer market.

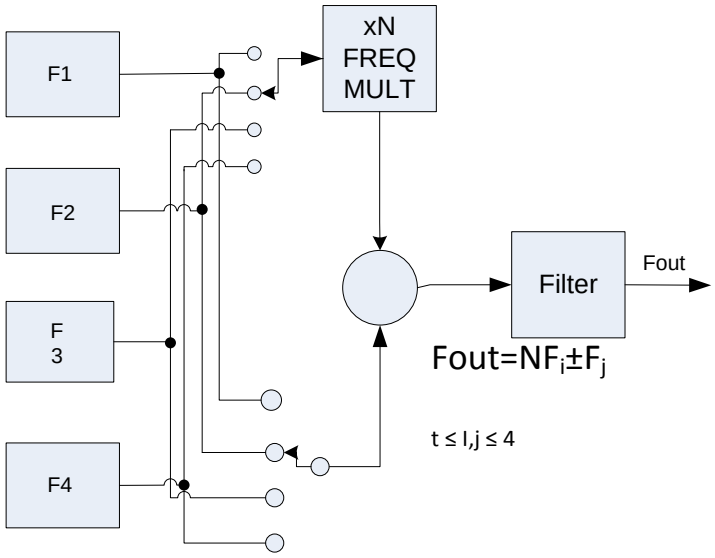

Figure 2.2. Direct Frequency Synthesizer block diagram [2]

2.1.2 Direct Digital Synthesizers: These are purely digital synthesizers. They consist of an accumulator, memory and a DAC. An external system is used to supply the input digital commands to kick start the operation. The accumulator generates a set of pulses upon receiving the digital input commands from the system and stores them in a read only memory. These pulses will be fetched and fed to a DAC to generate an equivalent analog output signal [2]. These kinds of synthesizers are quite flexible and easy to handle. But, they are too noisy in their operation as they are completely digital in nature.

2.1.3 Indirect Frequency Synthesizers: These are further categorized into two types, namely analog indirect synthesizers and digital indirect synthesizers [2]. These kinds of frequency synthesizers work on the principle of phase locking. They include a phase detector, charge pump, loop filter, frequency divider and voltage controlled oscillator as their core blocks.

In analog indirect synthesizers frequency acquisition is done by coarsely tuning the voltage controlled oscillator to be near the required locking frequency [2]. An analog multiplier is used as the phase detector in these synthesizers. A notable thing in these kinds of synthesizers is they do not employ a frequency divider in the feedback for self-frequency tuning as can be seen in Figure 2.3. On the other hand, digital PLLs contain a digital phase detector and a frequency divider in the feedback path. These synthesizers accomplish phase locking by varying the divider ratio digitally. A digital PLL-based synthesizer is a common example of digital indirect frequency synthesizers.

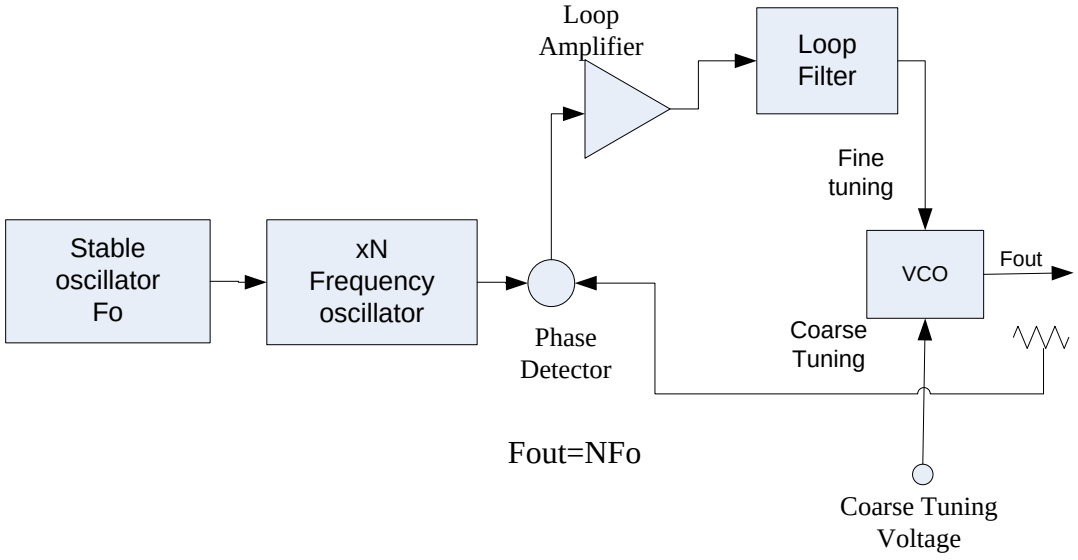

Figure 2.3. Analog indirect frequency synthesizer block schematic [2]

The digital indirect frequency synthesizers achieve a channel spacing equals to or a fraction of the input reference frequency by incorporating a programmable divider in the feedback loop. It should be kept in mind that the output phase noise is greatly dependent on the divider ratio. Hence, it should be kept as low as possible for better synthesizer performance.

The main advantages of indirect frequency synthesizers are that they occupy much less space, consume less power and filter out the spurious signal components with the help of a low-pass filter. The disadvantages of using them include longer settling time and more noise [2]. As it has to tune itself to a new frequency when the divider ratio is changed, it takes a decent amount of time to settle to a new frequency. The settling time can be brought down to a better level by increasing the charge pump current supplied to the loop filter. So the more current that is supplied, the lower the settling time of the synthesizer. The divider in the feedback path is the main source of noise injected into the loop.

An indirect digital synthesizer has been chosen for this project because of its simplicity and relevance to the application. Here, it is required to switch between twelve channels in the 433 MHz frequency range, each with a 2 MHz channel spacing which is equal to the crystal input reference frequency. The power consumption is reduced by decreasing the charge pump bias current and avoiding the short circuit power at the cost of increased settling time. The noise level is brought down by proper loop filter design.

2.2 PLL-based Frequency Synthesizers

The PLL-based frequency synthesizer is an example of digital indirect frequency synthesizers. These synthesizers generate the oscillation in phase with the input reference

frequency. They are broadly classified into two types, namely integer-N and fractional-N frequency synthesizers.

In the integer-N type, the output frequency is always an integer multiple of the input reference frequency, where as the fractional-N synthesizer can have a fraction of the input reference frequency at its output [3-5]. The fractional-N synthesizer achieves this by changing its divider modulus in a regular fashion so that the effective average divider ratio can result in the required fractional frequency output. The divider modulus is varied by using a variety of methods in fractional synthesizers namely phase interpolating, pulse swallowing, random jittering and ΔΣ fractional-N synthesizing method [3].

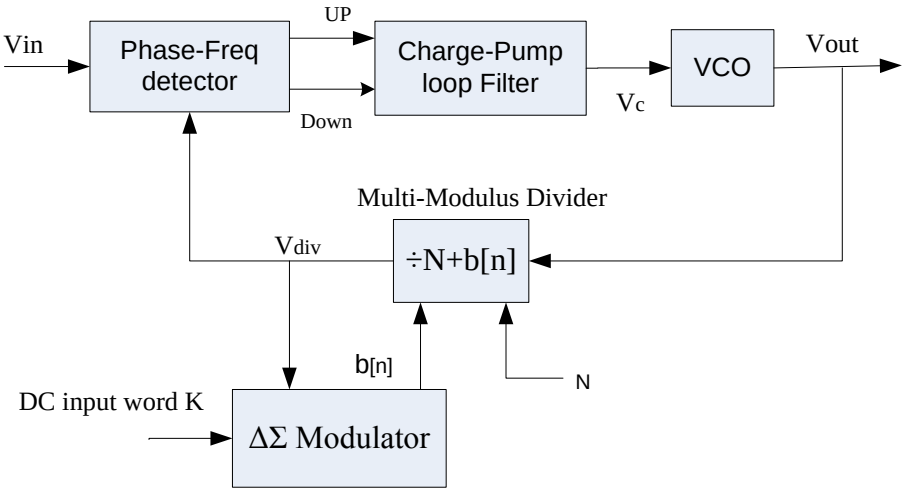

Figure 2.4. ΔΣ modulator based fractional-N frequency synthesizer [4]

Figure 2.4 shows an example of a fractional-N frequency synthesizer implementing the ΔΣ modulator in its feedback for varying the divider ratio [4]. The required divider ratio to obtain the fractional frequency output is used as the integer DC input word. The input word will be encoded by the modulator and fed to the multi-modulus divider to obtain the required

fractional frequency [4]. The process of encoding the DC input word involves a quantizer, which adds quantization noise to the encoded output resulting in more phase noise and jitter at the output frequency spectrum [3-5]. It consumes comparatively less power because of its low modulus divider ratio.

On the other hand, the integer-N synthesizer includes a simple regular programmable divider in the feedback path as shown in Figure 2.5. It consists of a phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO) and frequency divider. The PFD compares the phase of the input reference signal (F_{REF}) with the frequency divided signal (F_{DIV}) and generates a difference signal at the output. The difference signal feeds into the charge pump which will source or sink the equivalent current to the loop filter. The loop filter, with its RC elements, converts the incoming current into an error voltage and feeds it into the VCO. The error voltage varies the varactor capacitance (in LC oscillators) thus tuning the VCO frequency.

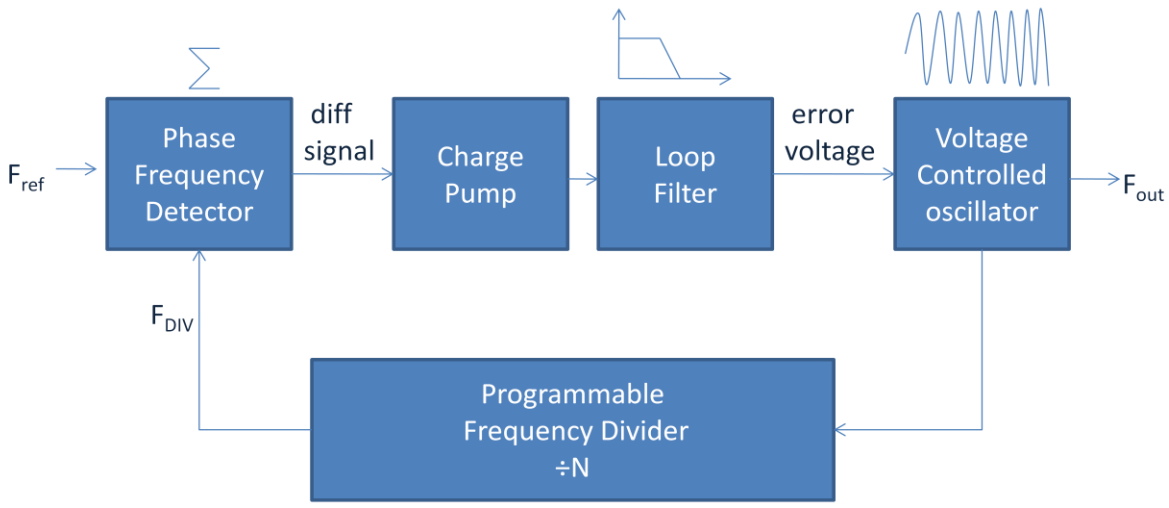

Figure 2.5. PLL based synthesizer block diagram

2.3 How a PLL Works as a Synthesizer

For a PLL to act as a frequency synthesizer, it should be able to vary its output frequency. This can be done in two ways: using a programmable frequency divider or varying the input reference frequency.

Consider the case of a programmable frequency divider with fixed input reference frequency seen in Figure 2.6. A 500 MHz PLL would produce sustained oscillations with a 500 MHz VCO, a divide-by-500 divider and a 1 MHz input reference signal. If a 600 MHz frequency is required at the output, then it can be done by varying the divider ratio from divide-by-500 to 600.

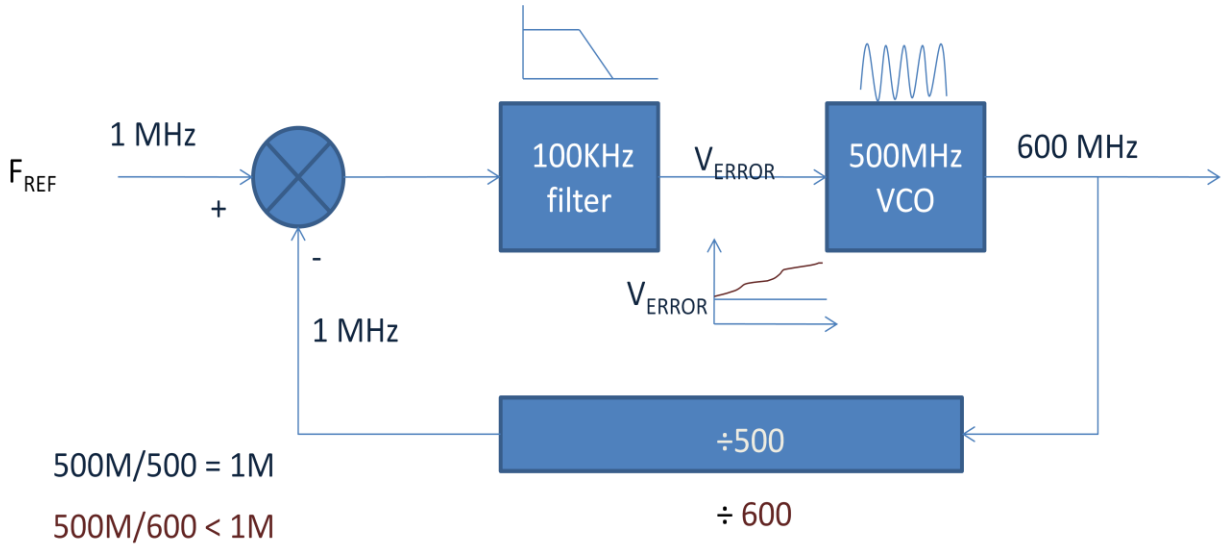

Figure 2.6. Illustration of how a PLL acts as a synthesizer

The divide-by-600 divider with 500 MHz VCO would produce a signal which is less than 1 MHz in frequency. This signal, when compared with the 1 MHz input reference signal, would generate a positive difference signal and thus, a positive control voltage to the VCO. This control

voltage corrects the VCO frequency in a way that would reduce the difference between the two input signals at the PFD. In turn, that would reduce the error control voltage fed into the VCO and thus the difference in phase of the PFD inputs. Eventually, within the transient settling time, the VCO would tune itself to 600 MHz and the PLL will be locked at 600 MHz.

2.4 Applications

PLL-based frequency synthesizers are found in almost all types of communication circuits. These synthesizers are used mainly in mobile transceivers, satellite transceivers, AM/FM radio receivers, automatic frequency controls (AFC), Doppler correction, walky-talky's and GPS systems for frequency detection, frequency generation and frequency demodulation. These find use in radar, military, aerospace and satellite applications.

Chapter 3

PLL block design in 130nm IBM-CMOS Process

The frequency synthesizer blocks, namely a phase-frequency detector (PFD), charge pump, loop filter and a frequency divider are designed in the 130 nm IBM-CMOS process for the wireless transceiver chip. The design detail of the each individual block is mentioned below.

3.1 Tristate Phase Frequency Detector

A tristate PFD is an asynchronous sequential digital logic block which compares the phases of two incoming signals and generates an error signal. The sequential phase detector is a digital block and it usually consists of D Flip-Flops (DFF) and NAND gates. The advantage of using sequential phase detectors over traditional analog phase detectors is that they possess the capability of detecting any difference in input frequency along with phase [8]. They do this by generating an error pulse signal on one of its outputs whenever a frequency difference exists at the input.

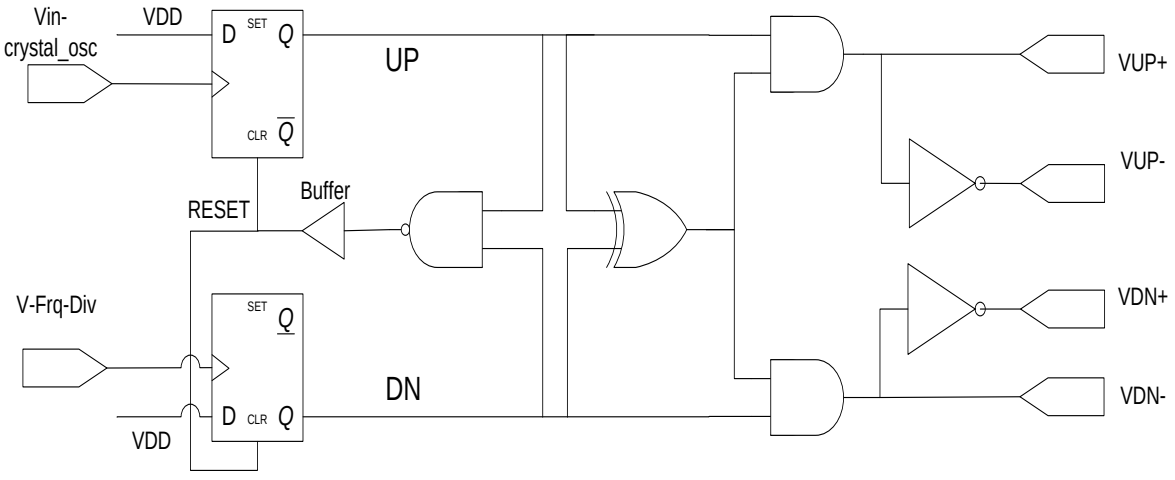

Figure 3.1. Tristate PFD schematic

A variety of PFD architectures are proposed in the literature such as a dual-slope PFD for fast locking [12], using a modified D-latch in a PFD for improved phase frequency sensitivity [13] and a high-speed capable PFD[17]. A simple low power, dead-zone protected and spur-free tristate PFD has been chosen for this project to meet the design specifications. It has been designed using the 130nm IBM-CMOS process. Figure 3.1 shows construction of the PFD designed for this project [6-14].

3.1.1 PFD Circuit Design

The two DFF's along with the NAND gate and buffer perform a phase comparison, while the XOR and two AND gates help in suppressing sudden impulses. Whenever the crystal oscillator signal leads the frequency divided signal, an error pulse signal appears on the UP rail. Similarly, whenever the crystal oscillator signal lags the frequency divided signal, an error pulse signal appears on the DN rail. The waveform below illustrates the working logic of the PFD.

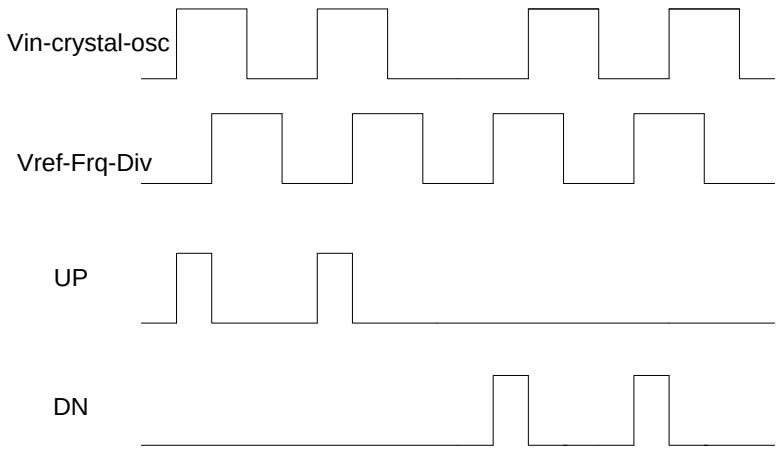

Figure 3.2. PFD sample output graphs

Whenever the two input signals are in-phase, both UP and DN rails go logic high. Then the NAND gate turns on and resets both the DFF's. This is known as the stable locked state of operation of the PFD. Without the buffer in the reset path, the PFD runs the risk of falling into the dead-zone. When the synthesizer is in lock mode, i.e. the Vin-crystal-osc and V-Frq-div are in phase, any minute phase variation in either of the two inputs having a time period less than the propagation delay of the circuit would not appear at the output and will be reset. Therefore, the synthesizer cannot automatically correct the frequency of the VCO to nullify the error and thus, it runs with this constant phase error. This is called the dead-zone, and this problem would be solved by adding an extra buffer element in the RESET path [8].

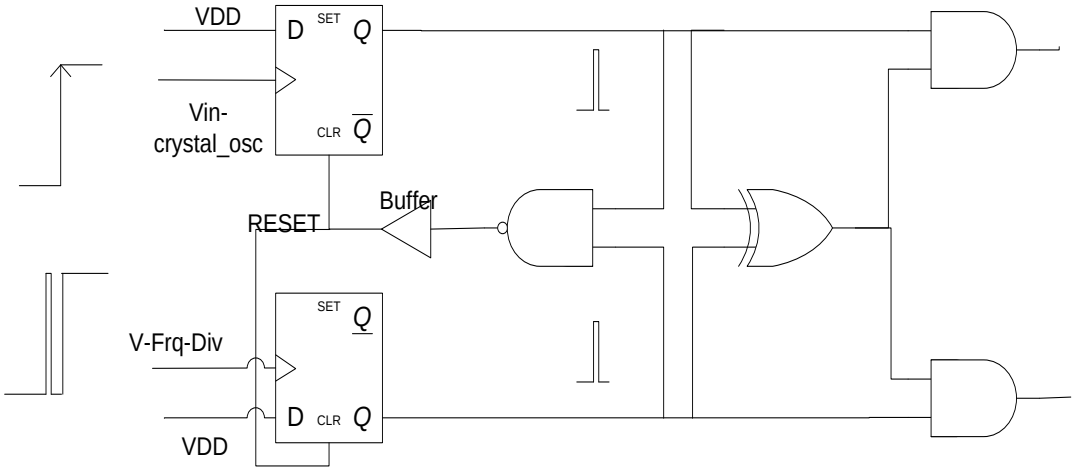

Figure 3.3. PFD with input falling in dead-zone and out spikes

But, this extra buffer element has the disadvantage of limiting the maximum frequency of operation of the PFD which is about 2.9 GHz in this case [8-9]. The maximum operating frequency of the PFD is related to the propagation delay as

The maximum operating frequency of PFD = 1 / (propagation delay of complete reset path)

$$\sim \quad 1 / (200p + 54p + 90p)$$

$$\sim \quad 2.90 \text{ G Hz}$$

The PFD enters locked stable condition when the two inputs are in phase. Any sudden variations on the UP or DN output rails of the PFD output would result in unwanted sourcing or sinking current in the charge pump. It varies the VCO control voltage consequently disturbing the stable oscillation frequency of the synthesizer. The XOR gate helps in suppressing these impulse variations which have a time period that is less than the propagation delay of the XOR gate [8-9].

If a spike appears on both the UP and DN rails simultaneously, then it would cause the current source and current sink in the subsequent charge-pump stage to turn on at the same time. This results in a direct path between the power supply and ground in the following charge pump stage drawing huge amounts of short circuit current. The XOR AND gate combination help in avoiding this by suppressing the spikes on the UP and DN rails [8]. Also, when in the idle state, the PFD runs in high-impedance mode consuming a negligible amount of power. Therefore, this tristate PFD is well optimized for low power operation. The simulated power consumption is calculated to be about 40 μW.

3.1.2 Simulation Results

The graph in Figure 3.4 shows the simulated output waveform of the tristate PFD. From the graph, it can be observed that when the crystal oscillator signal is leading the divider output a pulse appears on the UP rail. Likewise, a pulse on the DN rail appears when the crystal input is lagging the divider output.

Simulating change in operating temperature has very little effect on the working of the PFD. When the temperature increases as high as 125 ˚C there is only a 6 µV increase in the average output voltage of the PFD which would not have any significant effect on the operating region of the subsequent charge pump stage. Hence, the change in temperature has very little effect on the operation of the PFD and the subsequent charge pump stage. Figure 3.5 below shows the change in average PFD output with respect to the change in temperature.

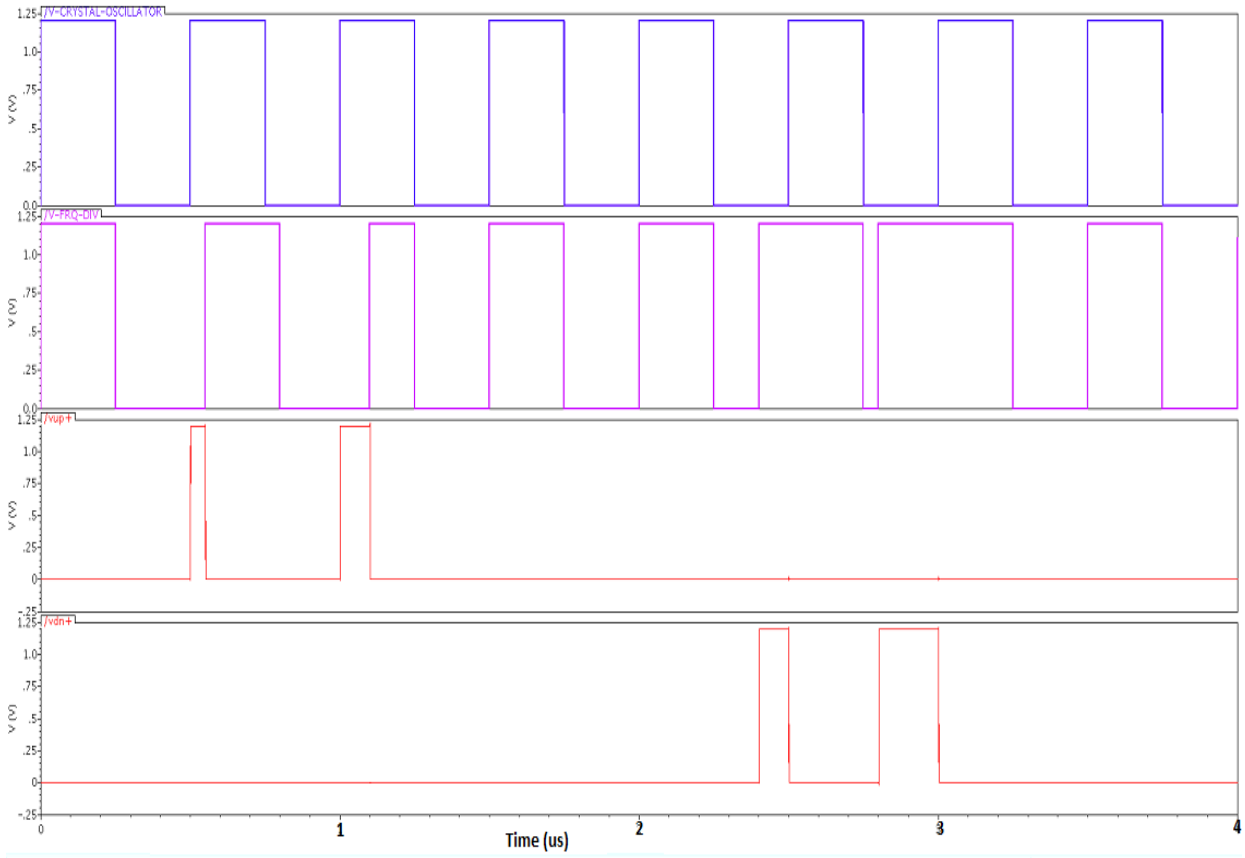

Figure 3.4. Tristate PFD output waveform

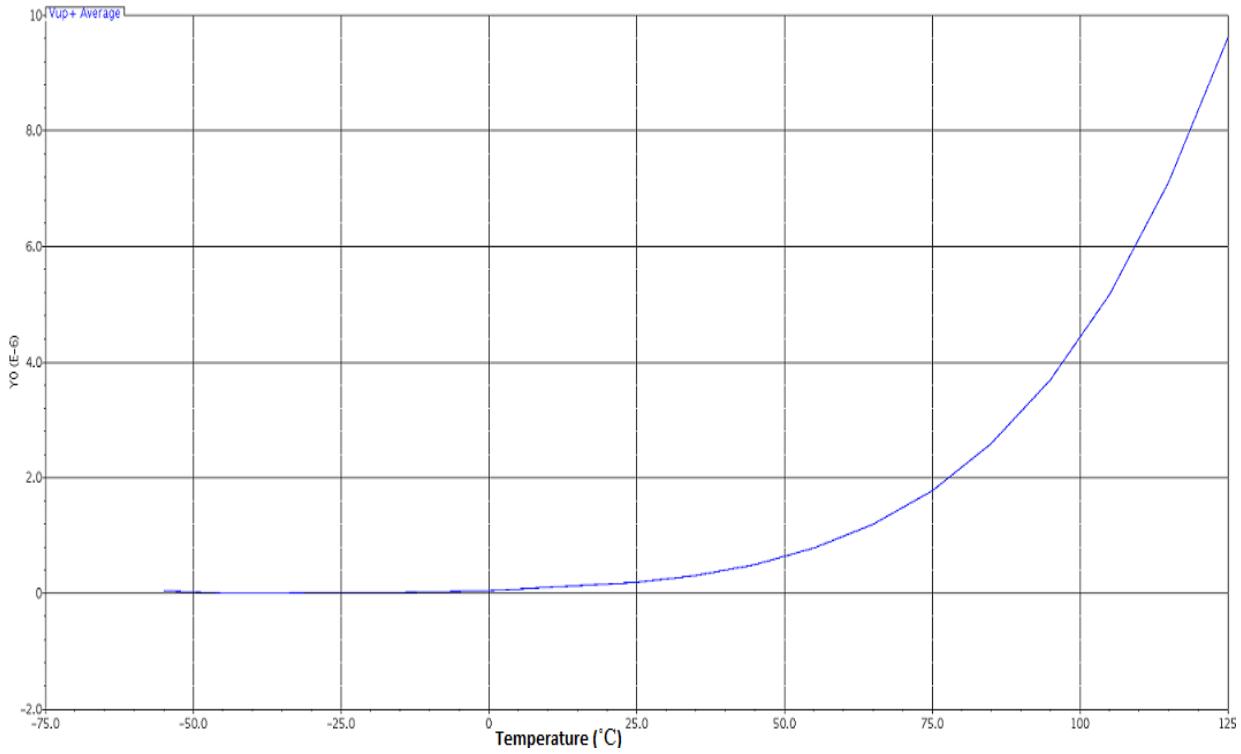

Figure 3.5. Change in average PFD output with temperature

The average PFD output varies linearly with the input phase variation. The average output voltage of the PFD increases linearly with the increase in input phase difference and drops off suddenly at the end of the clock cycle i.e. when approaching 360˚ phase difference of the subsequent clock cycle. The increase in average PFD voltage increases the following charge pump stage's driving current and thus the produced VCO control voltage. The simulated phase sensitivity curve of a 2 MHz (0.5 µs period) input signal for four clock cycles is as shown in the graph in Figure 3.6.

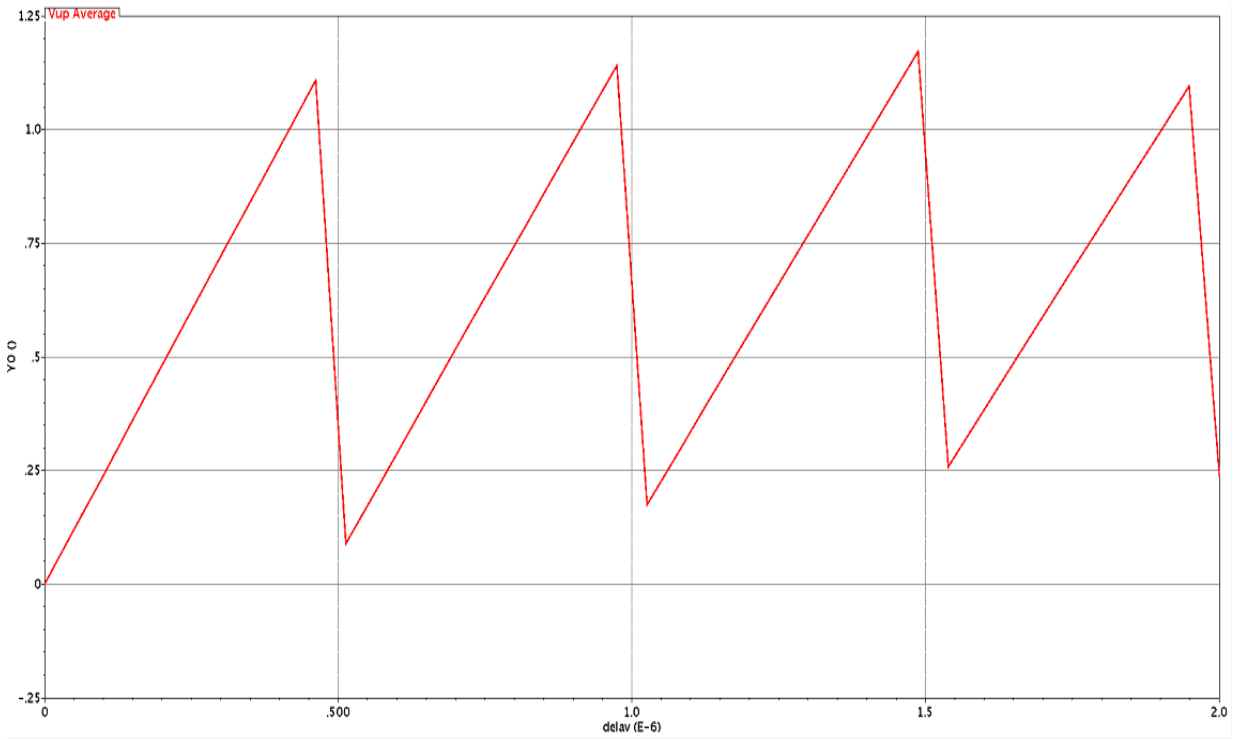

Figure 3.6. Phase sensitivity plot of PFD

Table 3.1 summarizes the design parameters of the tristate PFD as designed.

Table 3.1 PFD Design Parameters

Parameter	**Value**
Reference input	2 MHz
Frequency divided input (866 M/433)	2 MHz
PFD bandwidth	2.9 GHz
Power consumption	7 µW
Dead zone protection	Yes
Spur sppression	Yes

3.2 Differential Charge Pump

The charge pump controls the current flowing into and out of the loop filter. It consists of a current source and a current sink, which are controlled by the incoming error pulse signal generated by the PFD. Figure 3.7 shows the block schematic of a simple current amplifier based charge pump [8-9]. Whenever an error pulse is generated on the UP rail at the PFD output, it triggers the top current source to supply current to the filter capacitor. Then, the supplied current charges the filter capacitor and generates a positive control voltage to be fed into the voltage controlled oscillator. Likewise, an error signal on the DN rail at the PFD output would trigger the bottom current sink, discharging current from the loop filter capacitor. Therefore, it produces a negative control voltage to tune the VCO frequency in the opposite way.

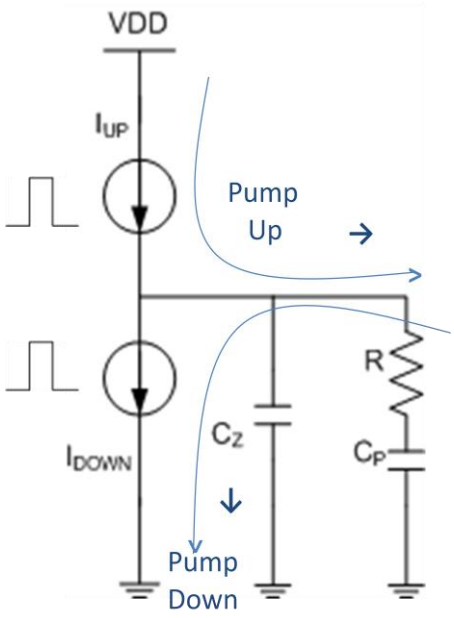

Figure 3.7. Simple charge-pump schematic [8] [9]

An op-amp integrator is a good alternate for a charge pump. It does both the functions of converting the input error pulse signal into an equivalent control voltage and filtering out the high frequency components. But, it consumes a lot of die area. So usually it is not preferred for

on-chip applications. A variety of charge pump architectures such as a current amplifier based high-speed charge pump [17], a dual-slope charge pump architecture for fast locking [12], a high-speed and glitch free common-mode feedback based differential charge pump [18] and a low-voltage, high current capable architecture [19-21] have been used over the last decade for different applications. A differential charge pump circuit with RC loop filter has been chosen for this wireless transceiver design project because of its design simplicity, good noise immunity and low power consumption. It has been designed using the 130 nm IBM-CMOS process. Figure 3.8 shows the circuit schematic of the charge pump designed [6-7].

3.2.1 Charge Pump Design

The designed charge pump is a differential input and single ended output charge pump circuit. Each differential amplifier unit on either side is designed to be of unity gain. These take the differential UP and DN signals from the PFD output and feed the central differential amplifier with current mirror load. This inner differential amplifier either supplies the current into the loop filter or sinks the current from the filter capacitor, based on its input.

The differential amplifier on each of the two ends acts as an input buffer to the charge pump. The input signal has been negated on the output node of the each differential pair and is fed to the PFET instead of the NFET. Hence, the effect of negation has been nullified and the differential pair acts as a buffer. The active load has the benefit of reducing the on-resistance by itself while current flows through it, unlike fixed passive load resistors. The gate-drain tied PFETs act as active load. The transistors M13, M14 and resistor R1 form a current mirror supplying fixed bias current to the differential pair. This is also true of transistors M15, M16 and resistor R2. The bias current flows constantly through the differential circuit.

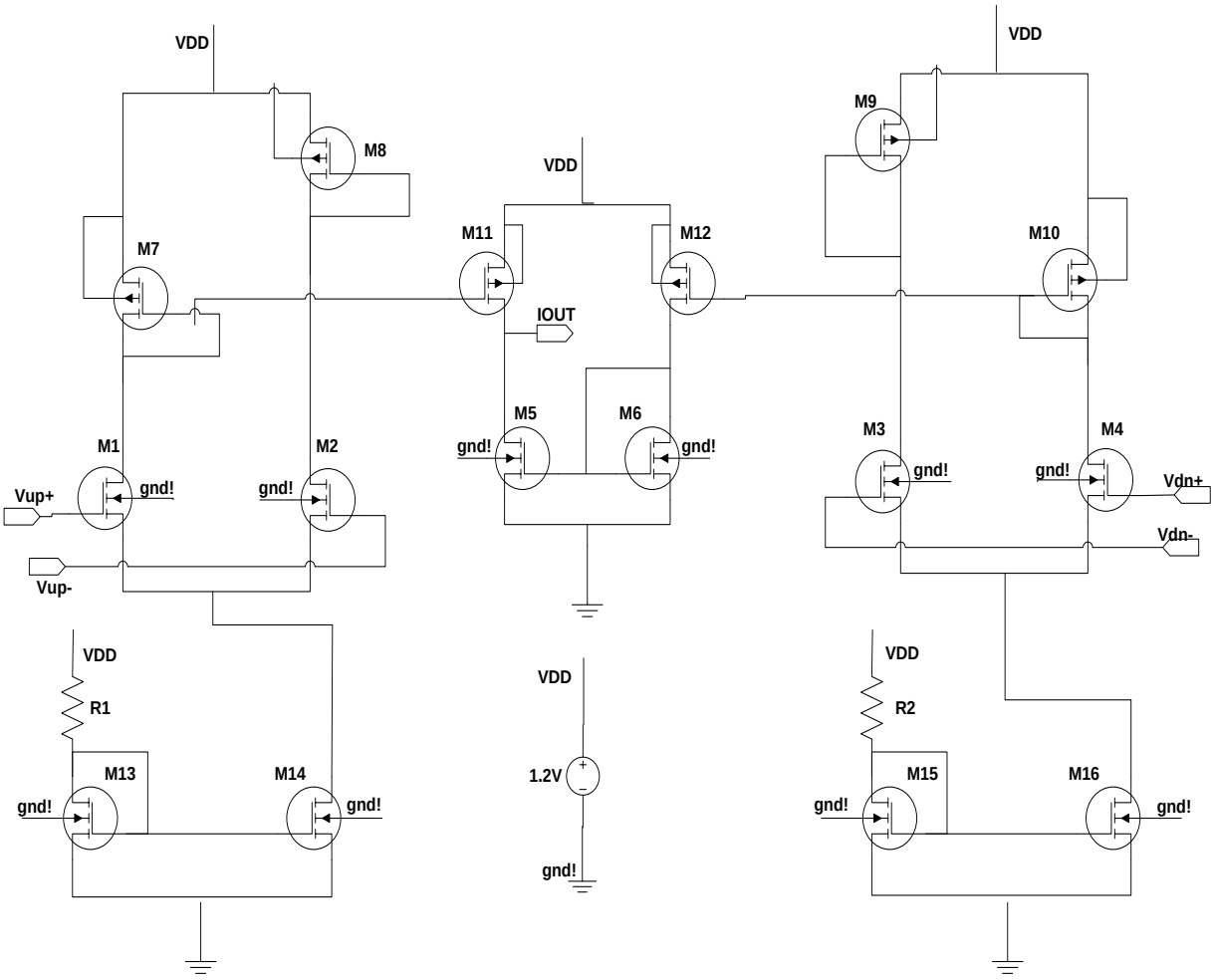

Figure 3.8. Differential charge pump schematic [6-7]

The constant current flowing through the buffers effectively reduces the switching power loss. Also, the amount of power dissipation is brought down by decreasing the biasing current to as low as 100 µA. In addition, the decreased bias current reduces the noise generation proportionately. By taking inputs differentially these buffers help in suppressing the common mode input noise injected into the charge pump [6-7]. So the input noise has been suppressed to a better extent and not transmitted across the charge pump to the VCO.

The differential pair transistors on either end have been designed to be of unity gain with optimum aspect ratio. A 73 kΩ resistor has been chosen for the current mirror load and a 12 µm/0.24 µm aspect ratio has been derived for the gate-drain tied transistor to obtain the 100 µA current from the 1.2 V power supply. This current is in turn reflected in the adjacent common-gate connected transistor. The current flowing through this current mirror acts as the biasing current for top differential transistor setup. The implemented biasing current mirror circuit is as shown in Figure 3.9.

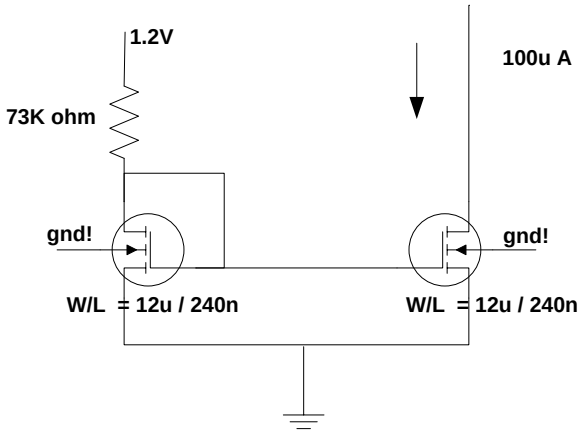

Figure 3.9. Current Mirror design

The central differential charge pump PFETs take the input from the neighboring differential units. The NMOS transistor pair acts as a current mirror load. Whenever a negative pulse is received on M11 the charge pump sources the current and the NMOS transistors M5, M6 and the PMOS transistor M12 are turned off. On the other hand, if a negative pulse is received on M12 then M6 turns on with its diode connection and consequently turns on the common-gate transistor M5. The differential charge pump setup designed and implemented is as shown in Figure 3.10.

The differential charge pump designed is capable of sourcing and sinking 7 µA of current. The lower the charge pump current, the lower the noise transmitted across the loop [3-6]. So it also helps in reducing the amount of noise around the loop. Partially, the reduced noise level has been achieved by avoiding the constant current supplying tail current source [29]. But, the reduced charge pump current has the negative effect of increasing the settling time of the PLL loop [3-4]. The simulated power consumption of this charge pump block is calculated to be 35.34 µW.

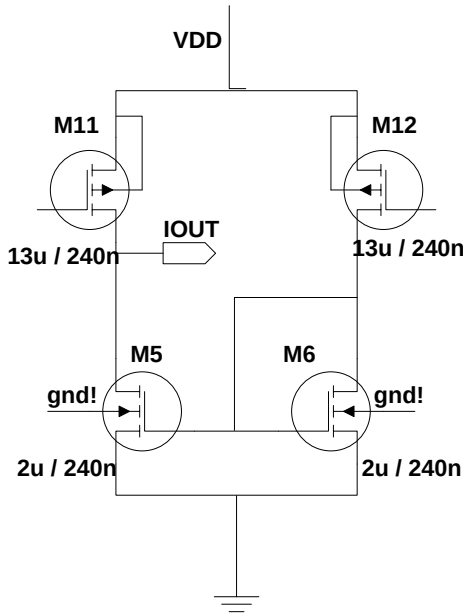

Figure 3.10. Differential charge pump design

3.2.2 Simulation Data

Power supply and temperature variation have a direct impact on the charge pump performance. The output current increases with increasing supply voltage. As the supply voltage increases, it also increases the current driven by the output transistor by increasing its

transconductance (g_m) and reducing the channel resistance (R_{DSON}). The graph in Figure 3.11 shows the change in charge pump output current with power supply variation.

Similarly, charge pump output current increases with rise in temperature. As the temperature increases, the g_m of the transistors increases predominantly over the increase in channel resistance (RDS_{ON}). Hence, it results in increased driving current. Figure 3.12 plots the change in charge pump output current with rise in temperature. The Table 3.2 shows the design parameters of the CP stage as implemented in 130 nm CMOS.

Table 3.2 Charge Pump Design Parameters

Parameter	**Value**
I_{CP}	7 µA
Biasing current	100 µA
Power consumption	35 µW
R	73 kΩ

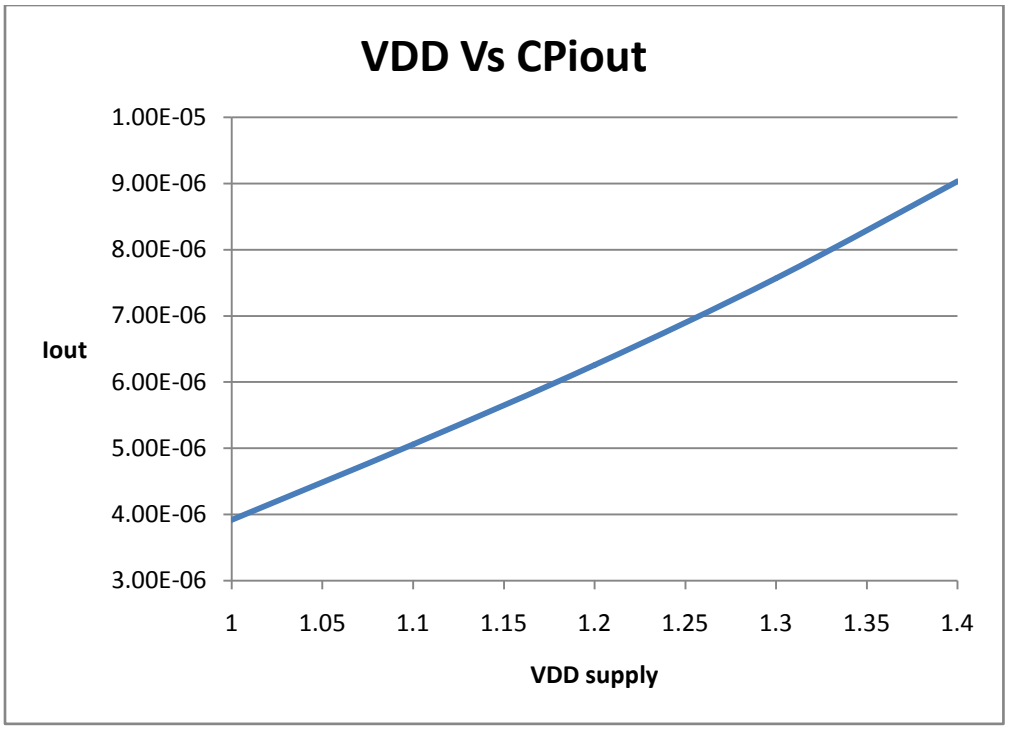

Figure 3.11 Charge pump output current variation with power supply

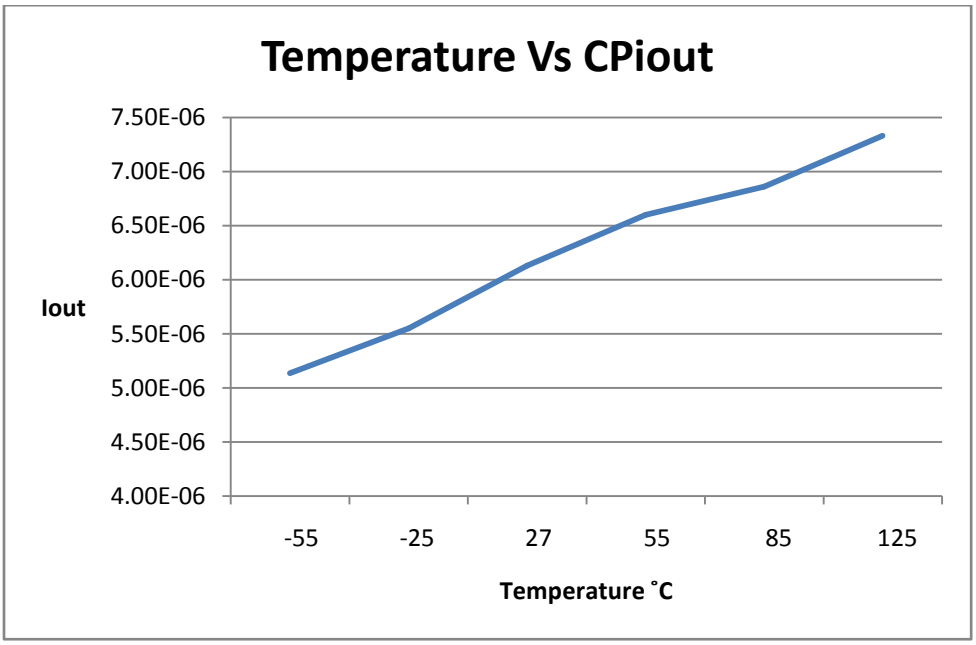

Figure 3.12 Charge pump output current variation with power supply

3.3 On-chip RC Loop Filter

The loop filter is a critical component in deciding the loop dynamics of the PLL. A loop filter is included in the PLL to stabilize the VCO frequency by filtering out the unwanted high frequency components. The capacitive component of the loop filter accumulates the charge proportional to the amount of charge pump current supplied. So it helps in converting the supplied charge pump current to the equivalent VCO control voltage. This voltage feeds into the following VCO stage and alters its frequency of operation.

There are two types of filters, namely active filters and passive filters. An op-amp integrator shown in Figure 3.13 is a simple example of an active loop filter [8]. An op-amp in combination with an RC circuit filters out the high frequency noise and generates the VCO control voltage by integrating the incoming error pulse signal. As these active filters include an op-amp, resistor and a capacitor they occupy a lot of chip area. Thus, active filters are not preferred for integrated circuit (IC) applications in general. Rather, they are mostly used in board level discrete IC implementation.

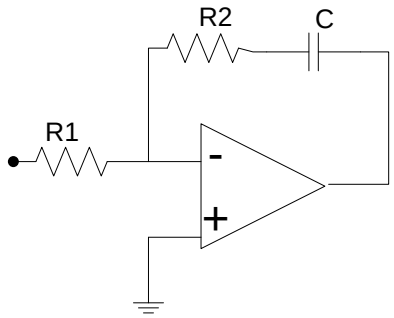

Figure 3.13. Active loop filter schematic

3.3.1 Filter Circuit Design

A simple RC filter shown in the Figure 3.14 is designed and implemented on-chip as a part of this project. The R and C_P components add a zero to the open loop transfer function of the PLL. It helps in suppressing the noise from the input reference and other PLL blocks. But, inclusion of the resistor results in a very high frequency noise and ripple on the VCO control voltage across the filter which would in turn affect the VCO oscillation frequency [8]. This can be reduced to a better extent by decreasing the filter bandwidth, but this affects the loop settling time. And, the bandwidth shrinking is also limited by the size of on-chip filter capacitor. So a pole is introduced into the loop transfer function by placing a capacitor C_Z in parallel with R and C_P. It helps in grounding the high frequency noise across the loop filter and hence stabilizes the VCO control voltage.

Generally, the loop bandwidth or filter cutoff frequency is assumed to be 1/10 of the input reference frequency to avoid any reference feed-through to the VCO [6, 8, 11]. The cutoff frequency of the RC filter is calculated as

$$\omega_{lpf} = \frac{\omega ref}{10} \tag{3.1}$$

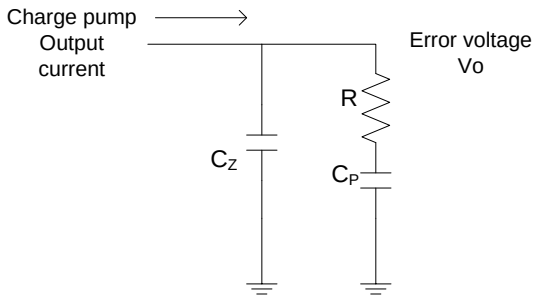

Figure 3.14. On-chip RC loop filter

The transfer function of the loop filter shown in Figure 3.14 is given by

$$= \frac{\left(R + \frac{1}{SCp}\right)\left(\frac{1}{SCz}\right)}{R + \frac{1}{SCp} + \frac{1}{SCz}} \quad => \frac{1 + SRCp}{S^2RCpCz + SCz + SCp}$$

$$= \frac{1 + S\tau_z}{S(Cp + Cz)(1 + S\tau_p)}$$

Where, time constant $\tau_z = RCp$

$$\tau_p = R\frac{Cp\,Cz}{Cp + Cz} = RCz \quad \text{for } Cz << Cp$$

So, frequency of pole $\omega_p = 1/RCz$

frequency of zero $\omega_z = 1/RCp$

For maintaining stability of the system, zero and pole frequencies are assumed to be

$$\omega_p = 4\omega_{lpf} \quad \text{and} \quad \omega_z = \frac{1}{4}\omega_{lpf} \tag{3.2}$$

The liner model of the entire loop can be represented as in the following Figure 3.15.

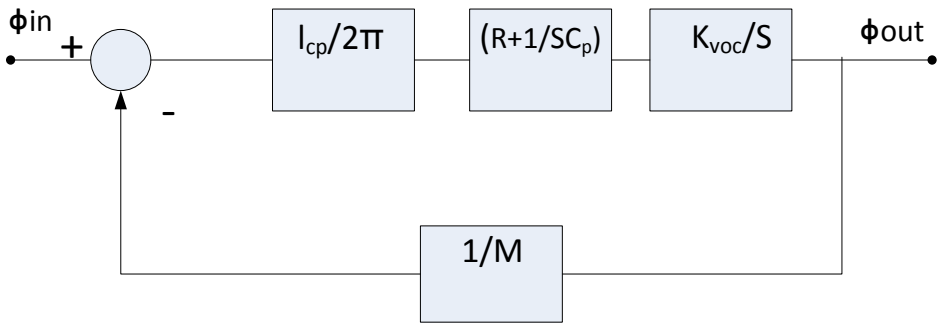

Figure 3.15. Equivalent linear model of the entire PLL loop [11]

Also, the closed loop transfer function of the entire loop can be written as [11]

$$H(s) = \frac{\frac{I_{CP}}{2\pi} K_{VCO} \ (SR + \frac{1}{C_P})}{S^2 + SR\frac{I_{CP}}{2\pi M} K_{VCO} + \frac{I_{CP}}{2\pi M C_P} K_{VCO}}$$

Equating it to the 2nd order system closed loop transfer function from control theory [9, 11],

$$H(s) = \frac{\omega_n^2}{S^2 + 2\zeta\omega_n S + \omega_n^2}$$

we obtain [9, 11],

$$\omega_n = \sqrt{\frac{I_{CP}}{2\pi M C_P} K_{VCO}} \quad (3.3)$$

$$\zeta = \frac{R}{2}\sqrt{\frac{I_{CP} C_P}{2\pi M} K_{VCO}} \quad (3.4)$$

$$\omega_{LPF} = 2\zeta\omega_n = \frac{R I_{CP}}{2\pi M} K_{VCO} \quad (3.4)$$

The loop filer design parameters decide the PLL's loop settling time, loop bandwidth, oscillation damping and the amount of noise injected into the VCO [4, 6]. The PLL needs a narrower filter bandwidth for better noise suppression. But, a narrow bandwidth results in small pole (ω_p) and zero (ω_z) frequencies. So for a given value of filter resistance R, it increases the loop filter capacitance (Cp, Cz) values. Therefore, it increases the transient settling time of the PLL. Hence, the bandwidth and noise should be traded off with the settling time of the PLL.

The loop filter R,C values are calculated by substituting the specifications in Table 3.3 in the MATLAB routine in APPENDIX I . The R, C_P and C_z values are approximately calculated by following the above mentioned equations and then fine tuned using the MATLAB routine to

obtaing better phase margin and required cross over frequency i.e. the loop BW. Figure 3.16 shows the bode plot obatined from the matlab routine.

Table 3.3 Loop Filter Design Parameters

K_{VCO}	310.8 MHz/V
I_{CP}	7 µA
C_P	10.613 pF
C_z	663 fF
R	300 kΩ
Division ratio(M)	433
Steady state VCO control voltage	598 mV

The gain cross over frequency (or) loop bandwidth and the phase margin simulated are marked on the bode plot. The following parameters are calculated from the matlab simulation.

Loop bandwidth = 215 kHz

Damping factor (ζ) = 1

Phase Margin = 63˚

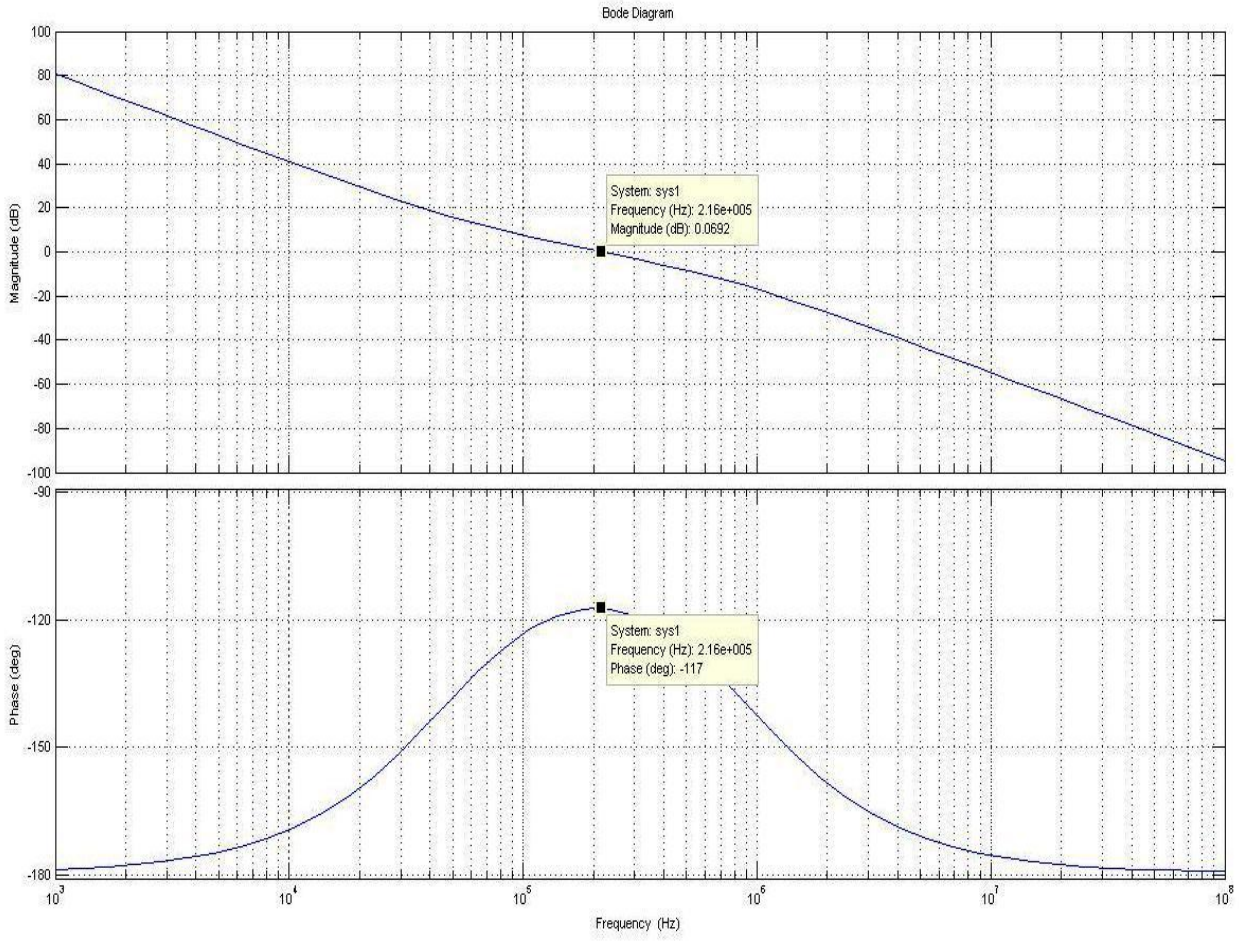

Figure 3.16 Bode plot representing the open loop PLL transfer function

3.3.2 Simulation Results

Figure 3.17 shows the voltage variation across the filter capacitor as the input phase varies. The charge pump driving current increases with positive phase difference at the PFD output. The increase in charge pump current results in an increase in the VCO control voltage and viceversa. Whenever the loop is in locked condition a 598 mV of constant error control voltage is maintained at the VCO input node.

Figure 3.18 shows the change in voltage across the loop filter with varying power supply. The increase in VDD and temperature increases the g_m of the conducting charge pump transistors

thus increasing the supplied current. Thus, it increases the VCO control voltage across the filter capacitor. The temperature variation of the control voltage has been depicted in Figure 3.19.

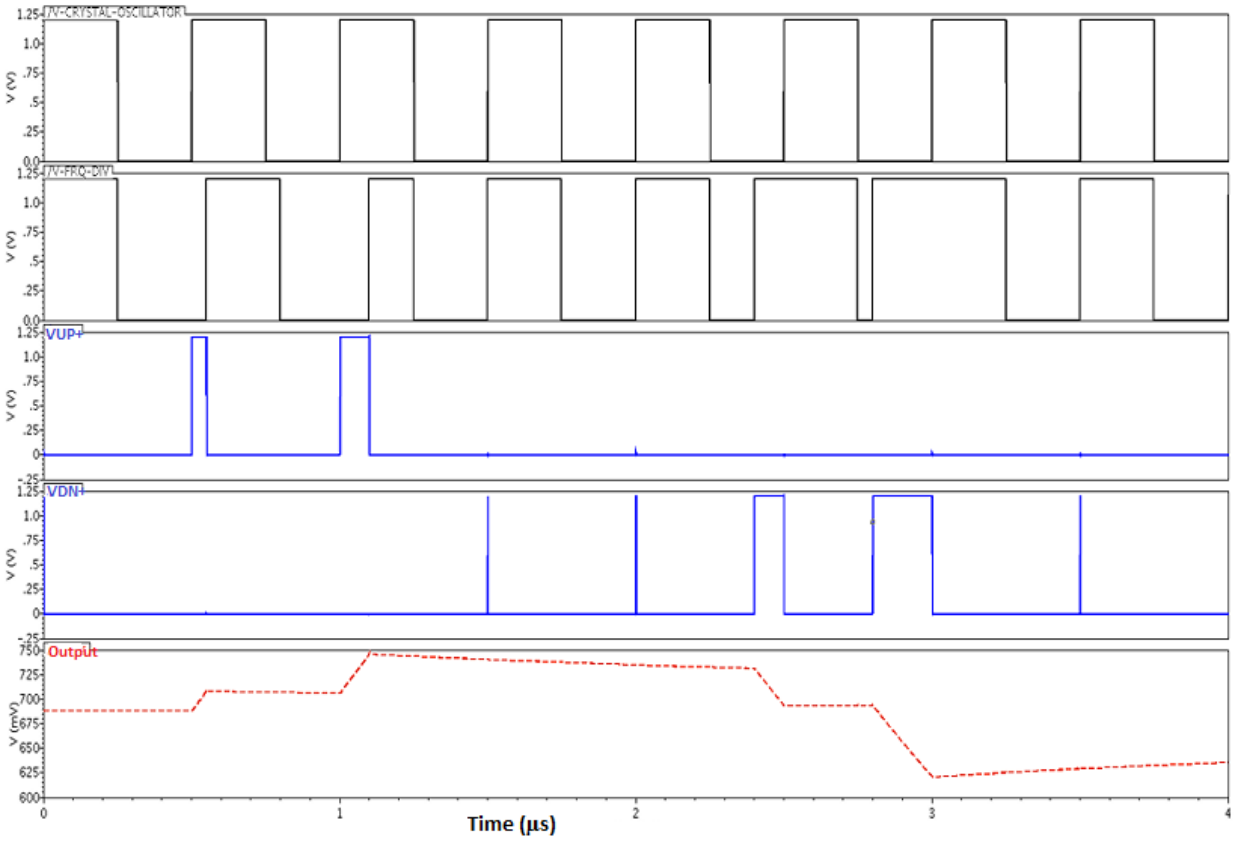

Figure 3.17. Voltage variation across the loop filter with input phase change.

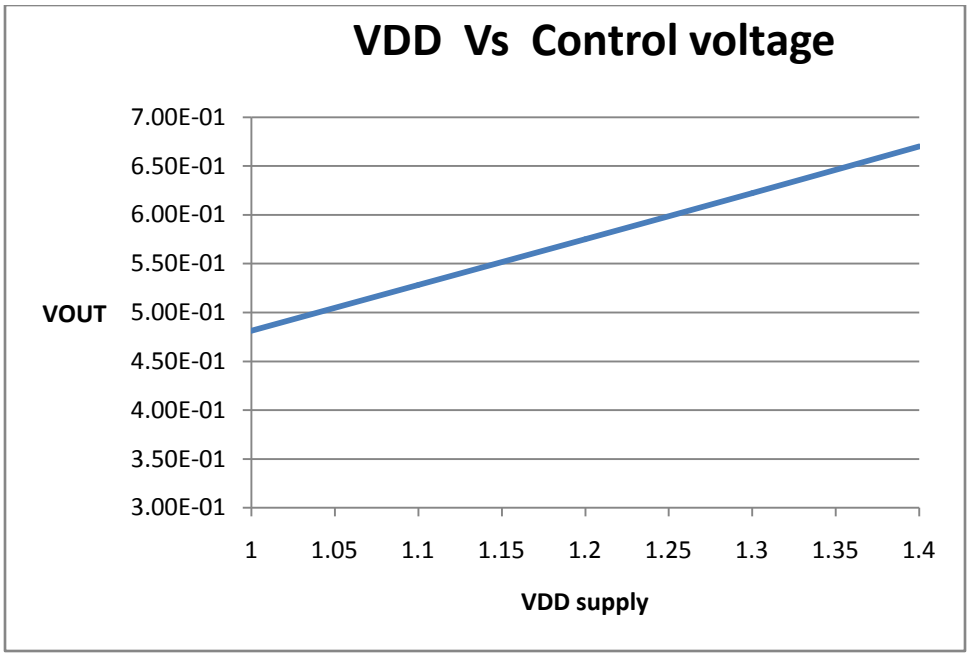

Figure 3.18. Control voltage variation with change in VDD.

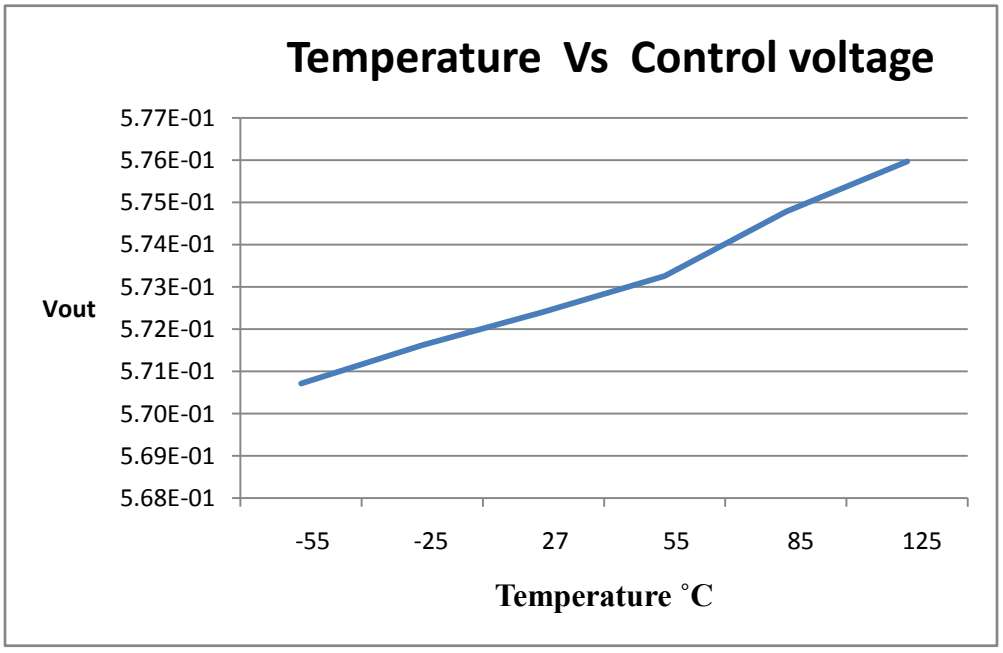

Figure 3.2. Control voltage variation with change in temperature.

3.4 Dual-Modulus Frequency Divider

Frequency synthesizers with high VCO oscillating frequency and a direct feedback connection to the input phase comparator need an equivalent stable crystal oscillator reference. But, it would be very difficult to find a crystal with hundreds or thousands of mega hertz operation. So a frequency divider is included in the feedback path from VCO output to the PFD input. It helps in dividing the incoming VCO frequency to a lower value and feeds in to the PFD for frequency and phase comparison. So, it helps in bringing down the required stable PFD input reference which is very critical in high frequency applications.

A dual modulus divider is generally used as the frequency divider in PLLs. In very high frequency applications, a counter is used along with the main divider to accomplish the task of frequency division. The counter helps in reducing the burden on the dual modulus divider. Figure3.20 shows the block schematic of a simple frequency divider including counter. The prescaler divides the VCO output to a certain ratio and then feeds it to the counter for further division.

The main drawback of including the additional counter is that it requires the achievable PLL channel spacing to be different from that of input reference frequency. But, with increasing frequency division ratio the performance of CMOS based dividers comes down. Therefore, the additional circuitry is mandatory in the very high frequency range.

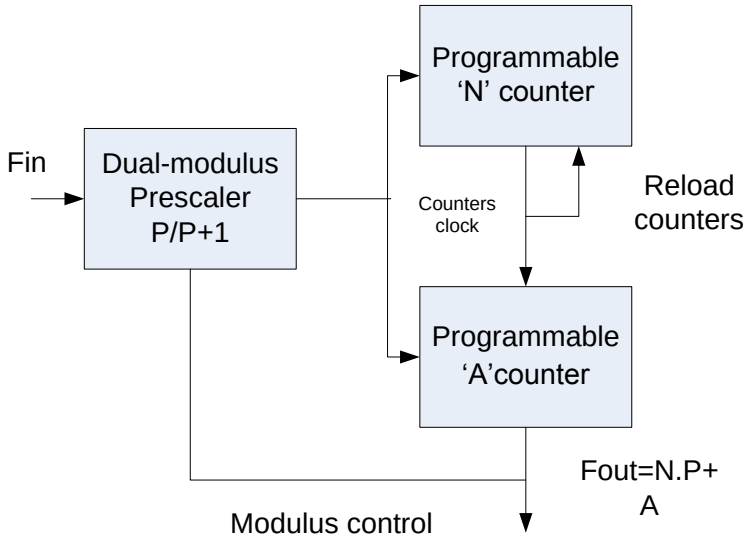

Figure 3.3 A programmable divider block schematic [24]

3.4.1 Divider Circuit Design

A programmable frequency divider has been designed as part of this project. It performs variable frequency division with the help of its programmable digital input bits. It can be programmed to give out any output frequency by setting its modulus bits. It consists of a set of 8 multi-modulus divide-by-2/3 blocks cascaded together to achieve division ratio in the range of 256 - 511. A divide-by-2/3 block does the function of either divide by 2 or divide by 3 based on the mod input. The configuration of each divide by 2/3 block is shown in Figure 3.21 [7, 24].

Each divide-by-2/3 block has an input (F_{IN}), output (F_{OUT}), modulus in (Modin), modulus out (Modout) and a mod (Modulus) pin. Whenever the mod pin is supplied a logic '0', the DFF in the feedback path gets disabled. So, the two DFFs in the forward path of the divider act in master-slave configuration achieving a divide-by-2 signal. On the other hand when the mod pin is logic '1', an additional clock delay is introduced by the DFF in the feedback. Therefore, a divide-by-3 signal is produced at the output. F_{IN} and F_{OUT} pins act as input and output pins. The Modin and Modout are the division-return signal pins i.e. they recursively feedback the divided

output signal into the loop. The Modin signal is generated by the last mod-2/3 block in the chain and is clocked up the chain for every cycle of the divided output [24, 25]. This feedback signal helps in reducing jitter and noise along the divider path. Figure 3.22 shows the pin connections of the all 8 divide-by-2/3 stages.

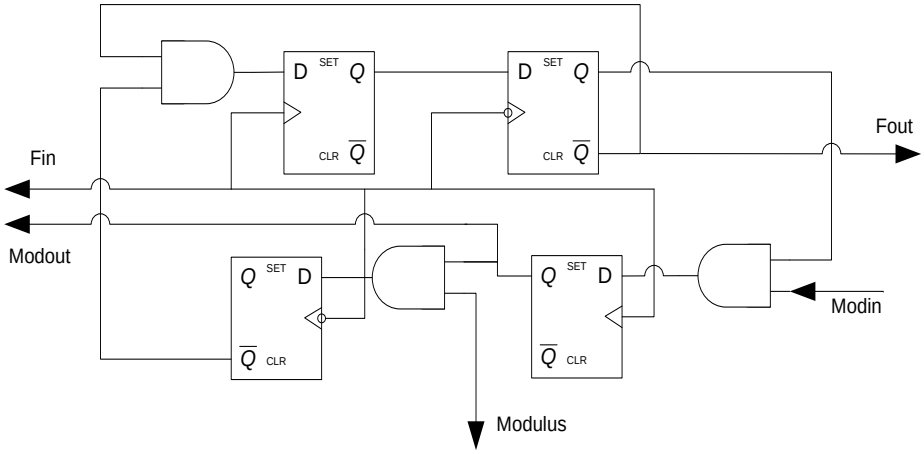

Figure 3.4. Divide by 2/3 module.

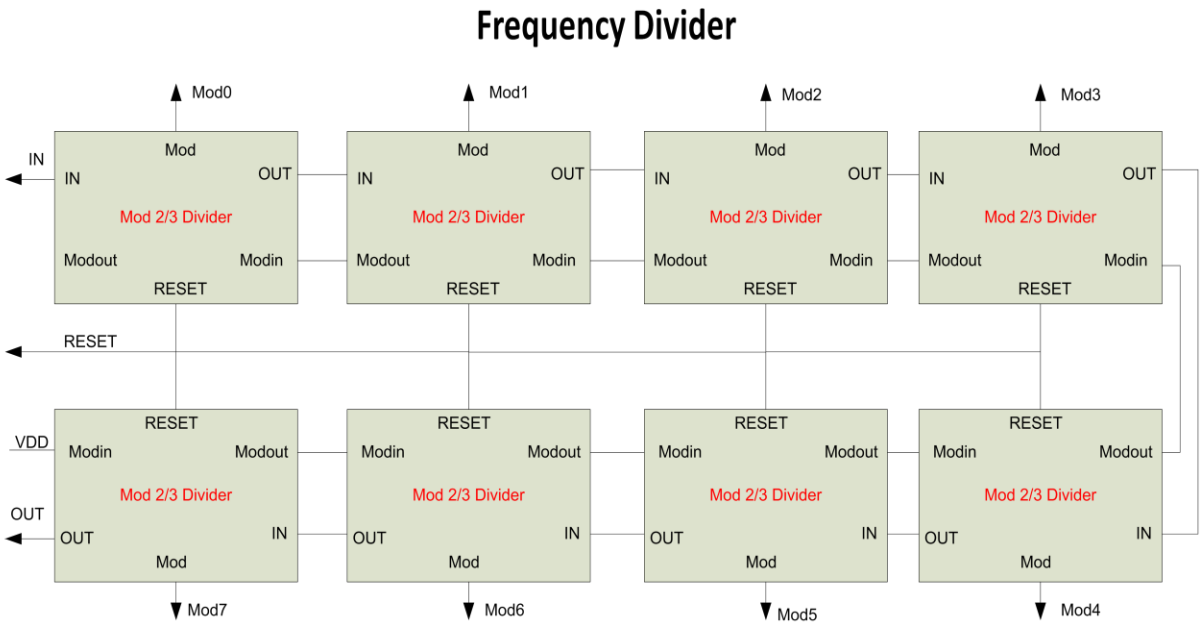

Figure 3.5. Programmable frequency divider block diagram.

The general equation defining the output divider ratio with mod bits is given by

Divider ratio = $P_0 + 2P_1 + 4P_2 + 8P_3 + 16P_4 + 32P_5 + 64P_6 + 128P_7 + 256$

The modulus bits are programmed with the following bit pattern to achieve divide-by-433 operation.

Mod0	Mod1	Mod2	Mod3	Mod4	Mod5	Mod6	Mod7
1	0	0	0	1	1	0	1

It is a programmable divider; so it can perform any other division ratio by appropriately programming its input bits following the above equation.

3.4.2 Simulation Results

Figure 3.23 shows results graph obtained by simulating the divide-by-433 divider. Each signal represents the divided output at different stages along the frequency divider path. The top square signal in red represents the 2 MHz signal obtained at the output by driving the 866 MHz VCO output signal. The frequency divider design parameters are tabulated in the Table 3.4.

Table 3.4 Frequency Divider Design Parameters

Parameter	Value
Divider ratio	433
Division Range	256 - 511
Power consumption	220 µW
Output frequency	2 MHz
VCO output frequency	866 MHz

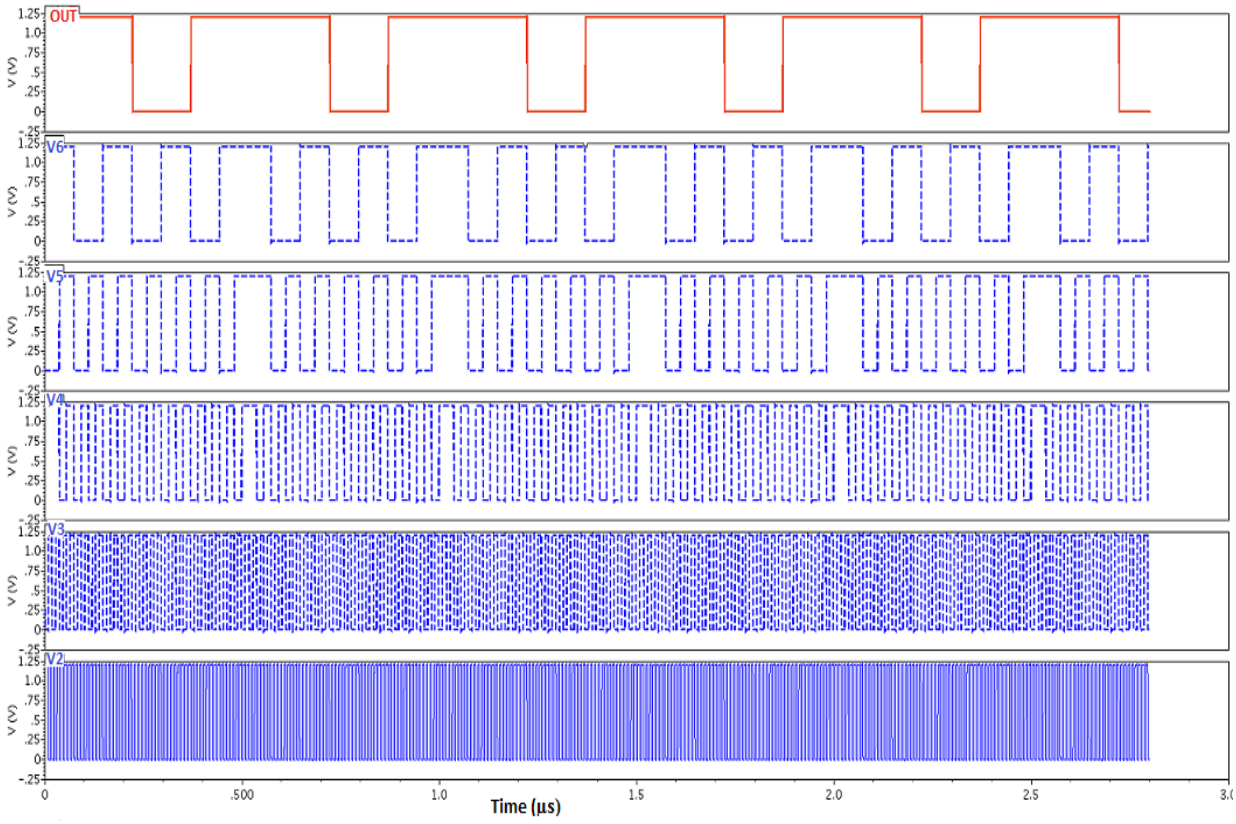

Figure 3.6. Frequency divider output graph

3.5 Voltage Controlled Oscillator

Voltage controlled oscillator (VCO) is used as the source of frequency generation. In frequency synthesizers, VCO achieves good frequency stability with a feedback loop and a stable crystal reference at the input.

A variety of oscillator types exists namely, relaxation oscillators, ring oscillators, crystal oscillators and tuned oscillators. But, only the ring oscillators, the relaxation oscillators or the tuned oscillators are considered for on-chip applications. The relaxation oscillators produce oscillating signal by repeatedly charging a capacitor and discharging though a resistor so, it

involves energy dissipation. Tuned oscillators on the other hand consist of a simple tank circuit with inductor L and capacitor C. The L and C values are chosen such that the tank circuit oscillates at a known frequency. Tuned oscillators can achieve low noise by increasing its quality factor (Q). Where, quality factor is defined as

$$\text{Quality factor (Q)} = 2\pi * \frac{(Total\ energy\ stored)}{(Energy\ lost\ per\ cycle)} \tag{3.5}$$

$$= 2\pi * \frac{(0.5\ C\ V^2)}{\left(\frac{V^2}{2 * R_P * f}\right)}$$

$$= 2\pi f * R_P C$$

$$= \omega C R_P \tag{3.6}$$

The resonant frequency of the LC tank circuit is given by $(\omega) = \sqrt{\frac{1}{LC}}$

Quality factor (Q) = $\omega\ R_P\ C = \frac{R_P}{X_C} = \frac{R_P}{X_L}$

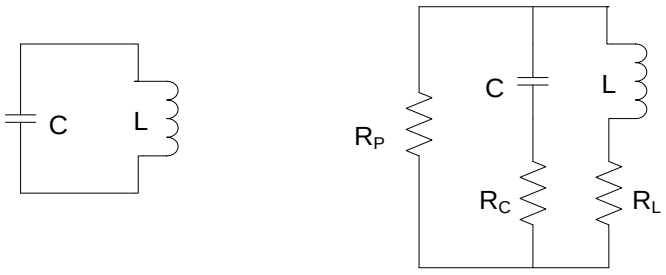

Figure 3.7. a) LC tank circuit b) LC tank circuit with parasitic elements

Tuned oscillators are more preferred over the relaxation oscillators because of their low phase noise, high spectral purity and good frequency stability at high frequencies. Choosing a proper

inductor and a capacitor is the key factor in oscillator design. The series resistance associated with the capacitor (R_C), inductor (R_L) and the parallel resistance R_P determines the amount of power consumption and the noise generated in the LC oscillator [31]. Figure 3.24 shows the LC tank circuit and the associated parasitic components.

3.5.1 VCO Design

A variety of VCO architectures are proposed in the literature such as, oscillators with bond wire inductors for low noise and low power consumption [31], hollow spiral inductor for least skin effect and lowest metal losses to achieve reduced phase noise [32] and a cumulative on-chip spiral inductor, bondwire and packaged die inductance for achieving high Q factor in a LC tank circuit [33]. A complementary, differential cross-coupled oscillator with negative resistance feature ($-g_m$) is used for this project which is shown in the Figure 3.25 [35]. Unlike NMOS or PMOS only differential oscillators, the complementary cross-coupled differential oscillator restricts the peak voltage of the oscillations to supply voltage. The PMOS transistor turns off when the voltage across the inductor exceeds the supply and the NMOS transistor conducts the bias current controlled by the tail current mirror when it is turned on [30]. The output VREF node helps in varying the varactor capacitance and hence the oscillation frequency. The tail current mirror supplies a constant bias current through the differential pair and therefore decides the amount of power consumption and the phase noise produced. Figure 3.26 shows the voltage controlled oscillator output simulated in Cadence Spectre. The circuit is designed in 130nm IBM-CMOS process.

A simple two inverter buffer shown in Figure 3.27 is added at the end of VCO to drive the IO pad [35]. It helps to avoid any impact the pad capacitance will have on the VCO operation. This buffer is designed by MSCAD lab student Kacie Woodmansee.

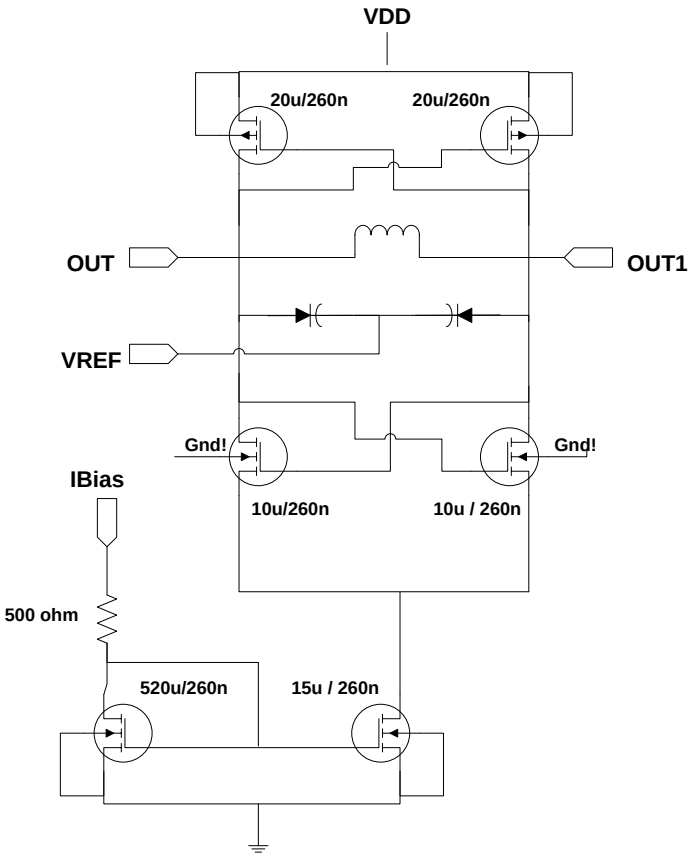

Figure 3.8. Differential cross-coupled oscillator [35]

3.5.2 Simulation Data

The simulated VCO output signal with buffer in place is as shown in the Figure 3.28. The added buffer converts sinusoidal VCO output to a square wave signal.

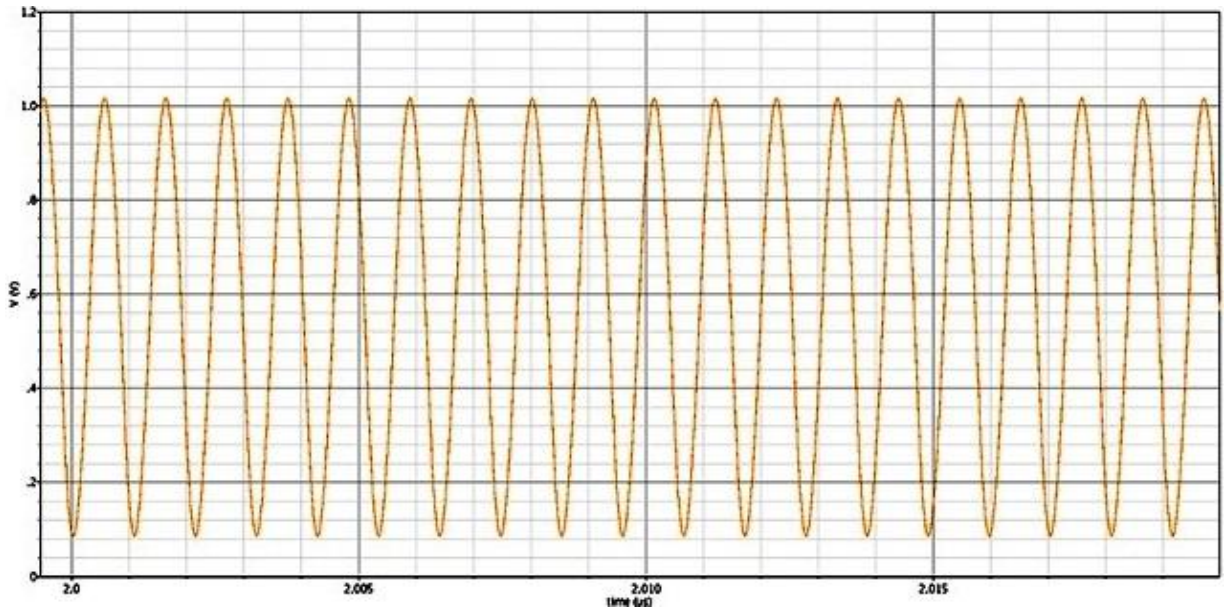

Figure 3.9. Voltage controlled oscillator output signal

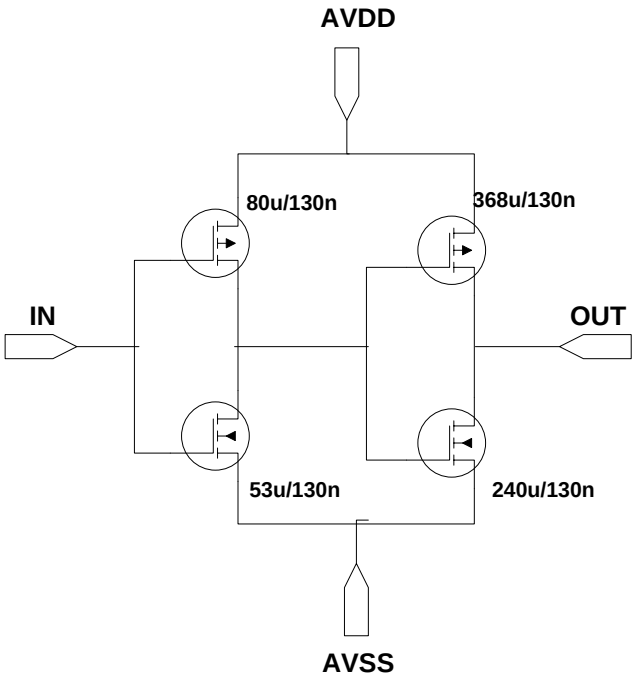

Figure 3.10. Output buffer for VCO [35]

The variation in oscillation frequency with control voltage and temperature is plotted in Figure 3.29. As the control voltage increases, the reverse voltage across the varactor increases. Therefore, it decreases the value of the varactor capacitance. The decreased capacitance results in increased oscillation frequency. Also, with increase in temperature the bias current produced by the tail current mirror decreases. Therefore, the oscillation frequency decreases too.

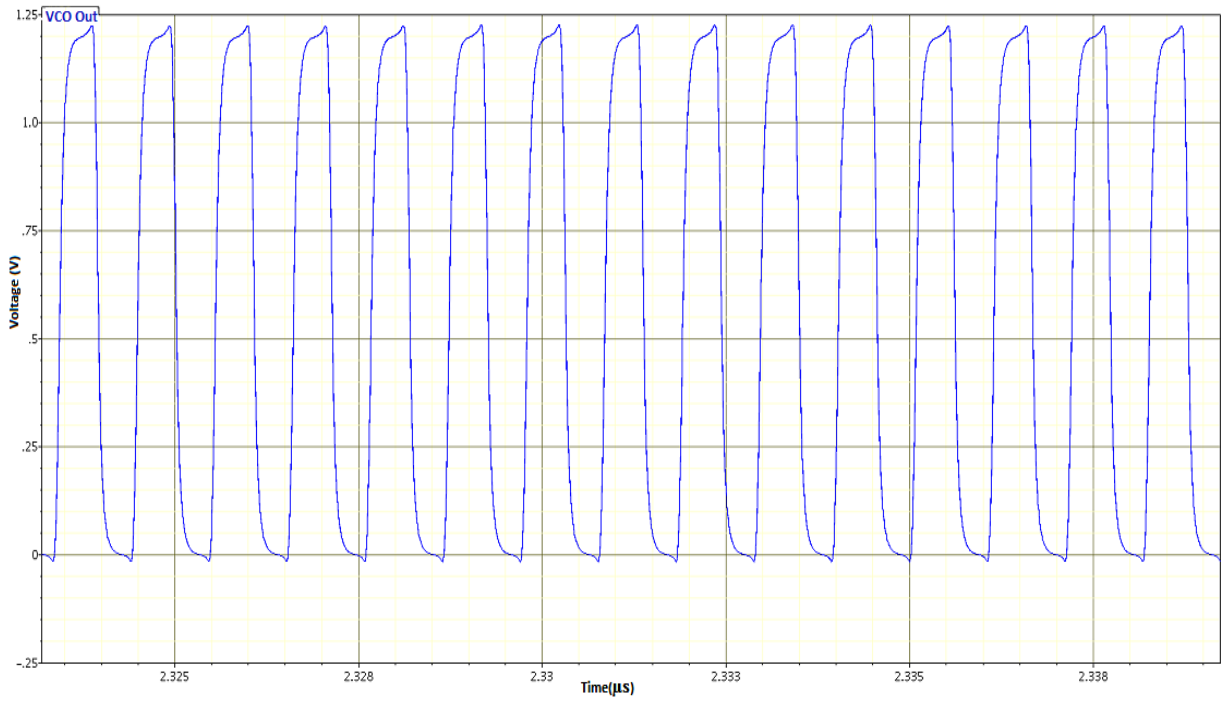

Figure 3.11 VCO output signal with buffer

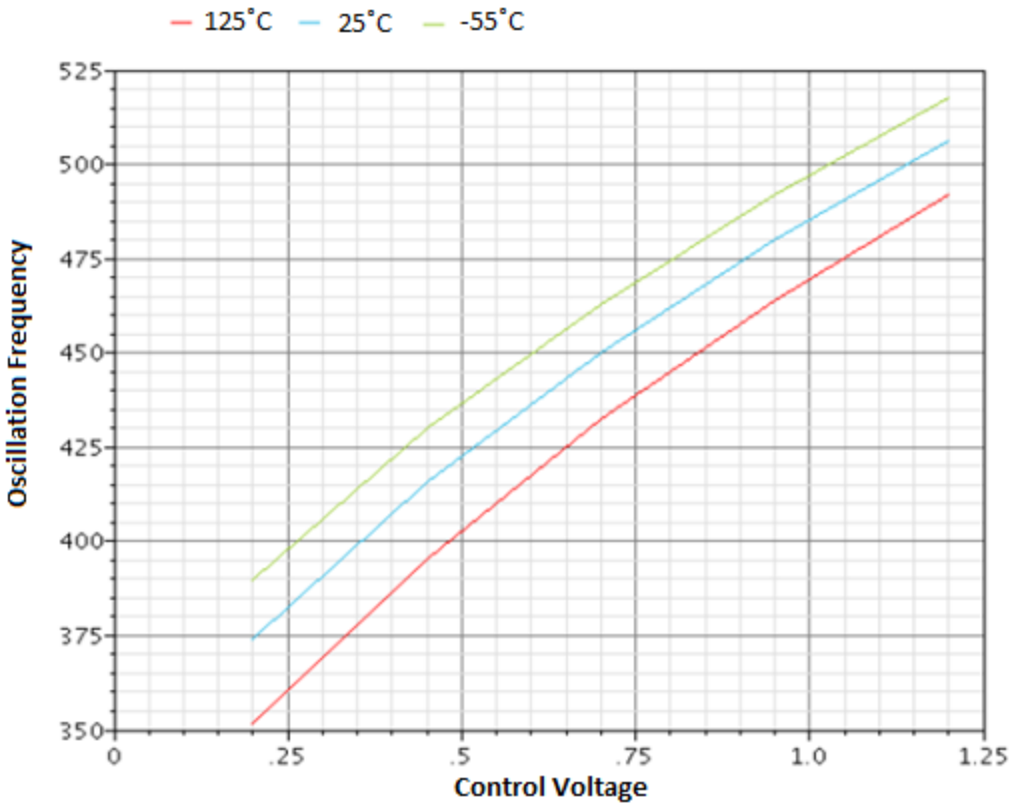

Figure 3.12 Oscillation frequency with varying control voltage [35]

Phase Noise: Phase noise is defined as the amount of noise power in a unity bandwidth, at a certain offset frequency with respect to the original carrier signal. Phase noise is defined by the following equation and is usually measured in dBc/Hz [30].

$$\text{Phase noise} = 10*\log\left[\frac{(\text{Noise power in unity bandwidth at } \Delta\omega \text{ offset frequency})}{(\text{original carrier power at } \omega_o \text{ frequency})}\right]$$

So, the oscillator with more negative phase noise value in dBc/Hz has the least phase noise. Figure3.30 plots the simulated phase noise of VCO at different offset frequencies. The phase noise decreases gradually with increase in offset frequency. Also, with increase in temperature the phase noise increases too.

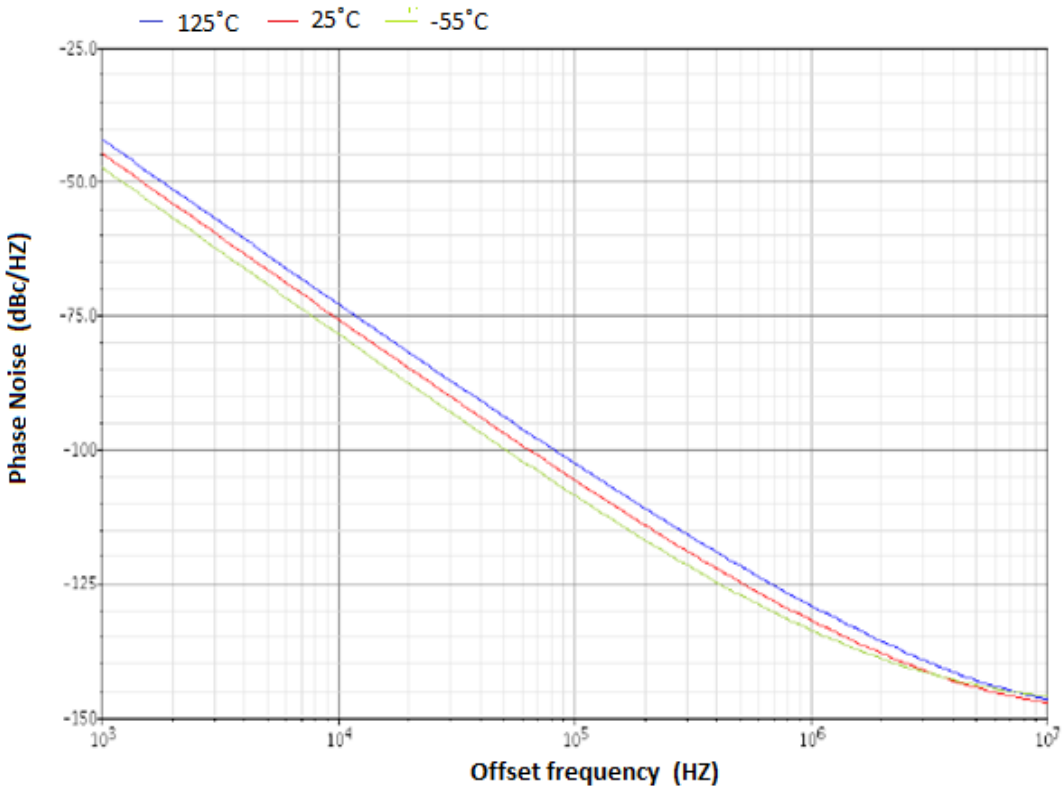

Figure 3.13. Phase Noise with varying offset frequency [35]

Table 3.5 lists all the design parameters measured in simulation for the VCO block. These details are obtained from the VCO design datasheet written by Kacie Woodmansee [36].

Table 3.5 VCO Design Parameters

Parameter	Value
Frequency swing(÷2)	374.3-517.8 MHz
Tuning sensitivity (K_{VCO})	310M Hz/V
Power consumption	2.63 mW
Phase noise@1M Hz offset	-131 dBc/Hz
Phase noise@100K Hz offset	-105.6 dBc/Hz
Tuning voltage	0.2 – 1.2 V

Chapter 4

Integration and Layout

All the phase locked loop blocks discussed in Chapter 3 are integrated together. The PFD, charge pump, loop filter and VCO are connected in series and the frequency divider in the feedback path. A step by step procedure has been followed while integrating i.e. PFD and CP are simulated together first. Then, the loop filter is attached at the end and simulated. The VCO is attached to the combined PFD, CP and filter block and simulated to verify its working. At the end, the frequency divider is attached in the feedback path to check the complete loop functionality.

Integrating the PFD and the CP was simple and straightforward. But, the CP output current had to be brought down from an initially assumed 100 µA to 7 µA when combined with the loop filter for maintaining loop stability. Using the equations mentioned in Chapter 3 loop filter design, the passive component values in the filter are adjusted such that the PLL has the required loop bandwidth, damping factor, settling time and also occupies less die area. The real challenge was to integrate the PFD, CP, filter block with the VCO. The VCO requires a control voltage of 598 mV when running in stable locked state to maintain sustained oscillations at 866 MHz. None of the charge pump and the loop filter parameters could be varied because of the loop stability concerns. So a resistive divider shown in the Figure 4.1 is connected at the end of the filter to facilitate this function to integrate with the VCO. A high resistance value is chosen so that it will not affect both the loop filter properties and the VCO oscillation frequency. The resistive divider helps in maintaining the 598 mV of control voltage at the VCO input in stable state while allowing it to swing with the input phase variation.

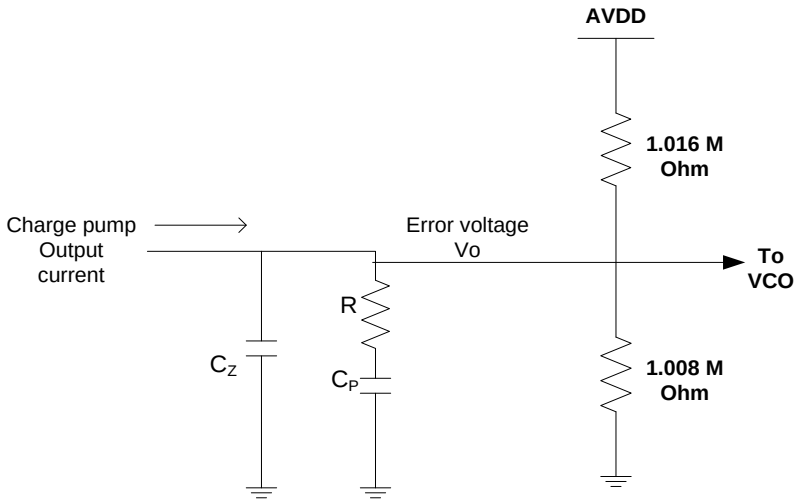

Figure 4.1. Resistor divider used for LPF and VCO integration

The main drawback of using the resistive divider is the VCO can only oscillate in a very limited range around 866 MHz frequency. The resistor divider was brought in mistakenly while running the open loop simulation of the combined PFD, CP, Filter and the VCO blocks. The closed loop action wasn't considered while integrating the VCO with the PFD, CP and the loop filter. When the PLL is running in closed loop even without the resistor divider the phase detector should provide an error pulse signal to the charge-pump, which would charge the filter capacitor to the required VCO input control voltage and kick it up. So, the required VCO start up voltage would be acquired by the closed loop action without the need of any additional start up circuitry for VCO, and the oscillator could be tuned over its complete frequency range.

In addition, the resistor divider setup slows down the loop response time. So, for future work run the closed loop simulation of existing PLL circuit without the resistor divider and analyze its behavior. Based on that, the charge-pump or the loop filter parameters can be modified for improving the design.

4.1 Integrated Blocks Simulation

Figure 4.2 shows the simulated VCO output frequency graph with Integrated PFD, CP, LPF and VCO block. A small phase difference is induced during the initial time period (0 µs – 5 µs) of the simulation using external sources to make sure the VCO frequency would vary accordingly. After that, the simulation runs in zero phase difference i.e. the steady state and an 866 MHz oscillating frequency is observed at the VCO output.

The phase noise analysis on the integrated PFD, CP, LPF and VCO block is performed over temperature and the simulated plot is shown in the Figure 4.3. The phase noise decreases with the increasing offset frequency as expected. At lower offset frequencies, the phase noise at -55 ˚C dominates the phase noise at 27 ˚C. This can be attributed to the non uniform behavior of the passive component models used in low pass filter for simulation.

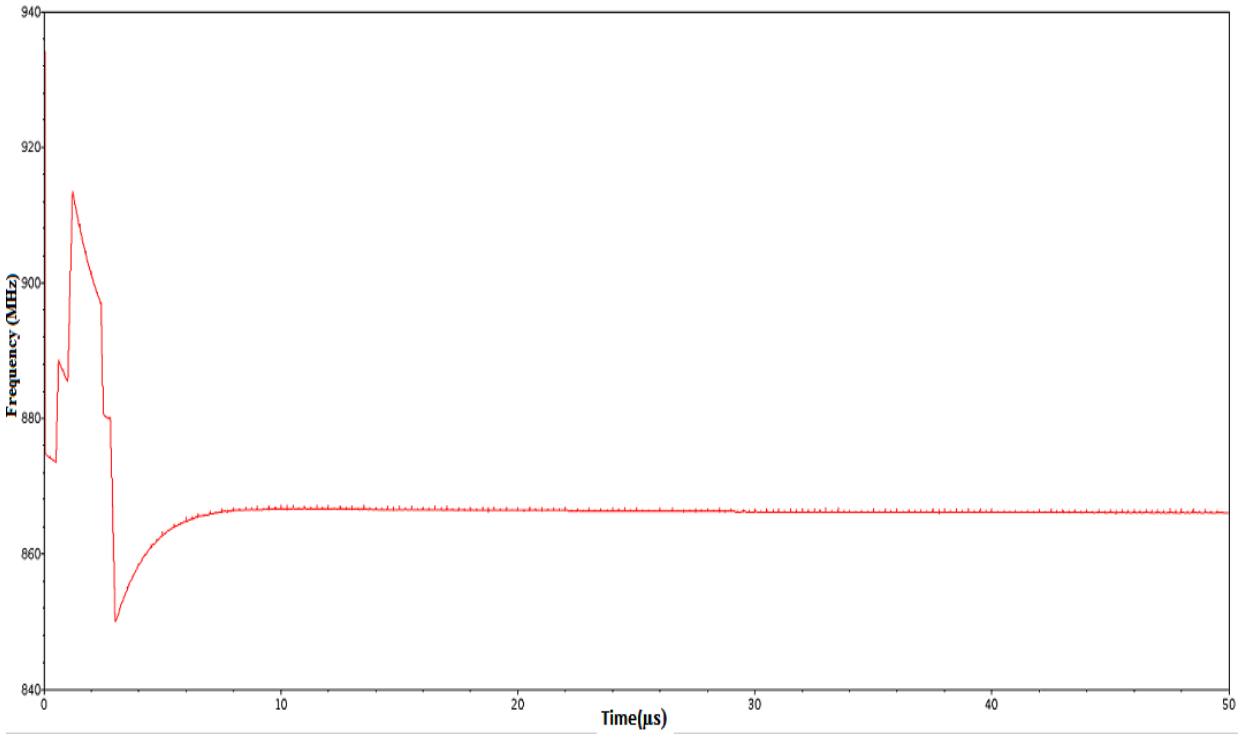

Figure 4.2. VCO frequency graph simulated with combined PFD, CP, LPF and VCO block

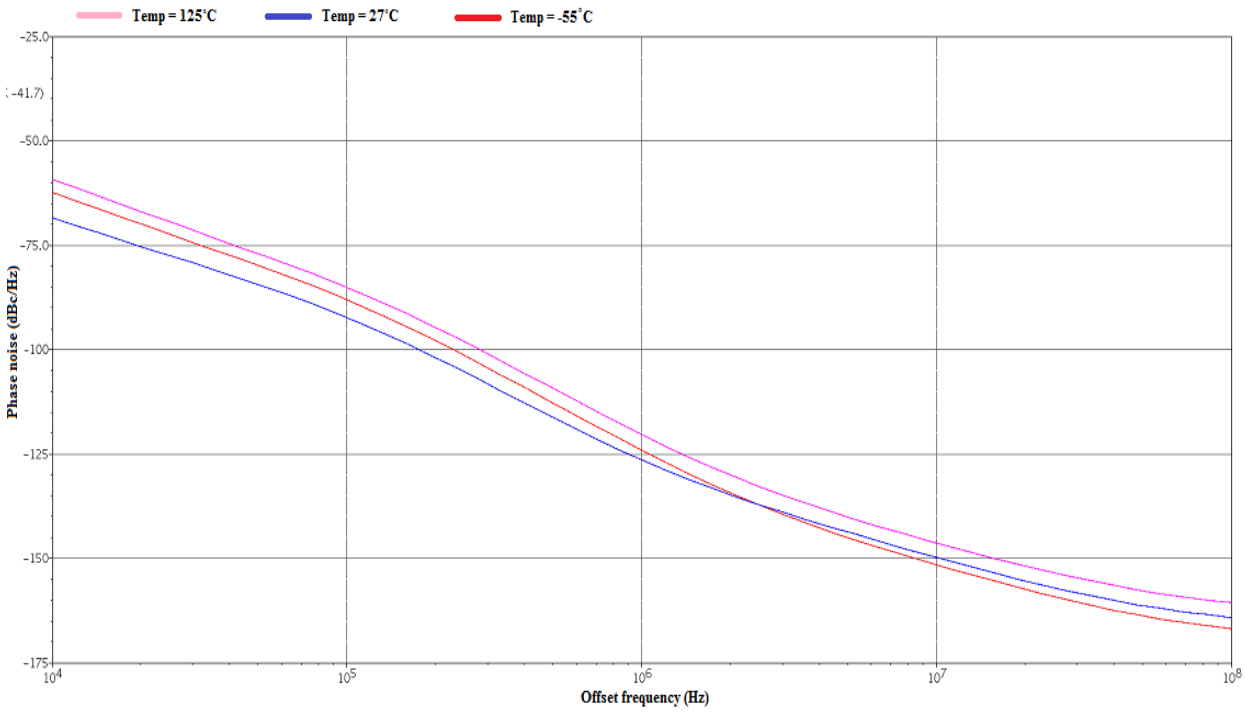

Figure 4.3 Phase noise plot of PFD, CP, LPF and VCO combined block

Finally, the frequency divider is integrated with the rest of the blocks and a 2 MHz signal is observed at the divider output with little phase error as shown in the Figure 4.5. The complete PLL loop simulation is done and the PLL is observed to be locking at 866 MHz with 1% error. Figure 4.5 shows the PLL frequency locking at 866 MHz frequency and the frequency divider's output frequency graph locking at 2 MHz is shown in Figure 4.6.

Settling time: Settling time of a PLL is defined as the time taken for 10% to 90% of the change in output frequency. It can be calculated by measuring the time taken for change in PLL output frequency when the division ratio of the frequency divider is varied. Alternately, input crystal reference frequency can be changed slightly without disturbing the linear operation of the PLL loop to measure settling time.

The transient settling time of the closed loop PLL can be calculated from its output frequency response. Figure 4.6 shows the divider output frequency response when running in the closed-loop mode. An approximately 5 µs of transient settling time was measured from figure 4.6 which is very close to the theoretical expected value i.e. inverse of the PLL loop bandwidth.

$$\text{Settling time} = \frac{1}{(\text{PLL loop bandwidth})}$$

$$= \frac{1}{(200\text{ k})}$$

$$= 5\ \mu s$$

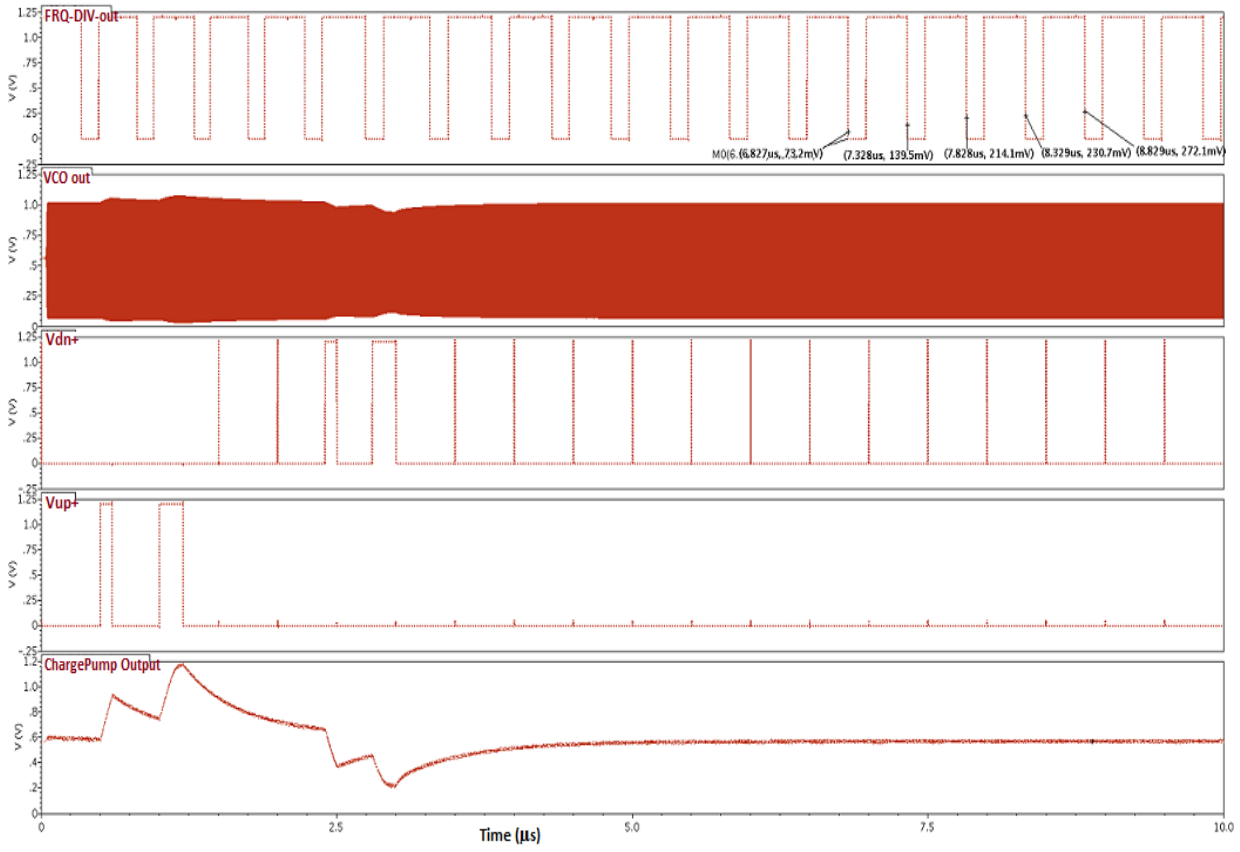

Figure 4.4. PFD, CP, VCO, Frequency divider output graphs simulated with all the blocks connected together in open-loop i.e. except the divider output signal fed to the PFD input

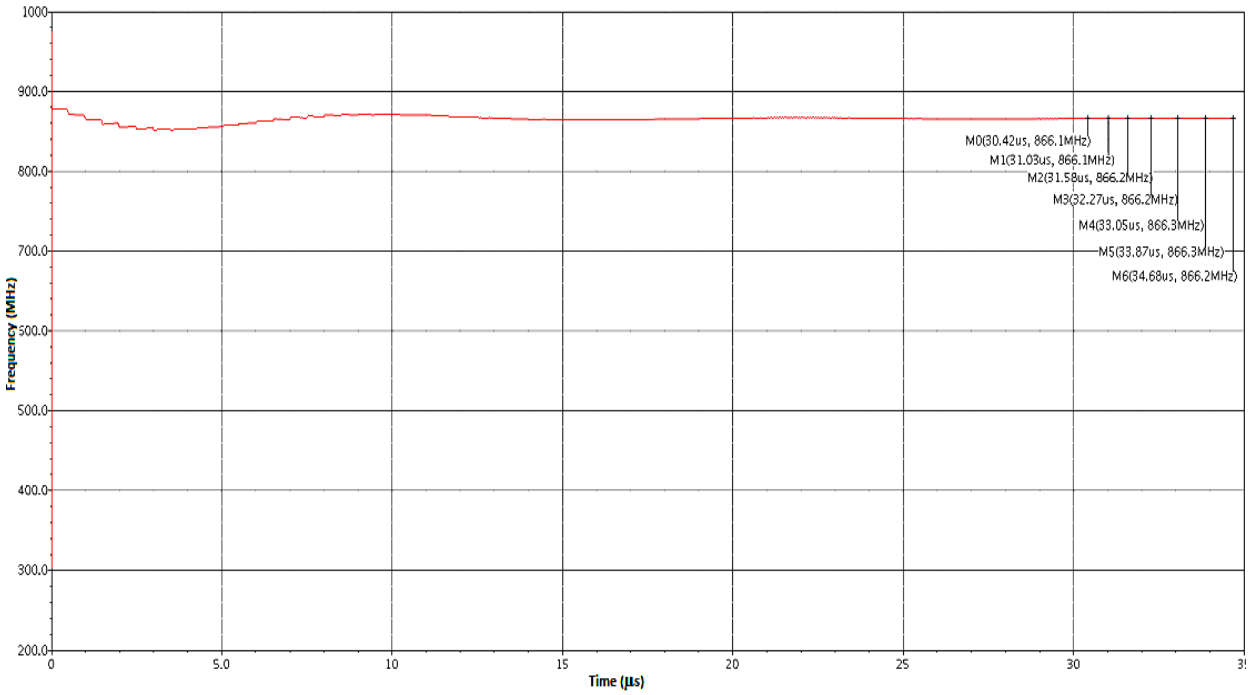

Figure 4.5. PLL output frequency plot with closed loop simulation

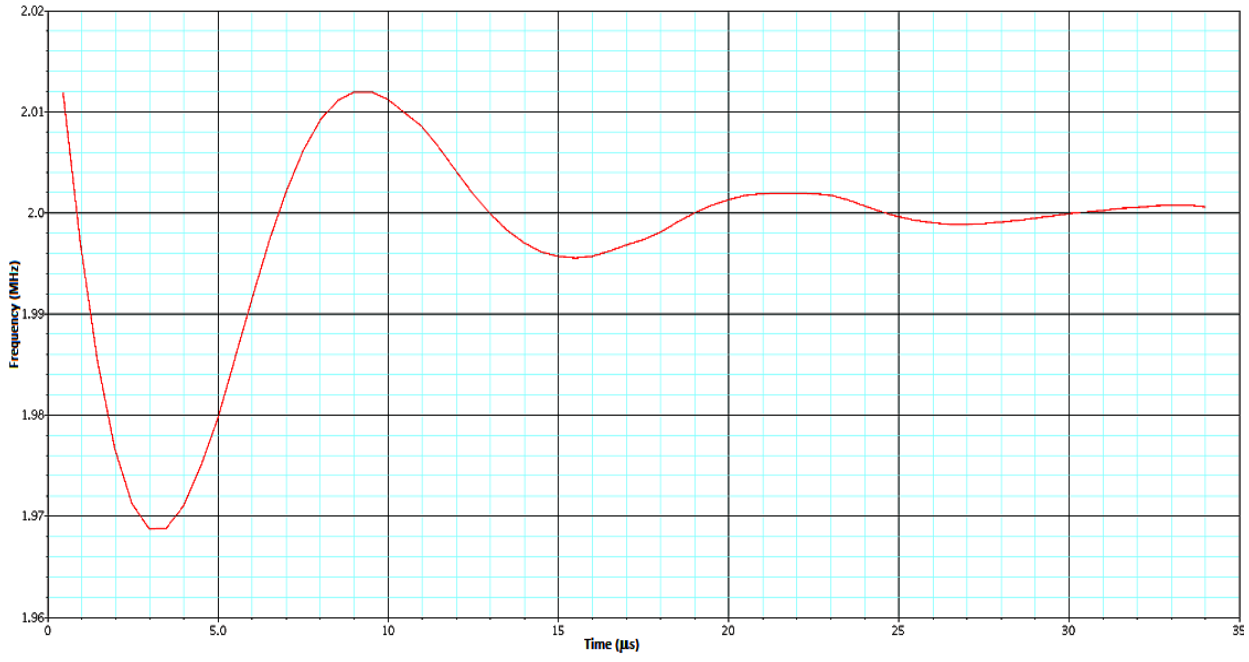

Figure 4.6. Divider output frequency plot during PLL closed loop simulation

4.2 Layout Design Considerations

The individual PLL blocks layout was done and integrated in 130nm IBM-CMOS process using Cadence Virtuoso tool. The layout occupies about 910 µm x 700 µm of area with pads.

4.2.1 IBM-CMOS cmrf8sf Process Info

The cmrf8sf process supports 1.2 V, 2.5 V IO supply devices. An 8-layer metal stack is chosen for this project. They are M1, M2, M3 (3 thin metal), MQ, MG (2 thick metal) and LY, E1, MA (3 Thick RF metal). The thick RF metal layers have very low resistance hence they are used for implementing on-chip capacitors and inductors. This process has a variety of transistors namely low power or high V_T, low V_T, zero V_T and regular MOS transistors. The low power transistors were chosen for designing the analog portion of the PLL block because of their low leakage and low power consumption characteristics. In addition N+ diffusion, P+ ploy, precision poly, silicided poly and K_X thin film resistors are provided in cmrf8sf process. Resistors which can provide the required resistance value are chosen to meet the design specifications. The top three thick RF metal layers are used for implementing on-chip inductors and capacitors. the cmrf8sf process provides both metal capacitors and diffusion capacitors. This process also provides single metal layer, two metal layer series and parallel inductors for use in RF applications. The advantage of metal capacitors over gate-oxide capacitors is that they do not have any parasitic effects with respect to Si substrate. Also, the capacitance will not vary with applied body voltage in metal capacitors. Therefore, the cmrf8sf process is best suited for low power, high performance RF circuit design applications such as Bluetooth, WLAN and GPS.

4.2.2 Layout Design Guidelines

The below mentioned layout guidelines are followed in drawing the PLL layout.

- No long metal traces are used unless required
- Sufficient gap between adjacent metal traces is provided to avoid signal or noise coupling
- Orthogonal power supply and signal rails are drawn to avoid power supply coupled noise induced onto the signal traces
- No bends in short signal traces (in the order of quarter wavelength) to avoid transmission line effects
- Substrate ring around the MOS transistors help in suppressing the substrate noise
- Digital traces are drawn with sufficient thickness to reduce delay
- Narrow metal traces are avoided for reduced ohmic loss
- Non-minimum device geometries are used for better performance
- Tie downs are used to avoid floating gate or antenna error i.e. the risk of gate-oxide break down

The differential charge pump block was drawn as symmetrical as possible to avoid any mismatch effects. The below mentioned layout effects were taken into consideration while drawing the PLL layout.

Latch up: All the transistors used in PLL circuit from the cmrf8sf design library are provided with a default substrate guard ring. So, the transistors are inherently latch up free and no extra

measures are taken to avoid it. P-substrate contacts and N-well contacts are made wherever it is required.

Electro-migration: Electro-migration is the process of degradation of metal interconnects due to high current density or high temperature. Redundant via is used in the design to avoid wearing off the metal at joints. Also, the metal traces are made sufficiently thick based on the current that need to flow through the metal trace and the current density limitation of the metal rail.

Hot Carrier Effect: Hot carriers are created by high electric fields. Under the influence of a huge electric field the channel or substrate carriers displace and get trapped in the gate-oxide region. In result, it affects the threshold voltage of the device and hence, disrupts the normal operation. It is mainly caused by high signal switching times. So, the signals with high duty factors are avoided to the best possible.

Floating Gate Effect: A floating gate is a poly which is not electrically connected to the N+ diffusion or P+ diffusion. The ratio of poly to metal beyond a certain proportion would disrupt the gate-oxide and hence damages the device. So, an N+ diffusion to substrate tie down is provided in the PLL design to clamp the high voltages to ground without damaging the gate oxide.

4.2.3 Post Layout Checks

Once the layout is done, Design Rule Check (DRC) is performed on each individual circuit layout block using both ASSURA and DIVA tools. After the layout passes DRC, the Layout Versus Schematic (LVS) check is done on each individual block using both ASSURA and DIVA tools. Following that, QRC extraction is done on each layout block which is LVS clean for extracting the parasitic components using ASSURA RCX tool. Capacitive parasitic (C

only) components are only extracted from the layout instead of both RC (resistance and capacitance parasitic) because of some technical limitations imposed by the tool. Simulation with post extracted layout is performed on each individual block to ensure that the circuit works after receiving the fabricated IC. Finally, all of the above mentioned DRC, LVS, QRC steps are repeated on the integrated PLL block. Figure 4.7 shows the PLL layout with pads sent to foundry for fabrication. It also shows the pad names and the respective IC package pin numbers.

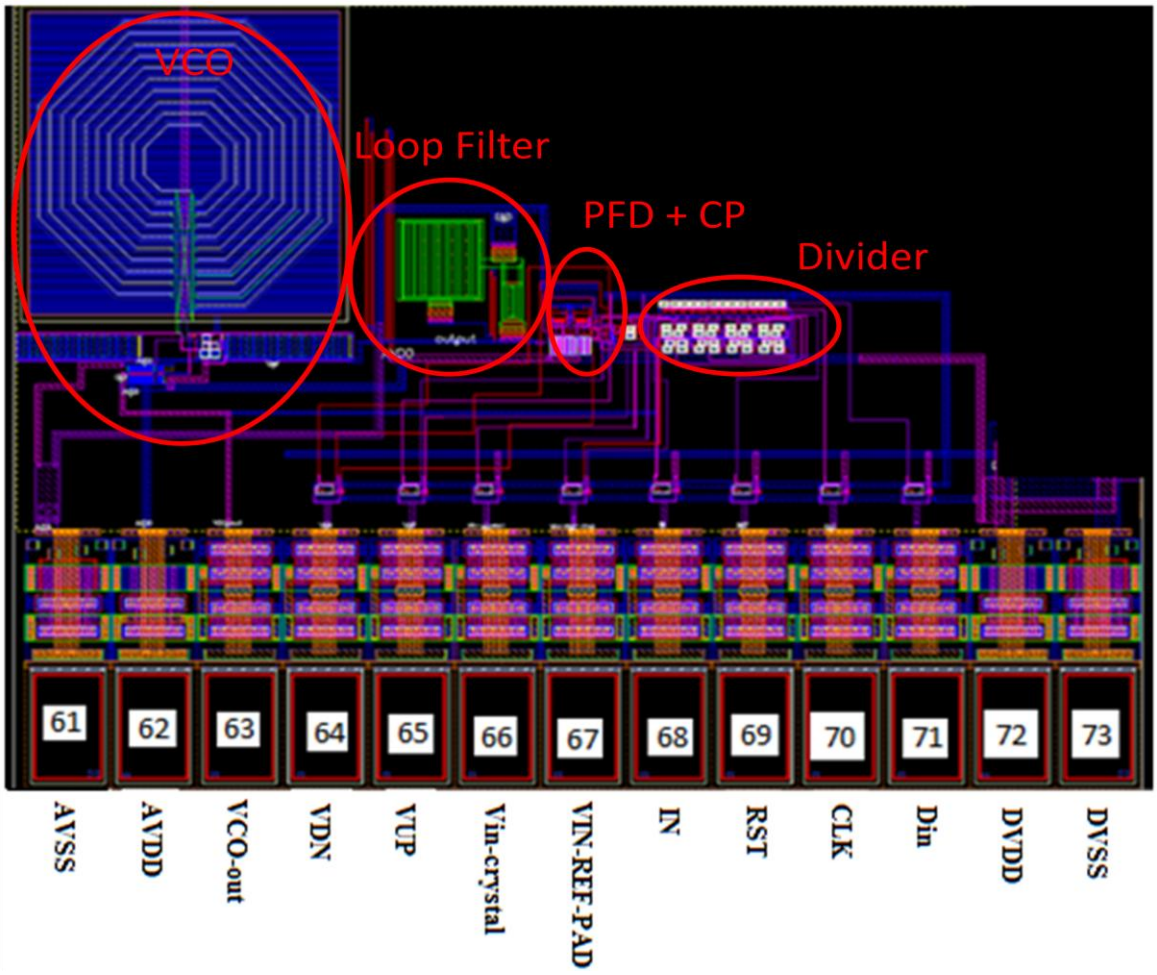

Figure 4.7. Complete PLL layout with pads

4.2.4 Layout issues needs to be addressed

Though proper layout guidelines were followed in drawing the individual PLL blocks layout, it can be improved further in terms of arrangement of the sub blocks and the floor plan. The following improvements could be done to the existing integrated PLL layout.

- Gap between the pads and the complete integrated PLL block can be reduced.
- Divider can be placed beneath the PFD, CP, LPF blocks in such a way that the divider input is very close to the VCO output and the divider output is close to the PFD input. Reducing the length of metal trace carrying 866 MHz signal helps in avoiding the transmission line effects and additional parasitic.
- Charge pump layout can be done using common-centroid layout technique to achieve better matching of the differential pair transistors.
- Though the individual blocks are spread out sparsely because of available die area, all other sub blocks except VCO could have been very well fit beneath the VCO block.

The following figure 4.8 shows all the circuits namely the PLL, the dead-time generator and the ADC taped out by team at UA in AUG 2010. Appendix II shows the complete GAANN-ROKE die layout taped out in AUG 2010. It consists of an ARM core and couple of other blocks (band gap reference, Mixer etc.) designed by the team at University of Southampton along with the UA circuits.

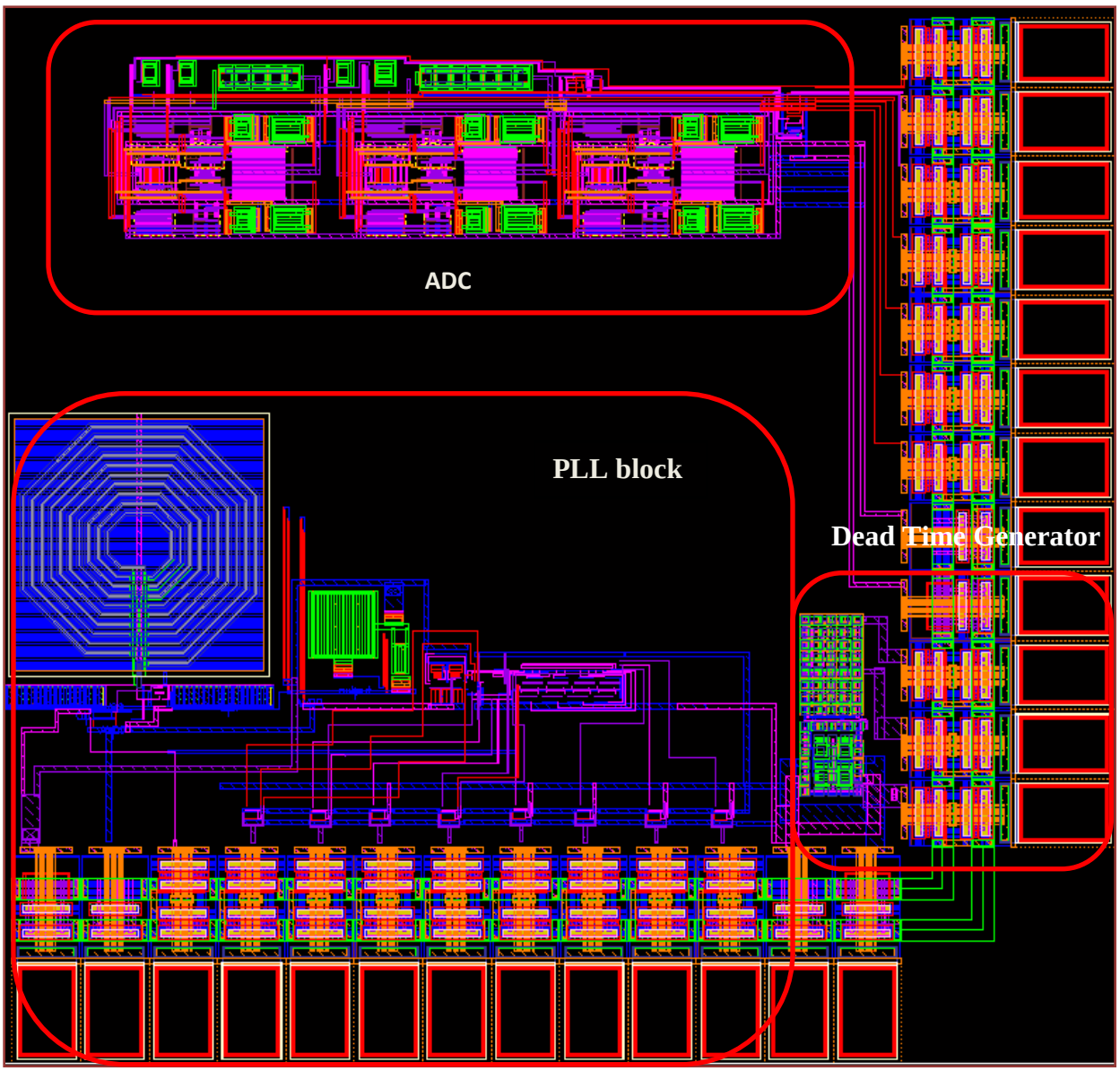

Figure 4.8. GAANN-AUG 2010 Complete UARK die layout.

Chapter 5

Testing

The on-chip blocks are interconnected in such a way that it requires the least pad count. Four on-chip multiplexers are used to interface the PFD and the charge pump and another multiplexer to join the frequency divider and the PFD. The multiplexer in combination with the tristate buffer helps in both input and output. Also, it decreases the required pad count and hence the occupied die area. A 13-bit on-chip serial-in, parallel-out shift register is designed for feeding in the digital logic data to the on-chip circuitry. All the selection bits for the multiplexer and modulo bits for the frequency divider come from the on-chip shift-register. The frequency divider needs an 8-bit digital input for programming the required divider ratio and the other five bits of data controls the selection inputs of the multiplexers as well as the enable function of the tristate buffers. This on-chip shift register is designed using 130nm IBM-CMOS process. Also, to minimize the number of pads the digital VDD and GND are combined with the adjacent circuit DVDD and DVSS pads eliminating redundant ones.

Figure 5.1 shows the on-chip arrangement of the blocks as explained above. The Ext VUP, Ext VDN and EXT input pins (Vin-ref-pad) are connected to three bi-directional pads. They act as output pins when EN is logic ‘1’ and takes in the external input when EN is logic ‘0’. So they perform the dual function of outputting VUP, VDN and frequency divider signals and feed in the external inputs to those pins.

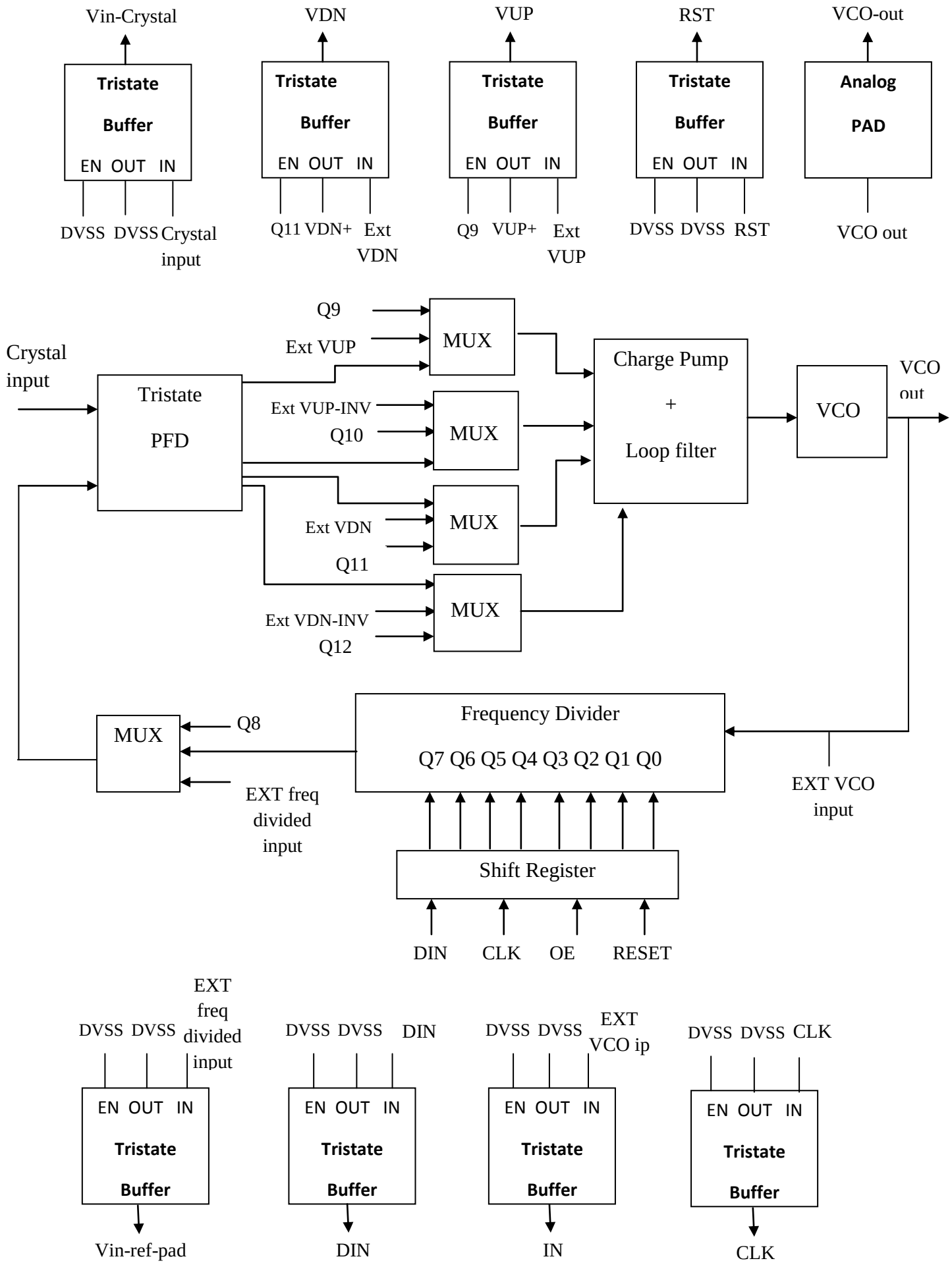

Figure 5.1. On-chip PLL blocks arrangement

5.1 External Data Feeding Circuitry

An external data feeding circuit has been designed using two 8-bit CD74HC165E shift registers, and a mechanical switch with a 555 timer programmed as a Schmitt trigger for switch de-bouncing. The de-bounced switch generates the clock (CLK) pulse required for both the external and on-chip shift registers. Two 8-bit shift registers are connected in series to feed in the 13 bit data serially on to the on-chip shift register. These external shift registers are capable of taking in both the asynchronous parallel inputs and a serial input and produces a synchronous serial output. Figure 5.2 shows the external discrete component arrangement explained above. The output signals (DIN, CLK) obtained from this setup are shown in the Figure 5.3. The below mentioned shift register data needs to be fed in for closed loop operation of the PLL.

Shift Register I: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7

1 0 0 0 1 1 0 1

Shift Register II: Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 ~ (Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15)

1 1 1 1 1 0 0 0

The shift register I bits decide the division ratio of the frequency divider. The above mentioned shift register I data programs the divider for a divide-by-433 operation. The general equation defining the output divider ratio with division bits is given by

Divider ratio = $Q_0 + 2Q_1 + 4Q_2 + 8Q_3 + 16Q_4 + 32Q_5 + 64Q_6 + 128Q_7 + 256$

The shift register II bits select the appropriate data at multiplexer's input. The shift register II data feeds in first and occupies the most significant digit places in the on-chip shift register. Table 5.1 clearly explains the functionality of each of the 13 bits of the on-chip shift register. Each of the IO pins description is provided in Table 5.4.

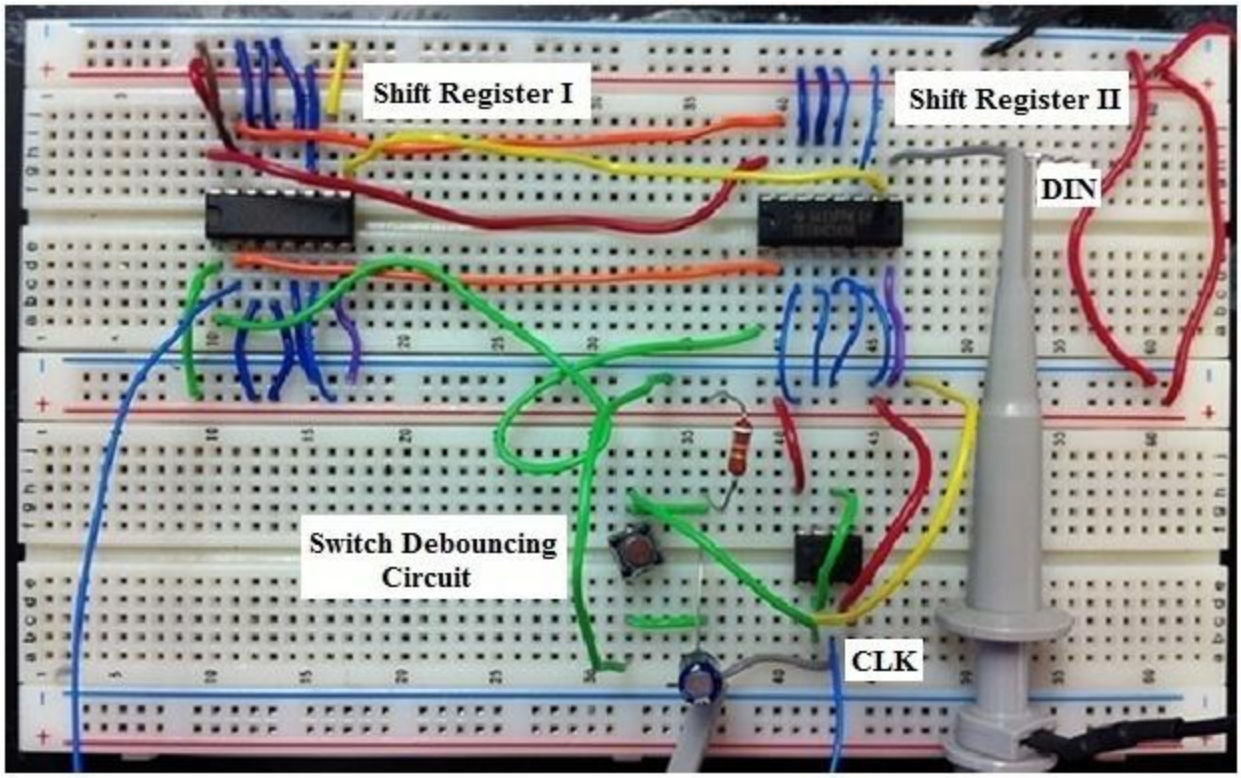

Figure 5.2. External discrete component arrangement for DIN, CLK generation

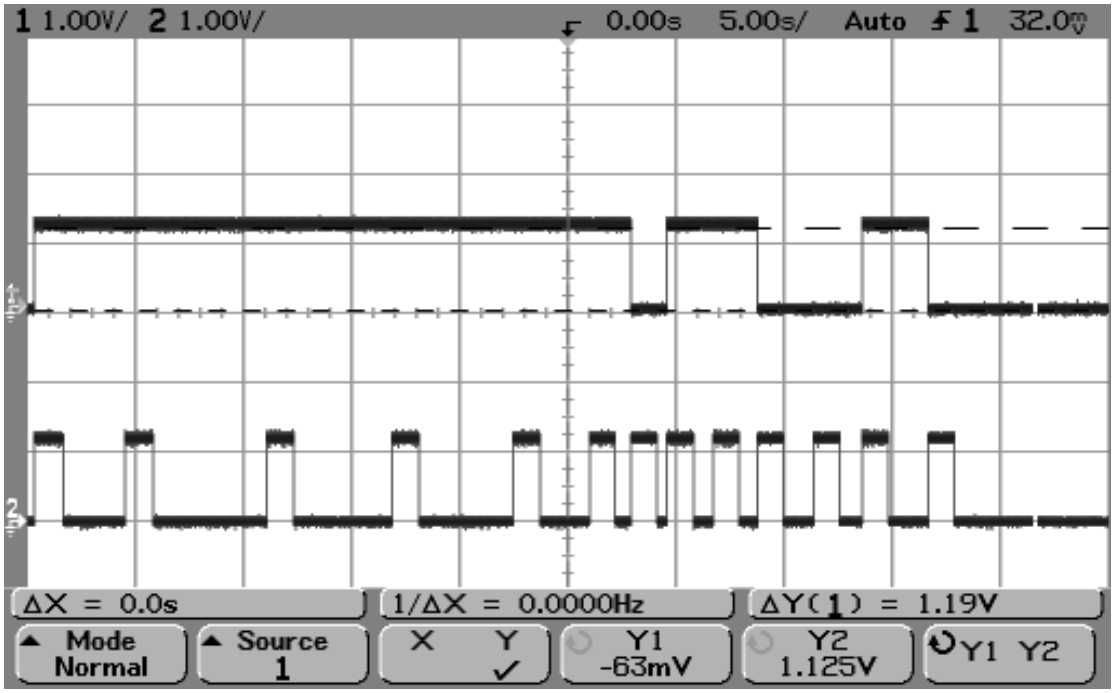

Figure 5.3. Externally generated DIN, CLK signal waveforms

Table 5.1 Shift-register Bit Function Description

	Function	Bit '0'	Bit '1'
Q0-Q7	Programs the frequency divider & decides the divider ratio	÷256 if all '0's	÷511 if all '1's
Q8	Configures MUX & tristate buffer to allow either external PFD input or read Divider output	Allows external input to PFD & Disconnects the internal divider output connection to PFD input	Outputs divider output for read & no external PFD input is allowed
Q9,Q10	Configures MUX & tristate buffer to connect PFD output (V_{UP+}, V_{UP-}) to CP input internally and also allows to read PFD output(V_{UP+}) at the pad [OR] allow external CP input and disconnect the internal PFD-CP connection	Allows external CP input and disconnects the internal PFD-CP connection. No PFD output (V_{UP+}) can be read at the output pads.	Connects PFD output (V_{UP+}, V_{UP-}) to CP input internally and also allows to read PFD (V_{UP+}) output at the pad
Q11,Q12	Configures MUX & tristate buffer to connect PFD output (V_{DN+}, V_{DN-}) to CP input internally and also allows to read PFD output(V_{DN+}) at the pad [OR] allow external CP input and disconnect the internal PFD-CP connection	Allows external CP input and disconnects the internal PFD-CP connection. No PFD output (V_{DN+}) can be read at the output pads.	Connects PFD output (V_{DN+}, V_{DN-}) to CP input internally and also allows to read PFD (V_{DN+}) output at the pad

5.2 PCB design:

A printed circuit board (PCB) has been designed for testing the frequency synthesizer IC. A two layer board with a ground plane has been chosen for this purpose. Figure 5.4 shows the PCB layout designed using EAGLE software. Below mentioned set of rules are followed in designing this board.

- LT3021 regulator is used for 1.2 V supply to suppress the power supply noise

- Decoupling capacitors of 0.01 µF are placed close to the chip on PCB to stop the high frequency supply noise from being fed to the circuit
- Via and cross-overs are avoided for reducing the parasitic capacitance and inductances
- BNC connectors are terminated with a 50 Ω impedance to ground for impedance matching with the oscilloscope probe
- Short metal traces are run for high frequency RF signal to avoid transmission line effects
- Jumpers are avoided on high frequency signal traces to avoid inducing parasitics and therefore the associated noise
- A copper ground plane is used for suppressing the analog and digital signal noise and to avoid noise interference with the other signal traces on the board
- Moderate copper thickness is maintained for all the on-board traces for good thermal performance
- SMA connectors are made available on board for over temperature testing using the cryo chamber

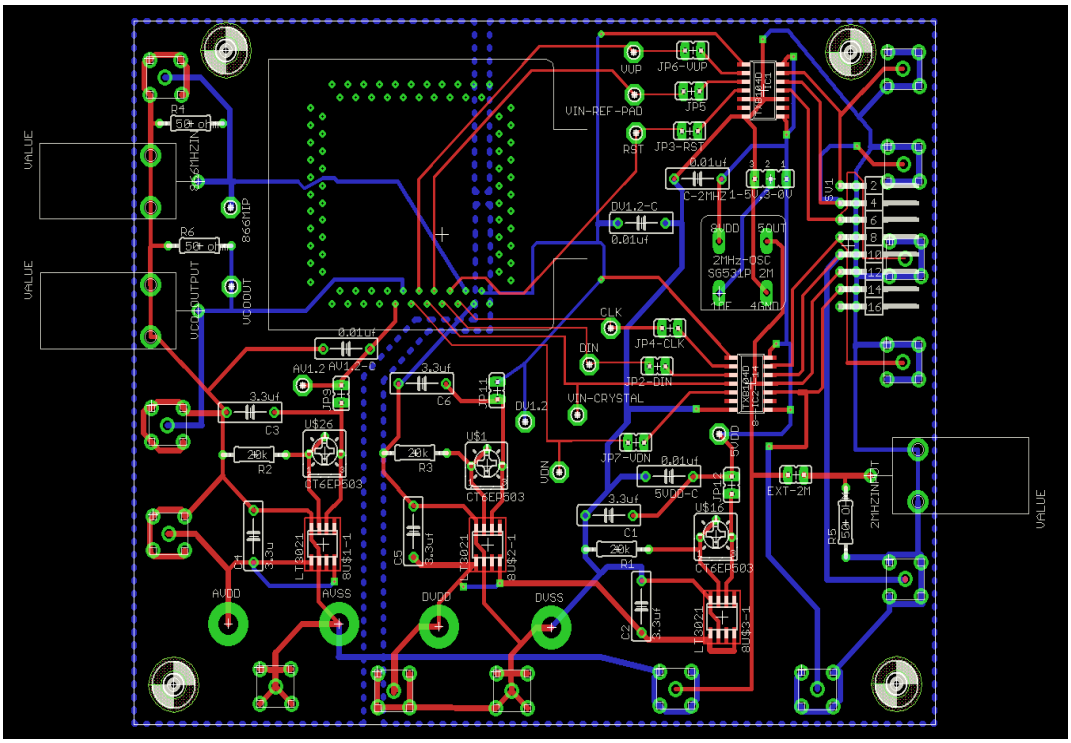

Figure 5.4. PCB test board schematic

5.3 Bench Test Results

The individual PLL blocks functionality has been tested and verified at the room temperature. Phase frequency detector works as expected at the required 2 MHz frequency. An expected frequency divided signal is observed at the output of the frequency divider. Charge pump and the loop filter combined output is integrated with VCO input internally on-chip. So, the CP and LPF do not have any pad outs to verify their functionality individually. But, the integrated CP, LPF, VCO blocks appeared to be working fine except that the VCO does not have a long input tuning range i.e. the VCO frequency does not vary gradually over a range of input control voltage. Instead, the VCO oscillates only either at 867 MHz in the stable state or at 967 MHz when input control signal is at 1.2 V. Because of extremely low VCO signal strength the closed loop PLL functionality could not be observed at room temperature.

Figures 5.5, 5.6 and 5.7 show the VCO frequency spectrum obtained from a spectrum analyzer. The charge pump and low pass filter could not be tested individually. So, all the three CP, LPF and VCO blocks were tested together on the bench. When both the charge pump inputs were fed 0 V, a tiny -66dBm VCO signal was observed on the spectrum analyzer oscillating at 867 MHz. When the charge pump positive input was raised gradually by pumping in the discrete pulses no change in VCO frequency was noticed and vice versa. When stream of pulses were fed to the CP positive input or equivalently a 1.2 V dc signal, the VCO frequency jumps to 967 MHz. Similarly, when the CP negative input is supplied with a stream of pulses or a 1.2 V dc input, a slight drop in VCO frequency in noticed i.e. an 863 MHz signal with -64.5 dBm signal strength.

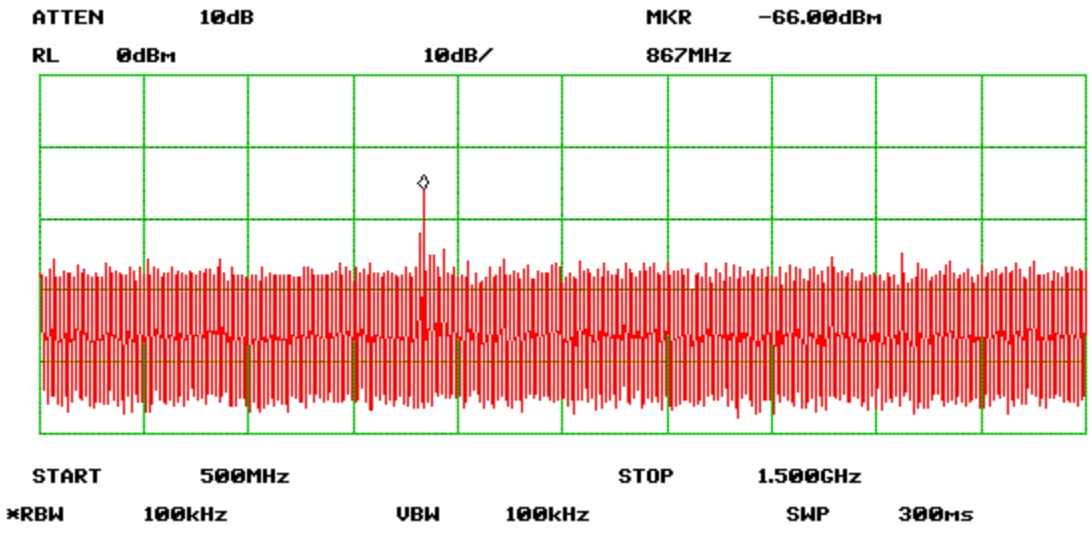

Figure 5.5. VCO signal spectrum with VUP-0v, VDN-0v and oscillating at 867 MHz

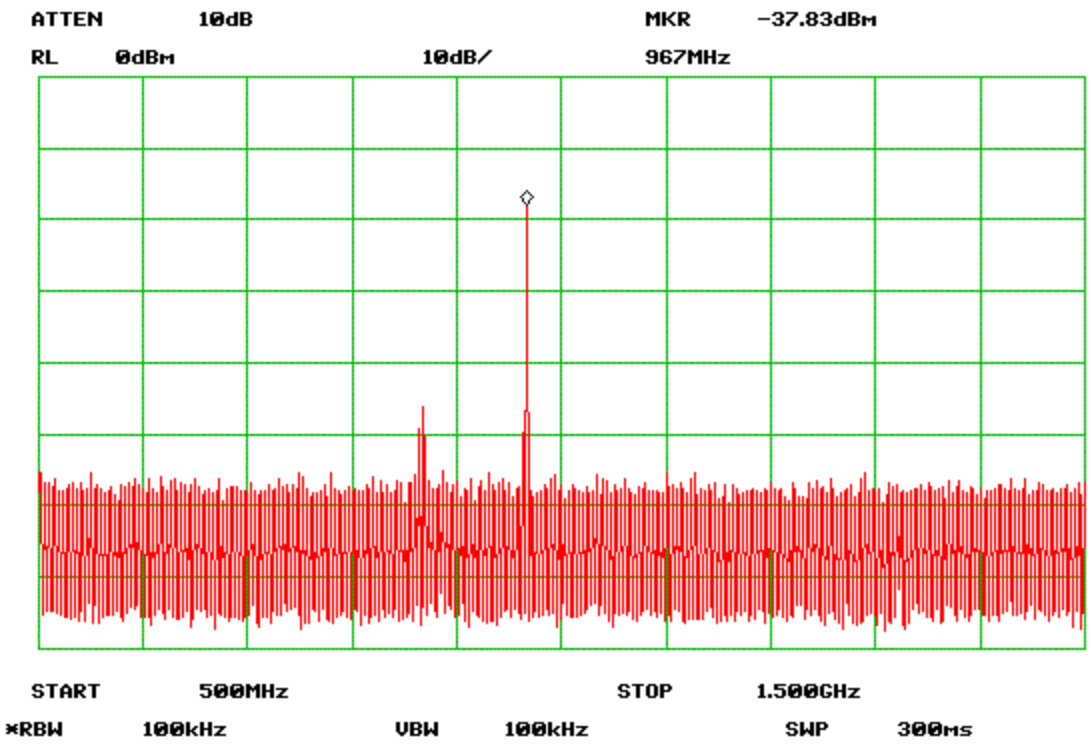

Figure 5.6. VCO signal spectrum with VUP =1.2 V, VDN =0 V and oscillating at 967 MHz

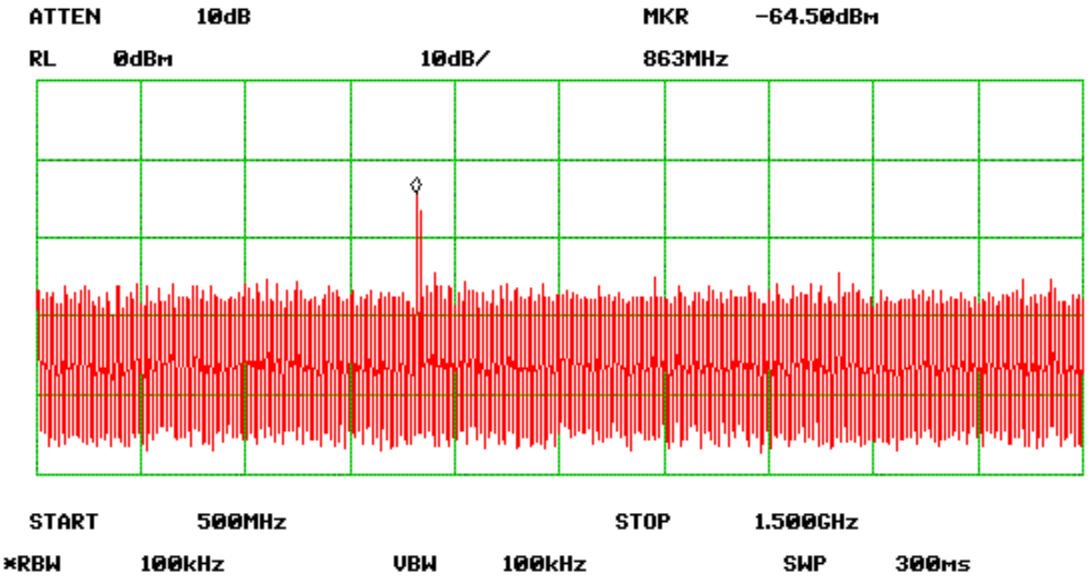

Figure 5.7. VCO signal spectrum with VUP= 0 V, VDN=1.2 V and oscillating at 863 MHz

There were issues while testing the frequency divider circuit. Firstly, the required bit pattern for a divide-by-433 operation could not be fed in. The shift register data was prone to noisy input clock pulses. So, a fixed logic '1' is being fed to all the data bits which program the divider ratio to divide-by-511 instead of divide-by-433. Secondly, the VCO output is directly connected to the divider input internally. This internal connection was made based on two reasons.

1) 866 MHz frequency signal cannot be fed in externally because of high pad capacitance
2) Assuming that the analog power supply (AVDD) can be turned off while testing the digital divider

The analog and digital power supplies were shorted because of the common pad ring. Therefore, the frequency divider could not be tested with an external input signal when the whole chip is powered up with a 1.2 V supply voltage i.e. the oscillating VCO signal affects the external divider input signal. So, the VDD had to be brought down from 1.2 V to 0.6 V to suppress the effect of VCO signal on the externally fed in divider input signal.

At 0.6 V power supply, a theoretically expected output signal is observed at the divider output on the bench. Figure 5.8 shows the 29.35 kHz signal obtained at the divider output after a divide-by-511 with a 15 MHz external input signal. Similarly, a 194.5 kHz signal is observed at the divider output after a divide-by-511 with a 100 MHz input signal as shown in the Figure 5.9. At higher frequencies, operation of the divider is effected by the running VCO oscillations and the additional pad capacitance imposed on the signal trace. Divider input would not receive the sharp signal transitions and the divider would not respond as it is expected to beyond 100 MHz external frequency input. So, functionality of the divider could not be verified at room temp beyond 100 MHz frequency.

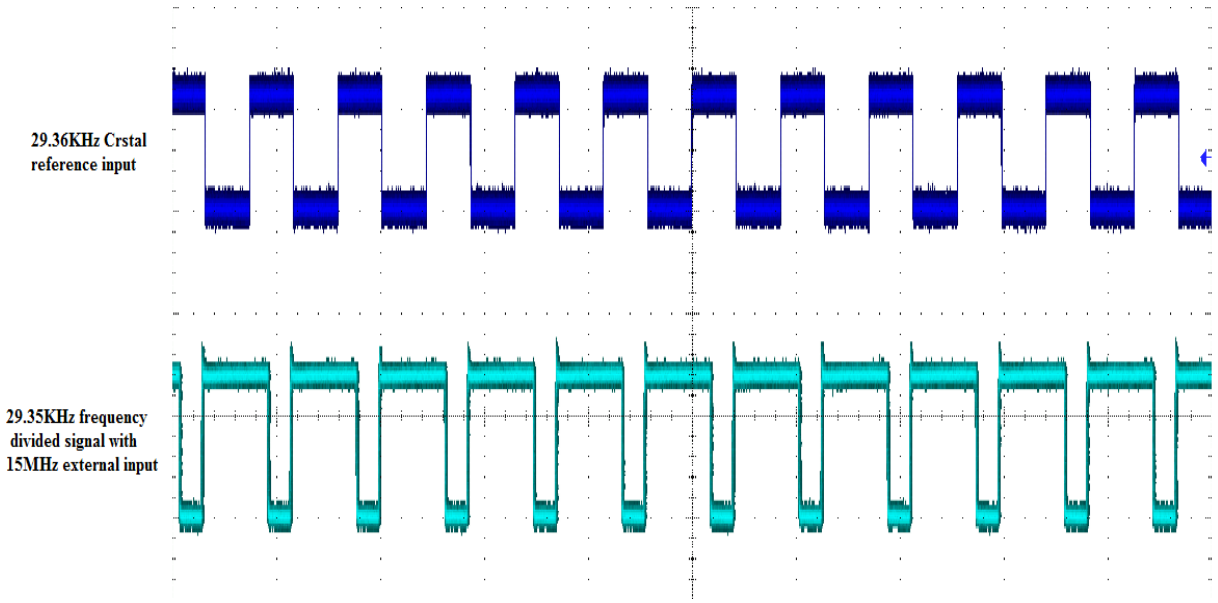

Figure 5.8. A 29.35 kHz signal at the divider output with an external 15 MHz input (divide-by-511)

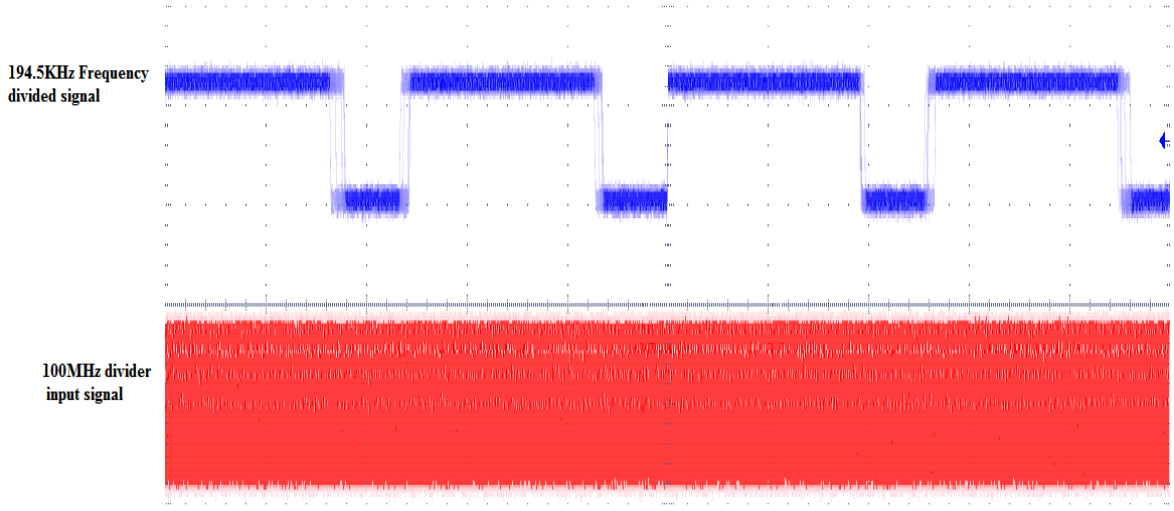

Figure 5.9. A 194.5 kHz signal at the divider output with an external 100 MHz input (divide-by-511)

The 29.35 kHz divider output signal generated is internally fed to one of the PFD input. A positive pulse is observed on the VUP rail as the crystal input reference signal leads the

frequency divider output signal. Similarly, a positive pulse appears on the VDN rail when the crystal input signal lags the frequency divided signal at the PFD input. Figures 5.11 and 5.12 show the PFD outputs obtained at 29.35 kHz frequency. Whenever the two PFD input signals are in phase, the in-built reset circuitry triggers and resets both the outputs. Hence, no pulse signal will appear at the PFD output when both the inputs are in phase as shown in the Figure 5.13.

Figure 5.10 shows the PFD sensitivity graph plotted for a 29.35 kHz input signal for four cycles. For every signal cycle, with increasing phase difference at the PFD input, the average voltage of the output VUP pulse increases gradually and then drops down to zero at the end. Table 5.2 lists the measurements of change in PFD output VUP pulse-width with increasing delay, obtained from the test bench.

Table 5.2 PFD Delay Vs Average Output Voltage

Delay (µs)	VUP pulse width (µs)	Average pulse voltage(V)
10	23.49	0.829058824
20	13.8	0.487058824
30	4.053	0.143047059
34	33.43	1.179882353
45	23.15	0.817058824
55	12.46	0.439764706
60	7.316	0.258211765
68	32.99	1.164352941
80	22.37	0.789529412
95	6.651	0.234741176
102	1.101	0.038858824
105	31.6	1.115294118
120	14.93	0.526941176
130	5.565	0.196411765
136	0.466	0.016447059

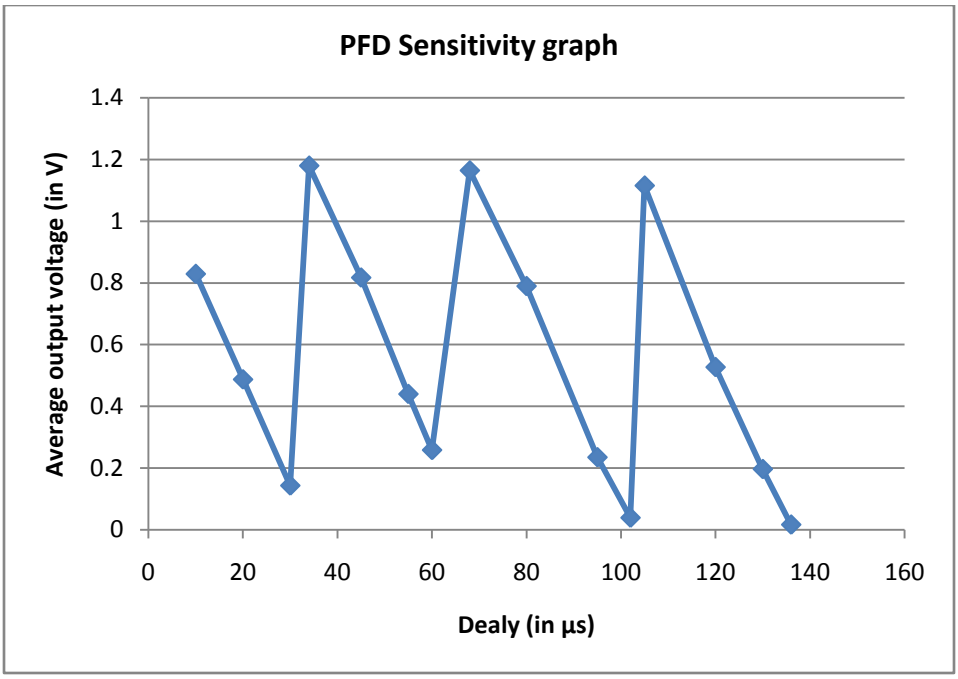

Figure 5.10. PFD sensitivity graph with data obtained from the test bench

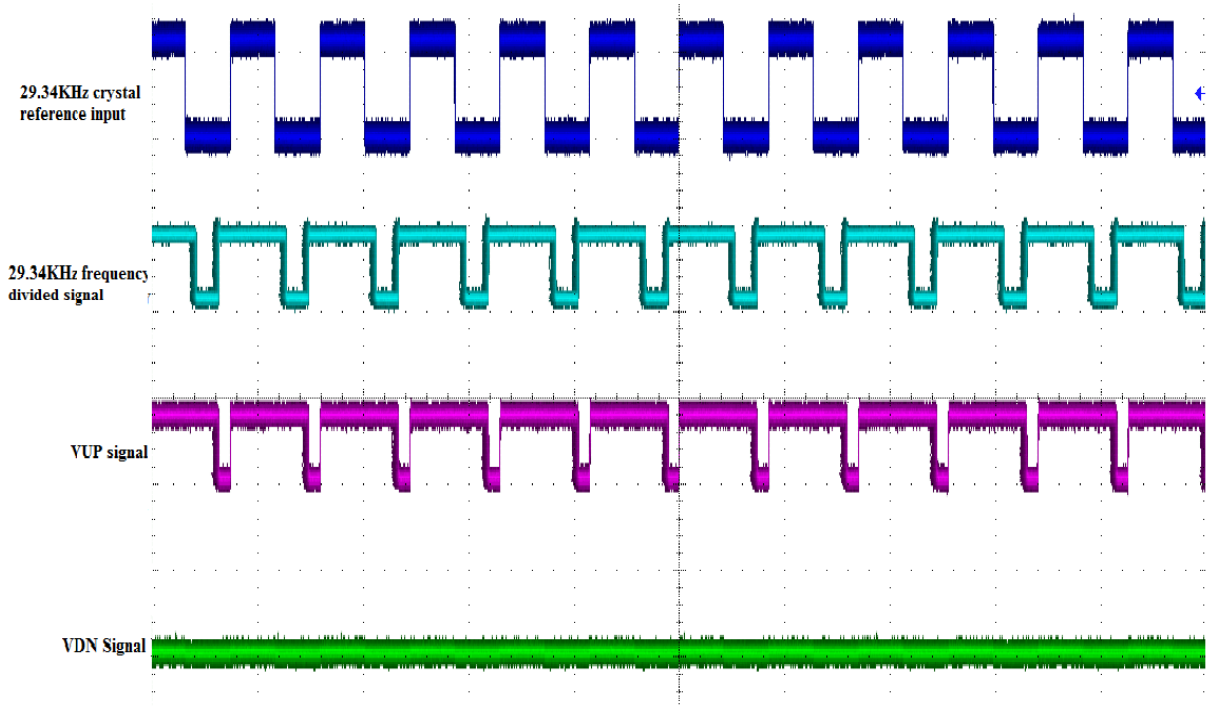

Figure 5.11. A positive VUP pulse as a result of leading PFD crystal input reference

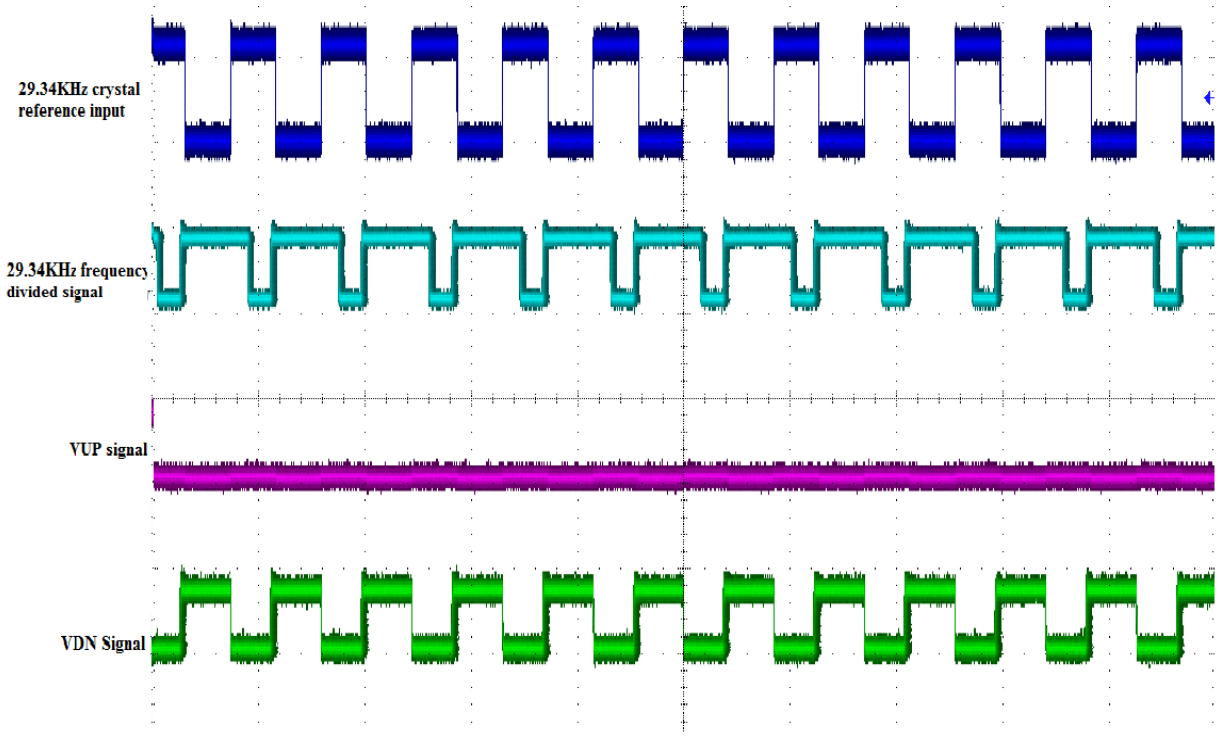

Figure 5.12. A positive VDN pulse as a result of lagging PFD crystal input reference

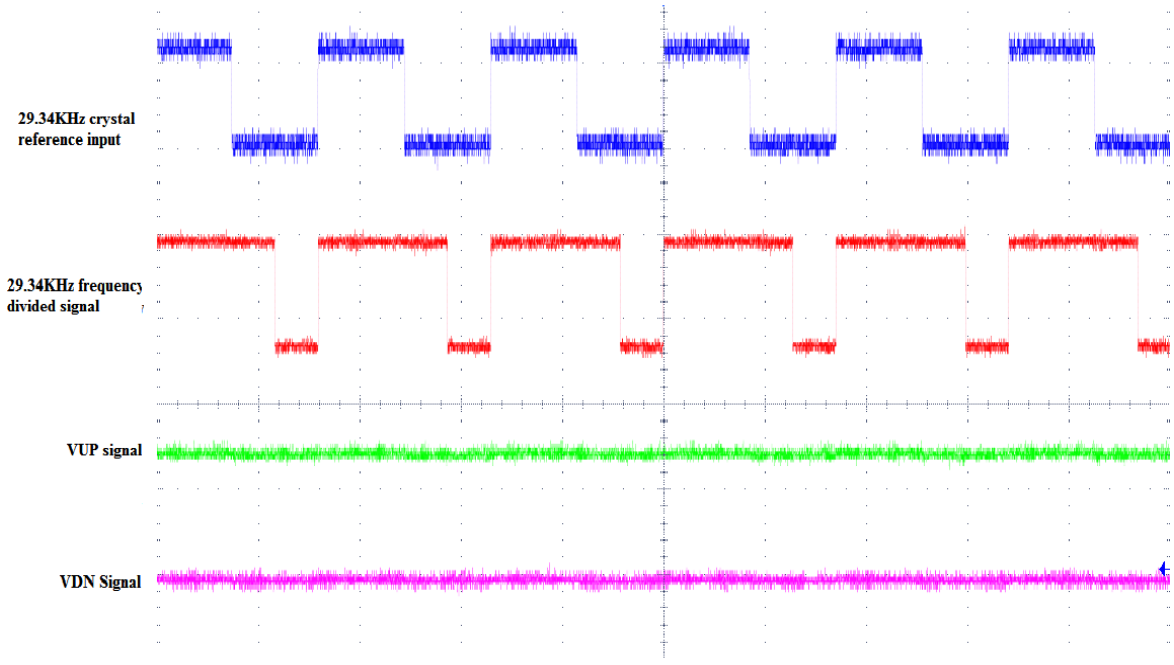

Figure 5.13. No VUP and VDN signal as a result of zero phase difference at the PFD input

At 125 ˚C:

The PFD and the divider have shown similar responses at 125 ˚C as those at room temperature. But, the VCO stops working after 85 ˚C and does not oscillate at all at 125 ˚C temperature.

At -50 ˚C:

The circuit was tested at -50 ˚C temperature. Both the PFD and divider functionality has been verified at the rated frequencies. PFD works perfectly at 2 MHz frequency and the divider does a divide-by-511 with 984 MHz on chip VCO signal resulting in 1.93 MHz output.

The closed loop functionality of the PLL loop could be observed at -50˚C. In stable state i.e. with zero input phase difference loop oscillates at 861 MHz frequency instead of 866 MHz. When the crystal input reference frequency is varied to introduce some positive phase difference, the VCO frequency increases as it is expected to and oscillates about 984 MHz.

Figure 5.14 and figure 5.15 shows the divider and the PFD outputs obtained from the test bench while the PLL is running in closed-loop mode. A 1.929 MHz and 1.933 MHz signal is observed at the divider output after a divide-by-511 when the PFD input phase difference is set at two different values i.e. VCO responds to the input phase variation and correct its frequency accordingly in the neighborhood of 984 MHz. Therefore, the divider output frequency changes with varying VCO frequency at its input. But, the loop does not correct itself and the phase difference at the PFD output will not become zero by itself when the phase difference is induced externally by varying the reference frequency. So, the loop locking mechanism was not observed on bench.

When the 1.929MHz signal is compared with an externally supplied 1MHz signal, a somewhat erratic variation in VUP, VDN outputs is observed as in figure 5.16 and 5.17. It can be because of the reason that the input frequency difference is beyond the designed PLL loop bandwidth which is 200 kHz. The VCO frequency spectrum obtained while the loop is running in the closed loop mode is shown in Figure 5.19 and 5.20.

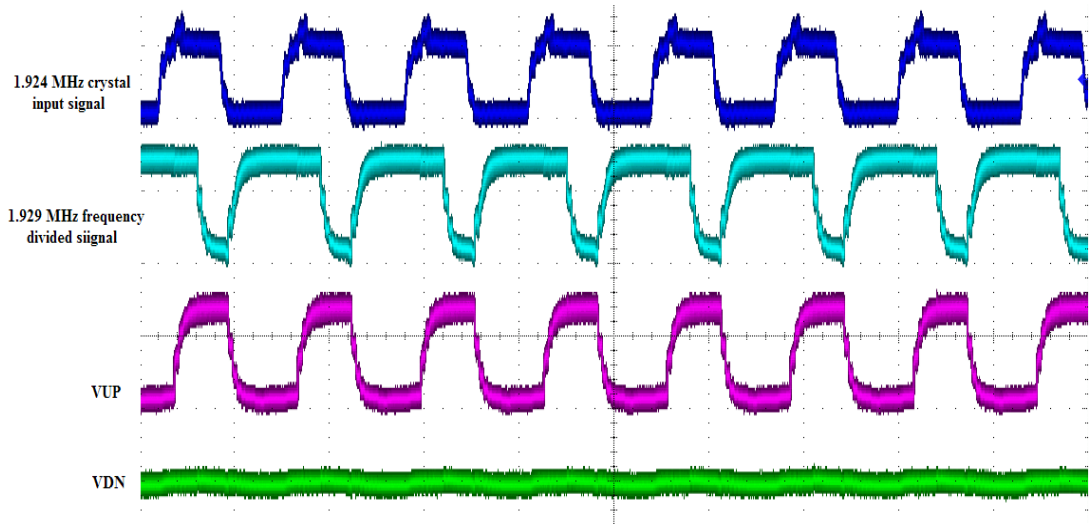

Figure 5.14 A positive VUP signal while the loop runs in closed loop mode

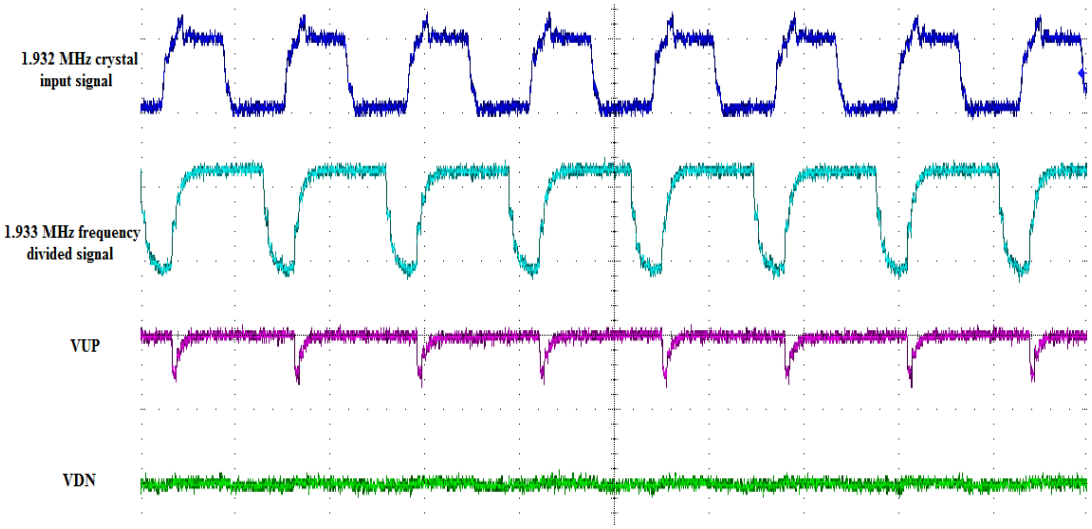

Figure 5.15 A positive VUP pulse when the input phase difference of two PFD inputs was at maximum while the loop runs in closed loop mode

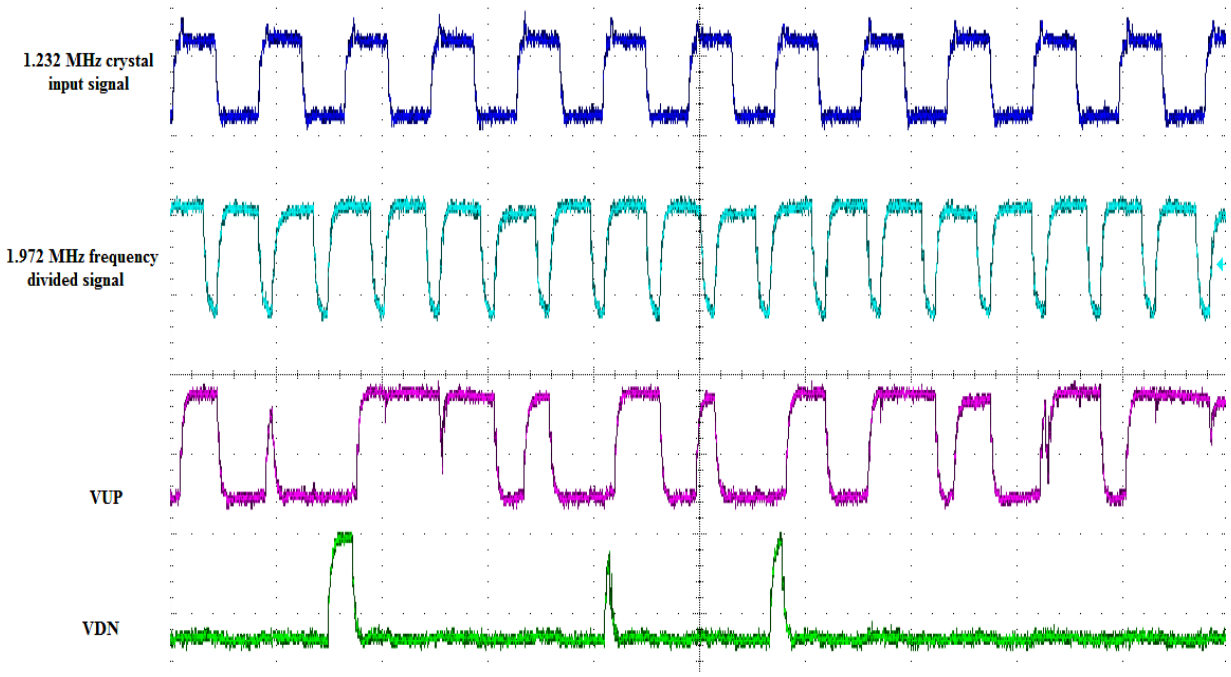

Figure 5.16. PFD and divider output signals observed while the PLL is in closed loop operation

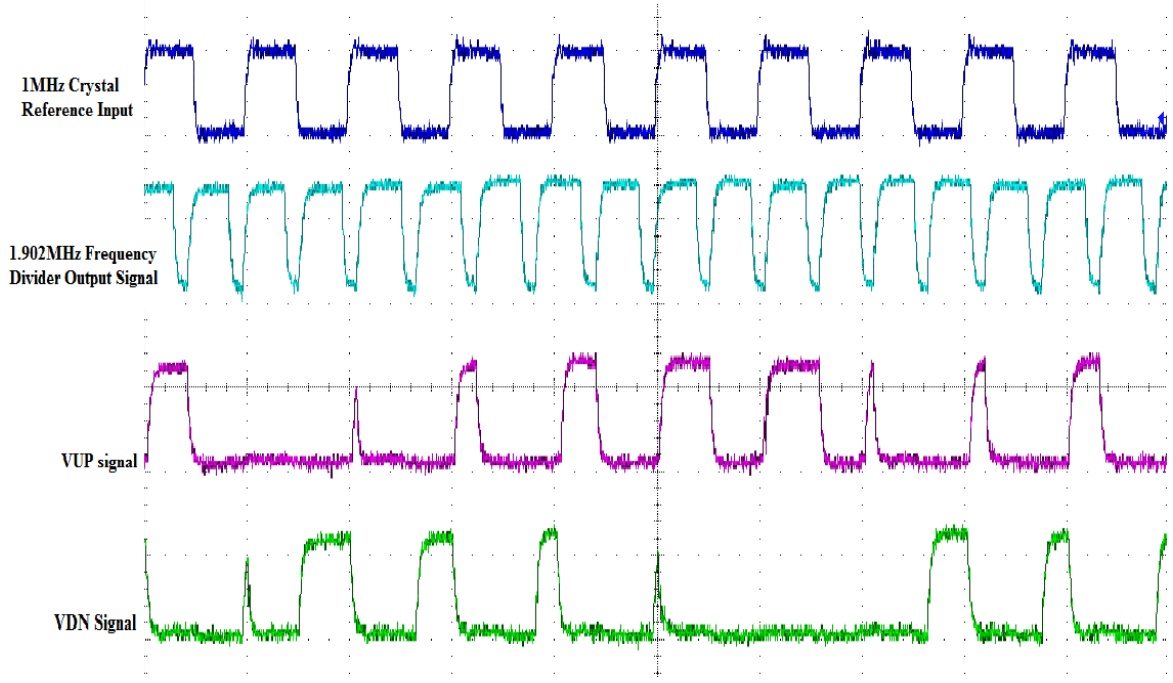

Figure 5.17. PFD and divider output signals observed while the PLL is in closed loop operation

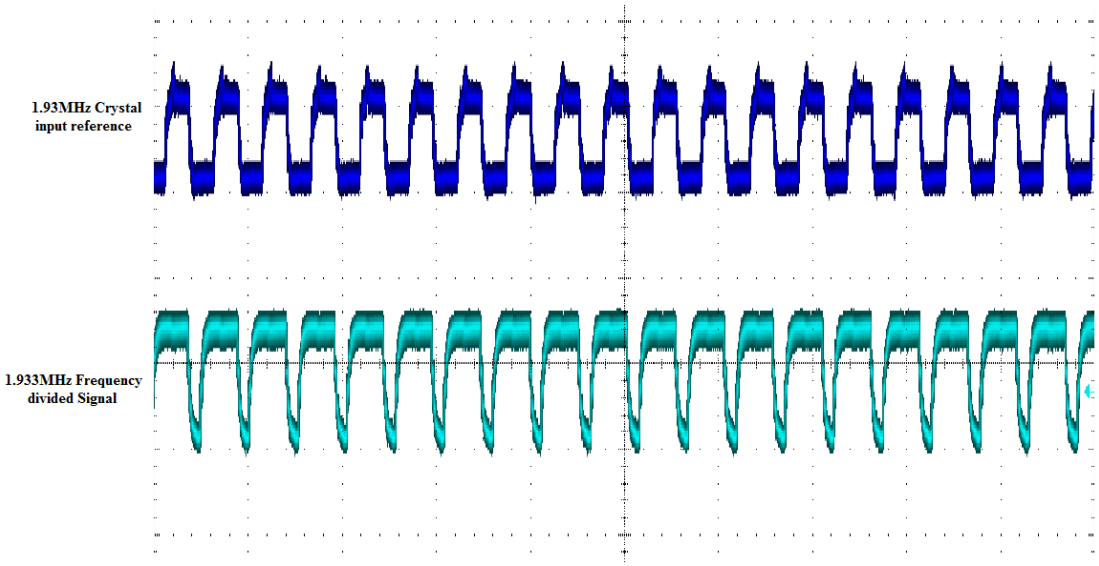

Figure 5.18. A 1.933MHz signal at the divider output while running in closed loop mode

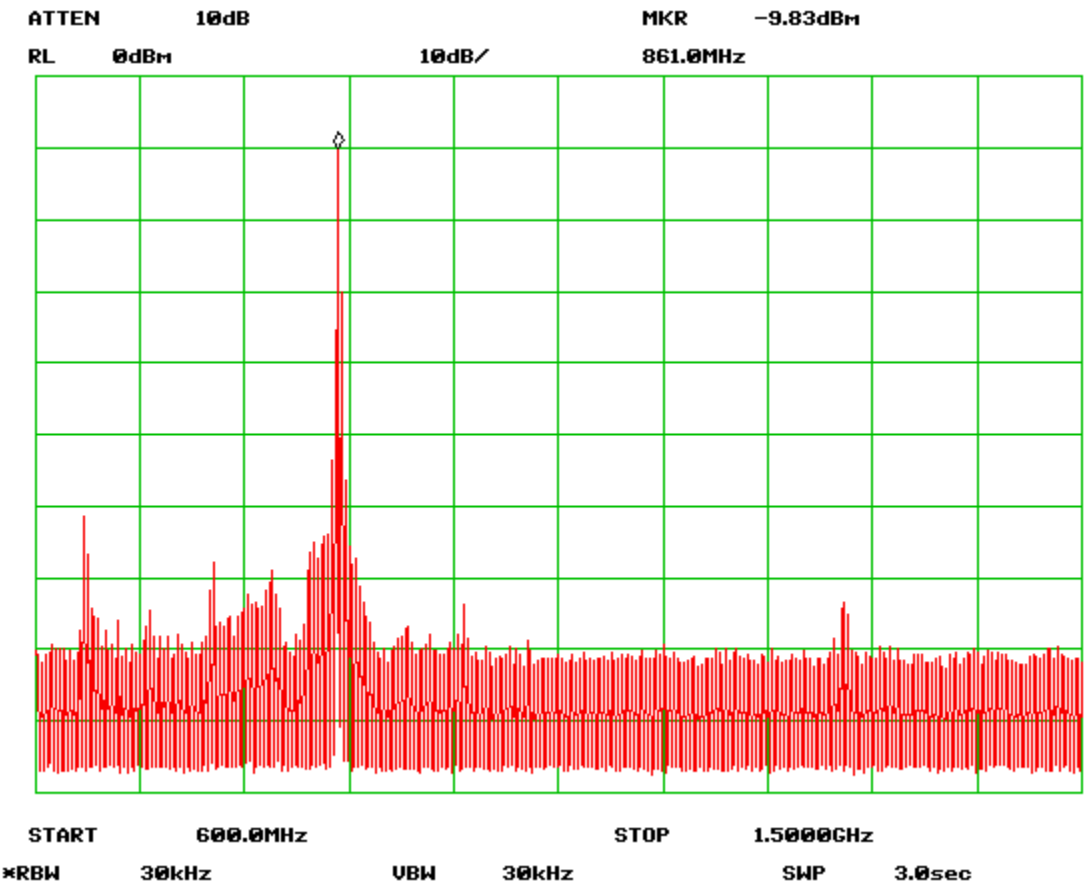

Figure 5.19. VCO steady-state frequency spectrum while operating at -50 ˚C.

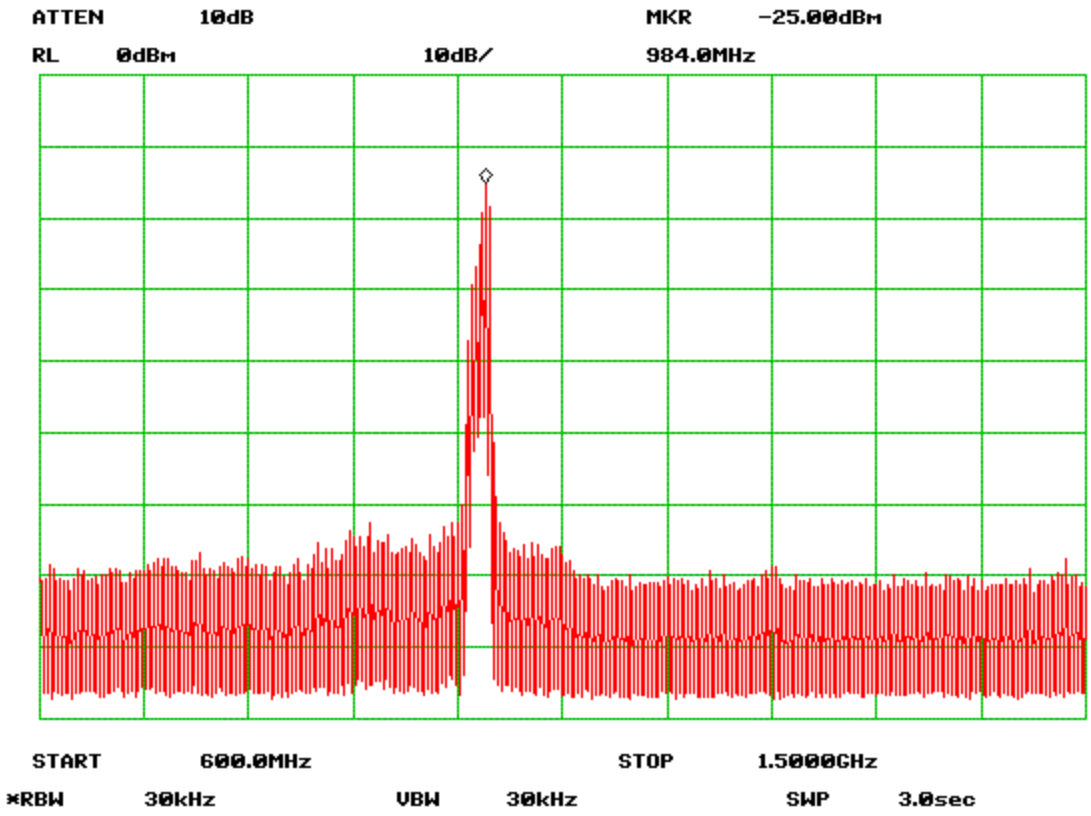

Figure 5.20. VCO frequency spectrum with a constant VUP signal operating at -50 ˚C.

Table 5.3 Equipment Required For Testing

Agilent 54622D Mixed Signal Oscilloscope
Tektronix MSO4104 Mixed Signal Oscilloscope
Hewlett Packard 8563A Spectrum Analyzer
Tektronix AWG5012C Arbitrary Waveform Generator
Agilent 34401A 6 ½ Digital Multimeter
Agilent E3631A Triple Output DC Power Supply
CRYO Chamber
Printed Circuit Board

Table 5.4 Frequency Synthesizer IC - I/O Pin Description

LCC Pin number	Pad name	Pad name description
61	AVSS	Analog ground: 0 V_{AC}
62	AVDD	Analog Power supply: 1.2 V_{AC}
63	VCO-out	Frequency Synthesizer(VCO) Output
64	VDN	External pulse input to charge pump & outputs VDN
65	VUP	External pulse input to charge pump & outputs VUP
66	Vin-crystal	Reference crystal oscillator input to PFD : 2 MHz
67	VIN-REF-PAD	External frequency divided signal : 2 MHz (to feed into PFD) & outputs Frequency divided signal
68	IN	External input to Frequency divider : 0-866 MHz
69	RST	shift register(SR) reset : Active Low Pulse
70	CLK	Clock input to the shift register
71	Din	Data input to the SR : 13 bit pulse sequence
72	DVDD	Digital Power supply: 1.2 V_{DC}
73	DVSS	Digital ground: 0 V_{DC}

Chapter 6

Conclusions and Future Work

In this thesis, different frequency synthesizer topologies, features and merits are analyzed. Finally, a PLL-based frequency synthesizer has been chosen for design as part of the wireless transceiver design project. All the individual PLL sub-blocks namely the phase detector, charge pump, loop filter, voltage controlled oscillator and the frequency divider blocks, design techniques, strategies employed for low power operation, simulation and test results are presented in detail.

A 1.2 V, 866 MHz low power PLL-based frequency synthesizer is designed and fabricated in 130nm IBM 8RF-DM CMOS process. An 866 MHz frequency VCO, 2 MHz crystal reference at the tristate PFD input, 7 µA charge pump output current, 200 kHz bandwidth on-chip loop filter and a programmable frequency divider are used for this purpose. The required transceiver channel spacing for locking at different radio frequencies is facilitated by varying the divider ratio. The whole PLL consumes about 2.89 mW power in simulation.

The functionality of individual PLL circuit blocks has been tested and verified on the bench. The phase frequency detector and the frequency divider work as expected at the rated frequency. The charge pump and loop filter could not be tested individually because of no pad availability on the chip. The combined CP, LPF and VCO block works as expected but, with a limited frequency output range at -50 ˚C. This may be due to either the CP or the VCO circuit not working as they are supposed to. Considering the fact that the individual VCO block has similar behavior, the reason behind this issue can be partially attributed to the limited range functionality of the VCO circuit and is further exacerbated by the resistor divider biasing scheme

used in the output of the charge pump. Finally, it is observed that all the individual PLL blocks work to their full strength while operating at -50 ˚C. But, the loop does not correct by itself and the input phase difference would not become zero automatically. So, the locking mechanism could not be observed on test bench with the existing setup. To conclude, there is room for significant improvement with respect to design and layout. Also, more future work needs to be done to produce a robust PLL.

6.1 Future work:

The following improvements could be done to the existing PLL circuit. The future work includes, but is not limited to:

- Improved design-for-test configuration for the chip
- Perfect locking needs to be achieved by proper integration of the loop filter with VCO
- Run closed loop PLL simulation without the resistor divider and analyze its performance
- Prescaler and a counter preceding the divider stage to improve PLL noise immunity
- Improve layout design to avoid noise and subsequent effects in digital portion of the chip
- ΔΣ modulator can be attached to the existing programmable divider to achieve fractional-N division
- Bias circuit is needed for the charge pump which is immune to power supply and temperature variations
- CML based latches can be used at the initial stages of the frequency divider for reduced power consumption
- Addition of a lock detection circuitry i.e. a digital lock detect signal can be used which will be set high when the phase difference on three successive phase detector cycles is less than a certain time period.

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[1] BOLDED ENTRIES ARE CONSIDERED KEY REFERENCES FOR THIS WORK.

APPENDIX I

MATLAB Routine for obtaining Loop filter design parameters:

- Plug in the Italicized variable values and observe the output bode-plot for good phase margin and cross-over frequency
- *Source :* obtained from ROKE project team at University of Southampton.

```
clear;
CP_I=7e-6;
KPFD=CP_I/(2*pi);
KVCO=300.8e6*2*pi;
C1=10.613e-12;
C2=0.663e-12;
R=300e3;
N=433;
omeganrad=sqrt((KPFD*KVCO)/(N*C1));
damp=(omeganrad/2)*R*C1
omegan=omeganrad/(2*pi)
numLF=[(R*C1) 1];
denLF=[(R*C1*C2) (C1+C2) 0];
LFtf=tf(numLF, denLF);
numVCO=[KVCO];
denVCO=[1 0];
KVCOtf=tf(numVCO, denVCO);
Opentf=(LFtf*KVCOtf*KPFD)/N;
Closetf=(Opentf)/(1+Opentf) ;
P = bodeoptions;
```

```
P.FreqUnits = 'Hz';
sys1 = (LFtf*KVCOtf*(1/1)*KPFD)/N;
sys2=  ((LFtf*KVCOtf*KPFD)/(1+((LFtf*KVCOtf*KPFD)/N))/N);
sysVCOnoise=(1/(1+(LFtf*KVCOtf*KPFD/N)))
% figure(1)
% step(Closetf);
figure(1)
h = bodeplot(sys1,P);
grid on
figure(2)
h = bodeplot(sys2,P);
grid on
figure(3)
h = bodeplot(sysVCOnoise,P);
grid on
```

Result:

Damping factor (ζ) = 1.0776

Omegan (ω_n) = 1.0773e+005

Transfer function =

$$\frac{2.111\mathrm{E}^{-018}\,\mathrm{S}^3 + 1.128\mathrm{E}^{-011}\,\mathrm{S}^2}{2.111\mathrm{E}^{-018}\,\mathrm{S}^3 + 1.128\mathrm{E}^{-011}\,\mathrm{S}^2 + 1.548\mathrm{E}^{-005}\,\mathrm{S} + 4.863}$$

APPENDIX II

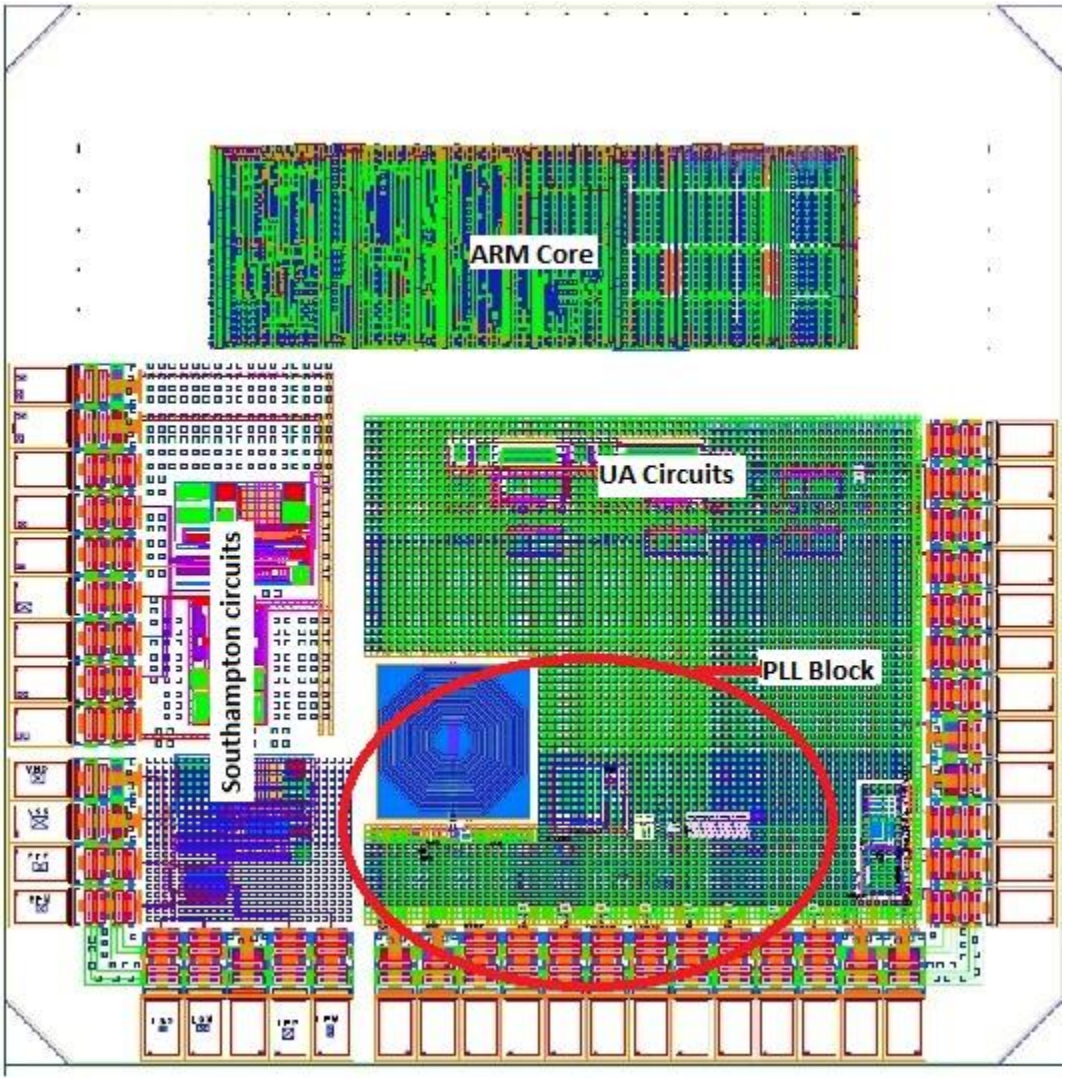

Figure I GAANN ROKE AUG 2010 complete chip

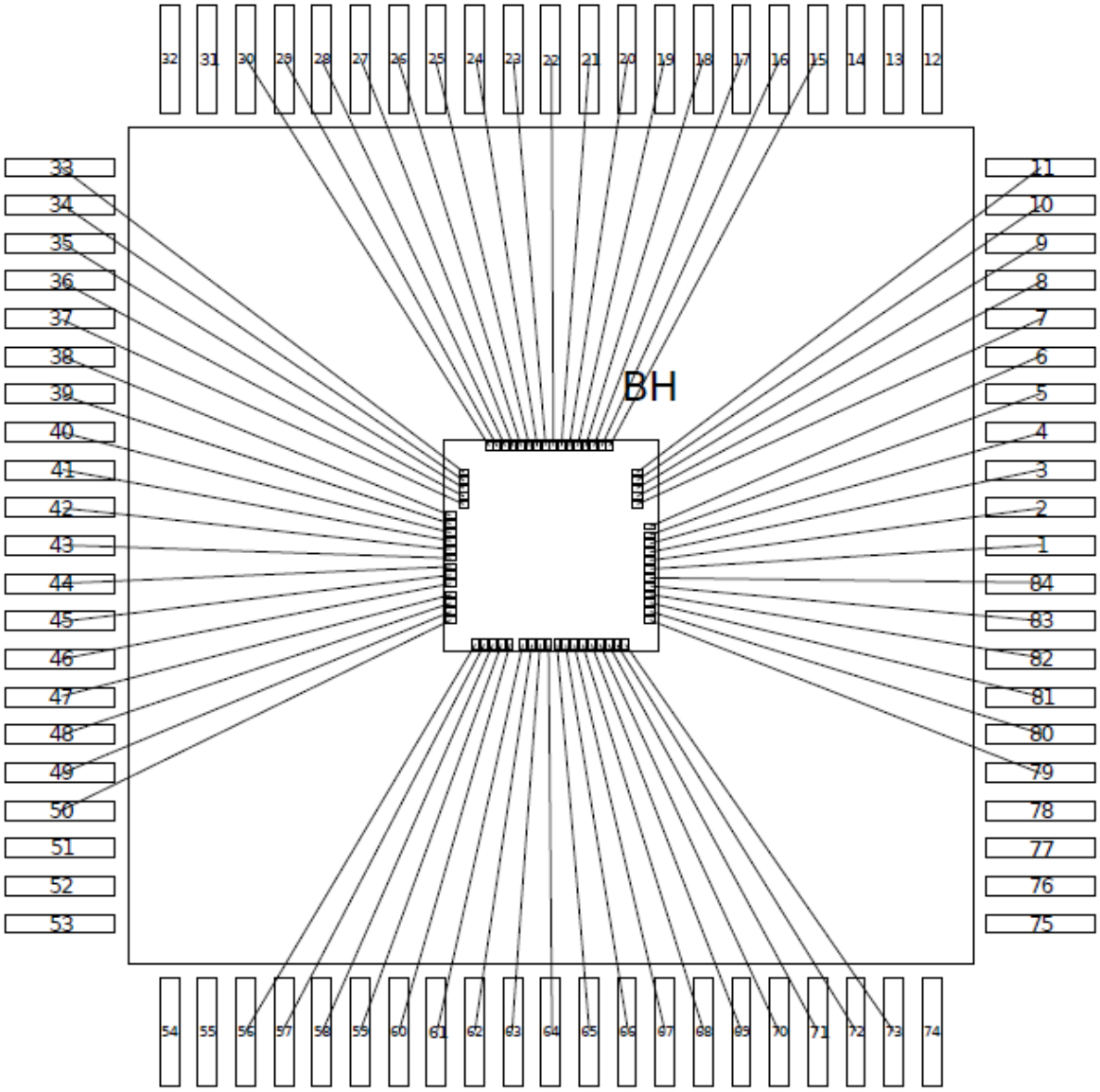

Figure II Bonding diagram (PLL pins 61-73)

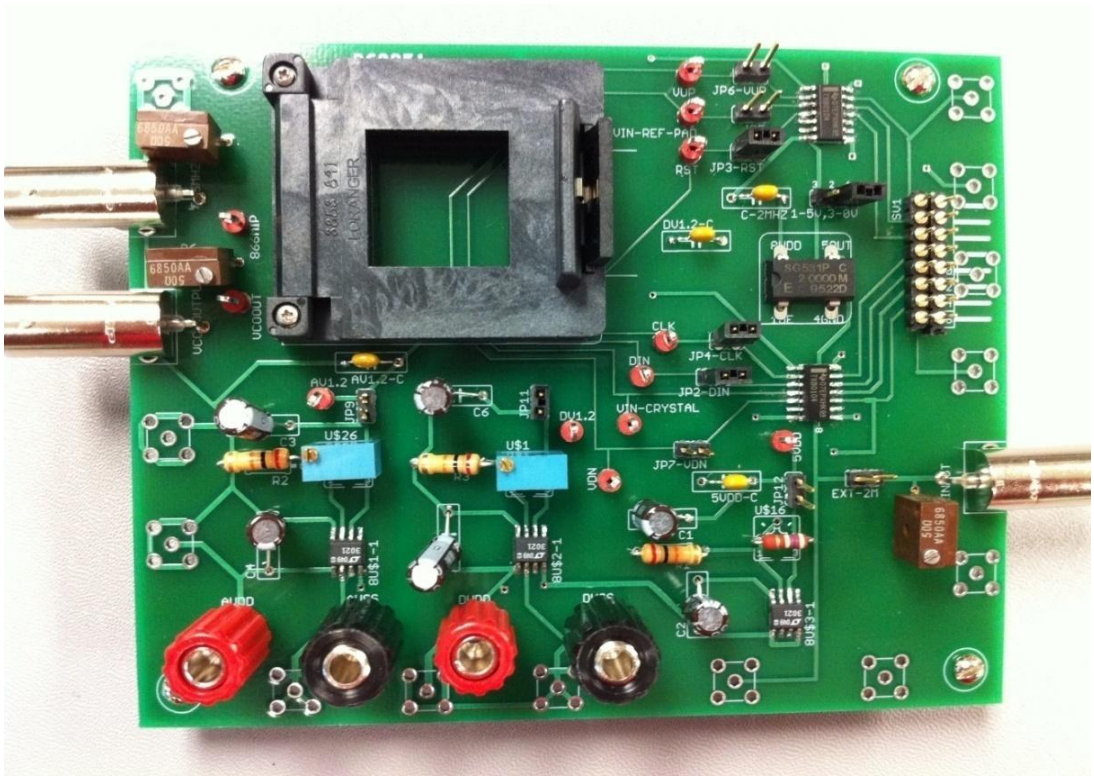

Figure III Image of the PCB test board used for testing