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Design of a High Dynamic Range CMOS Variable Gain Amplifier for Wireless Sensor Networks

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Design of a High Dynamic Range CMOS Variable Gain Amplifier for Wireless Sensor Networks

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of the requirements for the degree of
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By

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ABSTRACT

This thesis presents the design, simulation, layout and testing results for a dB-linear, high dynamic gain range CMOS variable gain amplifier (VGA). The design adopts a new approximated exponential equation called the *pseudo* exponential equation to implement the dB-linear function. The proposed VGA is designed to have an extremely wide gain variation, small chip area, low supply voltage, and controllable dynamic gain range. The gain variation of the 3-stage VGA is implemented by a voltage to current converter. It controls the bias currents of each VGA cell, so that the output gain of each cell can be controlled. In order to stabilize the output common mode voltage of each VGA cell under the variation of its bias currents, a common mode feedback circuit is introduced in the VGA. The VGA was fabricated in IBM's CMRF8SF 130 nm CMOS process.

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to the Graduate Council

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CHAPTER 1

Introduction

A Variable Gain Amplifier (VGA), also known as a programmable gain amplifier (PGA) in some cases, is needed in many baseband circuits for electronic system, especially in many RF communication systems that require an automatic gain control (AGC) loop [1]. In an RF receiver, it plays an important role by controlling the input signal's power level and normalizing the average amplitude of the signal to a reference voltage. By implementing variable gain amplifier in the communication system, the capability of the system is enhanced.

The VGA in this thesis is designed directly for the RF receiver channel for a wireless sensor network chip – a mixed signal system that combines an RF transmitter, an RF receiver, a DSP core, and sensor processing as shown in Figure 1.1.

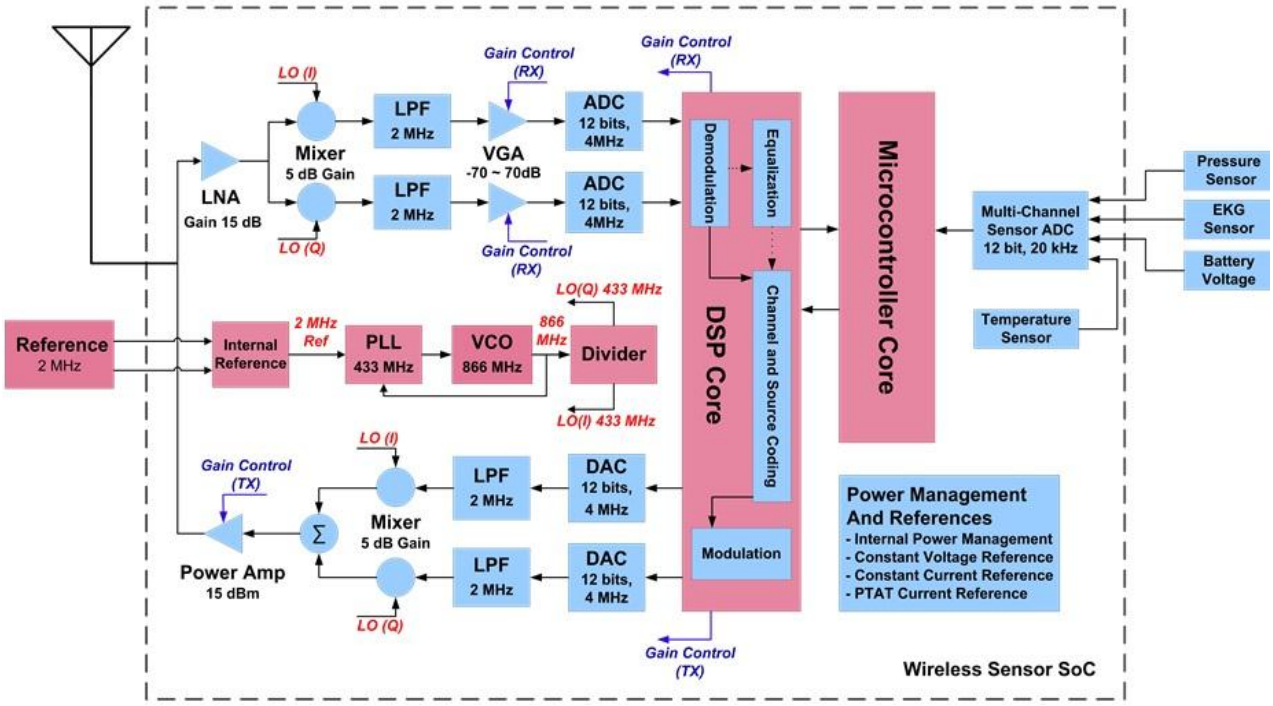


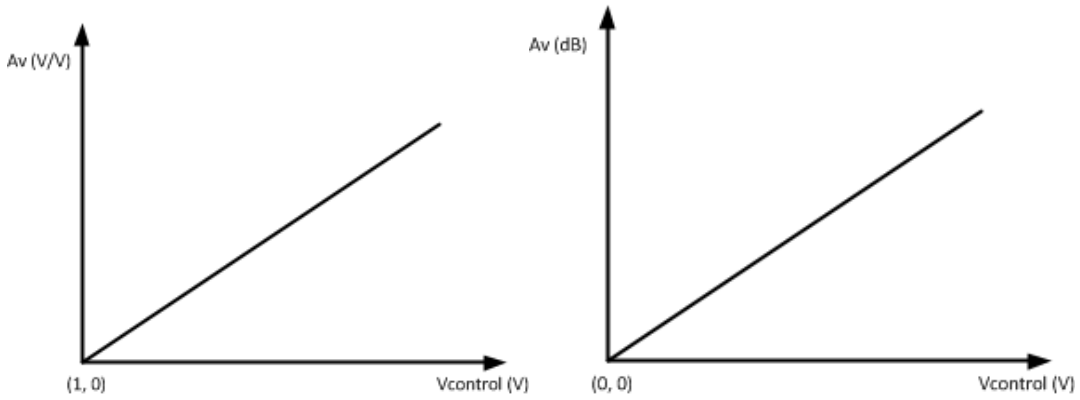
Figure 1.1. Wireless sensor network with the VGA.

In the RF receiver of Figure 1.1, it is required to place a VGA between the filter and the analog to digital converter (ADC) to adjust the output signals from the low pass filter to the input signal level which is required by the ADC to operate properly [2]. The VGA is required to provide a wide bandwidth up to 2 MHz, and minimum power consumption. In addition, as the VGA is used before the ADC, its bandwidth and linearity should be comparable with those of the ADC; otherwise, the performance of the ADC will be degraded [2]. Therefore, the VGA is indispensible in an RF transceiver, providing the largest signal-to-noise ratio to the ADC stage possible and improving the overall dynamic range of the system. The required specifications of this VGA are shown in Table 1.1.

Table 1.1. VGA Design Specifications

Technology	Gain Range	Bandwidth	Power Consumption	Power Supply
IBM 0.13 μm CMOS process	0 ~ 70 dB	$f_{-3dB} \geq 2$ MHz	≤ 10 mW	1.2 V

In this design, the gain of the VGA is controlled by a control voltage provided by the DSP. Normally there are two types of linear variation of the VGA gain: linear in amplitude and linear in decibel. One can intuitively distinguish these two concepts by their name. Linear in amplitude means that the numerical gain of the VGA is proportional with control voltage, while linear in decibel means the dB gain is proportional with control voltage. The plot of these two kinds of gain variation is given in Figure 1.2.



(a) Linear in amplitude (b) linear in dB

Figure 1.2. Two types of gain variation

The proposed VGA in this thesis work is expected to have a dB-linear gain variation. It will be proven shortly in Chapter 3 that if the VGA gain varies exponentially with respect to the control voltage, the settling time of the AGC loop is constant and independent of the absolute gain [3]. This improves the efficiency of the AGC loop and enables it to operate over a wide dynamic range [4]. After the study of a number of VGA topologies that possesses an exponential gain control characteristic, a VGA topology that implements a pseudo-exponential function is proposed to achieve a gain that varies dB-linearly with respect to the control voltage in this thesis.

The dB-linear function is basically a non-exponential polynomial that approximates a logarithmic function. The method to implement this special kind of mathematical equation in the practical design of the proposed VGA will be fully discussed in Chapter 4. The proposed VGA uses a CMOS fully-differential architecture. It has differential-input, differential-output, and differential-gain control voltage. It includes an NMOS differential pair with NMOS diode-connected load. The input pair and the load use separate bias currents which are controlled by the differential control voltage. Therefore, when the biasing currents are changed, the gain of the VGA is varied.

The thesis is organized as follows. The fundamental concepts of VGA and several commonly used VGA topologies will be presented in Chapter 2. The mathematical models used to achieve a dB-linear VGA will be deduced in Chapter 3. The proposed VGA design is presented in Chapter 4, including simulation results of the schematic. Chapter 5 describes the physical layout of the chip. Experimental results from the fabricated chip will be covered in Chapter 6, followed by some conclusions in Chapter 7.

CHAPTER 2

Basic VGA Topologies

In this chapter, three commonly used VGA topologies are introduced. Different VGA topologies have been developed to fulfill the needs of specific design applications. The advantages and drawbacks of each of the VGA topologies based on their gain control principles, linearization, and the power consumption have been comprehensively discussed and then compared. In order to optimize the performance of each application, the appropriate topology and process has to be considered.

The four commonly used VGA structures are: (a) feedback-based VGA; (b) analog multiplier based VGA; (c) differential pair with source degeneration; and (d) differential pair with diode-connected loads.

2.1 Feedback Based VGA

Variable feedback resistances can be implemented to design a variable gain amplifier [5]. The feedback resistance can be a switched resistive network or MOSFETs operating in deep triode region as a controlled linear resistor. A voltage amplifier with feedback resistances has a constant gain bandwidth product [6]; therefore when the gain increases, bandwidth is decreased. It causes poor delay dispersion characteristics. Adjusting the compensation of the amplifier along with the gain setting could possibly decrease this influence by increasing the gain bandwidth product when the gain increases. The VGA shown in Figure 2.1 is based on an operational amplifier that uses switches to decrease the compensation capacitance for higher gains. This topology is the very basic form for VGA functionality. The number of gain sets is equal to the number of switched capacitors. Whenever a resistor is switched on, a discrete is provided by the VGA, and the gain value is equal to the ratio of the reference resistor R_f and the switched resistor

R_x. However, this circuit suffers from several deficiencies. First, it is impossible for this circuit to have an accurate continuous output voltage gain. Therefore, it may not be compatible with other circuitry for certain applications. Second, it requires more resistors and more chip area when more gain settings are necessary [5].

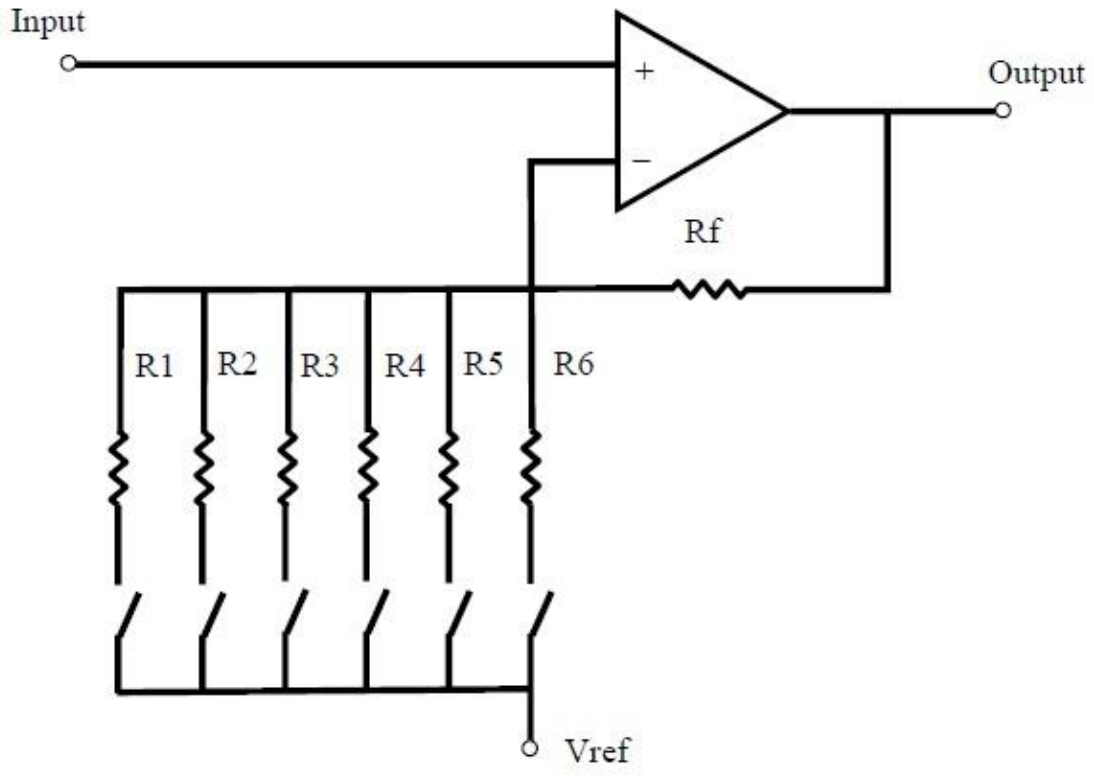


Figure 2.1. Feedback based VGA [5].

2.2 Analog Multiplier

Another commonly used topology in VGA design is the analog multiplier [2]. It serves as a linearized transconductor if one of its inputs is a dc signal. The structure of the analog multiplier VGA is shown in Figure 2.2.

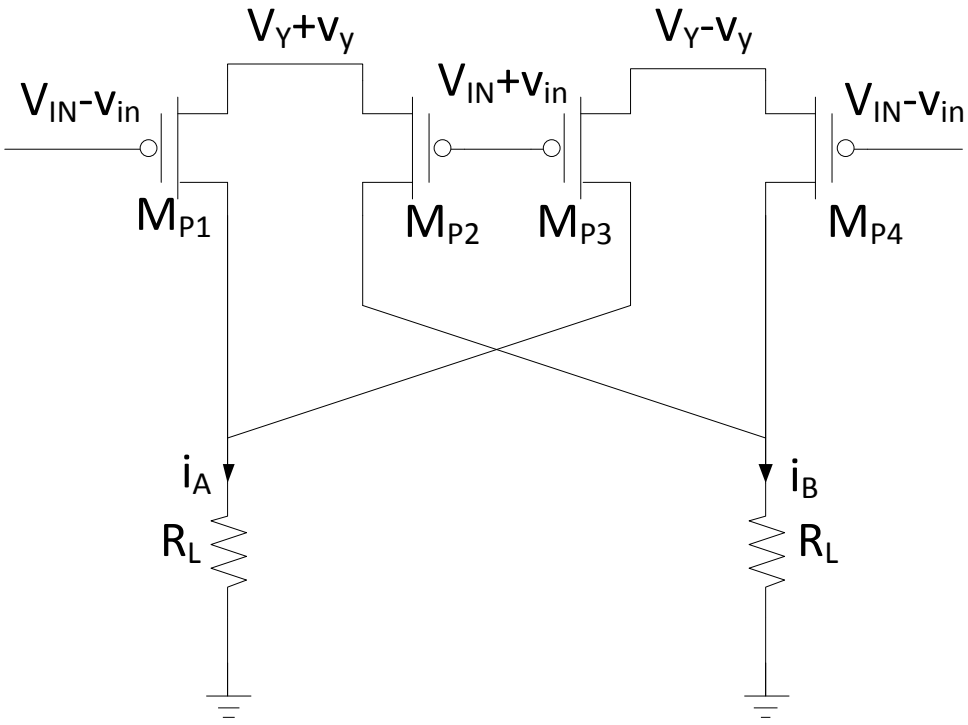


Figure 2.2. Analog multiplier based VGA [2].

In the analog multiplier based VGA schematic above, V_Y is the common-mode voltage for small-signal v_y, and V_{IN} is the common-mode voltage for small-signal $v_{in.}$ All the transistors are operating in saturation region. According to the voltages in the schematic, we could calculate the overall transconductance of the amplifier, which is given in Eq. (2.1) as

$$G_m = 2\mu_p C_{ox}\left(\frac{W}{L}\right)v_y \tag{2.1}$$

If the channel length modulation and body effect are ignored and both of the differential pairs are assumed to be perfectly matched, it is possible to consider that the transconductance of the analog multiplier is linear [2]. The dc voltage gain of the analog multiplier based VGA with resistive load R_L is given in Eq. (2.2).

$$A_v(0) = 2\mu_p C_{ox}\left(\frac{W}{L}\right)v_y R_L \tag{2.2}$$

According to Eq. (2.2), the variable gain is achieved by changing the control voltage V_y. The advantages and drawbacks of this kind of topology are discussed below.

The linear range of the multiplier-based VGA depends on the control voltage v_y. Therefore, when the control voltage V_y increases with the dc voltage gain, the linear range of the analog multiplier is reduced linearly [2]. The load resistor of the analog multiplier can be replaced by a diode connected transistor which is shown in Figure 2.3.

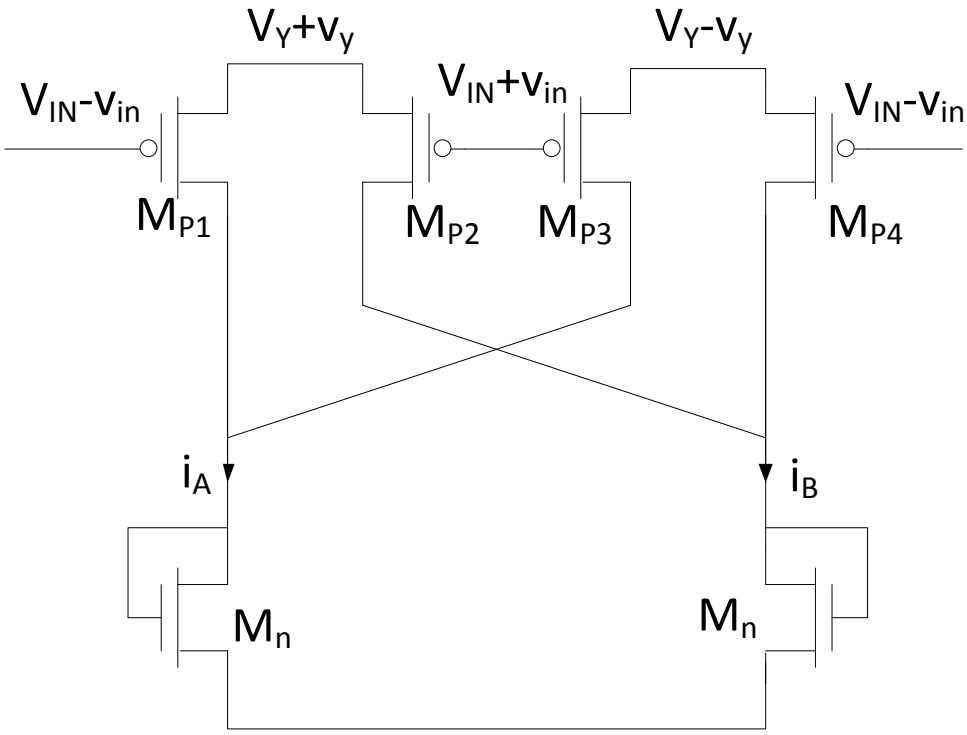


Figure 2.3. Analog multiplier based VGA with active load [2].

In order to satisfy the requirement that all transistors need to operate in the saturation region, the output of the amplifier is limited to a certain range so that the whole amplifier can operate in the linear region. Therefore the linear range of the analog multiplier based VGA is given in Eq. (2.3).

$$V_{linear-range} = \frac{1}{2}\left(V_{dd} - V_{DSATbp} - V_{DSATp} - V_{DSATn} - V_{thn}\right) \qquad (2.3)$$

V_{DSATbp} is the saturation voltage of the PMOS bias transistor which is not shown in the schematic. It is used to provide the source voltage of input pairs of the amplifier. V_{DSATp} is the saturation voltage of the input PMOS pairs. V_{DSATn} is the saturation voltage of the diode-connected NMOS transistor. And V_{thn} is the threshold voltage of the NMOS transistor.

As$V_{DSATp} = V_Y + v_y - V_{IN} - |V_{thp}|$,Eq. (2.3) can be written as

$$V_{linear-range} = \frac{1}{2}\left[V_{dd} - V_{DSATbp} - \left(V_Y + v_y - V_{IN} - |V_{thp}|\right) - V_{DSATn} - V_{thn}\right] \quad (2.4)$$

In addition, according to Eq. (2.2), an expression can be deduced for v_y, which is shown in Eq. (2.5).

$$v_y = \frac{A_v(0)}{2\mu_p C_{ox}\left(\frac{W}{L}\right)R_L} \quad (2.5)$$

Then if V_y is substituted in Eq. (2.4) with Eq. (2.5)

$$V_{linear-range} = \frac{1}{2}\left[V_{dd} - V_{DSATbp} - V_Y - \frac{A_v(0)}{2\mu_p C_{ox}\left(\frac{W}{L}\right)R_L} + V_{IN} + |V_{thp}| - V_{DSATn} - V_{thn}\right] \quad (2.6)$$

Eq. (2.6) indicates that increasing the dc voltage gain $A_v(0)$ could cause the linear range to drop proportionally. As we are designing a VGA with a large active gain range, this may not be achieved by the analog multiplier based topology.

2.3 Differential Pair with Source Degeneration

The differential pair with source degeneration is also commonly used for VGA design topology [2]. As shown in Figure 2.4, the advantages and drawbacks of this topology are also quite obvious in the coming discussion. A good linearity can be achieved by using this topology, but it has some serious issues regarding the transconductance.

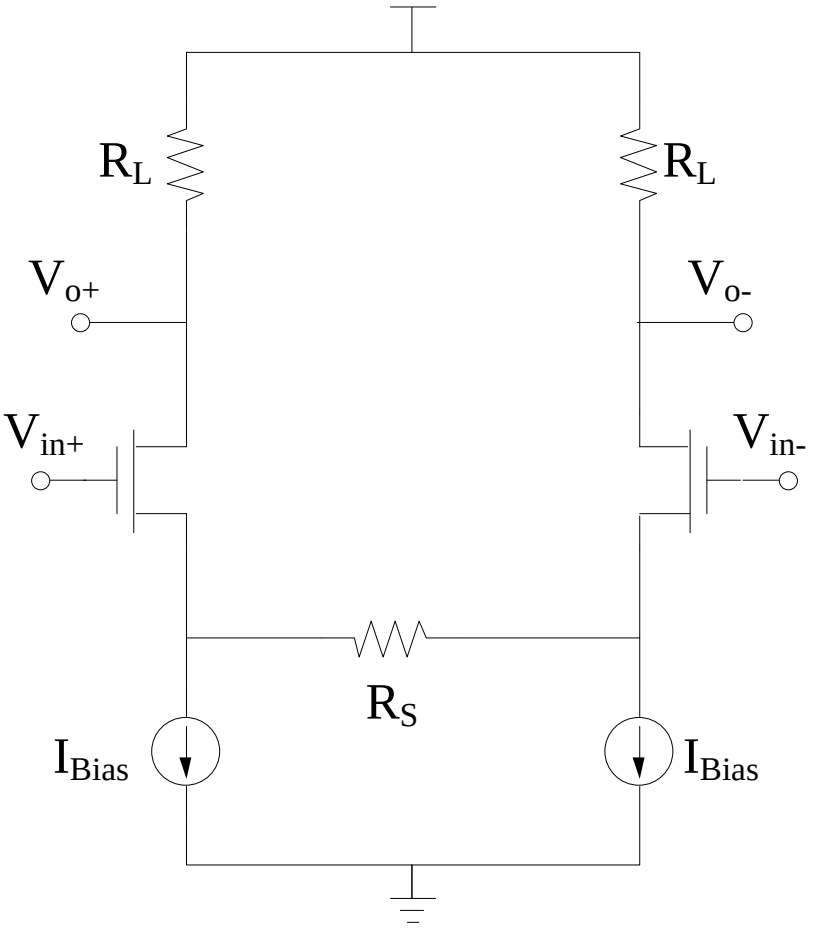


Figure 2.4. Differential pair with source degeneration [2].

It is possible to cut the differential amplifier in half and make two single-ended common source amplifiers with source degeneration resistors, which are now $R_S/2$ in value. Therefore, the overall transconductance of the differential amplifier is determined by Eq. (2.7).

$$G_m = \frac{g_m}{1+\frac{g_m R_S}{2}} \tag{2.7}$$

In Eq. (2.7), R_S is the source degeneration resistor, and $g_m R_S/2$ is the source degeneration factor.

Usually the source degeneration factor $g_m R_S/2$ is much larger than 1, therefore if we ignore the 1 in the denominator of the overall transconductance, Eq. (2.7) becomes

$$G_m \approx \frac{g_m}{\frac{g_m R_S}{2}} = \frac{2}{R_S} \tag{2.8}$$

In this case, the transconductance of the differential pair with source degeneration is merely determined by the source degeneration resistor R_S. By changing the value of R_S, the amplifier gain can be tuned. Compared to the transconductance of the simple differential pair, the effective g_m of differential pairs with source degeneration is only 1/(N+1) times that of the simple differential pair. Therefore, a relatively large gain can be achieved by this topology. However, a large output resistance is required, which is not preferred in designing a voltage amplifier. Therefore, this topology is still not suitable for the proposed VGA.

2.4 Differential Pair with Diode Connected Load

Amplifiers based on differential pair with diode connected loads have recently been proposed for design of VGAs. As shown in Figure 2.5, the input voltage signal is converted into a current using a non-linear input differential pair, then the differential currents are converted back into voltage using a load based on another differential pair which is diode connected. The diode-connected transistors have a smaller transconductance.

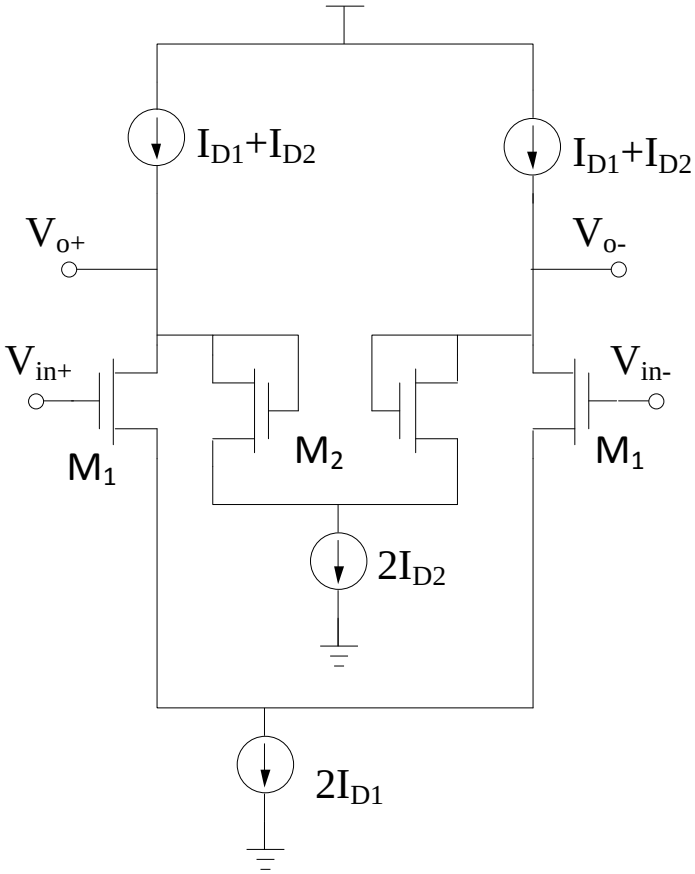


Figure 2.5. Differential pair with diode connected load [7].

The resistance of the diode connected load, NMOS transistor M_2 is $1/g_{m2}$, which is much smaller than the output resistance of NMOS input pair M_1 and the output resistance of current source $I_{D1}+I_{D2}$ which is implemented by a PMOS transistor [8]. Therefore the dc voltage gain of this topology is given by

$$A_v(0) = \frac{g_{m1}}{g_{m2}} = \frac{\sqrt{2K_n'\left(\frac{W}{L}\right)_1 I_{D1}}}{\sqrt{2K_n'\left(\frac{W}{L}\right)_2 I_{D2}}} \qquad (2.9)$$

Eq. (2.9) shows that the dc voltage gain of the differential pair with diode connected load is linear and continuous. The gain is independent of the value of each biasing current of the NMOS transistors because the gain is determined by the ratio of the two biasing currents. This

kind of characteristic ensures that this topology is insensitive to process and temperature variation [2].

As the output resistance of the amplifier is $1/g_{m2}$, which is much smaller than regular output resistance of transistors, the amplifier could drive a relatively low valued resistive load.

2.5 Comparison of Commonly Used VGA Topologies

The feedback based VGA is the very basic form of a variable gain amplifier design. It's simple in structure and easy to implement. However, it is impossible for it to provide a continuous gain variation at an accurate level. This makes it unsuitable for modern VGA design.

The analog multiplier provides a good linearity and a solid controllability on gain variation, but the output swing of this amplifier is greatly limited by the gain. Therefore, an analog multiplier still lacks the ability to meet the design requirement.

Good linearity can also be provided by a differential pair with source degeneration. The reason is this topology has a large source degeneration factor that can linearize the drain current. However, the transconductance is also attenuated by the large source degeneration factor, and so is the gain. As the proposed VGA has a 70dB high gain range, this topology was deemed unsuitable as well.

In order to achieve the best performance on the VGA designed, the differential pair with diode connected load is proposed. However, all the current VGA topologies mentioned above cannot meet the requirement of dB linear gain variation. Therefore, a new approach on the gain control circuit has to be proposed. The principle of the dB-linear gain control circuit will be further described in Chapter 3.

CHAPTER 3

Pseudo-Exponential Approximation

3.1 Why use decibel

The gain of an amplifier is defined as a ratio of two similar dimensioned quantities [9]. In most cases, like a voltage amplifier, the ratio is V/V. Alternatively, for a number of reasons; the amplifier gain could be expressed with a logarithmic measure. And specifically the voltage gain A_v can be expressed as

$$Gain = 20\log(A_V)\ dB \tag{3.1}$$

The reason for defining the unit of gain as decibel, which involves relatively complicated mathematics is that they have some unique advantages [9].

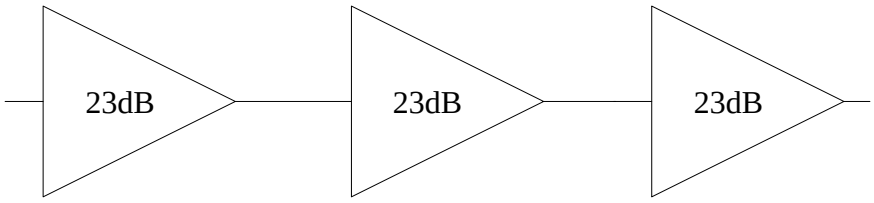


Figure 3.1. Three stage amplifier.

Firstly, as shown in Figure 3.1, it allows the implementation of addition or subtraction directly on the gain and the signal [9]. In Figure 3.1, the overall gain of a three stage VGA with each of its stages providing 23 dB gain is simply 23 dB + 23 dB + 23 dB = 69 dB. While using voltage ratios or amplitudes in this calculation would be much more complicated.

Secondly, decibels work exactly the same both ways round [9]. For example, if 1 mV signal is applied to a VGA and 8 mV is observed at the output, the gain of the amplifier is 8. However, if the gain of the same VGA is set to another value, and a 1 mV signal is observed at the output with 8 mV signal input, the gain is now 0.125. This value seems much different from 8. However, if decibel is used in the gain calculation, those two gains of the same VGA become:

$20\log_{10} 8 = 18$ dB, and $20\log_{10} 0.125 = -18$ dB. In other words, when the gain is expressed in dB, inverse ratios are the same only negative [9].

The third advantage of decibel is that it can express a scale of values over a very large dynamic range without losing fine detail [9].

Figure 3.2 is a spectrum analyzer plot with the y-axis showing signal voltage. A large carrier is clearly seen, but there is also something else higher up the frequency band which is hardly visible.

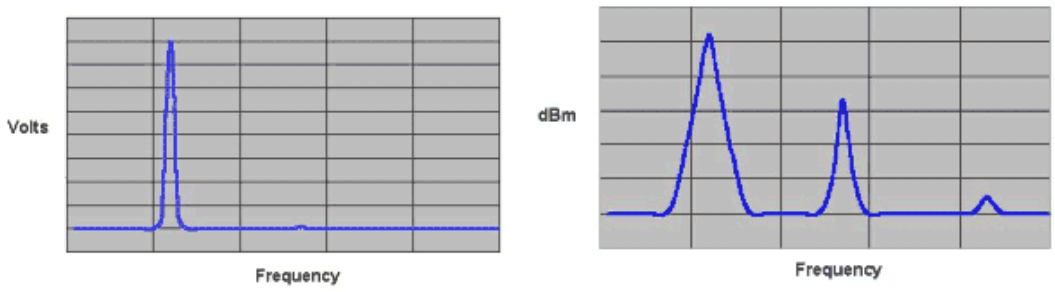


Figure 3.2. Spectrum analyzer plot with different units [9].

If the unit of y-axis is converted to dB instead of voltage, it is possible to see the detail of the smaller carrier higher up the frequency band, and there is a third, even smaller one, which was not visible at all on the linear voltage plot.

3.2 Why linear in decibel

AGC (Automatic Gain Control) systems are widely used in digital communication channels [3]. Usually, error free recovery of data from the input signal cannot occur until the AGC circuit has adjusted the amplitude of the incoming signal. Such amplitude acquisition usually occurs during a preamble where known data are transmitted. The preamble duration must exceed the acquisition or settling time of the AGC loop, but its duration should be minimized for efficient use of the channel bandwidth. If the AGC circuit is designed such that the acquisition time is a function of the input amplitude, then the preamble is forced to be longer in duration

than the slowest possible AGC circuit acquisition time. Consequently, to optimize system performance, the AGC loop settling time should be well defined and signal independent.

If the system response is fixed, for example sine waves of a certain bandwidth; settling time of the system is determined by its time constant. It will be seen shortly that if the variable gain amplifier within the AGC system has a dB-linear gain variation, and the input and output signals of AGC are expressed in dB, then the time constant of AGC system is independent.

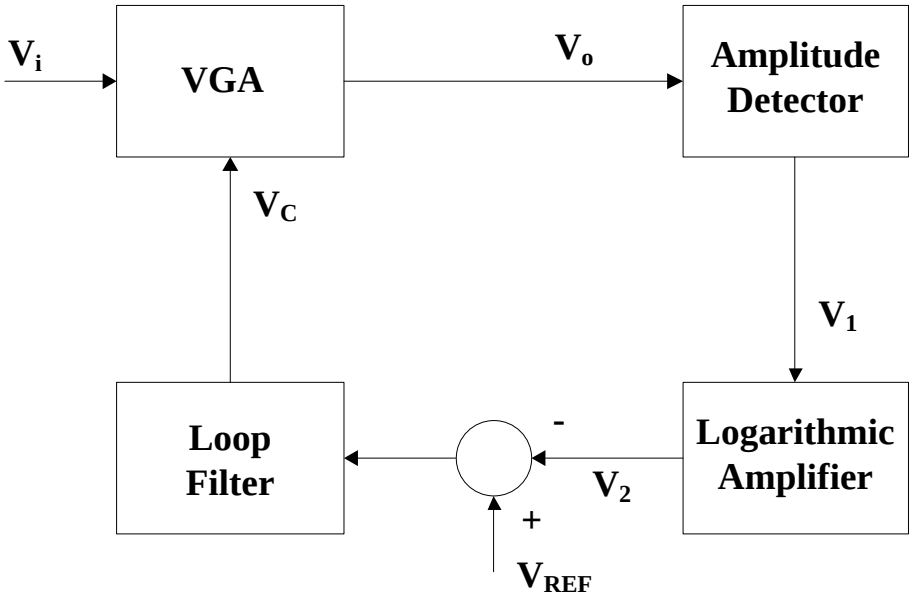


Figure 3.3. Block diagram of a decibel-based AGC system [10].

Figure 3.3 shows the block diagram of a generalized decibel-based AGC system. The gain function of the VGA is $G(V_C)$, which means that the gain is controlled by control voltage V_C. The amplitude detector and the loop filter together form a close loop circuit and monitor the amplitude of the output signal of the VGA. Then they adjust the gain of the VGA by varying the control voltage, which is the output of the loop filter, until the amplitude of the VGA output signal is equal to the dc reference voltage V_{REF}. The output signal of the VGA is the product of gain times input signal.

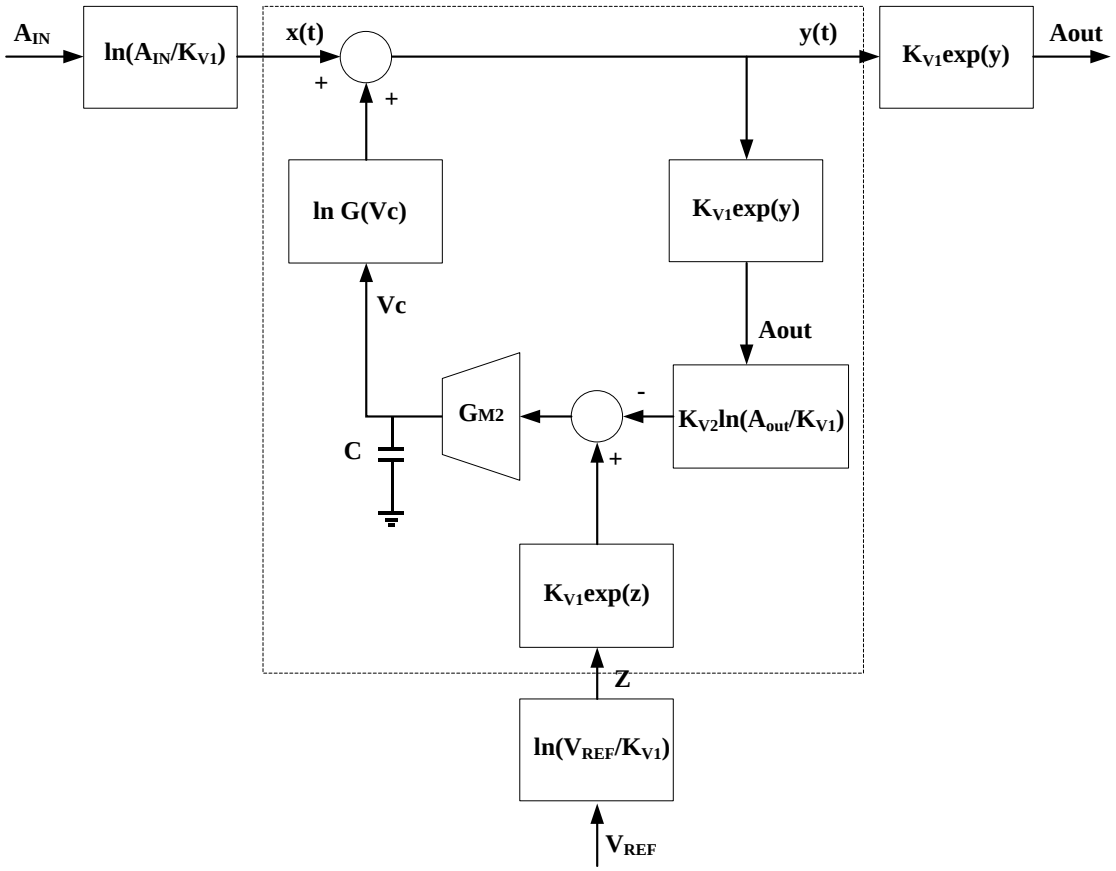


Figure 3.4. Mathematical model of decibel-based AGC system [3].

The mathematical model of the AGC block in Figure 3.4 is established in Figure 3.4. All signal amplitudes are converted to decibels from out of the dash-lined block. The input-output amplitude of the VGA is expressed by

$$A_{out} = K_{V1}\exp\left\{\ln[G(V_C)] + \ln\left(\frac{A_{IN}}{K_{V1}}\right)\right\} \qquad (3.2)$$

K_{V1} and K_{V2} are constants with the same unit as A_{IN} and A_{OUT} which is Volts. x(t) is the input amplitude $A_{IN}(t)$ in decibel, and y(t) is the output amplitude $A_{out}(t)$ in decibel. A linear response from x(t) to y(t) means that the AGC system's linear response from x(t) to y(t) will be linear in dB. The loop filter in Figure 3.4 is shown as an integrator in Figure 3.5, with a transfer function $H(s) = \frac{G_{M2}}{sC}$.

Therefore, the output y(t) in Figure 3.5 is given by

$$y(t) = x(t) + \ln[G(V_C)] \tag{3.3}$$

The gain control voltage, which is the output voltage of the integrator, is given by

$$V_C(t) = \int_0^t \frac{G_{M2}}{C}\left\{K_{V1}e^{Z} - K_{V2}\ln\left[e^{y(\tau)}\right]\right\}d(\tau) \tag{3.4}$$

Taking the derivative of Eq. (3.3) and substituting the result in the derivative of Eq. (3.4), then Eq. (3.5) is obtained.

$$\frac{dy}{dt} = \frac{dx}{dt} + \frac{1}{G(V_C)}\frac{dG}{dV_C}\frac{G_{M2}}{C}\left[K_{V1}e^{Z} - K_{V2}\ln e^{y(t)}\right] \tag{3.5}$$

Eq. (3.5) describes a nonlinear system response of y(t) to an input x(t) unless constraints are placed on the function [3]. After rewriting, Eq. (3.5) simply gives

$$\frac{dy}{dt} + \frac{1}{G(V_C)}\frac{dG}{dV_C}\frac{G_{M2}}{C}K_{V2}y(t) = \frac{dx}{dt} + \frac{1}{G(V_C)}\frac{dG}{dV_C}\frac{G_{M2}}{C}V_{REF} \tag{3.6}$$

The time constant, τ, is given by Eq. (3.7).

$$\tau = \left[\frac{1}{G(V_C)}\frac{dG}{dV_C}\frac{G_{M2}}{C}K_{V2}\right]^{-1} \tag{3.7}$$

Now, as discussed before, the settling time is determined by the time constant of the system if the system response is given. This creates a constraint that $\frac{1}{G(V_C)}\frac{dG}{dV_C}\frac{G_{M2}}{C}K_{V2}$ should equal to a constant value. Therefore,

$$\frac{1}{G(V_C)}\frac{dG}{dV_C}\frac{G_{M2}}{C}K_{V2} = K_x \tag{3.8}$$

where K_X is a constant. Rearranging Eq. (3.8) by integrating both sides of the equation gives the function of control voltage

$$G(V_C) = K_y e^{\frac{K_X C}{K_{V2}G_{M2}}V_C} \tag{3.9}$$

where K_y is the constant of integration. One can easily determine from Eq (3.9) that the gain should vary linearly with the control voltage, if a constant settling time is required.

3.3 Pseudo-exponential approximation method

The problem now becomes how to implement dB linear function in a CMOS variable gain amplifier when a dB linear gain characteristic is necessary for AGC system. As discussed earlier in Chapter 1 and Chapter 2 the dB linear voltage to current (V to I) converter is the key component of the proposed VGA, and it is also the main circuit that implements the dB linear function in the VGA. However, it is clear that dB linear function cannot be directly applied to CMOS technology. The reason behind is that CMOS transistors follow a square law characteristic in strong inversion instead of exponential characteristic [11]:

$$I_d \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{3.10}$$

However, in the weak inversion mode of CMOS technology, the sub-threshold current exhibits an exponential function of gate-source voltage:

$$I_D \approx I_{D0} e^{V_{GS}/\zeta V_T} \tag{3.11}$$

Since such conditions are met by only a large device width or low drain current; and the speed of sub-threshold circuits is severely limited.

It is relatively easy to obtain dB linear function in bipolar technology, because when the Early effect is neglected, the collector current is an exponential function of base-emitter voltage:

$$I_c = I_s e^{V_{BE}/V_T} \tag{3.12}$$

However, the main problem in bipolar technology is that it's not suitable for low power circuit design [11], and for integrating analog and mixed-signal circuit on the same chip. Besides, good performance bipolar transistors are not readily available in the conventional technology [11]. This raises the possibility of using BiCMOS technology. Despite its greater process complexity compared to CMOS, BiCMOS technology is also not suitable for this VGA design because of the extremely high cost over CMOS technology [12].

Since there is no MOS device that shows exponential characteristic when operating in the saturation region, a new method named pseudo-exponential equation is applied in the proposed design.

According to a Taylor's series expansion, a general exponential function could be expressed as

$$e^{ax} = 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 + \cdots + \frac{a^n}{n!}x^n + \cdots \quad (3.13)$$

where 'a' is the coefficient of the Taylor's series, and x is the independent variable respectively. When$|ax| \geq 1$, the Taylor series becomes a divergent series, and the exponential function cannot be implemented by a low order polynomial. Therefore only if $|ax| \ll 1$, can the exponential function can be approximated with small deviation from the ideal exponential function by eliminating the higher order terms. When the higher terms are neglected, the approximation equation with only the first and second order terms is given as

$$e^{ax} \approx 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2 \quad (3.14)$$

Although the plot of approximation equation $e^{ax} \approx 1 + \frac{a}{1!}x + \frac{a^2}{2!}x^2$ is close enough to that of an ideal exponential equation, it is still difficult to implement it in CMOS technology due to the existence of both first and second order terms. It is necessary to find a method to either degrade the second order term or upgrade the first order term. Therefore, a "combined approximation method" is proposed.

Expand the monomial expression $\frac{1+x}{1-x}$ in a Taylor's series,

$$\frac{1+x}{1-x} = 1 + 2x + 2x^2 + 2x^3 + 2x^4 + 2x^5 + \cdots \quad (3.15)$$

If the terms higher than second order are ignored, Eq. (3.15) is given by

$$\frac{1+x}{1-x} \approx 1 + 2x + 2x^2 \quad (3.16)$$

When ‘a’ in Eq. (3.14) is given a value of 2, then Eq. (3.14) becomes

$$e^{2x} \approx 1 + 2x + 2x^2 \tag{3.17}$$

It is obvious that the right part of Eq. (3.16) and (3.17) are exactly the same, so these two equations can be combined together and made into a new approximation equation for an ideal exponential equation as given in Eq. (3.18).

$$e^{2x} \approx \frac{1+x}{1-x} \tag{3.18}$$

Eq. (3.18) is called a *pseudo*-exponential equation. A graphical comparison between the pseudo-exponential approximation and the ideal exponential equation is given in Figure 3.5.

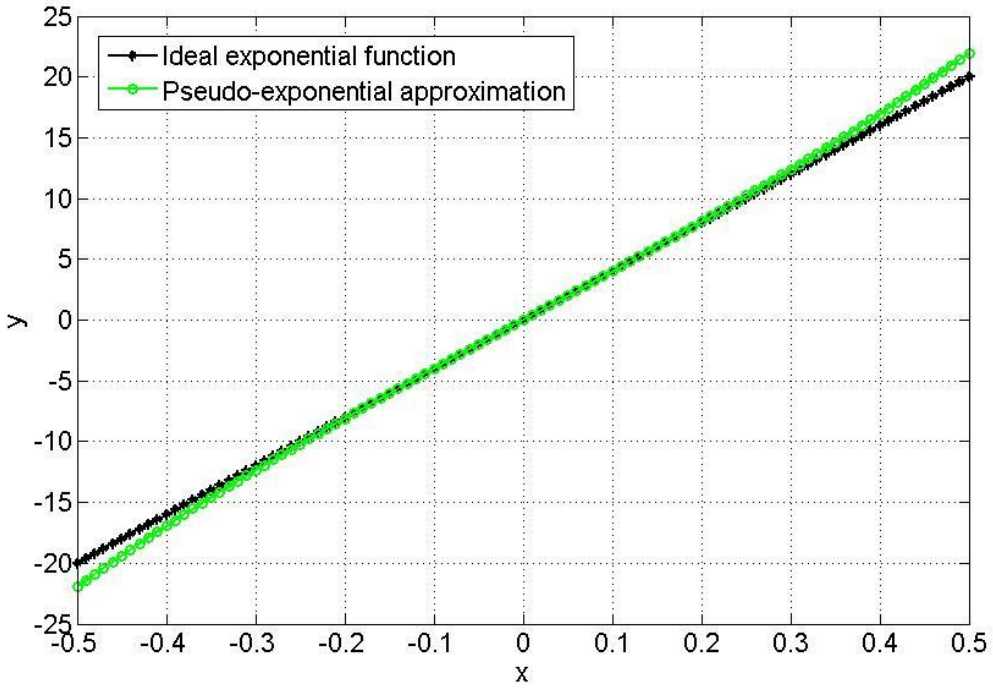


Figure 3.5. Comparison between pseudo-exponential equation and ideal exponential equation.

The scale of x is linear and the scale of y is logarithmic in Figure 3.5. The pseudo-exponential equation provides a highly accurate approximation to the ideal exponential equation

with less error. The practical circuit design to implement pseudo-exponential equation in the proposed VGA to achieve dB-linearity will be fully described in Chapter 4.

CHAPTER 4

Variable Gain Amplifier Design

In this chapter, the challenges of the proposed variable gain amplifier are summarized. The VGA's most important requirement is to provide a 0 to 70 dB active gain which is linear in dB. Therefore a special mathematical model called pseudo-exponential, which was introduced in previous chapter, is implemented in the circuit design to satisfy the requirement. Finally, the detailed calculations for the proposed VGA are given throughout the entire design procedure.

4.1 Design Specifications

In this design, the objective of the proposed VGA is to achieve large variable gain range with large bandwidth, with the gain variation being linear in dB with good linearity.

Some of the critical specifications are given in Table 4.1.

Table 4.1. Variable Gain Amplifier Design Specifications

Parameter	Value
Process	IBM 0.13 μm CMOS process
Supply Voltage	1.2 V
Gain Range	0 ~ 70 dB
Bandwidth	2 MHz

4.2 Circuit Design

The variable gain amplifier was designed according to the specifications given in Table 4.1. The design procedure is described in detail from the system level design. Then each sub-block of the VGA control system is explained.

From the system-level point of view, the proposed VGA design could be divided into three categories:

1) Gain amplification schemes
2) Variable gain control schemes
3) Compensation capacitors

The 70dB gain range is distributed into three amplification stages. Each amplification stage provides a 0 to 23.5dB gain range. The gain of each stage is controlled by the same control voltage through the control unit. With the combination of the three stages, a large variable gain range is obtained. The block diagram of the proposed VGA is shown in Figure 4.1.

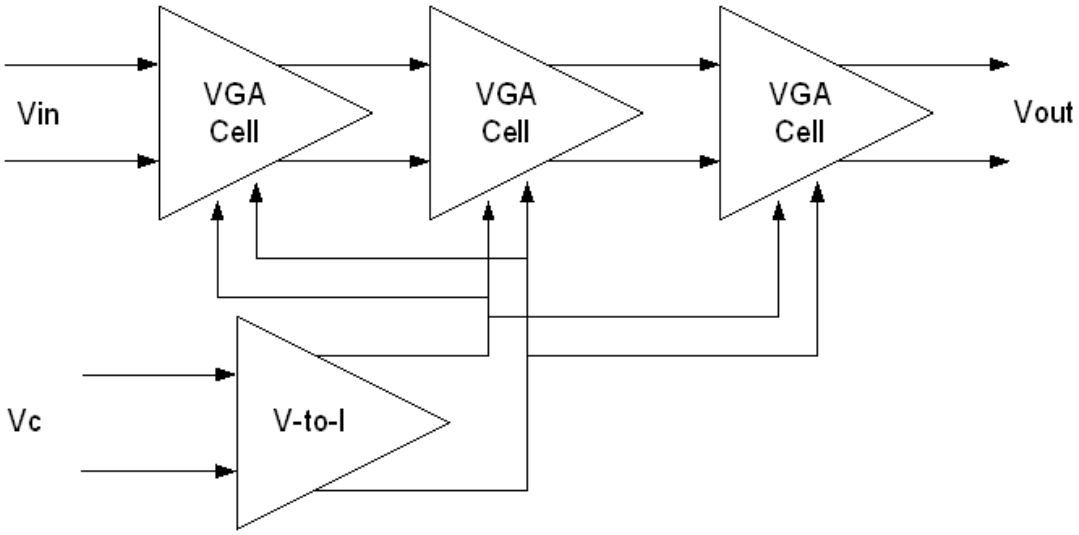


Figure 4.1. Block diagram of the proposed VGA

4.2.1 Gain amplification stage

A gain amplification scheme (stage) is basically composed of two NMOS pairs, MN7 and MN8, MN9 and MN10. The first pair is the differential input pair, while the second one, with both of its transistors diode connected, serves as an active load. These NMOS pairs are biased by two current sources which are implemented by two NMOS transistors MN11 and MN12. The schematic of the gain amplification stage is shown in Figure 4.2. Although the PMOS pair MP5

and MP6 also contribute to the output resistance of the amplifier, their main function is to stabilize the output common-mode voltage by setting the voltage of their gate voltages, since their gates are connected. As the PMOS differential pair MP5 and MP6 are not diode connected, their output resistances are much larger than those of diode connected NMOS transistors MN9 and MN10. Therefore, the total output resistance of the fully-differential gain amplification stage is approximately equal to the output resistance of MN9 and MN10 according to Ohm's law.

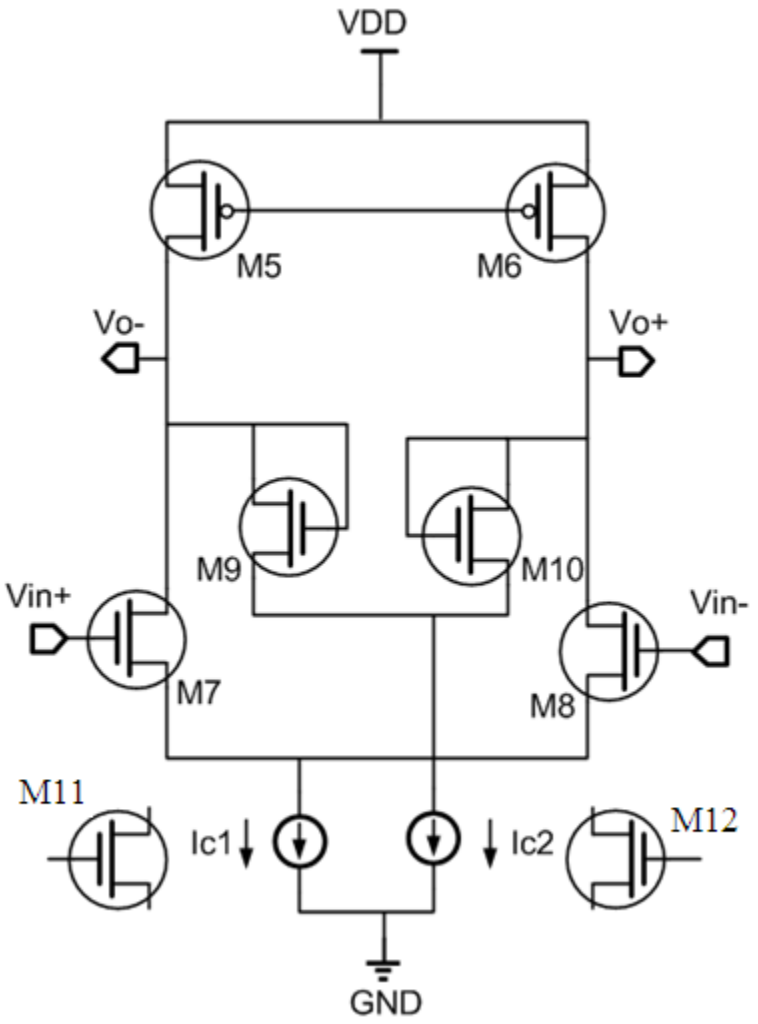


Figure 4.2. Gain amplification stage.

The NMOS input pair MN7 and MN8 and the current source transistor MN11 determine the input common-mode range of the amplifier. The minimum limit of the input common-mode

range is the value of the input voltage at which the NMOS transistor MN11 of the current source leaves the saturation region. It has been discussed in previous chapters that MN11 and MN12 serve as voltage controlled current sources, therefore the gate-source voltages of transistor MN11 and MN12 are not constant. So we shall consider the worst case of the VGA in which the gain is set to its maximum limit by 200mV control voltage. Eq. 4.1 is used to calculate the lower limit of the input common-mode voltage.

$$\mathrm{Vicm(min)} = \mathrm{V_{DS11}} + \mathrm{V_{OV7}} + \mathrm{V_{thn}} \tag{4.1}$$

$$\mathrm{Vicm(min)} = 320\mathrm{mV} - 136\mathrm{mV} + 316\mathrm{mV} = 500\mathrm{mV} = 0.5\mathrm{V}$$

The maximum limit of the input common-mode voltage is obtained when the input differential pair MN7 and MN8 is leaving saturation region, or MP5 and MP6 is leaving saturation region. Eq. (4.2) is used to calculate the upper limit of the input common-mode voltage.

$$\mathrm{Vicm(max)} = \mathrm{V_{dd}} - \mathrm{V_{OV5}} + \mathrm{V_{thn}} \tag{4.2}$$

$$\mathrm{Vicm(max)} = 1200\mathrm{mV} - 260\mathrm{mV} + 257\mathrm{mV} = 1.19\mathrm{V}$$

Therefore, the minimum input common-mode voltage is equal to the drain-source voltage of transistor MN11 plus the overdrive voltage of transistor MN7 and its threshold voltage. The maximum input common-mode voltage is equal to the power supply voltage minus the overdrive voltage of transistor MP5 plus the threshold voltage of MN7.

The aspect ratio of the input NMOS pair should be carefully chosen according to the variable current provided by the voltage controlled current source MN11. When the variable current increases, the source voltage of the input pair also increases. This may easily break the biasing condition of the entire amplifier if the aspect ratio of the input pair is not well calculated. The typical electrical parameters of both the NMOS and PMOS transistors are listed in Table

4.2. Eq. (4.3) and (4.4) show the drain current equations of the NMOS and PMOS transistors respectively, ignoring channel length modulation.

Table 4.2. Normal Key Parameters for the CMOS Transistors

	NMOS	PMOS
Threshold Voltage (V_T)	0.7V	-0.7V
Transconductance Parameter (K')	96 μA/ V ²	53 μA/ V ²

The drain current equation of NMOS transistors is

$$\mathbf{I_d = \frac{1}{2} K'_n \frac{W}{L} (V_{GS} - V_{thn})^2} \tag{4.3}$$

The drain current equation of PMOS transistors is

$$\mathbf{I_d = \frac{1}{2} K'_p \frac{W}{L} \left(V_{SG} - |V_{thp}|\right)^2} \tag{4.4}$$

In order to satisfy the requirement of both achieving a high enough slew rate to drive the capacitive load and low power consumption of the entire circuit, the total bias current of the gain amplification stage, which is mirrored from the gain control unit, is set to be $I_{C1} + I_{C2} = 1$ mV. The calculation of the aspect ratios of the transistors in the gain amplification stage is started from input common-mode range. It is originally expected that $V_{icm(max)} = 1.2$ V, and $V_{icm(min)} = 0.4$ V.

When input common-mode voltage reaches 1.2 V, transistor MN7 should still in saturation mode. Therefore, the aspect ratio of MP5 should satisfy the equation

$$V_{icm(max)} = V_{dd} - \sqrt{\frac{I_{C1}+I_{C2}}{K_{P5}\left(\frac{W}{L}\right)_5}} + V_{thn7} \tag{4.5}$$

As current sources I_{C1} and I_{C2} are controlled by their gate voltages, their drain voltages are not constant. Those drain voltages, which are defined as V_{dc1} and V_{dc2}, follow the drain voltages of the diode connect NMOS transistors in the gain control unit. Therefore, the aspect ratio of MN7 in the gain amplification stage should satisfy the requirement that when input

common-mode voltage reaches the minimum value, it is still possible for the drain voltage V_{dc1} to reach its maximum value. In other words, the gain could reach its maximum value under lowest input common-mode voltage. This is expressed in Eq. (4.6).

$$V_{icm(min)} = 0 + \sqrt{\frac{I_{C1}+I_{C2}}{K_{n7}\left(\frac{W}{L}\right)_7}} + V_{thn7} + V_{dc1(max)} \qquad (4.6)$$

The aspect ratios of current sources MN11 and MN12 are same with that of the diode connect NMOS transistors in gain control unit in order to mirror the bias current. Table 4.3 shows the calculated aspect ratio of transistors in gain amplification stage.

Table 4.3. Aspect Ratios of Transistors in Gain Amplification Stage

MP5, MP6	MN7, MN8, MN9, MN10	MN11, MN12
55.6 μm/240 nm	250 μm/240 nm	62.5 μm/240 nm

In the schematic, the input differential pair has an aspect ratio of 160 μm/240 nm, the gate connected PMOS pair has an aspect ratio of 48 μm/240 nm, and the two transistors of the two current sources have an equal aspect ratio of 48 μm/240 nm. Those aspect ratios are of course integers, which is not the case in hand calculation. The reason for that is to improve the performance of computer simulation. Right now, the only transistors which the aspect ratio are not determined are the diode connected MN9 and MN10. Here they are made to be the same size as NMOS input pair NM7 and MN8. The reason for this will be discussed later.

Since the aspect ratio of each of the transistors has been calculated in the gain amplification stage, it is now important to analyze the small-signal by establishing the small-signal model of the amplifier. In this paper all the small-signal models represents half of the differential circuit, assuming that the differential circuit is ideally matched. Although mismatching of differential circuit could not be avoided during fabrication, this ideal model is

accurate enough for the very first schematic simulation on computer. The small-signal model of gain amplification stage is shown in Figure 4.3.

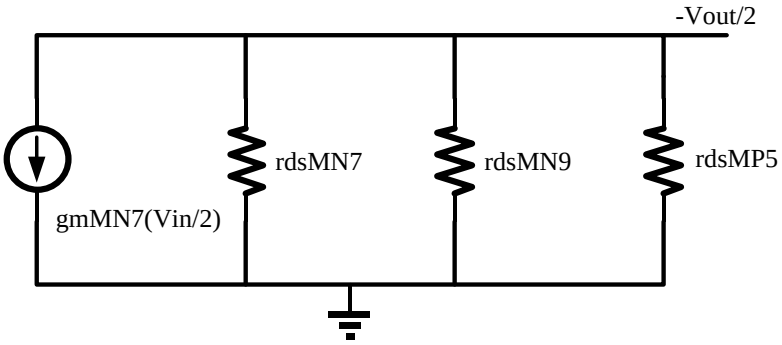


Figure 4.3. Small signal model of gain amplification stage.

First, the overall gain of the gain amplification stage is derived from the small-signal model above, as shown in Eq. (4.7). The overall transconductance of this stage is equal to that of transistor MN7 and MN8 because those transistors are the only two that amplify signal. The total output resistance is equal to the parallel drain source resistance of transistors MN7, MN9 and MP5.

$$\frac{\mathrm{Vout}}{\mathrm{Vin}} = -\mathrm{g_{mMN7}}(\mathrm{r_{dsMN7}} \parallel \mathrm{r_{dsMN9}} \parallel \mathrm{r_{dsMP5}}) \tag{4.7}$$

As the load transistors MN9 and MN10 are diode connected, the resistance r_{dsMN9} in Eq. (4.7) will be much smaller than the r_{dsMN7} and r_{dsMP5} resistances. According to Ohm's law, r_{dsMN9} is dominant in Eq. (4.7); therefore Eq. (4.7) could be written in a simpler way.

$$\mathrm{A_{ol}} = \frac{\mathrm{Vout}}{\mathrm{Vin}} \approx -\mathrm{g_{mMN7}}(\mathrm{r_{dsMN9}}) \tag{4.8}$$

The calculation of the value of the gain in one stage is done by following Eq. (4.8). The transconductance g_{mMN7} is calculated first. As the biasing dc current I_{c1} in each of the input branches has been determined, the transconductance g_{mMN7} is determined by Eq. (4.9).

$$\mathrm{g_{mMN7}} = \sqrt{2K_n'\left(\frac{W_7}{\mathrm{L_7}}\right)\mathrm{I_{c1}}} \tag{4.9}$$

And the total output resistance, which is approximated by the output resistance of diode connected MN9, is given in Eq. (4.10).

$$r_{ds11} = \frac{1}{g_{mMN9}} = \frac{1}{\sqrt{2K_n'\left(\frac{W_9}{L_9}\right)I_{c2}}} \tag{4.10}$$

The gain is the product of g_{mMN7} and $_{rds11}$ in Eq. (4.9) and (4.10), which is shown in Eq. (4.11).

$$A_{ol} = g_{mMN7}r_{ds11} = \frac{\sqrt{2K_n'\left(\frac{W_7}{L_7}\right)I_{c1}}}{\sqrt{2K_n'\left(\frac{W_9}{L_9}\right)I_{c2}}} = \sqrt{\frac{I_{c1}}{I_{c2}}} \tag{4.11}$$

Eq. (4.11) plays an important role in the design of variable gain control unit. This will be shown shortly.

4.2.2 Gain amplification Stage Common-mode Feedback Circuit

According to Eq. (4.11), the gain of an amplification stage is determined by the ratio of two variable biasing currents I_{c1} and I_{c2}. However, these two variable currents may easily shift the output common-mode voltage by changing the dc biasing of the gain amplification stage, and therefore limit the output range. In order to maintain a stable output common-mode voltage and achieve a maximum output range, the common-mode feedback (CMFB) circuit is applied. The purpose of the CMFB circuit, which is shown in Figure 4.4, is to sense the difference between the external voltage reference V_{ref}, and the average value of the differential common-mode output voltage converted by two large resistors. The resistors are connected to the gate of the transistor opposite to the one which gate is controlled by V_g. Then, the CMFB circuit regulates the common-mode output voltage to a certain value close to V_g [8].

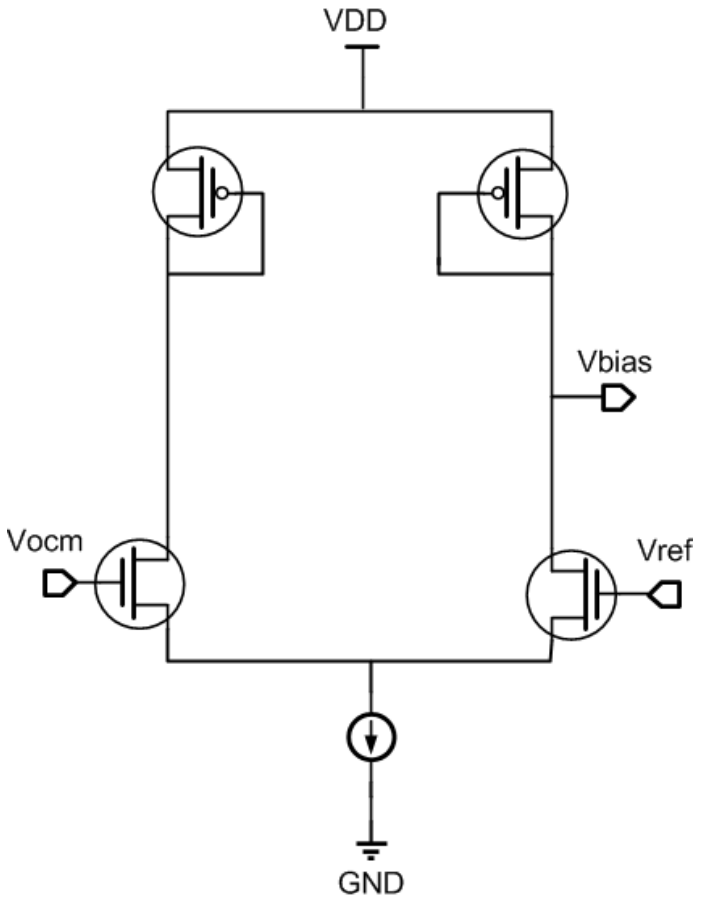


Figure 4.4. Input common-mode feedback circuit.

When V_{ref} and the average common-mode output differ from each other, the common-mode circuit, which is basically an operational amplifier, adjusts the gate voltage of gate connected transistor MP5 and MP6 by its output V_{bias}. By regulating the diode connected PMOS load gate voltage, the current in the differential input pair gets adjusted until the average output common-mode voltage V_{ocm} becomes equal to V_{ref}. The adjustment is needed to avoid variation of the output common-mode voltage.

As V_{ocm} increases above the desired common-mode voltage set by V_{ref}, the current increases through transistors in the feedback circuit. Consequently, as V_{bias} increases, the current in both sides of the gain amplification stage decreases, lowering the common-mode voltage until

it equals V_{ref}. Therefore, the common-mode feedback voltage, V_{bias}, is directly related to the disturbance in the common-mode voltage.

At this point, the design of all three gain amplification stage of the proposed variable gain amplifier has been accomplished, because all of those stages, even including the output stage, are identical. The output stage is designed to drive two 10 pF capacitive loads with a relatively high slew rate. The total bias current for output stage is 1mA, thus it is possible to calculate the slew rate of the output stage by putting the values of capacitive load and bias current into Eq. (4.12).

$$\text{SlewRate} = \frac{I_{C1}+I_{c2}}{C_{load}} \tag{4.12}$$

$$\text{SlewRate} = \frac{I_{C1}+I_{c2}}{C_{load}} = \frac{1\text{mA}}{20\text{pF}} = 50\ \text{V}/\mu\text{s}$$

According to the slew rate calculated in Eq. (4.10), the total bias current provided by the two current sources could easily drive the 10pF capacitive load with a high enough slew rage.

4.2.3 Variable gain control stage

The purpose for designing the gain control unit is to control the gain of all the three gain amplification stages simultaneously by a differential control voltage. The key to the gain control unit design is that it makes sure the gain varies exponentially according to the control voltage.

The schematic of the gain control unit is shown in Figure 4.5.

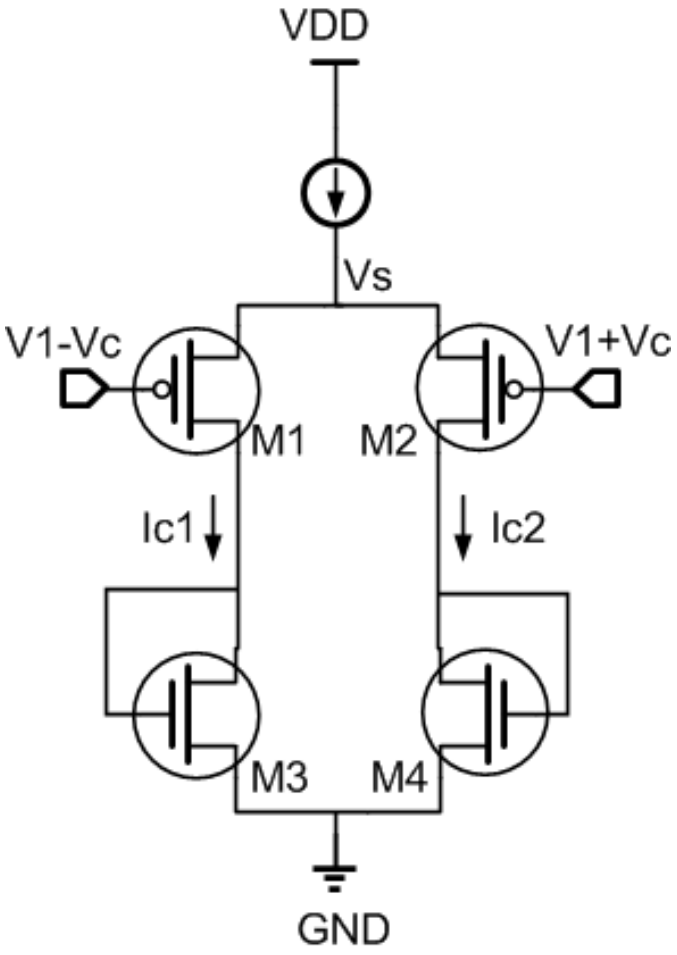


Figure 4.5. Gain control unit schematic.

It is basically a PMOS differential amplifier with NMOS diode connected load. As the gates of MN3 and MN4 are connected to the gates of the two current sources in each of the gain amplification stage, the gain control unit is controlling the gain by varying the bias currents of each of the gain amplification stage.

The input PMOS transistors MP1 and MP2 are biased by a 300mV dc voltage V_1. The differential dc control voltages, $+V_C$ and $-V_C$, which serve as the small controlling signal, are superimposed on the dc bias voltage V_1 on each of the gates of the input pair. Therefore the gate voltages of MP1 and MP2 are V_1+V_C and V_1-V_C. As the sources of MP1 and MP2 are connected, it can be assumed that the common-source voltage is V_S. Then by using drain current

equation in saturation, expressions for the current in each of the branch, I_{C1} and I_{C2}, respectively, can be found as in Eq. (4.13) and (4.14).

$$I_{C1} = \frac{1}{2} K'_{p1} \frac{W_{P1}}{L_{P1}} [V_S - (V_1 - V_C) - |V_{THP}|]^2$$

$$= \frac{1}{2} K'_{p1} \frac{W_{P1}}{L_{P1}} [V_S - V_1 - |V_{THP}| + V_C]^2 \quad (4.13)$$

$$I_{C2} = \frac{1}{2} K'_{p2} \frac{W_{P2}}{L_{P2}} [V_S - (V_1 + V_C) - |V_{THP}|]^2$$

$$= \frac{1}{2} K'_{p2} \frac{W_{P2}}{L_{P2}} [V_S - V_1 - |V_{THP}| - V_C]^2 \quad (4.14)$$

The aspect ratio of MP1 and MP2 are chosen to make sure that even if the control voltage V_C reaches its maximum value, the transistor which carries the most current is still in saturation mode. And the diode connected NMOS transistors are designed to have the same aspect ratio with the current sources in each of the gain amplification stage, so that the currents in the gain control unit is mirrored to the gain amplification stages.

One logical question to ask is "why is the gain control unit designed in such way that the current in each of the branches is expressed by Eq. (4.13) and (4.14)?" The answer is to implement the pseudo-exponential equation in the schematic of the VGA to realize a dB-linear performance. According to the design of the gain amplification stage, the gain is expressed in Eq. (4.11) which is repeated below.

$$A_{ol} = g_{mMN7} r_{ds11} = \frac{\sqrt{2K'_n \left(\frac{W_7}{L_7}\right) I_{c1}}}{\sqrt{2K'_n \left(\frac{W_9}{L_9}\right) I_{c2}}} = \sqrt{\frac{I_{c1}}{I_{c2}}} \quad (4.15)$$

If I_{C1} and I_{C2} in Eq. (4.15) are replaced by Eq. (4.13) and (4.14). The gain is now

$$A_{ol} = \sqrt{\frac{I_{c1}}{I_{c2}}} = \sqrt{\frac{\frac{1}{2} K'_{p2} \frac{W_{P2}}{L_{P2}} [V_S - V_1 + V_C - |V_{THP}|]^2}{\frac{1}{2} K'_{p2} \frac{W_{P2}}{L_{P2}} [V_S - V_1 - |V_{THP}| - V_C]^2}} = \frac{1 + \frac{V_C}{V_1 - V_S - |V_{THP}|}}{1 - \frac{V_C}{V_1 - V_S - |V_{THP}|}} \quad (4.16)$$

According to the pseudo-exponential method discussed in Chapter 3 that if $|x| \ll 1$, then $e^{2x} \approx \frac{1+x}{1-x}$. As the maximum value of V_C is only 1/3 of $V_1 - V_S - |V_{THP}|$, it is possible to apply pseudo-exponential method to Eq. (4.16), which is shown in Eq. (4.17).

$$A_{ol} = \frac{1+\frac{V_C}{V_1 - V_S - |V_{THP}|}}{1-\frac{V_C}{V_1 - V_S - |V_{THP}|}} \approx e^{\frac{2V_C}{V_1 - V_S - |V_{THP}|}} \tag{4.17}$$

By employing the logarithmic function on both sides of Eq. (4.17), a linear function between dB gain and control voltage is derived, as shown in Eq. (4.18).

$$20\log_{10} A_{ol} \approx 20\log_{10} e^{\frac{2V_C}{V_1 - V_S - |V_{THP}|}} = CV_C \tag{4.18}$$

As C is a constant in Eq. (4.18), the design of a dB-linear variable gain amplifier is fulfilled.

4.3 Simulation

After the schematic of the VGA is calculated and established in Cadence, the next step in the design process will be verifying its performance through simulation. Test benches will be setup to test different performances including transient performance, dc performance and ac performance at both room temperature and over temperature. The simulations were performed using the Cadence simulator Spectre. The VGA's main performance characteristics will be discribled throughout this section.

4.3.1 Test bench and simulation environment

Test benches were setup to simulate the main characteristics including dc, ac and transient responses, and environments that the VGA would be exposed to in order to simulate the VGA's performances as accurately as possible. Each simulation environment was designed to verify a specific behavior of the VGA.

4.3.2 DC performance

For verifying dc performance of the VGA, the following simulations are involved: dc input-offset voltage, input common-mode range, and output voltage swing. The schematic of the test bench used for dc performance is shown in Figure 4.6. The load capacitors for the VGA were chosen to be 10 pF in order to meet with the input capacitance of Tektronix MSO 4104 oscilloscope. In all dc performance simulations, the gain control voltage is set to 200mV, so that the VGA operates with maximum voltage gain (70 dB). The reason is that the VGA consumes highest current when control voltage is set to maximum value.

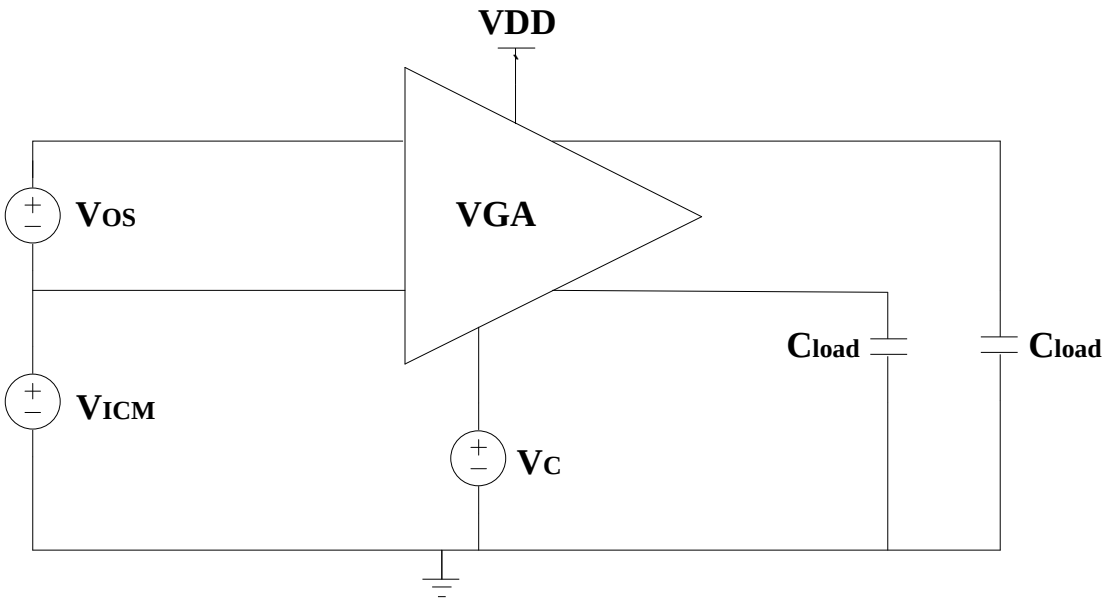


Figure 4.6. Test bench used for dc performance.

The first performance of the VGA simulated is the input offset voltage. The positive and negative input voltage, V_{in+} and V_{in-} are supplied with 600mV dc voltage, and V_{os} is swept from -10mV to 10mV, which gives a 20mV differential input voltage swing. The simulation results are shown in Figures 4.7, 4.8 and 4.9 for different temperature environment. It can be seen that when the output voltages reach 600mV, which is the expected output common-mode voltage, the offset voltage V_{os} is very close to 0.V

As the input offset voltage source V_{os} is set up to 20mV under a 70dB high gain, the input offset voltage simulation results also show the output voltage swing at each temperature. The output voltage swing at 27 ^{0}C is from 0.195 V to 1.01 V, at 125^{0}C it is from 0.325 V to 0.898 V and at -55^{0}C it is from 0.075V to 1.1V.

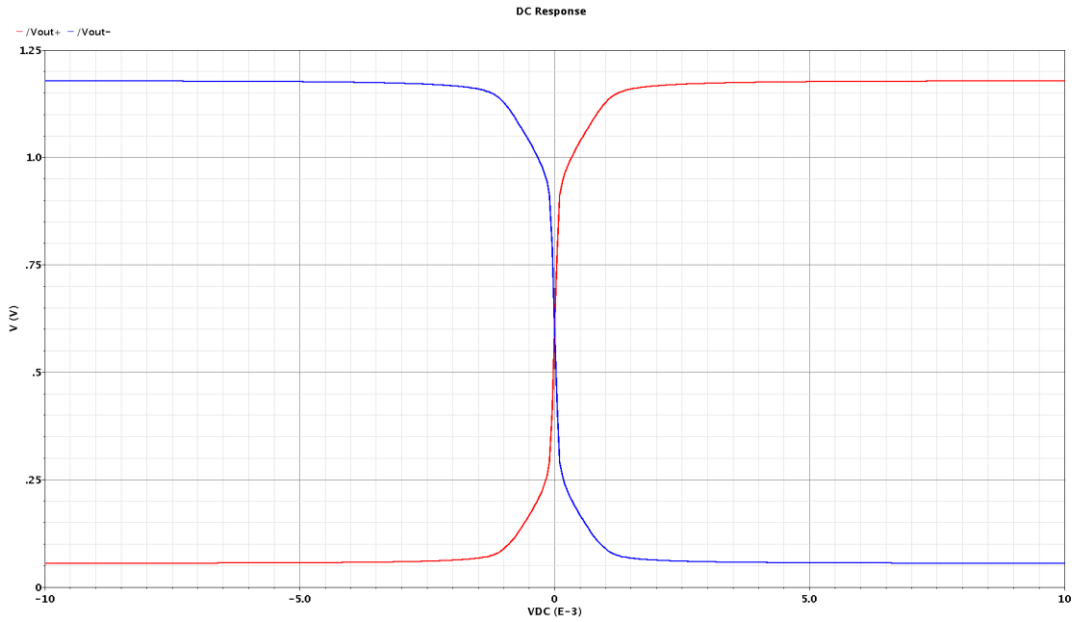


Figure 4.7. Input offset voltage and output swing simulation at 27 ^{0}C.

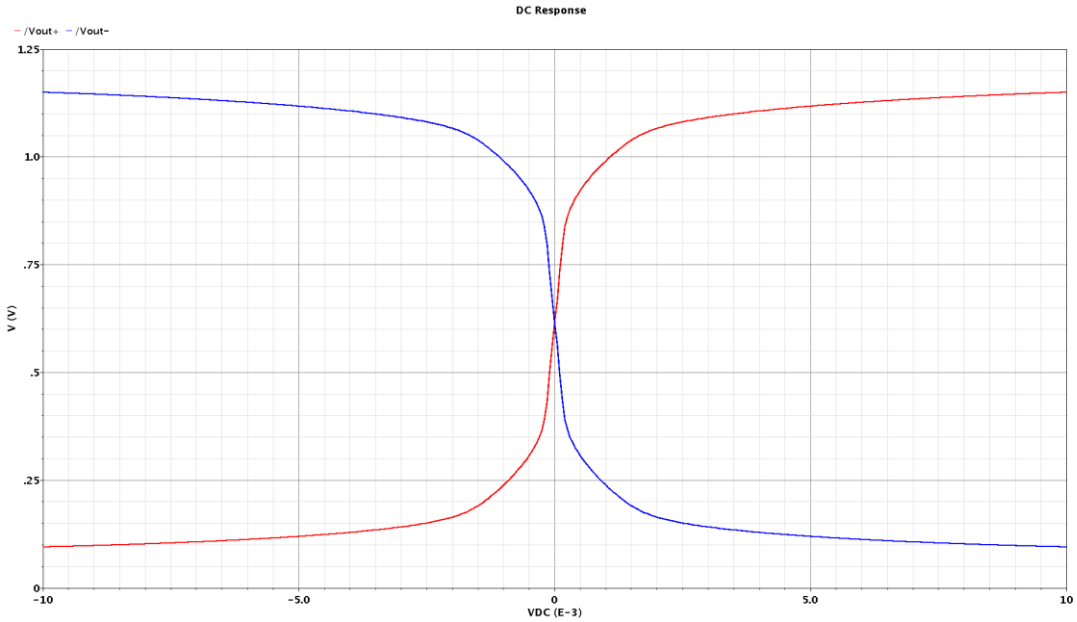


Figure 4.8. Input offset voltage and output swing simulation at 125 ^{0}C.

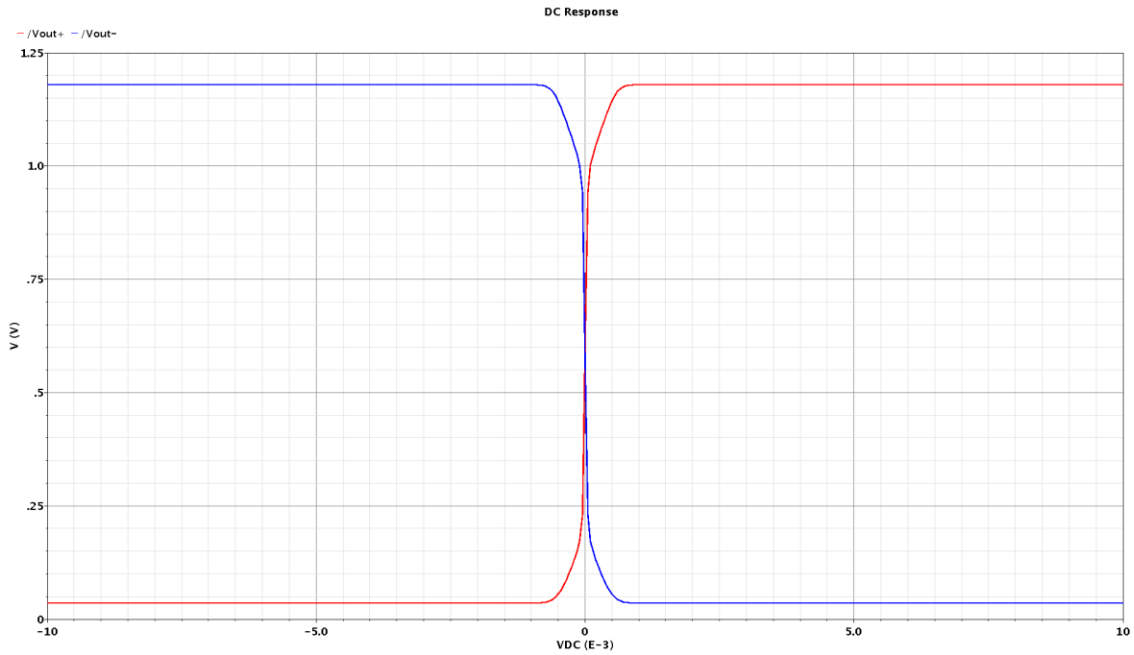


Figure 4.9. Input offset voltage and output swing simulation at -55 ^{0}C.

Another important dc behavior of the variable gain amplifier is the input common-mode range (ICMR). A constant output voltage for a swept input common-mode voltage within the ICMR ensures a linear output performance. In the ICMR simulation, the input common-mode voltage is swept from rail to rail (0 to 1.2 V). Output voltage should stay around 600 mV, as maintained by the common-mode feedback circuit, when the input common-mode voltage is in a proper range. In the simulation, a ±10 mV tolerance on the output common-mode voltage is assumed. The simulation results observed at different temperatures are shown in Figures 4.10, 4.11, and 4.12. The simulated ICMR was 0.47 V to 1.2 V at room temperature (27 ^{0}C), 0.7 V to 1.2 V at 125 ^{0}C and 0.4 V to 1.2 V and at -55 ^{0}C. Recall the minimum and maximum value of ICMR (worst case) calculated in Eqs. (3.1) and (3.2) are 0.5 V and 1.19 V, respectively. Therefore, the simulation results correspond well with calculated data.

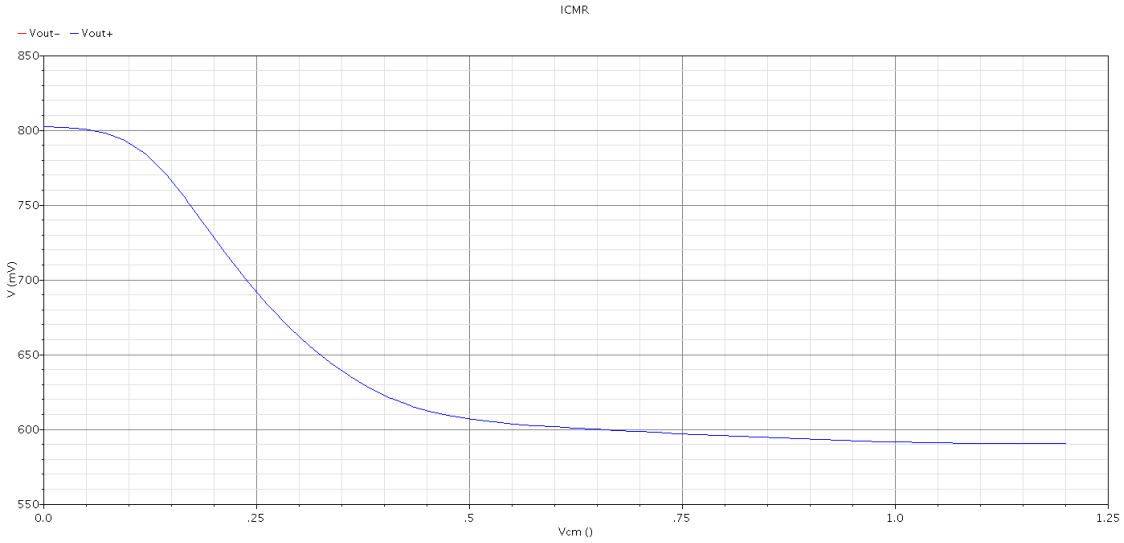


Figure 4.10. Input common-mode range simulation at 27 ^{0}C.

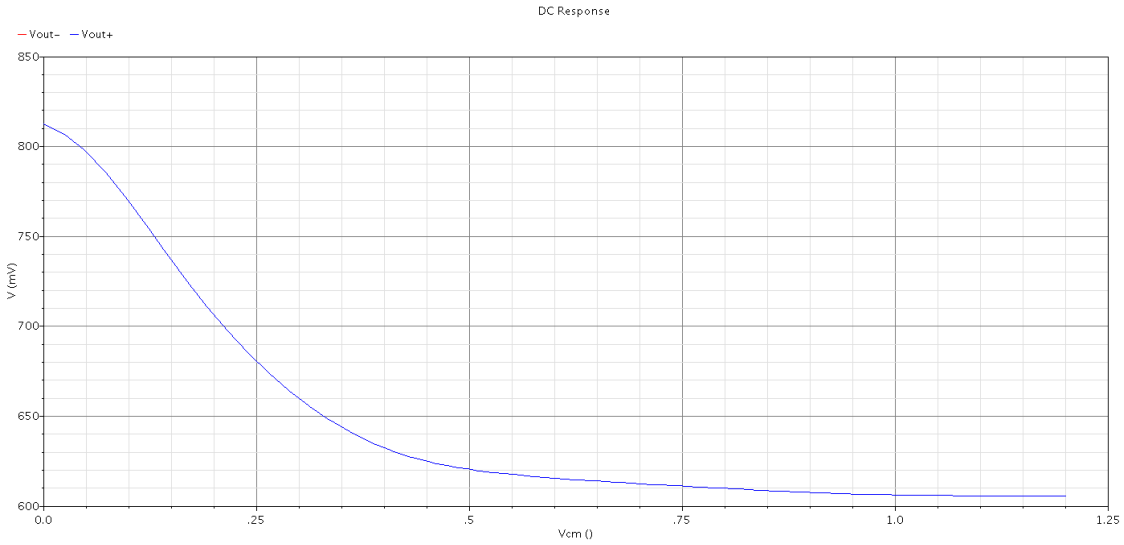


Figure 4.11. Input common-mode range simulation at 125 ^{0}C.

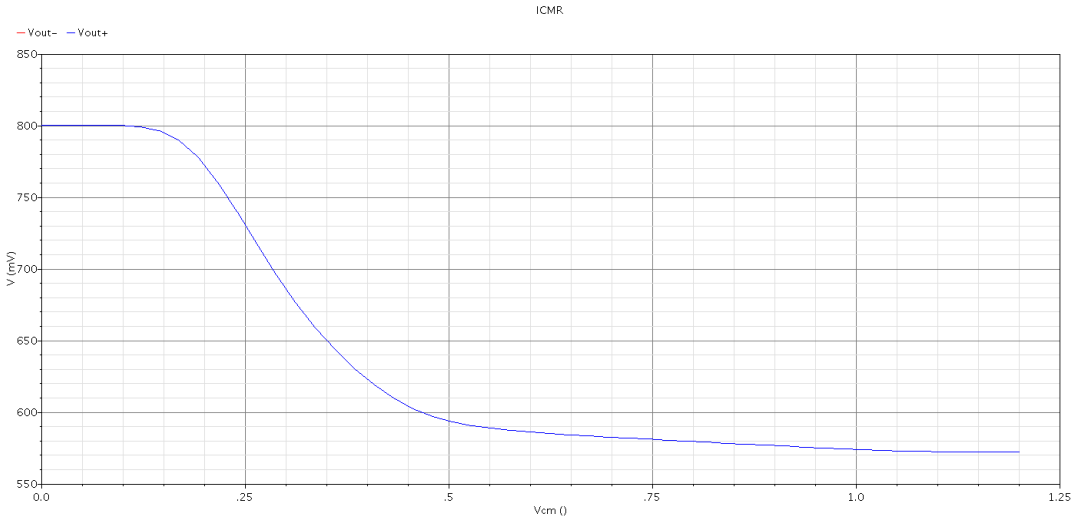


Figure 4.12. Input common-mode range simulation at -55 ^{0}C.

However, it is true that the input common mode range is decreased when temperature goes up. That means when temperature is going up, it is more difficult for the VGA to hold the output common-mode voltage at 600 mV. The reason for that is, when temperature increases, the bias current in the CMFB circuit also increases, as shown in the simulation result in Figure 4.13.

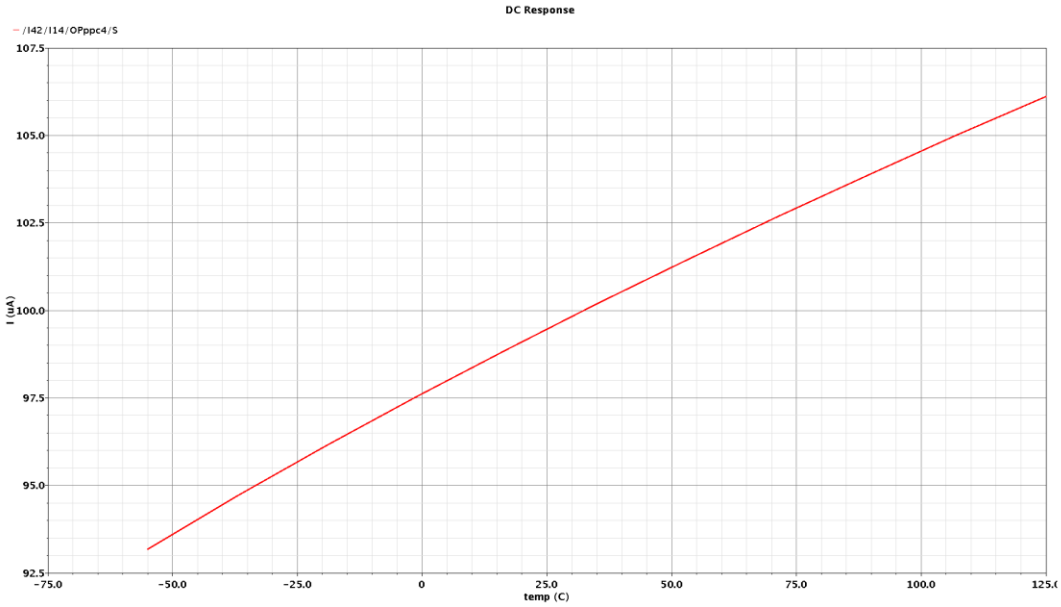


Figure 4.13. Variation of CMFB bias current across temperature.

According to Figure 4.13, when temperature increases, the bias current of the CMFB circuit, which is basically an amplifier, is increased. Therefore, the gain of the CMFB circuit is decreased. In that case the CMFB circuit cannot provide a “strong” enough output voltage to regulate the output common mode voltage back to 600 mV.

The dc power consumption is also involved in dc performance simulation. Dc power consumption should be as low as possible to satisfy the requirement of low power design. Figure 4.14 shows the total current consumed by the VGA across temperature from -55 ^{0}C to 125 ^{0}C. At 27 ^{0}C the current is 5.6 mA, at 125 ^{0}C the current is 6.1 mA and at -55 ^{0}C the current is 5.1 mA. Therefore, the dc power consumption range is from 6.1 mW to 7.3 mW.

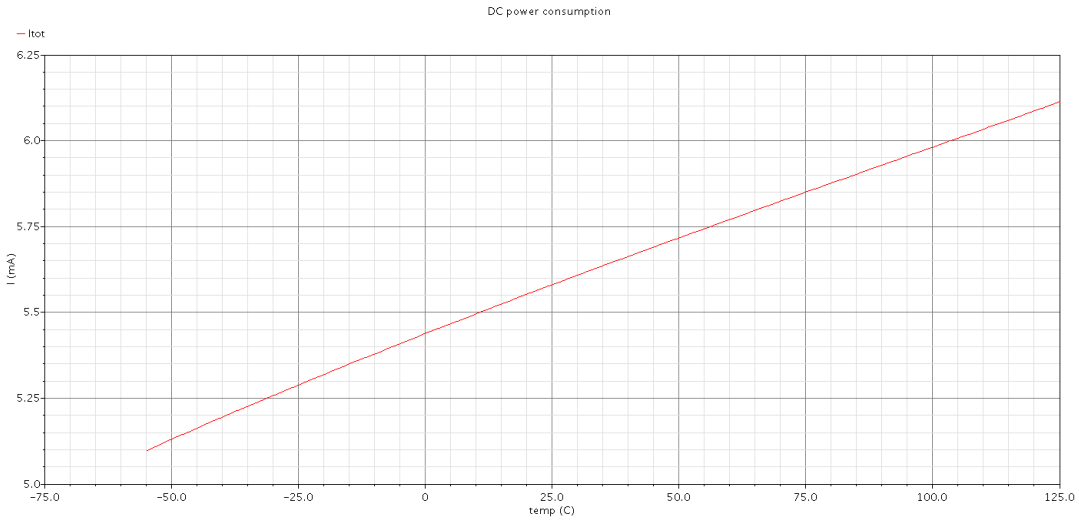


Figure 4.14. Total dc current driven by VGA across temperature.

4.3.3 AC performance

In order to check the ac performance of the proposed variable gain amplifier, the set of simulations includes: voltage gain range across temperature, 3 dB gain bandwidth, gain linearity and pole placement Figure 4.15 shows the test bench used to simulate ac performances of the VGA. Voltage gain simulation is run on both highest gain and lowest gain as shown in Figure 4.16 and 4.17.

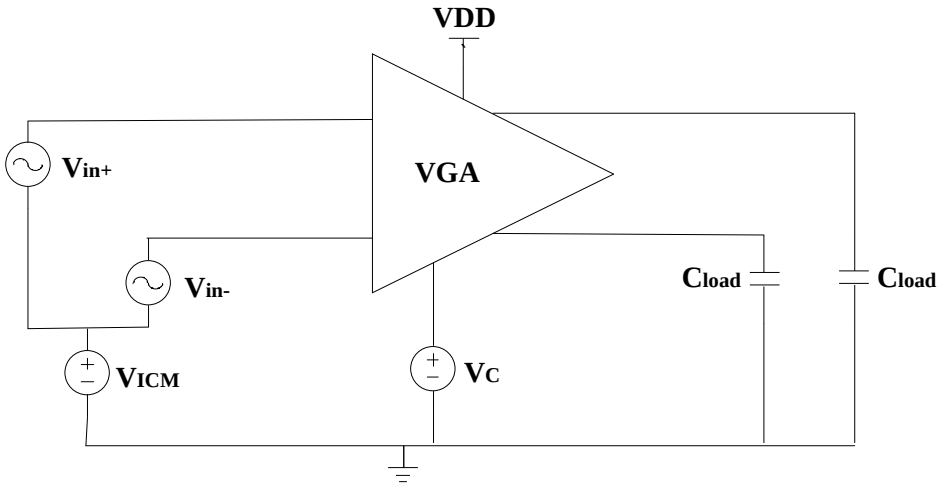


Figure 4.15. Test bench used for AC performance.

The 3 dB gain of the VGA is shown on the same plot. Table 4.3 shows the ac simulated parameters for both temperature extremes with control voltage V_C set to both maximum value and minimum value.

Table 4.4. Simulation Results of AC Parameters

Parameter	Temperature	Simulated Value
Voltage Gain (V_C max)	-55 ^{0}C 22 ^{0}C 125 ^{0}C	77.46 dB 70.97 dB 59.23 dB
Voltage Gain (V_C min)	-55 ^{0}C 22 ^{0}C 125 ^{0}C	3.186 mdB -970 mdB -1.837 dB
-3 dB Bandwidth (V_C max)	-55 ^{0}C 22 ^{0}C 125 ^{0}C	12.97 MHz 13.1 MHz 14.8 MHz
-3 dB Bandwidth (V_C min)	-55 ^{0}C 22 ^{0}C 125 ^{0}C	74.46 MHZ 68.58 MHZ 64.47 MHZ

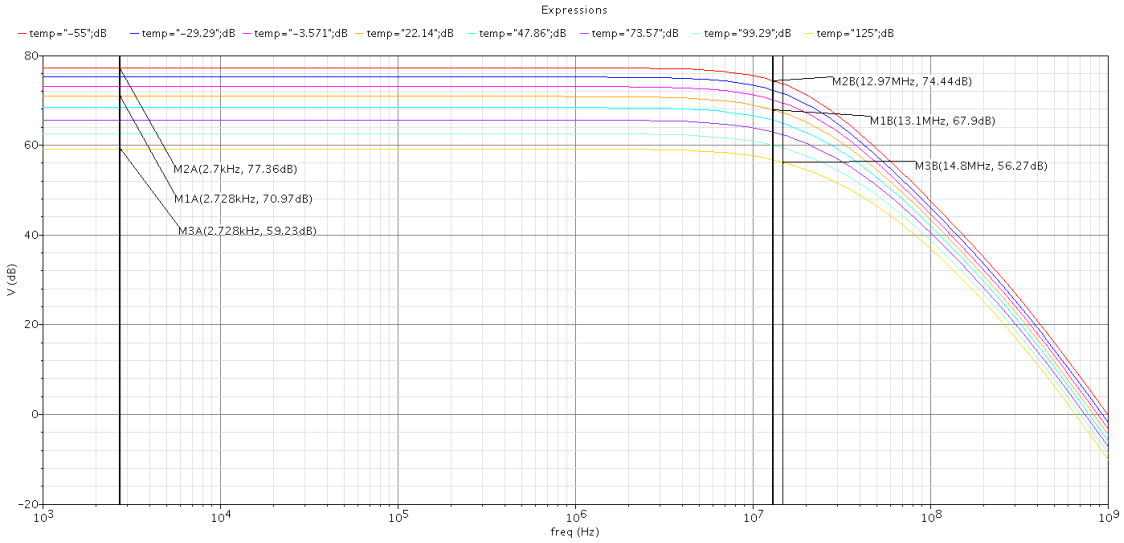


Figure 4.16. Bode plot of highest gain.

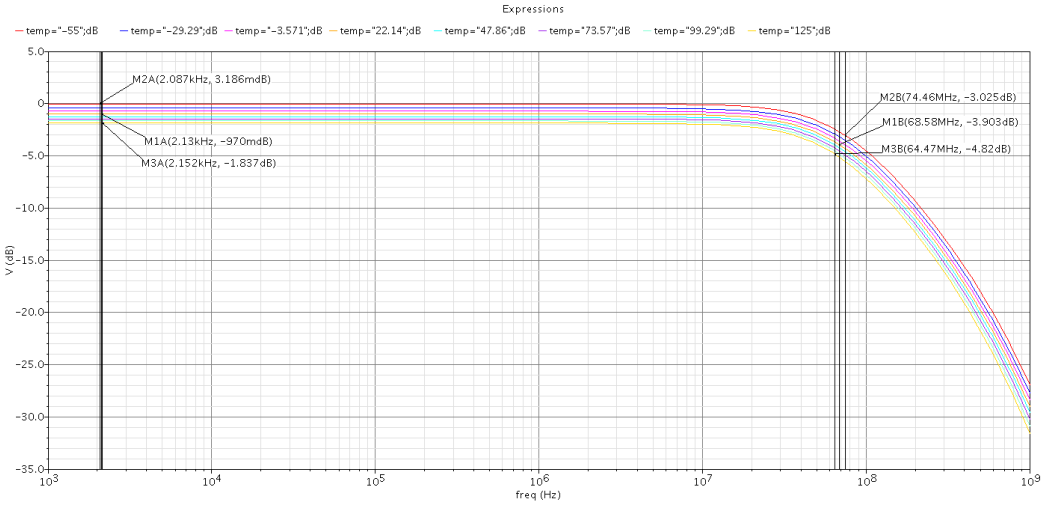


Figure 4.17. Bode plot of lowest gain.

As the proposed VGA has reached the 70 dB gain range and 3 dB bandwidth requirement, the next measurement of simulation will be the gain variation under control voltage, which is the most important performance of a dB-linear VGA. The simulation is run using ac sweep on the variable of control voltage V_C. V_C goes from 0 to 200 mV, controlling the dc voltage gain from approximately 0 dB to 70 dB. Therefore, the plot should be ideally a straight

line with a constant slope. The simulation result on gain variation is shown in Figures 4.18, 4.19 and 4.20 for each temperature, respectively.

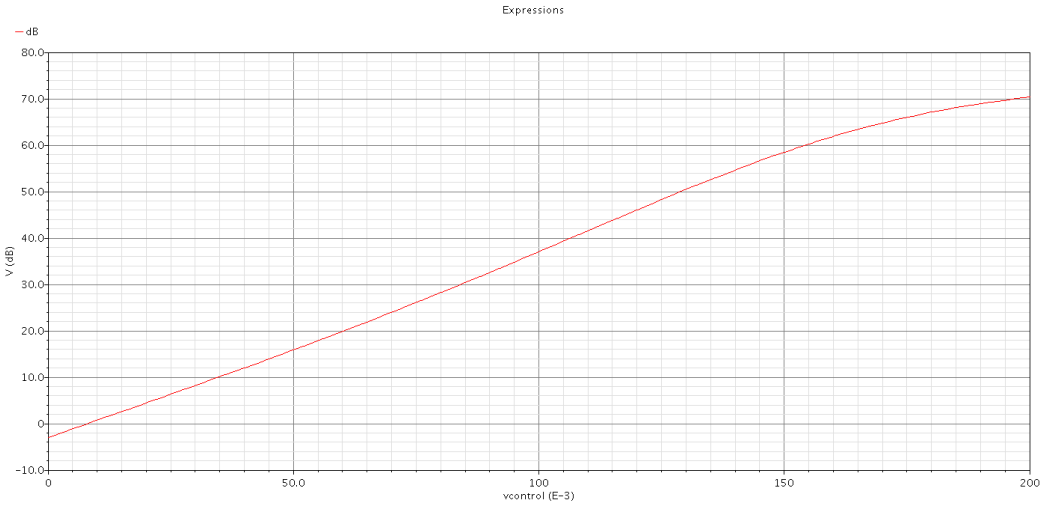


Figure 4.18. dB gain vs. control voltage at 27 ^{0}C.

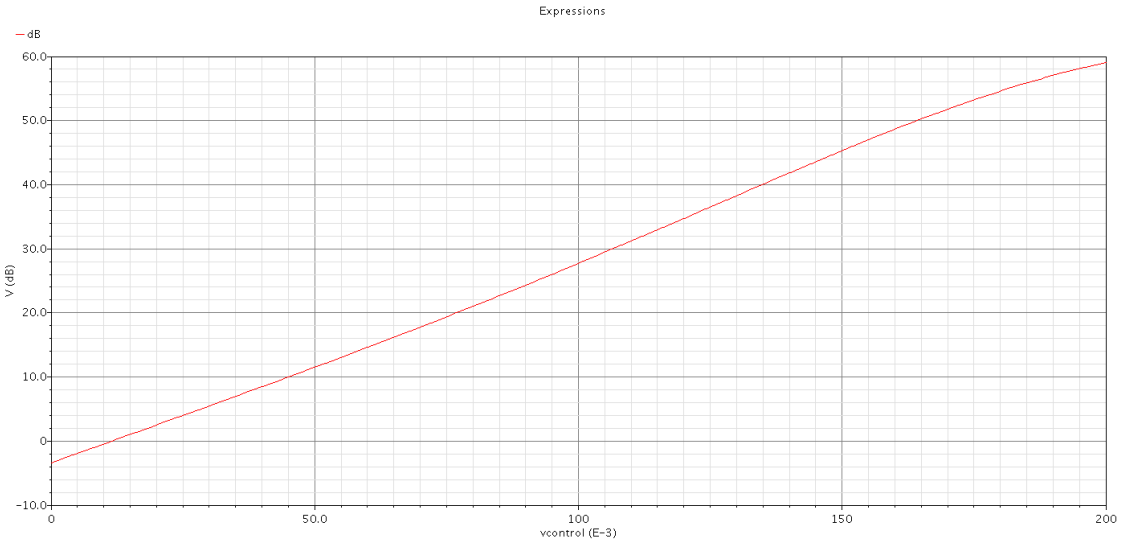


Figure 4.19. dB gain vs. control voltage at 125 ^{0}C.

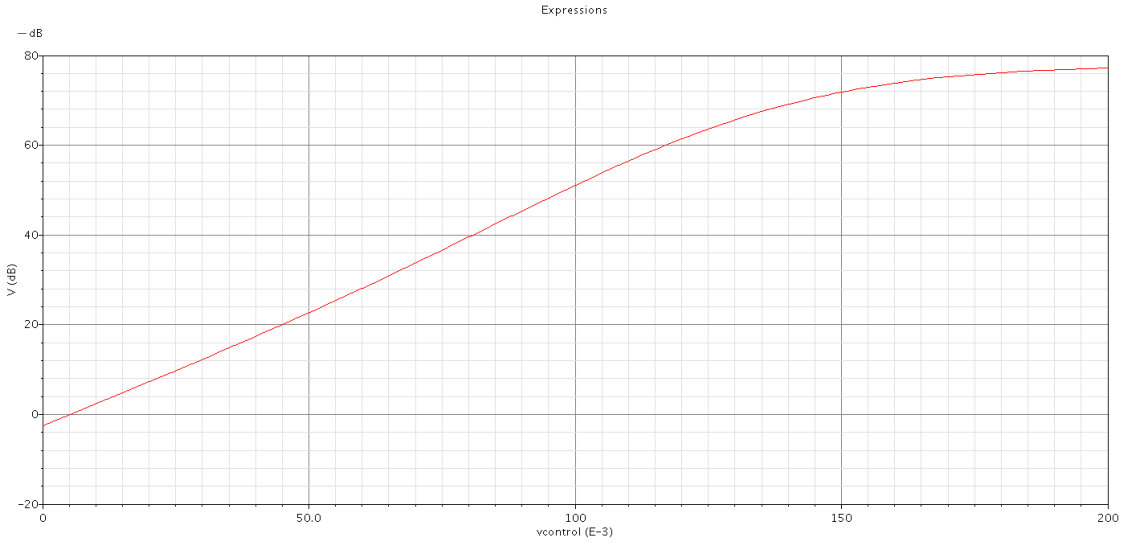


Figure 4.20. dB gain vs. control voltage at -55 ^{0}C.

According to those three figures above, when temperature increases, the dB-linearity of the VGA becomes better. The reason for this is that the dc voltage gain increases when temperature decreases and vice versa. So the output of the VGA may get saturated easily, causing the gain to increase "slower", and therefore causing the distortion on the dB-gain linearity. Another set of simulation is run below to verify why the gain falls when temperature increases.

Recall from the schematic of the gain amplification stage that the voltage gain is determined by the ratio of two bias currents I_{C1} and I_{C2}. As the gain falls when temperature increases, it is reasonable to assume that the bias currents I_{C1} and I_{C2} may vary according to temperature. Therefore, a temperature sweep simulation from -55 ^{0}C to 125 ^{0}C is run to measure the two bias currents of each of the three gain amplification stage. Figure 4.21 shows the variation of I_{C1} and I_{C2} in each of the stages.

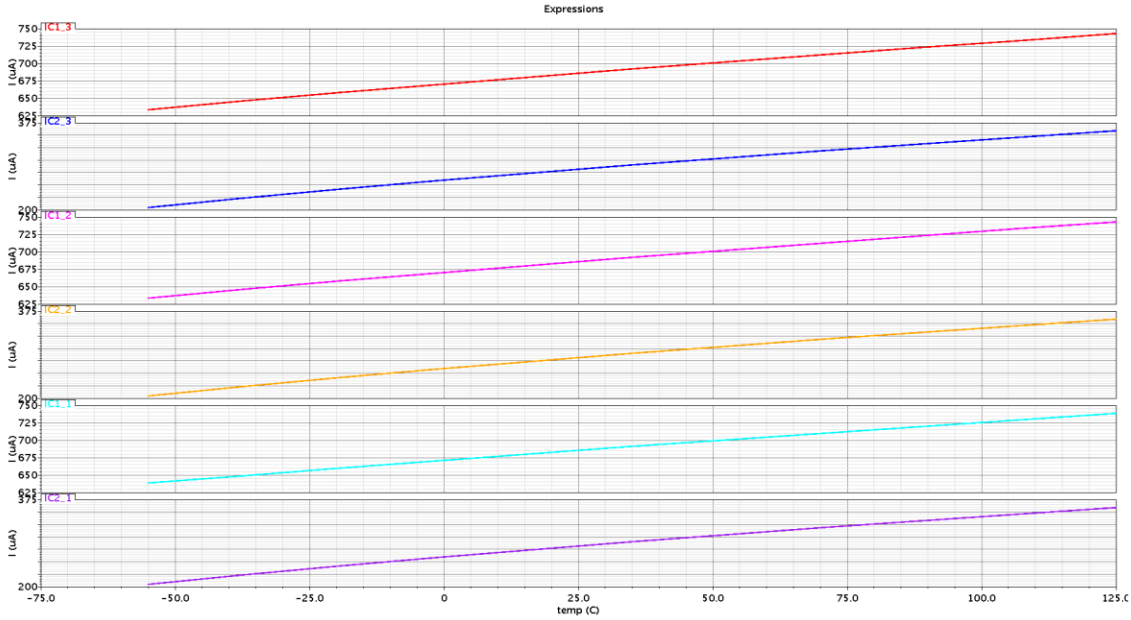


Figure 4.21. Bias current variation with temperature

According to Figure 4.21, when temperature increases, the two bias currents I_{C1} and I_{C2} also increase at nearly the same rate. In a given ratio, if both the numerator and the denominator are increased by the same amount, the value of the ratio will be decreased. Therefore, if the bias currents I_{C1} and I_{C2} increase with same rate, the gain, which is determined by their ratio, will be decreased.

The next measurement will check the pole placement of the whole circuit. The proposed VGA is designed to be an open loop system. And there is no feedback from its output to its input when it is operating in the RF channel. Therefore, if the system is supposed to be stable, it is necessary to make sure that all the poles are in the left half plane. Figure 4.22 shows all pole placements in the VGA circuit. It is obvious that the real part of each pole is negative, and that ensures a stable VGA circuit.

Poles (Hz)

	Real	Imaginary	Qfactor
1	-1.61941e+07	0.00000e+00	5.00000e-01
2	-2.90961e+07	0.00000e+00	5.00000e-01
3	-3.61149e+08	0.00000e+00	5.00000e-01
4	-1.61004e+09	+/- 3.93869e+09	1.32141e+00
5	-1.21832e+09	+/- 4.21599e+09	1.80104e+00
6	-5.74014e+09	0.00000e+00	5.00000e-01
7	-6.02683e+09	0.00000e+00	5.00000e-01
8	-6.99537e+09	0.00000e+00	5.00000e-01
9	-9.29963e+09	0.00000e+00	5.00000e-01
10	-3.16255e+10	0.00000e+00	5.00000e-01
11	-3.16311e+10	0.00000e+00	5.00000e-01
12	-1.10215e+11	0.00000e+00	5.00000e-01
13	-1.15753e+11	0.00000e+00	5.00000e-01
14	-1.58078e+10	+/- 1.21643e+11	3.87993e+00
15	-1.30414e+11	0.00000e+00	5.00000e-01
16	-1.30648e+11	0.00000e+00	5.00000e-01
17	-1.38878e+11	0.00000e+00	5.00000e-01
18	-1.38949e+11	0.00000e+00	5.00000e-01
19	-1.96481e+11	0.00000e+00	5.00000e-01
20	-1.96482e+11	0.00000e+00	5.00000e-01
21	-1.99651e+11	0.00000e+00	5.00000e-01
22	-1.99656e+11	0.00000e+00	5.00000e-01
23	-2.84991e+11	0.00000e+00	5.00000e-01
24	-2.96543e+11	0.00000e+00	5.00000e-01
25	-5.45649e+11	0.00000e+00	5.00000e-01
26	-5.56358e+11	0.00000e+00	5.00000e-01
27	-5.57101e+11	0.00000e+00	5.00000e-01
28	-5.59864e+11	0.00000e+00	5.00000e-01
29	-7.01285e+11	0.00000e+00	5.00000e-01
30	-7.01356e+11	0.00000e+00	5.00000e-01

Figure 4.22. Pole placement of VGA circuit.

4.3.4 Output settling time

How fast the output signal may settle in response to the control voltage alternating is another important performance of the VGA. If the VGA has short signal settling time, it may greatly increase the working efficiency of the AGC loop where it is located, and even the whole RF channel. In order to measure the settling time a piecewise linear (PWL) voltage source is used to provide a gain control voltage with sudden steps, and the resulting output waveform variation is observed. In this measurement, five control voltage levels are set in the PWL voltage source. Those voltage levels are 0 mV, 10 mV, 50 mV, 100 mV, 150 mV and 200 mV. Each voltage level lasts for 1 μs to provide adequate time for settling, and then it immediately jumps

to the next higher control voltage level. A transient simulation is run to observe the variance of output signal waveform. Figure 4.23 shows the test bench for measuring the VGA settling time.

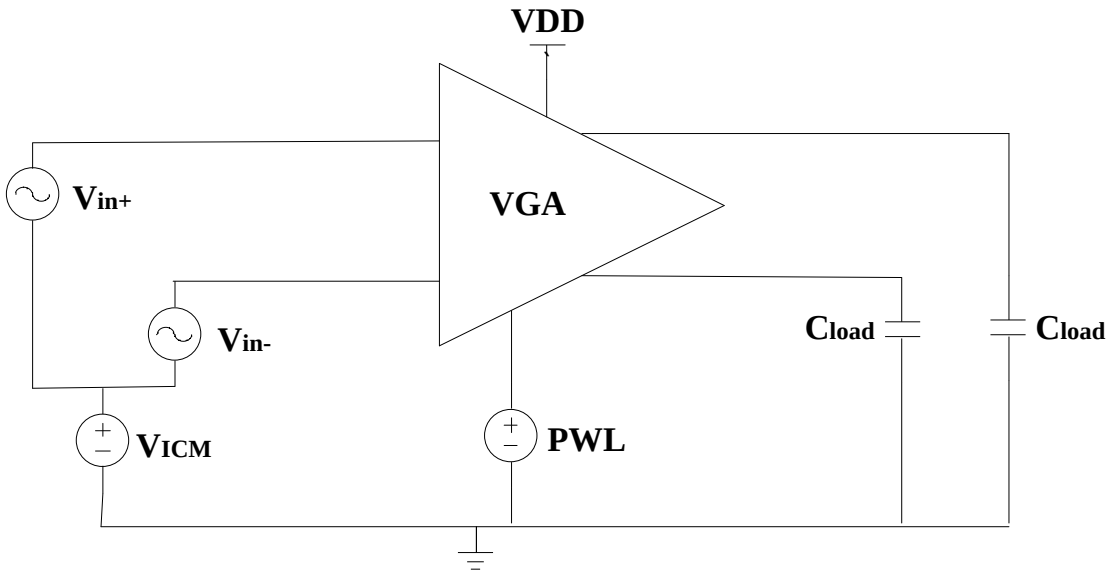


Figure 4.23. Test bench for the VGA settling time.

In the transient simulation, in order to ensure that the gain-change settling time can be accurately observed the input signal frequency is set to 20MHz. This is 10 times the required bandwidth for the circuit. The input signal amplitude is set to 20 mV. The simulation result of output waveform variation is shown in Figures 4.24 - 4.29. It is clear in Figure 4.24 that the gain of the signal starts to change immediately when the gain control voltage jumps from one value to another. And it is also shown from Figure 4.25 to 4.28 that the observed settling time of output is very short with small overshoot.

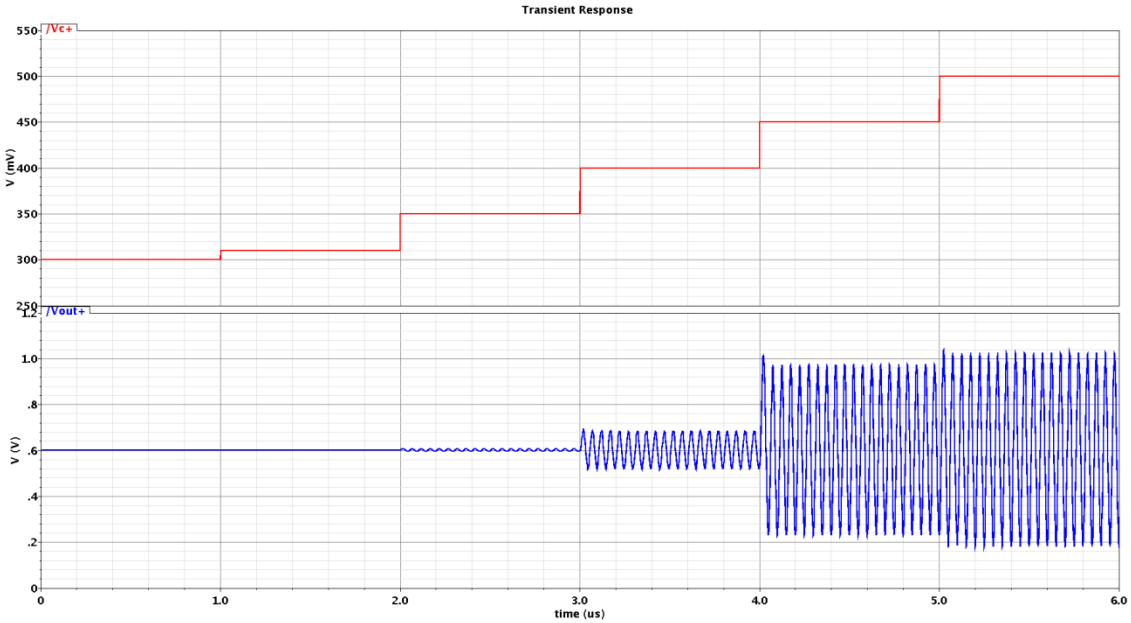


Figure 4.24. Output signal level variation under each control voltage jump.

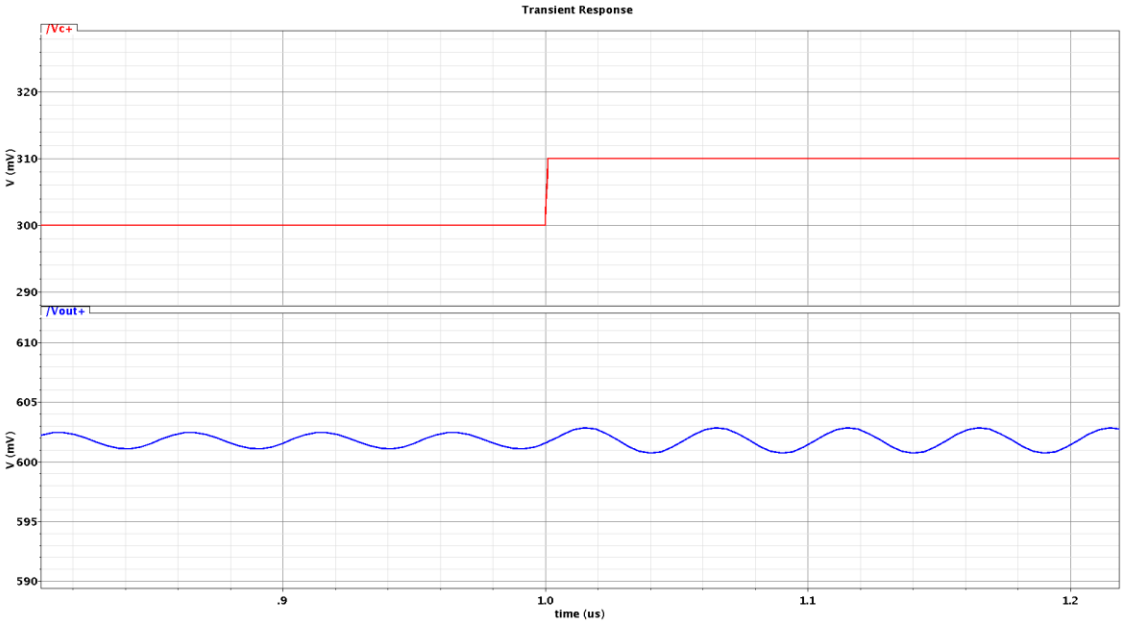


Figure 4.25. Output signal variation when control voltage jumps from 0 to 10 mV.

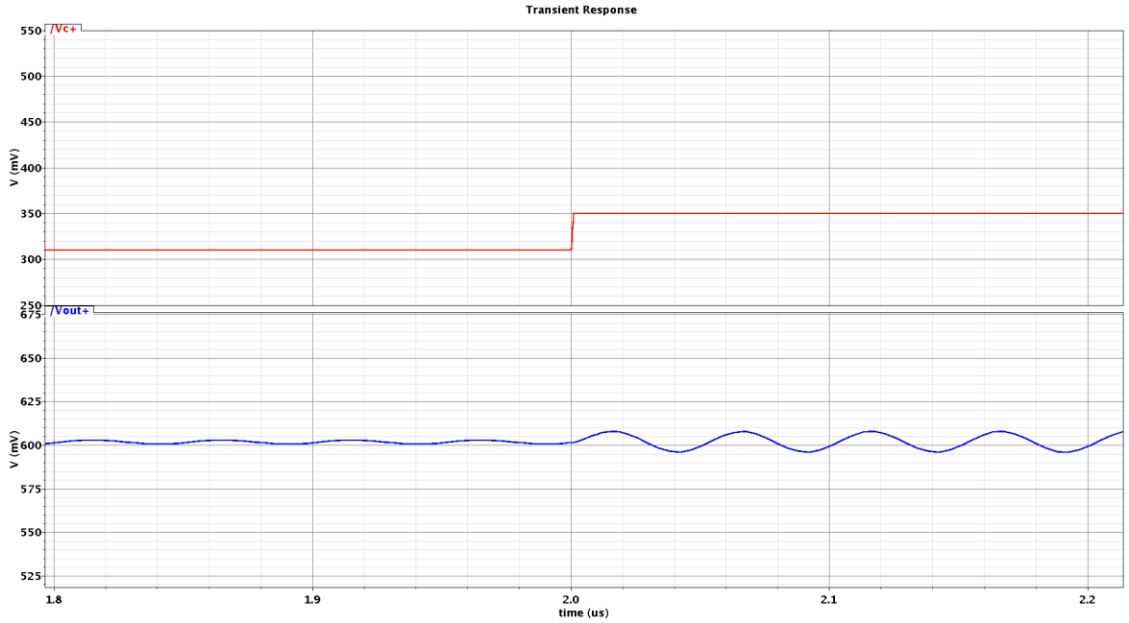


Figure 4.26. Output signal variation when control voltage jumps from 10 mV to 50 mV.

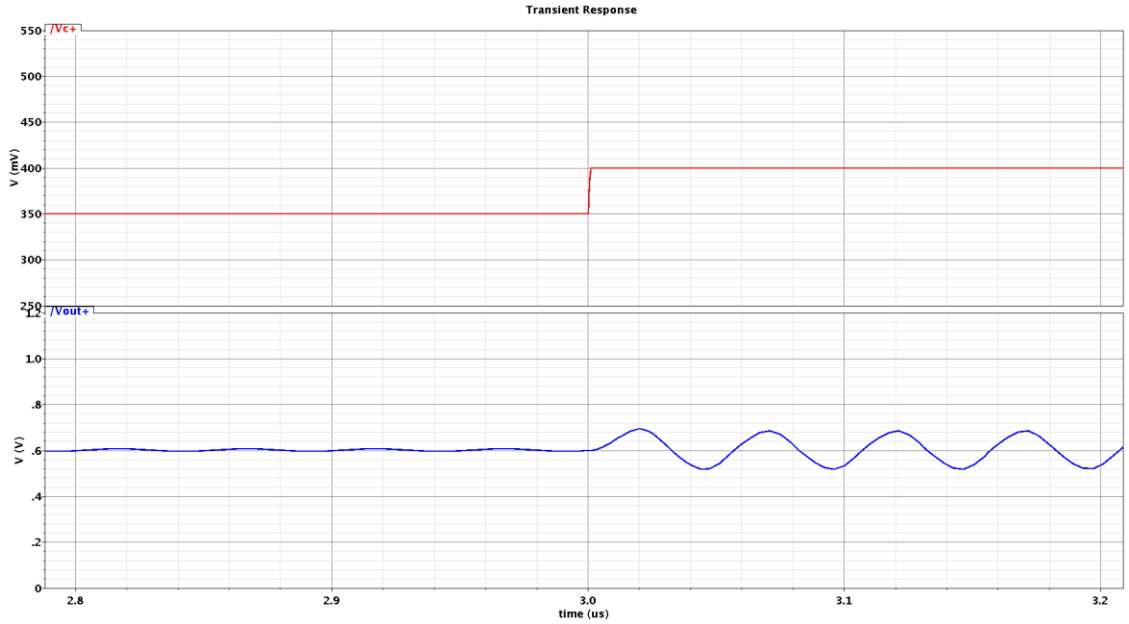


Figure 4.27. Output signal variation when control voltage jumps from 50 mV to 100 mV.

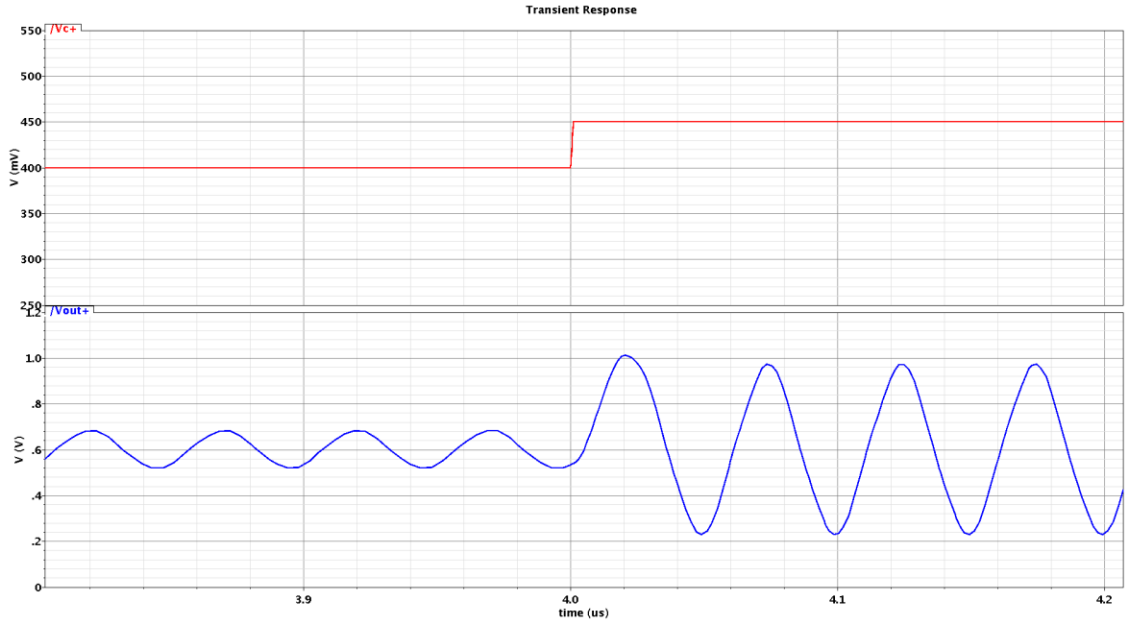


Figure 4.28. Output signal variation when control voltage jumps from 100 mV to 150 mV.

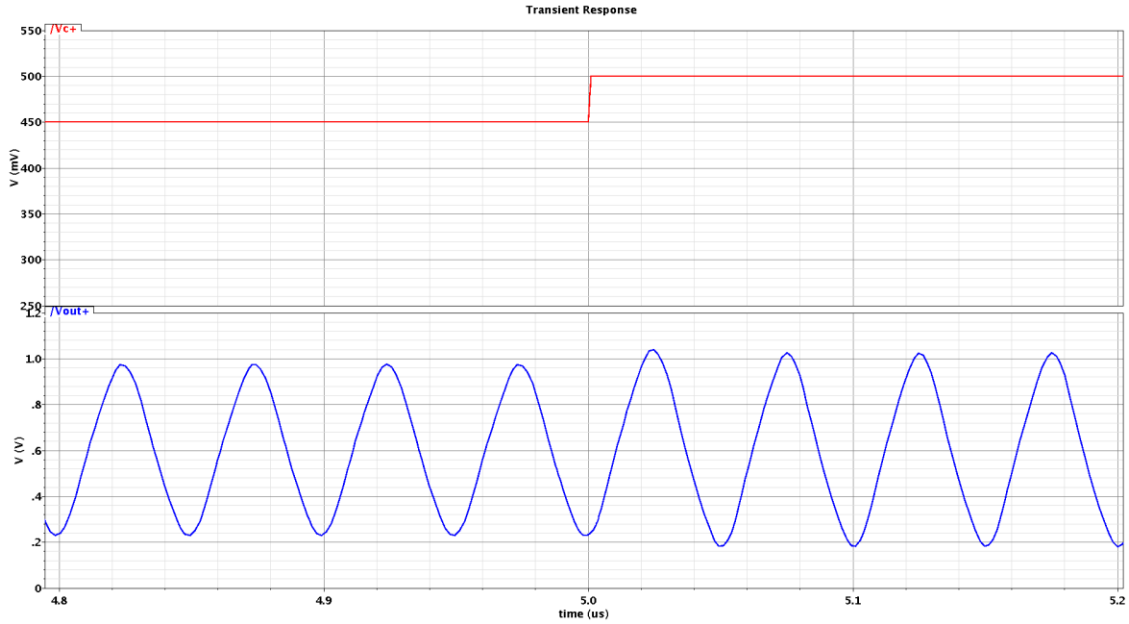


Figure 4.29. Output signal variation when control voltage jumps from 150 mV to 200 mV.

In the waveform of Figure 4.29, the output signal is amplified only slightly when control voltage reaches a higher level. The reason for this is that the signal amplitude of the output has saturated due to the circuit's output swing limitation. However, even though the output is saturated, it still responds quickly to the control voltage.

CHAPTER 5

Physical design

5.1 Chip Layout

The final step of the design flow is the physical design which is commonly known as layout in circuit design. The fully-differential variable gain amplifier is laid out using the Virtuoso layout editor inside the Cadence design kit. The main circuit layout of the VGA with dimension is shown in Figure 5.1.

Figure 5.1. Main circuit layout of VGA.

The layout of the VGA circuit is divided into four parts, as introduced in Chapter 4: gain control stage which is circled in red above, three identical gain amplification stages and their respective common-mode feedbacks which are circled in black. Table 5.1 lists the nine external pin coordinates that were bonded out and eventually would be connected to the pad ring of the die.

Table 5.1. Pins of VGA Circuit Layout

I/O	Location	Coordinate	Access layer
V_{dd}	Right	(2103, 3251)	MG
GND	Top	(2075, 3548)	MG
V_{in+}	Top	(1956, 3537)	MQ
V_{in-}	Top	(1992, 3537)	MQ
V_{out-}	Bottom	(2038, 3173)	MQ
V_{out+}	Bottom	(2060, 3194)	MQ
V_{g}	Bottom	(2003, 3156)	MQ
V_{C+}	Top	(2016, 3537)	MQ
V_{C-}	Top	(2039, 3543)	MQ

Layout in 0.13 μm technology requires careful attention to the effects of parasitic resistance and capacitance. They can seriously affect the performance of the circuit. Symmetry and minimization of area are also quite important for the layout of the fully-differential VGA circuit. The layout of the VGA in this thesis has been developed to meet all these requirements as closely as possible. Some of the techniques that have been employed for creating a good layout are discussed here.

5.2 Layout techniques

It is essential to have a very symmetric layout in order to minimize mismatches. Other advantages of symmetry are better common mode and power supply noise rejection and reduced even-harmonic distortion [14]. Especially for the proposed fully-differential VGA with differential gain control voltage, a matched layout becomes more important. To achieve a better matching between two components, like transistors, it is very important that they be laid out in the same orientation. This is because certain steps in lithography and wafer processing behave differently along different axes, giving rise to mismatches if two components are not oriented along the same axis [14]. Although it is possible to reduce short channel effect by using very

long transistors, this increases the mismatch due to the gradients along a certain axis. In order to solve this problem, common centroid layout method is applied to the VGA layout.

The common-centroid principle consists of matching multiple devices canceling linear gradient errors [14]. It makes the common center points (the centroids) of two devices coincide. The two devices that should be matched with each other, like the PMOS or NMOS differential pairs that make up most of the VGA circuit are divided into equal segments and in a certain pattern so that their centroids coincide. Figure 5.2 shows an example of such a common-centroid layout.

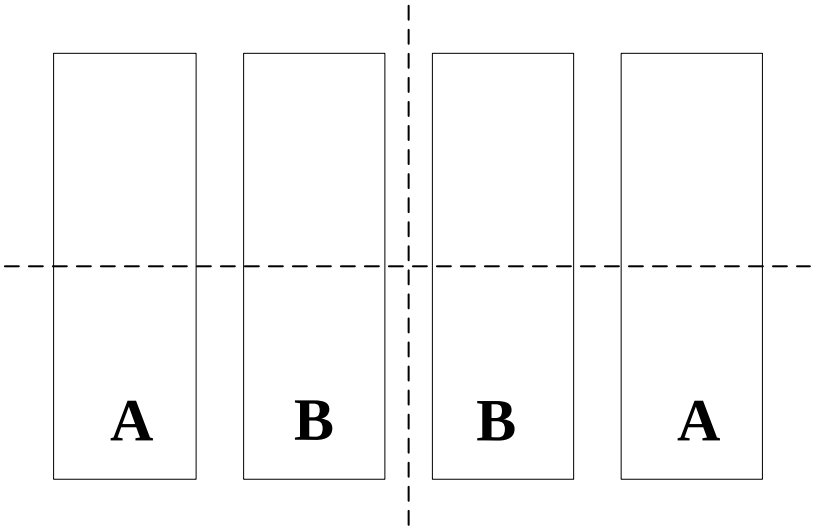


Figure 5.2. One example of common-centroid layout [14].

The VGA transistor layout should obey all four rules of common-centroid layout listed below in order to achieve a good matching [14]:

1- Coincidence: The centroids of the matched transistors coincide at least approximately.

2- Symmetry: The transistor array should be symmetric in both X and Y axes.

3- Dispersion: The array should exhibit the highest possible degree of dispersion.

4- Compactness: The array should be as compact as possible.

The example of Figure 5.2 shows the device array in only one dimension. Hence it is called the “one-dimensional array”. The devices can also be arranged to form a two-dimensional array [14]. The two dimensional array, which is applied in the layout of the VGA, gives better cancellation of gradients than the one-dimensional array [14].

If the matched transistors are large enough to be divided into more than two pieces, for example four pieces, then these components could be arranged in an array of two rows and two columns. This kind of arrangement is usually called cross-coupled pair [14]. The example of cross-coupled pair is shown in Figure 5.3. In this thesis, all the transistor pairs are layout in this pattern.

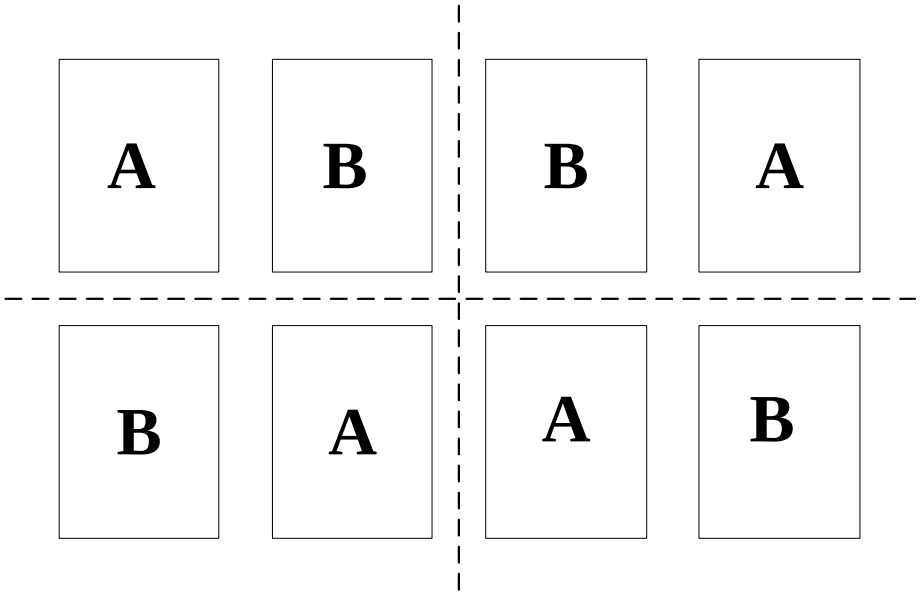


Figure 5.3. Example of crossed-coupled pairs [14].

Figure 5.3 and 5.4 shows the layout of gain amplification stage and gain control unit respectively using common-centroid layout method.

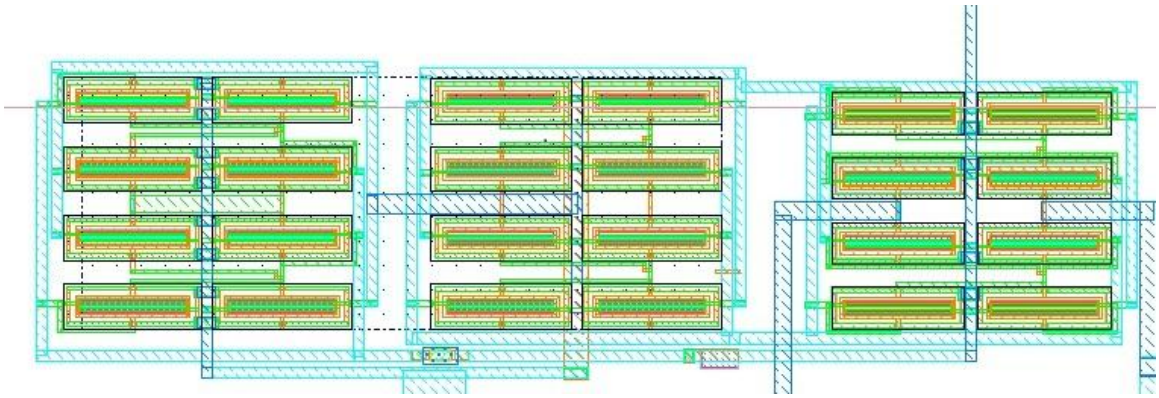


Figure 5.4. Layout of gain control unit

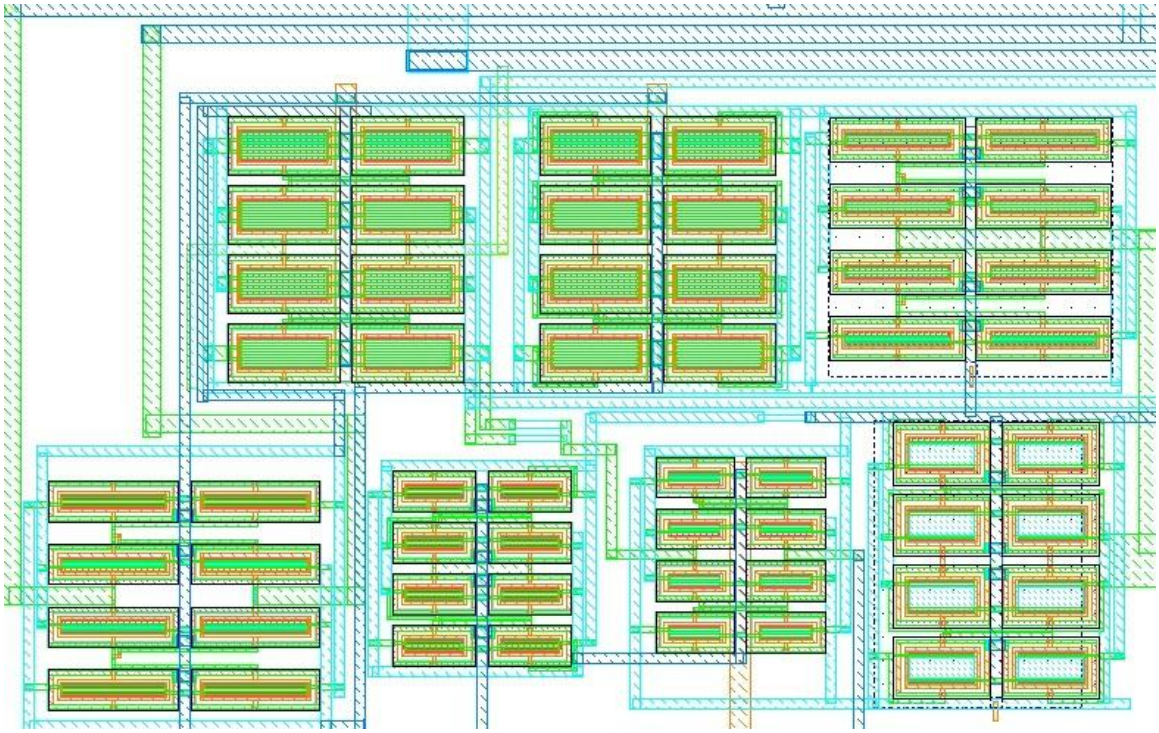


Figure 5.5. Layout of gain amplification stage

The three gain amplification stages and the gain control unit are also placed approximately symmetrical. This again improves the matching of the entire circuit.

CHAPTER 6

Variable Gain Amplifier Testing

Although the circuit simulation passes the design requirement and the layout is done with great care, it is far from being successful in this circuit design until the chip is tested after it has been fabricated. A printed circuit board (PCB) is designed using Eagle PCB Layout software to reproduce the test benches used for test setup. Different performances of the VGA including transient performance, dc performance and ac performance will be tested on the PCB.

6.1 Package Information

The VGA was bonded out and packaged at MOSIS Integrated Circuit Fabrication Service. The package used is a 64-pin plastic surface mounted package. The name of the package for the VGA chip is OCP_QFN_9X9_64A. Since it is a flat no leads package, it is directly soldered on the test board for testing. Figure 6.1 shows the bonding diagram for the VGA. The VGA is located at the up left corner of the package, and the pins connected to the pads of VGA are numbered. The pin out information is detailed in Table 6.1.

Table 6.1. Bonding Diagram Pin Out Information

Pin #	Corresponding signal
62	V_{in+}
61	V_{in-}
60	V_{C+}
59	V_{C-}
58	GND
57	V_{dd}
54	V_{OUT+}
53	V_{out-}
52	V_{g}

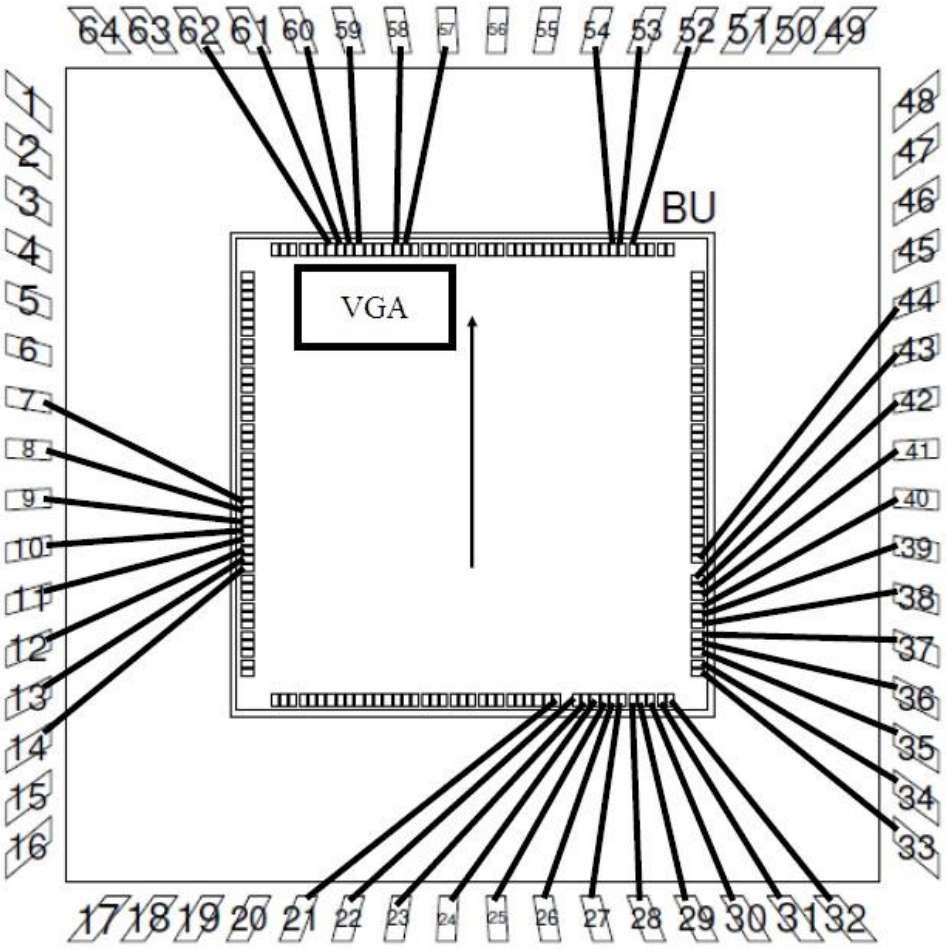


Figure 6.1. Bonding diagram of the VGA chip.

6.2 Test Board Design

A test board is indispensible for integrated circuit testing. It is not only used for the package to be plugged in, but also for establishing all the test benches used to measure the performance of the circuit designed. It has three layers: top metal layer, bottom metal layer and the ground plane. The ground plane is a copper layer that appears to most signals as an infinite ground potential. This helps reduce noise and helps ensure that all the electronic parts on the PCB compare different signals' voltages to the same reference potential. It consists of several I/O ports, like SMA and BNC connectors, for the I/O signal of the VGA package placed on it. Two MCP1825 voltage regulators are put on the test board, providing 1.2 V and 3.3 V power supply

for both the VGA chip and the operational amplifiers. Those amplifiers along with the several resistors are also soldered on the test board, they are used to assist with the testing of some of the VGA performance. This will be discussed in detail later. Figure 6.2 shows the layout of the test board.

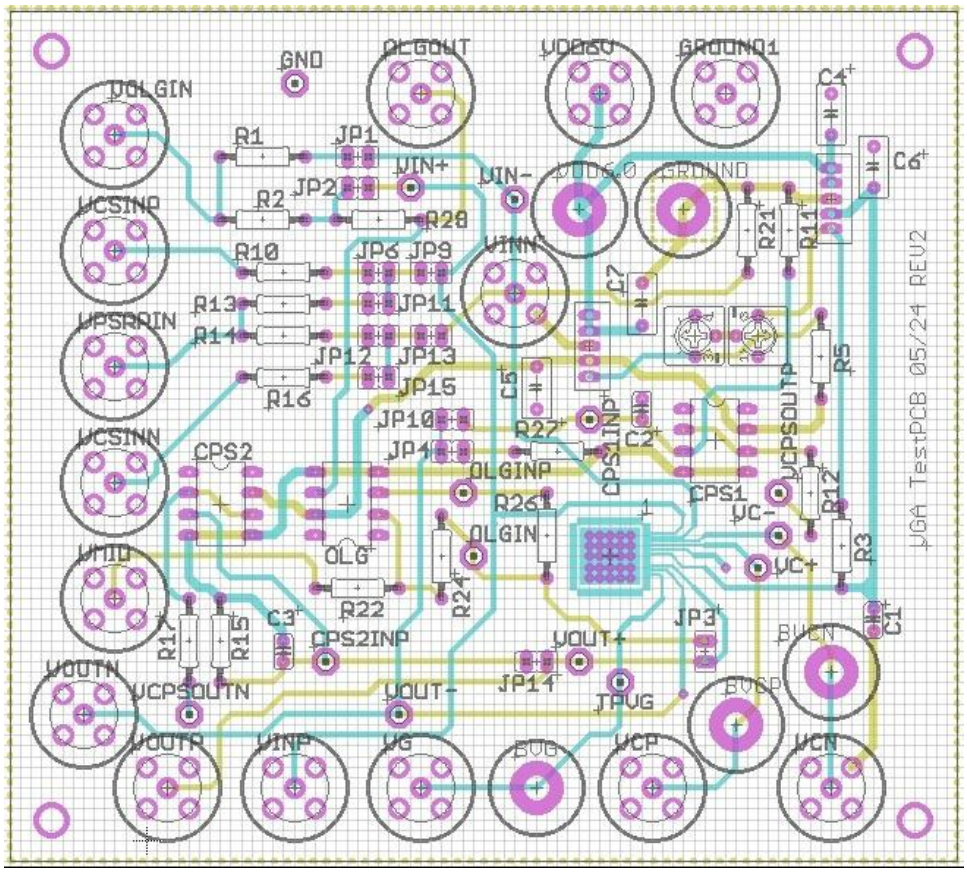


Figure 6.2. Test board layout.

6.3 Test Bench Setup

The first step for setting up the test bench is connecting the required signals to the test board. The test signals are mainly provided by the function generator and the dc power supply. The list of all the equipment used for testing is given in Table 6.2. Figure 6.3 is the diagram of the general test setup. It shows the connections between testing equipment, test board and the oscilloscope used to observe test results.

Table 6.2. Equipment Used for Testing the Amplifier

Hewlett Packard 6216A Power Supply
HAMEG HM7044 Programable Power Supply
Tektronix MSO4104 Mixed Signal Oscilloscope
Agilent 10074C Oscilloscope probes 10 MΩ & 10 pF
Hewlett Packard 3245A Universal Source
Fluke 45 Dual Display Multimeter
Fluke 73 Multimeter

The general test bench setup procedure is listed below. All the testing is taken after the general test bench setup procedure is completed.

1. Function generator, power supply and ground are connected the printed circuit board.
2. V_{C+} and V_{C-} are set to the respective voltage (+200 mV for maximum 70 dB gain and 0 for 0 dB gain) depending on the test.
3. DC power supplies are prechecked to have been set to the correct value before turned on.
4. V_{in+} and V_{in-} are set to the respective ac voltages combined with 600 mV common mode dc voltage.
5. Power supplies are turned on.

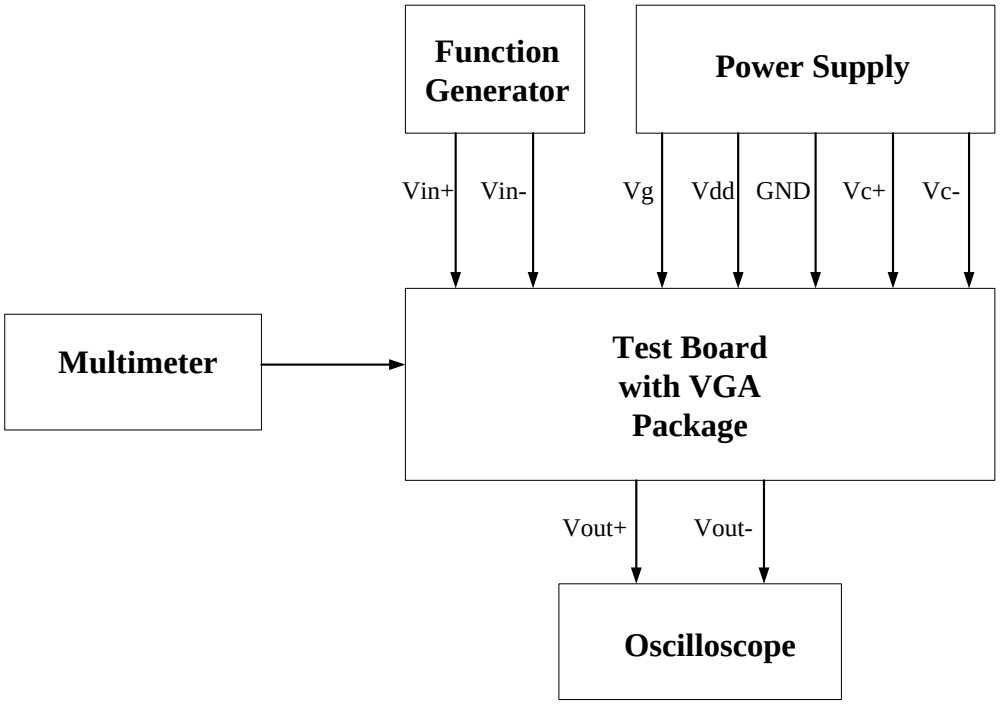


Figure 6.3. General testing setup diagram

6.4 Experimental results

The circuit testing which is performed at room temperature is described in this section. The first is the dc testing, which involves input common-mode range, input offset and the output swing.

6.4.1 Offset voltage and output swing

The offset voltage testing is combined with output swing testing. For output swing measurement, a 600 mV common-mode voltage is applied to each of the input node separately using HAMEG programmable power supply. Then, the differential voltage is varied in 10 mV steps. The output voltage is measured. During this test, the gain is set to be small enough so that the output does not sweep so fast, thereby giving an accurate result. Figure 6.4 shows the measurement of input offset voltage and the output swing.

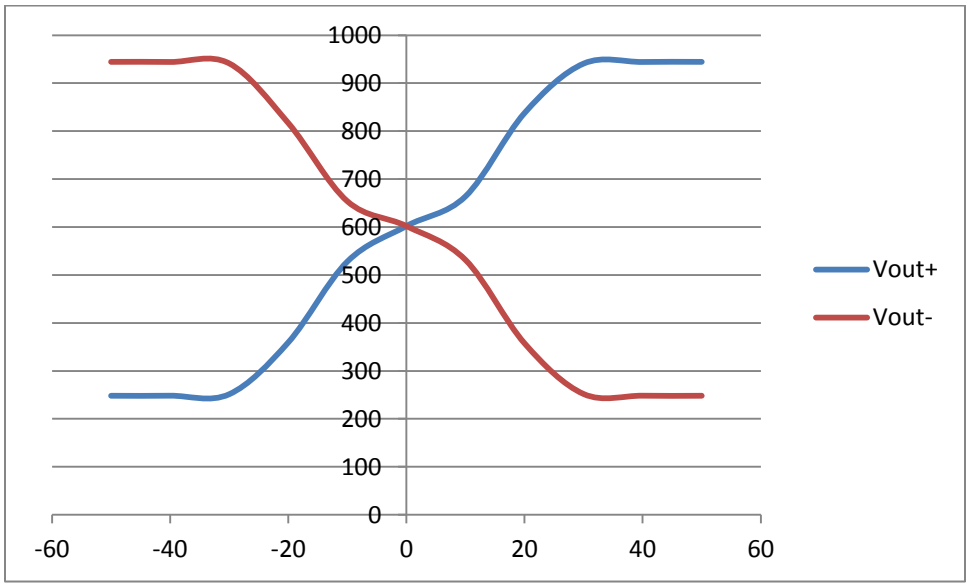


Figure 6.4. Input offset voltage and output swing.

For offset voltage measurement, the gain of VGA is set to 16 dB, which is 6.3 V/V. Then the two input nodes are connected together and are applied with 600 mV common-mode voltage.

A 3.3 mV voltage difference is measured at the output nodes. Therefore, the input offset voltage is calculated by 3.3 mV / 6.3 = 0.5 mV.

6.4.2 Input common-mode range

As the differential output nodes of the first stage are in the package, it is only possible to measure the common-mode voltage of the third stage output, which is the output of the chip. However, the problem is that when the input common-mode voltage is out of range, and output common-mode voltage of the first stage shifts away from 600 mV (which is fixed by common-mode feedback), the common-mode feedback of second and third stages start to regulate this out of range signal, and may "pull" it back to 600 mV at the final output. Therefore the input common-mode range should stay deeply in the voltage range observed from simulation. The measurements illustrate this effect as shown in Figures 6.5 and 6.6.

Figure 6.5. Output voltages under 0 to 1.2 V input sweep.

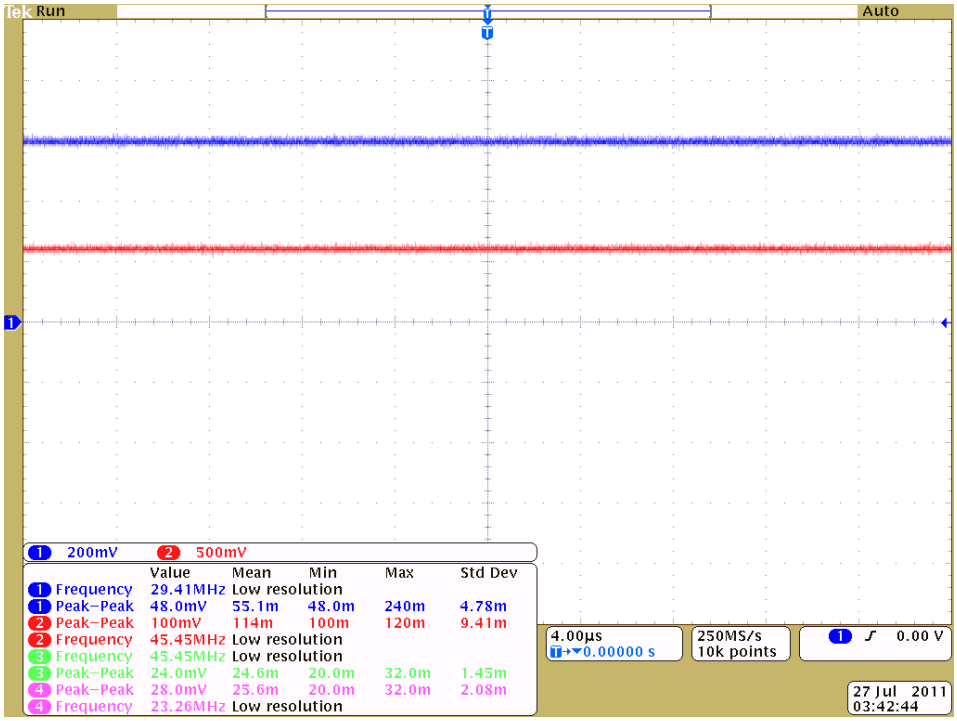


Figure 6.6. Output voltages under 0 to 1.2 V input sweep with negative output scale changed to 500 mV.

Figure 6.5 indicates that the output voltages stay at 600 mV during the sweeping of input common-mode voltage from 0 to 1.2 V. Because the two output voltage levels on the oscilloscope overlap with each other, it is hard to see their value clearly at the same time. Therefore, the scale of V_{out-} is turned up to 500 mV in the oscilloscope which is shown in Figure 6.6. Figure 6.6 clearly indicates that the voltages of V_{out+} and V_{out-} stay at 600 mV.

6.4.3 Gain testing

Theoretically, the way to test each gain of the VGA is to apply a small-signal to the input, then measure the output voltage at each gain control voltage. However this method is impossible to realize. Since the VGA has a 70 dB maximum gain, it is difficult to measure high gains by applying a voltage directly to the input of the VGA without causing it to saturate. Actually even the input offset voltage may cause the VGA output to saturate.

This problem is overcome using a second op amp connected in a feedback [15] path as shown in Figure 6.7. The second amplifier is called a nulling amplifier.

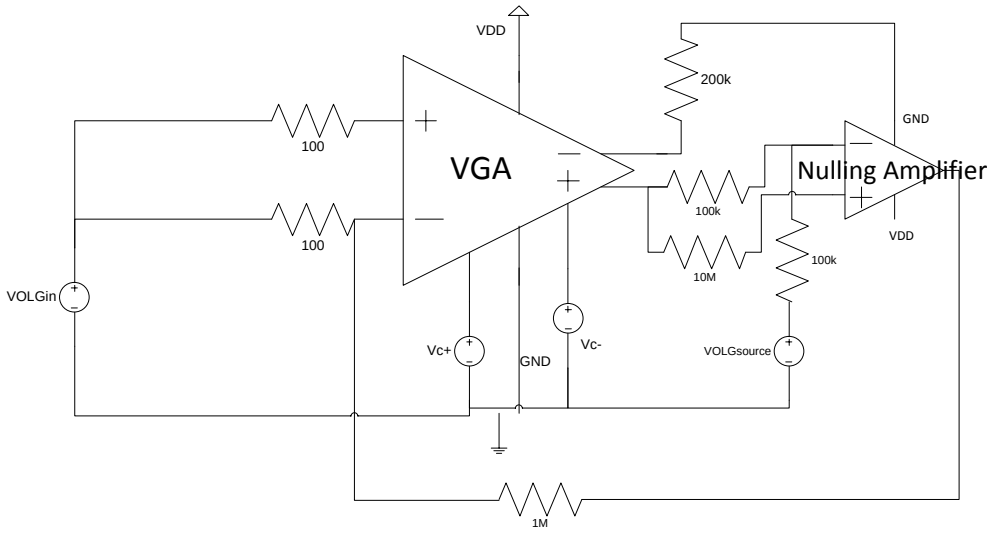


Figure 6.7. Gain test setup using nulling amplifier [15].

The gain is calculated using Eq. (6.1) shown below.

$$\text{Gain} = 20\log\left[-\frac{100+1\text{M}\Omega}{50}\frac{\Delta\text{VOLG}_{\text{source}}}{\Delta\text{Vo}_{\text{null}}}\right] \qquad (6.1)$$

The gains which are set by a control voltage larger than 40 mV are calculated using Eq. (6.1) and the rest are measured by transient testing using the oscilloscope. The control voltage varies from 0 to 200 mV in a 10 mV step. Figure 6.8, 6.9, 6.10 and 6.11 show the output voltages under low gains.

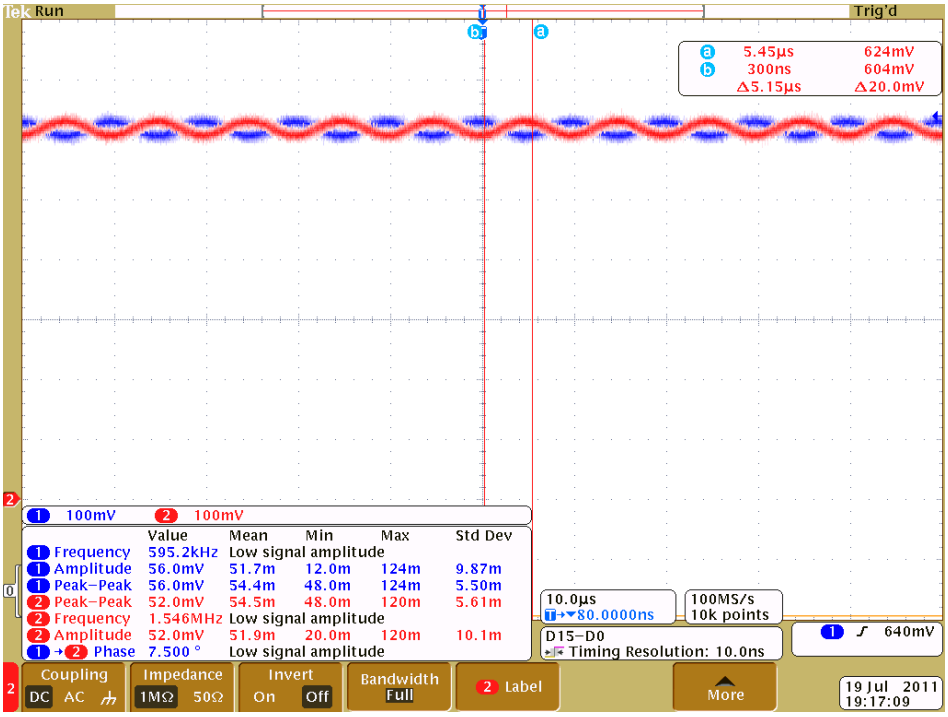


Figure 6.8. Unity gain output under 0 mV control voltage.

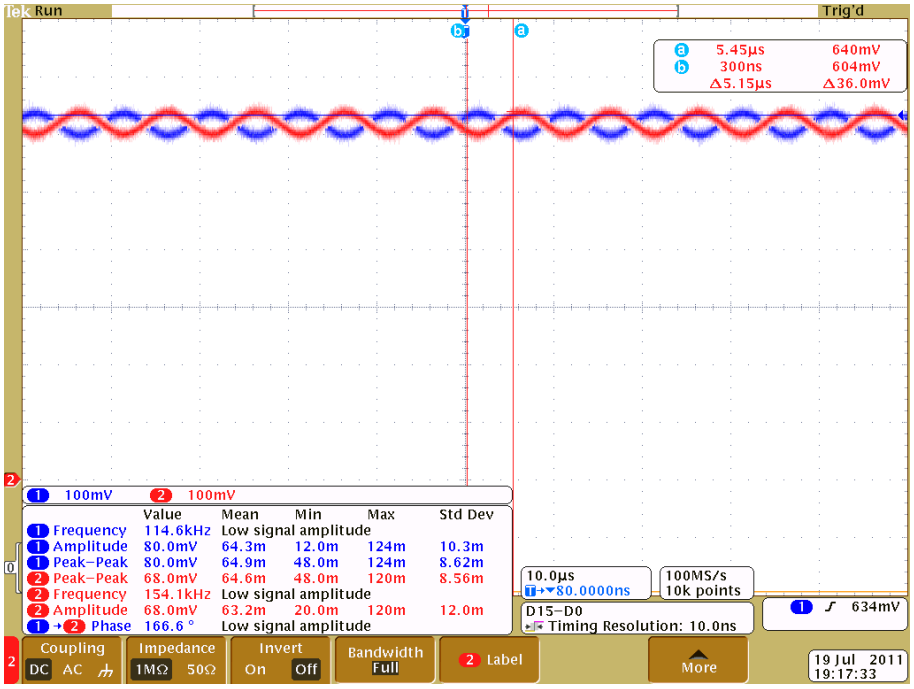


Figure 6.9. 1.5 dB gain output under 10 mV control voltage.

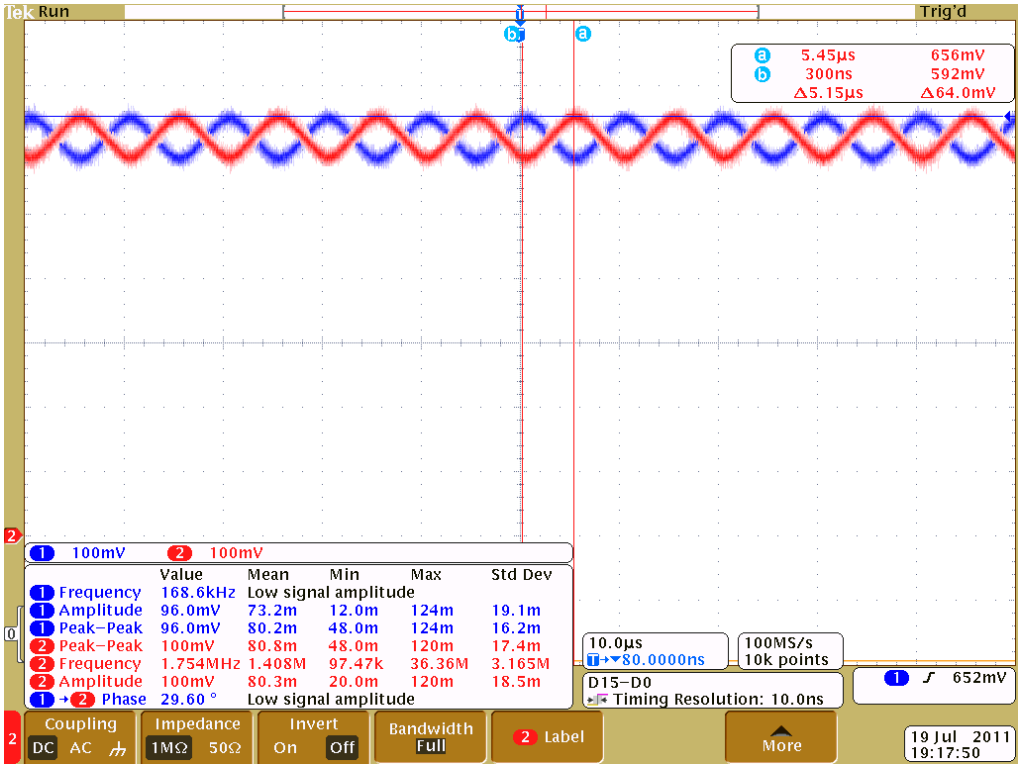


Figure 6.10. 4.6 dB gain output under 20 mV control voltage.

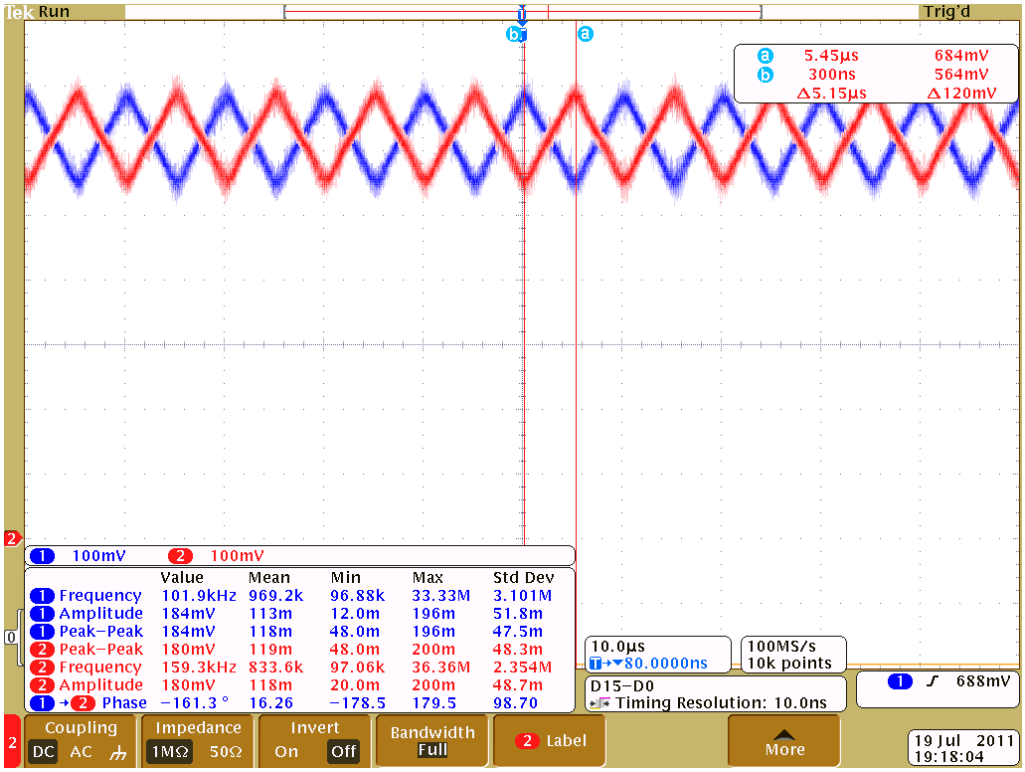


Figure 6.11. 9 dB gain output under 30 mV control voltage.

Figure 6.12 shows the gain variation under different control voltage. Comparing with the simulation result it is almost linear with little distortion.

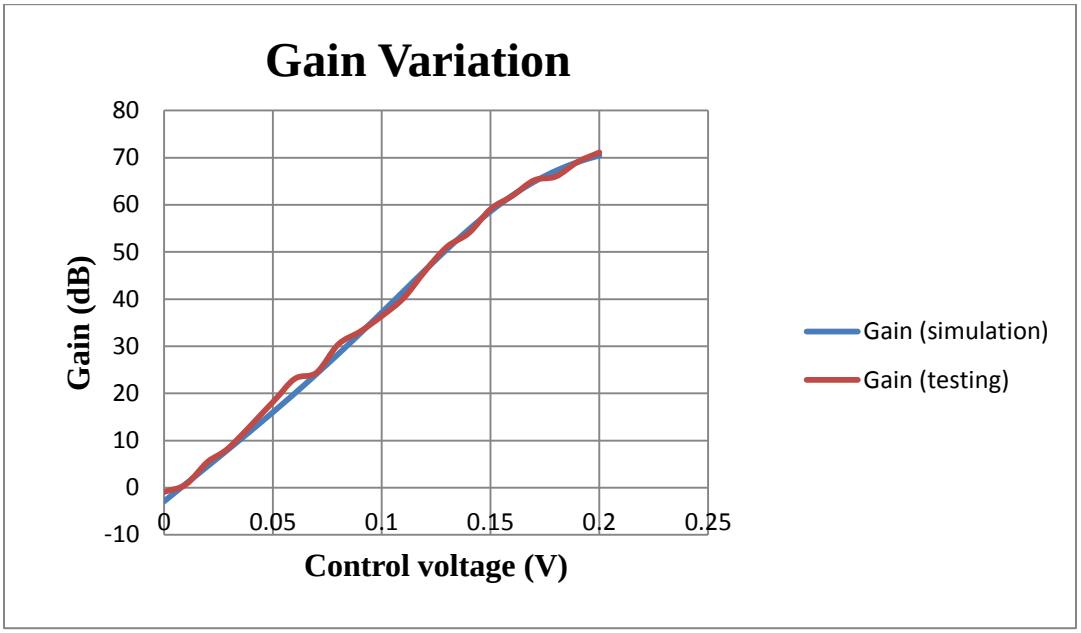


Figure 6.12. dB-linear gain of the VGA.

In Figure 6.11, the output signal starts slewing and causes distortion on the waveform. The slewing can be caused by three aspects of the VGA: load capacitance, input signal frequency and low slew rate. However, simulation with varied load capacitance and signal frequencies indicates that those two aspects do not affect the output signal much. To further understand this effect, a set of simulations was run to check both the positive and negative slew rates at different gain settings from 0 dB to 200 dB. Table 6.3 shows the simulation results.

Table 6.3. Slew Rates under Different Gain Settings

Gain (dB)	-2.9	1.5	4.6	9	12.1
SR_+ (V/μs)	30	48.5	53.6	66.9	111.5
SR_- (V/μs)	-31	-48.6	-55.4	-73.6	-118.8

16	26	37	48	59	70
151.8	188.7	186.5	175	174	171
-161.1	205.5	210.8	203.5	201	203.5

According to Table 6.3, the slew rate is low when the gain of the VGA is low, and then the slew rate starts to increase drastically as the gain increases. Therefore, when the slew rate is low under low gain sets, the output signal is slew limited and distorted. When the gain increases high enough, the slew rate also increases, providing more power to drive the load capacitance which stops the output signal from slewing.

CHAPTER 7

Future Work and Conclusions

7.1 Future Work to Improve the VGA

Although the VGA as designed meets all the design specifications and requirements, it still suffers from several defects. Therefore future work needs to be undertaken to solve these problems before the VGA is integrated to the RF transceiver.

As the three gain stages of the VGA are completely identical, the output swing of the VGA is limited. That means if the input voltage at the first stage is large, the output at the third stage may easily be saturated. This problem could be solved by using a different output stage as the third stage. As each of the gain stage provides dB-linear gain, the addition of a fixed gain output stage may not affect the overall gain linearity of the whole system. Figure 7.1 shows the block diagram of VGA with output stage added.

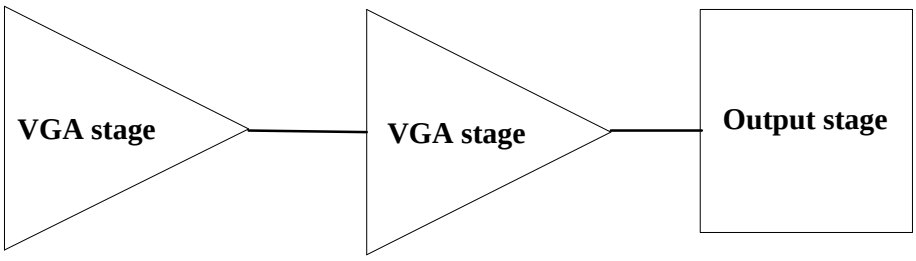


Figure 7.1. Improved VGA with output stage

Another advantage of adding a fixed gain output stage to the VGA is that it could reduce the distortion at the output. Recall the transient simulation that if the input amplitude is large, the output is distorted due to the limited output swing. Therefore, if the VGA has a large enough output swing, the output distortion could be reduced.

The most important reason for using a constant gain output stage is that it could greatly improve the gain linearity of the VGA, as shown in Figures 7.2 and 7.3.

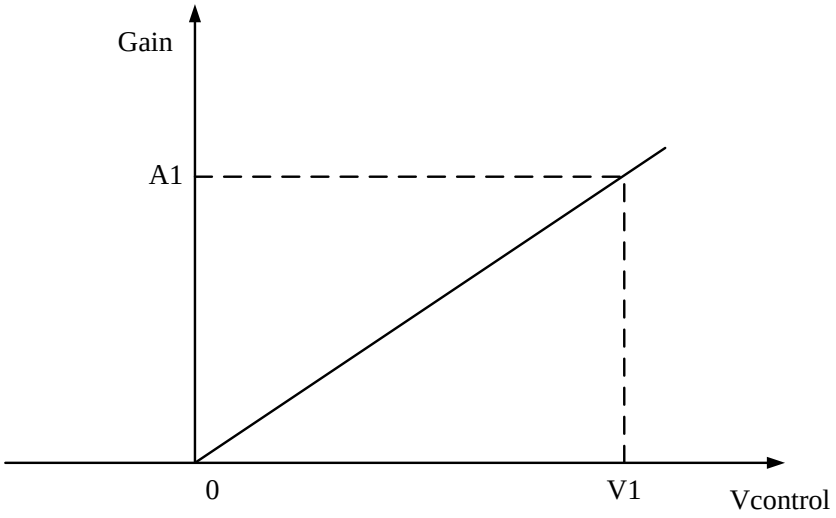


Figure 7.2. Gain variation plot of currently designed VGA.

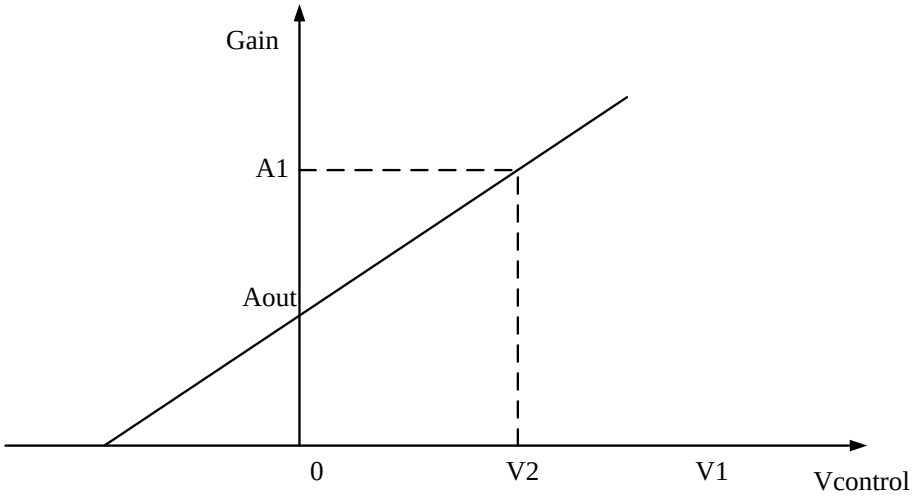


Figure 7.3. Gain variation plot of the improved VGA.

According to gain variation simulation result in Figure 4.18, the error of gain linearity is increasing during high gain under high control voltage. This is because when the gain control voltage increases, it is getting close to the limitation of pseudo-exponential equation. Therefore, it is always better to decrease the absolute range of control voltage while still maintaining the gain range.

By adding a fixed gain output stage, this goal could be achieved. Figure 7.2 shows the gain variation of currently designed VGA. The control voltage needs to reach the voltage of V_1 in order to set the required high gain. And V_1 may be close to the limitation of pseudo-exponential equation. However, in Figure 7.3, which is the gain variation plot of the improved VGA with constant gain output stage, negative control voltage could be utilized. So in Figure 7.3, the gain range remains the same while the control voltage range is greatly reduced. Therefore, a better gain linearity is provided by the improved VGA.

7.2 Conclusion

The presented thesis covers the design flow and chip testing of a fully-differential variable gain amplifier for wireless sensor network applications. The design was made to work in an RF transceiver to adjust the output signals from the low pass filter to input signal level of the ADC. The VGA eventually would be integrated in the system level design.

The fully-differential CMOS Variable Gain Amplifier (VGA) consists of differential pairs with diode connected loads, differential current control circuit, and common-mode feedback circuit. The gain is varied by the changing of two biasing currents for both the differential pair and the diode connected load. This kind of topology has many more advantages than drawbacks; therefore it could enable the VGA to achieve better performance than competing VGA topologies. As the VGA is required to have dB-linear gain variation, the pseudo-exponential approximation method is applied in the VGA design. This method gives an accurate approximation of an ideal exponential function, and enables the VGA to have accurately approximated dB-linear gain.

The VGA has been designed in the IBM 0.13μm CMOS processes. A careful layout using common-centroid layout techniques has greatly improved the performance of the VGA. In

addition, in order to eliminate the existing defects, such as output distortion and error in gain linearity, the VGA needs some future work to be improved.

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