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Thermal and Electrical Parasitic Modeling for Multi-Chip Power Module Layout Synthesis

Thermal and Electrical Parasitic Modeling for Multi-Chip Power Module Layout Synthesis

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

By

Zihao Gong
University of Arkansas
Bachelor of Science in Electrical Engineering, 2010

December 2012
University of Arkansas

Abstract

This thesis presents thermal and electrical parasitic modeling approaches for layout synthesis of Multi-Chip Power Modules (MCPMs). MCPMs integrate power semiconductor devices and drive electronics into a single package. As the switching frequency of power devices increases, the size of the passive components are greatly reduced leading to gains in efficiency and cost reduction. In order to increase switching frequency, electrical parasitics in MCPMs need to be reduced through tighter electronic integrations and smaller packages. As package size is decreased, temperature increases due to less heat dissipation capability. Thus, it is crucial to consider both thermal and electrical parasitics in order to avoid premature device failure. Traditionally, the evaluation of the temperature and electrical parasitics of an MCPM requires the layout to be changed iteratively by hand and verified via finite element analysis (FEA) tools. The novel thermal and electrical parasitics models developed in this thesis predict temperature and electrical parasitics of an MCPM according to varied layouts. Multi-Objective optimization methods are applied to the models to find optimal layouts and tradeoffs of MCPM layouts.

This thesis is approved for
Recommendation to the
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Chapter 1 Introduction

1.1 Background and Motivation

Power electronics systems compose an important piece of most alternative energy systems such as solar power, wind power, electric vehicles, etc. Power semiconductor devices, the main driving force in a power electronics system, are constantly made to switch faster in order to achieve higher efficiency and power density. However, electrical parasitics and thermal issues become more critical as the switching frequency and power density increase. For example, parasitic inductance and capacitance impose an upper limit of switching frequency because of voltage spikes, ringing, and electromagnetic interference (EMI). Voltage spikes across devices can lead to device failure due to parasitic inductance under large switching currents. EMI can cause malfunctioning of control circuitry because of radiated noise that disrupts control signaling [1]. Also, thermal overstressing can cause separation of substrate layers and fracturing of power devices due to coefficient of thermal expansion (CTE) mismatch. Thus, reduction of electrical parasitics and temperature is very important in power electronics systems.

Multi-Chip Power Modules (MCPMs) reduce electrical parasitics associated with traces and bond wires between control circuits and power semiconductor devices by integrating them into one compact package [2]. However, thermal management becomes a critical issue as packages become more compact and heat dissipation capability decreases. In an MCPM (Fig. 1.1), the die positions and trace shapes beneath the die play an important role in determining the temperature and heat flux distribution. To have better thermal performance, the die need to be spaced farther apart and the trace area needs to be expanded. However, this increases the

electrical parasitics in traces and bond wires. Thus, both electrical parasitics and temperature can be traded off during layout optimization.

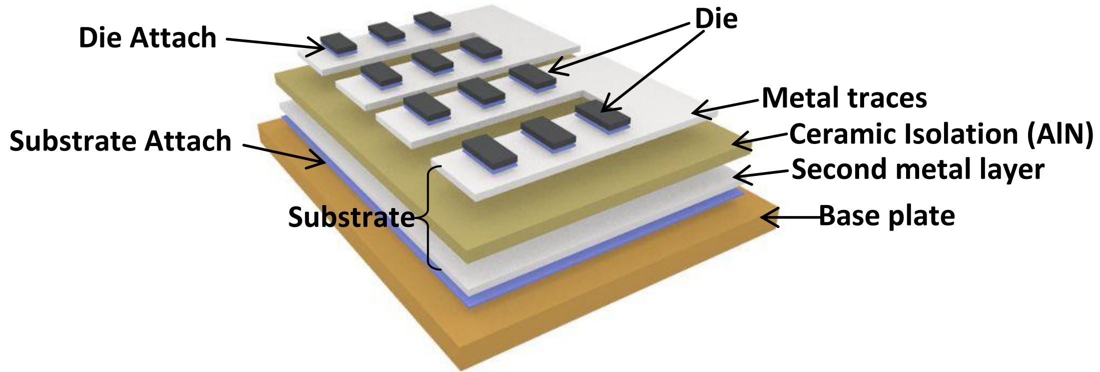


Figure 1.1: Simplified structure of an MCPM

In a conventional MCPM design process, a layout is first obtained based on circuit topology, geometric parameters, and design rules. Geometric parameters include die location and trace dimensions, while design rules typically include constraints such as minimum die spacing, minimum trace spacing, and trace thickness, etc. With the initial design in hand, electrical parasitics are extracted from the layout by an electrical parasitic extraction tool. Using the extracted results, a back-annotated electrical model is then analyzed in a circuit simulator to obtain electrical performance and heat loss information for the MCPM. Finally, a model of the MCPM is constructed in a thermal FEA tool to estimate its thermal performance using the obtained heat loss information along with ambient temperature, air-flow rate, and geometric layout. To obtain an optimal layout with lowest temperature and least electrical parasitics, geometric parameters of the layout are changed iteratively until the desired thermal and electrical performance is met [2]. For each design cycle, a time consuming thermal and electrical analysis needs to be performed.

Thermal analysis and electrical parasitic extraction are important steps in the design process because they provide information about temperature and electrical parasitics to help the designer determine the best layout. Thermal analysis is performed by finite element analysis (FEA) tools, such as SolidWorks and ANSYS Workbench [3]. Electrical parasitic extraction is commonly performed by electromagnetic field solvers based on the finite element method (FEM), such as Ansoft Q3D [4]. In the design process, FEA tools consume large amounts time while performing thermal and electrical parasitic analyses, and thus have a strong effect on the overall design process time. Further, it is inefficient to build the same MCPM model in different tools in order to perform different analyses. The objective of this thesis is to create geometry-based thermal and electrical parasitic models that may be applied efficiently for MCPM layout synthesis. These models should be able to provide reasonably accurate temperature and electrical parasitic estimation with greatly reduced time as compared to FEA tools. A multi-objective optimization algorithm can then be applied to find best trade-off solutions between thermal and electrical parasitics.

1.2 Thermal Modeling Approaches

To solve for temperature in MCPMs, a thermal FEA tool can be used, where the heat transfer equation in partial differential form is solved numerically. However, it is very computationally expensive and thus an analytic equation to solve heat transfer problems is desired. The closest related work solves the heat equation analytically by separation of variables for a system with two material layers; one containing the electronic devices and the other the substrate [5]. However, the MCPMs considered in this thesis have multiple layers of materials, where two levels of spread resistance are considered. Thus, the analytical solution presented in [5] cannot be applied to thermal modeling of MCPMs considered in this thesis.

To represent heat flow correctly and predict thermal behavior quickly, a thermal model topology is formed in analogy to electrical circuits with thermal resistance and thermal capacitance [6]. Then, the thermal resistance and capacitance are characterized by a thermal FEA tool. This is where most thermal modeling methods stop, with a characterization for a single design. In this thesis, a thermal modeling method is developed to estimate temperature changes of die under varied trace shapes, die locations, and die quantities. The key to determining temperature is to have an accurate estimation of spread resistance, which exists between layers with different areas and is highly dependent on trace shapes and die locations. The developed model uses spatial superposition of temperature and heat flux distributions to predict the change of thermal spread resistance [5]. Initial distributions of temperature and heat flux are obtained from a thermal FEA tool, which are then used by the thermal modeling algorithm, to predict thermal behavior accurately. The thermal model developed in this thesis has a significant speed up as compared to thermal FEA tools, around 10,000 times. The large speedup in thermal modeling opens up opportunities for multi-objective optimization when simultaneously considering electrical parasitics.

1.3 Electrical Parasitic Modeling Approaches

As switching frequency increases, electrical parasitics become critical in electrical behavior because they cause efficiency losses, voltage spikes, and electromagnetic interference (EMI) problems. The key to alleviating these problems is to reduce electrical parasitics in general. There are many different methods to extract the electrical parasitics of resistance, capacitance, and inductance. Most electromagnetic solvers apply the finite element method (FEM), the finite difference method (FDM), and the boundary element method (BEM) to solve Maxwell's differential equations [7]. These numerical methods are computationally expensive

and time consuming. Faster models are needed to gauge electrical parasitics under layout variation. Some related efforts describe how to model resistance and inductance of micro-strip transmission line structures, and several of the results can be applied to inductance and resistance modeling in MCPMs because there are structural similarities between micro-strips and MCPMs. The exact formulas of resistance and inductance are determined for the thin and long traces sitting on an infinite ground plane in micro-strip structures [8], [9], [10]. The exact formulas developed are based on conformal mapping techniques developed by [11]. However, MCPM traces possess a finite thickness and finite-sized ground plane. The closed-form equations for resistance and inductance of micro-strip structures that take into account the finite thickness of the traces are described in [12] and are discussed in further detail later in the thesis.

In this thesis, an inductance model of trace is developed by applying micro-strip impedance techniques, and is characterized by Ansoft Q3D to account for a finite ground plane. A resistance modeling process of the traces is illustrated by using techniques developed in micro-strip structures to account for the thickness of the traces [12]. These analytic formulas estimate electrical parasitics very quickly with some sacrifice of accuracy.

In capacitance modeling, conformal mapping techniques can be applied to account for the fringe capacitance [13], [14]. Conformal mapping techniques are generally used to transform some inconvenient geometry to a much simpler one, which helps find solutions to Laplace's equation. However, this approach is based on the assumption that the trace is infinitely long and thin. Since MCPM traces have finite length and are much thicker than micro-strip traces, conformal mapping techniques cannot be appropriately applied to capacitance modeling in MCPMs. The parasitic capacitances present in MCPMs are very similar to parasitic capacitances of interconnect in VLSI because the length and thickness of interconnects in VLSI are about the

same relative size [15]. As in VLSI, an MCPM's primary component in capacitance modeling involves the fringing electric field lines on the side surfaces of traces. Thus, a modeling process is described to help approximate this fringe capacitance effect.

1.4 Thesis Outline

Fig. 1.2 shows the overall flow of the proposed MCPM layout synthesis tool. The thermal and electrical parasitic models contribute a significant portion of the layout tool. The objective of this thesis is to create thermal and electrical parasitic models which can be utilized for MCPM layout synthesis. The optimal layouts are generated by applying a multi-objective optimization algorithm in order to find the best tradeoff between thermal and electrical parasitics. In the modeling process, an initial layout design, including geometry sizes and material properties, needs to be provided first. Then, a thermal behavior extraction tool, such as ANSYS Workbench, is used to create the lumped thermal model. An electrical parasitic extraction tool, such as Ansoft Q3D Extractor, is used to create a lumped electrical parasitic model. Finally, the thermal and electrical parasitic models are integrated into a multi-objective optimization problem which generates a set of optimal layouts.

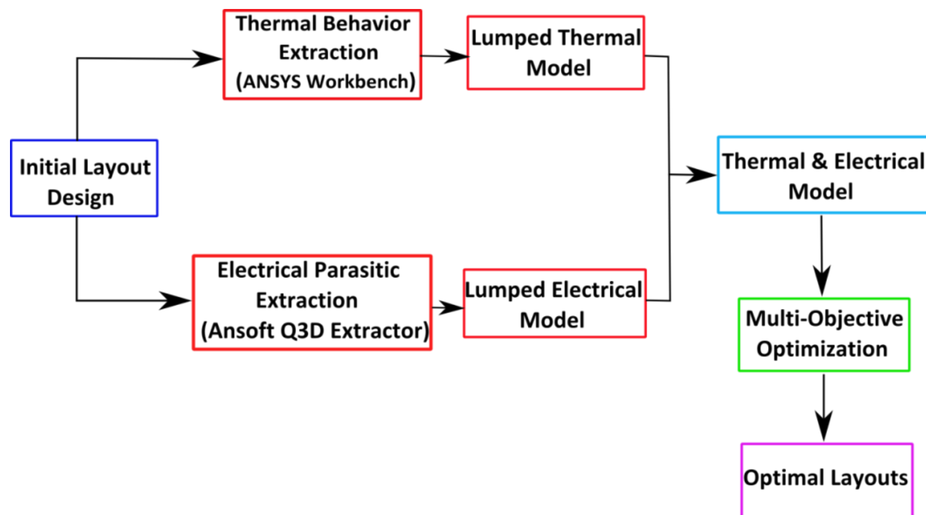


Figure 1.2: MCPM layout synthesis tool flow chart

There are five chapters in this thesis. Chapter 1 is the introduction, which describes the general background of MCPMs, the motivation of this work, and the modeling approaches of thermal and electrical parasitic models. Chapter 2 concentrates on thermal modeling for MCPMs. In this chapter, the thermal model topology is developed and verified. The thermal modeling characterization process is described, and then the fast thermal modeling algorithm is developed and verified. Chapter 3 concentrates on electrical parasitic modeling for MCPMs. In this chapter, resistance, inductance, and capacitance models associated with traces in MCPMs are formed and verified. Resistance and inductance models of bond wires are introduced. A parasitic extraction algorithm is developed using the parasitic models and verified with a single switching position example. Chapter 4 demonstrates a multi-objective optimization where thermal and electrical parasitic models are integrated to produce a set of optimal layouts. Chapter 5 is the conclusion and future work.

Chapter 2 Thermal Modeling for MCPMs

In this chapter, a novel thermal modeling method which estimates temperature under varying trace shapes, die locations, and die quantities is described. First, a lumped element thermal model topology, which represents heat flow in MCPMs, is formed by thermal resistance and thermal capacitance elements, and is verified with a thermal FEA tool. Then, a thermal modeling algorithm is developed to determine an accurate thermal resistance for the thermal model topology. An initial characterization of temperature and heat flux from a thermal FEA tool is used in the thermal modeling algorithm in order to predict an accurate estimation of thermal spread resistance. Last, the thermal model is verified to predict steady-state temperature correctly under varying layout, die positioning, and die quantities.

2.1 Thermal Model Topology and Verification

In this section, a lumped element thermal model topology of MCPMs is described. In steady-state thermal analysis, the thermal model topology consists of only thermal resistances and heat sources. For full transient thermal analysis, both thermal capacitances and thermal coupling coefficients need to be included in the thermal model topology. The thermal model developed in this thesis only predicts steady-state temperature because it simplifies the model to make quicker solutions. However, for thermal model topology verification, thermal capacitances are included and an extraction algorithm is developed. Thermal resistances and capacitances in the thermal model topology, as shown in Fig. 2.3, are extracted with ANSYS. Next, the thermal

model topology is constructed in the multi-disciplinary Saber circuit simulator [16], and the transient temperature data from Saber is compared to the data from ANSYS for verification.

2.1.1 Thermal Model Topology

In any thermal system, heat energy disperses through three mechanisms: conduction, convection, and radiation [17]. Conduction allows heat energy generated by the semiconductor die to flow down through the substrate and base plate layers of the system where it is finally dissipated into the ambient environment by convection. Heat dissipation by black body radiation only contributes a small part to the heat dissipation, so it is neglected.

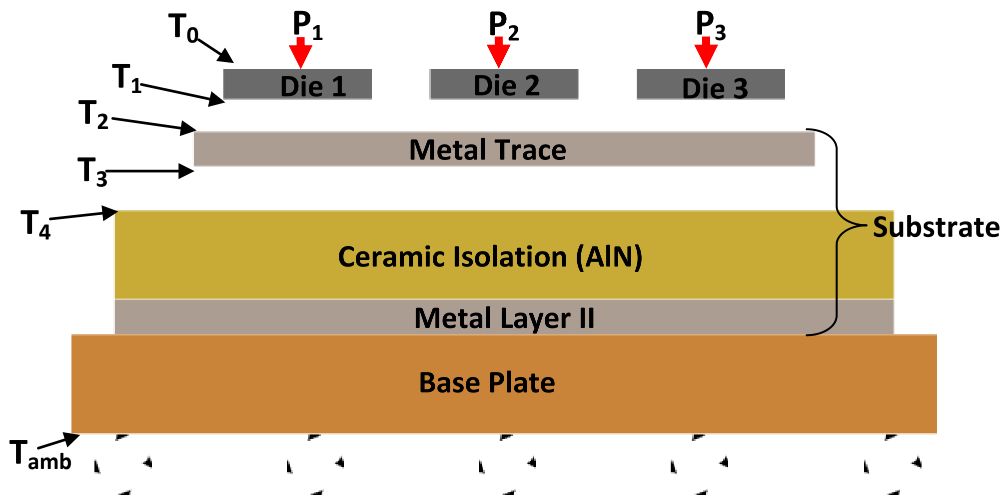


Figure 2.1: Cross-section view of an MCPM

A lumped element thermal model is created in analogy to an electrical circuit, where heat flow is analogous to current, temperature to voltage, and thermal impedance to electrical impedance (Table 2.1). The lumped thermal model can be represented by a Foster network which is formed by RC tanks, where each layer in an MCPM is represented by an RC tank (Fig. 2.2). It is equivalent to a Cauer network (Fig. 2.2) by applying the Foster-to-Cauer transformation [18]. With the Cauer network, the calculation of thermal capacitance is determined by only the transient temperature from the upper node of a capacitance since the lower node is connected to

ground. The Foster network requires transient temperature differences from both nodes of a capacitance. Therefore, the Cauer network is used for the lumped thermal model.

A thermal model topology of an MCPM with three die is shown in Fig. 2.3. The heat flow, P_n, is determined by the electrical power loss from the die and is modeled as a constant heat source. The branch highlighted in red in Fig. 2.3 can be duplicated depending on the quantity of die in an MCPM. Each material layer in Fig. 2.1 is represented by a thermal resistance and a thermal capacitance.

Table 2.1: Equivalent Thermal and Electrical Parameters

Thermal		Electrical	
Temperature	T in *K*	Voltage	U in *V*
Heat Flow	P in *W*	Current	I in *A*
Thermal Resistance	R_{th} in *K/W*	Resistance	R in *V/A*
Thermal Capacitance	C_{th} in *Ws/k*	Capacitance	C in *As/V*

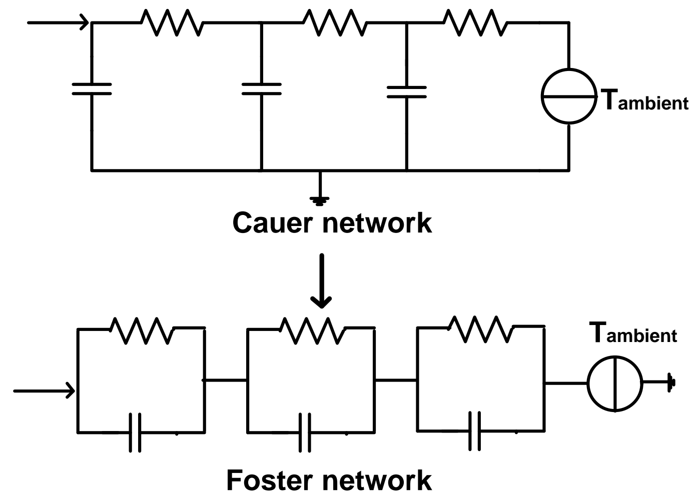


Figure 2.2: Cauer and Foster equivalent networks

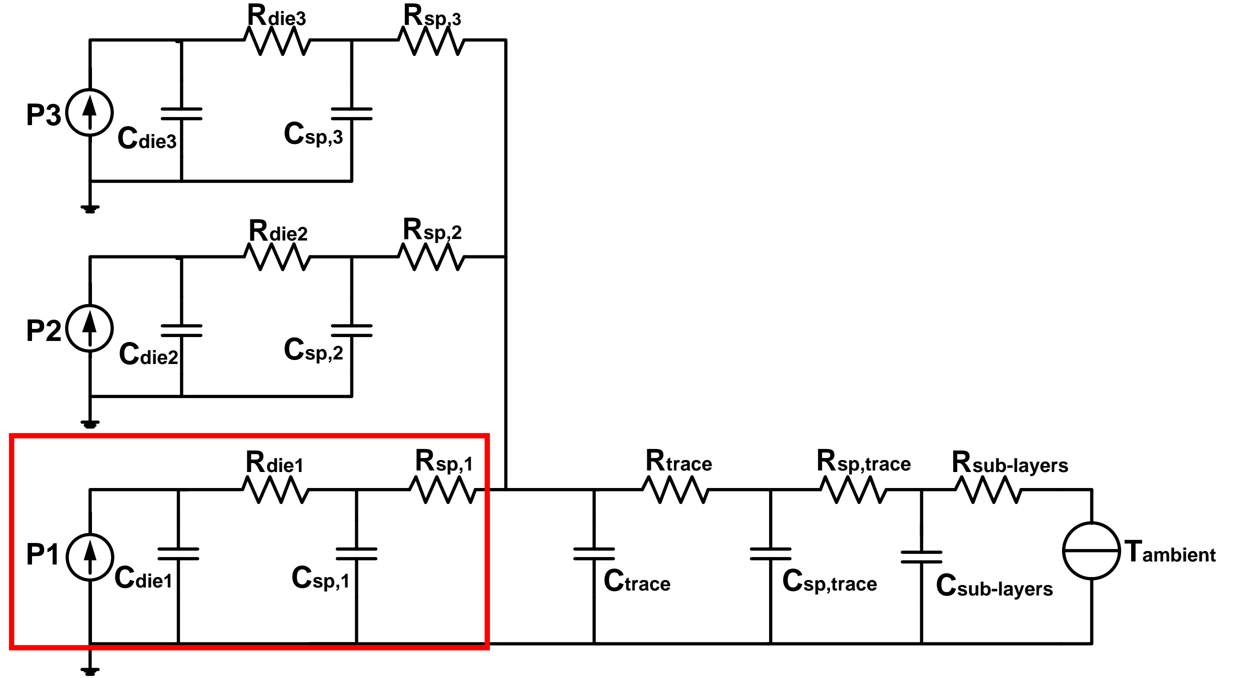


Figure 2.3: Thermal model topology (Cauer form) of an MCPM

The thermal resistance of each layer and thermal spread resistance [17], existing between two layers with different conduction area, can both be determined by:

$$R_{thermal} = \frac{T_i - T_{i+1}}{P} \quad . \tag{2.1}$$

where T_i and T_{i+1} are the average temperatures of the start and end surfaces of the layer and P is the heat flow through the layer [6], [19]. The thermal resistance of the trace layer is small because of its thinness and relatively high thermal conductivity, thus it can be neglected in the thermal model topology. Thermal resistance in each layer remains constant under layout variation because the trace layer is the only layer in which material is either added or removed. However, the set of spread resistances $R_{sp,n}$ which exist between the die and the trace change significantly when die positions and trace shapes vary. The spread resistance between trace and isolation $R_{sp,trace}$ varies only with respect to trace shape not die position. Therefore, a method to predict these spread resistances under varying layouts is the key to fast thermal modeling.

2.1.2 Thermal Model Topology Verification

In order to verify the thermal model topology, thermal resistance and capacitance values need to be determined. The average temperature of each surface in an MCPM under steady-state and transient conditions is extracted from ANSYS. As an illustrative example of the thermal parameter extraction process, an MCPM provided by Arkansas Power Electronics International Inc. (APEI) is analyzed [20]. Table 2.2 shows the geometric sizes and material properties of each layer for the APEI power module. To begin the extraction process, a model with three die as shown in Fig. 2.4 sitting on a block of non-etched trace is built and solved with sufficient mesh in ANSYS. The temperature distribution across the surface of the module is shown in Fig. 2.4, where red and blue represent the highest and lowest temperatures, respectively.

Table 2.2: Geometric Sizes and Material Properties of Layers

Material (layer)	Length (mm)	Width (mm)	Thickness (mm)	Thermal Conductivity $(W/mm.k)$	Specific Heat $(J/g.k)$	Density $(g.mm^3)$
Si (die)	4.8	2.4	0.35	0.153	0.703	0.00234
Al I (DBA)	24.00	31.2	0.41	0.24	0.92	0.0027
AlN (DBA)	83.82	54.61	0.64	0.02	0.734	0.00326
Al II (DBA)	83.82	54.61	0.41	0.24	0.92	0.0027
Solder	83.82	54.61	0.1	0.065	0.213	0.00728
Cu (base plate)	91.44	74.93	3.81	0.386	0.381	0.00395

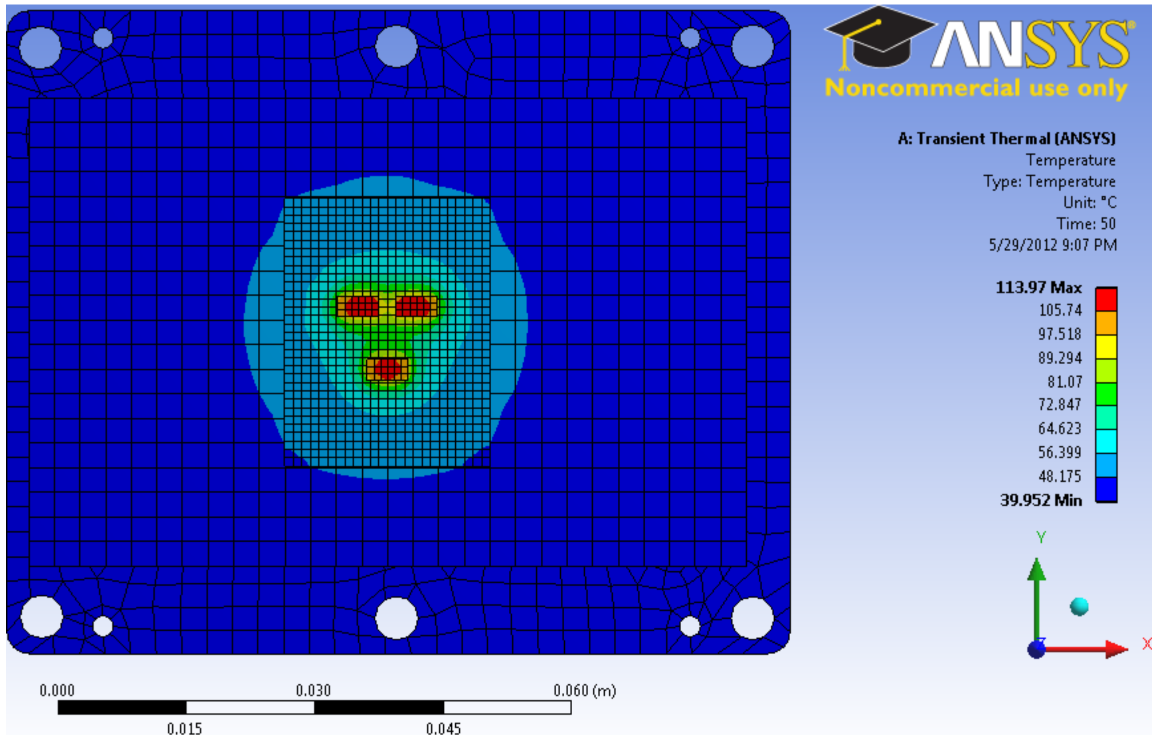


Figure 2.4: Temperature distribution in an MCPM

The steady-state temperature data, averaged over area, is extracted from each surface in the MCPM, and Eq. (2.1) is applied to determine thermal resistance of each layer. The extraction algorithm is then developed to determine thermal capacitance as follows. In ANSYS, transient data is provided for each node, such as the node with the highest temperature and the node with the lowest temperature of a surface. To estimate the average transient temperature for a surface which consists of many nodes, the temperature data from each node is required. Thus, the average transient temperature of a surface is determined by taking the average of all the node values. However, this is very computationally expensive because there are thousands of nodes per surface. To reduce the computational cost, Eq. (2.2) is developed to calculate the average transient temperature for a surface $T_{Ave_tran\,i}(t)$ based on only the transient data for the highest and lowest temperature nodes of a surface.

$$T_{Ave_tran\,i}(t) = T_{Max_\,tran\,i}(t) - c\left(T_{Max_tran\,i}(t) - T_{Min_tran\,i}(t)\right) \tag{2.2}$$

where $T_{Max_tran\,i}(t)$ is the transient temperature for the node with the highest temperature of the surface, and $T_{Min_tran\,i}(t)$ is the transient temperature for the node with the lowest temperature of the surface, and c is the characterization coefficient determined by the steady-state temperature. In Fig. 2.5, the average transient temperature of a surface over time (red) always falls somewhere in between the transient highest temperature (blue) and lowest temperature (green). The characterization coefficient c is used to determine the position of the average transient temperature with respect to the highest and lowest temperatures. To determine c, the highest temperature $T_{Max\,i}(\infty)$, the lowest temperature $T_{Min\,i}(\infty)$, and the average temperature $T_{avg\,i}(\infty)$ of the surface under steady-state conditions ($t = \infty$) are extracted. Then, c is formed by Eq. (2.3):

$$c = \frac{T_{Max\,i}(\infty) - T_{avg\,i}(\infty)}{T_{Max\,i}(\infty) - T_{Min\,i}(\infty)}\,. \tag{2.3}$$

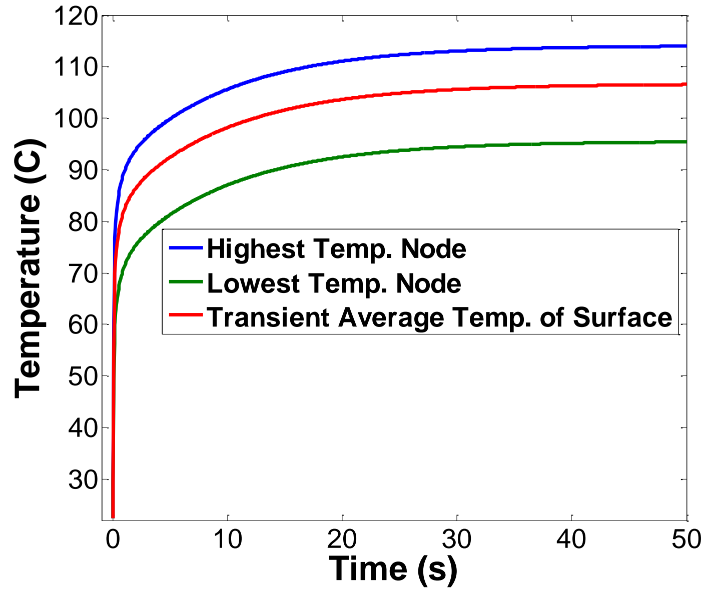


Figure 2.5: Transient average temperature in a surface

Since each layer is constructed with a resistance and capacitance as shown in Fig. 2.6, the heat flow through a thermal capacitance $P_{Ci}(t)$ is found by applying KCL to the attached node. Thus, it is determined by Eq. (2.3), where $P_{R(i-1)}(t)$ is the heat flow through thermal resistance of the previous layer, and $P_{Ri}(t)$ is the heat flow through thermal resistance of current layer. The heat flow $P_{Ri}(t)$ and $P_{R(i-1)}(t)$ are determined by Eq. (2.4) which is the electrical equivalent of Ohm's Law.

$$P_{Ci}(t) = P_{R(i-1)}(t) - P_{Ri}(t) \tag{2.3}$$

$$P_{Ri}(t) = \frac{T_{Ave_tran\,i}(t) - T_{Ave_tran\,i+1}(t)}{R_i} \tag{2.4}$$

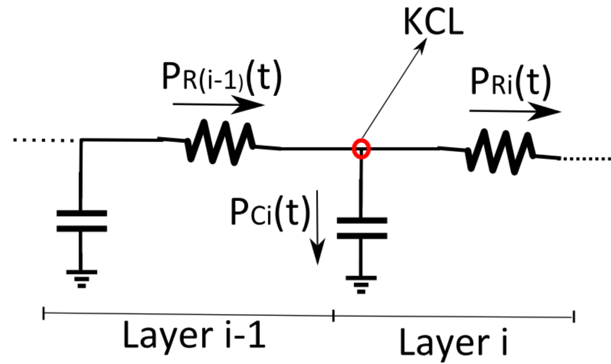


Figure 2.6: Heat flow through thermal capacitance

By making an analogy to an electrical circuit, where $i = C\frac{dv}{dt}$, the equation to determine the thermal capacitance is formed in Eq. (2.5), where $T_{Ave_tran\,i}(t)$ is determined by Eq. (2.2), $P_{Ci}(t)$ is determined by Eq. (2.3).

$$C_i = \frac{P_{Ci}(t)}{dT_{Ave_tran\,i}(t)/dt} \tag{2.5}$$

Applying the thermal extraction algorithms developed above, each thermal parameter in the thermal model topology as shown in Fig. 2.3 is determined and the result is shown in Table 2.3.

Table 2.3: Thermal Parameters Values in Thermal Model Topology

R	**Rdie1**	**Rsp1**	**Rdie2**	**Rsp2**	**Rdie3**	**Rsp3**	**Rtrace**	**Rsp,trace**	**Rsub-layers**
k/W	0.2250	0.9736	0.2256	0.9757	0.2258	0.8991	0.0022	0.3140	0.2015
C	**Cdie1**	**Csp1**	**Cdie2**	**Csp2**	**Cdie3**	**Csp3**	**Ctrace**	**Csp,trace**	**Csub-layers**
Ws/k	0.0029	0.1000	0.0029	0.1000	0.0029	0.1000	0.3813	0.1047	51.6678

The thermal model topology is constructed in the Saber circuit simulator for verification purposes. All die are turned on simultaneously because the thermal model topology doesn't include thermal coupling coefficients between die. Instead, the thermal model topology aggregates the thermal coupling effects into the spread resistances of each die by applying Eq. (2.1). The average temperature of a die's bottom surface and trace's top surface along with heat flow from a die are used to compute each die's spread resistance. This aggregation process only works as long as all die in the thermal topology emit the same heat flow so that as a group they all experience the same relative temperatures as found during the characterization process. For example, if a system was characterized with 40 W of dissipation from each die, correct temperatures could be found when all die are operating at 20 W, but not if some die were at 10 W, 15 W or 0 W (off). This is due to modeling the thermal system linearly without coupling coefficients. It is also possible that other devices in a layout may dissipate more or less heat with respect to others in the system. These die must have their heat flow decreased or increased in linear proportion to the heat flows of die characterized at different heat flows in order to expect correct temperatures from the thermal network.

In order to consider thermal coupling coefficients in the network, more advanced multi-port modeling techniques, such as a using a thermal impedance matrix, would be required [21]. While this might appear to be a big limitation, SiC power modules use paralleled die to increase current flow and thus the die share the same heat flow making this is an applicable assumption. The steady-state and transient data of temperature in each layer from Saber match the data from

ANSYS with high accuracy thus confirming the topology. Fig. 2.7 shows the transient temperature comparison between Saber and ANSYS of the die in the APEI power module.

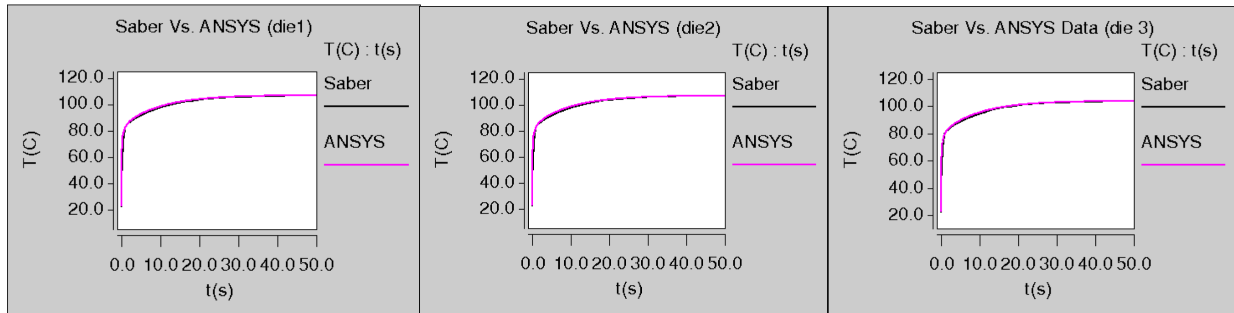


Figure 2.7: Thermal model topology verification

2.2 Thermal Model Characterization

The thermal modeling algorithm requires temperature and heat flux distribution data in order to determine spread resistances and thus accurate module temperatures. In this thesis, a rectangular contour representation of temperature and heat flux is used because of two reasons. First, rectangular contours ease the model's computational complexity by transforming large amounts of data points represented by a two dimensional array into contours with values stored in a one dimensional array. Second, the rectangular contours require much less computation compared to other polygonal contours, but they still provide sufficient data for modeling temperature and heat flux distributions. Later on, the thermal modeling algorithm uses these contour based representations of temperature and heat flux distributions to approximate spread resistances under layout variation. This section is dedicated to the conversion of these distributions into contour format.

The temperature and heat flux distributions on the top surface of the isolation layer for a single die on non-etched trace shown in Fig. 2.8(a) is extracted from ANSYS and saved in a regular grid format. As shown in Fig. 2.8(b), the top of the isolation layer is selected based on the

principle that the temperature distribution can be directly mapped from the top surface of isolation layer to the top surface of trace and die bottom on a point to point basis. The temperature difference between points directly above and below each other is relatively small (~0.2 °C).

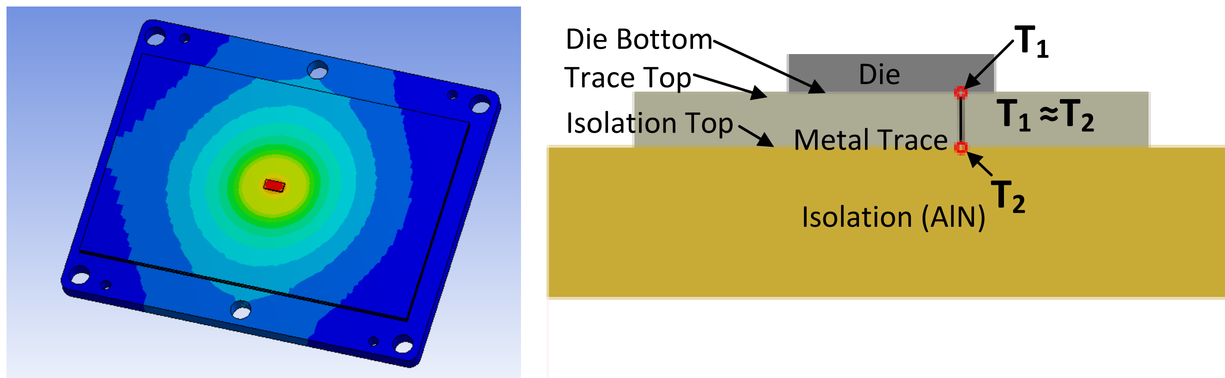


Figure 2.8(a): Single die on a non-etched trace; (b): Temperature point to point mapping

To form contours for both temperature and heat flux distributions, the same process is applied. First, two slices of data are taken from the X and Y axes. Second, a set of uniformly spaced points are found along the upper half of the Y axis, and are mapped to half of the X axis as shown in Fig. 2.9. A derivative based spacing of points was implemented where the density of points is proportional to the slope of the curve. However, this yields poor performance in the optimization process because the trade-off region resides along the lower temperature regions of the curve which coincidentally have the lowest slope. A simple uniform spacing of points along the axis gives more points in the trade-off region, and provides sufficient accuracy to the optimization results. A third choice would be to allocate the most points in the best trade-off regions of the curve. This is a subjective measure though, and could only be obtained after post-processing the optimization results.

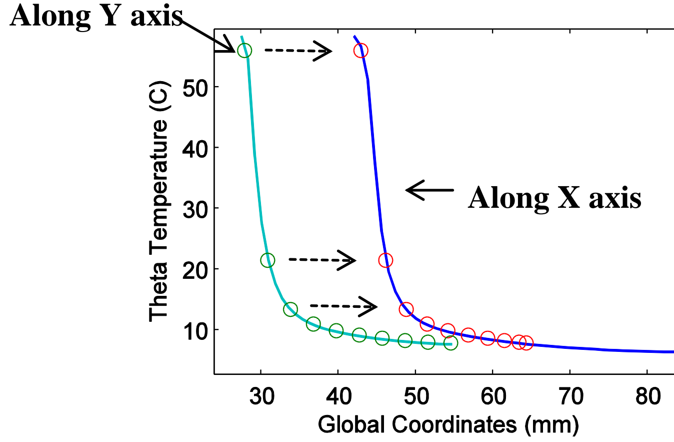


Figure 2.9: Mapping points from Y-axis to X-axis

Next, each X-Y pair of points (red and green) is used to form a rectangle which is symmetric about the module center as shown in Fig 2.10(a). A set of rectangular contours S_n is formed from R_n by removing the smaller rectangle above from the larger rectangle below, except for the first contour S_0 which is equivalent to R_0:

$$S_n = R_n \backslash R_{n-1} \tag{2.6}$$

where \ represents the set theoretic difference between larger and smaller rectangular regions. A set theoretic difference can be visualized by a Venn diagram. The difference operation on a region A and region B would take place by removing the shared middle region between A and B. The magnitude of each contour is determined by numerical integration over the underlying distribution. A representation of the processed contours is shown in Fig. 2.10(b).

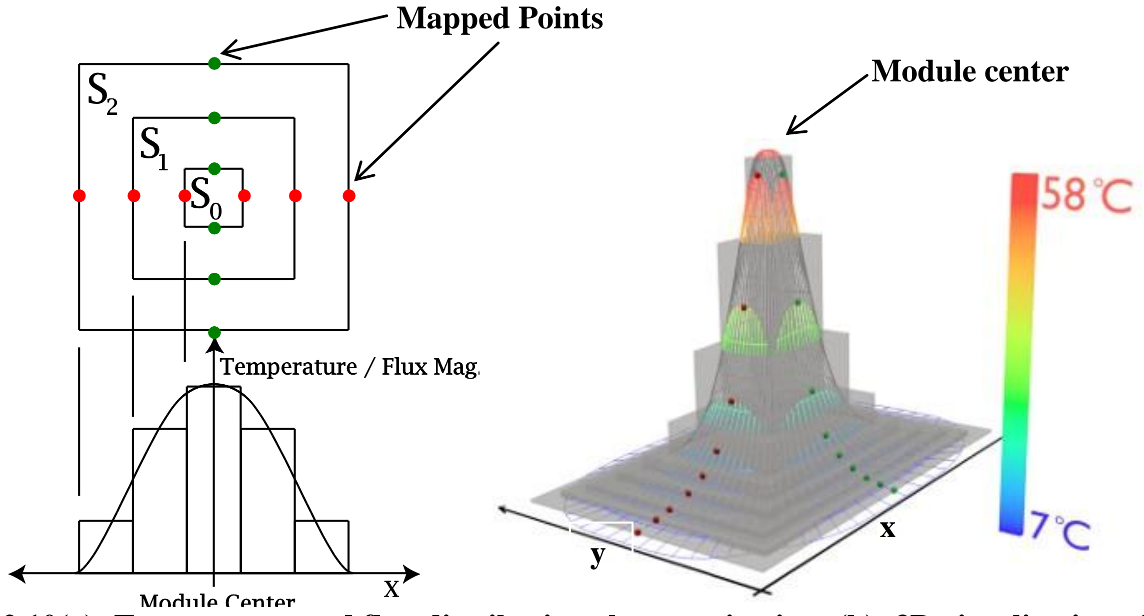


Figure 2.10(a): Temperature and flux distribution characterization; (b): 3D visualization of rectangular contours

In order to place multiple temperature distributions in superposition, the ambient temperature needs to be subtracted out from the distribution:

$$\theta(x, y, z = Z_{isolation}) = T(x, y, z = Z_{isolation}) - T_{amb} \quad (2.7)$$

The symbol θ represents a temperature that is referenced to the ambient temperature.

The average temperature of the metal trace and die increases as the trace shrinks because of less dissipation area. This temperature behavior is hard to predict given only the temperature and flux distribution information for the maximized trace. A trace scaling characterization process is needed to save the average temperature of the metal trace and bottom of a die as the trace area is decreased. This dataset helps keep the thermal modeling algorithm on track as trace area decreases significantly from the original characterization conditions.

2.3 Thermal Modeling Algorithm

The spread resistance of each die R_{sp_n} is highly dependent on die placement and trace layout. It is the sum of the thermal coupling resistance R_{C_n} and the edge effect resistance R_{E_n} as shown in Eq. (2.8) [22].

$$R_{sp_n} = R_{C_n} + R_{E_n} \quad (2.8)$$

The thermal coupling resistance R_{C_n} is calculated by applying superposition of a neighboring die's temperature contributions [22]. For illustration, a neighboring die with characterized temperature contours and a die with orange footprint are placed closely in Fig. 2.11. The die's temperature is affected by the neighboring die. Therefore, the temperature of the die is the sum of its original self temperature and temperature contribution from neighboring die:

$$\theta_{die_n} = \theta_{die_self} + \frac{1}{A_{die}} \sum_{i=0}^{C-1} \theta_{contrib_i} \times A_i \quad (2.9)$$

where A_{die} is the area of the footprint of die_n , A_i is the area of the intersection, $\theta_{contrib_i}$ is the average temperature value of the intersecting contour, and C is the total number of intersecting contours. θ_{die_self} is the average temperature of the die by itself (original temperature) and is found by linear interpolation of the trace scaling data based on metal trace area. R_{C_n} is finally calculated using the equation for thermal resistance:

$$R_{C_n} = \frac{\theta_{die_n} - \theta_{trace_all}}{P_0} \quad (2.10)$$

where P_0 is the heat flow from die_n and $\theta_{trace_all} = \theta_{trace} \times N$. θ_{trace} is the average temperature of the trace which is found by interpolation of the trace scaling data based on the metal trace area. N represents the number of die in the system. Basically, θ_{trace_all} is the average temperature of the trace when all other die are present and adding their temperature to the trace, thus multiplication by N.

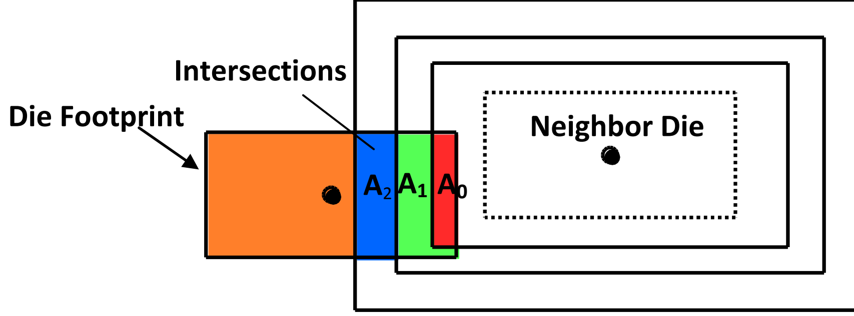


Figure 2.11: Thermal coupling intersections

The edge effect is determined by the decrease of heat conduction ability when a die is getting close to the edge of a trace [22]. A die has less effective cross-sectional area to dissipate heat as it moves from the trace center to the edge, therefore increasing its temperature. To demonstrate this, a die with its superimposed rectangular heat flux contours is placed near the edge of a trace depicted in gray (Fig. 2.12). The intersection is found between the heat flux contours and a set of trace rectangles, where this set of trace rectangles represents the trace layout in an MCPM. Then, the effective heat flow P_E is determined by the integration of each contour's heat flux in this intersection area:

$$P_E = \sum_{i=0}^{F-1} f_i \times U_i \,. \tag{2.11}$$

where f_i is the flux value of the contour and U_i is the intersection area. The edge effect resistance is then calculated by

$$R_{E,n} = \frac{\Delta\theta_{DT}}{P_E} - \frac{\Delta\theta_{DT}}{P_0} = \frac{\Delta\theta_{DT}(P_0 - P_E)}{P_0 \cdot P_E}\,. \tag{2.12}$$

where $\Delta\theta_{DT} = \theta_{die_self} - \theta_{trace}$ is from the earlier trace scaling interpolations in the thermal characterization section. The edge effect resistance $R_{E,n}$ increases because of the decrease in effective heat flow P_E. Thus, $R_{E,n}$ is formed by taking the difference from the original heat flow P_0 as shown in Eq. (2.12). To further illustrate, when the effective heat flow P_E is equal to the

original heat flow P_0 the edge effect resistance is reduced to zero thus contributing no extra resistance to the network.

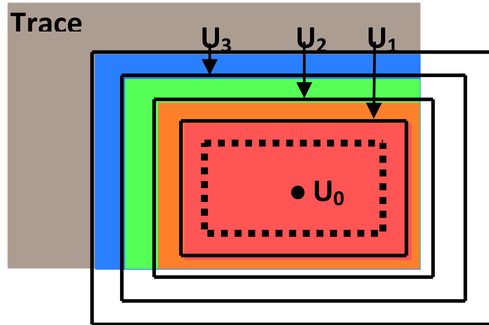


Figure 2.12: Edge effect intersections

The trace to isolation spread resistance $R_{sp,trace}$ is computed by $\frac{\theta_{trace} - \theta_{isolation}}{P_0}$. $\theta_{isolation}$ is found during the characterization process and is simply the average temperature of the isolation layer at its top surface for a single die. $\theta_{isolation}$ does not change significantly with dramatic changes in die position and trace shape and size, so a single average temperature value recorded from the characterization is sufficient. θ_{trace} is found via interpolation of the trace scaling data as mentioned earlier.

With all the thermal resistances determined by the algorithm described in previous sections, a thermal resistance matrix then is derived from the thermal model topology. This matrix and a vector of heat flows from each die in the network are used to solve for the average die temperatures.

2.4 Thermal Model Verification

To test the model's accuracy, the die temperatures from the model are compared with die temperatures from ANSYS under varying die locations and trace shapes. Fig. 2.13 shows an experiment that tests both the edge and thermal coupling effects from the model. In the test set up, die 1 is stationary while die 2 is moving from the trace edge towards the center. Fig. 2.14 is

die 2's temperature under varying distance, *d*, from the trace edge. The model predicts high temperature when die 2 is close to the edge (due to the edge effect) or close to the other die (due to thermal coupling). The temperature from the model has good agreement with the temperature from ANSYS with a maximum error of 6%.

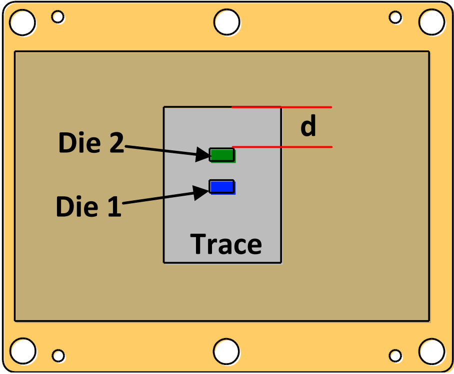


Figure 2.13: Edge and coupling effect experiment

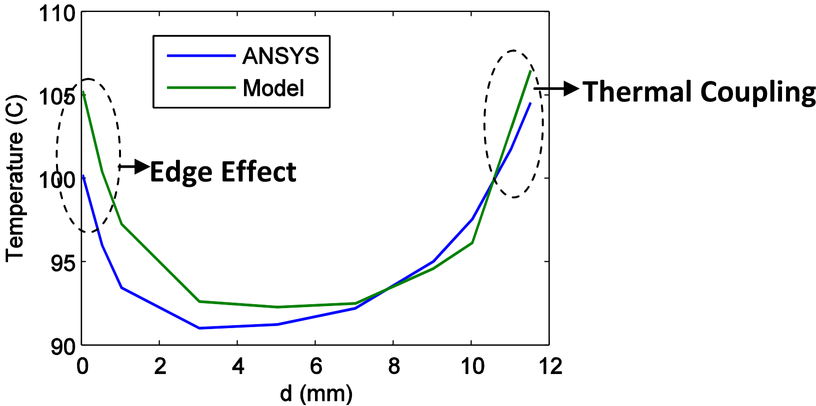


Figure 2.14: Model vs. ANSYS temperature of die 2

Fig. 2.15 shows an experiment that tests the model's accuracy with an increasing quantity of die in a system. In Fig. 2.16, the temperatures of Die 0 from the model and ANSYS are compared for an increasing amount of die corresponding to the experimental setup in Fig. 2.15. The model tracks the increase of temperature well and shows a maximum error of 2.9% in the experiment.

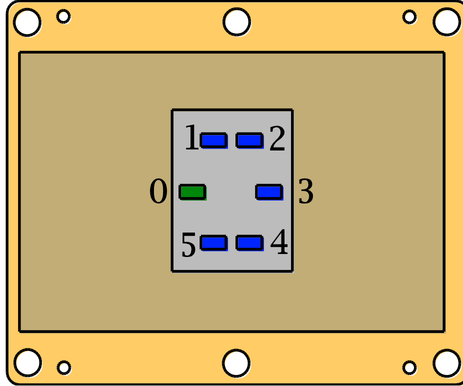


Figure 2.15: Die quantity experimental setup

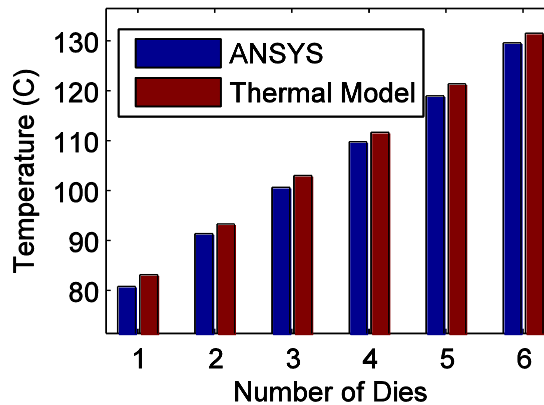


Figure 2.16: Average top surface temperature of die 0 with increasing die quantity

The thermal model, implemented in Python, is found to run about 10,000 times faster than the ANSYS FEA model. Both the thermal model and ANSYS were simulated on an Intel Core i7-870 clocked at 2.93 GHz per core. Table 2.3 shows the actual time comparison between the model and ANSYS when there are 1 die and 6 die in the system. The asymptotic computational complexity of the thermal modeling algorithm is $O(n^2)$ with n being the quantity of die. This is due to the evaluation of each die with every other die when computing thermal coupling. In conclusion, the thermal model is within the accuracy needed for layout optimization and much faster than ANSYS. This provides a time saving advantage in thermal analysis allowing many different layout configurations to be evaluated.

Table 2.4: Time Comparison (Fast Model vs. ANSYS)

	1 Die	6 Die
ANSYS	13.13 s	18.00 s
Model	116 μs	1794 μs

Chapter 3 Electrical Parasitic Modeling for MCPMs

Electrical parasitic resistance, inductance, and capacitance exists in the traces, the leads, and the bond wires of MCPMs. Fig. 3.1(a) shows a layout of an MCPM with one switching position where multiple devices are paralleled. For a half bridge topology, the layout in the low side switching position is almost symmetrical to the layout in the high side switching position. In this thesis, it is assumed the layout of low side switching position is symmetrical to the high side switching position. Thus, the electrical parasitics for only half of the layout, one switching position, are considered.

In Fig. 3.1(a), the drain, source, and gate traces are formed with rectangular bars, and the devices are connected to the traces through bond wires. Fig. 3.1(b) is the lumped electrical parasitic topology corresponding to the layout shown in Fig. 3.1(a). In Fig. 3.1(b), the electrical parasitics existing in the traces and the bond wires are in lumped form. The parasitics associated with the leads are not included in the topology because the leads do not change geometry while the layout is varied during the optimization process. As shown in Fig. 3.1(b), the major parasitics that need to be considered are trace inductance and resistance, bond wires inductance and resistance, and trace to ground plane capacitance. The capacitance that exists between traces is very small so it is neglected in electrical parasitic modeling process. Also, the capacitance associated with the bond wires is negligible.

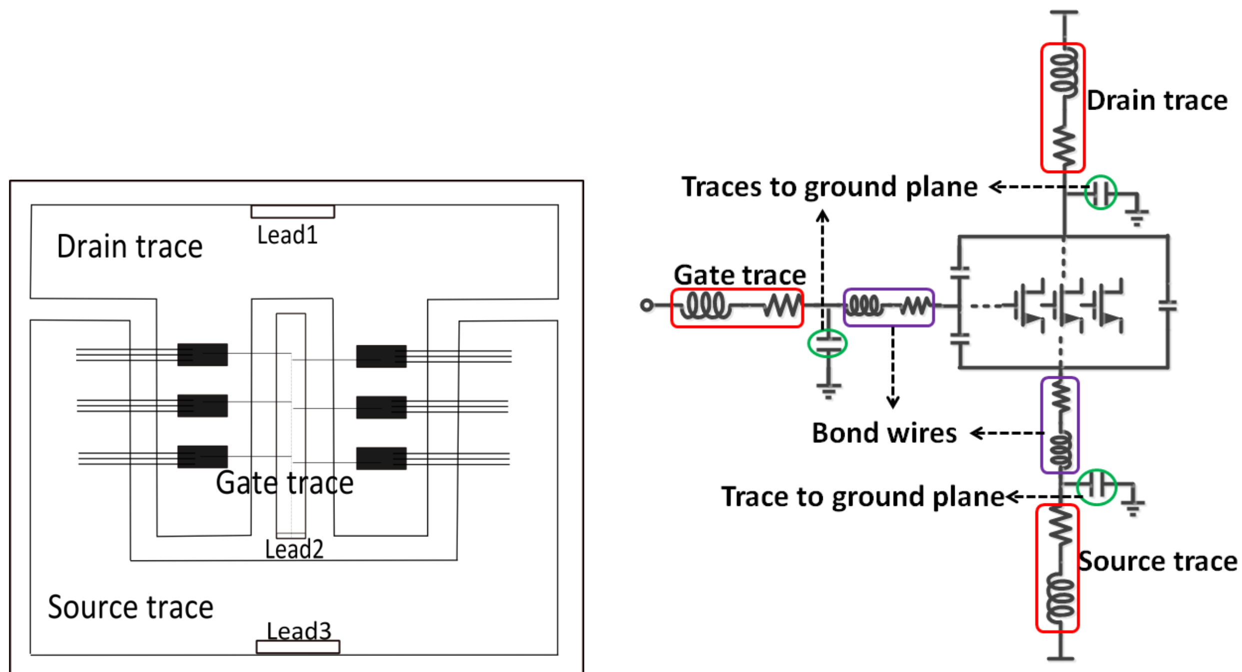


Figure 3.1(a): Layout of one switching position; (b): Lumped electrical parasitic topology

To achieve optimal thermal and electrical behavior of an MCPM, the layout needs to be varied to find an optimal design with the lowest temperature and the least electrical parasitics. The layout variations include the geometry sizes and traces, bond wires material properties, as well as the die locations. Table 3.1 lists all variation parameters associated with traces, bond wires, and die, where h is the separation between traces and the ground plane, ϵ_r is the permittivity of the isolation material, and d is the distance between bond wires. In this thesis, the variation parameters considered for layout optimization are trace width and length, die location, and bond wire length. The trace thickness, layer material properties, and other parameters are set to be constant. Accurate estimation of electrical parasitics under varying layouts is the key in the optimization process.

Table 3.1: The Layout Variation Parameters

	Geometry Sizes				Material Properties		
Trace (Substrate)	width (w)	length (l)	thickness (t)	separation (h)	conductivity (σ)	permeability (μ_r)	permittivity (ϵ_r)
Bond Wires	radius (r)	length (l)	distance (d)	--	conductivity (σ)	--	--
Die	locations				--		

In this chapter, a background study is first given to help understand the different effects that are essential to electrical parasitic modeling for MCPMs. Then, the electrical parasitic resistance, inductance, and capacitance models for the traces are developed and verified with Ansoft Q3D. The electrical parasitic resistance and inductance models of bond wires in parallel are described. Last, an extraction algorithm to determine parasitics in a single module current path is developed and verified by comparison to Ansoft Q3D.

3.1 Background

As AC current flows through a given layout, there are multiple effects contributing to the variation of electrical parasitic values. The skin effect redistributes the current through the conductor causing changes to the effective conduction area, thus changing the resistance [23]. The ground plane effect reduces inductance significantly [24]. Also, the proximity effect, caused by magnetic field interaction between adjacent current paths, leads to uneven current distribution in conductors, which is another factor causing variation of resistance [23]. Mutual inductance between conducting traces and parallel bond wires contribute to their total inductance. These effects are the influential factors on electrical parasitics in MCPMs. Thus, they are first studied independently, and then taken into account during the modeling process.

3.1.1 Frequency Dependent Resistance and Inductance

Under DC operating conditions, current is uniformly distributed in rectangular trace. Under AC conditions, the current tends to concentrate at the surface of the trace as frequency increases (Fig. 3.2(a)). For a trace in an MCPM (Fig. 3.2(b)), the current tends to be concentrated at the bottom surface of the trace because the electric fields between the trace and the ground plane attract charge to the bottom surface [12].

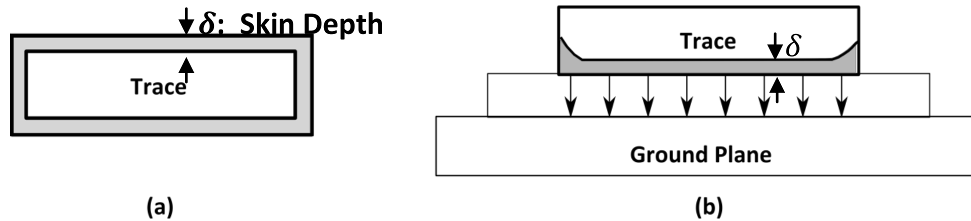


Figure 3.2: Current conduction under AC conditions

The resistance and inductance of a single rectangular trace in an MCPM change with respect to frequency. The resistance increases with the square root of frequency at high frequency as shown in Fig. 3.3(a). On the other hand, inductance converges to a constant value at high frequency as shown in Fig. 3.3(b). The change of inductance in a frequency range of 100 kHz to 1 MHz is less than 2%. This is within a typical switching frequency range (20 kHz and up) for SiC power electronics. Therefore, it is assumed that the inductance is independent of frequency for the following MCPM inductance models.

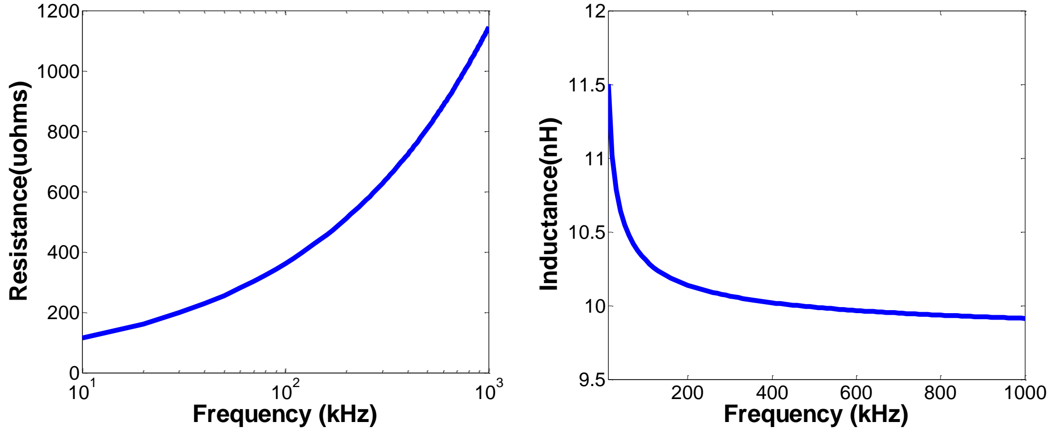


Figure 3.3(a): Frequency dependent resistance; (b): Frequency dependent inductance

The skin depth of the trace in an MCPM (Fig. 3.2) is determined by Eq. (3.1), where μ_0 is permeability, σ is conductivity, and f is frequency.

$$\delta = \frac{1}{\sqrt{\pi \mu_0 \sigma f}} \tag{3.1}$$

Then, the equation to determine AC resistance is shown in Eq. (3.2) [12].

$$R_{ac} = \frac{l}{\sigma A} = \frac{l}{\sigma w \delta} = \frac{l}{w}\sqrt{\frac{\pi \mu_0 f}{\sigma}} \tag{3.2}$$

This approximation assumes that all the current flows through the skin depth portion of the conductor. However, it is estimated only 63% of current goes through the skin depth portion [12]. Thus, this model is inaccurate in predicting resistance at high frequency. A better resistance model of traces is developed by applying techniques used in micro-strip transmission line structures, and is further described in the resistance modeling section.

3.1.2 Ground Plane Effect

In printed circuits boards (PCBs), the ground plane is used to dissipate heat, reduce stray inductance, and provide signal shielding [26]. One of the major contributions of the ground plane

is to reduce trace inductance in PCBs [24]. This phenomenon is called the ground plane effect and has been thoroughly studied in micro-strip structures. Some of these results can be applied to electrical parasitic modeling of traces in MCPMs because there are some similarities between MCPMs and micro-strip structures. Fig. 3.4 illustrates that an MCPM is analogous to a micro-strip structure. The rectangular trace in an MCPM is analogous to a signal conductor in a micro-strip structure. The isolation layer of the substrate is analogous to the dielectric layer. The second metal in substrate together with the base plate is analogous to the ground plane. However, there are two distinguishing features between MCPMs and micro-strip structures. First, there is a finite ground plane in an MCPM, while the micro-strip structure has an infinite and ideal ground plane. Second, the traces in micro-strips are very long and thin compared to the traces in MCPMs. These differences lead to the sacrifice of accuracy in inductance modeling of the traces in MCPMs.

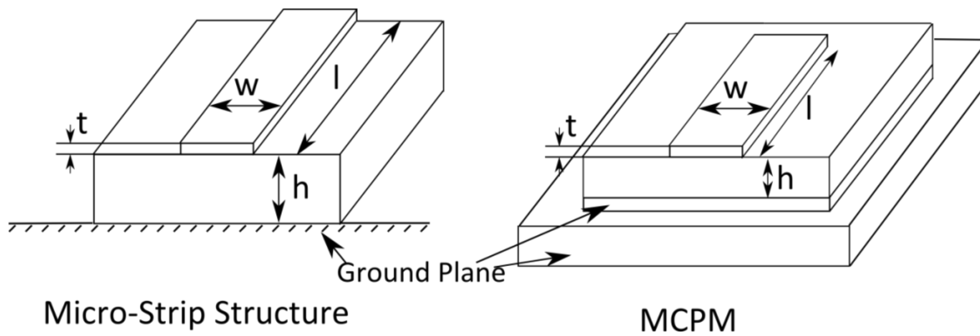


Figure 3.4: MCPM and Micro-Strip structure comparison

As shown in Fig. 3.5, the inductance of a rectangular trace is reduced significantly due to the ground plane effect. This phenomenon is illustrated in Fig. 3.6, where two filaments of current, one from the trace and the other one from the return plane right below the trace, form a loop. [12].

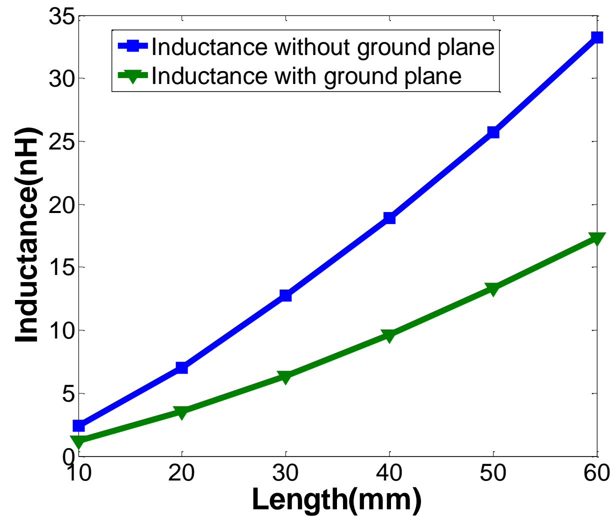


Figure 3.5: Inductance reduction with ground plane effect

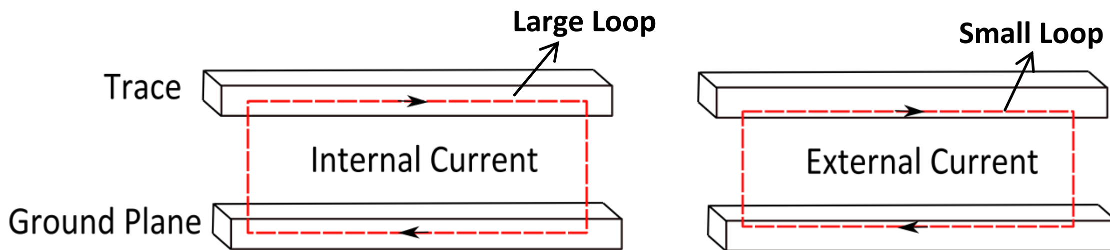


Figure 3.6: Filament of current interacting with the ground plane

Since the trace and the ground plane carry currents in opposite directions, the magnetic flux linkage around the closer parts of the conductors decreases while it increases in the farther parts [23]. This is the reason why the current tends to concentrate in the bottom surface of the trace and the top surface of the ground plane. As shown in Fig. 3.6, there is primarily internal current at low frequencies and external current at high frequencies. As the external current path becomes the dominant conduction mode, the inductance loop formed by the trace and the ground plane shrinks, which results in a smaller path inductance. With an infinite ground plane, current is fully concentrated at the plane's top surface where the smallest inductance loop is formed, thus having the least inductance [12]. Another explanation of reduced inductance is that the ground

plane generates a more confined electromagnetic field that shields signals which decreases inductance [24].

3.1.3 Self-Partial and Mutual-Partial Inductances

The inductance associated with a conductor, such as a trace or a bond wire, includes the self-partial inductance and the mutual-partial inductance, where self-partial inductance is associated with a conductor when there are no other currents flowing in surrounding conductors, and the mutual-partial inductance is the inductance contributing from other currents flowing in adjacent conductors [27]. Fig. 3.7 illustrates that the total inductance of a conductor is the sum of the self-partial inductance L_p and the mutual-partial inductances M_{ji} contributing from other current carrying conductors. If one of the other conductors has an opposite current direction, the mutual-partial inductance contributing from this conductor is negative. On the other hand, the mutual-partial inductance is positive when the currents flow in the same direction.

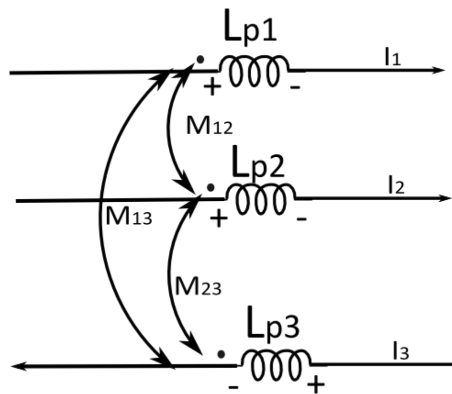


Figure 3.7: Self-partial and mutual-partial inductance

For the MCPM layout in Fig. 3.8, currents in the traces, labeled with different colors, flow in the same direction, so the contribution of mutual inductances between the traces are positive. The self-partial inductances of the traces are labeled L_{p1} to L_{p4}, and the mutual-partial

inductance between the traces are M_{ji}, where the mutual-partial inductance between trace 1 and trace 4 (M_{14}) is negligible because of large separation. Mutual-partial inductances also exist between bond wires (circled in red) which will be discussed in section 3.3.2.

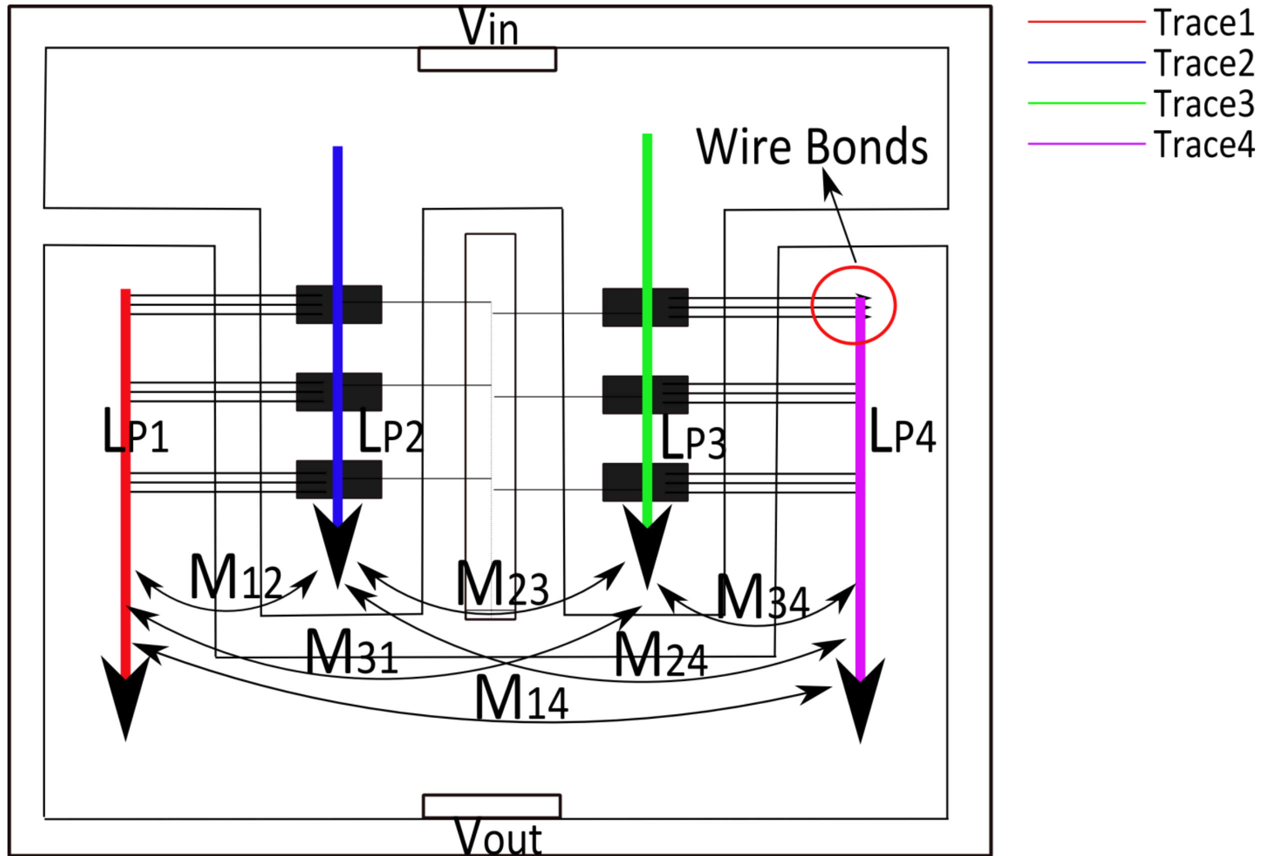


Figure 3.8: Current paths in traces

To determine the mutual inductance between two parallel traces, an exact closed form formula with a three-fold integration is developed in [28]. It calculates the mutual inductance between two parallel rectangular traces that are spaced in any relative position. In an MCPM, rectangular traces in the layout are in parallel and always reside in the same layer level (metal trace layer). Thus, the mutual inductance model developed in [28] can be applied to determine mutual inductances of traces in MCPMs.

In this thesis, the mutual inductance between the traces is not implemented because the self-partial inductance gives accurate trending prediction of the total inductance in varying layouts. Also, since only half of the layout (Fig. 3.8) is needed in the optimization process, there are only two current carrying traces in the half layout. The mutual inductance between them is relatively small compared to the self-partial inductance, thus can be ignored. However, the mutual inductance needs to be included in the future in order to consider many current carrying traces.

3.2 Electrical Parasitic Modeling of Traces

A resistance model of a trace with finite thickness is developed for micro-strip structures, and is applied to determine the resistance of traces in MCPMs. The inductance of a micro-strip can also be derived under the assumption that it is a perfect conductor carrying a transverse electromagnetic mode (TEM) wave. It is assumed that the micro-strip has an infinite and ideal ground plane for the inductance method. Since it is necessary to calculate the inductance of traces in MCPMs with a finite ground plane, an average model is formed by combining inductance derived for micro-strips and inductance of a rectangular trace with no ground plane effect (completely isolated). Finally, to determine an accurate capacitance model of traces, fringe capacitance is taken into account.

3.2.1 Trace Resistance Model and Verification

3.2.1.1 Trace Resistance Model

Unlike the trace inductance which is reduced significantly by the ground plane effect, the AC resistance is not changed much by the ground plane effect. In Fig. 3.9(b), AC resistance of a trace with the ground plane (Fig. 3.9(a)) increased by 8% as compared to without a ground plane. However, AC resistance stays about the same as the size of the ground plane varies. Since the

size of the ground plane doesn't change the AC resistance significantly the assumption that an MCPM is very similar to a micro-strip structure with a finite thickness conductor is valid when only considering AC resistance. Thus, the equations to calculate resistance for micro-strip structures with finite thickness conductors can be properly applied to estimate the AC resistance for trace in an MCPM .

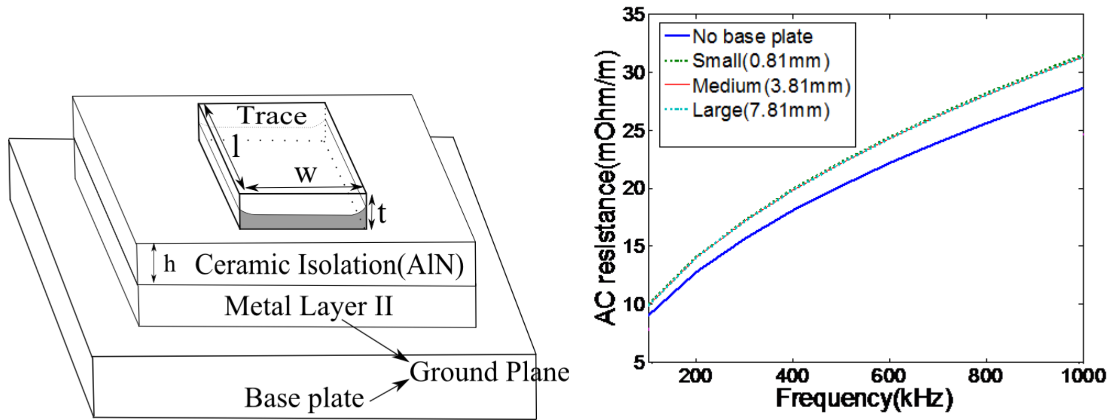


Figure 3.9(a): Rectangular trace in an MCPM; (b): AC resistance with ground plane effect

To obtain an accurate analytical formula for AC resistance of traces with finite thickness in micro-strip structures, conformal mapping techniques as described in [11] and [25], are applied and yield the solution:

$$R_{ac} = LR \frac{lR_0}{2\pi^2 w}\left(\pi + ln\frac{4\pi w}{t}\right). \tag{3.3}$$

where

$$R_0 = \sqrt{\frac{2\pi f \mu_0}{\sigma}} \text{ , and}$$

$$LR = 0.94 + 0.134\frac{w}{h} - 0.0062(\frac{w}{h})^2 \ .$$

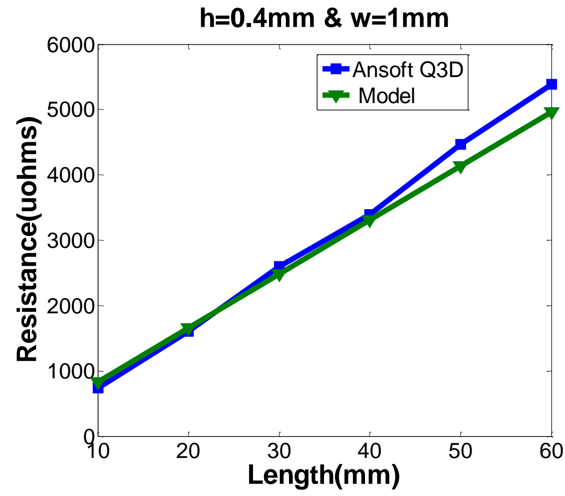
This model is applied to estimate the resistance of traces in MCPMs (Fig. 3.9(a)), where w, l, and t are the width, length and thickness of a trace, respectively, and h is the separation between a trace and the ground plane.

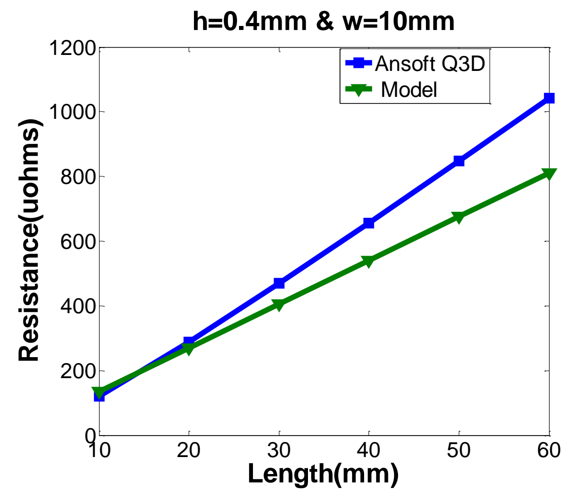
3.2.1.2 Trace Resistance Model Verification

To test the model's accuracy, an MCPM is modeled in Ansoft Q3D and frequency is swept from 100 kHz to 1 MHz. As frequency increases, the resistance values from the model correspond well with the resistance values from Ansoft Q3D. The error percent is constant over frequency because skin effect resistance increases with the square root of frequency which is captured accurately by the analytic model. As a result, the test can be run under a single high frequency (300 kHz) but still represents the error percentage of the model for all frequencies. The second copper layer with relatively small sizes is combined with the copper base plate to form the ground plane. In this test, the ground plane has dimensions of 74.93 x 91.44 mm and thickness of 3.81 mm, and the trace has a thickness of 0.41mm.

This test is set up in order to verify the model under varying separation (between trace and ground plane) and trace width and length. The separation between the trace and the ground plane is changed between 0.4 mm to 0.8 mm with increment of 0.2 mm. For each separation increment, the width of the trace is varied from 1 mm to 10 mm with increment of 3 mm. Under each pair of separation and width, the length of the trace is varied from 10 mm to 60 mm with increment of 10 mm. This results in a total of 72 data points under the variance of these three parameters.

The test results show that the model has good agreement with the results from Ansoft Q3D, where four corner cases are shown in Fig. 3.10. Fig. 3.10(a) is the resistance comparison with respect to trace length between the model and Ansoft Q3D with a 0.4 mm ground plane separation and a 1 mm trace width. The next three figures (Fig. 3.10(b-d)) show the comparison between Ansoft Q3D and the model for other corner cases of ground plane and trace width separations.


h=0.4mm & w=1mm
Resistance(uohms)
Length(mm)
Ansoft Q3D
Model
6000
5000
4000
3000
2000
1000
0
10
20
30
40
50
60


h=0.4mm & w=10mm
Resistance(uohms)
Length(mm)
Ansoft Q3D
Model
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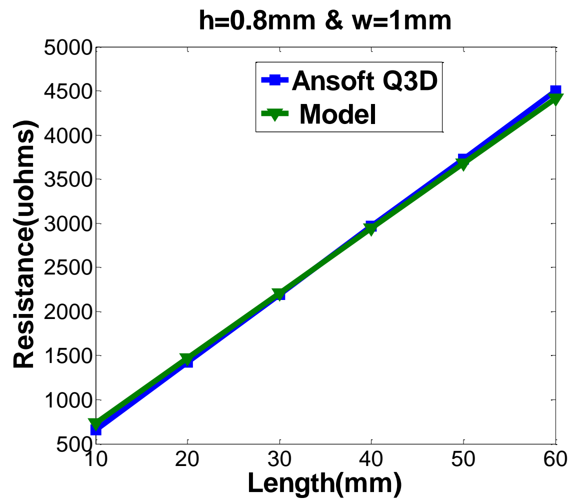
1000
800
600
400
200
0
10
20
30
40
50
60


h=0.8mm & w=1mm
Resistance(uohms)
Length(mm)
Ansoft Q3D
Model
5000
4500
4000
3500
3000
2500
2000
1500
1000
500
10
20
30
40
50
60

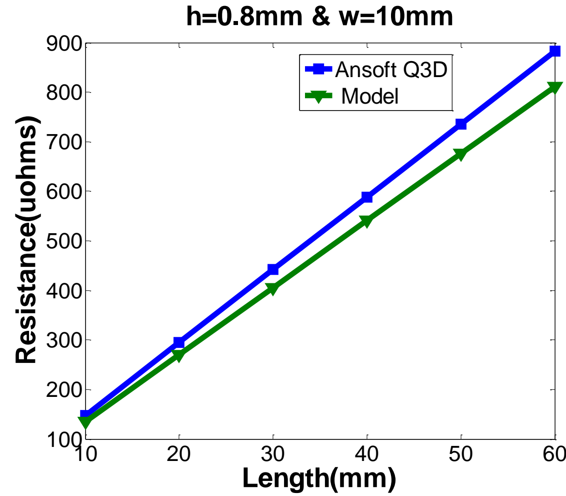


Figure 3.10(a-d): Trace resistance comparison (Model vs. Ansoft Q3D)

A maximum divergence occurs when the ground plane separation is the smallest and the trace width is the widest (Fig. 3.10(b)). Table 3.2 shows the error percentage of the model versus Ansoft Q3D. The model generally predicts less resistance as compared to Ansoft Q3D and takes on a maximum error of -22.1% for this experimental set.

Table 3.2: Resistance Model Error for Corner Cases

Error %	h=0.4mm		h=0.8mm	
l(mm)	w=1mm	w=10mm	w=1mm	w=10mm
10	11.8	12.2	11.1	-8.2
20	2.9	-6.3	3.3	-8.2
30	-4.6	-13.6	0.8	-8.2
40	-2.4	-17.7	-0.9	-8.2
50	-7.3	-20.2	-1.2	-8.2
60	-7.8	-22.1	-1.9	-8.2

3.2.2 Trace Inductance Model and Verification

3.2.2.1 Trace Inductance Model

The inductance for a trace with no ground plane effect is developed in [28]. Without the ground plane effect, there is no mutual inductance contributing to the partial-inductance of the

trace because there is no image current formed in a ground plane below the trace. The exact formula for this inductance calculation is very complicated. A simplified closed-form equation for inductance is formulated in [12]:

$$L' = \frac{\mu_0 l}{2\pi}\left[\log\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{2}{9}\left(\frac{w+t}{l}\right)\right]. \tag{3.4}$$

where μ_0 is the permeability of free space, l is the trace length, w is the trace width, and t is the trace thickness. This closed-form equation produces high accuracy under the condition that $l > w > t$.

To derive inductance with the ground plane effect, it is assumed the ground plane is infinite and a perfect conductor. Thus, the current propagates along the micro-strip transmission line without power loss. The characteristic impedance (Z_0) for the micro-strip under this condition is purely real, and is determined by Eq. (3.5), where L_0 and C_0 are the per unit length value of inductance and capacitance. The phase velocity (v_p) of a signal propagating in the micro-strip transmission line is defined in Eq. (3.6) [12].

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \tag{3.5}$$

$$v_p = \sqrt{\frac{1}{L_0 C_0}} \tag{3.6}$$

Therefore, the inductance per unit length in Eq. (3.7) is determined by combining Eq. (3.5) and Eq. (3.6).

$$L_0 = \frac{Z_0}{v_p} \tag{3.7}$$

The phase velocity can also be calculated from the dielectric properties [12]:

$$v_p = \frac{c}{\sqrt{\mu_r \epsilon_{eff}}} \; . \tag{3.8}$$

where c is the light speed in vacuum, μ_r is the relative magnetic permeability of the dielectric, and ϵ_{eff} is the effective relative permittivity of the dielectric. By substituting Eq. (3.8) into Eq. (3.7), the equation to calculate the inductance in a micro-strip structure is yielded:

$$L'' = l \frac{Z_0}{c} \sqrt{\mu_r \epsilon_{eff}} \; . \tag{3.9}$$

As seen from Eq. (3.9), an accurate estimation of characteristic impedance (Z_0) ensures an accurate inductance value. The related works [8], [9], [10] propose accurate models for characteristic impedance, but these only apply to infinitesimally thin conductors. The formulas developed in [11] account for the finite thickness of a conductor:

$$Z_0 = \sqrt{\frac{\epsilon_0 \mu_0}{\epsilon_{eff}} \frac{1}{C_a}} \; . \tag{3.10}$$

Where C_a is determined by Eq. (3.11), and the effective dielectric permittivity ϵ_{eff} is given by Eq. (3.12). The effective width of a micro-strip w_e in Eq. (3.13) is used to determine ϵ_{eff} in Eq. (3.12).

$$C_a = \epsilon_0 \left(\frac{w_e}{h} + 1.393 + 0.667 \ln \left(\frac{w_e}{h} + 1.444 \right) \right); \quad \frac{w_e}{h} > 1 \tag{3.11}$$

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} (1 + 12 \frac{h}{w_e})^{-1/2} - 0.217(\epsilon_r - 1) \frac{t}{\sqrt{w_e h}}; \quad \frac{w}{h} > 1 \tag{3.12}$$

$$w_e = w + 0.398t \left(1 + ln \frac{2h}{t} \right); \quad \frac{w}{h} > \frac{1}{2\pi} \tag{3.13}$$

In micro-strip structures, the ground plane is assumed to be ideal, which means the current returns through only the very top surface of the ground plane [24]. In MCPMs, the bottom metal layer of the substrate and the base plate are combined into a single ground plane which has a finite size and conductance value. When the dimensions and material conductivity of

the ground plane are varied, the image currents are affected and thus the inductance varies. Fig. 3.11 shows inductance changes under increasing sizes of the ground plane in an MCPM. The inductance of a trace decreases as the size of the ground plane increases. Thus, a trace without a ground plane yields a maximum inductance and an infinite ground plane yields a minimum inductance as can be seen in Fig. 3.11.

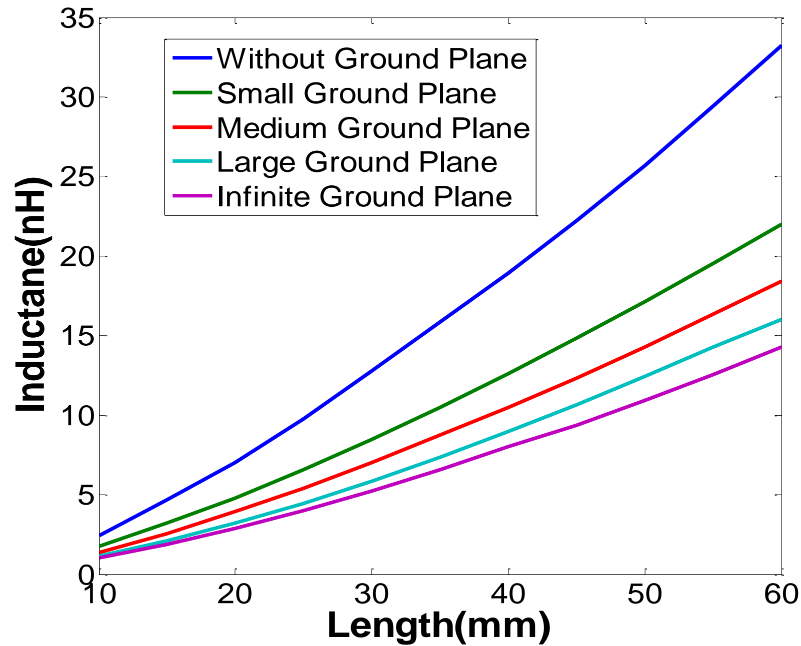


Figure 3.11: Inductance variation with increasing size of ground plane

Inductance in systems with a finite ground plane can be estimated by an analytical expression developed for micro-strip structures with an infinitesimally thin trace [29]. But this model does not work well for MCPMs because their traces have a substantial thickness. Thus, an inductance model, given by Eq. (3.14), is formed by taking the average of the inductance without the ground plane effect L', given by Eq. (3.4), and the inductance with an infinite ground plane L'', given by Eq. (3.9).

$$L = \frac{L' + L''}{2} \tag{3.14}$$

This model provides a good estimation for the inductance of traces on a finite ground plane, and its accuracy is confirmed in the verification section. The following section is an investigation of a parasitic extraction tool, FastHenry [30]. It provides another way for the layout synthesis tool to extract parasitic inductance in an MCPM. Inductance values from FastHenry and the fast model are compared to values from Ansoft Q3D in the verification section.

3.2.2.2 Trace Inductance Extraction by FastHenry

In this subsection, FastHenry, a multipole-accelerated 3-D inductance extraction program, is investigated to extract inductance in MCPMs. FastHenry applies discretization of an integral formulation to solve electromagnetic problems such that the frequency dependent resistance and inductance can be extracted from a system [31]. Electrical parasitics associated with each conductor in the system are modeled by rectangular cylinders which are defined by a start and stop point and some width and height. In order to approximate the skin effect, each rectangular cylinder is further subdivided into parallel filaments. However, FastHenry has an inaccuracy associated with the ground plane effect. The inaccuracy stems from a difference in ground plane meshing between Ansoft Q3D (mesh) and FastHenry (discretization). To remove this inaccuracy, an effective separation between the traces and the ground plane is found for FastHenry.

Fig. 3.12 illustrates the difference between the ground plane mesh in FastHenry and Ansoft Q3D. As shown in Fig. 3.12, there is only one layer of mesh in FastHenry compared to the multiple layers of mesh in Ansoft Q3D. The mesh in the ground plane determines the inductance extraction accuracy. Under the ground plane effect, the current concentrates to the

bottom surface of the trace and the top surface of the ground plane. The effective separation between the currents in the trace and the ground plane is close to h, and it is approximated to h as shown in Fig. 3.12. The effective separation determines the size of the inductance loop formed by the trace and the ground plane, thus it is important in the inductance calculation. Since Ansoft Q3D has multiple layers of mesh in the ground plane, it can calculate ground plane effect correctly. On the other hand, FastHenry with only one layer of mesh in the ground plane estimates the effective separation as $h + t'/2$ instead of h, which causes inaccurate estimation. To remove FastHenry's inaccuracy, the effective separation is set to h instead of $h + t'/2$. The result of this procedure is discussed in the following verification section.

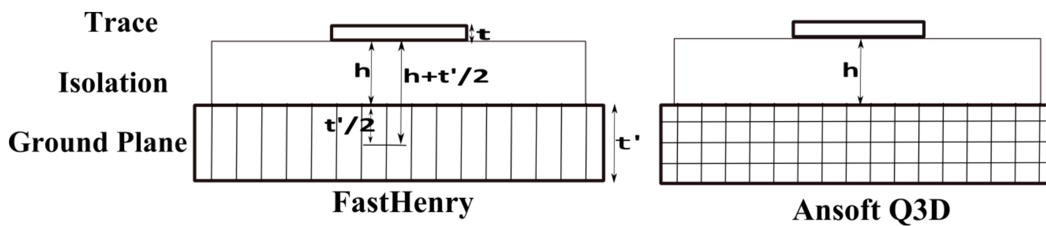


Figure 3.12: Different mesh of the ground plane

3.2.2.3 Trace Inductance Model Verification

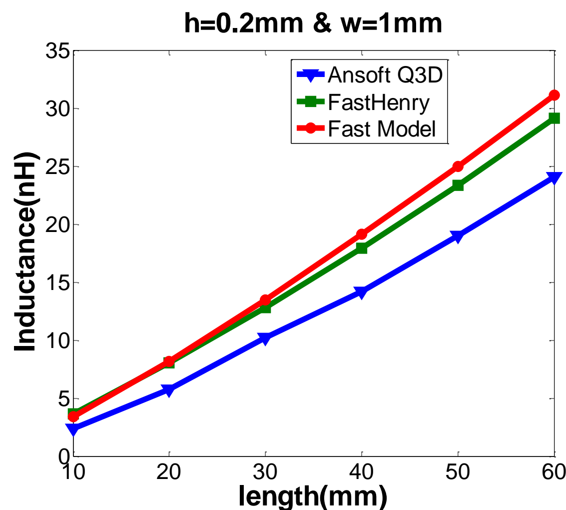
To verify the model, an equivalent MCPM is built in both FastHenry and Ansoft Q3D. Since the inductance is independent of frequency in frequency range of 100 kHz to 1MHz, the test is set to run at a frequency of 300 kHz. The ground plane has dimensions of 74.93 x 91.44 mm and thickness of 3.81mm, and the trace has thickness of 0.41 mm.

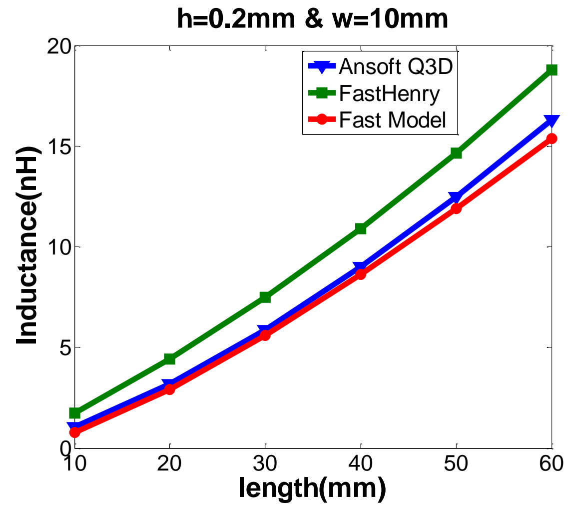
This test is set up in order to verify the model under varying separation (between trace and ground plane) and trace width and length. The ground plane separation is varied between 0.2 mm to 0.8 mm with increment of 0.2 mm. For each separation, the trace width is varied from 1

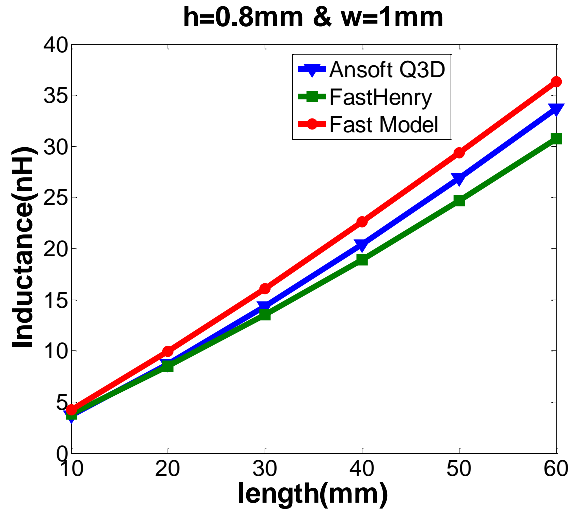
mm to 10 mm with increment of 3 mm. Under each pair of ground plane separation and trace width, trace length is varied from 10 mm to 60 mm with increment of 10 mm.

Inductances given by FastHenry and the model are both compared with Ansoft Q3D, and four corner tests are shown in Fig. 3.13 with each figure shows the inductance changing with respect to the length of the trace. Fig. 3.13(a) displays the resistance with respect to trace length between the model, FastHenry, and Ansoft Q3D with a 0.2 mm ground plane separation and a 1 mm trace width. The next three figures (Fig. 3.13(b-d)) show the comparison between the model, FastHenry, and Ansoft Q3D for other corner cases of ground plane separation and trace width.

The test results show that the model follows the same trend as compared to Ansoft Q3D. The model is generally accurate with the error percentages shown in Table 3.3, where the largest error percentage of the model occurs when the ground plane separation and trace width are both the least (Fig. 3.13(a)). As shown in Fig. 3.13(a) and (b), the model produces less error than FastHenry when the separation between the trace and the ground plane is small. FastHenry is mainly used to do the parasitic extraction of very long interconnects in VLSI. Therefore, it gives better performance as the length of the trace increases.







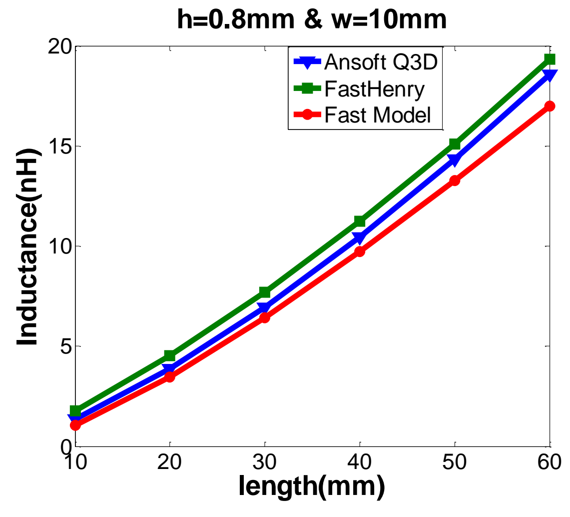


Figure 3.13(a-d): Inductance comparison between the Model, FastHenry, and Ansoft Q3D

Table 3.3: Inductance Model Error for Corner Cases

Error %	h=0.2mm				h=0.8mm			
	w=1mm		w=10mm		w=1mm		w=10mm	
L(mm)	FastHenry	Model	FastHenry	Model	FastHenry	Model	FastHenry	Model
10	54.4	44.2	63.3	-28.0	4.2	16.3	29.9	-24.0
20	39.3	41.5	38.7	-8.1	-2.2	14.0	17.7	-10.1
30	25.7	32.2	27.4	-4.7	-5.5	12.2	11.0	-7.6
40	26.4	35.0	21.3	-4.2	-7.2	10.8	7.5	-7.1
50	22.8	31.6	17.5	-4.7	-8.3	9.2	5.3	-7.6
60	20.8	29.1	15.3	-5.8	-8.8	7.8	4.1	-8.5

3.2.3 Capacitance Model and Verification

3.2.3.1 Capacitance Model

Capacitance in MCPMs exists in two forms: one is the capacitance between traces, and the capacitance between traces and the ground plane. However, the coupling capacitances that exist between traces are much smaller as compared to the capacitances between traces and the ground plane due to very small effective area between traces. Therefore, only the capacitances between traces and the ground plane are modeled.

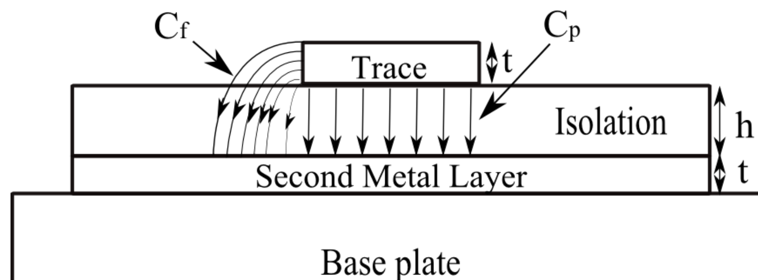


Figure 3.14: Parallel plate and fringe capacitance

Fig. 3.14 illustrates a cross-sectional view of a trace with electric fields between the trace and the second metal layer of the substrate. The total capacitance is the sum of the parallel plate

capacitance C_p and the fringe capacitance C_f. The equation to calculate the capacitance of a parallel plate is $k\epsilon_0 \frac{A}{h}$, where k is relative dielectric coefficient of the dielectric layer, ϵ_0 is the vacuum permittivity, A is the bottom area of the trace, and h is the separation between the trace and the ground plane.

When the trace is long, thus having larger area, the fringe capacitance contributes less to the total capacitance. The calculation of capacitance based on parallel plate is accurate. However, it becomes inaccurate when the trace shrinks. This is due to the increasing contribution of the fringe capacitance to the total capacitance, thus fringe capacitance C_f needs to be modeled and included in the total capacitance:

$$C = C_p + C_f. \tag{3.15}$$

In fringe capacitance modeling (Fig. 3.15), the effective area A_{eff} is determined by the sum of all the side surface's areas in Eq. (3.16). The effective separation h_{eff} falls between the h (ground plane separation) and $h + t$ (sum of ground plane separation and trace thickness). To approximate the calculation, an average between these is taken to determine the effective separation given in Eq. (3.17).

$$A_{eff} = 2wt + 2lt \tag{3.16}$$

$$h_{eff} = \frac{2h + t}{2};\ h \le h_{eff} \le h + t \tag{3.17}$$

The effective dielectric constant is formulated by averaging how much electric field lines are fringing through the passivation material and how much pass through the isolation layer (Fig. 3.15). This is achieved by using quasistatic approximations of Maxwell's equations [12]. A solution (Eq. (3.18)) is available for the effective dielectric constant k_{eff} where electric field lines fringe through air and isolation [11]. Although this solution considers field lines passing

through air instead of passivation material, it can still be used to accurately approximate fringe capacitance because of the following two reasons. First, the isolation layer is normally much thicker than the trace, which means the amount of electric field lines that go through the passivation material is relatively smaller than the amount of electric field lines that go through the isolation layer. Second, the relative dielectric constant of passivation materials (ε_r) tends to be around 2-3 which is much smaller than dielectric constant of the isolation layer, (e.g. AlN~ 9). The passivation material's dielectric constant is close to the dielectric constant of air. Therefore, there is only a small difference in the effective dielectric constant in an MCPM if the passivation material is replaced with air.

$$k_{eff} = \frac{k+1}{2} + \frac{k-1}{2}(1 + \frac{12h}{w})^{-1/2} - 0.217(k-1)\frac{t}{\sqrt{wh}} \tag{3.18}$$

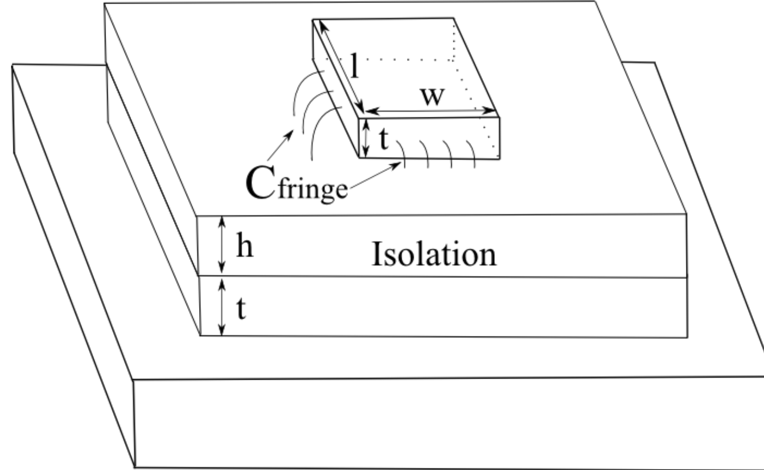


Figure 3.15: Fringe capacitance modeling

Therefore, the equation for total capacitance by taking account for the fringe capacitance is:

$$C = k\epsilon_0 \frac{wl}{h} + k_{eff}\epsilon_0 \frac{A_{eff}}{h_{eff}} \ . \tag{3.19}$$

3.2.3.2 Capacitance Model Verification

For verification, capacitance values from the model are compared to values from Ansoft Q3D. The thickness of the trace is set to 0.41 mm. The separation between the trace and the ground plane varies between 0.2 mm and 0.8 mm with an increment of 0.2 mm. For each ground plane separation, the trace width varies between 1 mm to 10 mm with an increment of 3 mm. For each pair of ground plane separation and trace width, the length of the trace varies from 10 mm to 60 mm with an increment of 10 mm.

Table 3.4 shows the error percentage of the model in corner cases as compared to Ansoft Q3D. This shows that the model provides good estimation of capacitance as the length changes from 10 mm to 60 mm. A maximum error of 26.8% occurs when the ground plane separation is the largest and the trace width is the smallest. Under most cases, the error is less than 7%, and is less than 3% when the ground plane separation is the least.

Table 3.4: Capacitance Model Error for Corner Cases

Error %	h=0.2mm				h=0.8mm			
l(mm)	w=1mm	w=4mm	w=7mm	w=10mm	w=1mm	w=4mm	w=7mm	w=10mm
10	-0.3	-2.0	-2.8	-2.3	25.5	11.1	7.5	5.7
20	-0.3	-2.0	-1.7	-1.6	26.4	9.8	6.5	5.0
30	-0.4	-2.7	-1.9	-1.5	26.8	8.6	5.6	4.4
40	-0.5	-2.0	-1.7	-2.5	26.3	9.6	5.7	3.9
50	-0.4	-2.7	-3.0	-2.4	26.2	8.0	5.4	4.1
60	-0.6	-2.5	-2.8	-2.4	25.9	9.5	5.1	3.7

3.3 Electrical Parasitic Modeling of Bond Wires

3.3.1 Bond Wire Resistance Model

At high frequencies between 100 kHz and 1 MHz, the skin effect causes current to concentrate at the surface of the bond wires and resistance increases with the square root of

frequency. The effective cross-sectional area (Fig. 3.16) of current conduction is determined by the contour area:

$$A_{eff} = \pi r^2 - \pi (r-\delta)^2 \,. \tag{3.20}$$

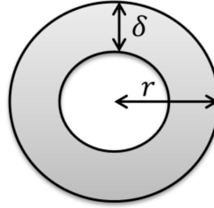


Figure 3.16: Cross-section of a bond wire

In Eq. (3.20), δ is the skin depth, and r is the bond wire radius. The equation to determine AC resistance is $l\rho/A_{eff}$, where l is the length of the bond wire and ρ is the resistivity of the wire material. This model has high accuracy when $r \gg \delta$, but becomes extremely inaccurate when $\frac{2r}{\delta} < \pi$ [32]. A model developed in [33] improves the accuracy by using a modified Lorentzian correction, and the equation derived to calculate the effective conduction area is:

$$A_{eff} = \pi\left(2\mathrm{r}\delta' - \delta'^2\right)(1 + \mathrm{c}) \tag{3.21}$$

where effective skin depth (δ') and the Lorentzian correction coefficient (c) are found using:

$$\delta' = \delta\left(1 - \exp\left(-\frac{r}{\delta}\right)\right); \;\; z = 0.62006r/\delta \;\; , \tag{3.22}$$

$$c = 0.189774/(1 + 0.27248(z^{1.82938} - z^{-0.099457})^2)^{1.0941} \tag{3.23}$$

in which δ is the skin depth and r is radius of the bond wire.

If there are multiple bond wires in parallel, the current conducting through one wire causes the current to distribute unevenly in the other wires. This phenomenon is called the proximity effect [23]. In an MCPM, currents in the bond wires generally flow in the same direction which causes currents to concentrate on the furthest edges between two adjacent bond

wires. This uneven current distribution has an influence on the AC resistance of the bond wires. However, if the separation between the bond wires is much larger than the bond wire radius, the proximity effect has much less contribution to the resistance compared to the skin effect. When bond wires get closer, the proximity effect increases the AC resistance of bond wires. The AC resistance of a bond wire under the proximity effect requires formulation of integral equations for transverse current distribution in the bond wire [34]. The formulation procedure differs with bond wire spacing, current direction, and frequency. A solution is presented to determine resistance under the proximity effect for two parallel round wires carrying equal currents in [34]. To consider multiple bond wires, further research is required. In the APEI power module, the separation between the bond wires (0.6 mm) is much larger compared to the bond wires radius (0.0635 mm to 0.254 mm), thus the proximity effect is not considered in resistance modeling of the bond wires.

3.3.2 Bond Wire Inductance Model

At high frequency between 100 kHz and 1MHz, inductance becomes relatively constant. The self-partial inductance of a round wire conductor under high frequency is given by [12]:

$$L_P = \frac{\mu_0 l}{2\pi}\left(\ln\left(\frac{2l}{r}\right) - 1\right). \tag{3.24}$$

The mutual partial inductance between two parallel round wire conductors carrying current in the same direction is determined by [12]:

$$M = \frac{\mu_0 l}{2\pi}\left(\ln\left(\frac{1}{d} + \sqrt{1 + \frac{l^2}{d^2}}\right) - \sqrt{1 + \frac{l^2}{d^2}} + \frac{d}{l}\right). \tag{3.25}$$

Where r is the radius of the wire, d is the distance between wires, and l is the effective length of the wire. In Fig. 3.17, a standard JEDEC 4-point bond wire model provided in Ansoft Q3D is used in the layout models [4]. The effective length of the bond wire is determined by:

$$l_{eff} = h1 + \frac{1}{8}d + \sqrt{(h1 + h2)^2 + (\frac{7}{8}d)^2}\,. \tag{3.26}$$

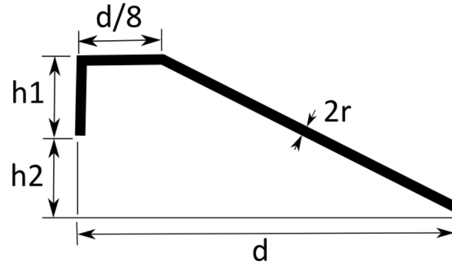


Figure 3.17: Geometric sizes of a standard JEDEC 4 point bond wire

The total inductance associated with one bond wire is the sum of the self-partial inductance and the mutual-partial inductance contributing from other bond wires. If currents in round wire conductors flow in the same direction and all wires have the same radius and length, the total inductance (L_m) of mth wire out of n bond wires in parallel is determined by:

$$L_m = L_P + \sum_{i=1}^{n} M_{mi}\,; i \neq m\ . \tag{3.27}$$

Where M_{mi} is the mutual partial inductance contributing from other bond wires. The distance between the bond wires and the ground plane is large so the ground plane effect is negligible because of its small reduction of inductance. This model predicts inductance associated with multiple bond wires accurately.

The electrical parasitics of bond wires are included in the model and the verification is described in the following sections. In MCPMs, it is favorable to use as many bond wires as possible in parallel in order to reduce parasitic resistance and inductance [35]. Therefore, the electrical parasitics associated with bond wires are much smaller than electrical parasitics

associated with traces if there are sufficient amount of bond wires paralleled in a layout. For modeling purposes, the electrical parasitics of bond wires are included in the model and the verification is described in the next sections.

3.4 Overall Electrical Parasitic Verification

3.4.1 Switching Loop Inductance

To ensure semiconductor devices work with high reliability and efficiency, parasitic resistance and inductance need to be reduced. In an electrical parasitic topology (Fig. 3.18), the switching loop inductance is the major cause of parasitic ringing in packages [36]. The parasitic ringing under fast switching frequency is even more sensitive in the switching loop compared to the gate loop [36]. Therefore, to predict an accurate inductance of the switching loop is critical. The switching loop inductance (Fig. 3.18) is the sum of the inductances in the switching loop path, including inductances of the drain trace, the source trace, and the bond wires. A similar summation applies to resistance estimation for the switching loop.

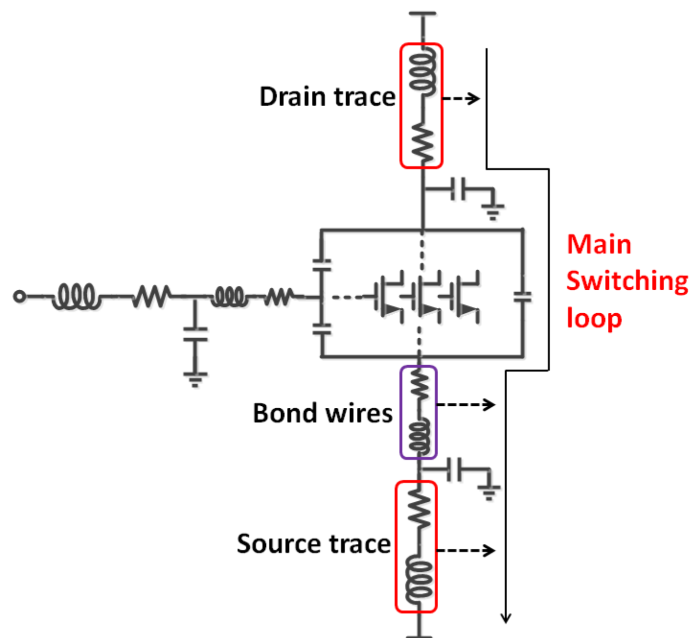


Figure 3.18: The main switching loop

3.4.2 Extraction Algorithm

The purpose of the extraction algorithm is to provide a fast analysis for resistance and inductance extraction in a current path of an MCPM layout. The following extraction algorithm is given for a single switching position in a layout with multiple paralleled die. Fig. 3.19 illustrates the extraction algorithm for half of a layout. Since the other half is symmetrical, electrical parasitic extraction is only applied to half the layout. The switching loop inductance is the sum of the inductances of each segment in the current path, where the inductance of each segment is determined by the trace inductance model.

The trace inductance is nonlinear with respect to trace length because the slope increases as the length of trace increases. It is important to preserve this nonlinearity in order to maintain model accuracy. Preservation of nonlinearity applies to the segments on the same trace with different current paths flowing through them. For example as shown in Fig. 3.19, both L_A and L_{ab} segments are in the same trace, they share current path A, but only L_{ab} resides in current path B. Therefore, L_{ab} is determined by $L_B - L_A$, where L_A and L_B are the self-partial inductance of paths A and B. The same idea applies to segments of L_{bc}, L_{ab1}, and L_{bc1}, and they are determined by $L_C - L_B$, $L_{A1} - L_{B1}$, and $L_{B1} - L_{C1}$, respectively. L_C, L_{A1}, L_{B1} and L_{C1} are self-partial inductances associated with current paths C, A1, B1, and C1 in Fig. 3.19.

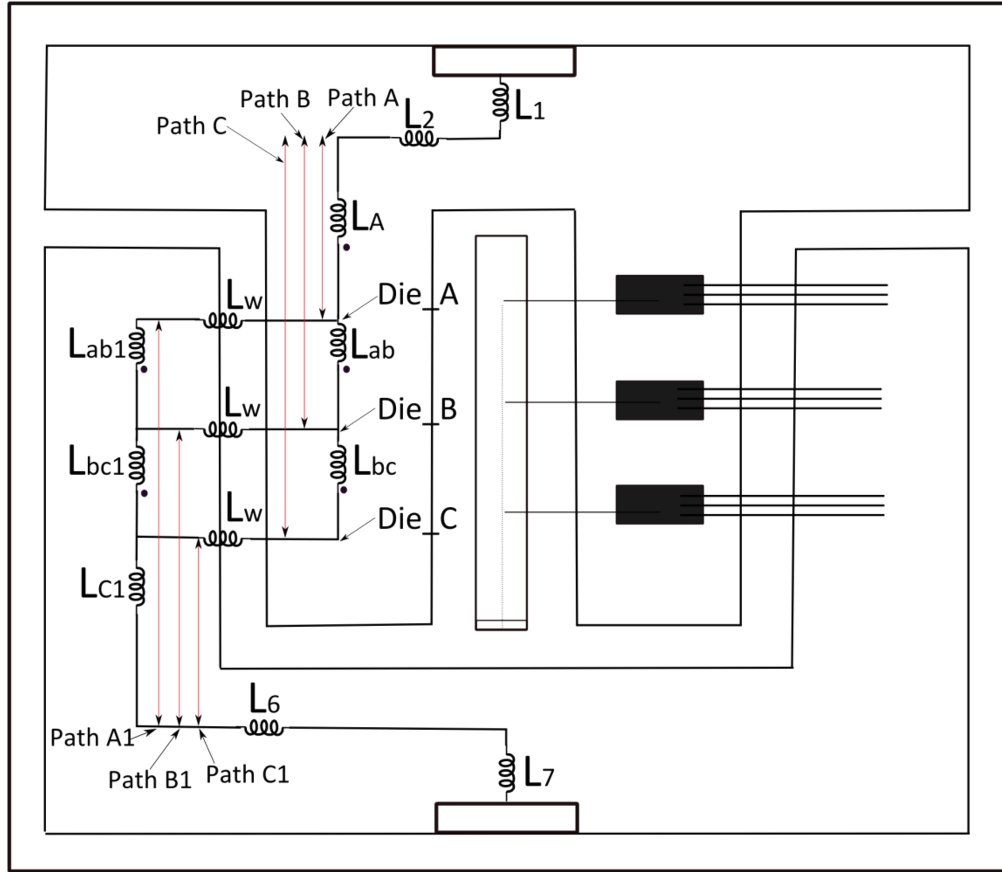


Figure 3.19: Parasitic extraction in a current path

The total inductance for half the layout in a current path is determined by the sum of the inductance of each segment:

$$L = L_1 + L_2 + L_A + L_{equ} + L_{C1} + L_6 + L_7\ . \tag{3.28}$$

L_{equ} is the equivalent inductance of the Wheatstone bridge shown between segments L_A and L_{C1} in Fig. 3.19. To determine the inductance of the Wheatstone bridge, Fig. 3.20 is used to derive the equation for it. The Wheatstone bridge is simplified by using the delta to wye transform as shown in Fig. 3.20 and the equivalent inductance is found via Eq. (3.29).

$$L_{equ} = L_{11} + (L_{22} + L_{bc1})//\,(L_{33} + L_{bc} + L_w) \tag{3.29}$$

where

$$L_{11} = \frac{(L_w + L_{ab1})L_{ab}}{2L_w + L_{ab} + L_{ab1}}$$

$$L_{22} = \frac{(L_w + L_{ab1})L_w}{2L_w + L_{ab} + L_{ab1}}$$

$$L_{33} = \frac{L_w L_{ab}}{2L_w + L_{ab} + L_{ab1}}$$

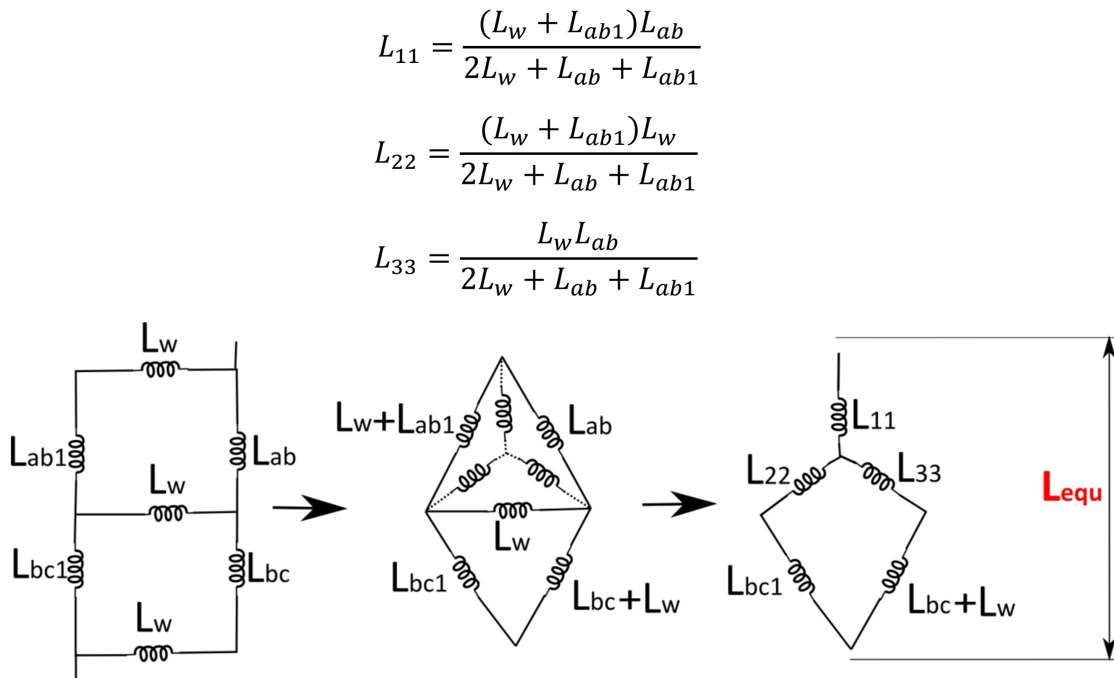


Figure 3.20: Inductance of the Wheatstone bridge

The extraction algorithm for half of the layout developed above is able to represent the inductance changes under the optimization process for both half and full layouts because of the symmetrical layout configuration.

In the extraction algorithm described above, the mutual inductance is not included. To include mutual inductance in the extraction algorithm requires identification of effective lengths of current carrying traces in both the half and full layouts. Then, a proper method to estimate mutual inductance of each segment in the traces needs to be developed. The amount of inductance contributed by the mutual inductances is around 1.2 to 3.1 *nH* from Ansoft Q3D data in APEI layouts, thus represents a small portion of the total path inductance.

The same extraction algorithm is applied to resistance extraction for a current path. Therefore, the resistance of a half layout is given by Eq. (3.30), where R_{equ} is the resistance of the Wheatstone bridge.

$$R = R_1 + R_2 + R_A + R_{equ} + R_{C1} + R_6 + R_7 \tag{3.30}$$

Eq. (3.31) gives the resistance of a full layout. The resistance of the full layout is reduced by almost half because of the addition of the other half of the layout. The resistances R_1 and R_7 are not reduced by half because these current paths are shared between the two symmetrical halves and thus do not reduce the total resistance.

$$R = R_1 + R_7 + (R_2 + R_A + R_{equ} + R_{C1} + R_6)/2 \tag{3.31}$$

3.4.3 Extraction Algorithm Verification

To verify the extraction algorithm, electrical parasitics are extracted for half of the layout in an APEI power module as shown in Fig. 3.21. Then, the electrical parasitics are calculated with the extraction algorithm and compared to parasitic values extracted from Ansoft Q3D. The geometric parameters including trace width, trace length, trace separation, die location, and bond wire length are shown in Fig. 3.21. Some parameters not shown are diameter of bond wires (0.25 mm) and separation between adjacent bond wires (0.6 mm).

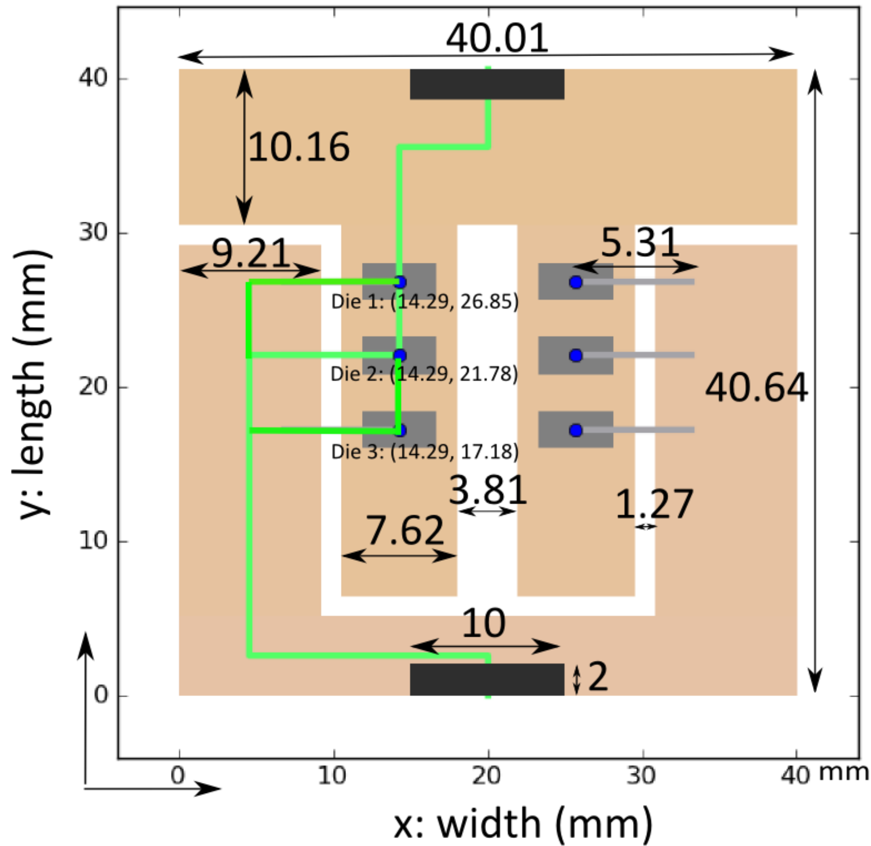


Figure 3.21: Geometric sizes of APEI power module

The inductance of the current path (green) in Fig. 3.21 is 8.85 *nH* given by the model, while it is 11.09 *nH* by Ansoft Q3D. The model predicts 2.24 *nH* less inductance than Ansoft Q3D. One of the major reasons is that there is mutual inductance between trace 1 and trace 2, as shown in Fig. 3.22 below, which increases the total inductance in the current path. Also, the effective current path length estimated by the extraction algorithm is longer than the actual current path length because of the corner effect. In the corner effect (Fig. 3.22), the current concentrates to the inner corners which shorten the current path and result in smaller inductance. However, the contribution of mutual inductance (3.04 *nH*) between current carrying traces is

larger than the reduction of inductance by the corner effect (-1.2 *nH*). Therefore, the model still predicts less inductance than Ansoft Q3D.

To compare the speed between the fast model and Ansoft Q3D, both models are run on the same computer. The fast model, implemented in Python, evaluates the switching loop inductance of the layout shown in Fig. 3.21 in 110 μs while Ansoft Q3D requires 291 s. Thus, the fast model is about one million times faster than Ansoft Q3D, which provides a major time saving advantage in electrical parasitic extraction allowing many different layout configurations to be evaluated quickly.

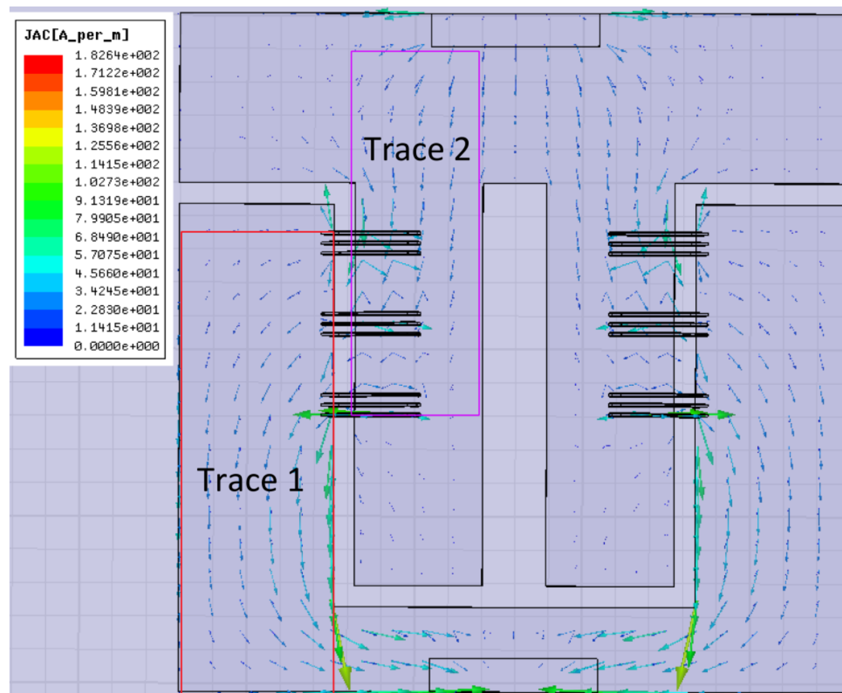


Figure 3.22: Layout current distribution from Ansoft Q3D

Fig. 3.23(a) shows a comparison between the model and Ansoft Q3D for frequency dependent resistance in a half layout from 100 kHz to 1 MHz. Fig. 3.23(b) shows the error percentage of the model as compared to Ansoft Q3D for the resistance over frequency. In the figure, resistance values provided by the model correspond well with the values from Ansoft Q3D with a maximum error of -22%. As the frequency increases the error percentage decreases.

While Fig. 3.24(a) shows the resistance changes with frequency for a full layout given by the model and Ansoft Q3D. Fig. 3.24(b) shows the error percentage of the model as compared to Ansoft Q3D. The model predicts resistance with a maximum error of -14%.

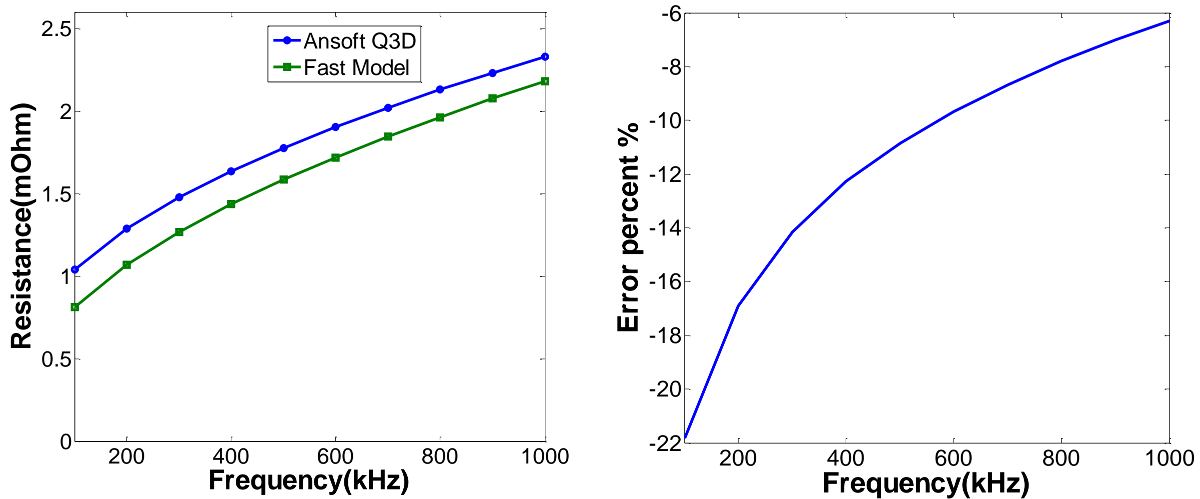


Figure 3.23(a): Half layout resistance verification (Model vs. Ansoft Q3D); (b): Error of the model compared to Ansoft Q3D in half layout

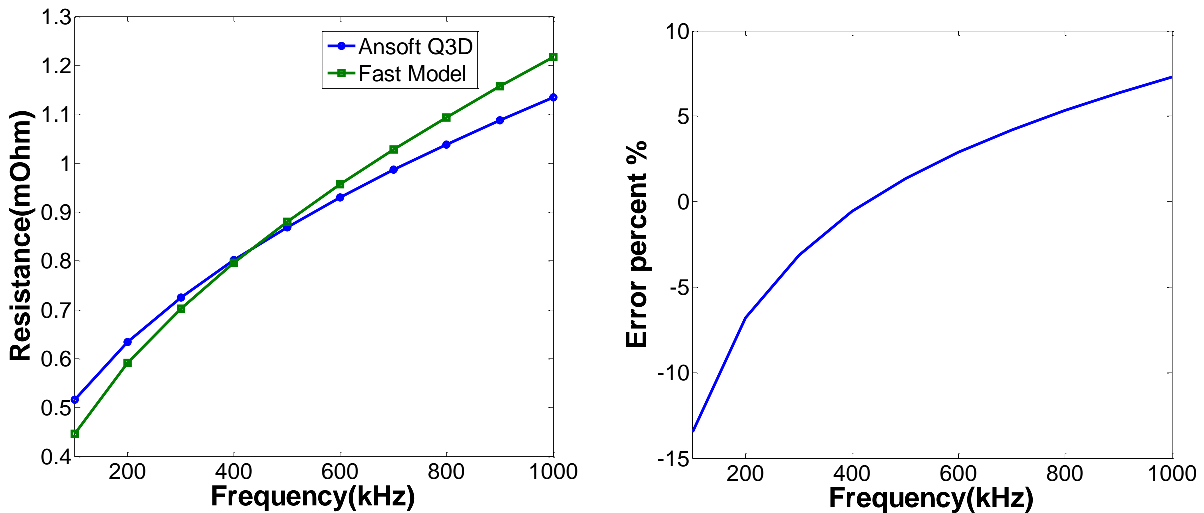


Figure 3.24(a): Full layout resistance verification (Model vs. Ansoft Q3D); (b): Error of the model compared to Ansoft Q3D in full layout

The capacitance between source, drain, and gate traces to the ground plane from the model and Ansoft Q3D is given in Table 3.5, and it shows the model is highly accurate and predicts capacitance to less than 6% error.

Table 3.5: Traces to Ground Plane Capacitance Verification (Model vs. Ansoft Q3D)

Unit: *pF*	**Model**	**Ansoft Q3D**	**Error %**
Source	67.0	67.7	-0.9%
Drain	77.2	79.4	-2.7%
Gate	13.9	14.6	-5.3%

Chapter 4 Thermal and Electrical Parasitic Optimization

In this chapter, the thermal and electrical parasitic models that have been developed in the previous chapters are integrated into a multi-objective optimization algorithm. The multi-objective optimization algorithm is applied to find the optimal trade-off solutions of temperature and electrical parasitics for a layout. First, an introduction of multi-objective optimization is described. Next, a demonstration of multi-objective optimization between temperature and the switching loop inductance is presented.

4.1 Multi-Objective Optimization

Brett Shook, an MSEE candidate working on the MCPM layout synthesis tool, contributed to the implementation of the thermal and electrical parasitic models used by the multi-objective optimization system. He has done a survey of optimization algorithms, and selected a multi-objective optimization algorithm to find best trade-off between multiple objectives. The results in this section were obtained via a piece of software written by Shook that integrates the models and optimization process.

Multi-objective optimization seeks to find trade off solutions for more than two objectives that are conflict to each other. A single solution which can optimize all objectives simultaneously is impossible because the other objectives worsen when trying to optimize one objective further. In a multi-objective problem, a dominated solution is one that is beat out on all objectives, thus it is dominated by some other solution to the problem. While the non-dominated solutions represent the best solutions to the problem and eventually form a Pareto front [36]. In

this thesis, a multi-objective genetic algorithm, the non-dominated sorting genetic algorithm II (NSGA-II), is used to find the best trade-off solutions between temperature and switching loop inductance for layout optimization [37].

In the layout design process, spacing die further apart reduces thermal coupling and thus temperature. To space the die further apart, traces need to be expanded and the bond wires extended which leads to more electrical parasitics in the layout. To reduce both temperature and electrical parasitics, multi-objective optimization is applied to find the best trade-off solutions. Fig. 4.1 shows a multi-objective trade-off curve, a Pareto front, between temperature and electrical parasitics where the boxes represent particular solutions to an MCPM layout design. The boxes on the red curve are the non-dominated solutions (green boxes) with the best trade-off between temperature and electrical parasitics, while the rest of boxes in blue are the dominated solutions which give worse performance in both objectives compared to the non-dominated solutions.

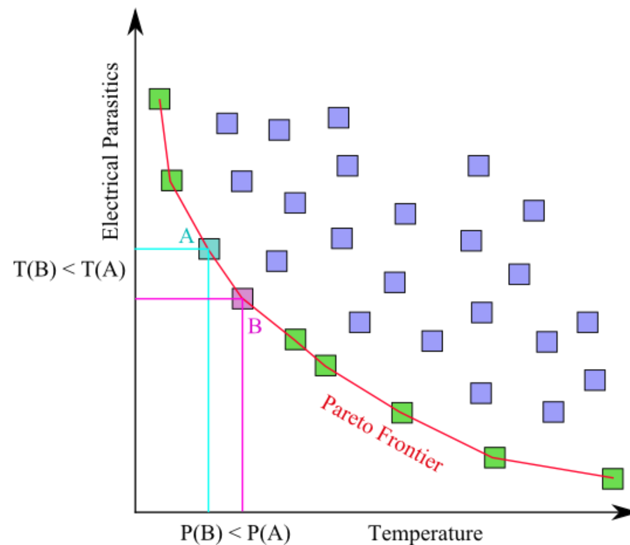


Figure 4.1: Multi-objective trade off curve

In this thesis, the temperature objective considered is the maximum average temperature of the top surface of die in the system, while the electrical parasitic objective can be chosen from a specific resistance, inductance, or capacitance in a layout depending on designer's preference. Depending on the designer's objective, a solution matching their criteria can be chosen from the Pareto front. For example, solution B provides a better solution of an electrical parasitic than solution A but worse temperature. Vice versa, solution A provides a better solution of temperature than solution B, but a worse electrical parasitics.

4.2 Demonstration

To evaluate the fast thermal and parasitic models, a demonstration is set up to find the best trade-off between maximum average temperature of the top surface of the die and the switching loop inductance. A Pareto front in Fig. 4.2 is formed by non-dominated solutions after execution of the multi-objective optimization algorithm. The x-axis is maximum die temperature and y-axis is the switching loop inductance. Optimal designs can be chosen from this Pareto front. As shown in Fig. 4.2, layouts A and B are solutions from the Pareto front. Solution A favors temperature as compared to solution B, while solution B favors loop inductance. As shown in the design A, in order to favor temperature, bond wires are longer, trace is expanded, and die are further apart. While design B shows die spacing are smaller and bond wires are shorter in order to reduce loop inductance. Also, it is shown that the APEI design solution falls in the dominated solution area.

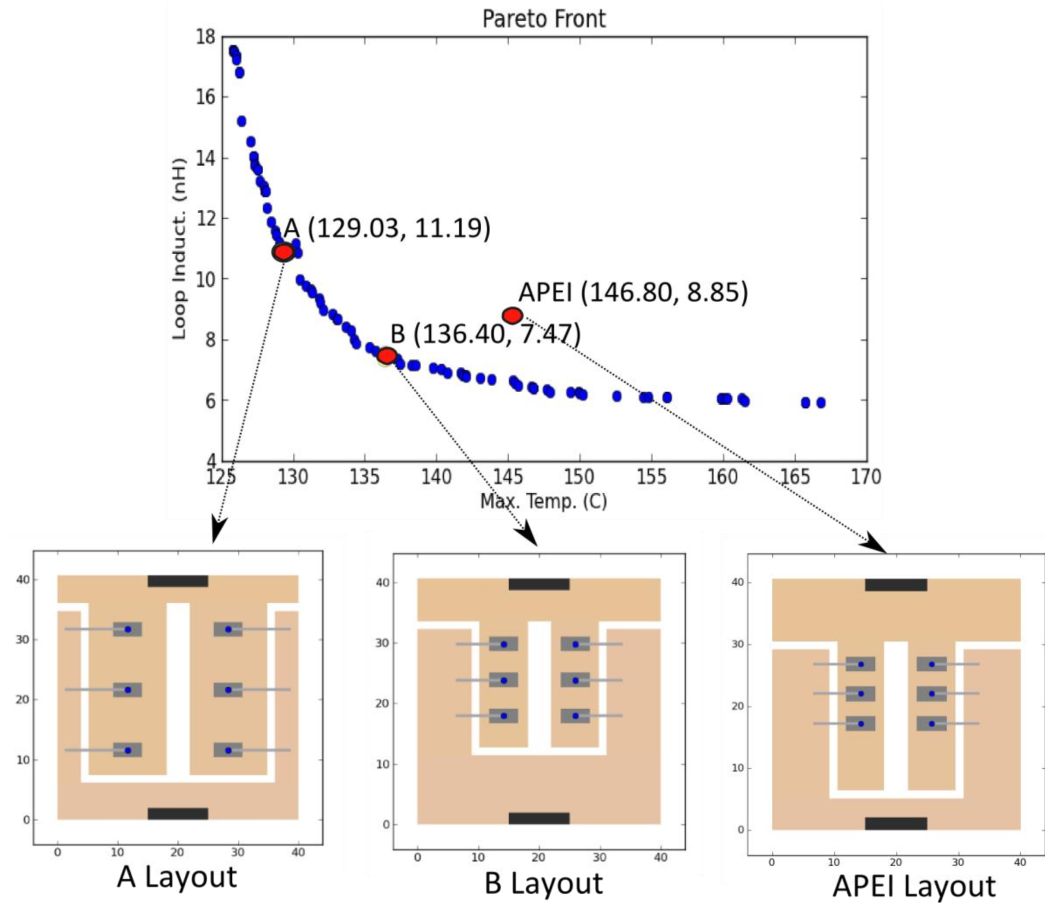


Figure 4.2: Pareto front and layout designs

To verify the optimized results, layout design B is built in both ANSYS and Ansoft Q3D, and the temperature (Max. and Ave. temp) and the loop inductance are compared to the APEI layout design. Table 4.1 shows temperature and loop inductance comparison between APEI and B layouts from both the fast models and the FEA tools (ANSYS and Ansoft Q3D). The maximum die temperature in the APEI layout and layout B (Fig. 4.3) is 143 ℃ and 134 ℃, respectively, which means layout B maximum die temperature is cooler by 9 ℃. The average temperature of the die in the APEI layout and layout B is 138 ℃ and 131 ℃, respectively, which means layout B decreases average temperature by 7 ℃. Also, note that layout B has 1.4 *nH* less loop inductance than the APEI layout as seen from Table 4.1.

Table 4.1: Data Comparison between APEI and B Layouts (Models vs. FEA Tools)

		Max. Temp	Ave. Temp	Loop Ind.
APEI Layout	Fast Models	147 °C	143 °C	8.9 *nH*
	FEA Tools	143 °C	138 °C	11.1 *nH*
B Layout	Fast Models	136 °C	133 °C	7.5 *nH*
	FEA Tools	134 °C	131 °C	9.7 *nH*

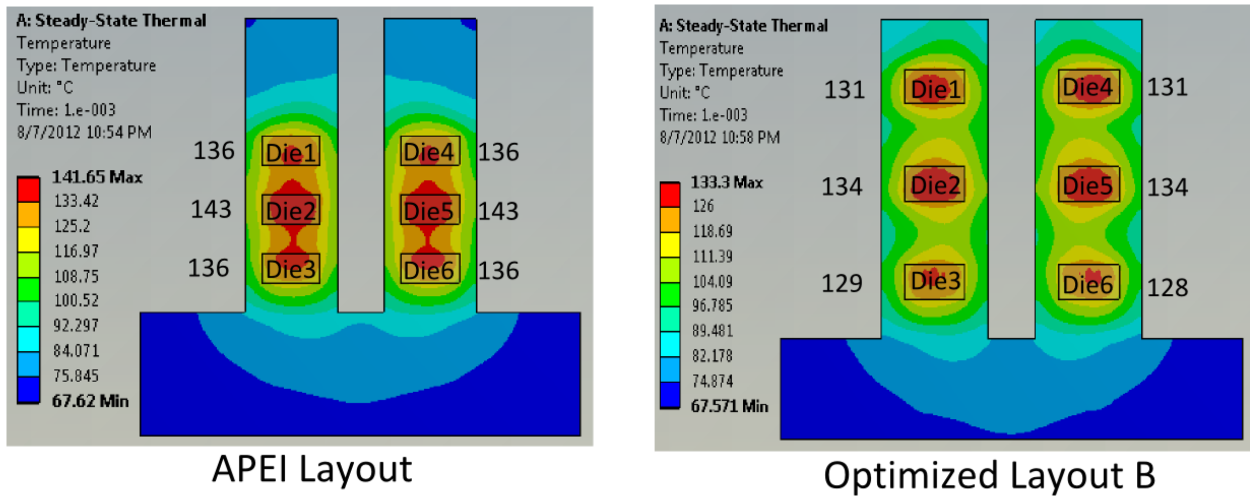


Figure 4.3: Temperature distributions of APEI and B layout designs

Using a multi-objective optimization approach, a package designer is able to obtain optimal designs and tradeoff performance quickly. This greatly reduces design cycle time because layout solutions can be quickly found that match the desired performance criteria.

Chapter 5 Conclusions and Future Work

5.1 Summary and Conclusions

In this thesis, a novel thermal model is developed for MCPMs, and it is verified to predict temperature accurately under varying layouts. The thermal model provides a large speed up in estimating temperature as compared to a thermal FEA tool. An electrical parasitic model for MCPMs is developed using techniques from micro-strip transmission lines, where an extraction algorithm is developed to extract electrical parasitics in a current path of a switching position layout. It is verified to predict electrical parasitics accurately and with a great speed up as compared to existing electrical parasitic extraction tools. The thermal and electrical parasitic models are integrated to execute a multi-objective optimization in order to achieve optimal solutions of layout. Those solutions representing the best trade-off between temperature and electrical parasitics are obtained in a short time, thus facilitating the layout design process in MCPMs.

5.2 Recommendations for Future Work

The thermal model is developed with initial characterization data from a thermal FEA tool in order to ensure accurate temperature approximation. In the future, an automatic thermal characterization would ease the process of getting information from a thermal FEA tool. Also, the thermal model developed in this thesis estimates steady-state temperature of power devices in MCPMs where all die are turned on simultaneously without thermal coupling between die. In the future, a transient thermal model could be developed with thermal coupling coefficients between

die in order to estimate transient thermal behavior where there is interaction between die in MCPMs [38], [19].

The inductance model developed in this thesis neglects the corner effect and mutual inductance thus causing some error. In the future, an inductance model accounting for the corner effect and mutual inductance would improve the model accuracy. The effective current path length could be estimated under the corner effect. The effective length of current carrying traces could also be determined in order to approximate mutual inductance. Then, the extraction algorithm could be developed to account for corner effect and mutual inductance. Also, the resistance model for bond wires does not include proximity effect. In the future, formulation of integral equations for transverse current distribution in the bond wire would be applied to account for proximity effect when there are multiple bond wires. This would increase the resistance model accuracy as the proximity becomes a dominant effect in parallel bond wires.

The thermal model developed in this thesis is based on constant substrate sizes, and the material in each layer does not change. In the future, the model would provide more design options to the package designers if it would consider different materials in each layer and be able to change the substrate size of an MCPM. The thermal model and electrical parasitic models developed in this thesis are modules to be integrated into an MCPM layout synthesis tool. This synthesis tool will help package designers find optimal layout solutions with the lowest temperature and the least electrical parasitics. In the future, a mechanical stress model and EMI model of MCPMs could be developed and integrated into the MCPM layout synthesis tool. Thus, this opens up more opportunities for multi-objective optimization in MCPM design.

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