University of Arkansas, Fayetteville
ScholarWorks@UARK

Theses and Dissertations

12-2011

Investigation Of A Floating Load Buck Dc-Dc Switching Converter

Hong Tan
University of Arkansas, Fayetteville

Follow this and additional works at: http://scholarworks.uark.edu/etd

 Part of the VLSI and Circuits, Embedded and Hardware Systems Commons

Recommended Citation
Tan, Hong, "Investigation Of A Floating Load Buck Dc-Dc Switching Converter" (2011). *Theses and Dissertations*. 136.
http://scholarworks.uark.edu/etd/136

This Thesis is brought to you for free and open access by ScholarWorks@UARK. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of ScholarWorks@UARK. For more information, please contact scholar@uark.edu, ccmiddle@uark.edu.

INVESTIGATION OF A FLOATING LOAD BUCK DC-DC SWITCHING CONVERTER

INVESTIGATION OF A FLOATING LOAD BUCK DC-DC SWITCHING CONVERTER

A thesis submitted in partial fulfillment
of the requirements for the degree of
Masters of Science in Electrical Engineering

By

Hong Tan
University of Arkansas
Bachelor of Science in Electrical Engineering, 2009

December 2011
University of Arkansas

ABSTRACT

A floating load buck DC-DC switching converter was analyzed, simulated, designed and prototyped. The floating load buck converter is first compared to the conventional buck converter. It was found that both the floating load buck converter and conventional buck converter exhibit similar conversion characteristics despite the differences in the placement of their output inductors. A floating load buck converter was designed to be used as a high-voltage off-line light-emitting diodes (LEDs) driver using a Texas Instruments' TPS92001 controller. Finally, the characteristics of this floating load buck converter LED driver were experimentally examined.

This thesis is approved for Recommendation
to the Graduate Council

Thesis Director:

_____

Dr. Simon Ang

Thesis Committee:

_____

Dr. H. Alan Mantooth

_____

Dr. Scott Smith

THESIS DUPLICATION RELEASE

I hereby authorize the University of Arkansas Libraries to duplicate this Thesis when needed for research and/or scholarship.

Agreed _____
Hong Tan

Refused _____
Hong Tan

ACKNOWLEDGEMENTS

I would like to express my gratitude to Dr. Simon Ang for his support and guidance throughout my Master's thesis work. I would also thank Dr. H. Alan Mantooth and Dr. Scott Smith for being part of my thesis committee.

I would like to thank my parents and my sisters and brothers in Christ for their utmost support, love and encouragement.

I am also thankful with Texas Instrument for always providing with the project's resources to design and test the floating load buck converter.

DEDICATION

This paper is dedicated to my Lord and Savior Jesus Christ.

TABLE OF CONTENTS

TABLE OF CONTENTS vii
LIST OF FIGURE viii
LIST OF TABLES x
CHAPTER 1 1
INTRODUCTION 1
1.1 Background 1
1.2 Organization of this thesis 2
CHAPTER 2 3
FLOATING LOAD BUCK CONVERTER 3
2.1 Floating load buck converter 3
2.2 State-Space Averaged Model for an Ideal Floating Load Buck Converter 8
2.3 Control Schemes 11
2.4 Theoretical Calculation 12
CHAPTER 3 15
SIMULATION OF THE FLOAT LOAD BUCK CONVERTER 15
3.1 Introduction to PSpice 15
3.2 Open-loop Simulation 16
3.2.1 Floating Load Buck Converter 16
3.2.2 Comparison with Conventional Buck Converter 17
3.3 Closed loop Simulation 22
3.3.1 Floating Load Buck Converter 22
3.4 Introduction to MATLAB/SIMULINK 29
3.5 Open loop Simulation 30
3.5.1 Floating Load Buck Converter 30
3.5.2 Comparison with Conventional Buck Converter 34
3.6 Closed loop Simulation 37
3.6.1 Floating Load Buck Converter 37
CHAPTER 4 40
EXPERIMENTAL RESULTS 40
4.1 Circuit Block Analysis of the TPS92001 Controller 40
4.2 Functional Blocks of TPS92001 Controller [7] 43
4.3 Characterization of the floating load buck LED driver 48
CHAPTER 5 59
CONCLUSION 59
BIBLIGRAPHY 60
APPENDIX A 62

LIST OF FIGURE

Figure 1.1. DC-DC switching power supply system [12]. 2
Figure 2.1. Circuit schematic of a floating load buck converter. 3
Figure 2.2. Mode 1 equivalent circuit for the floating load buck converter ($0< t \leq t_{on}$). 4
Figure 2.3. Mode 2 equivalent circuit for the floating load buck converter ($t_{on}< t \leq T$). 5
Figure 2.4. Discontinuous mode inductor current waveform [1]. 7
Figure 2.5. Discontinuous mode 2 equivalent circuit for the floating load buck converter ($t_{on}< t \leq t_2$). 8
Figure 2.6. Discontinuous mode 2 equivalent circuit for the floating load buck converter ($t_2< t \leq T$). 8
Figure 2.7. State-space average model circuit schematic of an ideal floating load buck converter. 9
Figure 2.8. Floating load buck converter switched model for *d*T interval. 9
Figure 2.9. Floating load buck converter switched model for (1-*d)*T interval. 10
Figure 2.10. Fixed frequency PWM controller. 12
Figure 3.1. Open loop simulation circuit for a floating load buck converter. 16
Figure 3.2. Output voltage of the open-loop floating load buck converter. 17
Figure 3.3. Inductor current and capacitor current waveforms. 17
Figure 3.4. Open loop simulation circuit schematic for floating load buck converter. 18
Figure 3.5. Open loop simulation circuit schematic for conventional buck converter. 18
Figure 3.6. Transient response due to a load change at time=20msec for floating load buck. 19
Figure 3.7. Transient response due to a load change at time=20msec for conventional buck. 20
Figure 3.8. (a) The voltage across the ideal switch (b) The voltage across diode. 21
Figure 3.9. (a) The voltage across the ideal switch (b) The voltage across diode. 21
Figure 3.10. Closed loop simulation circuit for a floating load buck converter. 22
Figure 3.11. The PSpice diode model [16]. 23
Figure 3.12. Output voltage of the simulated closed loop floating load buck converter. 24
Figure 3.13. Inductor current from the simulated closed loop floating load buck converter. 25
Figure 3.14. Simulation testing points shows on the floating load buck converter. 25
Figure 3.15. Waveforms under the testing circuit for a floating load buck converter. 28
Figure 3.16. Open loop simulation circuit for a floating load buck converter. 30
Figure 3.17. Sawtooth waveform block settings. 31
Figure 3.18. Inside the PWM signal model for the floating load buck converter. 31
Figure 3.19. Subsystem model for open loop floating load buck converter. 32
Figure 3.20. Output voltage waveform and inductor current waveform. 33
Figure 3.21. PWM signal and sawtooth waveforms. 33
Figure 3.22 Open loop simulation circuit for a conventional buck converter. 34
Figure 3.23. Inside the PWM signal model for the conventional buck converter. 35
Figure 3.24. Subsystem model for the conventional buck converter. 35
Figure 3.25. Output voltage waveform and inductor current waveform. 36

Figure 3.26. Top level system model for digital controlled floating load buck converter. 37
Figure 3.27. Output voltage waveform and inductor current waveform. 38
Figure 3.28. Waveform details in the digital controller. 39
Figure 4.1. Circuit schematic for TPS92001. 40
Figure 4.2. Voltage regulator formed by R_5, D_5, R_4 and Q. 41
Figure 4.3. Function blocks inside the TPS92001. 43
Figure 4.4. Initial start point inside the TPS92001. 45
Figure 4.5. When $1V < V_{ss} < 0.5V$, inside the TPS92001. 46
Figure 4.6. When $V_{ss} > 1V$, inside the TPS92001. 47
Figure 4.7. Test circuit at R6 for gate drive signal. 48
Figure 4.8. Gate signal output captured on R6. 49
Figure 4.9. Test circuit for the current-sensed signal. 50
Figure 4.10. Waveforms for the current-sensed signal. 51
Figure 4.11. Test circuit for the Feedback pin signal. 52
Figure 4.12. Waveforms for the Feedback pin signal. 52
Figure 4.13. Test circuit for the oscillator signal. 53
Figure 4.14. Waveforms for the oscillator signal. 54
Figure 4.15. Sawtooth signal from R_{13}. 54
Figure 4.16. Test circuit for free-wheeling diode. 55
Figure 4.17. Waveforms for free-wheeling diode. 56
Figure 4.18. Test circuit for the drain of FQT4N25. 56
Figure 4.19. Waveforms for the drain signal of FQT4N25. 57
Figure 4.20. Test circuit for the Reference pin signal. 58
Figure 4.21. Reference pin signal from TPS92001D. 58

LIST OF TABLES

Table 3.1. Parameters of the PSpcie Diode Model [15]. 23

CHAPTER 1

Introduction

1.1 Background

Switching converters are widely employed in the power electronics industry. They have been commonly used for DC-DC power conversion as shown in Figure1.1. High switching frequencies result in high switching losses for these switching converters. As such, much research is needed to improve efficiency, decrease system dimension, and lower system costs.

The conventional buck converter is one of the basic topologies in DC-DC switching converters. It involves the basic electronic components, such as MOSFET, resistors, inductors, capacitors and several diodes, and it does not require a transformer; so it is relatively simple to design. Normally, a large output RC filter will connects to the output load to achieve small ripple output current.

The floating load buck converter is called floating load due to the fact that it has both terminals of the output load floating. These terminals are not referenced to either the power or ground. It should be noted that the conventional buck converter drives a grounded load. The inductor in the floating load buck converter is in different position, and the output load is floating.

The reason that we would like to study the floating load buck converter is because it has some significant advantages. First of all, considering the cost for the LED drivers, this is one of the cheapest choices. Second, it is ideal for high voltage application since the drive voltage does not depend on the supply voltage. Third, the load from the input

requires no isolation; as such the design does not need a transformer. Fourth, the output capacitance is small, enabling the use of compact, high temperature components. Last, it can be used as an ideal high brightness LED driver when a DC supply voltage greater than the maximum voltage of the HB LED string is available [1].

1.2 Organization of this thesis

This thesis is organized into four chapters. Chapter 2 provides the background for this work. It discusses the basic theory of the floating load buck converter topology. Chapter 3 discusses the two different simulation tools used in this thesis, PSpice and Simulink. Chapter 3 presents and discusses the simulation results between the floating load buck converter and the conventional buck converter. Chapter 4 provides the analysis of the TPS92001, bench testing of a floating load buck converter, using the TPS92001 controller, and compares the captured waveform results to the simulation results. Chapter 5 concludes the thesis.

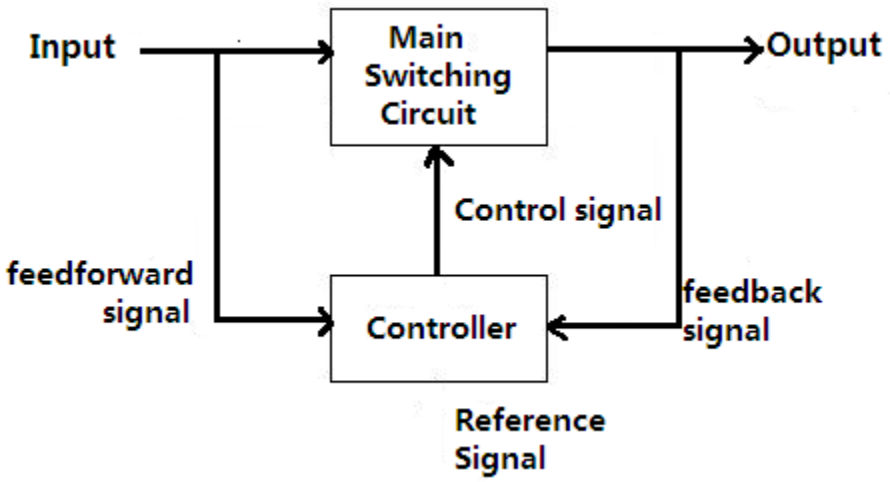


Figure 1.1. DC-DC switching power supply system [12].

CHAPTER 2

Floating Load Buck Converter

2.1 Floating load buck converter

The floating load buck converter using a power MOSFET is shown in Figure 2.1. In a floating load buck converter, the average output voltage V_o (t) is lower than its input voltage V_s. Similar to the conventional buck converter, the operation of the floating load buck converter can be divided into two modes, depending on the switching actions. According to the continuity of the current flowing through the output inductor, the floating load buck converter can be operating either in the continuous mode or the discontinuous mode similar to the conventional buck converter [2].

Continuous Mode:

Mode1 ($0< t \leq t_{on}$), Q_s switches on

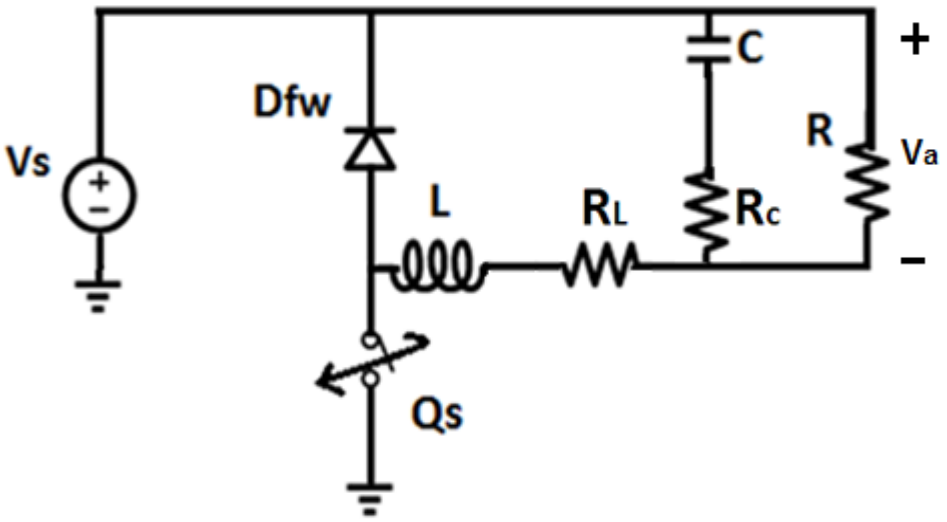


Figure 2.1. Circuit schematic of a floating load buck converter.

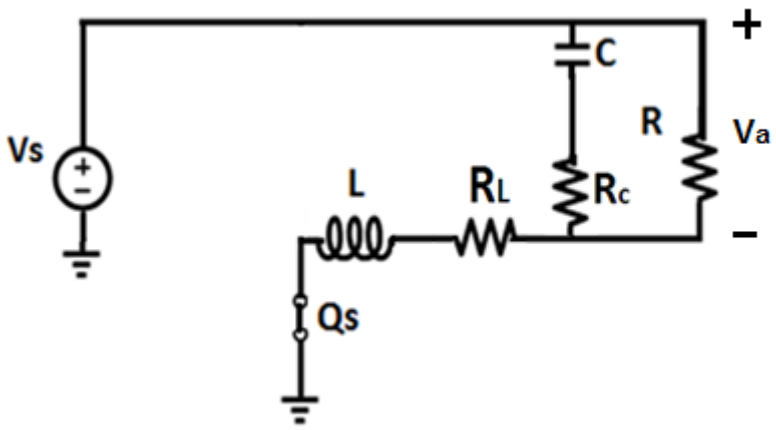


Figure 2.2. Mode 1 equivalent circuit for the floating load buck converter ($0< t \leq t_{on}$).

During mode 1, at the beginning of the switching cycle (at t=0), the switching transistor Q_s is switched on and the free -wheeling diode D_{fw} is switched off. The equivalent circuit during mode 1 is shown in Figure 2.2. Since the input voltage V_s is greater than the average output voltage V_a, the inductor current increases due to the applied input voltage. As such the inductor is being charged and the voltage across the inductor L is:

$$V_L(t) = L\frac{di}{dt} \tag{2-1}$$

For a typical large inductance value, the inductor current $i_L(t)$ increases linearly because of the inductance value. The increase in inductor current is given by

$$\Delta I_{on} = \frac{V_L}{L} * t_{on} \tag{2-2}$$

The voltage across the inductor is $V_L = V_s - V_a$,

$$\Delta I_{on} = \frac{Vs - Va}{L} * t_{on} \tag{2-3}$$

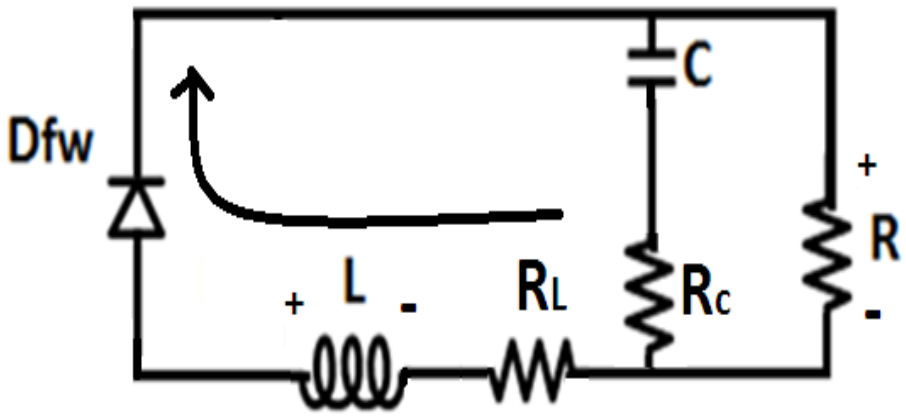


Figure 2.3. Mode 2 equivalent circuit for the floating load buck converter (t_{on}< t ≤T).

or $$V_s - V_a = L\frac{I_2 - I_1}{t_{on}} = L\frac{\Delta I_{on}}{t_{on}} \quad (2\text{-}4)$$

The duration for mode 1 is $$t_{on} = \frac{L * \Delta I_{on}}{(V_s - V_a)} \quad (2\text{-}5)$$

Mode 2(t_{on}< t ≤T), Q_s switches off

At t = t_{on}, the transistor Q_s switches off, the free-wheeling diode D_{fw} is switched on, and Mode 2 begins. The equivalent circuit for mode 2 is shown in Figure 2.3.

As the current flowing through the inductor cannot be interrupted, its voltage polarity across the inductor immediately reverses to maintain the same current which had been flowing through just prior to switching off of the switching transistor Q_s. Once the inductor voltage changes its polarity, the freewheeling diode D_{fw} conducts. The inductor is discharging, and the inductor current falls. The energy stored in the inductor is transferred to the capacitor and consumed by the load. For a large inductance value,

typically found in switching converters, the inductor current $i_L(t)$ will also falls linearly. The decrease in inductor current during Mode 2 for the duration, t_{off} is given by

$$\Delta I_{off} = \frac{V_a}{L} * t_{off} \quad (2\text{-}6)$$

or

$$V_a = L * \frac{\Delta I_{off}}{t_{off}} \quad (2\text{-}7)$$

The duration for mode 1 is

$$t_{off} = \frac{L * \Delta I_{off}}{V_a} \quad (2\text{-}8)$$

For steady-state operation, the peak to peak current ripple in the inductor during the Mode 1 ($0< t \leq t_{on}$) and during the Mode 2 ($t_{on}< t \leq T$) are the same, which is $\Delta I_{on} = \Delta I_{off}$.

From equations (2-3) and (2-6), we obtain

$$\frac{Vs - Va}{L} * t_{on} = \frac{V_a}{L} * t_{off} \quad (2\text{-}9)$$

Define D as the duty cycle. Substituting $t_{on} = DT$ and $t_{off} = (1 - D)T$ into equation (2-9) gives

$$\frac{Vs - Va}{L} * D = \frac{V_a}{L} * (1 - D) \quad (2\text{-}10)$$

Or

$$V_a = V_s * D \quad (2\text{-}11)$$

From equation (2-11), the average output voltage V_a of the floating load buck converter is the product of the duty cycle D and the input voltage V_s, since

$$T = \frac{1}{f_s} = t_{on} + t_{off} \quad (2\text{-}12)$$

$$\frac{1}{f_s} = \frac{L*\Delta I_{on}}{(V_s - V_a)} + \frac{L*\Delta I_{off}}{V_a} \quad (2\text{-}13)$$

Therefore, the current ripple in the inductor can be expressed as

$$\Delta I = \frac{D*V_s(1-D)}{f_s*L} \quad (2\text{-}14)$$

Discontinuous Mode:

In certain cases, the energy stored in the inductor is completely expended just prior to the beginning of the next switching cycle as shown in Figure 2.4. At the point when $i_L = 0$, the value of L is defined as the critical inductance *L*c. The peak inductor current increasing about twice this value compared to continuous mode operation. Thus [1],

$$I_{LP} = 2I_L = \frac{(V_s - V_a)D}{f_s L_C} \quad (2\text{-}15)$$

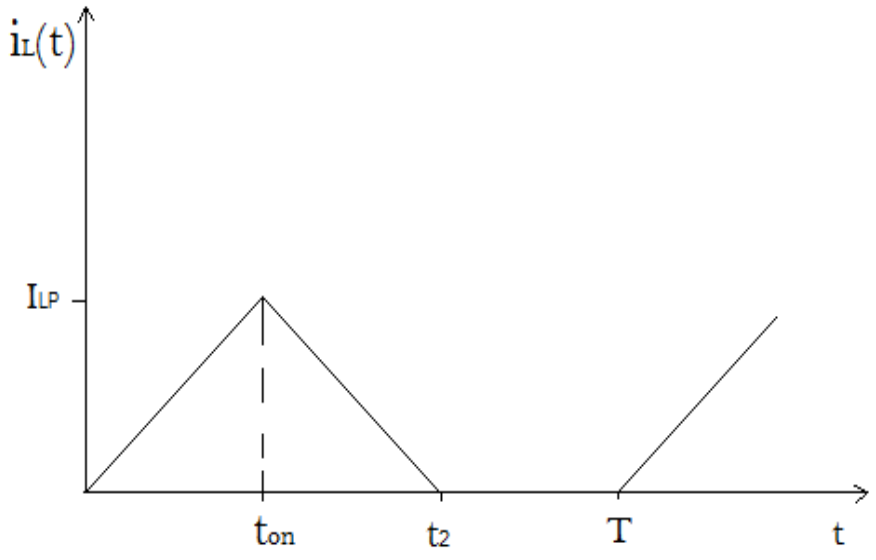


Figure 2.4. Discontinuous mode inductor current waveform [1].

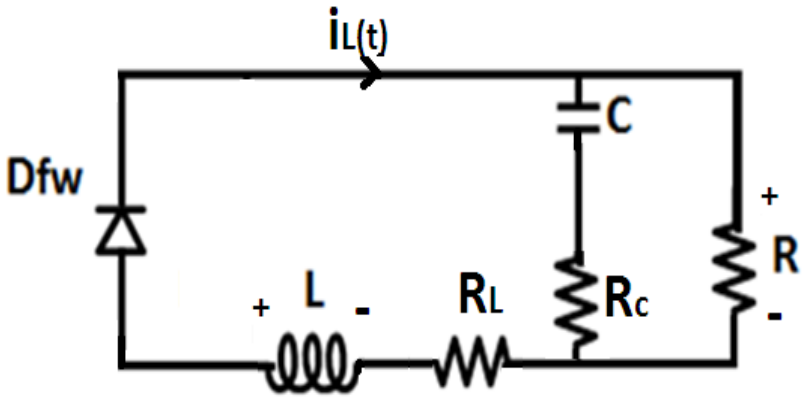


Figure 2.5. Discontinuous mode 2 equivalent circuit for the floating load buck converter ($t_{on} < t \leq t_2$).

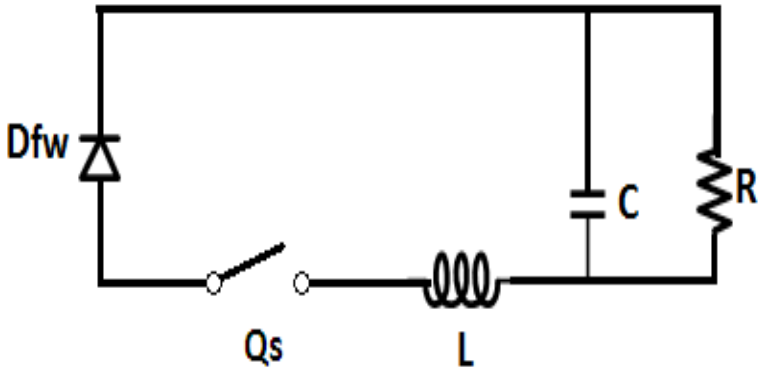


Figure 2.6. Discontinuous mode 2 equivalent circuit for the floating load buck converter ($t_2 < t \leq T$).

The equivalent circuits for the floating load buck converter operating under discontinuous mode are shown in Figures 2.5 and 2.6.

2.2 State-Space Averaged Model for an Ideal Floating Load Buck Converter

In a control system, the state space model can be used to represents a physical system by a set of first-order differential or difference equations. It consist all the possible internal states of the dynamic linear system [3]. In our work, state-space

averaging approximation technique is chosen to approximate the floating load buck switching converter as a continuous linear system.

State variables for this floating load buck converter are chosen as the inductor current, x_1, and the capacitor voltage, x_2 as shown in Figure 2.7. With the assumption of ideal switching devices, two switched models are shown in Figures 2.8 and 2.9.

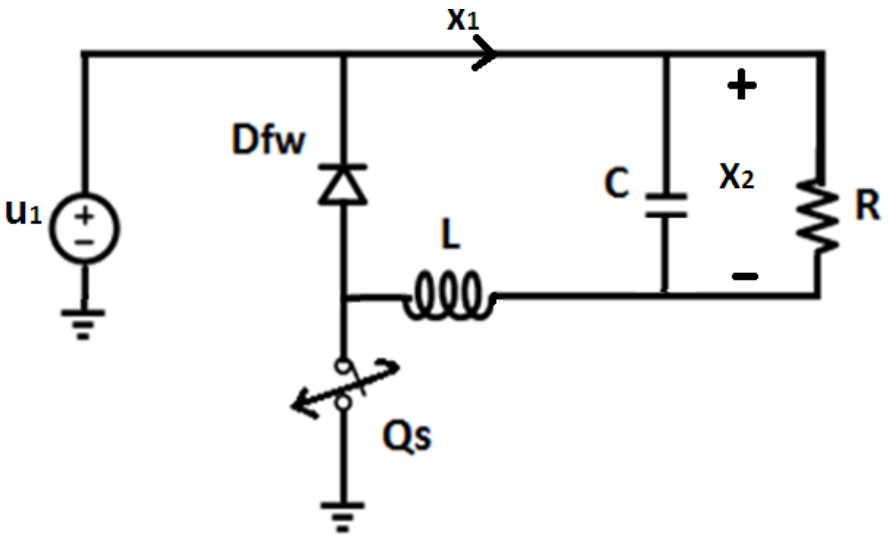


Figure 2.7. State-space average model circuit schematic of an ideal floating load buck converter.

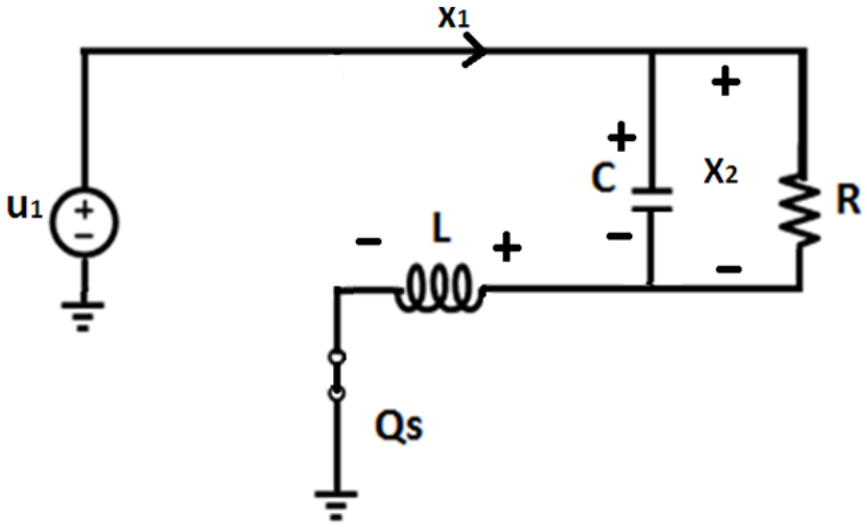


Figure 2.8. Floating load buck converter switched model for *d*T interval.

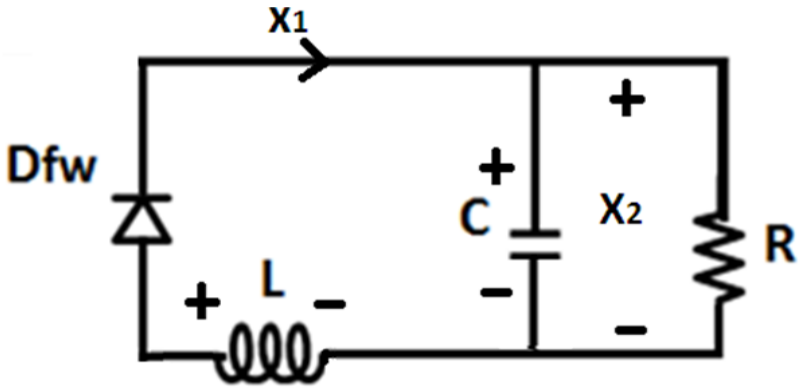


Figure 2.9. Floating load buck converter switched model for (1-*d*)T interval.

During the interval when the switching transistor is on, using Kirchoff's voltage law in Figure 2.8, the state equation can be defined as

$$u_1 = L * \dot{x}_1 + x_2 \tag{2-16}$$

Applying Kirchoff's current law shown in Figure 2.8, the state equation is

$$x_1 = C * \dot{x}_2 + \frac{x_2}{R} \tag{2-17}$$

Similarly, apply Kirchoff's voltage law in Figure 2.9 for the interval when the switch is off, the state equation is

$$0 = L * \dot{x}_1 + x_2 \tag{2-18}$$

Then, using Kirchoff's current law in Figure 2.9, the state equation is

$$x_1 = C * \dot{x}_2 + \frac{x_2}{R} \tag{2-19}$$

State equations for interval *d*T written in matrix form is,

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} [u_1] \tag{2-20}$$

State equations for interval (1-*d)*T written in matrix form is,

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \end{bmatrix} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [u_1] \tag{2-21}$$

The state-space averaged state coefficient matrix is

$$\bar{A} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} d + \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} (1-d) \tag{2-22}$$

With the state-space averaged source coefficient matrix is

$$\bar{B} = \begin{bmatrix} 1/L \\ 0 \end{bmatrix} d + \begin{bmatrix} 0 \\ 0 \end{bmatrix} (1-d) = \begin{bmatrix} d/L \\ 0 \end{bmatrix} \tag{2-23}$$

The state-space averaged equations for the floating load buck converter in matrix form are

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \end{bmatrix} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} d/L \\ 0 \end{bmatrix} [u_1] \tag{2-24}$$

These state-space average equations are identical to those for the conventional buck converters [2].

2.3 Control Schemes

There are several control schemes that has been used for controlling switching mode converters. Current mode Pulse Width Modulation (PWM) control will be used in this thesis project as shown in Figure 2.10. The PWM signal modulates the switch on and off durations, so it controls the inductor energized time period within each switching cycle to maintain the desired voltage or current level at the output. Fixed-frequency

PWM control will be chosen instead of the variable frequency to avoid the unwanted electromagnetic interferences. In order to compare the output voltage error signal to the inductor current sensing signal, the inductor current sensing signal should be converted to a sense voltage signal based on the current mode control design [4]. In a current mode PWM controller, if the duty cycle exceeds 50%, slope compensation is usually required to avoid sub-harmonic oscillation.

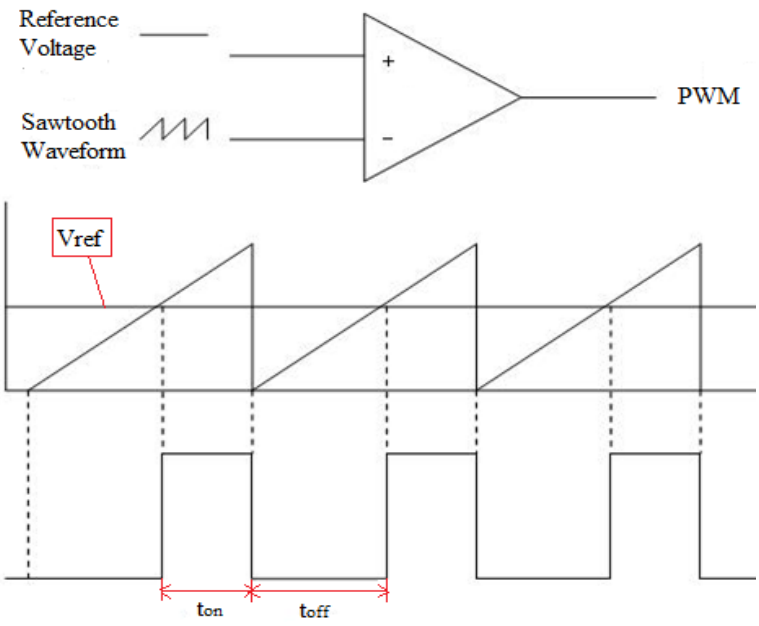


Figure 2.10. Fixed frequency PWM controller.

2.4 Theoretical Calculation

The objective of this section is to obtain component values for the simulation of the floating load buck converter.

For an average output current,

$$I_{oa} = \frac{200mA + 400mA}{2} = 300\text{mA} \qquad (2\text{-}25)$$

The average load resistance is,

$$R_{L_{avg}} = \frac{1.5V}{300mA} = 5\Omega \tag{2-26}$$

And the minimum load resistance is:

$$R_{L_{min}} = \frac{V_0}{I_0} = \frac{1.5V}{400mA} = 2.14\Omega \tag{2-27}$$

A load resistance value 2.8 Ω will be chosen for simulation.

The duty cycle of the floating load buck converter can be determined as:

$$D = \frac{V_R}{V_s} = \frac{1.5V}{15V} = 0.1 \tag{2-28}$$

If the output inductor is chosen to be smaller than the critical inductance at the highest load current, the converter would operate in the discontinuous mode:

$$L \leq \frac{R_{L_{min}}(1-D)}{2f_s} = \frac{2.14\times0.9}{2\times10000} = 96.3\mu H \tag{2-29}$$

An smaller inductance value of 87μH is chosen. With this inductor values, the ideal peak-to-peak ideal inductor ripple current is:

$$\Delta I = \frac{V_s D(1-D)}{f_s L} = \frac{15\times0.1\times0.9}{10000\times87u} = 1.552A \tag{2-30}$$

The output capacitance should be calculated to satisfy the output voltage ripple requirement at full load:

$$\frac{\Delta v_a}{V_a} \leq 5\% \tag{2-31}$$

$$\frac{V_S D(1-D)}{8 f_S^2 L C V_a} \leq 5\% \tag{2-32}$$

Then,

$$C \geq \frac{V_S * D * (1-D)}{8 * f_s^2 * L * V_a * 0.05} = \frac{15 * 0.1 * (1-0.1)}{8 * 10000^2 * 87 * 10^{-6} * 1.5 * 0.05} = 258.62 \mu F \tag{2-33}$$

In practice, a value of 470μF is chosen. The chosen output capacitance is usually much larger than the calculated value in order to reduce the equivalent series resistance (ESR) on the capacitors. It is a normal practice to further reduce the ripple voltage by paralleling several capacitors to reduce their ESRs.

CHAPTER 3

Simulation of the Float Load Buck Converter

3.1 Introduction to PSpice

PSpice is a version of the standard circuit simulator Spice. It is widely used as a simulation tool to analyze analog circuit performance in both steady-state and transient operations. PSpice is licensed from the MicroSim Corporation, which is one of the many commercial derivatives of the University of California at Berkeley's SPICE (Simulation Program with Integrated Circuit Emphasis) simulation tool[5].

To obtain a circuit file for a PSpice simulation, the first step is to draw the circuit diagram and then number all the nodes using the schematic capture feature in PSpice. An electrical circuit node consists of at least two connections. Components models can be found in the PSpice libraries. Basically, the simulation can be performed using various levels of device and component modeling. Once the circuit is drawn, and checked for connections, user can create a simulation profile for the simulation. The user can place the probes to a specific point in the circuit to visualize the current and voltage waveforms.

3.2 Open-loop Simulation

3.2.1 Floating Load Buck Converter

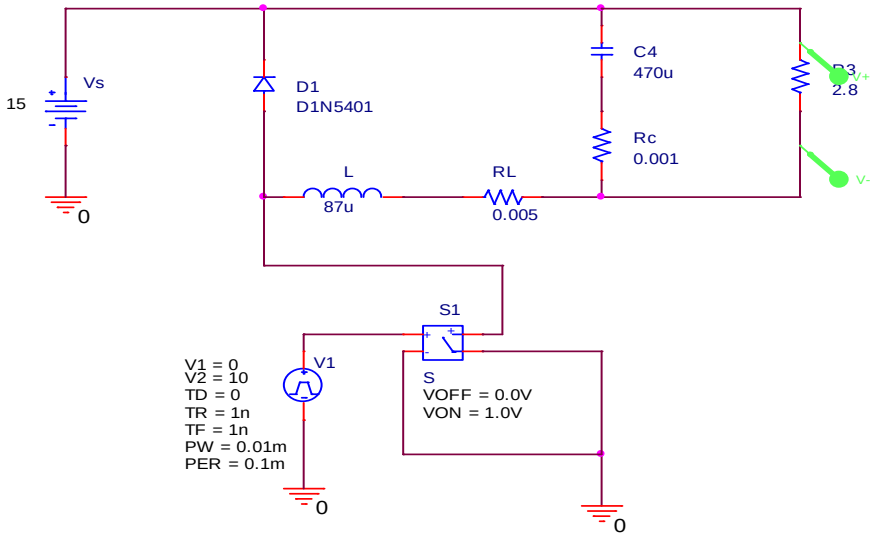


Figure 3.1. Open-loop simulation circuit for a floating load buck converter.

The open-loop floating load buck converter was designed using PSpice with the values calculated from Chapter 2. Figure 3.1 shows the PSpice circuit schematic for the simulation of the open-loop floating load buck converter. Ideal switch S_1 is used to represent the switching element. The voltage pulse generator V_1 functions as a PWM signal generator, it generates the duty cycle, the rise, and fall time of the pulse for the converter. As shown, the switching frequency is 10 kHz.

Figure 3.2 shows that the output voltage of the open-loop floating load buck converter to be at 1.5V. This is as predicted from the duty cycle.

Figure 3.3 shows the current across the inductor and capacitor of simulated floating load buck converter. The discontinuity in the inductor current waveform

indicates that the open-loop floating load buck converter is operating in discontinuous mode.

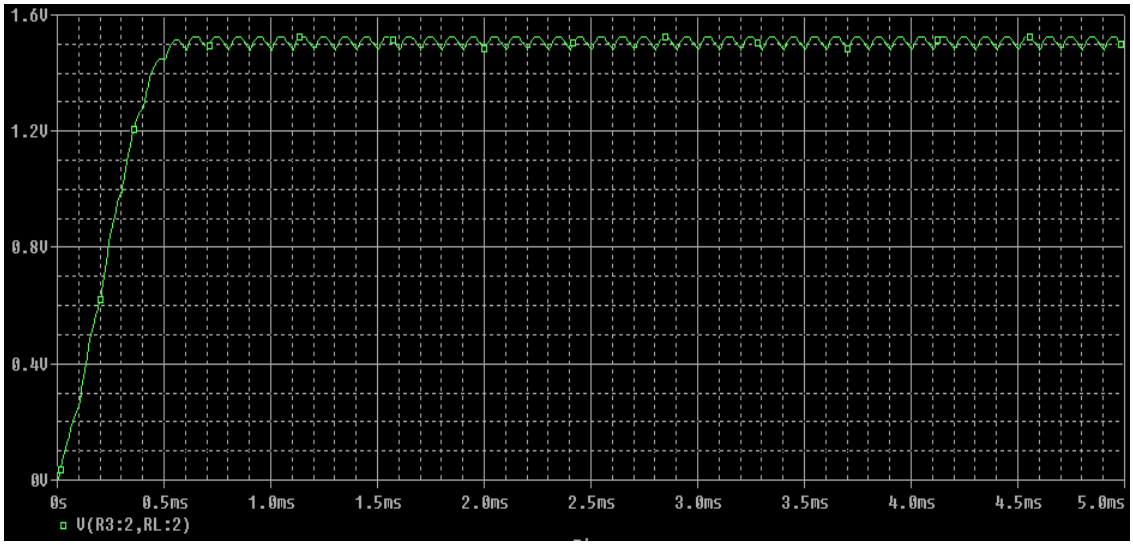


Figure 3.2. Output voltage of the open-loop floating load buck converter.

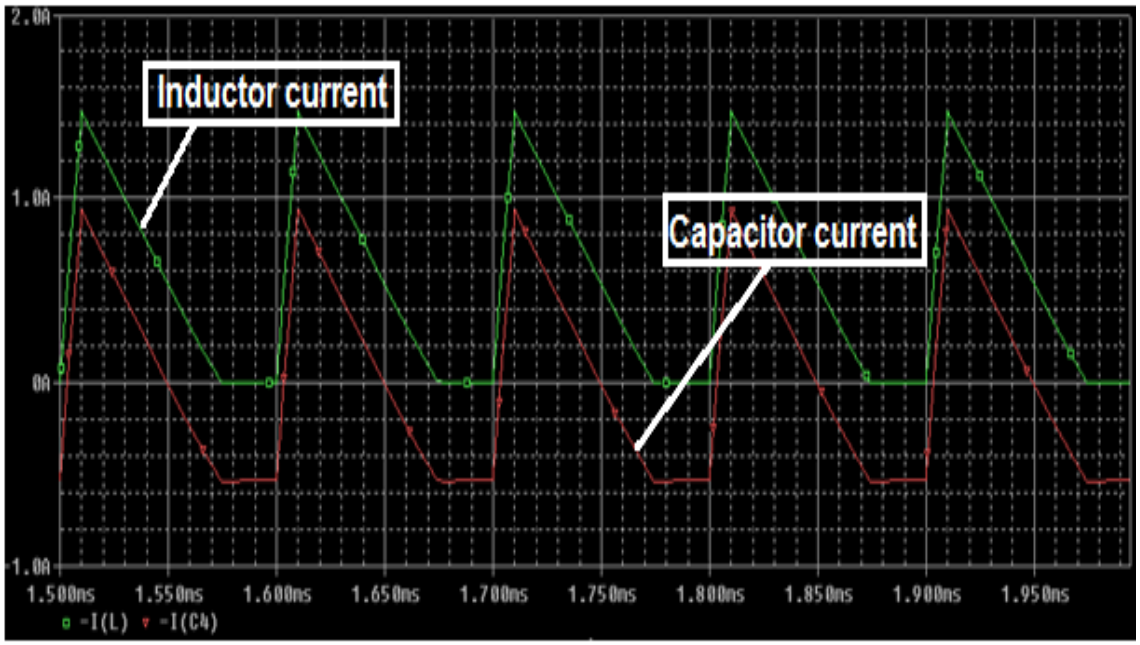


Figure 3.3. Inductor current and capacitor current waveforms.

3.2.2 Comparison with Conventional Buck Converter

For comparison purpose, the same ideal switches, diodes, inductors, and capacitors for both floating load buck converter and buck converter were used for the simulation.

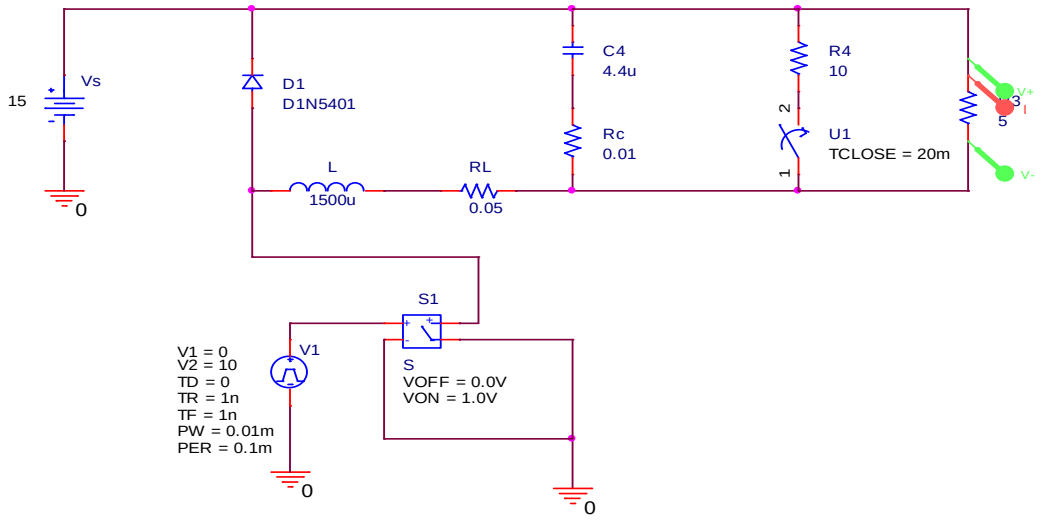


Figure 3.4. Open-loop simulation circuit schematic for floating load buck converter.

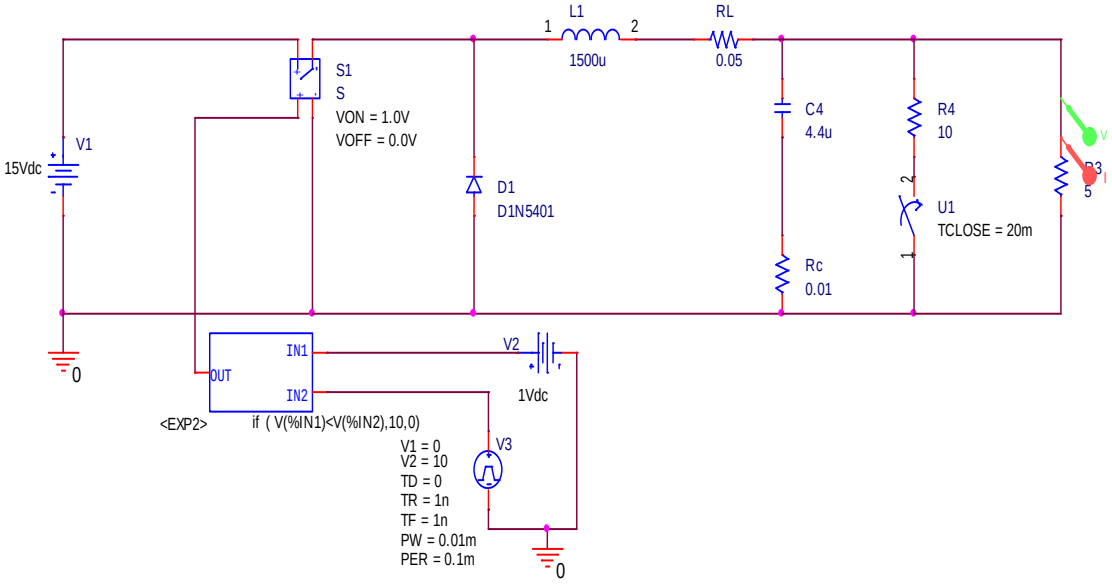


Figure 3.5. Open-loop simulation circuit schematic for conventional buck converter.

Figures 3.4 and 3.5 show the circuit schematic for the floating load buck converter and the conventional buck converter, respectively.

Figure 3.6 (a) shows the current transient response while Figure 3.6 (b) shows the voltage transient response from the floating load buck converter.

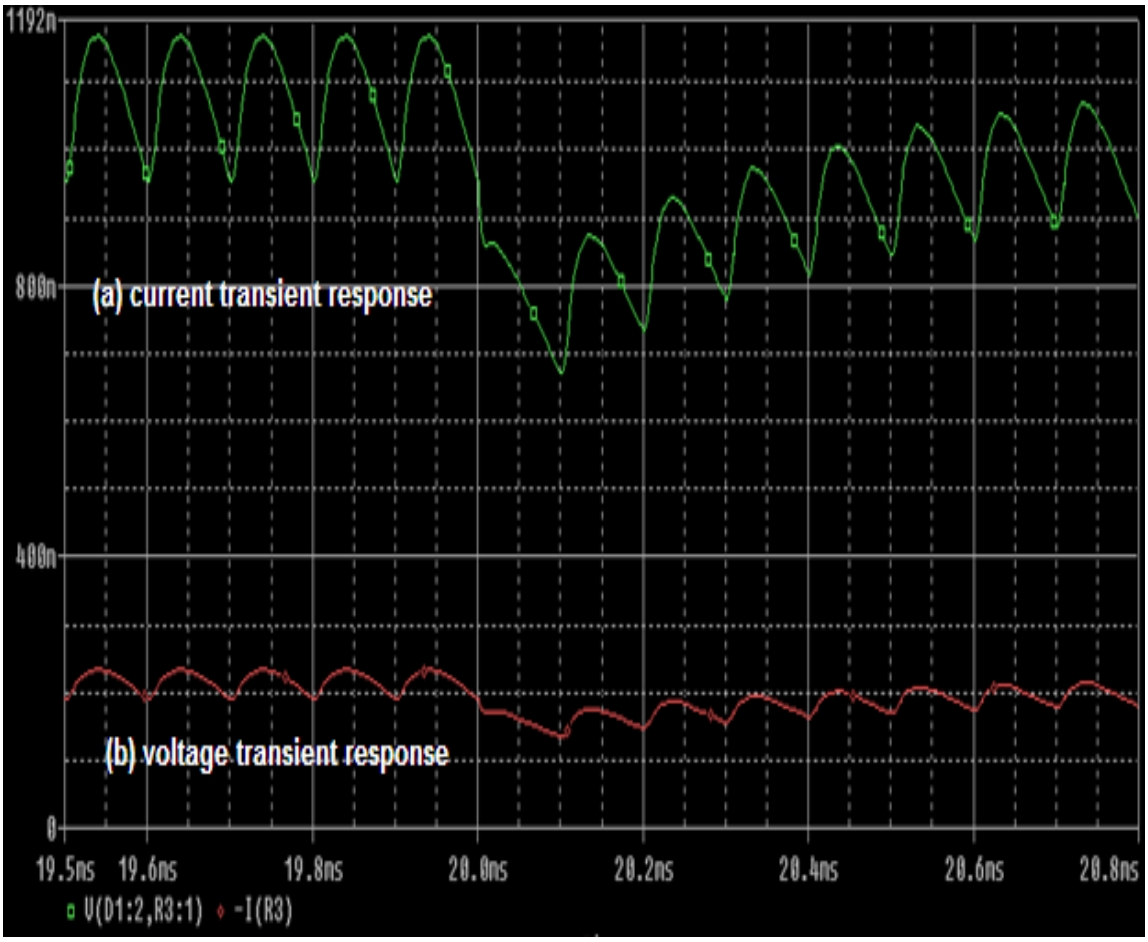


Figure 3.6. Transient response due to a load change at time=20msec for floating load buck.

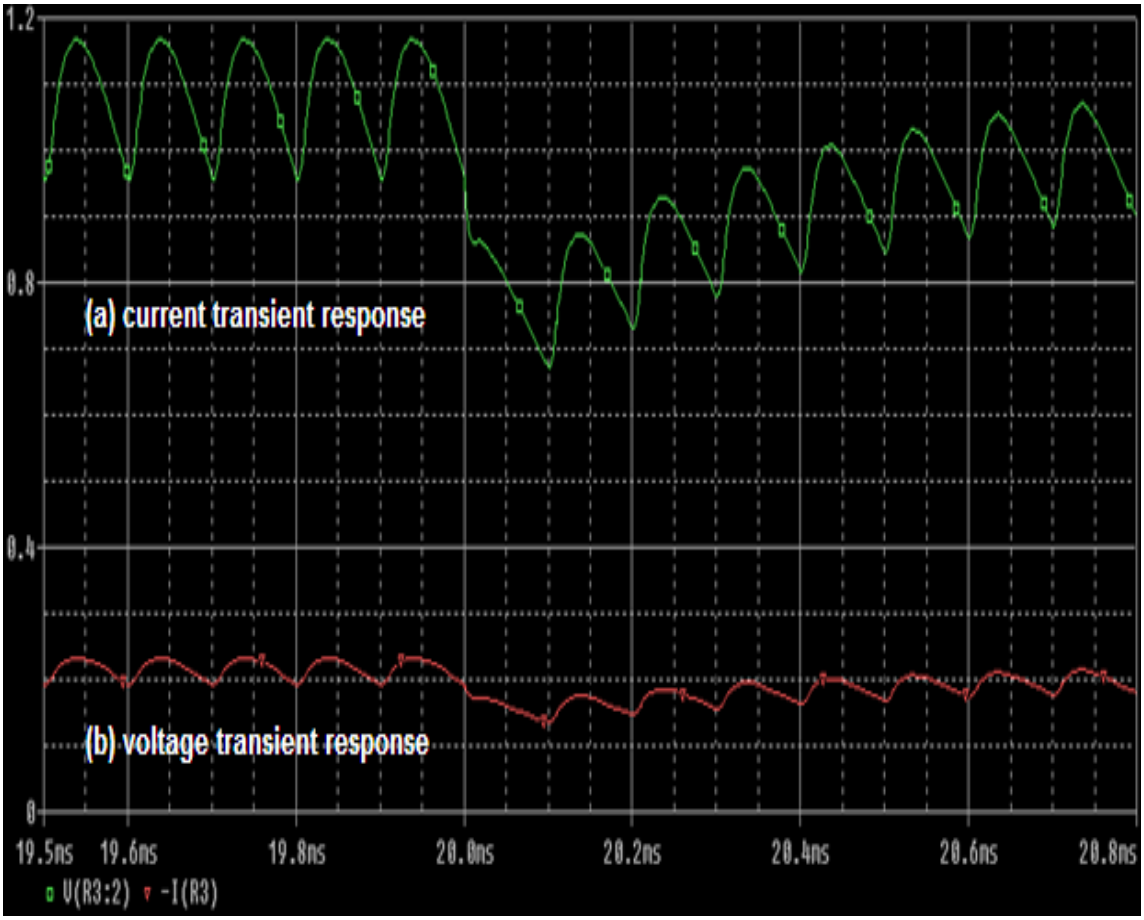


Figure 3.7. Transient response due to a load change at time=20msec for conventional buck.

Figure 3.7 (a) shows the current transient response while Figure 3.7 (b) shows the voltage transient response for the conventional buck converter. Comparing the transient response from Figures 3.6 (a) and 3.6 (b) and Figures 3.7 (a) and 3.7 (b), we can see that they exhibit similar behaviors.

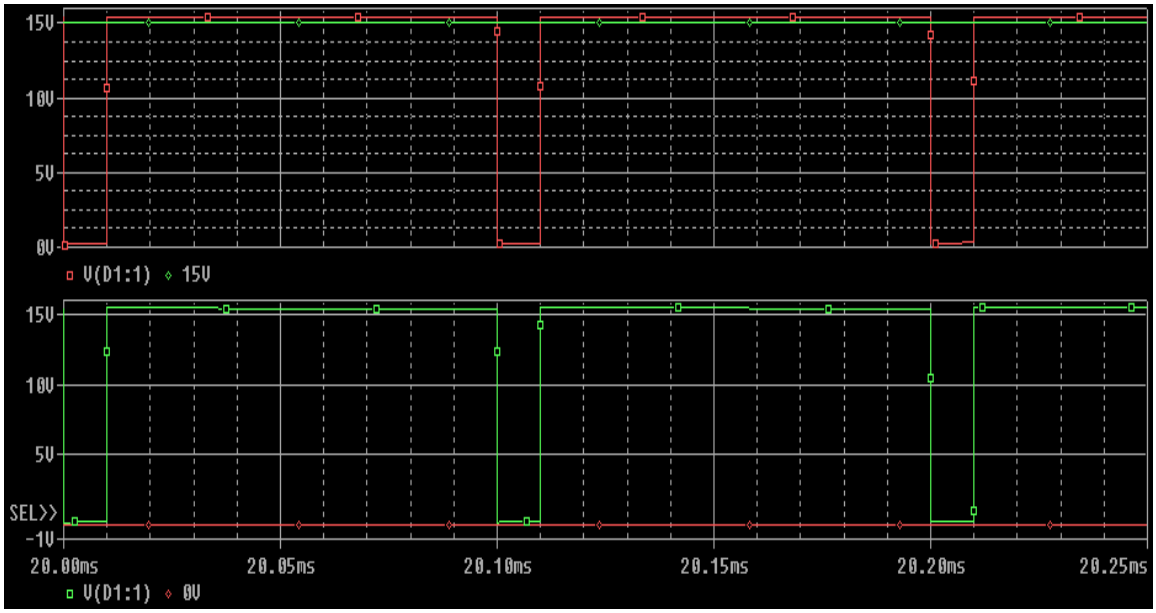


Figure 3.8. (a) The voltage across the ideal switch (b) The voltage across diode.

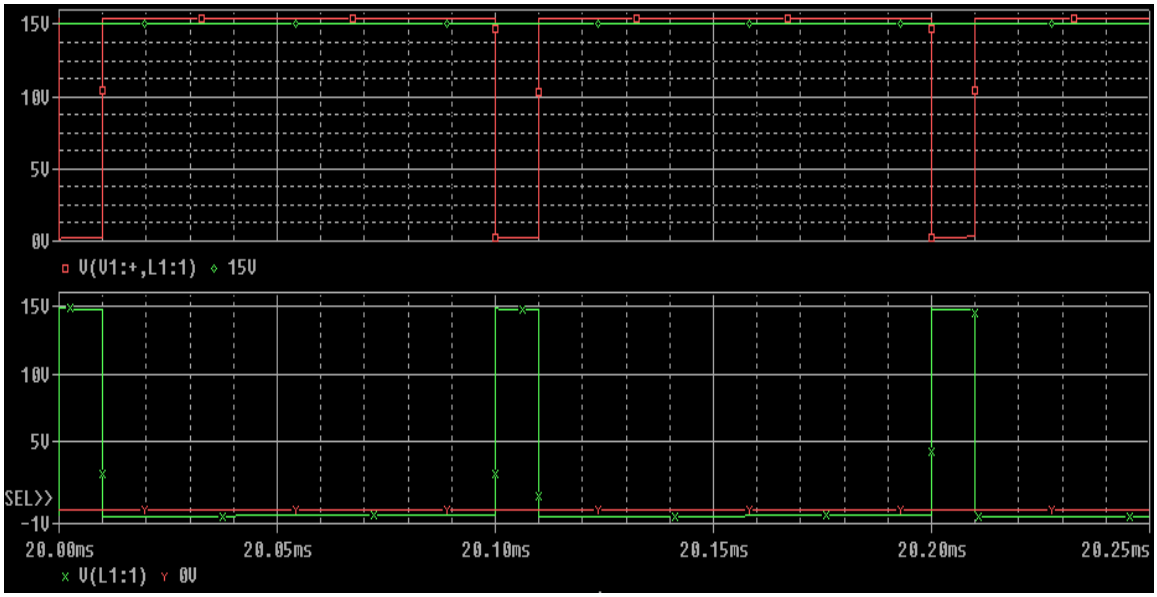


Figure 3.9. (a) The voltage across the ideal switch (b) The voltage across diode.

Figure 3.8 (a) shows the voltage across the ideal switch while Figure 3.8 (b) shows the voltage across the diodes from the floating load buck converter. Figure 3.9 (a) shows the voltage across the ideal switch while Figure 3.9 (b) shows the voltage across the diodes from the conventional buck converter.

Comparing the voltage across the ideal switch and diodes from Figures 3.8 (a) and 3.8 (b) and Figures 3.9 (a) and 3.9 (b), we can observe that they have exactly the same amount of voltage drop on the ideal switches as well as on the diodes.

3.3 Closed loop Simulation

3.3.1 Floating Load Buck Converter

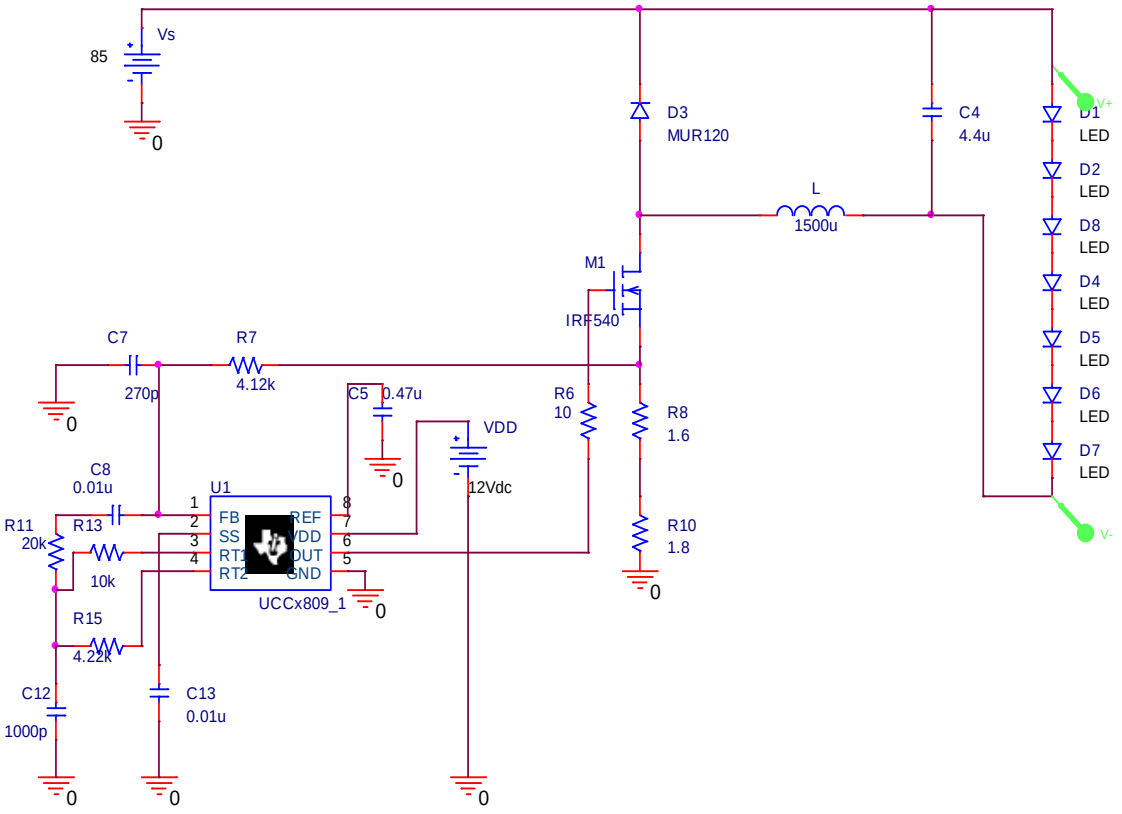


Figure 3.10. Closed loop simulation circuit for a floating load buck converter.

Figure 3.10 shows the circuit schematic of the closed loop simulation of the floating load buck converter operating as a LED driver for seven white LEDs using a Texas Instrument's TPS92001 controller. The TPS92001 is modeled as a UCCX809_1 controller as shown in Appendix A. The details of this closed loop floating load buck converter are discussed in Chapter 4.

Equations (3-1), (3-2) and (3-3) were used to determine the PSpice diode model parameters values [6]. As shown in Fig 3.11, the LED diode model was built by changing an existing diode model. Table 3.1 describes all the PSpice parameters individually.

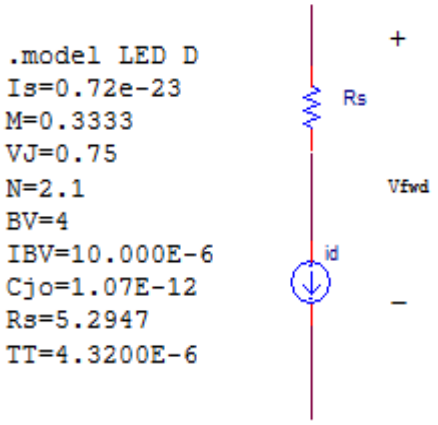


Figure 3.11. The PSpice diode model [6].

Pspice Parameter	Description	Units
Is	Saturation current	A
N	Emission coefficient	
RS	Ohmic resistance	Ω
VJ	Built-in potential	V
CJ0	Zero-bias depletion (junction) capacitance	F
M	Grading coefficient	
TT	Transit time	s
BV	Breakdown voltage	V
IBV	Reverse current at Breakdown voltage	A

Table 3.1. Parameters of the PSpcie Diode Model [7].

$$I_{fwd} = I_S * (e^{Vd/N*Vt} - 1) \quad (3\text{-}1)$$

$$V_d = N * V_t * \ln\left(\frac{I_{fwd}}{I_s}+1\right) \quad (3\text{-}2)$$

$$V_{fwd} = I_{fwd} * R_s + N * V_t * \ln\left(\frac{I_{fwd}}{I_s}+1\right) \quad (3\text{-}3)$$

Figure 3.12 shows the output voltage of the simulated closed loop LED driver. For seven LED diodes, the output voltage is expected to be 19.8V.

The current across the inductor is shown in Figure 3.13. As can be seen, the continuity of the current waveform indicates that the floating load buck converter is operating in its continuous mode.

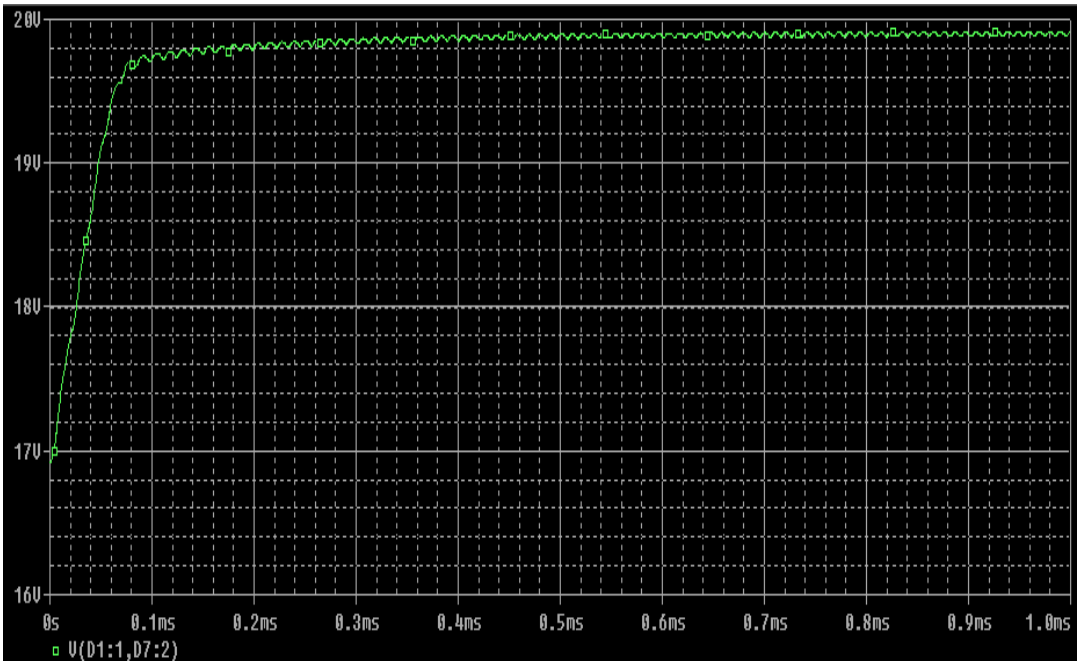


Figure 3.12. Output voltage of the simulated closed loop floating load buck converter.

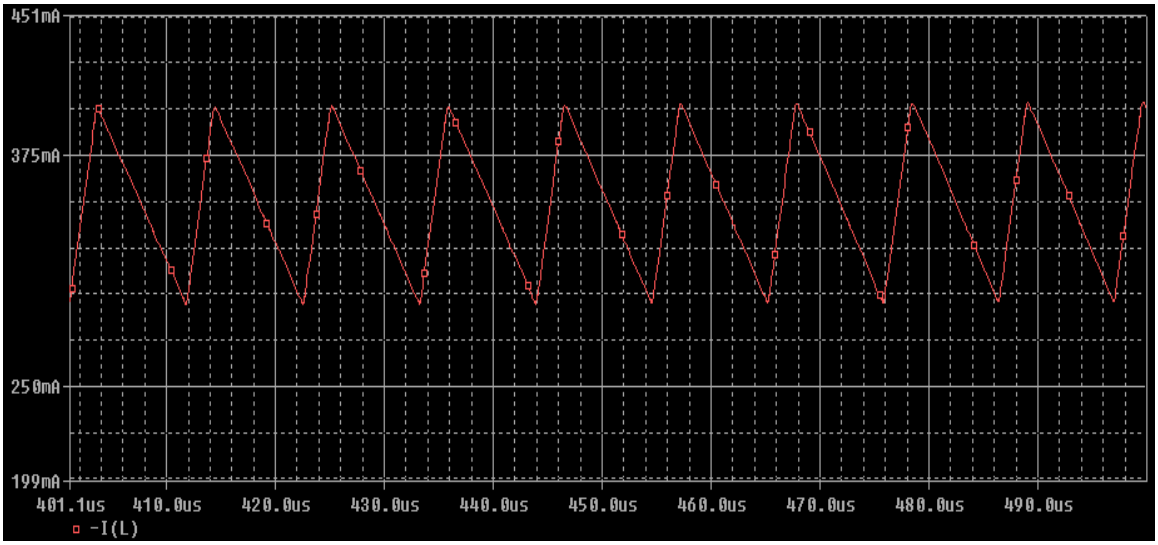


Figure 3.13. Inductor current from the simulated closed loop floating load buck converter.

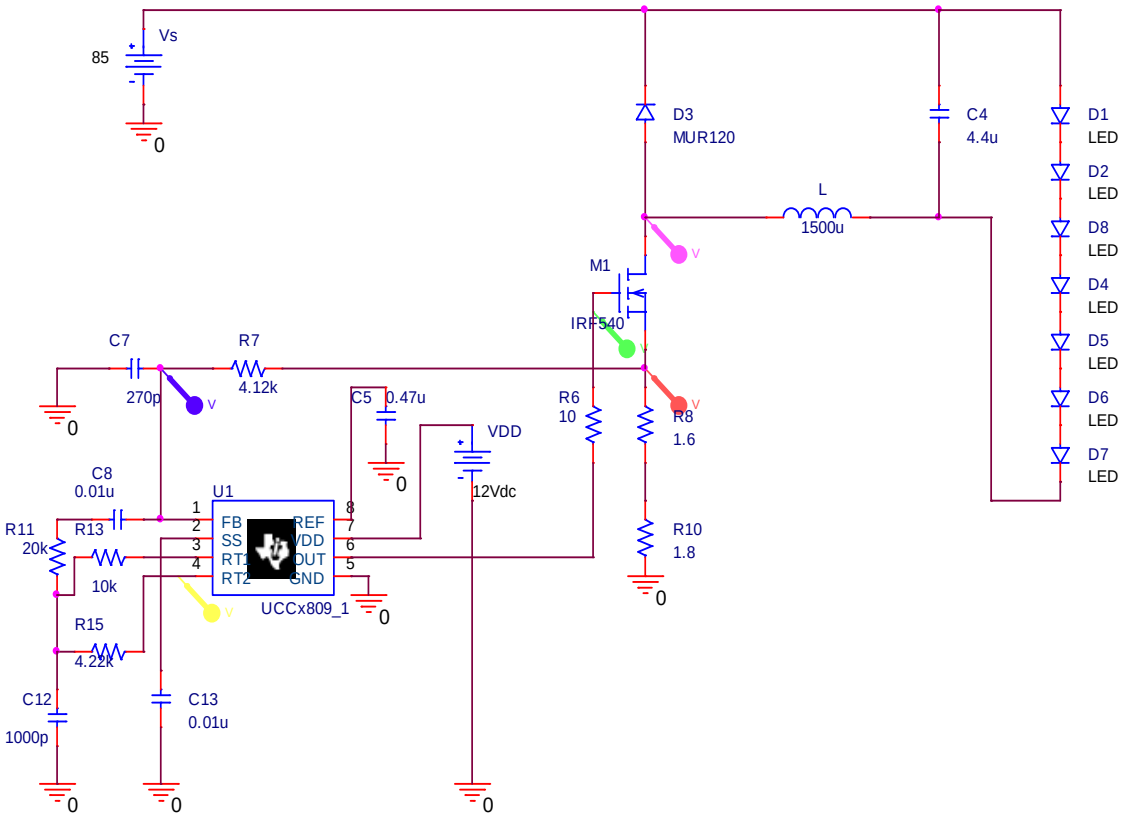


Figure 3.14. Simulation testing points shows on the floating load buck converter.

Figure 3.14 shows the circuit nodes for the captured waveforms shown in Figure 3.15.

As shown in Fig 3.14, seven diode models are used to modify LED load. A DC voltage of 85V was used as the input power supply. The Texas Instruments' UCCX809_1 PSpice model was chosen as the controller and driver for the isolated DC-to-DC fixed frequency floating load buck converter. A 12V DC power supply connected to pin6 of the controller is to provide the power to the chip. There is an internal oscillator inside the chip, which creates a sawtooth waveform for the PWM comparator by charging and discharging a timing capacitor. The R_{13}, R_{15} and C_{12} set the switching frequency of the converter according to the equations (3-4) and (3-5) [8].

$$f_{osc} = (0.74*(C_{12}+27pF)*(R_{13}+R_{15}))^{-1} \quad (3\text{-}4)$$

$$D_{max}=0.74*R_{13}*(C_{12}+27pF)* f_{osc} \quad (3\text{-}5)$$

In this simulated closed loop floating load buck converter, the switching frequency is set to be about 92.53 kHz. As such, the switching time period will be around 10.8µs. As shown in Figure 3.15, the switching time period is shown to be about 10.5µs, which is closed to the design value. The duty cycle is about 23.81%, which satisfies the converting ratio between the input and output voltages, which is $\frac{V_{out}}{V_{in}} = \frac{19.8V}{85V} = 23.29\%$ for the converter.

Figure 3.15(a) shows the gate drive signal output from the PWM controller. This signal is used to drive the MOSFET switch, turning it on and off. Figure 3.15(b) indicates the sensing signal across the current sensing resistor at the source circuitry of the power MOSFET using a resistor sensing technique. Figure 3.15(c) shows the sensing feedback

signal at the FB or CS pin of the TPS92001 controller. The signal is input to the controller through the FB or CS pin. Figure 3.15(d) shows the sawtooth signal of the TPS92001 PWM controller, which indicates the switching frequency for the switching converter. Figure 3.15(e) shows the voltage waveform from the free-wheeling diode. As can be seen, diode conducts when the switch turns off. These waveforms will be compared to experimentally obtained waveforms in Chapter4.

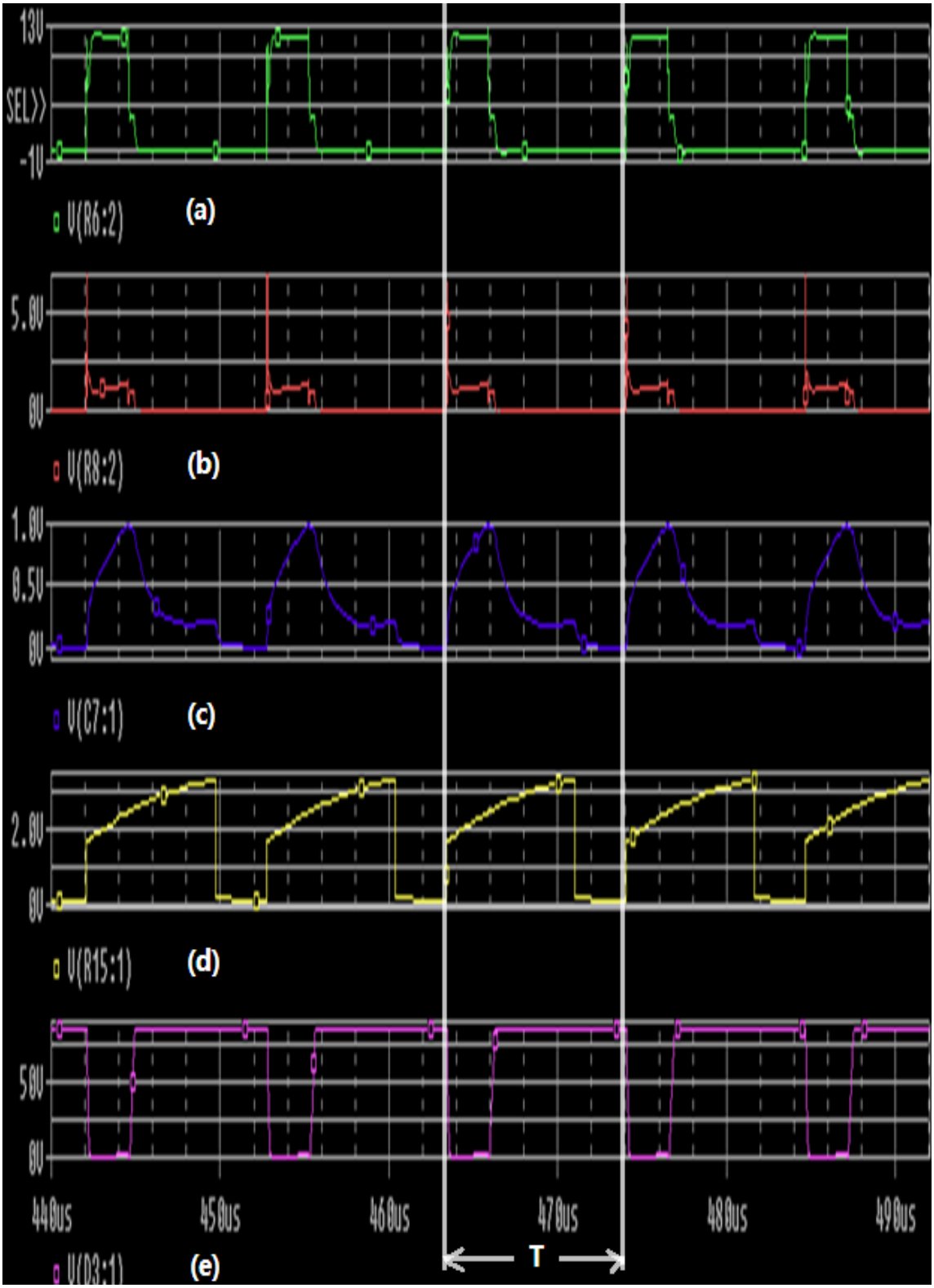


Figure 3.15. Waveforms under the testing circuit for a floating load buck converter.

3.4 Introduction to MATLAB/SIMULINK

Simulink, developed by the MathWorks, Inc., is a program that runs as a companion to MATLAB. It is a software package for modeling, simulating, and analyzing dynamical systems [9]. For modeling, Simulink provides a graphical user interface for building models as block diagrams. After defining a model, the simulation can be performed using a choice of many integration methods, either from the Simulink menus or by running commands in the MATLAB's command window. Using scope and other display blocks, Simulink shows the simulation results while the simulation is running [10].

3.5 Open loop Simulation

3.5.1 Floating Load Buck Converter

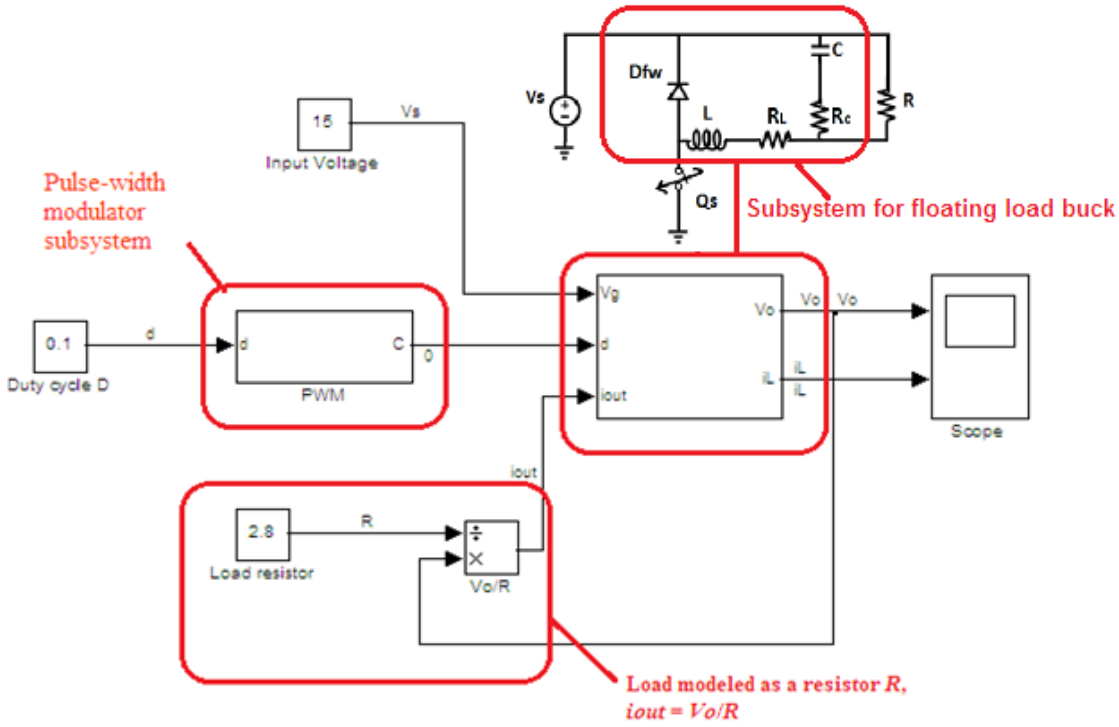


Figure 3.16. Open loop simulation circuit for a floating load buck converter.

Figure 3.16 shows the SIMULINK simulation circuit schematic for an open loop floating load buck converter.

The sawtooth waveform block time value is set to be [0 0.001e-4 1e-4] as shown in Figure 3.17, which indicates that the switching frequency is 10 kHz. Figure 3.18 shows the Pulse-width modulator (PWM) signal model for the floating load buck converter.

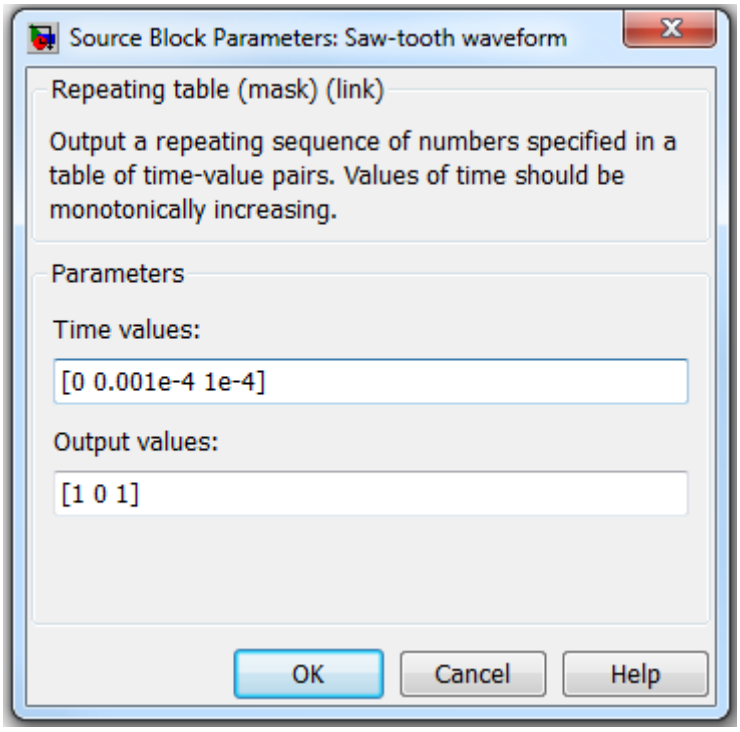


Figure 3.17. Sawtooth waveform block settings.

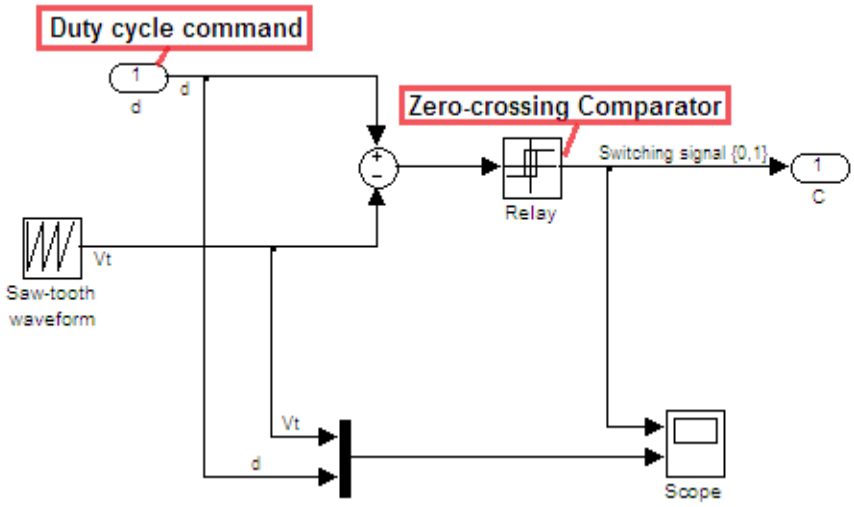


Figure 3.18. Inside the PWM signal model for the floating load buck converter.

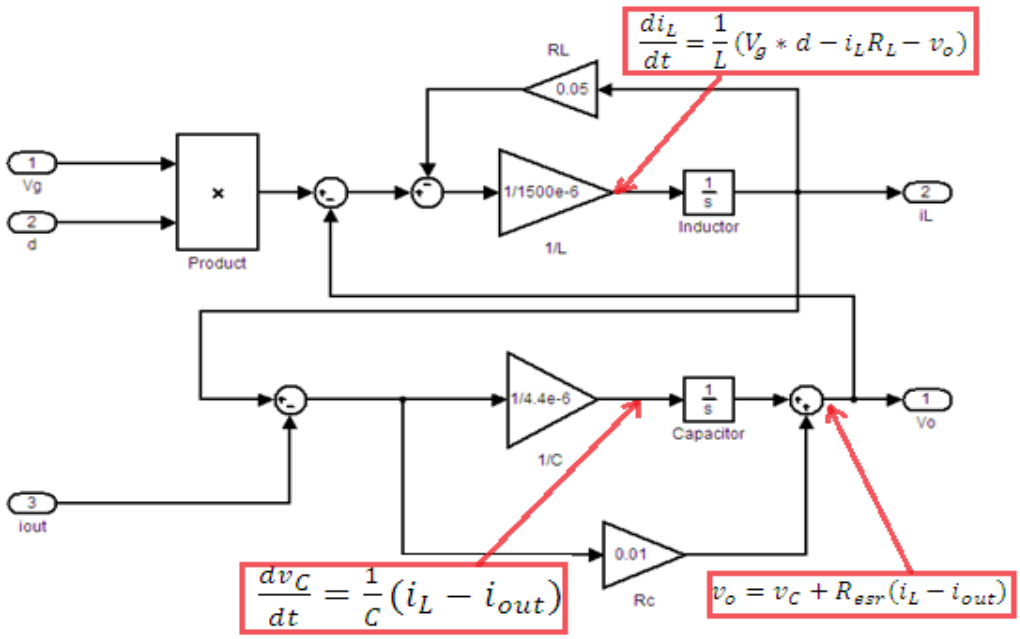


Figure 3.19. Subsystem model for open loop floating load buck converter.

Figure 3.19 shows the subsystem model for the simulated open loop floating load buck converter.

Figure 3.19 shows the output voltage waveform and the inductor current waveform. The average output voltage is around 1.5V, which is correct according to the 10% duty cycle. The current flowing through the inductor shows the continuity of its waveform, which indicates that the floating load buck converter is operating in continuous mode.

The waveforms captured in Figure 3.20 shows the PWM signals and the reference voltage signal compared with sawtooth signal waveforms. As can be seen, the 10% duty cycle can be clearly observed.

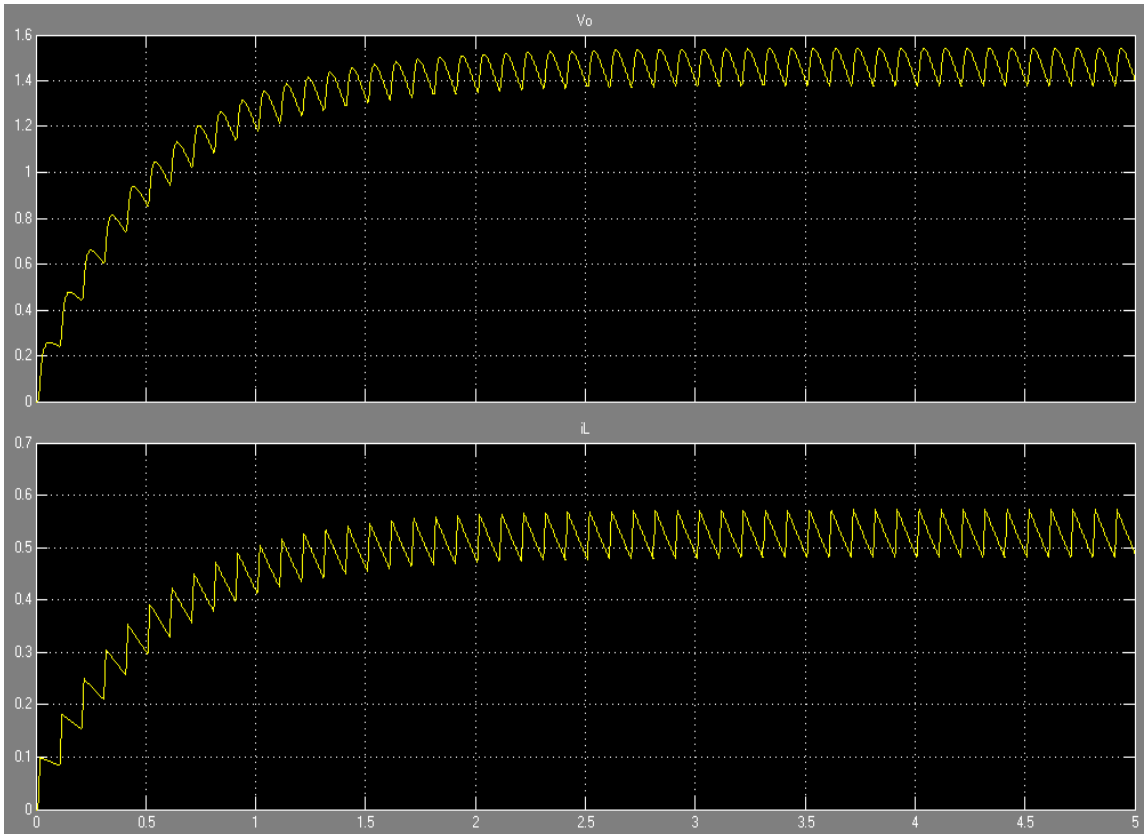


Figure 3.20. Output voltage waveform and inductor current waveform.

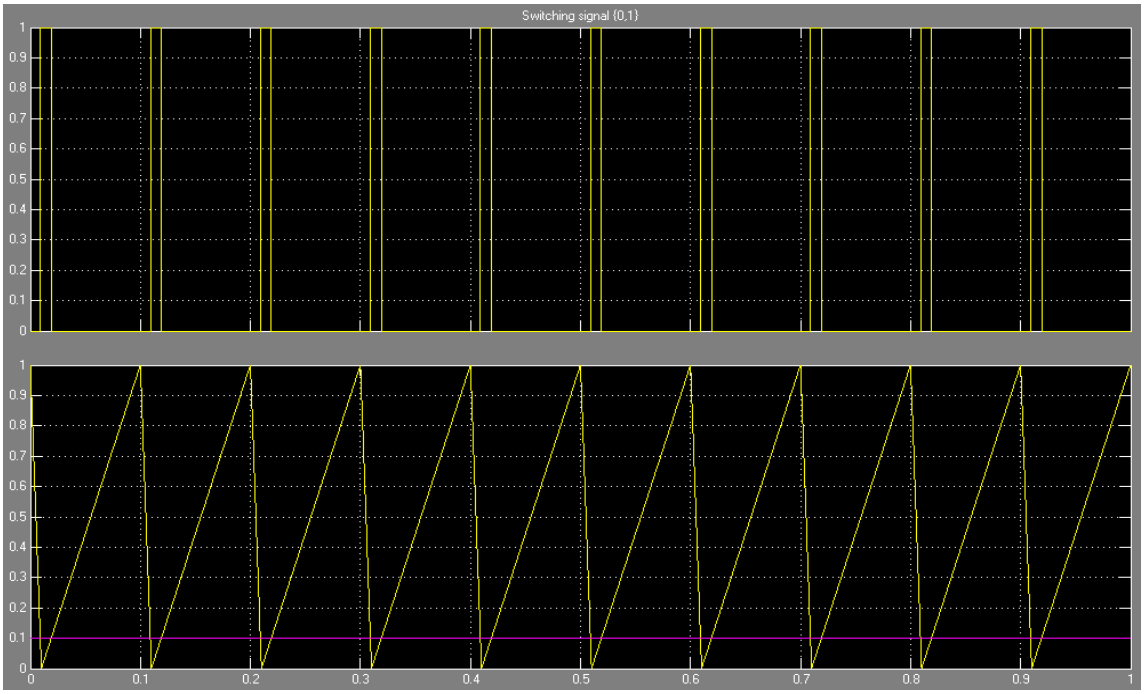


Figure 3.21. PWM signal and sawtooth waveforms.

3.5.2 Comparison with Conventional Buck Converter

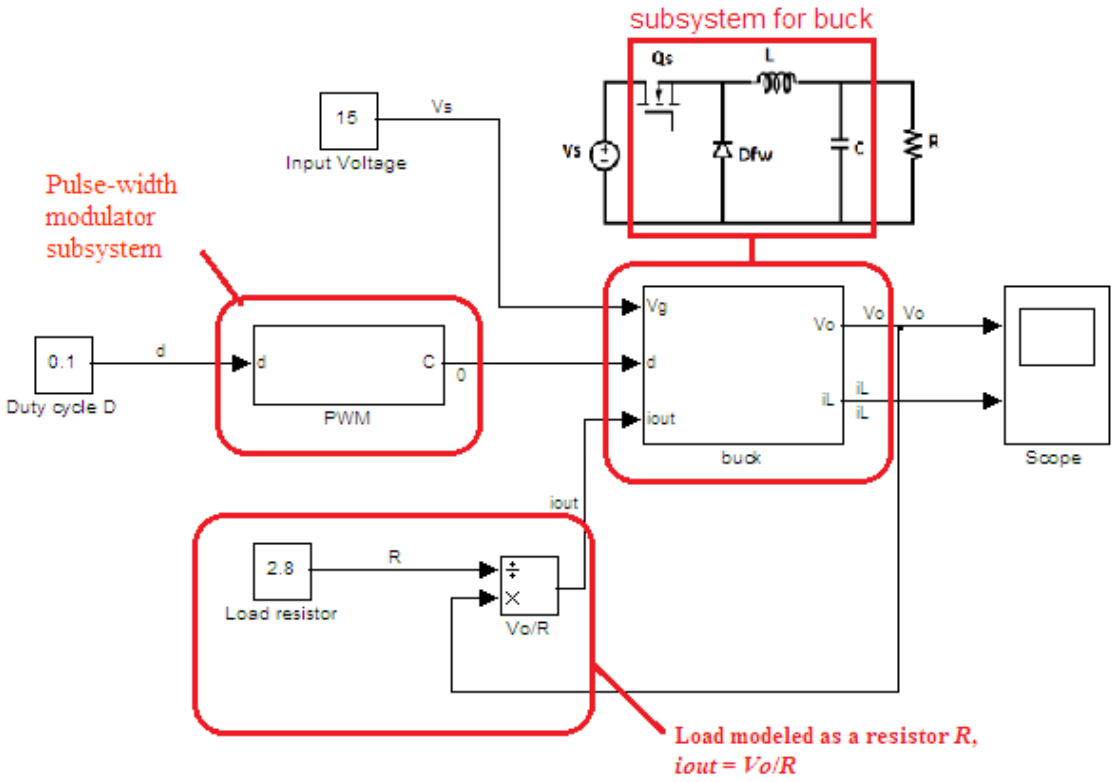


Figure 3.22 Open loop simulation circuit for a conventional buck converter.

Figure 3.22 shows the SIMULINK simulation circuit schematic for an open-loop conventional buck converter. The simulation blocks are indicated in Figure 3.22.

Figure 3.23 shows the Pulse-width modulator (PWM) signal model, which is exactly same as the floating load buck converter as shown in Figure 3.18.

Figure 3.24 indicates what is inside the Subsystem model for the conventional buck converter. Although the conventional buck converter and floating load buck converter have the inductor placed in different position, their subsystem models are exactly the same.

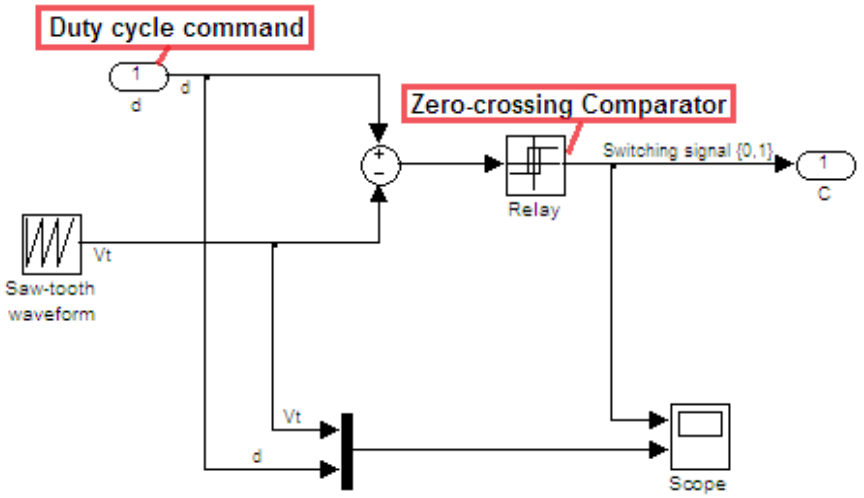


Figure 3.23. Inside the PWM signal model for the conventional buck converter.

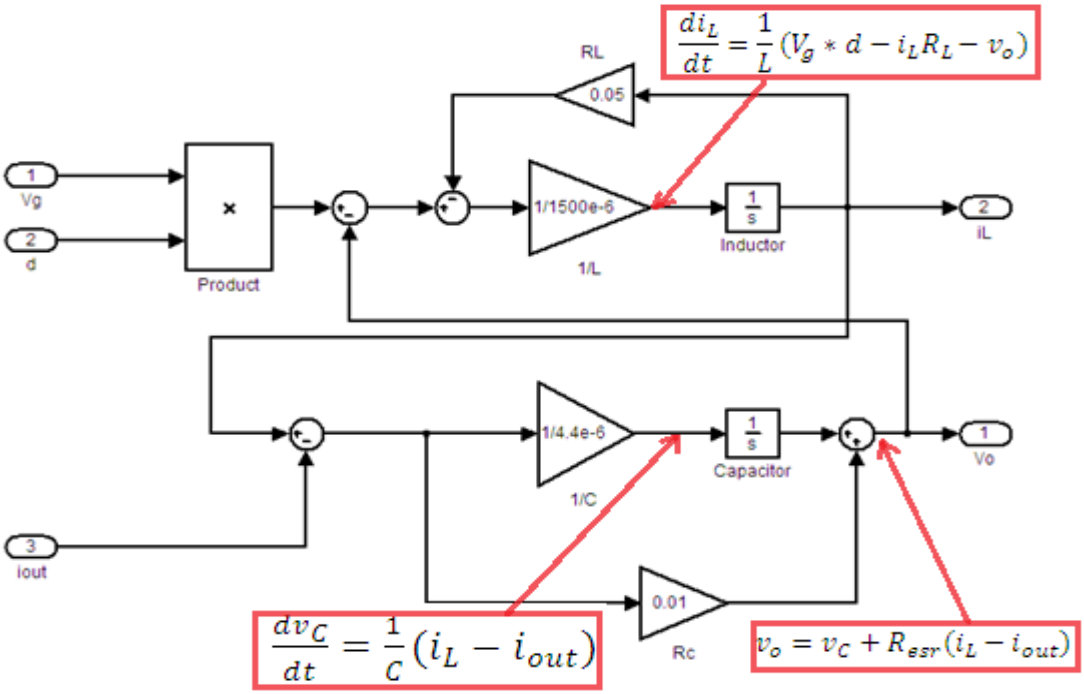


Figure 3.24. Subsystem model for the conventional buck converter.

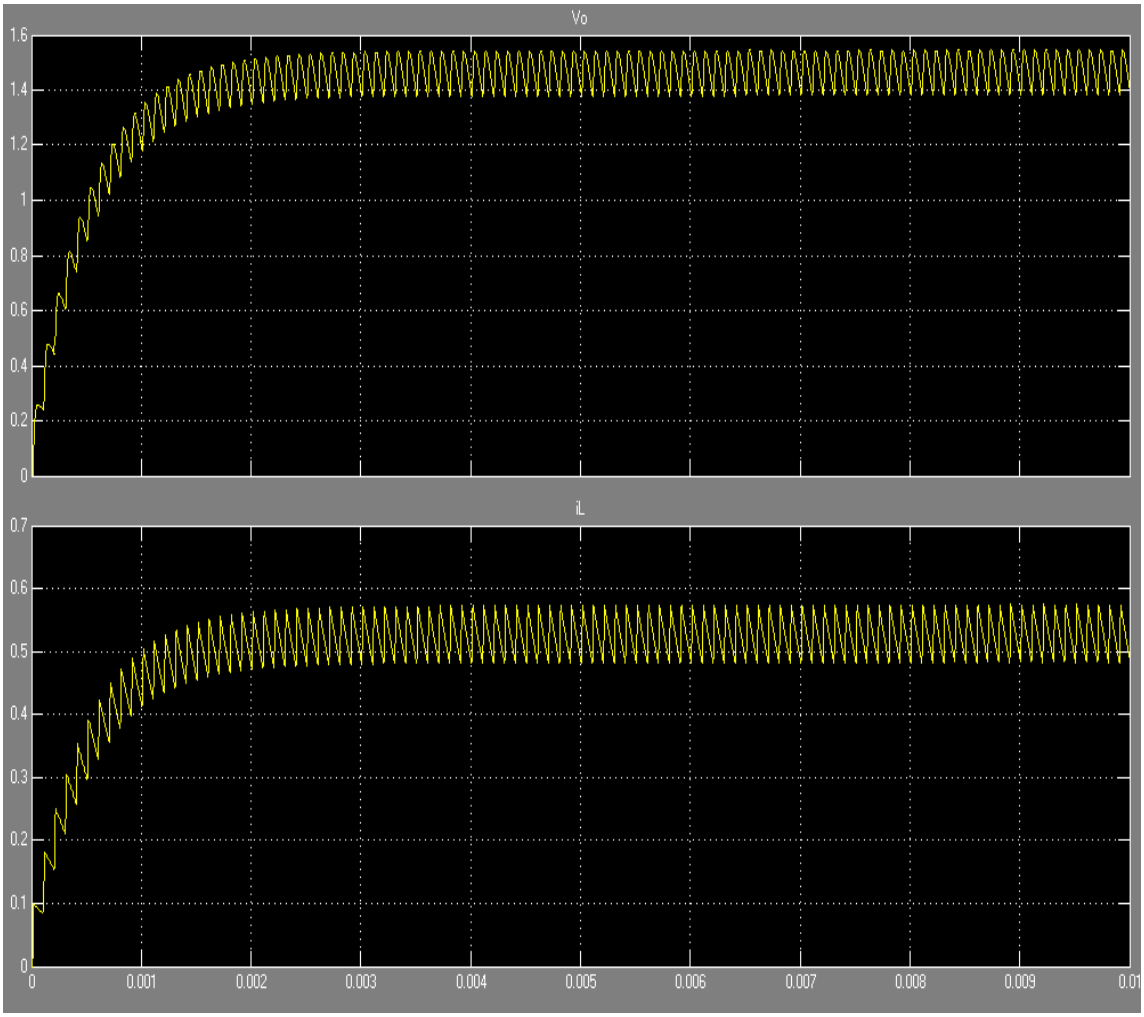


Figure 3.25. Output voltage waveform and inductor current waveform.

Figure 3.25 shows the captured waveforms which shows the average output voltage to be about 1.5V. The inductor current shows that the conventional buck converter is operating under continuous mode.

By using SIMULINK, the function blocks for both the floating load buck converter and the conventional buck converter such as PWM signal model and the subsystem model are exactly the same; as such their simulation results are identical.

3.6 Closed loop Simulation

3.6.1 Floating Load Buck Converter

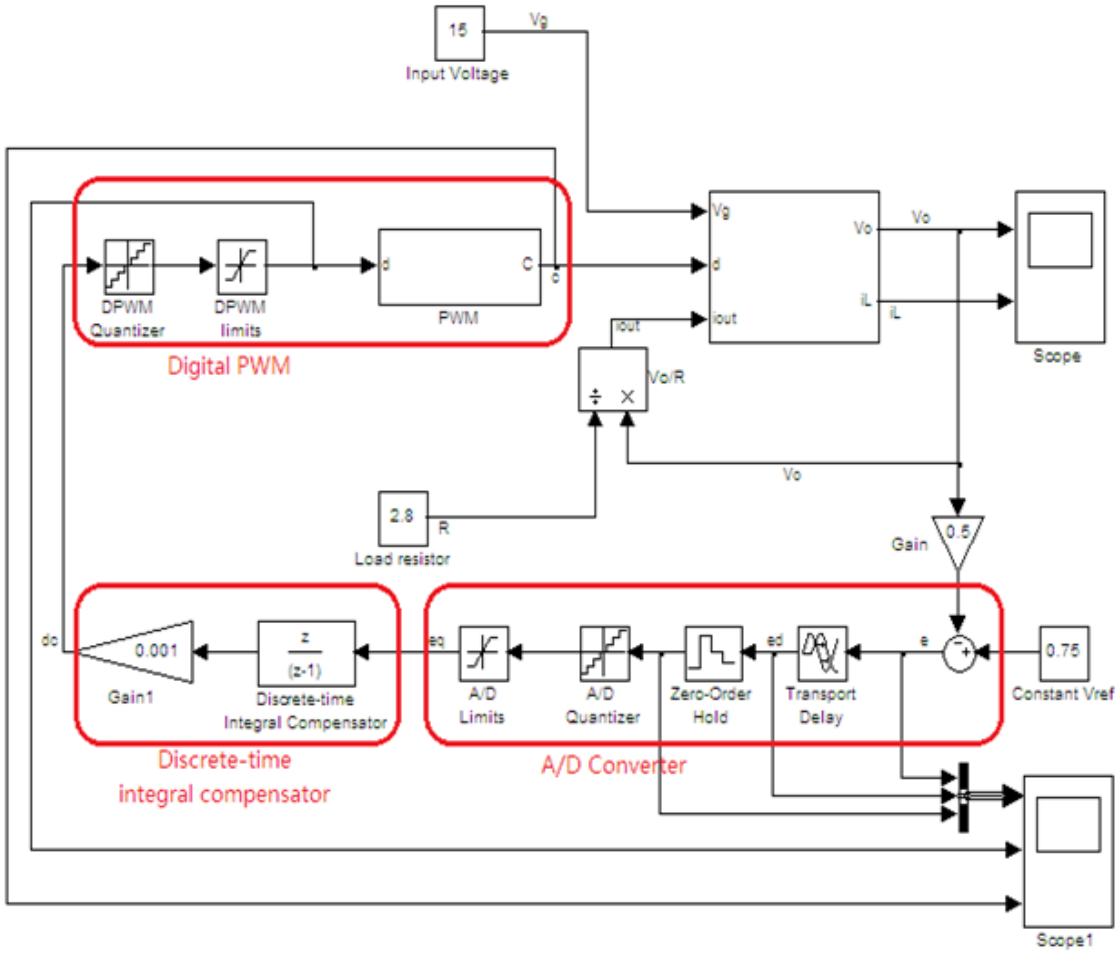


Figure 3.26. Top level system model for digital controlled floating load buck converter.

Figure 3.26 shows the system model for the digital controlled buck converter. The digital controller includes the A/D converter, the Discrete-time integral compensator, and the Digital PWM.

Figure 3.27 shows the output voltage and the inductor current waveforms for the closed-loop floating load buck converter.

Figure 3.28 shows more details on the error signals with error delays, and the duty cycle command DC.

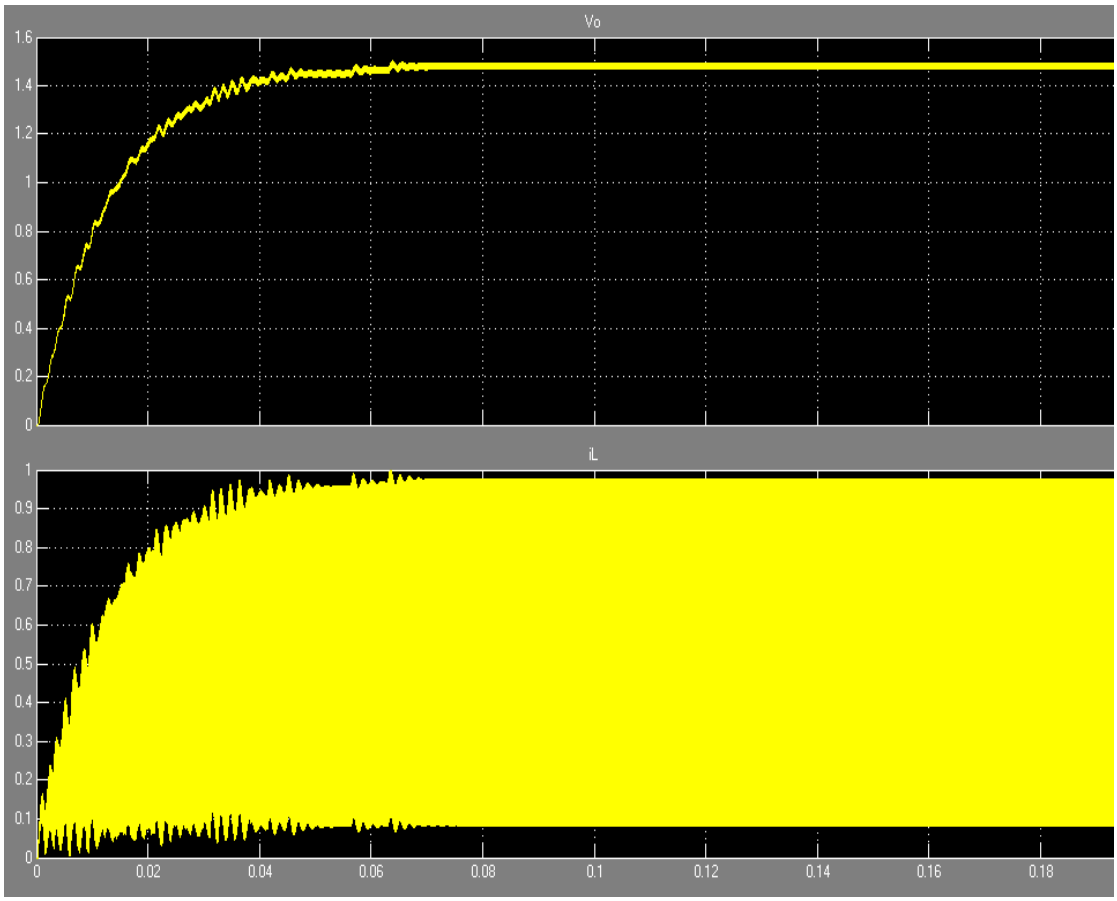


Figure 3.27. Output voltage waveform and inductor current waveform.

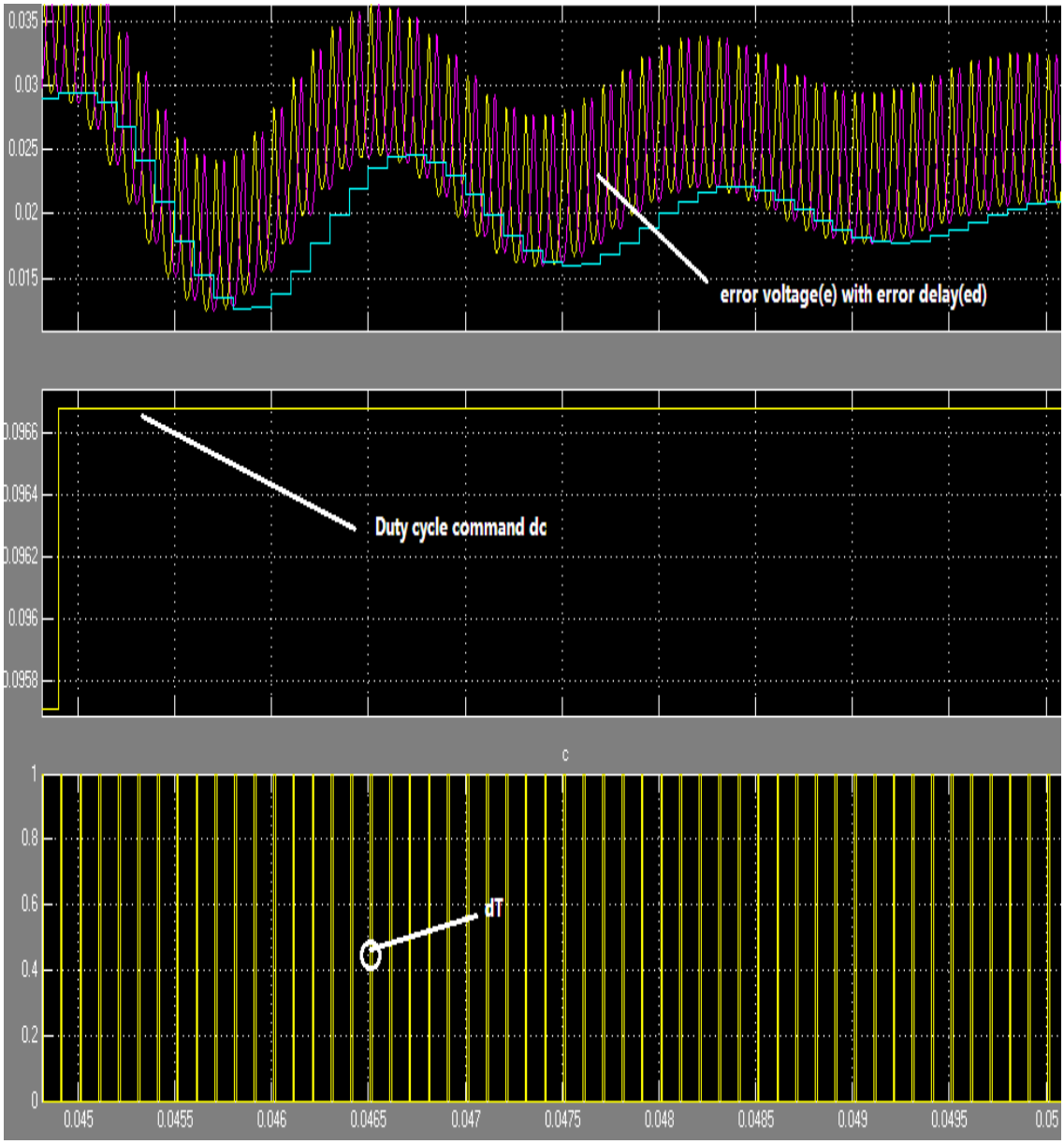


Figure 3.28. Waveform details in the digital controller.

CHAPTER 4

Experimental Results

4.1 Circuit Block Analysis of the TPS92001 Controller

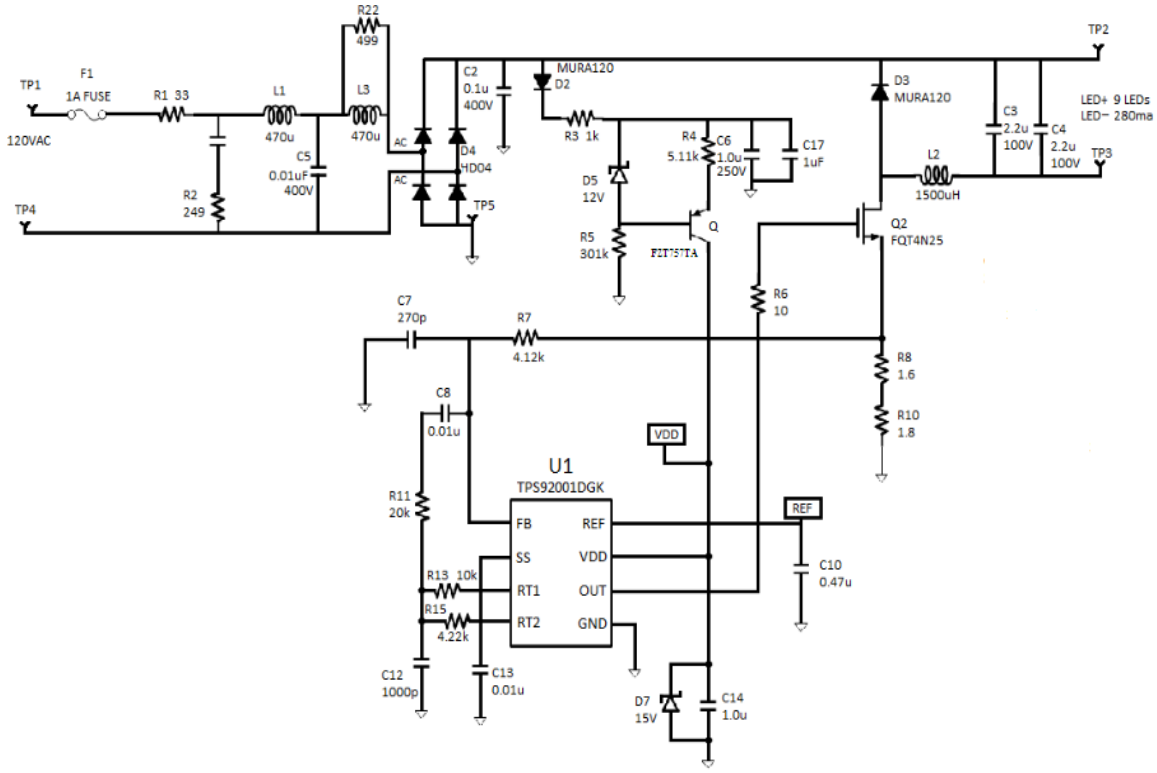


Figure 4.1. Circuit schematic for TPS92001.

Figure 4.1 shows the circuit schematic for the LED driver using a floating load buck converter with a Texas Instruments TPS92001 controller. The input is a 120VAC directly from the AC mains. The inductor L_1 and capacitor C_5 form a filter network with a RC time constant. To control the current flowing through the LEDs, a current sensing resistor is placed in the source circuitry of Q_2.

A bridge circuit consisting of four INHD04 diodes rectifies the Alternating Current (AC) voltage to Direct Current (DC) voltage. By using four diodes, the bridge

rectifier achieves a full-wave rectification. The rectifier circuit converts the 120VAC power source to a DC voltage for the operation of the device. The TPS92001 controller derives its DC power supply from the circuit connected to D_2. C_6 is the decoupling capacitor. In case there will be AC signal superimposed on the DC power line, C_6 can remove these unwanted signals. R_3, D_5 and Q formed a voltage regulator sub-circuit. The R_3 in series with D_5 helps to limit the current, and also improve the voltage regulation. Also, the D_7 12V zener diode connected to the collector circuitry of Q regulates the voltage to maintain a regulated 12V for the TPS92001.

R_5, D_5, R_4 and Q form a voltage regulator for the TPS92001 chip as shown in Figure 4.2. The reason for using a voltage regulator instead of a simple resistor to supply the chip is to maintain a constant supply voltage despites a large change in the AC main voltage.

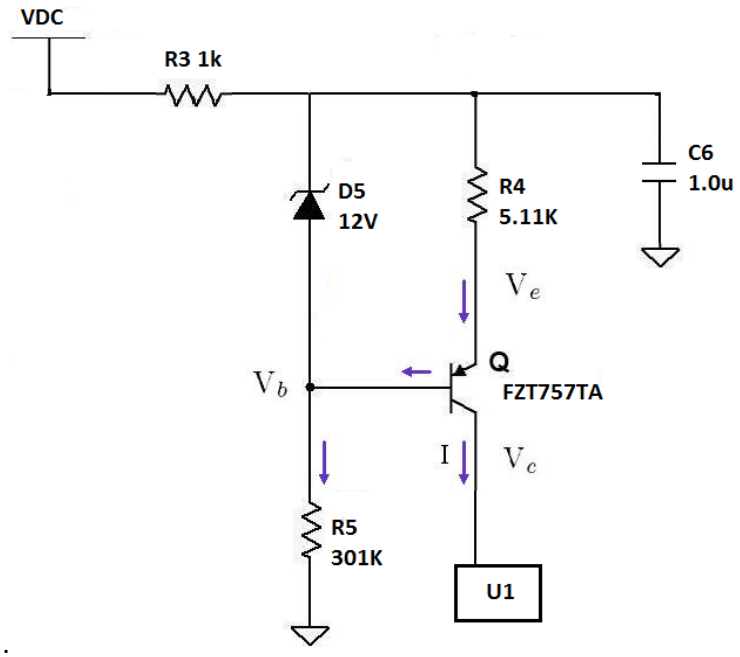


Figure 4.2. Voltage regulator formed by R_5, D_5, R_4 and Q.

For an input AC of 63V, the rectified DC supply is $63V \times \sqrt{2} = 89.10V$, so the input DC is about 89V. The FZT757TA PNP transistor has a β (h_{FE}) value about 50 [11]. The voltage dropped at the zener diode is around 12V. So, the voltage dropped on R3 is

$$V_{R3} = 89V - 12V - I_{BQ}R_5 \tag{4-1}$$

The base-emitter loop yields,

$$12V = I_{EQ}R_4 + 0.7V \tag{4-2}$$

$$I_{EQ} = \frac{12 - 0.7}{5.11K} = 2.2114mA \tag{4-3}$$

So,

$$I_{BQ} = \frac{I_{EQ}}{\beta} = 0.0442mA \tag{4-4}$$

$$V_{R3} = 89V - 12V - 0.0442mA * R_5 = 63.70V \approx 64V \tag{4-5}$$

$$V_C = 89V - 64V - I_{EQ} * R_4 - 0.7V = 12.99V \approx 13V \tag{4-6}$$

As the calculations shown above, the voltage regulation supply a voltage about 13V for the TPS92001 chip without consideration of any power losses.

4.2 Functional Blocks of TPS92001 Controller [8]

For a switching mode power converter, the PWM controller contains control and drive circuitries. The PWM controller TPS92001 inside the circuit shown in Figure 4.1 not only generates the PWM signals on the gate pin, but also performs current regulation through the current sensing. This general purpose LED lighting PWM controller supports both isolated and non-isolated topologies. The functional block diagram for the TPS92001 controller is shown in Figure 4.3.

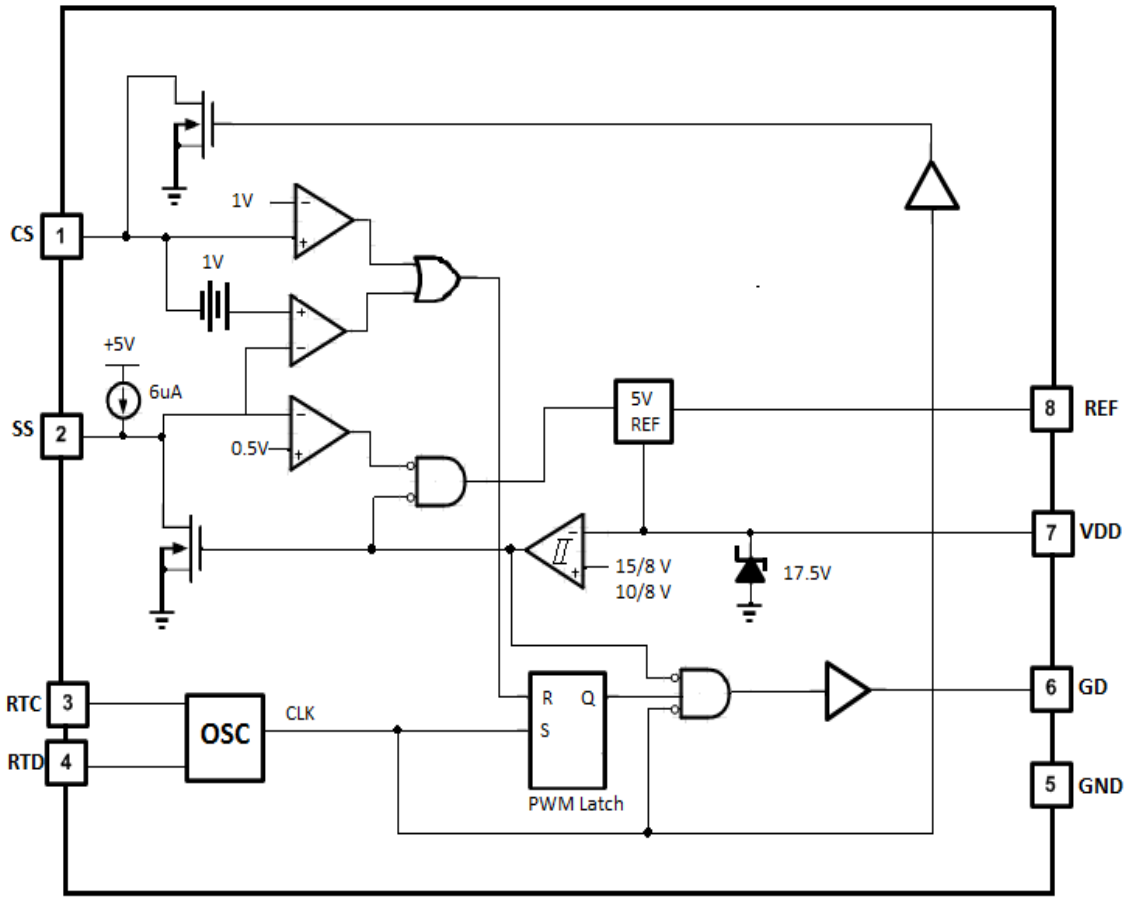


Figure 4.3. Function blocks inside the TPS92001.

Pin“CS” also called pin “FB” is the summing node for the sensing feedback signals and slope compensation. As shown in Figure 4.1, the voltage at the capacitor C_7 is

discharged by the internal NMOS transistor during the PWM off time. Pin“SS” is pin for the soft start. A capacitor C_{13} is connected to this node. This capacitor is being charged by the internal 6μA current source as shown in Fig 4.3. Pin “VDD” and pin “GND” are the supply input voltage and ground, respectively for the chip. Pin “GD” is the high current driver output. Pin “RTC” and pin “RTD” generate a sawtooth waveform through an oscillator network. By changing several resistor and capacitor components values, the duty cycle for the output driver pin GD can be changed. As shown in Figure 4.1, R_{13}, R_{15}, and C_{12} connected to these pins determine the switching frequency and the duty cycle for the floating load buck converter. Depending on the input voltage V_{ss}, there are three cases [8]:

Case 1. When V_{ss} < 0.5V,

As shown in Figure 4.4, for the initial start point, the V_{ss} at pin “SS” is less than 0.5V. This voltage is compared with a 0.5V in Part A, and the output of the comparator yields a logic “High” to the input of the NAND gate. Consequently, the output for the NAND gate gives a logic “Low” as an input signal to the 5V reference voltage source, so the pin ”REF” has an output signal “Low”. As shown in Part B, the V_{ss} is also compared with a 1V voltage, so it gives a logic “High” to the OR gate, which yields a logic “High” to reset input of the PWM Latch.

“VDD” pin provide an under voltage lockout function for this chip. If the supply voltage VDD is less than 15/8V or 10/8V, the Schmit trigger will output logic “High”. This goes to Part C, through the NAND gate, the pin “GD” will stay low, so the chip will

not function. Also, the output signal “Low” from the Schmit trigger will disable the NMOS in PartD.

However, if the “VDD” pin receives the correct power supply voltage, it will trigger the Schmit trigger to output a logic “Low”. When this signal goes to Part C, as mentioned before, the reset pin has a logic “High” so the output Q is logic “Low”, then the output to pin “GD” will be low.

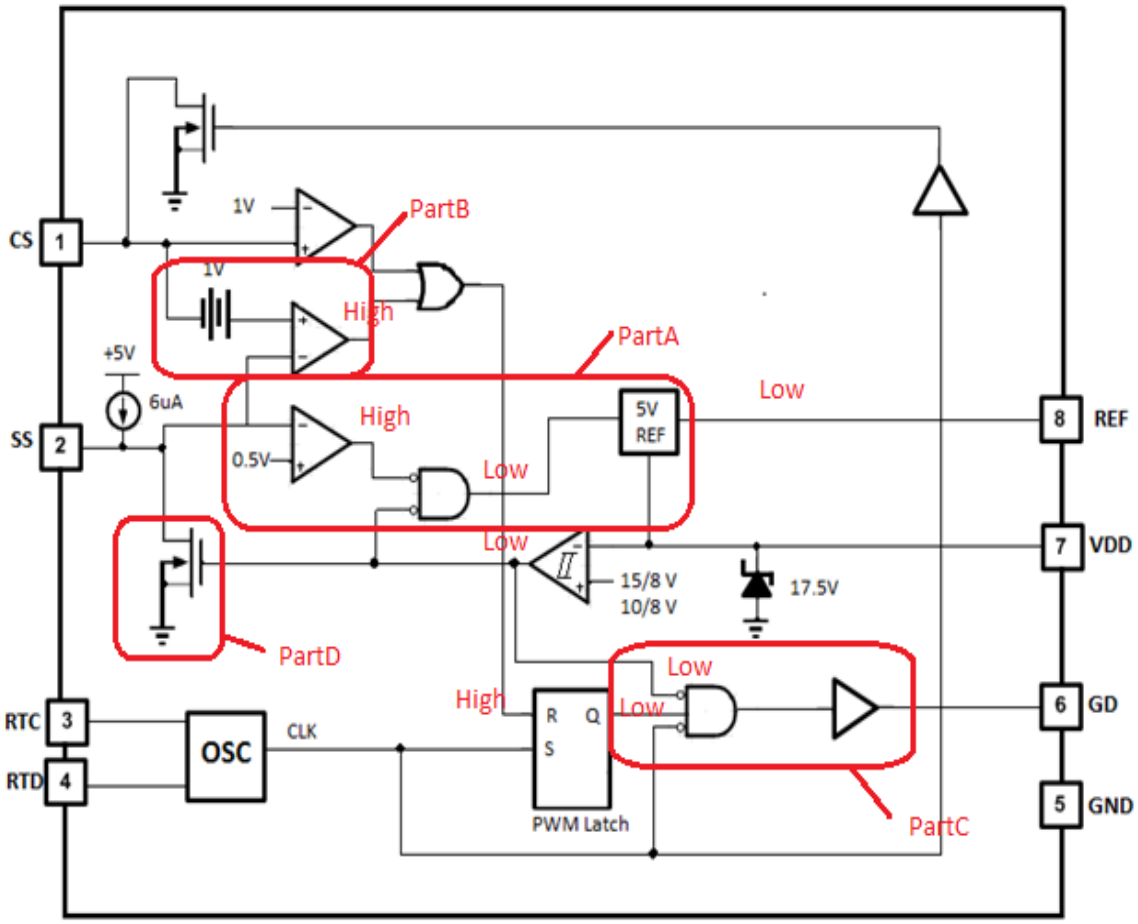


Figure 4.4. Initial start point inside the TPS92001.

In this case, although the oscillator will still function, but the output signal from the “GD” pin remains low.

Case 2. When 1V < V_{ss} < 0.5V,

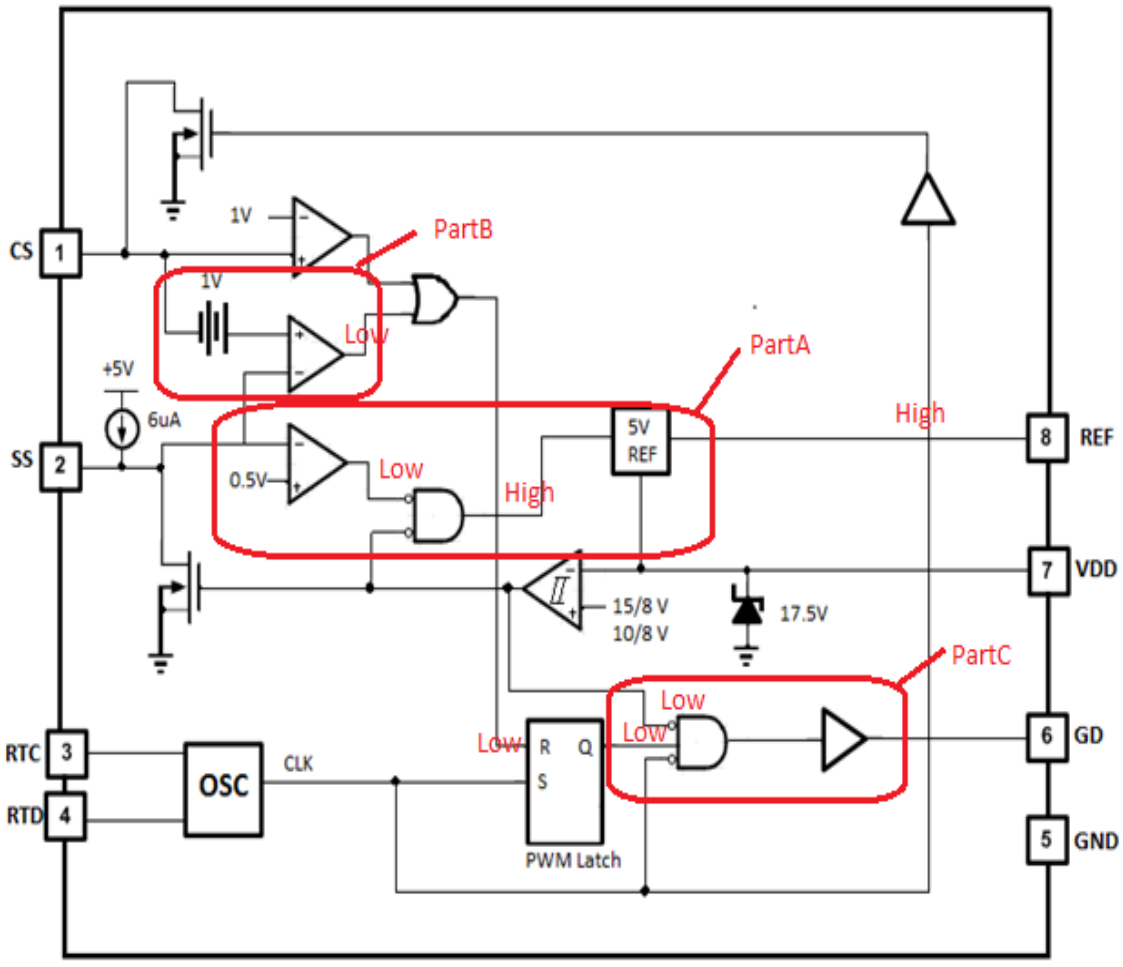


Figure 4.5. When 1V < V_{ss} < 0.5V, inside the TPS92001.

The C_{13} is charging up by the internal 6μA current source at the "SS" pin, so the V_{ss} is increasing. When V_{ss} increases to above 0.5V but less than 1V, this is the second time period.

At first, the signal is compared with the 0.5V in Figure 4.5 Part A, it gives an output logic "Low" for the input to the NAND gate. Then, the output for the NAND gate gives a logic "High" as an input signal to the 5V reference voltage source, so the "REF"

pin yield a 5V reference signal. As shown in Part B, the V_{ss} is also compared with the 1V, so it gives a logic “low” to the OR gate, which yields a logic “low” to the reset pin of the PWM Latch, enabling the PWM signals.

Case 3. When Vss > 1V,

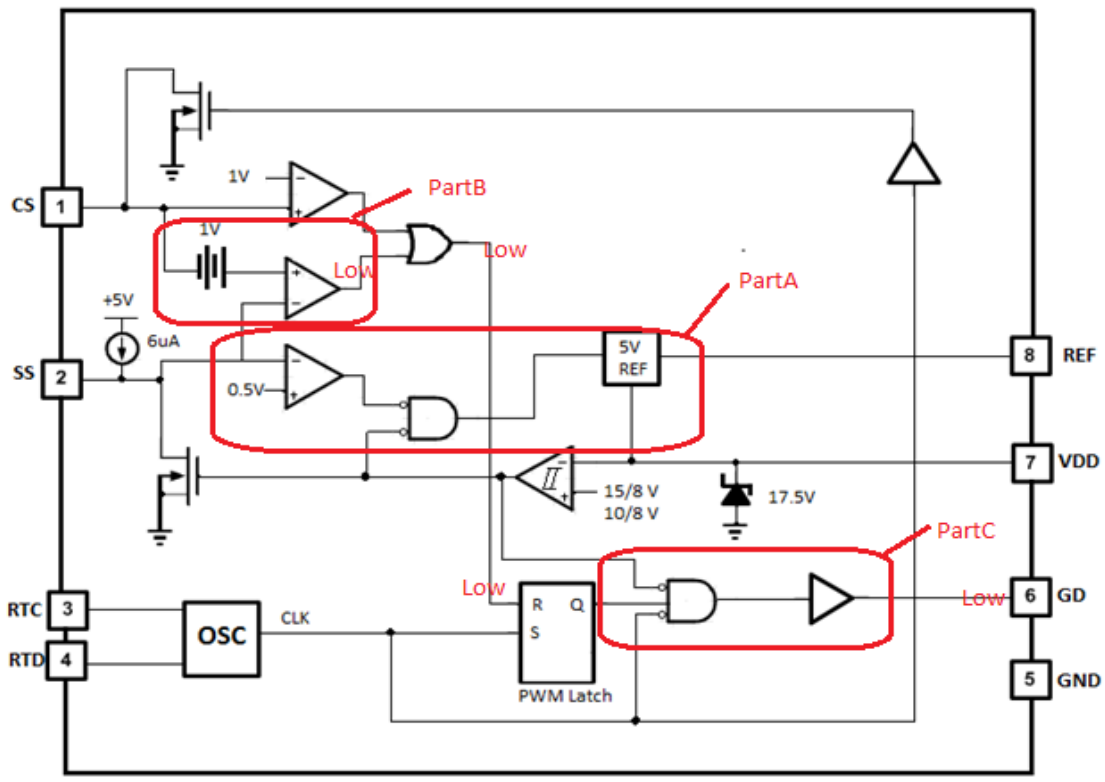


Figure 4.6. When V_{ss} > 1V, inside the TPS92001.

When Vss is greater than 1V, this signal is first compared in Part B, the output from the comparator gives a logic “Low”, it passes through the OR gate, giving a logic “Low” to the reset pin of the PWM Latch. If the voltage at pin “CS” exceeds the 1V threshold voltage, it will reset the PWM latch and modulates the “GD” pin on-time to zero.

4.3 Characterization of the floating load buck LED driver

The TPS92001-based floating load buck LED driver was prototyped and characterized. For safety reasons, an isolated AC main input of 63V was used. An isolation transformer was connected to the AC mains, the input of the inverting buck LED driver was connected to a variable transformer. The load consists of seven 1-W white LEDs with a rated current of 350mA.

A. Gate Drive Signal

Figure 4.7 shows the test circuit for the testing of the gate drive signal.

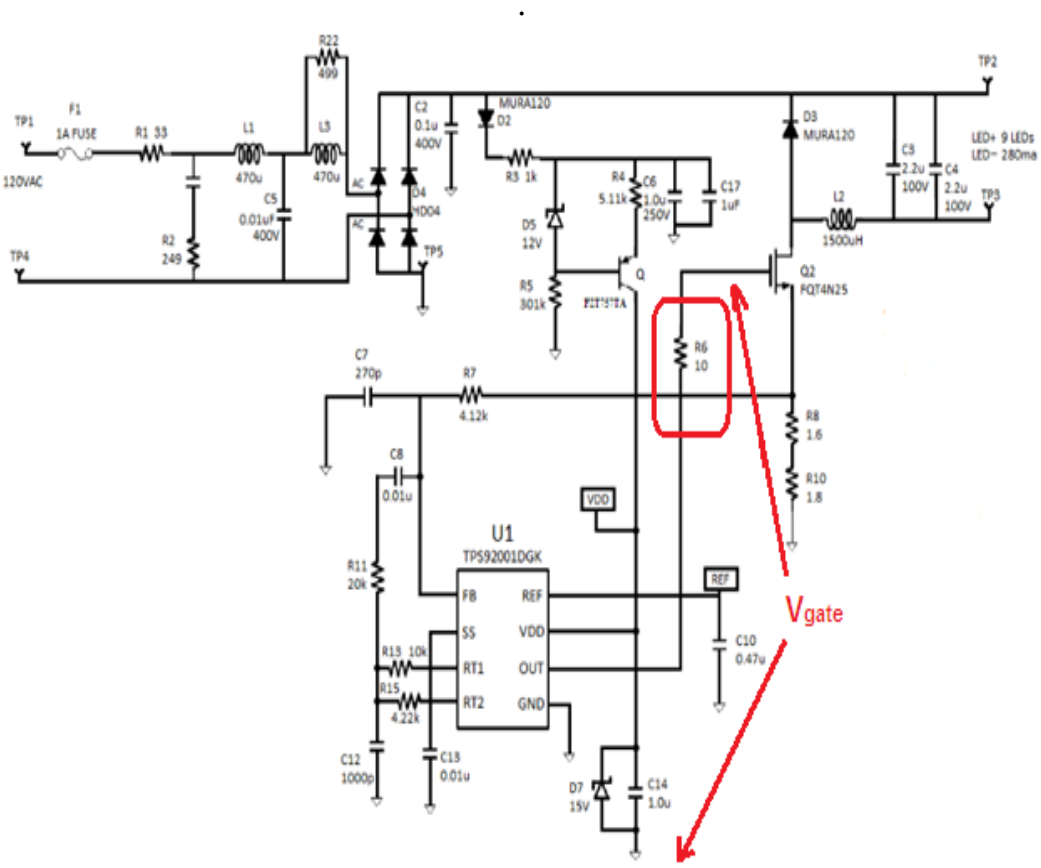


Figure 4.7. Test circuit at R6 for gate drive signal.

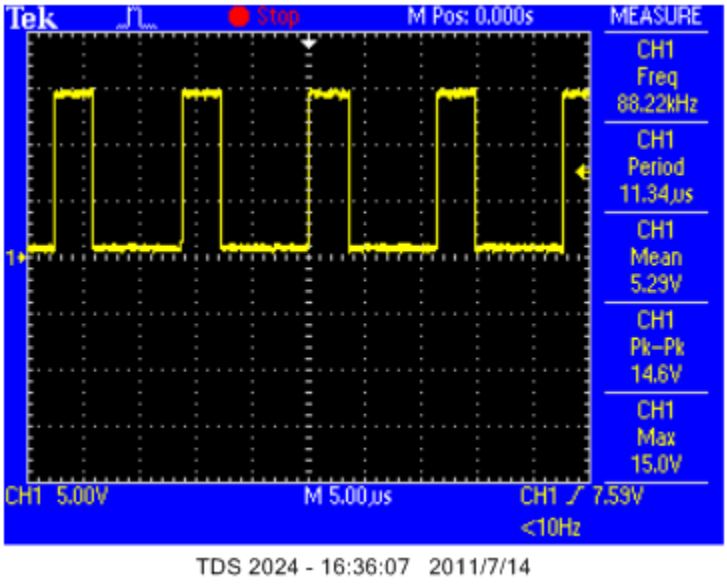


Figure 4.8. Gate signal output captured on R6.

Figure 4.8 shows the switching waveform for the gate signal. As can be seen, the switching frequency is around 88kHz with a duty cycle D of about 27.3% when the AC main is 63V with a load current of 117mA. The amplitude of the gate signal is about 15V. The experiemtal waveforms obtained are very similar to the simulated waveforms shown in Figure 3.15 (a).

B. Current-sensed Signal

The node voltage between the source of the switching tansistor Q_2 and the current-sensed resistor(R_8 and R_{10}) shown in Figure 4.9 represents the current-sensed voltage. The current flowing through the LEDs is approximately $V_{sense}/(R_8+R_{10})$.

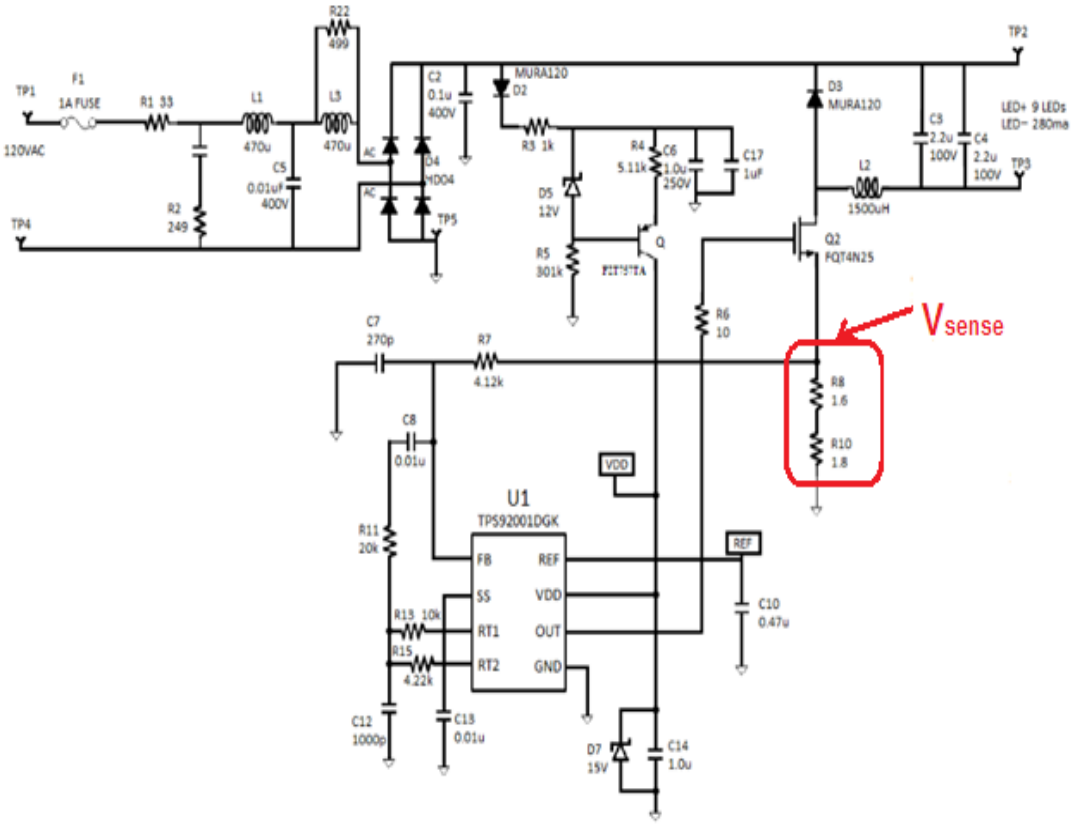
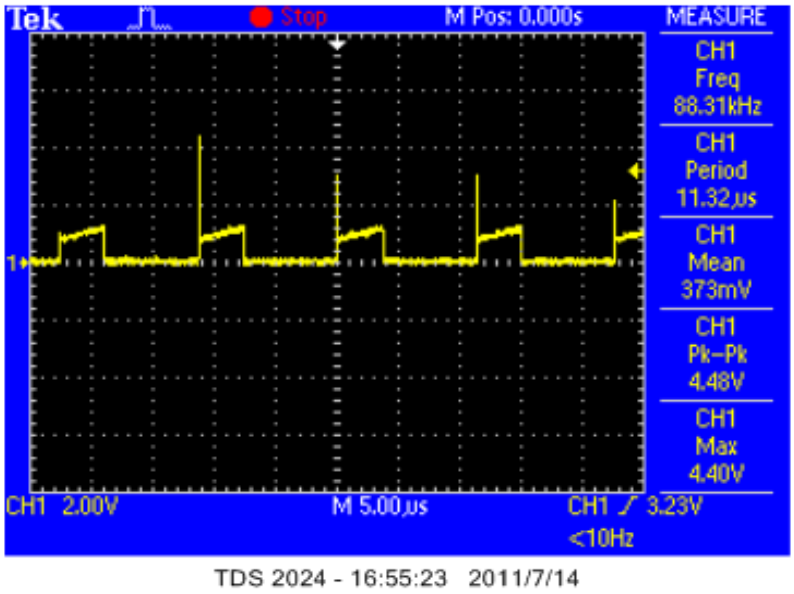


Figure 4.9. Test circuit for the current-sensed signal.

From Figure 4.10, a peak value current of 4.40V/(1.6Ω+1.8Ω) = 623.53mA was measured. The current-sensed signal increases approximatly from 300mV to 600mV. This indicates that the LEDs current varies from 88 mA to 176mA as the power switching transistor is switched on. The duty cycle is about 27.3%. The spikes are due to the inductive kicks during switching. The experiemtal waveforms obtained are very similar to the simulated waveforms shown in Figure 3.15 (b).



.

Figure 4.10. Waveforms for the current-sensed signal.

C. Feedback pin FB signal

As can be seen in Figure 4.11, the feedback pin of the TPS92001 controller is connected to the current sense resistors (R_8 and R_{10}) and the source of the switching tansistor Q_2. R_{11} and C_8 couple the sawtooth signal to the feedback "FB" pin. The current-sensed signal adds to this signal at the "FB" pin. So that a 1V-threshold is obtained. Above 1V, the TPS92001 controller triggers and resets the PWM latch. Capacitor C_7 serves as a filtering capcacitor to remove the current spike shown in Figure 4.10.

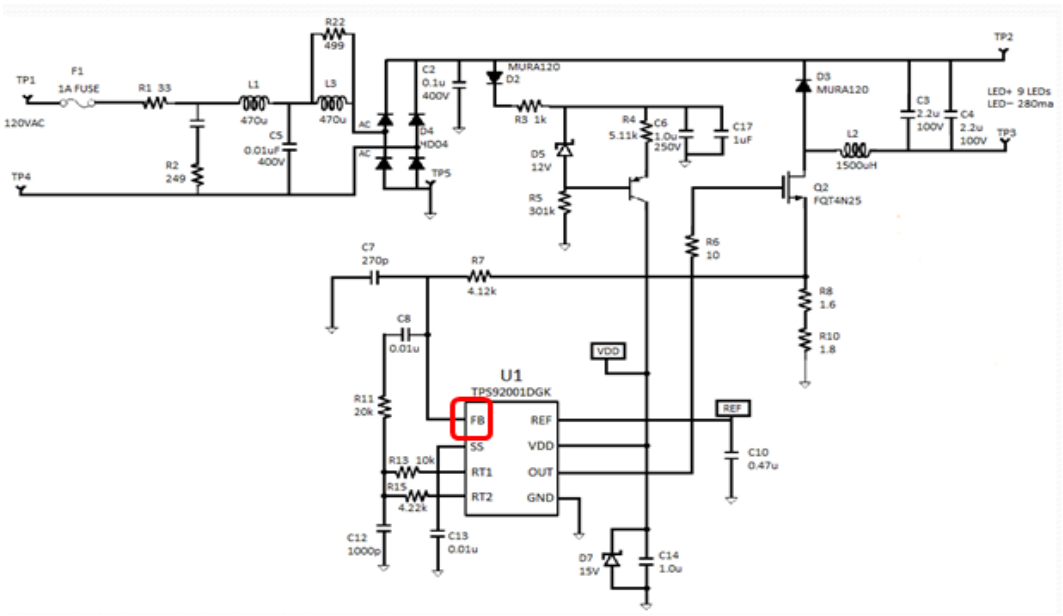
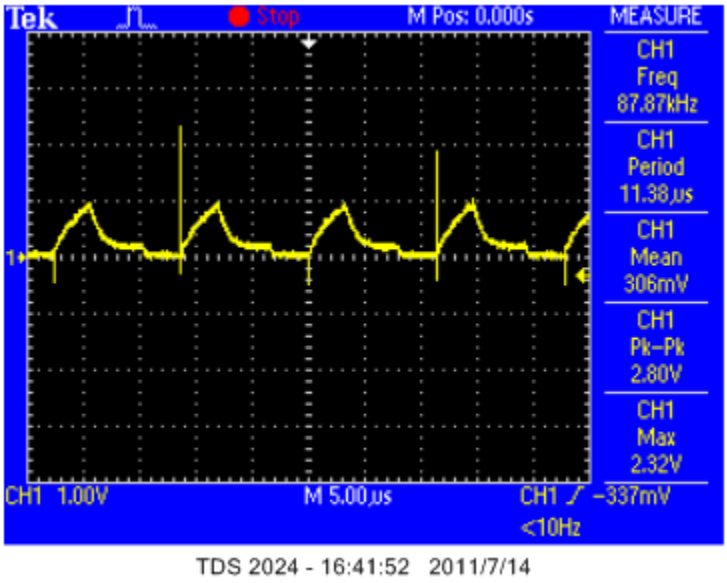


Figure 4.11. Test circuit for the Feedback pin signal.



.

Figure 4.12. Waveforms for the Feedback pin signal.

Figure 4.12 shows the feedback signal on “FB” pin. The experiemtal waveforms obtained are very similar to the simulated waveforms shown in Figure 3.15 (c).

D. Oscillator Signal of TPS92001.

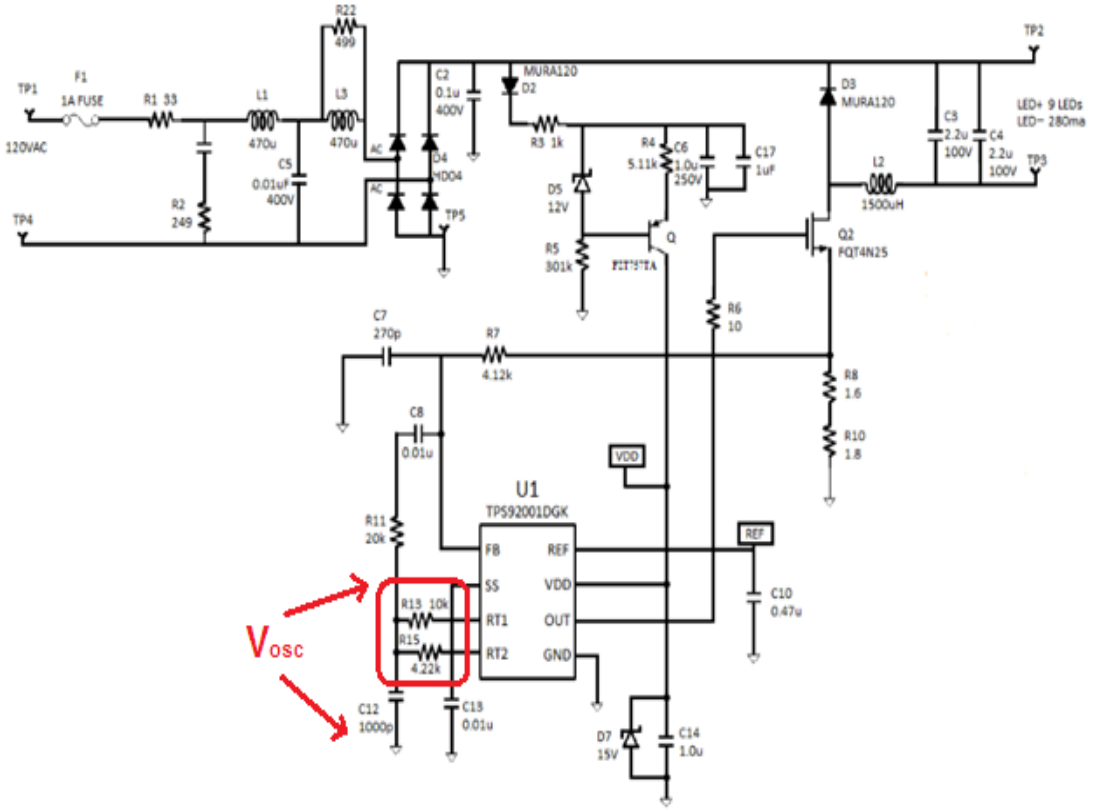


Figure 4.13. Test circuit for the oscillator signal.

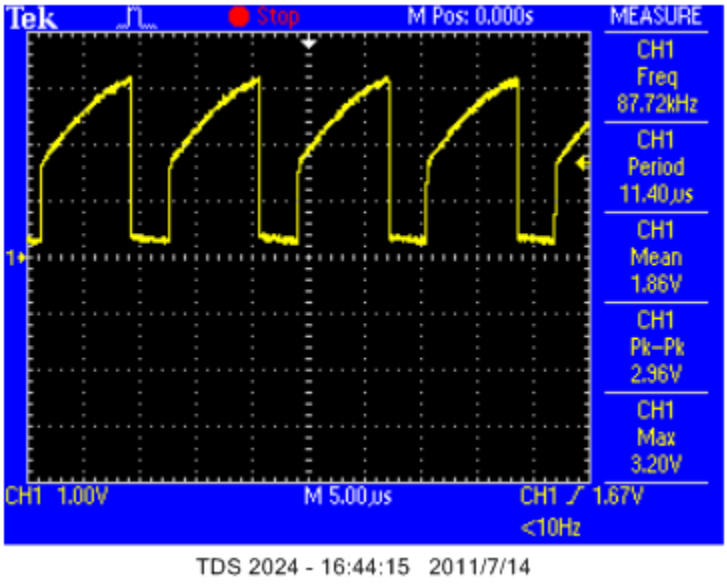


Figure 4.14. Waveforms for the oscillator signal.

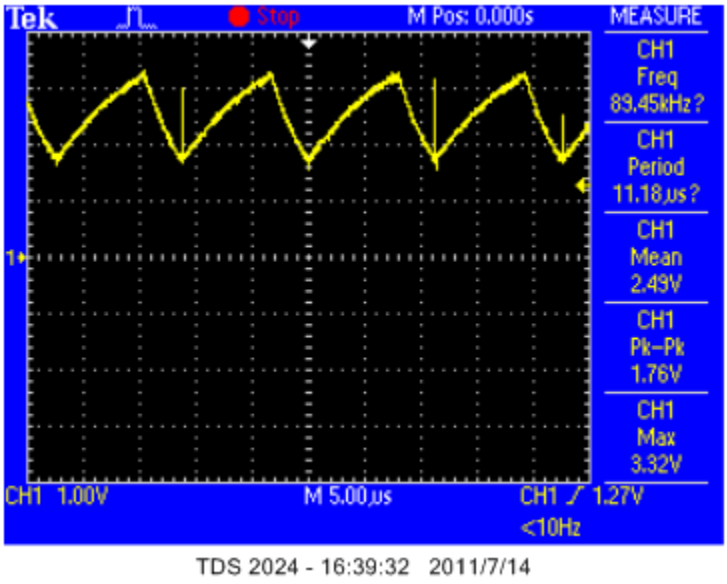


Figure 4.15. Sawtooth signal from R_{13}.

Figure 4.13 shows the measurement circuit for the oscillator signal of the TPS92001.

The waveforms shown in Figure 4.14 are the signals captured from the oscillator from Pin “RT2” on TPS92001 chip. As can be seen in Figure4.14, the oscillator signal is a sawtooth with a peak-to-peak value of 1.76V and an oscillator frequency of 89kHz, which is very close to the caclulated switching frequency of 93kHz. The discrepancy in switching frequency is due mainly to the differences of the component values used in the simulation and actual circuit implementation. The experiemtal waveforms obtained in Figure 4.14 are very similar to the simulated waveforms shown in Figure 3.15 (d).

E. Free-wheeling Diode

Figure 4.16 shows the test circuit for the free-wheeling diode. Figure 4.17 shows the signals from the switching diode D3 on the main circuit. The free-wheeling diode

switches on when Q_3 is off. It shows the average input DC voltage is around 84V after it passed through the bridge rectifier and the filter net work. The maximam DC voltage can go up to 90V. The calculation shows that with an input AC of around 63V, the rectified output DC supply is to be around 89V without considering all the losses.

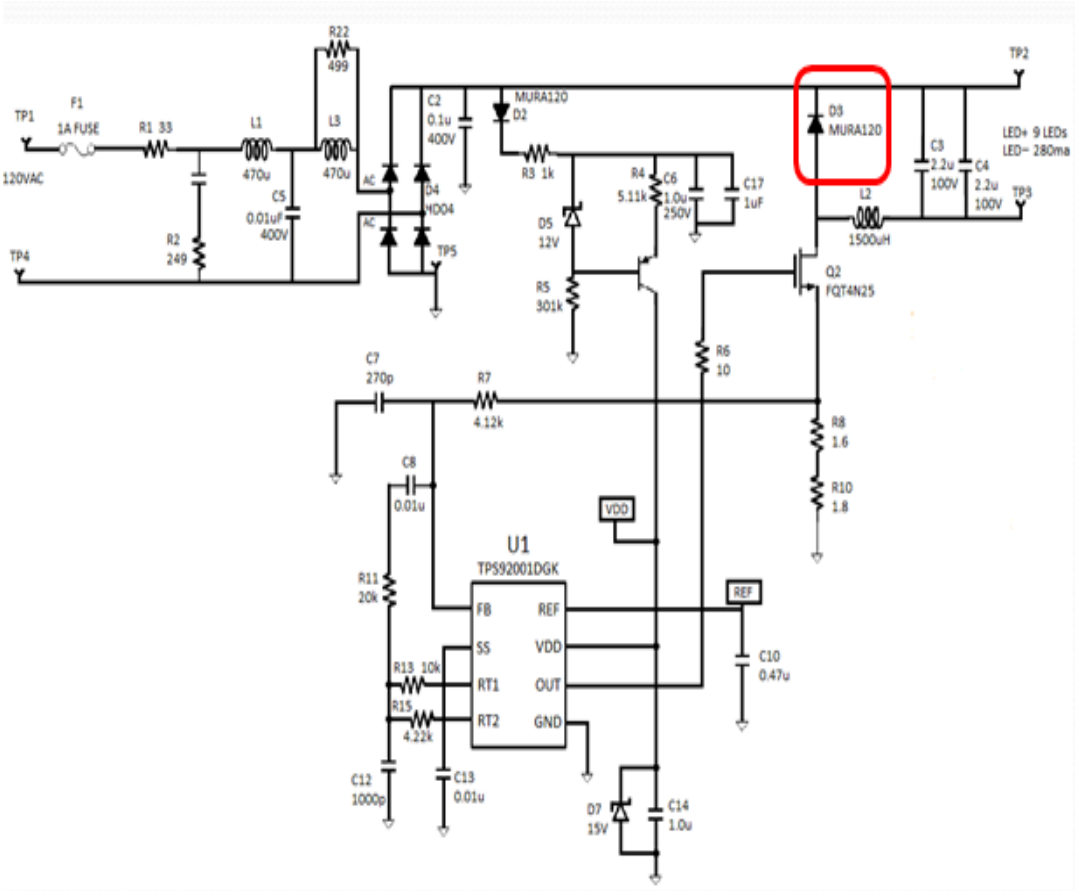


Figure 4.16. Test circuit for free-wheeling diode.

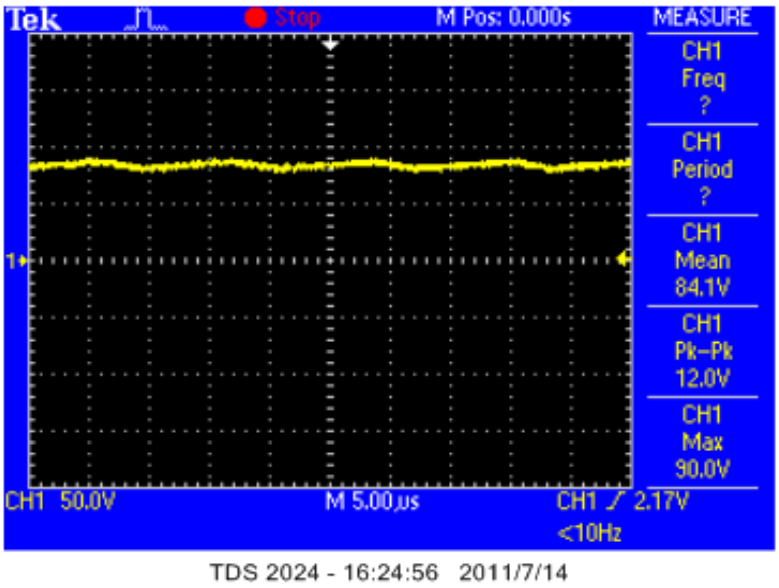


Figure 4.17. Waveforms for free-wheeling diode.

F. Signal from the drain of swtich transistor Q_2

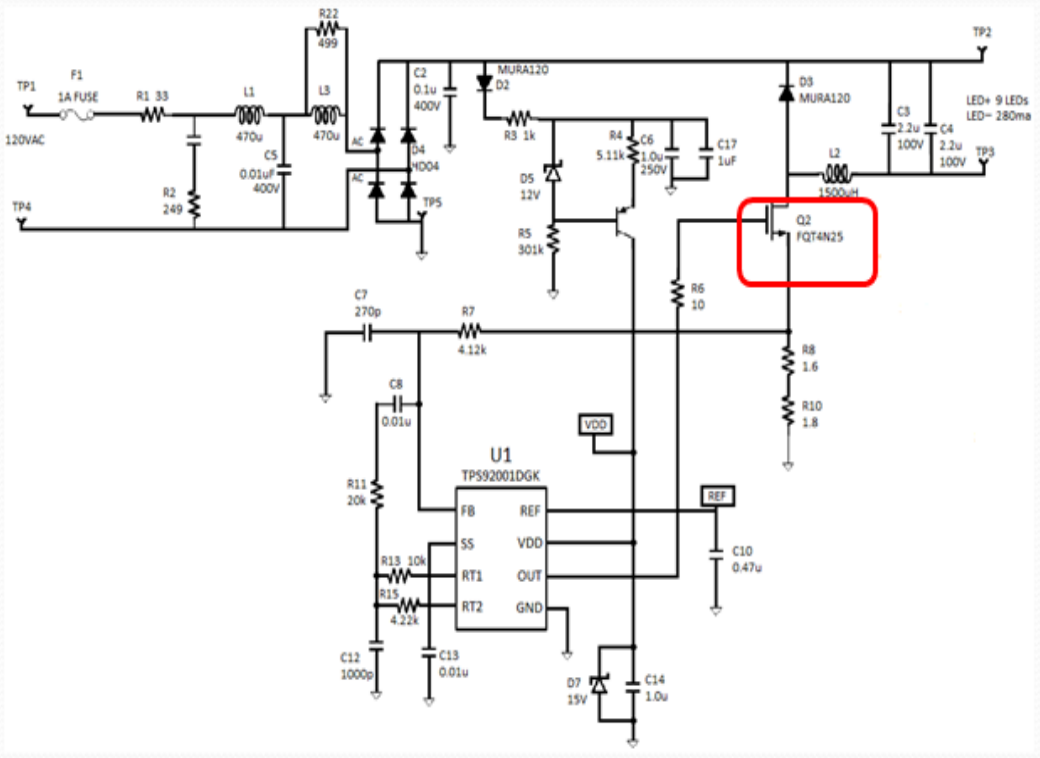


Figure 4.18. Test circuit for the drain of FQT4N25.

Fig 4.18 shows the test circuit for the drain voltage of the switching transistor Q_2.

Fig 4.19 shows the voltage waveform at the drain of Q_2 with the switching frequency is about 89kHz. When the switch is on, the drain voltage is near zero. However, when the switch is off, the drain voltage is above 78V. The experiemtal waveforms obtained are very similar to the simulated waveforms shown in Figure 3.15(e). A duty cycle about 73% is indicated. Similarly, the experiemtal waveforms obtained in Figure 4.19 are very similar to the simulated waveforms shown in Figure 3.15 (e).

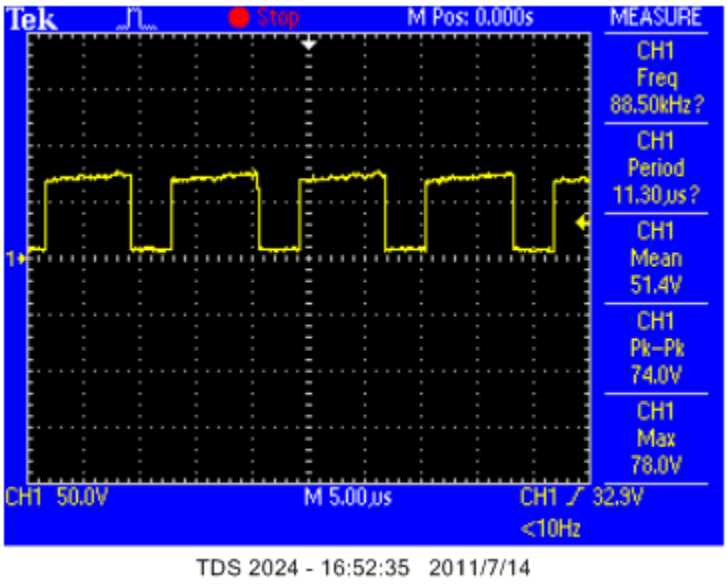


Figure 4.19. Waveforms for the drain signal of FQT4N25.

G. Reference voltage on TPS92001D

Figure 4.20 shows the test circuit for the pin “REF” on TPS92001D. The reference signal shown in Figure 4.21 is a constant DC voltage of 5V which indicates that the chip is function correctly.

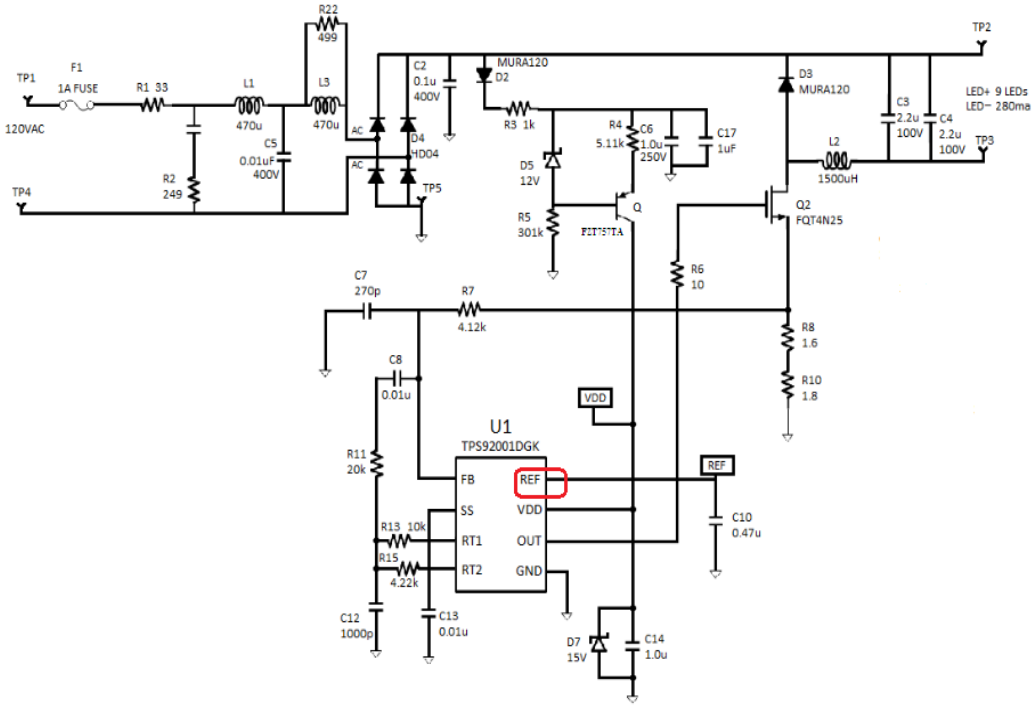


Figure 4.20. Test circuit for the Reference pin signal.

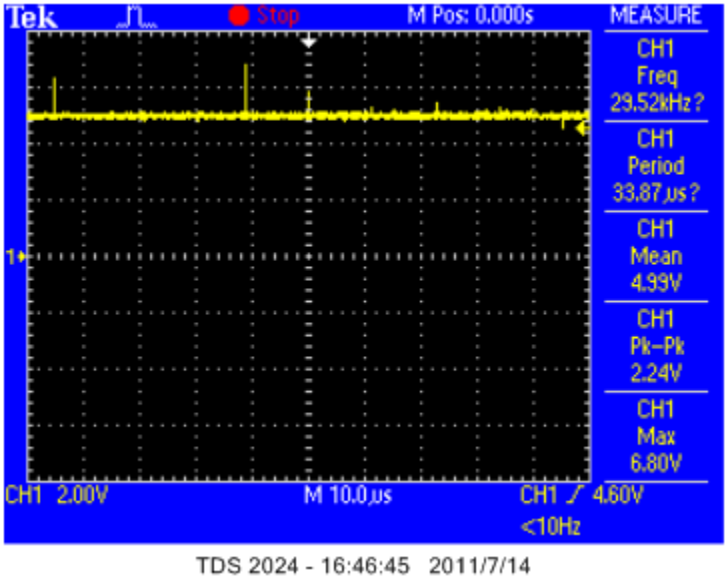


Figure 4.21. Reference pin signal from TPS92001D.

CHAPTER 5

Conclusion

A floating load buck LED driver was analyzed, design and prototyped. It was found that the characteristics of the floating load buck converter are similar to those of the conventional buck converter despites of the difference in the placement of output inductor. The floating load buck converter was successfully prototyped to drive seven white LED diodes. The advantages of the floating load buck converter make it a very attractive off-line high voltage LED driver.

BIBLIGRAPHY

[1] Barry Loveridge; “Floating Load Buck Topology for HB LEDs,” CYPRESS PERFORM, April 7, 2009.

[2] Simon Ang, Alejandro Oliva; *Power-Switching Converters* 2nd Edition, CRC Press, 2005

[3] Rowell, Derek. "State-Space Representation of LTI Systems." Http://web.mit.edu/. MIT, Oct. 2002. Web. 13 July 2011

[4] Smith, Greg. “Understanding Nonlinear Slope-compensation: a Graphical Analysis” *EETimes*. National Semiconductor, 11 May 2007. Web. 12 July 2011. <http://www.eetimes.com/design/power-management-design/4012202/Understanding-nonlinear-slope-compensation-a-graphical-analysis>.

[5] J. Alvin Connelly and Pyung Choi, “Macromodeling with SPICE,” Englewood Cliffs: PRENTICE HALL, 1992, pp.17-30.

[6] Mollet, Sam. "Analyze LED Characteristics with PSpice |EDN." Homepage| EDN.13 July 2011. <http://www.edn.com/article/502892_Analyze_LED_characteristics_with_PSpice.php>.

[7] Sedra, Adel S., and Kenneth Carless. Smith. Microelectronic Circuits. New York: Oxford UP, 2004. Print.

[8] "General Purpose LED Lighting PWM Controller." *Texas Instruments*. Feb. 2010. Web. 16 June 2011. <http://www.ti.com>.

[9]D.J.Higham and N.J.Higham, *MATLAB Guide*, SIAM, Philadelphia, 2000.

[10] D. C. Hanselman and B. Littlefield, *Mastering MATLAB* 6, *A Comprehensive Tutorial and Reference*, Prentice{Hall, Upper Saddle River, NJ, 2000.

[11] “SOT223 PNP SILICON PLANAR HIGH VOLTAGE TRANSISTOR.” Diodes.cn. ISSUE 4. JANUARY 1996. <http://www.diodes.com/datasheets/FZT757.pdf>.

[12] Application Report *Understand Buck Converter Stages in Switchmode Power Supplies*, Texas Instruments. SLVA057, March1999

[13] Abraham I. Pressman, *Switching Power Supply Design*, McGraw-Hill (1998)

[14] Day, Michael. "LED-driver Considerations." *Analog and Mixed-Signal Products* (2004): N. pag. Web. 8 June 2011. <http://focus.ti.com/lit/an/slyt084/slyt084.pdf>.

[15] E. Rogers, "*Control Loop Modeling of Switching Power Supplies*", Proceedings of EETimes Analog & Mixed-Signal Applications Conference, July 13–14,1998, San Jose, CA.

[16] Su, J.H.; Chen, J.J.; Wu, D.S.; "*Learning feedback controller design of switching converters via Matlab/Simulink*" Education, IEEE Transactions on, Volume: 45 Issue: 4, Nov. 2002 Page(s): 307 -315

APPENDIX A

Micro Model for UCC2809

```
* UCCx809-1
********************************************************************************
* (C) Copyright 2009 Texas Instruments Incorporated. All rights reserved.
********************************************************************************
** This model is designed as an aid for customers of Texas Instruments.
** TI and its licensors and suppliers make no warranties, either expressed
** or implied, with respect to this model, including the warranties of
** merchantability or fitness for a particular purpose. The model is
** provided solely on an "as is" basis. The entire risk as to its quality
** and performance is with the customer
********************************************************************************
*
* This model was developed for Texas Instruments Incorporated by:
*   AEi Systems, LLC
*   5777 W. Century Blvd., Suite 876
*   Los Angeles, California  90045
*
* This model is subject to change without notice. Neither Texas Instruments Incorporated
* nor AEi Systems is responsible for updating this model.
* For more information regarding modeling services, model libraries and simulation
* products, please call AEi Systems at (310) 216-1144, or contact AEi Systems by email:
* info@AENG.com. Or visit AEi Systems on the web at http://www.AENG.com.
*
********************************************************************************
*
** Released by: Analog eLab Design Center, Texas Instruments Inc.
* Part: UCC1809-1, UCC2809-1, and UCC3809-1,
* Date: 08/28/2009
* Model Type: Transient
* Simulator: PSpice
* Simulator Version: 16.0.0.p001
* Reference Design: Based on PMP665
* Datasheet: SLUS166B - NOVEMBER 1999 - REVISED NOVEMBER 2004
*
********************************************************************************
*
* Updates:
*
* Final 1.00
* Release to Web.
*
```

```
********************************************************************************
******
.SUBCKT UCCx809_1 FB SS RT1 RT2 Gnd Out Vdd Ref
****************************************
$CDNENCSTART
eee8c5c7a2bc4b01f045f303678664e7916da0bae22e8cb0bba041dd67c69ce448ea701
48a9ac1670c8926c1ac5057c8ccfcd77bf87ca9dc675668663bb5180d
8d1bc80c06f871c6c77e911f29f94db969fec2fec4df0cb6b294f6a760b5bb2f1c8e00b
4d57d473ff7768608afccc6eb7dcc0f146546e2985b5652ae1d276d77
****************************************
ec9f0d421d535b11ef85457a8943bba883e9027594e7355245667617679157 8b04976a1
a6cae8b7afeb0c2d46ab7210bb1612b8855c93a7199eaf7488bed9cdb
****************************************
f5b794104454237ea642ec8162309773782ec7c45271a6c8ea5dbc08aa93444e6aef9db
696221ecb5fd33a0276f5768d5ddfba14936c137bb26ba4ac5faf244b
8d4378728875d47705fb813fd34bcbca61f7f6a71b7e7d195c022347d29639c2efb1066
50aefe7391e23ab969eacc50d09c217b9ded38b5ce6685af7259e0d85
5127a6eab36081f0e68582eaf4f60a90e350afc1050d01b0a88a9dcc70a8f794f862162
7c4ab5a512abae5e3ed90dfe1e8bc408e1d93a6b1611a54062a032705
**********************************
8d4378728875d4773488398fa66488c306f4bb66d4cdc760194fbf0ac7db1ad1e4f6f34
cf8ffdb9505702d9f0b9c75517e9133a87fc04bf079cc7174003d4482
ed345a8e530999ab2dca40b4125f6dbafeb0c2d46ab7210bb1612b8855c93a711d8619f
6ef399b86053811b856b1dd71f91483a619dc8fc358a7267575e84068
8d4378728875d477d57c281ebffbb7d205702d9f0b9c75517e9133a87fc04bf07e2e276
e94fcb557513d03239beee2cd4963fed85d8570bf0afcd4a94f1c0891
**********************************
419a3a3ea5f414f589bd8996556838beae83b94dbffc812f18a8c98406840c9d99ff025
6b14ce458a286ab8191b33007ccb92990a33dd5db07ffbf9f4f887226
a978e94c36773adbe8a348f0e7b4fe0d7353264ebf8b0551e024190b992f8941aad0cae
5ebf3019a1d59f017ea29ff9d719a7a786bb5fc7d90ace418673b5596
0628fec51db38b2b706b807646b803710c17921bfe77bb70a48aa12cf3ed1aff7c71114
91f076ea533b00c364a34e79e4b8430674087a76f3add4a6ef3a43d6b
ea7d714a872e2eda706b807646b803712c23faa6c812e57cd99062375b2d2dc6f776860
8afccc6eb7dcc0f146546e298c79835e3f70d46773dbcc058438e3ffc
18425e2b5346162a547b1e3ee80d6baac8aca21d6bd160a893f0978bcaae26c25e907de
ffd12c5ffbb6ee243faaf09ac05702d9f0b9c7551552080591558 1717
c3d4cb9b306e4fab7353264ebf8b0551e024190b992f8941aad0cae5ebf3019a1d59f01
7ea29ff9d719a7a786bb5fc7de5a535a3efa3b85d94f71c251ba39091
**********************************
74d138d5844b3340058148d64d6b80d373d133d59ee5d6ac131bd9d397ac7063aa2ff92
b89da7c05907a77ff924ee9cc7c7111491f076ea5904effa3f3300cd6
e6bc4e66f4be09ed78ee89a98c1fd8936dd30c81dfdede944d5b1b73307b13037c71114
91f076ea533b00c364a34e79e4b8430674087a76f3add4a6ef3a43d6b
b92ff291a9e9d697058148d64d6b80d373d133d59ee5d6ac151286b48419f2c284c20df
dd0bb81cc014e34778e547a1ff7768608afccc6eb8a3087372c6ebb9e
54fb15ab14a0abcd72e1f6ce2acf15316dd30c81dfdede944d5b1b73307b13037c71114
91f076ea533b00c364a34e79e4b8430674087a76f3add4a6ef3a43d6b
*IUV VDD uvlo DC=80u
c713153b1818191f6b6c4528a2f67912644126c9831a96bd1d59f017ea29ff9d719a7a7
86bb5fc7de5a535a3efa3b85d144bff1ec37ba4cdb145580620fae923
8d4378728875d477e7eb8546cf2f223d0820da44be823604a8cb9624e1b0eefe05702d9
f0b9c75517e9133a87fc04bf07e2e276e94fcb557f24876b77a610898
6c25efb829c401581223a73353d3296ddd6651cd4bf067f86aef9db696221ecb5fd33a0
276f5768d5ddfba14936c137bb81fb86988a70414b7ead7291a083fd2
```

```
78b7f4a85a313df6f69bfa539de45a28db4e7d93dcfa1c7670e75d3152b48452f776860
8afccc6eb7dcc0f146546e298c79835e3f70d46773dbcc058438e3ffc
8d4378728875d477eef53e7f3f71883f06f4bb66d4cdc760126f762602a501dfe4c9ae8
f3d6491d67c7111491f076ea533b00c364a34e79ed76a1df7ac66189c
**********************************************
27b69d1425059981b9502326f055c31964bc8dfb8b58d700feb0c2d46ab7210bb1612b8
855c93a711d8619f6ef399b86053811b856b1dd7132b815445d182ba2
**********************************************
d4e0c5fd57e7035ee3596e6a8dcdab49aa4f2bb62771be50dcc49485b181f40cf9ca380
cc58d05d70dfd4046fe93b29a6e20e67007ce8a439c1ed0ad5afcabc8
55c1fc83d899a54303dbfd8a57cc629ccdba200cb9ff0be78ad832f6907043a8f45251f
6dba3bf4411b904d22aa0e59405702d9f0b9c7551552080591558171 7
4baf814dc7b6c301c6d651eb900a3a50445ff178dbcb845d641b1e529168d4e5e73b454
d73eb8c9aa66e20c2a1c7b3bfeb0c2d46ab7210b6b594affdd22b4fb
6bab9733435b404256e15feb584ba205d999c79ca8451295ebcc5ab511ddaa2c11b904d
22aa0e59405702d9f0b9c75517e9133a87fc04bf079cc7174003d4482
72903aefe5cd16f3df055017914031e992822dea7c65a18ca88a9dcc70a8f794f862162
7c4ab5a512abae5e3ed90dfe1e8bc408e1d93a6b1611a54062a032705
7b27ad51fee896a767604a65b8e1660973d133d59ee5d6ac9551113ed0230d711b6b72c
61580da8753f437384f9a7c2dba1ffa159e5a0366d38aff4e12555a5d
1cb228201de3d38a038a7afd6bc9772ccd060946ffc4e91111017f169722a85242e0b18
eb2e12f197231ef268d3262c58fa89d08439e085c07ffbf9f4f887226
55c1fc83d899a54313dc6e0da8d2ccd0871fb15cd2636bd4644988e2cf06f7edfeb0c2d
46ab7210bb1612b8855c93a711d8619f6ef399b86c9c2cb168f4ec8ee
acb50733a6636111a9418fb34b63bea6c5b3bc678e2fcadb50be95b5851bb2657032479
0963ed4be3a5cca671126ccea4457d53f329d91a8fa45b3704cb37268
e78d27c0e46090912ca50b688f0a5e537747ae655db3151f02848d886a3f951ed9f67ce
656360fcd94dcde0ef250b7c7b5f1c17ee7956303675668663bb5180d
154ede75e676e9ec320eb9f4079549eea88a9dcc70a8f794f8621627c4ab5a512abae5e
3ed90dfe1e8bc408e1d93a6b12611429df9767e905186a1996225a5eb
c2e84fd033bf71f5bb3170a29498d5f67c7111491f076ea533b00c364a34e79e4b84306
74087a76fb357fd0b1a71da699cb82d0b8594e763b461a438511dd76a
9bc8abb58df596ae89a7d22bdc40a8281d4e452fee093da4f7768608afccc6eb7dcc0f1
46546e298c79835e3f70d4677595af0e0b225ca225389b68b55f95dcf
ae04666baeadb9b83af83aa77cc65bf136806a8e381bf9a01d59f017ea29ff9d719a7a7
86bb5fc7de5a535a3efa3b85d144bff1ec37ba4cdb145580620fae923
85b71fda9a0aee346c6e874f2bbeb5880b2838dc801489b6644126c9831a96bd1d59f01
7ea29ff9d719a7a786bb5fc7de5a535a3efa3b85d94f71c251ba39091
8d4378728875d4770000c95307f798869e2a64ac42ab874343ad856cd4b14f31af73be7
7fddadc466aef9db696221ecb5fd33a0276f5768d155801e2e7b0393c
64fc38616d32ed97b716f52bdd779725feb0c2d46ab7210bb1612b8855c93a711d8619f
6ef399b86053811b856b1dd71f91483a619dc8fc358a7267575e84068
6c51504d4c7efe4ede3909a35ba556db1e23ab969eacc50d09c217b9ded38b5c31f1cc8
cb35a861cd7a360f103fa06019085b46f3dd6c5a144a656db44720cf3
b1ee433c328090cb6c6e874f2bbeb588f49e2892fcadba72644126c9831a96bd1d59f01
7ea29ff9d719a7a786bb5fc7de5a535a3efa3b85d94f71c251ba39091
8d4378728875d4779002311f07c1b3ec9e2a64ac42ab8743f80a45fe6a7ebcd4bc69f8b
36f03e83105702d9f0b9c75517e9133a87fc04bf079cc7174003d4482
$CDNENCFINISH
.ENDS UCCx809_1
```