University of Arkansas, Fayetteville
ScholarWorks@UARK

Theses and Dissertations

12-2011

Modeling of SIC P-Channel Insulated Gate Bipolar Transistors (IGBTS)

Mahmood Saadeh
University of Arkansas

Follow this and additional works at: http://scholarworks.uark.edu/etd

Part of the VLSI and Circuits, Embedded and Hardware Systems Commons

Recommended Citation
Saadeh, Mahmood, "Modeling of SIC P-Channel Insulated Gate Bipolar Transistors (IGBTS)" (2011). *Theses and Dissertations*. 240.
http://scholarworks.uark.edu/etd/240

This Thesis is brought to you for free and open access by ScholarWorks@UARK. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of ScholarWorks@UARK. For more information, please contact scholar@uark.edu, ccmiddle@uark.edu.

MODELING OF SIC P-CHANNEL INSULATED GATE BIPOLAR TRANSISTORS (IGBTS)

MODELING OF SIC P-CHANNEL INSULATED GATE BIPOLAR TRANSISTORS (IGBTS)

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

By

Mahmood Shihadeh Saadeh
Jordan University of Science & Technology
Bachelor of Science in Electrical Engineering 2009

December 2011
University of Arkansas

ABSTRACT

A new physics-based IGBT compact model has been developed for circuit simulation of silicon (Si) or silicon carbide (SiC) devices. The model accurately predicts the steady-state output, transfer and switching characteristics of the IGBT under a variety of different conditions. This is the first IGBT model to predict the behavior of p-channel SiC IGBTs. Previous work on IGBT models has focused on Si n-channel IGBTs [1-3]. This unified model is not limited to SiC p-channel IGBTs; the user has the option to select between Si or SiC, and n-channel or p-channel, making it the first IGBT model that captures the physics of all of these device and material types. The model also accounts for temperature effects, often referred to as temperature scaling, that have been experimentally validated up to 300 ºC for SiC. Validation of n-channel and p-channel devices was accomplished by fitting the steady-state characteristics and inductive load switching transient waveforms. 15-kV p-channel IGBTs supplied by Cree were among those used for validation [6]. The fitting was achieved using Certify, a software tool developed at the University of Arkansas. A parameter extraction recipe for the model was developed for simple parameter extraction using data that are readily available from datasheets. That fitting tool is available to the public through the National Center for Reliable Electric Power Transmission website (ncrept.eleg.uark.edu). The model and parameter extraction recipe will also be made available to the public through NCREPT.

This dissertation is approved for recommendation
to the Graduate Council

Dissertation Director

____
Dr. H. Alan Mantooth

Dissertation Committee:

____
Dr. Juan Balda

____
Dr. Roy McCann

THESIS DUPLICATION RELEASE

I hereby authorize the University of Arkansas Libraries to duplicate this dissertation when needed for research and/or scholarship.

Agreed ________________________________
Mahmood Shihadeh Saadeh

Refused ________________________________
Mahmood Shihadeh Saadeh

ACKNOWLEDGEMENTS

I would like to express my appreciation to my advisor Dr. Alan Mantooth for his continued support and guidance throughout my MSEE study. Besides my advisor I would like to thank the rest of my thesis committee for their support. I am grateful to Cree, Inc. for providing the data, and devices used in this thesis. I would also like to thank my friends for their continued support and encouragement especially through the final steps in preparing this thesis. I also would like to thank my parents and siblings for being there for me and for all they have done for me throughout the years. Special thanks to my older brother for his help, support, and encouragement throughout my graduate study.

Mahmood S. Saadeh

Table of Contents

CHAPTER 1 1

Introduction 1

1.1 Overview of IGBTs 1

1.2 Survey of IGBT Models 8

1.3 The Unified IGBT Model 9

CHAPTER 2 12

Silicon Carbide Power Semiconductor Devices 12

2.1 Introduction 12

2.2 SiC properties & device characteristics 12

2.3 System Advantages 16

CHAPTER 3 18

The Unified IGBT Model 18

3.1 Introduction 18

3.2 Mobility 20

3.3. Breakdown 26

3.4. Tail Current 28

3.5. Capacitances and Charges 30

3.6. Model Current Components 33

3.7. Temperature Effects 36

3.8. The Equations Section 40

CHAPTER 4 42

Characterization and Parameter Extraction 42

4.1 IGBT Characteristics 42

4.2 Parameter extraction 44

CHAPTER 5 61

Conclusions and Future Work 61

5.1. Conclusions 61

5.2 Future Work Recommendations 62

Bibliography 63

CHAPTER 1

Introduction

1.1 Overview of IGBTs

1.1.1 History of IGBTs

The Insulated Gate Bipolar Transistor (IGBT) is a four layer voltage-controlled bipolar device. It was first demonstrated by Baliga in 1979 when he was with General Electric R&D [1]. Even though the IGBT was first demonstrated by Baliga in 1979, the concept of using a gate to control a vertical channel was being investigated as far back as the 1950s, mainly in France [2] and Japan [3]. This concept of a gate controlling a vertical channel was first described as a PNP junction bipolar transistor (BJT) driven by an n-channel Metal Oxide Field Effect Transistor (MOSFET) by Baliga in 1984 [4]. The first silicon IGBT was introduced commercially in 1983 [5]. Since 1983, IGBTs have come a long way in terms of device ratings and characteristics. Silicon carbide IGBTs are not yet available commercially, but are available as R&D devices.

1.1.2 The Subcircuit Model

Figure 1.1 presents the structure of an n-channel IGBT. It can be seen that it is the same as the structure of an n-channel MOSFET with the addition of the heavily doped substrate. The effect of this heavily doped substrate is that instead of having an anti-parallel body diode as in a MOSFET, IGBTs have a bipolar component. Adding this new layer introduced a new junction that can be considered as a PIN diode. Figure 1.2 shows the PIN-MOSFET subcircuit model. The subcircuit model could also be looked at as a MOSFET driving a bipolar transistor, as the p-n junction that composes the body diode in a MOSFET is now a *pnp* bipolar transistor in the IGBT. Figure 1.3 shows the MOSFET-BJT subcircuit model.

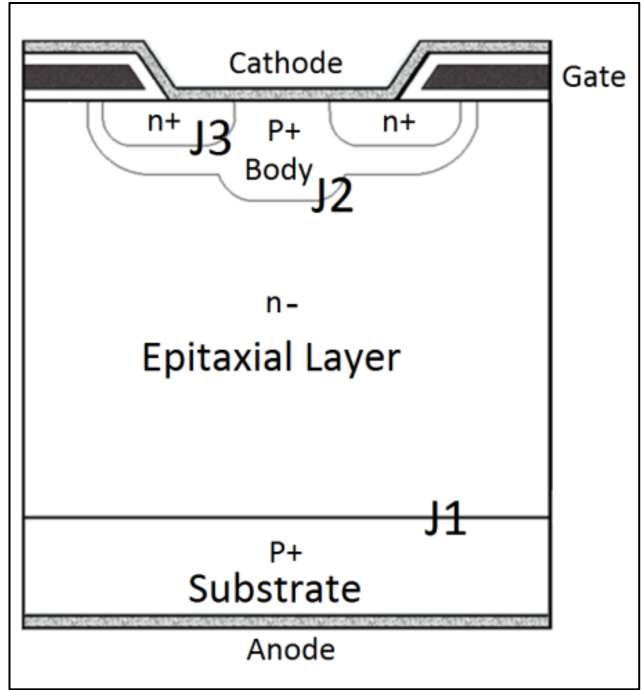

Fig. 1.1. N-Channel IGBT structure.

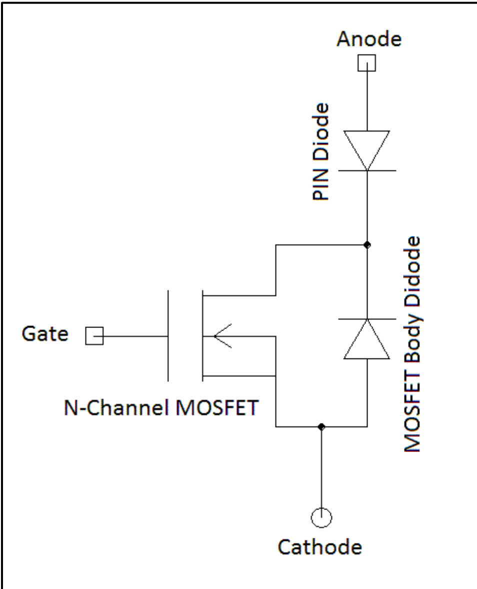

Fig. 1.2. MOSFET-PIN rectifier subcircuit model.

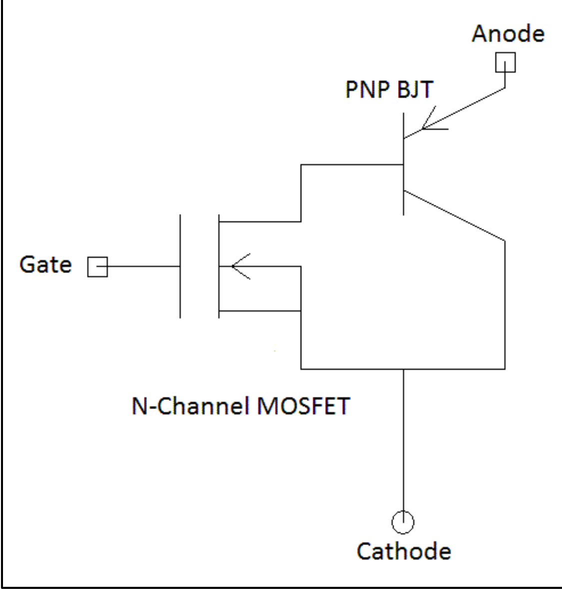

Fig. 1.3. MOSFET-BJT subcircuit model.

1.1.3 Modes of Operation

1.1.3.1 Reverse Blocking Mode

Reverse blocking is when the gate is shorted to the cathode, the cathode is at a positive potential, and the anode is at a negative potential relative to the cathode. At this condition, junctions J1 and J3 are reverse biased while junction J2 is forward biased. The reversed junctions J1 and J3 prevent current flow in the device, and voltage builds up mainly across junction J1. Most of the depletion region extends through the epitaxial layer due to its low doping. The reverse blocking voltage of the IGBT depends mainly on the width and doping of the low doped epitaxial layer, otherwise called the drift region.

1.1.3.2 Forward Blocking and Conduction Modes

If the voltage across the anode-cathode is reversed while maintaining the gate shorted to the cathode, junctions J1 and J3 will become forward biased, and junction J2 will become reverse biased. Thus, the forward blocking voltage will be supported by junction J2, and in this case, the depletion region primarily extends into the lightly doped epitaxial layer.

1.1.3.3 Forward Conduction Mode

The forward conduction mode is achieved by applying a positive voltage across the gate-cathode while maintaining the positive anode-cathode voltage. The gate-cathode voltage needs to be large enough to invert the body region underneath the gate, thus forming a channel. This channel once formed will connect the highly doped n+ region to the epitaxial layer, and electrons will diffuse from the highly doped region to the lightly doped region. Once electrons are in the lightly doped region they will drift due to the field effect from the drain to the source of the

MOSFET causing the potential of the epitaxial layer to drop near the highly doped body region to a point where the junction J1 becomes forward biased. Now that junction J1 is forward biased, a high density of holes will be injected from the substrate region to the epitaxial layer. At very high anode to cathode voltages, the amount of injected carriers could be up to 100-1000 times of the background doping of the epitaxial layer, constituting what is called high level injection. This high concentration of holes in the epitaxial layer attracts electrons from the cathode contact. The excess concentration of electrons and holes in the lightly doped epitaxial layer enhances its conductivity. This mechanism is referred to as conductivity modulation, and it results in a very low on-state resistance.

1.1.4 Status of SiC IGBTs

Although not commercially available, 15 kV p-channel SiC IGBTs have been reported [6]. In the meantime, silicon IGBTs are the primary devices in use for power electronic applications as they offer higher switching speeds than current controlled devices such as GTOs. They also offer higher blocking voltages with less conduction losses than MOSFETs, making IGBTs the best choice for medium voltage, medium frequency applications. Currently silicon IGBTs are available with up to 6.5 kV-1.2 kA ratings competing with silicon GTOs [6]. Although 6.5 kV IGBTs are available, the use of the 3.5 kV devices in modular configurations is more common as the 6.5 kV devices are relatively slow.

1.1.5 Modeling & Simulation

Simulation is an essential step in power electronic systems design. As a matter of fact, it is important for the design of any electrical circuit. The importance of simulation arises from the fact that it saves the designers time, and effort. Most importantly, it reduces the cost of

prototyping. Simulation is important for verifying the concept of the design before prototyping begins, as many problems in the design can be foreseen in the simulation. Once the design is verified through simulation, then prototyping can begin. Simulation is also important for large systems, where it can be broken into smaller blocks, and each block could be simulated and verified on its own before integrating the whole system.

A simulation is only as accurate as the model. Models range in accuracy from a less accurate level-0 model to a highly accurate level-4 model. Level-0 models are behavioral models that are composed completely from empirical equations, and lack any physical equations, or any empirical equations that model second order or above physical effects. A level-0 model is only concerned with the input and output characteristics, and is not all that accurate. Level-4 models are models that are purely physical and predict every detail of the device. A level-4 model is deals with charge carriers, and the associated electric field produced inside the device. A level-4 model is accurate enough that it will predict physical effects in the devices. Level-1 to level -3 models describe the basic behavior of the devices. Specific physical effects that are observed form the device's characteristics can be added to the model. These physical effects can be described by physical or empirical equations.

Physical effects can be first order effects or second order effects. First order effects are the effects that describe the basic behavior of the device, like linear capacitances, and intrinsic resistances. Second order effects are the effects that are more detailed, like conductivity modulation, avalanche breakdown, and mobility reduction. The classification of what level the model is depends on what physical effects are modeled; the more second order effects are modeled the more predictive the model will be.

The first step in device modeling is to have a comprehensive understanding of the device's characteristics, its basic operation, and the more detailed physical phenomena that takes place in the device. An understanding of the how the device physics leads to the specific characteristics of the device is needed.

The level of accuracy is determined by selecting what effects to include in the model, as different levels of models serve different purposes. The more accurate the model is, the more complicated it is and the model formulation and simulation becomes more time consuming. For a basic proof of concept simulation, a high level accuracy is not necessary as it consumes time and computation power. High accuracy physical models, like a level-4 model, would be needed when the purpose of the model is to help understand the physics of the device, and the design is at the device level.

Next, the mathematical representation of the model is developed. The model equations need to be formulated and derived from the physics of the device. In this step all the first and second order effects are mathematically described as they relate to the characteristics in the different operation modes and regions.

Lastly, the mathematical representation of the model and the different effects included are put together in a model using a hardware description language (HDL). Different simulators support different languages; for example, the Spectre simulator uses Verilog-A, and Saber uses MAST.

1.2 Survey of IGBT Models

Since the invention of the IGBT, more than fifty papers have been published on IGBT models [7]. Hefner developed the first complete analytical, charge controlled model suitable for circuit simulation [8]. The main two IGBT models developed are the Hefner model and the Kraus model [9]. Both models have been implemented in MAST. The two models have been developed using different approaches. The Hefner model depends on the redistribution of charge within the drift region, while the Krause model models the charge extraction from the drift region by the electric field and by emitter back injection [9]. Hefner modeled the nonquasi-static effects caused by the fast penetration of the space charge layer edge. Nonlinear capacitances, conductivity modulation are also present in the Hefner model. This model was also extended to an electro-thermal model. Krause modeled the nonzero minority carrier concentration at the emitter edge. The Hefner model was adopted by many modelers and simulators. It is used in the Saber simulator and in PSPICE, and is well described in the literature.

Another model worth mentioning is the Lauritzen lumped charge IGBT model [10]. It offers a simpler parameter extraction recipe, but compromises the accuracy in doing so. Although the Hefner model provides very high accuracy, is commonly used, and is available in the simulators PSPICE and Saber, the parameter extraction procedure is complicated enough, that it is only practical for simulator vendors, and power semiconductor device manufacturers to create model libraries. An automated parameter extraction software was developed for the Hefner model by the National Institute of Standards and Technology (NIST) [11]. Although the parameter extraction software developed by NIST is automated, it requires detailed complex measurements for the device under test (DUT) that only few laboratories in the world have capabilities of performing [12]. Another parameter extraction method has been developed by

Lauritzen, but it is only suitable for the lumped charge IGBT model [10]. Many simpler parameter extraction techniques have been developed by the academic society for the Hefner model [13].

1.3 The Unified IGBT Model

A new physics-based IGBT compact model has been developed for circuit simulation of silicon (Si) or silicon carbide (SiC) devices. The model accurately predicts the steady-state output, transfer and switching characteristics of the IGBT under a variety of different conditions. This is the first IGBT model to predict the behavior of p-channel SiC IGBTs. Previous research on IGBT models have focused on Si n-channel IGBTs. The unified model is not limited to SiC p-channel IGBTs. The user has the option to select between Si or SiC, and n-channel or p-channel, making it the first IGBT model that captures the physics of all of these device and material types. The model also accounts for temperature effects, often referred to as temperature scaling, that have been experimentally validated up to 125 °C for silicon and 225 °C for SiC. Validation of the n-channel and p-channel devices for both Si and SiC was accomplished by fitting the steady-state characteristics and inductive load switching transient waveforms. 12-kV p-channel IGBTs supplied by Cree, and 600-V n-channel IGBTs from International Rectifier were among those used for validation [14]. The fitting was achieved using Certify, a software tool developed at the University of Arkansas. A parameter extraction recipe for the model was developed for simple parameter extraction using data that are readily available from datasheets. That fitting tool is available to the public through the National Center for Reliable Electric Power Transmission's website (ncrept.eleg.uark.edu). The model and parameter extraction recipe will also be made available to the public through NCREPT.

1.3.1 IGBT modeling

This unified model is a physical model based on the Hefner IGBT model [15]. This model predicts the operation of the device under both steady-state and transient operation. A circuit representation that has been used in previous models to describe and predict the operation of Si n-channel IGBTs is leveraged. It consists of a MOSFET driving an NPN BJT. The BJT components in this model are very different than traditional BJT models. This is due to a wide, low-doped base region that has a low gain. Given the current densities of the IGBT, the BJT component will be in high level injection conditions, so ambipolar transport equations are used to describe carrier transport.

The model uses the latest mobility model for SiC. Different parameters have been introduced to account for the reduction in channel mobility due to high electric field introduced by high gate voltages. The MOSFET current component is split into two components: I_{MOSL} and I_{MOSH}, representing the low and high level currents, respectively. This is done to enable modeling of the soft knee transition in SiC for the transconductance. The two current components, I_{MOSL} and I_{MOSH}, have independent threshold voltage parameters, V_{TL} and V_{TH}, and independent transconductance parameters K_{FL}, K_{PL}, and K_{FH}, K_{PH}, respectively. This parallel channel offers much better control of the main channel current inside the model. K_{FL} and K_{PL} were introduced to account for the different current values in the linear and saturation region due to the non-uniform density in the channel. The charge equations have been formulated as the integral of the capacitances over voltage to ensure the conservation of charge. In order to simplify the transient parameter extraction, the various internal capacitances in the model have been combined to obtain the terminal capacitances Ciss, Coss, and Crss which are normally given in device datasheets.

1.3.2 Parameter extraction

The parameter extraction software package Certify was developed at the University of Arkansas [17]. It automates the parameter extraction procedure. The software needs a parameter extraction recipe and the target data to extract the parameters. The parameter extraction recipe is a set of different simulations to run the associated test conditions and specified algorithms for parameter extraction and fitting.

CHAPTER 2

Silicon Carbide Power Semiconductor Devices

2.1 Introduction

Silicon Carbide (SiC) is the logical choice for fabricating power semiconductor devices for its superior properties. The superior properties of SiC allow the fabrication of power semiconductor devices with improved characteristics resulting in better power electronic systems. This chapter will discuss the properties of SiC, and how that leads to better power semiconductor devices, and better power electronic systems.

2.2 SiC properties & device characteristics

An ideal power semiconductor device has a couple of characteristics that are of importance. It should have the ability to block large voltages in forward and reverse mode with very little current flowing through the device, and conduct large currents when switched on, with very little voltage drop across the device. It should also be able to transition from conduction mode to blocking mode almost instantaneously. And finally, it should consume very little power. Ideal power semiconductor devices do not exist, but if a comparison were to be made between Si and SiC devices, SiC devices clearly would have the most resemblance to ideal switches.

Silicon power semiconductor device's capabilities have advanced tremendously over the past decades due to the demand of improved performance. The improved performance was achieved due to the high level of maturity of silicon technology, where large substrates are produced with very low defects. Silicon devices have reached material limitations, preventing any major advances in the technology. Characteristics such as blocking voltage, forward current,

leakage current, and switching frequency capabilities are not predicted to improve in Si devices. The limitations on those characteristics are due to the properties of silicon as will be discussed later.

When compared to Si, SiC allows the fabrication of thinner drift regions (0.1x) with higher doping (10x), thus having 100 times the blocking capability of silicon, and 0.001 times the resistance of silicon, leading to lower power dissipation and higher switching speeds [18].

The superior properties of SiC has always been known to the power semiconductor devices research community, but it was not until recently that silicon carbide technology reached a level of maturity allowing the fabrication of large wafers with low defects, thus making it commercially feasible to fabricate SiC power semiconductor devices[19]. SiC is the most prominent in power electronics, but GaN may be the material of the future. Years from now, there may be diamond power semiconductor devices for critical applications, as it has the most superior properties [20].

SiC and GaN both promise superior device characteristics mainly due to their wide bandgap, and higher breakdown electric field. SiC, and GaN are not new materials, nor were their properties discovered recently. In fact SiC was a very good candidate to be used for semiconductor devices before silicon due to its superior properties, but the inability to grow large SiC substrates with low defects was an issue. On the contrary, silicon could be grown in large wafers and with very low defects. Thus silicon was the more attractive choice for research and development, and device fabrication.

The key advantage of SiC over Si is the wide bandgap. The wider bandgap allows the operation of power semiconductor devices at higher temperatures, higher blocking voltages, and

in higher radiation environments. Wide bandgap means it takes more energy to transfer an electron from the valance band to conduction band, making the device more immune to temperature and radiation affects. This property also translates into higher breakdown electric field, which is the reason behind the higher blocking voltage capabilities.

The main properties to study when comparing semiconductor materials for power semiconductor applications are the bandgap, saturation drift velocity, critical electric field, electron and hole mobility, and thermal conductivity. Table 2.1 shows a comparison of these properties of the different materials discussed. It can be seen that while most of the properties of SiC are much better than those of Si, the mobility of SiC is less than that of silicon. When it comes to device characteristics it is evident that the advantages of SiC over Si overcome the advantages of Si over SiC.

Each of the properties in Table 2.1 below has in impact on the improvement in the characteristics of the power semiconductor device. The superior properties of SiC are discussed below as they pertain to the specific device characteristic.

Table 2.1. Properties of Different Semiconductors

Material	**Eg @300 K (eV)**	**Vsat (cm/s)**	**Ec (V/cm)**	**εr**	**µn @ 300k (cm2/V·s)**	**µp @ 300k (cm2/V·s)**	**Thermal conductivity (W/m·k)**
Si	1.11	10^7	3x10^5	11.7	1450	450	150
3C-SiC	2.3	2.5x10^7	2x10^6	9.6	1000	45	500
6H-SiC	2.9	2x10^7	2.6x10^6	9.7	415	90	480
4H-SiC	3.2	2x10^7	3x10^6	10	950	115	400
GaN	3.39	2x10^7	5x10^6	8.9	1000	350	130
Diamond	5.6	3x10^7	5.6x10^7	5.7	2200	1800	2000

2.2.1 Wide Bandgap

The bandgap is the energy required to transfer a charge carrier from the valance band to the conduction band. The wider the bandgap is the less sensitive it is to radiation and thermal and electric field stresses. The wide bandgap of SiC leads to higher blocking voltages, lower conduction losses, lower switching losses, lower leakage current, and higher temperature operation. It also allows the fabrication of drift regions that are 10 times thinner with 10 times the doping of silicon. Thus, SiC devices have two orders of magnitude lower on-state resistance than Si devices leading to lower on-state power losses. The wide bandgap also contributes to the faster switching speeds of SiC devices. Figure 2.1 illustrates the bandgap, conduction band, and valance band.

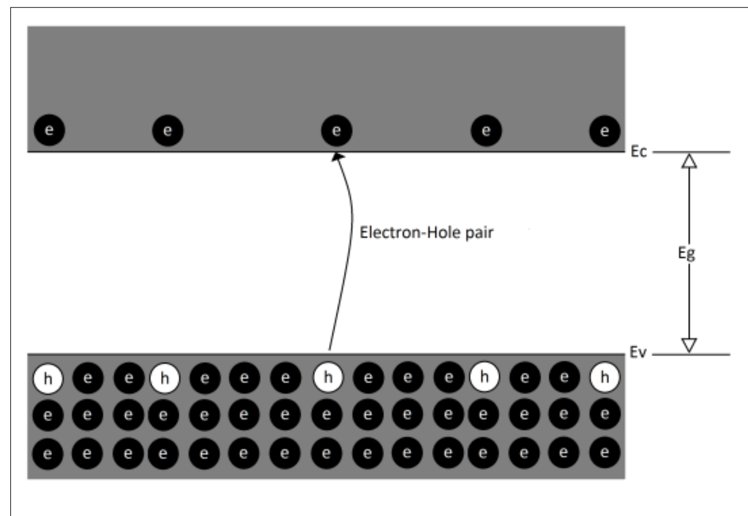

Fig. 2.1. Bandgap of a semiconductor device.

2.2.2 High Drift Saturation Velocity

The drift saturation velocity is the highest speed a charge carrier can travel within the material. The high drift saturation velocity of SiC contributes to the faster switching speeds of SiC devices. The low power loss per switching cycle allows the switching of the devices at higher switching frequencies. It also contributes to the higher current density of SiC devices.

2.2.3. Thermal Conductivity

The thermal conductivity of SiC is over 400-500 W/(m-K), which is about three times that of Si. The thermal conductivity of SiC being slightly higher than the thermal conductivity of copper makes it easier to remove the heat from SiC devices, than from Si devices.. The ease of heat removal from the device leads to slower thermal buildup thus allowing the device to operate at higher junction temperatures.

2.2.4 Critical Electric Field

The critical electric field is the breakdown electric field of the material per square area. The critical electric field contributes to the higher blocking voltage capability of SiC devices due to the higher breakdown electric field.

2.3 System Advantages

These superior properties of the material and the resulting improvements in characteristics of the SiC power semiconductor devices enable building better power electronic systems.

The faster switching speeds of the devices result in less switching losses, thus improving efficiency of the system. It also means that the devices can now be switched at higher

frequencies thus resulting in less harmonic content for high frequency inverters. Less harmonic content is favorable for power quality issues and because it reduces the size and footprint of the passives needed for filtering. Switching at higher frequencies also reduces the size of energy storage elements required and thus the physical size of these elements can be made smaller.

Higher operating temperature of SiC devices can simplify and reduce cooling systems complexity and footprint.

Fewer stacked devices are needed for high voltage applications due to the higher blocking voltage. This reduces the size and the complexity of voltage sharing networks. This all improves the system reliability.

The wide bandgap nature of SiC makes systems less sensitive to temperature and radiation variation, which improves the overall stability of the system. The wide bandgap also leads to reduced leakage current in the devices, thus reducing the standby power consumption.

Even though SiC has higher current density, Si IGBTs have much higher current ratings because they are wafer level in scale. Current SiC devices are considered low current devices in comparison. But as SiC technology matures enough to enable the fabrication of devices with similar sizes to Si devices, SiC devices will offer devices with higher current ratings.

CHAPTER 3

The Unified IGBT Model

3.1 Introduction

This model is based on the Hefner Si IGBT model [8]. The topology used in both models is displayed below in Figure 3.1. This topology is based on the analog circuit representation of the model equations. Two internal nodes are necessary to implement this model, the drain and the emitter nodes. Each of the current components in the topology below is discussed later, along with the associated elements.

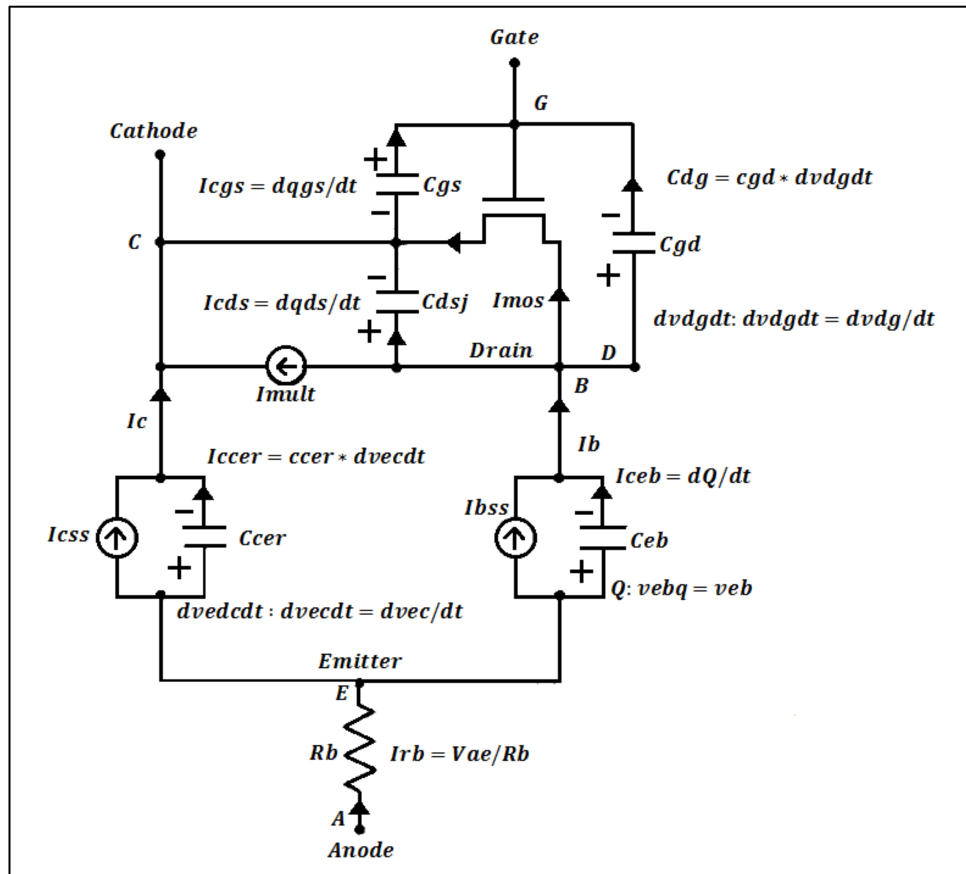

Fig. 3.1. The model topology [8].

This model was implemented in Modlyng, and then a MAST template was generated. A MAST template consists of several different sections. These sections include the template header, the header declarations, the local declarations section, the parameters section, the values section, the control section, and finally, the equations section.

The template header defines the name of the template, the ports of the template, and the template parameters. Header declarations define the parameters that are used in the header. The local declarations section is used to declare the values(Vals) and variables (Vars) that are used in the model. The parameters section is used to manipulate the parameters that are declared in the header, or the calculated model parameters that are not declared in the header. Calculated model parameters can only depend on parameters that are declared in the header. In the values section values are manipulated and the variables are prepared to be solved. The values section is also the section where the behavior of the device is described, and all the physical effects are implemented in the model.

In the control section, specific information is provided to the simulator to aid convergence. This information includes Newton steps, sample points, and plot sets. The control section is not mandatory as the simulator can guess the needed information, but providing information that is optimized for the specific model will improve the overall performance of the model. The equations section is used to describe the characteristics of the terminals of the model, and to specify the fashion in which the variables in the system are solved. The equations in the equation section can either be a simple relation of a terminal current as it relates to values from the values section, or it can be used to force the simulator to solve for a variable iteratively until a certain condition is met.

3.2 Mobility

3.2.1.Low Field Mobility Modeling

Mobility is the ability of charge carriers to move in the semiconductor material. In other words, it governs the charge carrier transport in the semiconductor material. It can be expressed as the average particle drift velocity per unit of electric field as in Equation (3.1) [22].

$$\mu_x = -\frac{\langle V_x \rangle}{\mathcal{E}_x} \tag{3.1}$$

At low electric fields the relation between the mobility and the charge carrier velocity is linear, and the mobility is constant at μ_o (lower field mobility). The low field mobility depends on the doping and on the temperature. Equation (3.2) describes the dependence of the low field mobility on doping.

$$\mu_o = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N}{N_{ref}}\right)^{\alpha}} \tag{3.2}$$

In the equation, N is the total doping concentration in the material, and μ_{min}, μ_{max}, N_{ref}, and α are fitting parameters [23]. These are fitting parameters for the mobility model of the material, not for the device itself. The mobility is measured in a bulk material for different samples with different doping. Then, the measured data is fitted to the analytical equation above.

Equations (3.3) through (3.6) describe the low field mobility of n-type and p-type materials, for both silicon and silicon carbide. The equations were obtained by substituting the appropriate fitting parameters into Equation (3.2). The fitting parameters were obtained from [24]. Table 3.1 summarizes the fitting parameters used.

For Si:

$$mu_{n0} = \frac{5.10*10^{18}+92*Nb^{0.91}}{3.75*10^{15}+Nb^{0.91}} \quad (3.3)$$

$$mu_{p0} = \frac{2.9*10^{15}+47.7*Nb^{0.76}}{5.86*10^{12}+Nb^{0.76}} \quad (3.4)$$

For 4H-SiC:

$$mu_{n0} = \frac{4.05*10^{13}+20*Nb^{0.61}}{3.55*10^{10}+Nb^{0.61}} \quad (3.5)$$

$$mu_{p0} = \frac{9.3*10^{11}+10*Nb^{0.56}}{5.3*10^{9}+Nb^{0.56}} \quad (3.6)$$

Table 3.1. Mobility Model Parameters

Parameter	Si	4H-SiC
Minimum and maximum electron mobility μ_{minn}, μ_{maxn}. (cm^2/V.s)	65 1360	50 950
Minimum and maximum hole mobility μ_{minp}, μ_{maxp}. (cm^2/V.s)	50 505	10 180
Electron an hole ionization coefficients α_n, α_n	0.91 0.63	0.76 0.56
Reference electron and hole concentrations N_{refn}, N_{refp}	8.5e1 6.3e1	2.2e17 2.35e17

3.2.2. Temperature Dependent Mobility

Equation (3.7) is the general form of the empirical equation that describes the relationship between mobility and temperature [25].

$$\mu = \mu_o \left(\frac{T}{T_o}\right)^{\gamma} \tag{3.7}$$

In Equation 3.7, μ_o is the low field mobility, T is the temperature, T_o is the nominal temperature, and γ is a fitting parameter.

Equations (3.8) through (3.11) describe the relationship between mobility and temperature for n-type and p-type materials, for both silicon and silicon carbide.

For Si:

$$mu_n = mu_{n0} \left(\frac{T}{300}\right)^{-2.42} \tag{3.8}$$

$$mu_p = mu_{p0} \left(\frac{T}{300}\right)^{-2.20} \tag{3.9}$$

For 4H-SiC:

$$mu_n = 1140 \left(\frac{T}{300}\right)^{-2.70} \tag{3.10}$$

$$mu_p = 1140 \left(\frac{T}{300}\right)^{-2.50} \tag{3.11}$$

3.2.3. Mobility Degradation

The actual mobility in power semiconductor devices is not exactly as described in Equations (3.8) through (3.11) due to some degradation factors. The effective mobility in IGBTs is described in Equation (3.12) below.

$$mu_{eff} = mu_n + mu_p p * \frac{q}{q+qb} \quad (3.12)$$

As the electric field in the channel increases, the velocity of the carriers in the channel increase linearly. However, as the velocity increases it will reach a saturation velocity. The saturation velocity is reached due to the scattering of the energetic electrons at high velocities. This will effectively reduce the carrier mobility in the channel.

At high carrier concentrations, carrier-carrier scattering will take place due to the excess carrier concentration at the emitter edge of the base, which is designated as $p0$. The last term in Equation (3.12) is approximated as described in Equation (3.13) below:

$$\frac{q}{q+qb} = \frac{p0}{p0+nb+Nsat} \approx \frac{p0}{p0+nb} \quad (3.13)$$

Where p0 is the excess carrier concentration at the emitter edge of the base, $Nsat$ is the component of base collector space charge due to velocity saturation, and qb is the background base charge.

Using the approximation above, the effective mobility can be approximated as described in Equation (3.14).

$$mu_{eff} = mu_n + \frac{mu_p * \frac{p0}{nb}}{\frac{p0}{nb}+1} \quad (3.14)$$

The value $Nsat$ is dependent on I_c andI_{mos}. Both current components are dependent on the space charge qb; thus,$Nsat$ has to be solved iteratively. The use of the approximation above eliminates the need for the variable $Nsat$ that was solved for iteratively therefore improving simulation speed and convergence.

The effective mobility mu_{eff} is used for the calculation of the drift region conductivity modulated base resistance in the forward conduction mode. In the reverse blocking mode, conductivity modulation does not take place so the base resistance is calculated using mu_n or mu_p depending on the type of the device.

In the blocking mode the equation governing the base resistance is:

$$rb = \frac{w}{mu_n * a * q * nb} + rs \quad (3.15)$$

In the case of forward conduction mode, the equation becomes:

$$rb = \frac{w}{mu_{eff} * a * q * neff} + rs \quad (3.16)$$

To improve convergence and simulation speed, the equations for rb , mu_{eff}, and n_{eff} were broken into smaller and simpler parts. A couple of simple equations are easier and faster for the simulator to solve rather than one big complex equation. Figure 3.2 below shows the code fragment used to calculate the conductivity modulated base resistance rb.

Charge carrier mobility in the MOSFET inversion layer is lower than that in the drift region. This is due to presence of the gate oxide. The electron is not solely a particle. It has some properties of both a particle and an electromagnetic wave. These particle-wave properties of the electron are referred to as a wave function. Boundary condition continuity laws require that the

electrons at the boundary between the oxide and the channel must have the same mobility in both regions. High electric field at the channel surface will push the electron wave function more into the oxide, thus reducing the mobility of the charge carriers in the inversion layer near the oxide. This is modeled as electric field dependent mobility in the MOSFET channel region.

```
w2l = w/2/l

tanh2 = tanh(w2l)

qtop0 = math_charge * model-> a * l * tanh2

p0 = qceb/qtop0

p0_nb = p0/model-> nb

sinh1 = sinh(w/l)

sinh2 = sinh(w2l)

mueff = mun + mup * p0_nb/(p0_nb + 1)

neff1 = sqrt(1 + p0_nb * p0_nb/sinh1/sinh1)

neff2 = neff1 * tanh2

neff3 = 1 + p0_nb/sinh1 * tanh2

nratio = neff2/neff3

if (nratio <= model-> fc_neff)     neff = w2l * model-> nb * neff1/atanh(nratio)

else                               neff = w2l * model-> nb * neff1/atanh(model-> fc_neff)

rb = w/(mueff * model-> a * math_charge * neff) + model-> rs
```

Fig. 3.2. Conductivity modulated resistance rb code fragment.

This phenomenon is very important at submicron channel lengths. In power semiconductor devices this is important due to the roughness of the oxide-semiconductor interface and is referred to as surface roughness scattering. In the case of strong inversion, the high electric field caused by the oxide fixed charges and the ionized fixed charges in the semiconductor acts normal to the oxide-semiconductor interface and increases the effect of the surface roughness scattering. It raises the need for this effect to be modeled. The effect of this mobility reduction translates into transconductance reduction due to the transverse electric field in the channel region. Theta is an empirical parameter which models the transconductance reduction due to the transverse electric field in the MOSFET channel. It is modeled as a function of V_{gs}. The transconductance reduction due to the transverse electric field was also investigated in [26].

$mu_{fact}$is the mobility reduction factor implemented in the model. $mu_{fact}$is dependent on theta and the gate voltage.

$$mu_{fact} = 1 + theta_t * \left(v_{gs-}vt_t\right) \tag{3.17}$$

This mobility reduction factor is realized in the model by directly reducing the MOSFET current component using the following equation in the appropriate conditions.

$$i_{mos} = \frac{i_{mos}}{mufact} \tag{3.18}$$

3.3. Breakdown

Every semiconductor device has a limit on the maximum voltage that can be applied across the device. This voltage is known as the maximum blocking voltage or the breakdown voltage. The name breakdown voltage comes from the breakdown behavior of the device after

that voltage is exceeded. Breakdown is best described as a fast increase in current with respect to voltage. The breakdown voltage is a key parameter for power semiconductor devices.

Breakdown is caused by the impact ionization mechanism and avalanche multiplication. Even though avalanche multiplication is not destructive for IGBTs, if the current passing through the device due to avalanche multiplication exceeds the current rating of the device, it will destroy the device.

As the drain-source voltage is increased, the electric field in the channel is increased leading to an avalanche breakdown in the channel at the drain. This breakdown causes the device to behave like a p-n diode. The avalanche breakdown generates holes that move from the drain to the source right under the inversion layer. These holes bias the body diode which causes electrons to be injected as minority carriers in the drift region. These electrons cause more holes to be generated in the inversion layer. This phenomenon creates a positive feedback that reduces the drain-source breakdown voltage. The second order effect of avalanche multiplication within the base collector depletion region is implemented by introducing the avalanche multiplication factor m.

$$m = \frac{1}{1-\left(\frac{v_{ds}}{bvcbo_t}\right)^{bvn_t}} \tag{3.19}$$

The avalanche multiplication factor is then linearized in the region described in Equation (3.20).

$$v_{ds} >= fc_{bvcbo} * bvcbo_t \tag{3.20}$$

Piecewise linearization is implemented as follows:

$$m = \left(\frac{1}{\left(1 - fc_bvcbo^{bvn_t}\right)^2}\right) * \left(\left(\frac{bvn_t}{bvcbo_t}\right) * fc_{bvcbo}{}^{(bvn_t - 1)} * v_{ds} + 1 - fc_{bvcbo}{}^{bvn_t} * (bvn_t + 1)\right) \quad (3.21)$$

bvn_t is the temperature dependent avalanche multiplication exponent. bvn is the avalanche multiplication parameter.

$$bvn_t = bvn * \left(\frac{1}{t_{rat}}\right)^{bvntexp} \quad (3.22)$$

bvf_t is the temperature dependent avalanche uniformity factor. bvf is the avalanche uniformity factor parameter.

$$bvf_t = bvf * \left(\frac{1}{t_{rat}}\right)^{bvftexp} \quad (3.23)$$

$bvcbo_t$ is the collector base breakdown voltage, and is described in Equation (3.24).

$$bvcbo_t = \frac{bvf_t * 5.34 * 10^{13}}{n_b{}^{0.75}} \quad (3.24)$$

The avalanche multiplication breakdown effect is introduced by the current component I_{mult}. I_{mult} is described by Equations (3.25) and (3.26) below.

$$i_{gen} = \frac{q * n_i * a * \sqrt{2 * \epsilon * abs\left(\frac{V_{ds}}{q * n_b}\right)}}{tauhl_t} \quad (3.25)$$

$$I_{mult} = (m - 1) * abs(i_{mos} + i_{cc}) + i_{gen} * m \quad (3.26)$$

3.4. Tail Current

IGBTs exhibit a current tail due to charge storage in the base region of the bipolar component of the device. The presence of the tail current causes slower switching speed compared to MOSFETs. During this longer switching period the device sees high voltage and

high current simultaneously causing high switching losses, leading to a limitation on the frequency at which the device could be switched.

When the gate voltage of the IGBT is switched to a value below the MOSFET component threshold, the channel disappears, the channel current of the MOSFET is removed, and the base current supply to the bipolar transistor is interrupted. The base current of the bipolar transistor decays rapidly as the MOSFET channel disappears, but the bipolar collector current cannot decay as fast due to the presence of excess carriers in the epitaxial layer (the base region). These excess carriers or stored charges decay by recombination in the base region and carrier injection into the emitter region, resulting in the slower second phase of the turn-off switching. This turn-off switching can be divided into two phases; Phase one is the rapid decrease in current due to the fast interruption of the base current, and phase two is the slow decrease in current due to the stored excess carriers in the epitaxial layer. This slowly decreasing current component is referred to as the tail current because it tails off after the rapid decrease phase.

The tail current is modeled through the parameter $tauhl$, the high level injection life time. The rate of decrease of the tail current is related to the high level injection life time as described by Equation (3.27) below.

$$\frac{d\ln I_t}{dt} = \frac{d\, I_t/dt}{I_t} \approx -\frac{1}{\tau_{hl}}\left(1 + \frac{I_T}{I_k^{\tau}}\right) \tag{3.27}$$

I_k^{τ} is the current above which the current tail time constant is decreased due to the injection of charge carriers into the emitter. Equation (3.28) describes the relationship between $I_k^{\tau}$and the high level injection life time, and the emitter saturation current.

$$I_k^{\tau} = \frac{q^2 A^2 D_p n_i^2}{\tau_{hl} * I_{sne}} \tag{3.28}$$

Equation (3.29) describes the relationship between the high level injection life time $tauhl$ and the emitter to base current.

$$i_{bp} = \frac{qceb}{tauhl_t} + \left(\frac{qceb}{qb}\right)^2 * 4 * \left(\frac{n_b}{n_i}\right)^2 * isne_t \tag{3.29}$$

In this equation $isne_t$ is the emitter electron saturation current, or hole saturation current in case of a p-channel device. $qceb$ is the emitter to base charge, and qb is the background base charge.

3.5. Capacitances and Charges

The gate source capacitance c_{gs} and the oxide capacitance c_{oxd} are implemented in this model as constant parameters. This is a reasonable assumption as these capacitances are a function of the device structure, and the operation point of the device does not affect them. The gate drain capacitance is composed only of the oxide capacitance. The charge on the gate source capacitor qc_{gs} is calculated by simply multiplying the capacitance by the voltage across the capacitance as in Equation (3.30).

$$qc_{gs} = c_{gs} * v_{gs} \tag{3.30}$$

$$c_{gd} = c_{oxd} \tag{3.31}$$

The zero bias junction capacitance cj_0 is the capacitance of a pn junction under zero bias. It is important to calculate the actual junction capacitances under different biasing conditions. It is given by Equation (3.32) below.

$$cj_0 = \left(\frac{\in * nb * q}{2 * pb}\right)^{mj} \tag{3.32}$$

The base collector capacitor is $cbcj$. It is calculated as follows in Equation (3.33). It is a function of the zero bias junction capacitance since it is a biased junction capacitance. This capacitance is responsible for charge storage in the base region and the tail current in the device.

$$cbcj = \left\{ \begin{array}{ll} vds \geq -fc * pb & cbcj = \left(a * cjo * \frac{pb}{pb+vds}\right)^{mj} \\ vds < -fc * pbc & bcj = \left(a * cjo * \frac{\left(1-(1+mj)*fc-mj*\frac{vds}{pb}\right)}{(1-fc)^{mj+1}}\right) \end{array} \right\} \quad (3.33)$$

The drain source capacitance $cdsj$ is the junction capacitance between the drain and the source. It is similar to the base collector capacitor with different dimensions; hence it is calculated as a function of the base collector capacitance. The emitter to collector redistribution capacitance $ccer$ is necessary for the calculation of the redistribution current, which is responsible for supplying the accumulation of charge. This is due to the base width changing with different bias conditions. The emitter to collector capacitance is also calculated as function of the base collector capacitor $cbcj$.

$$cdsj = \frac{cbcj*ads}{a} \quad (3.34)$$

$$ccer = cbcj * \frac{qceb}{3*qb} \quad (3.35)$$

qb is the background base charge.

$$qb = a * w * nb * q \quad (3.36)$$

The charge on the drain source capacitor and the zero bias base charge are calculated from doping, area, permittivity, and voltage as in Equations (3.37) and (3.38), respectively.

$$qcdsj = ads * \sqrt{(2 * \in * (vds + pb) * q * nb)} \quad (3.37)$$

$$qceb0 = a * \sqrt{2 * \in * q * nb * pb} \quad (3.38)$$

$qceb$ is the emitter to base charge. It is the charge responsible for the tail current in the turn off switching of the device. It is found iteratively as per Equation (3.39) below. The meaning of this equation is "find $qceb$ such that$V_{ebj} = V_{eb}$". V_{ebj} is the calculated value of the emitter base voltage. $V_{eb}$is the terminal value of the emitter base voltage.

$$qceb : \ V_{ebj} = V_{eb} \quad (3.39)$$

The calculated emitter base voltage$V_{ebj}$is a nonlinear function of $qceb$. It is calculated in the values section of the model as in Equation (3.40) below.

$$V_{ebj} = \begin{cases} V_{ebdep} & , qceb < \quad 0 \\ \frac{qceb * V_{ebdif}}{qceb0} & , qceb0 < qceb \geq 0 \\ V_{ebdif} & , qceb \geq qceb0 \end{cases} \quad (3.40)$$

The different conditions in (3.40) represent the reverse mode, forward blocking, and forward conduction respectively. The calculated emitter base voltage represents the voltage across the emitter base junction under those different modes.

$V_{ebdif}$is the emitter to base diffusion voltage, and V_{ebdep} is the emitter to base depletion voltage. Equations (3.41) and (3.42) describe how to calculateV_{ebdif} , andV_{ebdep} respectively.

$$V_{ebdif=} k * \frac{temp}{q} * ln\left(\left(\frac{p_0}{(n_i)^2} + \frac{1}{n_b}\right) * (n_b + p_0)\right) - \frac{D_c}{\pi_{nc}} * \ln\left(\frac{p_0 + n_b}{n_b}\right) \quad (3.41)$$

$$V_{ebdep} = \ p_b - \frac{(qceb - qceb0)^2}{2 * q * n_b * \in * a^2} \quad (3.42)$$

3.6. Model Current Components

After the conductivity modulation has been accounted for, and the conductivity modulated resistance has been calculated, Equation (3.43) is used to calculate the total emitter current.

$$i_{rb} = \frac{V_{ae}}{r_b} \qquad (3.43)$$

The emitter to collector current i_{cp} is the emitter current component that does not depend on the time derivative of the emitter collector voltage. It is calculated in Equation (3.45). The term b is the ambipolar mobility ratio; it is the ratio of the mobility of electrons to that of holes. dp is the hole diffusivity, or the diffusion coefficient.It is governed by the Einstein relation.

$$dp = mu_p * v_{th} \qquad (3.44)$$

$$i_{cp} = \left(\frac{b}{1+b}\right) * i_{rb} + \left(\frac{b}{1+b}\right)\left(\frac{4*dp*qceb}{w^2}\right) \qquad (3.45)$$

The emitter collector redistribution currenti_{ccer} represents the component of the collector current that is dependent on the derivative of the base collector voltage as it varies with the variation of the base boundary while changing the applied voltage. It is responsible for the accumulation of charge that is due to the varying base width. It is calculated in Equation (3.46).

$$i_{ccer} = ccer * dvbcdt * wvds \qquad (3.46)$$

Finally, the total collector current is calculated by adding the dc current and the redistribution current as described below in Equation (3.47).

$$i_{cc} = i_{cp} + i_{ccer} \qquad (3.47)$$

The drain gate capacitor current, i_{cdg} is calculated in the same fashion as the emitter collector redistribution current. Equation (3.48) is used to calculate the drain gate capacitor current.

$$i_{cdg} = cgd * dvdgdt * wvds \tag{3.48}$$

Icp represents the component of the base current that does not depend on the time derivative of the base charge $qceb$. $Ibp$is described in Equation (3.29).

The MOSFET channel drain source current, $I_{mos}$is described in the code fragment in Figure3.3 below. After the MOSFET drain source current is calculated, it is reduced to account for the transverse electric field mobility reduction discussed earlier. Then, a minimum slope of $g_{min}$is implemented to ensure that the model converges.

```
if (vds >= 0) {
        if (vgs > vt_t) {
                if (vds <= (vgs − vt_t)/kf_t) {
                        imos = kp_t * kf_t * (vgs − vt_t −  kf_t * vds/2) * vds
                        }
                else imos = 0.5 * kp_t * (vgs − vt_t) ** 2
        else imos = 0
imos = imos + model−> gmin * m_channel * (vgs + vds)
if(vgs >= vt_t )      mufact = 1 + theta_t * (vgs − vt_t)
else                  mufact = 1
imos = imos/mufact
}
else {
        if (m_channel * (vgs − vds) > vt_t) {
                if (−vds <= (m_channel * (vgs − vds) − vt_t)/kf_t) {
                      imos = kp_t * kf_t * (m_channel * (vgs − vds) − vt_t + kf_t * vds/2) * vds
                        }
                else imos = −0.5 * kp_t * (m_channel * (vgs − vds) − vt_t) ** 2
                }
        else imos = 0
}
imos = imos + model−> gmin * m_channel * (vgs − vds)
if (m_channel * (vgs − vds) >= vt_t )  mufact = 1 + theta_t * m_channel * ((vgs − vds) − vt_t)
else                                    mufact = 1
imos = imos/mufact
```

Fig. 3.3. MOSFET current I_{mos} code fragment.

3.7. Temperature Effects

Power semiconductor devices conduct a relatively high current when in conduction mode. This high current will cause the device to heat up. For SiC devices in particular, power devices are operated at high temperature; thus, any power semiconductor devices should take into account the complete temperature range of operation. This is done by considering temperature dependence of the material properties, and physical effects as well as temperature scaling of the parameters.

3.7.1. Temperature Dependence

Material properties, such as the intrinsic carrier concentration, change with temperature. Besides material properties changing with temperature, some effects that do not exist at lower temperatures, can exist in the device at higher temperatures. Mobility reduction due to lattice vibration that occurs at high temperatures is an example of these effects.

Table 3.2 gives a list of the temperature dependent material properties. It is worth noting that the temperature dependence of some of these properties varies from silicon to silicon carbide, and from n-type to p-type materials. The equations governing those properties are presented in the relevant sections.

Table 3.2.Temperature Dependent Properties.

Property	Description
Mun	electron mobility
Mup	hole mobility
Ni	intrinsic carrier concentration
Vth	thermal voltage

Below are the temperature dependent Equations of the properties in Table 3.2 above.

$$v_{th} = k * \frac{temp}{q} \tag{3.49}$$

Where k is the Boltzmann constant in eV/K.

For Si:

$$n_i = 3.88 * 10^{16} * \frac{temp^{1.5}}{e^{\frac{7000}{temp}}} \tag{3.50}$$

For 4H-SiC

$$n_i = 4.082 * 10^{16} * \frac{temp^{1.5}}{e^{\frac{7000}{temp}}} \tag{3.51}$$

3.7.2. Temperature Scaling

Besides temperature dependence, temperature scaling is also needed in the model. Temperature scaling is different than temperature dependence as it is deals with fitting parameters rather than physical properties or physical effects. Temperature scaling is done by extracting the model parameters at room temperature, then scaling those parameters as they are expected to vary with temperature inside the model. The model user should not need to change the parameters to simulate the device at different temperatures. Changing the simulation temperature should inherently scale the parameters inside the model. This is normally done by first extracting the model parameters at a couple of different temperatures. Then, a relationship of the parameter variance with temperature is extracted. The relationship between each temperature dependent parameter and temperature is extracted by plotting the parameter against temperature and then fitting the resulting curve to an empirical equation that performs the

temperature scaling for the parameter. In Table 3.3, the temperature scaled parameters are listed with their temperature scaling coefficients.

Even though the parameters that are temperature scaled represent first or second order effects that can be explained physically, the equations that are used to scale them over temperature are completely empirical. The parameter temperature scaling can be either linear or nonlinear. The linear temperature scaling is expressed by adding a component to the parameter that is a function of the difference between the operation temperature and the nominal temperature. The nonlinear temperature scaling is expressed by multiplying the parameter by the ratio of the operation temperature to the nominal temperature raised to the power of temperature coefficient of that specific parameter. The equations that are used for temperature scaling are presented below, divided into linear and nonlinear.

Table 3.3. Temperature Scaled Parameters.

Parameter	Description	Temperature Scaled Parameter	Temperature Coefficient
$\boldsymbol{kp}$	MOSFET channel Transconductance in saturation region	kp_t	$kptexp$
$\boldsymbol{kf}$	Ratio of kp in triode region to that in the saturation region	kf_t	$kftexp$
$\boldsymbol{Theta}$	Transconductance reduction factor due to transverse electric field in the MOSFET	$theta_t$	$thetatexp$
$\boldsymbol{tauhl}$	High level excess carrier lifetime	$tauhl_t$	$tauhltexp$
$\boldsymbol{isne}$	Emitter electron saturation current	$isne_t$	$isnetexp$
$\boldsymbol{vt}$	MOSFET channel threshold voltage	vt_t	$vttco$
$\boldsymbol{vtd}$	gate drain depletion threshold	vtd_t	$vtdtco$
$\boldsymbol{bvn}$	Avalanche multiplication exponent	bvn_t	$bvntexp$
$\boldsymbol{bvf}$	Avalanche uniformity factor	bvf_t	$bvftexp$

Nonlinear temperature scaling:

$$k_{pt} = k_p * \left(t_{rat}{}^{k_{ptexp}}\right) \quad (3.52)$$

$$k_{ft} = k_f * \left(t_{rat}{}^{k_{ftexp}}\right) \quad (3.53)$$

$$tauhl_t = tauhl * \left(\frac{1}{t_{rat}}\right)^{tauhltexp} \quad (3.54)$$

$$bvn_t = bvn * \left(\frac{1}{t_{rat}}\right)^{bvntexp} \quad (3.55)$$

$$bvf_t = bvf * \left(\frac{1}{t_{rat}}\right)^{bvftexp} \quad (3.56)$$

$$theta_t = theta * \left(\frac{1}{t_{rat}}\right)^{thetatexp} \quad (3.57)$$

$$isne_t = isne * \left(\frac{1}{t_{rat}}\right)^{isnetexp} * e^{1.4*10^4*\left(\frac{1}{tnom}-\frac{1}{temp}\right)} \quad (3.58)$$

$$t_{rat} = \frac{tnom}{templim} \quad (3.59)$$

t_{rat} is the ratio of the operating temperature to the nominal temperature used for the nonlinear temperature scaling. The nominal temperature is set at room temperature.

Linear temperature scaling:

$$vt_t = v_t + vttco * (temp - tnom) \quad (3.60)$$

$$vtd_t = vtd_t + vtdtco * (temp - tnom) \quad (3.61)$$

The specific steps to perform temperature scaling are listed as follows:

- Turn off temperature scaling by setting the temperature scaled parameter equal to the original parameter
- Set $tnom$ to room temperature
- Perform parameter extraction for the temperature measurements at each temperature
- Plot each parameter with respect to temperature
- Fit the parameter over temperature curves to the equations presented above

It is worth noting that the temperature dependence has been done using either temperature ratio, or temperature difference. If absolute temperature was used for temperature scaling it would have been harder to turn off temperature scaling without affecting the temperature dependent properties.

3.8.The Equations Section

The equations governing branch currents and the independent variables go in the last section of the model, the equations section. In the equations section the current components are added together to form the respective branch currents. Also the equations governing the variables that are solved for iteratively are in the equations section. The variables are calculated iteratively until a certain condition is met. The equations section is divided into two parts, one for p-channel devices and the other for n-channel devices. The equations section of this model is shown below in Figure 3.4.

The equations section is the only section of the MAST model template where a differential term is allowed. Therefore some of the current components that are in Figure 3.4 appear in the equations section for the first time in the model.

```
equations {
if(channel == p_channel) {
        i(g->k) +=   - d_by_dt(qcgs)
        i(d->g) += -icdg
        if(model->bvf == inf)  i(d->k) += -imos - d_by_dt(qcdsj)
                else {
                        i(d->k) += -imos - imult - vds/rds - d_by_dt(qcdsj)
                }
        i(e->k) += -icc
        i(e->d) += -ibp - d_by_dt(qceb)
        i(a->e) += -irb
        vdgx:d_by_dt(vdgx_w) = dvdgdt
        vdsx:d_by_dt(vdsx_w) = dvbcdt
        qceb:vebj = veb - model->voff
        }
else {
        i(g->k) +=   d_by_dt(qcgs)
        i(d->g) += icdg
        if(model->bvf == inf)  i(d->k) += imos + d_by_dt(qcdsj)
                else {
                        i(d->k) += imos + imult + vds/rds + d_by_dt(qcdsj)
                }
        i(e->k) += icc
        i(e->d) += ibp + d_by_dt(qceb)
        i(a->e) += irb
        vdgx:d_by_dt(vdgx_w) = dvdgdt
        vdsx:d_by_dt(vdsx_w) = dvbcdt
        qceb:vebj = veb + model->voff
        }
}
```

Fig. 3.4. The equations section.

CHAPTER 4

Characterization and Parameter Extraction

4.1 IGBT Characteristics

4.1.1 Steady state characteristics

The steady state characteristics of an IGBT are the output characteristics and the transfer characteristics. The output characteristics are obtained by plotting the collector current verses the collector-emitter voltage at a constant gate voltage. The output characteristics are normally displayed as a family of curves where the output characteristics are plotted for several different gate voltages. The shape of the output characteristics of an IGBT is similar to the shape of the characteristics of MOSFETs with an offset voltage. The voltage offset is due to the additional junction in the IGBT structure preventing the voltage across the IGBT to drop below the voltage of a diode when in conduction mode. As the collector emitter voltage increases the internal collector base voltage is increased after the voltage exceeds the built in voltage the collector current starts increasing rapidly provided that the gate voltage is above the threshold voltage. The current will keep increasing with increasing voltage to a point where the MOSFET channel gets pinched off. After pinch off the current does not increase with increasing voltage, and the device is said to be saturated. The saturation current varies with a varying gate voltage. The higher the gate voltage is the higher the saturation current, causing the entire output family of saturation current curves to shift upwards. Pinch off or saturation occurs when collector emitter voltage is greater than the gate voltage minus the channel threshold voltage, and the collector current becomes independent of any increase of the voltage applied to the drain.

The transfer characteristics are obtained by plotting the collector current versus the gate voltage at a constant collector emitter voltage. The transfer characteristics are often referred to as the transconductance characteristics as the gradient at any given point on the curve would represent the transconductance. As the gate voltage increases beyond the gate threshold voltage, the MOSFET channel starts to form. Once the MOSFET channel is formed the current starts increasing rapidly with the increase of gate voltage. As mentioned above the higher the gate voltage the higher the output current saturation is, but as the gate voltage is increased to a certain point a flattening in the increase of the saturation current is observed. This is due to the interaction of the saturation effect in MOSFET component of the IGBT and the gain limiting in the BJT component of the IGBT.

4.1.2 Switching characteristics

Because IGBTs are voltage controlled devices the control signal is a voltage signal, and is applied at the gate of the device. A gate signal large enough needs to be applied at the gate to insure that the device operates in the linear region with low voltage drop rather than in the saturation region.

Turning on the IGBT requires applying a large gate emitter voltage across the device. Even though IGBTs are gate controlled devices, the turn on switching speed of the device depends on the gate current rather than the gate voltage. Increasing the gate voltage increases the saturation limit on the device but it does not influence the turn on speed of the device. IGBT turn on can be viewed as a charging capacitor, where turning on the IGBT requires the charging of the gate emitter capacitance to the applied gate emitter voltage. The larger the current is the faster the device will turn on.

Turning off the device requires the removal of the gate voltage. A series gate resistance is required to provide a path for the gate emitter capacitor to discharge as the discharge of the gate emitter capacitor is required to turn the device off. The gate series resistance has an upper limit and a lower limit. The lower limit on the gate resistance is to limit the current flowing through the gate as the rated current through the gate is on the order of milliamps. The upper limit on the gate series resistance is to limit its influence on the turn off speed as it controls the fast current decay phase of the turn off transition.

4.2 Parameter extraction

Parameter extraction was accomplished using Certify. Certify is a fitting tool that works with the simulator to extract the parameters of the model. Certify supports the Saber and Spectre simulators. The netlist, top level model, and the parameter extraction recipe need to be specified for Certify. The parameter extraction recipe consists of the analysis that needs to be done, parameters to output, and signals to fit along with the target files. Once Certify has the needed files and the recipe it launches its own browser. In the browser the user loads the target files and runs the simulation based on a preliminary guess of the parameters. Then the user zooms into specific regions and fits a specific subset of the parameters that influences the characteristics of a specific region. It is noteworthy that the extracted parameters are not exact as they are based on fitting rather than on physical analysis. A more accurate parameter extraction method was developed in [7].

Table 4.1. Temperature Scaled Parameters.

Parameter	Description
wb	Metallurgical base width
nb	Epitaxial layer doping concentration
a	Device active area
agd	Gate drain overlap active area
rs	Intrinsic series resistance
kph	MOSFET channel transconductance in linear region
kpl	Transconductance in linear region for lower currents
$kptexp$	Temperature exponent for kp
kfh	Ratio of kp in saturation region to that in the linear region
kfl	Kf for lower currents
$kftexp$	Temperature exponent for kf
$Theta$	Transconductance reduction factor due to transverse electric field in the MOSFET
$thetatex$	Temperature exponent for Theta
$tauhl$	High level excess carrier lifetime
$tauhltex$	Temperature exponent for $tauhl$
$isne$	Emitter electron saturation current
$isnetexp$	Temperature exponent for $isne$
vth	MOSFET channel threshold voltage
vtl	Low thershold voltage
$vttco$	Temperature coefficient for vt
vtd	Gate drain depletion threshold
$vtdtco$	Temperature coefficient for vtd
bvn	Avalanche multiplication exponent
$bvntexp$	Temperature exponent for bvn
bvf	Avalanche uniformity factor
$bvftexp$	Temperature exponent for bvf
cgs	Gate to source capacitance
$coxd$	Gate drain oxide capacitance
$tnom$	Temperature for which parameters apply
$alpha$	Temp. exponent for mobilities
$gmin$	Minimum slope for MOSFET current
fc	Forward-bias non-ideal junction capacitance coefficient.
mj	Junction grading coefficient
fc_bvcb	Breakdown voltage coefficient
fc_neff	Concentration ratio coefficient

Certify optimizes the fitting by means of error minimization. Therefore the fitting is based on extracting the parameters from the device's characteristics and no manufacturing details about the device are required. This is due to the fact that circuit designers do not always have the internal details of the devices as it is not commercially practical for the manufacturer to release such information.

A common practice in modeling is to perform the fitting of the dc transfer characteristics on a semi-logarithmic scale as it eases the extraction of some of the parameters in exponential equations. Using a semi-logarithmic scale for fitting produces more accurate fits as the error between the simulation and the actual data would not be misleading at lower currents.

In low voltage field effect devices the drain-source operating voltage is normally low. And the difference between the operation voltage and the threshold voltage is very low, causing the device to operate in the subthreshold mode at weak inversion of the channel, thus modeling the subthreshold region in the device characteristics is very important. This raises the need for performing the fitting in a semi-logarithmic scale for improved accuracy.

Power semiconductor devices are primarily used as switches, thus the device is normally operated either in the strong inversion mode, or in the blocking mode. Since the device is not normally operated in the weak inversion mode, it is not as critical to do the fitting in a semi-logarithmic scale as it is for low power devices. The fitting was done in a semi-logarithmic scale to ensure more accurate fitting.

Figure 4.1 below is a representation of the circuit schematic used to obtain the switching waveforms of the p-channel device. Figure 4.2 below is a representation of the schematic used to obtain the steady state characteristics of the device.

A complete list of the model parameters is given in Table 4.1 below. Figure 4.3 and Figure 4.4 shows generic output and transfer characteristics showing which parameters need to fit which regions. The parameter extraction starts with the extraction of low current threshold voltage VTL and the Transconductance gain parameter KPL from region I of the transfer characteristics where the device has barely turned on. Then the high current threshold voltage VTH and the transconductance gain KPH are extracted from the linear slope in region II of the transfer characteristics. The current reduction factor theta can be extracted from region III. After the parameters have been extracted from the transfer characteristics; they are refined by fitting the output characteristics.

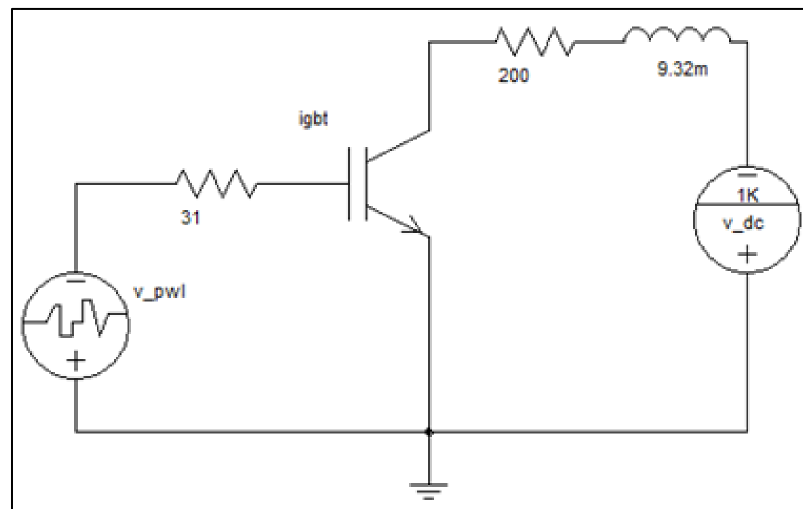

Fig. 4.1. Circuit schematic used for switching measurements.

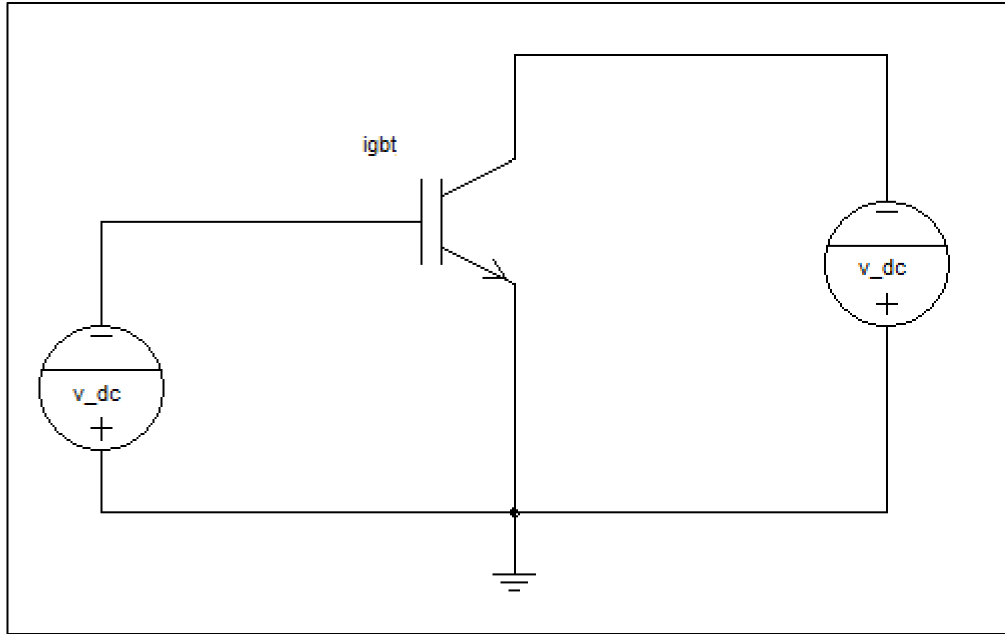

Fig. 4.2. Circuit schematic used for steady state characterization.

Figures 4.5 through 4.8 show the simulated and measured steady state output, and transfer characteristics for a 4H-SiC 15 kV p-channel IGBTs from Cree Inc. The data was provided by Cree Inc. for the purpose of model development. Figures 4.9 and 4.10 show the simulated and measured switching characteristics for the device. The model was also validated for 4H-SiC n-channel IGBTs. Figures 4.11 through 4.14 show the fits for the n-channel device. Table 4.2 below shows the extracted parameter values.

Table 4.2 Extracted Parameters for n-hannel and p-channel 4H-SiC IGBTs

Parameter	Value		Parameter	Value	
	N-IGBT	P-IGBT		N-IGBT	P-IGBT
$\boldsymbol{wb}$	8.35e-3	8.38e-3	$vttco$	-0.02	-0.01
$\boldsymbol{nb}$	200t	200t	$isne$	10f	10f
$\boldsymbol{a}$	0.1	0.1	$isnetexp$	0	0
$\boldsymbol{agd}$	0.05	0.05	bvf	1	1
$\boldsymbol{rs}$	0.004	0.01	$bvftexp$	0	0
$\boldsymbol{kph}$	2	1.2	cgs	2n	2n
$\boldsymbol{kptexp}$	0.8	0.6	$coxd$	1n	1n
$\boldsymbol{kf}$	0.45	0.32	$tnom$	300	300
$\boldsymbol{kftexp}$	0.1	0.05	$alpha$	-2.7	-2.5
$\boldsymbol{Theta}$	0.005	0.01	$tauhl$	0.55u	0.62u
$\boldsymbol{thetatexp}$	0.002	0.004	$tauhltexp$	0.24	0.2
$\boldsymbol{vth}$	7.5	9.5			

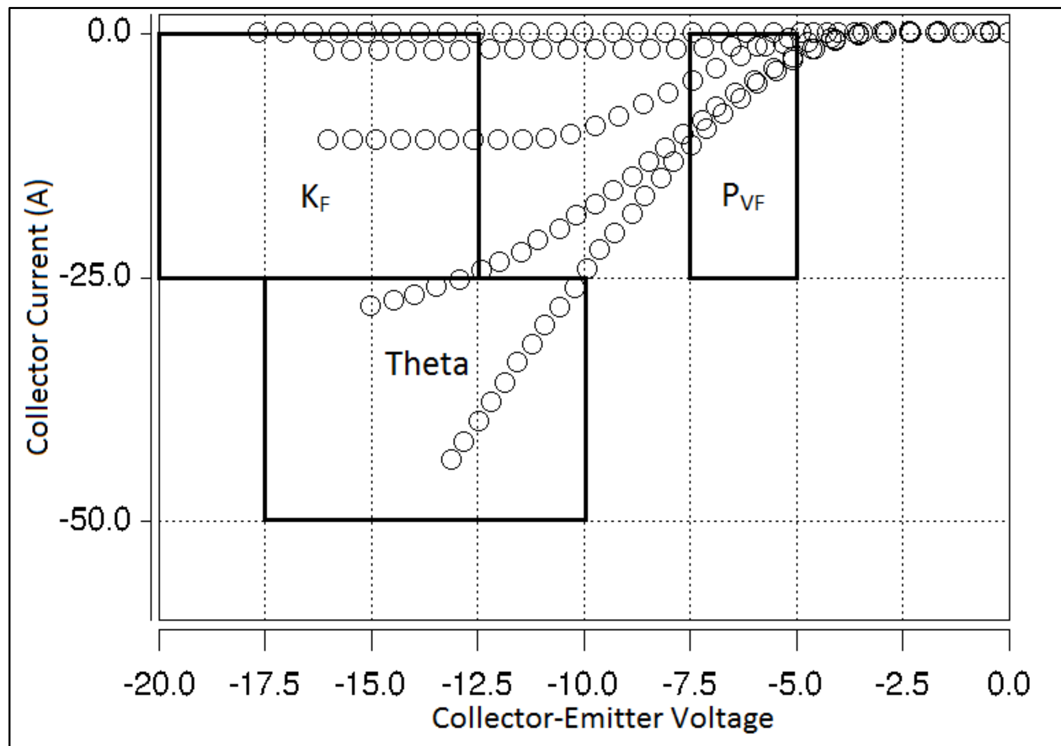

Fig. 4.3. P-channel IGBT generic output characteristics

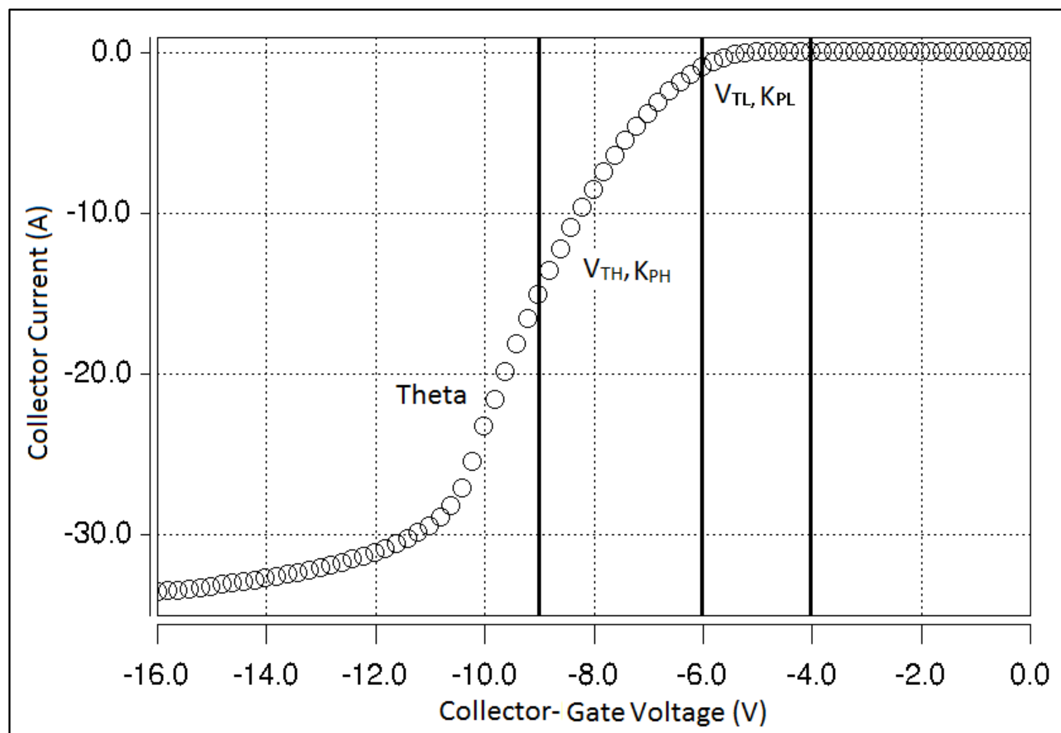

Fig. 4.4. P-channel IGBT transfer Characteristics.

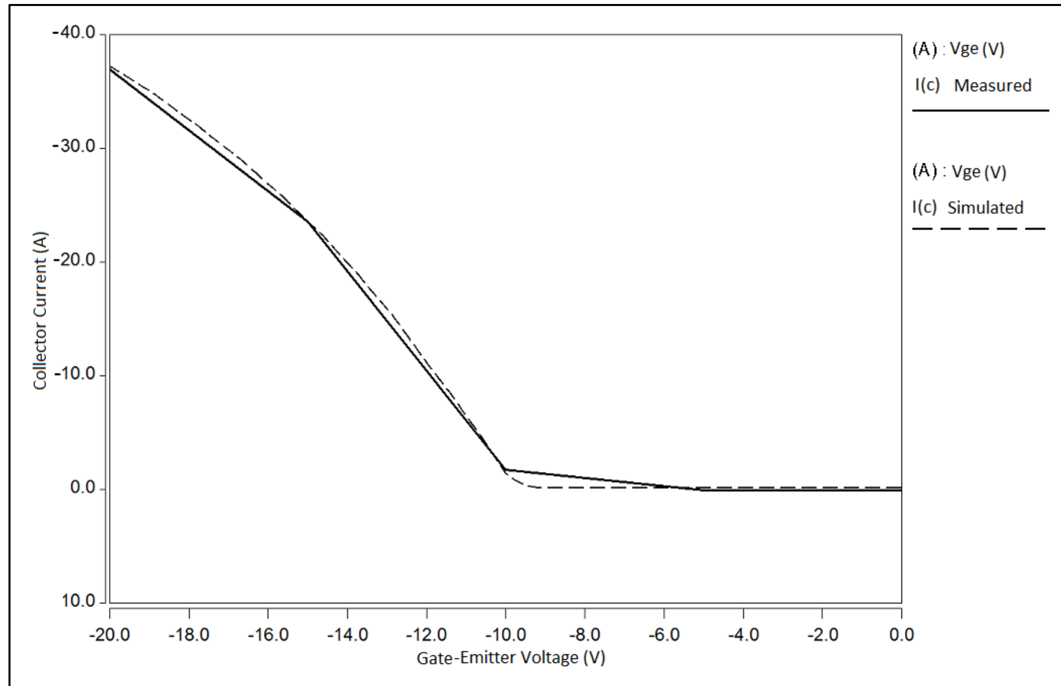

Fig. 4.5. Measured and simulated transfer characteristics for a 15kV 4H-SiC p-channel IGBT.

Figure 4.5 shows the measured and simulated transfer characteristics for the 15kV 4H-SiC p-channel device. The measured results consist of four points only as the transfer characteristics were not provided by Cree. The transfer characteristics were extracted from the output characteristics as the output characteristics were provided for several gate voltages. Figure 4.5 shows a good fit as the simulation results fits all four data points extracted. The transfer characteristics are typically obtained by measuring the output current while sweeping the gate voltage at a constant collector-emitter voltage. This measurement is normally taken using a curve tracer like the Tektronix 371B. Different leads are used for force and sense to minimize the parasitic resistance in the circuit.

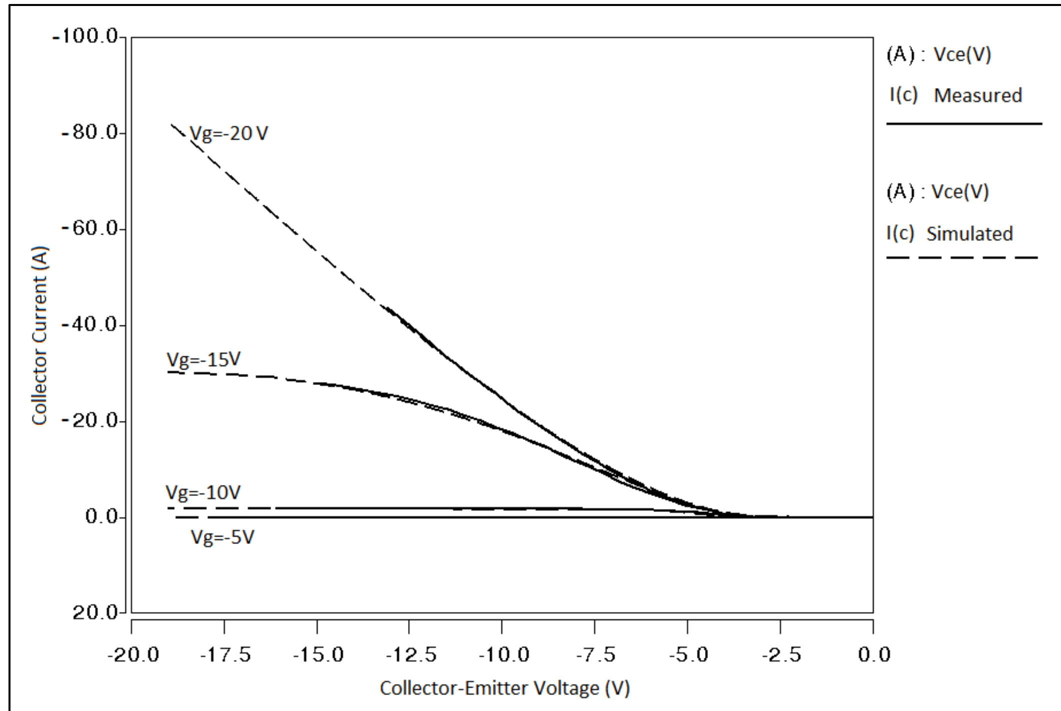

Fig. 4.6. Measured and simulated output characteristics for a 15kV 4H-SiC p-channel IGBT.

Figure 4.6 shows the measured and simulated output characteristics for a 4H-SiC device. The output characteristics are provided for gate voltages of 5V, 10V, 15V, and 20V at room temperature. The saturation affect mentioned earlier can be observed for gate voltage 10V and 15V. The 5V curve coincides with the x-axes because the gate threshold voltage is 9.5V. A very good fit is obtained for the output characteristics. The output characteristics are obtained by measuring the output current while sweeping the collector-emitter voltage for constant gate voltages. This measurement is also done using a curve tracer.

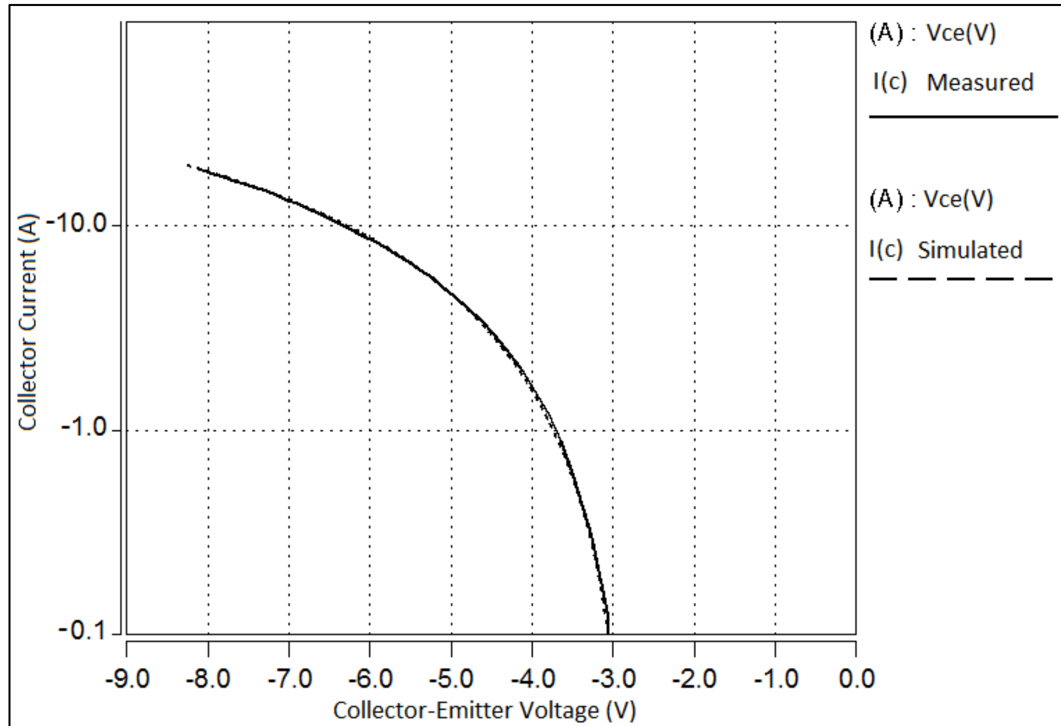

Fig. 4.7. Fitted output characteristics at Vg=15V for a 15kV 4H-SiC p-channel IGBT in log scale.

Figure 4.7 shows the measured and simulated output characteristics fit in log scale for a gate voltage of 15V at room temperature for the 4H-SiC device. It is the same fit provided in Figure 4.6 displayed in log scale to show the quality of the fit.

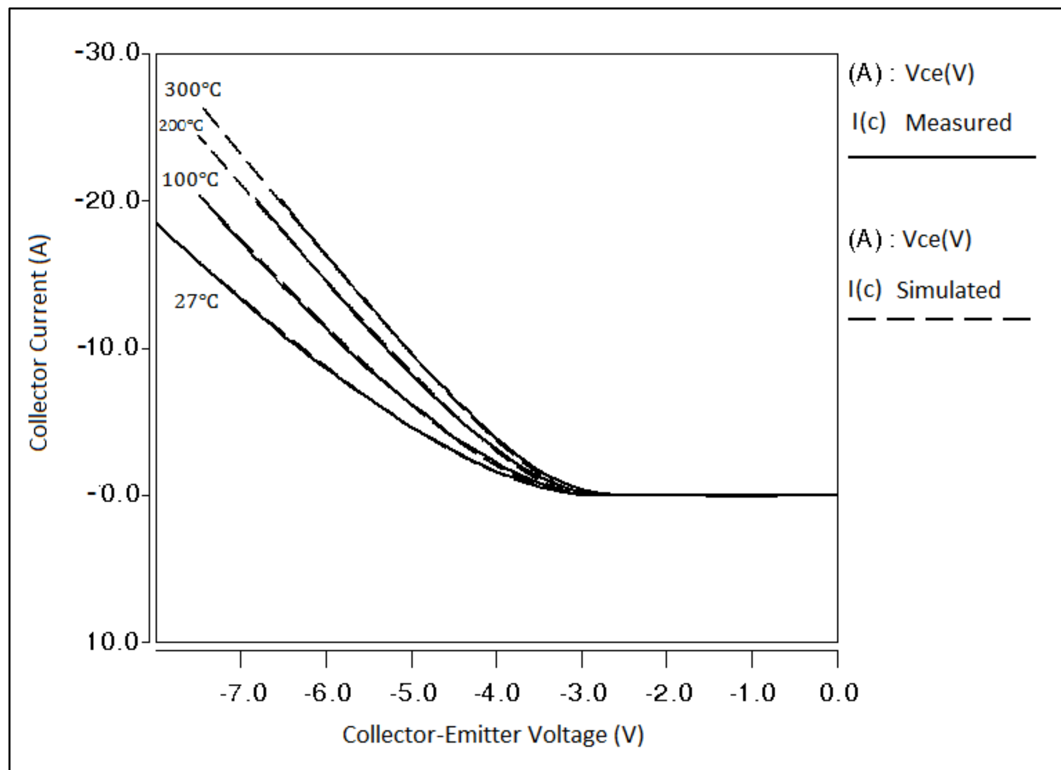

Fig. 4.8. Fitted output characteristics for a 15kV 4H-SiC p-channel IGBT at different temperatures.

Figure 4.8 shows the measured and simulated output characteristics at 15V gate voltage over temperature for the 4H-SiC device. The temperature was varied from room temperature to 300° C. It can be noticed that the threshold voltage of the p-channel devices has negative temperature coefficient opposite of n-channel devices.

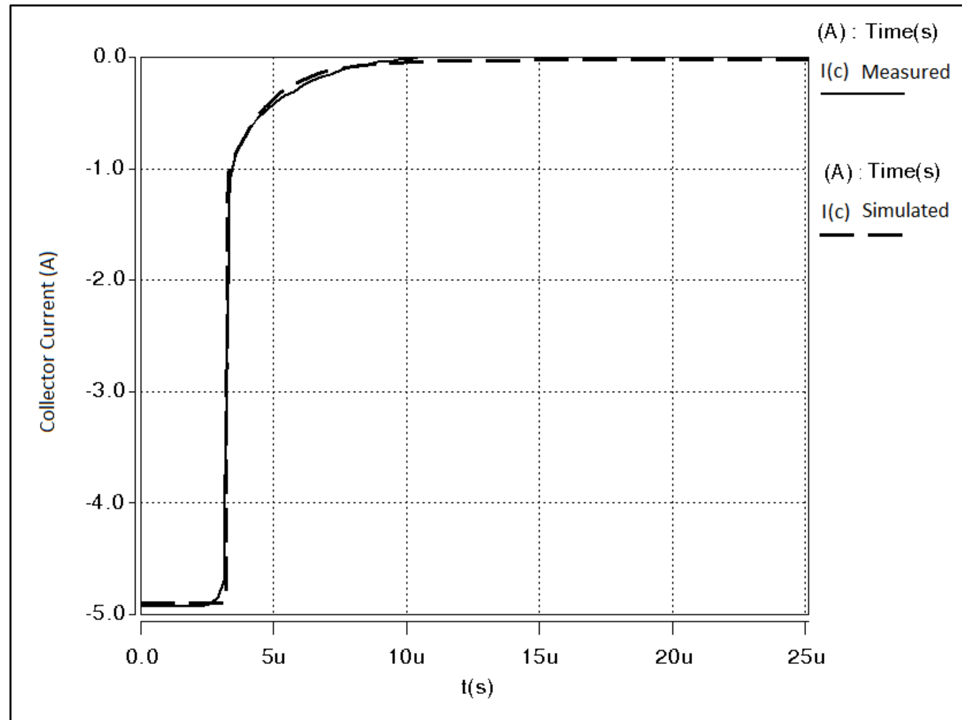

Fig. 4.9. Measured and simulated current switching waveform for a 15kV 4H-SiC p-channel IGBT.

Figure 4.9 shows the measured and simulated current switching waveform for the 4H-SiC p-channel device. The fast current decay phase and the current tail phase of the turn off switching can be clearly identified. The fast decay phase occurs in nanoseconds, the current tail takes more than 5 microseconds to decay to zero. It is noteworthy that the y-axes scale is negative as this is a p-channel device and the current follows from emitter to collector. The figure shows that a good fit has been achieved. This measurement is done using the circuit in Figure 4.1.

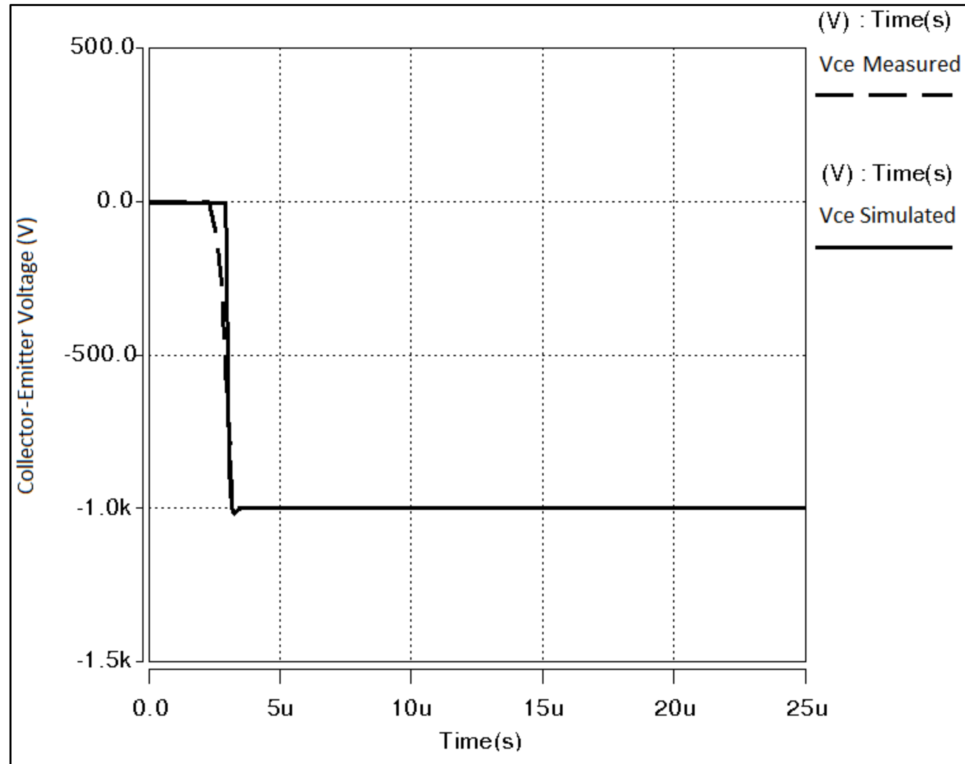

Fig. 4.10. Measured and simulated current switching waveform for a 15kV 4H-SiC p-channel IGBT.

Figure 4.10 shows the simulated and measured voltage switching waveforms for the 4H-SiC devices. Low voltage appears across the device when it's on, then when the device is turned off the full voltage applied by the power source is blocked by the device and the voltage across the device rises to 1kV. This measurement is also done using the circuit in Figure 4.2.

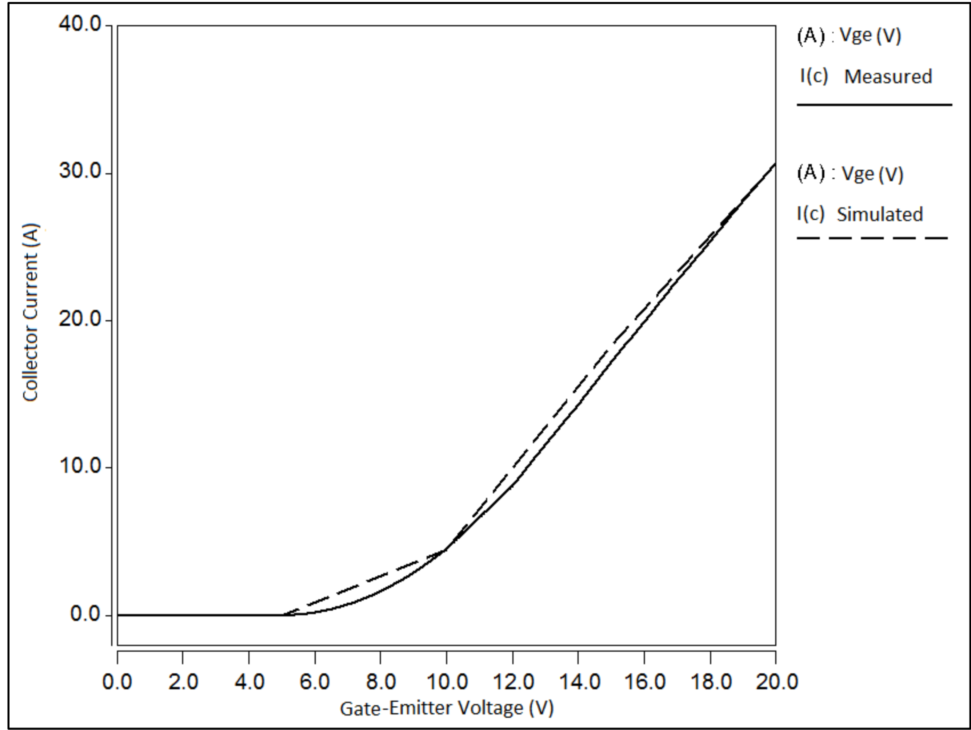

Fig. 4.11. Measured and simulated transfer characteristics for a 15kV 4H-SiC n-channel IGBT.

Figure 4.11 shows the measured and simulated transfer characteristics for the 15kV 4H-SiC n-channel device. This device has a gate threshold voltage of 7.5V. A good fit for the transfer characteristics has been achieved.

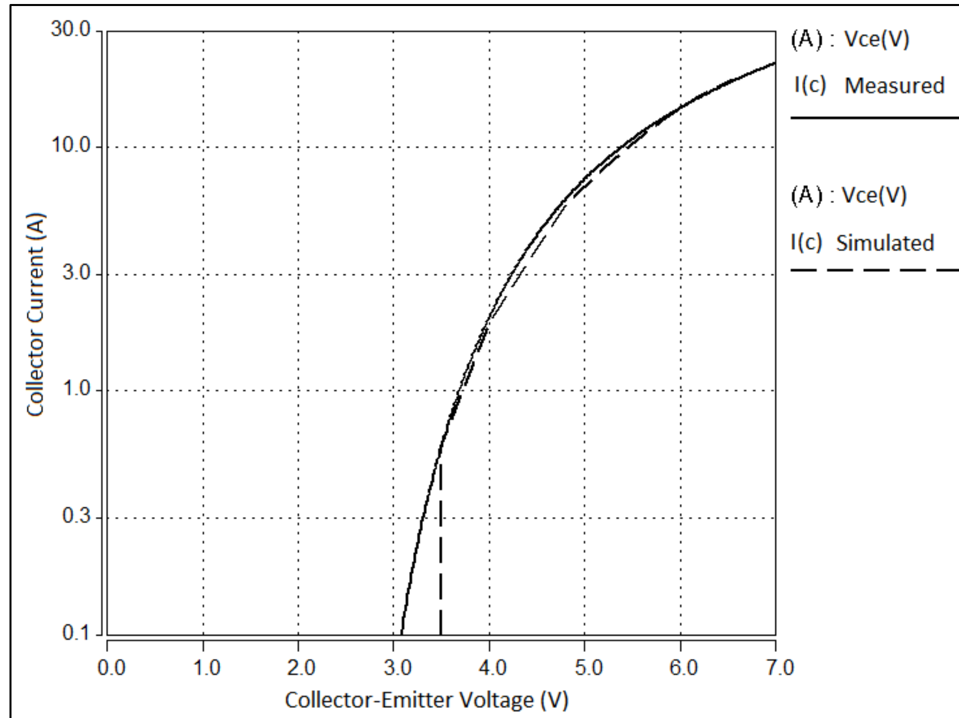

Fig. 4.12. Fitted output characteristics at Vg=15V for a 15kV 4H-SiC n-channel IGBT in log scale.

Figure 4.12 shows the simulated and measured output characteristics of the 15kV 4H-SiC n-channel device in log scale at room temperature. This output characteristic was obtained at a gate voltage of 15V.

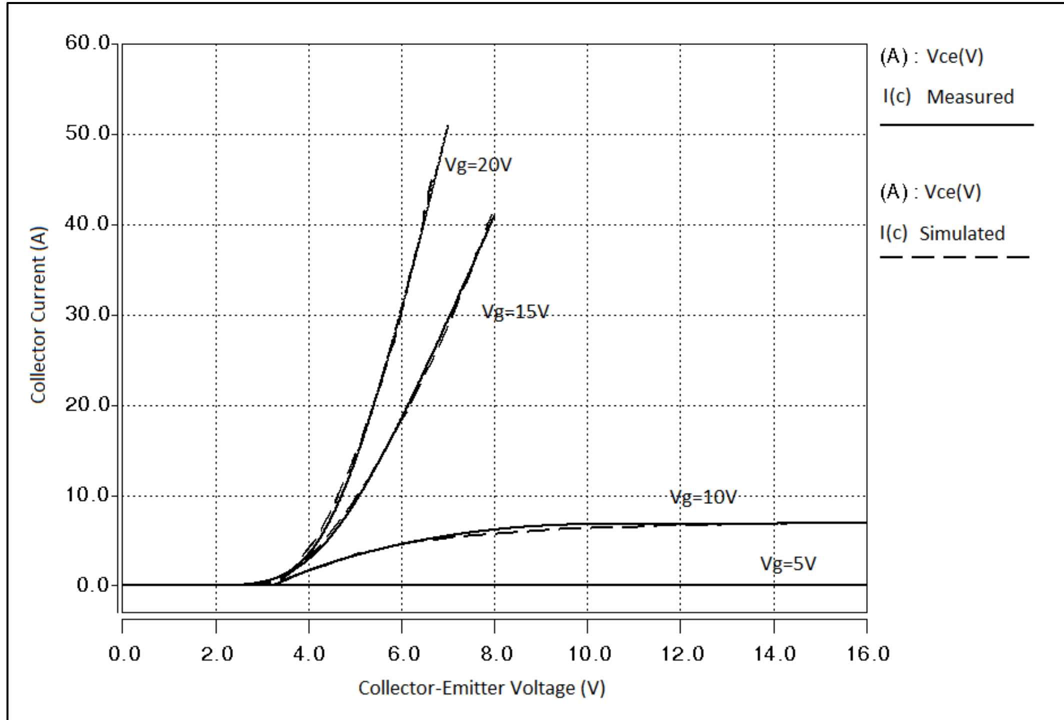

Fig. 4.13. Measured and simulated output characteristics for a 15kV 4H-SiC n-channel IGBT.

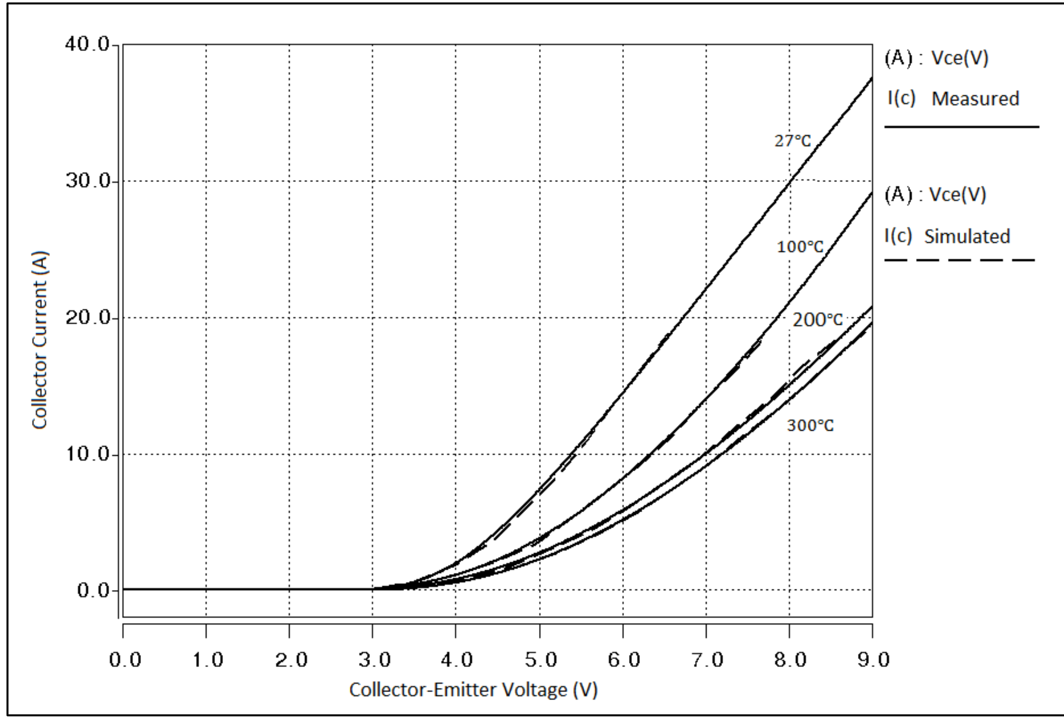

Fig. 4.14. Fitted output characteristics for a 15kV 4H-SiC n-channel IGBT at different temperatures.

Figures 4.13 and 4.14 show the fit for the output characteristics of the 15 kV device at different gate voltages at room temperature, and different temperatures at a gate voltage of 15V respectively. The positive temperature coefficient of the threshold voltage can be clearly seen in Figure 4.14.

CHAPTER 5

Conclusions and Future Work

5.1. Conclusions

A physics-based IGBT model capable of predicting the characteristics of Si and SiC IGBTs for both n-channel and p-channel structures has been presented. This is the first IGBT model that predicts the behavior of p-channel IGBTs and SiC IGBTs. IGBTs are the preferred devices when it comes to medium voltage, medium frequency applications. SiC IGBTs and more specifically p-channel SiC IGBTs are penetrating the high voltage application range competing with GTOs. The projection for SiC p-channel IGBTs is to have 15 kV-100A devices commercially available by 2013 [27]. Those new SiC p-channel devices will mainly be attractive for smart grid systems [28]. These expectations, projections, and goals mentioned above give the relevance of the work presented in this thesis. The importance of the model comes from the importance of the device it models and the need of accurate models suitable for circuit simulation.

Once a good model has been developed circuits can be simulated and prototyping can be avoided. A model's importance is measured by the impact it has in the industry. A model's impact in the industry is dependent on the quality of the model, and more importantly the need for the device it models. The Hefner IGBT model is estimated to have an annual impact of $40M in the industry. The unified IGBT model presented here has the potential to impact the industry similar to the Hefner model as SiC IGBTs and p-channel SiC IGBTs have promising future.

Simulation fits for Cree's 12 kV SiC p-channel IGBTs were presented. The model was experimentally validated for steady-state and switching characteristics. The model was validated

over temperature up to 125 °C for silicon and 225 °C for SiC. The validation process was done on R&D devices that were made available through Cree, as SiC p-channel IGBTs are not available commercially.

5.2 Future Work Recommendations

5.2.1 Electro-thermal Modeling

IGBTs modular configurations are very common, as they provide off the shelf solutions to high voltage applications [27]. Thermal management is of great importance when building power electronic modules. Electro-thermal modeling and self-heating models are desirable when using modular configurations for power electronic applications. It is recommended that the model developed in this work be extended to obtain an electro-thermal version that includes self-heating effects.

5.2.2 Automation of IGBT Characterization

Characterization is a very important step in device modeling. Characterization helps in understanding the physics, and the behavior of the device before the modeling effort even begins. And after the model is developed and ready, characterization is necessary for the purpose of validation. The characterization process can be tedious and time consuming. Most curve tracers, including the one used to perform some the characterization work of this thesis (Tektronix 371B), can be controlled through a computer for setting up the test, and for data acquisition. It is recommended that static characterization be automated as the characterization process is not device specific.

Bibliography

[1] B. J. Baliga, "Power junction gate field controlled devices," in *Electron Devices Meeting, 1979 International*, 1979, vol. 25, pp. 76- 78.

[2] S. Teszner and R. Gicquel, "Gridistor—A new field-effect device," *Proceedings of the IEEE*, vol. 52, no. 12, pp. 1502- 1513, Dec. 1964.

[3] J. Nishizawa, T. Terasaki, and J. Shibata, "Field-effect transistor versus analog transistor (static induction transistor)," *IEEE Transactions on Electron Devices*, vol. 22, no. 4, pp. 185- 197, Apr. 1975.

[4] M. F. Chang et al., "Comparison of n and p channel IGTs," in *Electron Devices Meeting, 1984 International*, 1984, vol. 30, pp. 278- 281.

[5] V. K. Khanna, *The insulated gate bipolar transistor: IGBT theory and design*. IEEE Press, 2003.

[6] A. K. Agarwal, "An overview of SiC power devices," in *2010 International Conference on Power, Control and Embedded Systems (ICPCES)*, 2010, pp. 1-4.

[7] Kuang Sheng, B. W. Williams, and S. J. Finney, "A review of IGBT models," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1250-1266, Nov. 2000.

[8] A. R. HEFNER, "CHARACTERIZATION AND MODELING OF THE POWER INSULATED GATE BIPOLAR TRANSISTOR," University of Maryland College Park, United States -- Maryland, 1987.

[9] A. N. Githiari, B. M. Gordon, R. A. McMahon, Zhong-Min Li, and P. A. Mawby, "A comparison of IGBT models for use in circuit design," *IEEE Transactions on Power Electronics*, vol. 14, no. 4, pp. 607-614, Jul. 1999.

[10] P. O. Lauritzen, G. K. Andersen, and M. Helsper, "A basic IGBT model with easy parameter extraction," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*, 2001, vol. 4, pp. 2160-2165 vol. 4.

[11] A. Hefner and S. Bouche, "Automated parameter extraction software for advanced IGBT modeling," in *The 7th Workshop on Computers in Power Electronics, 2000. COMPEL 2000*, 2000, pp. 10-18.

[12] X. Kang, E. Santi, J. L. Hudgins, P. R. Palmer, and J. F. Donlon, "Parameter extraction for a physics-based circuit simulator IGBT model," in *Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2003. APEC '03*, 2003, vol. 2, pp. 946- 952 vol.2.

[13] R. Withanage, N. Shammas, S. Tennakoorr, C. Oates, and W. Crookes, “Igbt Parameter Extraction for the Hefner IGBT Model,” in *Universities Power Engineering Conference, 2006. UPEC ’06. Proceedings of the 41st International*, 2006, vol. 2, pp. 613-617.

[14] Qingchun Zhang, M. Das, J. Sumakeris, R. Callanan, and A. Agarwal, “12-kV p-Channel IGBTs With Low On-Resistance in 4H-SiC,” *IEEE Electron Device Letters*, vol. 29, no. 9, pp. 1027-1029, Sep. 2008.

[15] A. R. Hefner and D. M. Diebolt, “An experimentally verified IGBT model implemented in the Sabercircuit simulator,” *IEEE Transactions on Power Electronics*, vol. 9, no. 5, pp. 532-542, Sep. 1994.

[16] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and Sei-Hyung Ryu, “Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence,” *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 353-363, Mar. 2007.

[17] Weifeng Li, O. Abbasi, N. S. Hingora, Yongfeng Feng, and H. A. Mantooth, “Certify— A characterization and validation tool for behavioral models,” in *Behavioral Modeling and Simulation Workshop, 2007. BMAS 2007. IEEE International*, 2007, pp. 40-45.

[18] T. R. McNutt, A. R. Hefner, H. A. Mantooth, D. Berning, and Sei-Hyung Ryu, “Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence,” *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 353-363, Mar. 2007.

[19] J. A. Cooper, M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour, “Status and prospects for SiC power MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 49, no. 4, pp. 658-664, Apr. 2002.

[20] J. Millan, “Wide band-gap power semiconductor devices,” *IET Circuits, Devices & Systems*, vol. 1, no. 5, pp. 372-379, Oct. 2007.

[21] A. R. Hefner and D. M. Diebolt, “An experimentally verified IGBT model implemented in the Sabercircuit simulator,” in *, 22nd Annual IEEE Power Electronics Specialists Conference, 1991. PESC ’91 Record*, 1991, pp. 10-19.

[22] B. G. Streetman, *Solid state electronic devices*. Prentice-Hall, 1980.

[23] H. Matsuura et al., “Dependence of acceptor levels and hole mobility on acceptor density and temperature in Al-doped p-type 4H-SiC epilayers,” *Journal of Applied Physics*, vol. 96, no. 5, pp. 2708-2715, Sep. 2004.

[24] M. Chinthavali, L. M. Tolbert, and B. Ozpineci, “SiC GTO thyristor model for HVDC interface,” in *IEEE Power Engineering Society General Meeting, 2004*, 2004, pp. 680- 685 Vol.1.

[25] B. J. Baliga, *Fundamentals of power semiconductor devices*. Springer, 2008.

[26] E. Platania et al., “A Physics-Based Model for a SiC JFET Accounting for Electric-Field-Dependent Mobility,” *IEEE Transactions on Industry Applications*, vol. 47, no. 1, pp. 199-211, Feb. 2011.

[27] A. K. Agarwal, “An overview of SiC power devices,” in *2010 International Conference on Power, Control and Embedded Systems (ICPCES)*, 2010, pp. 1-4.

[28] J. W. Palmour, J. Q. Zhang, M. K. Das, R. Callanan, A. K. Agarwal, and D. E. Grider, “SiC power devices for Smart Grid systems,” in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 1006-1013.