HIGH PERFORMANCE GNRFET DEVICES FOR HIGH-SPEED LOW-POWER ANALOG AND DIGITAL APPLICATIONS

A Thesis

Submitted to the Faculty

of

Purdue University

by

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In Partial Fulfillment of the

Requirements for the Degree

of

Masters of Science in Electrical and Computer Engineering

May 2019

Purdue University

Indianapolis, Indiana

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I would like to dedicate to my family and friends who supported me throughout this journey

ACKNOWLEDGMENTS

I would like to thank my thesis advisor Dr. Maher E. Rizkalla for his endorsement, support and motivation.

I am also grateful to Dr. Trond Ytterdal of Norwegian University of Science and Technology (NTNU) for his ideas and for patiently analyzing my work.

I want to thank my thesis committee Dr. Brian King and Dr. Mohamed El-Sharkawy for their suggestions.

I also want to thank Professor Maryam Rahmani for providing GNRFET device library and Professor Rob Meagher for his help with IT support for simulations.

I also want to extend my thanks to Ms. Sherrie Tucker for her help to complete all the documentation in time with perfection.

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SYMBOLS

V	Voltage
G	Giga
Hz	Hertz
dbs	DeciBels
$Iref$	Reference Current
F	Frequency
W	Width
L	Length
μ	Micro
c	Centi
p	Pico
A	Ampere
W	Watt
s	Second
n	Nano
m	Milli
f	Femto

ABBREVIATIONS

GNRFET	Graphene Nano Ribbon Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
IBM	International Business Machines
CTO	Cheif Technical Officer
ULSI	Ultra Large Scale Integration
MOS	Metal Oxide Semiconductor
RF	Radio Frequency
DAC	Digital-to-Analog Converter
DSP	Digital Signal Processing
ADC	Analog-to-Digital Converter
IUPUI	Indiana University Purdue University Indianapolis
VLSI	Very Large Scale Integration
PMOS	Positive Metal Oxide Semiconductor
NMOS	Negative Metal Oxide Semiconductor
ALU	Arithmetic Logic Units
GPU	Graphical Processing Unit
LSB	Least Significant Bit
MSB	Most Significant Bit
MUX	Multiplexer
AC	Alternating Current
TIQ	Threshold Inverting Quantization
IoT	Internet of Things

ABSTRACT

Patnala, Mounica. M.S.E.C.E., Purdue University, May 2019. High Performance GNRFET Devices for High-Speed Low-Power Analog and Digital Applications. Major Professor: Maher E. Rizkalla.

Recent ULSI (ultra large scale integration) technology emphasizes small size devices, featuring low power and high switching speed. Moore′s law has been followed successfully in scaling down the silicon device in order to enhance the level of integration with high performances until conventional devices failed to cop up with further scaling due to limitations with ballistic effects, and challenges with accommodating dopant fluctuation, mobility degradation, among other device parameters. Recently, Graphene based devices offered alternative approach, featuring small size and high performances. This includes high carrier mobility, high carrier density, high robustness, and high thermal conductivity. These unique characteristics made the Graphene devices attractive for high speed electronic architectures. In this research, Graphene devices were integrated into applications with analog, digital, and mixed signals based systems.

Graphene devices were briefly explored in electronics applications since its first model developed by the University of Illinois, Champaign in 2013. This study emphasizes the validation of the model in various applications with analog, digital, and mixed signals. At the analog level, the model was used for voltage and power amplifiers; classes A, B, and AB. At the digital level, the device model was validated within the universal gates, adders, multipliers, subtractors, multiplexers, demultiplexers, encoders, and comparators. The study was also extended to include Graphene devices for serializers, the digital systems incorporated into the data structure storage. At the mixed signal level, the device model was validated for the DACs/ADCs. In all

components, the features of the new devices were emphasized as compared with the existing silicon technology. The system functionality and dynamic performances were also elaborated. The study also covered the linearity characteristics of the devices within full input range operation.

GNRFETs with a minimum channel length of 10nm and an input voltage 0.7V were considered in the study. An electronic design platform ADS (Advanced Design Systems) was used in the simulations. The power amplifiers showed noise figure as low as 0.064dbs for class A, and 0.32 dbs for class B, and 0.69 dbs for class AB power amplifiers. The design was stable and as high as 5.12 for class A, 1.02 for class B, and 1.014 for class AB. The stability factor was estimated at 2GHz operation. The harmonics were as low as -100 dbs for class A, -60 dbs for class B, and -50dbs for class AB, all simulated at 1GHz. The device was incorporated into ADC system, and as low as 24.5 μWatt power consumption and 40 nsec rise time were observed. Likewise, the DAC showed low power consumption as of 4.51 μWatt. The serializer showed as minimum power consumption of the order of 0.4mW.

These results showed that these nanoscale devices have potential future for high-speed communication systems, medical devices, computer architecture and dynamic Nano electromechanical (NEMS) which provides ultra-level of integration, incorporating embedded and IoT devices supporting this technology. Results of analog and digital components showed superiority over other silicon transistor technologies in their ultra-low power consumption and high switching speed.

1. INTRODUCTION

For years, the world of transistors has been governed by Moore′s Law, which states that the number of transistors in semiconductor circuit doubles every 18 months and this scaling thumb rule started running into challenges for CMOS transistors. In 2003, the IBM Microelectronics CTO Dr. Bernard S. Meyerson, stated at the International Electronics Forum in Prague: Scaling is already dead, but nobody noticed it had stopped breathing and its lips had turned blue [1]. The advanced ULSI technology is in need of high speed, low power devices with less feature sizes, and recent studies gave a path to a new variety of technologies known as post-silicon technology [2]. This technology came with changes in channel size, shape, and material. This study gives hope for a new era of new MOS type graphene-based transistors. This work emphasizes the GNRFET structure, its device characteristics and its benefits in analog and digital circuitries.

This study considers the preamplifier and the power amplifier of integrated amplifier systems. This covers their operation and input/output characteristics. Preamplifiers are voltage amplifiers that boost the voltage gain, then the signal is fed into the power amplifier to drive the signal with high power efficiency [3]. Types A, B, and AB are the three classes considered in this study.

In modern communications, the very high clock frequency and dynamic range of video signal processing, digital signal synthesis, and wireless communications demand high-speed and high accuracy with high resolution analog- to-digital ADCs. ADCs are commonly used in RF systems including mobile phones, dealing with analog signals from sounds and images. The need of high sampling rate and bandwidth of wireless networking and radar communication necessitate the use of high-speed ADCs. If the speed of the ADC is high, no further frequency translation is necessary for the RF mixers and filters, and this may result in less complex high-performance systems.

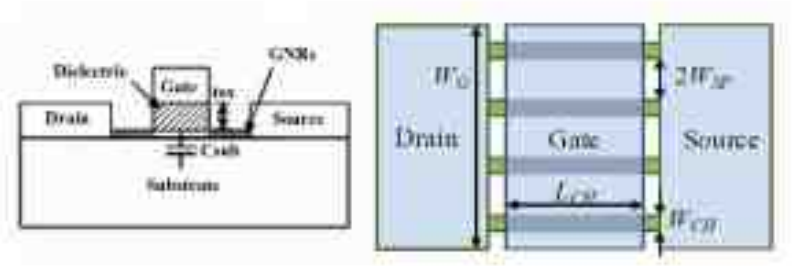


Fig. 1.1. Structure of GNRFET

High speed ADCs are also important in industrial control and medical applications [4].

In this work, we studied and implemented 2-bit, 3-bit and 4-bit DACs. For mixed signal applications, DACs are the most essential blocks. High-speed and low power DACs are necessary for DSP systems, display electronics, and data acquisition systems, among others [5].

1.1 Device Structure

The Graphene Nano Ribbon Field Effect Transistors (GNRFETs) are integrated with an array of graphene nanoribbons. GNRFET uses silicon substrate, with graphene drain and source regions, where drain and source are heavily doped. Graphene is a signal atomic layer of graphite and is of two-dimensional honey comb structure. The high mobility of the material enhances their switching speed and dynamic performance. Graphene is a good conducting material, when patterned into nano-scale ribbons with a band gap opens due to lateral quantum confinement, and this makes it acting as a semiconductor. In a GNRFET, multiple nanoribbons are connected in parallel to increase device strength and to form wide conducting contacts. Figure 1.1 demonstrates the 4 ribbon structure of the GNRFET device [6].

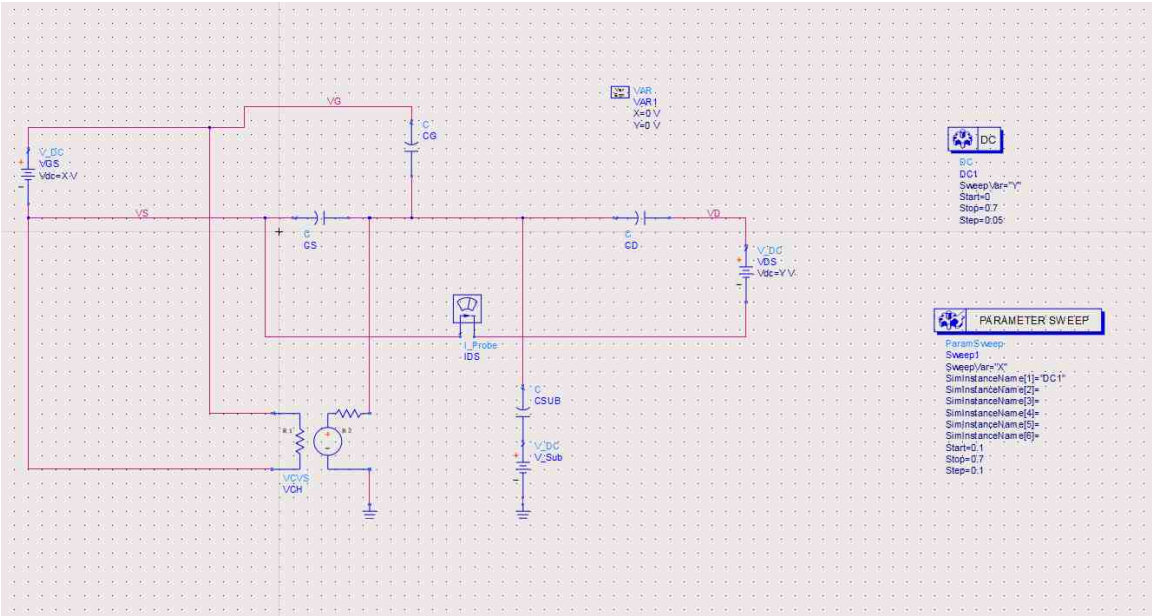


Fig. 1.2. The SPICE GNRFET Model

The device SPICE model as developed by the University of Illinois, Urbana, Champaign is given in Figure 1.2. The device parameters that characterize its performance are:

1. VGS is gate to source voltage.
2. VDS is drain to source voltage.
3. IDS is the current flowing through the channel.
4. Capacitors CG, CD, CS, Csub and VCH are used to vary currents when the channel charges and discharges [6].

Like MOSFETs, GNRFETs are also available as P-type and N-type GNRFETs. The I-V characteristics of the N-type GNRFET and P-type GNRFET devices were simulated at the IUPUI VLSI laboratory and were given in Figures 1.3 and 1.4 respectively. The simulation was based on a VDD value of 0.7V, and a threshold voltage of 0.3V [6].

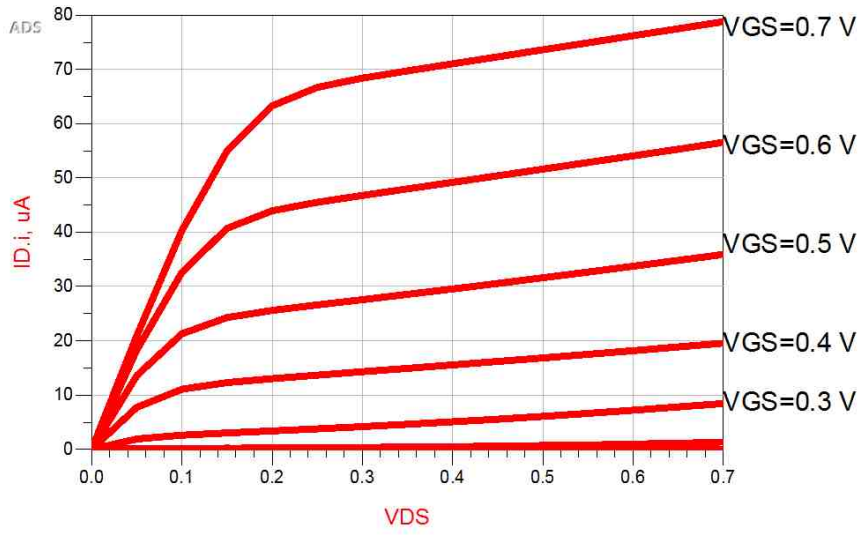


Fig. 1.3. IV Characteristics of N-type GNRFET

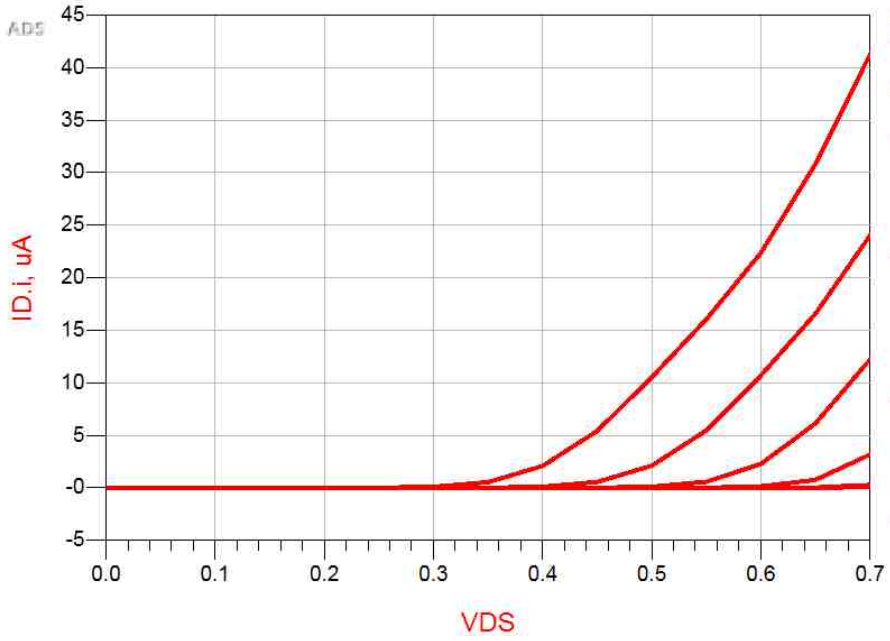


Fig. 1.4. IV Characteristics of P-type GNRFET

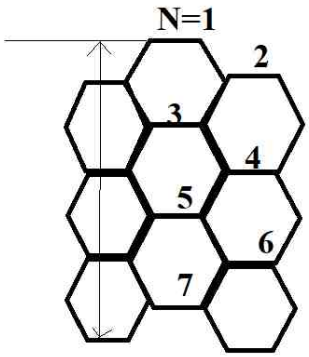


Fig. 1.5. Dimer Lines in Graphene Nano Ribbon with Arm-chair Structure

1.1.1 Computing the Device Width

The channel width of the GNRFET is calculated based on the number of dimer lines in a graphene nano-ribbon [6] is given by the equation:

$$\text{width of GNRFET} = \frac{\sqrt{3}}{2}(\text{N+1})\text{dcc}$$

where N = number of dimer lines

dcc = carbon-carbon bond length = 0.142nm

Figure 1.5 shows the dimer lines in arm chair chirality of GNR.

1.1.2 Computing the Sub-bands

A positive sub-band edge ϵ_α [6] is given by the equation:

$$\epsilon_\alpha = \mid t(1 + 2cos(\tfrac{\pi\alpha}{N+1}) + \delta\epsilon_\alpha) \mid$$

Where N = number of dimer lines

t = 2.7 eV (tight binding hoping parameter)

α = Subband index ($1 \leq \alpha$)

$\delta\epsilon_\alpha$ = edge correction factor = $\frac{4vt}{N+1}cos^2(\frac{\alpha}{N+1})$

Where v =0.12 eV (is the edge correction of hopping parameter at edges in tight binding Hamiltonian).

The most two lowest sub-bands have a first order effect on charge and currents, so our model provides high accuracy and short computation time [6].

1.1.3 Computing the Channel Charge

QCH is derived from carrier density. Electron density nα in sub-band α [6] is given by equation

$$n\alpha = \int_0^\infty f(E) * D(E)dE$$

$$\text{Where f(E) = Fermi Dirac distribution function} = \frac{1}{(1+e^{\frac{(E-E(F))}{KT}})}$$

$$\text{D(E) = density of states} = (\frac{2\sqrt{M}}{\pi h})\frac{(\epsilon\alpha+E)}{\sqrt{(E\epsilon\alpha(E+2\epsilon\alpha))}}$$

Where h= Planck's constant

M= effective mass

K= Boltzmann's constant

1.1.4 The Breakdown Voltage

Typical GNRFET breakdown voltage is in the range of 0.5 to 3 V for different channel lengths. The short channel and high mean free path of graphene is up to 400nm, result in high ionization rate and breakdown at high biases. For example, GNRFET with 22nm width formed by mechanical exfoliated has a breakdown voltage of 2.5V. GNRFET with 10-20nm width formed by chemical vapor deposition has breakdown current density 4×10^{-7} A/cm^2 [6].

1.2 Device Parameters

1.2.1 Electron Mobility

Electron mobility is defined as the ease with which an electron can move through a semiconductor due to an electric field. It is denoted by μ and has units $cm^2/(V.s)$ [7]. For better performance, electron mobility should be high. In case of graphene, it is $1500cm^2/(V.s)$ [8].

1.2.2 Leakage Current

Leakage current is the measure of leaked current between source and drain when the transistor is turned off. The leakage current increases with decrease in channel length. Although the channel lengths of the device technologies discussed here are low, leakage current remains low due to the nano scale materials used and the changes in gate structure [9]. The leakage current of GNRFET device is 1771 pA [8].

1.2.3 Leakage Power

The unwanted subthreshold current present in the transistor when it is off times VDS. Leakage power is strongly influenced by transistors threshold voltage [10] and the GNRFET has near 1240 pW [8].

1.2.4 Ion / Ioff

The ratio of maximum drain current to off leakage current defines the switching performance of a device [11]. The on-off ratio of GNRFET is as high as 40,000. [8]

1.2.5 Delay

The time gap between the application of input signal and the visible affect at the output of GNRFET is near 2.79 ps [8]. The unique device parameters make it good candidate in future high speed low power systems.

1.3 Organization of Thesis

Chapter 2 covers digital components incorporated with GNRFET device and their truth tables, boolean expressions and transient analysis responses. Chapter 3 covers GNRFET based power amplifiers and differential amplifiers with their power gain, noise figure and stability factors. Chapter 4 emphasizes Analog-to-Digital converters

and Digital-to-Analog converters and their power consumption analysis. Chapter 5 gives the results and discussions of the work presented in this thesis, and Chapter 6 concludes the work and suggests some future work to follow.

2. THE GNRFET DIGITAL DEVICES AND CIRCUITS

This chapter emphasis the feasibility of Graphene Nano-ribbon field effect transistors in implementation of combinational logic circuits such as logic gates, adders, multipliers, muliplexers, Demultiplexers, Encoders, decoders, comparators and flipflops. Transient analysis was performed using ADS platform. The simulation of GNRFET device used is with channel length of 10nm and supply voltage 0.7V.

2.1 Logic Gates

The basic logic gates are NAND, NOR, NOT, AND, OR, XOR and XNOR gates. NAND and NOR gates are known as Universal gates since other logic gates can be derived from these gates, and the remaining gates are known to be derived gates. These logic gates are building blocks of other combinational logic gates.

2.1.1 The NOT Gate

Not gate is made of gnrfetpmos pull-up and gnrfetnmos pull-down devices. For a high input voltage of 0.7V the gnrfetpmos is switched off and gnrfetnmos is switched on to give an output voltage 0V. Similarly, for a low input voltage of 0V the gnrfetnmos is switched off and gnrfetpmos is switched on to give an output voltage 0.7V. The schematic of a NOT gate is given in Figure 2.1. The transient analysis response is given in Figure 2.2.

2.1.2 The NAND Gate

The 2-bit NAND gate is designed using two gnrfetpmos in parallel acting as pull-up tree, connected with two gnrfetnmos in series acting as pull-down tree. The schematic

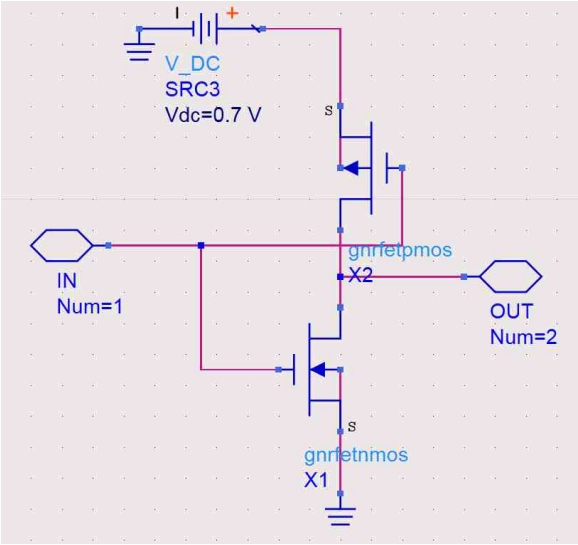


Fig. 2.1. NOT Gate Schematic

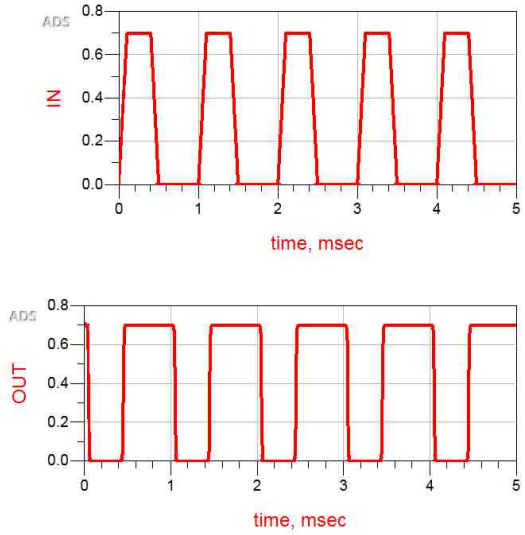


Fig. 2.2. NOT Gate Output

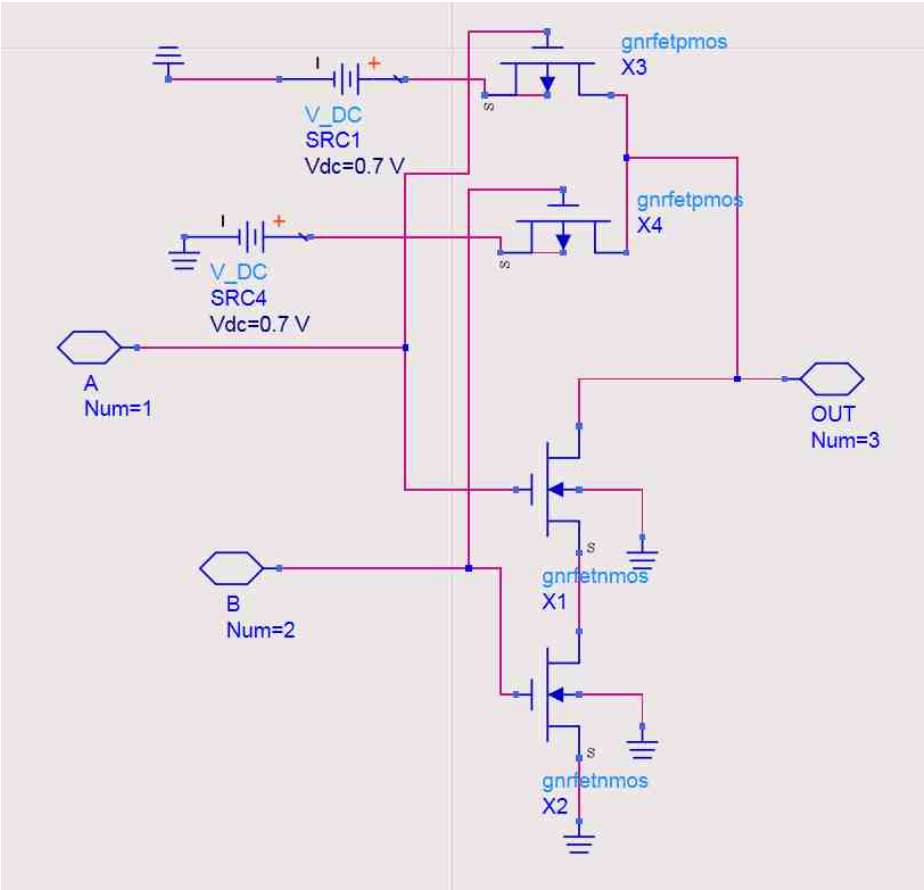


Fig. 2.3. NAND Gate Schematic

of the 2-input NAND gate is given in Figure 2.3, and the transient analysis response is shown in Figure 2.4.

2.1.3 The NOR Gate

The 2-bit NOR gate is designed using two gnrfetpmos in series acting as pull-up tree, connected with two gnrfetnmos in parallel acting as pull-down tree. The schematic of the 2-input NOR gate is given in Figure 2.5, and its transient analysis response is shown in Figure 2.6.

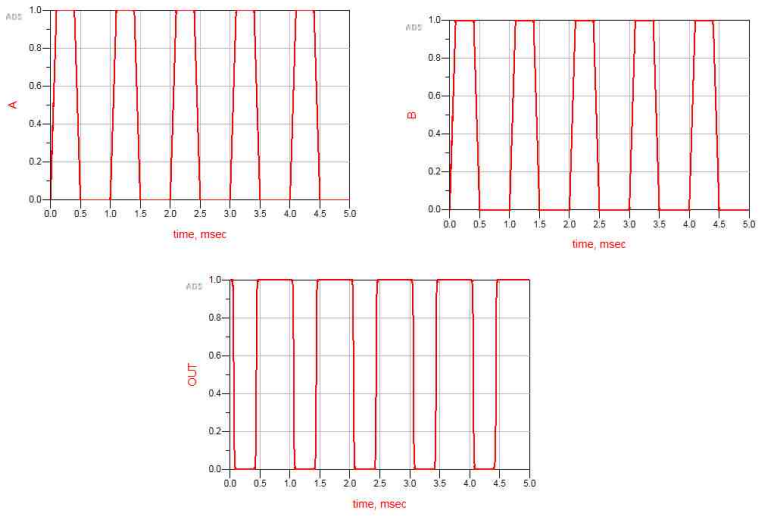


Fig. 2.4. NAND Gate Output

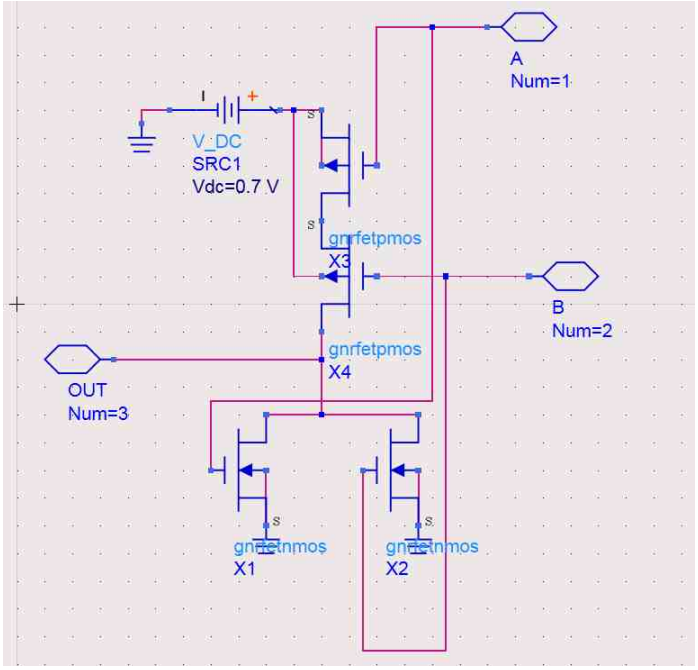


Fig. 2.5. NOR Gate Schematic

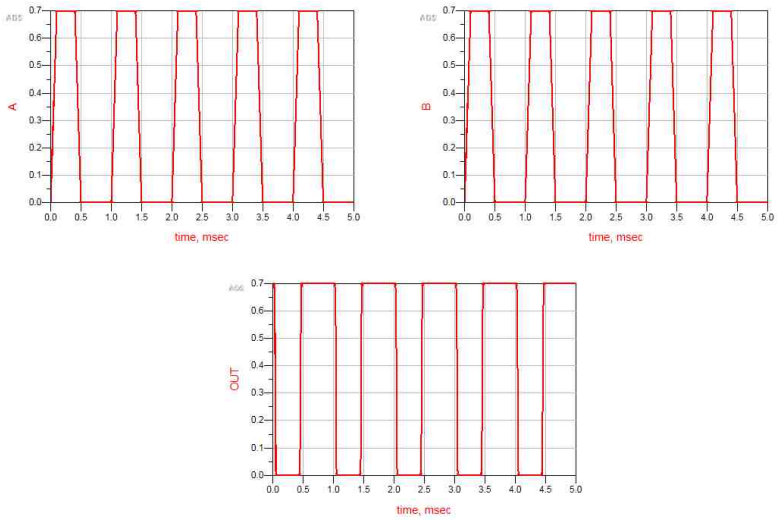


Fig. 2.6. NOR Gate Output

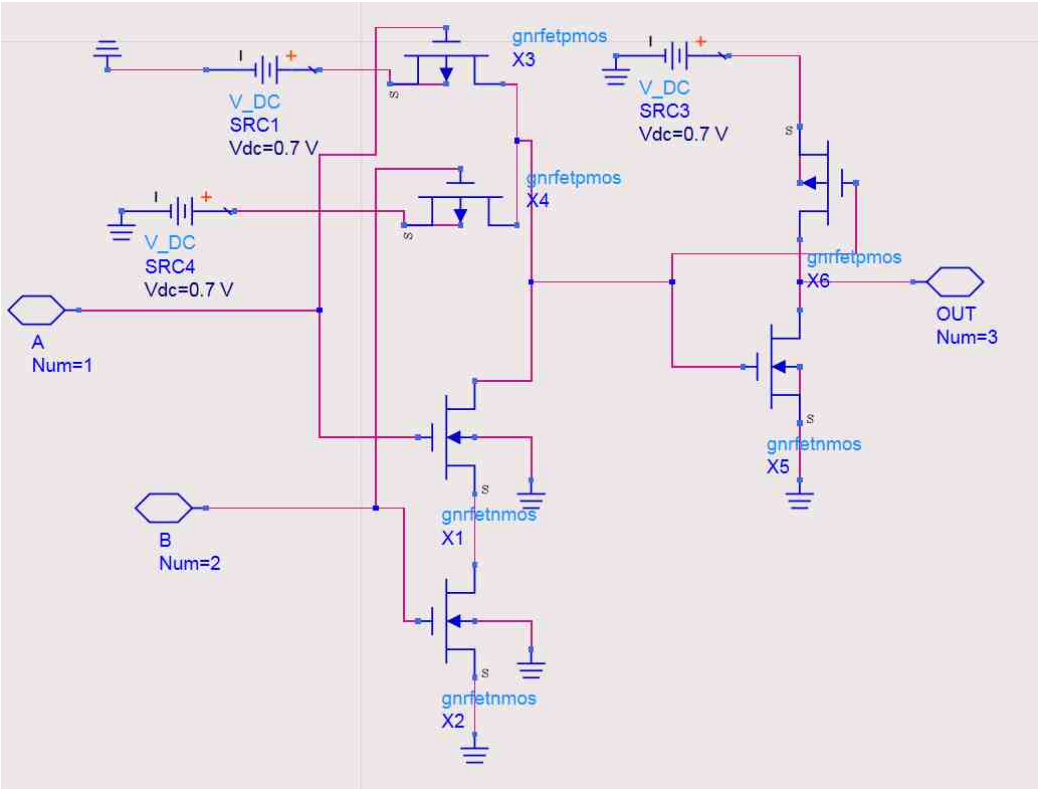


Fig. 2.7. AND Gate Schematic

2.1.4 The AND Gate

The AND gate was designed by pull-up gnrfetpmos and pull-down gnrfetnmos. The schematic of the 2-input AND gate is given in Figure 2.7, and its transient analysis response is shown in Figure 2.8.

2.1.5 The OR Gate

Likewise, the OR gate was designed with pull-up gnrfetpmos and pull-down gnrfetnmos. The schematic of the 2-input OR gate is given in Figure 2.9 and its transient analysis response is shown in Figure 2.10.

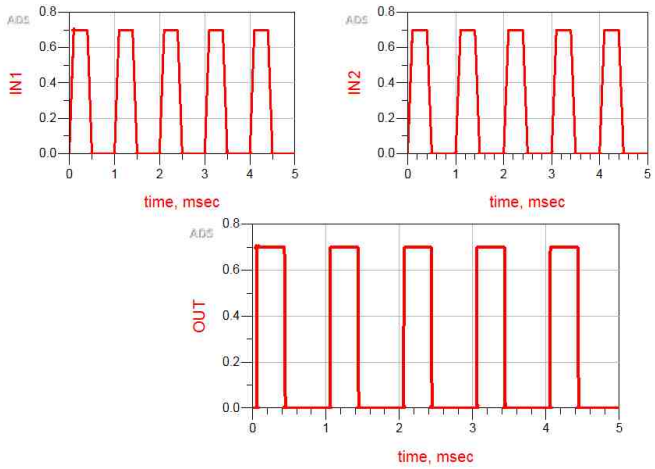


Fig. 2.8. AND Gate Output

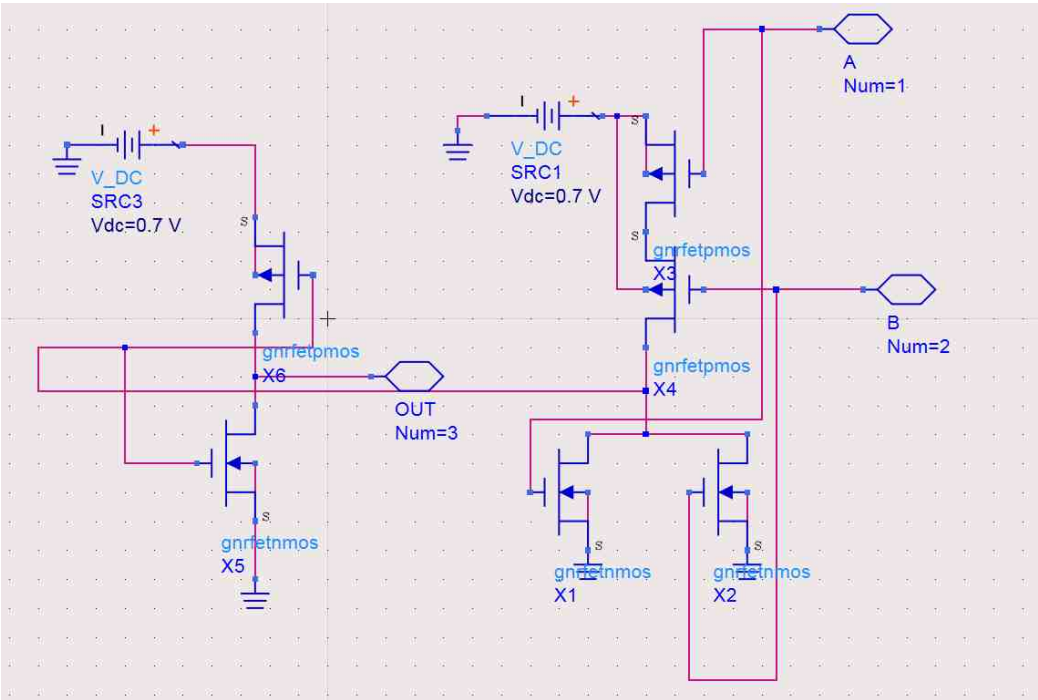


Fig. 2.9. OR Gate Schematic

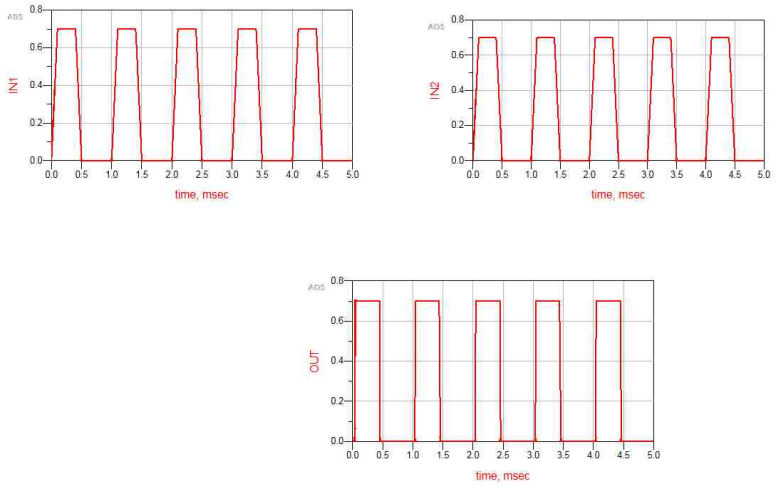


Fig. 2.10. OR Gate Output

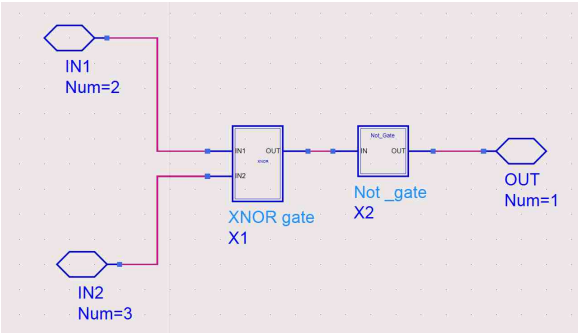


Fig. 2.11. XOR Gate Schematic

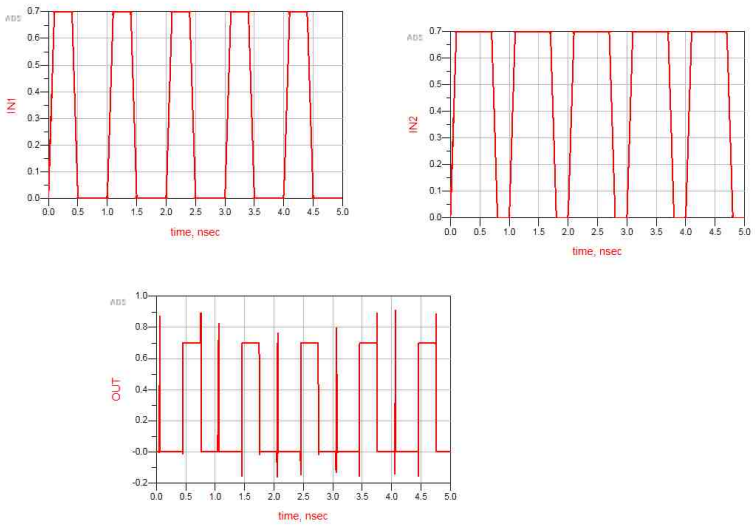


Fig. 2.12. XOR Gate Output

2.1.6 XOR Gate

The boolean expression of the XOR gate is given by

$$\text{A XOR B} = \text{A}\overline{B} + \overline{A}\text{B}$$

The schematic of the 2-input XOR gate is given in Figure 2.11, and the transient analysis response is shown in Figure 2.12.

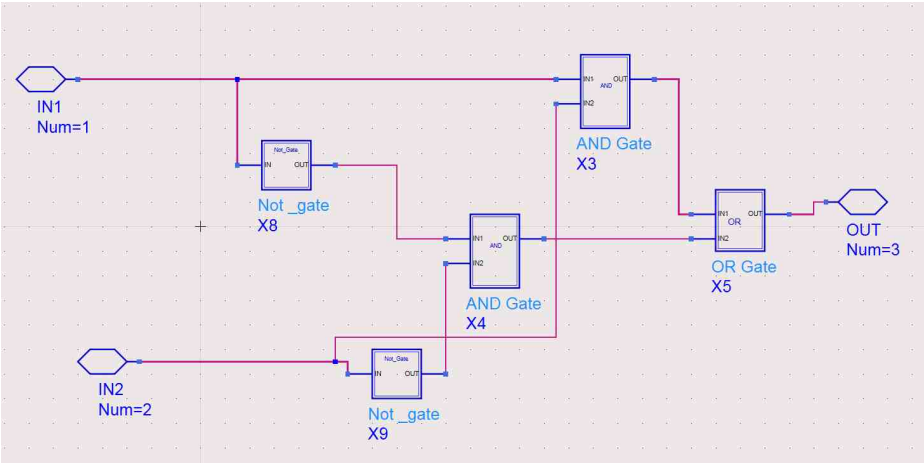


Fig. 2.13. XNOR Gate Schematic

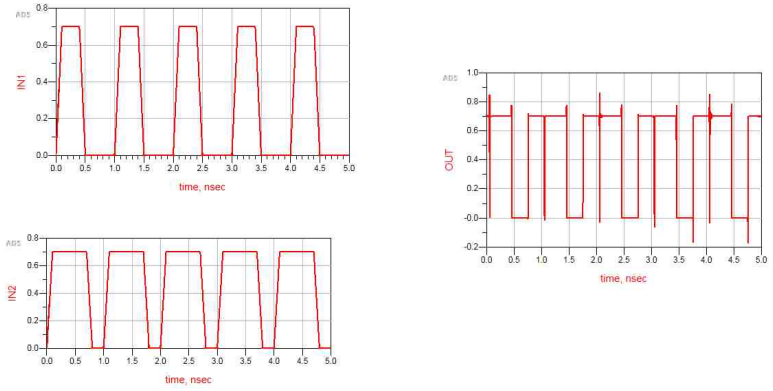


Fig. 2.14. XNOR Gate Output

2.1.7 XNOR Gate

The boolean expression of the XNOR gate is given by

$$\text{A XNOR B} = \text{AB}+\overline{AB}$$

The schematic of the 2-input XNOR gate is given in Figure 2.13, and the transient analysis response is shown in Figure 2.14.

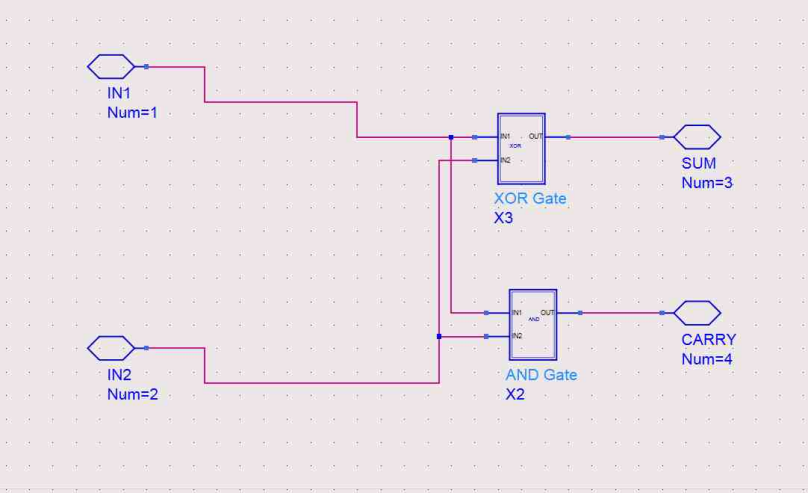


Fig. 2.15. Half Adder Schematic

2.2 Adders

Adders are the most important devices used in digital systems where processing of binary numbers are required. They are mostly used in Arithmetic Logic Units (ALUs), Program Counters, timers, Digital Signal Processing, and Graphical Processing Units (GPUs) oriented systems for reducing complexity [12]. Low power half adder, full adder, parallel adder, and ripple carry adder are designed and simulated using ADS.

2.2.1 Half Adder

The half adder adds two binary bits and gives sum and carry. The boolean expressions for sum and carry are given below for inputs A and B

$$sum = A\ XOR\ B = A\overline{B}\ + \overline{A}B$$

$$carry = A\ AND\ B = AB$$

The schematic of the half adder and the transient response are given in Figures 2.15 and 2.16 respectively.

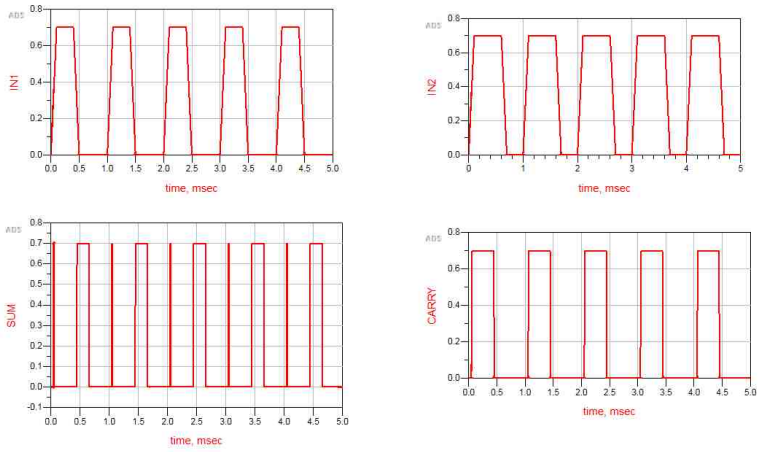


Fig. 2.16. Half Adder Output

2.2.2 Full Adder

The boolean expressions for sum and carry are given below for inputs A,B and C.

$$sum = A\ XOR\ B\ XOR\ C$$

$$carry = (A\ AND\ B)\ OR\ (B\ AND\ C)\ OR\ (A\ AND\ C) = AB + BC + CA$$

The schematic of full adder and the transient response are given in Figures 2.17 and 2.18 respectively.

Two 4-bit parallel adders implemented in this study are ripple carry adder and carry look ahead adder.

2.2.3 Ripple carry adder

Considering two 4-bit inputs A ($A_4A_3A_2A_1$) and B ($B_4B_3B_2B_1$) with LSBs A_1 and B_1, are added using a half adder with sum_1 as the final sum and the carry (C_1) called an internal carry, and is added to the next significant bit. Then a full adder is used to add the three bits $A_2 + B_2 + C_1$ which generates sum_2 and an internal carry C_2. Similarly for the remaining bits such as $(A_3 + B_3 + C_2)$ and MSB $(A_4 + B_4 + C_3)$. The schematic of 4-bit ripple carry adder and its transient analysis are shown in Figures 2.19, and 2.20 respectively. The mathematical expressions of 4-bit ripple carry adder for inputs A, B and output sum are given as:

$$sum_1 = A_1 + B_1$$

$$sum_2 = A_2 + B_2 + C_1$$

$$sum_3 = A_3 + B_3 + C_2$$

$$sum_4 = A_4 + B_4 + C_3$$

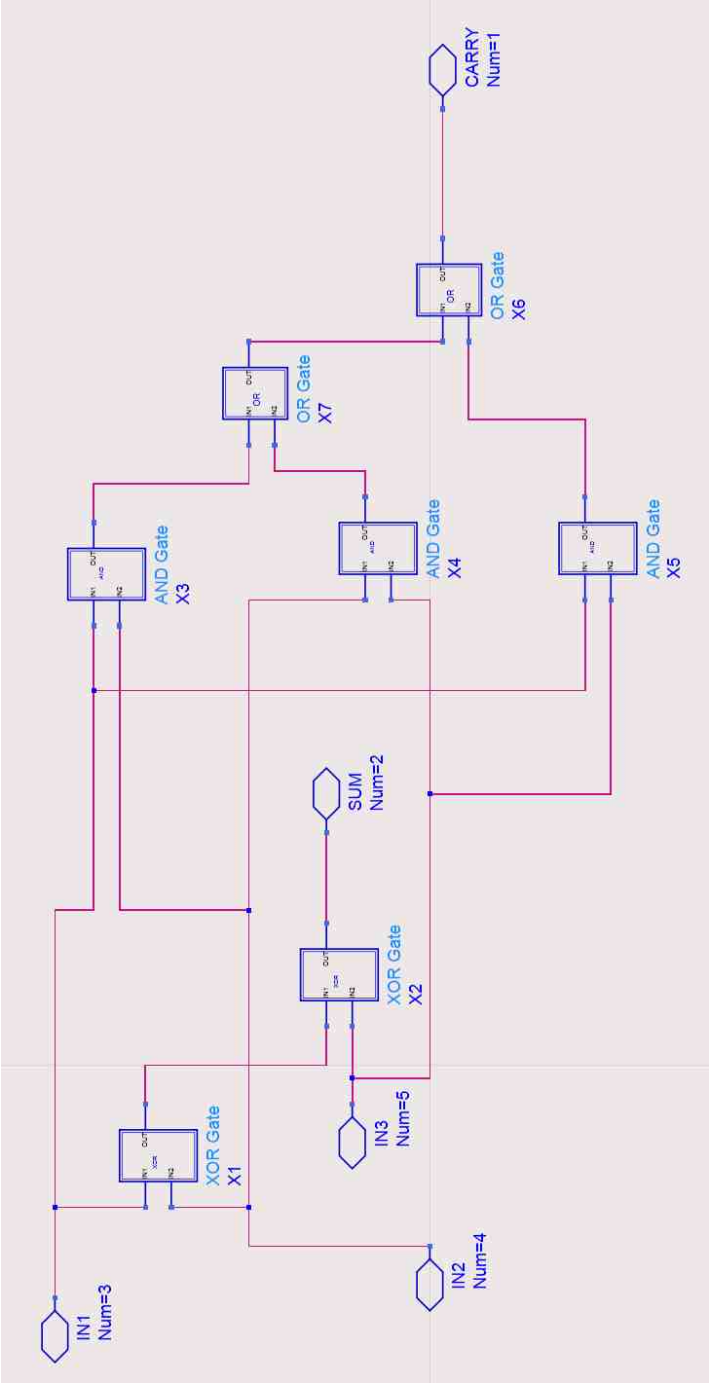


Fig. 2.17. Full Adder Schematic

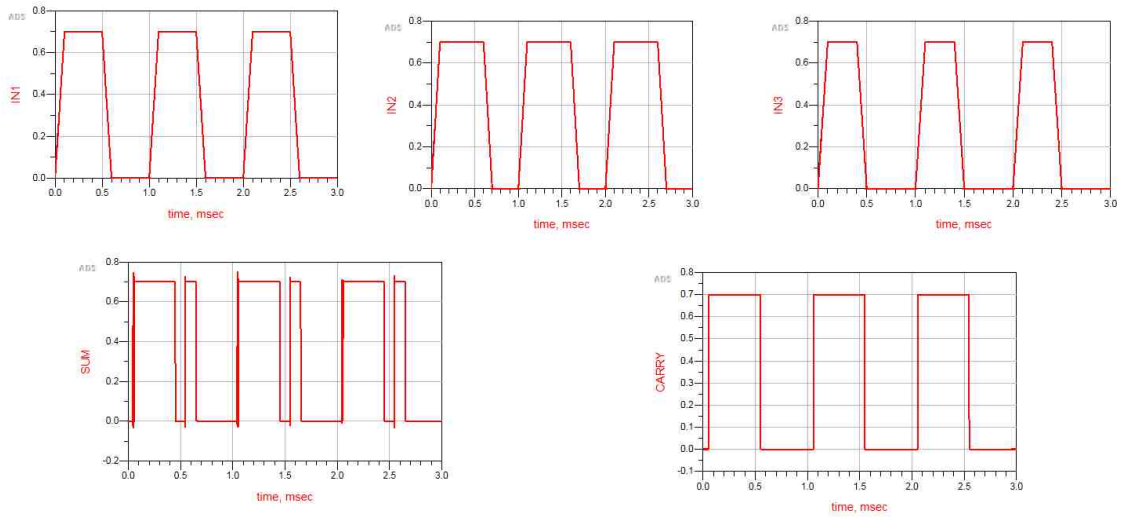


Fig. 2.18. Full Adder Output

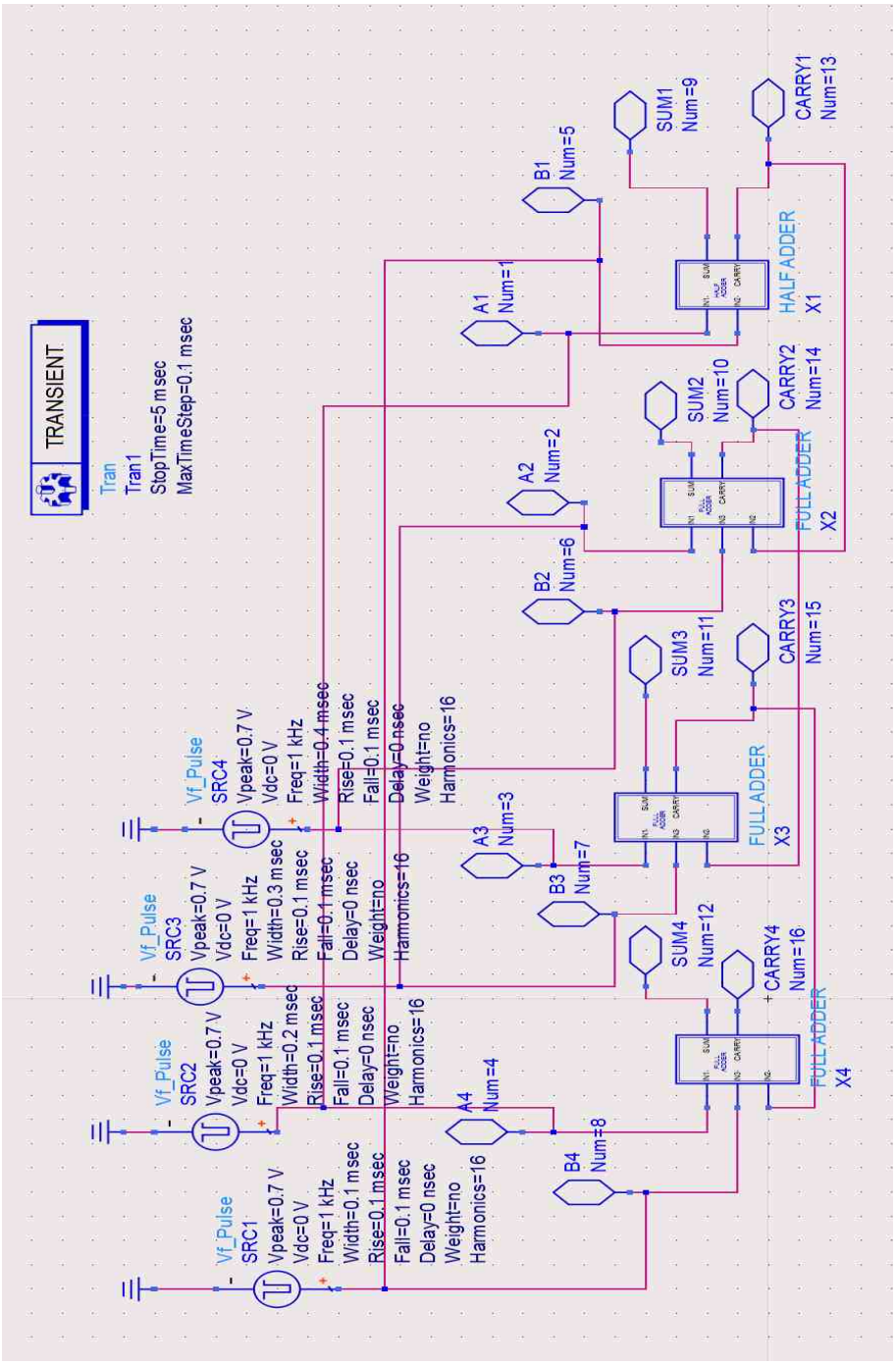


Fig. 2.19. Ripple Carry Adder Schematic

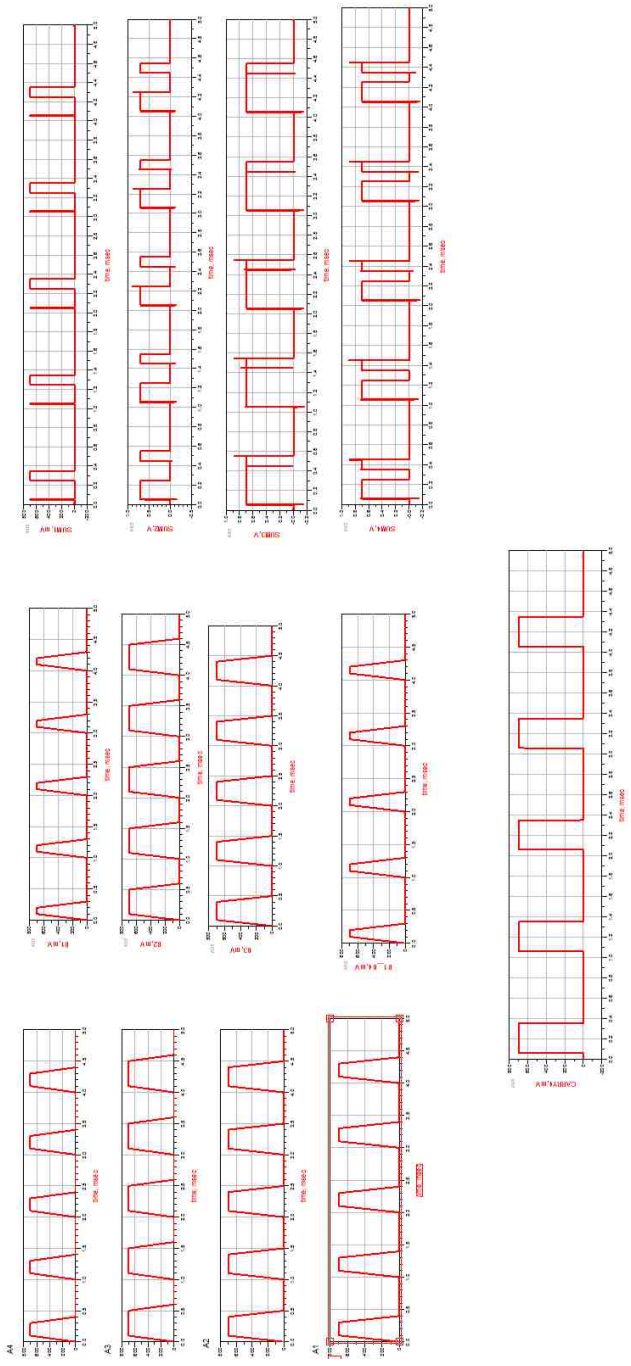


Fig. 2.20. Ripple Carry Adder Output

2.2.4 Carry Look Ahead Adder

The carry look ahead adder is mainly used when both inputs are high or when one of the bits in two input binary numbers is 1 with a carry from the previous bit 1. The implementation of carry look ahead adder is done by generating all P_i and G_i, where P_i is carry propagate signal and G_i is carry generate signal. Boolean expressions of G, P, and the Sum and Carry outputs are given as:

$$P_i = A_i \ XOR \ B_i$$

$$G_i = A_i \ AND \ B_i$$

$$Sum_i = P_i \ XOR \ Carry_i$$

$$Carry_(i+1) = G_i \ OR \ (P_i \ AND \ Carry_i)$$

The schematics and transient analysis response of the carry look ahead adder are shown in Figures 2.21 and 2.22 respectively.

2.3 Binary Subtractors

Binary subtractors are used to substract two binary numbers. It is mainly used for decision making. Binary subtractors produce the difference and borrow. For subtracting, the subtractor uses the basic rule of subtraction i.e., if a lower number is subtracted from a higher number it will produce a difference without a borrow, and if a higher number is subtracted from a lower number, it will produce the difference with a borrow. In this study, a binary half subtractor and a full subtractor are designed and implemented.

2.3.1 Half Subtractor

In half subtractor two binary bits are subtracted for producing the difference and borrow. The truth table of the half subtractor is:

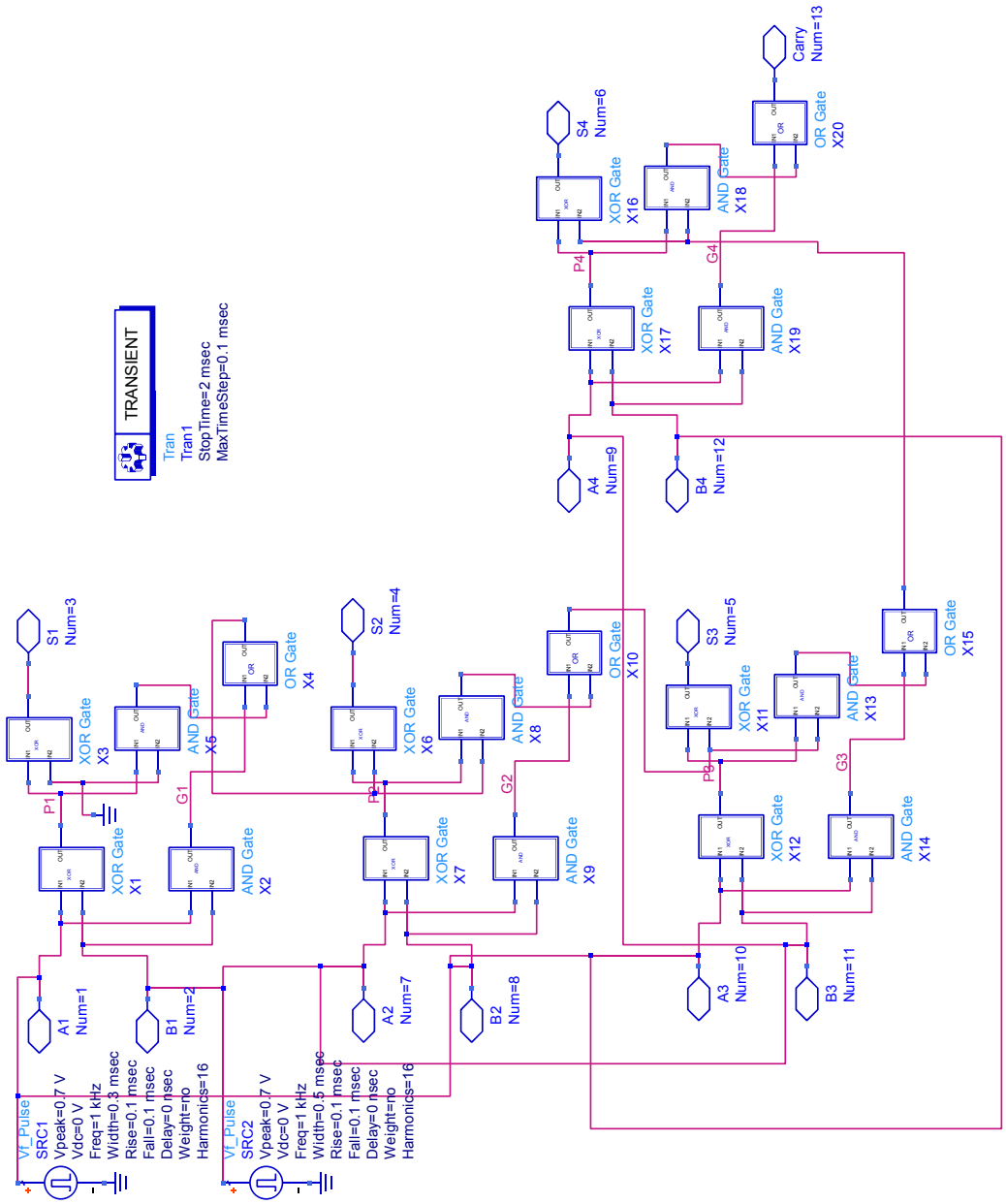


Fig. 2.21. Carry Look Ahead Adder Schematic

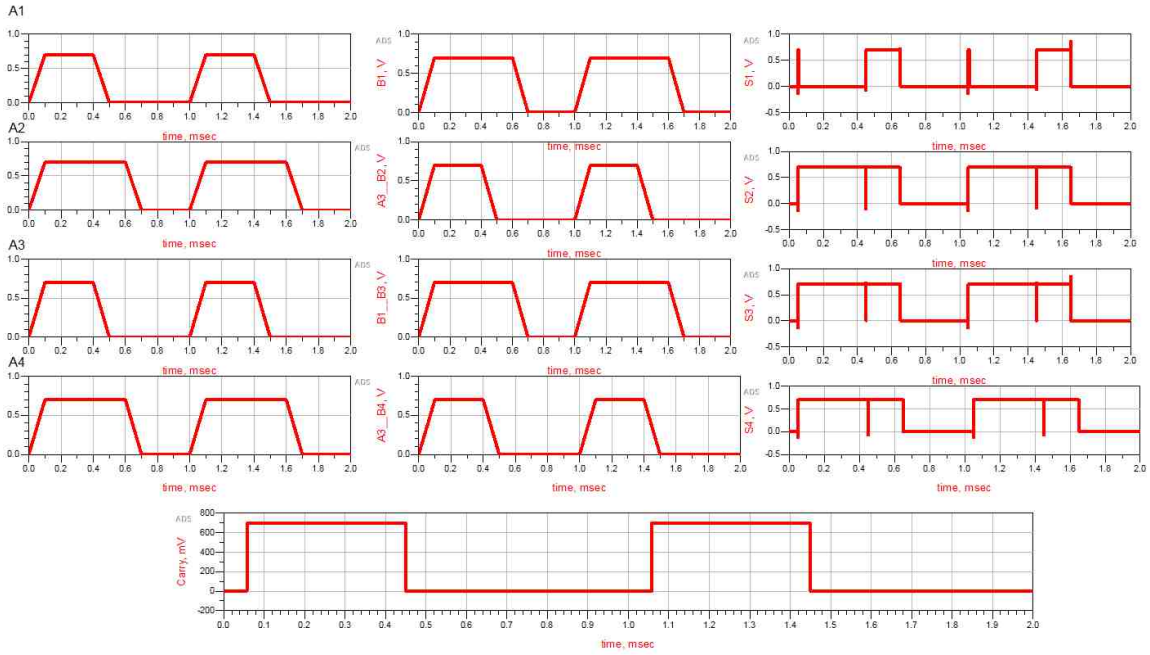


Fig. 2.22. Carry Look Ahead Adder Output

A	B	Difference	Borrow
0	0	0	0
0	1	1	0
1	0	1	1
1	1	0	0

The boolean expressions derived from the truth table for the difference and borrow in terms of the inputs A and B are:

$$Difference = A\ XOR\ B = A\overline{B}\ +\overline{A}B$$

$$Borrow = \overline{A}\ AND\ B$$

The schematics of the full subtractor and the transient response are given in Figures 2.23 and 2.24 respectively.

2.3.2 Full Subtractor

In full subtractor three binary bits named A, B and C are used to get the difference and borrow outputs. The truth table of the full subtractor showing all the different combinations of inputs is:

A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1

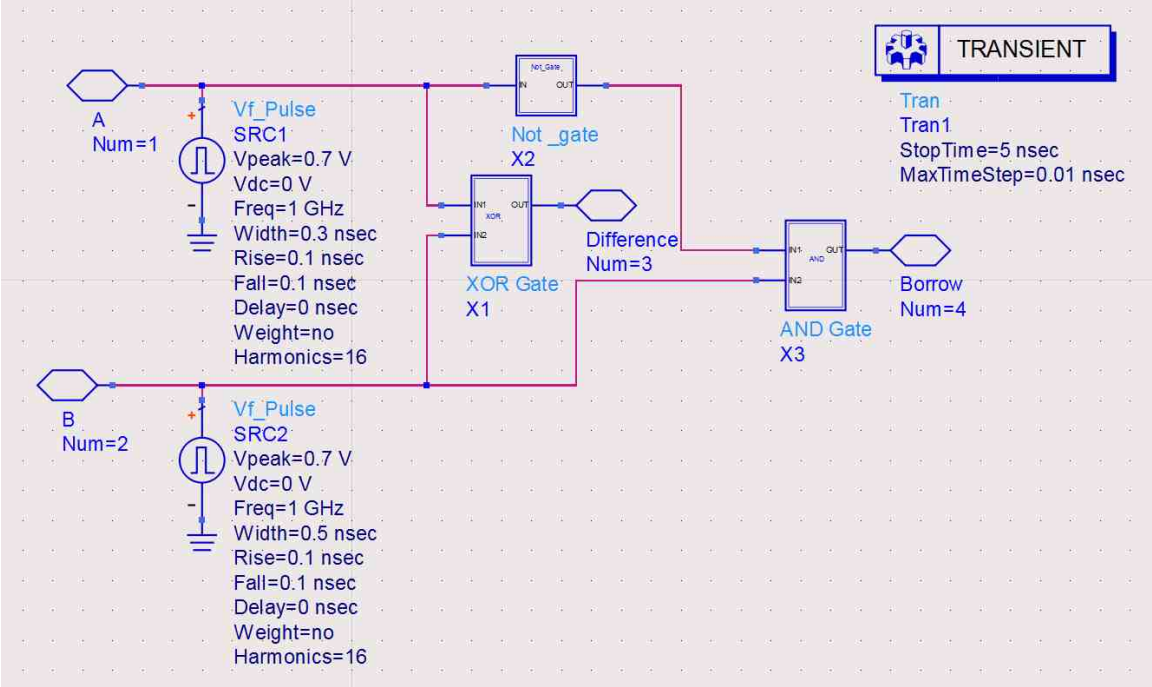


Fig. 2.23. Half Subtractor Schematic

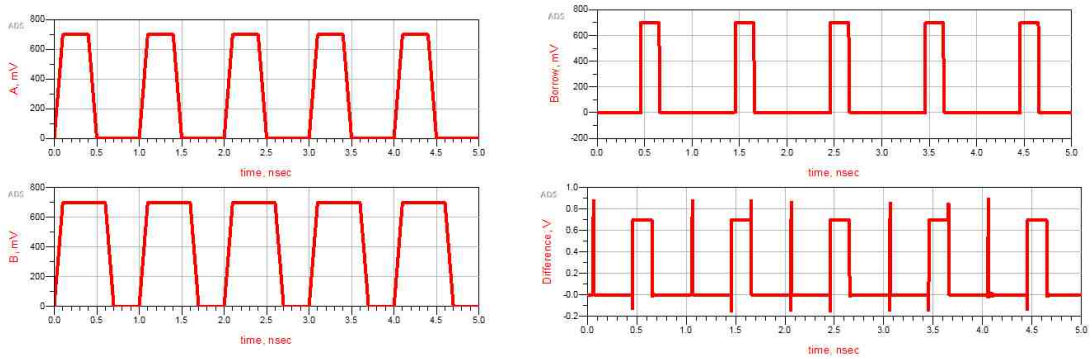


Fig. 2.24. Half Subtractor Output

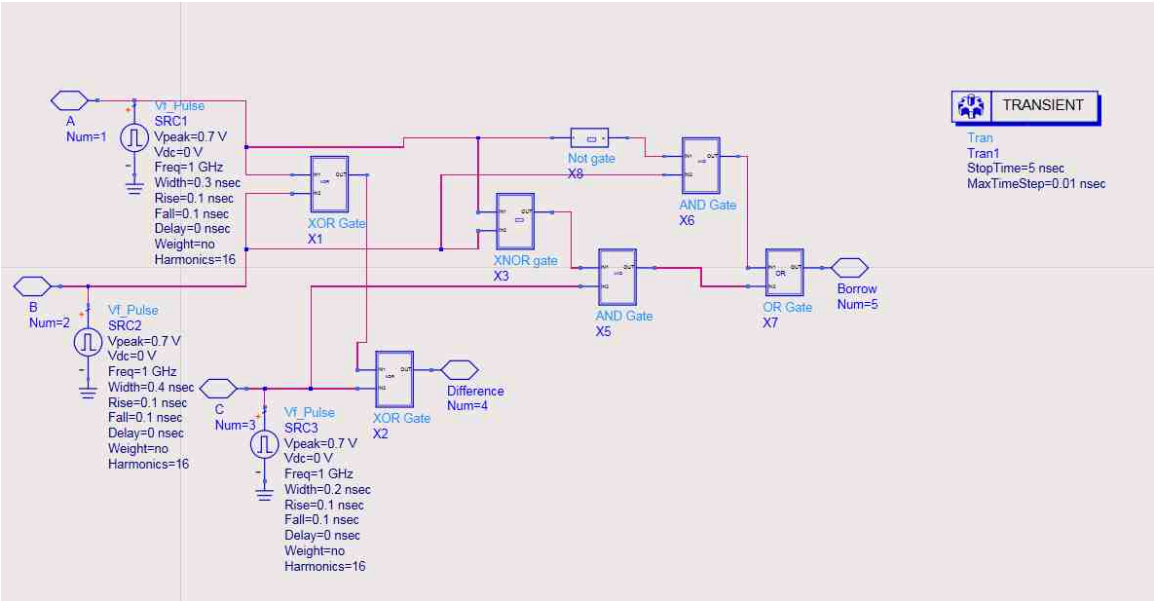


Fig. 2.25. Full Subtractor Schematic

The boolean expressions derived from the truth table for the difference and borrow in terms of the inputs A, B and C are:

$$Difference = A\ XOR\ B\ XOR\ C$$

$$Borrow = ((A\ XNOR\ B)\ AND\ C)\ OR\ (\overline{A}\ AND\ B)$$

The schematics of the full subtractor and the transient response are given in Figures 2.25 and 2.26 respectively.

2.4 Binary Multiplier

Binary multipliers are electronic digital devices used for multiplying two binary numbers. The inputs used are called multiplicand and multiplier. The bit size of the final product is the sum of bit sizes of multiplicand and multiplier. Partial products are obtained using AND gates, and these partial products are added using half adders and full adders. In this study, 2×2 and 3×3 multipliers are implemented.

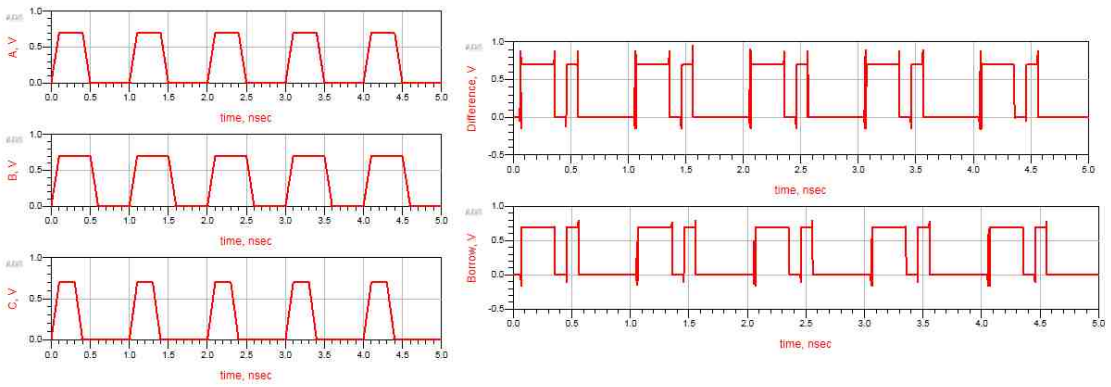


Fig. 2.26. Full Subtractor Output

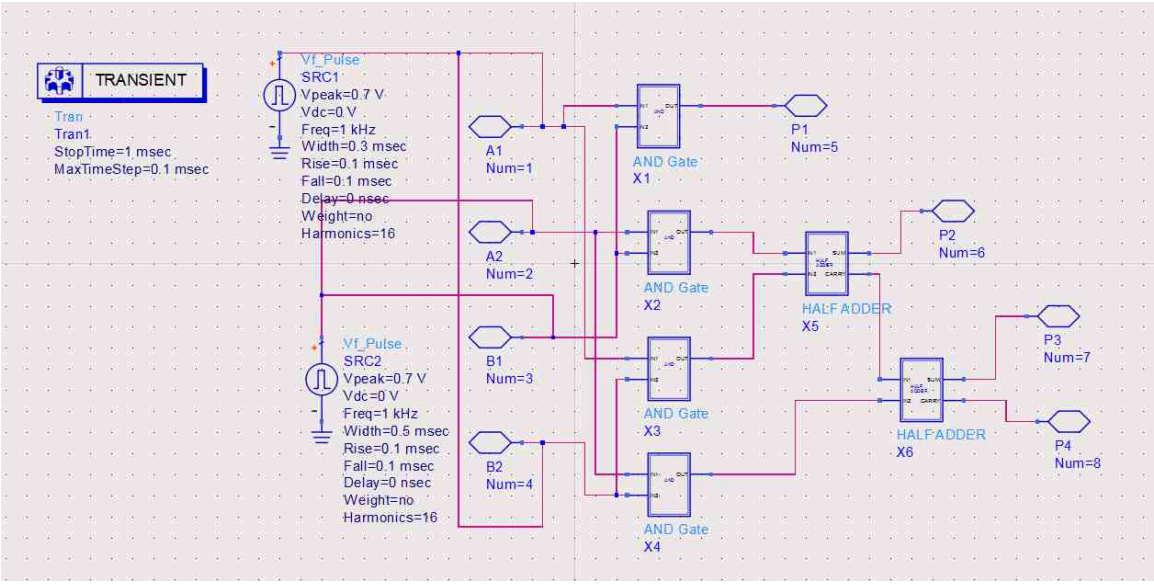


Fig. 2.27. 2×2 Multiplier Schematic

2.4.1 2×2 Binary Multiplier

In 2×2 multiplier, 2-bit binary inputs are used. Multiplicand A_2A_1 is first multiplied by the LSB of the multiplier B_1, obtained from the AND operation. The multiplicand A_2A_1 is then multiplied with the MSB of multiplier, B_1, then the two products are added using full adders and half adders. The schematics and transient analysis are shown in Figures 2.27 and 2.28, respectively.

2.4.2 3×3 Binary Multiplier

In 3×3 multiplier, 3-bit binary inputs are used. Multiplicand $A_3A_2A_1$ is first multiplied by LSB of multiplier B_1, obtained from the AND operation. The multiplicand $A_3A_2A_1$ is multiplied with next significant bit of multiplier B_2. Likewise, the multiplicand $A_3A_2A_1$ is multiplied with next significant bit of multiplier B_3. Finally, add all the products using full adders and half adders. The schematics and transient analysis are shown in Figures 2.29 and 2.30, respectively.

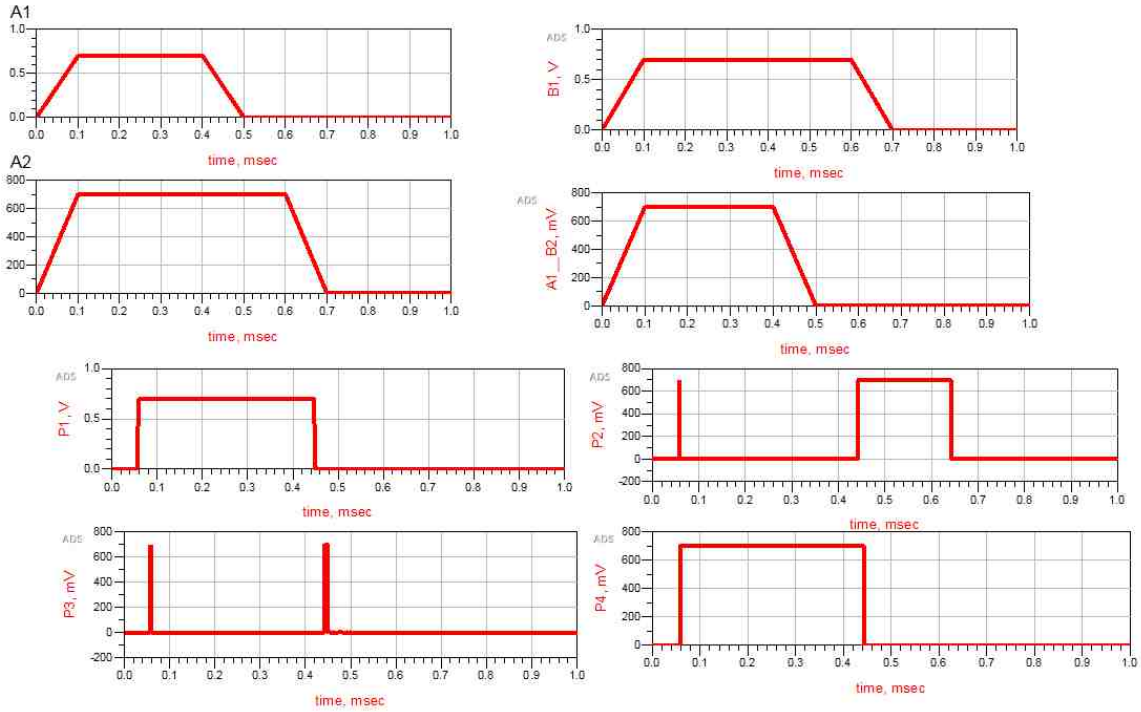


Fig. 2.28. 2×2 Multiplier Output

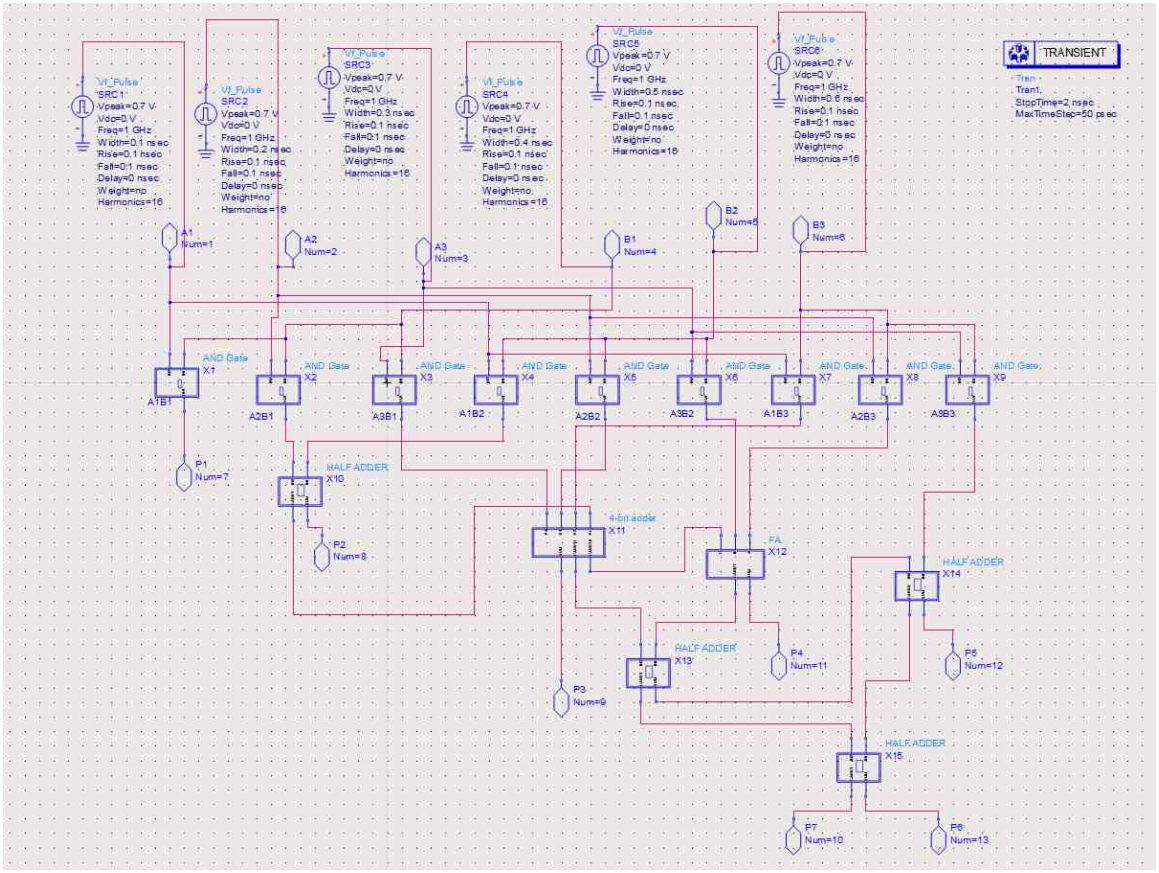


Fig. 2.29. 3×3 Multiplier Schematic

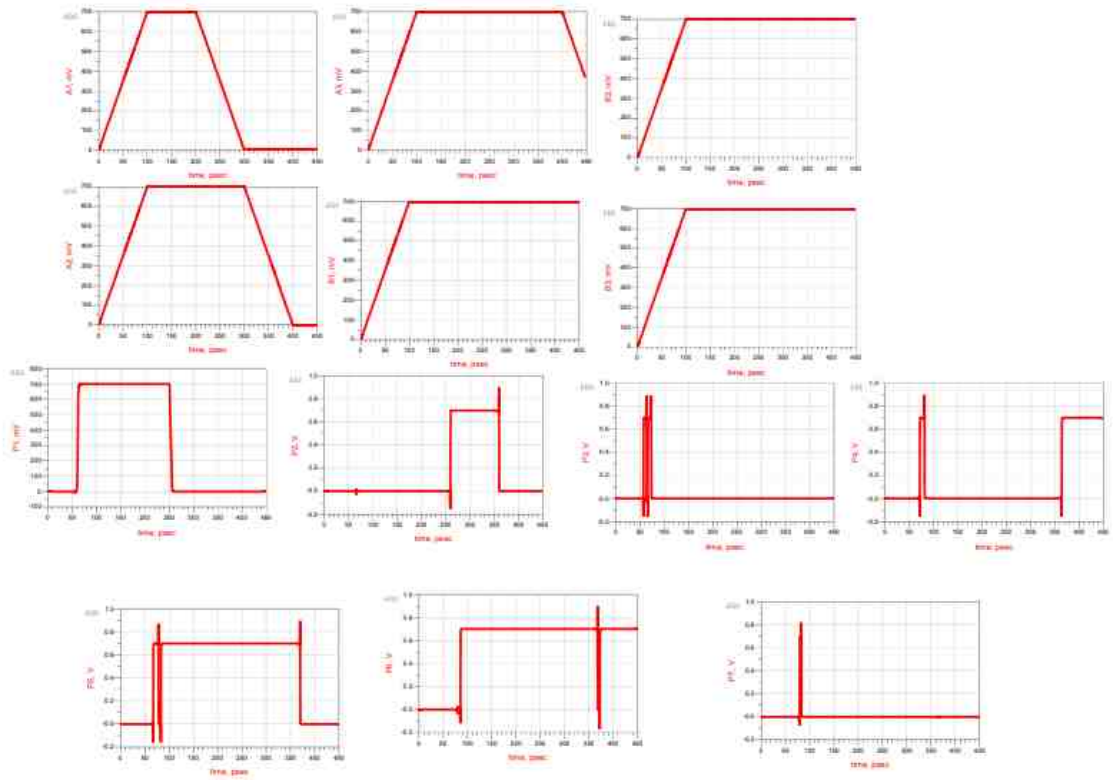


Fig. 2.30. 3×3 Multiplier Output

2.5 Multiplexer

Multiplexers are used to combine data from different sources to one single data. The select lines helps the mux to select a particular input to be switched as an output. In this study, 2:1 MUX and 4:1 MUX, were designed and simulated.

2.5.1 2:1 Multiplexer

The 2:1 MUX is designed with 2 inputs, 1 select line, and an output. The truth table for the MUX inputs A, B, and the select line select is given as,

Select	**Output**
0	A
1	B

The boolean expression of the 2:1 MUX is given as,

$$Output = \overline{Select}\ A\ +\ Select\ B$$

The schematics of the 2:1 MUX and transient response are shown in Figures 2.31 and 2.32, respectively.

2.5.2 4:1 Multiplexer

A 4:1 MUX is designed with 4 inputs, 2 select lines and an output. The truth table for MUX inputs A, B, C, D and select lines select1 and select2 are:

Select2	**Select1**	**Output**
0	0	A
0	1	B
1	0	C
1	1	D

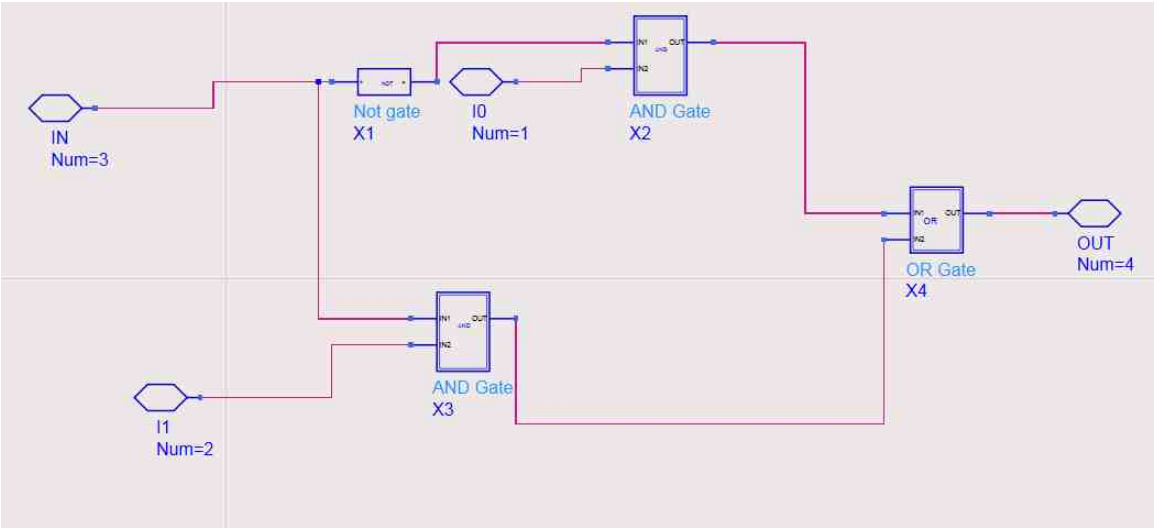


Fig. 2.31. 2:1 MUX Schematic

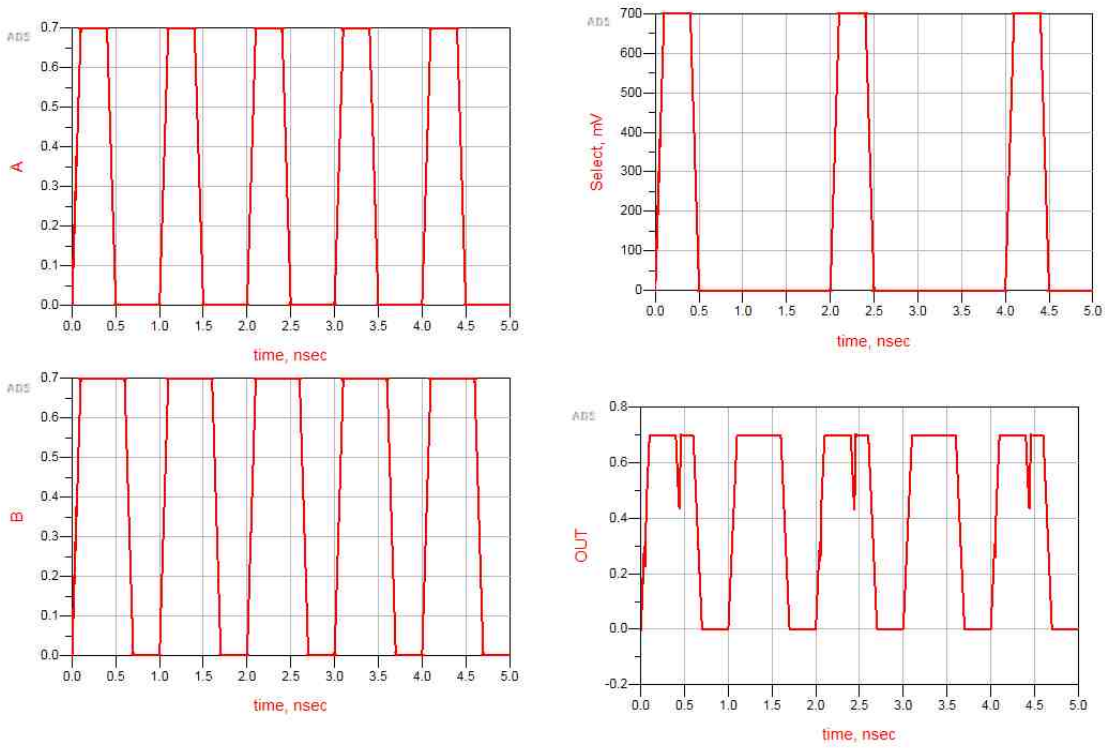


Fig. 2.32. 2:1 MUX Output

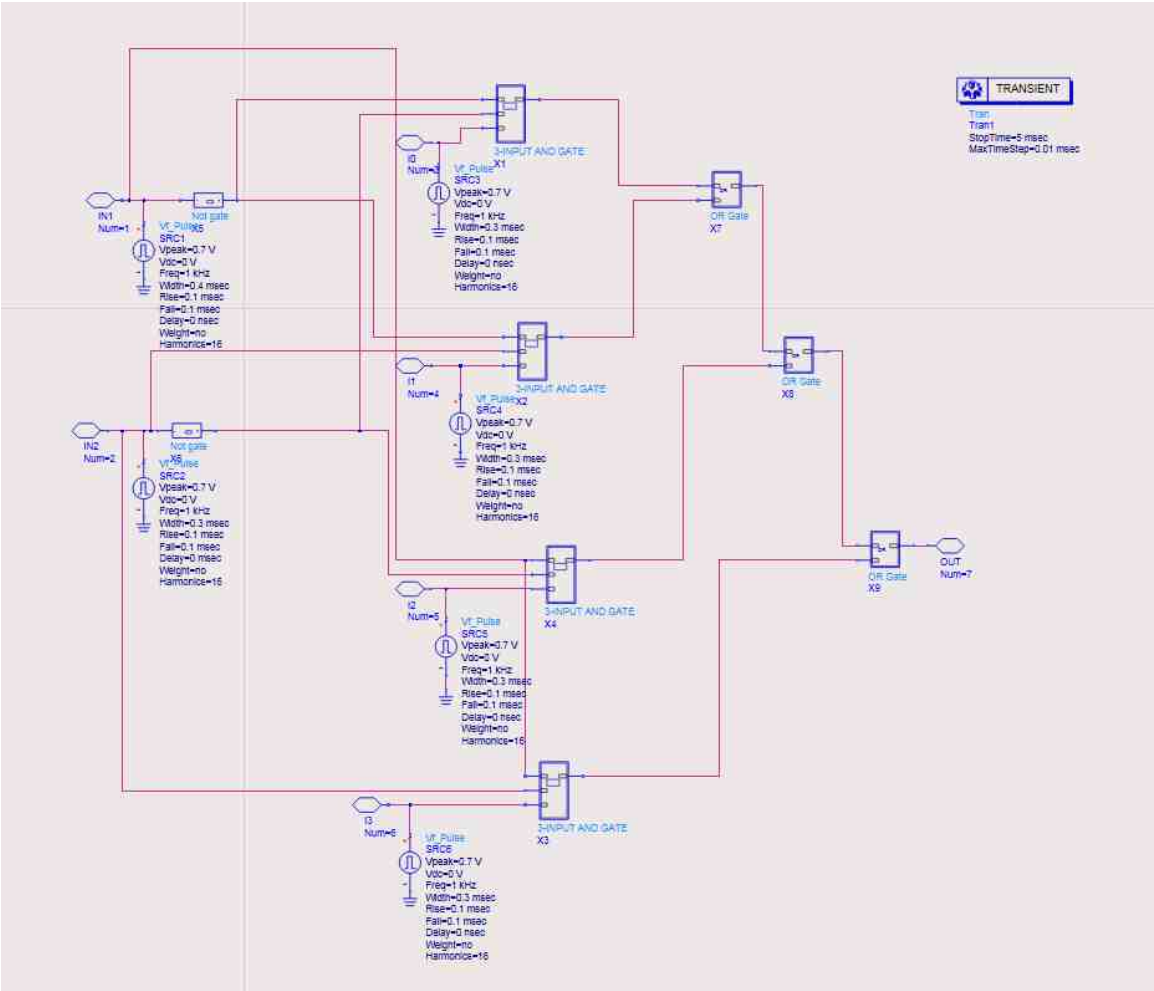


Fig. 2.33. 4:1 MUX Schematic

The boolean expression of the 4:1 mux is given as:

$$Output = \overline{Select2}\ \overline{Select1}\ A + \overline{Select2}\ Select1\ B + Select2\ \overline{Select1}\ C + Select2\ Select1\ D$$

The schematics of the 4:1 MUX and its transient response are shown in Figures 2.33 and 2.34, respectively.

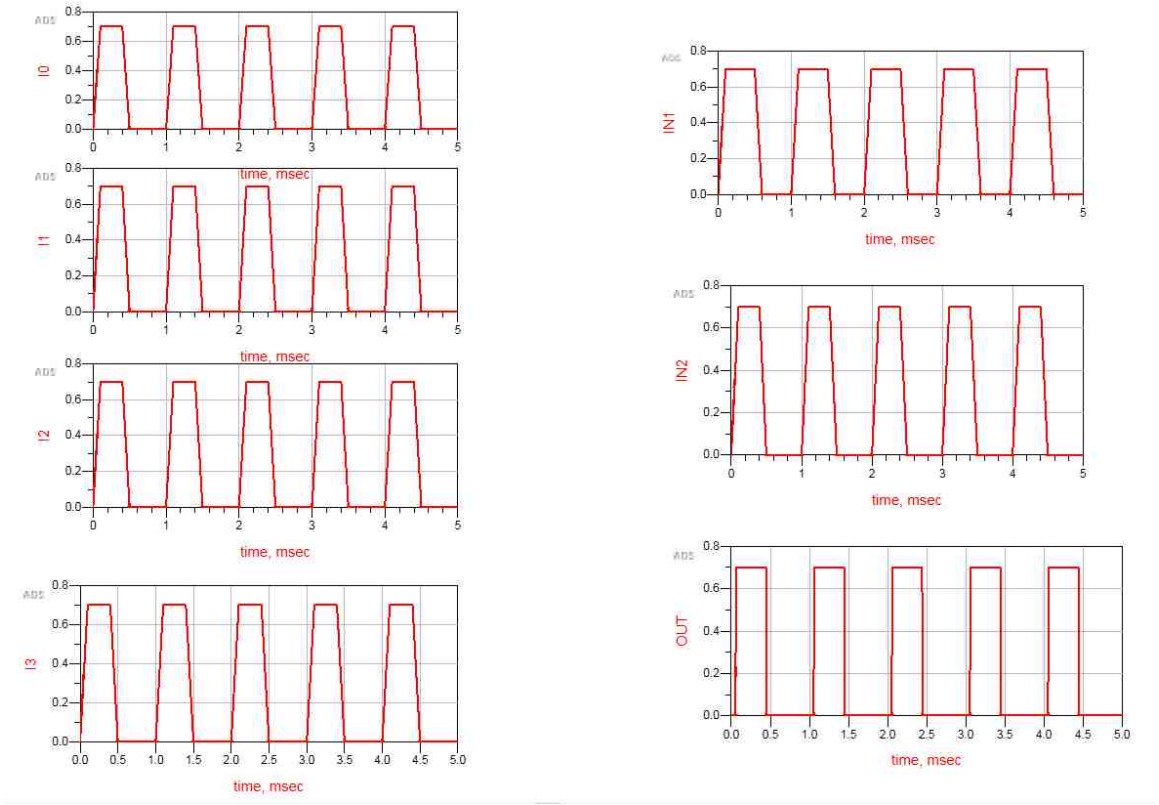


Fig. 2.34. 4:1 MUX Output

2.6 Demultiplexer

A Demux distributes one input into required number of outputs, so known as data distributor. In this study, 1:4 Demux is implemented. A 1:4 Demux is designed with one input, two select lines and four outputs. The truth table for 1:4 Demux is given below with input named Data, select lines named sel1, sel2 and outputs A,B,C, and D.

Input	**Sel2**	**Sel1**	**Output**
Data	0	0	A
Data	0	1	B
Data	1	0	C
Data	1	1	D

The boolean expressions of the 1:4 Demux is given as:

$$A = Data\ \overline{sel}1\ \overline{sel}2$$
$$B = Data\ sel1\ \overline{sel}2$$
$$C = Data\ \overline{sel}1\ sel2$$
$$D = Data\ sel1\ sel2$$

The schematics of the 1:4 Demux and its transient response are shown in Figures 2.35 and 2.36, respectively.

2.7 Comparator

The comparator circuit compares the magnitude of two digital circuits. In this study, 1-bit comparator and 2-bit comparator were implemented.

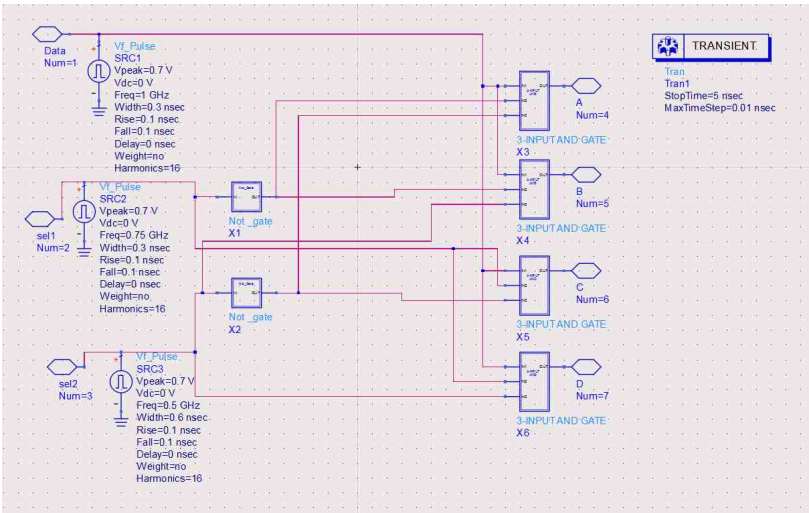


Fig. 2.35. 1:4 Demux Schematic

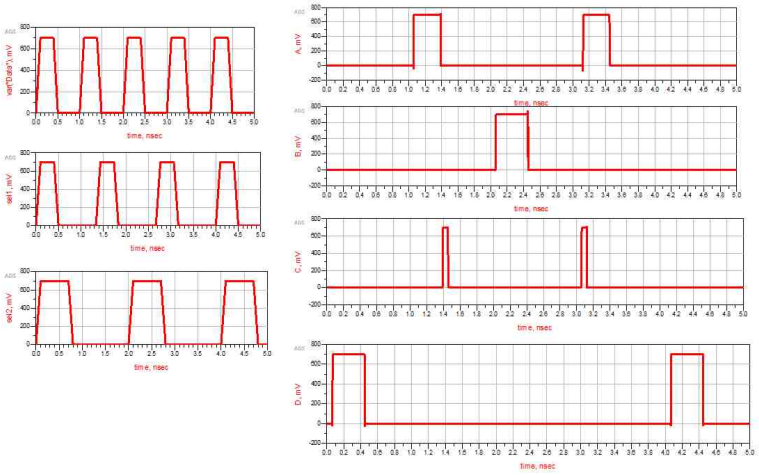


Fig. 2.36. 1:4 Demux Output

2.7.1 1-bit Comparator

It compares the magnitude of two 1-bit binary signals to determine whether one input is greater than, less than or equal to the second input. The truth table of the 1-bit comparator is given below:

A	**B**	**A>B**	**A=B**	**A<B**
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

The boolean expressions of the 1-bit comparator are given as,

$$(A > B) : A\ \overline{B}$$
$$(A = B) : \overline{A}\ \overline{B} + AB = A\ XNOR\ B$$
$$(A < B) : \overline{A}\ B$$

The schematics and transient analysis are shown in Figures 2.37 and 2.38 respectively.

2.7.2 2-bit Comparator

This compares the magnitude of two 2-bit binary signals to determine whether one input is greater than, less than or equal to the second input. The truth table of the 2-bit comparator is given below:

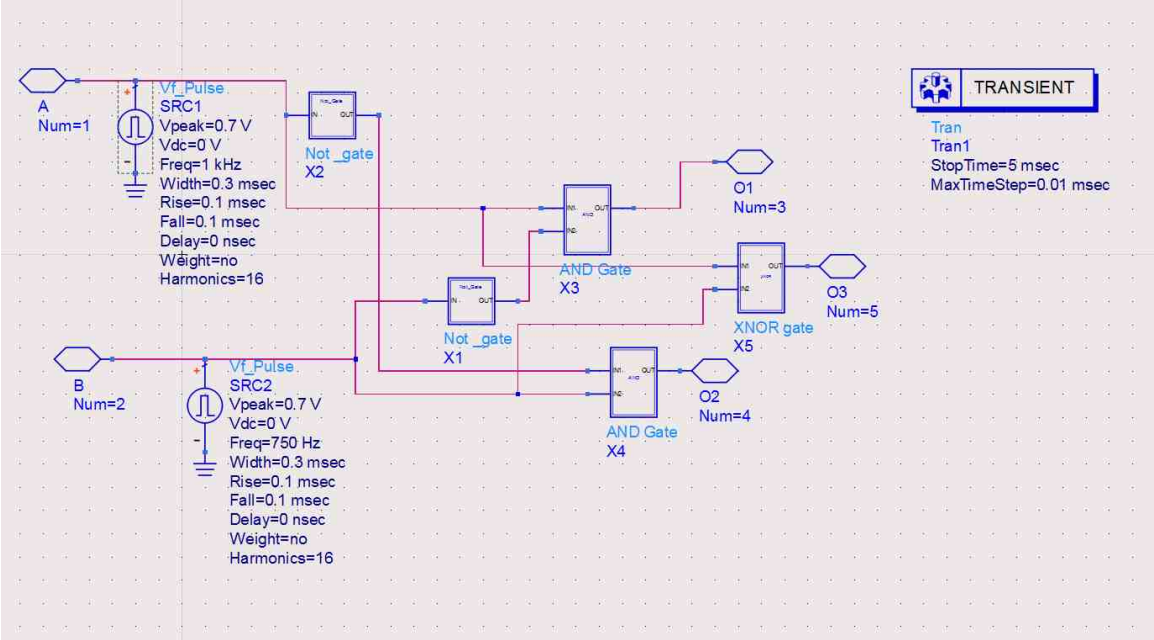


Fig. 2.37. 1-bit Comparator Schematic

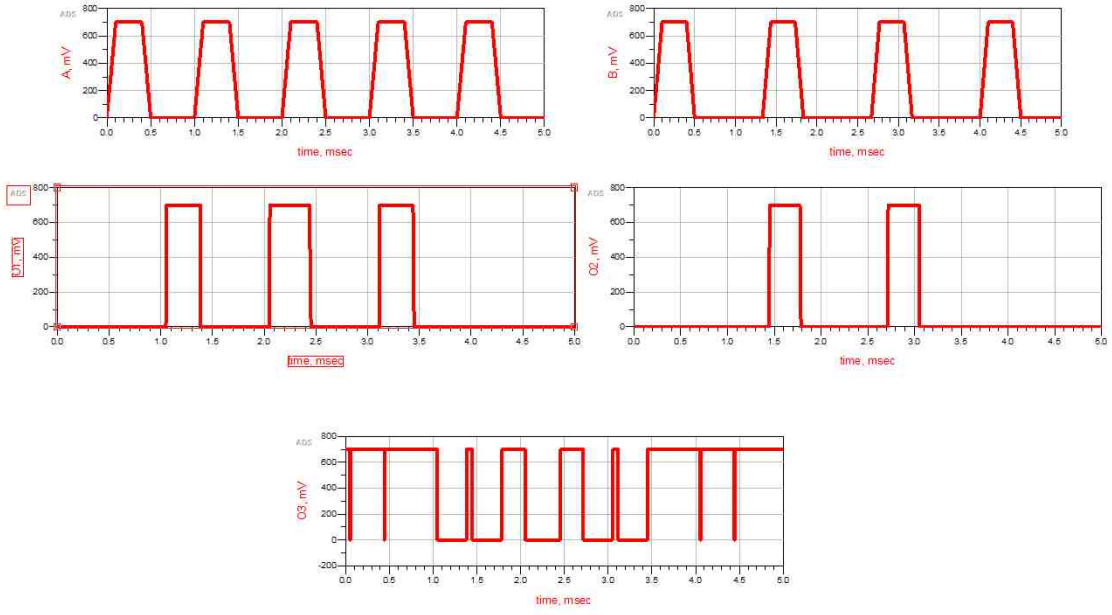


Fig. 2.38. 1-bit Comparator Output

A_2	A_1	B_2	B_1	$A>B$	$A=B$	$A<B$
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

The boolean expressions of the 2-bit comparator are given as,

$$(A > B) : A_2\overline{B_2} + A_1\overline{B_2}\ \overline{B_1} + A_2A_1\overline{B_1}$$

$$(A = B) : (\overline{A_1}\ \overline{B_1} + A_1B_1)(\overline{A_2}\ \overline{B_2} + A_2\ B_2) = (A_1\ XNOR\ B_1)(A_2\ XNOR\ B_2)$$

$$(A < B) : \overline{A_2}\ B_2 + \overline{A_1}\ B_2\ B_1 + \overline{A_2}\ \overline{A_1}\ B1$$

The schematic and transient analysis are shown in figures 2.39 and 2.40, respectively.

2.8 Digital Encoders

Digital Encoders take the input and convert it into equivalent binary code. For an n-bit encoder, 2^n input lines are used. The encoders implemented in this study are 4×2 and 8×3.

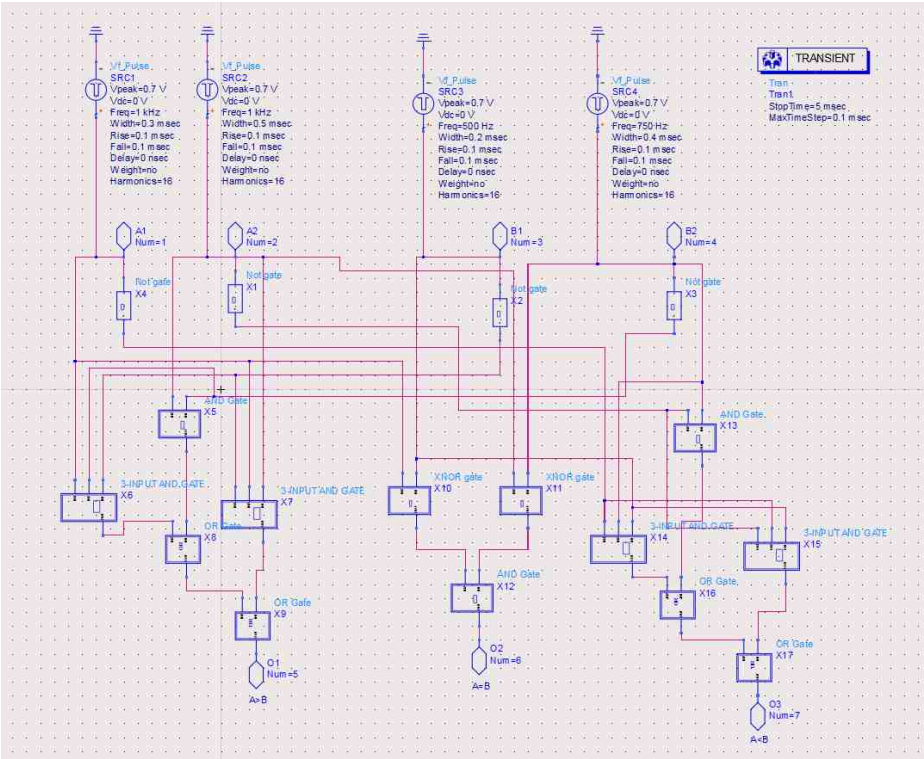


Fig. 2.39. 2-bit Comparator Schematic

2.8.1 4×2 Digital Encoder

For 2-bit Encoder, 4 input lines are used. It is also known as 4×2 Encoder. The truth table of the 2-bit encoder is given as,

D3	D2	D1	D0	Q1	Q0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

The schematics and transient analysis are shown in Figures 2.41 and 2.42, respectively.

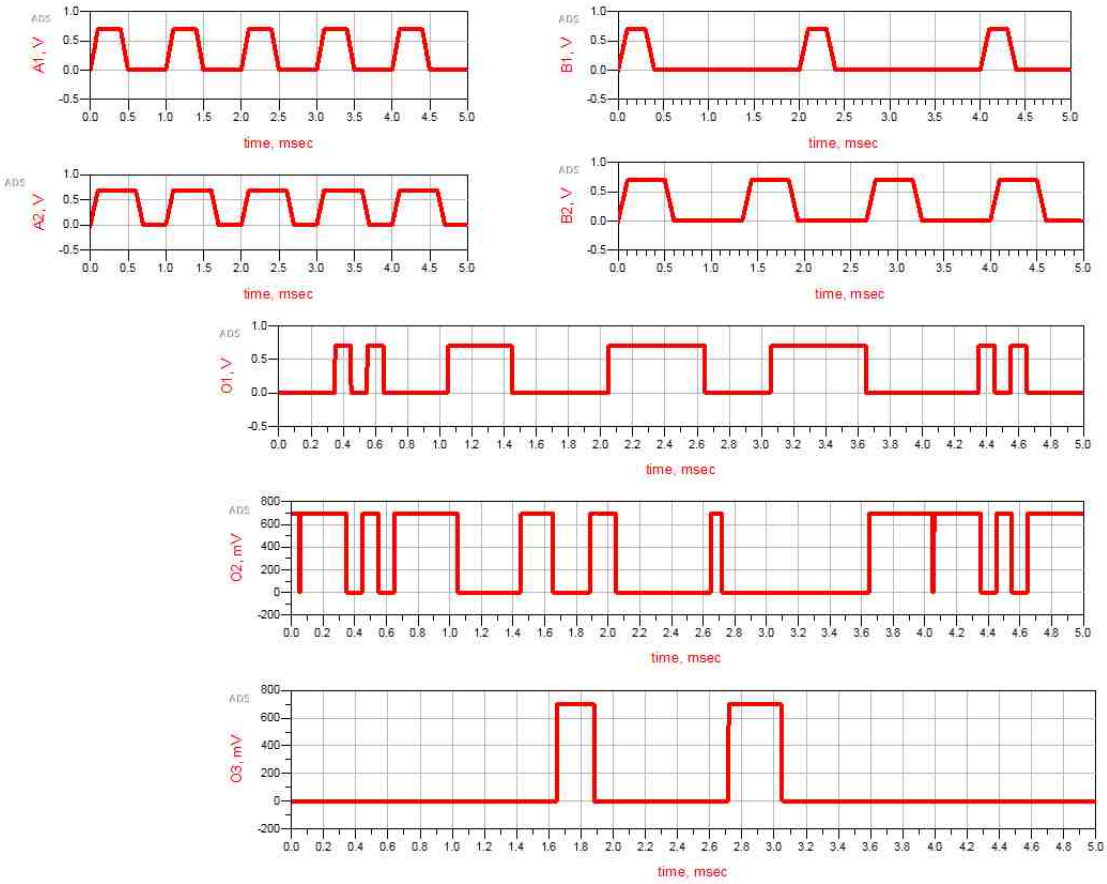


Fig. 2.40. 2-bit Comparator Output

2.8.2 8×3 Digital Encoder

For 3-bit Encoder, 8 input lines are used. It is also known as 8×3 Encoder. The truth table of the 3-bit encoder is shown as,

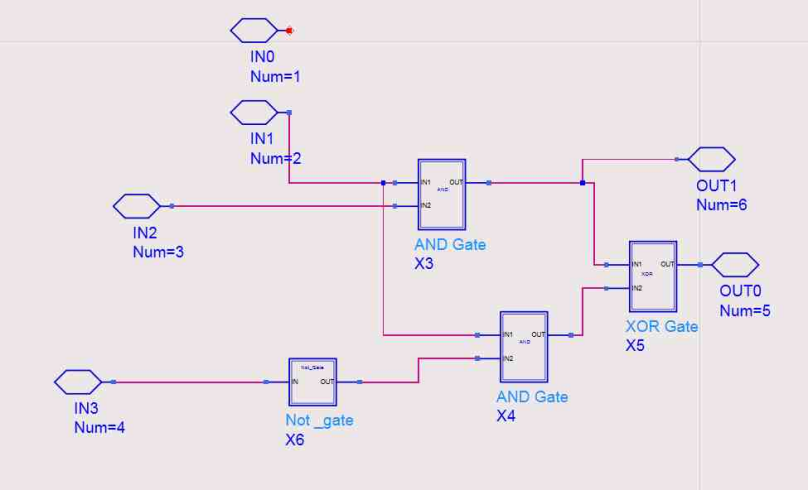


Fig. 2.41. 4×2 Encoder Schematic

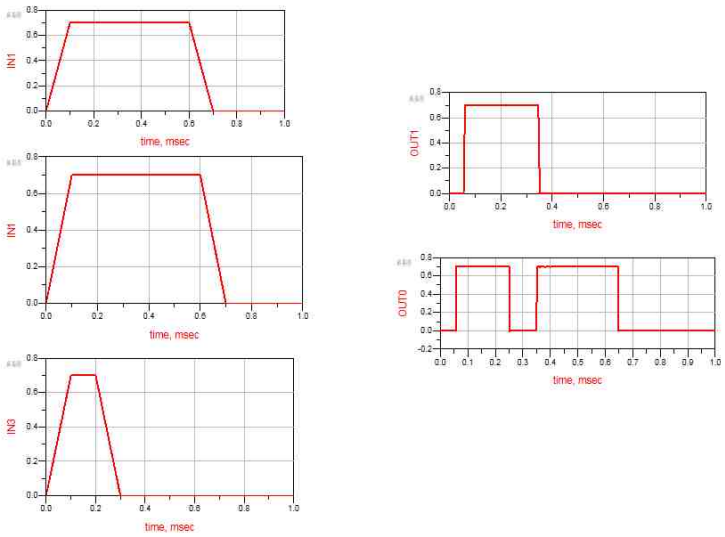


Fig. 2.42. 4×2 Encoder Output

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

The schematics and transient analysis are shown in the Figures 2.43 and 2.44, respectively.

2.9 2:1 Serializer

The serializer is a promising device that accesses and stores data efficiently. It has high gain, high speed, and good memory bandwidth. Powerful applications may include internal buses of a microprocessor that connect to slow devices such as RAMs. Data must be accessed in parallel to fetch and store for high performance.

In this study, 2:1 Serializer was designed and simulated in ADS. The Deven and Dodd are the two parallel data inputs given to a serializer to get a serial output. In this design, for simulation, the Clock, Deven and Dodd were given voltage pulses with different pulse widths as shown in Figure 2.45. The transient analysis of the serializer is shown in Figure 2.46. The serializer is designed using edge triggered D-flipflops, and a 2:1 transmission gate multiplexer. The schematics and timing diagram of the D-flipflop used in the serializer are shown in Figures 2.47 and 2.48 respectively. The design multiplexer used transmission gates inorder to reduce the number of transistors used, and accordingly the power consumption. Furthermore, this design occupies less area on the chip. The schematics of transmission gate and output is shown in Figures 2.49 and 2.50 respectively. Deven and Dodd are given as

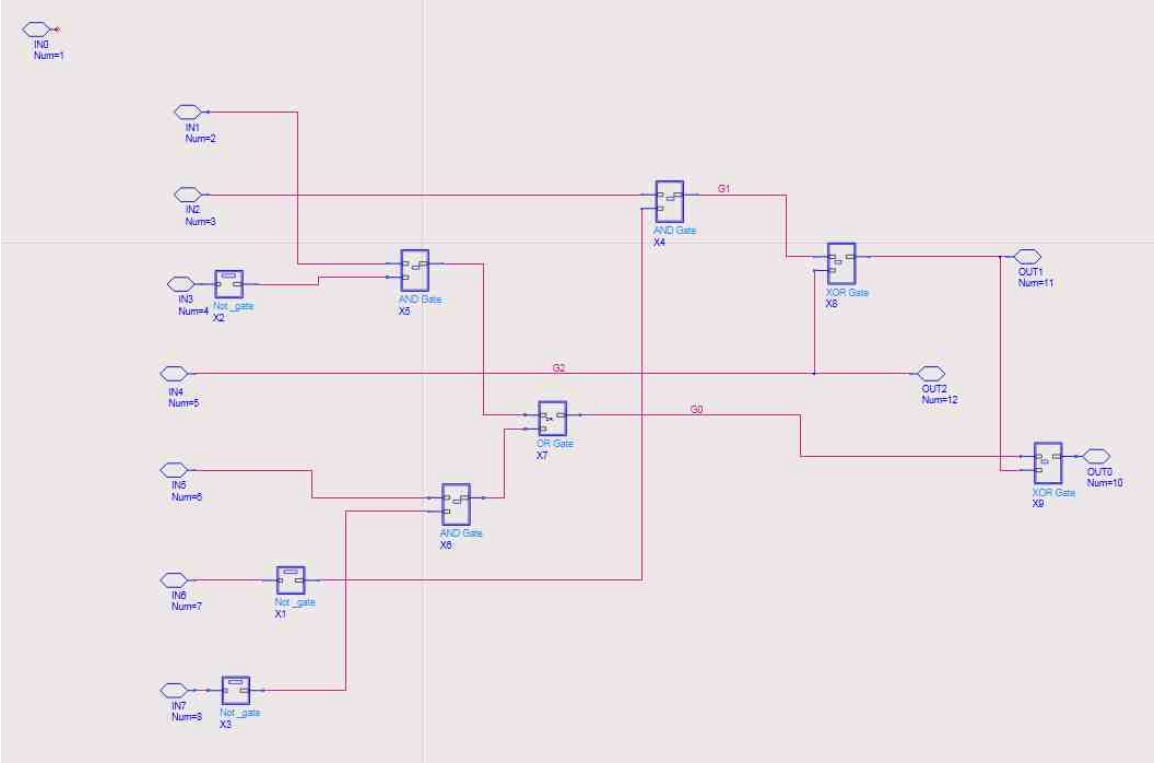


Fig. 2.43. 8×3 Encoder Schematic

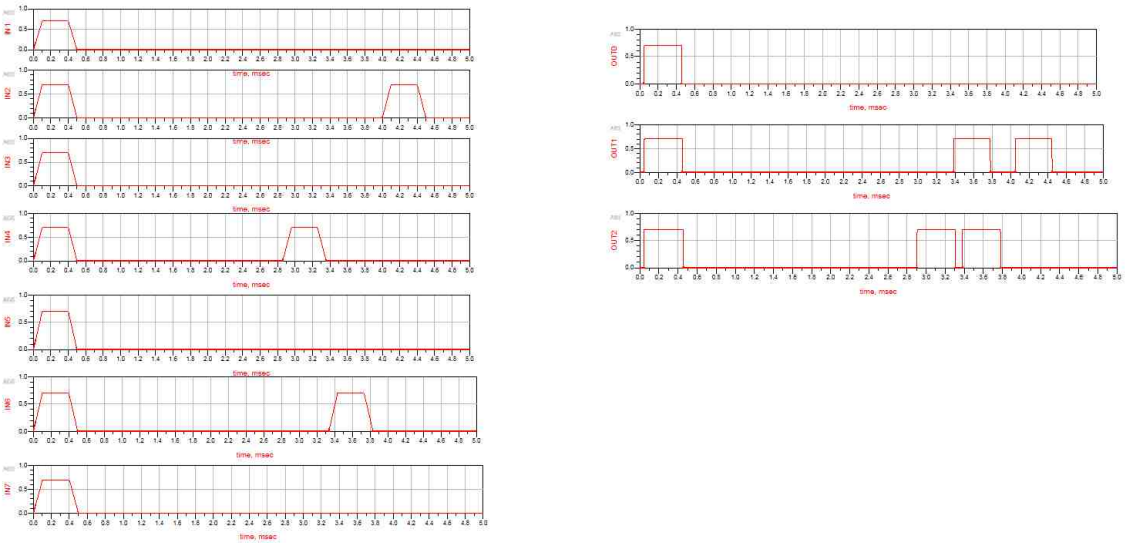


Fig. 2.44. 8×3 Encoder Output

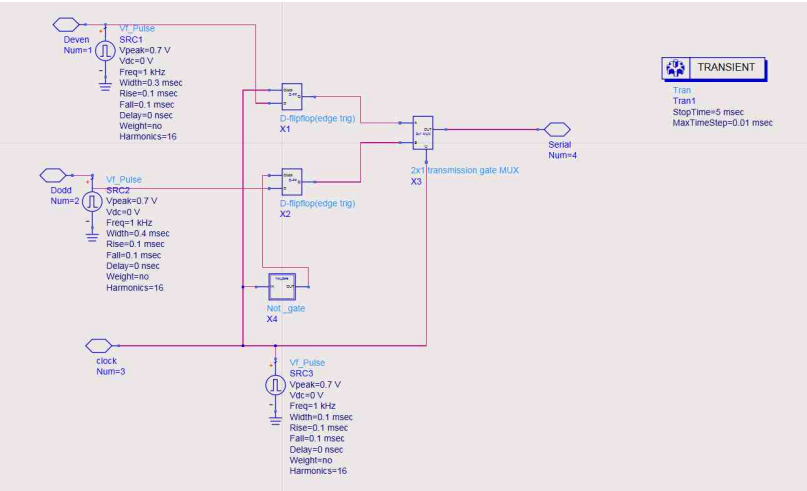


Fig. 2.45. 2:1 Serializer Schematic

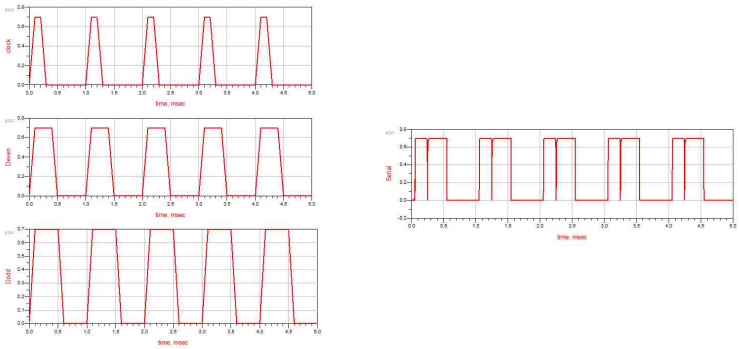


Fig. 2.46. 2:1 Serializer Output

D-inputs for clock synchronized edge triggered flipflops. For a low clock signal, the multiplexer gives Deven as output, and for a high clock signal the multiplexer gives Dodd as output.

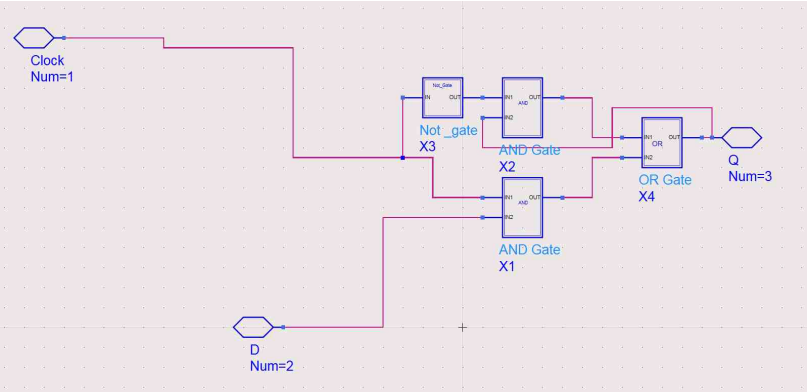


Fig. 2.47. D-Flipflop Schematic

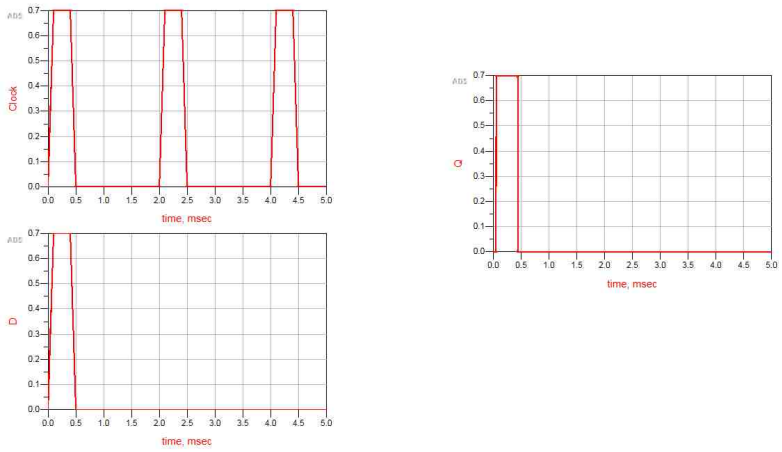


Fig. 2.48. D-Flipflop Output

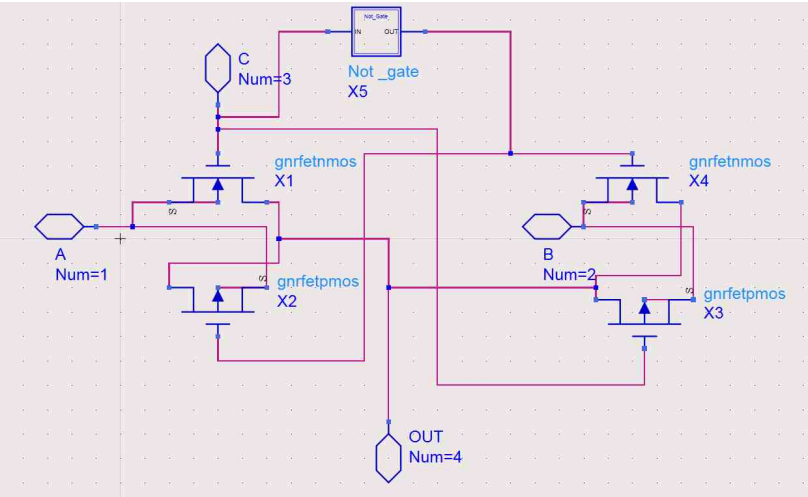


Fig. 2.49. Transmission Gate MUX Schematic

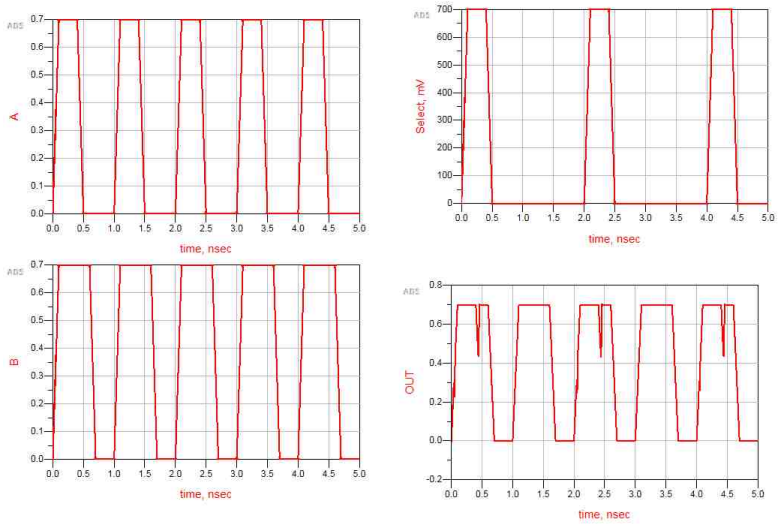


Fig. 2.50. Transmission Gate MUX Output

3. THE GNRFET ANALOG DEVICES AND CIRCUITS

The analog devices implemented in this study are Power amplifiers and differential voltage amplifier. The different power amplifier classes implemented in this study were class A, Class B and Class AB. These were implemented to study the power gain, noise figure, stability, and harmonics for GNRFET based amplifiers. These high-speed amplifiers have wide range of applications in real world such as sound systems, wireless communications, satellite systems, embedded systems, and IoT systems.

3.1 Class A Power Amplifier

In class A amplifier the output power flows through one complete cycle of the input AC signal. Class A operates in the linear region of the I-V characteristics of the GNRFET. Class A amplifiers can amplify small signals with no distortion but at low power and low efficiency rate [13].The schematics design of class A amplifier is shown in Figure 3.1. The input and output characteristics are shown in Figures 3.2 and 3.3 respectively. The voltage gain of this amplifier is near unity.

The power gain, noise figure, stability factor K, source and load impedances are calculated. Figure 3.4 and 3.5 show the stability and Noise Figure respectively. Figure 3.6 shows the power gain, noise figure and their corresponding impedances. Figure 3.7 shows the harmonics of class A amplifier.

3.2 Class B Power Amplifier

In class B amplifier the output power flows for only half cycle of the input AC cycle. Class B power amplifier shows high efficiency when compared to the class A amplifier. Class B power amplifier exhibits distortion which is the main disadvantage

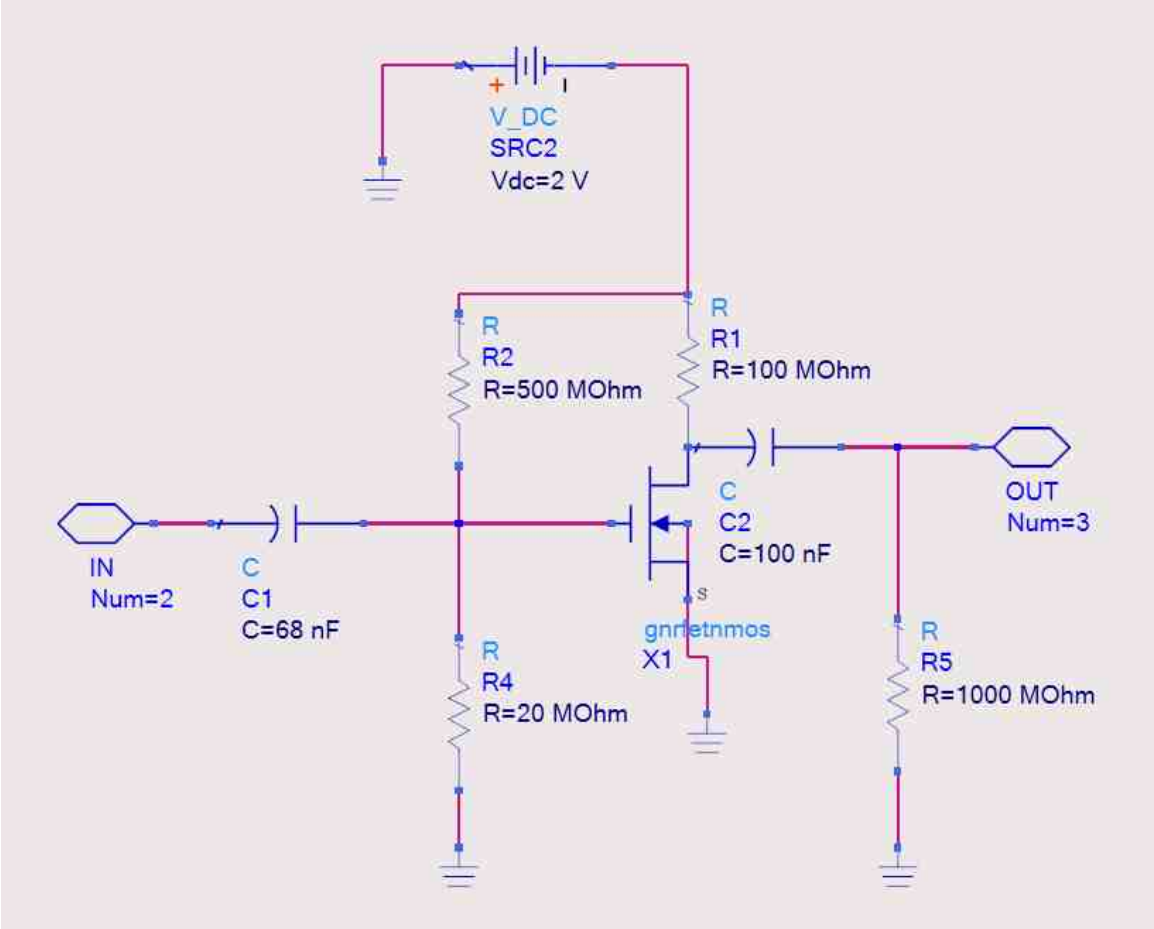


Fig. 3.1. Class A Power Amplifier Schematic

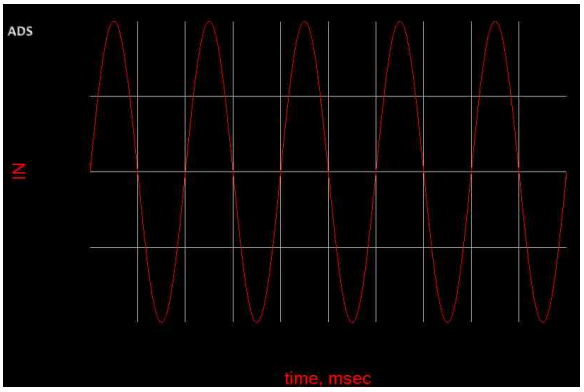


Fig. 3.2. Class A Input Signal

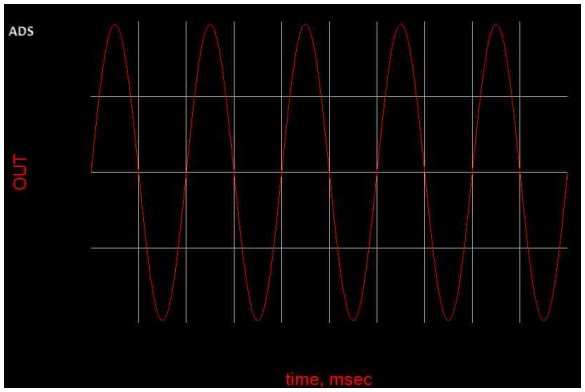


Fig. 3.3. Class A Output Signal

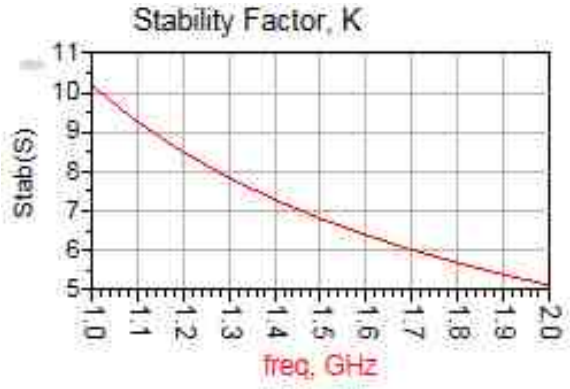


Fig. 3.4. Graph Representing Class A Stability

Fig. 3.5. Graph Representing Class A Noise Figure

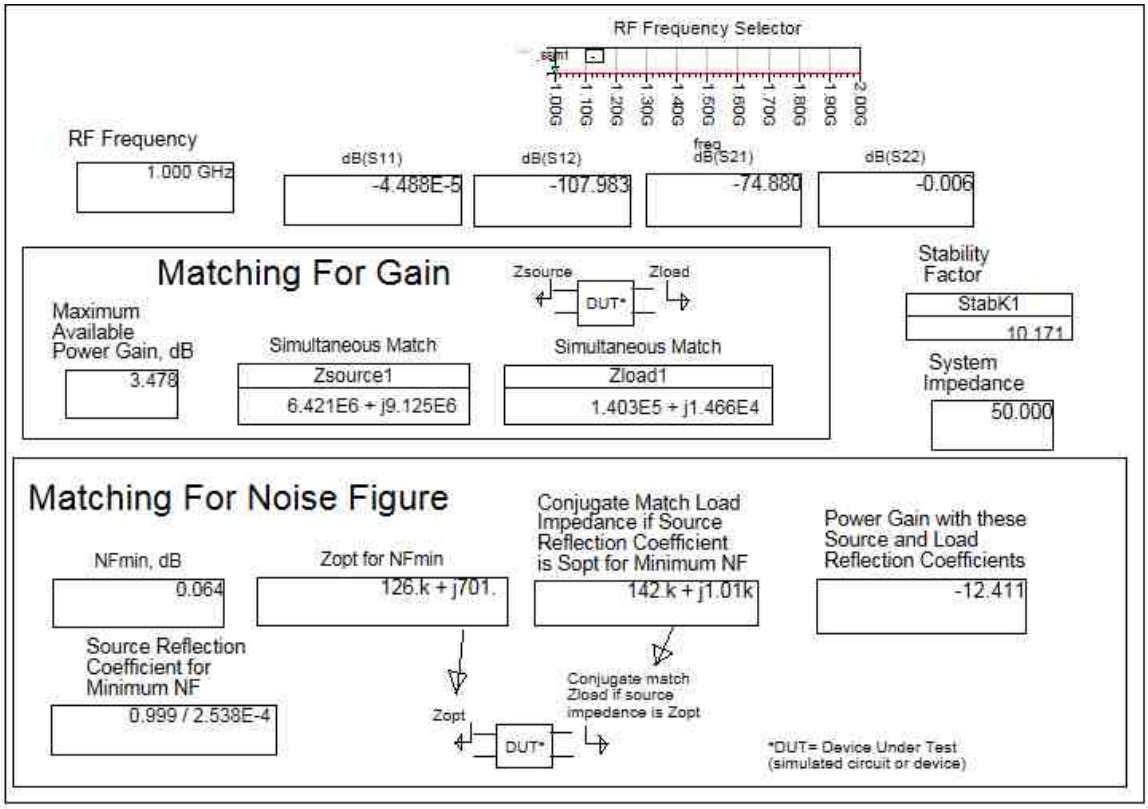
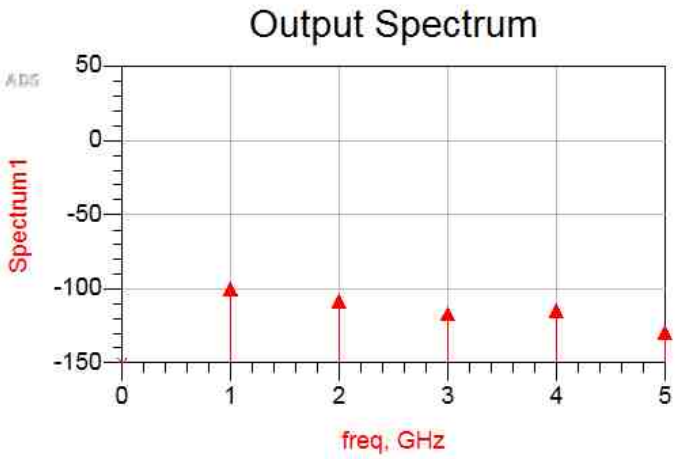


Fig. 3.6. Class A Power Gain, Noise Figure and Corresponding Input, Output Impedances



Fundamental Frequency

1.000 GHz

Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
-8.589	-17.048	-14.906	-29.399

Fig. 3.7. Class A Harmonics

of this class [14]. The schematic design of class B amplifier is shown in Figure 3.8. The input and output characteristics of class B amplifier are shown in Figures 3.9 and 3.10 respectively.

The power gain, noise figure, stability factor K, source and load impedances are calculated. Figure 3.11 and 3.12 show the stability factor and Noise Figure respectively. Figure 3.13 shows the power gain, noise figure, and their corresponding impedances. Figure 3.14 shows harmonics of class B amplifier.

3.3 Class AB Power Amplifier

Class AB is formed by combining class A and class B to combine the advantages of both classes. The output power in class AB amplifier flows for more than half cycle and less than a complete cycle of the AC input cycle. The distortion of the class B is eliminated and the efficiency is increased [15]. The schematic design of class AB amplifier is shown in Figure 3.15. The input and output characteristics of class AB amplifier are shown in Figures 3.16 and 3.17 respectively.

The power gain, noise figure, stability factor K, source and load impedances are calculated. Figure 3.18 and 3.19 show the stability factor and Noise Figure respectively. Figure 3.20 shows the power gain, noise figure and their corresponding impedances. Figure 3.21 shows harmonics of class AB amplifier.

3.4 Differential Amplifier

It is a voltage amplifier. The output voltage is the voltage difference between two inputs. The differential amplifier may also provide voltage gain. The schematics and transient analysis are shown in Figures 3.22 and 3.23, respectively.

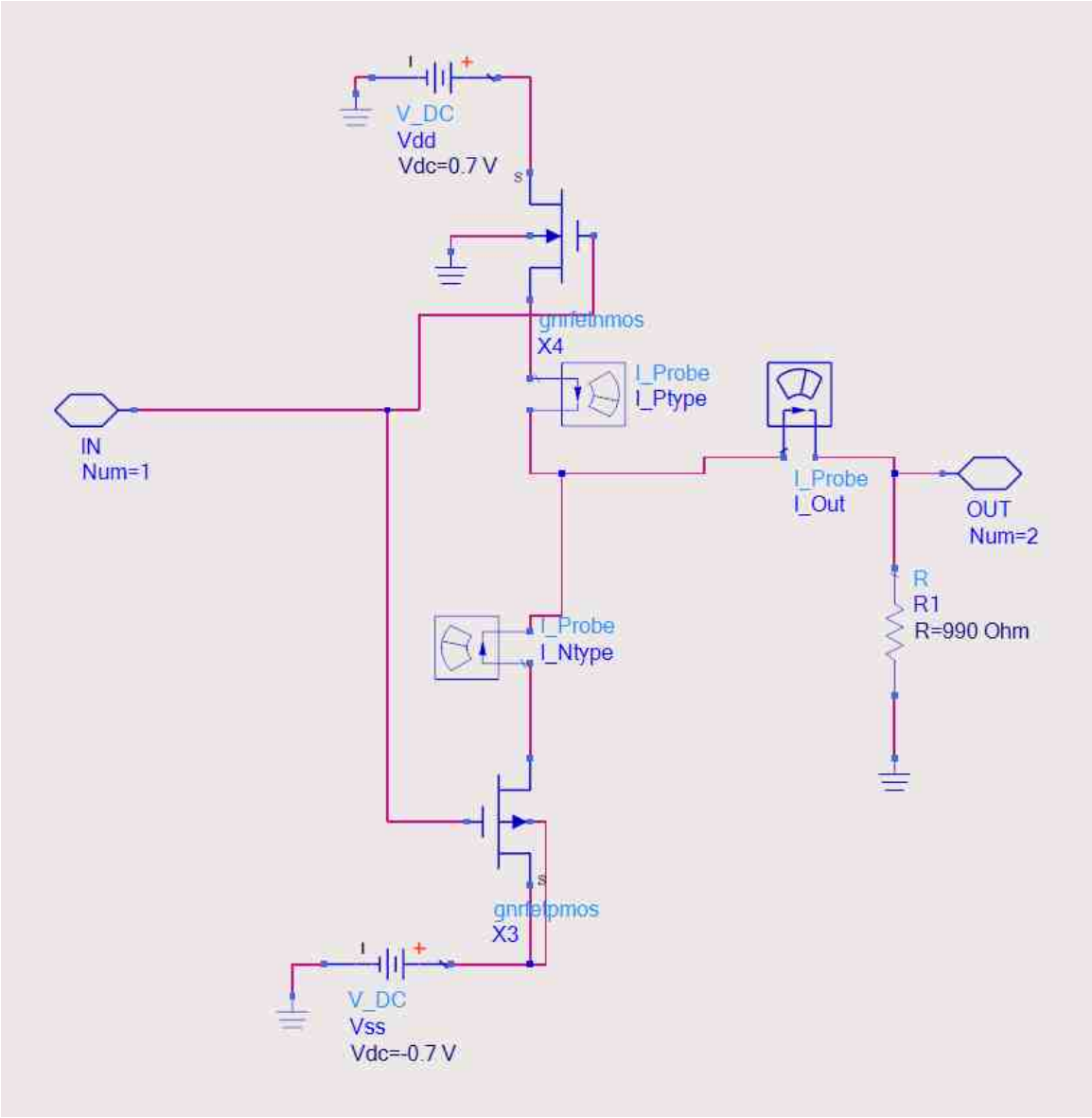


Fig. 3.8. Class B Power Amplifier Schematic

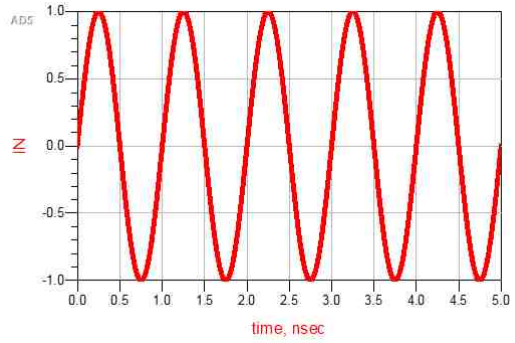


Fig. 3.9. Class B Input Signal

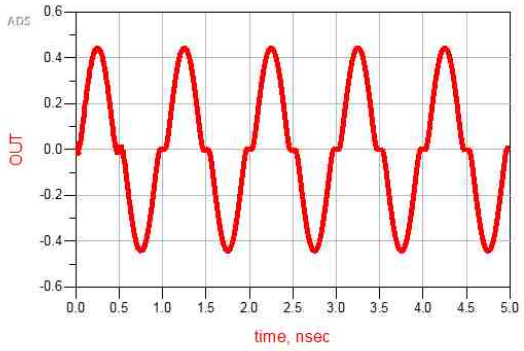


Fig. 3.10. Class B Output Signal

Fig. 3.11. Graph Representing Class B Stability

Fig. 3.12. Graph Representing Class B Noise Figure

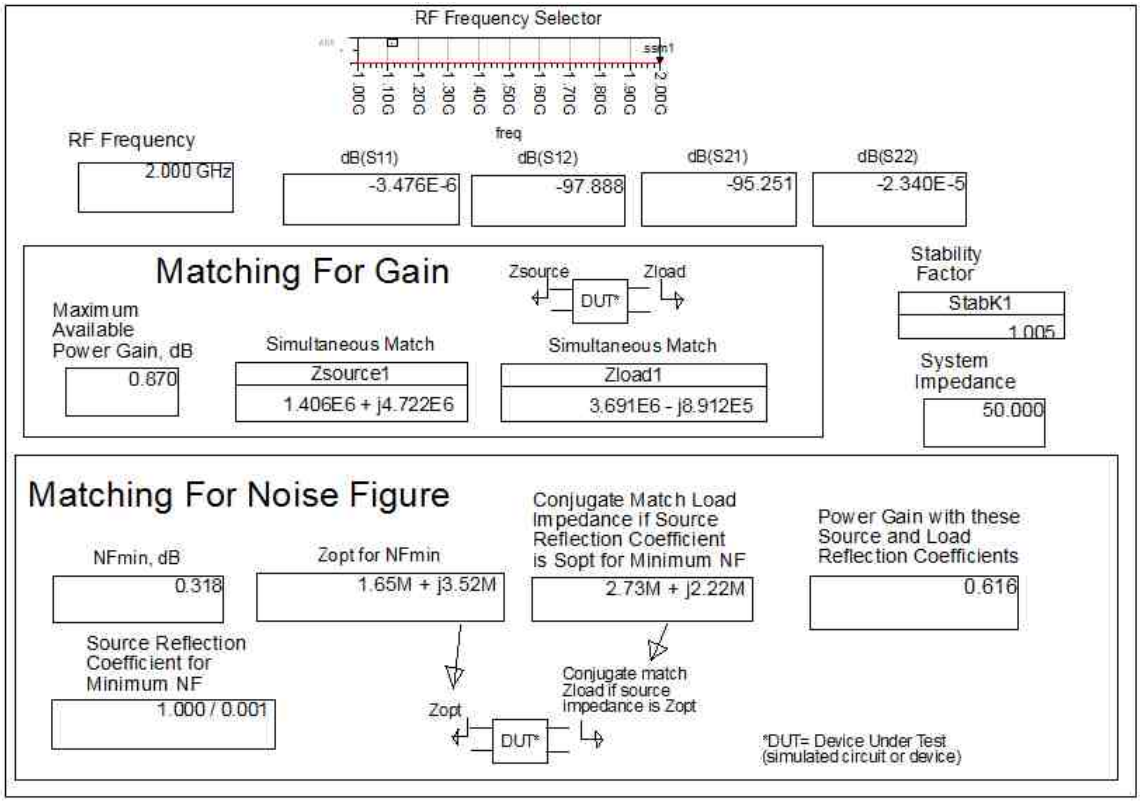
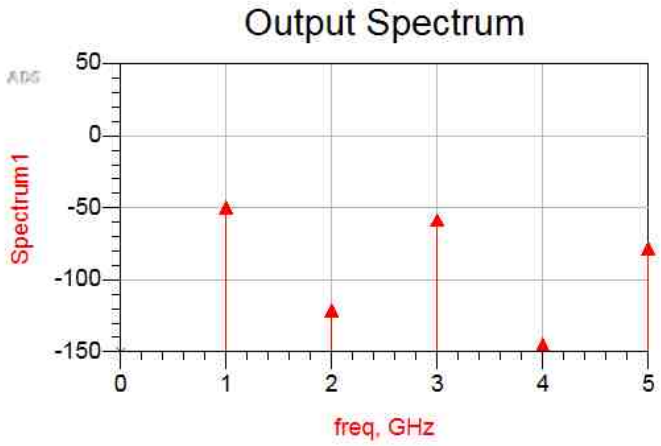


Fig. 3.13. Class B Power Gain, Noise Figure and Corresponding Input, Output Impedances



Fundamental Frequency

1.000 GHz

Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
-71.458	-8.946	-95.143	-28.440

Fig. 3.14. Class B Harmonics

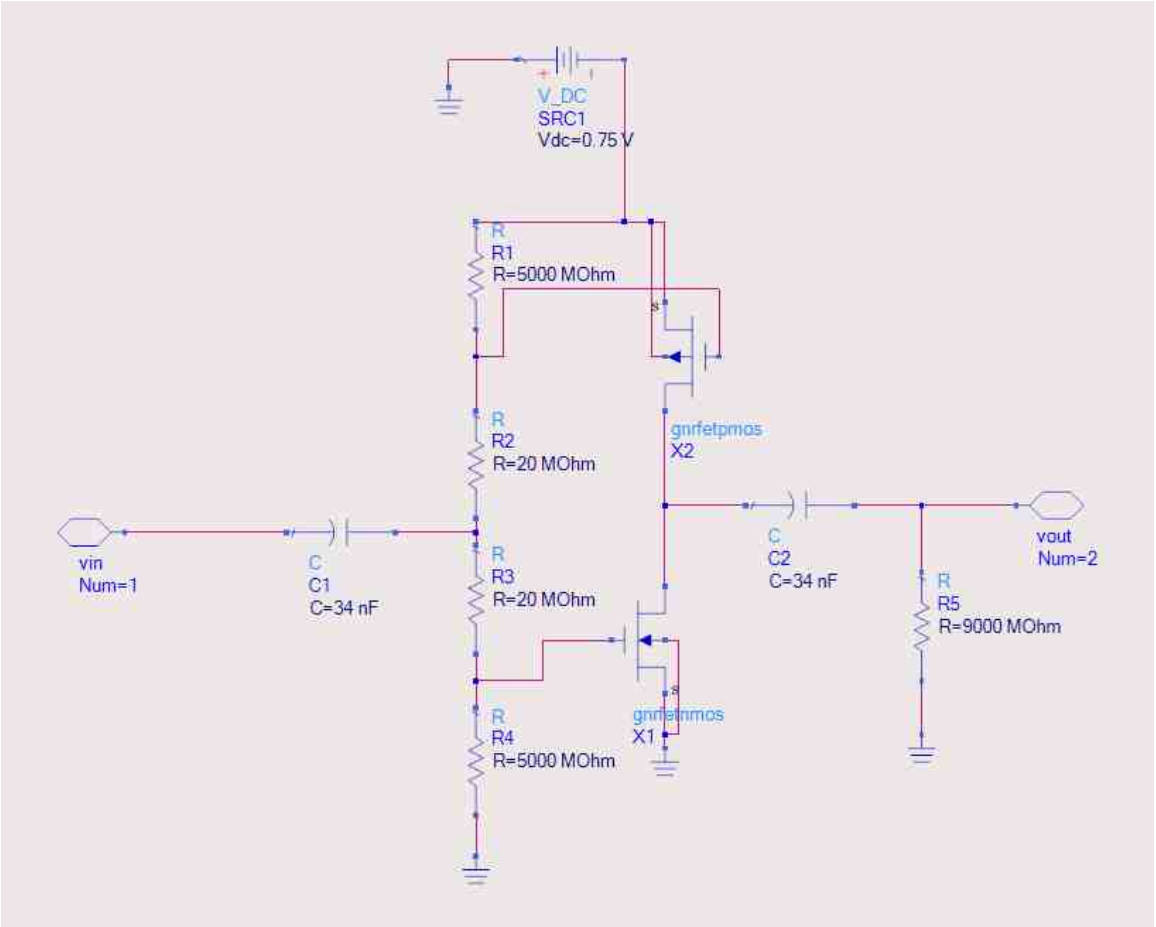


Fig. 3.15. Class AB Power Amplifier Schematic

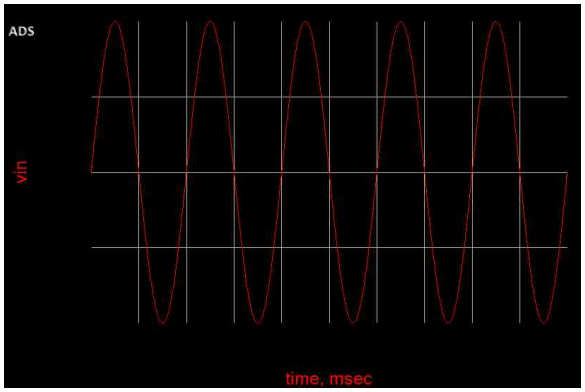


Fig. 3.16. Class AB Input Signal

Fig. 3.17. Class AB Output Signal

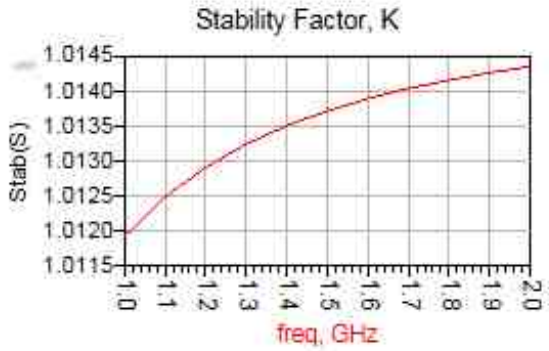


Fig. 3.18. Graph Representing Class AB Stability

Fig. 3.19. Graph Representing Class AB Noise Figure

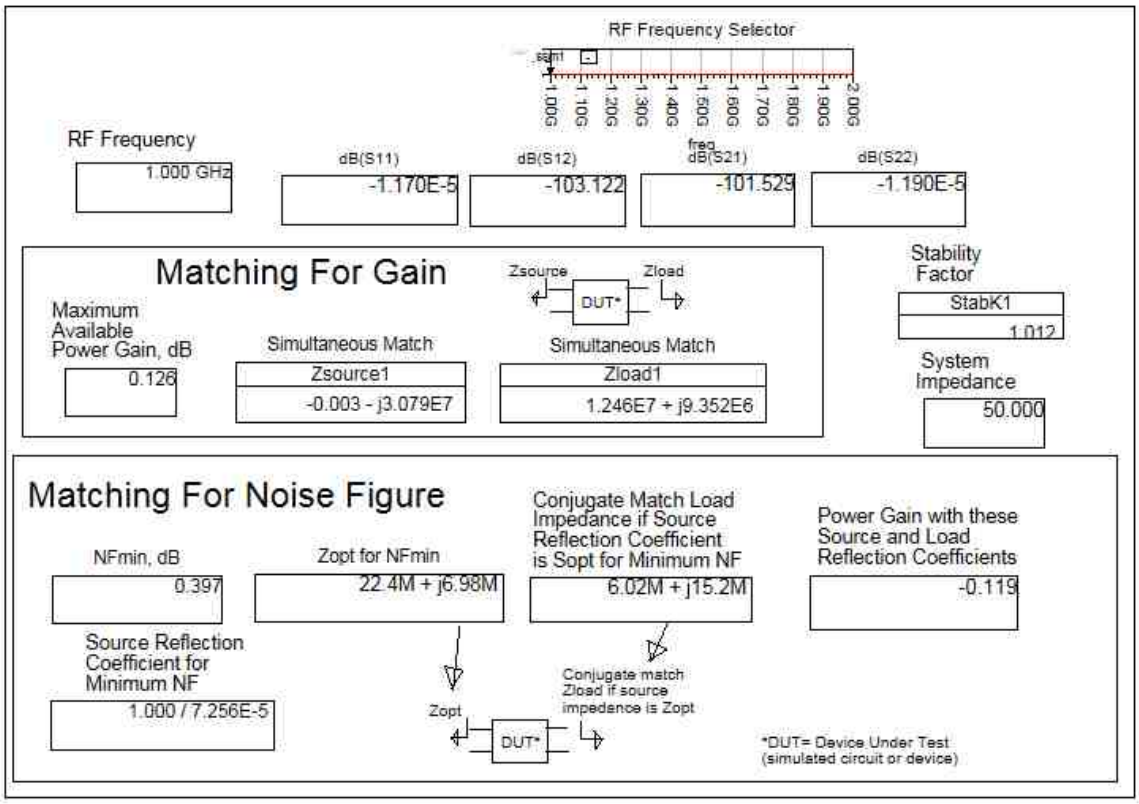
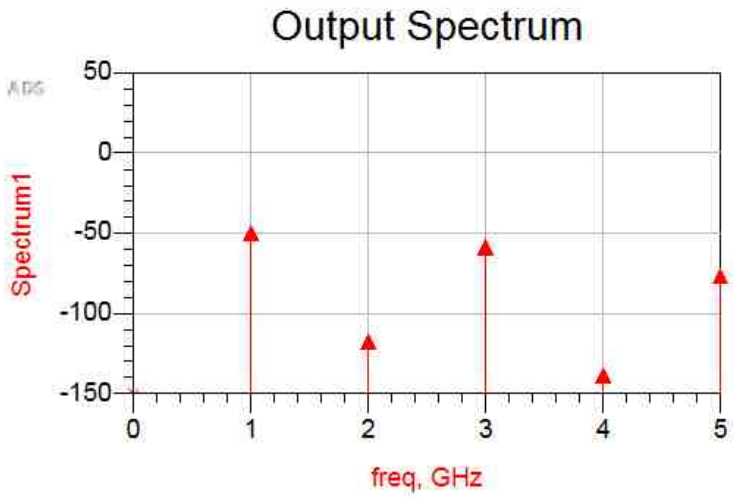


Fig. 3.20. Class AB Power Gain, Noise Figure and Corresponding Input, Output Impedances



Fundamental Frequency

1.000 GHz

Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
-67.870	-8.938	-88.949	-27.324

Fig. 3.21. Class AB Harmonics

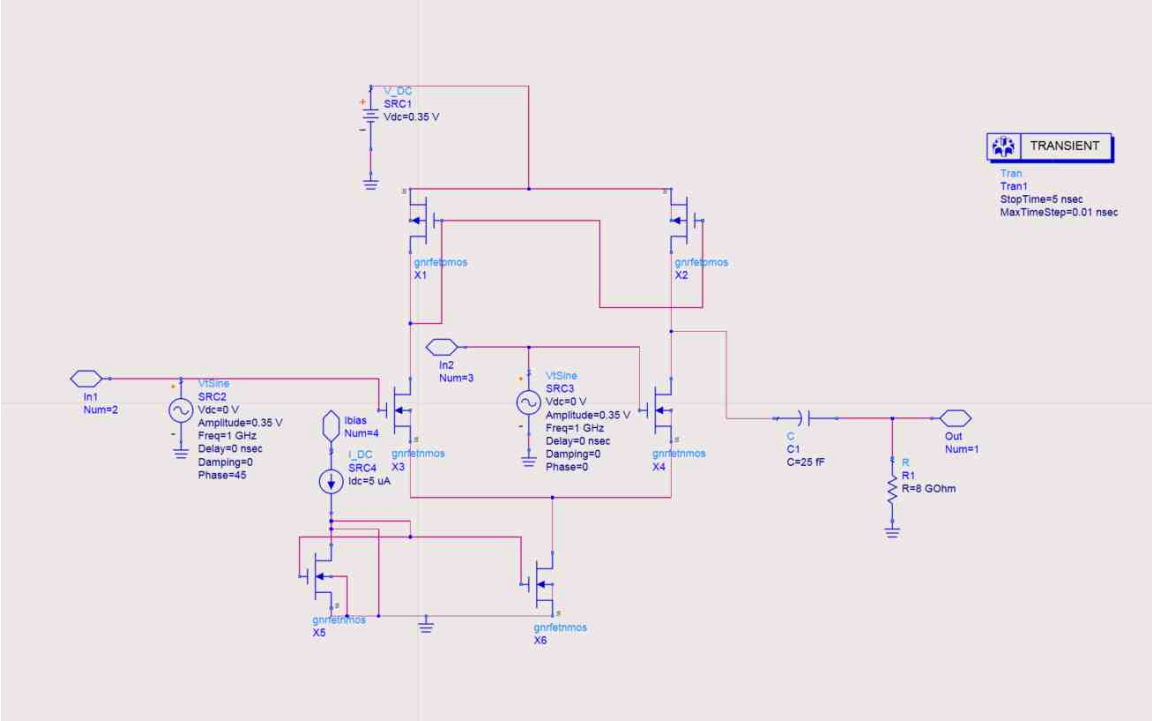


Fig. 3.22. Differential Amplifier Schematic

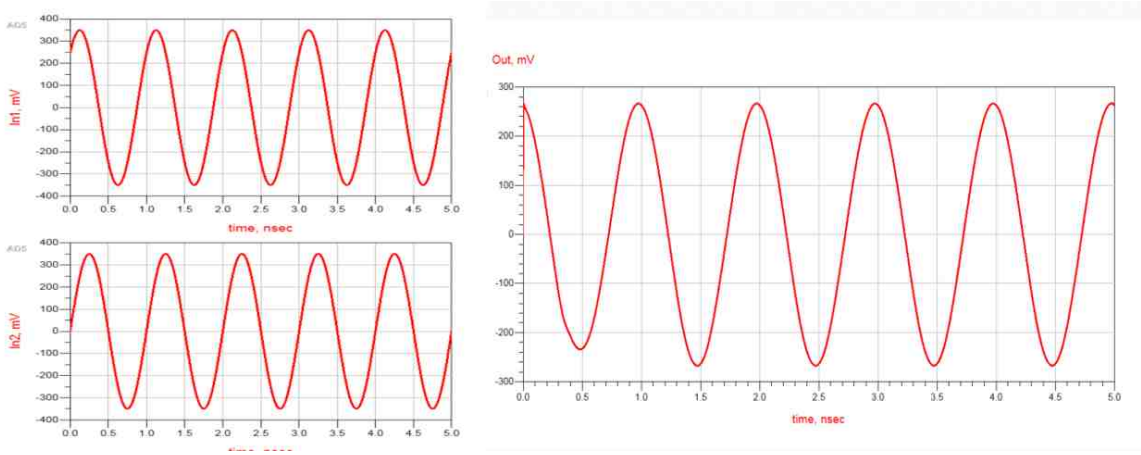


Fig. 3.23. Differential Amplifier Output

4. THE GNRFET MIXED SIGNAL DEVICES AND CIRCUITS

Mixed signal circuits are designed using both analog and digital devices. Mixed signal circuits are used in many applications such as communications, embedded systems and IoT devices and systems [16]. Analog-to-Digital converters and Digital-to-Analog converters are implemented in this study. ADS platform with minimum 10nm channel sized GNRFET with an input voltage of 0.7V was considered.

4.1 Analog-to-Digital Converters (ADC)

ADCs are among the essential components in mixed signal systems where both analog and digital devices are integrated. Physical quantities available in real world need analog-to-digital converters to convert analog signals into digital form, in order to enable DSP processors evaluate the analog information and process it as needed [17]. In this work, TIQ (Threshold Inverting Quantization) comparator using two cascaded inverters as a voltage comparator and thermometer code to binary code encoder are used [18]. The block diagram of an ADC is shown in Figure 4.1.

In TIQ, first inverter switches the voltage internally whereas second inverter acts as a gain booster and manages the propagation delay. As the number of graphene nano ribbons of the P-type and N-type GNRFETs varied, the inverters generate different switching voltages, which act as the reference voltage to compare the input analog signal with TIQs are arranged in parallel. For n-bit ADC, we need 2^n TIQ comparators [19]. The schematic of the TIQ is shown in the Figure 4.2.

The encoder used here is a thermometer code to binary code encoder. Firstly, the thermometer code was converted to the grey code, then to the binary code. The

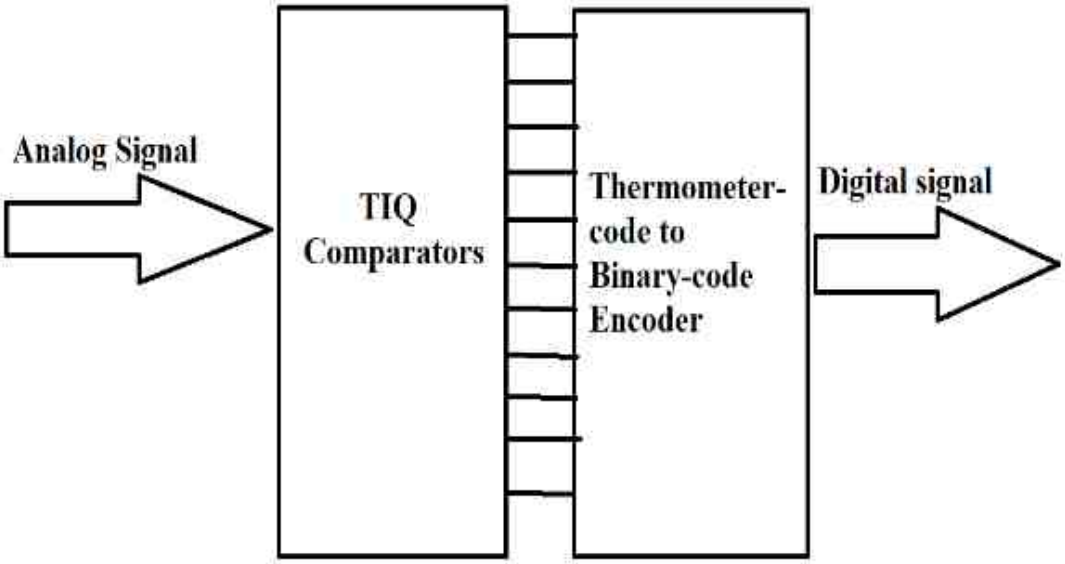


Fig. 4.1. ADC Block Diagram

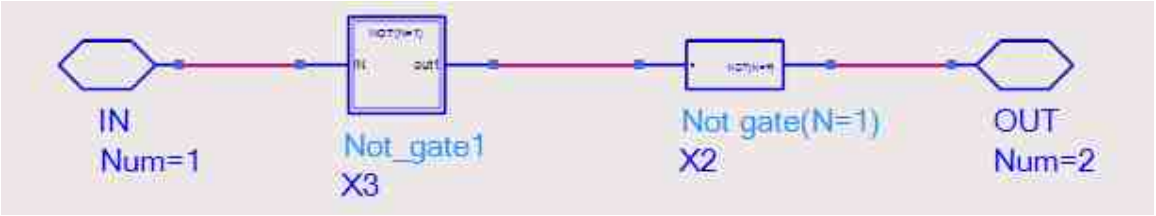


Fig. 4.2. TIQ Schematic

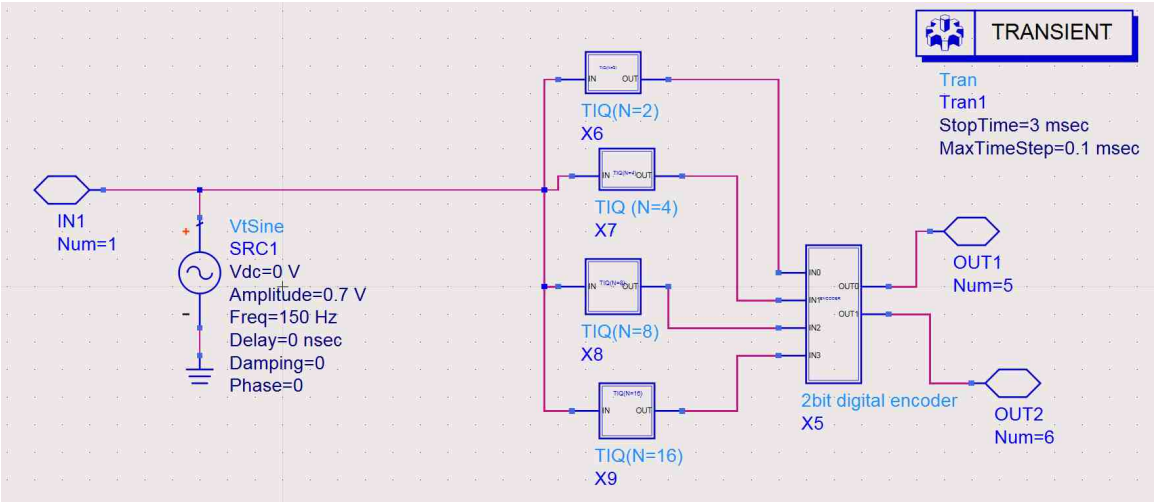


Fig. 4.3. 2-bit ADC Schematic

inputs of the encoder were taken from the outputs of TIQs that wer arranged in parallel [19].

The ADCs implemented in this study were 2-bit, 3-bit, and 4-bit ADCs.

4.1.1 2-bit ADC

In order to design the 2-bit ADC, 4 different TIQs were used. When P-type GNRFET uses number of ribbons equals 2, the N-type GNRFET uses a number of ribbons to be 15. Similarly, the remaining combinations (P-type GNRFET, N-type GNRFET) used were (4,13), (8,9), (16,1). The encoder used in 2-bit ADC was 4X2 Encoder. The schematics and transient response of the 2-bit ADC are shown in Figures 4.3 and 4.4 respectively.

4.1.2 3-bit ADC

In order to design 3-bit ADC, 8 different TIQs were used. When P-type GNRFET uses number of ribbons equals 1, the N-type GNRFET uses a number of ribbons to

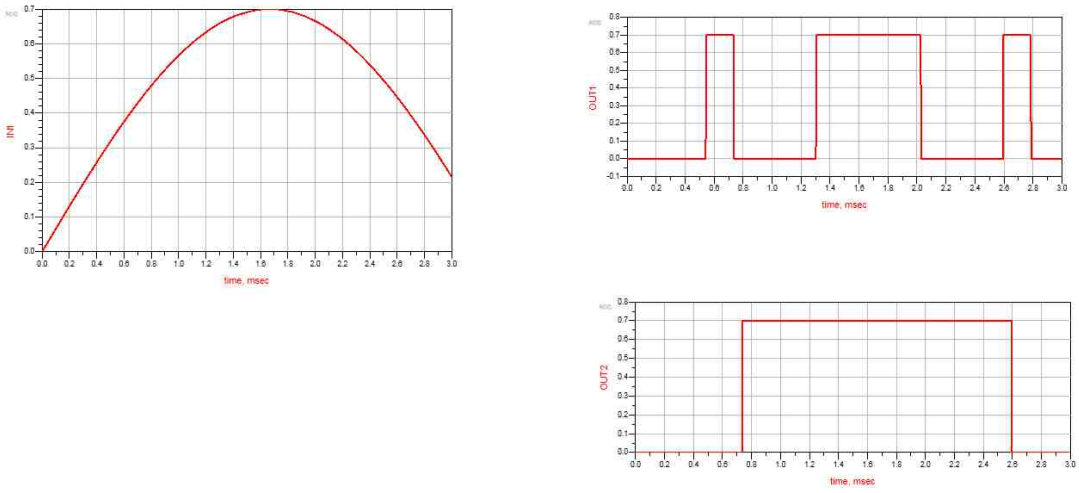


Fig. 4.4. 2-bit ADC Output

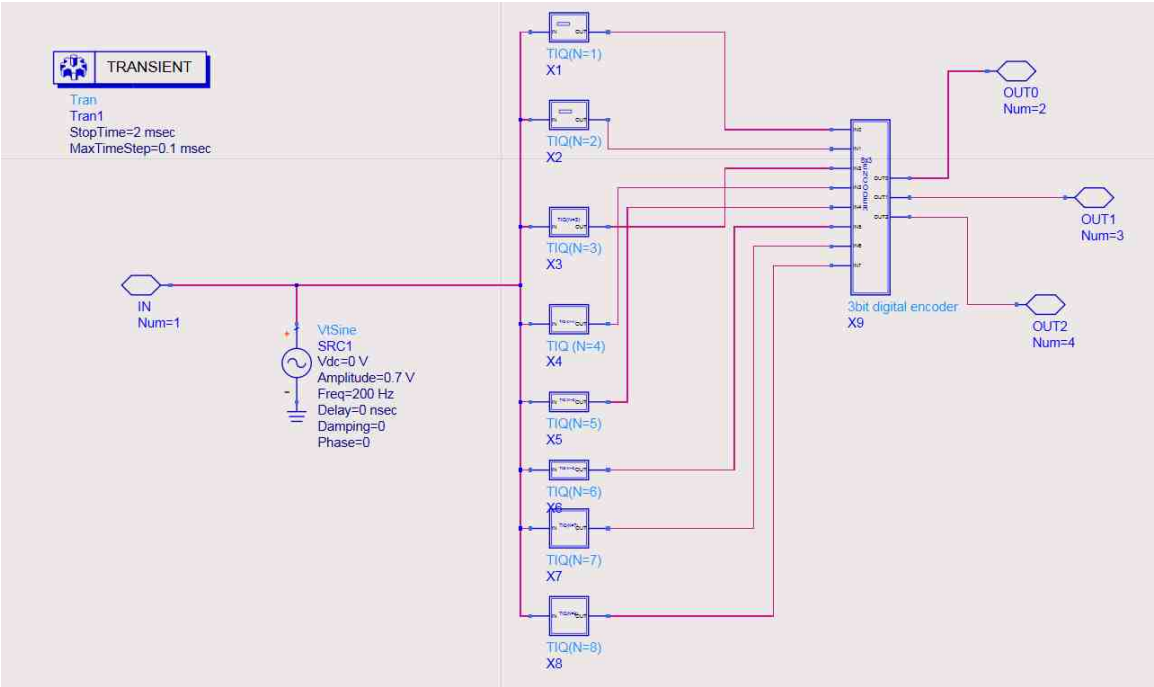


Fig. 4.5. 3-bit ADC Schematic

be 16. Similarly, the remaining combinations (P-type GNRFET, N-type GNRFET) used were (2,15), (3,14), (4,13), (5,12), (6, 11), (7,10), (8,9). The encoder used in 3-bit ADC was 8X3 Encoder. The schematics and transient response of the 3-bit ADC are shown in Figures 4.5 and 4.6 respectively.

4.1.3 4-bit ADC

In order to design 4-bit ADC, 16 different TIQs were used. When P-type GNRFET uses number of ribbons equals 1, the N-type GNRFET uses a number of ribbons to be 16. Similarly, the remaining combinations (P-type GNRFET, N-type GNRFET) used were (2,15), (3,14), (4,13), (5,12), (6, 11), (7,10), (8,9), (9,8), (10,7), (11,6), (12,5), (13,4), (14,3), (15,2), (16,1). The encoder used in 4-bit ADC was 16X4 Encoder. The

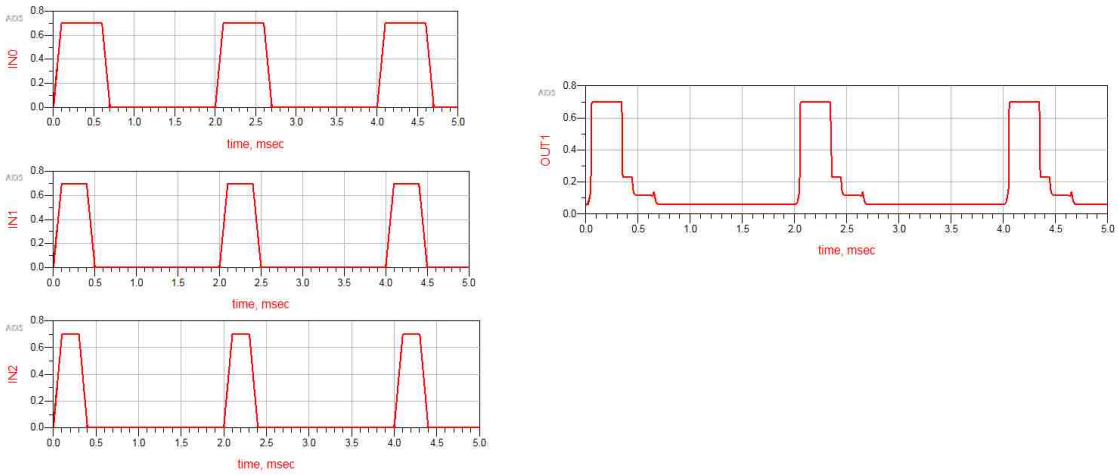


Fig. 4.6. 3-bit ADC Output

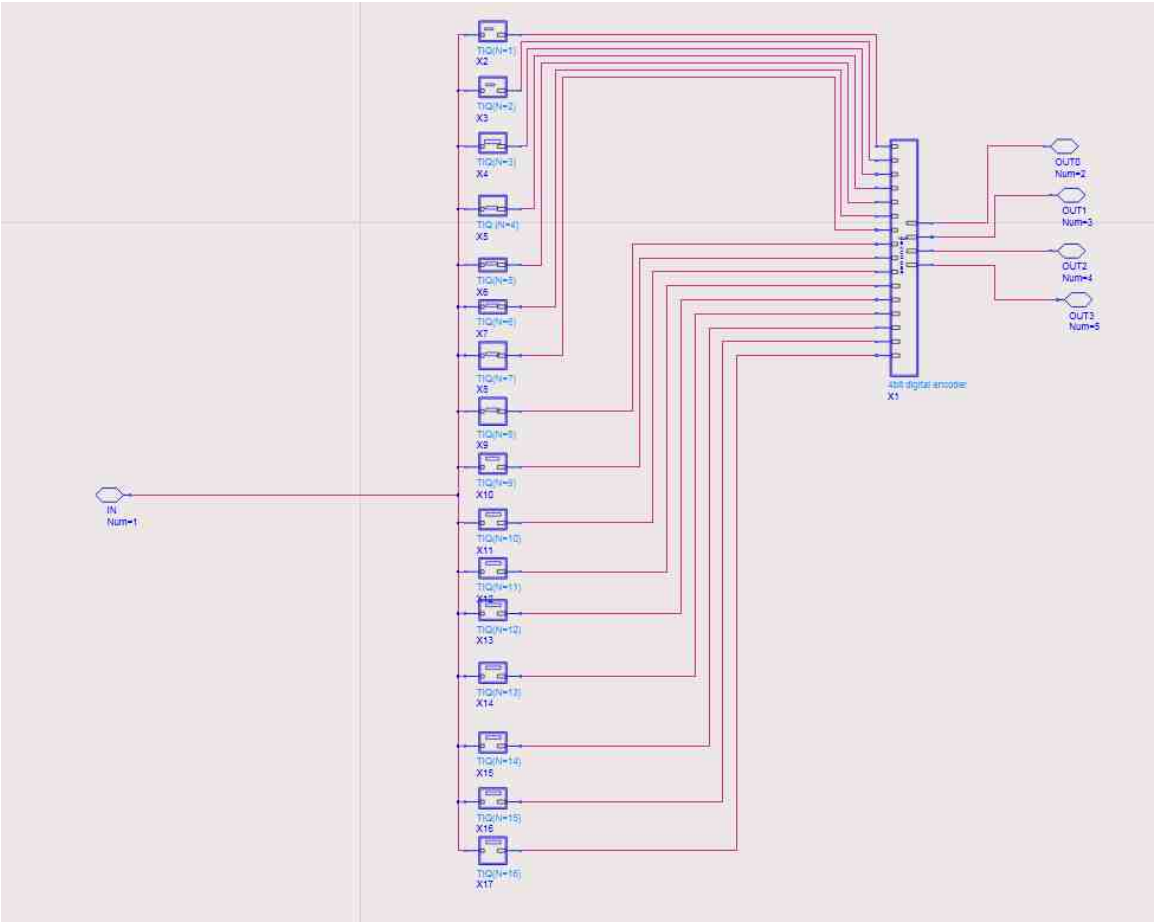


Fig. 4.7. 4-bit ADC Schematic

schematic and transient response of the 4-bit ADC are shown in Figures 4.7 and 4.8 respectively.

4.2 Digital-to-Analog Converters (DAC)

The DAC circuit uses current mirror for dividing the reference current according to W-2W topology, so the current flows through the first two FET transistors in the circuit is Iref/2 which is considered as Most Significant Bit (MSB). Similarly, the current flowing through the last two FET devices will be Iref/2^n which is considered

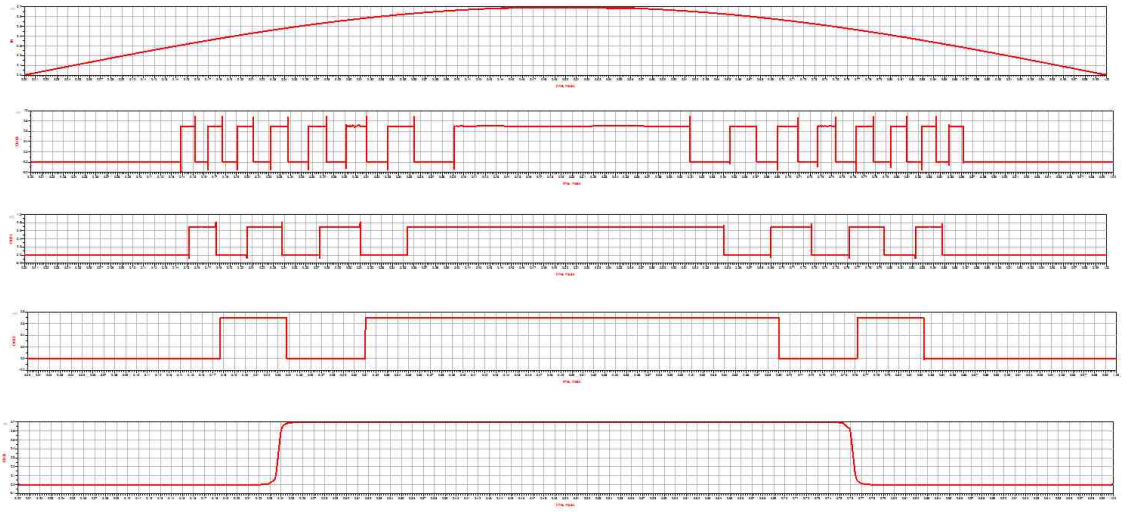


Fig. 4.8. 4-bit ADC Output

as Least Significant Bit (LSB). For Implementing DACs, we used 5 μA reference current (Iref). The input supply voltage is taken 0.7 V. Capacitors are taken in the fF range.

W-2W Current Mirror topology is a contemporary technique for implementing DACs [20]. When two FET devices of W/L topology are connected source to source and drain to drain then the equivalent FET topology is (2W/L). If two devices are connected; drain of one FET device with W/L topology is connected with source of other FET device with W/L topology. The equivalent FET topology is then equal to (W/2L). There will be a smaller number of FET devices which means less layout area, and this is the main feature of this topology. The area of the FET DAC [21] using this topology is given by:

$$A_i = 1/\eta * \Sigma\ W_i\ L_i$$

Where η is the layout fill factor with $\eta < 1$

Figure 4.9 shows the W-2W topology. Figures 4.10 and 4.11 show the schematics and transient response of the 2-bit DAC respectively. Figures 4.12 and 4.13 show the schematics and transient response of the 3-bit DAC respectively. Figures 4.14 and 4.15 show the schematics and transient response of the 4-bit DAC respectively.

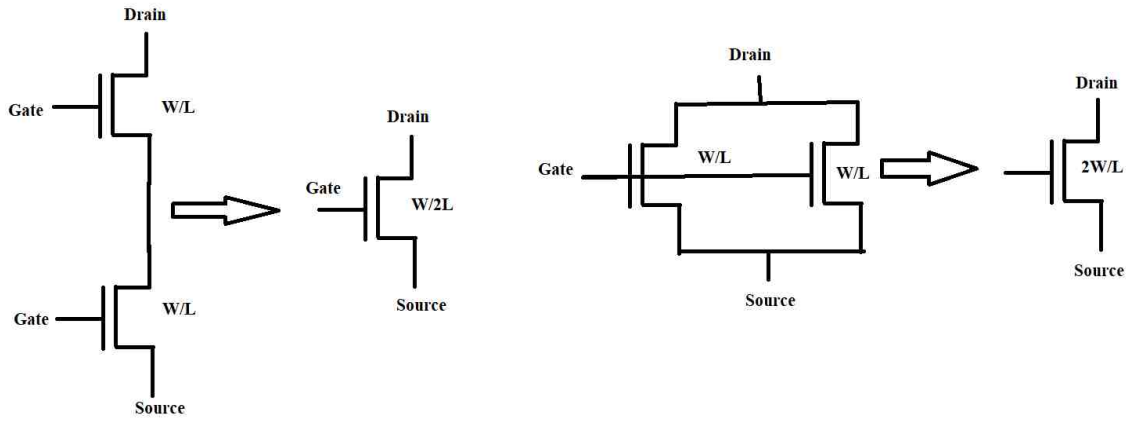


Fig. 4.9. W-2W Topology

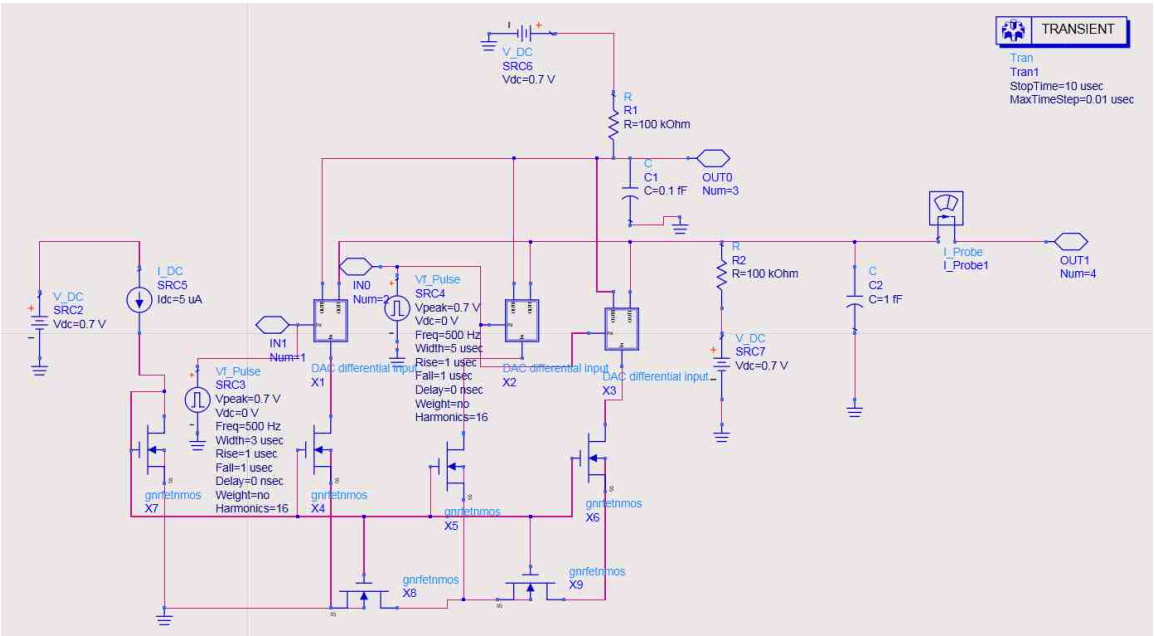


Fig. 4.10. 2-bit DAC Schematic

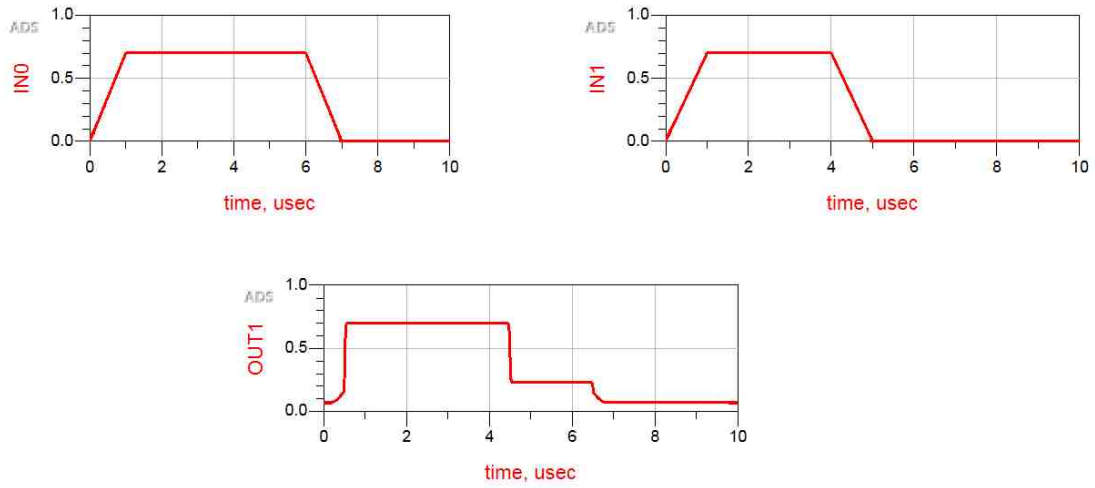


Fig. 4.11. 2-bit DAC Output

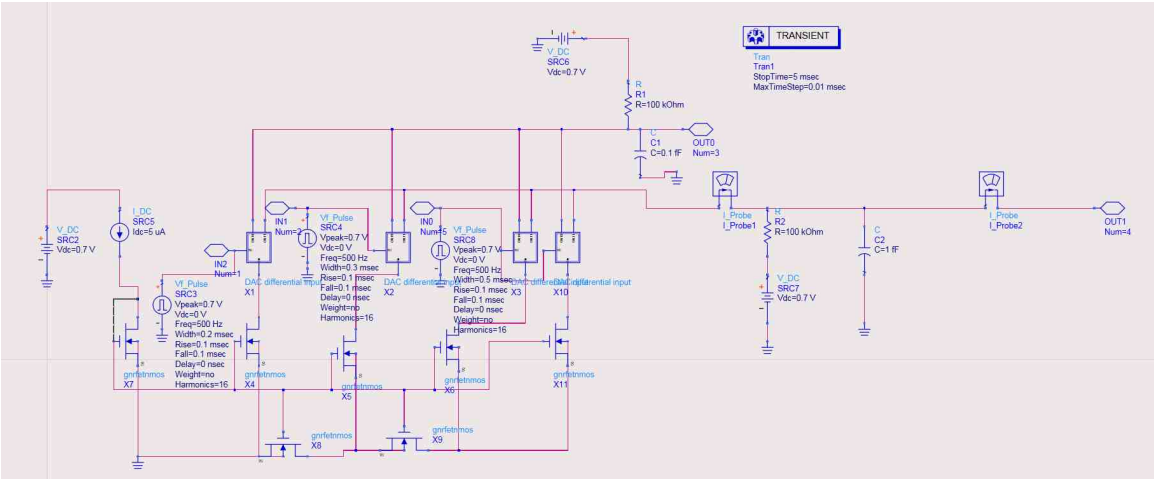


Fig. 4.12. 3-bit DAC Schematic

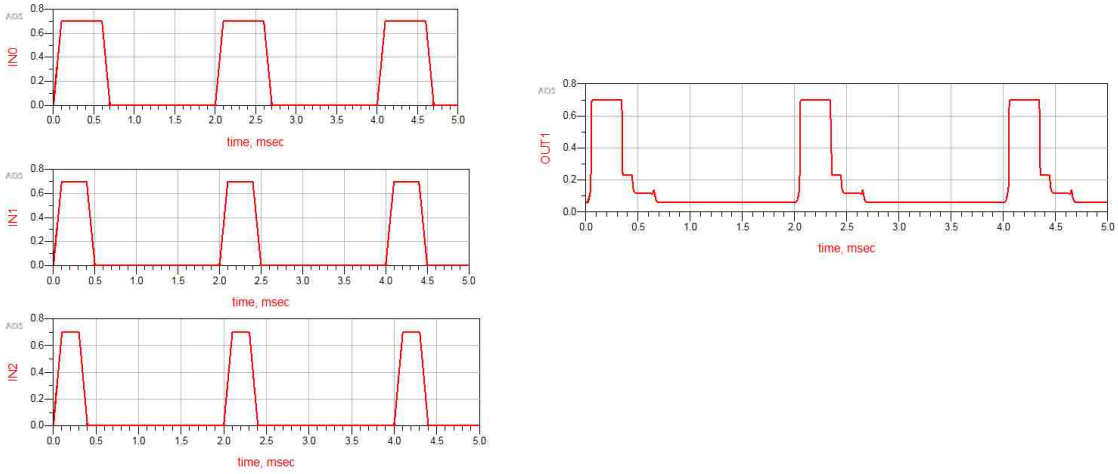


Fig. 4.13. 3-bit DAC Output

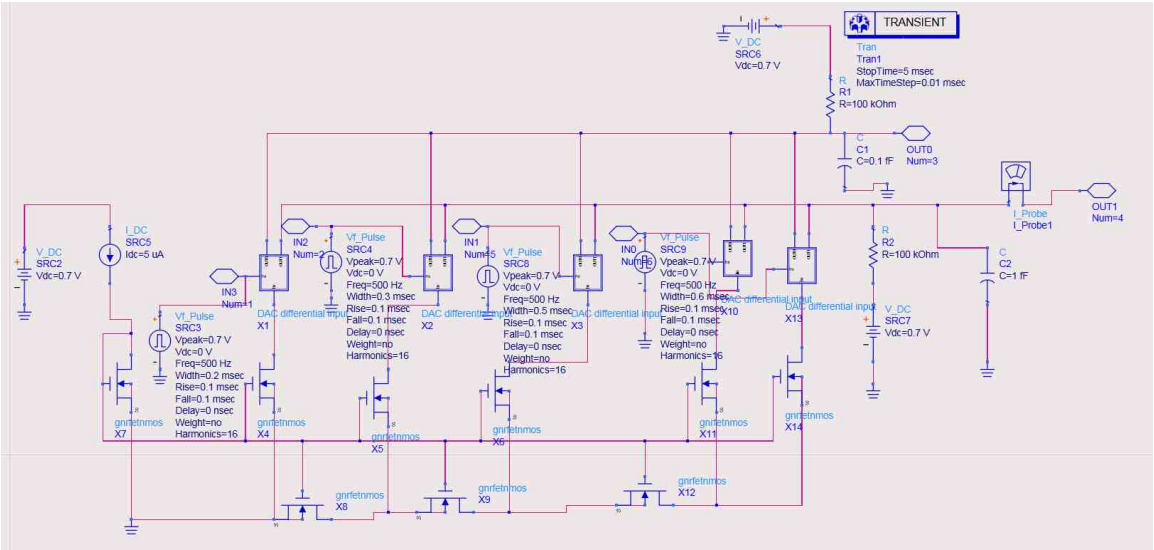


Fig. 4.14. 4-bit DAC Schematic

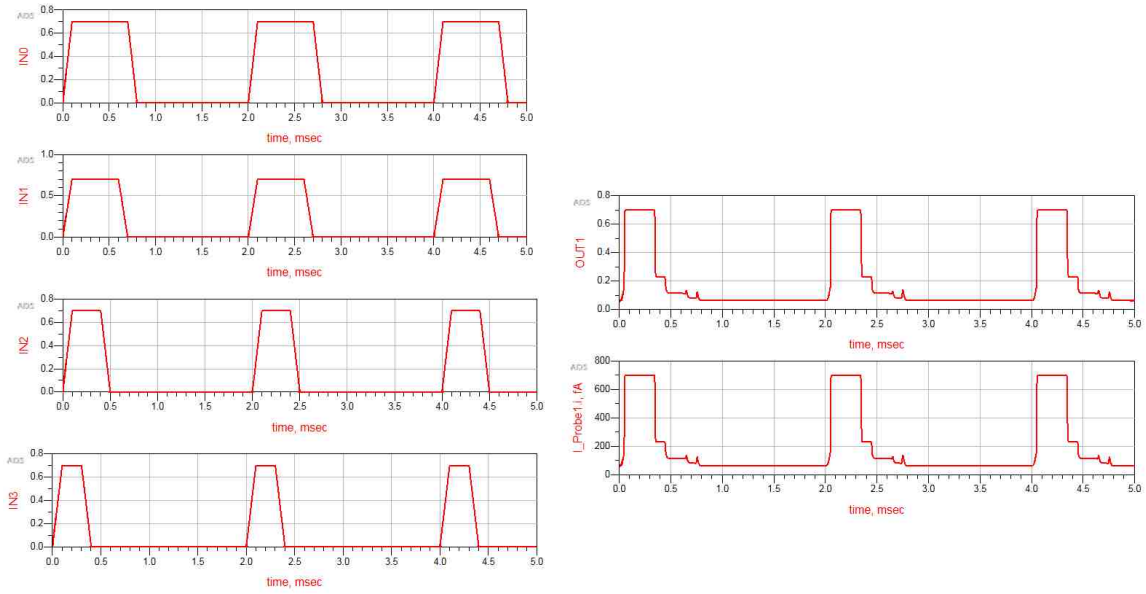


Fig. 4.15. 4-bit DAC Output

5. RESULTS AND DISCUSSIONS

In this chapter, the characteristics of devices implemented in this study were discussed. Table 5.1 gives the power consumption of digital circuits implemented in this study. Table 5.2 gives power gain, noise figure, stability factor of power amplifiers at 2GHz designed and implemented in this study. The power consumption of 4-bit ADC is found to be 24.5 μW with 40nsec rise time. Table 5.3 represents the characteristics of the Digital-to-Analog Converters.

It also presents a comparative data between the most advanced devices in silicon technology and the data obtained in this study. Table 5.4 presents available data for the FinFET device characteristics. Even though, very limited information available for the FinFET devices, what presented here reflects the features and drawbacks of both.

Table 5.1.
Power Consumption of all Digital Components

Digital Component	Static Power	Dynamic Power
NOT Gate	0.6pW	0.12pW
NAND Gate	0.9pW	0.09pW
NOR Gate	1.2pW	0.09pW
XOR Gate	4.9pW	122nW
XNOR Gate	2.1pW	122nW
Half Adder	85nW	214nW
Full Adder	126nW	490nW
Ripple Carry Adder	151nW	1.8μW
Carry Look Ahead Adder	286nW	0.3μW
Half Subtractor	28.1nW	214nW
Full Subtractor	57.3nW	490nW
2X2 Multiplier	51.5nW	122nW
3X3 Multiplier	173nW	30.6 μW
2:1 MUX	11.8nW	-
4:1 MUX	28.7nW	-
1:4 Demux	15.7nW	-
1-bit Comparator	62.3nW	306nW
2-bit Comparator	89.7nW	490nW
4X2 Encoder	40nW	490nW
8X3 Encoder	72.8 nW	735nW
Serializer	400nW	-

Table 5.2.
Characteristics of the Power Amplifiers

Power Amplifier	Power Gain	Noise Figure	Stability
Class A	3.478dB	0.064dB	10.171
Class B	0.870dB	0.318dB	1.005
Class AB	0.126dB	0.397dB	1.012

Table 5.3.
Characteristics of the DACs

DAC Device	Power Consumption	SNDR	INL	DNL
2-bit	4.431μW	13.8	0.625LSB	0.88LSB
3-bit	4.48μW	19.8	0.3125LSB	0.63LSB
4-bit	4.51μW	25.8	0.156LSB	0.39LSB

Table 5.4.
Comparison of FinFET and GNRFET

Characteristics	FinFET	GNRFET
Input Supply Voltage	0.7 V	0.7 v
Electron Mobility	575 cm^2/(V.s)	1500cm^2/(V.s)
Leakage Current	4157pA	1771pA
Ion/Ioff	17500 A/A	40000 A/A
Leakage Power	2910pW	1240pW
Delay	2.82ps	2.79ps

6. CONCLUSION AND FUTURE WORK

In this study, the GNRFET device model developed at the University of Illinois, Champaign has been verified for various applications including digital, analog and mixed signals. With minor modifications to the device parameters, reflecting the channel specifications used in the model, device performance proved to be stable in its operation for various components. The employment of the GNRFET devices in these components has resulted in unique characteristics including low power consumption and high switching speed. The GNRFET devices considered in the design was of 10nm channel length, suggesting successful applications for the ULSI (ultra large scale integrated circuits) that are suitable for future computer architectures including GPUs and CPUs. The data received in this study is superior over the silicon technology as compared to the most advanced FinFET devices, in its power consumption and switching speed. The 10nm nano scale channel length considered in this work may result in comparable level of integration with FinFET technology. Lack of available data on the 7nm scale FinFET makes it hard to draw a fair conclusion on other issues related to the manufacturing processes, packaging etc. Furthermore, since GNRFET devices are still in prototyping stage makes it challenging to draw a conclusion at the system level for fair comparison, and this is reserved for future considerations. The designed serializer gave output with minimum data loss. The building blocks of the serializer used were also designed at high efficiency.

The study shows successful designs for the three power amplifier classes A, B, and AB with proper characteristics, including very low power consumption, low noise figures, high stability factors, and minimum harmonics. The designed amplifiers were including passive components, so further study can extend to power amplifier design with active components. Various attempts were made for the active loads, however some issues were still remaining with output performance. A phase shift and a dc

output component were observed, and the relation between Vout and Vd was not found accurate. This may be attributed to the capacitive components associated with the device model, leading to the output phase shift. The circuit seems to have some mismatching operating conditions, resulting in a dc output. Future efforts should emphasize different designs for proper differential to single output conversion. Device sizing may also be an issue for adjusting the stage gain. These efforts were also reserved for future considerations. GNRFET ADCs and DACs designed and simulated in this study have less rise time and low power consumption as compared to current technology.

Future work may continue to address issues related to RF applications with interfacing to IoT and embedded devices that makes it suitable for high speed 5G communications, computer architectures, and medical technology. Applying GNRFET to PLL (phase Locked Loops), an important unit in communications and computers may be considered for future implementation. This includes phase detectors and voltage controlled oscillators. Issues of impedance matching when interfacing these devices with FinFET technology may be of great interest to integrate features of both technology.

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