PURDUE UNIVERSITY
GRADUATE SCHOOL
Thesis/Dissertation Acceptance

This is to certify that the thesis/dissertation prepared

By Kaiyang Liu

Entitled

A Selective Polarity DC-DC Converter with Virtually Infinite Voltage Levels

For the degree of Master of Science in Electrical and Computer Engineering

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Head of the Departmental Graduate Program Date

A SELECTIVE POLARITY DC-DC CONVERTER WITH VIRTUALLY INFINITE VOLTAGE LEVELS

A Thesis

Submitted to the Faculty

of

Purdue University

by

Kaiyang Liu

In Partial Fulfillment of the

Requirements for the Degree

of

Master of Science in Electrical and Computer Engineering

August 2016

Purdue University

Indianapolis, Indiana

For my parents

ACKNOWLEDGMENTS

This research would not have been possible without the help and guidance of Dr. Afshin Izadian. In spite of having a busy schedule, Dr. Izadian took time to discuss the progress of my work every week. The discussions with Dr. Izadian helped me learn and make progress in my work. It was his continuous support and motivation that I could complete my research. I am also thankful to Dr. Maher Rizkalla, for his constant support throughout the course of my work and Dr. Lingxi Li, for taking time out of his busy schedule to be a part of my advisory committee. I would also like to thank the Departments of Electrical and Computer Engineering and Technology for allowing the collaboration between the two departments for research. I would like to thank Ms. Sherrie Tucker for helping me throughout the Masters program.

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ABSTRACT

Liu, Kaiyang. M.S.E.C.E., Purdue University, August 2016. A Selective Polarity DC-DC Converter With Virtually Infinite Voltage Levels. Major Professor: Afshin Izadian.

This research introduces a new design of a converter modified from SEPIC converter (Single end primary inductive converter), capable of generating desired voltage levels and polarities. The new switching converter topology allows for boost and buck of the input voltage theoretically achieving infinite positive and negative voltage levels. The proposed topology utilizes single high frequency switch to perform the power conversion which simplifies the design of the gate driver, but meanwhile, it still retains the ability to provide a wide range of output voltage. Mathematical modeling of the converter and computer simulations are validated by experimental data. To verify its performance a prototype was designed and built. It is experimentally proven that the circuit can generate a desired voltage in the range of voltages up to 170 V, delivering 480 Watts of power to a resistive load.

1. INTRODUCTION

1.1 DC-DC Converters

DC-DC converter is usually form a very important part in many different industrial applications [1–7]. As an example, it is highly utilized in Fuel Cell Vehicle, because it smoothly and fast controls the output power of the Fuel Cell. As the basic function, DC-DC converter has its advantage of high reliability, high efficiency, high stability, and high power density [8]. These characteristics satisfy the requirement for most of the industrial applications. Therefore, a DC-DC converter with the ability to step up and step down the input voltage and have met the basic characteristics have important practical industrial utilization.

The basic topologies of the DC-DC converter can be classified in two different types: isolated converter and non-isolated converter [9]. While comparing with these two different types of DC-DC converter, it can be observed that the isolated DC-DC converter does not able to achieve the same level of high efficiency as the non-isolated one. As the reason, the isolated DC-DC converter performs the voltage conversion through using a transformer, which is considered to have too much power consumption [8]. Therefore, with higher efficiency, non-isolated DC-DC converter is often used in industrial applications. The latter also contains single-switch topologies, which includes two-switch cascade converter, Cuk converter, boost-buck converter, single-ended-primary-inductance converter (SEPIC), and some other novel converters with coupled inductors [10–12]. Cuk converter, boost-buck converter, and single-ended-primary-inductance converter (SEPIC) are three main types of converters. The conventional buck-boost converters and Cuk converters are called inverting converters, because in their basic form, the polarity of the output voltage can be reversed from the input voltage. As a noninverting buck-boost converter, SEPIC converter has been

attracting much attention since the polarity of their output voltage stay stable and the components bear lower stress. Due to the absence of direct energy transfer path, the voltage and current stress of the single-switch converter are usually high.

Nowadays, many of those industrial applications, such as photovoltaic [13], [14], fuel cell energy system [15], [16], high-intensity discharge lamp (HID), DC back-up energy systems, and electric vehicle, required high voltage gain DC-DC converters. Especially for photovoltaic energy conversion system and fuel cell systems, in order to connect to the grid-connected inverter, they usually need high step up and large input current DC-DC converter to boost the low voltage (18V-56V) to a high voltage (200V-400V). As another example, high-intensity discharge lamp (HID) demands for high voltage gain DC-DC converters to raise a 12V battery voltage to a steady operated 100V output voltage while it is applied for automobile headlamps [17], [18]. Conventional DC-DC boost converter is not suitable for high voltage gain application because of high voltage stress and high duty cycle. Theoretically, a basic boost converter can achieve infinite voltage gain if the duty cycle is able to set to an extremely high percentage. However, in practice, the parasitic elements of inductors, capacitors, and power transistors will limit the peak value of the voltage gain that the boost converter can step up to. On the other hand, a serious reverse-recovery problem of the rectifier diode may be induced the extremely high duty cycle operation, and also cause large current ripples [19].

To achieve high voltage gain without using an extremely high duty cycle, several different types of topologies can be selected from, including cascaded boost converter [20], coupled inductor [21] and transformer topologies [22]. As mentioned before, transformer may consume much energy, which leads to a lower efficiency comparing with the other solutions. Cascaded designs required more number of switches and gate driver circuits, so these converters requires large space on board and complicate switching map [23]. The multilevel boost design also usually has disadvantage such as high current stress of the switches, complexity (these converters contain large number of parts), bad performance in case of wide load variation. Coupled inductors

is another technique used in the high step up converters. For example, a high step-up parallel boost converter with coupled inductors is introduced in [24]. In these type of converters, due to the input current ripple, there is a limitation on the duty cycle of the switch and number of parallel phase.

Single-ended-primary-inductance converter (SEPIC) is a good choice for many of the industrial application that required high voltage gain such as photovoltaic. The advantage of using SEPIC can be concluded as the following 4 points [25]: 1. It is a noninverting buck-boost converter. Output voltage will stay with the same polarity, 2. Input current is continuous, 3. Has the capability to work in both step-up and step-down modes. 4. Low amount of EMI because of the low input current ripple [26], [27]. Increasing the output voltage can be performed by increase the duty cycle of the main switch.

1.2 DC Microgrid

The rise of the concern of the fossil oil depletion and environmental issues has lead the energy demand as well as concern towards renewable and green energy increasing dramatically. The focus of researches and industrial production has gradually shifted into this direction. Most of renewable energy units generate DC output voltage, and required power electronic devices like high voltage gain DC-DC converter to adapt their output to network conditions [28]. On the other hand, the consumer equipment such as computers, TV, LED lighting, electronic gadgets, BLDC fan etc., need the DC power of various voltages and polarities to operate normally [29]. However, the performance of all those DC loads need conversion of the available AC power into DC power, and most of the conversion stages are completed using traditional low-efficient rectifiers. Therefore, power flows from the source to the load need to go through several DC-AC-DC power conversion stages, which result in substantial energy losses. For this reason, in many cases, using DC microgrids to transmit power seems more justified since it avoided all these conversions. Comparing with the AC microgrid,

the advantage of the DC microgrid can be summarized as follows [30–34]: 1) More efficient power transmission, 2) Few wires are required in a bipolar system than a three phase system, 3) Better stability of system operation, 4) No reactance in line, 5) DC system does not require frequency monitoring , 6) Limited transient and its stability issues, 7) No electromagnetic interference, 8) Lower line resistance.

Distributed generation system (DG) is a system that mostly uses renewable energy sources of power and appears as a viable alternative to reduce transmission losses, increase reliability, and reduce the need for large power plants [35]. In the DG systems, DC microgrid can be used for optimal control of power flow from the sources to loads [36], [37]. A high quality power will be supplied to consumers through the DC microgrid. The power transmission in DC microgrid can be performed with single wire, two wire, and even three wire, which can divide DC microgrid into three different DC-link types: Monopolar, Bipolar, and Homopolar. Within all three types of DC-link types, Bipolar is commonly implemented for residential and industrial distributions. Bipolar DC microgrid contains three wires. One with positive polarity, one with negative polarity and one that connects to the ground [38]. Comparing with a unipolar system, bipolar transmission lines have the following advantages [28]: higher reliability, because if one line fails the power transmission can still be performed for half of the loads; increased energy transmission capacity; reduced current levels with about half the current drawn in unipolar transmission line; lower power losses.

1.3 About This Thesis

This paper presents a new SEPIC-base DC-DC converter that utilizes one high frequency transistor to generate selective polarity voltages. The voltage levels generated through this converter can reach infinite levels. This depends on the resolution of the pulse width in PWM control structure. In conventional power converters [39–43], a voltage step up or step down may require additional power circuit and control algorithms. Yet these converters achieve digital 2, 3, 5 or 7 voltage levels. Compared with

traditional two-stage amplifiers and conventional DC-DC power converters, the new single-stage switching converter is able to boost and buck the supply voltage, change the polarity of the load voltage, and generate virtually infinite voltage level for the output voltage only through changing the direction of the diode and duty cycle of the transistor without using any additional power circuit or control algorithm. It not only reduce the size and cost, but also decrease the efficiency.

One other topology that is always used to generate either positive or negative output voltages is controlled AC-DC rectifier. By modifying the firing angle of the rectifier control unit, not only the output voltage polarity can be selected, the level of output voltage can also be adjusted. This effect has a good use in a DC motor driver which can expand its operating regions to 4 quadrants. On the other hand, another converter that has the ability to step up and step down voltage in both polarities is a 5-switch bipolar buck-boost converter [44]. Comparing with the controlled AC-DC rectifier and 5-switch topology with the converter proposed in this paper, the proposed converter has the lower amount of switches, which means it demands simpler control method, and consuming lower energy. With only one switch to control, the liberty of needing synchronized operation of several switches and utilization of multiple parallel structure converters.

A comprehensive introduction of the new SEPIC-base DC-DC converter is given in the following eight chapters. In chapter II, the configuration of the circuit is introduced, the circuit diagram and an introduction of the circuit are given. Chapter III explains how the proposed converter operates. Four basic operating modes are briefly described. Chapter IV specifically analyses converter behavior under these four different operating modes and details the principles of the operations. Formulas and state-space mathematical models of each mode are also demonstrated in this chapter. Chapter V presents the sizing process for the elements in the converter in order to generate the desired output. The small signal analysis is finished in chapter VI, and the transfer function is obtained as result and tested in MATLAB to prove the transfer function is actually corresponding to the system. In chapter VII, the stability

of the proposed converter in both positive peak and negative peak has been analyzed, and the results of the experiment validation for both simulation model and practical experimental prototype are presented in chapter VIII. Besides, details of the prototype setup, chart of tested duty cycle with matched output voltage, and the analysis of the results are also included in chapter VIII to provide a better understanding of the validation results. In the end of this paper, final conclusions are drawn in chapter IX to summarize the properties and re-emphasized the superiority, originality, and the importance of the proposed converter.

2. SELECTIVE POLARITY DC-DC CONVERTER

2.1 Circuit Configuration

The SPEIC based converter that is introduced in this section is shown in Figure 2.1. It is designed based on a conventional SEPIC converter and has some components modified in order to achieve the feature of polarity changing. This new converter allows the load current to conduct in both directions (selective), hence creating positive and negative load voltage (on-demand). The boost converter in the first stage of the SEPIC converter has the ability to adjust the voltage level through changing the duty cycle of the power switch, and the relay that connected with diodes D_1 and D_2 has the ability to determine the direction of the load current flow.

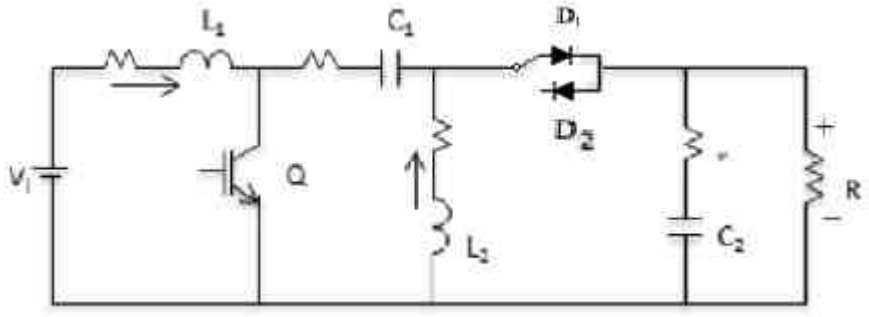

Fig. 2.1. New selective polarity DC-DC converter

The unique feature of this new converter, comparing with classical SEPIC converter, is the replacement of the diode by a new set of devices that two diodes D_1 and D_2 connect to the two branches of a selector switch in opposite directions, which allows either of the diodes to be conducted into the circuit and control the direction of the load current. As the main switch to adjust the voltage level of the output, a

MOSFET is utilized here to provide high frequency switching. The MOSFET and the selector switch are both controlled by a microcontroller Arduino Due.

In order to generate the output voltage with requested polarity, the position of the switch is selected on demand. In order to improve the response time and reduce the passive component size, this converter is required to operate at a fixed switching frequency. The carrier frequency is set to 8 kHz for both positive and negative output voltages. This frequency was experimentally validated to be able to maximize the power conversion and voltage amplitudes. As the frequency is set to a fixed value, duty cycle becomes the only control command to influence the converters performance.

Since the converter can perform voltage change in both polarities, a negative sign is required in front of the duty cycle while presenting the duty cycle for the situation that the converter is operating for generating the negative voltage. When the selector is set to D_1, the forward-direction-diode is connected in the circuit. The current pass through the diode D1 and conduct forward direction to the load. In this case, the duty cycle is positive. With the main switch Q and diode D_1 turn ON and OFF alternatively, a positive voltage will be generated at the load.

For generating negative voltage, a similar process is required where the main switch is switching at 8 kHz and the selector switch is set to diode D_2, a negative (sign) duty cycle is utilized to control the conversion. By turning the main switch Q and diode D_2 ON and OFF alternatively, a negative voltage will be generated at the load.

2.2 Modes of Operation

The proposed converter has two operation modes: positive mode and negative mode. The state space averaging technique is applied here to analyze the behavior of the converter in each mode. By using this technique, the state space representation of each mode of operation is obtained and the overall system governing equations are

presented as an averaged system over a cycle. Since the converter can operate in both positive and negative modes, the analysis for these modes will be provided separately.

A. Positive Voltage Mode

While in positive mode, the converter is operated as shown in Figure 2.2 and 2.3. The selector switch change to position D_1 and connect the forward-direction-diode D_1 into the circuit which allow the forward-direction current to generate positive voltage at the load. In this situation, the main switch Q and D_1 are synchronized. While the main switch Q is ON, inductor L_1 draw energy directly from the source and causes a linear increase of current to charge the inductor. Inductor L_2 draws energy from capacitor C_1. The charged output capacitor C_2 discharges through the inductor L_2 and provides the load current. While Q is OFF, capacitor C_1 is charged by the source, and sum of the current that go through L_1 and L_2 form the load current and generate positive voltage at load.

B. Negative Voltage Mode

While in negative mode, the converter is operated as shown in Figure 2.4 and 2.5. The selector switch connects diode D_2 into the circuit. The main switch Q and D_2 are synchronized and the same procedure as in positive peak voltage is followed. Load current direction will be reversed and this will introduce a transition mode to the system operation. With the main switch Q and diode D_2 turn ON and OFF alternatively, this mode continuously operates and generates negative voltage at load. Operations are presented as follow:

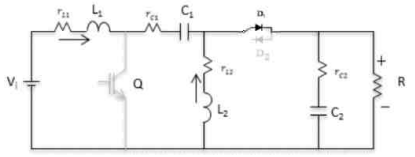

Fig. 2.2. Positive mode I, Q and D1 are synchronized, Q: OFF, D2: ON.

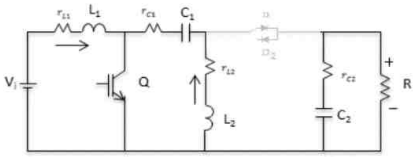

Fig. 2.3. Positive mode II, Q and D_1 are synchronized, Q: ON, D_1: OFF.

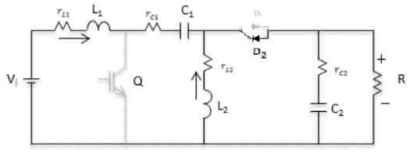

Fig. 2.4. Negative mode I, Q and D_1 are synchronized, Q: Off, D_2: ON.

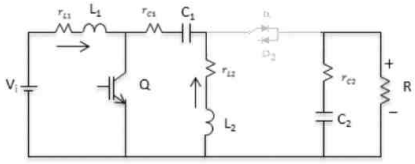

Fig. 2.5. Negative mode II, Q and D_1 are synchronized, Q: ON, D_2: OFF.

The status of the voltage and current of components in the converter are also shown in figure 3A and 3B separately for different polarities.

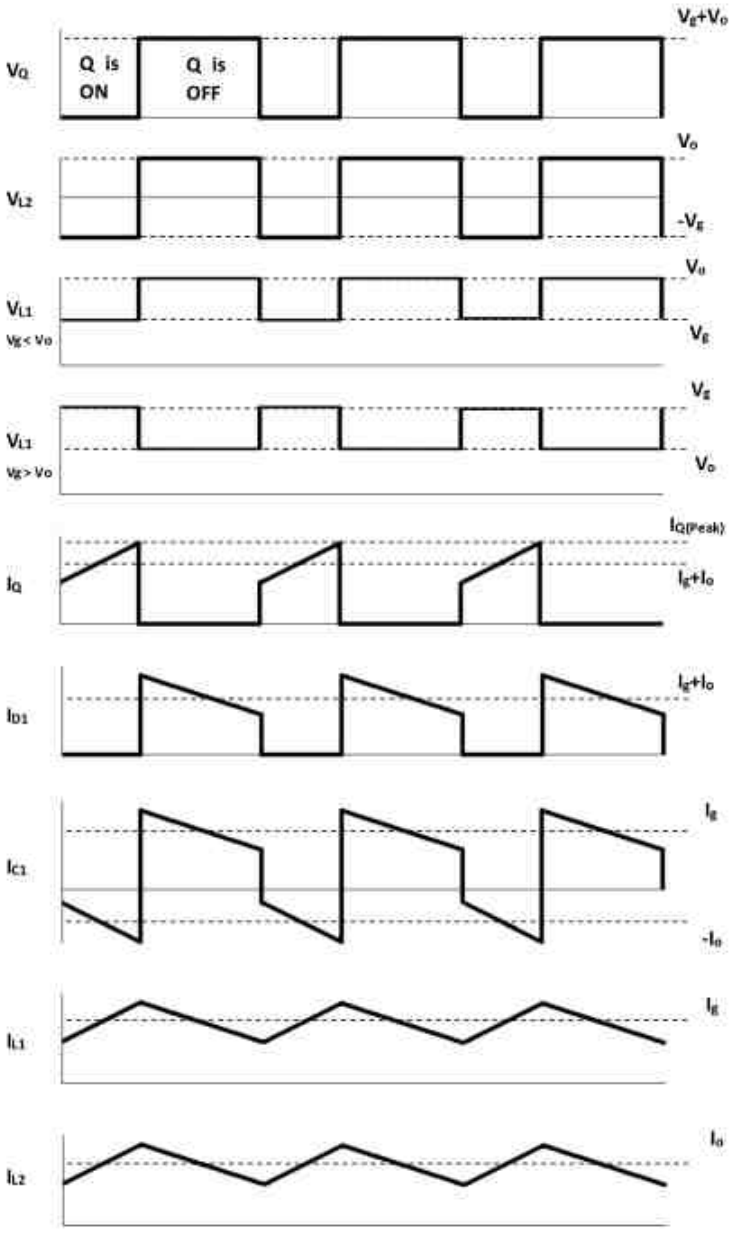

Fig. 2.6. Voltages and currents of the components in the converter under the positive mode

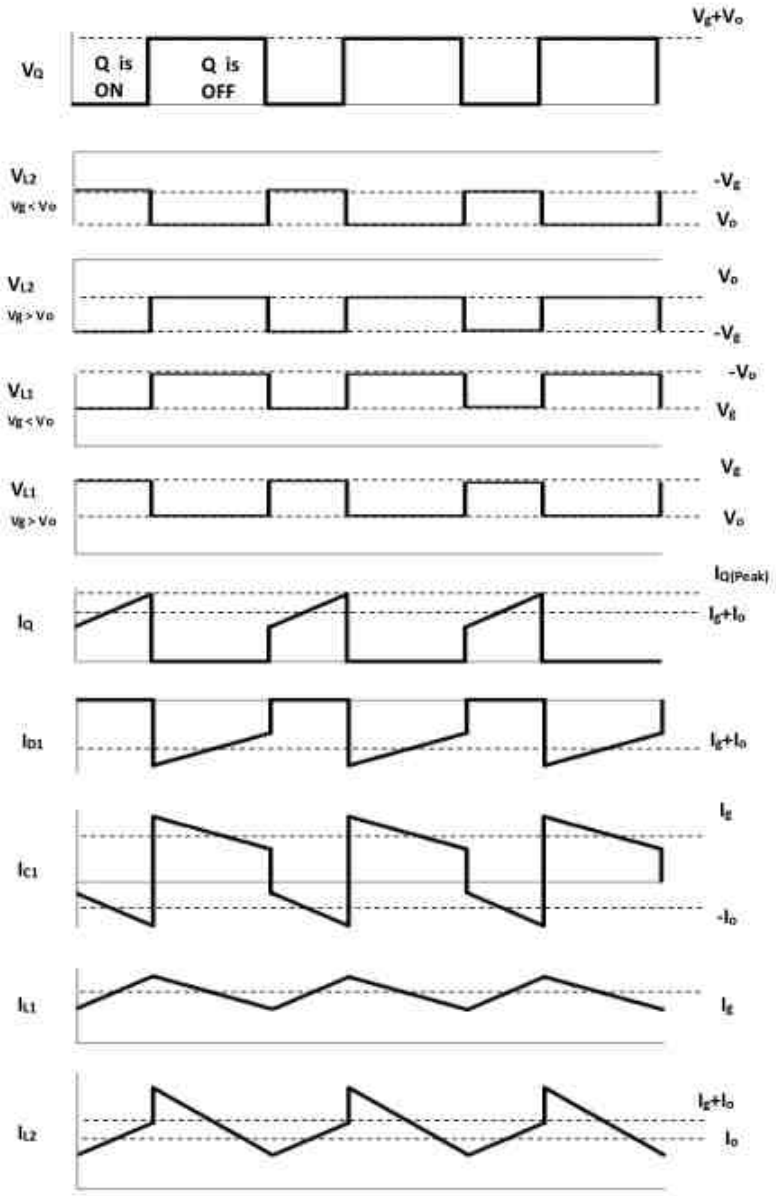

Fig. 2.7. Voltages and currents of the components in the converter under the positive mode

2.3 Sizing

As one of the most critical process in the procedure of designing a converter, sizing the inductors and capacitors in the converter gives a reference of the size range that can guarantee the converter is able to operate normally. Appropriately sizing the components in the converter can reduce the voltage and current ripples, increase the efficiency of the power transformation, and ensure that the system is operating safely. Since the new designed DC-DC converter has the ability to operate in both positive mode and negative mode, therefore, the sizing procedure is doing separately in each mode in order to evaluate the size comprehensively.

The proposed DC-DC converter is designed to generate a DC voltage output with the range equals to 0-170V with virtually infinite voltage level by using a 30V DC source. The maximum input current is 20A. Assume the efficiency of the converter is 90%, the maximum output current can be calculated and equals 3.2A. A MOSFET is utilized in this converter performing as the switching device. The MOSFET is switching at 8.3 kHz. The sizing will be analyzed separately in two parts for different polarities, and in each part, the size of six components, including duty cycle, inductor, MOSFET, diode, capacitor C_1, and output capacitor C_2, will be analyzed and showed.

A. Positive Mode

1. Duty Cycle

While the diode is conducting in the forward direction, the converter is working in the position mode. The converter work as a normal SEPIC converter in this mode and generate positive output voltage on the load. Assume that the converter is operating in an ideal situation, the relationship between the input and output voltage can be expressed by the duty cycle of the main switch, D, as follow:

$$\frac{V_o + V_{FWD}}{V_g} = \frac{D}{1-D} = \frac{I_g}{I_o} \tag{1}$$

V_{FWD} denotes the forward voltage drop of the diode D_1. Since the converter is assumed to be ideal, the efficiency of the power transmission is assumed to be 100%. The power generates at the load is equal to the power drain from the source. Therefore, the input and output current can also expressed by the duty cycle D. Through using this formula, the equation can be rewritten as follow in order to calculate the duty cycle D for corresponding output voltage:

$$D = \frac{V_o + V_{FWD}}{V_g + V_o + V_{FWD}} = \frac{170 + 4.4}{30 + 170 + 4.4} = 85.3\% \tag{2}$$

By solving the equation above, the value of D for generating a 170V output voltage can be calculated as 85.3%.

2. Inductor

To start designing a PWM switching regulator, one of the very first step is to make decision of how much ripple current is allowed for the inductor. The allowed ripple current is denoted as I_L . If the inductor ripple current is too large, the EMI is increased, on the other hand, if I_L is too small, it will cause unstable of the PWM operation. The best way to size the inductor ripple current I_L is to follow the rule of thumb and make it 20% to 40% of the input current. So that, the inductor ripple current can be calculated as follow:

$$\Delta I_L = \frac{30\% \times I_g}{\eta} = 30\% \times \frac{18.43}{90\%} = 6.14A \tag{3}$$

Where η represents the estimated worst-case efficiency. η was estimated at the minimum of the input voltage which was fixed at 30V and maximum of the output current which could be obtain through using Eqn. (4). Since the converter was assumed operating with 90% efficiency, 10% of power was lost in the transfer process, thus the maximum output power was equal to 90% of the maximum of the input power, which was 540W.

The input current was calculated as 18.43A, which was less than the maximum input current, so it was within the range for input current. Thus the input current I_g is equal to 18.43A.

$$I_g = \frac{D}{1-D} I_o = \frac{0.853}{1-0.853} = \frac{540}{170} = 18.43A \tag{4}$$

The inductor L_1 is drawing energy from the source when the main switch Q is turned on, and meanwhile inductor L_2 is charged by the capacitor C_1. Both of the inductors are charging in this mode. However, if the switch Q is turned off, both of the inductors L_1 and L_2 release energy to the load. The equation below represents the size of the inductors L_1 and L_2, which are generated from the continuous current analysis of the inductors. The worst case is considered for both inductor in order to obtain the equations. Design the converter using the inductors in the range of these sizes guarantees the continuous conduction.

$$L_1 = L_2 \geq \frac{DV_g}{2\Delta I_L f_{sw}} = \frac{0.853 \times 30}{2 \times 6.14 \times 8300} = 251.07\mu H \tag{5}$$

The peak current for the inductors can be defined as showed in the following:

$$I_{L1_{Peak}} = \frac{I_g}{\eta} \times (1 + \frac{30\%}{2}) = \frac{18.43}{90\%} \times 1.15 = 23.55A \tag{6}$$

$$I_{L2_{Peak}} = I_o + \frac{\Delta I_L}{2} = \frac{540}{170} + \frac{6.14}{2} = 6.25A \tag{7}$$

3. MOSFET

As the main switch of the converter, the MOSFET Q need to be carefully sized in order to make sure that the selected MOSFET has the ability to bear the peak voltage and allow the peak current to flow without breaking down. At the same time, a well selected MOSFET could also minimize the power-dissipation losses. On the other hand, the current rating or the current limit of the MOSFET is an important factor in determine the maximum output current of the SEPIC converter.

According to Section 2.2 Modes of Operation, the maximum voltage across the MOSFET is the sum of input and output voltage $V_g + V_o$. And as for the current rating of the MOSFET, the peak current rating can be expressed in equation 8 as showed below:

$$I_{Q_{Peak}} = I_{L1_{Peak}} + I_{L2_{Peak}} = I_o + \frac{I_g}{\eta} + I_L \tag{8}$$

$$I_{Q_{Peak}} = 23.55 + 6.25 = 3.18 + 20.48 + 6.14 = 29.8A \tag{9}$$

Besides the peak current rating of the MOSFET, the RMS current that would flow through the MOSFET is another consideration in sizing, the RMS current is given in equation (10):

$$I_{Q_{RMS}} = I_o \sqrt{\frac{(V_g + V_o + V_{FWD}) \times (V_O + V_{FWD})}{V_g^2}}$$

$$= 3.18 \times \sqrt{\frac{(30 + 170 + 4.4) \times (30 + 4.4)}{30^2}} = 19.99A \tag{10}$$

4. Diode

The two critical considerations while sizing for the output diode are the peak current and reverse voltage. When consider the converter in the positive mode, the peak current that the diode should have ability to handle is the same as the peak current for the other active component MOSFET Q.

$$I_{D_{1Peak}} = I_{Q_{Peak}} = 29.8A \tag{11}$$

As for the other factor used for sizing a diode in a SEPIC converter, the reverse voltage of the diode D_1 that is able to withstand is supposed to be greater than the maximum voltage of the MOSFET Q, $V_{Q_{Peak}}$. As the Figure 2.6 showed in the section 2.2, the maximum of $V_{Q_{Peak}}$ can be calculated as the sum of the source voltage, output voltage, and forward diode voltage, hence the reverse voltage of D_1 should be size as:

$$V_{RD_1} \geq V_{Q_{Peak}} = V_g + V_o + V_{FWD} = 30 + 170 + 4.4 = 204.4V \tag{12}$$

Since the diode has the same average current as the output load, the power dissipated on the diode can be calculated as:

$$P_{D_1} = V_{FWD} \times I_o = 4.4 \times \frac{540}{170} = 13.98W \tag{13}$$

5. Capacitor C_1

Since the ripple of the voltage across the capacitor C_1 could be calculated as:

$$\Delta V_{C_1} = \frac{I_o D}{C_1 f_{sw}} \tag{14}$$

The size of the capacitance can be expressed as following:

$$C_1 \geq \frac{I_o D}{\Delta V_{C_1} f_{sw}} \tag{15}$$

The voltage ripple of the capacitor C_1 is the only variable in this equation, so that the capacitance will be sized according to the need for the ripple value. While considering building the prototype, oil-filled capacitors were considered to be used as the capacitors in the converter, thus the value selection for the ripple were basically depends on the voltage rating of the oil-filled capacitors. Mostly, the voltage rating of the capacitors are between 370V and 440V. Therefore, to make sure the capacitor selection is working for the items that satisfied both of the voltage ratings, the voltage ripple is set to 370V in the calculation.

$$C_1 \geq \frac{\frac{540}{170} \times 85.3\%}{370 \times 8300} = 0.88\mu F \tag{16}$$

6. Output Capacitor C_2

While the MOSFET is switched ON, the inductor L_2 is charging, and the load current is totally provided by the output capacitor C_2. In this reason, the output capacitor need to reach a balance between the capacitance and the ESR, which means the capacitance of the selected capacitor has to be large enough to provide to load current in the ON time, but at the same time, it should not generate too much ESR. Figure 2.8 shows how the output voltage ripple is controlled by the ESR, ESL, and the bulk capacitor. The ripple has been broke down in two parts, ESR and capacitance itself, to show how the ripple is form and related to the output current. The RMS

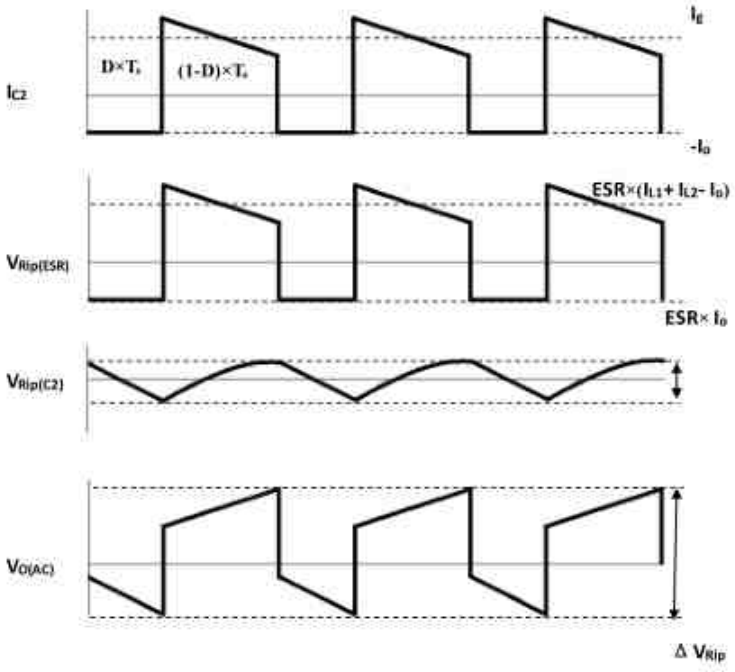

Fig. 2.8. Voltage ripple of output capacitor C_2 in positive mode

current rating for the output capacitor C_2 can be computed using the formula showed in equation (17):

$$I_{C_{out}} = I_o\sqrt{\frac{D}{1-D}} \tag{17}$$

By considering the ripple voltage is form by half of the ESR and half of the ripple caused by the capacitance itself, the ripple should be less than the sum of these two values like what is showed in equation (20).

$$V_{Rip_{ESC}} = \frac{\Delta V_{Rip}}{2(I_{L1_{Peak}} + I_{L2_{Peak}})} \tag{18}$$

$$C_2 \geq \frac{2I_oD}{\Delta V_{Rip} f_{sw}} \tag{19}$$

$$\Delta V_{Rip} \leq \frac{I_oD}{C_2 f_{sw}} + (I_{L1_{Peak}} + I_{L2_{Peak}}) V_{Rip_{ESC}} \tag{20}$$

By modifying the equation 20, the output capacitor can be sized by the following equation:

$$C_2 \geq \frac{I_o \times D}{(\Delta V_{Rip} - (I_{L1_{Peak}} + I_{L2_{Peak}}) \times V_{Rip_{ESC}}) \times f_{sw}} = 1.48\mu F \tag{21}$$

Same as the isolate capacitor, the ripple voltage is chosen between 370V and 440V. In order to fit both of the voltage rating, 370V is used as the ripple voltage to ensure the size of the output capacitor is correct. And, as the result for the output capacitor sizing, the capacitor need to be larger than $1.48\mu F$ to guarantee the converter is working.

B. Negative Mode

1. Duty Cycle

Since the duty cycle for the negative cycle is denoted as negative numbers, according to the analysis and calculation that has been done in section 3.2, the duty cycle for the negative half can be computed as:

$$D_{neg} = \frac{V_o + V_{FWDN}}{V_g - V_o - V_{FWDN}} = \frac{-170 - 4.4}{30 + 170 + 4.4} = -85.3\% \tag{22}$$

2. Inductor

Since the working status of the inductor L_1 and L_2 are different between operating in positive and negative mode, the size of the inductors need to be sized by using

a new method. By observing the operation mode of the inductors showed in figure 3B, the inductor L_2 is operated in a different way than in the positive mode, which means L_2 is not able to be sized along with inductor L_1 anymore. They need to be sized separately.

After the polarity of the output is changed, the current status of the inductor L_1 remains the same. The current of L_1 decreased almost $2I_g$ in $(1-D)T_s$ second. The relationship is showed as below:

$$2I_g = \frac{V_o \times (1-D)T_s}{L_1} = \frac{V_g \times D}{L_1 \times f_{sw}} \tag{23}$$

So that the boundary of the size for inductor L_1 can be calculated by:

$$L_1 \geq \frac{V_g \times D}{2I_g \times f_{sw}} = \frac{30 \times 85.3\%}{2 \times 18.43 \times 8300} = 83.64\mu H \tag{24}$$

As for the inductor L_2, the current status is changed after the polarity is changed. Different than the current of inductor L_1, the current reduces $I_o + I_g$ in $(1-D)T_s$ second. This change can be expressed as equation (24):

$$I_g + I_O = \frac{V_o \times (1-D)T_s}{L_2} = \frac{V_o \times (1-D)}{L_2 \times f_{sw}} \tag{25}$$

So that the boundary of the size for inductor L2 can be calculated by:

$$L_2 \geq \frac{V_o \times (1-D)}{(I_g + I_o) \times f_{sw}} = \frac{170 \times (1-85.3\%)}{18.43 + \frac{540}{170} \times 8300} = 139.33\mu H \tag{26}$$

Combining the size for both positive mode and negative mode, both the inductor L_1 and L_2 should be greater than $251.07\mu H$. The peak current for the inductors can be defined as showed in the following:

$$I_{L1_{Peak}} = \frac{I_g}{\eta} \times (1 + \frac{30\%}{2}) = \frac{18.43}{90\%} \times 1.15 = 23.55A \tag{27}$$

$$I_{L2_{Peak}} = I_o + I_g = \frac{540}{170} + 18.43 = 21.61A \tag{28}$$

3. MOSFET

Since the peak current for the inductor L_2 is changed, the peak current for the MOSFET will change also as showed below:

$$I_{Q_{Peak}} = I_{L1_{Peak}} + I_{L2_{Peak}} = 23.55 + 21.61 = 45.16A \tag{29}$$

4. Diode

The peak current for the reverse direction diode should equal to the peak current for the inductor L_2.

$$I_{D_{2Peak}} = I_{L_{2Peak}} = 21.61A \tag{30}$$

As for the reverse voltage of the diode D_2, the diode D_2 should be able to withstand the voltage greater than the sum of output voltage and forward voltage of the diode:

$$V_{RD_1} \geq -(V_o + V_{FWDN}) = -(-170 - 4.4) = 174.4V \tag{31}$$

And the power dissipated on the diode can be calculated as:

$$P_{D_2} = V_{FWDN} \times I_o = -4.4 \times -\frac{540}{170} = 13.98W \tag{32}$$

5. Capacitor C_1

Since the operation for the isolate capacitorC_1 does not make any difference after the output polarity is changed, the size process on C_1 remain the same as positive mode.

6. Output Capacitor C_2

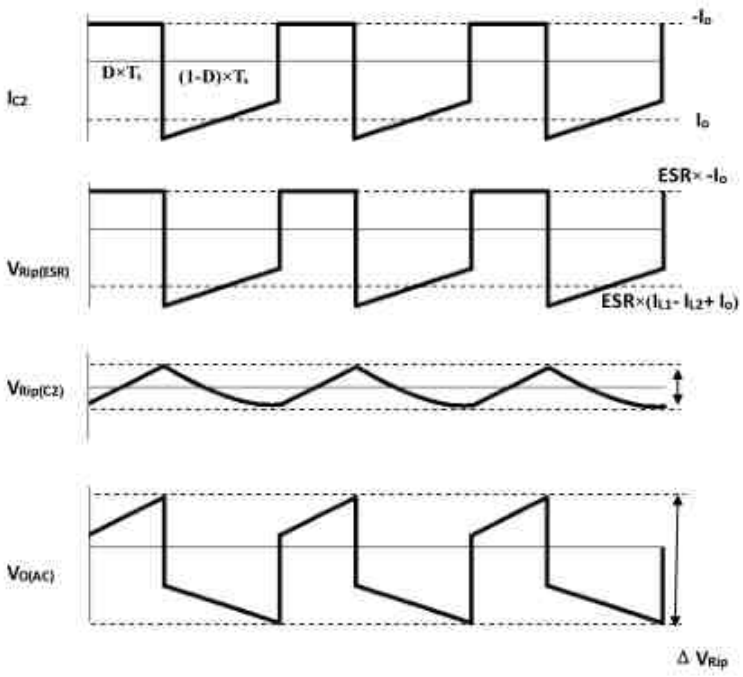

Fig. 2.9. Voltage ripple of output capacitor C_2 in negative mode

Figure 2.9 demonstrate the difference of the voltage ripple of the output capacitor C_2 in the negative mode. By still considering the ripple voltage is form by half of the ESR and half of the ripple caused by the capacitance itself, the ripple of the voltage can be modified and rewritten as showed in equation 20.

$$V_{Rip_{ESC}} = \frac{\Delta V_{Rip}}{2(I_{L2_{Peak}} - I_{L1_{Peak}})} \tag{33}$$

$$C_2 \geq \frac{2I_oD}{\Delta V_{Rip} f_{sw}} \tag{34}$$

$$\Delta V_{Rip} \leq \frac{I_oD}{C_2 f_{sw}} + (I_{L2_{Peak}} - I_{L1_{Peak}})V_{Rip_{ESC}} \tag{35}$$

So that, the output capacitor can be sized by the following equation:

$$C_2 \geq \frac{I_o \times D}{(\Delta V_{Rip} - (I_{L2_{Peak}} - I_{L1_{Peak}}) \times V_{Rip_{ESC}}) \times f_{sw}} = 0.92\mu F \tag{36}$$

2.4 Simulink Model

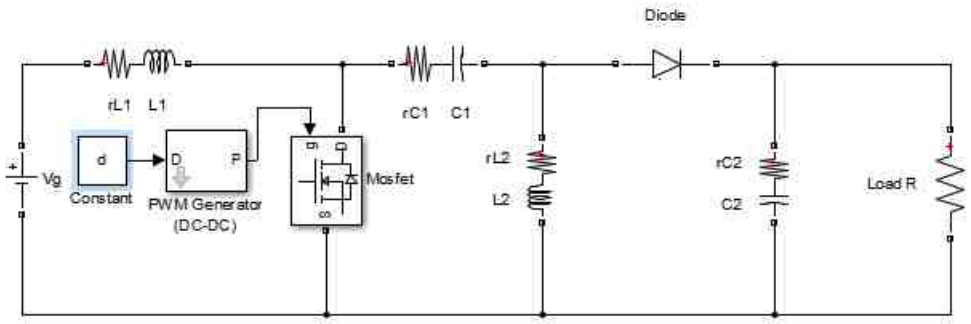

Fig. 2.10. Simulink model of the new DC-DC converter in positive mode by using Simpowersystem tool box in Matlab

Since the new SEPIC based DC-DC converter is a brand new topology, in order to discover the performance and capability of the new design, a Simulation model is needed to provide necessary information for the new design. The Simulink model of the new SEPIC based DC-DC converter is shown in Figure 2.10. This model is built in Matlab by using Simpowersystem tool box. Simpowersystem tool box provides components and tools for modeling and simulating electrical power system.

In this Simulink model, a DC voltage source is applied as source. The circuit is built according to the schematic of a classical SEPIC converter. Each inductor and capacitor is connected to the circuit with a resistor connected in series. These resistors are playing the role of the parasitic resistors of those components. The status of each components are closely monitored by a voltage measurement block and a current measurement block. For each measurement block, two scopes are connected to present a comprehensive view of how each component is operating. The other scope is connected to the measurement block after a mean value block. The data that go through the mean value block will be averaged. The output and input power are calculated by multiply voltage with current. The power conversion efficiency is also measured real time when the operating conditions change.

Although Figure 2.10 only displays the Simulink model for positive mode, the model for negative mode can be easy formed by conducting the diode in the circuit with a reverse direction.

2.5 Simulation Result

Simulations of the converter operation have been done through running the simulation models in Simulink. The simulations simulated the operation of the converter under different condition in both positive and negative modes and tried to generate different voltage on the output load. The result of the simulation will be presented after average to give a mean value for all the readings. By doing this way, the parameters can be easily estimated and the relation between parameters can be clearly observed. An analysis for the result will be given after each graph, and a conclusion will be given in the end of each section.

A. Average Simulation Results of Positive Output Voltage

In this part, three samples of the average simulation result is presented to display the performance of the proposed converter under different operation modes including boost and buck modes. Each graph in this part is form by eight sub-graphs, which represent eight critical parameters that are able to comprehensively demonstrate the performance of the converter. The eight parameters involves output voltage, output current, inductors current (current that go through inductor L_1 and L_2 separately), diode current, transistor current, voltage of capacitor C_1, and voltage across the diode.

All the results showed in this part are obtained after averaging, which means the results will only provide a reading of a consistent mean value of each parameter while the converter is working in a stable condition, and no detail of the waveform for the outputs of the eight parameters will be given.

Figure 2.11 presents the performance of the converter while duty cycle is set to 79.5%. In this situation, the converter operates at boost mode and generates the peak positive output voltage, which is equal to 170V. Since the input current is also the current that flows through inductor L_1, the power transmission efficiency can be calculated as $\frac{V_o I_o}{V_{in} I_{L1}} = \frac{170V \times 1.133A}{30V \times 11.4A} = \frac{192.61W}{342W} = 56.3\%$. The steady state output current, diode current, and inductor L_2 current can be observed to be basically the same, and the inductor L_1 current is also very close to transistor current. While observing for the voltage across capacitor C_1 and Diode, it can be noticed that the mean value of V_{C_1} is close to the voltage of input source and the mean value of V_D equals to the output voltage. These observations can convincingly prove the analysis for the current introduced in section 2.3 modes of operation and section 2.4 sizing is correct.

Comparing the current for first stage with the second stage, it can be easily noticed that the input current is very large, which is 11.4A. Inductor L_1 draws large energy from the source. In this reason, lots of energy will spend on the parasitic resistors and cause energy loss. This can explain the reason why the voltage across capacitor C_1, V_{C_1} is a little less than the input voltage V_g. On the other hand, the components, such as inductor L_1 and transistor Q, will suffer with large current and generate lots of heats. Therefore, to deal with the situation like this, the items selected for the inductor L_1 and transistor must have ability to allow large current to go through. Meanwhile, heat sinks and some other heat reduction methods are also employed on these items in order to avoid overheat and make sure the converter is working safely. The details of how these heats reduction methods are applied will be specifically introduced in the chapter 4.3. At the same time, the current flow through the output cycle is pretty small comparing with the input current, and the average value for the output current is only 1.133A.

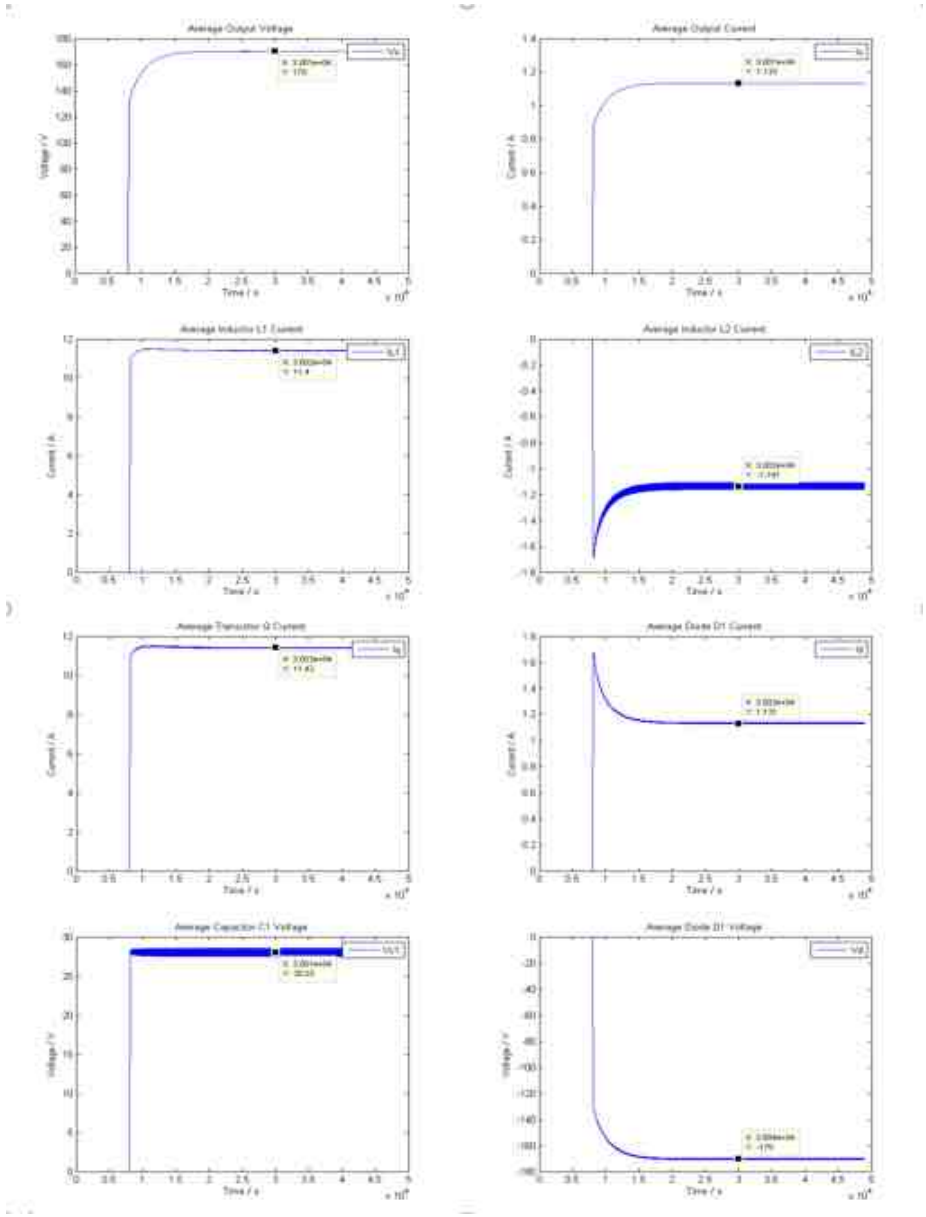

Fig. 2.11. Output Voltage V_o, Output Current I_o, Inductors Current I_{L_1} & I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode. (Duty cycle=79.5%, V_o=170V, I_o=1.133A, I_{L_1}=11.4A, I_{L_2}=-1.141A, I_q=11.42A, I_d=1.131A, V_{C_1}=28.03V, V_D=170)

The second example of the eight critical parameters showed below demonstrate the converter behavior while the converter is operating to only boost the load voltage to 60V, which is equal to two times of the input. Figure 2.12 presents the performance

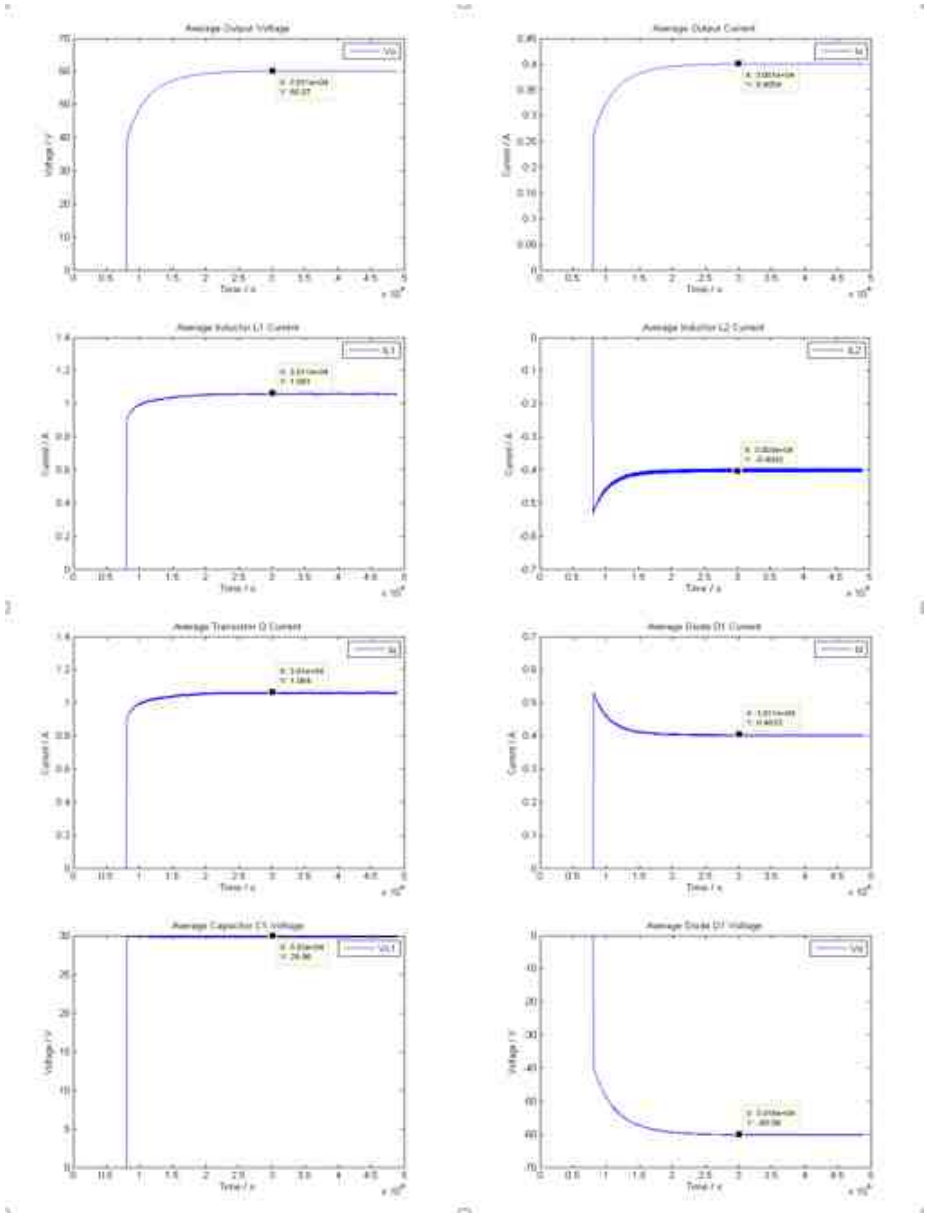

Fig. 2.12. Output Voltage V_o, Output Current I_o, Inductors Current I_{L_1} & I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode. (Duty cycle=28.7%, V_o=60.07V, I_o=0.4A, I_{L_1}=1.06A, I_{L_2}=-0.4042A, I_q=1.064A, I_d=0.403A, V_{C_1}=29.96V, V_D=60.08V)

of the converter while duty cycle is set to 28.7%. In this situation, the converter still operates at a boost mode, however, only boost the voltage to 60V. Since the input current is also the current that flows through inductor L_1, the power efficiency can be calculated as$\frac{V_o I_o}{V_{in} I_{L1}} = \frac{60.07V \times 0.4004A}{30V \times 1.061A} = \frac{24.05W}{31.83W} = 75.56\%$. Compare this results with the one from last example which is also operating in a boost mode, currents are much smaller. Input current changes from 13A to 0.1926A, and output current changes from 1.189A to 0.2388A. These changes reduce the power spend on the parasitic resistors and lead to a dramatic increase in power conversion efficiency, which changes from 56.3% to 75.56%. This change can also be observed from the change of the voltage across the capacitor C_1. The capacitor voltage increased from 28.03V to 29.96V. It is much closer to the input voltage 30V as it supposed to be and less voltage was spent on the parasitic resistors and cause power loss.

Besides, the waveform between current of inductor L_2 and diode D_1, Current of inductor L_1 and Transistor Q, and Voltage across diode D_1 and Load Voltage are very similar and they also share the same value just like the previous example. These observation demonstrate and validate the circuit behavior of the converter in boost mode.

The third example of the positive mode demonstrate how the converter operating in a buck mode. Same as the previous examples, graphs of the eight critical parameters will be presented and the average value will be given. Figure 2.13 presents

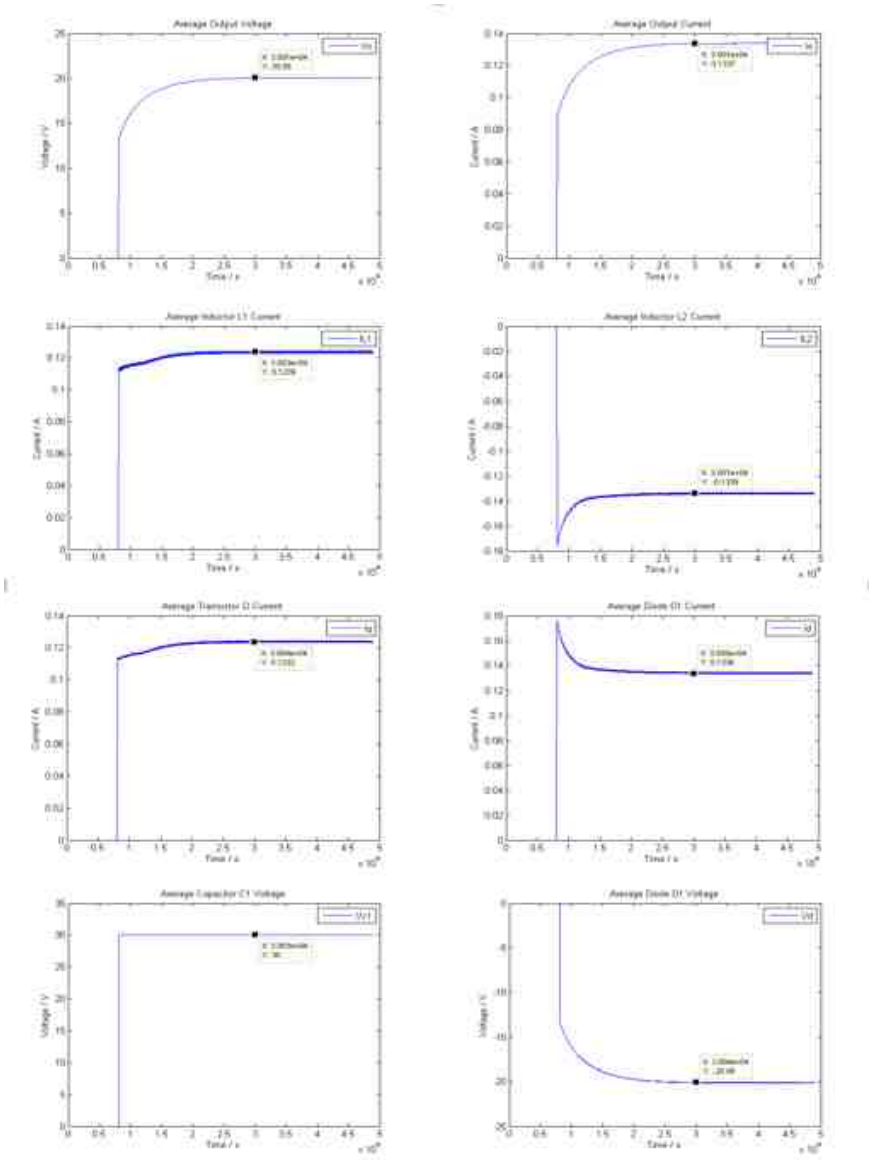

Fig. 2.13. Output Voltage V_o, Output Current I_o, Inductors Current I_{L_1} & I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode. (Duty cycle=10.3%, V_o=20.05V, I_o=0.1337A, I_{L_1}=0.124A, I_{L_2}=-0.134A, I_q=0.123A, I_d=0.1336A, V_{C_1}=30V, V_D=20.06V)

the performance of the converter while duty cycle is set to 10.3%. In this situation, the converter operates at the buck mode. The power transmission efficiency equal to$\frac{V_o I_o}{V_{in} I_{L1}} = \frac{20.05V \times 0.1337A}{30V \times 0.1239A} = \frac{2.68W}{3.717W} = 72.12\%$ Three figures in this part have completely showed the wide range output of the proposed DC-DC converter and its capability of operating in both boost mode and buck mode for positive peak. The output range is covered from 0V to 170V continuously, and basically every voltage levels in this range is reachable if the PWM switch allows the duty cycle to reach every percentage from 0.01 to 1. On the other hand, these figures also exhibits the feature that the proposed converter generates stable outputs. As it can be observed in the figures, the output voltage and currents flowing through each important components are able to reach a stable state after a very short period and generate a constant output voltage on the load. The power transmission efficiency of the converter is between 54% to 80%. The power transmission efficiency for high output voltage is low is due to the high input current and current ripples. Much energy is consumed by the parasitic resistors of the components such as inductors, capacitors, and transistor. Since the source is a constant DC source, the input current will decreased as the output voltage is getting smaller. Therefore, the power transmission rate exhibits a decreasing trend with duty cycle increased.

Three figure of results in both boost and buck mode are presented here in order to demonstrate and briefly expound the abilities of the proposed converter. More results in both boost and buck modes are also provided in Appendix to give a more comprehensive view of the ability of the converter.

B. Average Simulation Results of Negative Output Voltage

As the critical innovation of the topology, how is the converter performing while reversed the direction of the diode in classic SEPIC converter will be focused. The following graphs are the simulation results generated by the converter while it is operating in negative mode. Similar to what has been done for the positive mode,

measurements of eight critical parameters including output voltage, output current, inductors current (current that go through inductor L_1 and L_2 separatly), diode current, transistor current, voltage of capacitor C_1, and voltage across the diode have been done and presented in this part as the result of the simulation for the negative peak in order to prove whether the converter is able to generate negative voltage by changing the direction of the diode and operated as introduced in the previous chapter. The peak output voltage for negative mode can also be obtained by setting the duty cycle to -83.3%. The converter is operating in boost mode in this situation and the output voltage is boosted to -169.5V from 30V. As it can be observed, by conducting the diode into the circuit in reversed direction, the polarity of the output voltage can actually be reversed and become negative while the source remain using a constant DC power supply which providing positive 30V input voltage constantly.

By comparing the results for positive and negative 170V, many similar characteristics can be observed, such as large input current, and small output current. The input current is equal to 10.81A. It is slightly smaller than 11.4A for the positive peak, however, they are still pretty close. Same as the input current, 1.13A is also close to 1.141A. The current situations for the input side for both positive mode and negative mode could be proved to be following the same pattern since nothing was changed in this half. As for the output side, the diode was conducting into the circuit in a reversed direction, hence the direction of output current and inductor L_2 were changed along with it. However, the waveform of the current keeps the same shape as the positive mode, which means the modification of the direction for the diode did not change the mean value of the current flowing through the inductor L_2, but just the direction. By using the data recorded in this result, the power transmission efficiency can be obtained by using the formula $\frac{V_o I_o}{V_{in} I_{L1}} = \frac{-169.5V \times -1.13A}{30V \times 10.81A} = \frac{191.54W}{324.3W} = 59.05\%$.

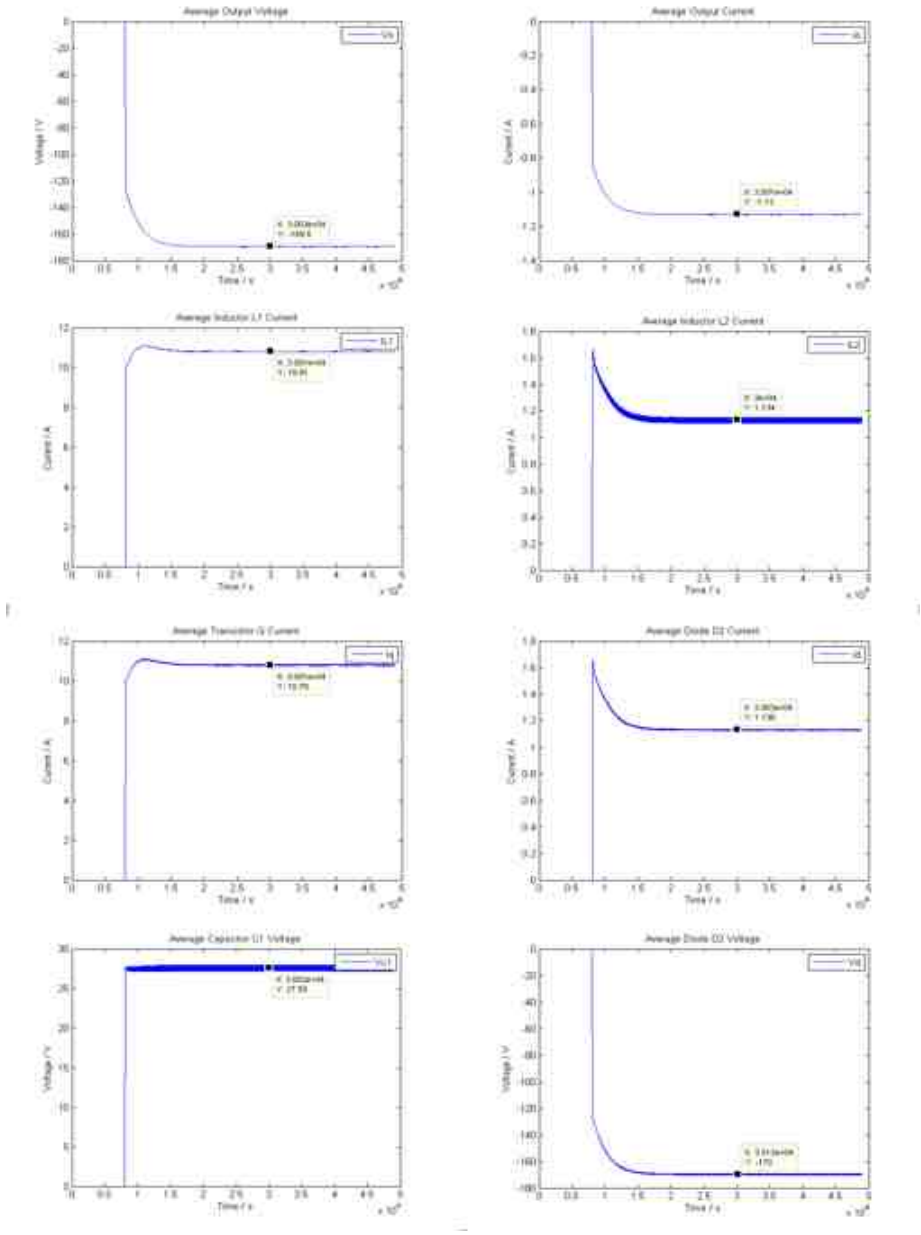

Fig. 2.14. Output Voltage V_o, Output Current I_o, Inductors Current I_{L_1} & I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode. (Duty cycle=-83.3%, V_o=-169.5V, I_o=-1.13A, I_{L_1}=10.81A, I_{L_2}=1.134A, I_q=10.79A, I_d=1.136A, V_{C_1}=27.59V, V_D=-170V)

In order to make a best comparison for the converter between positive mode and negative mode, the condition for the -60V was chosen using as the second example of the negative mode. Comparing the result with 60V for the positive mode, they

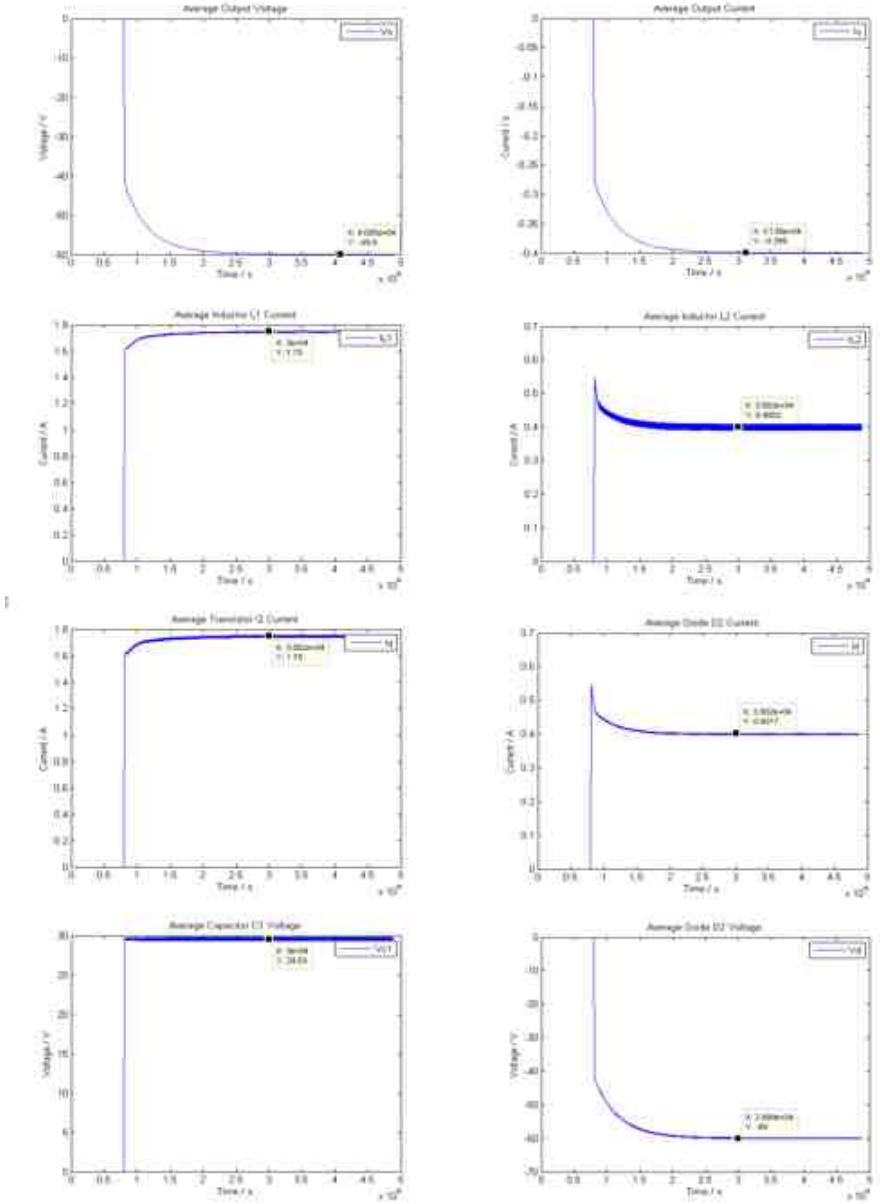

Fig. 2.15. Output Voltage V_o, Output Current I_o, Inductors Current I_{L_1} & I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode. (Duty cycle=-45.3%, V_o=-59.9V, I_o=-0.399A, I_{L_1}=1.75A, I_{L_2}=0.4002A, I_q=1.75A, I_d=0.4017A, V_{C_1}=29.53V, V_D=-60V)

both have a similar mean value for output current, which is around 0.4A but with different polarity. Meanwhile, while comparing the input current, the mean value for the input current can be observed to be much larger than the one in positive mode. From 1.061A to 1.75A, the input current increased by 0.689A after changing the diode direction. So, the input current could observed to be affected by the modification of the diode direction. More power was draw from the source but only deliver the same amount of power at the output lead to a low efficiency of the power transmission. The power transmission rate for this mode is $\frac{V_o I_o}{V_{in} I_{L1}} = \frac{-59.9V \times -0.399A}{30V \times 1.75A} = \frac{23.9W}{52.5W} = 45.52\%$.

The third example gives the result for the situation which the output voltage equals -20V. The converter operates in buck mode in this situation and presents its performance for performing step down voltage. The power transmission efficiency is

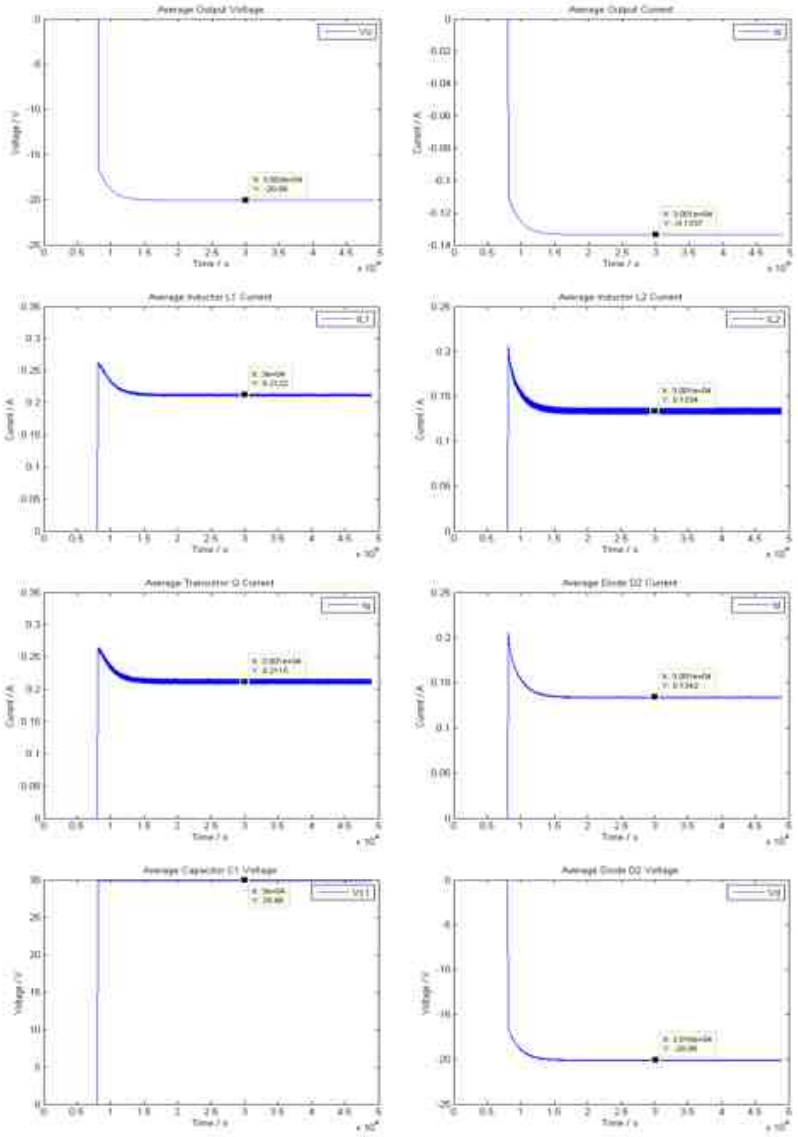

Fig. 2.16. Output Voltage V_o, Output Current I_o, Inductors Current I_{L_1} & I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode. (Duty cycle=-23.3%, V_o=-20.06V, I_o=-0.134A, I_{L_1}=0.212A, I_{L_2}=0.1334A, I_q=0.2115A, I_d=0.134A, V_{C_1}=29.98V, V_D=-20.06V)

equal to $\frac{V_o I_o}{V_{in} I_{L1}} = \frac{-20.06V \times -0.1337A}{30V \times 0.2122A} = \frac{2.68W}{6.37W} = 42.13\%$. Comparing the reading with the one for positive peak, the main difference is still existing in input current. The input current is equal to 0.2122A, it is larger than 0.1239A. On the other hand, the waveform presented having a different shape as the 20V situation. These differences indicate that while conducting the diode in a reverse direction and change the operation mode of the converter to negative mode, not only the current direction of the output side is changed, but also the current in the input side will perform a big change which is totally different than the original mode. This change will cause the inductor L_1 to draw more energy from the source to generate the same level of output voltage at the load, which cause large power loss and lower the efficiency.

In this section, the average simulation results for both positive and negative peaks are showed separately in boost mode, buck mode, and the mode when output voltage is equal to input. These results demonstrate the capability of the proposed converter that it is able of generating wide range of outputs in both polarities with virtually infinite voltage levels. The new-designed DC-DC converter is possible to generate any voltage between -170V to 170V, and the output voltage is only controlled by changing duty cycle of the transistor. The current for each element in the circuit is reasonable and possible to achieve in practical experiment.

3. MATHEMATICAL ANALYSIS

3.1 State-space Averaging model

The input and output voltages of the converter in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) can be obtain as follows:

$$\frac{V_{out}(CCM)}{V_{in}} = \frac{D}{1-D} or \frac{D}{1+D} \tag{37}$$

$$\frac{V_{out}(DCM)}{V_{in}} = \pm D \cdot \sqrt{\frac{R \cdot T_s}{2 \cdot L_{eq}}} \tag{38}$$

$$\frac{1}{L_{eq}} = \frac{1}{L_1} + \frac{1}{L_2} \tag{39}$$

Duty cycle is the ratio of the conducting time to the whole switching period Ts and is represented by D. The ideal duty cycle for the switching should be between 0 to 100% (0¡D¡1). In each half cycle, the converter ideally operate in buck mode if the value of D is less than 50%, and operate in boost mode if D is larger than 50%.

A. Positive Peak Voltage Generation

When the converter is operating in the mode as shown in Figure 2.2, the switch Q is off and D_1 is on for duty cycle $1-D$. In opposite, when the converter operates in the situation as shown in Figure 2.3, the switch is on and D_1 is off for period of D. To model the system, five equations is considered in each set of the state space system. Four of the five equations represent the four state variable dynamics: i_{L_1}, i_{L_2}, v_{C_1}, v_{C_2} and one equation represents the output voltage of the circuit V_o. Equations representing mode I (Figure. 2.2) and mode II (Figure. 2.3) are as follows:

Mode I: When Q is off and D_1 is on:

$$\begin{cases} \frac{di_{L1}}{dt} = -\frac{\left(r_{L1}+r_{C1}+\frac{Rr_{C2}}{R+r_{C2}}\right)}{L_1} i_{L1} - \frac{\frac{Rr_{C2}}{R+r_{C2}}}{L_1} i_{L2} - \frac{1}{L_1} v_{C1} + \frac{\frac{R}{R+r_{C2}}}{L_1} v_{C2} + \frac{Vi}{L_1} \\ \frac{di_{L2}}{dt} = \frac{\frac{Rr_{C2}}{(R+r_{C2})}}{L_2} i_{L1} - \frac{r_{L2}+\frac{Rr_{C2}}{R+r_{C2}}}{L_2} i_{L2} - \frac{\frac{R}{R+r_{C2}}}{L_2} v_{C2} \\ \frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L1} \\ \frac{dv_{C2}}{dt} = \frac{\frac{R}{(R+r_{C2})}}{C_2} i_{L1} + \frac{\frac{R}{(R+r_{C2})}}{C_2} i_{L2} - \frac{\frac{1}{(R+r_{C2})}}{C_2} v_{C2} \\ V_o = \frac{Rr_{C2}}{R+r_{C2}} i_{L1} + \frac{Rr_{C2}}{R+r_{C2}} i_{L2} + \frac{R}{R+r_{C2}} v_{C2} \end{cases} \tag{40}$$

Mode II: When Q is on and D_1 is off:

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{V_i}{L_1} - \frac{r_{L1}}{L_1} i_{L1} \\ \frac{di_{L2}}{dt} = -\frac{(r_{L2}+r_{C1})}{L_2} i_{L1} + \frac{1}{L_2} v_{C1} \\ \frac{dv_{C1}}{dt} = -\frac{1}{C_1} i_{L2} \\ \frac{dv_{C2}}{dt} = -\frac{1}{C_2(R+r_{C2})} v_{C2} \\ V_o = \frac{R}{R+r_{C2}} v_{C2} \end{cases} \tag{41}$$

If the state value is defined as $x = [i_{L_1}, i_{L_2}, v_{C_1}, v_{C_2}]$, the averaged state space model of positive peak voltage can be obtained as equation (48).

$$\begin{cases} \dot{x} = A^+_{avg} x + B^+_{avg} u \\ V_o = C^+_{avg} x \end{cases} \tag{42}$$

Then the averaged model parameters of the positive operation mode can be obtained as showed in equation (43) - (45).The average model presents the average situation of the operations of the converter in positive mode.

$$A_{avg}^{+} =$$

$$\begin{bmatrix} \frac{1}{L_1}\left(-r_{L1} + (D-1)\left(rc1 + \frac{Rr_{C2}}{R+r_{C2}}\right)\right) & \frac{(D-1)Rr_{C2}}{L_1(R+r_{C2})} & \frac{D-1}{L_1} & \frac{(D-1)R}{L_1(R+r_{C2})} \\ \frac{(D-1)Rr_{C2}}{L_2(R+r_{C2})} & \frac{(D-1)Rr_{C2}-(R+r_{C2})(Dr_{C1}+r_{L2})}{L_2(R+r_{C2})} & \frac{D}{L_2} & \frac{(D-1)R}{L_2(R+r_{C2})} \\ \frac{1-D}{C_1} & -\frac{D}{C_1} & 0 & 0 \\ \frac{(1-D)R}{C_2(R+r_{C2})} & \frac{(1-D)R}{C_2(R+r_{C2})} & 0 & -\frac{1}{C_2(R+r_{C2})} \end{bmatrix} \quad (43)$$

$$B_{avg}^{+} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^{T} . \quad (44)$$

$$C_{avg}^{+} = \begin{bmatrix} \frac{(1-D)Rr_{C2}}{C_2(R+r_{C2})} & \frac{(1-D)Rr_{C2}}{C_2(R+r_{C2})} & 0 & \frac{R}{R+r_{C2}} \end{bmatrix} . \quad (45)$$

B. Negative Peak Voltage Generation

Mode III and mode IV represent the situation of the operation that were shown in Figure 2.4 and 2.5. In mode III, the switch Q is off and D_2 is on for duty cycle $1 - D$, and in Mode IV, the switch is on and D_2 is off for period of T_s. Same as the previous modes, each set of state space system consist of five equations, four of which represent the four state variable dynamics $iL1, iL2, vC1, vC2$ and one equation to represent the output voltage of the circuit V_o. Equations representing mode III (Figure. 2.6) and mode IV (Figure. 2.7) are as follows:

Mode III: When Q is off and D_2 is on:

$$\begin{cases} \frac{di_{L1}}{dt} = -\frac{\left(r_{L1}+r_{C1}+\frac{Rr_{C2}}{R+r_{C2}}\right)}{L_1} i_{L1} + \frac{\frac{Rr_{C2}}{R+r_{C2}}}{L_1} i_{L2} - \frac{1}{L_1} v_{C1} + \frac{\frac{R}{R+r_{C2}}}{L_1} v_{C2} + \frac{Vi}{L_1} \\ \frac{di_{L2}}{dt} = \frac{\frac{Rr_{C2}}{(R+r_{C2})}}{L_2} i_{L1} - \frac{r_{L2}+\frac{Rr_{C2}}{R+r_{C2}}}{L_2} i_{L2} - \frac{\frac{R}{R+r_{C2}}}{L_2} v_{C2} \\ \frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L1} \\ \frac{dv_{C2}}{dt} = -\frac{\frac{R}{(R+r_{C2})}}{C_2} i_{L1} + \frac{\frac{R}{(R+r_{C2})}}{C_2} i_{L2} - \frac{1}{C_2(R+r_{C2})} v_{C2} \\ V_o = -\frac{Rr_{C2}}{R+r_{C2}} i_{L1} + \frac{Rr_{C2}}{R+r_{C2}} i_{L2} + \frac{R}{R+r_{C2}} v_{C2} \end{cases} \quad (46)$$

Mode IV: When Q is on and D_2 is off:

$$\begin{cases} \frac{di_{L1}}{dt} = \frac{V_i}{L_1} - \frac{r_{L1}}{L_1} i_{L1} \\ \frac{di_{L2}}{dt} = -\frac{(r_{L2}+r_{C1})}{L_2} i_{L2} - \frac{1}{L_2} v_{C1} \\ \frac{dv_{C1}}{dt} = \frac{1}{C_1} i_{L2} \\ \frac{dv_{C2}}{dt} = -\frac{1}{C_2(R+r_{C2})} v_{C2} \\ V_o = \frac{R}{R+r_{C2}} v_{C2} \end{cases} \tag{47}$$

Considering $x = [i_{L_1}, i_{L_2}, v_{C_1}, v_{C_2}]$, the averaged state space model of negative peak voltage can be obtained as:

$$\begin{cases} \dot{x} = A_{avg}^{-} x + B_{avg}^{-} u \\ V_o = C_{avg}^{-} x \end{cases} \tag{48}$$

The negative peak averaged model parameters can be obtained as:

$$A_{avg}^{-} = \begin{bmatrix} \frac{1}{L_1}\left(-r_{L1} + (D-1)\left(r_{C1} + \frac{Rr_{C2}}{R+r_{C2}}\right)\right) & \frac{(1-D)Rr_{C2}}{L_1(R+r_{C2})} & \frac{D-1}{L_1} & \frac{(1-D)R}{L_1(R+r_{C2})} \\ \frac{(1-D)Rr_{C2}}{L_2 2(R+r_{C2})} & -\frac{(Dr_{C2}+r_{L2})}{L_2} + \frac{(D-1)Rr_{C2}}{L_2(R+r_{C2})} & -\frac{D}{L_2} & \frac{(D-1)R}{L_2(R+r_{C2})} \\ \frac{1-D}{C_1} & \frac{D}{C_1} & 0 & 0 \\ \frac{(D-1)R}{C_2(R+r_{C2})} & \frac{(1-D)R}{C_2(R+r_{C2})} & 0 & -\frac{1}{C_2(R+r_{C2})} \end{bmatrix} \tag{49}$$

$$B_{avg}^{-} = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}^T, \tag{50}$$

$$C_{avg}^{-} = \begin{bmatrix} \frac{(D-1)Rrc2}{(R+rc2)} & \frac{(1-D)Rrc2}{(R+rc2)} & 0 & \frac{R}{R+rc2} \end{bmatrix}. \tag{51}$$

3.2 Transfer Function

In order to do the small signal analysis of the converter, Vorprians PWM switch model [8] is utilized. Figure 3.1 shows the equivalent circuit. As introduced in Vorprians model, the MOSFET and the diode in the converter were replaced by a PWM switch equivalent to a 1:D transformer, where D is the duty cycle of the control signal. After obtained the simplified circuit, with the input voltage V_d and duty cycle

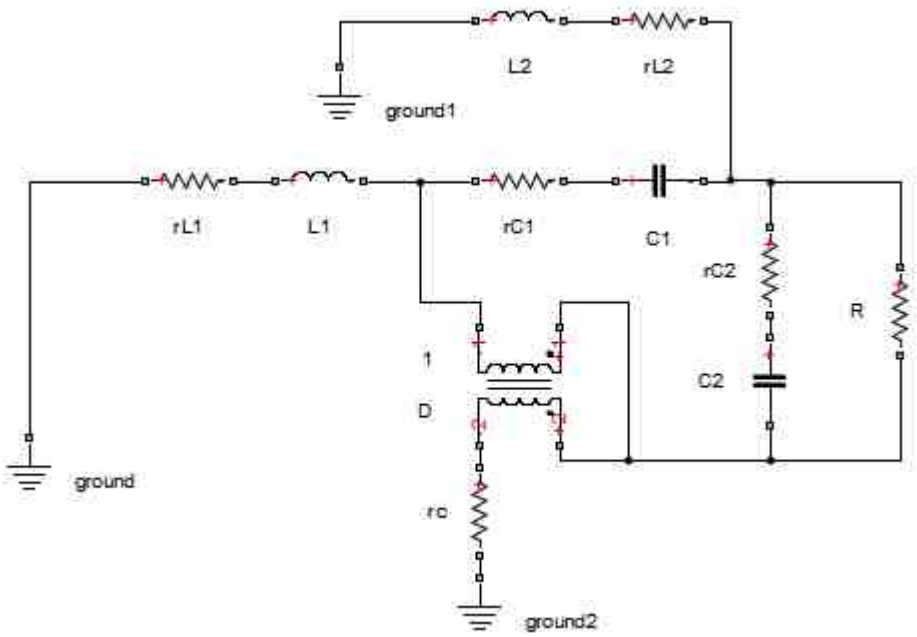

Fig. 3.1. The redrawn circuit for DC analysis by using the Vorprians PWM switch model

d set to 0, by using the equation as follows, the small-signal control-to-output transfer function can be obtained:

$$\frac{V_o}{d} = k_d \frac{N_d s}{D_s} \tag{52}$$

The converter introduced here is a well-designed forth order converter, therefore the denominator consists of two quadratic factors. Those factors have well separated resonance which are almost entirely damped by the load. The parasitic resistances of the components such as inductors and capacitors make almost no effect on those two resonant frequencies of $D(s)$ and contribute very little to the damping of the resonances while the converter is operating with normal loading conditions. Therefore, the expression of $D(s)$ can be rewritten from:

$$D(s) = 1+a_1 s+a_2 s+a_2 s^2+a_3 s^3+a_4 s^4 \; to \; D(s) = (1+\frac{s}{\omega_1 Q_1}+\frac{s^2}{\omega_1^2})(1+\frac{s}{\omega_2 Q_2}+\frac{s^2}{\omega_2^2}) \tag{53}$$

$$a1 \approx \frac{1}{\omega_1 Q_1}, \tag{54}$$

$$a2 \approx \frac{1}{\omega_1^2}, \tag{55}$$

$$a3 \approx \frac{1}{\omega_1 Q_1 \omega_2^2} + \frac{1}{\omega_2 Q_2 \omega_1^2}, \tag{54}$$

$$a4 \approx \frac{1}{\omega_1^2 \omega_2^2} \tag{55}$$

For DC analysis, the DC source is set to zero, inductors become short circuits, and capacitors become open circuits. The circuit can be redrawn as shown in Figure 3.2. After analysis the reference circuit, the coefficients of $D(s)$ can be obtained as shown

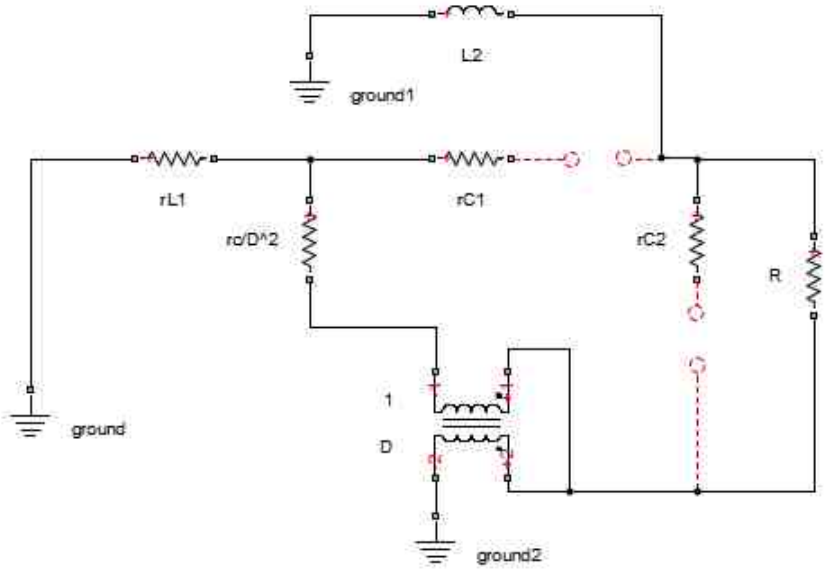

Fig. 3.2. Reference circuit indicating normal port conditions

below:

$$a_1 = \frac{L_1}{(\frac{D'}{D})^2 R} + \frac{L_2}{R} + C_2(r_{C2} + r_{L2} + \frac{r_C}{D'^2} + r_{L1}(\frac{D}{D'})^2) + C_1(r_{C1} + r_{L1} + r_{L2})/tag58$$

$$a_2 = L_1(C_2(\frac{D}{D'})^2 + C_1) + L_2(C_2 + C_1) \tag{59}$$

$$a_3 = L_1 L_2 C_1 \frac{1}{D'^2 R} \tag{60}$$

$$a4 = L_1 L_2 C_1 \frac{1}{D'^2} \tag{61}$$

Since a_1 to a_4 have explicit formula, it is much easier to determine the expression for$Q_1, Q_2, {}_1$, and ${}_2$.

$$Q_1 = \frac{R}{\omega_1 L_1 (\frac{D}{D'})^2 + L_2} \tag{62}$$

$$Q_2 = \frac{R}{\omega_2(L_1 + L_2)(\frac{C_1}{C_2})(\frac{\omega_1}{\omega_2})^2} \tag{63}$$

$$\omega_1 = \frac{1}{\sqrt{L_1(C_2(\frac{D}{D'})^2 + C_1) + L_2(C_1 + C_2)}} \tag{64}$$

$$\omega_2 = \sqrt{\frac{C_1(D'^2 + 1) + C_2(D^2 + 1)}{C_1 C_2 L_1}} \tag{65}$$

While calculating $N(s)$ for the negative peak, $N(s)$ corresponds to the null conditions in the response$V(s)$ to the excitation courses $\frac{V_D}{D}d$ and $I_c d$.

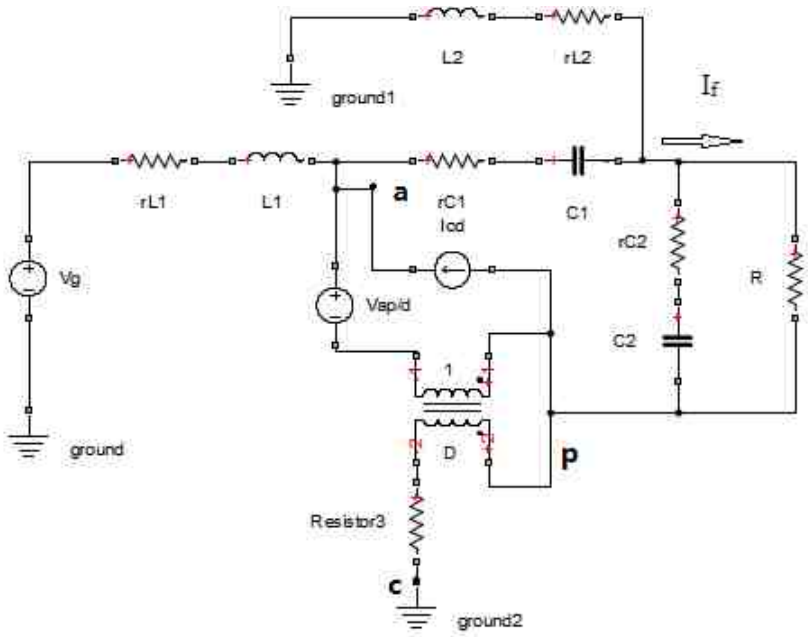

Fig. 3.3. Reference circuit indicating null conditions for negative peak

The first null is given by the zero of impedance across $Vo(s)$:

$$N_d(s) = (1 + sr_{c_2}C_2)N_2(s) \tag{66}$$

Second null is given by condition the current flow to load and capacitor C_2 if=0. Doing KCL at node P, KCl at node c, and KVL at the loop of L_1, C_1, and L_2. $N(s)$ for negative peak voltage can be easily calculated as:

$$N(s) = -(\frac{L_1L_2C_1}{R})(\frac{D}{D'(1+D)})s^3 + (C_1(L_1+L_2) + \frac{L_2C_1}{D})s^2 - (\frac{L_1}{R}(\frac{D^2}{D'(1+D)}) + \frac{C_1}{L_1}(L_1+L_2)R(\frac{D'(1+D)}{D^2}))s - 1 \quad (67)$$

Repeat the same procedure, the N(s) for the positive peak can also be calculated. However, the circuits used for positive peak and negative peak are different.

The referent circuit for the positive peak is shown in Figure 3.2f. Since the di-

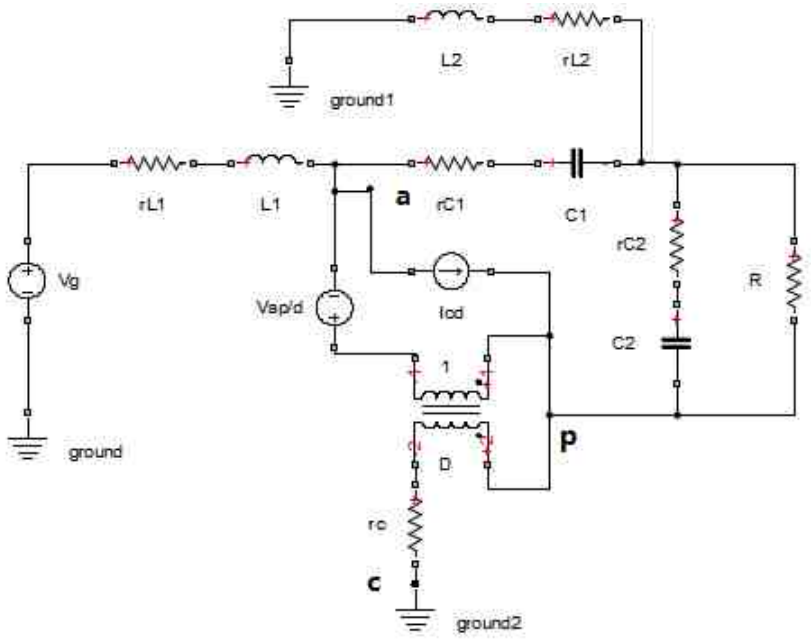

Fig. 3.4. Reference circuit indicating null conditions for positive peak

rection of the diode is different, the excitation sources $\frac{V_D}{D}d$ and I_cd have the different directions. This can be justified by considering current directions as expressed in positive peak. Therefore, $N(s)$ for positive peak is calculated as:

$$N(s) = -(\frac{L_1L_2C_1}{R})(\frac{D}{D'^2})s^3 + (C_1(L_1+L_2) + \frac{L_2C_1}{D})s^2 - (\frac{L_1}{R}(\frac{D}{D'})^2 + \frac{C_1}{L_1}(L_1+L_2)R(\frac{D'}{D})^2)s + 1 \quad (68)$$

With $k_d = \frac{1}{D'^2}$, by combining three terms $k_d, N(s)$, and $D(s)$, the control-to-output can be expressed. This will be discussed in next section.

3.3 Small-Signal Analysis

Through analyzing the new circuit with PWM switch, the converters transfer function can be obtained as a 4_{th} order system as follows: Control-to-output transfer function of the positive peak can be obtained as:

$$\frac{V_o}{d} \approx \frac{1}{D'^2} \frac{-\frac{(L_1L_2C_1)}{R}(\frac{D}{D'^2})s^3 + (C_1(L_1+L_2) + \frac{L_2C_1}{D})s^2 - (\frac{L_1}{R}(\frac{D}{D'}^2)}{(1+\frac{s}{\omega_1 Q_1} + \frac{s^2}{\omega_1^2})(1+\frac{s}{\omega_2 Q_2} + \frac{s^2}{\omega_2^2})} \\ \frac{+\frac{C_1}{L_1}(L_1+L_2)R(\frac{D'}{D})^2)s+1}{(1+\frac{s}{\omega_1 Q_1} + \frac{s^2}{\omega_1^2})(1+\frac{s}{\omega_2 Q_2} + \frac{s^2}{\omega_2^2})} \quad (69)$$

Control-to-output transfer function of the negative peak can be obtained as:

$$\frac{V_o}{d} \approx \frac{1}{D'^2} \frac{-\frac{(L_1L_2C_1)}{R}(\frac{D}{D'(1+D)})s^3 + (C_1(L_1+L_2) + \frac{L_2C_1}{D})s^2}{(1+\frac{s}{\omega_1 Q_1} + \frac{s^2}{\omega_1^2})(1+\frac{s}{\omega_2 Q_2} + \frac{s^2}{\omega_2^2})} \\ \frac{-(\frac{L_1}{R}(\frac{D}{D'(1+D)}^2) + \frac{C_1}{L_1}(L_1+L_2)R(\frac{D'(1+D)}{D})^2)s+1}{(1+\frac{s}{\omega_1 Q_1} + \frac{s^2}{\omega_1^2})(1+\frac{s}{\omega_2 Q_2} + \frac{s^2}{\omega_2^2})} \quad (70)$$

where:

$$Q_1 = \frac{R}{\omega_1 L_1(\frac{D}{D'})^2 + L_2} \quad (71)$$

$$Q_2 = \frac{R}{\omega_2(L_1+L_2)(\frac{C_1}{C_2})(\frac{\omega_1}{\omega_2})^2} \quad (72)$$

$$\omega_1 = \frac{1}{\sqrt{L_1(C_2(\frac{D}{D'})^2 + C_1) + L_2(C_1+C_2)}} \quad (73)$$

$$\omega_2 = \sqrt{\frac{C_1(D'^2+1) + C_2(D^2+1)}{C_1C_2L_1}} \quad (74)$$

$$D' = 1 - D \quad (75)$$

The transfer functions were also simulated in Simulink. The input d(s) is equal to the sum of the basic duty cycle D and the duty cycle variation Δd which is used as a control command. The parameters of the circuit are given in Table 3.1.

Table 3.1
Parameter of the new DC-DC converter

Parameters	**Value**	**Parameters**	**value**
Switching Frequency	8.3kHz	L_1	$307\mu H$
Duty Cycle	83.3%/79.5%	L_2	$307.8\mu H$
Input Voltage	30V	C_1	$1\mu F$
Load	150Ω	C_2	$80\mu F$

Figure 3.5 & 3.6 shows the simulation results from transfer function model comparing with the result from Simpowersystem model for the Positive output voltage. Figure 3.7 & 3.8 shows the simulation results from transfer function model comparing with the result from Simpowersystem model for the negative output voltage.

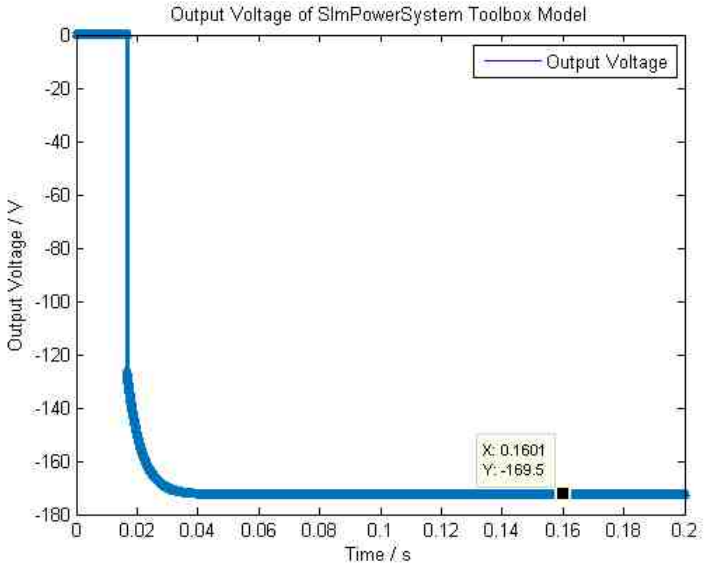

Fig. 3.5. Simulation result of negative peak from Simpowersystem model with D=-83.3%. V_o= -169.5V

As comparison, the simulation result of transfer function is given as follow. To better compare with the result from Simpowersystem, the simulation for the transfer function remain the same simulation time as the simulation for Simpowersystem.

The simulation results from the transfer function model reflects an original output voltage signal without any averaging or filter process which demonstrates oscillations before the waveform reach steady state. However, using averaging model removes the transient oscillations from the system response. Both simulations started at time 16.7ms, and reached positive 170V and negative 170V. This demonstrates the accuracy of the modeling and its matching with the results obtained from MATLAB Simpowersystem toolbox. The circuit can generate any voltage on-demand at any desired polarity.

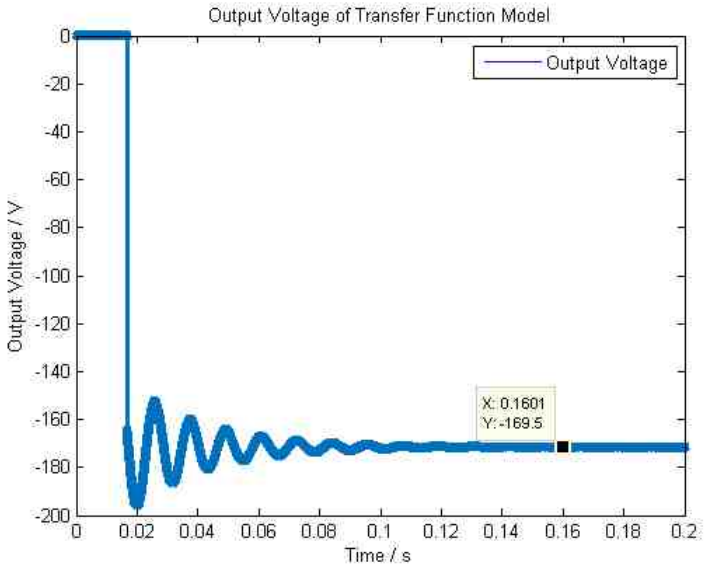

Fig. 3.6. Simulation result of negative peak from transfer function model with D=83.3%, Δd=-1.75% V_o= -169.5V

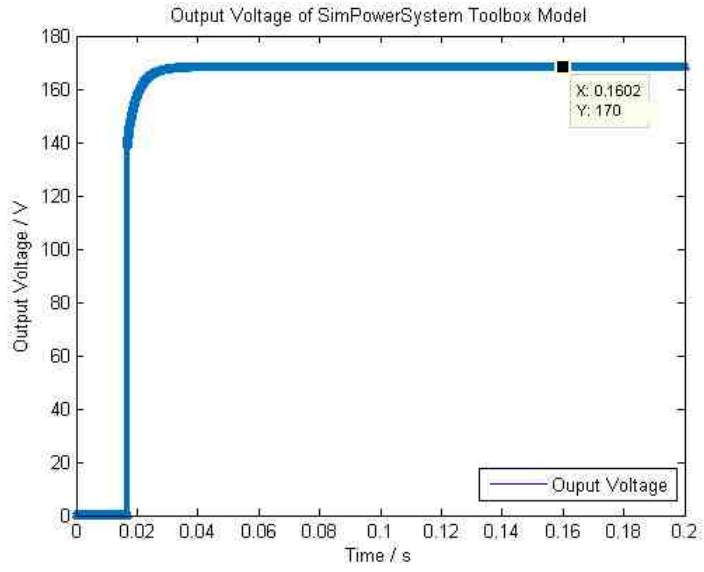

Fig. 3.7. Simulation result of positive peak from Simpowersystem model with duty cycle D=79.5%. output voltage V_o=170V

Since $\frac{V_o}{V_g} = \frac{d}{1-d}$ for the positive output and $\frac{V_o}{V_g} = \frac{d}{1+d}$ for negative output, in order to generate a ±170V of output voltage from 30V DC input, the duty cycle d calculated

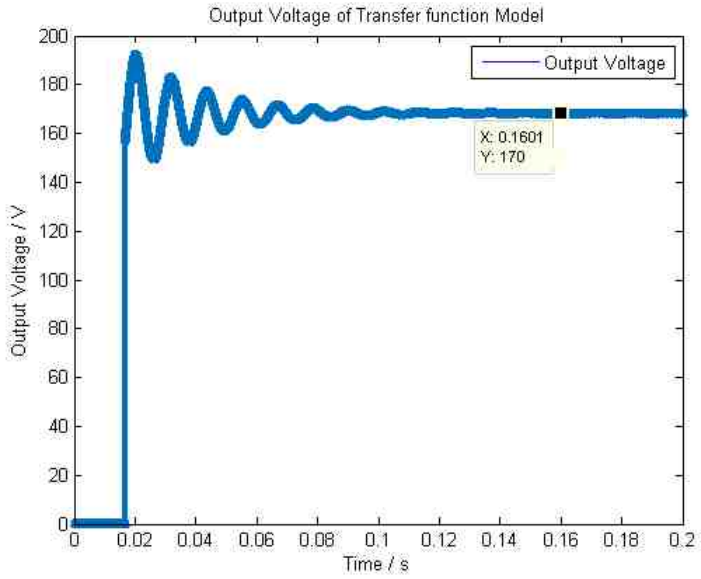

Fig. 3.8. Simulation result of positive peak from transfer function model with duty cycle D=79.5%, variation Δd=-5.32%. output voltage $V_o(Max)$=170V

from previous equation is d=85.3%. According to the Simpowersystem simulations the duty cycle D was set to 83.3% for positive and 79.5% for negative to generate a ±170V output. Considering the small signal variations of $d + \Delta d = D$, the variation Δd can be calculated as $\Delta d = D - d = 83.3\% - 85.15\% = -2.15\%$, which is close to the control signal which is -1.75% for negative mode. Similarly, for the positive mode, the PWM variation equals to $\Delta d = D - d = 79.5\% - 85.15\% = -5.65\%$, and the control signal is -5.32%, they are obviously close to each other. This control signal generates a ±170V in the output of the transfer functions. This slight deviation between the control signals to the PWM variation might be the consideration of inner circuit element resistances in capacitors and inductors.

3.4 Stability Analysis

In order to analyze the limits of stability of the proposed circuit in both positive and negative peaks, Bode plots of the transfer function are provided in Figure 14.

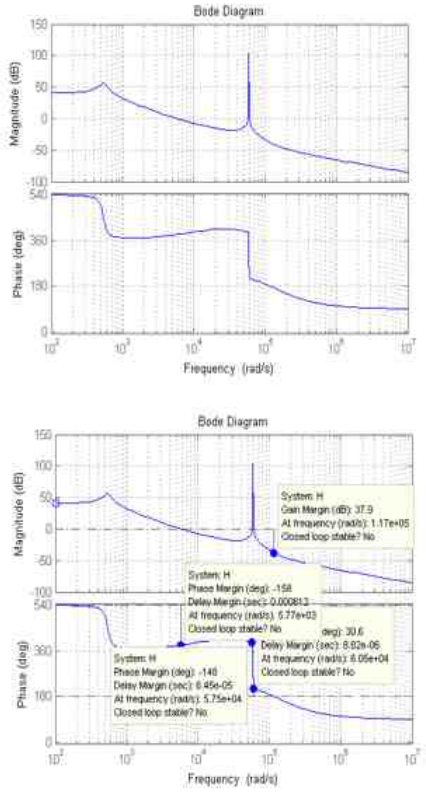

Fig. 3.9. Bode Plots for Negative Output Voltage

Figure 3.9 gives a presentation of the Bode diagram of the system operating in the negative mode. waveform is showed and the critical points are marked. the result can be easily told to be stable. The Bode diagram analysis result for positive peak is also given in Figure 3.10, which is also can be observed to be stable.

The Figure 15 shows the pole-zero maps for both of negative and positive output. For the positive one, the locations of zeros are all in the left half of the s-plane, which can proof the system is stable.

The Figure 3.11 & 3.12 shows the step response for both negative and positive output. The shapes of the response waveform for both polarity matched up with each other. The peak amplitude, overshoot and rise time for negative and positive output voltage can be observed as -178V, 78.5%, 2.03ms and 179V, 78.6%, 1.97ms. They are pretty close to each other. After 93.6ms for negative output and 93.3ms for

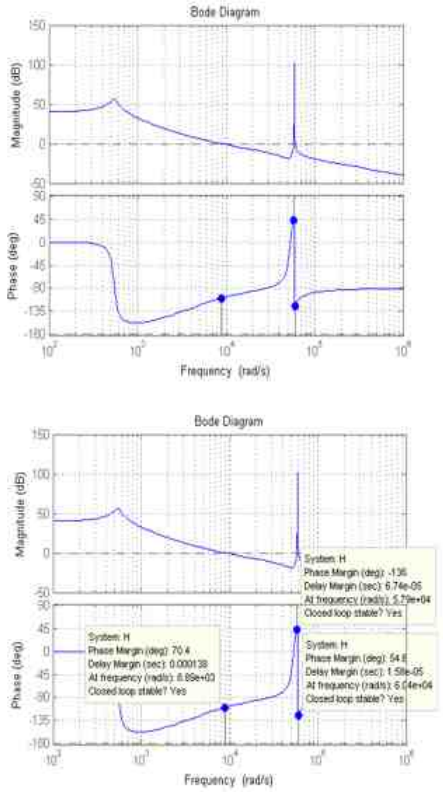

Fig. 3.10. Bode Plots for Positive Output Voltage

positive output, the signal settling at final value of -100V and 100V. Step responses for both polarities will finally reach steady state of ±100V, which means both system are stable and synchronized. In other word, this converter can reach the same peak for both negative output and positive output at the same time, which means they are equal and symmetric responses in positive and negative peaks.

The stable analysis results shows that the proposed converter has ability to stabilize the output signal and generate a stable output at the output load. Therefore, the converter is worthy for researching and has its value in applying in industrial applications.

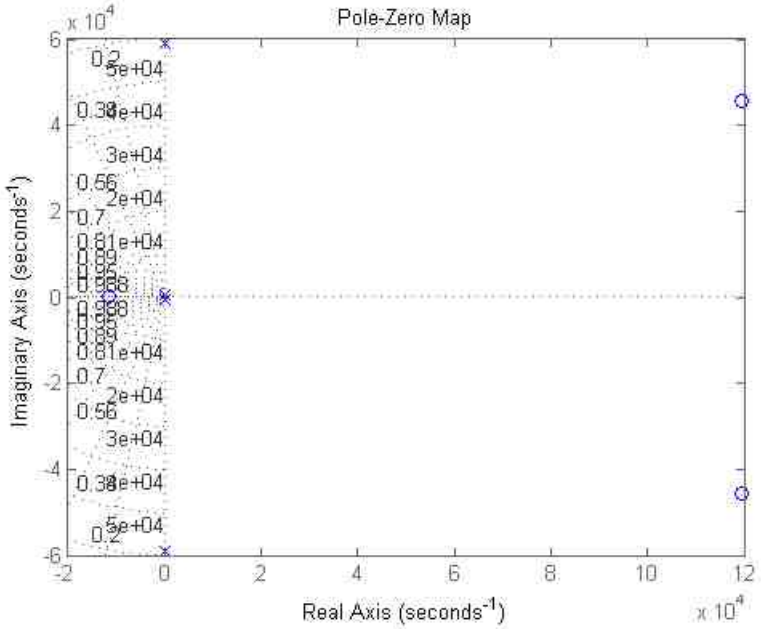

Fig. 3.11. Pole-Zero maps for Negative Peak

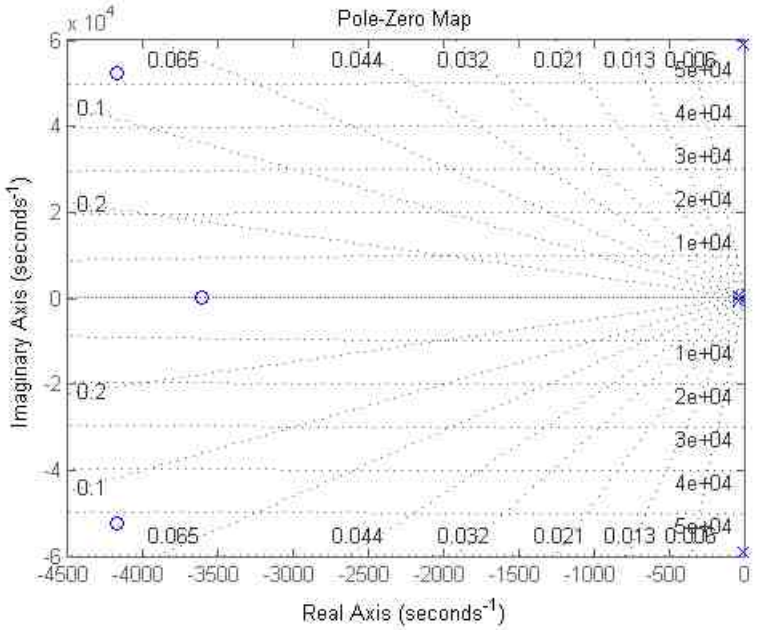

Fig. 3.12. Pole-Zero maps for Positive Peak

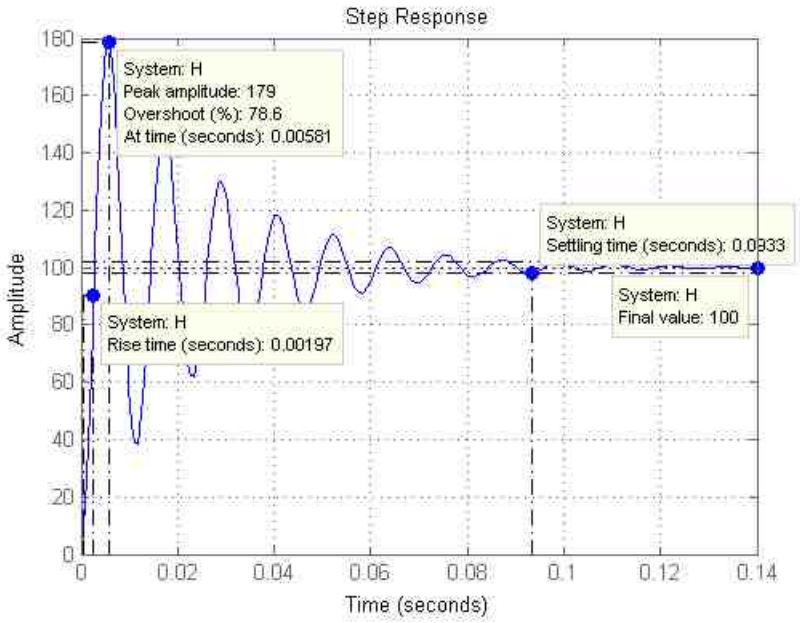

Fig. 3.13. Step Response for Negative Output Voltage

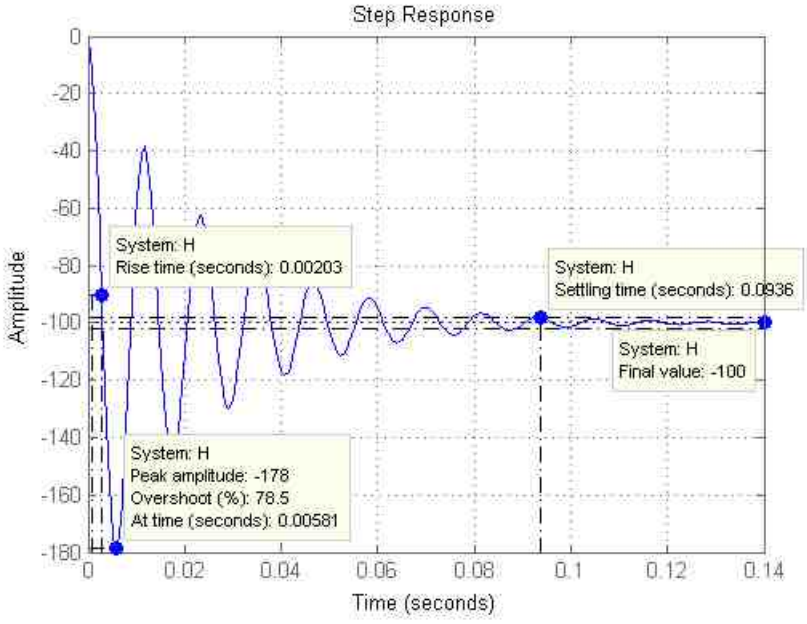

Fig. 3.14. Step Response for Positive Output Voltage

4. PROPOTYPE TESTING

4.1 Components Selection

After the simulation and the analysis have done for the proposed converter, a prototype is looking to be built to validate the results in practical way. Before actually building up and creating a PCB for the converter for validating, making selection for the right components of each element in the circuit according to the sizing calculation and simulation results was supposed to be ensured firstly. The sizing process in section 2.3 has set the boundaries for the size and some critical characteristics, such as maximum switching frequency, peak current and breakdown voltage, of each kind of component, and the simulation results showed in section 2.5 and 4.3 would also give a prediction for the performance of these components while operating with a certain size of component. Through following the guidance of the sizing process, the items can be selected within the proper range and to best fit with the predicted performance.

As the only switching device in the converter which taking charge in controlling the converter, the selection of MOSFET Q needed to be carefully considered. According to the sizing process, the MOSFET need to withstand a peak current of 29.8A for the positive peak and a peak current of 45.15A for the negative peak. So the drain-to-source current rating in the normal temperature of the MOSFET should be larger than 45.15A. On the other hand, according to the expectation of the voltage across the MOSFET, the peak voltage can be calculated as the sum of source voltage, load voltage, and forward voltage of the diode D_1, which equals 204.4V in total. So, the MOSFET should also has a maximum voltage rating larger than 204.4V. The MOSFET that is applied in this prototype building is IXFH60N50P3. Reference to its data sheet, the MOSFET has a maximum current rating and voltage rating

of 60A and 500V, which definitely larger than 45.15A and 204.4V. By observing the simulation results, the current peak is obviously within the range that allow the MOSFET to operate safely, so there is no need for any type of snubber circuit in order to protect the MOSFET. However, since the peak current is able to reach 45.15A, which is large enough to create a lot of heat, a heat sink and fan is assembled with the MOSFET and attached in the back of it to reduce the heat and avoid overheat.

Beside the MOSFET, diode is the other active component that take control of the converter. Selecting a correct diode for the converter can actually increase the system stability and efficiency of the voltage conversion. While doing the sizing for the diode, the two characteristics that have been focused were the peak current and reverse voltage. For the positive peak, the peak current and reverse voltage are as same as those for the MOSFET, which equal 29.8A and 204.4V. And as for the negative peak, the peak current and reverse voltage are smaller than positive peak, therefore, 29.8A and 204.4V are going to be used in selecting the suitable item. The diode that is selected to mount in the converter is 10A10 silicon diode with voltage rating from 50V to 1000V. Obviously, the voltage rating is large enough to ensure the converter working properly. However, on the other hand, the current rating of this diode is only 10A. Comparing with 29.8A, the current rating is too small to for the diode to perform it function, in this reason, 4 diodes are series connected together to prevent the overshoot current of the diode. 4 diodes are used is because the diode current may exist ripples, therefore, with one more diode series connected, it gives more rooms for the current ripple and ensure the safety and stability of the system.

The type of capacitor used in the converter is the oval run oil-filled capacitor. This type of capacitor is able to operate in a wild range of temperature between -40°C to 85°C, and has large voltage and current rating. While considering the converter may generate lots of heat and operate with large current, this type of capacitor has its comparative advantage comparing with the other type of capacitors and provide stability and reliability in the prototype building.

One of the other elements that play a big role in the proposed converter is inductor. The inductor in this converter is carefully designed and needs to satisfy some special requirement in order to allow the converter to generate the demanded output on the load. In this reason, in order to produce the best the results for the converter, the inductors need to be designed and built according to the requirements. How to design and build a suitable inductor to satisfy the desired qualities is going to be comprehensively introduced in the next section.

4.2 Inductor Manufacturing

Since the inductors in this converter is required to be designed in order to satisfy the need, the inductor could not be simply buy from the website. Those inductors would be designed and made according to the requirements. In this part, how a suitable inductor has been designed and produced will be introduced in this section.

According to the simulation introduced in the last section, the best selection of the inductor is $307\mu H$ for both of inductor L_1 and L_2. Reference to section 4.3, the simulation of the Simulink model has given the maximum of the inductor current that equals to 30A. So the designed inductors has to be able to allow the maximum current of 30A to pass through.

Before start designing the inductor, type of the inductor that is best fit for the requirement should be selected. The total types of inductors including pot core, RM core, E core, EC core, ETD core, EER core, PQ core, EP core, and toroidal core. Table 4.1 below lists all the consideration factors for all type of inductors.

Table 4.1
Considerations for Core Selection I

Type	**Pot**	**RM**	**E**	**EC, ET, EER**
Core Cost	High	High	Low	Medium
Bobbin Cost	Low	Low	Low	Medium
Winding Cost	Low	Low	Low	Low
W. Flexibility	Good	Good	Excellent	Excellent
Assembly	Simple	Simple	Simple	Medium
Mounting	Good	Good	Good	Fair
Heat Dissipation	Poor	Good	Excellent	Good
Shielding	Excellent	Good	Poor	Poor

Table 4.2
Considerations for Core Selection II

Type	**PQ**	**EP**	**Toroidal**
Core Cost	High	Medium	Very Low
Bobbin Cost	High	High	None
Winding Cost	Low	Low	High
W. Flexibility	Good	Good	Fair
Assembly	Simple	Simple	None
Mounting	Fair	Good	Poor
Heat Dissipation	Good	Poor	Good
Shielding	Fair	Excellent	Good

By considering the cost, heat dissipation, and shielding, the toroidal inductor is the type of inductor that fits the best with the proposed converter design. To design a single-layer toroid, the expression of the inductance is showed below:

$$L = \frac{\mu_e N^2 A_e}{I_e} = N^2 A_L \tag{76}$$

$$N = \sqrt{\frac{L}{A_L}} \tag{77}$$

Where μ_e denotes the flux density, N denotes number of turns, A_L denotes the inductance factor, A_e denotes the cross sectional area, and I_e denotes the average path length. Inductance factor A_L usually presents the inductance per turn or per square turn. It is generally provided by the manufacturer of the ferrite cores as one of the characteristic of the given magnetic core and the unit is $\frac{nH}{turn^2}$. If inductance factor A_L is given for the given core, the number of turns that is needed for creating an inductor with a certain inductance can be calculated using equation (76). However, before the calculation is able to be performed, there are many different sizes of ferrite toroidal core to be selected from. In order to choose the right core for creating the desired inductor, the sizing process for the core has to be done. The magnet wire that is using in creating the inductor has 22 AWG wire gauge. Due to the maximum current for 22 AWG is only 7A, 3 wires were wrapped together to create a wire with larger ampacity, which was able to allow a maximum 20A input current. On the other hand, by wrapping the wires together, the parasitic resistor of the inductor was reduced, which also reduce the power loss on the parasitic resistor. Since the maximum current has to satisfy the requirement to make sure the flux density is below some specified maximum, I_Max has to satisfy the following relationship:

$$I_{Max} \leq \frac{NB_{Max}A_e}{L} \tag{78}$$

$$A_e \geq \frac{LI_Max}{NB_{Max}} \tag{79}$$

By modifying the formula of equation (78), the area of the crossing section for the core can be sized as equation (79). On the other hand, due to the proposed inductor is created with single layer of magnet wire. The number of turns will also be limited by the inner diameter of the core and the size of the wire. Figure 4.1 and 4.2 demonstrates the dimensions of a toroidal core and magnet wire. $I.D.$ and $O.D.$

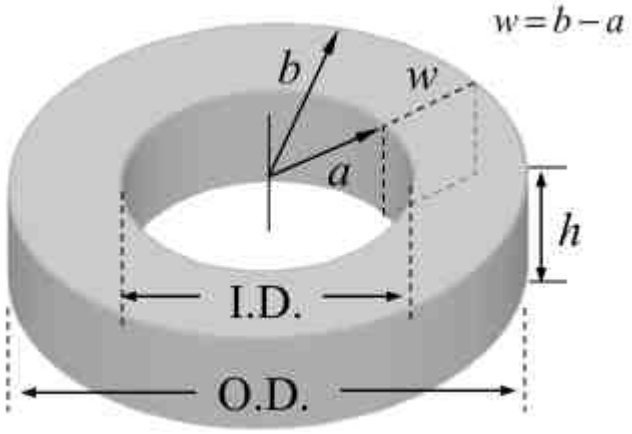

Fig. 4.1. Dimensions of toroidal core

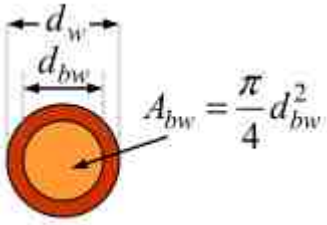

Fig. 4.2. Dimensions of magnet wire

denote the inner and outer diameter of the toroidal core, and a and b denote the inner and outer radius of the toroidal core. w denotes the width of the cross section, and h denotes the height of the core. As for the dimensions for the magnet wire, A_{bw}denotes the area for bare wire, d_{bw}denotes the diameter for the wire without insulation, and

d_{wd}enotes the diameter of the wire with insulation. The Number of turns is identified by the inner diameter and wire size of the magnet wire as expressed in equation (80).

$$Nd_w \leq 2\pi a \tag{80}$$

Since a is the inner radius of the toroidal core, it equals to half of the inner diameter $I.D.$ Therefore, equation (80) can be modified as:

$$I.D. \geq \frac{Nd_w}{\pi} \tag{81}$$

While comparing both of the equation (78) and (80), both of the equations expressed one of the critical dimensions of the correct core and contain a unknown value N in the expression. However, by multiple the area with the diameter, the unknown V will be canceled and a product will be given as:

$$A_e \times I.D. \geq \frac{Ld_w I_{Max}}{\pi B_{Max}} \tag{82}$$

The product of the cross sectional area and the inner diameter of the toroidal core can be used as the guidance in selecting the correct core for the toroid. The inductance of the desired inductor was $307\mu H$, the peak current was 24A, $B_{Max}$was assumed to be 0.3T, and the diameter of the wire is 0.644mm. Bring the values into the equation (81), the criteria value can be calculated as 510-6. The dimension of the chosen toroidal core gives the inner diameter equaled to 30mm, outer dimeter equaled 50mm, and the height equaled 20mm. The product between the cross sectional area A_e and inner diameter $I.D.$ equaled 610-6. This value satisfied the sizing criteria, which means it is the correct core for creating the inductor. The inductance factor $A_L$that had given for the selected core was 1400 nH, so that the number of turns N can be calculated as:

$$N = \sqrt{\frac{30710^{-6}}{140010^{-9}}} = 14.8turns \approx 15turns \tag{83}$$

Since the number of turns can only be an integer, the number of turns should be counted as 15 turns. Therefore, by creating a toroidal inductor with 15 turns of wire, the inductance equals $307\mu H$.

4.3 Experimental Verification

Experimental setup is utilized to validate the operation of the circuit as a comparison with the computer simulations. The prototype is tested and the output and each elements in the circuit are closely monitored. The load of the converter is parallel connected with an oscilloscope. Considering the current is possible to go extremely high and even go over 20A for some situation, high current probes are utilized to do the measurements. The first channel of the oscilloscope connected to the load and measuring the output voltage. Channel 3 and 4 are connected to two high current probes while measuring the current of source and load, inductors (including inductor L_1 and L_2), diode D_1 and D_2, and transistor Q. When measuring the voltage for capacitor C_1 and diode D_1 and D_2, Channel 3 and 4 are connected with two high voltage probes. To measure the voltage, channel 3 and channel4 are connected to the two ends of the capacitor or the diode, the measurement will be performed by doing the subtraction between these two channels using the math function on the oscilloscope. Oscilloscope give the reading of the mean value for each of the parameter. Corresponding to the simulation results, the experiment validation will still focus on those three output situations: $\pm$170V, $\pm$60V, and $\pm$30V. For the results of other output voltages, they will be given in the Appendix to show that the converter is not only worked for some certain conditions, and the proposed converter has the ability to produce the matching results for any voltage level of output voltage.

A. Experiment Results of Positive Output Voltage

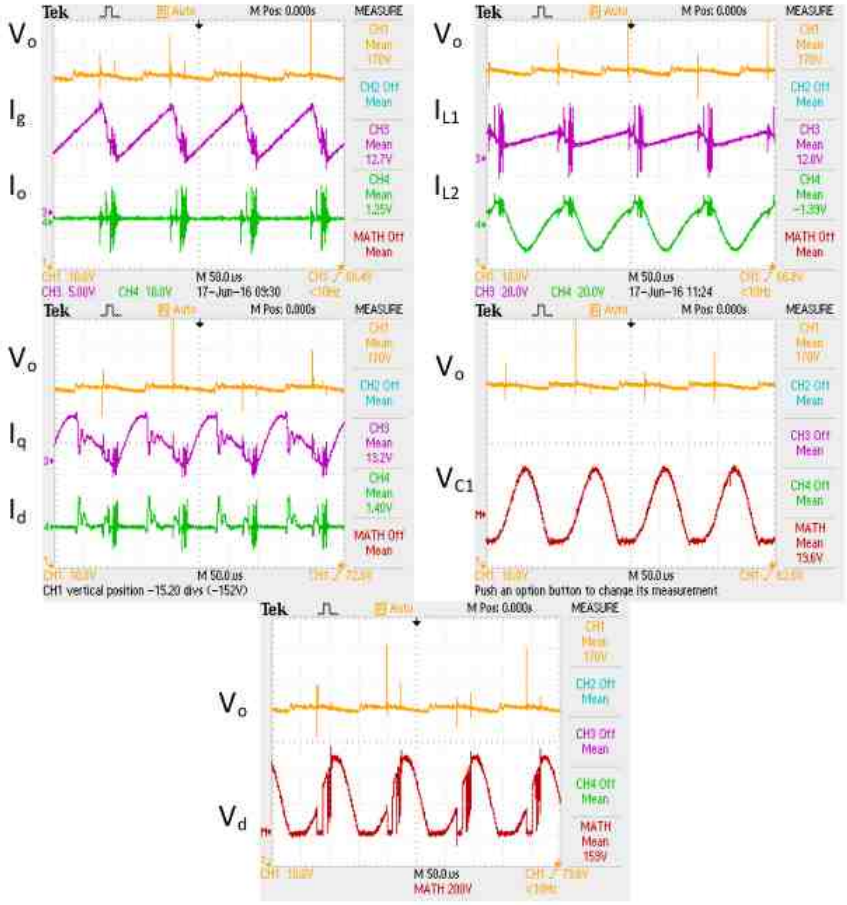

Fig. 4.3. Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode (170V).

The prototype generate 170V output when the MOSFET is driving at 8.3 kHz with duty cycle of 80.4%. The duty cycle for the simulation model to generate the same load voltage is 79.5%, they are very close. The power transmission rate of the converter can be calculated as $\frac{V_o I_o}{V_{in} I_{L1}} = \frac{170V \times 1.25A}{30V \times 12.7A} = \frac{212.5W}{381W} = 55.77\%$. The efficiency is similar to the one it has been expected in simulation. While looking into the currents, just like what happened for the simulation results, the input side currents,

including I_g, I_{L_1}, and I_q, are large and have a similar mean value around 13A, and the output side current, including I_o, I_{L_2}, and I_d, are small with a similar mean value around 1.3A. Comparing with the simulation results, the simulation result for 170V load voltage has the input side current equal to about 11.4A and output side current equals to around 1.13A. Consider the ripples of the experiment results and the error cause by the measurement devices, such as oscilloscope and current probes, the difference around 1A between the simulation result and the Experiment result is acceptable and the experiment results for the currents are very close to the result generated by the simulation model. Both result are considered to be match with each other.

As for the voltages, the waveform of the voltage is coincided with the expectation, but the mean value for the capacitor C_1 voltage only equals to 19.6V. According to analysis, the voltage of capacitor C_1 is supposed to equal to the source voltage ideally. In the simulation, the result of capacitor voltage equals 28.03V, even if it is not equaled to 30V, it still very close to 30V. Comparing the experiment result with the simulation result, the experiment result is too small for diode voltage. However, if observing the waveform between the experiment result and simulation result in the following section, the waveform seems pretty much the same and have not much difference. Therefore, to explain why the reading of the mean value of the voltage for capacitor C_1 is much smaller than expectation, the problem can be considered in the following three aspects: First of all, the mean value measurement for the oscilloscope will be affected by the scale of the display. With a larger scaler, the mean value measured for the waveform will be more inaccurate and the estimated value for the mean will be normally smaller than its actual value. The scale for the voltage across capacitor C_1 is 200V, so the scale is too large regarding the capacitor voltage. Secondary, while the proposed converter was operating under this situation, the input current was large, which is 12.7A. While this large current was flowing through the prototype, it generated lots of heat on each element due to the parasitic resistor. When those electronic elements are heated to a high temperature, the resistance of

the parasitic resistors will increased along with the temperature. With larger parasitic resistance, more voltage from source will be separated to the parasitic resistors and the voltage on capacitor C_1 will be reduced. Thirdly, many ripples were lies at the bottom part of the waveform. These ripples could also be concerned as a factor that leads the reading of the mean value to be smaller than it supposed to be. As showed in Figure 4.3, the ripples of the capacitor C_1 voltage were basically concentrated at the bottom of the waveform, and this may lower the estimation of the average value for the output voltage.

Similar to voltage of capacitor C_1, the voltage across diode D_1 is also much smaller than what it supposed to be. In simulation and mathematical analysis, the mean value of the diode D_1 is supposed to be equaled to the output voltage, however, it equals 159V and it is 11V less than 170V. The reason that may cause this difference can also be explained by the three issues listed above.

The second sample of the experiment result is where output voltage V_o is equaled to 60V. While the MOSFET was operating at 8.3 kHz with duty cycle of 33.5%,

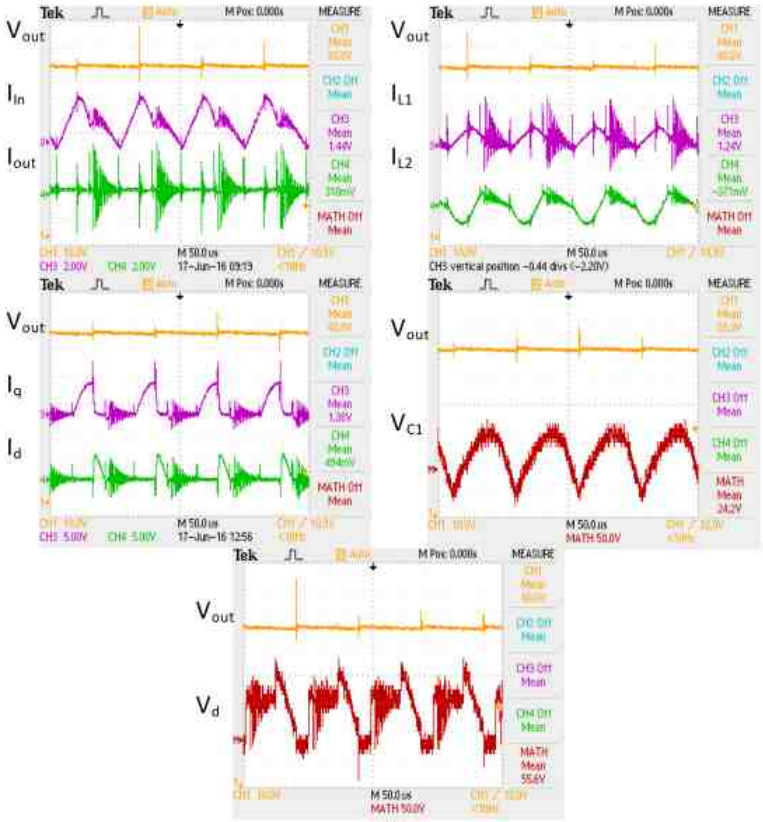

Fig. 4.4. Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode (60V).

the output voltage of the prototype equaled 60V. The conversion efficiency can be calculated as $\frac{V_o I_o}{V_{in} I_{L1}} = \frac{60V \times 0.318A}{30V \times 0.44A} = \frac{19.08W}{43.2W} = 44.17\%$. Comparing with the simulation result, this efficiency was much lower than it was expected. The reason that caused the difference was that the current measurements were not as same as the expectation. The input current equaled 1.44A, which was larger than 1.061A for the simulation result, and the output current was 0.318A, which was smaller than 0.4004A for the simulation result. This difference could also be explained by the three issue mentioned in the last example. Comparing the shape of the waveforms to the expectation shape

shown by figure 2.2 in section 2.2, the waveform has the same shape as expectation, even if there are lots of noise in the experiment results. When the duty cycle of the

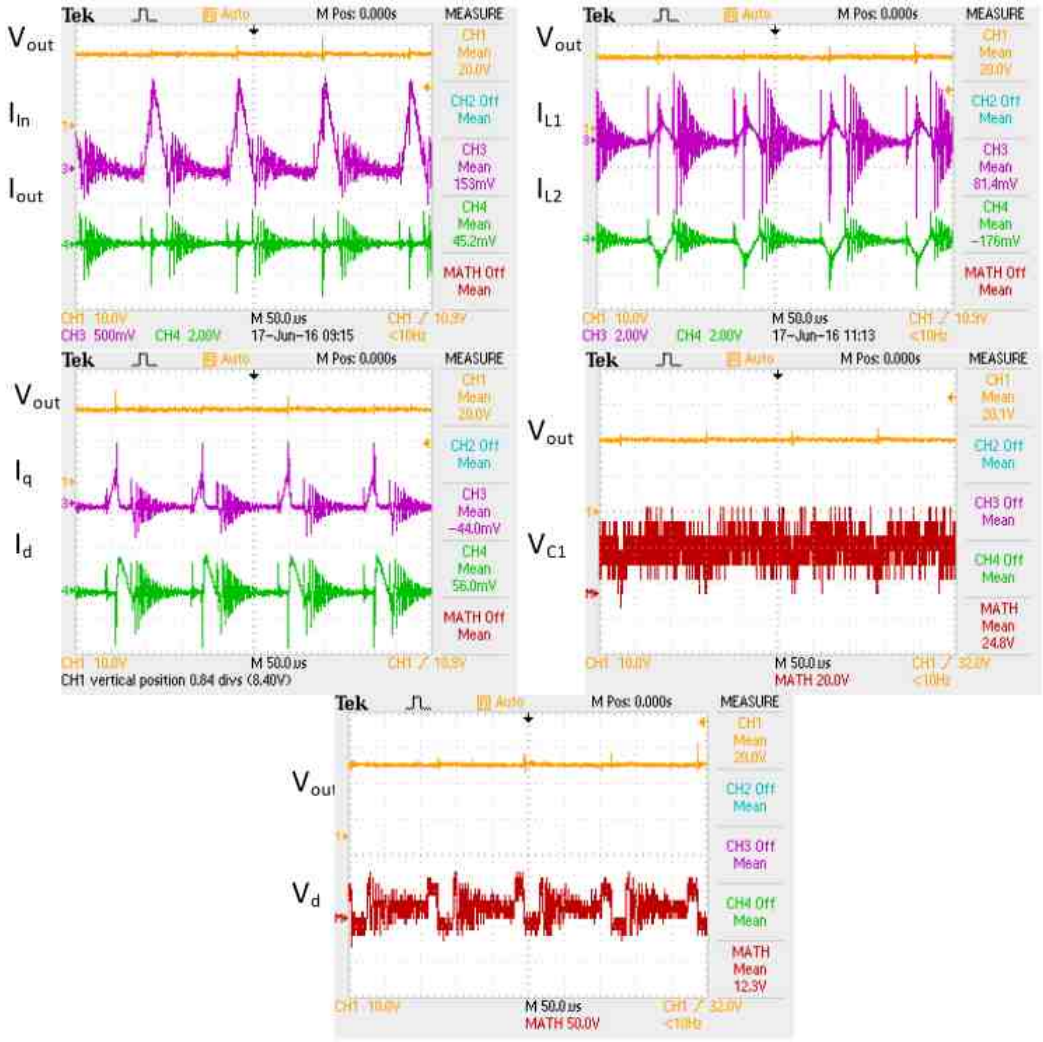

Fig. 4.5. Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive buck mode.

MOSFET is set to 11.4% with 8.3 kHz switching frequency, the proposed converter is operating in a buck mode and generate 20V voltage on the output load. The duty cycle for the simulation model to generate the same level of load voltage is 10.3%, they are very close. While computing the power transmission rate of the converter, the

data of the input and output current are generally used. However, as it can be noticed, comparing with the value of inductors current I_{L_2} and the result from simulation, the measured output voltage is too small as it supposed to be. The measurement error existing at the output current is considered to be caused by the noise of the waveform and the limitation of the oscilloscope for current measurement. Since the inductors current I_{L_2} is also equaled to output current, and at the same time, it is much closer to the simulation result of the output current, thus the power transmission rate can be calculated as $\frac{V_o I_o}{V_{in} I_{L1}} = \frac{20V \times 0.176A}{30V \times 0.153A} = \frac{3.52W}{4.59W} = 76.69\%$. Besides, the other data is close enough to the simulation and the waveform are in the expected shape.

B. Experiment Results of Positive Output Voltage

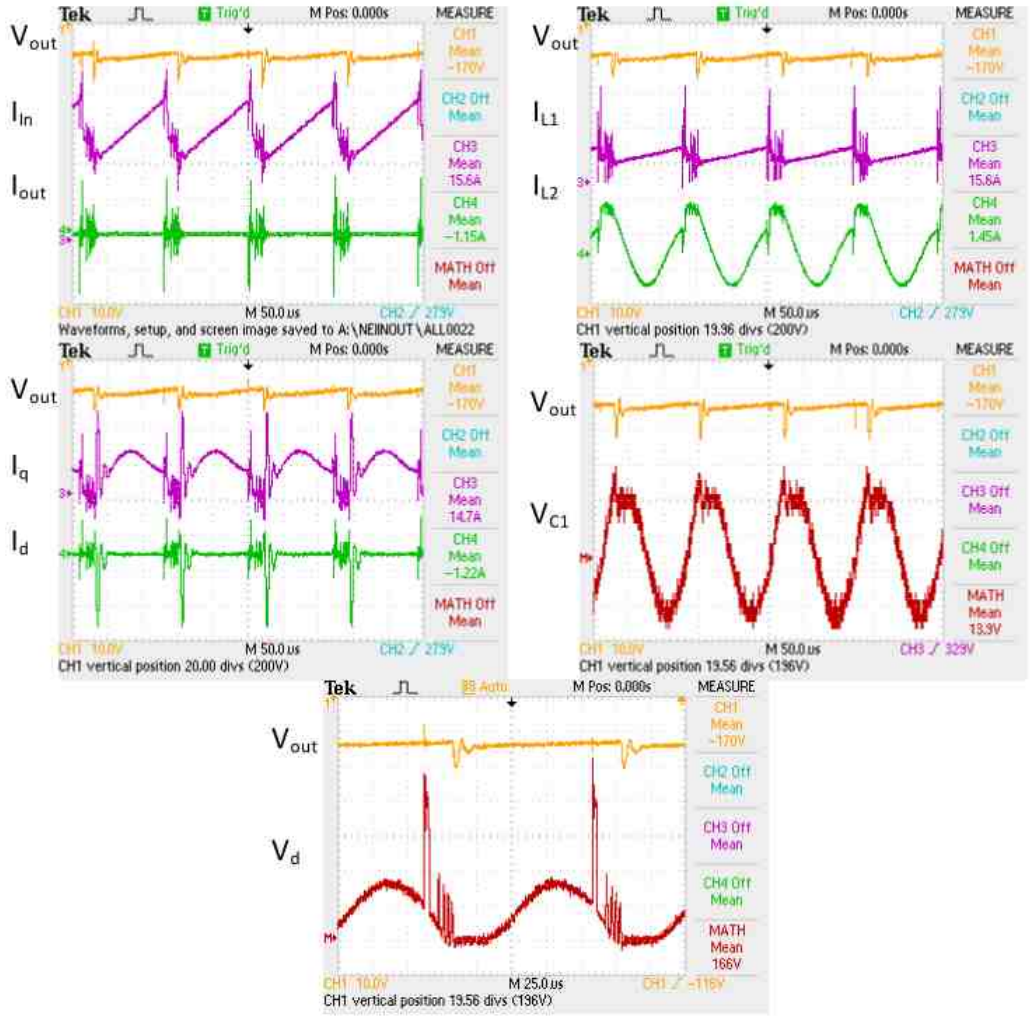

Fig. 4.6. Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for negative boost mode (-170V).

This result demonstrate the performance of the converter working in the negative mode. As expected in the previous section, the waveform that is changed after changing the direction of the diode and the polarity of the output voltage is inductor L_2 current and the voltage across the diode. Except these two characteristics, the rest of the elements remain the same shape, however, some of the readings still change their

polarity along with the output voltage, such as output current and diode current. The experiment result has matched with the expectation and showed the correctness of the expectation.

The readings of the experiments result are much closed to the simulation result, but while looking at the input side current, they can be found much larger than the simulation results and the voltage C_1 is much smaller than it in the simulation result. However, these are the same problems this converter has met for the positive peak, and these problem can be explain by those three main reasons, including measurement tools limitation, parasitic resistor, and large ripple. The power transmission rate is equaled to $\frac{V_o I_o}{V_{in} I_{L1}} = \frac{-170V \times -1.15A}{30V \times 15.6A} = \frac{195.5W}{468W} = 41.77\%$.

In this situation, the converter is working at a boost mode in negative mode, which step up the source voltage to twice of it in negative direction. The duty cycle is -

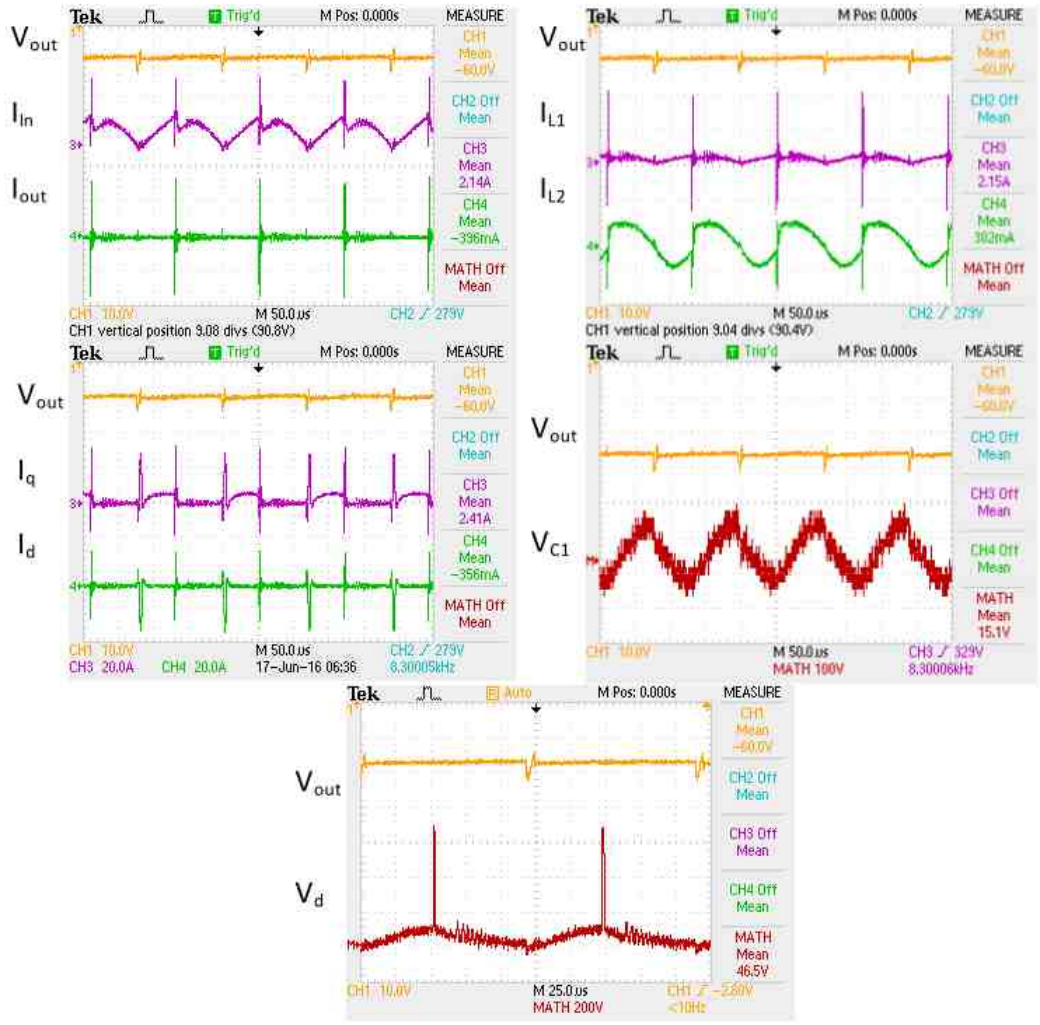

Fig. 4.7. Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode (-60V).

44.5%, and the output voltage is -60V. The shape of the waves still matched with the expectations with close mean values. The power transmission rate can be computed as: $\frac{V_o I_o}{V_{in} I_{L1}} = \frac{-60V \times -0.396A}{30V \times 2.14A} = \frac{23.76W}{64.2W} = 37.01\%$.

In this situation, the converter is working at a buck mode in negative mode, which step down the 30V source voltage to -20V. The duty cycle is -1.8%. The shape of

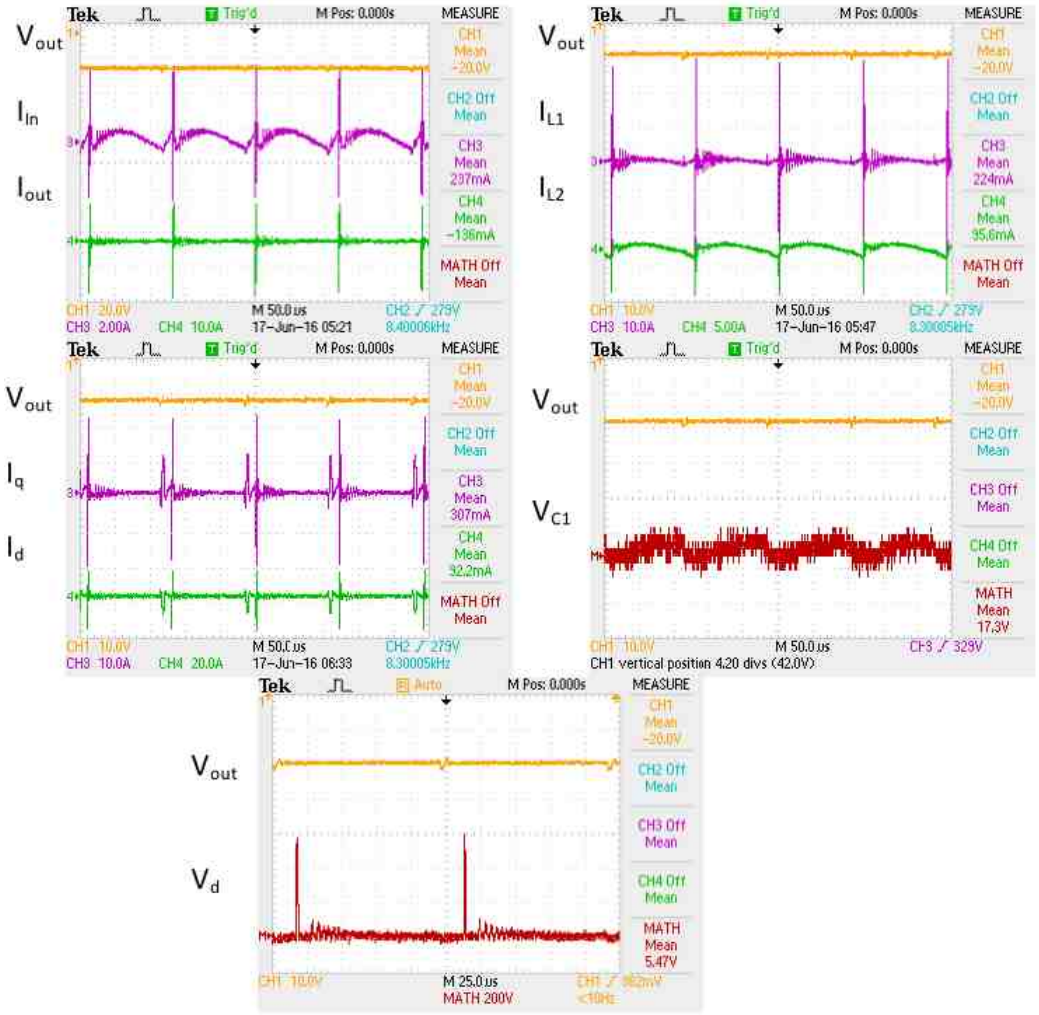

Fig. 4.8. Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive buck mode.

the waves still matched with the expectations with close mean values. The power transmission rate can be computed as: $\frac{V_o I_o}{V_{in} I_{L1}} = \frac{-20V \times -0.136A}{30V \times 0.237A} = \frac{2.72W}{7.11W} = 38.26\%$.

The comparison between the simulation results and experiment results are shown in Figure 4.9-4.14. The figures shown below demonstrate the comparisons of the eight

key measurement data, including Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current Id, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d.

C. Positive Output for Simulation vs Experiment

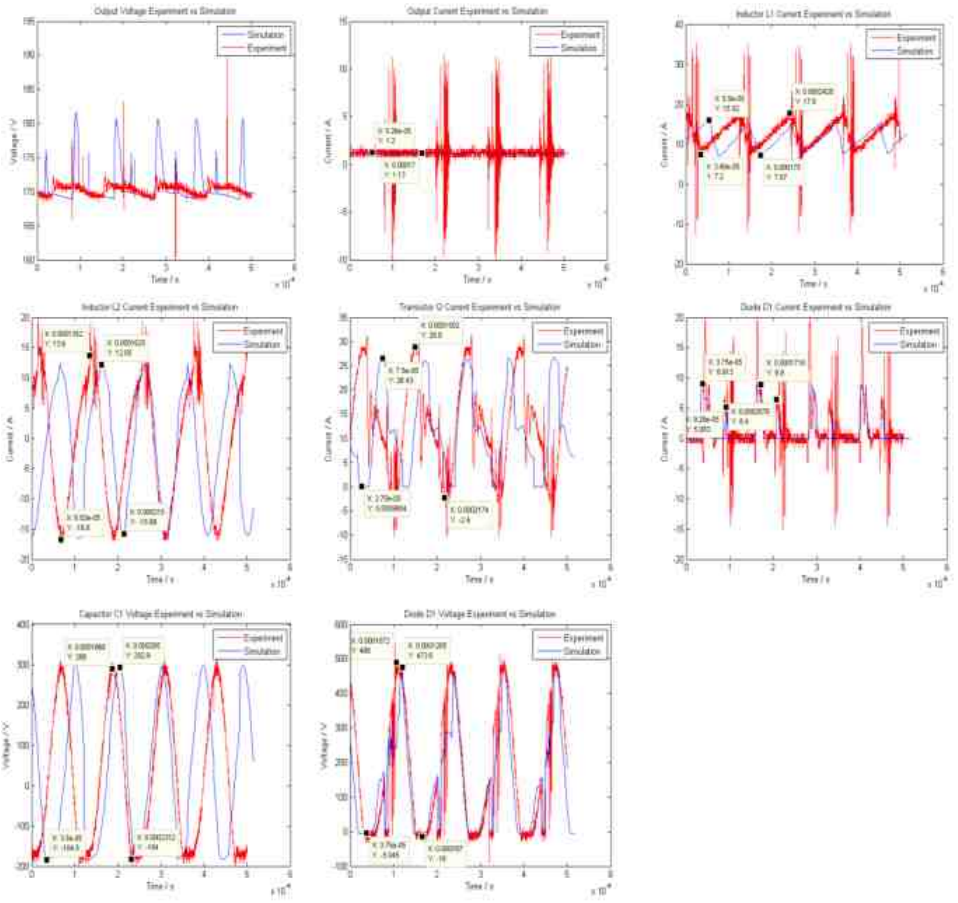

Fig. 4.9. Comparison of Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode (170V).

When the diode is conducted in forward direction, the converter is operating in positive mode and generate positive output voltage at the load. Once the converter is working in the positive mode, it work just like a normal SEPIC converter. Make

comparison between the simulation and experiment results, the waveform of the eight critical elements are basically matched with each other. Except output voltage V_o and current of inductor L_1, I_{L_1}, the results for other currents and voltages are pretty much showed in a matched waveform. They usually have close peak values and same shape.

As for the output voltage V_o, the main body of the waveform are coincided. The difference is the voltage ripples. The simulation result has a large ripple but the experiment result does not. However, while looking closely to the experiment output wave, some voltage ripples are still able to be identified. Even if those ripples are thinner than the simulation result, they have the same timing. And this can prove that the experiment result for the output voltage is actually matched with the simulation result.

And for the inductor current I_{L_1}, the previous experiment result has showed the actual input side current is usually larger than the simulation result, so it is normally to have the experiment result larger than the simulation.

The second sample give a comparison between the experiment result and simulation result where output voltage V_o is equaled to 60V. Figure. 4.10 presents another

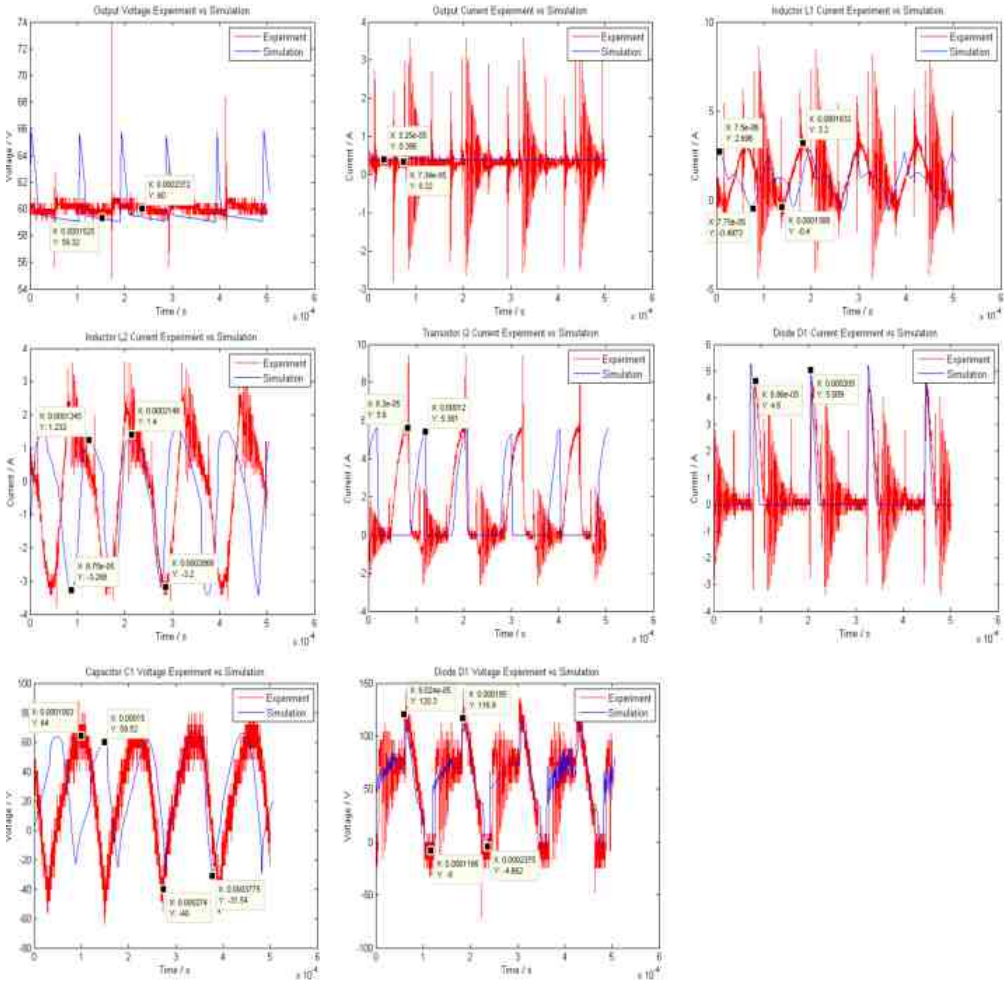

Fig. 4.10. Comparison of Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive boost mode (60V).

example of the converter working in the boost mode. Comparing with the previous condition, the output voltage presented in figure 21B is much smaller and it is only 60V. Similar to what happen in the 170V results, the output voltage has the same characteristic, and they can also be proved to be matched with the same analysis. While only generating 60V at output, the current that is required to finish the boost

conversion is lower than the current for boosting to large output voltage such as 170V. In this reason, less power will be draw from the source and thus less power will be consume in the process of power transmission. Therefore, with less power loss, the experimental result will be more closed to the simulation result, and it explains why the measured experiment inductor current in this situation is not much larger than the simulation result. The comparison of the shape and the critical values both showed the results of simulation and experiment are matched with each other, and prove the prototype is actually working as it is designed.

The following result shows the converters performance while in buck mode for positive peak. Figure 4.11 presents the simulation and experimental results for the

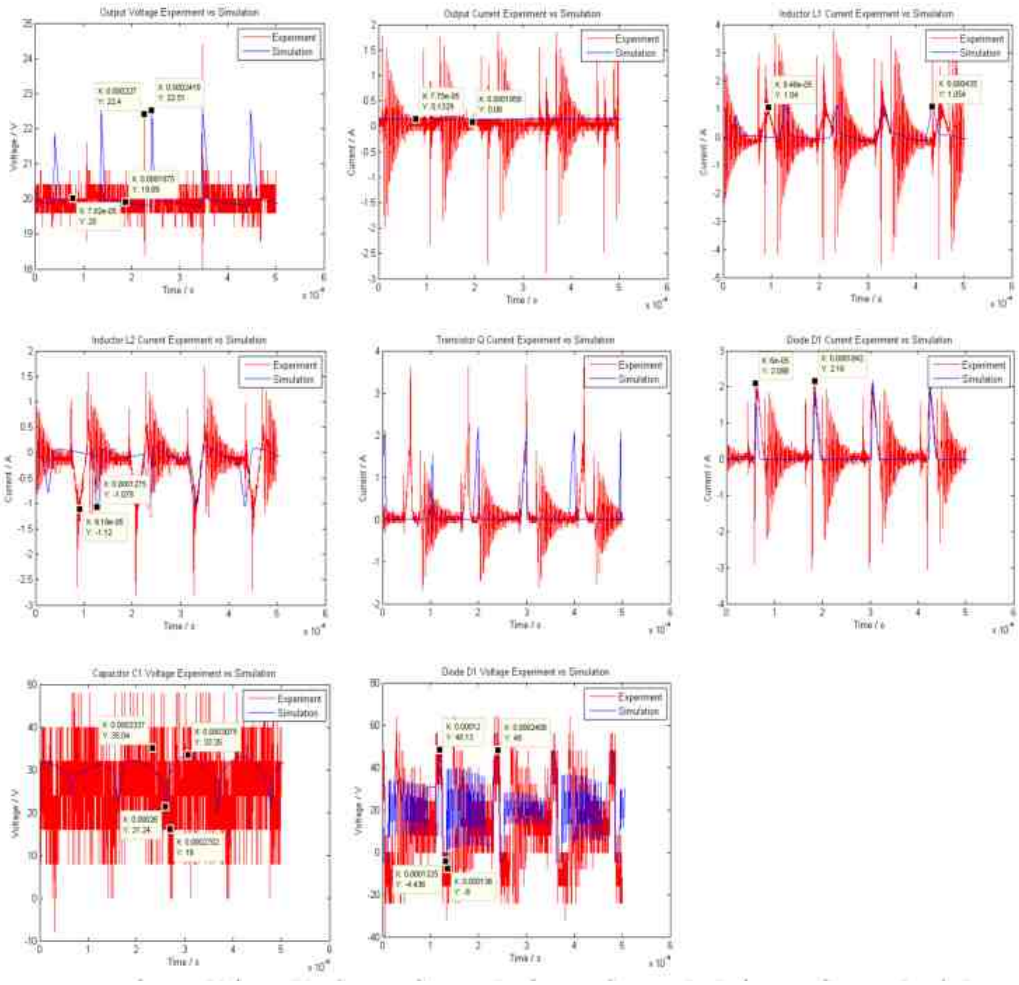

Fig. 4.11. Comparison of Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for positive buck mode.

situation that the simulation model is running at a duty cycle of -10.3% and the practical experiment is operating with duty cycle equals to -11.4%. In this situation, the converter is operating in a Buck mode, and steps down the input voltage from 30V to 20V. The simulation result of the output voltage is basically a constant value of -19.89V with some periodic spikes. Although the spike ripples had not the same

shape in the experimental result, some obvious voltage ripple can still be observed at the same timing as the spikes of the simulation result. For the output current, the average simulation result is 0.1329A and the experimental result has a middle value of 0.08A and average value of 0.045A. they are closed but the experiment result is still seemed a little bit lower than the simulation. However, considering the large current ripple of the experiment result, the difference is actually reasonable. The shape of the simulated inductors current are matched with the shape of the experimental result, and the average values are also pretty close. For current that go through diode and transistor, they normally remain 0 and have periodic pulses on them. Both the simulation results and experimental results of them have showed this behaviors and the period of the pulse on the wave is matched. The experiment reading for the voltage of capacitor C_1 looks noisy and it is due to the limitation of the measurement tools. But if taking a close observation to the wave, it is still able to see a similar waveform within the noises.

D. Negative Output for Simulation vs Experiment

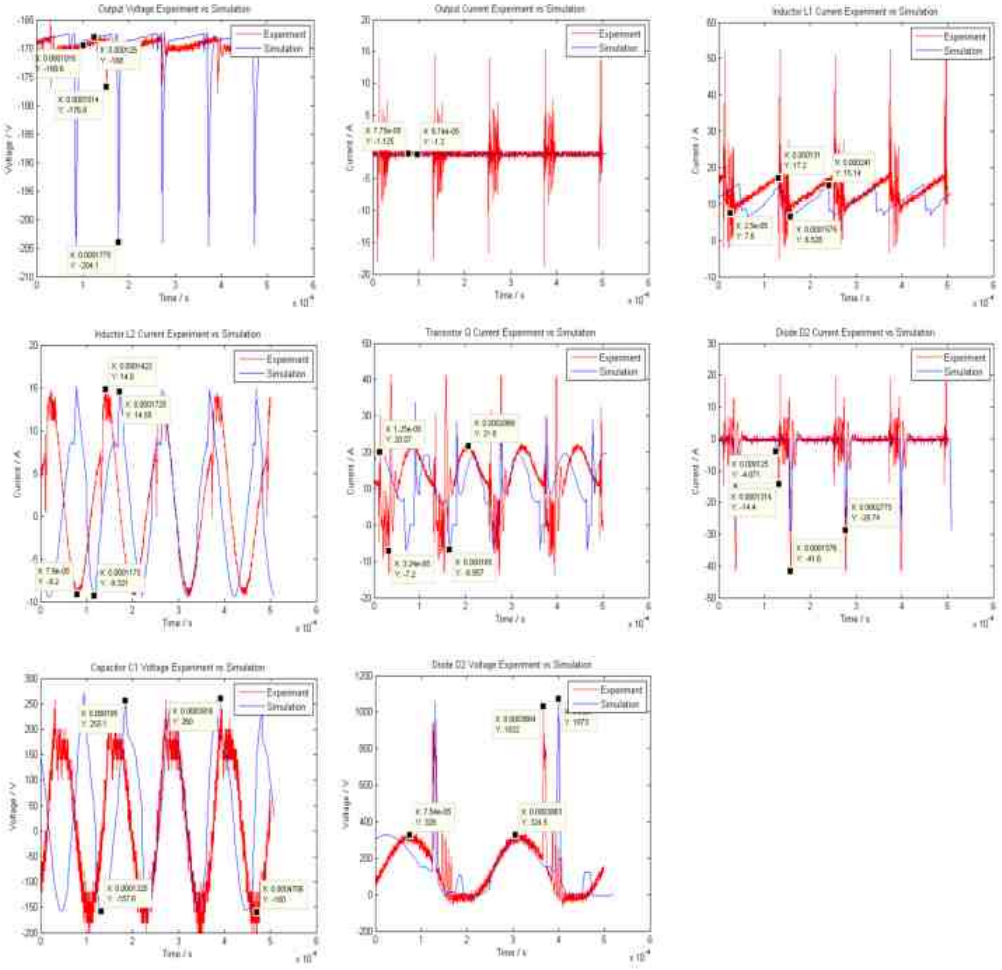

Fig. 4.12. Comparison of Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for negative boost mode (-170V).

Figure 4.12 presented above demonstrates the comparison between simulation result and experiment result of the converter while it is running in the negative mode and the duty cycle of the main switch Q is set to -84.1% for the simulation

and -83.3% for the practical experiment. In this condition, the converter is literally operating in the boost mode and the output voltage is boosted from a 30V input to -170V at output.

The waveform of the output voltage from simulation as seen in the figure is basically a constant value of -168.5V with a periodic ripple which has its peak value equal to -204.1V. As for the result of the practical experiment, the main body of the wave has a middle value of 168V, and the ripple is equaled to 176.8V. Comparing the simulation result with the experimental result of the output voltage, the middle value for the main body of wave are close to each other. Both of the waveform content periodic ripples, and the period of the ripples for simulation result and experimental result are 0.1125ms and 0.125ms. They are also very close. The ripples for both simulation reading and experimental reading are basically occurred at the same time even if the peak voltage ripples are quite different.

The waveform for inductors current are more complicate than the output current. The shapes of the simulation result and experimental result are matched. The waveform of current for each inductor have pretty much the same shape. The average reading of the current for inductor L_1 is 10.81A from simulation and 15.6A from practical experiment. Unlike the other comparison results, the experimental result for $I_{L_1}$is larger than the simulation result. This is due to the power loss for the power transmission in realistic is much larger than what it was expected in simulation. Therefore, the power that need to draw from the power source is larger than the expectation of the simulation. While the resistance stay remains the same, in order to draw more energy from the source, the input current must be larger than expectation. For inductor L_2, the positive peak of current I_{L_2} from the simulation is 14.8A and from the practical experiment is 14.55A. And the negative peak of current I_{L_2} from the simulation is -9.321A and from the practical experiment is -9.2A. These values are very close to each other, which can prove these two results are coincided.

The rest of the elements can be analyzed in the same way, and the waveform of them are well coincided. Those waves usually have the similar critical value regardless the ripples.

The second result in the negative mode shows the performance of the converter while it is generating a -60V output. Figure 4.13 is the comparison result between

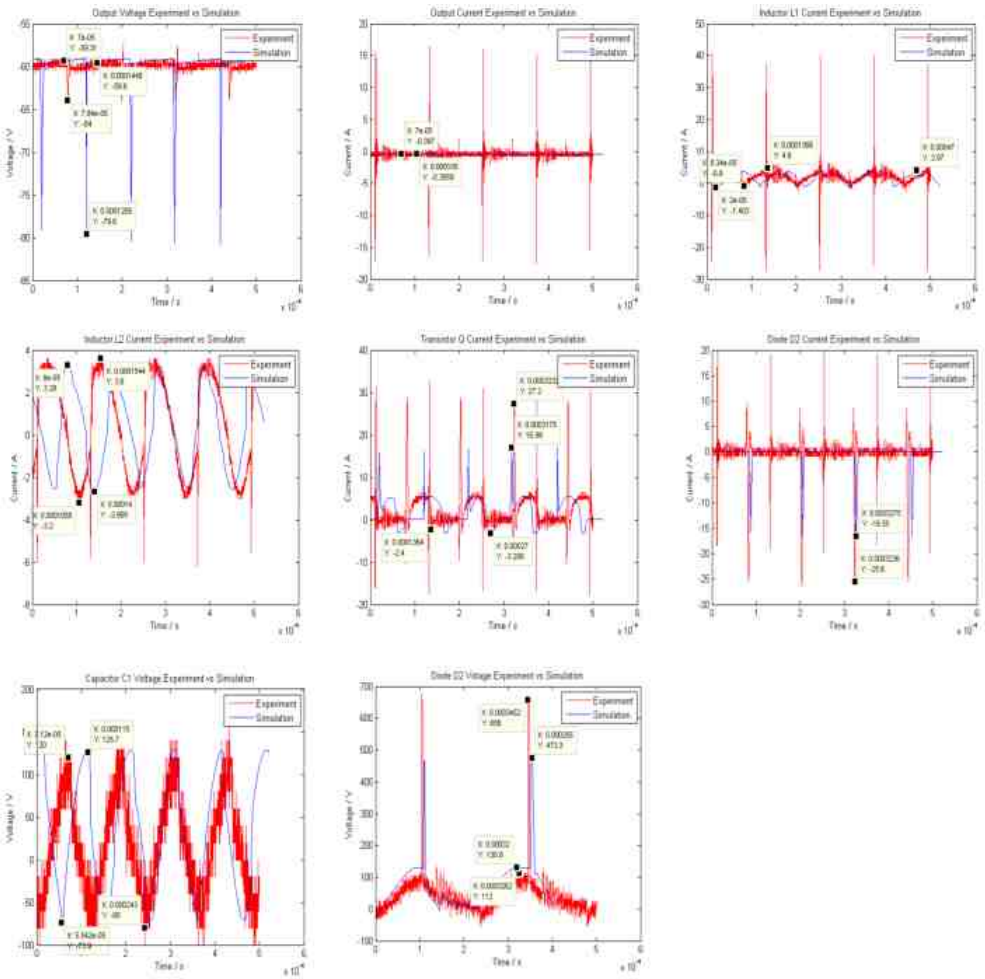

Fig. 4.13. Comparison of Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for negative boost mode (-60V).

the measurements of simulation and practical experiment while the converter is operating in a boost mode. The converter is trying to generate 60V output voltage

with a 30V input while the measurements are undergoing. Observing the figures, the experimental results of the currents and voltage are all have a very similar waveform to the results of simulation with similar critical points.

The results that are obtained separately from simulation and experiment are basically matched, which means the converter is actually worked as expected under this type of situation.

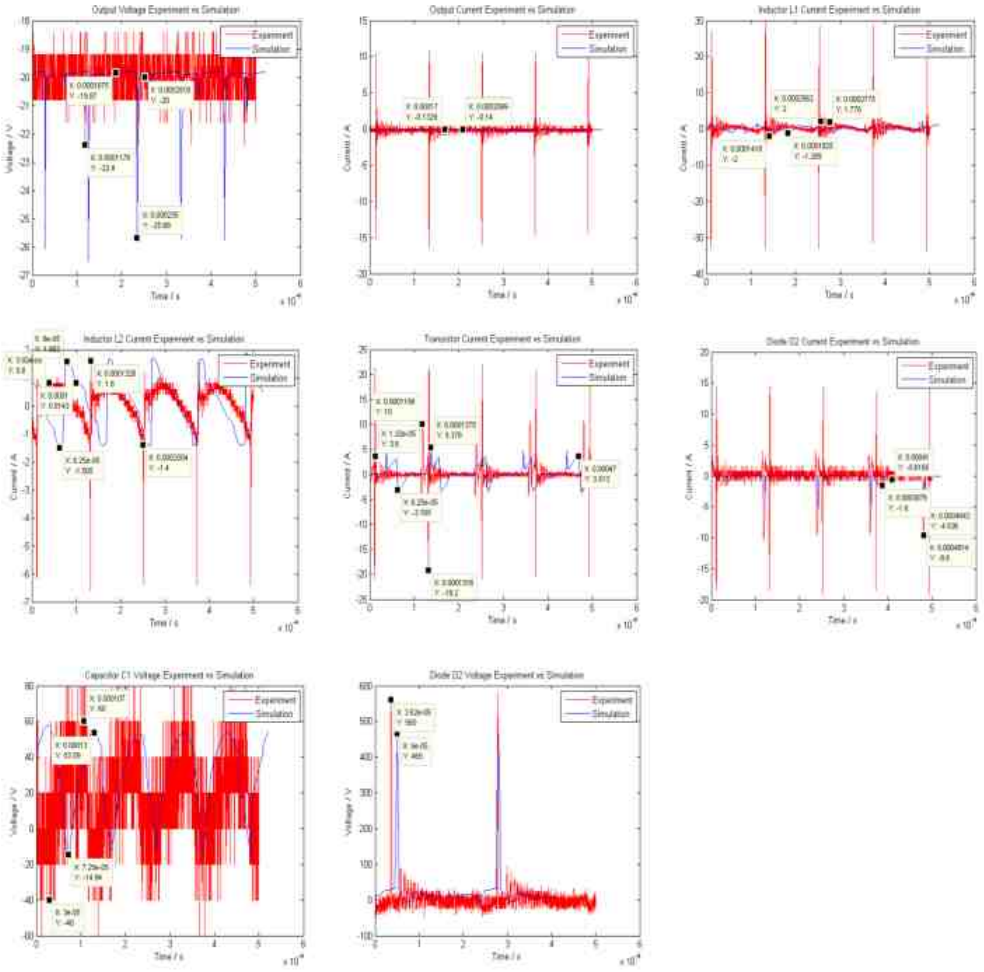

Fig. 4.14. Comparison of Output Voltage V_o, Source Current I_g, Output Current I_o, Inductors Current I_{L_1}&I_{L_2}, Diode Current I_d, Transistor Current I_q, Capacitor C_1 Voltage V_{C_1}, and Diode Voltage V_d for negative buck mode.

Figure 4.14 provides a demonstration of the performance of the proposed converter while it is operating in the buck mode. The 30V input voltage is stepped down to -20 V. As it can be observed in the figure, all the parameters that are measured have showed the coincidence between the experiment result and simulation result. In conclusion, the converter is proven to have the ability to perform the step down operation as it supposed to in its buck mode. The converter is still able to perform its function as expectation in buck mode.

5. SUMMARY

In this research, a new bipolar DC-DC converter has been presented. This converter can boost and buck the supply voltage in a wide range of output voltage and deliver both positive and negative voltages. The converter utilized only one switch to perform the power conversion. Comparing with other bipolar converter topologies high power conversion efficiencies can be achieved. With only one switch to achieve the power conversion, this design mostly simplifies the construction of the gate drive which makes it more suitable to construct in DC motor drives and DC microgrid and apply in many portable electronic devices. A simulation model, mathematical model, and experimental prototype has been developed and subjected to achieve the wide range of output voltage conversion. The simulation and experimental and mathematical results are matched with each other, which have verified the possibility to boost and buck the supply voltage in a range from 0 to $\pm$170V.

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