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A NON-CONVENTIONAL MULTILEVEL FLYING-CAPACITOR CONVERTER TOPOLOGY

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Euzeli Cipriano dos Santos

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Brian King

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A NON-CONVENTIONAL MULTILEVEL FLYING-CAPACITOR CONVERTER TOPOLOGY

A Thesis

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of

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Feyzullah Gulpinar

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This thesis is dedicated to my parents, sisters, brother.

For their endless love, support and encouragement.

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SYMBOLS

V_{dc}	Voltage across a component in the circuits
V_o	Voltage across load
i_o	Current through load
q_x	State of the switch "x"
$\frac{dv}{dt}$	Reflective wave
C	Capacitor
D	Diode
n	Neutral point of a circuit
v^*_{sin}	Reference sine signal for PWM method
v^*_{tx}	Carrier signal "x" for PWM method
v_C	Voltage across capacitor
i_C	Current through capacitor
$3-ph$	Three phase
R	Resistor
L	Inductance

ABBREVIATIONS

DC	Direct Current
AC	Alternating Current
EMC	Electromagnetic Compatibility
GND	Ground
GaN	Gallium Nitride
SiC	Silicon Carbide
PWM	Pulse-Width Modulation
EMI	Electromagnetic Interference
SPWM	Sinusoidal Pulse Width Modulation
SHE-PWM	Selective Harmonic Elimination - Pulse Width Modulation
SVM	Space Vector Modulation
IGBT	Insulated-Gate Bipolar Transistor
HVDC	High-Voltage Direct Current
NPC	Neutral Point Clamped
CMC	Cascaded Multilevel Converter
h-bridge	Half Bridge
PSIM	Power Electronics Simulation Software
DSP	Digital Signal Processor

ABSTRACT

Gulpinar, Feyzullah MSECE, Purdue University, December 2014. A Non-Conventional Multilevel Flying-Capacitor Converter Topology. Major Professor: Euzeli Cipriano dos Santos.

This research proposes state-of-the-art multilevel converter topologies and their modulation strategies, the implementation of a conventional flying-capacitor converter topology up to four-level, and a new four-level flying-capacitor H-Bridge converter configuration. The three phase version of this proposed four-level flying-capacitor H-Bridge converter is given as well in this study. The highlighted advantages of the proposed converter are as following: (1) the same blocking voltage for all switches employed in the configuration, (2) no capacitor midpoint connection is needed, (3) reduced number of passive elements as compared to the conventional solution, (4) reduced total dc source value by comparison with the conventional topology.

The proposed four-level capacitor-clamped H-Bridge converter can be utilized as a multilevel inverter application in an electrified railway system, or in hybrid electric vehicles.

In addition to the implementation of the proposed topology in this research, its experimental setup has been designed to validate the simulation results of the given converter topologies.

1. INTRODUCTION

1.1 Motivation

In many fields of industry, power electronics converters have found acceptance for various operation modes of different applications: the rectifier mode for the electrical energy transformation systems, and the inverter mode for the drive systems of electric machinery. For researchers in the area, to improve some particular issues of each mode is crucial such as reduction in electrical energy losses due to switching of semiconductor devices in rectifier mode, and making the distortions lower for the output waveform and for the input current draw of a converter in inverter mode.

The contribution to the power electronic converter topologies by developing a new one can be considered as the idea behind this thesis study. A new topology was designed in this research; also, a comparison between two converter topologies, the proposed configuration in this research and the conventional solution existed already in the literature, was made in terms of the following variables: the total values of DC sources, blocking voltages and the amount of semiconductor switching devices, and the number of passive circuit elements.

1.2 State-Of-The-Art and Literature Review

Power electronics have been a revolutionary area for electrical engineering because this discipline has always had innovative solutions to electrical power systems technology in its own time. Although there are a lot of definitions of power electronics, a conceptual description summarizes it: power electronics manages and alters the

stream of electrical energy based on a structure which performs the variety of tasks from the consumer devices. The Fig. 1.1 illustrates a block diagram of a power electronics system.

The first implementation of power electronics in practice was used to convert the alternating current (AC) into direct current by the invention of mercury arc rectifiers. Despite the first practical progress in the area, this first generation of power switch and converter had many difficulties (e.g., low rate efficiency); so the silicon-based switches were emerged in the field as a new approach to overcome those drawbacks. After the embracement of the solid-state power electronics or silicon-controlled rectifiers by the researchers and engineers at the beginning of the 1960s, the semiconductor devices have become the unique technology of the power electronics market. Since then, with the excellent activity in circuit topology innovations, the semiconductor power switches have been improved significantly, such as with the invention of Gallium Nitride (GaN) and Silicon Carbide (SiC) semiconductor technologies, by reaching high levels in respect to efficiency and compactness [1–7].

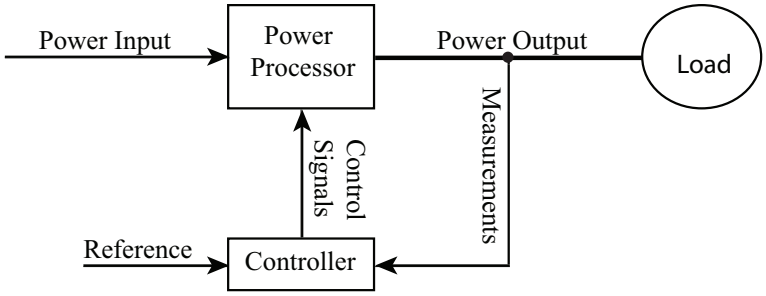


Fig. 1.1. Block diagram of a power electronics system.

1.2.1 Power Electronics Converters

A control circuit for each switch and by connecting the switches to each other, a power conversion system can be basically formed. Accordingly, a power electronic

converter is utilized in a broad range of electrical systems [8]. Some popular applications which include power conversion are itemized below:

- Electric machinery drive systems.
- The electric power generation by using renewable resources.
- Industrial robotics applications.
- Smart grid technologies.
- Electric and hybrid electric vehicles.

Power electronics converter system guarantees making the demands of the user loads fitting optimally to the related grid circuits. Since there are a few forms in electric energy conversion, it can be classified as the type of variables which is shown in Figure 1.2 [9].

A simple power converter can be constituted by some basic circuit elements: a voltage or current source, semiconductor switch, and load. By using the main properties and the characteristics of the power switches, the converter topology can be designed in a range of complexity: from an elementary structure to different desired configurations.

It should be noted that the term converter is appropriated to refer to a power electronics circuit that could perform in two modes of operation: inverter and rectifier modes. As a result, the converter is employed to state general term of this type of power electronics circuits, so all inverter mode configurations studied in this research apply also to rectifier mode [10].

1.2.2 Multilevel Converters

After the switching technology was released in the electrical engineering area, the power electronics converters were needed primarily for the utility applications and the

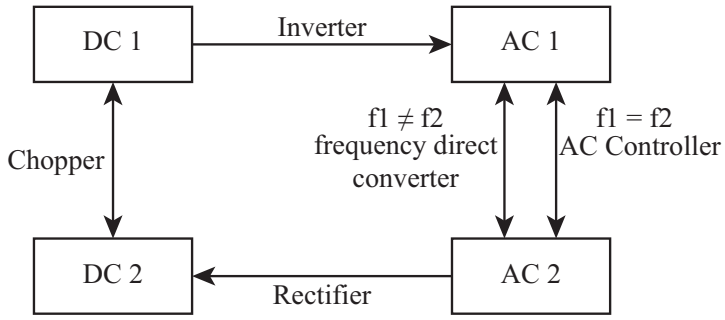


Fig. 1.2. Power Converter classification.

driver technologies of the electromechanical energy conversion systems. For that reason, to generate an AC voltage from a DC voltage, a conventional two-level inverter, which is demonstrated in Figure 1.3, was proposed in the literature. As a solution to the basic inverting demand, that conventional two-level converter is effective, however, it has some disadvantages such as harmonic distortions at the output waveform of the converter, electromagnetic interference, and high $\frac{dv}{dt}$ stresses [11]. Among those negative effects, especially harmonic distortion is a harmful characteristic for all power converter applications due to its nature which causes electrical energy losses in the switches and pulsation torques in the electromechanical conversion system [12]. To reduce mentioned adverse issues of the conventional two-level converters and to improve the efficiency in power converter systems, the idea of multilevel converter arose in the literature by the first usage of it as a new term, which was proposed in [13].

A power semiconductor device allows its switching voltage level to reach up to a specific value. Since some motor drivers and workaday appliances are required to connect to the medium-voltage power networks, the ability of working with higher power systems for a power converter has become necessary. Therefore, for decades, many multilevel converter topologies have been improved in order to perform compatibly those values of voltage levels. In addition to achieving higher power ratings, a multilevel converter empowers the renewable electric energy sources to be plugged into the converter circuits as their main voltage sources. Basically, a multilevel inverter

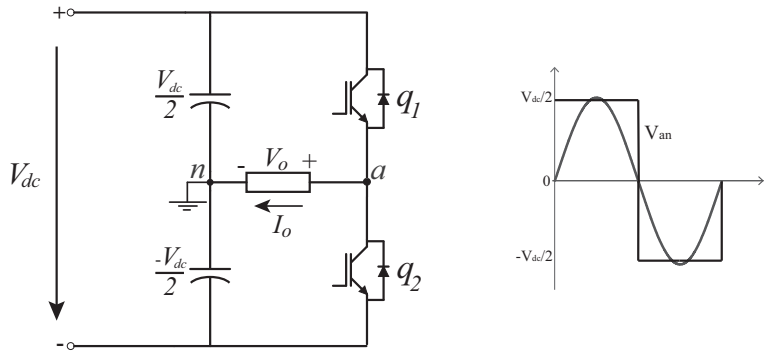


Fig. 1.3. A single phase leg of a conventional two-level converter and its two-level waveform.

reaches the higher level of voltages at its output waveform by the commutation of the power switches which aggregate those numerous voltage sources such as, batteries, photovoltaic arrays, wind turbines, and fuel cells [12, 14, 15].

A multilevel converter's output waveform in a staircase shape is superior to the conventional two-level converters. Beyond that, multilevel converters draw the input current with remarkably low distortion and help electromagnetic compatibility of a power system by generating the output waveform in lower $\frac{dv}{dt}$ rates. Additionally, the stress in the bearings of a motor can be reduced because of the configuration of these types of converters which generate low zero-sequence voltage [12, 14, 16].

In a converter, choosing the switching frequency of a power semiconductor device is critical. Multilevel converters can operate in a broad range of switching frequencies from the fundamental frequency to high switching frequencies. However, operating in the low values of switching frequencies is preferable, because the converter efficiency is better due to lower switching and conduction losses.

Although many multilevel converter configurations have been proposed recently, there are three popular structures among them: diode-clamped (neutral-clamped) [13]; capacitor-clamped (flying capacitors) [17] and cascaded (series) multilevel converter with isolated DC sources [18]. Many of the multilevel converter applications concentrate on some areas of power electronic applications, (e.g., industrial medium-

voltage motor drives [15], utility interface for renewable energy systems [19], the converter which can be connected with an electrical distribution system in both series and parallel manner [20], and electrical vehicle/hybrid electrical vehicle motor drives [21]).

Control circuits, also known as modulation strategies, for the switching technology of semiconductor power electronics devices are essential for all types of converters. Some popular modulation strategies used in multilevel converters are: sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), and space vector modulation (SVM) [22].

Diode-Clamped Multilevel Converter

The first multilevel converter topology in the literature, introduced in 1981 by Nabae et al. [13], basically specified a three-level diode-clamped converter topology, also called neutral-point clamped. After that, the topology was modified to extend the output waveform levels of diode-clamped converters up to six-level. Since then, they have been utilized in some industrial implementations such as static var compensator, variable-frequency motor drivers, and high-power electric systems [23–31].

A three-level diode-clamped multilevel inverter is represented in Fig. 1.4. It is named diode-clamped, because the conduction of the diodes, D_1 and D_2, confines the voltage across the power switches. Those diodes make this multilevel configuration different from the conventional two-level inverter. The operation of the converter topology is comprehensible from the Fig. 1.4. The task of the DC-link capacitors, C_1 and C_2, is to split the voltage of total DC sources into three levels. The load is connected to between point a and neutral point, n. By taking all possibilities of switching states into consideration as shown in Table 1.1, it can be seen that the output voltage consists of three DC voltage levels: $V_{dc}/2$, 0, $-V_{dc}/2$ [32].

Diode-clamped multilevel converters can be executed suitably at the medium AC voltage values, because the blocking voltages of the power switches (e.g., insulated

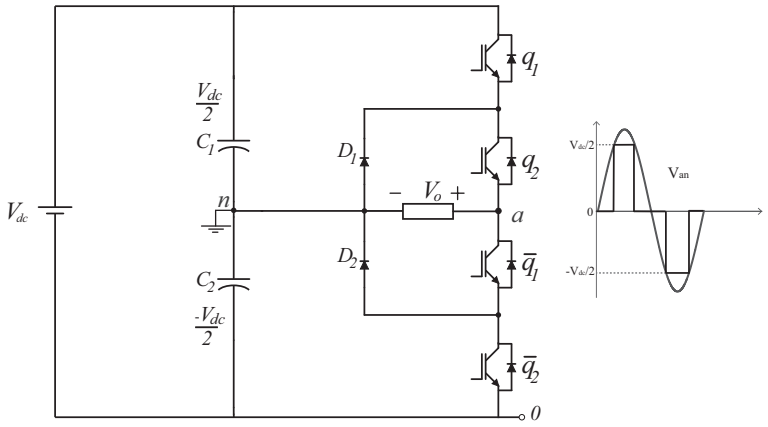


Fig. 1.4. A single phase leg of a three-level diode-clamped converter topology and its three-level output voltage waveform.

gate bipolar transistors) are restricted by the voltage values of the capacitors regardless of the number of levels. However, the output voltage levels greater than five of this type of configuration are not viewed as practical in the intermediate DC voltage values, because, the charging and discharging problems occur in diodes. These problems can be solved by attaching some additional serial diodes array to each diode, but the management of the stress across those diodes should be achieved carefully. Furthermore, the electrical energy losses in each of the power switches raise due to the increase of the number of levels in the same proportion. Fortunately, the power rating expands likewise, so the converter efficiency remains approximately the same [33–35].

Flying-Capacitor Multilevel Converter

A single phase-leg of a three-level capacitor-clamped, or flying-capacitor, multilevel converter is illustrated in Figure 1.5. This type of converter topology was first proposed in 1992. Utilization of the capacitors instead of diodes makes this converter different from the diode-clamped configuration [17].

Table 1.1.
The output voltages based on switching states.

State	$\{q_1\ q_2\}$	v_{an}
1	$\{0\ 0\}$	$-V_{dc}/2$
2	$\{0\ 1\}$	0
3	$\{1\ 0\}$	0
4	$\{1\ 1\}$	$V_{dc}/2$

The flying-capacitor converter operates in a similar manner to the diode-clamped topology; its output voltage values can be seen also in Table 1.1. In this kind of converter topology, the flying capacitors are charged and discharged based on some particular states of switches. In more detail, flying-capacitor C_F is charged when q_1 and q_1' are turned on, and is discharged when q_2 and q_2' are turned on. The charge of C_F can be balanced by an appropriate choice of the 0-level switch combination. In this type of topology, there is need for a number of DC-link capacitors as well to clamp voltage [12].

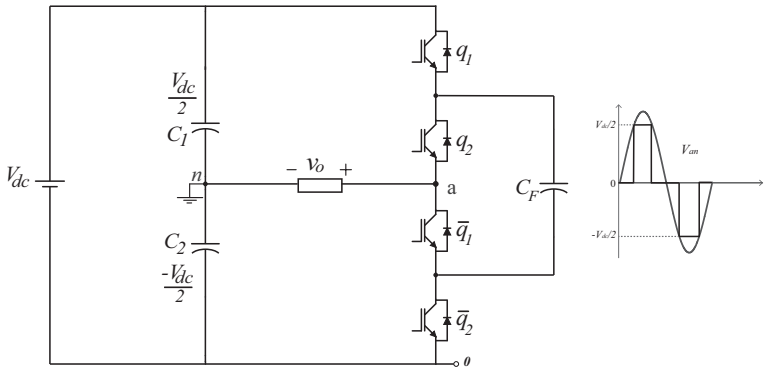


Fig. 1.5. A single phase leg of a three-level capacitor-clamped converter topology and its three-level output voltage waveform.

Having redundant switching states is a unique feature of the capacitor-clamped converter topology. That feature is not only used in clamping-capacitor voltage balancing issues, but also it helps to divide energy losses, which is caused by switching activities, among the semiconductor devices [36]. Making the flying-capacitors' voltages balanced in the practical implementations is required, because those capacitors are expected to distribute the input voltage and to clamp the voltage stress across the power switches. To perform an appropriate balancing of the flying capacitor, some methods such as natural balancing and some other balancing strategies based on closed loop controllers, can be applied in the flying-capacitor converter applications. Due to the nature of this topology, the voltages across the clamping-capacitors are different from each other. In the case of making the output voltage level higher (e.g., five or more level), the amount of flying-capacitors also needs to be increased which causes the converter to become more expensive [37–39].

Cascaded Multilevel Converter

A cascaded (series) half-bridge multilevel converter structure is formed by the combination of a few half-bridge converters and independent DC sources. It is aimed to avoid the usage of clamping-diodes and flying-capacitors by doing so [18]. In this type of configuration, the technique behind the generating of stepped voltage waveform is disparate from the other two popular topologies.

Figure 1.6 shows a single-phase leg of a nine-level cascaded converter with isolated DC sources. The multilevel output voltage of the converter is incorporated by the summation of three-level voltages ($+V_{dc}$, 0, $-V_{dc}$), which are generated by each of the half-bridge converters. As it can be seen from the Figure 1.6, the generated signal at the output side of converter is a nine-level AC voltage, waving from $-4V_{dc}$ to $+4V_{dc}$ by V_{dc} increment. Despite the absence of the filter in the circuit topology, the output waveform is considerable satisfactory in terms of being sinusoidal [40, 41].

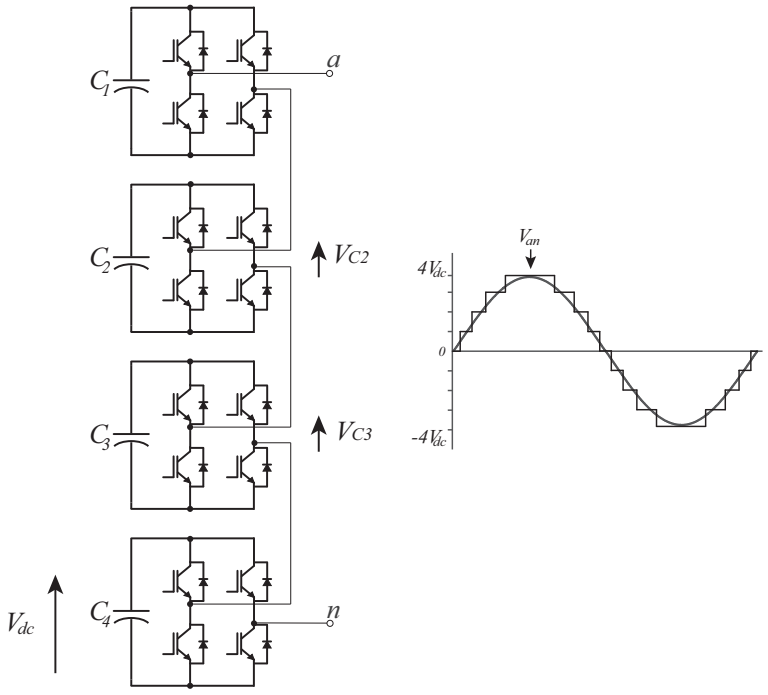


Fig. 1.6. Cascaded multicell converter topology and its waveform.

Cascaded multilevel converters can be utilized in some applications of electrical engineering such as an AC voltage generator in conditioning circuit of power line systems [42]. Also, this sort of converter has been implemented in electric vehicle industry as being responsible for charging the batteries which have the major task for traction systems of these vehicles [28].

Novel Multilevel Converter Structures

Some other multilevel converter topologies have been introduced in the area as a result of the combination, or modification of the basic three multilevel configurations. Moreover, a specific combination of the fundamental topologies can be made to design a particular utilization which demands converter circuits.

Generalized Multilevel Converter Arrangement

This class of topology is structured by an arrangement in which the voltages of semiconductor devices and capacitors become equal to each other. Actually, all converter topologies including the elementary two-level type with the desired number of levels can be acquired through the derivation of generalized multilevel converter configuration. A five level generalized multilevel inverter structure per phase leg is shown in Figure 1.7. [43–47].

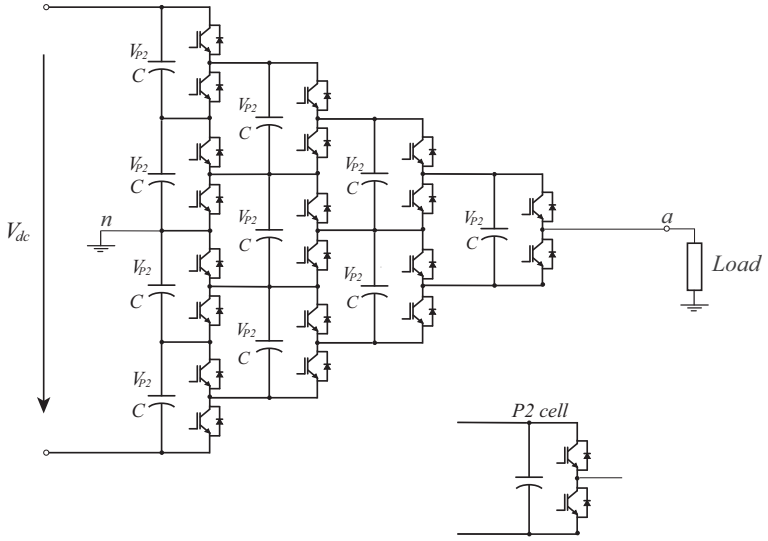


Fig. 1.7. Generalized P2 multilevel converter structure.

Hybrid Multilevel Converters

In order to improve the operation of converters in high-voltage applications, some hybrid architectures, which are named as mixed-level and asymmetric hybrid converter topologies, have been presented in literature. An example of mixed-level converter structure is demonstrated in Fig. 1.8. As distinct from the cascaded converter configuration, each half-bridge unit of it is substituted for the neutral-point clamped or flying-capacitor full-bridge converter units; also, less isolated DC sources are used to keep the same level at the output waveform because the voltage level of each replaced

half-bridge unit is doubled. Although the units' voltage levels are identical with each other in the mixed-level converter, an asymmetric hybrid multilevel topology can be an alternative solution by having unequal voltage levels among the full-bridge converter components. A challenging point for the implementation of these converters is that the control circuits of the power switches are substantially complicated. Also, in order to develop the efficiency of multilevel converters by decreasing the switching losses, some strategies were discovered to apply soft-switching circuits to the stated multilevel converter topologies [12, 47–57].

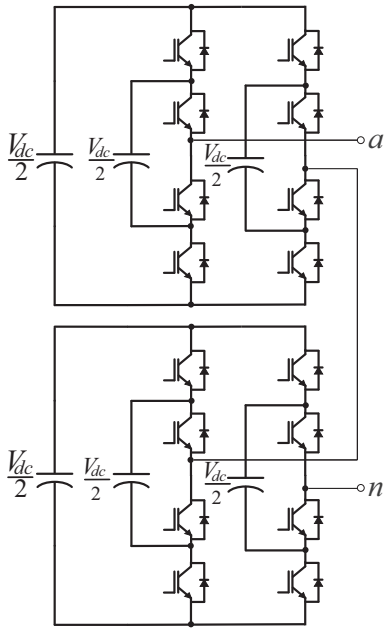


Fig. 1.8. A mixed-level hybrid cell multilevel topology.

1.2.3 Modulation Strategies for Multilevel Converters

Since Pulse Width Modulation (PWM) techniques emerged in the area, they have been become the primary control strategy for the switching devices of the converters. In order to use these PWM methods for the control units of multilevel converters as well, they can be modified particularly. Fig. 1.9 shows the classification of the modulation strategies based on their switching frequencies [58, 59]. Among all kinds of

PWM approaches in literature, three of them have taken the most attention for industrial applications of multilevel converters: multilevel space vector PWM (SVPWM), selective harmonic elimination PWM (SHEPWM), and sinusoidal PWM subject to triangular carrier signals [12, 60].

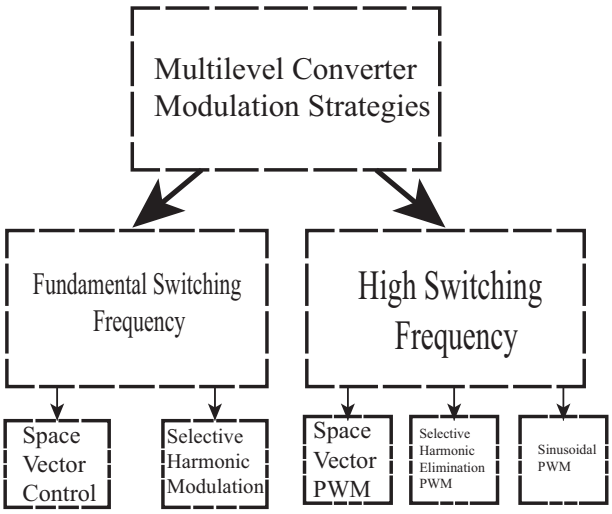


Fig. 1.9. Classification of PWM multilevel converter modulation methods.

Multilevel Space Vector PWM

SVPWM, also called as space vector modulation (SVM), was first proposed for neutral-point-clamped multilevel inverter in [61]. Since then, implementation of this technique has been advanced for other types of multilevel converter topologies; also, among other multilevel PWMs, its popularity has increased due to its flexibility to optimize switching waveforms and compatibility with digital signal processors (DSP) [62–65]. However, its application for more than three-level converter configurations is still challenging, because the higher number of levels at the output voltage of the converter means more switching states which demands complex calculations for the stated PWM method [12].

Selective Harmonic Elimination PWM

SHEPWM was first implemented for multilevel cascaded converters to minimize the total harmonic distortions. In this type of modulation method, some of the optimization approaches such as Newtons method and resultant method are utilized to eliminate certain harmonics of the converters output waveform; Fourier transform is helpful in the calculation of its odd harmonics [66–69]. Due to some distinct advantages of this method over other PWM strategies, however, it has a difficulty obtaining the exact solution of the nonlinear equations in [67] to find the switching angles.

Multilevel Carrier-Based Sinusoidal PWM

In a conventional converter, three major carrier-based PWM techniques, which also can be applied in multilevel converters, are utilized for converter's switching controller: space vector PWM (SVM), third harmonic injection PWM (THPWM), and sinusoidal PWM (SPWM) [47]. Because of its some distinct advantages over the other types such as compatibility with DSPs, sinusoidal PWM is more preferable among those. Its analog implementation consists of several carrier (triangular) and some reference (sinusoidal) signals. In terms of the reduction of the converter's output waveform harmonics, the phase-shifting or the level-shifting methods can be applied in SPWM technique [70–73].

1.3 Objectives

The primary goals of this thesis study is presented in this section as the following:

- Comprehension of power electronics converter topologies, especially multilevel inverter topologies and their modulation strategies.
- Modeling of the conventional four-level flying capacitor topology and implementation of level-shifting modulation strategy to this configuration.
- Propose a new four-level flying-capacitor topology and modeling of this configuration by considering its mathematical equations.
- Improvement of its own control strategy by using the carrier-based sinusoidal PWM approach to meet its operation demands.
- Simulation of the proposed topology and conventional configuration to test validation of theoretical expectations.
- Comparison between proposed and conventional topologies.
- Implementation of the proposed converter by assembling its components in experimental setup.
- Validation of the proposed converter via experimental results.

1.4 Thesis Organization

This study is organized as following:

- Chapter 2 presents the three-level and four-level conventional flying-capacitor multilevel converter topology to reveal the basic understanding of this configuration type.
- Chapter 3 proposes a new topology to the flying-capacitor multilevel converter area. In this chapter, its operation and modulation strategy are explained in detail.
- Chapter 4 explains the components of the experimental setup for implementing the proposed and conventional configurations. Also, the experimental results are given in this chapter.
- Chapter 5 illustrates the conclusions and future works for this thesis.

1.5 Conclusion

In this chapter, power electronics converters, multilevel topologies in detail, were covered. The modulation strategies in literature which are used as the controller of the power electronics switches were reviewed. It turned out that by using the main properties and characteristics of the power switches, the new multilevel converter topologies can be designed.

The motivation of the thesis study was expressed explicitly.

The literature of the multilevel converter topologies, and their modulation strategies, were comprehended. The most popular and relatively novel configurations were discussed.

The objective of this research was specified to provide an accurate description to reach the aims of this thesis study.

The thesis organization was proposed to show the general framework of this study.

2. CONVENTIONAL FOUR-LEVEL FLYING CAPACITOR TOPOLOGY

2.1 Introduction

Multilevel converters have become more remarkable for many manufacturers whose goal is to drive high-power medium-voltage systems. Also, they are often utilized to transmit high-voltage direct current (HVDC) in order to advance the performance of the system and lessen conversion losses by reducing $\frac{dv}{dt}$ and harmonics, which are produced by converter [74]. In comparison with the diode-clamped and series H-Bridge converters, the flying capacitor multilevel converter topology is relatively new in the area. It has several explicit advantages over the diode clamped and series H-Bridge topologies. For instance, there is no need for clamping diodes like in the diode clamped converters and isolated voltage sources are not demanded like in series H-Bridge converters. By taking these advantages into consideration, the flying capacitor multilevel converters are promising for industry and for many industrial applications [75]. In Fig. 2.1(a) and (b) the conventional single-phase three-level and four-level flying-capacitor converters are illustrated respectively.

The flying capacitor converter has a modular structure, but it has not been given attention from industry as much as diode-clamped or cascade multilevel converters. This is because the operation condition of capacitor-clamped converter's in which there is a need for higher switching frequencies to make the capacitors balanced properly. To balance the capacitors, there are mainly two methods: natural or a control-based balancing [76].

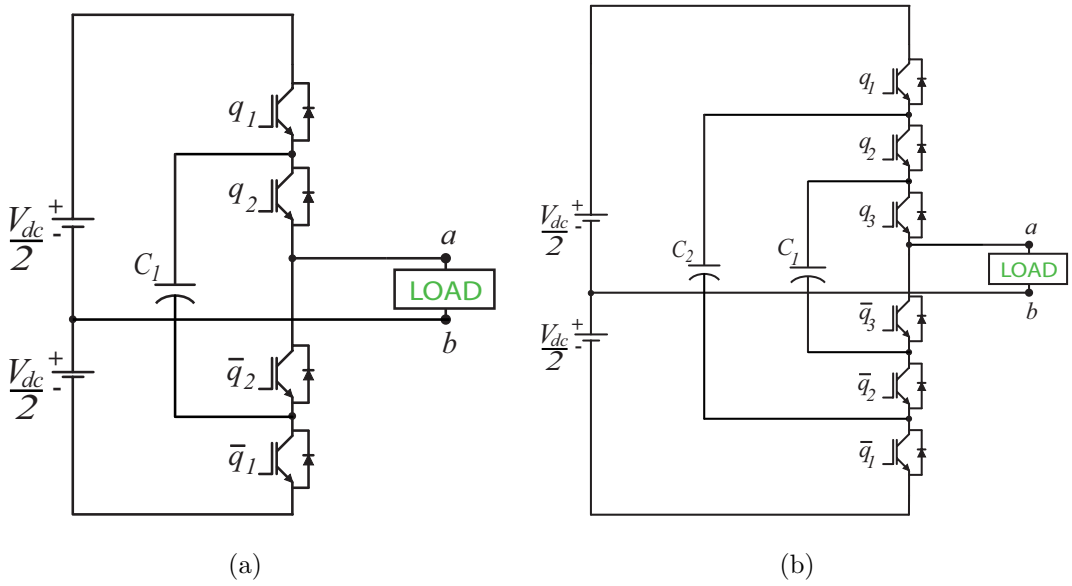


Fig. 2.1. Conventional single-phase flying-capacitor converter topologies (a) Three-level configuration. (b) Four-level configuration.

2.2 Converter Principle of Operation

Figure 2.1(a) shows one phase of the conventional three-phase four-level flying-capacitor converter topology. Its four-level version is, also, illustrated in Fig. 2.1(b). Conventional four-level capacitor-clamped converter structure is constituted by six controlled power electronics switching devices, which are complementary, (q_1, $\overline{q}_1$, q_2, $\overline{q}_2$, q_3, $\overline{q}_3$), two flying capacitors, and DC source. Since each flying capacitor is charged to a non-equivalent value of voltage, output voltages are generated in different values with the change of switching states of semiconductor devices; however, there may be some redundant states which generate the same output values. Flying capacitor C_1 is used to generate two-level waveform, C_2 is for three-level signal of output, and the leg, which is connected to two DC sources, is used to generate four-level output voltage. Cross voltages of flying capacitors are as following:

$$\begin{aligned} V_{C1} &= V_{dc}/3 \\ V_{C2} &= 2V_{dc}/3 \end{aligned} \tag{2.1}$$

2.3 Model

Based on the states of the switches, equivalent circuits of each state can be drawn to model the topology. Since switches are complementary, mainly three switches can be utilized to define the states. Each switching state and its corresponding voltage is given in Table 2.1. As it can be seen from Table 2.1, in some sequential states, the same output voltage is generated; such as state two and state three, so six switching states totally define the output voltage.

Table 2.1.
The switching states of the conventional four-level flying-capacitor topology and their corresponding output voltages.

State	$\{q_1\ q_2\ q_3\}$	$\{\overline{q}_1\ \overline{q}_2\ \overline{q}_3\}$	v_{ab}
1	{0 0 0}	{1 1 1}	$-V_{dc}/2$
2	{0 0 1}	{1 1 0}	$-V_{dc}/6$
3	{0 1 0}	{1 0 1}	$-V_{dc}/6$
4	{0 1 1}	{1 0 0}	$V_{dc}/6$
5	{1 0 0}	{0 1 1}	$-V_{dc}/6$
6	{1 0 1}	{0 1 0}	$V_{dc}/6$
7	{1 1 0}	{0 0 1}	$V_{dc}/6$
8	{1 1 1}	{0 0 0}	$V_{dc}/2$

Referring to Fig. 2.1(b), the branch which is responsible for generating three-level voltage, where C_2 is connected, the flying capacitor is charged to $2V_{dc}/3$, and the other branch, which produces two-level waveform, C_1 capacitor is charged to $V_{dc}/3$. Each blocking voltage drop of the power switches $V_{dc}/3$ in turned-off states. In the inverter mode of operation, the corresponding circuits of the topology are shown in Fig. 2.2.

In the first state,$q_1 = q_2 = q_3 = 0$, the load or output voltage v_{ab} or v_o is given by,

$$\begin{aligned} v_{ab} + V_{dc}/2 = 0 \\ v_{ab} = -V_{dc}/2 \end{aligned} \tag{2.2}$$

In the second state,

$$\begin{aligned} v_{ab} + V_{dc}/2 - V_{C1} = 0 \\ v_{ab} = -V_{dc}/6 \end{aligned} \tag{2.3}$$

The third state generates the same level output voltage with the second state,

$$\begin{aligned} v_{ab} + V_{dc}/2 - V_{C2} + V_{C1} = 0 \\ v_{ab} = -V_{dc}/6 \end{aligned} \tag{2.4}$$

in the fourth state, the output voltage turns negative value of the second or third state. The equation is given by,

$$\begin{aligned} v_{ab} + V_{dc}/2 - V_{C2} = 0 \\ v_{ab} = V_{dc}/6 \end{aligned} \tag{2.5}$$

The state five generates minus level voltage at the output,

$$\begin{aligned} v_{ab} - V_{dc}/2 + V_{C2} = 0 \\ v_{ab} = -V_{dc}/6 \end{aligned} \tag{2.6}$$

in the sixth state, the output voltage level sign switches from positive to negative by staying in the same magnitude,

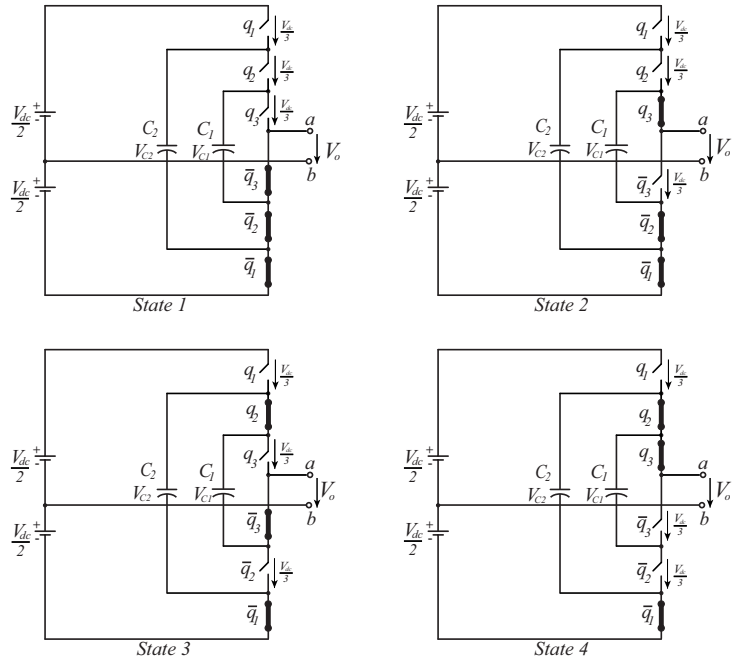
$$\begin{aligned} v_{ab} - V_{dc}/2 + V_{C2} - V_{C1} = 0 \\ v_{ab} = V_{dc}/6 \end{aligned} \tag{2.7}$$

the state seven generates the same level magnitude and sign with the state six, so the equation is given by,

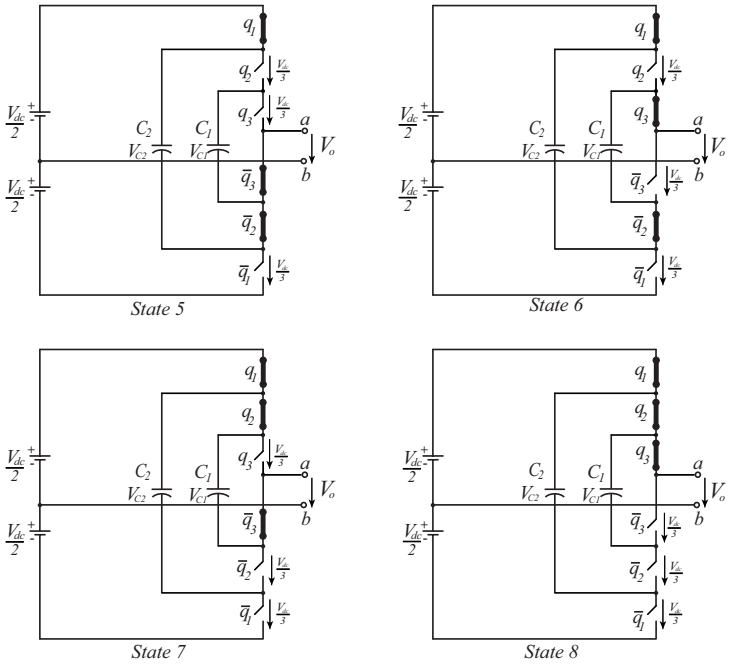
$$\begin{aligned} v_{ab} - V_{dc}/2 + V_{C1} = 0 \\ v_{ab} = V_{dc}/6 \end{aligned} \tag{2.8}$$

In the eight state,$q_1 = q_2 = q_3 = 1$, and the equation is given by,

$$\begin{aligned} v_{ab} - V_{dc}/2 = 0 \\ v_{ab} = V_{dc}/2 \end{aligned} \tag{2.9}$$



(a)



(b)

Fig. 2.2. The corresponding circuits of the states (a) States one to four. (b) States five to eight.

Taking consideration of these equations, the output voltage can be given or modeled mathematically by the following equation,

$$v_o = (2q_1 + 2q_2 + 2q_3 - 3)V_{dc}/6 \tag{2.10}$$

2.4 Modulation Strategy

For the conventional four-level flying-capacitor converter topology, four-level carrier-based sinusoidal PWM strategy has been used. In this approach, one sinusoidal waveform, which is called as desired voltage (v^*_{sin}) and one triangular carrier signal is employed for the generation of each level, so three triangular carrier signals in total (v^*_{t1}, v^*_{t2} and v^*_{t3}) are used. The same PWM approach is applied to the conventional three-level flying-capacitor converter topology as well.

In Fig. 2.3(a), the analog implementation of the PWM strategy for this converter is shown. Fig. 2.3(b) illustrates the PWM signals which consist of three carrier (triangular) waveforms and one sinusoidal waveform. The magnitude of the sinusoidal signal fluctuates between 1 and -1 and its frequency is selected as 60 Hz. The magnitude of the triangular signals are 2/3 and the level-shift technique has been performed. The frequency of the carrier signals has been chosen as 500Hz for the sake of illustration.

2.5 Flying Capacitor Control

In the real implementation of flying-capacitor topologies, the voltage control of the flying capacitors is very complex. In order to simplify the analysis of these converter topologies, the flying capacitors can be substituted by DC voltages. A three-level conventional flying-capacitor topology, which is substituted by a DC voltage, is shown in Fig. 2.4 above. However, in practical applications of this type of converter topologies, the control of the flying capacitors is necessary to be performed.

When the level-shift PWM approach is applied to the conventional three-level flying-capacitor topology, the results for the capacitor variables (v_c and i_c) are pre-

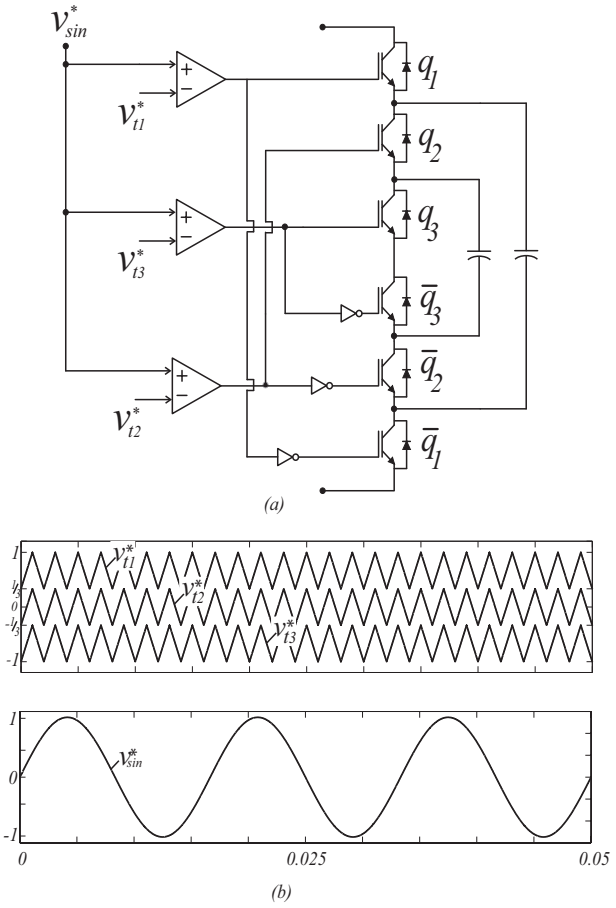


Fig. 2.3. Modulation strategy (a) PWM analog implementation strategy. (b) Waveforms of carrier and sinusoidal signals.

sented in Fig. 2.5. In this scenario, a value of $400V$ DC source was used for V_{dc}. The variations for the flying-capacitor voltage, which cause the low-frequency distortion at the output waveform, can be seen in the Fig. 2.5. Ideally, the expected voltage for v_c is a constant value which is equal to the half of the total value of DC sources. Basically, the control of flying-capacitor voltage aims to perform keeping v_c as constant as possible.

The polarity of the capacitor current in Fig. 2.5 has changed with the sinusoidal frequency increasing the ripple for v_c. The flying capacitor is only discharged during the positive half cycles of the reference (sinusoidal) voltage, because i_c is either zero

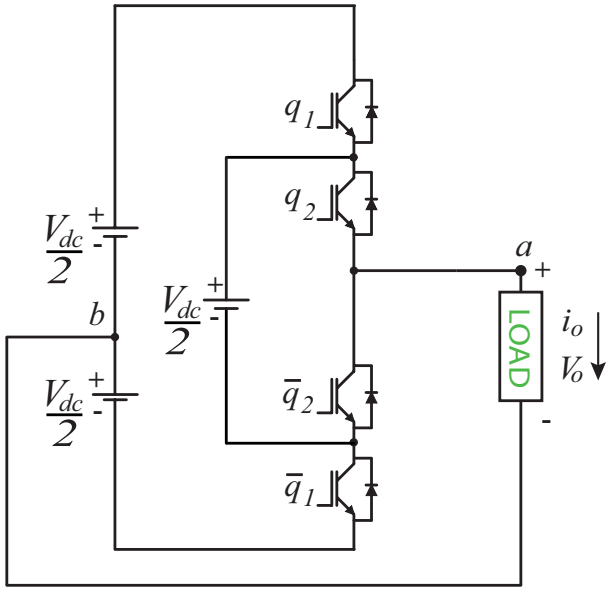


Fig. 2.4. Three-level flying-capacitor half-bridge converter, substituted by a dc voltage.

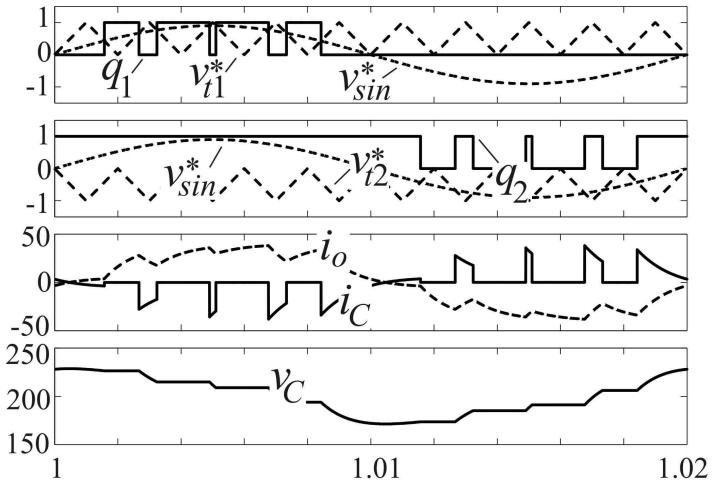


Fig. 2.5. Control and power waveforms for the half-bridge circuit with level-shift PWM.

or negative. On the other hand, i_c is either zero or positive, charging occurs for the flying capacitor during the negative half cycles of the sinusoidal voltage.

To reduce the ripple of the flying-capacitor voltage, another PWM strategy, phase-shift technique, can be used. In this method, phase shift of the carrier (triangular)

signals leads to the flying capacitor charging and discharging at the switching frequency. This will play an important role to keep v_c with reduced ripple.

As a result, there are some PWM approaches which are able to reduce the variations on the flying capacitor voltages. Making ripples less means reducing the distortions of the output voltages as well. Since the voltage control of the flying capacitor is not one of the objectives of this research, only basic information about it is presented in this study.

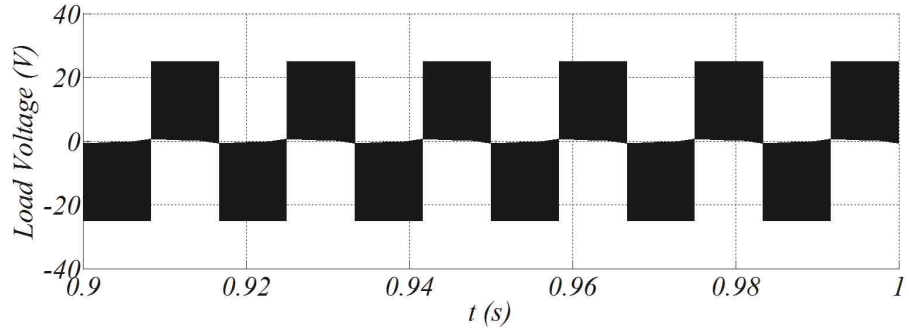
2.6 Simulation Results

Conventional three- and four-level flying capacitor converter topology has been performed in the platform of PSIM Simulation Software. The modulation strategy of the converter can be executed in PSIM by using its elements for analog implementation or its DLL blocks feature which link to C programming language codes. Both implementations were done in this research to make certain of the correctness of the results. The simulation results for Fig. 2.1(a) and (b) were attained for the parameters given below:

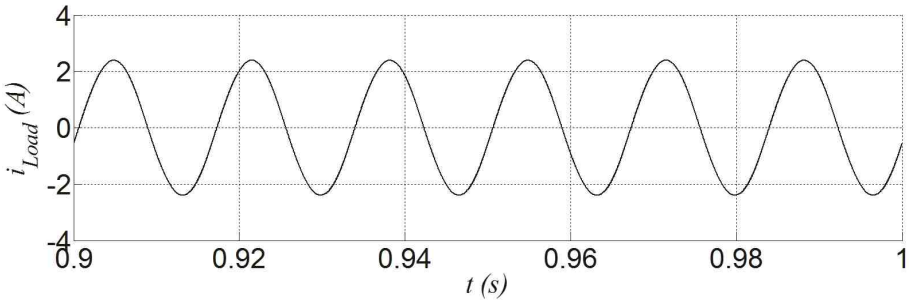
$V_{dc} = 50V;\ \ \frac{V_{dc}}{2} = 25V \quad f_s = 20kHz$
$C_1 = C_2 = 2200\mu F \qquad R = 10\Omega \qquad L = 7mH$

The results of the conventional single-phase three-level flying-capacitor converter topology with the level-shift PWM approach are shown in Fig. 2.6, Fig. 2.7 and Fig. 2.8. Fig. 2.6(a) depicts the load voltage, which is three-level as expected. In Fig. 2.6 (b) the load current is illustrated. To make some comparison in the next sections of this study, the simulated outcomes of the flying capacitor's voltage and current are given in Fig. 2.7(a) and (b). Also, to present a visual example for the blocking voltages of the switches, two of them, q_1's and q_2's, are shown in Fig. 2.8(a) and (b).

For the conventional single-phase four-level flying-capacitor converter topology, the simulation results are obtained as well. Since there are two flying capacitors in this configuration, their voltage control issue has appeared as a problem when the level-shift modulation strategy, which is given in Fig. 2.3, is used as the PWM implementation. By reason of the fact that analyzing the voltage control of the flying capacitors is not among the goals of this study, so these capacitors were substituted by DC voltage sources which are respectively: $V_{dc}/3$ and $2V_{dc}/3$ value of DC sources for C_1 and C_2. Fig. 2.9(a) shows the load voltage and Fig. 2.9(b) represents the load current outcome for the four-level version of this topology.

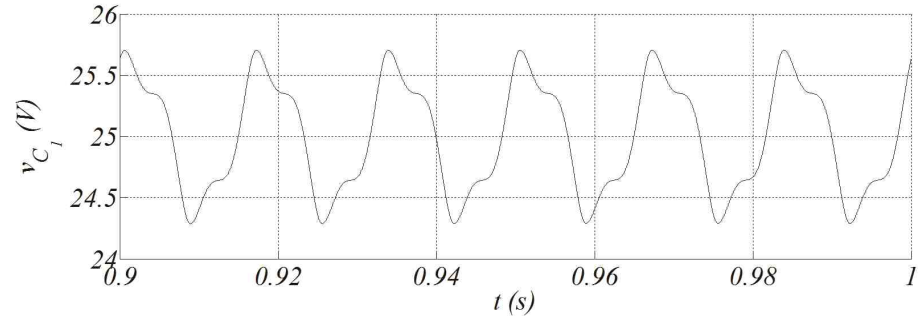


(a)

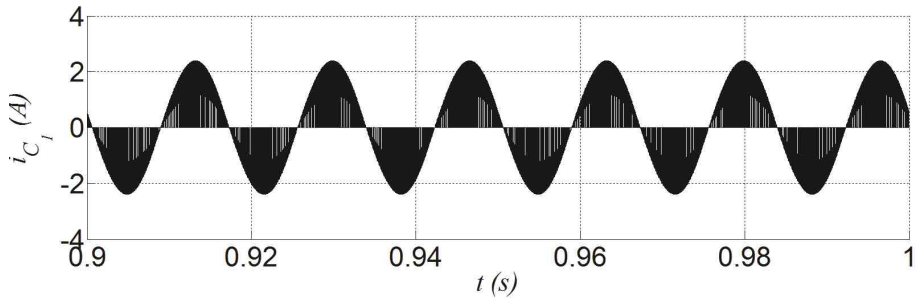


(b)

Fig. 2.6. Simulation results for the conventional three-level configuration: (a) Load Voltage. (b) Load Current.

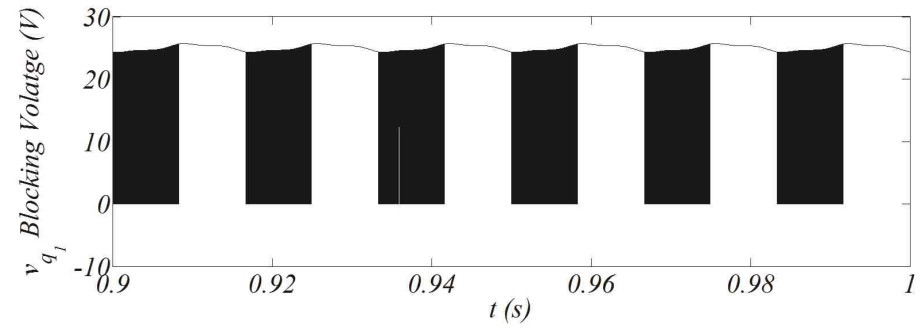


(a)

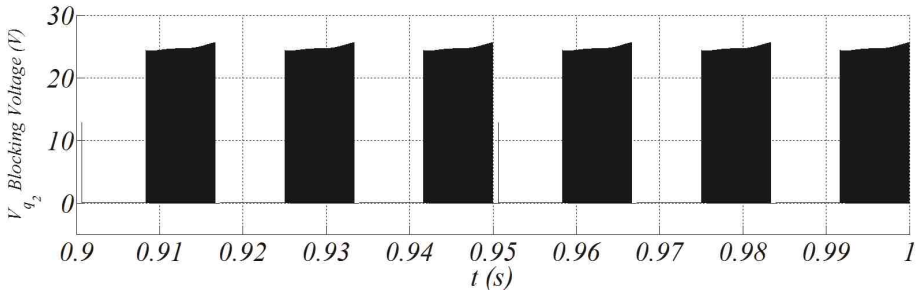


(b)

Fig. 2.7. Simulation results for the conventional three-level configuration: (a) Flying Capacitor Voltage. (b) Flying Capacitor Current.



(a)



(b)

Fig. 2.8. Simulation results for the conventional three-level configuration: Blocking Voltages of Switches (a) Switch q_1. (b) Switch q_2.

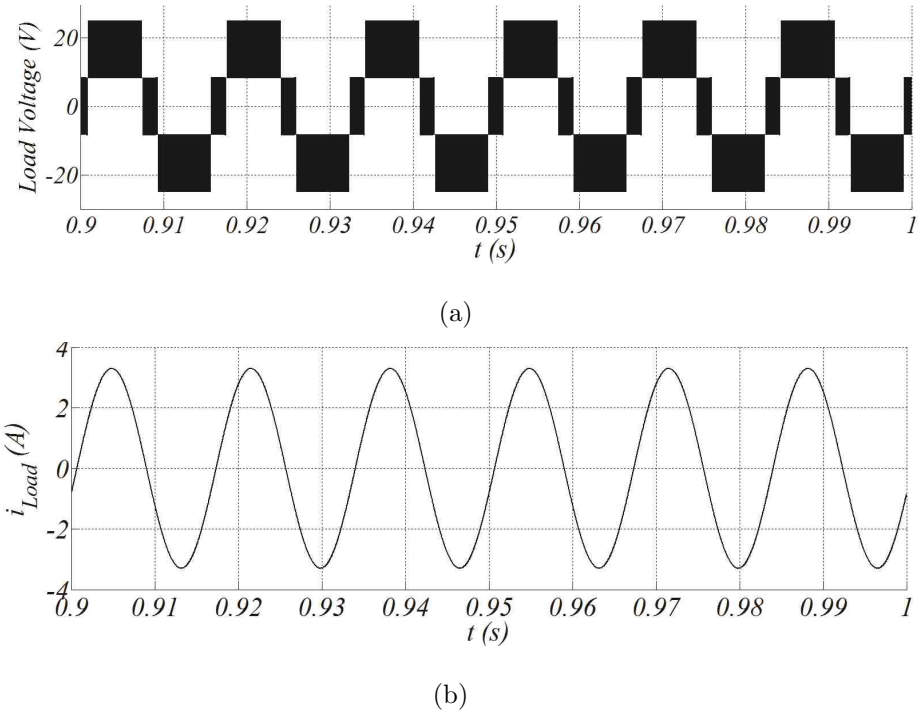


Fig. 2.9. Simulation results for the conventional four-level configuration: (a) Load Voltage. (b) Load Current.

2.7 Conclusion

In this chapter, the conventional three- and four-level half-bridge flying-capacitor topologies and a PWM approach, level shift method, for these configurations were presented. The voltage control issue of the flying capacitors were discussed briefly as well.

The background of the flying-capacitor topology as well as some superiorities over other two popular multilevel topologies, diode-clamped and cascaded, were explained.

The principle operation for the conventional four-level flying-capacitor converter topology was expressed.

The model of the four-level version of this kind of multilevel converters were obtained via the mathematical calculations from the equivalent circuits of the topology, based on switching states.

The modulation strategy was determined as level-shift PWM method and its analog implementation was visually illustrated by Figures.

The control of the flying-capacitor voltages was discussed briefly. The different PWM approaches how reducing the flying-capacitor voltage ripple as a natural balancing method was shown.

The simulated results for both level topology were displayed by the given parameters for the circuits.

3. FOUR-LEVEL HALF-BRIDGE CONVERTER TOPOLOGY

As stated in the previous sections, the most utilized multilevel configurations aspect of the industry interest are diode clamped (or NPC), cascade and flying capacitor multilevel inverters. These three main multilevel converter configurations are considered as the conventional ones and the other type multilevel topologies, introduced in the literature, are considered as non-conventional ones throughout this research.

3.1 Introduction

Beside the high and medium power systems, DC-AC multi-level converters for single-phase applications has been explored in the technical literature due to its importance in low power applications (e.g., reduced THD) as well. [77–82]. In [83] a single-phase multilevel converter for application in electrified railway was proposed, while in [84] a family of single-phase multi-level inverters without clamping diodes and flying capacitors was proposed. The single-phase converter in [85] uses two asymmetrical 4-level converters to generate the proposed hybrid cascade converter. Four-level inverters conceived for single-phase applications were explored in [86–90]. In [91], a novel five-level flying-capacitor half-bridge converter topology is presented.

The proposed H-bridge topology is depicted in Fig. 3.1. Such a configuration can operate either with three dc sources, which can be obtained through a set of PV arrays as in [92], or from a unique dc source with additional circuitry, as in [86]. The proposed converter can be considered as an intermediate configuration between the 3-level 4-switch H-bridge topology, as observed in Fig. 3.2(a) and the 5-level 8-switch H-bridge topology, as observed in Fig. 3.2(b). Then, following this nomenclature, the proposed converter is a flying-capacitor 4-level 6-switch H-Bridge topology.

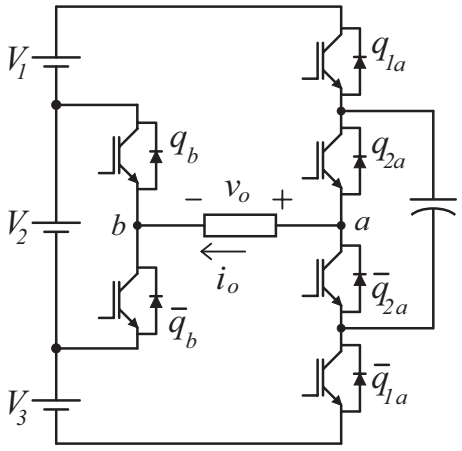
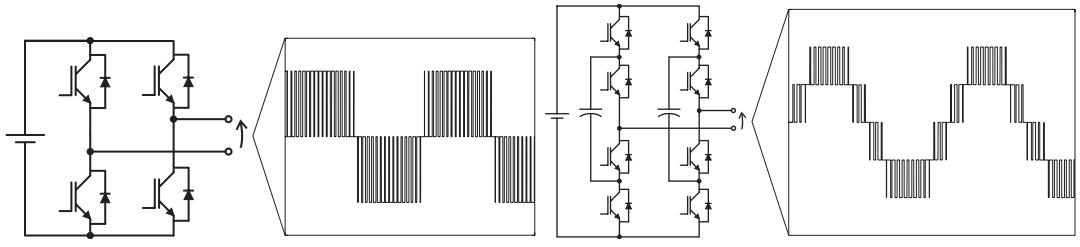


Fig. 3.1. Proposed flying capacitor four-level H-Bridge converter.

3.2 Proposed Converter Operation

The proposed H-bridge converter is constituted by six controlled switches (q_{1a}, $\overline{q}_{1a}$, q_{2a}, $\overline{q}_{2a}$, q_b, $\overline{q}_b$), a flying capacitor, and three dc sources. The switches q_{1a}, $\overline{q}_{1a}$, q_{2a} and $\overline{q}_{2a}$ are used in the flying-capacitor three-level leg, while the switches q_b and $\overline{q}_b$ are used to compose the two-level leg, the switches q_{1a}, q_{1b}, q_b are complementary to the switches $\overline{q}_{1a}$, $\overline{q}_{1b}$, $\overline{q}_b$, respectively. To guarantee that all power switches will operate under the same blocking voltage and to guarantee a symmetrical output voltage, it is necessary to make $V_1 = V_3 = V_{dc}$ and $V_2 = 2V_{dc}$.



(a) (b)

Fig. 3.2. Conventional configuration and its output voltage waveform. (a) 3-level 4-switch H-bridge topology. (b) 5-level 8-switch H-bridge topology.

Considering all possibilities of switching states available, which are totally six, the output voltage is determined by Table 3.1. In two possible states, current does not find any way to go through the circuit, so those two states were not shown in Table 3.1. From this table there are four voltage levels for v_o. Considering either dc sources with different values or new connections by using the same number of switches, it is possible to increase the number of levels at the output side of the proposed H-bridge converter.

Table 3.1.
Output voltage considering all switching states available.

State	$\{q_{1a}\ q_{2a}\ q_b\}$	v_o
1	{0 0 0}	$-V_{dc}$
2	{0 0 1}	$-3V_{dc}$
3	{0 1 0}	$-V_{dc}$
4	{0 1 1}	V_{dc}
5	{1 1 0}	$3V_{dc}$
6	{1 1 1}	V_{dc}

As observed in Fig. 3.1, the single-phase load is connected between the points a and b of the converter, which leads to an output voltage given by:

$$v_o = (2q_{1a} + 2q_{2a} - 2q_b - 1)V_{dc} \tag{3.1}$$

3.3 Modulation Strategy

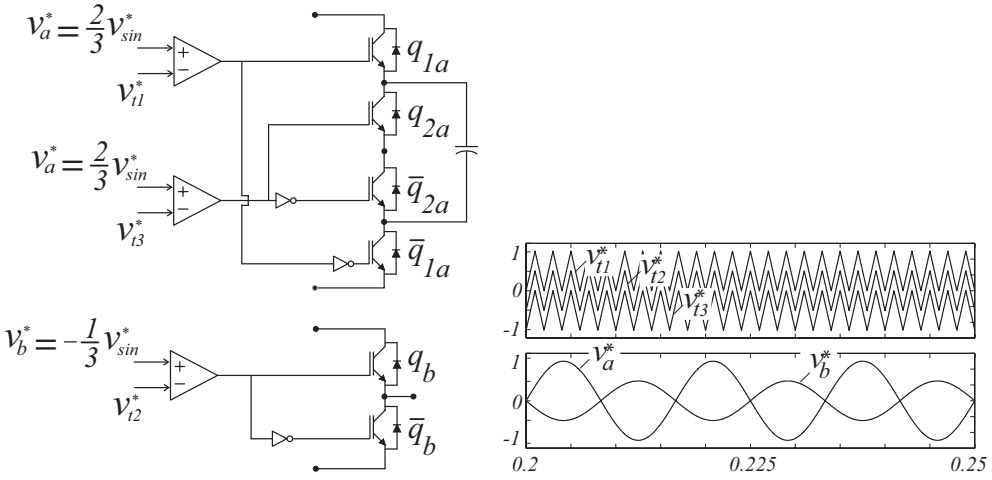
The modulation strategy for the proposed converter can be done assuming a combination of the two-level and three-level PWM approaches, which means that, one triangular carrier signal (v_{t2}^*) will be employed for the two-level leg, and two triangular carrier signals (v_{t1}^* and v_{t3}^*) will be used for a three-level leg. Since each leg is capable to synthesize different values of voltages, i.e., $2V_{dc}$ for the two-level leg and $4V_{dc}$ for

the three-level leg, the sinusoidal waveforms employed to define PWM signals should follow the same ratio. Indeed, there are two requirements: the reference voltage for the three-level leg is twice bigger than the two-level leg and their difference must be the desired voltage (v^*_{sin}). Taking these specifications in consideration leads to the definition of the reference sine voltages for PWM as following:

$$v^*_a = \frac{2}{3}v^*_{sin} \tag{3.2}$$

$$v^*_b = -\frac{1}{3}v^*_{sin} \tag{3.3}$$

Fig. 3.3(a) shows the analog implementation of the PWM approach for the proposed converter. Notice that the level-shift technique has been applied for the flying capacitor three-level leg. Fig. 3.3(b) shows the PWM signals with three triangular waveforms (v^*_{t1} and v^*_{t3} employed for the the three-level leg and v^*_{t2} used for the two-level leg) and two sinusoidal waveforms, as in equations (2) and (3). For the sake of illustration the frequency for v^*_{t1}, v^*_{t2} and v^*_{t3} is 500Hz.



(a) (b)

Fig. 3.3. (a) PWM analog implementation. (b) PWM waveforms.

3.4 Topological States

Each state, which is given by Table 3.1, has two topological circuits for both positive and negative currents, as illustrated in Figs. 3.4, 3.5, and 3.6.

Fig. 3.4(a) shows the generation of the level $-V_{dc}$ for positive and negative current respectively. It is noticable that the current flows through two diodes and a power switch in Fig. 3.4(a). On the other hand, for the negative load current, the current goes through two switches and one diode. From the related figures of topological states, it is understandable that how the flying capacitor is charged and discharged. The only scenario in which the charging and discharging of flying capacitor occurs is presented in the Fig. 3.5, states 3 and 4.

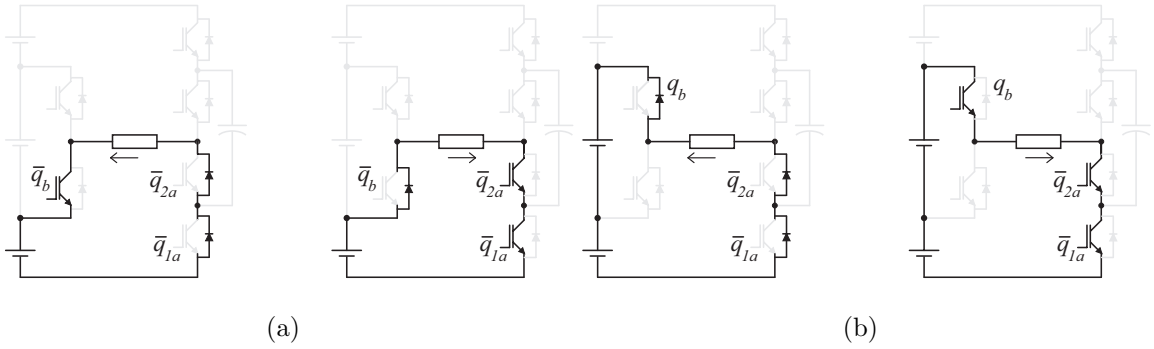


Fig. 3.4. Topological states in positive and negative currents of states 1 and 2.

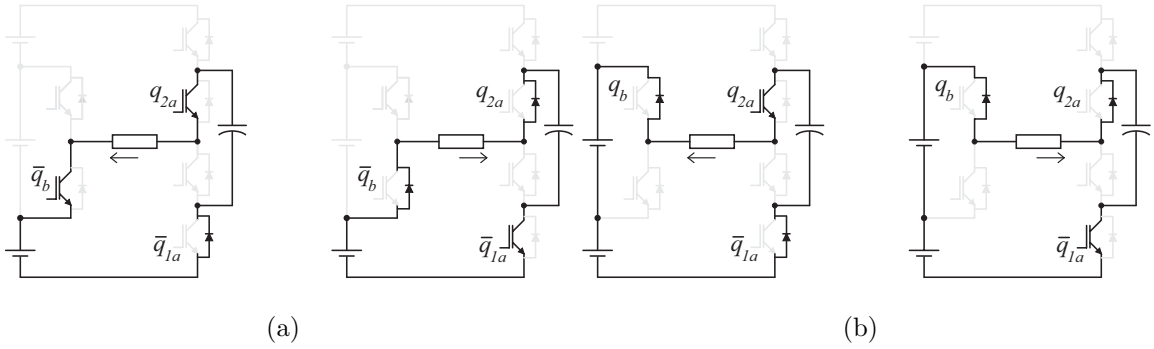
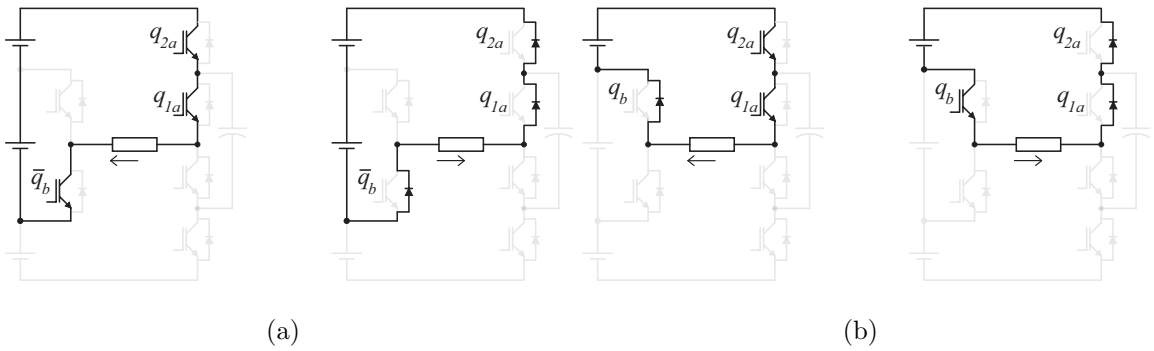


Fig. 3.5. Topological states in positive and negative currents of states 3 and 4.



(a) (b)

Fig. 3.6. Topological states in positive and negative currents of states 5 and 6.

3.5 Three-Phase Flying Capacitor Four-Level Converter

Fig. 3.7 shows the three-phase version of the proposed flying capacitor four-level converter by using a open-end motor drive system. As seen in Fig. 3.7, the three-phase machine is connected between the a, a+, b, b+, c and c+ of the converter. Output voltages are given by:

$$v_a = (2q_{1a} + 2q_{2a} - 2q_a - 1)V_{dc} \tag{3.4}$$

$$v_b = (2q_{1b} + 2q_{2b} - 2q_b - 1)V_{dc} \tag{3.5}$$

$$v_c = (2q_{1c} + 2q_{2c} - 2q_c - 1)V_{dc} \tag{3.6}$$

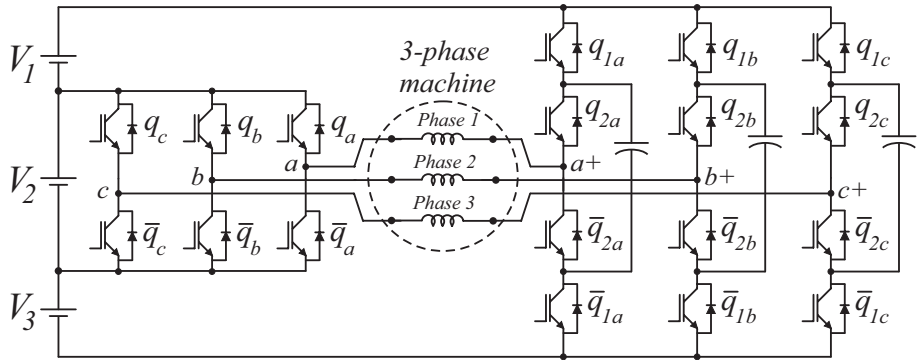


Fig. 3.7. Three-phase version of the proposed converter with open-end winding three-phase motor.

The modulation strategy for the three-phase version is the similar to single-phase one. The three triangular carrier signals will be used as the same, but the reference voltages will be employed with phase angles. To show reference voltages of each phases, the following equations are given:

$$v^*_{sin1} = V^* sin(wt) \tag{3.7}$$

$$v^*_{sin2} = V^* sin(wt - \frac{2\pi}{3}) \tag{3.8}$$

$$v^*_{sin3} = V^* sin(wt - \frac{4\pi}{3}) \tag{3.9}$$

The reference voltages lead to:

$$v^*_{a+} = \frac{2}{3} v^*_{sin1} \tag{3.10}$$

$$v^*_{a} = -\frac{1}{3} v^*_{sin1} \tag{3.11}$$

$$v^*_{b+} = \frac{2}{3} v^*_{sin2} \tag{3.12}$$

$$v^*_{b} = -\frac{1}{3} v^*_{sin2} \tag{3.13}$$

$$v^*_{c+} = \frac{2}{3} v^*_{sin3} \tag{3.14}$$

$$v^*_{c} = -\frac{1}{3} v^*_{sin3} \tag{3.15}$$

3.6 Comparison with Conventional Topology

The comparison between the proposed and the conventional topology in Fig. 2.1(b) is in terms of their blocking voltages, the number of semiconductor devices and passive elements. In Table II and Table III, the blocking voltages of the conventional topology and proposed one are shown. The blocking voltages of the switches are the same in both topology. To acquire the output voltages with the same value, totally the value of $1.33V_{dc}$ dc source is used in proposed topology, while, the value of $2V_{dc}$ dc source requires in the conventional topology. Also, in conventional one there are two flying capacitors for four-level output waveform, however, in the proposed one, the same level is generated with one flying capacitor. The number of switches stay the same.

State	$\{q_1\ q_2\ q_3\}$	V_{q1}	V_{q2}	V_{q3}	v_o
1	{0 0 0}	$0.67V_{dc}$	$0.67V_{dc}$	$0.67V_{dc}$	$-V_{dc}$
2	{0 0 1}	$0.67V_{dc}$	$0.67V_{dc}$	0	$-0.33V_{dc}$
3	{0 1 0}	$0.67V_{dc}$	0	$0.67V_{dc}$	$-0.33V_{dc}$
4	{0 1 1}	$0.67V_{dc}$	0	0	$0.33V_{dc}$
5	{1 1 0}	0	0	$0.67V_{dc}$	$0.33V_{dc}$
6	{1 1 1}	0	0	0	V_{dc}

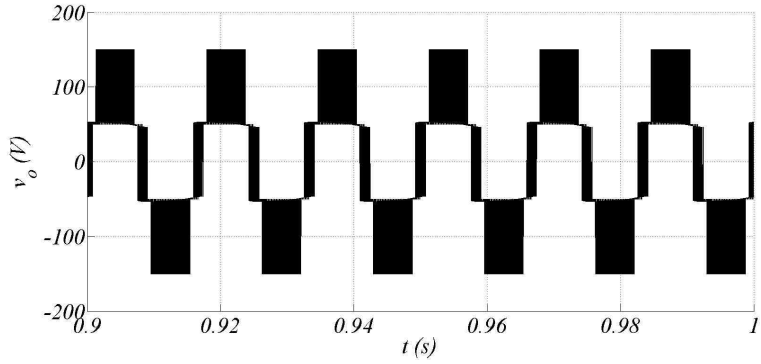
Table 3.2.
Conventional single-phase 4-level configuration.

State	$\{q_{1a}\ q_{2a}\ q_b\}$	V_{q1a}	V_{q2a}	V_{qb}	v_o
1	{0 0 0}	$0.67V_{dc}$	$0.67V_{dc}$	$0.67V_{dc}$	$-0.33V_{dc}$
2	{0 0 1}	$0.67V_{dc}$	$0.67V_{dc}$	0	$-V_{dc}$
3	{0 1 0}	$0.67V_{dc}$	0	$0.67V_{dc}$	$0.33V_{dc}$
4	{0 1 1}	$0.67V_{dc}$	0	0	$-0.33V_{dc}$
5	{1 1 0}	0	0	$0.67V_{dc}$	V_{dc}
6	{1 1 1}	0	0	0	$0.33V_{dc}$

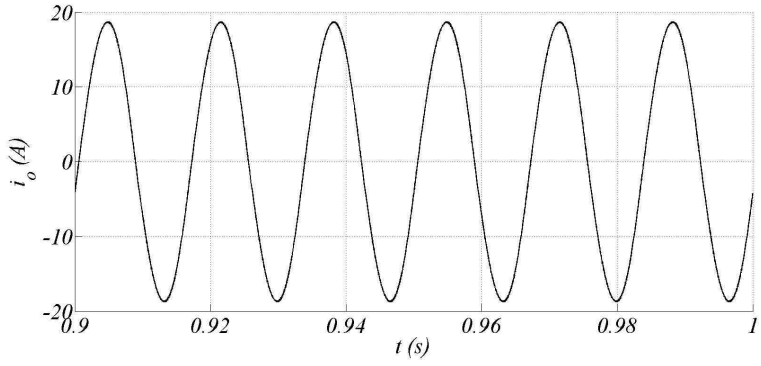
Table 3.3.
Proposed H-bridge converter blocking voltages.

3.7 Simulation Results

The proposed single-phase and three-phase converters were implemented by simulation with a switching frequency equal to 10kHz. The flying capacitor value was $C = 2200\mu F$ and $V_{dc} = 50V$. The single-phase RL load was given respectively by 5Ω and $5mH$. Figs. 3.8(a) and 3.8(b) show respectively load voltage and current. The design of the flying capacitor is an important aspect of the proposed converter, mainly to avoid the ripple associated with the levels V_{dc} and $-V_{dc}$. Fig. 3.9 presents the effect of the capacitor value through the voltage ripple. The result of Fig. 3.9(a) is for $C = 2200\mu F$, while in Fig. 3.9(b) is for $C = 4400\mu F$. The simulation results for the three-phase version of the proposed converter is presented in Fig. 3.10 and 3.11.

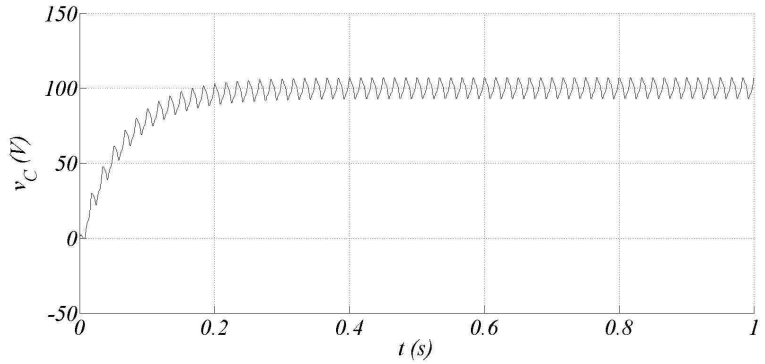


(a)

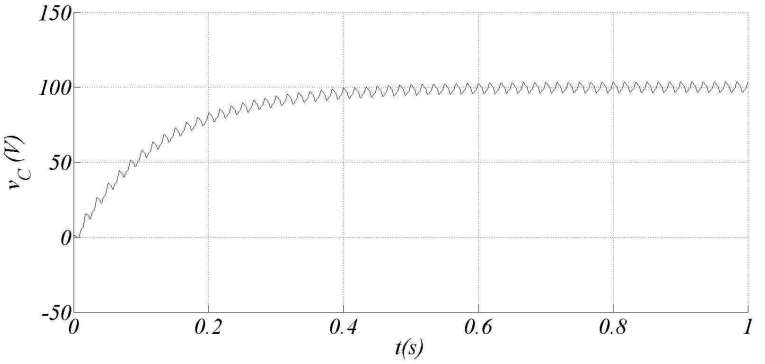


(b)

Fig. 3.8. Simulation results: (a) load voltage and (b) load current.



(a)



(b)

Fig. 3.9. Simulation results for the flying capacitor voltage with: (a) $C = 2200\mu F$ and (b) $C = 4400\mu F$.

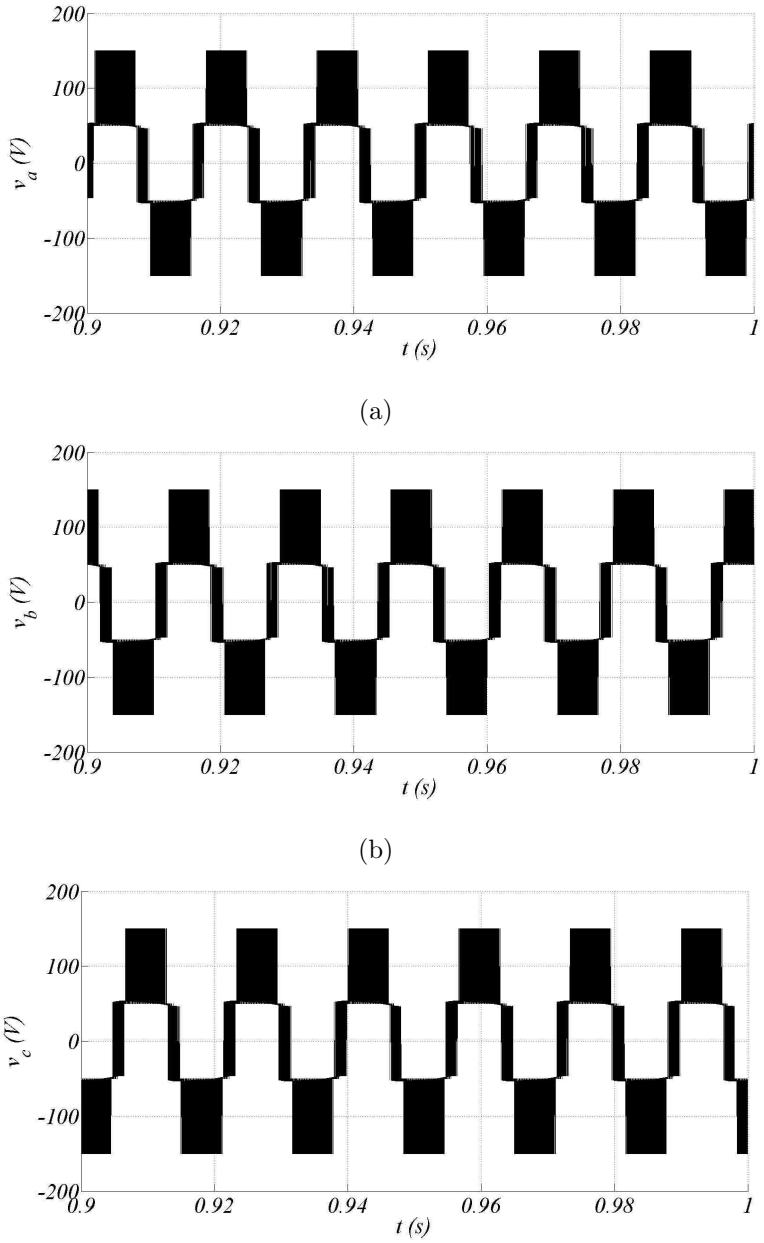


Fig. 3.10. Simulation results for three-phase proposed converter: (a) voltage of the phase 1, (b) voltage of the phase 2, (c) voltage of the phase 3.

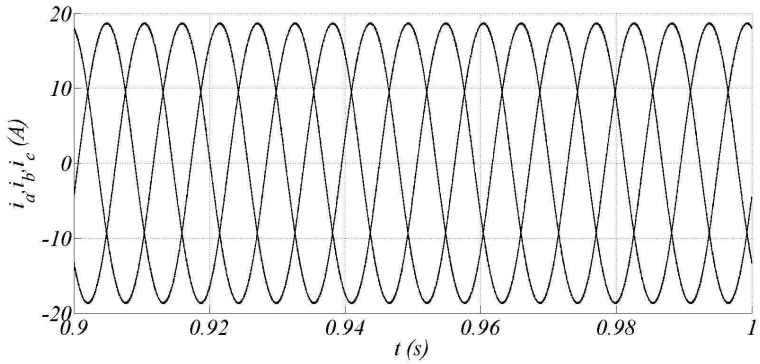


Fig. 3.11. Three-phase currents for the three-phase version of the proposed topology.

3.8 Conclusion

A new multilevel flying-capacitor topology and its PWM strategy were proposed in this chapter. This novel topology was named as flying-capacitor four-level half-bridge converter.

An introduction section was given to explain the need of the proposed converter topology in terms of industrial application. Also, the suitable dc sources for this proposed converter topology was searched.

The proposed converter operation was explained by giving its available switching states and corresponding generated output voltage levels table. An output voltage equation was derived based on this table.

Its modulation strategy in which a two-level and three-level PWM were combined was introduced. The level-shift technique was applied for the flying capacitor three-level leg.

To show visually how the positive and negative currents circulate and how charging and discharging of flying-capacitor occurs depends on the switching states, the topological states were depicted.

The three-phase version of the proposed converter topology was shown, and, the equations for its output voltages and PWM strategy were expressed as well.

A comparison between the single-phase version of the proposed and conventional single-phase four-level flying-capacitor topologies was made. Its results in terms of the blocking voltages were tabled.

The load voltages, load currents, and the flying capacitor voltages for the two different values of the flying-capacitor for both single-phase and three-phase version of the proposed topology were obtained from the analog implementation of the proposed converter and the simulation results were illustrated.

4. PROOF-OF-CONCEPT EXPERIMENTAL SETUP

In this chapter, the experimental setup is presented in two subsections: hardware and software descriptions. Also, experimental outcomes have been obtained by using that software or components such as DSP, IGBTs, the drivers of these switches, heat-sinks etc.

4.1 DSP

During the process for obtaining the experimental results, eZdsp F28335 board with Code Composer Studio DSK tools and power supply, which is from Spectrum DIGITAL Incorporated as shown in Fig. 4.1, is used in order to make implementation of PWM signals. In the case of the needs for Analog to Digital Converter (ADC) to acquire the signals from the circuits' output, this device can be useful as well.

In this board, TMS320F28335 Digital Signal Controller (DSC) from Texas Instruments (TI) is embedded. Fig. 4.2 depicts the basic configuration of the eZdsp F28335. It consists of four main blocks of logic: Analog Interface Connector, Input/Output Interface Connector, On-board Memory, JTAG Interface, and Embedded USB JTAG Controller Interface. The board uses USB port to connect to the computer and its supply voltage is 5 Volts which is converted from the grid via its own power supply converter. The DSP set is programmed by a software, named as Code Composer Studio DSK Tools which incorporates "C" compiler, assembler, linker, and debugger. For this research, the PWM signals are demanded in order to make ON or OFF states for IGBTs or MOESFET modules, so this DSP device is used to obtain required PWMs. eZdsp board has totally six ePWM module and each ePWM has two output signals for PWM: EPWMxA and EPWMxB. These two PWM outputs can be used in either

Fig. 4.1. eZdsp^{TM} F28335 board.

two independent output (with single-edge or dual-edge symmetric operations) or one independent output (with dual-edge asymmetric operation) configurations.

After explaining the basic specifications of this DSP board, it is required to state how to program and compile it. The DSP platform has its own CD to install Code Composer Studio DSK v3.3 software which is from TI. After installing this CD to a computer, the following steps should be proceeded carefully to make the DSP board worked properly:

- The power supply converter of the board, which comes with this device, has to be connected to grid voltage and its 5V output cable should be inserted to the board's designated connector, which is shown by P6 on board.
- The device must be connected to computer's USB port via board's J201 connector.

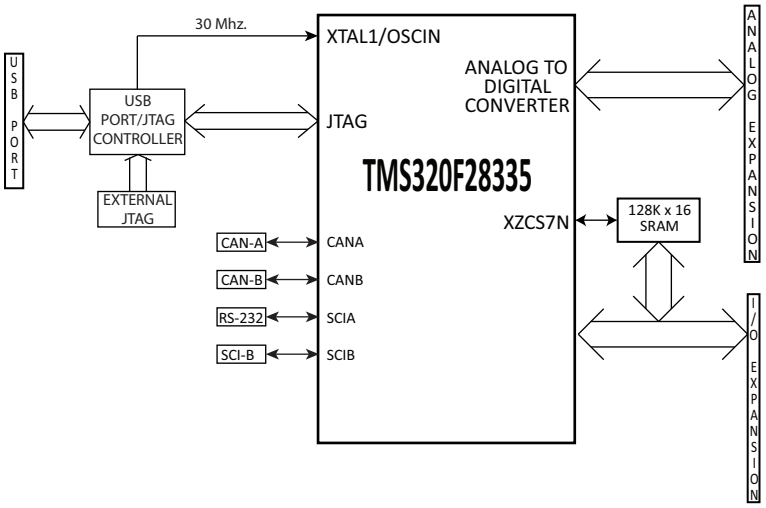


Fig. 4.2. Block diagram of eZdsp^{TM} F28335 board.

- In computer, by clicking to the icon "Setup CCStudio V3.3", eZdsp can be added to Code Composer, which is the specific software of this device.

Doing these steps is only beginning point of working with DSP. As mentioned before, many application of PWMs or designs which requires Analog to Digital Converter (ADC) can be implemented by employing this device. There are a lot of details in the steps of generating PWM output signals, but only some fundamental ones are presented here:

- DSP board has one TMS320F28335 DSC and this DSC includes six ePWM Modules, submodules and signal connections for an ePWM Module is illustrated in Fig. 4.3.

- For each ePWM module there are two output signals, EPWMxA and EPWMxB, which are made available external to the device through the GPIO peripheral and these outputs can be obtained for the users via P8, I/O connectors on the board.

- By configuring the time-base and counter-compare submodules' parameters, the desired codes for this research can be explained below:

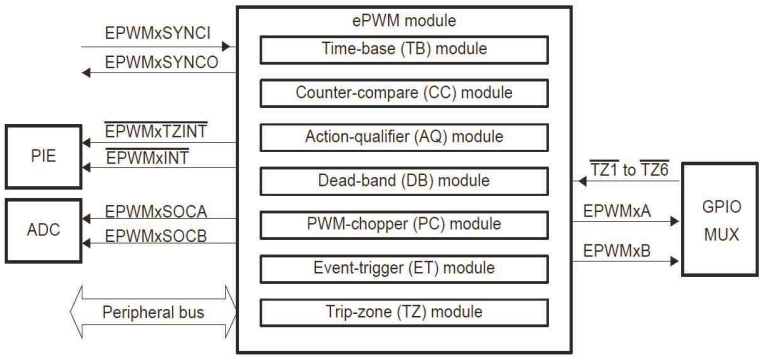


Fig. 4.3. Submodules and connections of signals for an ePWM Module.

- The ePWM timer period for controlling how often events occur is defined by adding the following codes to "DSP2833x_EPwm.c" file:
  - #define EPWM1_TIMER_TBPRD 7500
  - Epwm1Regs.TBPRD = EPWM1_TIMER_TBPRD;
- The time-base counter has three modes of operation, which is chosen by the control register of TBCTL, to count up, down, or up-and-down, illustrated in Fig. 4.4. The parameter is set to up-down count mode in this research.
  - Epwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UPDOWN;
- If synchronization is a requirement between ePWM modules, such as integer multiple frequencies of ePWM module 1, it can be managed by configuring one of them as master and others as slaves. In this research, there is no need for the multiple frequencies between the ePWM modules, so the synchronization of them are coded as disabled and are configured as master module, shown below:
  - Epwm1Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_DISABLE;
  - Epwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE;
- If a phase relationship is demanded with other ePWM modules, in this study it is set to zero, it can be performed by configuring following related parameter:

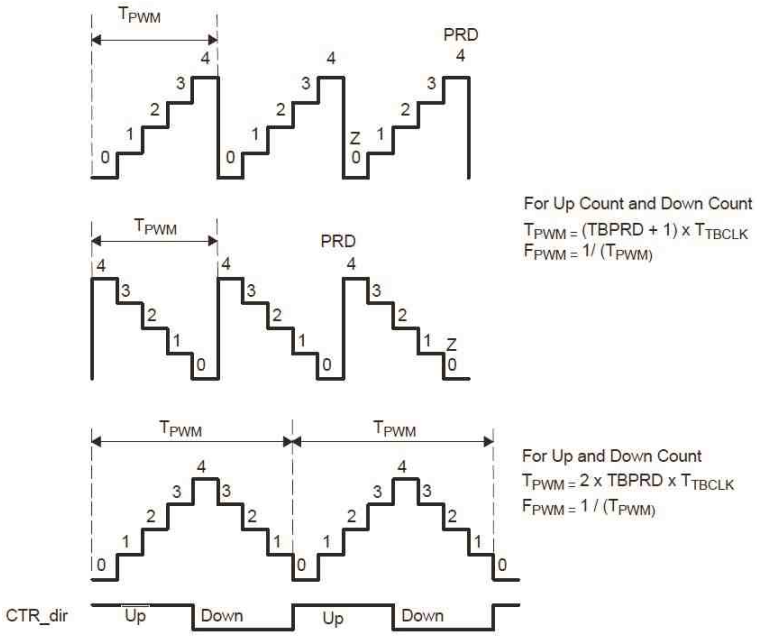


Fig. 4.4. An example of up-count, down-count or up and down count for time-base frequency and period.

  - Epwm1Regs.TBPHS.half.TBPHS = 0x0000;

- By configuring related parameters, the complementary signals can be generated as well. As it mentioned before, each ePWM module has two outputs: A and B. Output A or B can be set complementary by changing the parameters like in the following:

  - EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;
  - EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;

  Above, if the first parameter is made as "AQ_CLEAR" and the second is made "AQ_SET", the complementary signal of the original one can be obtained.

- In analog implementations of obtaining a PWM waveform, mainly two signals are needed: triangular (carrier) and reference (sinusoidal). Configuring parameters of these submodules of DSP, the triangular (carrier) signal can be generated, by selecting operation modes, up, down or up-down.

The codes to generate the sinusoidal signals are written in "C" programming language and added to "Example_2833xEPwmUpDownAQ.c" file. The only remaining step to create desired PWM waveform is comparing reference and carrier signals. The following configuration parameters proceed that duty, respectively, for A and B outputs: and these outputs can be acquired from designated pins via GPIOs on P8 connector embedded to the board as default.

* EPwm1Regs.CMPA.half.CMPA = specified_reference(sine)_signal*7500;
* EPwm1Regs.CMPB = specified_reference(sine)_signal*7500;

The number 7500 in the parameters, above, represents the carrier (triangular) signal's amplitude, which means it changes between 0 and 7500 TBCLK counts, and it can be defined by changing the value in corresponding parameters, which is given in one of the items above.

4.2 Power Semiconductor Switch and Heat-Sink

Basically, switching is needed when it comes to operation of any converter. In industrial applications, insulated gate bipolar transistors (IGBTs) are considirable used in circuits which requires high voltage and current at particular switching frequency. In this research, BSM 75 GB 60 DLC IGBT modules, from the company of Infineon, are implemented as switches to attain experimental results for the converters. The module is depicted in Fig. 4.5 and some of its technical specifications are given below:

- The collector-emitter voltage (V_{CE}) is up to 600 V.
- DC collector current (I_C) at $T_C = 75\,^{\circ}\mathrm{C}$ is up to 75 A and at $T_C = 25\,^{\circ}\mathrm{C}$ is up to 100 A.
- The gate-emitter voltage (V_{GE}) is between -20 and +20 V.
- The delay times for inductive loads: Turn-on ($t_{d,on}$) is 63 ns and turn-off ($t_{d,off}$) is 155ns at $25\,^{\circ}\mathrm{C}$.

Fig. 4.5. Infineon BSM 75 GB 60 DLC IGBT Module.

The IGBT Module has two switches as illustrated in its circuit diagram, Fig. 4.6. The signals for the gate-emitter and collector is obtained via the base board in which the driver of this IGBT is embedded by the user. More information about this part is in the next section.

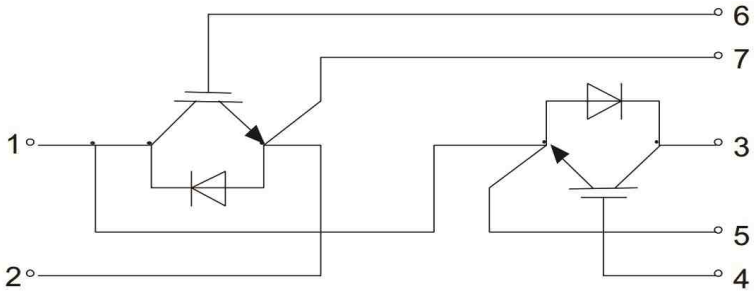


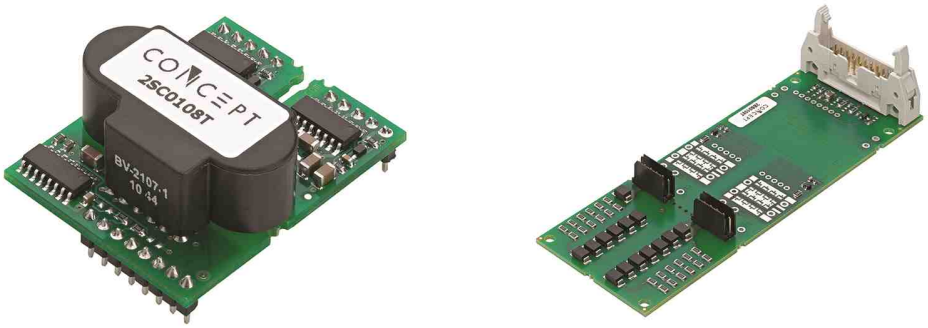
Fig. 4.6. Circuit diagram of BSM 75 GB 60 DLC IGBT Module.

As a nature of the systems through which current goes, the problem of increase of the temperature appears. Since the IGBT modules deal with high current rates in this study, up to 75A, they are mounted to an extruded aluminium heat sink which is $36cm$x$14cm$x$4cm$ as shown in Fig. 4.7. There is still some air gap, which acts as a thermal insulator, between IGBT modules and heat sink, even if IGBTS are mounted firmly to the surface of heatsink. To eliminate this air from the interface area and to give a mechanical strength to the bond between the heat sink and IGBT modules, a thermal compound is utilized in the attaching of heat sink and IGBTs.

Fig. 4.7. Aluminium Heat-Sink.

4.3 Driver of the IGBT and Driver's Base Board

Since there are many more alternative ways to drive IGBT, beacuse of its distinctive features, 2SC0108T2Ax-17 dual channel core driver, shown in Fig 4.8, and its base board 2BB0108T are used in this study. Some of the functions of driver and its integrated base board is presented in this section.



(a) (b)

Fig. 4.8. Driver of the IGBT and its base board. (a) driver core. (b) integrated base board.

The 2SC0108T2Ax-17 is a low-cost complete two channel driver, the block diagram of it is depicted in Fig. 4.9. Also, this driver can be used in many different applications, such as, solar and wind power converters, auxiliary converters for traction, and parallel-connected IGBT implementations. It is designed for applications which requires high reliability and to drive IGBT modules up to $600A/1200V$ or $450A/1700V$ DC collector currents and blocking voltages. The 2SC0108T2Ax-17 is a driver which has not only two channel, but also isolated DC/DC converter and short-circuit protection as well as monitoring of supply voltage, which is DC $15V$. Two output channels of this core are electrically isolated from the each other. It is versatile in small and medium power applications as an ideal driver platform due to the available $1W$ drive power and an output current of $8A$ on each of its channels. This driver has interface for input voltage between $3.3V$ and $15V$ logic level and, also, it generates gate-emitter voltage which swings from $+15V$ to $-8V$ for semiconductor devices. In Fig. 4.10, the connectors of the interface circuitry of the primary side, which is connected to DSP, and the secondary side, which is connected to IGBT modules, are illustrated.

The primary side interface of the core driver 2SC0108T is embedded with an 8-pin interface connector which has terminals for power-supply, signal inputs, status outputs for fault returns, mode selection input: half-bridge mode or direct mode, and an input to set the blocking time. By connecting a resistor to GND, the operating mode can be selected as:

- If direct mode is selected, each of channels is independent and channel 1 is directly driven by INA while channel 2 is driven by INB.

- If half-bridge mode is selected, INA behaves as the drive signal input while INB acts as the enable input. In this mode, complementary signals can be generated as shown in Fig 4.11. If INB is connected to 15V, when channel 1 is turned ON, channel 2 is turned OFF after a dead time and vice versa. This dead time can be determined by assembling gate resistors to basic board 2BB0108T.

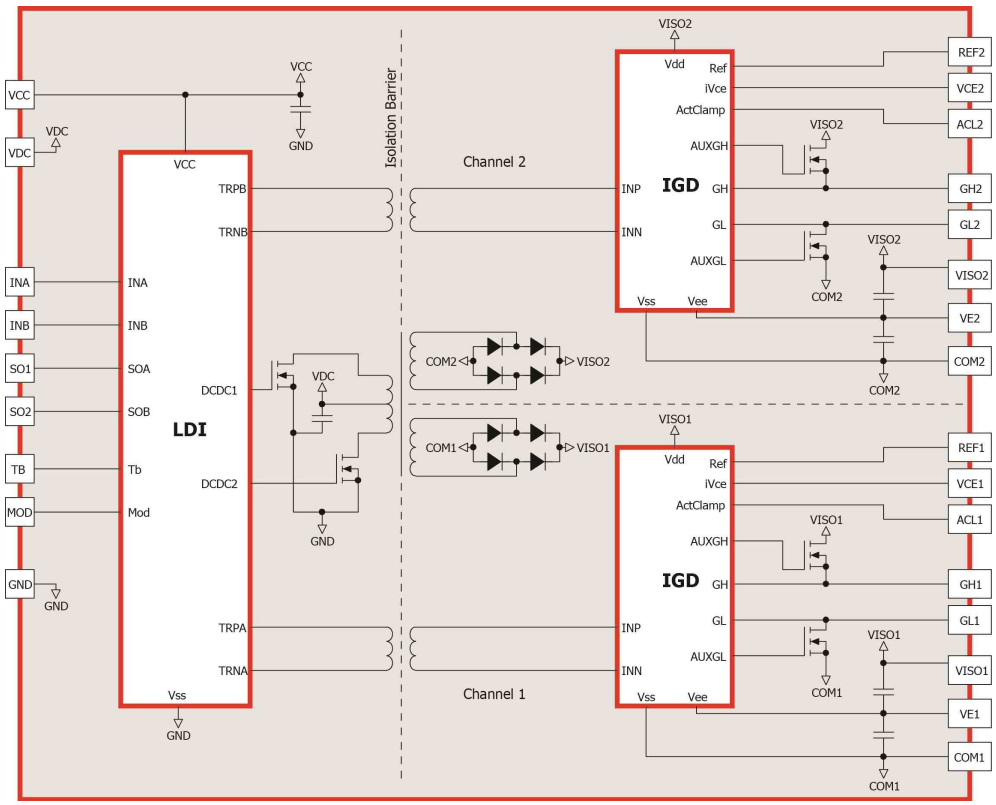
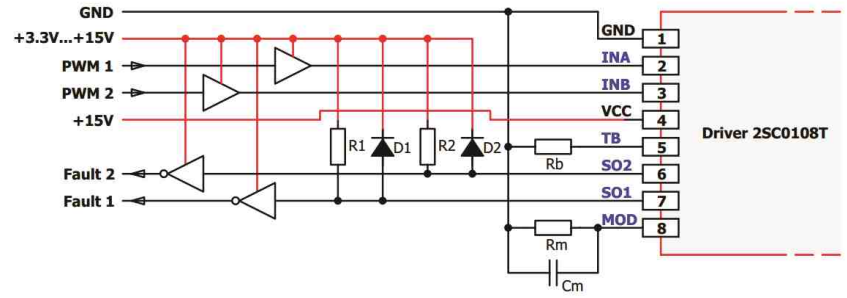
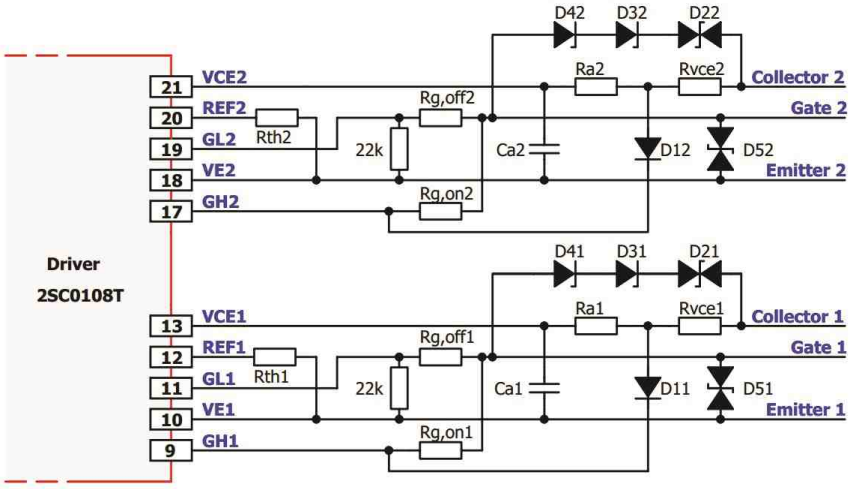


Fig. 4.9. Block diagram of the driver 2SC0108T.

INA and INB are pins for drive inputs, like PWM signals from DSP or controller. These two inputs safely recognize signals which are whole logic-level between 3.3V and 15V. SO1 and SO2 are pins for determining if there is any fault in the circuit. In the condition of no fault, these two outputs have high impedance and goes to a voltage of about 4V. When a fault condition is detected, the related status output goes to GND level. Primary side supply undervoltage, secondary side supply undervoltage, IGBT short-circuit or overcurrent can be counted as fault conditions. The terminal TB is employed for setting the blocking time which is calculated by a specific equation, details are given in driver's application manual. On the each secondary side of driver 2SC0108T, there is a 5-pin interface connector. The emitter, collector and gate terminals, which are fundamental needs for making IGBTs worked, can be obtained from these corresponding pins.



(a)



(b)

Fig. 4.10. User interface of the driver 2SC0108T. (a) primary side. (b) secondary side.

The base board 2BB0108T consists of three electrical interfaces, which is shown in Fig 4.13. The driver 2SC0108T is assembled to this basic board. On the base board, X1 and X2 are output connectors which are connected to the gate, collector and emitter of the IGBT module in the designated order. X3 is input terminal which is attached to DSP and 15V power supply,shown in Fig. 4.12, via a male 20-pin flat connector. Th ground pins of DSP, core driver, base board and power supply should be connected to the same GND point. Since there are many connections between these devices, to use less wire and to make that ground connections common, the

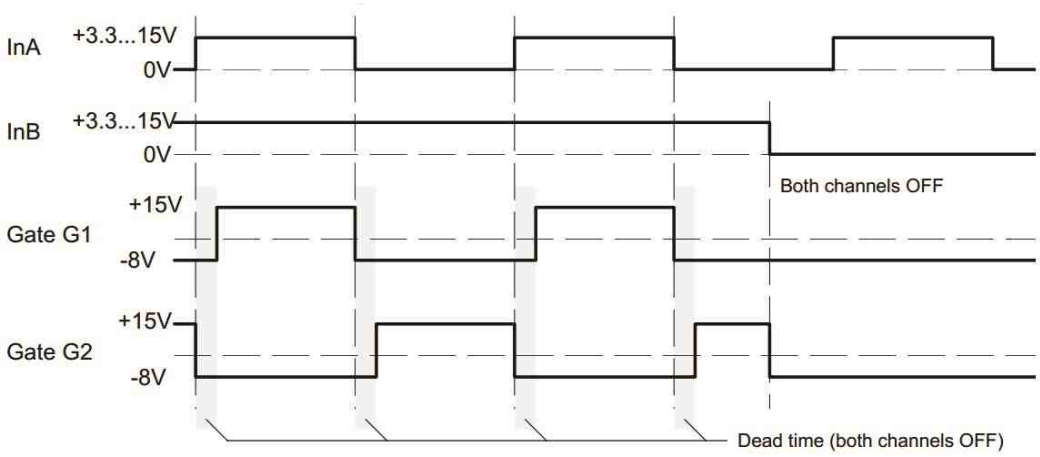


Fig. 4.11. Complementary signal in half-bridge mode.

printed circuit board is used which is depicted in Fig. 4.14 to connect all related device's pins each other.

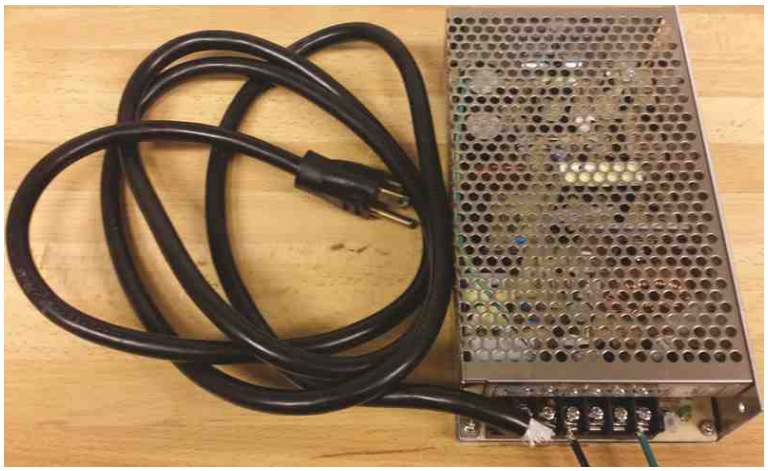


Fig. 4.12. 15V power supply.

4.4 Voltage Sources, Electrolytic Capacitors and Load Components

In the experimental setup of the proposed converters, the power source type, DC or AC, for the IGBT modules depend on the applications. In this research, the DC

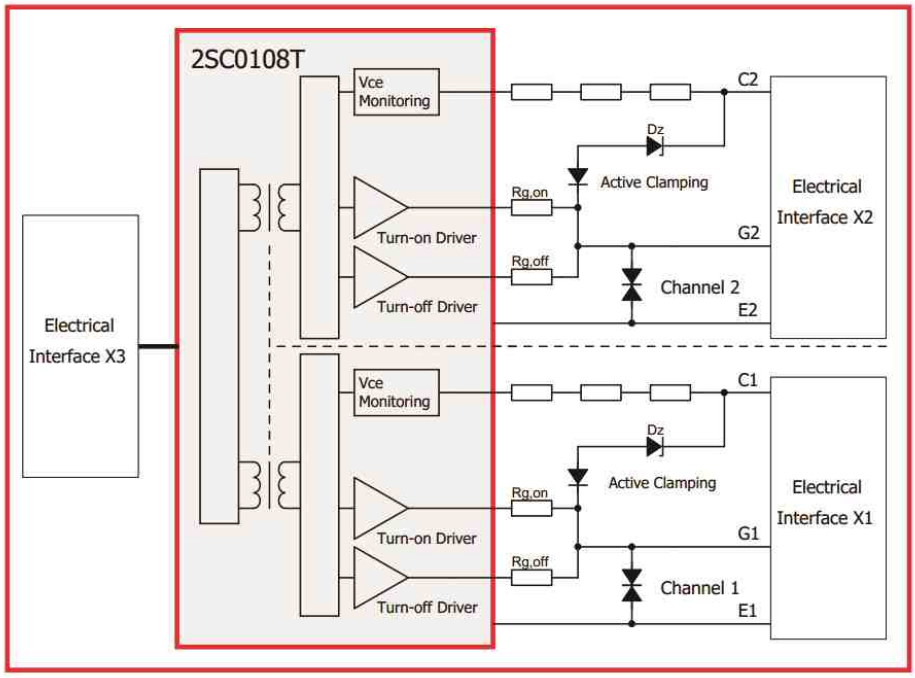


Fig. 4.13. Basic schematic of the 2BB0108T base board.

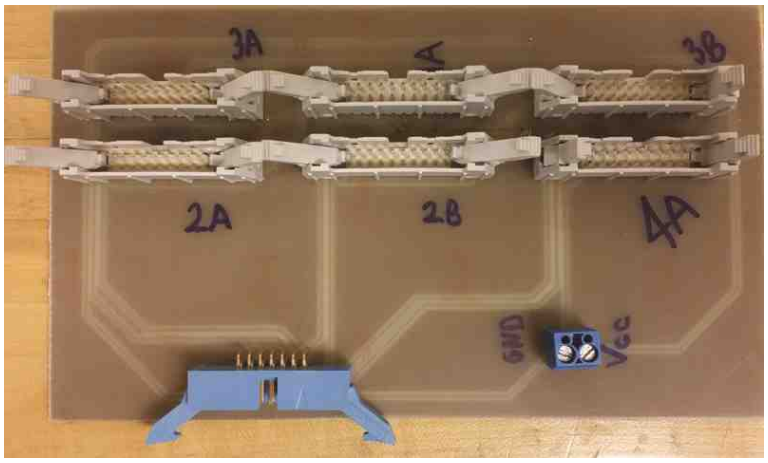


Fig. 4.14. Integrated printed circuit board.

sources are needed, so the source in DC mode and the battery are used, which are given in Fig. 4.15 (a) and (b) respectively. The main power supply has two channels, each of them has adjustable AC or DC voltage mode up to 135V. An 12V 18Ah battery is used as secondary DC source.

(a) (b)

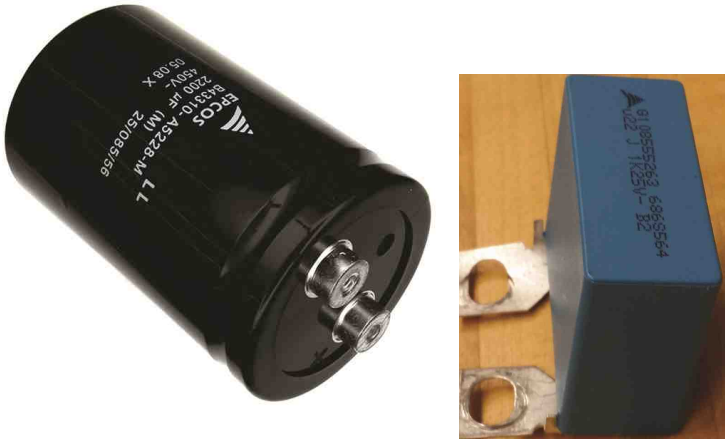
Fig. 4.15. DC sources: (a) main power source. (b) 12.5V battery.

The voltage source is a raw rectified DC supply, so it needs to be smoothed by the electrolytic capacitors. Also, these capactiors help to prevent the switching network from oscillating at an inappropriate moment. To do these duties, and, to use as flying capacitors as well, EPCOS 2200μF aluminum electrolytic capacitor, which is illustrated in Fig. 4.16(a), is employed in this study. Also, Fig. 4.16(b) shows film capacitor, utilized, which are connected parallel to voltage source's positive and negative outputs to reduce the effect of high variation of the voltage ($\frac{dv}{dt}$) in the implementations of the converters.

As inductance, one phase of the three-phase motor is employed, and, each has a value of 10Ω power resistor is assembled to the proposed circuits. These elements are shown in Fig.4.17 (a) and (b).

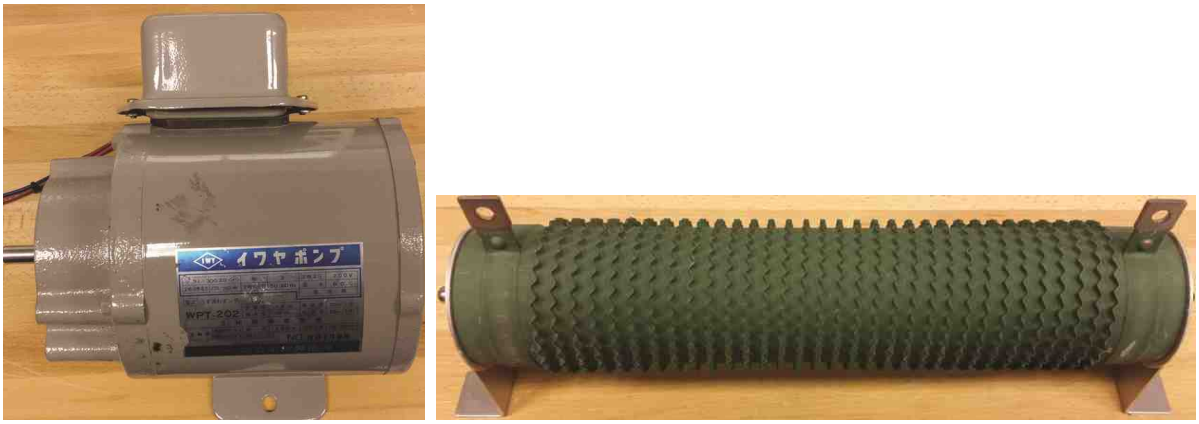
4.5 Experimental Results

The experimental outcomes are introduced in this section for conventional three-level flying capacitor topology and proposed flying capacitor four-level H-Bridge configuration as well. Although the simulations of proposed converter are presented for



(a) (b)

Fig. 4.16. Spectrum of capacitors: (a) electrolytic capacitor. (b) film capacitor.



(a) (b)

Fig. 4.17. Passive elements of circuits: (a) inductance motor. (b) resistor.

both single and three phases, only single phases of them are acquired by the results of experimental setup in this study. The setup for experiments is shown in Fig. 4.18. To obtain the results, some steps were followed during the process of obtaining results, which are given below:

- Taken safety measures before starting to each experiment.

- Checked the wires and connections of the IGBTs and all other equipments.
- Plugged the DSP device in and connected its output connector to the PCB via a 20-pin flat cable.
- Turned the value of 15V power supply on.
- Turned on DC source.
- Connected the oscilloscope probes to the outputs desired to measure.
- Run the codes from the Code-Composer platform via the computer.

4.5.1 Conventional Three-Level Converter

The conventional three-level configuration, illustrated in Fig. 2.1(a), is realized by the experimental setup. The parameters for it as the following:

Load: $R = 20\Omega, \quad L = 5mH, \quad C_1 = 2200\mu$

Each DC source was set $25V$ and six DC link capacitors were used for each output terminal of the DC source.

PWM signals of the complementary switches were obtained by the capability of 2BB0108T base board which can produce complementary one of a signal via the half-bridge mode. PWM signals for the switches q_1 and q_2 are depicted in Fig. 4.19. The load voltage output and current waveform of the conventional three-level flying-capacitor half-bridge converter are shown in Fig. 4.20(a). Flying capacitor voltage and current signals are depicted in Fig. 4.20(b).

4.5.2 Proposed Converter

The experiment of the proposed flying-capacitor four-level H-Bridge converter is performed for the parameters given below.

Load: $R = 20\Omega, \quad L = 5mH, \quad C = 4400\mu$

For V_2 a DC source which was the value of $25V$, for V_1 and V_3, two $12.5V$ batteries were utilized in this converter topology's experimental setup. In Fig. 4.21, the DSP signals for the switches q_b, q_{1a} and q_{2a} are illustrated. Fig. 4.22(a) shows the voltage and current of the output, and Fig. 4.22(b) depicts these quantities for flying capacitor. Fig. 4.23 depicts the blocking voltages of the three complementary switches. Also, to demonstrate the ripple differences, the flying-capacitor voltages are indicated in Fig. 4.24 for the two different values of the capacitors in lower level volt/div, which is a function of the oscilloscope.

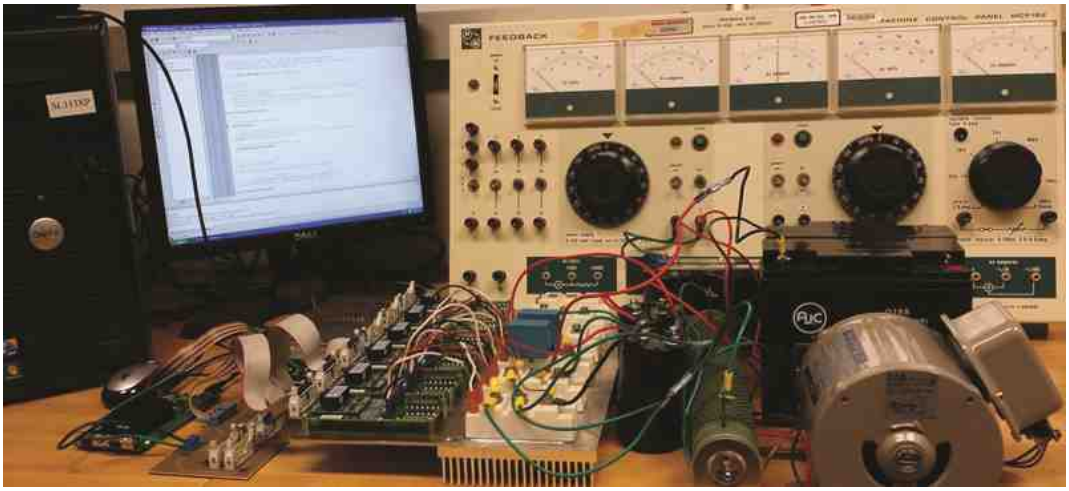


Fig. 4.18. The proof of experimental setup.

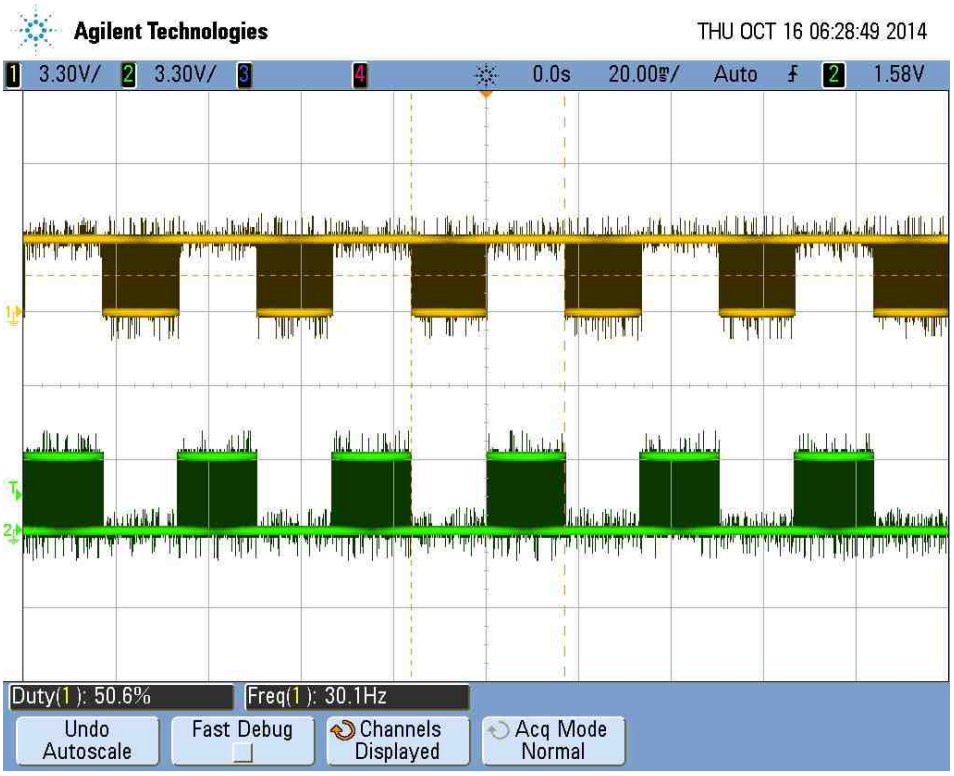
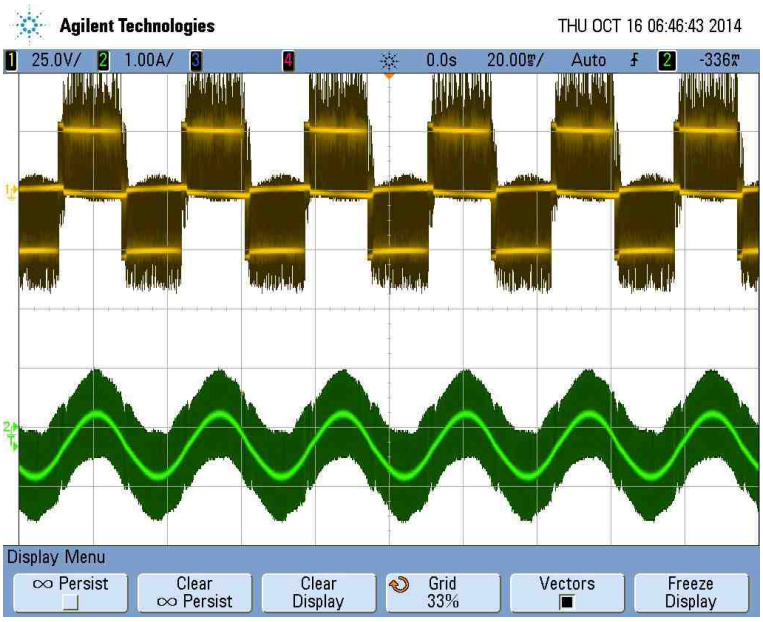
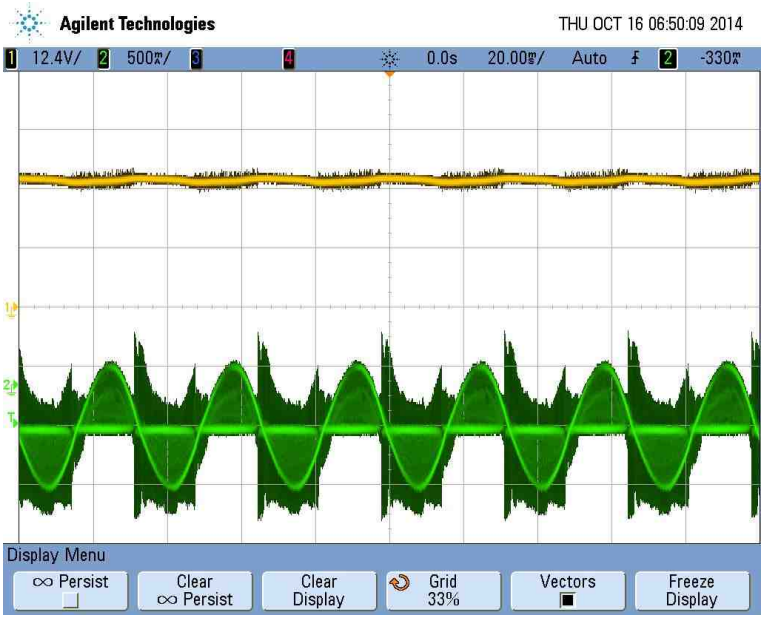


Fig. 4.19. PWM signals of the two switches for the conventional three-level flying-capacitor topology.



(a)



(b)

Fig. 4.20. Voltages and currents of the load and flying-capacitor in the conventional three-level flying-capacitor configuration: (a) load voltage and current. (b) flying-capacitor voltage and current.

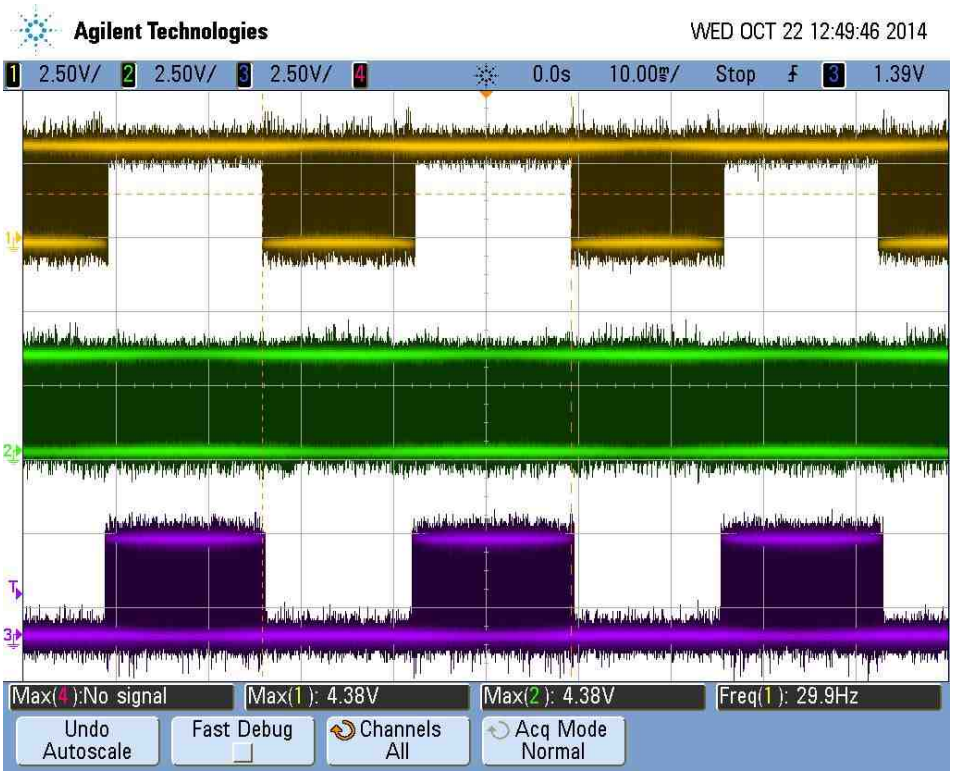
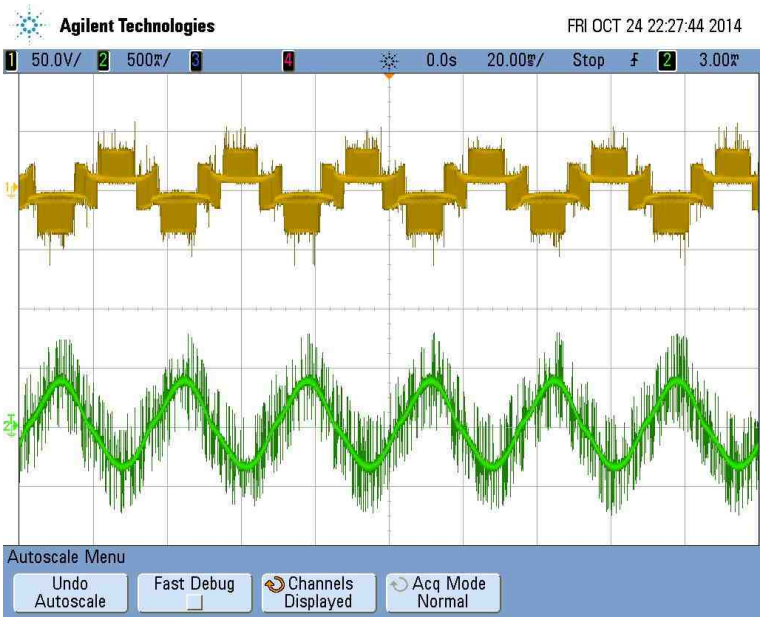
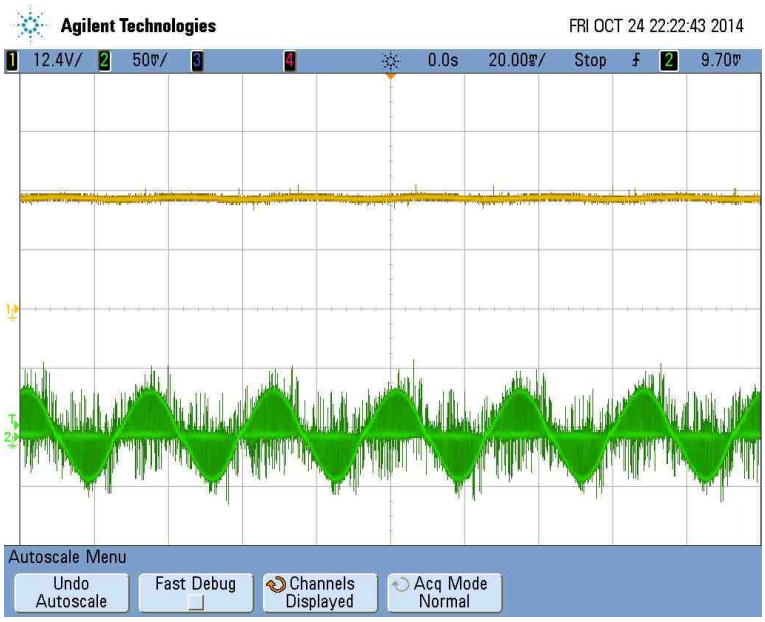


Fig. 4.21. PWM signal of three switches for proposed converter.

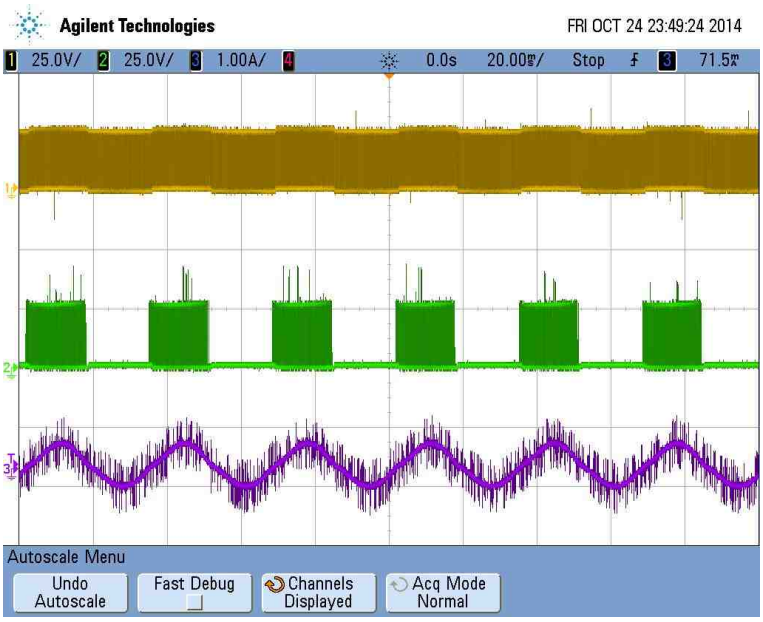


(a)

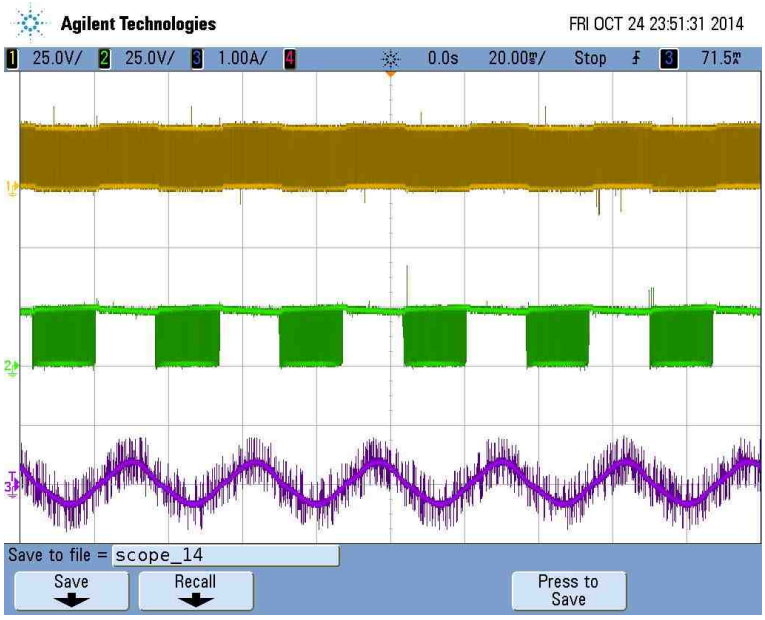


(b)

Fig. 4.22. Voltages and currents of the load and flying-capacitor in the proposed converter topology: (a) load voltage and current. (b) flying-capacitor voltage and current.

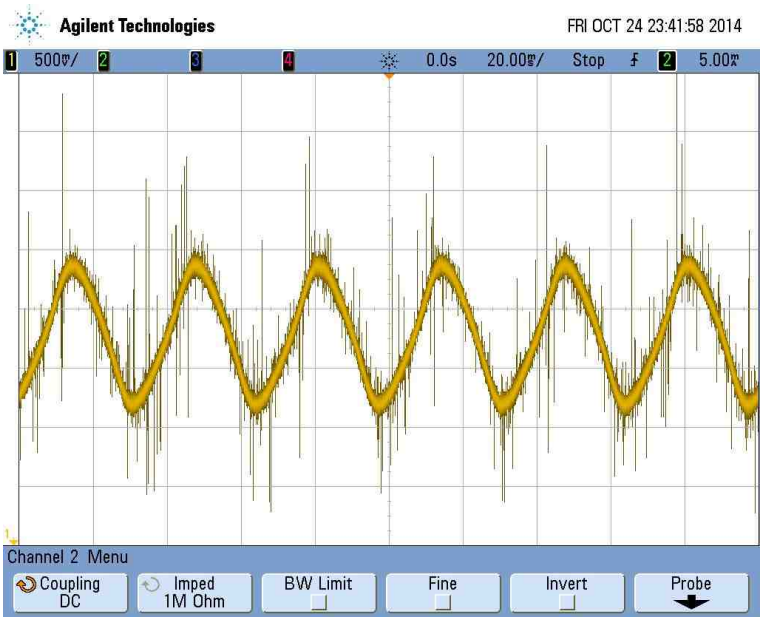


(a)

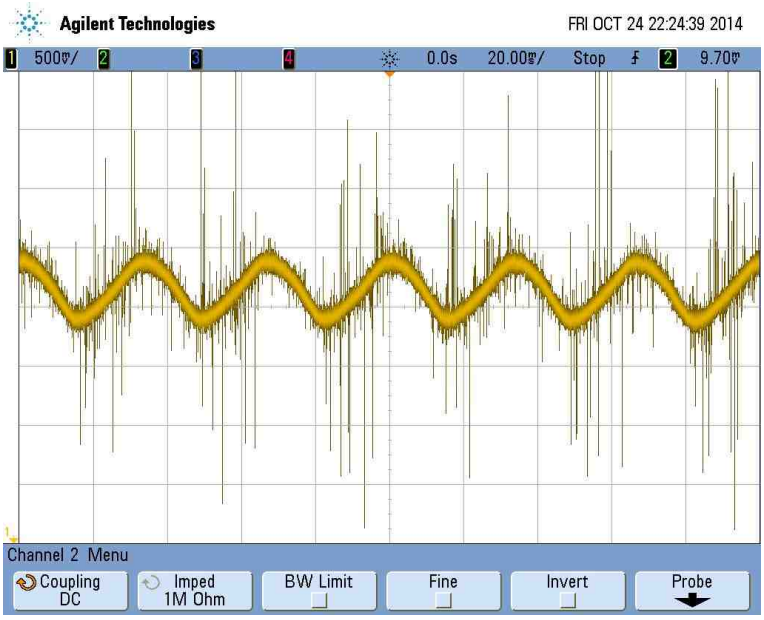


(b)

Fig. 4.23. Blocking voltages of the switches for proposed converter: (a) $\overline{q}_b$ and $\overline{q}_{2a}$. (b) $\overline{q}_b$ and $\overline{q}_{1a}$.



(a)



(b)

Fig. 4.24. Voltage ripples for flying capacitors: (a) $C = 2200\mu$F. (b) $C = 4400\mu$F.

4.6 Conclusion

In this chapter, the hardware, software, the switches, and load components which were used in this research were presented.

For the controller of the switches, a digital signal processor (DSP) was used as the main device to generate PWM signals. The heart of the experiment was generating the desired gate signals, so the background information about the DSP device and its software were explained in detail.

The power semiconductor switches were chosen as insulated gate bipolar transistor (IGBT) for this thesis study. The technical details about the switches and their heat-sink were described.

After obtaining the PWM signals from the DSP device, the driver and its additional circuit board were needed to make the switches worked properly. The chosen driver and its basic-board were expressed explicitly.

The voltage sources and batteries which needed to give the main power to the converters were given in this chapter as well.

Electrolytic capacitors and load components were presented with their technical parameters.

The experimetal setup was shown and experimental results were obtained for the conventional three- and proposed four-level flying-capacitor converter topologies.

5. CONCLUSIONS AND FUTURE WORKS

5.1 Conclusions

In this thesis study, state-of-the-art multilevel converter topologies and their modulation strategies, the implementation of a conventional flying-capacitor converter topology up to four-level, and a novel converter topology which was named four-level flying-capacitor H-Bridge converter were proposed. Also, a comparison between the proposed and the conventional four-level flying-capacitor converter topology was performed. The main advantages of the proposed converter are as the following: (1) the same blocking voltage for the all switches employed in the configuration, (2) no capacitor midpoint connection is needed, (3) reduced number of passive elements as compared to the conventional solution, (4) reduced total DC source value by comparison with the conventional topology.

The level-shift modulation strategy, which was used as the control method of the proposed topology, applied to the conventional flying-capacitor topology.

To make comparisons between the proposed H-Bridge configuration, the simulation results were attained for three- and four-level conventional topology.

The proposed topology and its modulation technique were presented and modeled. The simulation results were obtained for both single- and three-phase versions of it.

The simulation results showed that the proposed topology has the same blocking voltages for the all switches in comparison with the a novel flying-capacitor half-bridge five-level converter topology, which is presented in [91].

In the conventional solution of the flying-capacitor converter topology, the load is connected between the points of the switches' leg and the DC-Link capacitors. This type of connection causes the undesired low frequency current which circulates in the

DC-Link capacitors. In the proposed configuration, the load needs to be attached between the points of the legs of the switches, so that low frequency current was eliminated.

Voltage balancing of the flying capacitors for this kind of topology is an important issue. The number of the flying capacitors was reduced one degree with this topology as compared to the conventional solution. Even without voltage balancing, the proposed converter topology gave promising results.

To obtain the output voltages with the same value, the total value of $1.33V_{dc}$ DC source was used in the proposed converter topology, while the total value of $2V_{dc}$ DC source is needed in the conventional topology. This result may be useful for some DC/AC converter applications of hybrid electric vehicles.

Finally, the simulation results and the theoretical expectations of the proposed converter topology were validated by performing the experiment.

5.2 Future Works

This research needs to be studied on future works as follows:

- The voltage balancing problem of the flying capacitors. Although the simulation and experimental results are not adverse in terms of the effect of the flying capacitors' charging and discharging cycles, this still needs to be worked on and developed. There are two methods for performing this balancing issue: natural or a control-based balancing.

- Calculation of the losses for the conventional and proposed topologies, and making a comparison between them.

- Validating the simulation results of the three-phase version of the proposed configuration by collecting the experimental results.

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