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ENERGY CONVERSION UNIT WITH OPTIMIZED WAVEFORM GENERATION

A Thesis

Submitted to the Faculty

of

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by

Sally Sajadian

In Partial Fulfillment of the

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To my mother and my sister.

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ABSTRACT

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The substantial increase demand for electrical energy requires high efficient apparatus dealing with energy conversion. Several technologies have been suggested to implement power supplies with higher efficiency, such as multilevel and interleaved converters. This thesis proposes an energy conversion unit with an optimized number of output voltage levels per number of switches (nL/nS). The proposed five-level four-switch per phase converter has $nL/nS = 5/4$ which is by far the best relationship among the converters presented in technical literature. A comprehensive literature review on existing five-level converter topologies is done to compare the proposed topology with conventional multilevel converters. The most important characteristics of the proposed configuration are: (i) reduced number of semiconductor devices, while keeping a high number of levels at the output converter side, (ii) only one DC source without any need to balance capacitor voltages, (iii) high efficiency, (iv) there is no dead-time requirement for the converters operation, (v) leg isolation procedure with lower stress for the DC-link capacitor. Single-phase and three-phase version of the proposed converter is presented in this thesis. Details regarding the operation of the configuration and modulation strategy are presented, as well as the comparison between the proposed converter and the conventional ones. Simulated results are presented to validate the theoretical expectations. In addition a fault tolerant converter based on proposed topology for micro-grid systems is presented.

A hybrid pulse-width-modulation for the pre-fault operation and transition from the pre-fault to post-fault operation will be discussed. Selected steady-state and transient results are demonstrated to validate the theoretical modeling.

1. INTRODUCTION

The connection of different renewable energy sources to the grid using high efficient power electronics converters is a very important topic nowadays considering the increasing energy demands [1, 2]. Among the renewable energy systems, Photovoltaic (PV) systems have become feasible alternatives to meet environmental protection requirements and electricity demands. Also power converters are used in various sectors, ranging from industrial to residential applications [3, 4]. Power converters enable the efficient interconnection of different power sources such as renewable energy sources and storage systems to load and/or power the grid.

Power converters are made of power semiconductor switches and passive components. The increase in the power that needs to be managed by systems such as motor drives and distributed generation leads to the use of more voltage levels, leading to more complex structures based on a single and multi-cell converter such as multilevel converters. Photovoltaic systems are a very interesting example of power converter applications because it is not possible to deliver power from the PV module to the grid without a power conversion stage [5]. The use of power converters can improve the stability and power quality of the grid [6, 7].

Fig. 1.1 illustrates the general schematic of a grid connected photovoltaic system. As it is shown, the PV module is connected to a boosting topology DC/DC converter to ensure the maximum power is harvested and the system is operating at the optimal point [8]. Then it feeds power to a DC/AC converter through a DC-link capacitor. The DC/AC converter also known as inverter synthesizes appropriate voltage/current regulation and converts the DC voltage/current to AC voltage/current for the grid connection. The DC/AC converter is the key element in a PV system. The main focus of this thesis is shown by the dotted box in Fig. 1.1, which is a DC/AC converter.

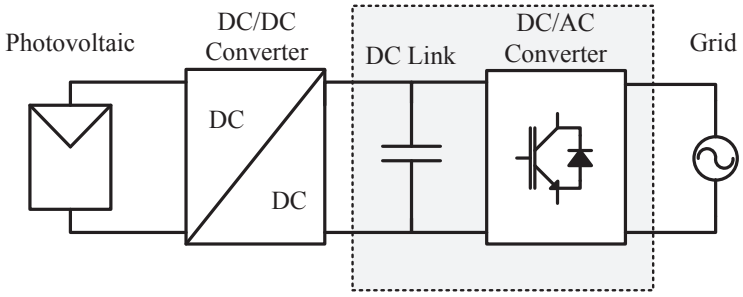


Fig. 1.1. Power converters for photovoltaic applications.

DC/AC converter can be divided into two categories: current source and voltage source converters. Each of these has two main subcategories as illustrated in Fig. 1.2. A voltage source inverter has a constant input voltage with negligible impedance. A current source inverter is fed by an adjustable current from the DC source of high impedance that is from a constant DC source. This thesis focuses on the DC/AC voltage source inverters with ability to synthesize multilevel voltages and with fault tolerance as well. The power converters studied in this thesis are characterized to have couple inductors placed at the output of the converter.

Since the 1990s, IGBT and MOSFET has been mainly used for all categories of DC/AC converters for wide range of applications such as: photovoltaic systems, active power filter, UPS, and motor drive systems. Therefore a wide range of DC/AC topologies are available in literature [9–13]. The new innovative DC/AC converter topologies recently developed are considering the reduction of manufacturing cost and boosting the efficiency [10, 14].

This chapter presents a review of the single-phase and three-phase DC/AC converters, then it moves into the multilevel converter topologies. In addition, the review of fault tolerant converters are presented in the sequence. Finally, the general schematic of the proposed DC/AC multilevel converter topology with an optimized number of levels per number of switches will be presented.

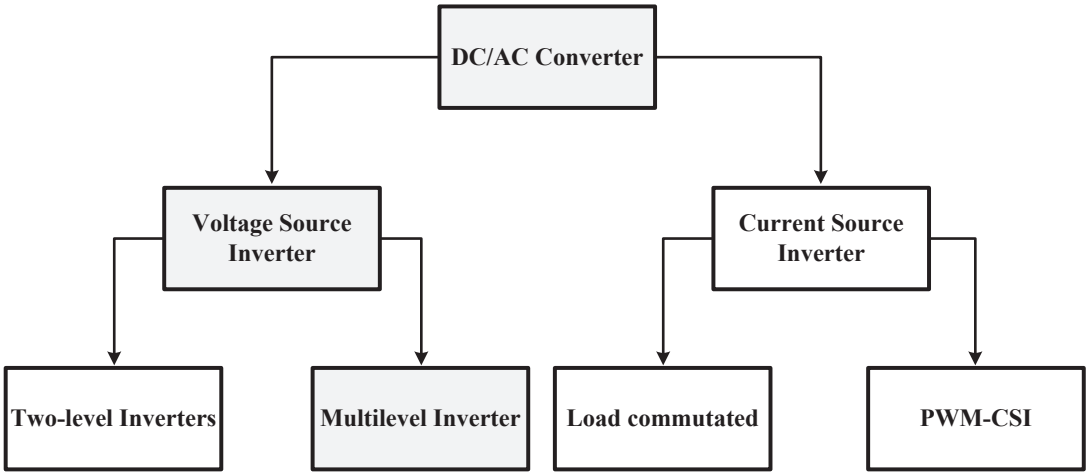


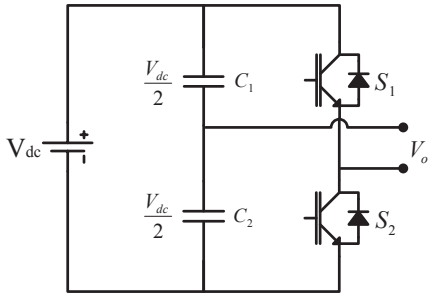
Fig. 1.2. Classification of DC/AC converters.

1.1 State of the Art

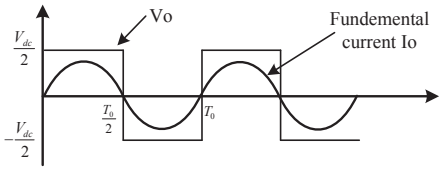
1.1.1 Singe-phase DC/AC Converter

A standard single-phase DC/AC converter can be in the half-bridge or full-bridge configuration, Figs. 1.3 (a) and 1.4 (b), respectively. A single-phase full-bridge converter consists of four switching devices. In the half-bridge topology the input DC voltage is split in two equal parts through capacitors C_1 and C_2. For the half-bridge converter the transistors turn on and off alternately, where each provide opposite polarity of V_{dc} across the load. The load is connected between the mid-point of the DC-link capacitor and the junction point of the two switches. The output voltage and fundamental current of the half-bridge converter is depicted in Fig. 1.3 (b). The shape of the output current is highly dependent on the type of the load, for a resistive load the output current matches the shape of the output voltage. However, for an inductive load the output current has a more sinusoidal shape due to the filtering property of the inductor. Also, for an inductive load one of the switches should always conduct to maintain continuity of the load. If the switches S_1 and S_2 are

turned on alternately with a duty ration of 0.5, the load voltage V_0 will be a square wave with a peak voltage equal to half of the input DC voltage. The output voltage is $\frac{1}{2}V_{dc}$ when the S_1 is turned ON and $-\frac{1}{2}V_{dc}$ when S_2 is turned ON.



(a)



(b)

Fig. 1.3. (a) Single-phase half-bridge DC/AC converter. (b) Output voltage and fundamental current of the half-bridge converter.

The peak to peak magnitude of the fundamental frequency of the square wave output voltage is equal to $\frac{4}{\pi}V_{dc}$. The rms value of the output voltage is given by:

$$V_0 = (\frac{2}{T_0}\int_0^{\frac{T_0}{2}} \frac{V_{dc}^2}{4})^{\frac{1}{2}} = \frac{V_{dc}}{2} \tag{1.1}$$

The steady state for an inductive load the circuit equations are given by:

$$Ri + L\frac{di}{dt} = \frac{1}{2}V_{dc} \text{ for } 0 < t < \frac{T}{2} \tag{1.2}$$

$$Ri + L\frac{di}{dt} = -\frac{1}{2}V_{dc} \text{ for } \frac{T}{2} < t < T \tag{1.3}$$

If the initial value of the current is assumed to be I_0, then by solving (1.2) and (1.3) the instantaneous output current can be determined:

$$i(t) = \frac{0.5V_{dc}}{R}(1 - e^{\frac{-t}{\tau}}) + I_0 e^{\frac{-t}{\tau}} \text{ for } 0 < t < \frac{T}{2} \tag{1.4}$$

$$i(t) = \frac{-0.5V_{dc}}{R}(1 - e^{\frac{-(t-\frac{t}{\tau})}{\tau}}) + [\frac{0.5V_{dc}}{R}(1 - e^{\frac{-t}{2\tau}}) + I_0 e^{\frac{-t}{2\tau}}] \text{ for } 0 < t < \frac{T}{2} \tag{1.5}$$

Equation 1.4 and 1.5 can be simplified as:

$$i(t) = \frac{0.5V_{dc}}{R}\frac{1 + e^{\frac{-T}{2\tau}} - 2e^{\frac{-t}{\tau}}}{1 + e^{\frac{-T}{2\tau}}} \text{ for } 0 < t < \frac{T}{2} \tag{1.6}$$

$$i(t) = \frac{-0.5V_{dc}}{R}\frac{V_{dc}}{R}\frac{e^{\frac{-(t-\frac{T}{2})}{\tau}}}{1 + e^{\frac{-T}{\tau}}} \text{ for } 0 < t < \frac{T}{2} \tag{1.7}$$

The single-phase full-bridge DC/AC converter can be thought of as two half-bridge circuits sharing the same DC bus. The full-bridge can generate an output power two times the half-bridge converter with the same input voltage. The full-bridge converter has two pole voltages V_{a0} and V_{b0}, both of the voltage poles are a square waveform however they usually have some phase difference. The single-phase load is connected between the points A and B of converter illustrated in Fig. 1.4 (a). For the full-bridge DC/AC converter illustrated in Fig. 1.4 (a), switches $S_{11} - S_{22}$ and $S_{21} - S_{12}$ are turn on and off alternately, where each pair provides opposite polarity of V_{dc} across the load. The circuit can produce three voltage levels in response to the switching signal, regardless of the current direction. The voltage equations for the full-bridge DC/AC converter are given by:

$$\frac{V_{dc}}{2}(S_{11} - S_{12}) = V_{an} + V_{n0} = V_{a0} \tag{1.8}$$

$$\frac{V_{dc}}{2}(S_{11} - S_{22}) = V_{bn} + V_{n0} = V_{b0} \tag{1.9}$$

$$V_{ab} = V_{an} - V_{bn} \tag{1.10}$$

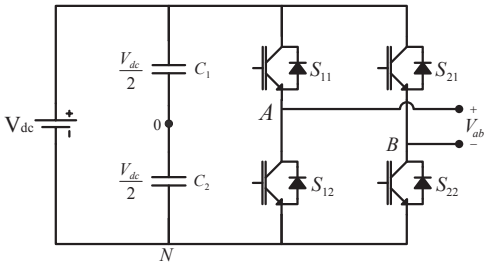
The voltages V_{an} and V_{bn} are the output voltages from phases A and B to an arbitrary point n, V_{no} is the neutral voltage between point n and the middle point of the input DC voltage. Finally the load voltage V_{ab} can be determined using (1.10). For an inductive load, the switch must be bidirectional. The steady state, the instantaneous current for an inductive load can be determined by using similar analysis previously applied for half-bridge converter:

$$i(t) = \frac{V_{dc}}{R} + (I_{min} - \frac{V_{dc}}{R})e^{\frac{-t}{\tau}} \text{ for } 0 < t < \frac{T}{2} \tag{1.11}$$

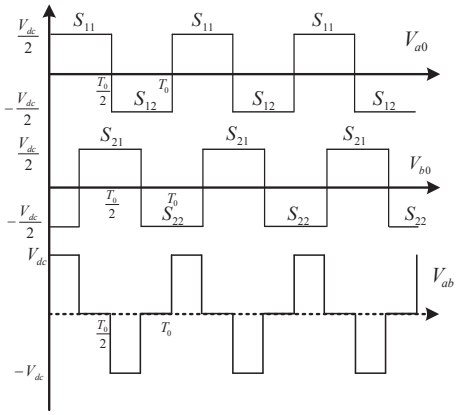
$$i(t) = -\frac{V_{dc}}{R} + (I_{max} + \frac{V_{dc}}{R})e^{-\frac{t-\frac{T}{2}}{\tau}} \text{ for } \frac{T}{2} < t < T \tag{1.12}$$

$$I_{max} = I_{min} = \frac{V_{dc}}{R}\frac{1 - e^{\frac{-T}{2\tau}}}{1 + \frac{-T}{2\tau}} \tag{1.13}$$

As it is illustrated by the voltage waveforms of Fig. 1.4 (b) for a full-bridge DC/AC converter with Pulse Width Modulation (PWM) [15] scheme, the output voltage is swung between V_{dc} and $-V_{dc}$. PWM produces an output waveform with spectrum consisting of a wanted waveform components plus distorted components around the switching frequency and its multiples [15]. Some sort of filtering is required to extract the desired component and eliminate the distorted unwanted components, they usually can introduce significant cost and weight into the design. We should keep in mind that the same time closing the switches $S_{11} - S_{12}$ or $S_{21} - S_{22}$ would cause a short circuit. Therefore when using these IGBT switches in experiment a dead-time or blanking time is implemented to avoid short circuit. The dead-time may cause a nonlinearity in the system, which can significantly increase total harmonic distortion (THD) and lead to discontinuous conduction states at zero-current crossing [16, 17]. The freewheeling diode of the IGBT switches prevent current to follow if all switches are open, these diodes permit lagging current to follow in inductive loads. We should note that $V_{ab} = 0$ in voltage waveforms of Fig. 1.4 (b) is not required but it can be used to reduce the rms value of the load voltage. The switches in the DC/AC converter have a very small thermal time constant and they cannot overheat more than a few milli-seconds. Consequently, the thermal limit may be reached, however,



(a)



(b)

Fig. 1.4. (a) Single-phase full-bridge DC/AC converter. (b) Phase and output voltages.

the load current passes through the switches only in alternate half cycles. It may be pointed out that each inverter switch consists of a controlled switch in anti-parallel with a diode. The distribution of current between the diode and the controlled switch will depend on the load power factor at the operating frequency. In general, both the diodes as well as the controlled switch should be rated to carry the peak load current.

1.1.2 Three-phase DC/AC Converter

Converters for three-phase systems consist of three power-poles as it is shown in Fig. 1.5 [3], type of switches depends on the application, in this figure a general form of switch is used . The application may be motor drives, three-phase Uninterruptible Power Supply (UPS) or in a three-phase utility system.

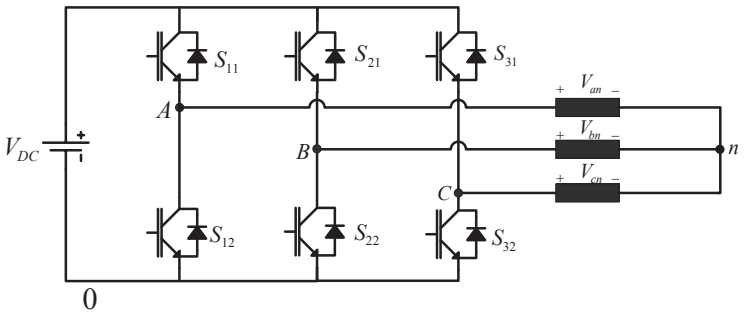


Fig. 1.5. Three-phase full-bridge DC/AC converter.

In Fig. 1.5, v^*_{an}, v^*_{bn}, and v^*_{cn} are the voltages to be synthesized:

$$v^*_{an} = \hat{V} sin(\omega t) \tag{1.14}$$

$$v^*_{bn} = \hat{V} sin(\omega t - 120^\circ) \tag{1.15}$$

$$v^*_{cn} = \hat{V} sin(\omega t - 240^\circ) \tag{1.16}$$

In order to obtain the averaged current drawn per phase from the voltage port of the switching power pole, we assume the inductive load is to be sinusoidal but lagging with respect to the switching cycle averaged voltages per phase by angle θ [3], by keeping in mind 1.5:

$$i_a = \hat{I} sin(\omega t - \theta) \tag{1.17}$$

$$i_b = \hat{I} sin(\omega t - \theta - 120^\circ) \tag{1.18}$$

$$i_c = \hat{I} sin(\omega t - \theta - 240^\circ) \tag{1.19}$$

Thus the averaged output power is given by:

$$p_0 = v_{aN}i_a + v_{bN}i_b + v_{cN}i_c \tag{1.20}$$

By equating the input and output power we have:

$$i_d(t)V_{dc} = v_{aN}i_a + v_{bN}i_b + v_{cN}i_c \tag{1.21}$$

$$i_d(t) = \frac{1}{V_{dc}}(v_{an}i_a + v_{bn}i_b + v_{cn}i_c) \tag{1.22}$$

Equation (1.22) shows sum of product of voltages and currents of each phase, which is the power supplied to the inductive load. By substituting equations (1.14-1.16) and (1.17-1.19) into (1.22) we have:

$$\begin{aligned} i_d(t) &= \frac{\hat{V}\hat{I}}{V_{dc}}(sin(\omega t)sin(\omega t - \theta) + sin(\omega t - 120^\circ)sin(\omega t - \theta - 120^\circ) + \\ &= sin(\omega t - 240^\circ)sin(\omega t - \theta - 240^\circ) \end{aligned} \tag{1.23}$$

By simplifying (1.23)

$$i_d(t) = I_d = \frac{3}{2}\frac{\hat{V}\hat{I}}{V_{dc}}cos\theta \tag{1.24}$$

1.1.3 Multilevel Converters

Due to the growing demands for reliable electrical energy resources and abundant requests for high efficiency devices, numerous research groups are studying and developing new solutions and technologies to achieve high performance power converters [18]. In this context, a multilevel converter is an interesting alternative for power conversion, since it allows efficient power supply, suitable for high voltage and high power applications [14,19–34]. Multilevel power converters have been around for more than 40 years [20,35–40]. The multilevel converters have many advantages such as low power dissipation on power switches, low common mode voltages, lower dv/dt to supply lower harmonic contents in output voltage/current, and low electromagnetic interference (EMI) outputs [41,42]. This section presents a brief introduction to the main types of multilevel converters such as diode-clamped and capacitor-clamped inverters.

The early use of multilevel converter was for high-power applications beginning with Neutral Point Clamped (NPC) inverter [19, 43–46]. Multilevel converters have been improved since their first generations to support the desirable characteristics such as reduced waveform distortion and low blocking voltage by switching devices [20, 22, 24, 47–49]. Within the literature, numerous papers can be found dealing with different sample topologies and designs of multilevel converters to improve their performance [10, 50–53]. The three main configurations are diode-clamped (or NPC), flying capacitor, and cascaded multilevel inverters [54, 55].

Recently, multilevel converters have been also used for low power systems; in particular photovoltaic applications because of the possibility to generate the high quality voltage waveforms with semiconductor switches operating near the fundamental frequency [56]. This thesis presents a DC/AC converter topology with an optimized number of levels per number of switches. Each phase of the proposed converter is constituted by four power switches and it is able to generate five levels. The proposed topology illustrated in Fig. 1.6 has an optimized relationship between the number of levels per number of switches, $nL/nS = 5/4$, which is by far the best relationship in the technical literature.

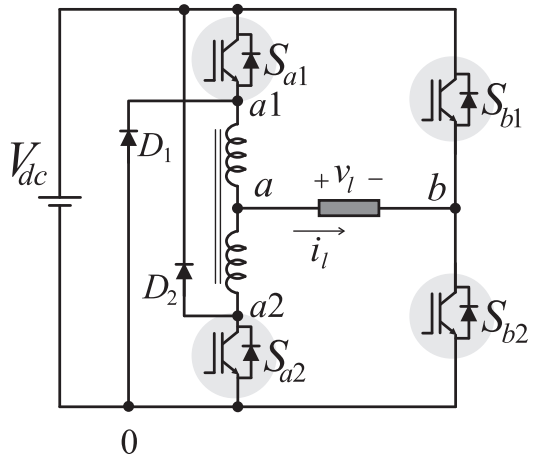


Fig. 1.6. Proposed 5 level 4 switch converter.

The most vital characteristics of the proposed topology in this paper are: (i) reduced number of semiconductor switches utilized in the converter by keeping the high number of levels at the output side of each phase, (ii) no need to control DC-link capacitor voltages as in NPC and flying capacitor topologies and (iii) reduced semiconductor losses which result in a higher efficiency converter.The detail principle of operation and PWM strategy of the proposed converter will be presented in the following chapters of this thesis.

For comparison purposes Fig. 1.7 illustrates some well-known converters able to generate a five-level voltage for a single-phase output. The numbers of levels per number of switches are given either by 5/8 or 5/6, which are less than 5/4 guaranteed by the proposed converter. Commonly most of multilevel converter topologies divide the main DC supply voltage into several smaller DC sources which are used to synthesize an AC voltage into stepped approximation of the required sinusoidal waveform [57].

The converter illustrated in Fig. 1.7 (a) [58] is commonly called Neutral Point Clamped (NPC) converter which is known as the simplest diode clamped inverter. This converter was first used in a three-level converter in which the mid-voltage level was defined as the neutral point [43, 59–62]. The first NPC PWM converter is presented in [19]. The NPC topology is a developed version of a classical two-level converter, this converter can be obtained by adding two new power semiconductor switches to the classical two-level converter topology per leg. As it is illustrated in Fig.1.7 (a) the DC bus voltage is divided by two by using two series connected bulk capacitors. The main difference of this topology with respect to the conventional two-level converter are the diodes, each diodes of the same leg clamp the switch voltage to half the level of DC bus voltage. The neutral point (N) is the middle point of these two capacitors. The purpose of adding the two diodes is to clamp the switch voltage into half of the level of the DC bus voltage. Without these diodes the output voltage levels would not be defined. The mode of operation is similar to a conventional two-level inverter but there are twice the voltage levels in each leg. This topology is able

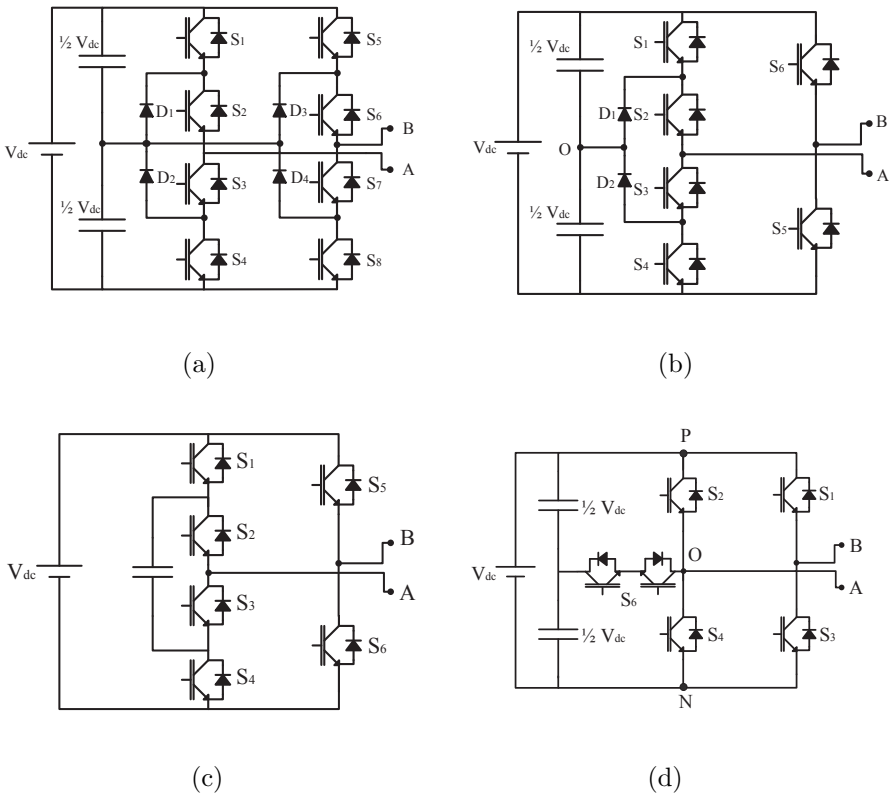


Fig. 1.7. Conventional five-level single-phase configurations with nL/nS given by: (a) 5/8, (b) 5/6, (c) 5/6 and (d) 5/6.

to generate output voltage levels of $\pm V_{dc}$, $\pm 1/2V_{dc}$ and 0. During the positive half cycle, the voltage V_{dc} can be obtained when S_7, S_8, S_1, and S_2 are ON. The voltage $1/2V_{dc}$ can be achieved when S_7, S_8, and S_2 are ON. Finally voltage 0 can be achieved when S_7, S_8, S_3, and S_4 are ON. Similarly during the negative half cycle, the voltage $-V_{dc}$ can be obtained when S_5, S_6, S_3, and S_4 are ON. The voltage $-1/2V_{dc}$ is given when S_5, S_6 , and S_3 are ON. Finally the voltage across load will be 0 when S_5, S_6, S_1, and S_2 are ON. Thus five voltage levels is generated by this topology.

The main disadvantage of this topology is, as the number of levels increases some diodes have to block large voltages. Therefore when the number of levels increases, the required number of diodes makes the system impractical. However, the main advantage of this topology is that only one DC supply is required, but for topologies of more than 3 levels, an extra balancing circuit or multiple DC supplies are required [60–63].

Fig. 1.7 (b) [32] is another topology of the diode clamped inverter, in this topology the number of levels per number of switches is 5/6 however for Fig. 1.7 (a) the number of switches per number of levels is 5/8. By appropriately controlling the switches, the five-level output voltage can be generated [64, 65].

In the topology illustrated in Fig. 1.7 (b), some restrictions should be applied to the switching operation: switches S_6 and S_5 present low frequency operation and cannot be turned-on and turned-off simultaneously; also switches S_2 and S_3 cannot be turned off simultaneously. Therefore by applying a suitable modulation technique, it is possible to obtain five levels of voltages at the output.

Modes of operation for the converter of Fig. 1.7 (b) is discussed in detail in [29,66]. During the positive half cycle switch S_5 is kept ON and Switch S_6 are kept OFF. Thus the voltage level of V_{dc} can be achieved when S_1, S_2, and S_5 is ON. The voltage level of $1/2V_{dc}$ can be achieved when S_2 and S_5 are ON. Finally the load voltage will be zero when S_3, S_4, and S_5 are ON. Similarly during the negative half cycle, the switch S_6 is ON and switch S_5 is kept OFF. Therefore the voltage of $-V_{dc}$ can be achieved when S_3, S_4, and S_6 are ON. The voltage of $-1/2V_{dc}$ can be obtained when S_6 and S_3 are ON. Finally the load voltage will be zero when S_6, S_1, and S_2 are ON.

The unbalanced capacitor voltage, due to the positive and negative flux current in the capacitor midpoint, causes oscillation. In order to mitigate these oscillations either the use of six independent sources or a more complicated control strategy to control the DC-link voltage is required [66].

We should note that by increasing the number of levels, the clamping diodes should block large voltages. Thus by considering that each blocking diode voltage rating is similar to the active device voltage rating, the required number of diodes for an m-level DC/AC converter can be determined by:

$$(m-1) \times (m-2) \tag{1.25}$$

Where m is the number of levels.

The converter illustrated in Fig. 1.7 (c) is commonly called the capacitor-clamped or flying capacitor converter. This topology is an alternative solution of the diode clamped inverter. This converter involves the series connection of capacitor clamped switching cells [67]. In this topology the clamping diodes are not needed. Also only one DC source is needed because this multilevel converter has a switching redundancy within the phase which can be used for balancing the flying capacitors. The major advantage is that without using a transformer the required number of levels can be obtained, thus the cost of the converter reduces. In the capacitor clamped DC/AC converter the capacitors within a phase leg are charged to different voltage levels. The switches within the phase leg are switched on to combine the capacitor voltage levels by taking into consideration that no capacitor is short-circuited and continuous current through the DC-link is maintained for each capacitor [67]. The capacitors must be set up with the required voltage level before applying the modulation scheme as an initial charge [68, 69]. This is one of the drawbacks of this topology because this may complicate the modulation strategy.

The mode of operations of this converter is similar to the converter illustrated in Fig.1.7 (b), but the voltage sharing between the switches is not made by the diodes. The voltage sharing between the switches is done by the means of capacitors, independent capacitors clamp the device voltage to one capacitor voltage level. Same as the converter of Fig. 1.7 (a) and (b), this topology also is able to generate output voltage levels of $\pm V_{dc}, \pm 1/2 V_{dc}$ and 0.

The number of capacitors increases rapidly by increasing the number of levels. Similar to NPC, the capacitor clamped inverter needs a large number of bulk capacitors. By taking this into consideration, the voltage rating of each capacitor is similar to the main power switch thus, for an m-level DC/AC converter the number of clamping capacitors required per phase is [10]:

$$\frac{(m-1)\times(m-2)}{2} \tag{1.26}$$

Where m is the number of levels.

The converter illustrated in Fig. 1.7 (d) is a modified version of the Neutral Point Clamped (NPC) inverter topology, which is formed by a full-bridge with an auxiliary switch to the neutral point [70–72]. This topology is commonly called an Auxiliary-Resonant-Commutated-Pole-Inverter (ARCPI). This topology has six semiconductor switches. It is clear, in this topology, the average number of semiconductors in the current path is lower, since the losses depend mainly on the number of semiconductors used, the modified version of NPC topology has better efficiency [70–72]. Among the soft switching scheme available in literature, the topology illustrated in Fig. 1.7 (d) has been mostly favored due to the small rating auxiliary circuit and full PWM operation [71–73]. However, one of the main drawbacks of this topology is triggering of the auxiliary switches. This requires additional measuring and timing which reduces the overall system reliability [74,75]. In addition, the extra measurements protect the auxiliary switches against over voltage cause circuit complexity [71].

The ARCPI topology is considered as one of the best schemes for high power application [76]. An uncertainty which remains with the basic ARCPI scheme illustrated in Fig. 1.7 (d) is the stability of the DC center voltage as mentioned in [77]. In positive half cycle, the voltage V_{dc} can be achieved when switch S_3 and S_2 are ON. The voltage $1/2V_{dc}$ can be obtained when switch S_3 and S_5 are ON. Finally the voltage across load will be zero when S_3 and S_4 are ON at the same time. During the negative half cycle, the voltage $-V_{dc}$ can be achieved when S_1 and S_4 are ON. The

voltage $-1/2V_{dc}$ can be obtained when S_1 and S_5 are ON. Finally the load voltage will be zero again when S_1 and S_2 are ON simultaneously [78].

1.1.4 Topologies with Fault Tolerance

The main advantages of the proposed multilevel converter when compared with solutions presented in the technical literature are higher number of levels using the same amount of power switching devices (six IGBTs), and no dead-time requirement for the converter's operation, which is an important aspect for high-frequency micro-grid systems [79, 80]. Considering the micro-grid point of view, there are different types of electrical equipment that may suffer with malfunction operation [81, 82] such as: i) distributed sources (PV panels, wind turbines, etc.), ii) storage systems, and iii) power electronics converters, etc. The Micro-grid systems is the realization of small networks in a Distributed Generation (DG) that are capable of optimizing benefits such as load management, demand side managements, and generation curtailment [81]. In order to achieve an acceptable level of reliability in a typical micro-grid system, fault tolerant operations of the system are very important. Indeed, faults in power electronics converters are really important since there are power electronics converters placed everywhere in the micro-grid environment, as observed in Fig. 1.8, where PE generically represents power electronics converters. Fig. 1.8 also shows a micro-grid system with a fault occurring in the DC/AC converter interfacing PV panel and the AC bus the fault tolerant converter considered is illustrated in Fig. 1.9. In fact, the improvement and development of the micro-grid systems reliability is critical for the optimal operation of electrical power produced by renewable energy sources such as photovoltaic and wind energy in micro-grid systems.

Specific kinds of faults can occur in these types of converters, for example, faults occurring in the power converter itself (open-circuit and short-circuit failures occurring in the converter power devices) or in the control subsystem. It is estimated that about 38% of the faults in voltage source conversion systems are due to failures of

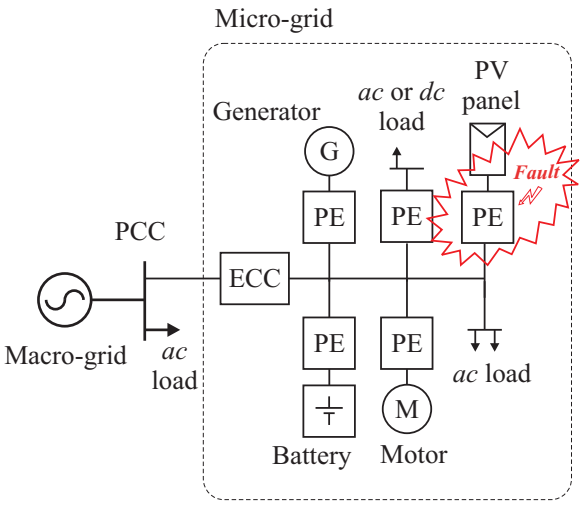


Fig. 1.8. Microgrid system facing a fault problem in the DC/AC converter.

power devices, which can be broadly categorized as short-circuit faults and open-switch faults [83, 84]. For a couple of decades, fault tolerant architecture have been introduced and developed gaining attention, they are commonly not complicated in terms of hardware topology and control [85–94].

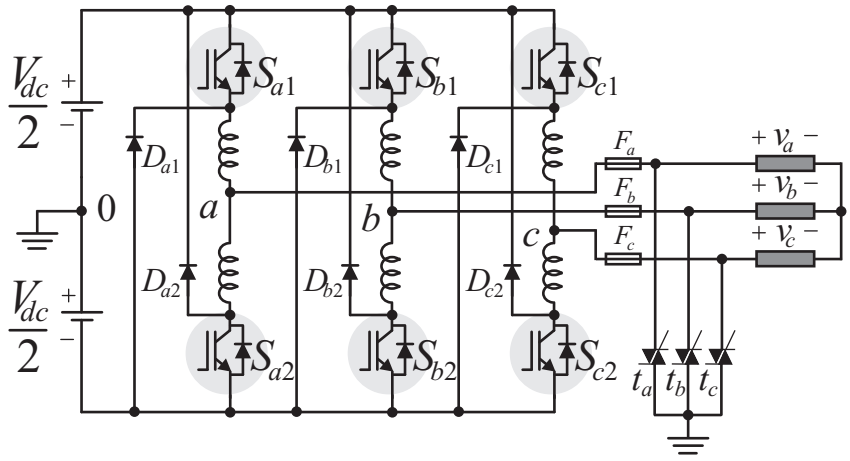


Fig. 1.9. DC/AC fault tolerant converter.

This thesis presents a fault tolerant converter designed for low power applications, as required in a microgrid system [95]. Selected steady-state and transient

outcomes are presented to validate the theoretical expectations. Furthermore, this thesis presents a hybrid pulse width modulation for the pre-fault operation as well as fault detection and leg-isolation procedure. Simulation results demonstrate the validity of the proposed method.

1.2 Continuation of the Work

The control of power electronics converters has been extensively studied in literature. There are several modulation techniques for multi-level inverters such as: space vector modulation (SVM) and pulse width modulation (PWM) [96–100]. Classical linear controllers when combined with a modulation strategy have become the most common used control schemes in industrial power converters [5, 25, 27, 101–104]. In this thesis, a detailed procedure of the modulation strategy for the proposed converter will be presented. However the closed loop control of the proposed converter under load variation is not covered in this thesis. Design of the closed loop controller for the proposed multilevel inverter is the future work of this thesis.

Closed loop current control of the multilevel inverter compensates for circuit non-idealities and performs the desired current tracking. The modulating signal at the input of the PWM will be the function of the actual load current which will be measured by current sensors. Given a modulation stage for the converter, any linear controller can be used with the proposed converter, the most common choice is a proportional-integral (PI) controller. The main control requirement is the dynamic performance and stability of the system [5, 15, 105]. Design of the closed loop control for the proposed converter is not straight forward and it has several challenges [5, 48]:

1. Fast dynamic for reference following under load variation with the smallest possible error.

2. Commonly the power electronics converters generate harmonic content which are measured as THD, the harmonic content introduced by the modulation and control strategy should be minimized.

3. The electromagnetic compatibility (EMC) of the converter should be taken into account, based on defined standards and regulations.

4. Good performance for a wide range of load and DC-link voltage condition, due to the nonlinear nature of the converter, this is a difficult goal to achieve.

To pursue this work in the future, the above mentioned challenges should be considered in designing the closed loop control of the proposed converter.

1.3 Technical Publications

The author has published three conference papers [106–108] during development of this thesis, which are related to the single-phase, three-phase, and the fault tolerant converter based on the proposed DC/AC converter topology.

1.4 Conclusion

The DC/AC converter also known as inverter does appropriate voltage/current regulation and converting the DC voltage/current to AC voltage/current for the grid connection. The DC/AC converter is the key element in a PV system. This thesis proposed a DC/AC converter for PV applications with five levels at the output converter side for the single-phase case and eleven levels for the three-phase case by using one split-wound coupled inductor and two extra diodes per phase. The proposed topology has an improved relationship between the number of levels per number of switches. In addition to the optimized relationship nL/nS, the most important characteristics of the proposed configuration are: (i) reduced number of semiconductor devices, while keeping the high number of levels at the output converter side, (ii) just one DC source without any need to balance the capacitor voltages, and (iii) high efficiency.

The proposed converter topology is used as a fault tolerant converter designed for low power applications, widely demanded and employed in a micro-grid environment. In comparison with the solutions presented in the technical literature, the proposed

design enhanced the following: i) It has a higher number of levels while using the same amount of controlled switching devices (six IGBTs). ii) There is no dead-time requirement for the converter's operation. This is an important characteristic for high-frequency micro-grid systems. iii) Leg isolation procedure with lower stress for the DC-link capacitor. Moreover, the study presents a hybrid pulse-width-modulation for the pre-fault operation.

2. SINGLE-PHASE 5L/4S TOPOLOGY

2.1 Introduction

This chapter proposes an energy conversion unit constituted by a single-phase DC/AC converter with five levels at the output converter side. The proposed converter has an optimized relationship between the number of levels per number of switches (nL/nS). The proposed five-level four-switch converter illustrated in Fig. 2.1, has nL/nS=5/4 which is by far the best relationship among the converters proposed in the technical literature. The most important characteristics of the proposed configuration are: (i) reduced number of semiconductor devices, while keeping a high number of levels at the output converter side, (ii) only one DC source without any need to balance capacitor voltages, and (iii) high efficiency. Details regarding the operation of the configuration and modulation strategy are presented, as well as the comparison between the proposed converter and the conventional ones. Simulated results are presented to validate the theoretical expectations.

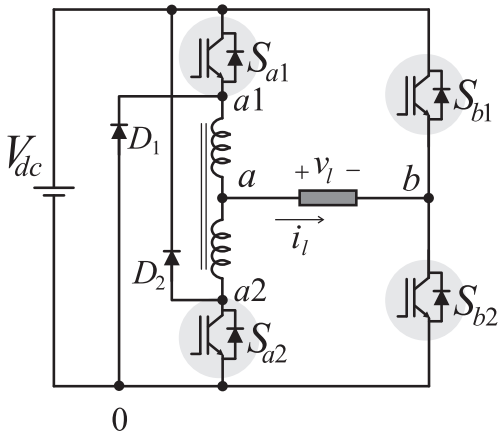


Fig. 2.1. Proposed 5-level 4-switch converter.

2.2 Converter Model

The proposed converter is constituted by four switching power devices (S_{a1}-S_{a2} and S_{b1}-S_{b2}), two diodes (D_1 and D_2) and one split-wound coupled inductor. The state of the switches can be represented by a binary variable, where S_j=0 means open switch and S_j=1 means closed switch (with $j = a1$, $a2$, $b1$ and $b2$).It is assumed that the currents in the coupled-windings are in continuous conduction mode, as highlighted in Fig. 2.2 (a) with $i_{a1} > 0$ and $i_{a2} > 0$. Figs. 2.2 (b), 2.2 (c), 2.2 (d) and 2.2 (e) show the equivalent circuit when (S_{a1}-S_{a2}) are equal to (0-0), (0-1), (1-0) and (1-1), respectively.

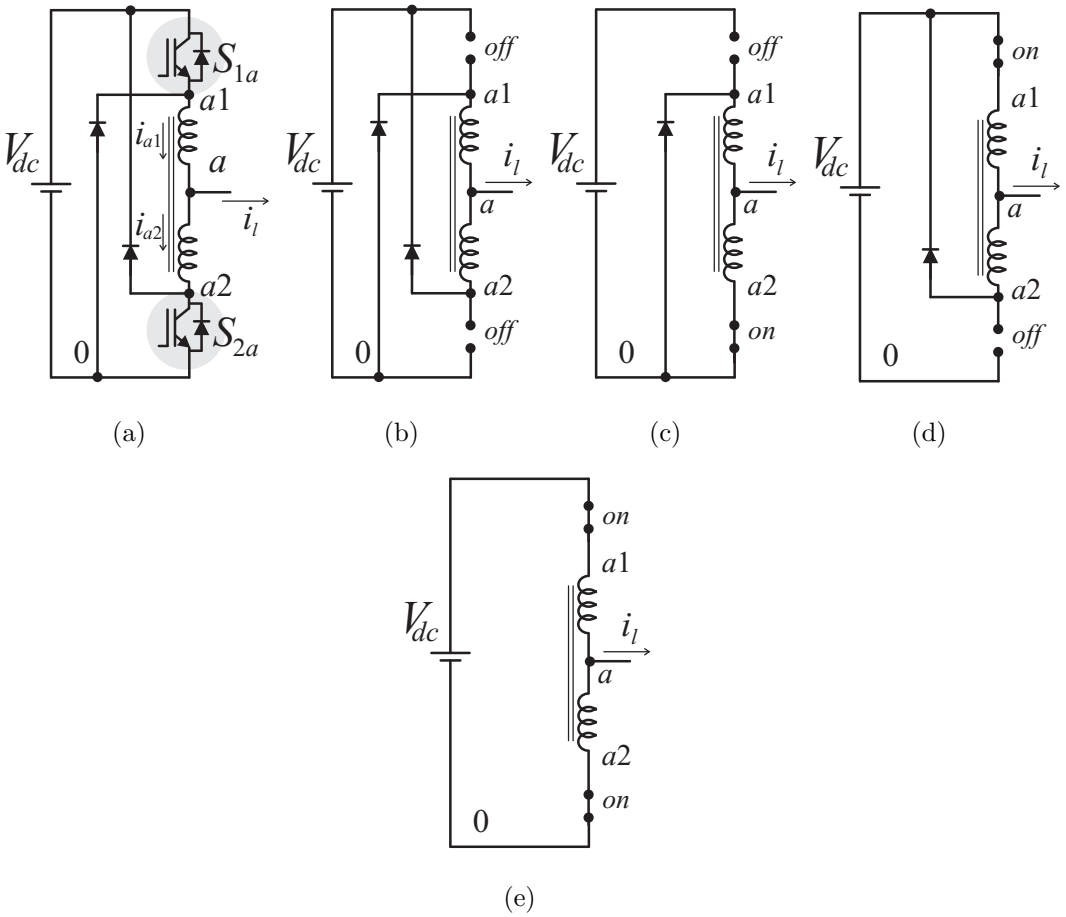
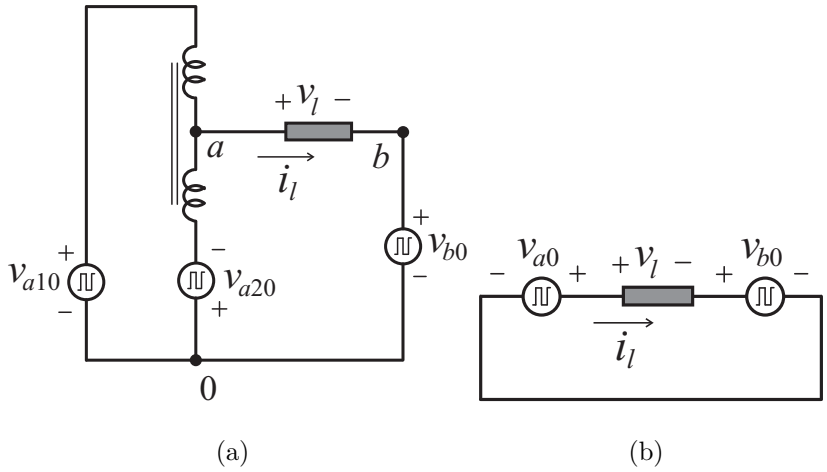


Fig. 2.2. (a) Operation in continuous conduction mode. (b) S_{a1}=S_{a2}=0. (c) S_{a1}=0 and S_{a2}=1. (d) S_{a1}=1 and S_{a2}=0. (e) S_{a1}=S_{a2}=1.



(a) (b)

Fig. 2.3. (a) Converter model. (b) Simplified converter model.

The voltages v_{a10} and v_{a20} (voltages from the points $a1$ and $a2$ to zero) can be expressed as a function of the state of the switches, as below:

$$v_{a10} = S_{a1} V_{dc} \tag{2.1}$$

$$v_{a20} = (1 - S_{a2})\, V_{dc} \tag{2.2}$$

It means that the converter can be modeled as in Fig. 2.3(a). In this figure v_{b0} is the voltage from point b to zero and it is given by:

$$v_{b0} = S_{b1} V_{dc} \tag{2.3}$$

Where $S_{b1} = 1 - S_{b2}$, meaning that the switches S_{b1} and S_{b2} are complementary to avoid a short circuit of the DC source. Then the voltages v_{a0} will be given by:

$$v_{a0} = \frac{1}{2}\,(v_{a10} + v_{a20}) \tag{2.4}$$

Once the voltages v_{a0} and v_{b0} were obtained, then the load voltage is given by:

$$v_l = v_{a0} - v_{b0} \tag{2.5}$$

From 2.5 it is possible to simplify and model the converter as depicted in Fig. 2.3 (b). Table 2.1 shows the converter voltages as a function of the state of the switches. Notice that there are five levels available at the output converter side.

Table 2.1.
Load voltage as a function of the switching states.

S_{a1}	S_{a2}	S_{b1}	v_{a10}	v_{a20}	v_{a0}	v_{b0}	v_{ind}	v_l
0	0	0	0	V_{dc}	$V_{dc}/2$	0	$-V_{dc}$	$V_{dc}/2$
0	0	1	0	V_{dc}	$V_{dc}/2$	V_{dc}	$-V_{dc}$	$-V_{dc}/2$
0	1	0	0	0	0	0	0	0
0	1	1	0	0	0	V_{dc}	0	$-V_{dc}$
1	0	0	V_{dc}	V_{dc}	V_{dc}	0	0	V_{dc}
1	0	1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	0	0
1	1	0	V_{dc}	0	$V_{dc}/2$	0	V_{dc}	$V_{dc}/2$
1	1	1	V_{dc}	0	$V_{dc}/2$	V_{dc}	V_{dc}	$-V_{dc}/2$

Another important variable in this circuit is the inductor voltage (v_{ind}), which will be used to guarantee the continuous conduction mode, this voltage is given by:

$$v_{ind} = v_{a10} - v_{a20} \tag{2.6}$$

2.3 PWM Strategy

From the model described before, both voltages v_l and v_{ind} have been obtained from the converter voltages v_{a10}, v_{a20} and v_{b0}. Now the gating signals S_{a1}, S_{a2}, S_{b1} and S_{b2} must be defined to generate the desired voltages v_l^* and v_{ind}^*, then since:

$$v_l^* = S_{a1}\frac{V_{dc}}{2} + (1 - S_{a2})\frac{V_{dc}}{2} - S_{b1}V_{dc} \tag{2.7}$$

$$v_{ind}^* = S_{a1}V_{dc} - (1 - S_{a2})V_{dc} \tag{2.8}$$

Those equations 2.7 and 2.8 are instantaneous expressions, which could be obtained throughout the average values in the switching period T_s.

The duty cycle of each switch can be defined as the instantaneous switching states, as follows:

$$D_{a1} = \frac{1}{T_s}\int_t^{t+T_s} S_{a1}(t)\,dt \tag{2.9}$$

$$D_{a2} = \frac{1}{T_s}\int_t^{t+T_s} S_{a2}(t)\,dt \tag{2.10}$$

$$D_{b1} = \frac{1}{T_s}\int_t^{t+T_s} S_{b1}(t)\,dt \tag{2.11}$$

$$D_{b2} = \frac{1}{T_s}\int_t^{t+T_s} S_{b2}(t)\,dt = 1 - D_{b1} \tag{2.12}$$

In terms of average values, equations 2.7 and 2.8 can be written respectively as:

$$\frac{2v_l^*}{V_{dc}} = D_{a1} + 1 - D_{a2} - 2D_{b1} \tag{2.13}$$

$$\frac{v_{ind}^*}{V_{dc}} = D_{a1} + D_{a2} - 1 \tag{2.14}$$

From 2.13 and 2.14 one possible solution for D_{a1} and D_{a2} is given below:

$$D_{a1} = \frac{v_{ind}^* + 2v_l^*}{2V_{dc}} + S_{b1} \tag{2.15}$$

$$D_{a2} = \frac{v_{ind}^* - 2v_l^*}{2V_{dc}} + 1 - S_{b1} \tag{2.16}$$

Once the voltages v_l^*, v_{ind}^* and V_{dc} are given, to complete the modulation scheme S_{b1} must be defined following these rules: (i) $S_{b1} = 1$ if $v_l^* < 0$ and $S_{b1} = 0$ if $v_l^* \geq 0$, as observed in Table 2.1. Notice that the leg b is operating at low frequency (the same frequency of the load), which represents an advantage due to switching losses reduction. Fig. 2.4 shows the analog solution for the PWM strategy presented in equations 2.15 and 2.16.

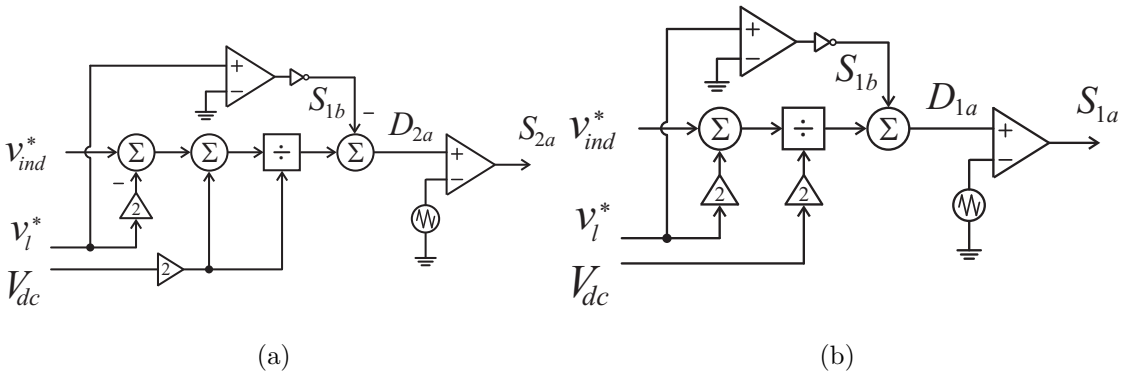


Fig. 2.4. Analog PWM Strategy: (a) implementation of equation 2.15 and (b) implementation of equation 2.16.

2.4 Comparison Among Proposed and Conventional Solutions

A direct comparison among the proposed converter (see Fig. 2.1) and the conventional ones presented in Fig. 1.7 (a simple H-bridge 4-swtich 3-level converter has also been added in this comparison) reveals some advantages for the 5-level 4-switch converter as presented in the Table 2.2, in this table FC stands for flying capacitor.

Table 2.2.
Comparison among configurations

	Number of power switches	Number of inductors diodes	Number of extra diodes	Number of DC-link capacitors	Number of levels
Proposed	4	1	2	1	5
H-bridge	4	0	0	1	3
Fig. 2(a)	8	0	4	2	5
Fig. 2(b)	6	0	2	2	5
Fig. 2(c)	6	0	0	$1 + FC$	5
Fig. 2(d)	6	0	0	2	5

Although using an inductor element, the proposed converter has the best nL/nS relationship, which gives benefits in terms of higher efficiency and reduced costs. Assuming the same switching frequency ($20KHz$) for the proposed converter and for the simple H-bridge converter (four switches), Fig. 2.5 shows a comparison between Weight Total Harmonic Distortion (WTHD) and modulation index (m_a) for the proposed converter and the conventional one. As expected, due to the increased number of levels the WTHD is lower for the proposed converter. Although reducing m_a for the proposed converter implies in reducing the number of levels at the output converter side, its WTHD is still lower than the one for the conventional converter. Another comparison between these two configurations was in terms of semiconductor power losses. In this case to guarantee a fair comparison, the switching frequency of the proposed converter was reduced until both converters reach the same WTHD level.

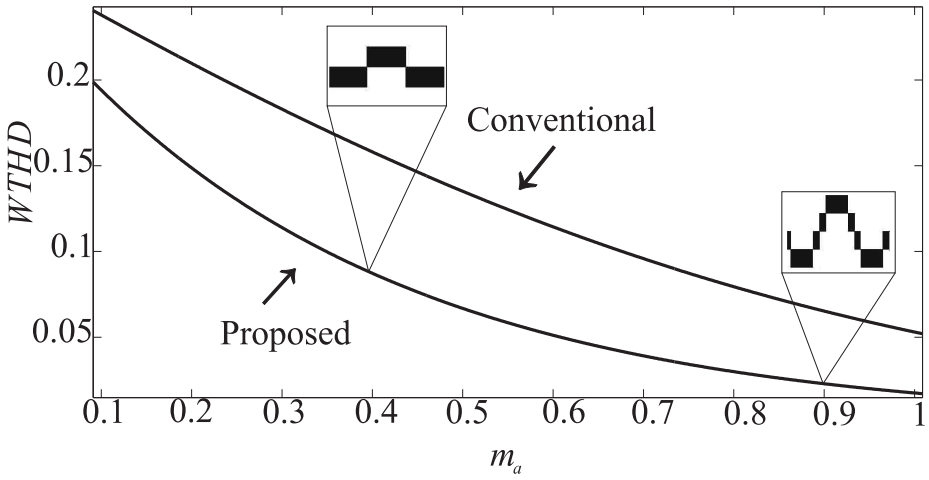


Fig. 2.5. Comparing WTHD versus m_a for proposed converter and conventional one.

Tables 2.3 and 2.4 show the losses of all the switches ($S_{b1}, S_{b2}, S_{a1}, S_{a2}$). For each switch, four kinds of losses are considered: (1) IGBT conduction losses, (2) IGBT switching losses, (3) diode conduction losses, and (4) diode switching losses. In addition, for the proposed converter the losses in the diodes D_1 and D_2 are also recorded. The sum of each column (S_total) for any individual switches and diodes shows the total losses for each of these elements in the corresponding converter. The sum of the values in the S_total row shows the total loss in the converter. From Tables 2.3 and 2.4, the losses for the proposed converter and the conventional converter are 8.45 and 16.3, respectively.

Table 2.3.
Losses for proposed converter

Proposed converter	S_{b1}	S_{b2}	S_{a1}	S_{a2}	D_1	D_2
Conduction IGBT	1.2	1.2	0.8	0.8	...	...
Switch IGBT	0.001	0.001	1	1	...	...
Conduction diode	0.025	0.025	0	0	1.08	1.08
Switch diode	0	0	0	0	0.1	0.1
S_total	1.226	1.226	1.8	1.8	1.18	1.18

Table 2.4.
Losses for conventional converter

Conventional converter	S_{b1}	S_{b2}	S_{a1}	S_{a2}
Conduction IGBT	2.49	2.48	2.48	2.49
Switch IGBT	1.16	1.15	1.15	1.14
Conduction diode	0.338	0.339	0.339	0.338
Switch diode	0.101	0.102	0.101	0.102
S_total	4.089	4.071	4.07	4.07

2.5 Simulation Results

The proposed converter has been simulated by using PSIM software. The experimental verification will be presented in Chapter 5. The load is given by $R = 39.6\Omega$, $L = 50\text{m}H$, the DC-link voltage source 375 is V, and the switching frequency is 5KHz. Fig. 2.6 shows the simulation results for the single-phase DC/AC converter. Fig. 2.6 (top) shows load voltage v_l which has 5 levels $(\pm V_{dc}, 0, \pm V_{dc}/2)$ and Fig. 2.6 (bottom) shows the load current i_l. In Fig. 2.7 it has been shown another set of the simulation results with the DC-link voltage source equal to $600\,V$. Fig. 2.7 (a) and 2.7 (b) show the current and voltage across each elements (switches, diodes and inductors) for the leg with inductors. Fig. 2.8 (top) shows, the comparison between the load current and the reference current for a closed-loop operation by using a PI controller. Notice that both waveforms match each other even for a hard step transient for the reference current at t=0.3s. In this case the amplitude of the current has changed to guarantee the effectiveness of the controller. Fig. 2.8 (middle) shows the reference voltage and Fig. 2.8 (bottom) shows the load voltage which is dependent on m_a. As expected from the theoretical analysis (see Fig. 2.5), the number of levels for the proposed circuit is dependent on the modulation index (m_a), which explains why prior to t=0.3s v_l has three levels and after 0.3s it has five levels.

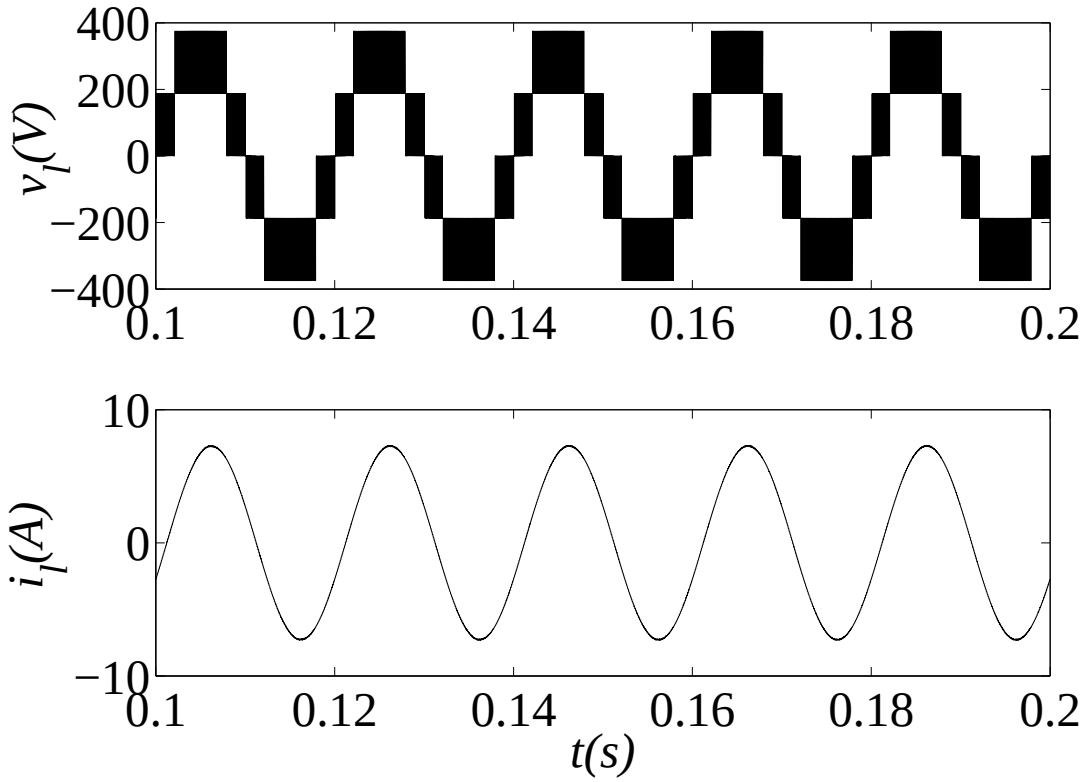
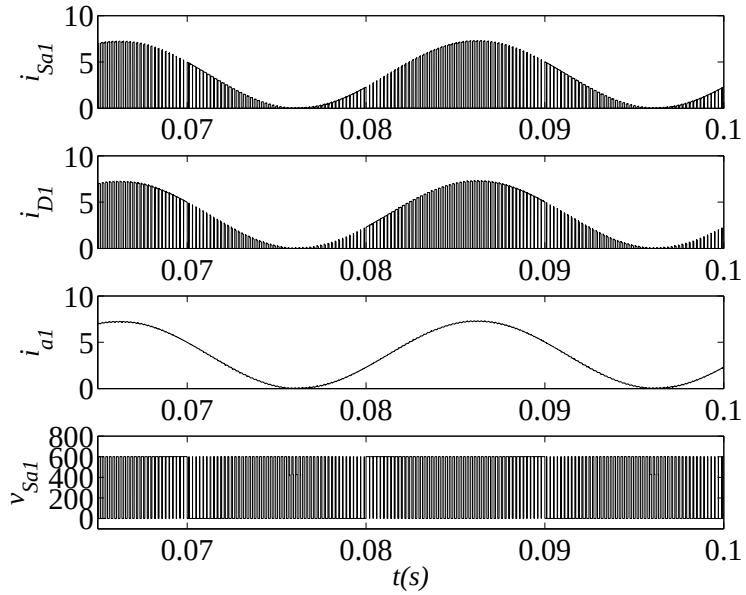
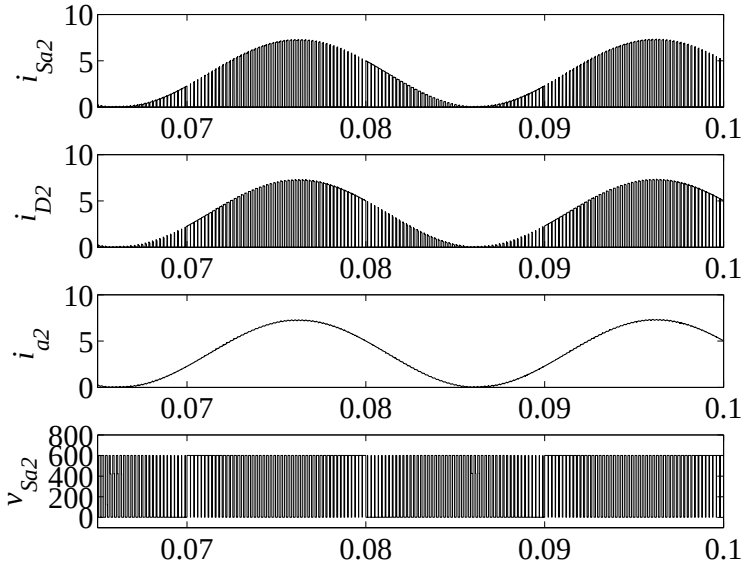


Fig. 2.6. Load voltage (top) and load current (bottom).



(a)



(b)

Fig. 2.7. Simulation results: (a) (from top to bottom) current through S_{a1}, current through D_1, current through top inductor and the voltage on S_{a1} (b) (from top to bottom) current through S_{a2}, current through D_2, current through bottom inductor and the voltage on S_{a2}.

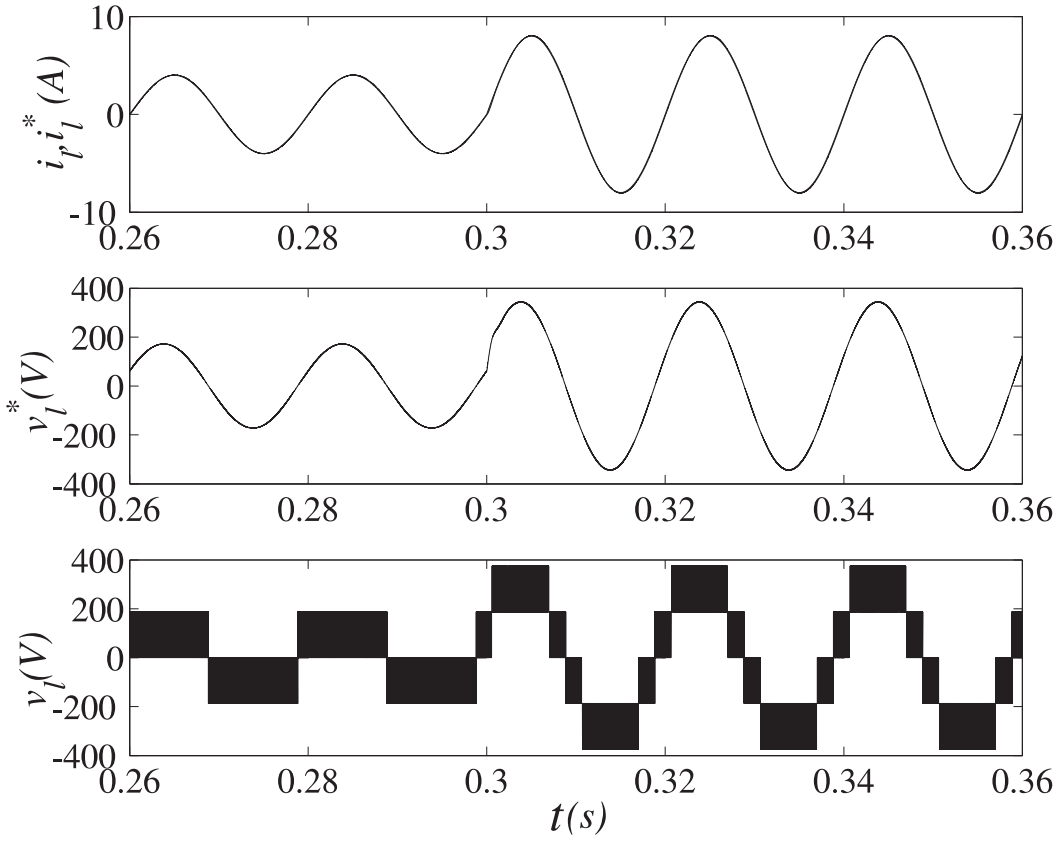


Fig. 2.8. From top to bottom load current and reference load current, reference load voltage, and load voltage.

2.6 RCD Snubber Circuit Design for 5-Level 4-Switch DC-AC Converter

This section presents the design of an RCD snubber circuit for the optimized single phase DC-AC converter. The purpose of this optimal design with RCD snubber is to lower the spike voltage of power switch and hence improving the efficiency and performance of the proposed converter. Existence of a significantly large spike voltage across the switch may damage the switch. Thus, a RCD clamp (using a resistor, a capacitor and a diode) is used in the proposed topology to clamp the voltage across the switch. Fig. 2.9 illustrates the proposed topology with RCD snubber circuit. As it is illustrated in Fig. 2.9, the RCD snubber circuit is not added for $S_{1b} - S_{2b}$ switches because they are operating with low switching frequency, thus by adding an RCD snubber circuit we just have extra power dissipation without having significant gain. In addition, from experimental results, we cannot observe a substantial voltage spike across $S_{1b} - S_{2b}$ switches, therefore it is not necessary to add an RCD snubber for these two switches.

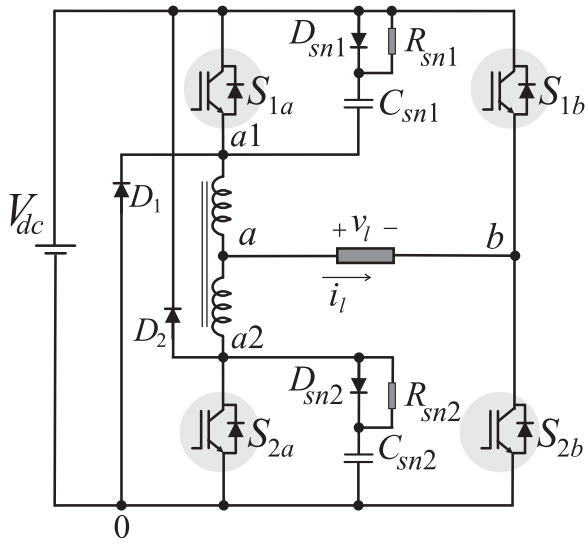
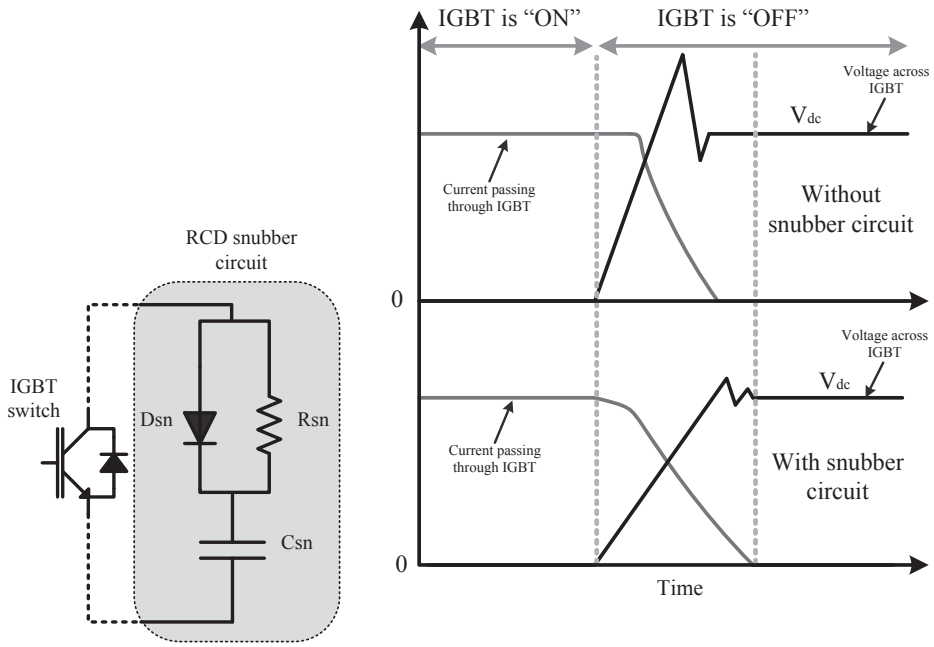


Fig. 2.9. Proposed 5-level 4-switch converter With RCD snubber.



(a) (b)

Fig. 2.10. (a) RCD snubber circuit for the IGBT switches. (b) RCD snubber circuit effect on voltage and current of the IGBT during switching.

2.6.1 RCD Snubber Model

Semiconductor power switches are commonly subject to the problem of spike voltage during the switching ON and OFF. Several methods exist to suppress this overvoltage, a possible solution is to install a snubber circuit [109] for the IGBTs, resistor-capacitor-diode (RCD) snubber circuit [110] is one of the common snubber schematics used to clamp the voltage across the switch. This snubber configuration, illustrated in Fig. 2.10 (a), is also known as a charge and discharge RCD snubber circuit. For the proposed multilevel converter, this snubber configuration has been chosen, since it is suitable for the converter's switching frequency and its power level.

RCD snubbers are typically used in medium to high current applications, its characteristics are [111]: (i) transfer power dissipation from the switch to a resistor, (ii) reduce total switching losses, (iii) reduce voltage and current ringing, and (iv) limit dI/dt or dV/dt. Fig. 2.10 (b) illustrates the effect of the snubber circuit on voltage and current of the IGBT.

Appropriate component selection and design of the RCD snubber is very important to improve the performance of the converter. However the average current in the snubber diode is not high but the peak current is considerable; thus the peak current should be basis for selecting the snubber diode. The diode should be also selected for the peak rating of the capacitor voltage. Also, the diode should have an ultra-fast recovery time. The minimum capacitance for the snubber can be calculated using the following equation [25, 111, 112]:

$$C_{sn} = \frac{L \times I_0^2}{V_{pk} - V_{dc}} \tag{2.17}$$

where L is the wiring parasitic or stray inductance, I_o is the collector current at IGBT turn off, V_{pk} is the peak voltage, and V_{dc} is the DC-link voltage. A typical value of the stray inductance is approximately $100nH$ [25]. For the proposed converter the maximum allowable peak voltage is assumed to be the 10% more than the DC-link voltage, we should keep in mind that this voltage should be less than the IGBT breakdown voltage. The power loss in the snubber resistor is directly proportional to the size of the snubber capacitor, thus a smaller capacitor results in lower power dissipation in resistor.

The function of the snubber resistor is to discharge the accumulated charge in the snubber capacitor before the IGBT turns-off again. In order to determine the required resistance value for the snubber circuit, we need to take into consideration the smallest time value between IGBT turn ON and OFF. For the proposed converter, this minimum time for IGBT of the high frequency leg is determined from the

simulation of the converter to be $1\mu s$ ($t_{min} = 1\mu s$). Now the resistor value can be determined using the following equation:

$$R_{sn} = \frac{t_{min}}{5C_{sn}} \tag{2.18}$$

The power dissipated in the RCD snubber circuit can be approximated by the capacitor value as:

$$P = \frac{1}{2}C_{sn}(V_c^2)f \tag{2.19}$$

where V_c is the capacitor voltage and f is the switching frequency.

2.6.2 Converter Model with Snubber

The high frequency leg of the converter with RCD snubber is illustrated in Fig. 2.11 (a), its four modes of operation is demonstrated in Fig.2.11 (b)-(e). Table 2.5 presents the snubber capacitor and load voltages as a function of switching states, the voltages v_{a10} and v_{a20} (voltages from the points $a1$ and $a2$ to zero) can be expressed as a function of the state of the switches, when C_{sn1} is fully charged as below:

$$v_{a10} = S_{a1}V_{dc} \tag{2.20}$$

$$v_{a20} = (1 - S_{a2})\,V_{dc} \tag{2.21}$$

Table 2.5.
Load voltage as a function of the switching states.

S_{a1}	S_{a2}	S_{b1}	v_{a10}	v_{a20}	v_{a0}	v_{b0}	v_{ind}	v_l	v_{Csn1}	v_{Csn2}
0	0	0	0	V_{dc}	$V_{dc}/2$	0	$-V_{dc}$	$V_{dc}/2$	V_{dc}	V_{dc}
0	0	1	0	V_{dc}	$V_{dc}/2$	V_{dc}	$-V_{dc}$	$-V_{dc}/2$	V_{dc}	V_{dc}
0	1	0	0	0	0	0	0	0	V_{dc}	0
0	1	1	0	0	0	V_{dc}	0	$-V_{dc}$	V_{dc}	0
1	0	0	V_{dc}	V_{dc}	V_{dc}	0	0	V_{dc}	0	V_{dc}
1	0	1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	0	0	0	V_{dc}
1	1	0	V_{dc}	0	$V_{dc}/2$	0	V_{dc}	$V_{dc}/2$	0	0
1	1	1	V_{dc}	0	$V_{dc}/2$	V_{dc}	V_{dc}	$-V_{dc}/2$	0	0

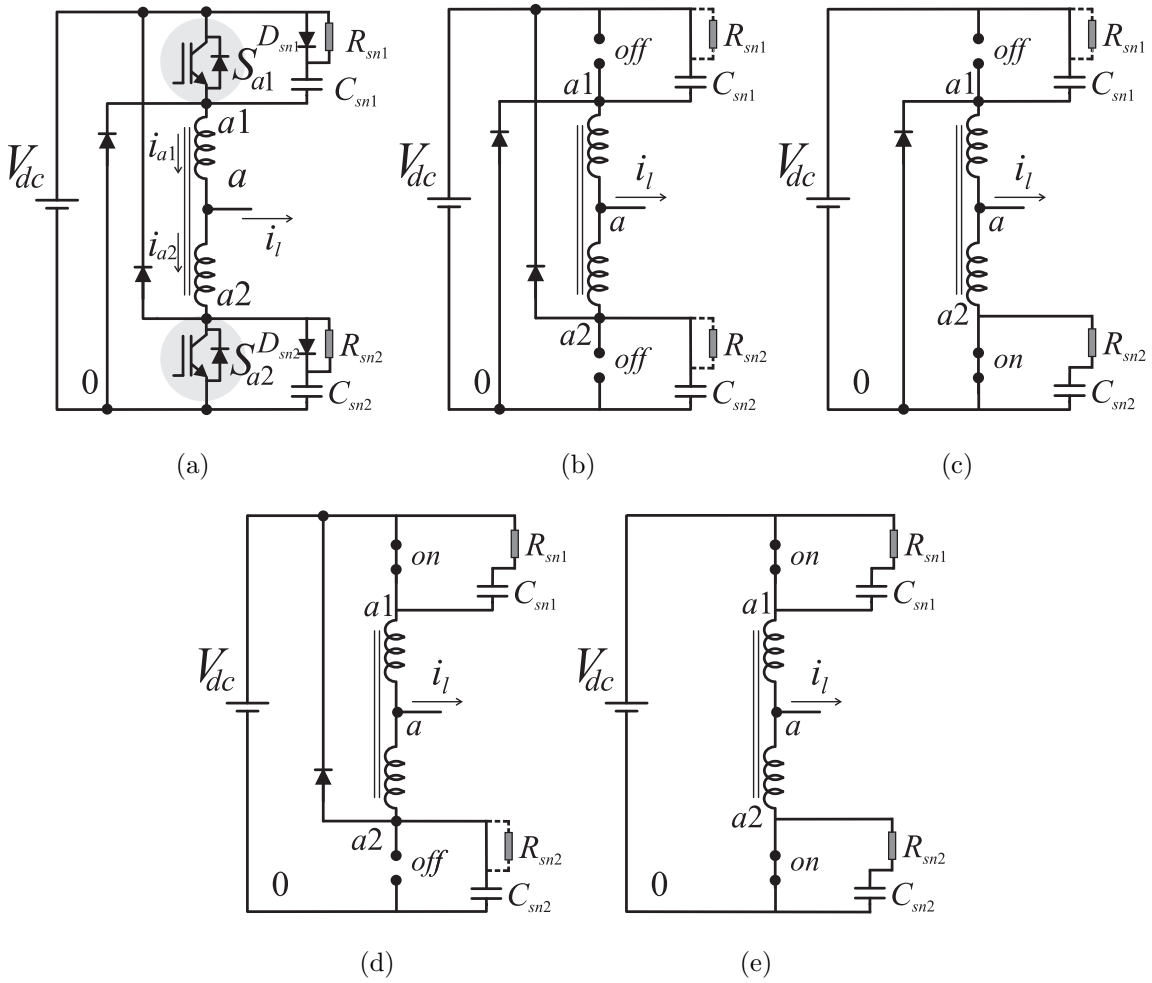


Fig. 2.11. (a) Operation in continuous conduction mode. (b) S_{a1}=S_{a2}=0. (c) S_{a1}=0 and S_{a2}=1. (d) S_{a1}=1 and S_{a2}=0. (e) S_{a1}=S_{a2}=1.

2.7 Conclusion

This chapter proposed a single-phase DC-AC converter with five levels at the output converter side by using one split-wound coupled inductor and two extra diodes. The proposed topology has an improved relationship between the number of levels per number of switches. A RCD snubber circuit is added across the IGBT switches to eliminate significant large voltage spikes, as results reducing the probability of switch failure. In addition to the optimized relationship nL/nS, the most important char-

acteristics of the proposed configuration are: (*i*) reduced number of semiconductor devices, while keeping the high number of levels at the output converter side, (*ii*) just one DC source without any need to balance the capacitor voltages, and (*iii*) high efficiency.

3. THREE-PHASE DC-AC CONVERTER WITH FIVE-LEVEL FOUR-SWITCH CHARACTERSTIC

3.1 Introduction

This chapter presents a three-phase DC-AC converter with an optimized number of levels per number of switches. Each phase of the proposed converter, illustrated in Fig. 3.1, includes four controlled power switches and it is able to generate five levels. The most significant characteristics of the proposed converter are: (*i*) reduced number of semiconductor devices, while keeping a high number of levels at the output side of each phase; (*ii*) no need to control the DC-link capacitor voltage as in NPC and flying capacitor topologies; and (*iii*) reduced semiconductor losses. The principle of operation, modulation technique, and modeling of the proposed converter are presented in this paper. The proposed configuration is simulated and validated experimentally.

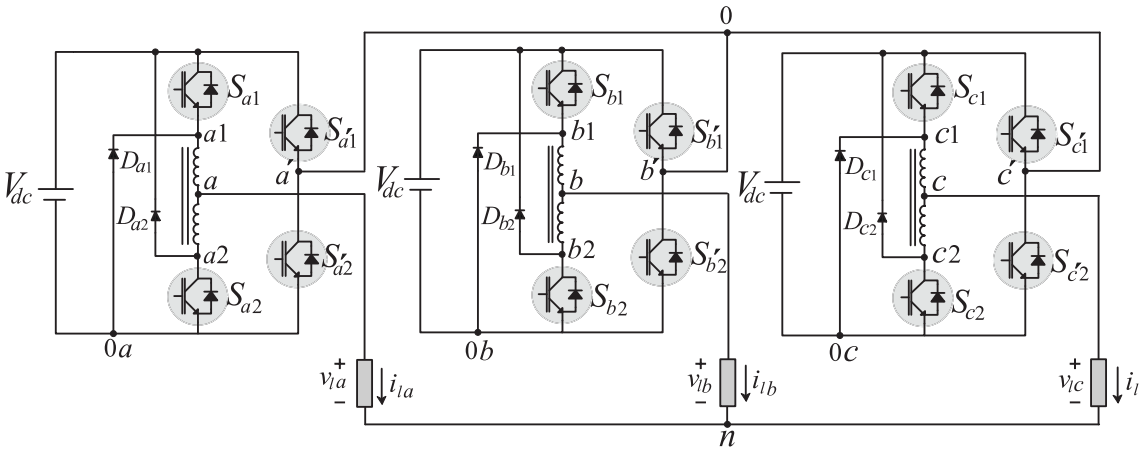


Fig. 3.1. Proposed converter with 5-level 4-switch per phase characteristic.

3.2 Converter Model

The proposed converter shown in Fig. 3.1 has 12 switching power devices (S_{x1}-S_{x2} and $S_{x'1}$-$S_{x'2}$); six diodes (D_{x1} and D_{x2}) with $x = a, b, c$ and three split-wound coupled inductors. The state of the switches can be represented by a binary variable, where S_j=0 means open switch and S_j=1 means closed switch (with $j = x1$, $x2$). It is assumed that the currents in the coupled-windings are in continuous conduction mode, as highlighted in Fig. 3.2 (a) with $i_{a1} > 0$ and $i_{a2} > 0$. Figs. 3.2(b), 3.2 (c), 3.2 (d) and 3.2 (e) show the equivalent circuit for one phase when (S_{x1}-S_{x2}) are equal to (0-0), (0-1), (1-0) and (1-1), respectively. The voltages v_{x10x} and v_{x20x} (voltages

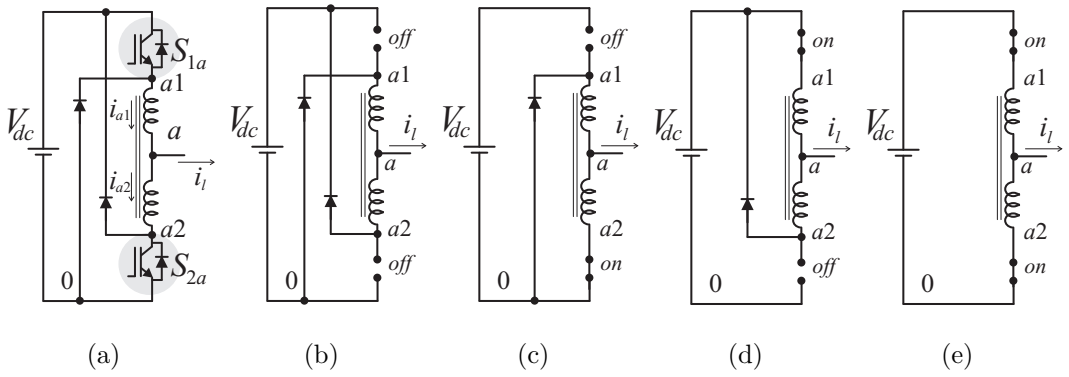


Fig. 3.2. (a) Operation in continuous conduction mode. (b) S_{a1}=S_{a2}=0. (c) S_{a1}=0 and S_{a2}=1. (d) S_{a1}=1 and S_{a2}=0. (e) S_{a1}=S_{a2}=1.

from the points $x1$ and $x2$ to $0x$) can be expressed as a function of the state of the switches, as below:

$$v_{a10a} = S_{a1} V_{dc} \tag{3.1}$$

$$v_{a20a} = (1 - S_{a2})\, V_{dc} \tag{3.2}$$

$$v_{b10b} = S_{b1} V_{dc} \tag{3.3}$$

$$v_{b20b} = (1 - S_{b2})\, V_{dc} \tag{3.4}$$

$$v_{c10c} = S_{c1} V_{dc} \tag{3.5}$$

$$v_{c20c} = (1 - S_{c2})\, V_{dc} \tag{3.6}$$

Then the voltages v_{x0x} will be given by:

$$v_{a0a} = \frac{1}{2}\left(v_{a10a} + v_{a20a}\right) \tag{3.7}$$
$$= \frac{1}{2}(S_{a1} - S_{a2} + 1)V_{dc} \tag{3.8}$$
$$v_{b0b} = \frac{1}{2}\left(v_{b10b} + v_{b20b}\right) \tag{3.9}$$
$$= \frac{1}{2}(S_{b1} - S_{b2} + 1)V_{dc} \tag{3.10}$$
$$v_{c0c} = \frac{1}{2}\left(v_{c10c} + v_{c20c}\right) \tag{3.11}$$
$$= \frac{1}{2}(S_{c1} - S_{c2} + 1)V_{dc} \tag{3.12}$$

The voltages from point x' to $0x$ are given by:

$$v_{a'0a} = S_{a'1}V_{dc} \tag{3.13}$$
$$v_{b'0b} = S_{b'1}V_{dc} \tag{3.14}$$
$$v_{c'0c} = S_{c'1}V_{dc} \tag{3.15}$$

where $S_{x'1} = 1 - S_{x'2}$, meaning that the switches $S_{x'1}$ and $S_{x'2}$ are complementary to avoid a short circuit of the DC-source. The proposed converter can be modeled as presented in Fig. 3.3.

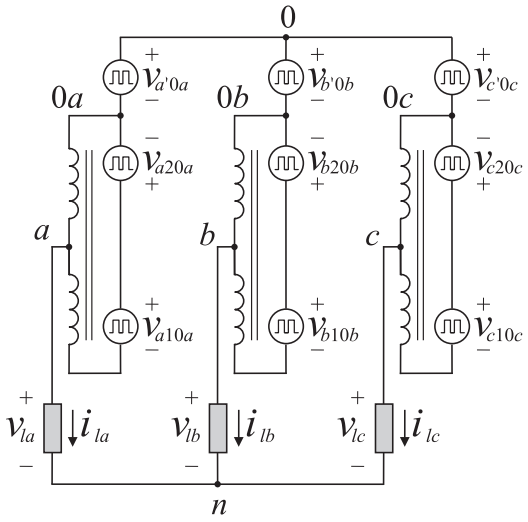


Fig. 3.3. Converter model for the proposed converter.

Once the voltages v_{x0x} and $v_{x'0x}$ were obtained, the voltages at the output of each converter's phase are given by:

$$v_A = v_{a0a} - v_{a'0a} \tag{3.16}$$
$$= \frac{1}{2}[S_{a1}V_{dc} + (1 - S_{a2})V_{dc}] - S_{a'1}V_{dc} \tag{3.17}$$
$$= \frac{1}{2}(S_{a1} - S_{a2} - S_{a'1} + 1)V_{dc} \tag{3.18}$$

$$v_B = v_{b0b} - v_{b'0b} \tag{3.19}$$
$$= \frac{1}{2}[S_{b1}V_{dc} + (1 - S_{b2})V_{dc}] - S_{b'1}V_{dc} \tag{3.20}$$
$$= \frac{1}{2}(S_{b1} - S_{b2} - S_{b'1} + 1)V_{dc} \tag{3.21}$$

$$v_C = v_{c0c} - v_{c'0c} \tag{3.22}$$
$$= \frac{1}{2}[S_{c1}V_{dc} + (1 - S_{c2})V_{dc}] - S_{c'1}V_{dc} \tag{3.23}$$
$$= \frac{1}{2}(S_{c1} - S_{c2} - S_{c'1} + 1)V_{dc} \tag{3.24}$$

Table 3.1 shows the converter voltages as a function of the state of the switches. Notice that there are five levels available at the output converter side for each leg.

Table 3.1.
Conventional voltages as a function of the switching states.

S_{x1}	S_{x2}	$S_{x'1}$	v_{x10x}	v_{x20x}	v_{x0x}	$v_{x'0x}$	v_{indx}	v_X
0	0	0	0	V_{dc}	$V_{dc}/2$	0	$-V_{dc}$	$V_{dc}/2$
0	0	1	0	V_{dc}	$V_{dc}/2$	V_{dc}	$-V_{dc}$	$-V_{dc}/2$
0	1	0	0	0	0	0	0	0
0	1	1	0	0	0	V_{dc}	0	$-V_{dc}$
1	0	0	V_{dc}	V_{dc}	V_{dc}	0	0	V_{dc}
1	0	1	V_{dc}	V_{dc}	V_{dc}	V_{dc}	0	0
1	1	0	V_{dc}	0	$V_{dc}/2$	0	V_{dc}	$V_{dc}/2$
1	1	1	V_{dc}	0	$V_{dc}/2$	V_{dc}	V_{dc}	$-V_{dc}/2$

Another important variable in this circuit is the inductor voltage (v_{indx}), which will be used to guarantee the continuous conduction mode, this voltage is given by:

$$v_{indx} = v_{x10x} - v_{x20x} \tag{3.25}$$

Fig. 3.4 shows a simplified three-phase converter model obtained from Fig. 3.3.

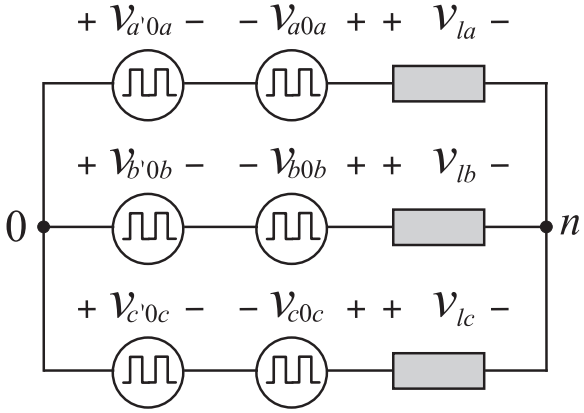


Fig. 3.4. Simplified three-phase converter model.

The load voltage for each phase is obtained from (3.26),(3.27), and (3.28) as below:

$$v_{la} = v_A - v_{n0} \tag{3.26}$$

$$v_{lb} = v_B - v_{n0} \tag{3.27}$$

$$v_{lc} = v_C - v_{n0} \tag{3.28}$$

After adding these three equations and assuming a balanced three phase voltage, it yields:

$$\begin{aligned} v_{la} + v_{lb} + v_{lc} &= v_A + v_B + v_C - 3v_{n0} \\ 0 &= v_A + v_B + v_C - 3v_{n0} \end{aligned}$$

which leads to:

$$v_{n0} = \frac{1}{3}(v_A + v_B + v_C) \tag{3.29}$$

Then it is possible to write the load voltages ($v_{la}, v_{lb},$ and v_{lc}) as a function of the switching states and DC-link voltage:

$$v_{la} = \frac{1}{3}(S_{a1} - S_{a2} - S_{a'1})V_{dc} - \frac{1}{6}(S_{b1} - S_{b2} - S_{b'1})V_{dc} - \frac{1}{6}(S_{c1} - S_{c2} - S_{c'1})V_{dc} \quad (3.30)$$

$$v_{lb} = \frac{1}{3}(S_{b1} - S_{b2} - S_{b'1})V_{dc} - \frac{1}{6}(S_{a1} - S_{a2} - S_{a'1})V_{dc} - \frac{1}{6}(S_{c1} - S_{c2} - S_{c'1})V_{dc} \quad (3.31)$$

$$v_{lc} = \frac{1}{3}(S_{c1} - S_{c2} - S_{c'1})V_{dc} - \frac{1}{6}(S_{b1} - S_{b2} - S_{b'1})V_{dc} - \frac{1}{6}(S_{a1} - S_{a2} - S_{a'1})V_{dc} \quad (3.32)$$

3.3 PWM Strategy

From the model described before, both voltages v_{lx} and v_{indx} have been obtained from the converter voltages v_{x10x}, v_{x20x}, and $v_{x'0x}$. Now the gating signals S_{x1}, S_{x2}, $S_{x'1}$, and $S_{x'2}$ ($x = a, b, c$) must be defined to generate the desired voltages v^*_{lx} and v^*_{indx}, as below:

$$v^*_{la} = S_{a1}\frac{V_{dc}}{2} + (1 - S_{a2})\frac{V_{dc}}{2} - S_{a'1}V_{dc} \quad (3.33)$$

$$v^*_{inda} = S_{a1}V_{dc} - (1 - S_{a2})V_{dc} \quad (3.34)$$

$$v_{lb}^{*} = S_{b1}\frac{V_{dc}}{2} + \left(1 - S_{b2}\right)\frac{V_{dc}}{2} - S_{b'1}V_{dc} \tag{3.35}$$

$$v_{indb}^{*} = S_{b1}V_{dc} - \left(1 - S_{b2}\right)V_{dc} \tag{3.36}$$

$$v_{lc}^{*} = S_{c1}\frac{V_{dc}}{2} + \left(1 - S_{c2}\right)\frac{V_{dc}}{2} - S_{c'1}V_{dc} \tag{3.37}$$

$$v_{indc}^{*} = S_{c1}V_{dc} - \left(1 - S_{c2}\right)V_{dc} \tag{3.38}$$

The equations (3.33)-(3.38) are instantaneous expressions, which could be obtained through the average values in the switching period T_s. The duty cycle of each switch can be defined as the instantaneous switching states, as follows:

$$D_{a1} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{a1}\left(t\right)dt \tag{3.39}$$

$$D_{a2} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{a2}\left(t\right)dt \tag{3.40}$$

$$D_{a'1} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{a'1}\left(t\right)dt \tag{3.41}$$

$$D_{a'2} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{a'2}\left(t\right)dt = 1 - D_{a'1} \tag{3.42}$$

$$D_{b1} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{b1}\left(t\right)dt \tag{3.43}$$

$$D_{b2} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{b2}\left(t\right)dt \tag{3.44}$$

$$D_{b'1} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{b'1}\left(t\right)dt \tag{3.45}$$

$$D_{b'2} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{b'2}\left(t\right)dt = 1 - D_{b'1} \tag{3.46}$$

$$D_{c1} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{c1}\left(t\right)dt \tag{3.47}$$

$$D_{c2} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{c2}\left(t\right)dt \tag{3.48}$$

$$D_{c'1} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{c'1}\left(t\right)dt \tag{3.49}$$

$$D_{c'2} = \frac{1}{T_s}\int_{t}^{t+T_s} S_{c'2}\left(t\right)dt = 1 - D_{c'1} \tag{3.50}$$

In terms of average values, equations (3.33)-(3.38) can be written respectively by:

$$\frac{2v_{la}^*}{V_{dc}} = D_{a1} + 1 - D_{a2} - 2D_{a'1} \tag{3.51}$$

$$\frac{v_{inda}^*}{V_{dc}} = D_{a1} + D_{a2} - 1 \tag{3.52}$$

$$\frac{2v_{lb}^*}{V_{dc}} = D_{b1} + 1 - D_{b2} - 2D_{b'1} \tag{3.53}$$

$$\frac{v_{indb}^*}{V_{dc}} = D_{x1} + D_{b2} - 1 \tag{3.54}$$

$$\frac{2v_{lc}^*}{V_{dc}} = D_{c1} + 1 - D_{c2} - 2D_{c'1} \tag{3.55}$$

$$\frac{v_{indc}^*}{V_{dc}} = D_{c1} + D_{c2} - 1 \tag{3.56}$$

From (3.51)-(3.56), one possible solution for D_{x1} and D_{x2} are given below:

$$D_{a1} = \frac{v_{inda}^* + 2v_{la}^*}{2V_{dc}} + S_{a'1} \tag{3.57}$$

$$D_{a2} = \frac{v_{inda}^* - 2v_{la}^*}{2V_{dc}} + 1 - S_{a'1} \tag{3.58}$$

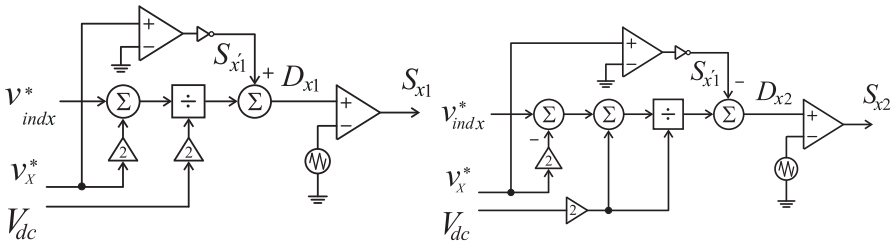
$$D_{b1} = \frac{v_{indb}^* + 2v_{lb}^*}{2V_{dc}} + S_{b'1} \tag{3.59}$$

$$D_{b2} = \frac{v_{indb}^* - 2v_{lb}^*}{2V_{dc}} + 1 - S_{b'1} \tag{3.60}$$

$$D_{c1} = \frac{v_{indc}^* + 2v_{lc}^*}{2V_{dc}} + S_{c'1} \tag{3.61}$$

$$D_{c2} = \frac{v_{indc}^* - 2v_{lc}^*}{2V_{dc}} + 1 - S_{c'1} \tag{3.62}$$

Once the voltages v_X^*, v_{indx}^* and V_{dc} are given, to complete the modulation scheme, $S_{x'1}$ must be defined from the following rules: (i) $S_{\ x'1} = 1$ if $v_X^* < 0$ and $S_{x'1} = 0$ if



(a) (b)

Fig. 3.5. PWM Strategy with $x = a, b,$ and c.

$v^*_X > 0$, as observed in Table 3.1. From the previous development, it is possible to obtain the analog PWM solution as in Fig. 3.5. Notice that the leg x' is operating at low frequency (the same frequency of the load), which represents an advantage due to switching losses reduction presented in the following section.

3.4 Simulation Results

The proposed converter has been simulated by using PSIM software. The conditions for the single-phase version of the proposed converter are given by: $R = 160\Omega$, switching frequency $20KHz$, and the DC-link voltage is 15V. The three-phase version of the proposed converter was simulated by using the following conditions: $R = 39.6\Omega$, $L = 5\text{m}H$, the DC-link voltage source is $375\,V$, and the switching frequency is $5KHz$ for each leg. Fig. 3.6 shows the simulation results. Fig. 3.7 shows the simulation results for the three-phase DC/AC converter. The top three subplots in Fig. 3.7 (a) show the load voltage for each phase that has 11 levels and the bottom subplot shows the three-phase load currents.

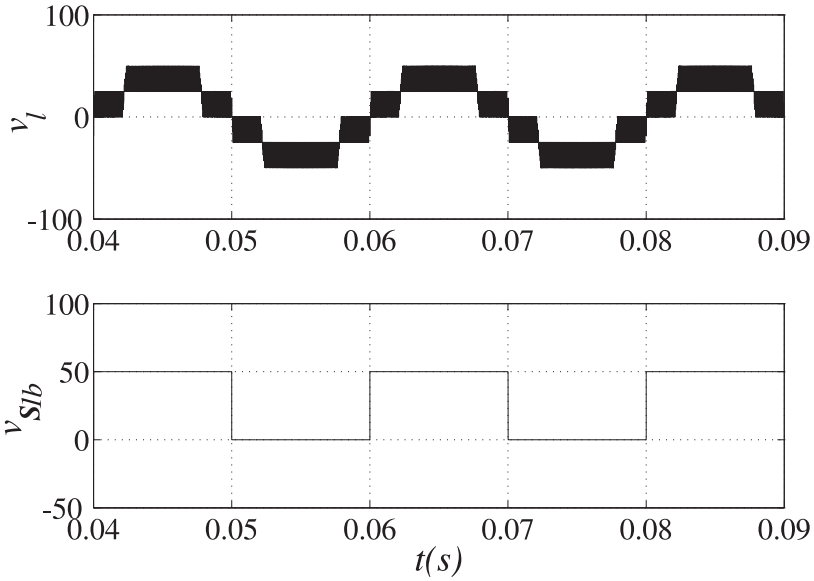


Fig. 3.6. Simulation results for single-phase converter.

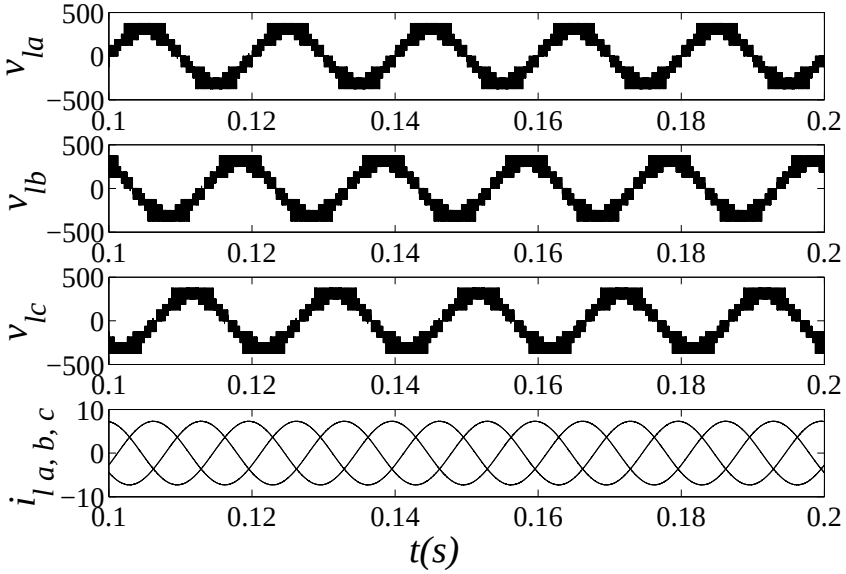


Fig. 3.7. Simulation results for three-phase converter.

3.5 Conclusion

This chapter proposed a three-phase DC/AC converter with 11 levels at the phase load voltage. Indeed, such a converter presents each phase with a 5-level 4-switch characteristic. The proposed topology has an improved relationship between the number of levels (nL) per number of switches (nS). In addition to the optimized relationship nL/nS, the most important characteristics of the proposed configuration are: (i) reduced number of semiconductor devices, while keeping a high number of levels at the output side of each phase; and (ii) reduced semiconductor losses. A loss comparison demonstrates that the proposed conventional can operate with higher efficiency.

4. FAULT-TOLERANT CONVERTER

4.1 Introduction

This chapter proposes a fault tolerant converter designed for low power applications, as required in a micro-grid environment. The main characteristics of this converter when compared with solutions presented in the technical literature are: i) higher number of levels using the same amount of controlled switching devices (six IGBTs), ii) no dead-time requirement for the converter's operation, which is an important aspect for high-frequency micro-grid systems and iii) leg isolation procedure with reduced stress for the DC-link capacitor. Furthermore, a hybrid pulse-width-modulation will be present for the pre-fault operation. Details regarding the transition from the pre-fault to post-fault operation is presented. Selected steady-state and transient results are presented to validate the theoretical expectations. The three-phase PWM inverter with split-wound coupled inductors was proposed in [113] and studied in [114].

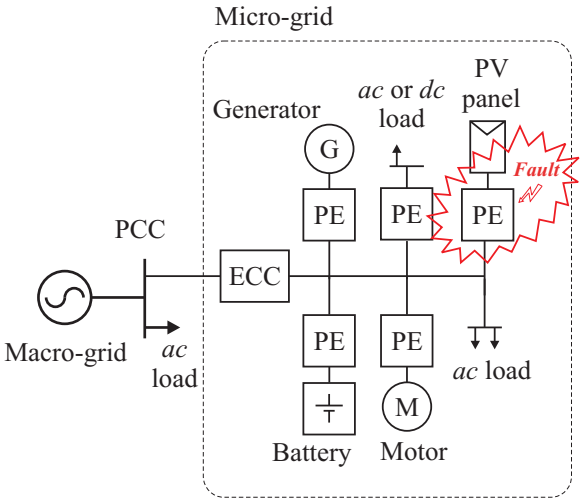


Fig. 4.1. (a) Microgrid system facing a fault problem in the DC-AC converter.

Considering the micro-grid point of view, there are different types of electrical equipment that may suffer with malfunction operation [81,82], such as: a) distributed sources (PV panels, wind turbines, etc.), b) storage systems, and c) power electronics converters, etc. Indeed, faults in power electronics converters are really important since there are power electronics converters placed everywhere in the micro-grid environment, as observed in Fig. 4.1, where PE generically represents power electronics converters. Fig. 4.1 also shows a micro-grid system with a fault occurring in the DC-AC converter interfacing PV panel and the AC bus. The proposed fault tolerant converter is illustrated in Fig. 4.2.

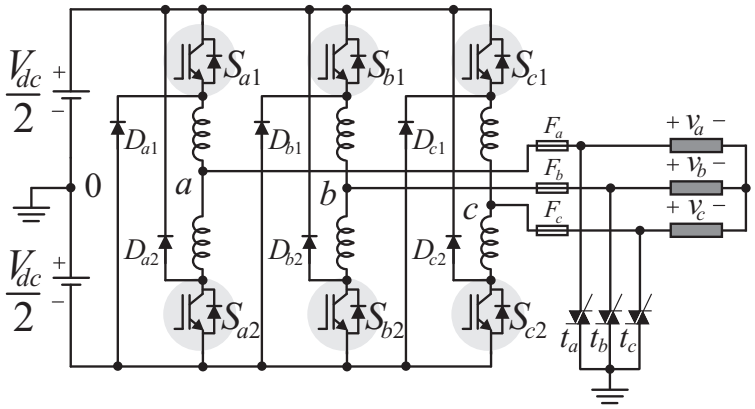


Fig. 4.2. DC-AC fault tolerant converter.

Specific kinds of faults can occur in these type of converters, for example, faults occurring in the power converter itself (open-circuit and short-circuit failures occurring in the converter power devices) or in the control subsystem. It is estimated that about 38% of the faults in voltage source conversion systems are due to failures of power devices, which can be broadly categorized as short-circuit faults and open-switch faults [83, 84].

4.1.1 Pre-fault Operation of the Converter

The studied three-phase PWM inverter with split-wound coupled inductors is constituted by switching power devices (q_{x1}-q_{x2}, with $x = a, b, c$), six diodes (d_{x1}-d_{x2}, with $x = a, b, c$) and three split-wound coupled inductors. The state of the switches can be represented by a binary variable, where q_{x1}=0 means an open switch and q_{x1}=1 means a closed switch.

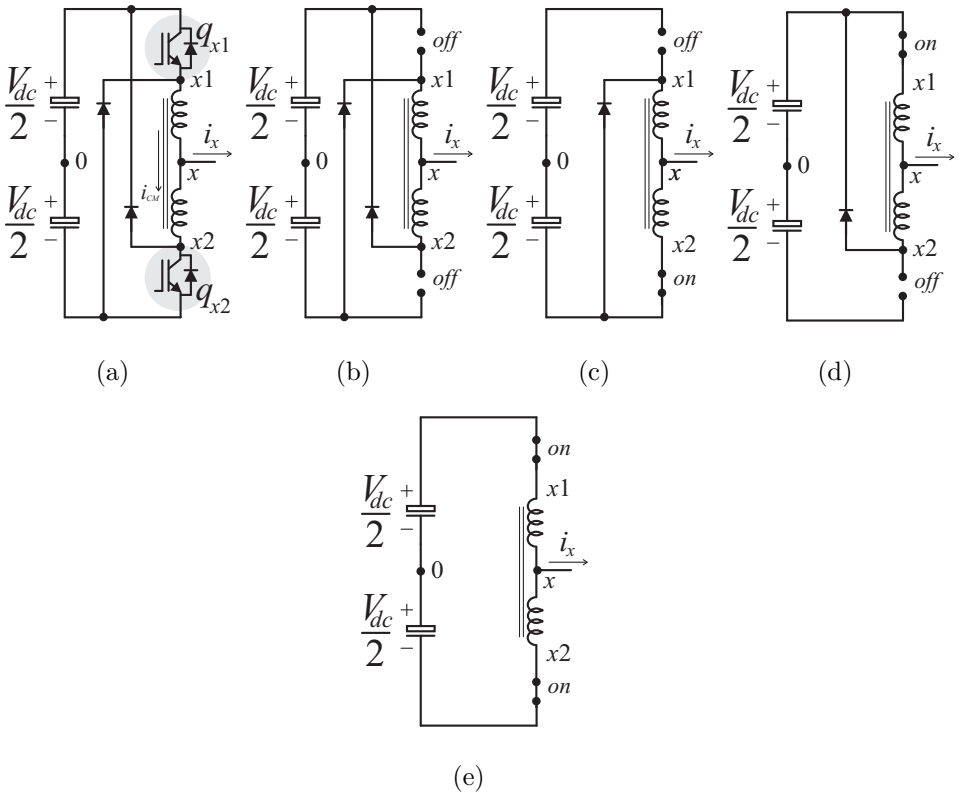


Fig. 4.3. (a)Operation in continuous conduction mode. (b)q_{x1}=q_{x2}=0. (c)q_{x1}=0 and q_{x2}=1. (d)q_{x1}=1 and q_{x2}=0. (e)q_{x1}=q_{x2}=1.

It is assumed that the currents in the coupled-windings are in continuous conduction mode, as highlighted in Fig. 4.3 (a). Figs. 4.3 (b), 4.3 (c), 4.3 (d) and 4.3 (e) show the equivalent circuit for each leg when (q_{x1},q_{x2}) are equal to (0,0), (0,1), (1,0) and (1,1), respectively.

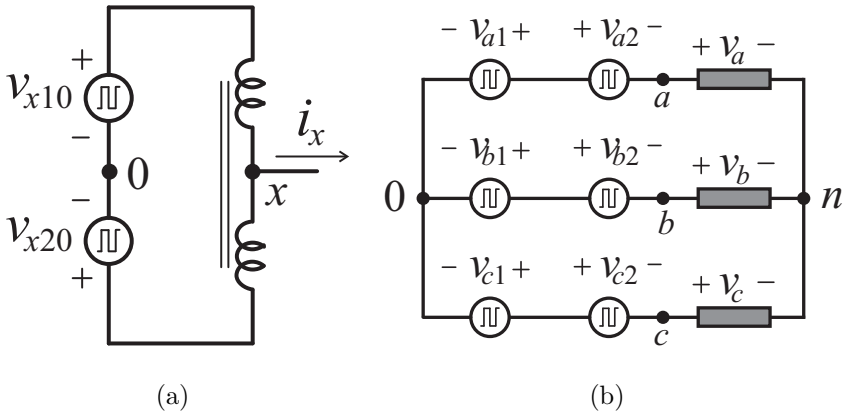


Fig. 4.4. (a) Leg model. (b) Model of three-phase PWM inverter with split-wound coupled inductors.

The voltages v_{x10} and v_{x20} (voltages from the points $x1$ and $x2$ to the DC-link capacitor midpoint) can be expressed as a function of the state of the switches q_{x1} and q_{x2}, respectively as following:

$$v_{x10} = (2q_{x1} - 1)\,\frac{V_{dc}}{2} \tag{4.1}$$

$$v_{x20} = (2q_{x2} - 1)\,\frac{-V_{dc}}{2} \tag{4.2}$$

This means that each leg can be modeled as in Fig. 4.4 (a). Then the pole voltages v_{x0} will be given by:

$$v_{x0} = \frac{1}{2}\,(v_{x10} + v_{x20}) \tag{4.3}$$

Hence from 4.1-4.3 it is possible to write v_{x0} as a function only of the state of the switches:

$$v_{x0} = (q_{x1} - q_{x2})\,\frac{V_{dc}}{2} \tag{4.4}$$

or

$$v_{x0} = v_{x1} - v_{x2} \tag{4.5}$$

From 4.5 it is possible to model the three-phase converter as depicted in Fig. 4.4 (b).

Table 4.1.
Pole voltage as a function of the switching states ($x = a, b, c$).

q_{x1}	q_{x2}	v_{x10}	v_{x20}	v_{x0}
0	0	$-V_{dc}/2$	$V_{dc}/2$	0
0	1	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$
1	0	$V_{dc}/2$	$V_{dc}/2$	$V_{dc}/2$
1	1	$V_{dc}/2$	$-V_{dc}/2$	0

Table 4.1 shows the pole voltages as a function of the state of the switches, where $x = a, b, c$. From this table, it is possible to validate the model presented in Fig. 4.4 (b) for the continuous conduction mode.

$$v_{x0} = (q_{x1} - q_{x2}) \frac{V_{dc}}{2} \tag{4.6}$$

$$v_{x0} = v_{x1} - v_{x2} \tag{4.7}$$

Where $v_{x1} = q_{x1}V_{dc}/2$ and $v_{x2} = q_{x2}V_{dc}/2$. Since 4.2 describes the behavior of the pole voltages, it is possible to draw the model of the three-phase PWM Inverter with split-wound coupled inductors as in Fig. 4.4.

4.1.2 PWM Strategy

If the desired voltage in the three-phase load is given by v_a^*, v_b^* and v_c^*, then the reference pole voltage can be written as:

$$v_{a0}^* = v_a^* + v_\mu^* \tag{4.8}$$

$$v_{b0}^* = v_b^* + v_\mu^* \tag{4.9}$$

$$v_{c0}^* = v_c^* + v_\mu^* \tag{4.10}$$

The voltage v_μ^* is introduced to minimize the voltage distortion, which can be calculated taking into account the general apportioning factor μ, that is:

$$v_\mu^* = E(\mu - \frac{1}{2}) - \mu v_{\max}^* + (\mu - 1)v_{\min}^* \tag{4.11}$$

Where $v^*_{\max} = \max V$, $v^*_{\min} = \min V$, and $V = \{v^*_a, v^*_b, v^*_c\}$. This expression was derived by using a similar approach for determining the three-phase PWM modulator [64, 65]. The apportioning factor μ ($0 \leq \mu \leq 1$) can be changed to reduce the THD (Total Harmonic Distortion) of the three-phase split-wound coupled inverter, as done for a conventional inverter [64,65]. Once the reference pole voltages were defined, the reference pole voltages v^*_{x1} and v^*_{x2} can be defined as following:

$$v^*_{x1} = \frac{v^*_{x0}}{2} \tag{4.12}$$

$$v^*_{x2} = -\frac{v^*_{x0}}{2} \tag{4.13}$$

Where v^*_{kx} is a voltage used to keep the converter in a continuous conduction mode.

4.1.3 Fault Detection Strategy

Power switch fault detection is based on the comparison between measured and estimated pole voltages. The estimated pole voltage (v_{x0e}) is expressed as a function of the switching states as follows $v_{x0e} = (q_{x1} - q_{x2})V_{dc}/2$ with $x = a, b, c$. In this equation q_{x1} and q_{x2} represent state of the switches S_{x1} and S_{x2}, respectively. The fault occurrence can be determined by analyzing the voltage error which can be obtained by comparing the measured and estimated pole voltages. This voltage error is given by: $\varepsilon = v_{x0} - v_{x0e}$, where v_{x0} is the measured pole voltage.

In normal operation, the measured and estimated pole voltages are equal, and thus, their difference is zero. But when a fault appears in one of those switches the value of the voltage error ε will not be zero anymore. This error signal will be used to determined which switch is under fault and then send the signal to triacs for reconfiguration purposes.

4.1.4 Leg-isolation Procedure

Fig. 4.5 shows the step by step procedure to isolate a leg under short-circuit failure, i.e., reconfiguration operation where upon information provided by the fault

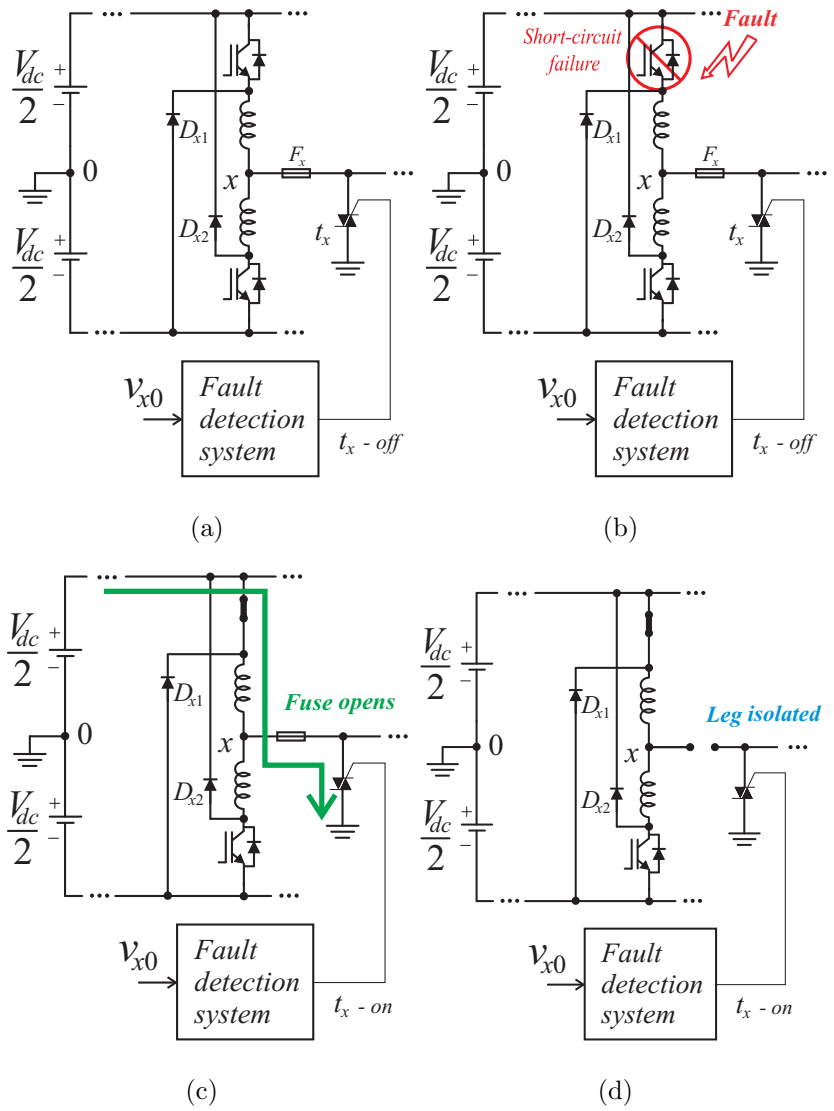


Fig. 4.5. Procedure for leg isolation: (a) healthy operation, (b) short-circuit failure, (c) triac on and (d) leg isolation.

detection system removes faulty components. Fig. 4.5 (a) shows the converter healthy operation, which means that the voltage error ε will be zero, then the Fault detection system will keep the triac off. Fig. 4.5 (b) highlights the moment of a short-circuit failure, once this fault is detected, the control system will turn on the triac, which will blow the fuse, as observed in Figs. 4.5 (c) and 4.5 (d). It's worth mentioning that, in a conventional converter, there is no inductor placed inside of the leg, which

means that the short-circuit current before the opening of fuses (i.e., interval of time between Figs. 4.5 (b) and 4.5 (d)) will pass through the DC-link capacitor. On the other hand, as observed in Fig. 4.5 (c) the coupled inductors avoid the instantaneous variation of the current, which will protect the DC-link capacitor.

4.1.5 Simulation Results

The PWM approach proposed in this paper has been validated by simulation, tested for a three-phase RL load ($R = 50\Omega, L = 15mH$). Figs 4.6-4.8 show the simulation results for $\mu = 0, \mu = 0.5$ and $\mu = 1$ respectively. From top to bottom; load current (i_a), reference pole voltage (v^*_{a0}), pole voltage (v_{a0}), and the voltages (v_{a10}) and (v_{a20}) (voltage from points a_1 and a_2 to the DC-link capacitor mid-point).

Fig. 4.9 (a) shows the post-fault configuration after the reconfiguration approach. Fig. 4.9 (b) shows the simulation results with a fault (short-circuit failure) occurring in switch S_{a1} at t = 0.05s, the variables in this figure are from top to bottom: triac gating signal (t_a), line-to-line voltage (v_{12}), three-phase currents (i_a, i_b and i_c) and fuse current (i_{Fa}). It is worth mentioning that no short-circuit current is observed (i.e., isolation without capacitor stress) in the isolation procedure.

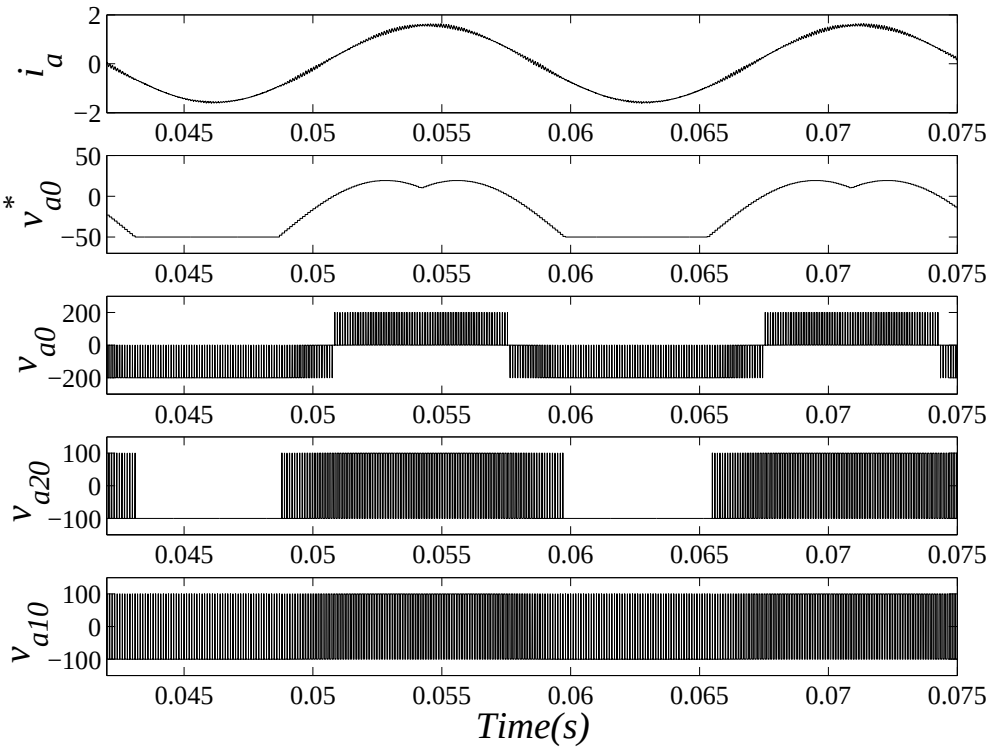


Fig. 4.6. Simulation results for one phase when $\mu = 0$ from top to bottom: load current, reference pole voltage, pole voltage and the voltages from points a_1 and a_2 to the DC-link capacitor.

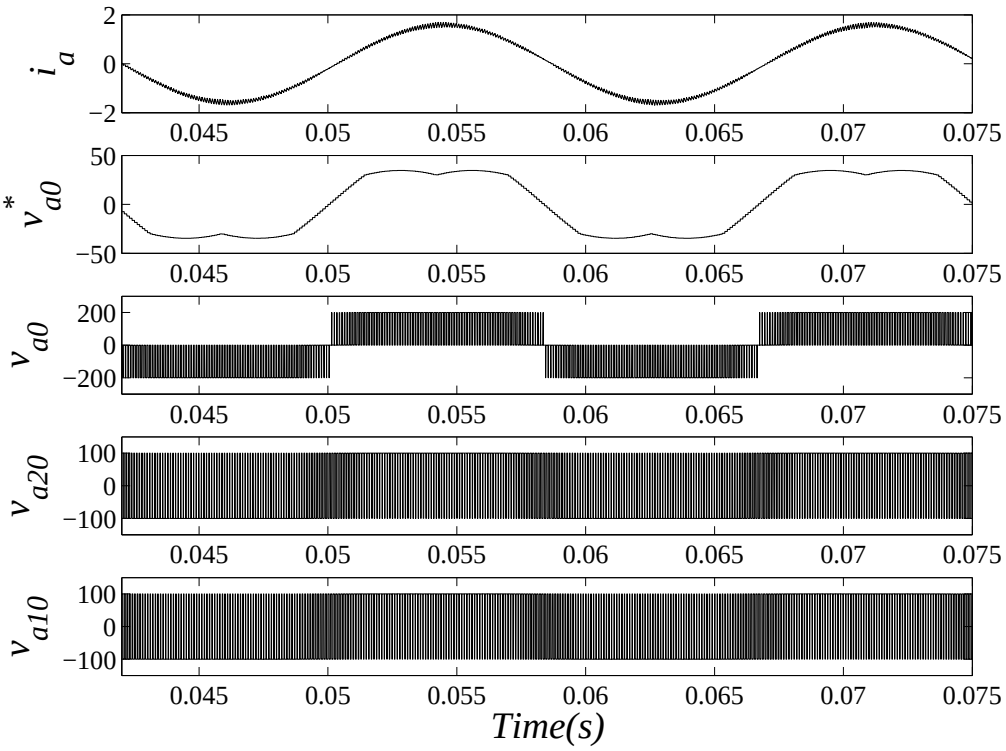


Fig. 4.7. Simulation results for one phase when $\mu = 0.5$ from top to bottom: load current, reference pole voltage, pole voltage and the voltages from points a_1 and a_2 to the DC-link capacitor.

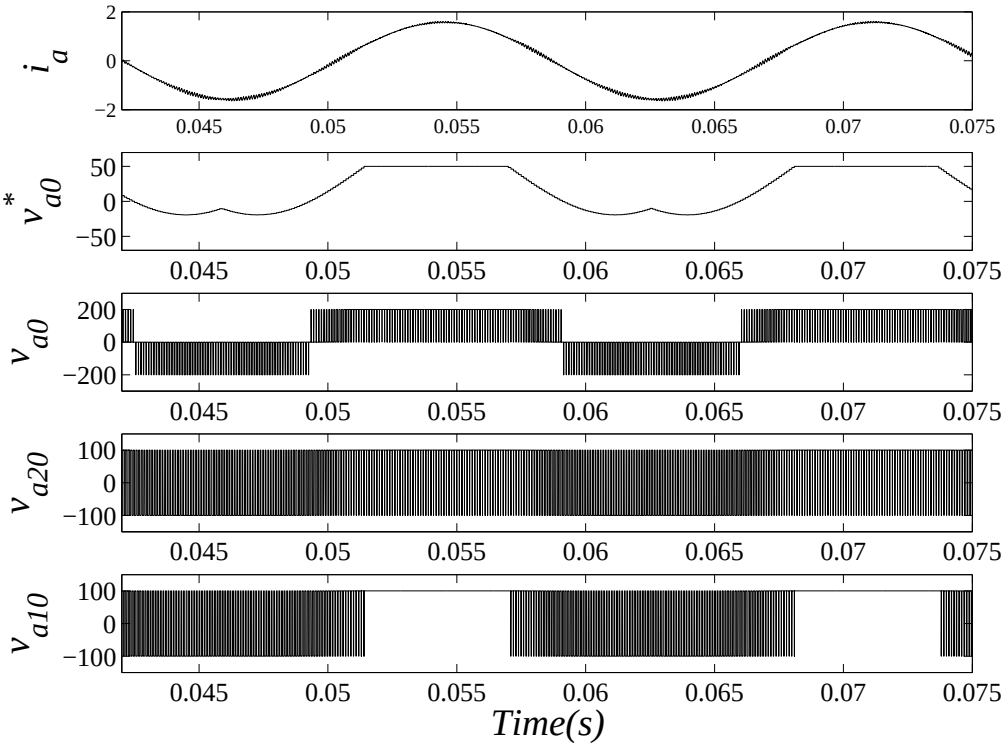
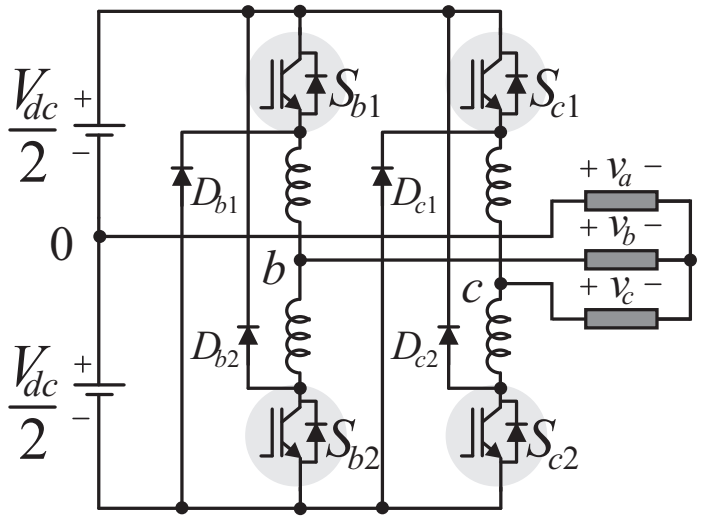
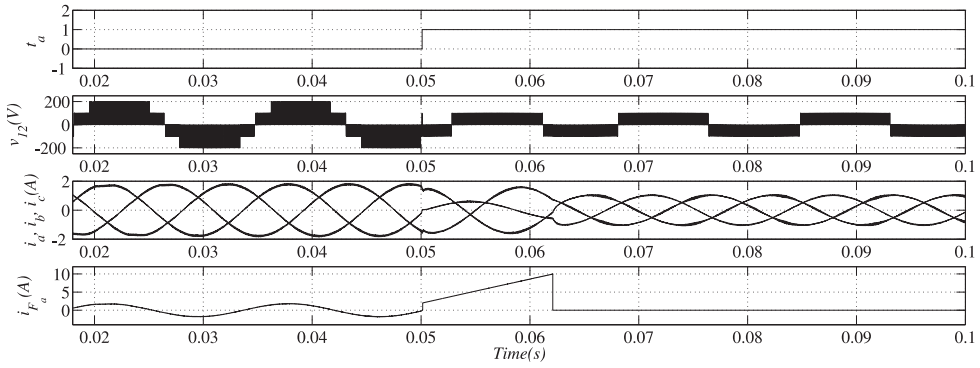


Fig. 4.8. Simulation results for one phase when $\mu = 1$ from top to bottom: load current, reference pole voltage, pole voltage and the voltages from points a_1 and a_2 to the DC-link capacitor.



(a)



(b)

Fig. 4.9. (a) Post-fault topology. (b) Simulation results showing from top to bottom: triac gating signal, line-to-line voltage, three-phase currents and fuse current.

4.1.6 Conclusion

This chapter presented a fault tolerant converter designed for low power applications, widely demanded and employed in a micro-grid environment. In comparison with the solutions presented in the technical literature, the proposed design enhanced the followings aspects: i) it has higher number of levels while using the same amount of controlled switching devices (six IGBTs); ii) there is no dead-time requirement for the converter's operation. This is an important characteristics for high-frequency micro-grid systems; and ii) leg isolation procedure with lower stress for the DC-link capacitor.

5. PROOF-OF-CONCEPT EXPERIMENTAL SETUP

This chapter presents all experimental results, the boards, type of the switches employed in this board, drivers, and information about Digital Signal Processing (DSP).

5.1 DSP

Fig. 5.1. DSP Board.

The switching signals for IGBTs in this thesis are determined by using Texas Instrument (TI) eZdsp starter kit TMS320F28335 illustrated in Fig. 5.1. This kit contains 128Kx16 asynchronous SRAM, the JTAG emulator, and F28335 target board. In this thesis the starter kit is used to generate two high frequency (10KHz) PWM signals and two complementary low frequency (50Hz) PWM signals, the modulation strategy of high frequency signals is explained in Chapter 2 of this thesis. The DSP

board is supplied by the grid through a power connector which converts the grid voltage to 5 volts. Code Composer Studio software (V3.3) is used to program the starter kit, this composer includes assembler, linker, compiler, and real-time debug support. Six PWMs can be generated by this DSP board and each PWM has a dual port (port A and B) which can be set to be complementary of each other if needed. For instance, for the proposed single-phase DC/AC converter, the first and second high frequency switching signals can be generated from each of the available six PWMs, in this case EPWM (Enhanced PWM) 1A and 3A are used. The third and fourth low frequency switching signals, which are complement of each other, can be obtained from dual port A and B of the EPWM2. The related codes for generation of the high frequency switching signals for the proposed converter are given as:

```
#define  h 100e-6
#define ws 628
float  D1b=0., s1b=0., s2b=0.,vs1_ref = 0., vs2_ref = 0., vs3_ref = 0.;
float va=0., vb=0., vc=0., E=400, teta = 0;
teta = teta + ws*h;
if (teta >= 2*pi)
{
    teta -= 2*pi;
}
va=311*sin(teta)
if   (va<= 0 )
{
s1b=1;
}
else
{
s1b=0;
}
```

```
vs2_ref=(((vb+2*va)/(2*E)+s1b);              //Da1
vs1_ref=(((vb-2*va+2*E)/(2*E)-s1b) ;        //Da2
```

It worth mentioning that the above two equations for D_{a1} and D_{a2} are explained in Chapter 2 equations 2.15 and 2.16. The related codes for the two low frequency switching signals are:

```
vc=A*sin(teta);
vs3_ref=vc;
```

Where amplitude A is a large number.

A dead-band function is used in order to avoid short circuit for the low frequency complementary switching signals. A dead-band can be added to EPWM2 by using the dead-band generator control register information presented in Table 5.1 and following codes:

```
// Set actions
EPwm2Regs.DBCTL.bit.IN_MODE =0*02;
EPwm2Regs.DBCTL.bit.POLSEL =0*01;
EPwm2Regs.DBCTL.bit.OUT_MODE =0*03;
//EPWMxA In (from the action-qualifier) is the source for rising-edge
//delayed signal, EPWMxB In (from the action-qualifier) is the source
//for falling-edge delayed signal.
//Active low complementary (ALC) mode. EPWMxA is inverted.
//Dead-band is fully enabled for both rising-edge delay on output
//EPWMxA and falling-edge delay on output EPWMxB.
//The input signal for the delay is determined by DBCTL[IN_MODE].
```

The dead-band delay value can be set using DBFED (Dead-Band Falling Edge Delay) and DBRED (Dead-Band Rising Edge Delay) functions, the equivalent delay values in μS as a function of DBFED and DBRED are presented in Table 5.2. In this case a dead-band value of 500 is used which is equivalent to 5 μs:

Table 5.1.
Dead-Band Generator Control Register (DBCTL) Field Descriptions.

Bits	Name	Value	Description
$15-6$	Reserved		Reserved
$5-4$	IN_MODE	00	EPWMA In (from the action-qualifier) is the source for both falling-edge and rising-edge delay.
		01	EPWMxB In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxA In (from the action-qualifier) is the source for falling-edge delayed signal.
		10	EPWMxA In (from the action-qualifier) is the source for rising-edge delayed signal. EPWMxB In (from the action-qualifier) is the source for falling-edge delayed signal.
		11	EPWMxB In (from the action-qualifier) is the source for both rising-edge delay and falling-edge delayed signal.
$3-2$	POLSEL	00	Active high (AH) mode. Neither EPWMxA nor EPWMxB is inverted.
		01	Active low complementary (ALC) mode. EPWMxA is inverted.
		10	Active high complementary (AHC). EPWMxB is inverted.
		11	Active low (AL) mode. Both EPWMxA and EPWMxB are inverted.
$1-0$	OUT_MODE	00	Dead-band generation is bypassed for both output signals. In this mode, both the EPWMxA and EPWMxB output signals from the action-qualifier are passed directly to the PWM-chopper submodule.
		01	Disable rising-edge delay. The EPWMxA signal from the action-qualifier is passed straight through to the EPWMxA input of the PWM-chopper submodule. The falling-edge delayed signal is seen on output EPWMxB. The input signal for the delay is determinedby DBCTL[IN_MODE].
		10	The rising-edge delayed signal is seen on output EPWMxA. The input signal for the delay is determined by DBCTL[IN_MODE]. Disable falling-edge delay. The EPWMxB signal from the action-qualifier is passed straight through to the EPWMxB input of the PWM-chopper submodule.
		11	Dead-band is fully enabled for both rising-edge delay on output EPWMxA and falling-edge delay on output EPWMxB. The input signal for the delay is determined by DBCTL[IN_MODE].

Table 5.2.
Dead-Band Delay Values in μs as a function of DBFED and DBRED.

Dead-Band Value	Dead-Band Delay μs		
DBFED,DBRED	TBCLK=SYSCLKOUT/1	TBCLK=SYSCLKOUT/2	TBCLK=SYSCLKOUT/4
1	0.01μ	0.02μ	0.04μ
5	0.05μ	0.10μ	0.20μ
10	0.10μ	0.20μ	0.40μ
100	1.00μ	2.00μ	4.00μ
200	2.00μ	4.00μ	8.00μ
300	3.00μ	6.00μ	12.00μ
400	4.00μ	8.00μ	16.00μ
500	5.00μ	10.00μ	20.00μ
600	6.00μ	12.00μ	24.00μ
700	7.00μ	14.00μ	28.00μ
800	8.00μ	16.00μ	32.00μ
900	9.00μ	18.00μ	36.00μ
1000	10.00μ	20.00μ	40.00μ

```
EPwm2Regs.DBFED = 500;
EPwm2Regs.DBRED = 500;
```

AQCTLA/B (Action-Qualifier Output A/B Control Register) function can be used to force EPWM high or low when the counter is incrementing or decrementing, more comprehensive information in this regard is available in [115]. For all four switching signals the following codes are used:

```
// Set actions
EPwm1Regs.AQCTLA.all = 0;
EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;        // Set: force EPWMxX output high.
EPwm1Regs.AQCTLA.bit.CAD = AQ_CLEAR;     //Clear: force EPWMxX output low
EPwm2Regs.AQCTLA.all = 0;
EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;
EPwm2Regs.AQCTLA.bit.CAD = AQ_CLEAR ;
EPwm2Regs.AQCTLB.all = 0;
```

```
EPwm2Regs.AQCTLB.bit.CBU = AQ_SET;
EPwm2Regs.AQCTLB.bit.CBD = AQ_CLEAR;
EPwm3Regs.AQCTLA.all = 0;
EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;
EPwm3Regs.AQCTLA.bit.CAD = AQ_CLEAR;
```

It should be keep in mind that for the low frequency switching signals generated by EPWM2 A and B, the Active Low Complementary (ALC) mode is set for the EPWM2. Therefore the EPWM2A is inverted; as a result the AQCTLA and AQCTLB should be identical.The GPIOs on the P8 connector of the DSP board are:

```
EPwm2Regs.CMPA.half.CMPA = vs3_ref*(7500);              //sb1
EPwm2Regs.CMPB = vs3_ref*(7500);                        //sb2
EPwm3Regs.CMPA.half.CMPA = vs2_ref*(7500);      //sa1
EPwm1Regs.CMPA.half.CMPA = vs1_ref*(7500);     //sa2
```

5.2 Experimental Prototype

In this thesis, the proposed converter is firstly built using the base board 2BB0108T illustrated in Fig. 5.2. Then the converter prototype is built on a Printed Circuit Board (PCB) to reduce the wiring which improves the efficiency of the converter.

Fig. 5.2. 2BB0108T Base board.

5.2.1 Converter Using the Base Board

The 2SC0108T dual driver as depicted in Fig. 5.3 is used for the BSM75GB60DLC IGBT modules due to its high efficiency, low cost, and its capability to protect circuit from a short circuit. A printed circuit board illustrated in Fig. 5.4 is built to connect DSP, power supply, and drivers; by using this board less wiring is needed.

Fig. 5.3. 2SC0108T dual driver.

Fig. 5.4. 2SC0108T dual driver.

The IGBT modules for the base board are illustrated in Fig. 5.5. This IGBT is from the EUPEC company which is used as a switch in this experimental setup. Collector-emitter voltage (VCE) can goes up to 600 volts and the collector current

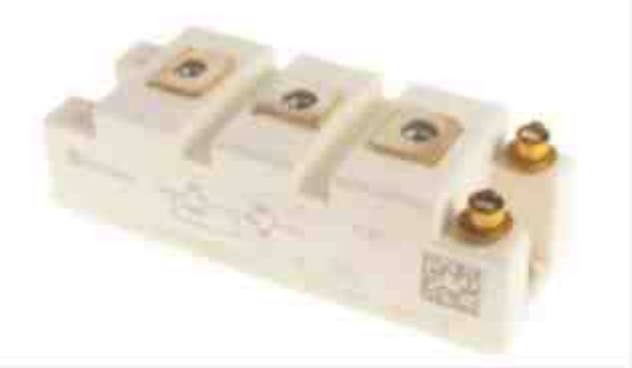


Fig. 5.5. BSM75GB60DLC IGBT modules.

at $75C^{\circ}$ and $25C^{\circ}$can go up to $75A$ and $100A$ respectively. To avoid the failure in the system due to rise in temperature of the IGBT switches, the power IGBTs must attach on the heat-sink illustrated in Fig. 5.6. The DC power supply for the proposed DC/AC converter is provided by the power supply illustrated in Fig. 5.7. A DC-link capacitor illustrated in Fig. 5.8 is used in the converter to avoid the switching network from oscillating at an inappropriate moment.

The coupled inductor illustrated in Fig. 5.9 for the proposed converter has 4 terminals, each inductor is $50\mu H$, $10A$ RMS, and $20KHz$. The core dimension of the coupled inductor is $2in.H \times 2in.W \times 2in.D$. Both inductors are placed on the center of the EE core. A resistive-inductive load with $R = 39.6\Omega$, $L = 5\text{m}H$ is considered for this experimental setup. Switching frequency of $20KHz$ and DC-link voltage of $15\,V$ is used in this setup. The experimental setup and results are illustrated in Fig. 5.10 and 5.11 respectively.

Fig. 5.6. Heat-sink for BSM75GB60DLC IGBT modules.

Fig. 5.7. DC Power Supply.

Fig. 5.8. DC-link capacitor.

Fig. 5.9. Coupled inductor.

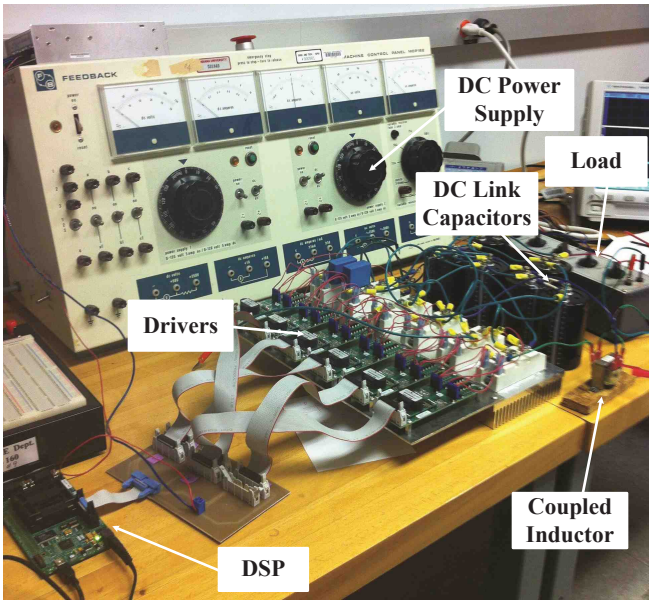


Fig. 5.10. Experimental setup.

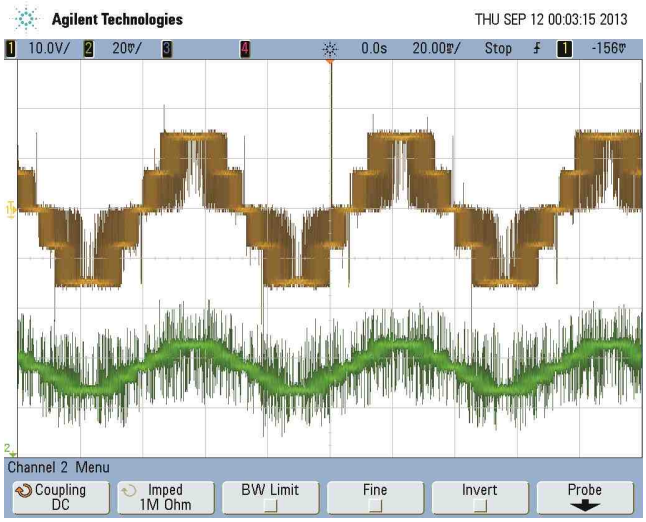


Fig. 5.11. Experimental results of the load voltage (top) and load current (bottom) using the base board and BSM75GB60DLC IGBT modules.

5.2.2 Converter Built on the PCB

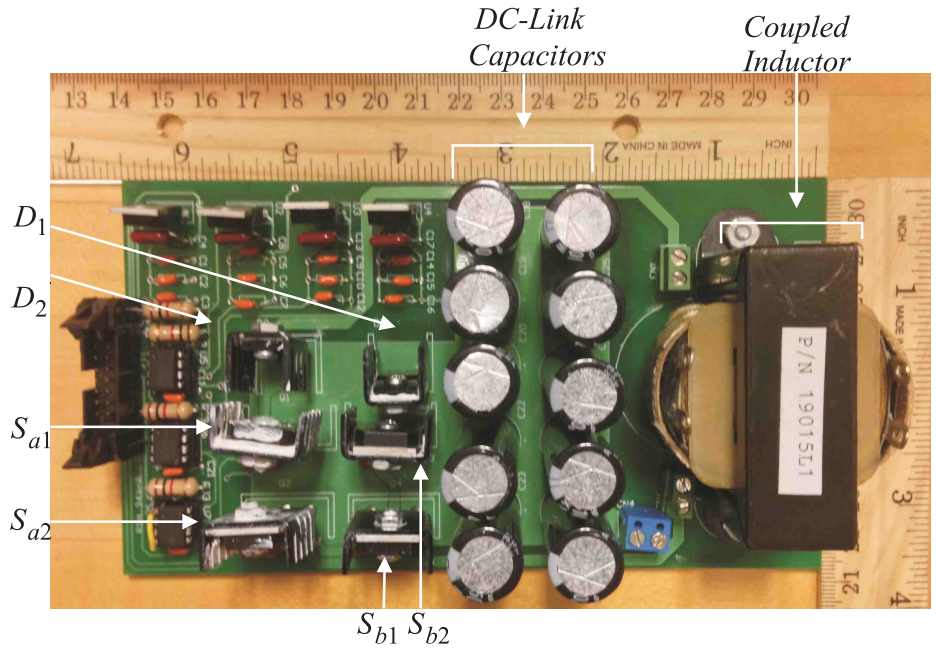
In this thesis the converter is built on a printed circuit board (PCB) to reduce the size of the converter and the amount of wiring. The PCB is designed by Altium software. In this prototype all drivers, IGBTs, DC-link capacitors, and coupled inductors are on a same board. The main components of the converter are four power MOSFETs (S_{a1}, S_{a2}, S_{b1} and S_{b2}- IXTQ460P2), four MOSFET drivers (MIC4420/4429), two power diodes (D_1 and D_2- BYC20X-600), ten electrolytic capacitors of 100μF each, and finally a coupled inductor. In order to protect the DSP board, HCPL-2231/32 optocoupler is used to connect the DSP board to the drivers. The selected power MOSFETs have the drain-source voltage and drain current maximum ratings of 500V and 24A respectively. The selected power diodes have extremely fast switching and low reverse recovery current characteristics. As discussed earlier in Chapter 2 of this thesis, in order to reduce the voltage spikes across the MOSFET, a RCD snubber is added to the converter high-frequency switches. The experimental prototype without and with RCD snubber circuit is illustrated in Fig. 5.12, this photo highlights the main components employed in the proposed single phase DC/AC converter.

Fig. 5.13 illustrates the experimental result of the voltage across switch S_{a1} for three cases. In Fig. 5.13 (a) no snubber is added across the switch S_{a1}, as it is shown the spike voltage across the switch is approximately $17.2\,V$. This spike voltage reduces to $14.5\,V$ in Fig. 5.13 (b) when RCD snubber circuit is added with capacitor $12nF$ and 16.6Ω resistor. In Fig. 5.13 (c) the snubber capacitor value increased to $47nF$ and the resistor remains at 16.6Ω, we can observe that the spike voltage substantially decreased and it is approximately $7.7\,V$. All results presented were obtained with the converter operating under the following conditions: switching frequency of $10KHz$, DC-link voltage of $50\,V$, and a resistive load of 100Ω, the load voltage v_l has 5 levels $(\pm V_{dc}, 0, \pm V_{dc}/2)$.

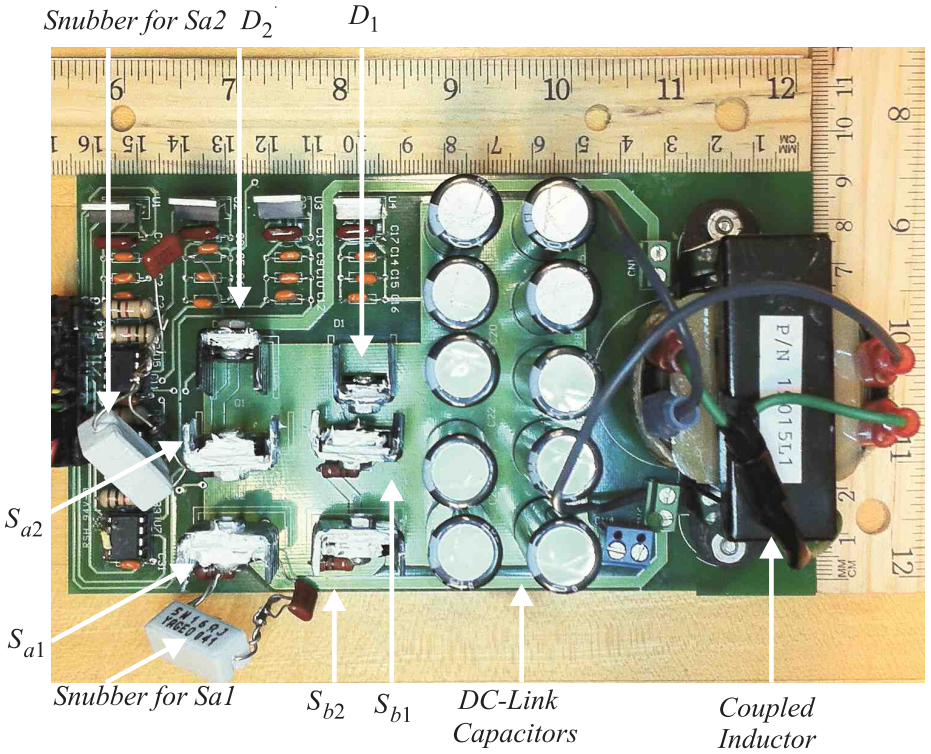
Fig. 5.14 (a) illustrates the experimental result without RCD snubber circuit, Fig. 5.14 (b) illustrates the experimental results with RCD snubber circuit when

the snubber capacitor is $12nF$ and resistor is 16.6Ω, and Fig. 5.14 (c) shows the experimental results with RCD snubber circuit when the snubber capacitor is $47nF$ and resistor is 16.6Ω.

Fig. 5.15 (a) presents the PWM signal for one leg of proposed fault tolerant converter, presented in Chapter 3, which is obtained in the experimental setup with the Digital Signal Processing (DSP). DSP generates the desired PWM to control each switch. In each leg currents have shifted 180° and the current of each leg has shifted 120°. The set of PWMs generated for the two legs are shown in Fig.5.15 (b).



(a)



(b)

Fig. 5.12. Experimental prototype (a) without RCD snubber (b) with RCD snubber.

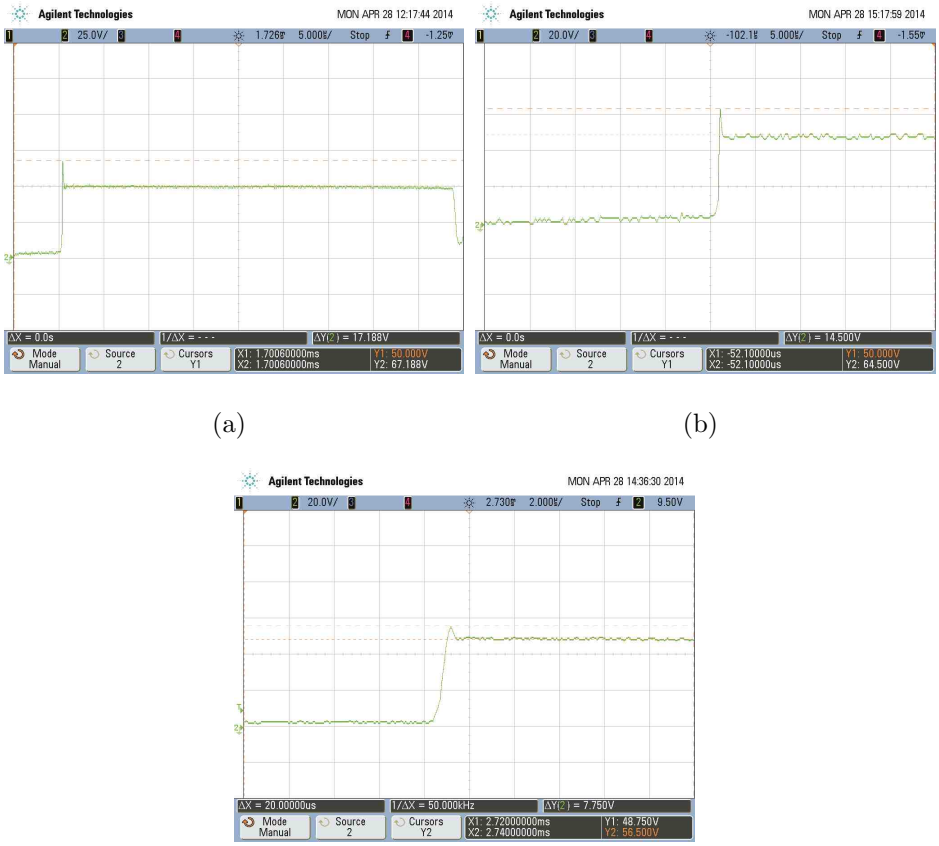
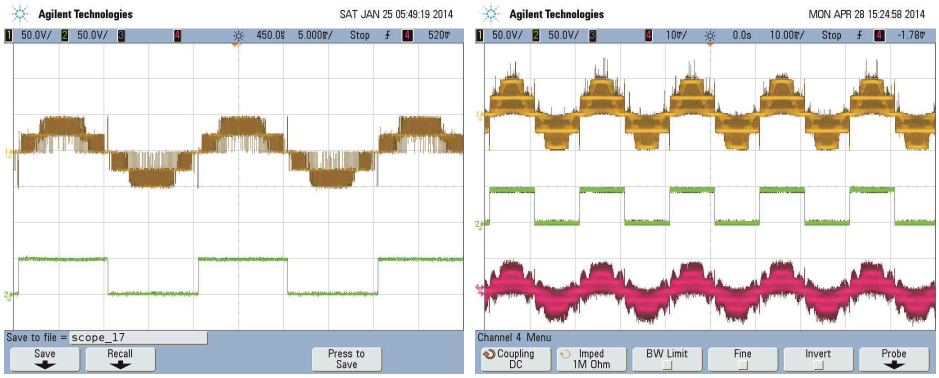
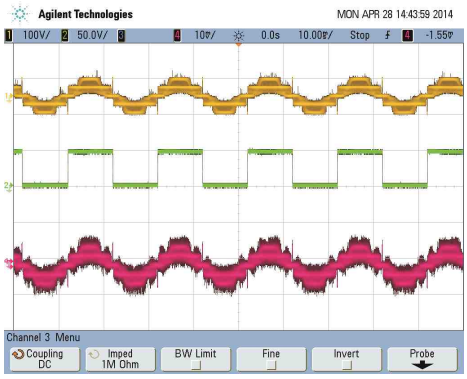


Fig. 5.13. Voltage across switch S_{a1} (a) no snubber (b) with snubber $12nF$ and 16.6Ω (c) with snubber $47nF$ and 16.6Ω.

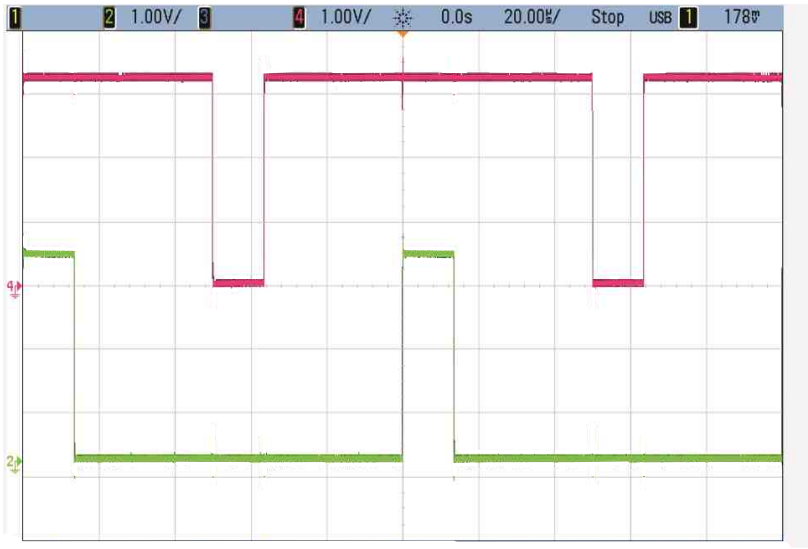


(a) (b)

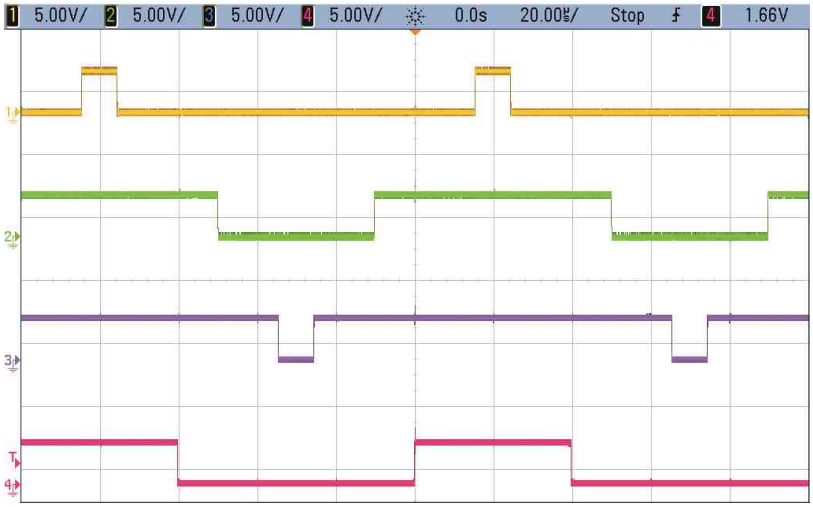


(c)

Fig. 5.14. (a) Experimental result (from top to bottom) load voltage, voltage for S_{b1}, and load current respectively (b) with snubber $12nF$ and 16.6Ω. (c) with snubber $47nF$ and 16.6Ω.



(a)



(b)

Fig. 5.15. (a) Experimental result to generate the PWM for one leg (b)Experimental result to generate PWMs for two legs.

6. CONCLUSION AND FUTURE WORK

6.1 Conclusions

This thesis focuses on the DC/AC voltage source inverters with ability to synthesize multilevel voltages. The increase in the power that needs to be managed by systems such as motor drives and distributed generation leads to the use of more voltage levels, leading to more complex structures based on a single and multi-cell converter such as multilevel converters. A multilevel converter is an interesting alternative for power conversion, since it allows an efficient power supply suitable for high voltage and high power applications. The proposed multilevel converter in this thesis has an optimized relationship between the number of levels per number of switches (nL/nS). The proposed five-level four-switch converter has $nL/nS = 5/4$ which is by far the best relationship among the converters proposed in the technical literature. The most important characteristics of the proposed configuration are: (i) reduced number of semiconductor devices, while keeping a high number of levels at the output converter side, (ii) only one DC source without any need to balance capacitor voltages, and (iii) high efficiency. Details regarding the operation of the proposed topology and modulation strategy for single and three phase converters are presented, as well as the comparison between the proposed converter and the conventional ones. Existence of a significantly large spike voltage across the switches may damage the switch. Thus, a RCD snubber circuit (using a resistor, a capacitor and a diode) is used in the proposed topology to clamp the voltage across the switch. Experimental results of the converter prototype with and without RCD snubber are presented to validate the simulation results. Considering a micro-grid system, fault tolerance operations of the system is very important in order to achieve a suitable level of reliability in a typical micro-grid system. Due to existence of plenty of power

electronic converters in micro-grid systems, fault tolerant in power electronics converters are really important. This thesis presents a fault tolerant converter designed for low power applications, as required in micro-grid systems. Furthermore, this thesis presents a hybrid pulse width modulation for the pre-fault operation as well as fault detection and leg-isolation procedure. Simulation results demonstrate the validity of the proposed method.

6.2 Future Work

To pursue this thesis in the future the following challenges should be considered:

1. Designing the coupled inductor filter using Finite-Element Analysis (FEA) tools [116, 117]. The FEA tools are able to consider all parasitic elements of the windings and as a result a more accurate filter can be designed for the proposed converter. A more accurate coupled inductor filter will reduce the amount of noises at the output voltage and current of the converter.

2. In the converter prototype three DC power supplies are used to provide a +5 V for optocouplers and MOSFET drivers. This makes the system bulky and adds some unwanted noises to the system. The future plan is to design the converter in a way to use only one power supply.

3. The modulation strategy in this thesis considered only open loop control. Design of the closed loop controller for the proposed multilevel inverter is the future work of this thesis. Closed loop current control of the multilevel inverter compensates for circuit non-idealities and performs the desired current tracking. Design of the closed loop control for the proposed converter is not straight forward and it has several challenges that should be considered such as: fast dynamic response, minimization of the THD introduced by modulation and control strategy, and good performance for wide range of load and DC-link voltages.

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