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Selective epitaxial growth techniques to integrate high-quality germanium on silicon

Darin Leonhardt

Department

SELECTIVE EPITAXIAL GROWTH TECHNIQUES TO INTEGRATE HIGH-QUALITY GERMANIUM ON SILICON

BY

DARIN LEONHARDT

B. S., Chemical Engineering, University of New Mexico, 2005

A. A. S., Semiconductor Manufacturing Technology, San Juan College, 1997

DISSERTATION

Submitted in Partial Fulfillment of the
Requirements for the Degree of

Doctor of Philosophy
Engineering

The University of New Mexico
Albuquerque, New Mexico
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DEDICATION

I dedicate this work, first and foremost, to my beautiful and longsuffering wife, Shasta Leonhardt. Her support and understanding of all the late nights and weekends spend studying and working in the lab has allowed me to fulfill my research goals for this work. Without the sacrifices she made in allowing me to pursue my dreams, none of this work would have been possible. She has stood by me through all the difficulties of graduate school and has been the best friend, helper, and partner I could have asked for.

Second, this work is dedicated to my parents and grandparents Jon Leonhardt, Beverly and Frosty Heath, Steve and Ellen Sample, Jean and Rodney Heath, and Eva and Henry Trujillo for their support and encouragement to fulfill my potential and pursue my dreams. I hope I have made them proud of my accomplishments and will continue to do so in my future endeavors.

Third, I also dedicate this work to my extended family and friends for their encouragement and understanding when I was often absent from family functions, both mentally and physically.

Last but not least, I also dedicate this work to our new baby girl, Estoria Monet Leonhardt. Her arrival has spurred me onward to the finish line.

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ABSTRACT

High-quality Ge-on-Si heterostructures have been actively pursued for many advanced applications, including near-infrared photodetectors, high-mobility field effect transistors, and virtual substrates for integrating III-V multijunction solar cells. However, growing epitaxial Ge on Si poses many engineering challenges, ranging from lattice mismatch, to thermal expansion coefficient mismatch, to non-planar morphological evolution. The lattice mismatch between Ge and Si often leads to a high density of threading dislocations. These dislocations, if not reduced, propagate through the subsequently grown GaAs layer, deteriorating its quality. To overcome these engineering challenges, we have developed three different approaches based on molecular beam epitaxy to significantly reduce, manage, or eliminate the defects in Ge films grown on Si.

The first approach involves the nucleation of Ge islands within nanoscale windows in a thin layer of chemically grown SiO_2 and successive island coalescence over the SiO_2 to form a continuous film. Nanoscale contact areas between Ge and Si effectively relieve the lattice mismatch stress between Ge/Si so that dislocations do not nucleate. We observe that annealing the nucleated islands prior to full coalescence also leads to Ge films that are free of defects, along with significant improvement in GaAs integrated on Ge. The second approach involves trapping dislocations in Ge between high aspect ratio walls of SiO_2. Defects form during coalescence of Ge from adjacent channels and at the corners of the SiO_2 walls due to stress resulting from differences in thermal expansion coefficients of Ge, Si, and SiO_2. The third approach involves filling etch pits, which reveal dislocations, with SiO_2 and subsequent Ge growth over SiO_2. The filling prevents dislocations in the lower Ge layer from propagating into the upper Ge layer. The third method reduces the defect density from 2.8×10^8 cm^{-2} to 9.1×10^6 cm^{-2}, and is proven to be the most effective at reducing the defects in epitaxial growth of Ge on Si. We expect that our engineering approaches may finally resolve a longstanding engineering challenge in heteroepitaxy, finally providing the cost reduction needed for widespread commercialization of multijunction solar cells, light-emitting diodes, and high-mobility transistors on Si substrates.

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ABBREVIATIONS

2D	two-dimensional
3D	three-dimensional
AFM	atomic force microscopy
APB	antiphase boundary
ARC	anti-reflective coating
BE	backscattered electrons
CL	cathodoluminescence
CMOS	complementary metal-oxide-semiconductor
CMP	chemical-mechanical polishing
CSL	coincident site lattice
CVD	chemical vapor deposition
DI	de-ionized
EDS	energy dispersive spectroscopy
EELS	electron energy loss spectroscopy
ELO	epitaxial lateral overgrowth
EPD	etch pit density
FIB	focused ion beam
GoS	germanium on silicon
HBT	heterojunction bipolar transistor
IL	interferometric lithography
LED	light emitting diode
MBE	molecular beam epitaxy

MFP	mean free path
MJ	multijunction
ML	monolayer
MOSFET	metal-oxide-semiconductor field-effect transistor
MOVPE	metal-organic vapor phase epitaxy
NREL	National Renewable Energy Laboratory
PBN	pyrolytic born nitride
PL	photoluminescence
PMMA	polymethyl methacryclate
PR	photoresist
RMS	root-mean-square roughness
SE	secondary electrons
SEM	scanning electron microscopy
SF	stacking fault
SK	stranski-krastanov
SLS	strained layer superlattice
SNL	Sandia National Laboratories
STEM	scanning transmission electron microscopy
TC	thermocouple
TD	threading dislocation
TDD	threading dislocation density
TEM	transmission electron microscopy
TMA	trimethylalluminum

TMG	trimethylgallium
VW	volmer-weber
XPS	x-ray photoelectron spectroscopy
XRD	x-ray diffraction

CHAPTER 1 INTRODUCTION

1.1 Importance and Applications of Heteroepitaxy

Heteroepitaxy is the integration of one crystalline material upon another where the materials have different physical properties. The field of heteroepitaxy has been intensely researched for several decades for three primary application areas: substrate engineering, heterojunction devices, and device integration. Figure 1-1 shows the bandgap versus lattice constant for several important semiconductors that are used for device fabrication.

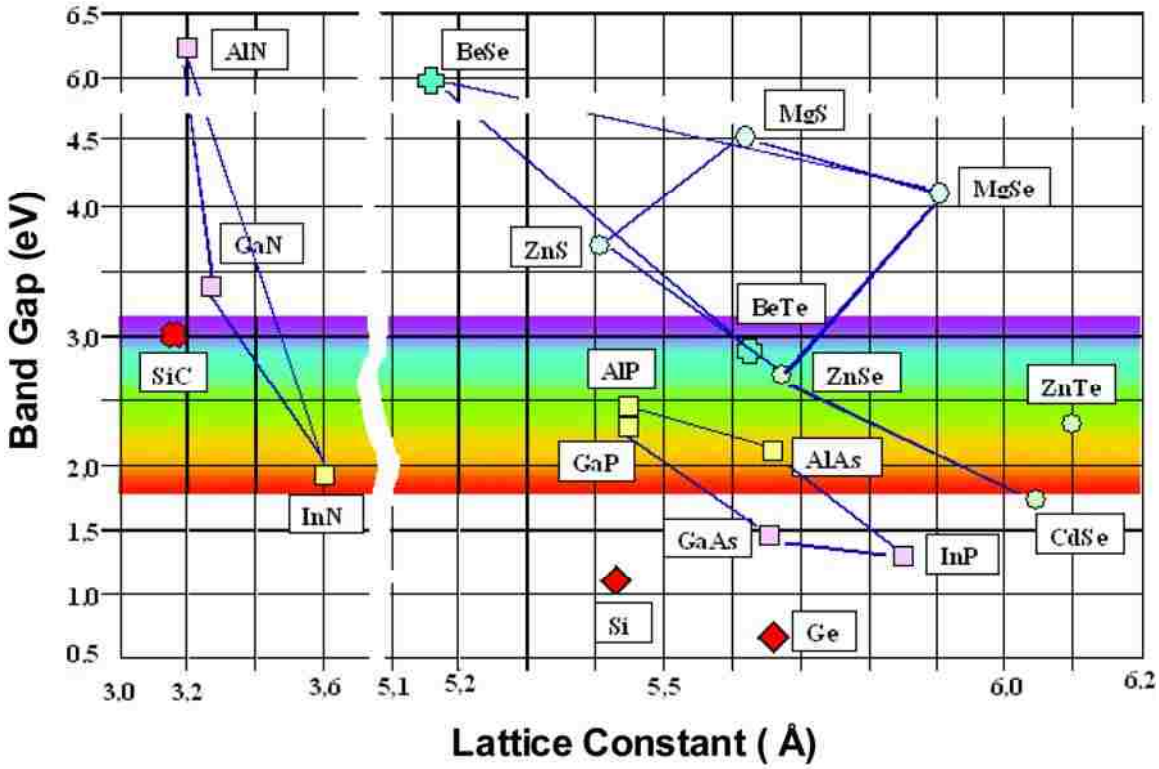


Figure 1-1. Band gap versus lattice constant for many important semiconductors.[1] Especially important is the Ge-GaAs-AlAs system that is widely researched due to the similarity of the lattice constants of the materials.

The band gap is an especially important property because it determines the emission and/or absorption wavelength of devices made from these materials such as light-emitting diodes (LEDs), solar cells, lasers, and detectors. In general, a combination of materials with different band gaps will require the use of heteroepitaxy due to the differing lattice constants of the materials.

Substrate engineering is necessary because many important semiconductors are not available in large-area, high-quality, single-crystal wafers. The few materials that are available as wafers include Si, Ge, GaAs, InP, SiC, and sapphire. However, Si is by far the most abundant material and available at much lower cost compared to the other semiconductors. A tremendous cost savings can be realized, therefore, by integrating devices made with these other materials onto Si substrates.

Heterojunction devices are another important application area of heteroepitaxy. Many devices now in commercial use require semiconductor heterojunctions. These devices include solar cells, high-brightness LEDs, and high-mobility transistors. Other devices still in the research phase that require heteroepitaxy include quantum dot and strained layer superlattice (SLS) lasers and detectors, and single-electron transistors.

Lastly, integrated circuits represent another area where heteroepitaxy can enable new capabilities. A single material cannot satisfy all the requirements for high-density digital circuits, sensors, modulators, and optoelectronic devices operating over a wide range of frequencies and wavelengths. Heteroepitaxy can be used to integrate the applications of several niche materials onto a single chip, leading to a substantial reduction in cost, size, and weight.

One of the most studied systems of heteroepitaxy is the Ge-Si system. Applications of Ge on Si (GoS) include the heterojunction bipolar transistor (HBT), and strained Si technology. The HBT is now used extensively in radio-frequency telecommunications and high-bandwidth instrumentation. Strained Si is created by epitaxial growth onto a Ge_xSi_{1-x} layer and is used to enhance mobility in complementary metal-oxide-semiconductor (CMOS) field-effect transistors.[2] In addition, the lattice constant of Ge closely matches that of III-V group materials such as GaAs and AlAs, as shown in Figure 1-1. Lattice mismatch is important in heteroepitaxy because it leads to the formation of defects in the material that degrade its electronic properties. This will be further discussed below. However, there are three important applications for integrating GaAs based materials onto Ge. The first application is multijunction (MJ) solar cells,[3-10] the second is monolithic integration of optoelectronics with Si CMOS technology,[11,12] and the third is high mobility CMOS electronics using nMOS III-V and pMOS Ge transistors[13-16].

First, MJ solar cells have achieved record efficiencies of over 40 %.[17] High efficiencies are achieved in these cells by using a series of III-V semiconductor materials that each absorbs a range of wavelengths in the solar spectrum. A schematic of an MJ solar cell is shown in Figure 1-2.

The MJ solar cells are primarily used in space power applications, but could also be useful for terrestrial applications if their cost can be reduced. Part of the high cost is due to the use of a Ge substrate on which the III-V active layers are deposited. A significant cost reduction can be achieved by using a cheaper Si substrate on which a thin film of Ge is grown. These 'virtual substrates' could replace the more expensive Ge

substrates if the GoS quality can match that of the Ge substrate. Silicon substrates also provide additional advantages over Ge for MJ solar cells. First, Si exists in abundance compared to Ge, which is produced as byproducts of zinc and coal mining.[18] Second, Si is mechanically stronger and less brittle than Ge, which is important for ease in processing

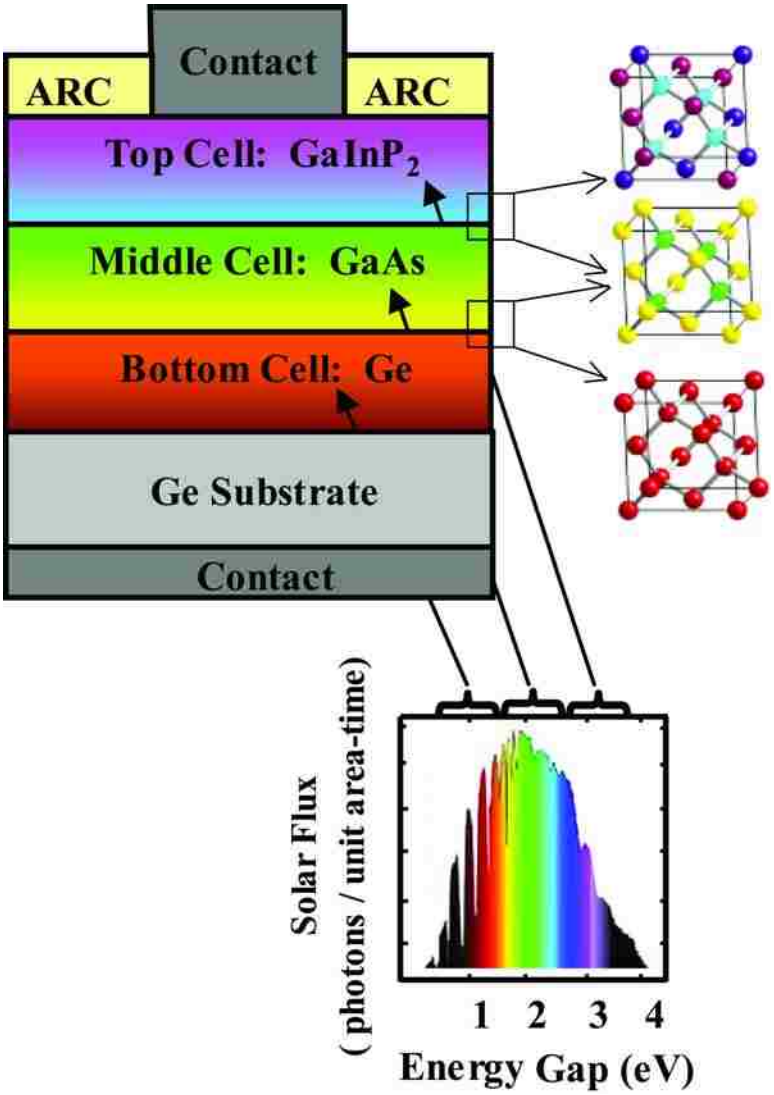


Figure 1-2. Schematic of a triple junction solar cell. The cell consists of a series of layers in order of largest to smallest bandgap from top to bottom. Each layer collects a range of the solar spectrum shown in the inset at the lower right. The III-V layers are closely lattice matched to one another and to the Ge substrate.

and obtaining higher yield. Third, Si is less dense than Ge, potentially reducing the overall weight of the solar array made for space applications. Virtual substrates can also be used to monolithically integrate optoelectronics with Si based CMOS technologies.

Optoelectronics such as semiconductor lasers and detectors can be used for optical interconnects for chip-to-chip communication with a large bandwidth. Having optoelectronics monolithically integrated with Si CMOS can achieve lower cost, lighter weight, and greater speed than having separate chips performing separate functions and interconnected with Cu wires.[19] Again, GoS can serve as a virtual substrate for integrating optoelectronics with Si electronics, taking advantage of the functionality of different semiconductors simultaneously on the same chip. An example of a III-V based optical device integrated onto a virtual substrate is shown in Figure 1-3. Lastly, III-V and Ge heteroepitaxy can both greatly extend the computing speed of CMOS electronics.

Silicon based CMOS electronics continue to approach fundamental physical limitations in shrinking the transistors to achieve faster computing speeds.[20,21] However, Ge has one of the highest hole mobilities of any semiconductor at 1900 $cm^2\ V^{-1}\text{-}s^{-1}$ compared to 480 $cm^2\ V^{-1}\text{-}s^{-1}$ for Si. Likewise, GaAs has an electron mobility of 8500 compared to 1350 $cm^2\ V^{-1}\text{-}s^{-1}$ for Si. Therefore, an ideal CMOS design will utilize Ge pMOS and GaAs nMOS transistors to achieve much greater switching speeds, as depicted in Figure 1-4.

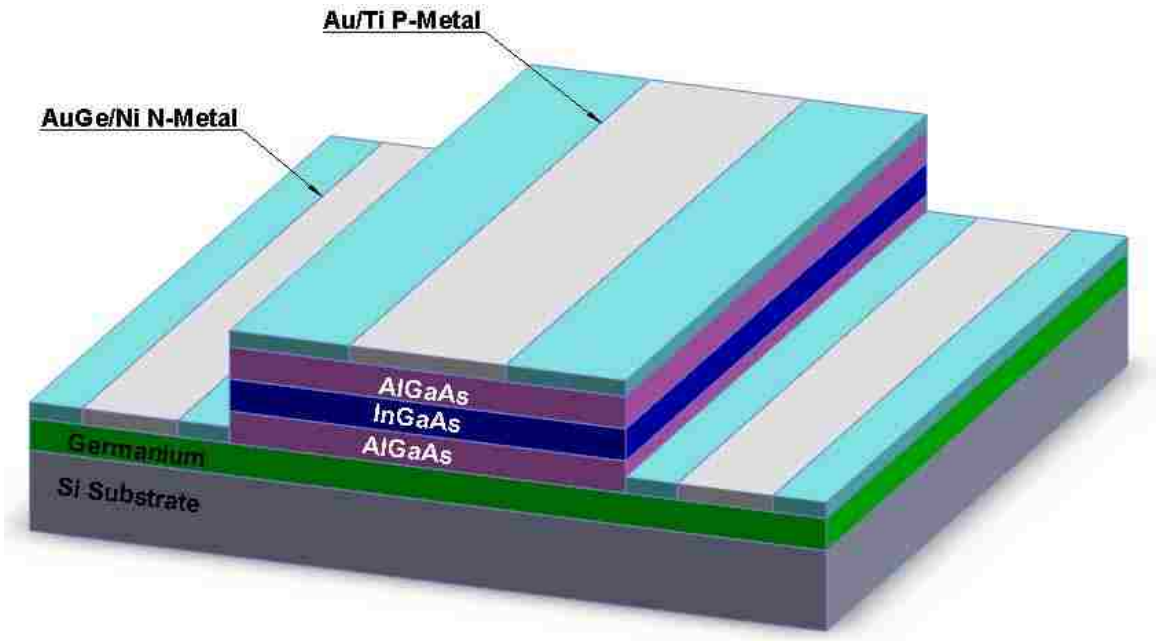


Figure 1-3. Optical interconnect architecture showing possibility of monolithic integration with Si based circuits.

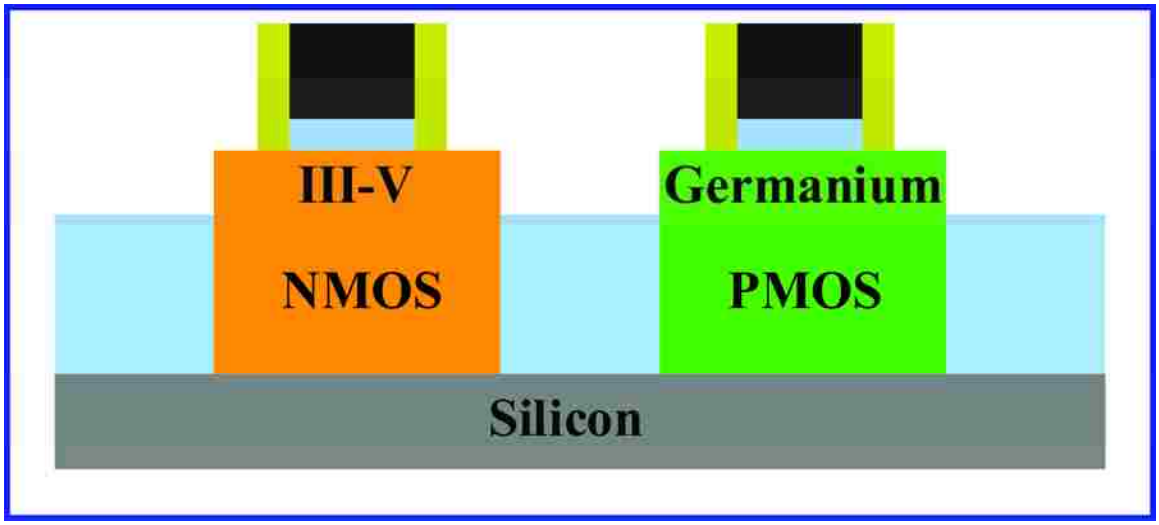


Figure 1-4. High mobility complementary metal-oxide-semiconductor electronics utilizing a Ge based p-metal oxide semiconductor and III-V n-metal oxide semiconductor structure.

1.2 Barriers to Integration of High-Quality Ge on Si

The viability of GoS virtual substrates for device applications has not yet been commercially demonstrated because of the difficulty in achieving Ge of sufficient quality. This is primarily due to the 4.2 % lattice mismatch and 116% thermal mismatch between Ge and Si. The former can result in threading dislocation densities (TDD) on the order of 10^9-10^{10} cm^{-2}, while the latter can lead to microcracks in Ge films that exceed about 5 microns in thickness as the sample cools from a growth temperature of 853 K. Both theoretical and experimental evidence suggests that the TDD in the Ge films must be less than 10^6 cm^{-2} to achieve a minority carrier lifetime in III-V films on GoS that is comparable to that of lattice-matched III-V growth on Ge and GaAs substrates.[22,23]

An additional difficulty in achieving high-quality heteroepitaxy of a divalent material such as GaAs on a monovalent material like Ge or Si is the formation of antiphase boundaries (APBs). An example of this defect is shown in Figure 1-5, and involves the formation of Ga-Ga or As-As bonds along the APB.

The APBs can form in at least two different ways. First, an APB occurs if an incomplete initial monolayer of either Ga or As forms on the surface of the monovalent material. The GaAs growth is usually initiated in an As overpressure to create a monolayer of As on the monovalent semiconductor surface. The vapor pressure of As is much greater than that of Ga, such that excess As readily desorbs from an As monolayer. In contrast, Ga can aggregate on the surface and form droplets. Second, APBs form at single height atomic steps that normally exist on single crystalline substrates due to a small unintentional angle of miscut relative to the crystal orientation. The suppression of

APBs is generally found to occur when using a substrate intentionally offcut by greater than 4 degrees toward a [110] direction.

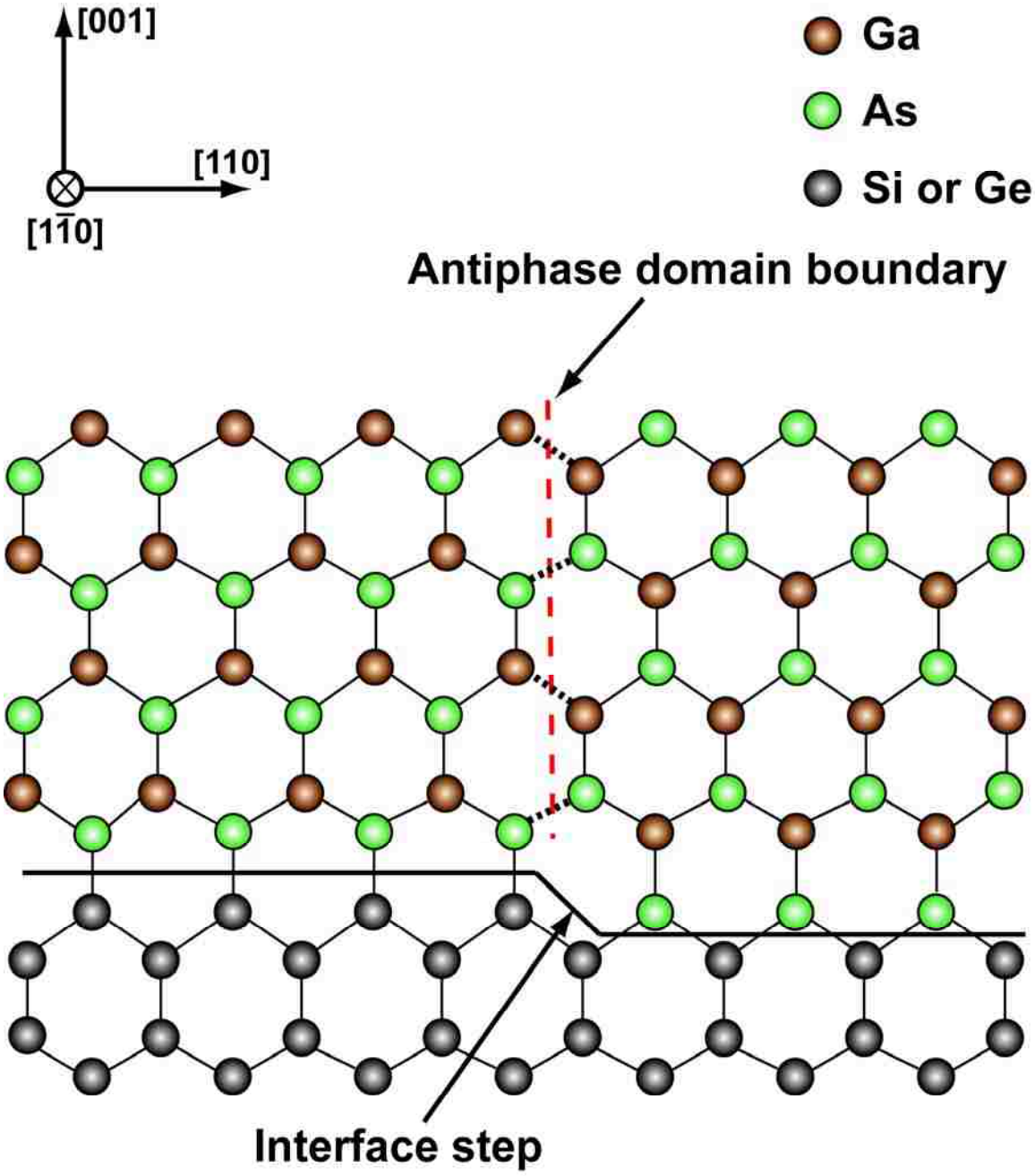


Figure 1-5. Antiphase domain boundary that occurs from the epitaxial growth of a zinc-blende structure on diamond cubic materials such as Ge or Si in the presence of single height atomic steps.

The explanation for the suppression of APBs using offcut substrates is that the large offcut angle favors the reconstruction of the surface into atomic steps of double height, as shown in Figure 1-6.[24] Complete monolayer nucleation on the double height reconstructed surface prevents the formation of APBs. While the formation of APBs can be suppressed by growing on offcut substrates, the problems associated with lattice and thermal expansion coefficient mismatch have not yet been resolved.

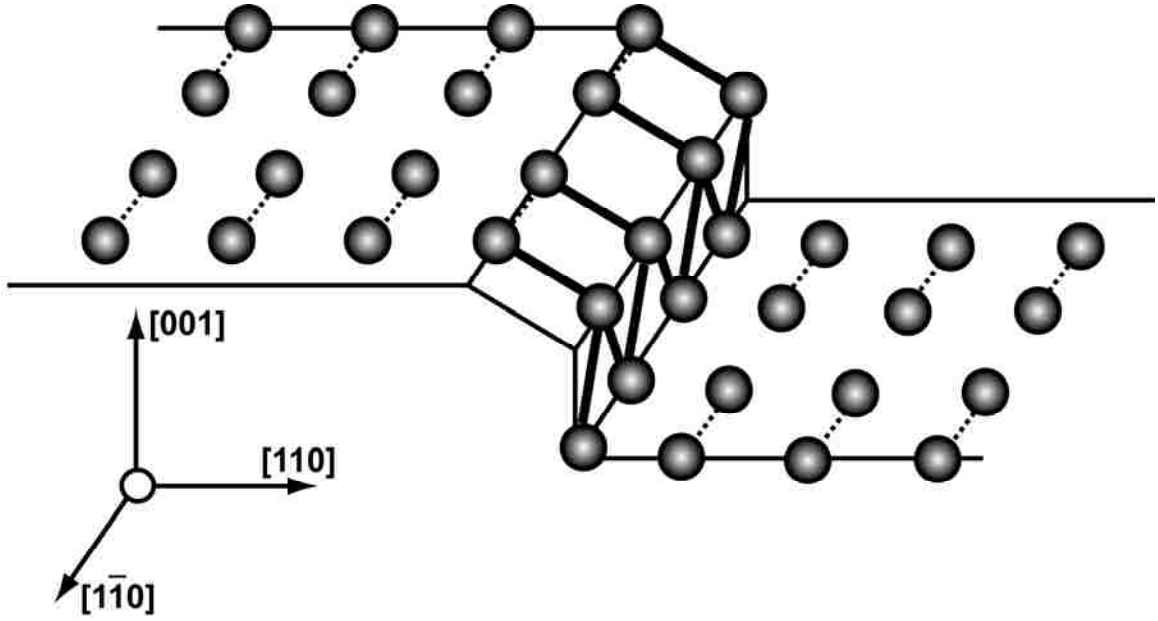


Figure 1-6. Rendition of the double height step reconstruction that occurs on substrates offcut by several degrees toward the [110] direction. The morphology suppresses the formation of anti-site defects occurring in zinc-blende epitaxy on diamond cubic materials.

1.3 Dislocation Nucleation Models

In heteroepitaxy, the lattice constant of the film is generally different from that of the substrate on which it is grown. The adoption of the substrate lattice constant by the epitaxial film leads to stress in the film and the eventual nucleation of dislocations to

relieve the stress. However, there is an energy barrier associated with the nucleation of dislocations. The energy barrier of the dislocations allows the film to adopt the lattice constant of the substrate in the early stages of growth when the film thickness is small. This stage of film growth is termed pseudomorphic growth. The lattice mismatch strain is defined as:

$$f = \frac{a_s - a_f}{a_s} \tag{1-1}$$

where a_s and a_f are the substrate and film lattice constants, respectively. The in-plane stress required to generate the in-plane strain $\varepsilon_{||}$, is based on Hooke's Law and is equal to

$$\sigma_{||} = 2G\frac{(1+\nu)}{(1-\nu)}\varepsilon_{||} = 2G\frac{(1+\nu)}{(1-\nu)}f \tag{1-2}$$

where G is the shear modulus and ν is the Poisson ratio. The in-plane stress leads to a tetragonal distortion of the lattice in the direction perpendicular to the growth direction. Figure 1-7 (a) shows an example of pseudomorphic growth for Ge on Si. The energy associated with lattice mismatch as a function of film thickness h is given by

$$E_{||} = 2G\frac{(1+\nu)}{(1-\nu)}hf^2 \tag{1-3}$$

Equation (1-3) shows that the energy of the system increases linearly with film thickness. However, there is a critical value of the film thickness at which the system can lower its total energy by nucleating stress-relieving dislocations, as shown in Figure 1-7 (b).

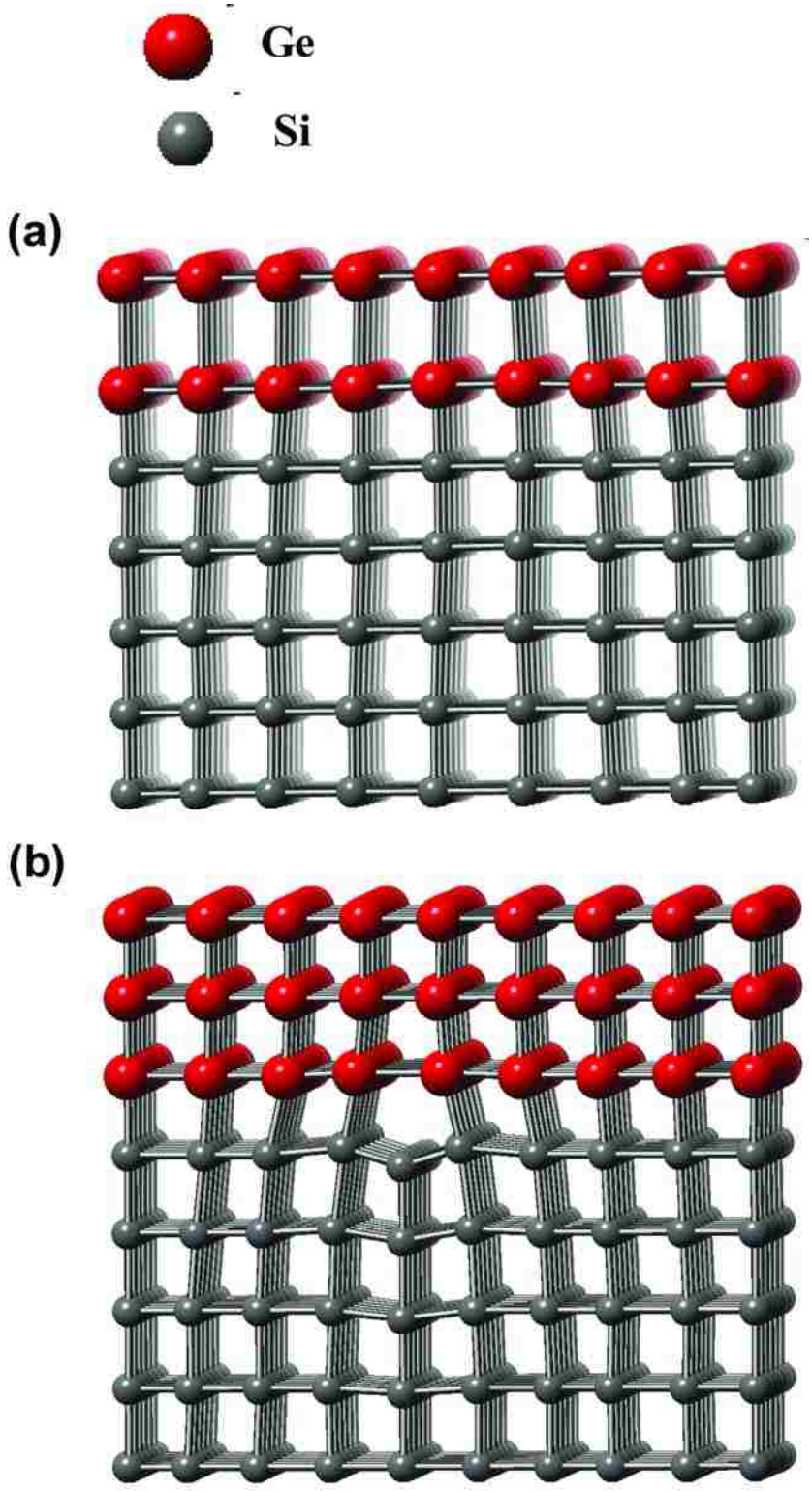


Figure 1-7. Image (a) shows the pseudomorphic growth of Ge on Si. Image 1-7(b) shows the nucleation of a misfit dislocation to relieve the stress at larger Ge thickness.

Matthews[25] derived the critical layer thickness based on total energy considerations. First, the energy associated with a square array of misfit dislocations with average separation S is

$$E_d = \frac{1}{S}\frac{Gb^2(1-\nu\cos^2\alpha)[\ln(R/b)+1]}{2\pi(1-\nu)} \tag{1-4}$$

where α is the angle between the Burgers vector and the line vector for the dislocations, b is the length of the Burgers vector, and R is the cutoff radius for the determination of the dislocation line energy. Matthews assumed R equal to the film thickness, h. Mismatch strain is relieved as dislocations begin to nucleate. The residual strain of the system with dislocations becomes

$$f - \varepsilon_{\|} = \frac{b\cos\alpha\cos\phi}{S} \tag{1-5}$$

where ϕ is the angle between the interface and the normal to the slip plane. The total energy of the system is equal to $E_{||} + E_d$. There will be a minimum total energy at equilibrium found from the condition

$$\frac{\partial(E_{\|} + E_d)}{\partial\varepsilon_{\|}} = 0 \tag{1-6}$$

The solution of Equation (1-6) gives the in-plane strain for energy minimization, or the equilibrium strain

$$\varepsilon_{\|}(eq) = \frac{f}{|f|}\frac{b(1-\nu\cos^2\alpha)[\ln(h/b)+1]}{8\pi h(1+\nu)\cos\lambda} \qquad (1\text{-}7)$$

The critical layer thickness for the onset of dislocation nucleation is the thickness for which $\varepsilon_{\|}(\text{eq}) = f$. Solving,

$$h_c = \frac{b(1-\nu\cos^2\alpha)[\ln(h_c/b)+1]}{8\pi|f|(1+\nu)\cos\lambda} \qquad (1\text{-}8)$$

van der Merwe[26,27] developed an alternative expression for the critical layer thickness by equating the strain energy in a pseudomorphic film to the interfacial energy of a network of misfit dislocations. The areal energy density of the misfit dislocation network was estimated to be

$$E_d \approx 9.5 f\left(\frac{Gb}{4\pi^2}\right) \qquad 1\text{-}9)$$

By setting Equations (1-3) and (1-9) equal and solving for the critical layer thickness, van der Merwe found

$$h_c = \left(\frac{1}{8\pi^2}\right)\left(\frac{1-\nu}{1+\nu}\right)\frac{a_s}{|f|} \qquad (1\text{-}10)$$

where a_s is the lattice constant of the substrate. The predictions for the critical thickness of Matthew's and van der Merwe's models are similar. Both models predict a critical thickness value of about 3 nm for GoS.

Some experimentally observed values of critical thickness for GoS are about ten times greater than 3 nm.

People and Bean[27] derived an alternative expression for the critical thickness that is in much better agreement with their experimentally observed values. Staring with Equation (1-3), People and Bean considered a dense network of screw dislocations at the interface with a spacing of

$$S = 2\sqrt{2}a_s \tag{1-11}$$

The areal energy density of this misfit dislocation array is

$$E_d \approx \frac{Gb^2}{8\pi\sqrt{2}a_s} \tag{1-12}$$

Setting Equations (1-3) and (1-10) equal to each other and solving for the thickness, they estimated the critical thickness to be

$$h_c = \left(\frac{1+\nu}{1-\nu}\right)\left(\frac{1}{16\pi\sqrt{2}}\right)\left(\frac{b^2}{a_f}\right)\left[\left(\frac{1}{f^2}\right)\ln\left(\frac{h_c}{b}\right)\right] \tag{1-13}$$

People and Bean used this expression to calculate the critical layer thickness for GoS as a function of composition in $Si_{1-x}Ge_x/Si$ (001), for which the lattice mismatch strain is $f = -0.04x$. These results are shown in Figure 1-8, along with the calculations of Matthews and van der Merwe. Also shown for comparison are experimental data for the $Si_{1-x}Ge_x/Si$ (001) heteroepitaxial system measured by Bean *et al.*[28], and Houghton[29]. The model by Matthews appears to be in better agreement with the data of Houghton, whereas the data from Bean is in better agreement with the model of People and Bean. The discrepancy in

the data is likely due to the finite resolution of the measurements made for the onset of dislocation nucleation. However, all the models predict that the critical thickness for GoS is only a few nanometers in thickness. This means that dislocations will be unavoidable for planar films of practical thickness. This has led to methods to reduce or manage dislocations in the film to acceptable levels.

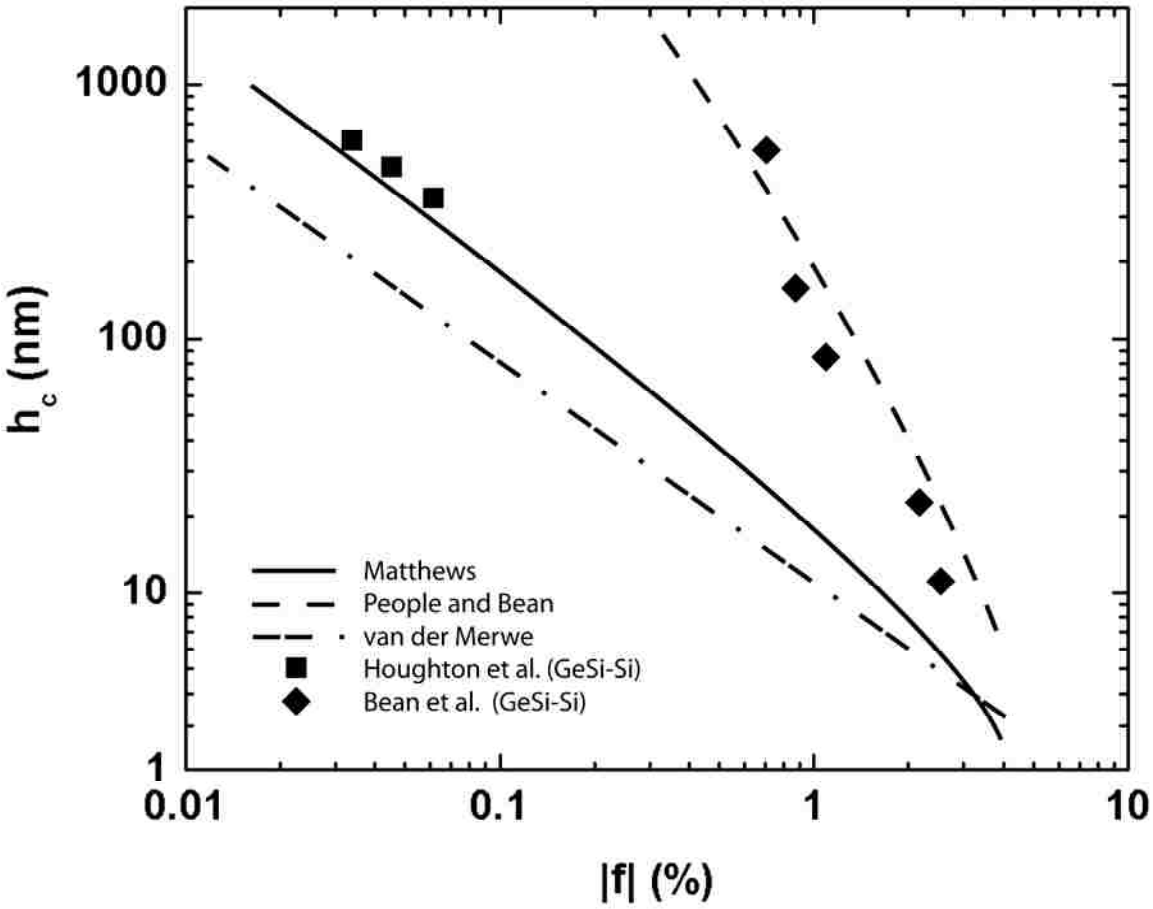


Figure 1-8. Comparison of different models for dislocation nucleation in heteroepitaxy. The data of Bean *et al*. appear to support the model of People and Bean, whereas the data of Houghton *et al*. are in better agreement with the model of Matthews.

1.4 Previous Approaches to Reduce Threading Dislocations in Heteroepitaxy

Graded buffer layers of $Si_{1-x}Ge_x$/Si, where *x* is slowly increased up to a value of 1, have been successful in reducing the TDD in the Ge films.[22,30-32] Slowly increasing the strain with increasing film thickness allows dislocations to nucleate more slowly and they are able to glide longer distances without becoming entangled with other dislocations. The glide of threading dislocations (TDs) leads to the formation of stress relieving misfit dislocation segments as shown in Figure 1-9.

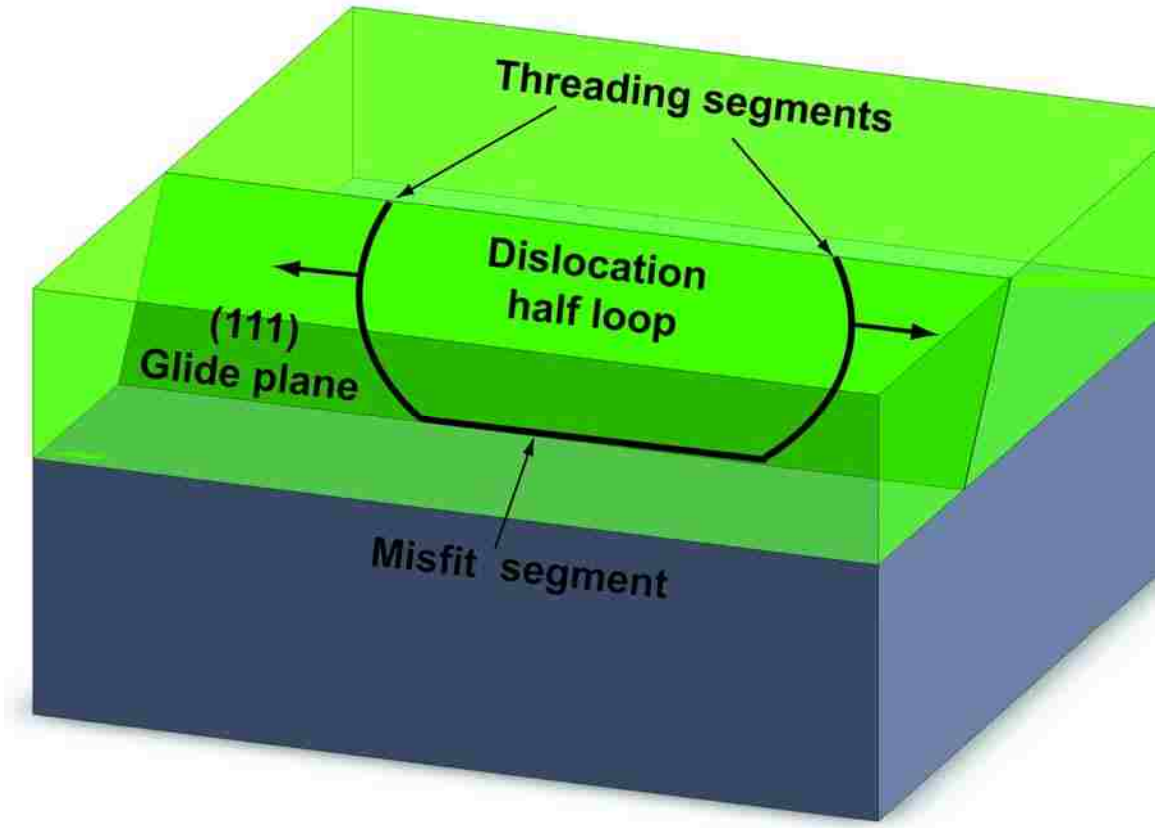


Figure 1-9. Glide of a threading dislocation to a boundary at the film edge leaving behind a misfit dislocation segment at the interface.

There are at least two major drawbacks to graded buffer layers. The first is that the stress fields from the misfit dislocation segments create surface undulations known as crosshatch that inhibit dislocation glide in the films. The pinning of dislocations at surface crosshatch leads to dislocation pileups and subsequent nucleation of additional dislocations.[33] Currie *et al*.[31] successfully applied chemical-mechanical polishing (CMP) to remove the surface undulations and achieved a TDD in the Ge films of 10^6 cm^{-2}. However, the second drawback to graded buffer films is the large film thickness that is required to achieve low TDD. The thick films exhibit cracking due to the mismatch in thermal expansion coefficient with the Si substrate when cooled from growth to room temperature. An alternative approach to reduce the TDD in heteroepitaxy is the use of a SLS.[34-39]

The stain fields associated with a pseudomorphically grown SLS will overlap with the strain fields associated with TDs. Depending on the relative signs of the strain fields, the dislocation may either be attracted to or repelled by the SLS. A compressive strain field emanating from the SLS will repel a compressive strain field associated with a TD. Oppositely, a tensile strain field emanating from the SLS will attract a TD associated with a compressive strain field. Figure 1-10 shows an example of a threading dislocation being bent into the (001) growth plane due to the interaction with a strained $Al_{0.3}Ga_{0.7}As$ layer on a GaAs film.

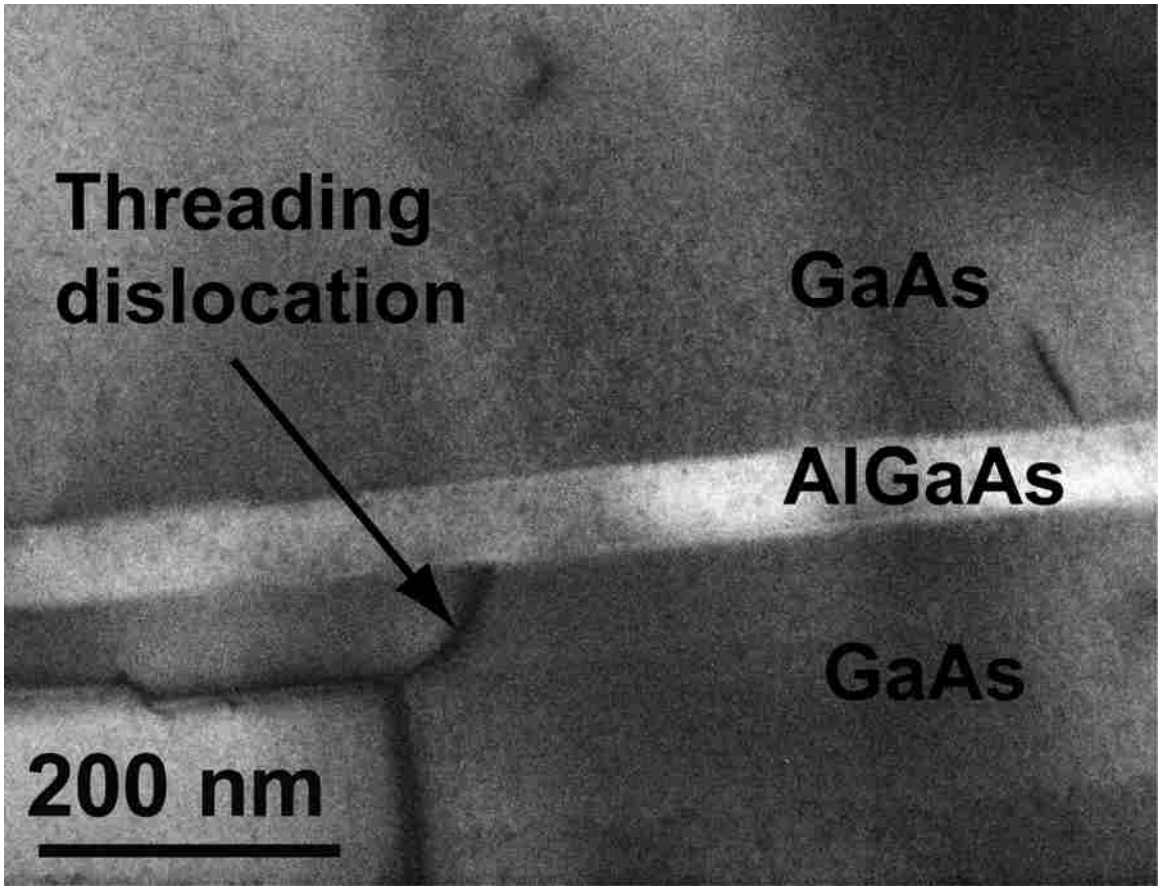


Figure 1-10. The principal of strained layer defect filtering is illustrated in the transmission electron microscope image of an $Al_{0.3}Ga_{0.7}As$-GaAs structure. The stress field of the $Al_{0.3}Ga_{0.7}As$ layer repels the stress field associated with the threading dislocation and bends it into the (001) growth plane.

However, in general, SLSs are not successful in greatly reducing the TDD in heteroepitaxy by much more than a factor of two or three. Another technique that has successfully reduced the TDD in heteroepitaxy is cyclical annealing.

Thermal cyclical annealing is method that employs a series of annealing cycles to promote glide and annihilation of TDs in the film. The TDs experience a thermally induced stress occurring from differences in thermal expansion coefficient between film and substrate, and this stress leads to glide of the TDs. The TDs in highly mismatched systems with large numbers of TDs often become entangled with one another, however,

inhibiting their glide motion. The result of thermal cyclical annealing is that the TDD in the film is only lowered by one or two orders of magnitude. Cyclical annealing also has the added drawback of requiring high temperatures that can cause significant intermixing between the film and substrate.[40-42] Another technique employed to lower the TDD in heteroepitaxy is the use of finite growth areas.

Finite growth areas are created on the substrate using a combination of lithography and etching to create raised mesas surrounded by amorphous material such as SiO_2. Heteroepitaxial growth then selectively takes place on top of the mesas. The finite lateral extent of the mesas allows TDs to glide short distances before reaching the edge of the mesa. The glide of a TD leaves behind a misfit dislocation at the interface, as depicted earlier in Figure 1-9. The effect of small growth areas is that fewer TDs become entangled with one another before creating stress-relieving misfit segments. Finite lateral growth has successfully demonstrated TDDs of 10^4 to10^5 cm^{-2} in GoS.[40,43,44] This method, while capable of achieving low TDD, has the considerable drawback of having only small areas on the substrate suitable for device fabrication. A related method called aspect ratio trapping has also produced small growth areas of high-quality heterepitaxy.[45-52]

Aspect ratio trapping involves the creation of narrow trenches or windows in a thick amorphous material such as SiO_2. The substrate is revealed at the bottom of the windows, and selective growth takes place within the openings. The finite growth area within the openings allows TDs to glide short distances before reaching the edge of the opening. In addition, the steep walls of the SiO_2 block any TDs not able to glide to the

edge of the openings. An example of aspect ratio trapping within trenches is pictured in Figure 1-11.

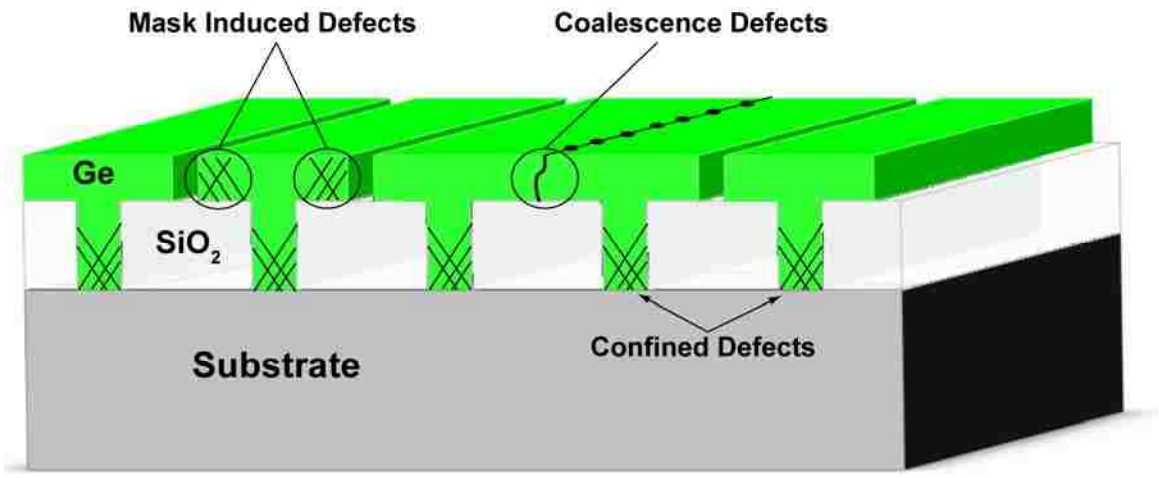


Figure 1-11. Heteroepitaxial growth selectively takes place within the patterned trenches and traps threading dislocations between the SiO_2 walls leading to high-quality material near the tops of the trenches. Coalescence of adjacent trenches, however, can lead to the nucleation of additional defects. In addition, the mask material itself may induce defects as the epitaxial film grows laterally over the mask regions.

If growth is allowed to continue above the pattern features, then eventually the growth fronts from adjacent openings will merge together. While coalescence of adjacent trenches leads to a continuous film for device fabrication, research shows that the regions where the growth fronts merge possess a large TDD.[48,52,53] Aspect ratio trapping has thus far produced similar TDD results to finite area growth, along with the same drawback of producing only small regions of device quality material. Finally, in an effort to overcome the limitations of the previous approaches, we use nanoheteroepitaxy as an approach to achieving low TDD heteroepitaxial films.[54-59]

Nanoheteroepitaxy utilizes the fact that additional strain relief mechanisms besides dislocation formation become dominant at very small length scales. For example,

Ge growth taking place on Si within windows in SiO_2 that are only a few nanometers in diameter can relax their strain by deforming outward over the SiO_2 layer, forming a mushroom shape. In addition, the lattice planes within the substrate also deform and absorb some of the mismatch strain. An example of this deformation is shown in Figure 1-12, based upon Finite Element Modeling (FEM) of the strain between a Ge island and Si substrate. [60-63]

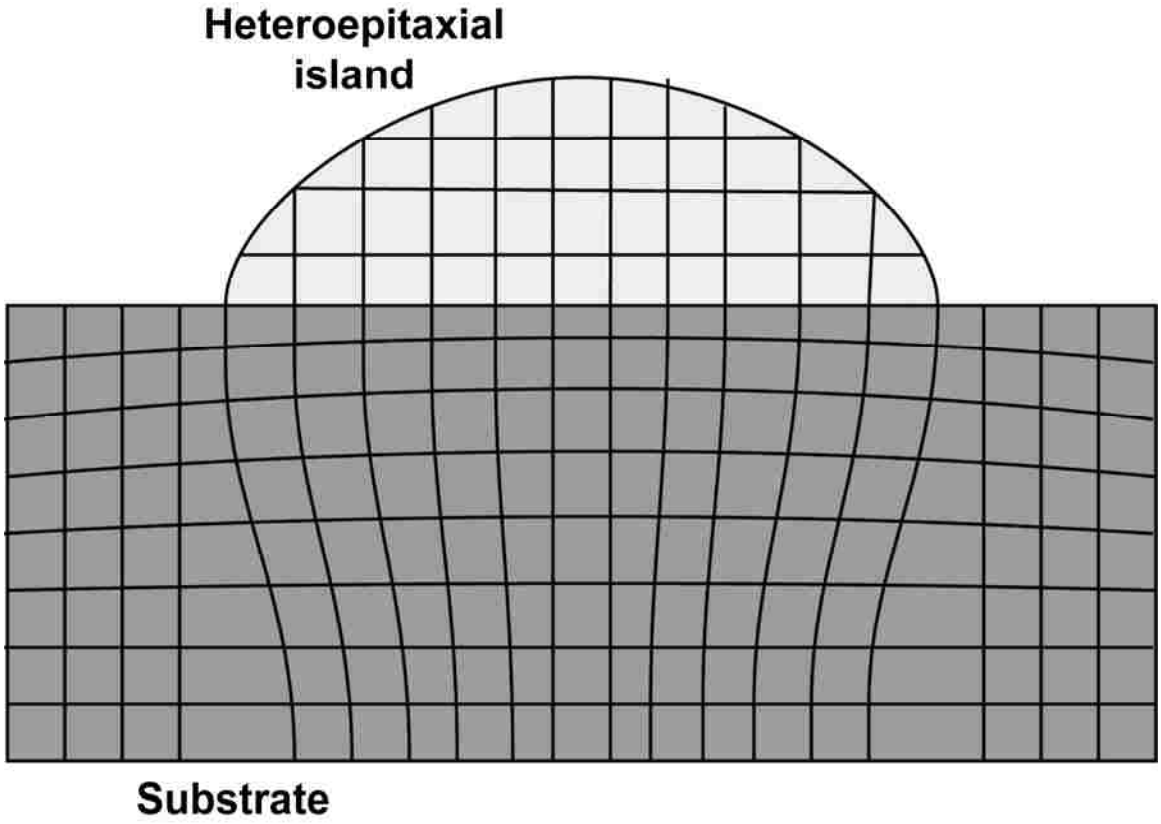


Figure 1-12. Finite element model showing the deformation of lattice planes occurring in the tensile strained heteroepitaxial island and within the compressively stained substrate.

Luryi and Suhir[64] were the first researchers to report a theory of lattice mismatch strain in nanoheteroepitaxy. Luryi and Suhir showed that in islands with lateral finite size the critical thickness depends on the island diameter. In their work, Luryi and Suhir calculated the critical layer thickness for mismatched heteroepitaxial islands that make

rigid contact with the substrate only on round seed pads having a diameter of 2*l*. They showed that in a GoS pseudomorphic structure, the strain in the heteroepitaxial layer decays exponentially with distance from the interface. Furthermore, the characteristic length h_e for the strain decay is on the order of the seed pad lateral dimension. Due to the exponential strain decay, the critical thickness increases as the island diameter is reduced. For a particular value of the lattice mismatch, there is an island diameter for which the critical thickness diverges to infinity, so that structures entirely free of misfit dislocations may be produced. The analysis of Luryi and Suhir[64] starts with an expression for the in-plane stress in the epitaxial deposit

$$\sigma_{\parallel} = f \frac{E}{1-\nu} \chi(y,z) \exp(-2\pi / 2l) \tag{1-14}$$

where E is Young's modulus, the z-axis is perpendicular to the substrate, and the y-axis lies in the plane of the interface, along the center of the seed pad, and

$$\chi(y,z) = \begin{cases} 1 - \dfrac{\cosh(ky)}{\cosh(kl)} & z \le h_e \\ 1 & z \ge h_e \end{cases} \tag{1-15}$$

where h_e is the effective range for the stress in the z-direction, to be determined below, and the interfacial compliance parameter k is given by

$$k = \left[\frac{3}{2}\left(\frac{1-\nu}{1+\nu}\right)\right]^{1/2}\frac{1}{h_e} \equiv \frac{\zeta}{h_e} \tag{1-16}$$

The strain energy density per unit volume is

$$\omega(y,z) = \frac{1-\nu}{E}\sigma_{\|}^{\ 2} \tag{1-17}$$

and is maximum at $y = 0$. The strain energy per unit area is found by integrating over the thickness of the epitaxial deposit and is maximum at y = 0, which is

$$E_s = \int_0^h \omega(0,z) = \frac{E}{1-\nu}\, f^{\,2} h_e^{\ 2} \tag{1-18}$$

The right-hand side of Equation (1-18) defines the characteristic thickness h_e, which is then given implicitly by

$$h_e = h\left\{\left[1-\sec h\left(\frac{\zeta l}{h_e}\right)\right]^2\left[1-\exp(-\pi h/l)\frac{l}{\pi h}\right]\right\} = h\left[\phi\left(\frac{l}{h}\right)\right]^2 \tag{1-19}$$

The right-hand side of this equation defines the reduction factor $\phi(l/h)$. For $l >> h$, $h_e \approx$ h, and for $l << h$,

$$h_e \approx \frac{1}{h}\left[1-\sec h(\zeta\pi)\right]^2 \tag{1-20}$$

The strain energy per unit area from Equation (1-18) is used in conjunction with an energy calculation for the critical thickness to find the critical layer thickness for an island of radius *l*. The result is

$$h_c^{\,l} = h_c[\phi(l / h_c^{\,l})\, f\,] \tag{1-21}$$

where Matthew's calculation for the critical thickness, Equation (1-8), is inserted into Equation 1-21 to yield

$$h_c^{\,l} = \frac{b(1-\nu\cos^2\alpha)[\ln(h_c^{\,l}/b)+1]}{8\pi\left|\phi(l / h_c^{\,l})\, f\right|(1+\nu)\cos\lambda} \tag{1-22}$$

The critical thickness is shown in Figure 1-13 as a function of lattice mismatch, with the island diameter $2l$ as a parameter. Matthew's calculation for the critical thickness, which assumed a planar film, corresponds to $2l \rightarrow \infty$.

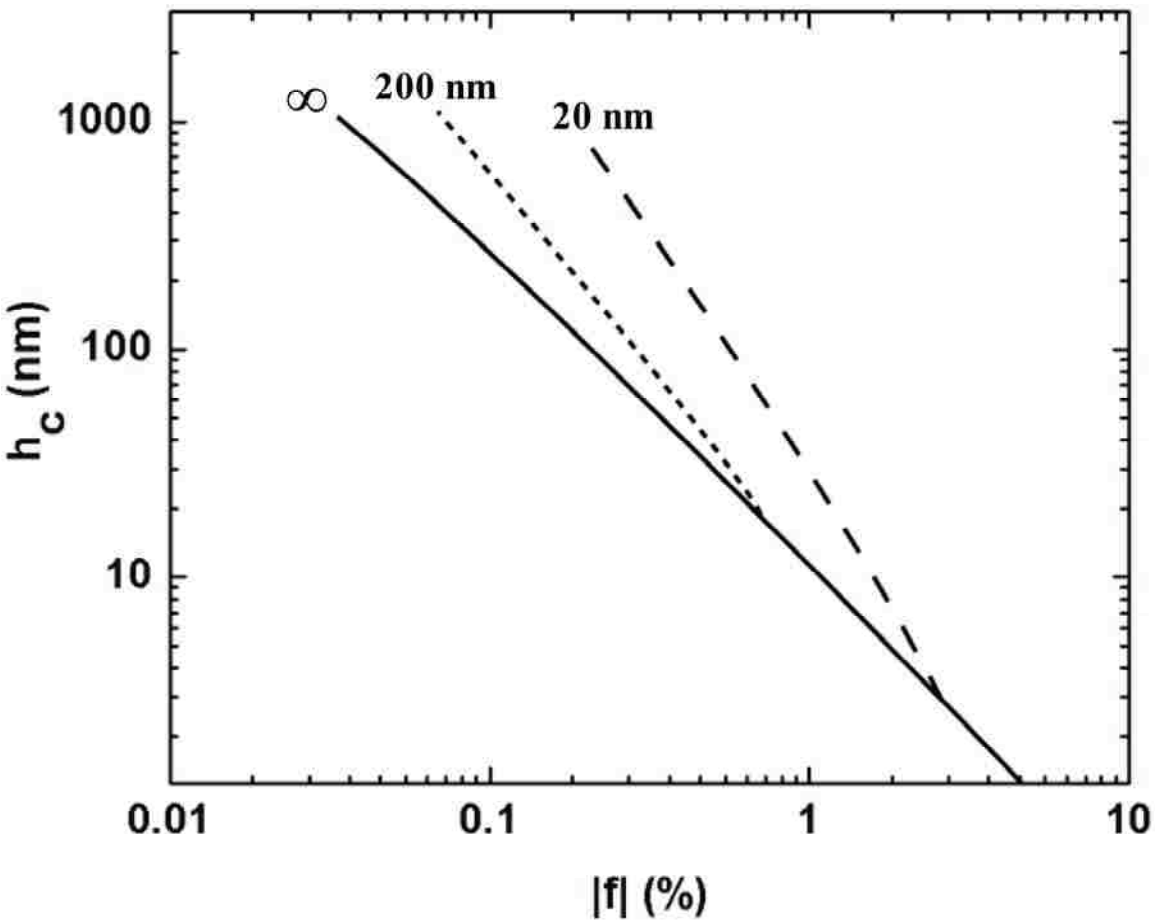


Figure 1-13. Critical thickness versus lattice mismatch based on Matthew's total energy calculation.[19] The solid line is Matthew's result for a planar film in contact with the substrate. The dotted and dashed lines represent an island of 200 and 20 nm, respectively, in contact with the substrate based on Luryi and Suhir's model.

For nanometer-scale islands, the critical thickness can be increased significantly. Additionally, for a given mismatch, there is a critical island diameter for which the critical thickness diverges to infinity. For GoS, this island diameter is approximately 10 nm, and is shown in Figure 1-14.

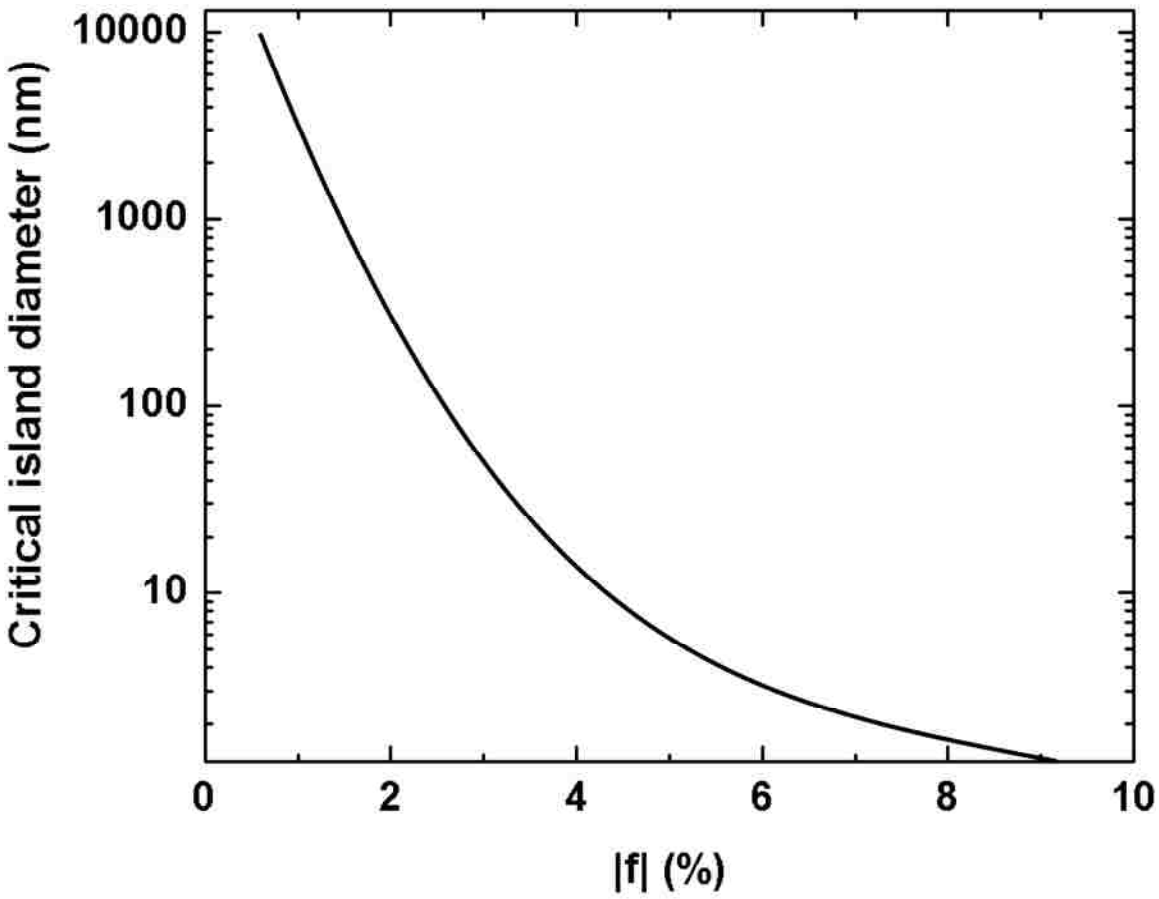


Figure 1-14. Critical island diameter versus lattice mismatch.[19] Island diameters below the solid line have infinite critical thickness for a given mismatch and will relax without the formation of dislocations.

Chapter 4 will describe our experiments in which the Ge seed pad diameters are less then 10 nm. Next, a review of molecular beam epitaxy is given, followed by a description of the deposition chamber used in this work.

CHAPTER 2 MOLECULAR BEAM EPITAXY

2.1 Theory of Evaporation

Most thin-film deposition techniques require a reduced pressure environment, and therefore, a discussion of vacuum science and vapor deposition is now given. The kinetic theory of gases provides the foundation for understanding the relationship between the atoms or molecules of a gas and measurable properties such as temperature and pressure. A basic assumption of the theory is that the gas molecules are in a continuous state of random motion, based on the temperature of the gas. The gas molecules collide both with the confining vessel walls and with one another. The number of collisions per unit area and time is dependent on the concentration or pressure of the gas. The following development of the kinetic theory of gases is based upon Ohring[65] and Smith.[66] The net result of the continual elastic collisions and exchange of kinetic energy is that a steady-state distribution of molecular velocities occurs given by the Maxwell-Boltzmann formula

$$f(\mathbf{v}) = \frac{1}{n}\frac{dn}{d\mathbf{v}} = \frac{4}{\sqrt{\pi}}\left|\frac{M}{2RT}\right|^{3/2}\mathbf{v}^2 \exp\left(-\frac{M\mathbf{v}^2}{2RT}\right) \qquad (2\text{-}1)$$

where v is velocity, n is the number of gas molecules present, M is the molecular weight of the gas, T is the temperature in Kelvin, and R is the gas constant on a per-mole basis. The root-mean-square (RMS) velocity of the gas molecules is given by

$$(\overline{\mathbf{v}}^2)^{1/2} = \left[\frac{\int_0^\infty \mathbf{v}^2 f(\mathbf{v}) d\mathbf{v}}{\int_0^\infty f(\mathbf{v}) d\mathbf{v}} \right]^{1/2} = \sqrt{\frac{3RT}{M}} \qquad (2\text{-}2)$$

This velocity depends only on the temperature and molecular weight of the gas. Implicit in the derivation of the Maxwell-Boltzmann distribution is the ideal gas law. In the ideal gas approximation, attractive and repulsive forces between the gas molecules are neglected, as well as the atomic volume that the gas molecules occupy. The ideal gas law is valid therefore, at high temperatures, and/or low pressures, as in vacuum deposition.

The pressure of a gas is related to the momentum transfer from the gas molecules to the vessel walls. The momentum of the gas molecules is related to their kinetic energy or temperature, thus

$$P = \frac{1}{3} \frac{nM}{N_A} \overline{\mathbf{v}}^2 = \frac{nRT}{N_A} \qquad (2\text{-}3)$$

where N_A is Avogadro's number. Equation (2-3) is an expression for the ideal gas law, with pressure depending on the number of gas molecules, *n*, and temperature. The gas molecules make continual collisions with the vessel walls and with each other. The mean distance that they travel between collisions is called the mean-free path, λ_{mfp}, and is an important quantity that depends on the pressure. It is given as

$$\lambda_{\mathbf{mfp}} = \frac{1}{\pi n d_c^{\,2}} \qquad (2\text{-}4)$$

where πd_c^2 is the collision cross section of a gas molecule. At pressures below 10^{-3} torr, λ_{mfp} is large enough that gas molecules effectively collide only with the vessel walls. One of the most important quantities in vacuum science and deposition is the gas impingement flux, Φ. It is equal to the frequency with which gas molecules impinge on a surface per unit area and time and is given by

$$\Phi = \int_0^{\infty} \mathbf{v}_x dn_x \tag{2-5}$$

Substituting Equation (2-2) into (2-5), the flux is equal to

$$\Phi = \frac{n}{(2\pi)^{1/2}} \left| \frac{M}{RT} \right|^{1/2} \int_0^{\infty} \mathbf{v}_x \exp\left(-\frac{Mvx2}{2RT} \right) d\mathbf{v}_x = n\sqrt{\frac{RT}{2\pi M}} \tag{2-6}$$

Substituting in the ideal gas law given by Equation (2-3) yields the useful formula

$$\Phi = 3.513 \times 10^{22} \frac{P}{\sqrt{MT}} \frac{\text{molecules}}{\text{cm}^2 - \text{s}} \tag{2-7}$$

where P is expressed in torr. A useful application of Equation (2-7) is the calculation of the time required to coat a surface with gas molecules. For the time to complete one monolayer coverage on a surface containing 10^{15} atoms cm^{-2}, the use of Equation (2-7) yields

$$\tau_c = \frac{10^{15}}{3.513 \times 10^{22}} \frac{(MT)^{1/2}}{P} = 2.85 \times 10^{-8} \frac{(MT)^{1/2}}{P} \text{sec} \qquad (2.8)$$

In air at atmospheric pressure and ambient temperature, a surface will acquire a monolayer of gas in 3.5 nanoseconds, assuming all impinging atoms stick to the surface. At a pressure of 10^{-10} torr, the surface will remain uncoated for 7.3 hours. These calculations demonstrate the importance of ultra-high vacuum background pressures when film purity is important.

2.2 Substrate-Source Geometry and Deposition Rate

Equation (2-7) gives the impingement rate of gas molecules on a surface, but this may not be equal to the deposition rate on the sample surface. There is a finite probability that molecules that impinge on the surface can be reflected back into the vacuum, and not stick to the surface. Equation (2-7) can be modified by multiplying by a sticking coefficient, *S*, which is the probability that an impinging molecule will stick to the surface. The sticking probability depends heavily on the kinetic energy of the impinging gas molecules and the substrate surface temperature. In addition, the deposition rate on the sample surface also depends on the orientation of the surface relative to the evaporation source. Gas molecules have large values of λ_{mfp} at low pressures, so that gas molecules being evaporated from a surface source will travel along straight trajectories until reaching the sample surface. Figure 2-1 shows the source-substrate geometry as it affects the deposition rate.

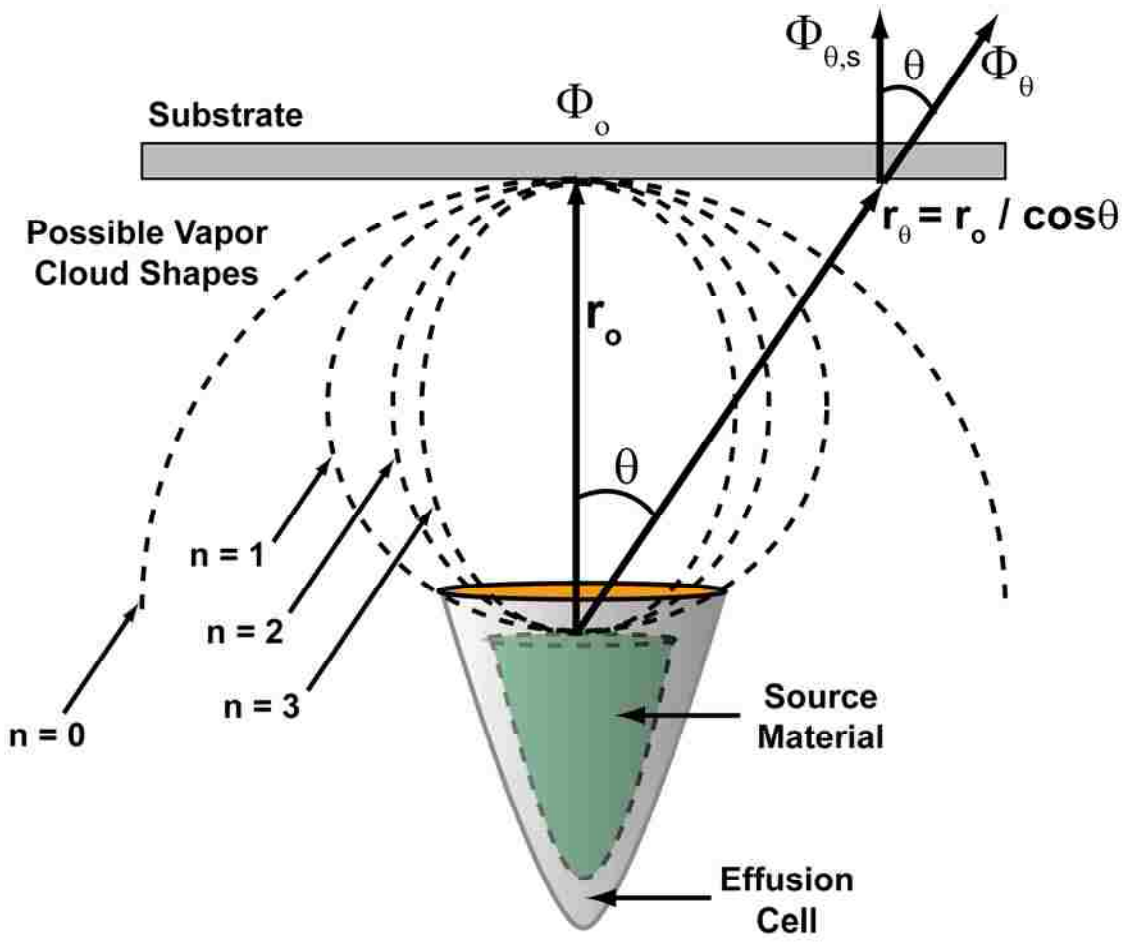


Figure 2-1. Substrate-source geometry affecting the deposition rate, after Smith.[66] The flux emanating from the effusion cell follows a cosine distribution. The cosine term is raised to the power *n*, reflecting the degree of collimation of the effusion flux.

The evaporation source is the effusion cell located at a distance r_o from the sample surface. Equation (2-7) describes the evaporation rate from the effusion cell at the sample surface based on the vapor pressure of the material being evaporated within the cell. The deposition rate $R_{\theta,s}$ on the sample surface depends on the distance from the source, r_o and the angle of the sample relative to the source, θ, and is given by

$$R_{\theta,s} = \frac{\Phi_o (n+4)\cos^{n+3}\theta}{\pi r^2{}_o} \qquad (2\text{-}9)$$

where n is an integer that describes the lobe shape of the vapor cloud distribution emerging from the effusion cell. The vapor cloud is lobe shaped and partially collimated because the evaporation source material is at some distance below the effusion cell opening. The deposition rate is maximal at the point on the sample perpendicular to the effusion source, and decreases at larger values of θ. A factor of $\cos^2\theta$ is introduced based on the additional distance r_θ from source to substrate at larger values of θ. An additional factor of $\cos\theta$ is introduced because the substrate surface is not perpendicular to the vapor cloud at $\theta > 0$. These geometric factors account for the $\cos^3\theta$ term in Equation (2-9), whereas the deviation of the vapor cloud shape from spherical to lobe-shaped introduces the factor $\cos^n\theta$. As n increases, the vapor cloud is more collimated and the deposition rate decreases more rapidly at increasing values of θ. The actual deposition rate on the substrate must generally be measured experimentally at different vapor pressures of the source material, and Equation (2-9) is then fit to the data to determine the parameter n.

2.3 Molecular Beam Epitaxy Experimental Setup

Figure 2-2 shows a schematic of the molecular beam epitaxy (MBE) deposition chamber used in this work. The deposition chamber is connected to an entrance load lock that is pumped with a turbomolecular pump operating at 240 L/s. The load lock is vented with pure N_2 gas and the pressure is monitored with a thermocouple (TC) and cold-cathode gauge for measuring low and high vacuum, respectively. The deposition chamber is pumped with a 500 L/s turbo pump and a 400L/s ion pump that produce a

base pressure of 5×10^{10} Torr, which is measured with an ion gauge. The effusion cell has a dual-filament with a double-walled pyrolytic

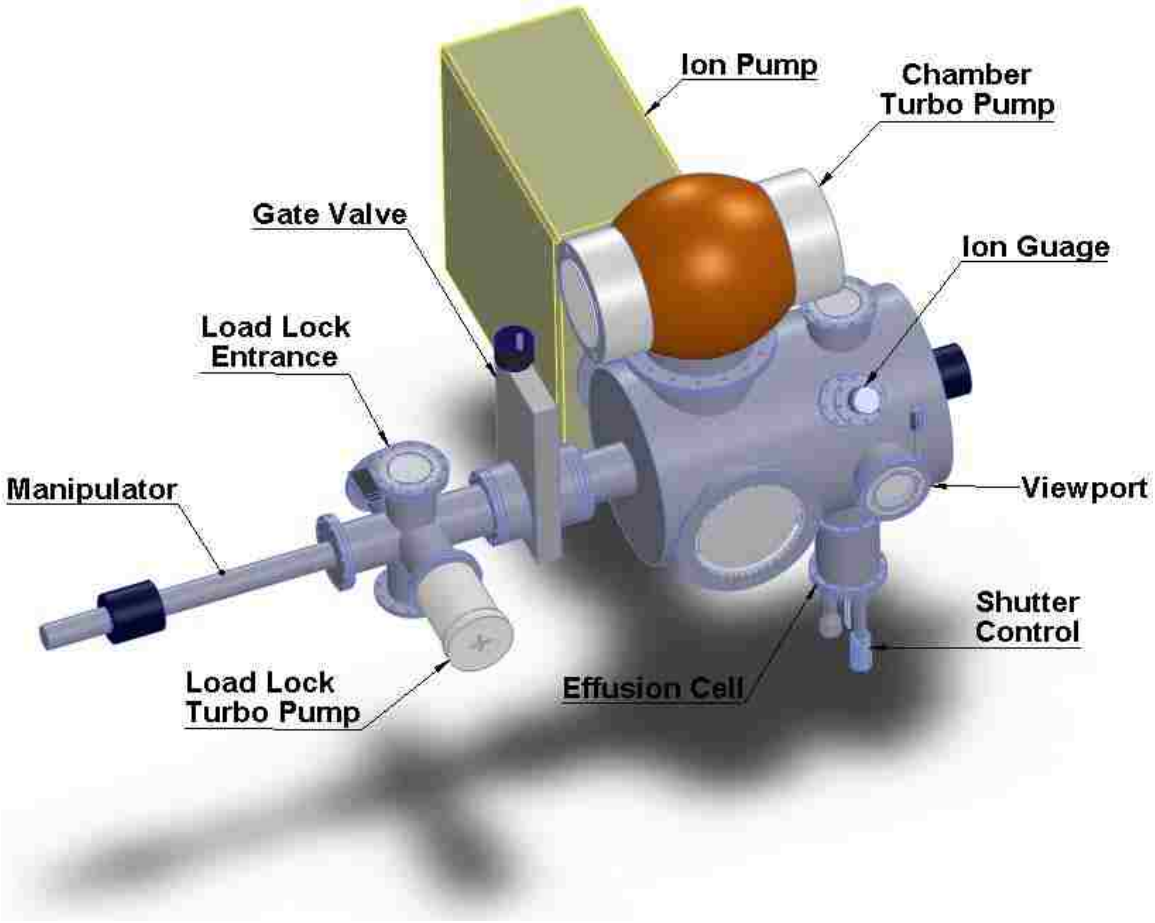


Figure 2-2. Schematic of the molecular beam epitaxy vacuum chamber used in this work with major components labeled.

boron nitride (PBN) crucible filled with Ge source material of 99.9999 % purity. The effusion cell temperature is measured using two TCs placed near the outside of the PBN crucible. The deposition rate is measured at a point on the sample that is perpendicular to the source at several substrate temperatures, where $\theta = 0$.

The measurement of the deposition rate is done by placing a clean 2-inch diameter Si substrate into the deposition chamber and depositing a thick Ge layer with the

Si substrate held at room temperature. The thickness is then measured using cross-sectional scanning electron microscopy (SEM). The deposition rate is then given by the Ge layer thickness divided by the time of deposition. The measurement is accurate to within about 1 % and is limited by the resolution of the SEM. Equation (2-7), (2-9), and the TC readings of the effusion cell are used to calculate the deposition rate based on published values[67] of Ge vapor pressure versus temperature. The deviation of the measured and calculated deposition rates allows calculation of the parameter *n*. The distance between the Ge source material and the substrate surface normal is measured at 16.7 cm, so that θ is 8.75º at the edge of the 2-inch Si substrate. The calculated value of *n* is 11, leading to a 15 % decrease in the deposition rate at the substrate edge as compared to the center. Appendix A shows a plot of the measured and calculated deposition rate using Equation (2-9) based on the vapor pressure of the Ge source material for a given TC reading and the measured parameters r_o and *n*. The solid line corresponds to the center of the sample where t = 0; the dashed line shows the deposition rate at the edge of the 2-inch wafer. The data points show the measured deposition rates at both the center (squares) and edge of the wafer (circles). The close agreement between Equation (2-9) and the measured values of deposition rate allows good predictive growth rates at other effusion cell temperatures. Appendix B shows detailed drawings and dimensions of the MBE chamber used in this work. Next, a description is given of the substrate heater and sample transfer system.

Figure 2-3 shows a schematic of the substrate heater transferable assembly. The substrate heater is a 50 mm × 50 mm plate consisting of a pyrolytic graphite filament encased in PBN and made by GE Advanced Materials. The substrate is mounted directly

on the heater using clips made of tungsten. The substrate heater power-leads are connected to banana plugs that are compatible in ultra-high vacuum. The substrate heater assembly is transferred to/from the deposition chamber from the load lock using a magnetically coupled manipulator. The deposition chamber is fitted with a receiver mounting that guides the heater assembly banana plugs into the female plug receptacles. These receptacles are connected, in turn, to a power feed-through vacuum fitting. The heater assembly has additional banana plug fittings to add a TC to the heater.

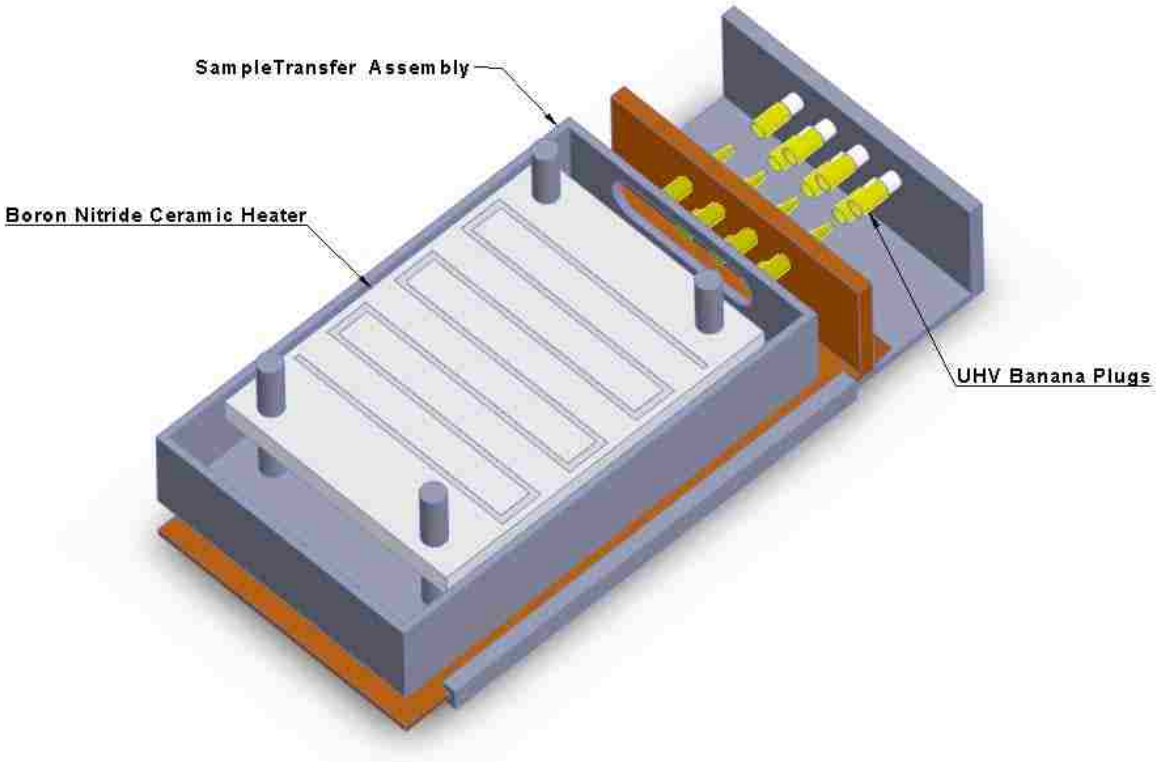


Figure 2-3. Schematic of the substrate heater assembly utilizing ultra-high vacuum compatible banana plugs for electrical connections.

The substrate heater calibration is done using a K-type TC mounted in the center of the heater. The heater power supply is manually operated to produce an output percent ranging from 0 to 35 % power. The temperature is measured from ambient to 1000 ºC using the TC. Additional measurements are also made using a pyrometer for temperatures from 700 to 1000 ºC. Appendix C shows a calibration plot of the pyrometer and TC readings versus percentage output on the power supply. The pyrometer and TC readings generally agree with each other within ± 8 ºC. Next, a brief review is given of the different characterization techniques used in this work.

CHAPTER 3 FUNDAMENTALS OF CHARACTERIZATION TECHNIQUES

3.1 X-ray Diffraction

X-ray diffraction is a non-destructive technique that is used to estimate the crystalline quality of thin films, as well as their composition and strain state. The method utilizes coherent x-rays that interact elastically with a specimen. Coherent x-rays are emitted from the sample at characteristic angles called Bragg angles. The Bragg angle is directly related to the lattice spacing of the material through Bragg's equation

$$n\lambda = 2d\sin\theta \tag{3-1}$$

where n is an integer, usually taken as 1, d is the spacing between lattice planes (the planes are denoted by their Miller indices), and θ is the Bragg angle. The x-ray source uses Cu K_α radiation of wavelength 0.154 nm, which is ideal for measuring the interatomic distances of 0.15 to 0.4 nm found in most materials. The Bragg angle of the symmetric (004) reflection is used in this work to measure the residual strain in the Ge films. The measurement of the (004) reflection gives the d-spacing in the direction perpendicular to the film surface. The full-width-half-maximum (FWHM) of the (004) reflection is used to assess the relative crystalline perfection of the Ge film, usually compared to a control sample. Figure 3-1 shows a schematic of the double crystal diffractometer-specimen geometry used in this work. The lower image in Figure 3-1 shows the basis of Equation (3-1) in probing the interatomic spacing in the sample using x-rays.

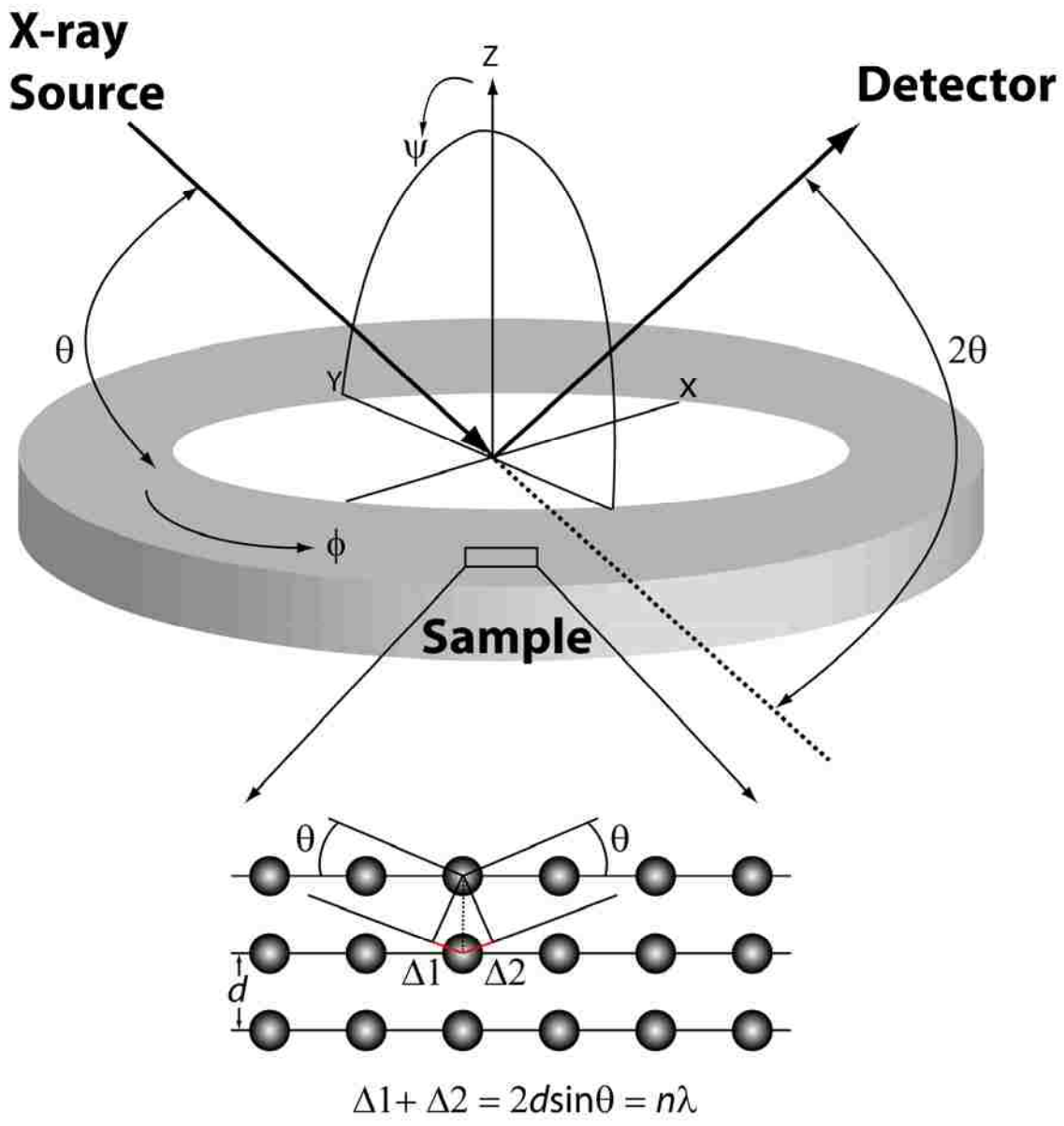


Figure 3-1. Schematic of the diffractometer-specimen geometry. The lower image shows the basis of Bragg's equation in probing the spacing of interatomic planes in the specimen using x-ray radiation.

Assessing the crystal quality of a material by the FWHM of the (004) peak must be used with caution because the line profile is a convolution of several factors. Some of the factors that cause peak broadening are residual strain, defects, small film thickness, and alloying of the film and substrate. The complicating factors sometimes require the use of

a model to simulate and fit a particular peak profile to deconvolute the factors. In addition, the FWHM is not sensitive to strains present from defects in the film below a density of approximately 10^7 cm^{-2}. Despite these complications, XRD is a relatively quick and nondestructive technique that is widely used in materials characterization.

3.2 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is a nondestructive surface-sensitive analytical technique that is commonly used to identify the chemical composition at the surface of a material. The technique of XPS is based upon the photoelectric effect, in which X-rays are used to dislodge core-shell electrons from the material. The following energy balance gives the kinetic energy, KE, of the emitted electrons

$$KE = h\nu - BE - \phi_s \tag{3-2}$$

where h is plank's constant, ν is the frequency of the incident radiation, BE is the binding energy of the core-shell electron of the chemical element in the sample (relative to the vacuum level), and ϕ_s is the spectrometer work function. The BE is equal to the ionization energy of the electron from the particular atomic orbital in which it resides. The BE is sensitive to the local bonding environment of the material and can therefore provide identification of compounds as well as individual elements. The energy of the radiation used in this work is 1253.6 eV, and corresponds to Mg K_α x-rays. The interaction depth of the radiation with the sample varies from 1 to several microns, however, most of the ionized electrons do not escape from the material. The interaction

probability of the emitted electrons with the sample from which they are emitted is such that only electrons existing within a few nanometers of the surface can escape without energy loss. The electrons emitted from the sample are collected and give rise to peaks in the energy spectrum. Electrons that are emitted near the surface that sustain energy losses give rise to the background of the spectrum. Figure 3-2 depicts the interaction of the incident radiation on the sample and the escape depth and intensity of the emitted core-shell electrons.

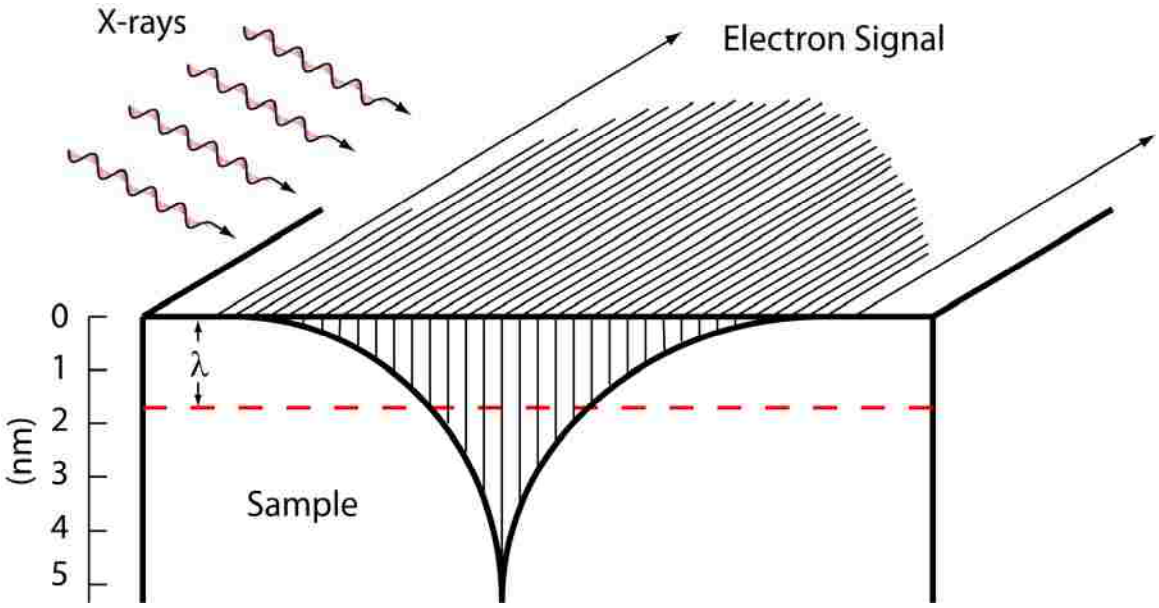


Figure 3-2. Pictorial representation of the distribution of the emission of core-shell electrons from the specimen due to absorption of x-rays, after Watts and Wolstenholme.[68]

The electrons emitted from the sample are collected by an electron spectrometer. The *KE* of the collected electrons is determined by applying a retarding potential that can vary from zero up to the incident radiation energy. The potential is varied until the emitted electrons are completely repelled by the collector, and the collected current drops to zero.

The analyzer is normally operated to accept only a range of energies of 50 eV, referred to as the pass energy. The number of electrons is digitally recorded for a given dwell time and is reported as counts per second. The spectrometer used in this work has an energy resolution of about 0.1 eV, and a schematic of the XPS chamber with major components labeled is shown in Figure 3-3.

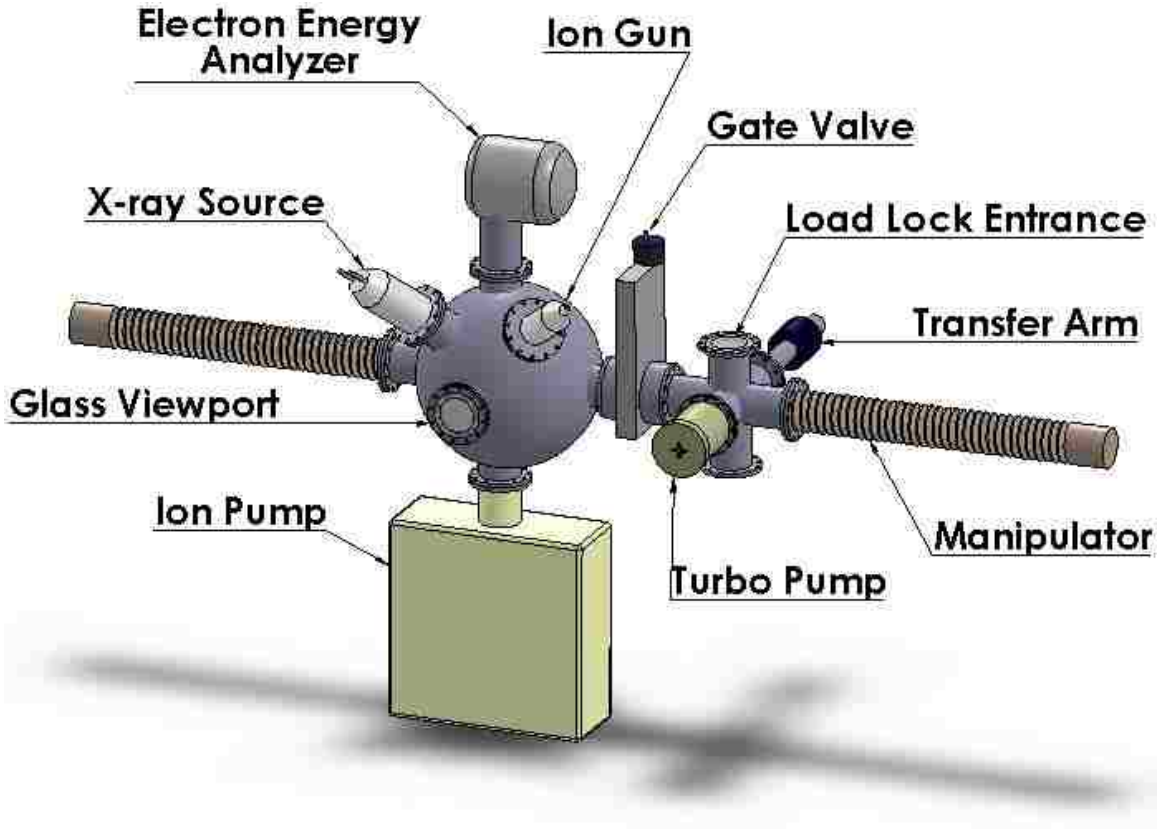


Figure 3-3. Depiction of the x-ray photoelectron spectroscopy chamber used in this work with major components labeled.

The XPS technique has a detection limit of about 0.1 atomic percent.[69] Quantitative analysis using XPS involves finding the relative concentrations of the constituent species. Quantitative analysis begins by measuring the peak areas of all detected species using an

appropriate background subtraction method. The concentration of species *x* is related to the area of the peak for that species by the following equation

$$C_x = \frac{I_x / S_x}{\sum_i I_i / S_i} \tag{3-3}$$

where I_x is the total measured intensity of species x (area under measured peak), S_x is an empirical parameter called a sensitivity factor for species *x*. The sensitivity factor is a parameter that encompasses a number of geometric, detector, and electron-specimen interaction variables. Sensitivity factors used for this work are listed in Wagner *et al*.[70]

3.3 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is used extensively throughout this work. It is the de-facto method for investigating a host of material properties and interfaces. It is capable of atomic spatial resolution and often combines the added capabilities of chemical spectroscopy such as energy dispersive (EDS) and electron energy loss (EELS) spectroscopy. The TEM technique is used in this work to characterize the structure and defect density of Ge and III-V films, measure residual strain, and determine orientation and composition of nanometer sized islands. Some drawbacks of TEM are that is a destructive technique that requires significant effort to prepare specimens, although with the advent of the Focused Ion Beam (FIB), sample preparation is becoming more routine. Samples are typically thinned to less than 100 nm thickness using a combination of mechanical thinning followed by ion polishing, although samples should be less than 50 nm for higher resolution. Figure 3-4 shows the apparatus used to mechanically thin specimens for TEM. The specimen is glued to a

glass work piece that is mounted on a tripod polishing jig. The specimen is mechanically ground on a silicon carbide impregnated polymer sheet that is mounted to a rotating wheel. The thickness of the sample after mechanical polishing is 7 to 15 μm. Ion polishing is used to remove the damage from mechanical grinding and for final thinning of the specimen to electron transparency. Ion polishing utilizes argon ions accelerated to several keV to sputter material from the specimen at glancing angles of 1 to 10 degrees with respect to the specimen surface. Figure 3-5 shows the operating principle of ion polishing.

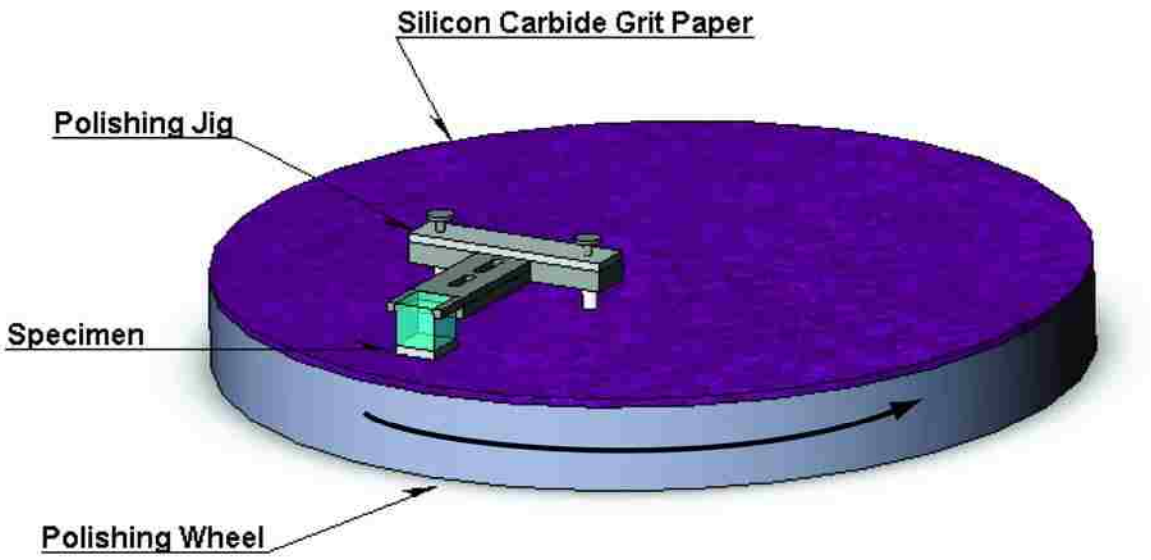


Figure 3-4. Apparatus for mechanically thinning transmission electron microscope specimens. The specimen is mounted to the tripod jig on the glass piece and ground down on a silicon carbide impregnated polymer sheet that is placed onto a rotating wheel.

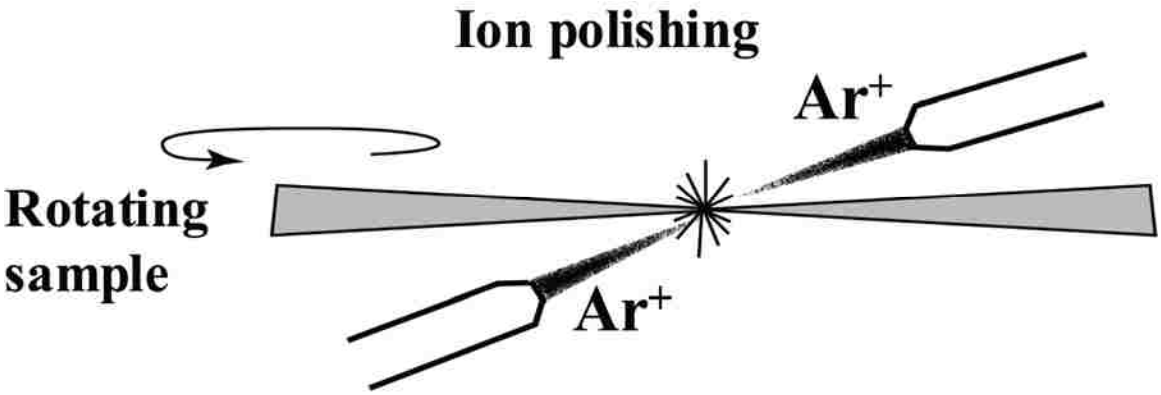


Figure 3-5. Operating principle of ion polishing that is used for final specimen thinning for the transmission electron microscope.

The thinned sample is then transparent to high-energy electrons, which is the basis for TEM. Figure 3-6 shows the major components of the TEM and the diffraction of electrons from a crystalline specimen.

In the TEM, a 200 keV beam of nearly temporally and spatially coherent electrons is focused onto the sample. The spatial resolution of the electrons is less than 1 angstrom, but due to a number of lens aberrations, the typical point resolution of the instrument is approximately 1.5 nm. Newer instruments with aberration correction can achieve sub-angstrom point resolutions. For crystalline specimens, many of the electrons that impinge on the sample get elastically scattered, i.e. diffracted. The diffracted beams occur at particular angles called Bragg angles, akin to x-ray diffraction. Diffraction occurs in the back focal plane of the TEM, and the diffraction pattern of the specimen can be imaged and digitally recorded for analysis. An aperture placed just below the objective lens of the microscope can also be used to filter out one or more of the diffracted beams from contributing to image formation of the specimen.

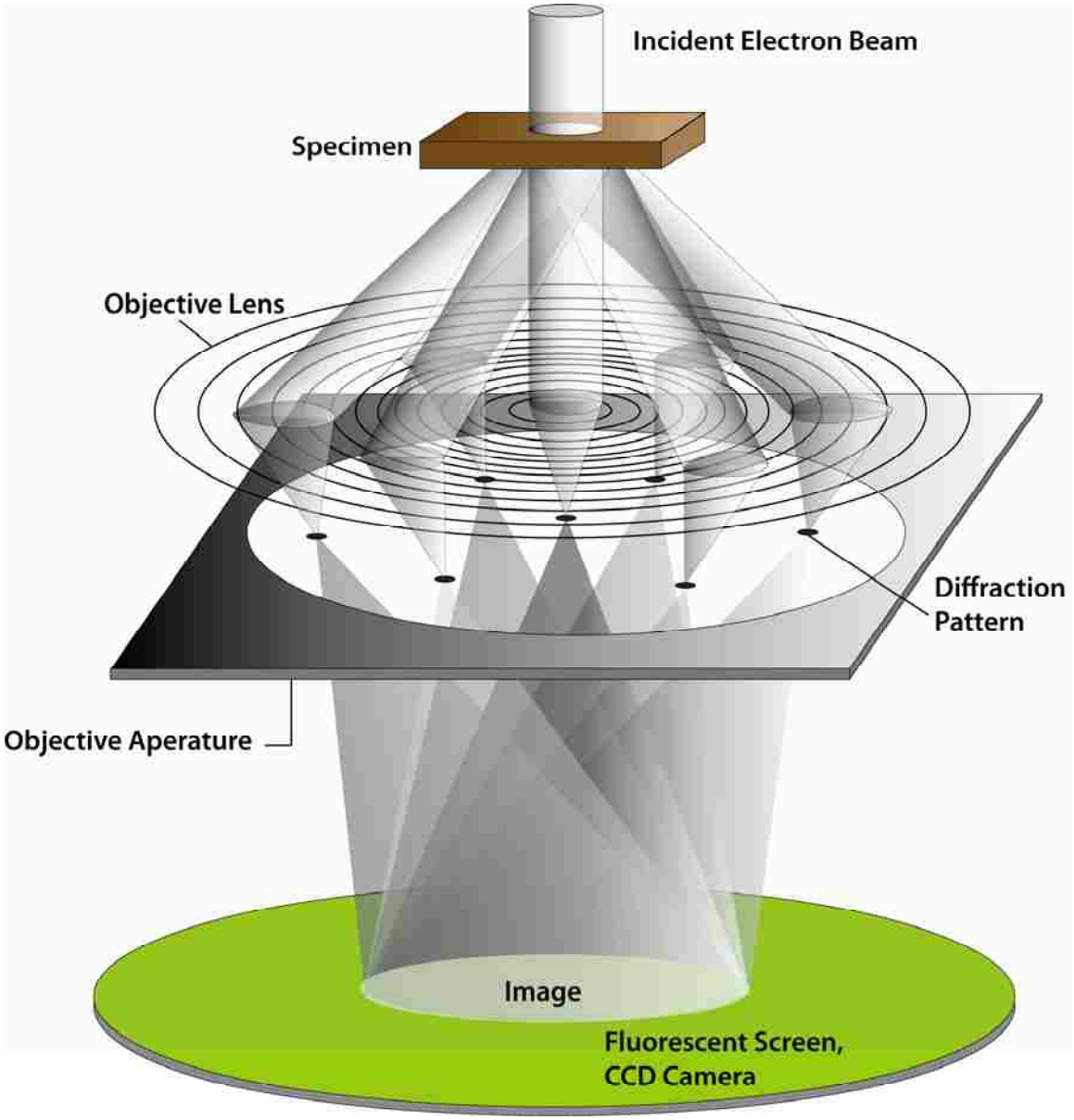


Figure 3-6. Schematic of a transmission electron microscope and interaction of incident electrons onto a crystalline specimen.

The basis of forming bight and dark-field images involves using either the transmitted (undiffracted) beam to form the image, or using one or more diffracted beams. In bright-field imaging, only the undiffracted beam is allowed to pass through the objective aperture, whereas in dark-field imaging, the undiffracted beam is blocked by the aperture. The advantage of bright and dark field imaging is the greatly enhanced

contrast that occurs, known as diffraction contrast. For example, in bright-field images, defects such as TDs often appear in images as dark lines. The TDs appear dark because the strain field that is present around the dislocation core bends some of the crystal planes into the Bragg condition for diffraction. Since the diffracted beams do not contribute to formation of the image, the diffracting region around the dislocation appears dark, and the defects can easily be seen in the image. In dark field imaging, the defects appear bright on a dark background, since the diffracting planes are the only ones contributing to the image formation. At higher resolution of crystalline specimens, a different type of contrast known as phase contrast occurs.

In phase contrast TEM, the specimen is tilted so that the incident electron beam is directed along a particular low index direction in a crystal. The resulting diffracted and transmitted beams then interfere with one another. The interference of the beams results in a fringe pattern in the image, and under certain conditions, the spacing between the fringes is directly related to the lattice spacing in the crystal. Figure 3-7 (a) shows an example of a crystalline Si specimen oriented along a [110] direction so that diffracted beams from (111), (220), and (113) planes can interfere and give rise to lattice fringes in a high-resolution TEM image. The accompanying diffraction pattern of the Si sample is also shown in Figure 3-7 (b).

In addition, the lattice fringe images can be Fourier filtered or transformed back into diffraction images for orientation and strain analysis at very high spatial resolution. In addition to the elastic interaction of the electron beam with the specimen in forming diffracted beams, inelastic scattering also occurs, forming the basis of the scanning transmission electron microscopy (STEM).

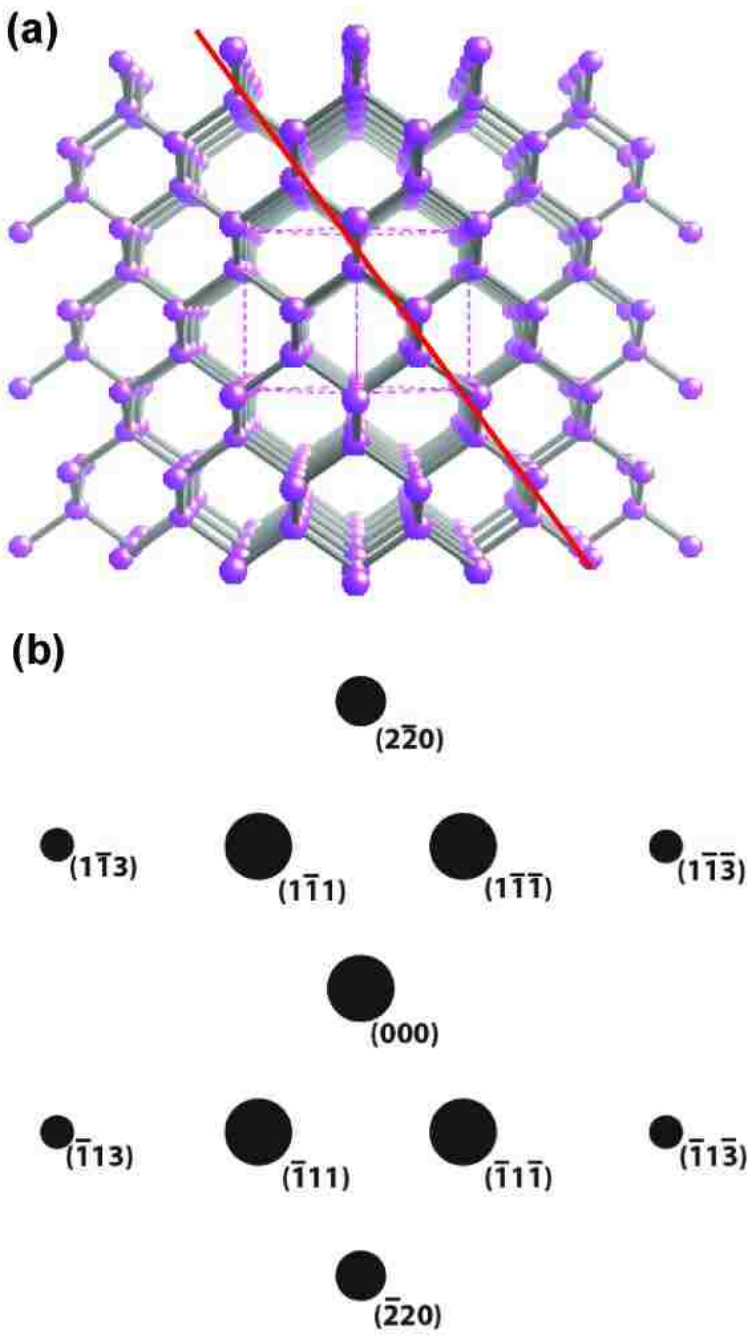


Figure 3-7. Image (a) shows the crystal structure of diamond cubic Si oriented along a [110] direction. The (111) plane is highlighted by the red line. Image 3-7(b)shows the diffraction pattern corresponding to the Si sample in image 3-7(a).

3.4 Scanning Transmission Electron Microscopy

In STEM mode, the electron beam is focused into a diameter less then 1 nm onto the sample, and is called an electron probe. The probe is then scanned across the specimen similar to SEM. Electrons that are transmitted and inelastically scattered through the sample at high angles are collected onto a charge coupled device to form an image of the specimen. The scanned area on the sample and the electron probe diameter determine the magnification of the image, and resolutions can be less than 1.5 nm. Image interpretation in STEM is usually much easier than phase contrast images in TEM. Another advantage of STEM mode is the use of small electron probe to excite a very small volume of material in the sample for electron spectroscopy. Nanometer resolution is possible in collecting spectroscopic information from emitted x-rays using EDS or from inelastically scattered electrons in EELS. The configuration and major components of STEM are shown in Figure 3-8.

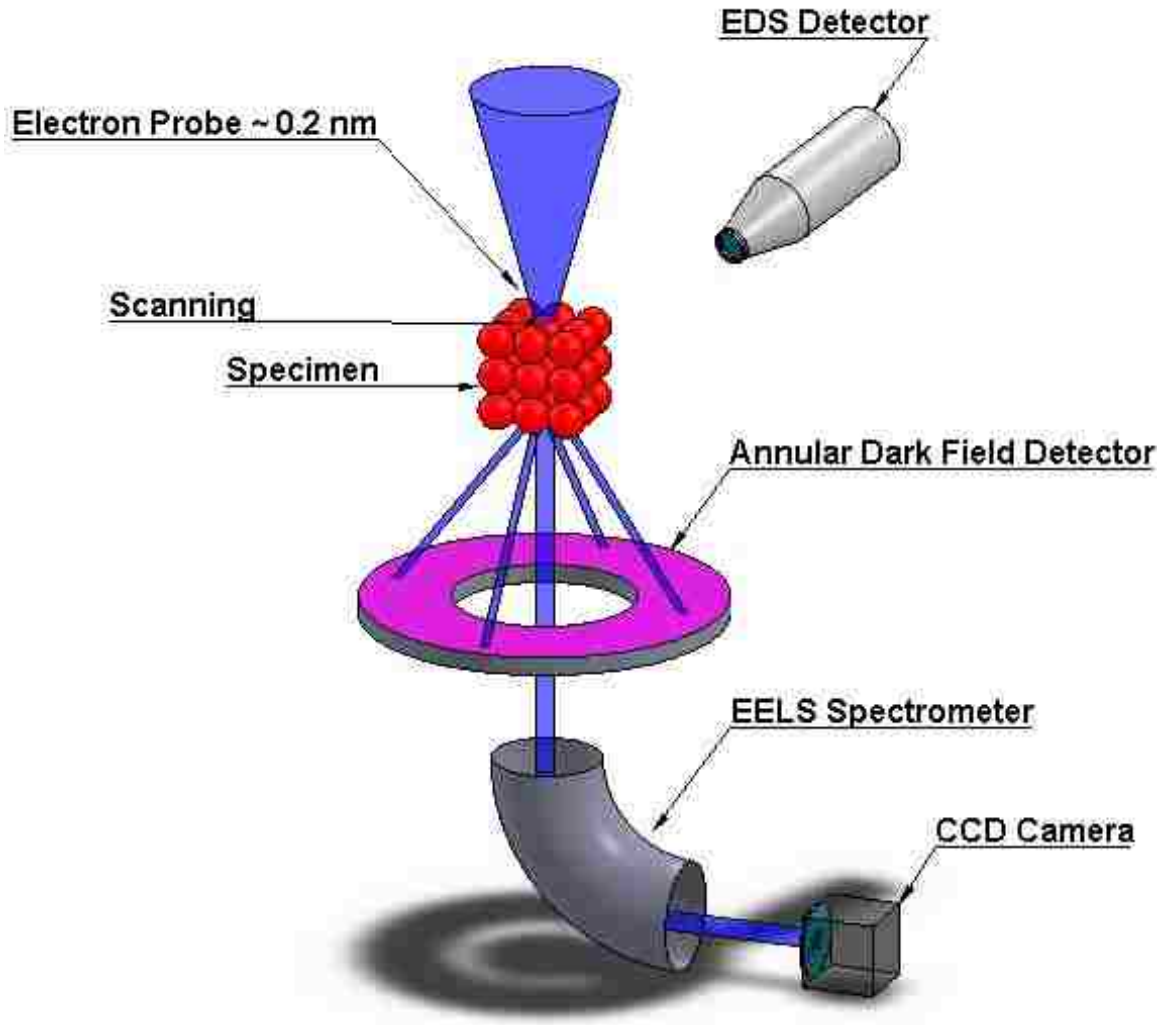


Figure 3-8. Scanning transmission electron microscope configuration with accompanying spectroscopic capability.

3.5 Energy Dispersive Spectroscopy

In EDS, x-rays are generated within the specimen due to inelastic scattering by electrons in the probe. The x-rays are collected into a Si-Li drift detector that converts the x-rays into an electronic signal. The accuracy and detectability of the method is dependent on the number of x-rays that can be collected. If high spatial resolution is desired, then a smaller probe size is best, however, the current in the probe is also

smaller, meaning that longer counting times are required to collect the signal. Excessively long collection times encounter two primary difficulties. One, the sample drifts during the time of the measurement. This problem can be offset with a drift correction algorithm in the EDS software that is applied to keep the probe on the same location on the sample. The second problem is that a carbon layer quickly deposits on the location of the specimen that is irradiated by the electron probe. The carbon film comes from decomposition of hydrocarbon contamination that exists due to imperfect vacuum in the TEM, and the carbon buildup will eventually cause loss of signal from the illuminated area. In this work, a total of 10,000 counts are collected using a 1 nm diameter probe size. This probe diameter contains enough current to make a composition measurement within a few minutes that is accurate within ±10 %. The detection limit of EDS is approximately 1 atomic percent.

3.6 Scanning Electron Microscopy

The SEM is used extensively in this work to measure the thickness of films and surface topography, and is often used in conjunction with other techniques such as EDS and backscatter diffraction orientation analysis. The SEM works by focusing and scanning a beam of electrons onto the sample surface. The electrons interact with the sample generating elastic and inelastic collisions. Elastically scattered electrons, known as backscattered electrons (BE) and inelastically scattered electrons, known as secondary electrons (SE) are emitted from the sample. The BE and SE electrons are collected into a detector and used to build an image on the screen. Although the diameter of the electron probe is 1 to 2 nm, the excited volume on the sample may be up to 1 μm in diameter for

30 keV electrons. The SE and BE are emitted from the entire excited volume and contribute to the image formation so that the resolution of the SEM is generally on the order of 5 to 10 nm. Using lower electron energies to excite a smaller volume of sample material and using coatings of high atomic number materials like Pt or Au can increase the resolution to 1 to 3 nm in some cases.[71] Figure 3.9 depicts the excitation processes occurring within the sample due to absorption of incident high-energy electrons from the probe; image (a) for 5 keV incident electrons, image (b) for 30 keV electrons.

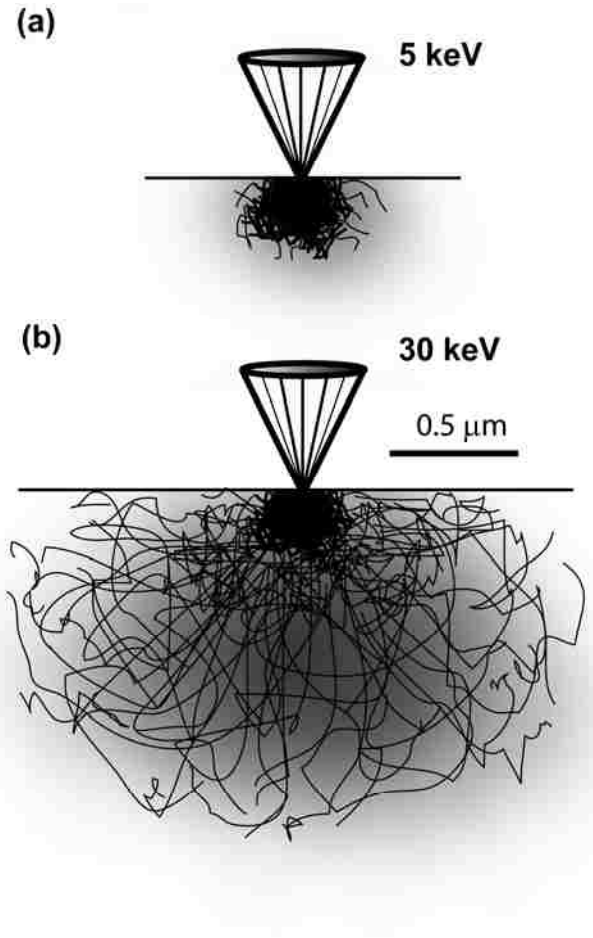


Figure 3-9. Depiction of the electronic excitation processes occurring within the sample due to absorption and scattering of high-energy incident electrons for 3-9(a) 5 keV, and 3-9(b) 30 keV incident electrons, after Goldstein *et al.*[71]

3.7 Focused Ion Beam

The FIB is a method of imaging and patterning materials using a beam of Ga ions. The technique works analogously to the SEM where the beam of Ga ions is scanned across the surface to generate SE and BE electrons that are used for image formation. The heavy Ga ions can also be focused into a small probe diameter on the sample surface such that material is sputtered from the irradiated area at a high rate. The sputtering effect is used to pattern and etch materials, including preparation of thin sections for TEM analysis. The ion beam instrument is also used in conjunction with SEM imaging to provide real-time monitoring of the patterning taking place with the ion beam, as shown in Figure 3-10.

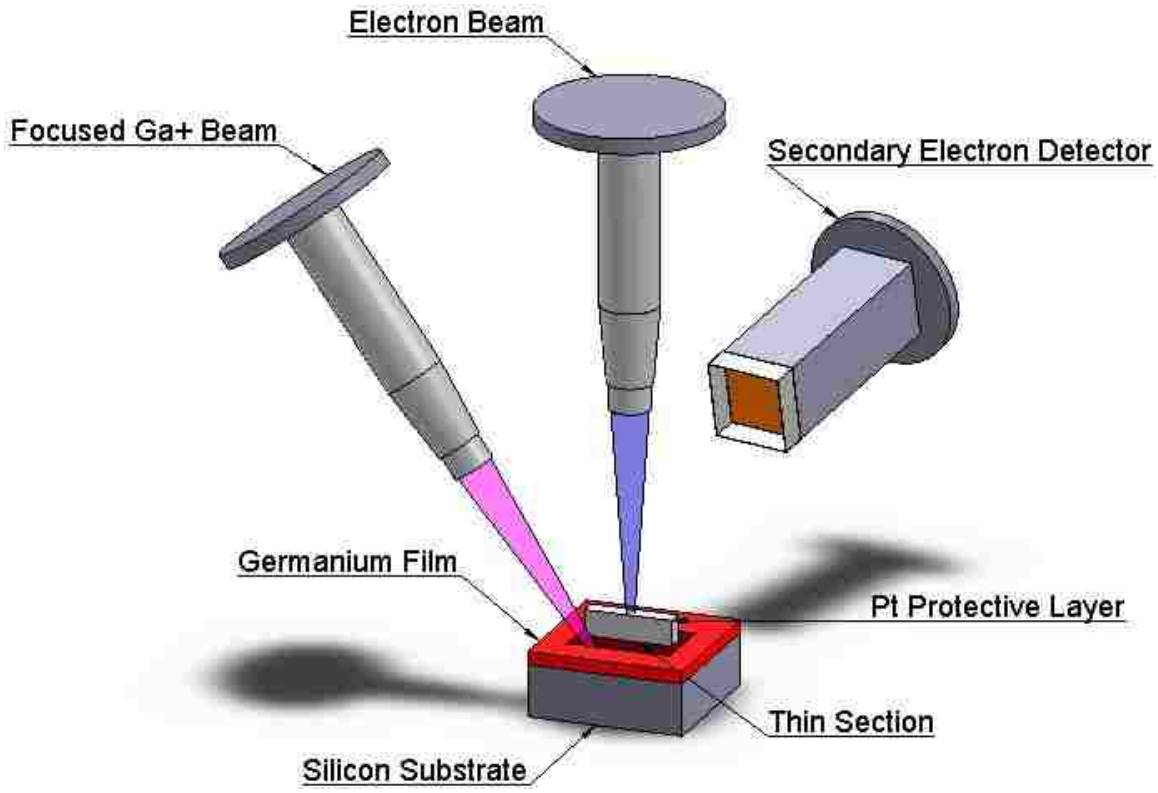


Figure 3-10. Operating principle of the scanning electron microscope and focused ion dual beam instrument that is used simultaneously for imaging and patterning.

A dual electron/ion beam instrument is used to prepare some of the cross-sectional TEM samples used in this work. Care must be taken to remove the damage done by irradiating the sample with 30 keV Ga ions. The damaged layer is up to 70 nm deep at 30 keV.[72] The instrument voltage is reduced to 5 keV for final specimen thinning, leaving a damaged layer only a few nm deep. High quality TEM specimens are regularly produced that are 50 nm or less in thickness in about 4 hours with the FIB. Figure 3-11 shows SEM images of the TEM specimen at different stages of preparation using the FIB.

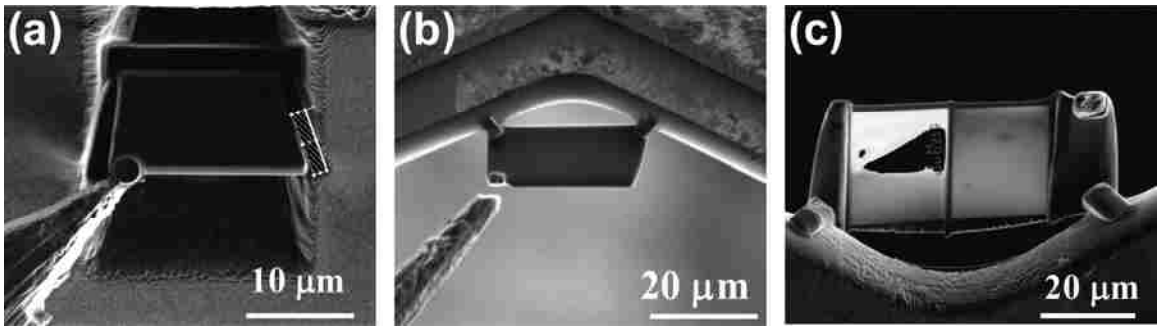


Figure 3-11. Specimen preparation for the transmission electron microscope using a focused ion beam. Image 3-11(a) shows the cross-section cut-out of the specimen being lifted out with a tungsten tip. Image 3-11(b) shows the specimen mounted to a copper half-grid. Image 3-11(c) shows the specimen after thinning to electron transparency. The left side of the specimen has been over thinned such that a hole has formed in the center.

3.8 Atomic Force Microscopy

Atomic force microscopy (AFM) is used to image topography by scanning a physical probe across the sample surface. The probe is a Si cantilever with a sharp tip at the end. The tip protrudes downward from one side of the Si cantilever and has a radius of curvature of 10 to 30 nm. The tip is scanned across the surface using piezoelectric

crystals. Topography on the sample surface causes the cantilever and tip to deflect up and down. The deflection of the cantilever is monitored as it moves across the sample surface with a HeNe laser that is reflected from the backside of the cantilever onto a position-sensitive photodetector. The deflection of the cantilever causes the reflected laser beam to change positions on the photodetector, and these changes are converted into height measurements that correspond to the sample topographic features. Figure 3-12 shows the primary components of the AFM.

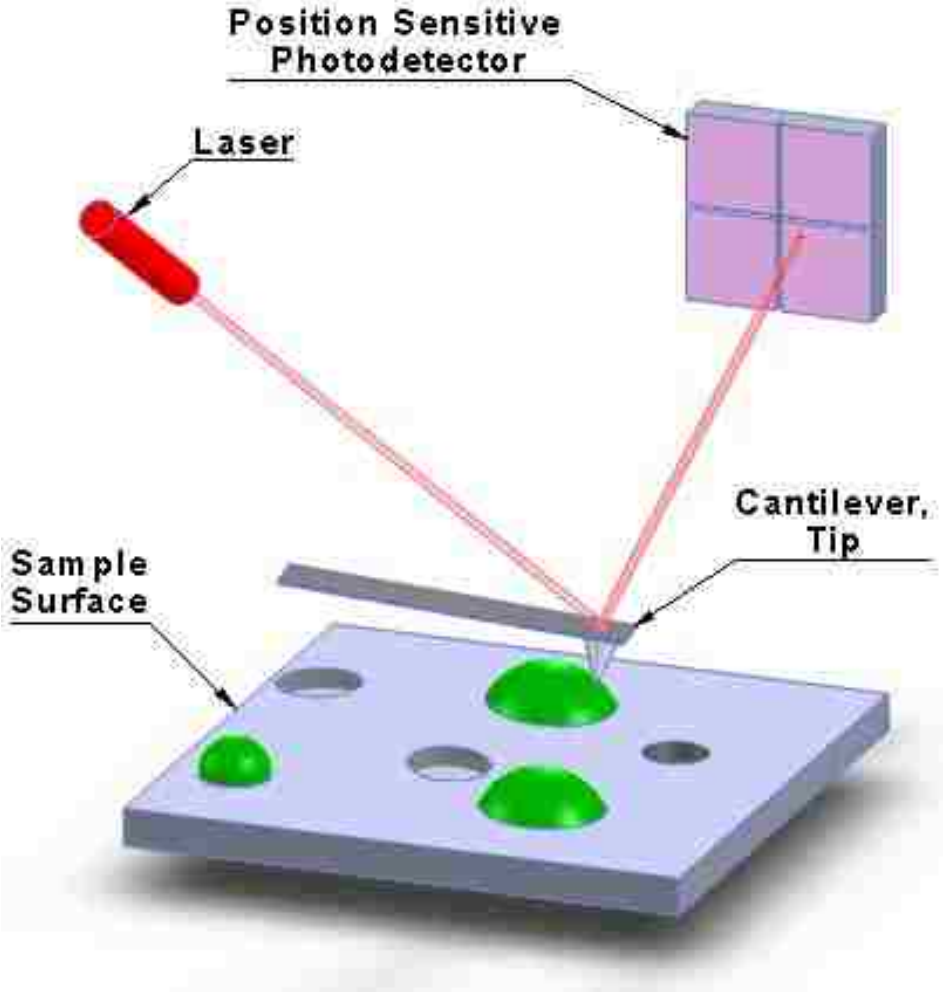


Figure 3-12. Illustration of the major components and operating principle of the atomic force microscope.

The AFM can be operated in contact or non-contact modes, but non-contact is usually preferable. Contact mode involves physically dragging the Si cantilever tip across the sample surface. The resulting topography measurements are most accurate for hard materials, but the tip can be worn and damaged while scanning. Additionally, the tip can easily become contaminated by small particles on the sample surface, decreasing the accuracy of the measurement in contact mode. Non-contact mode involves bringing the tip into close proximity to the sample surface such that van der Waals forces between the sample and tip cause the tip to deflect. This method is slightly less accurate in measuring the surface topography, but doesn't suffer from the drawbacks mentioned for contact mode, and non-contact is the mode used throughout the work shown here.

3.9 Etch Pit Density

Etch pit density (EPD) measurements are used to measure the number of certain types of defects that intersect a sample surface. The method works by creating a layer of oxide on the sample surface by exposing the sample to an oxidizing agent such as sulfuric or nitric acid. A second reagent such as HF is added to the oxidizer to subsequently dissolve the oxide on the sample. Often, water or acetic acid is used as a dilutant to control the etch rate of the sample. Etching of the sample reveals defects by selectively removing material at a faster rate at the defect site compared to the surrounding material, thereby creating a recessed area or pit at the defect site. The pits are then counted to provide an estimate for the number of defects intersecting the sample surface. The faster etch rate at defects such as dislocations, twins, stacking faults (SF), and APBs, is caused by the internal stress fields that exist around these defects. The excess stress around the

defects lowers the bond strength of the material making it more reactive to the etchant. The advantage of the etch pit density measurement is that it is fast and easy and can provide much more reliable counting statistics of the defect density in a material, especially indirect bandgap semiconductors that cannot use cathodoluminescence (CL) imaging for defect counting. Figure 3-13 illustrates the formation of etch pits created around the TDs intersecting a sample surface.

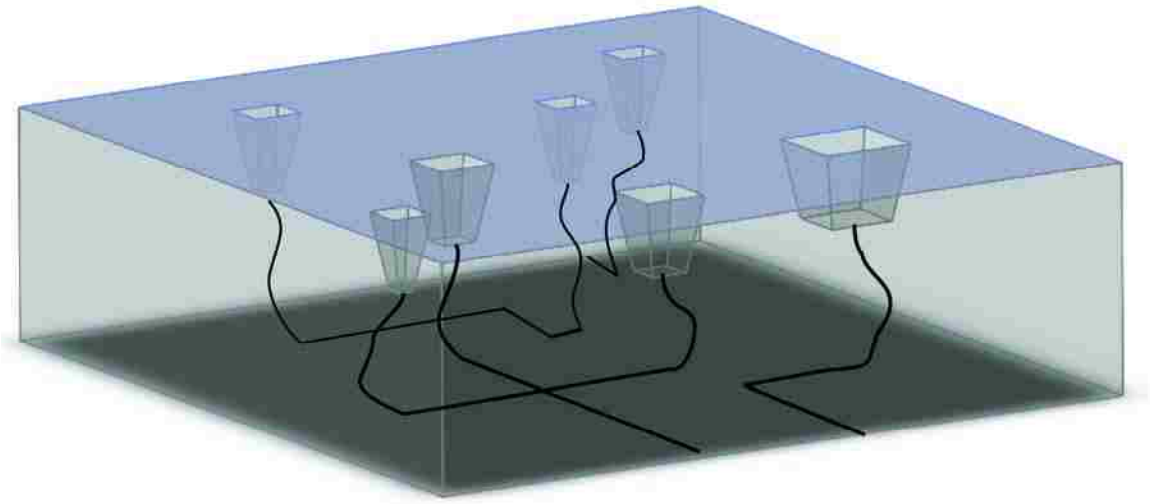


Figure 3-13. Stress fields occurring around threading dislocations in the sample cause those regions to etch faster than the surrounding material. Counting the etch pits can provide an estimate of the dislocation density in a material.

The drawback of the technique is that it may not reveal all defects in a material, and the defect density usually needs to be measured or calibrated with another technique such as plan-view TEM. The defect density usually must be below 4×10^8 cm^{-2} so that the pits can be clearly resolved from one another for accurate counting. Higher defect densities must be determined using TEM. The method of EPD overlaps nicely with measurements made with TEM because the lower limit of defect counting in the TEM is about 10^7 cm^{-2}.

3.10 Photoluminescence and Cathodoluminescence

Photoluminescence (PL) is an optical excitation technique in which photon emission is generated in a material using a coherent light source and the energy of the emitted photons are analyzed with a spectrometer. The advantages of PL are that the measurements are fast, easy, and nondestructive. The energy and intensity of the emitted photons gives information on the bandgap of the material, impurity type and concentration, residual strain, and defect density. In this work, the PL intensity is used to compare relative defect concentrations in a sample by comparison with a control sample. In addition, by measuring the decay rate of the PL signal, the minority carrier lifetime of the sample is obtained. The minority carrier lifetime of the sample is a strong function of the non-radiant recombination defect density in a material. The minority carrier lifetime is the most conclusive predictor of performance of minority carrier devices such as solar cells. The decay rate of the PL in this work is measured using time-correlated single-photon counting. Photon emission is generated in the sample using a low intensity pulsed laser source. The photon emission from the sample is collected into a photomultiplier tube where single photoelectron states are created and detected. The advantages of using low level light sources for PL decay measurement are added stability and better signal to noise ratio, as compared to using higher intensity excitation sources. The technique of CL is closely related to PL and provides similar information about the sample. In CL, high energy electrons are used to excite photons emission in a material rather than photons. The CL technique is, however, limited to direct bandgap materials to get appreciable photon generation from the sample. Advantages of CL include

nondestructive, fast, and easy measurements. The CL measurement also provides the advantage of being able to image the sample, including defects, at high spatial resolution. The CL measurement is a capability that is often added to an SEM, which provides a source of focused high-energy electrons for photon excitation of the sample.

3.11 Interferometric Lithography

Interferometric lithography (IL) is a patterning technique capable of generating periodic arrays of feature sizes less than 20 nm. The method involves the use of a coherent light source (355 nm fourth harmonic of an Nd:YAG laser) in which the laser beam is defocused to provide a large exposure area. The distance traveled by half of the laser beam is then changed by reflection from a plane mirror to create a phase difference between the reflected and unreflected portions of the beam. The reflected and unreflected parts of the beam then interfere with each other to produce an interference pattern on the photoresist (PR) coated sample. A single exposure and develop step results in the generation of an array of parallel lines in the PR. A second exposure on the sample that is rotated by 90^{o} with respect to the first exposure results in the generation of a square array of holes (posts) for negative PR (positive PR). The feature size is a function of the wavelength of the light that is used and the angle of the reflection from the plane mirror, and is given by the following relationship

$$p = \frac{\lambda}{2\sin\theta} \tag{3-4}$$

where p is the pitch of the feature, λ is the wavelength of the illumination source, and θ is the angle of reflection from the plane mirror. Figure 3-14 is a schematic of the IL setup used in this work.

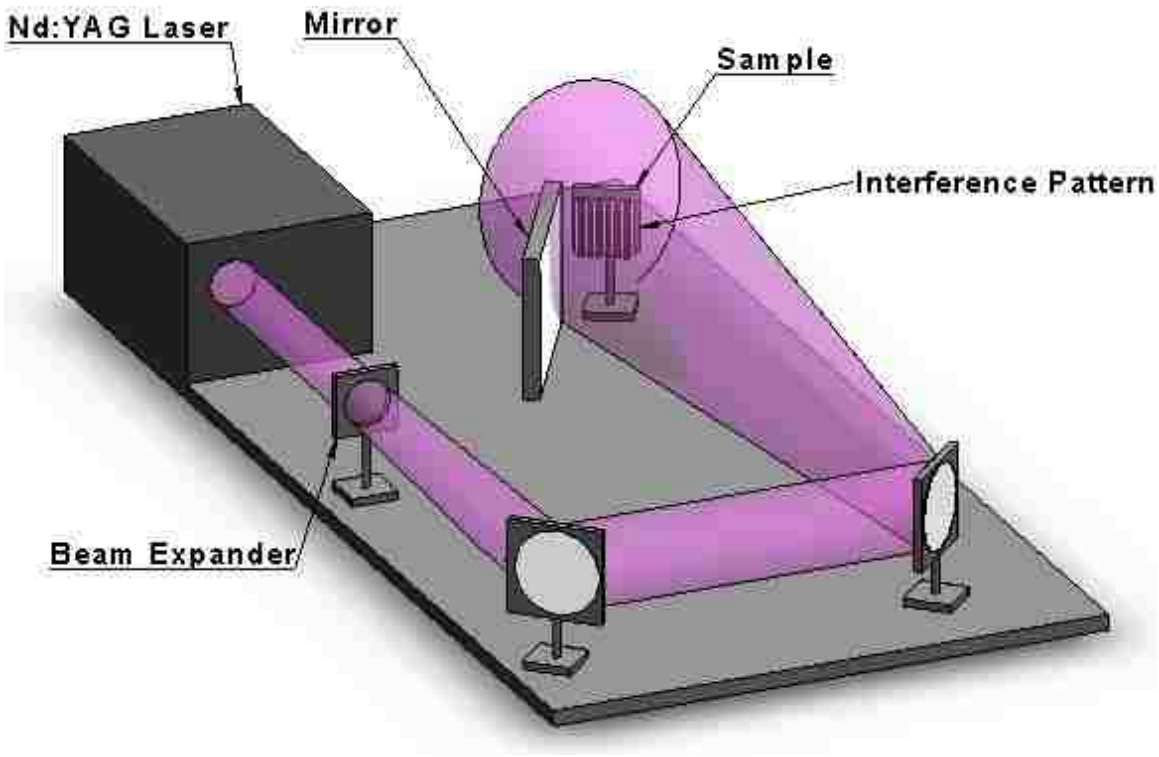


Figure 3-14. Schematic of the interferometric lithography experimental setup and operating principle.

The pitch refers to the wavelength of the pattern that is created, whereas duty cycle refers to the symmetry of the pattern. A one-dimensional array of trenches in patterned PR with a duty cycle of 50 % means that the width of the trench is equal to the width of the wall in the pattern. A duty cycle greater than 50 % means that the wall is wider than the trench width. The duty cycle can be varied by utilizing nonlinearities in the PR, such as exposure and development time. The typical pitch used in this work varies from 300 to 400 nm, and duty cycles greater than 50 %.

CHAPTER 4 SURFACE PROCESSES OCCURING DURING EPITAXY

4.1 Fundamentals of Epitaxy

Chapter 2 discussed the process of evaporation and the transport of vapor species from the effusion cell to the substrate surface. Chapter 4 discusses the atomistic processes occurring on the substrate surface due to the impingement of atoms from an evaporation source. The atomistic processes occurring on the surface include adsorption, surface diffusion, bonding, and desorption, each with potential energies represented by E_{ads}, E_{diff}, E_b, and E_{des}, in turn. The energetic terms represent the depth of potential energy wells for the various processes in which the adatoms interact on and with the surface of the substrate. The term E_{ads} is usually negligible in MBE where the adatoms are highly reactive neutral species. The term E_{diff} represents the potential energy that an adatom must overcome to hop from one adsorption site to another on the surface. The term E_b represents the binding energy of an adatom with another adatom of the same species. The E_{des} term represents the energy barrier for an adatom to leave the surface after adsorption, so that E_{des} is the bond energy of the adatom with the substrate surface. The energetic terms are unique to each material, but E_{diff} is generally about 3 times smaller than E_{des}.[73]

Figure 4-1 shows a simplified view of a crystalline material surface.

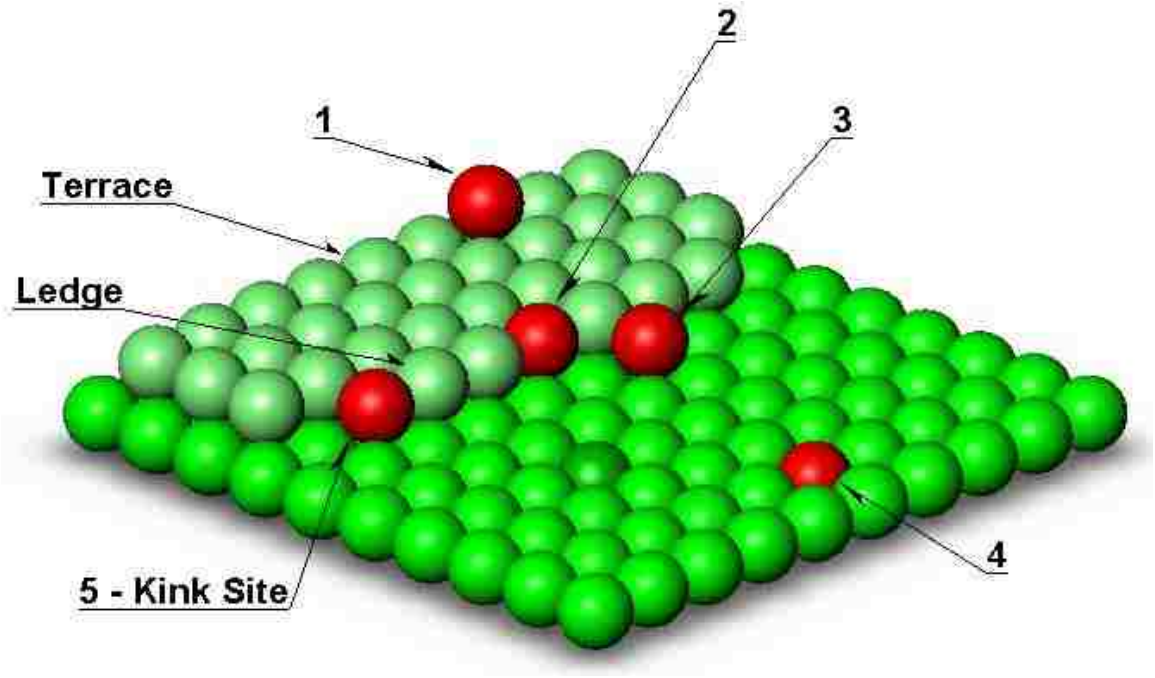


Figure 4-1. The Terrace-Ledge-Kink model of a crystalline surface showing the important features and bonding sites for adatoms (shown in red).

The surface shown in Figure 4-1 contains a structure consisting of terraces, ledges, and kinks that provide a variety of potential bonding sites for adatoms numbered 1 through 5, each possessing different values of E_{des}. The relative energies of E_{des} can be ranked using a nearest-neighbor bonding model. Bonding sites with a greater number of nearest-neighbor bonds represent deeper potential energy wells and greater values of E_{des}. For example, site one, on top of the terrace, has 3 nearest neighbor bonds, while site five has 9 bonds, compared to a total possible 12 bonds for an atom in the bulk of the material. Site five, called a kink site, is a particularly unique site because an adatom in this position has 6 nearest-neighbor bonds, exactly one half of the total possible bonds. Upon addition of an adatom to a kink site, another kink position is formed, and therefore, adatoms can be continually added or removed from kink sites without changing the overall free energy of the surface. Epitaxial growth occurring layer-by layer from adatom attachment to kink

sites is called step-flow growth and occurs at elevated temperatures on crystalline substrates. In general, there are three different modes of crystal growth that have been observed, and these are depicted in Figure 4-2.

The epitaxial growth mode shown in Figure 4-2 (a) occurs when islands grow either as 2-dimensional (2D) platelets or in the step-flow growth mode described above. Layer-by-layer growth is also known as Frank-van der Merwe growth and generally occurs in homoepitaxy, where the condensing vapor species is identical to the substrate material. The FM growth mode occurs for $E_b \leq E_{des}$, meaning that adatoms bond more strongly or equally as strong to substrate atoms as they do with other adatoms of the same species.

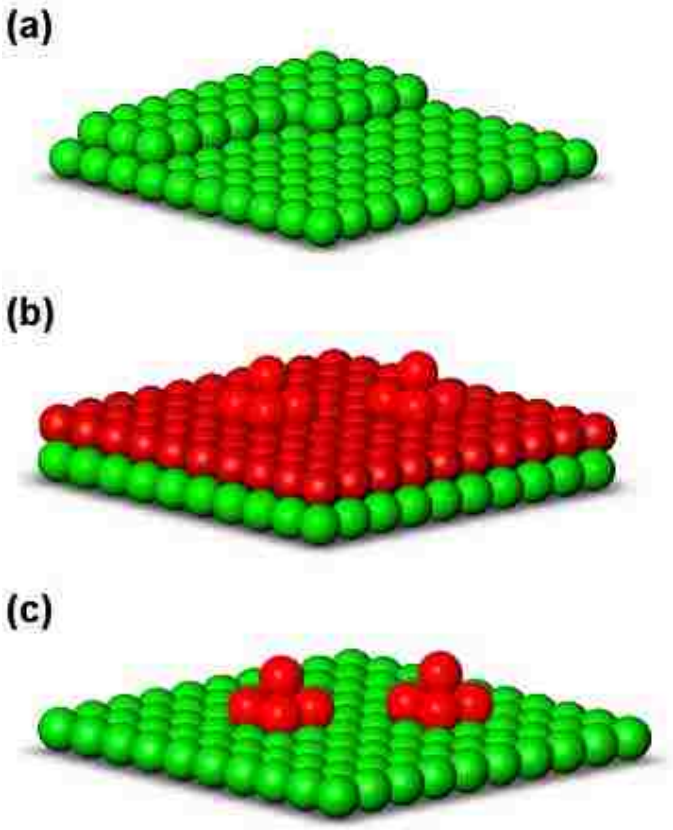


Figure 4-2. The three modes of epitaxy, 4-2(a) Frank-van der Mere, 4-2(b) Stranski-Krastanov, and 4-2(c) Volmer-Weber growth.

The growth mode pictured in Figure 4-2 (b) is called Stranski-Krastanov (SK) growth and occurs when growth is initially layer-by-layer, but is later driven into a 3-dimensional (3D) island growth mode. The SK growth mode occurs for $E_b < E_{des}$, where the bond formed between the adatom and the substrate is stronger than the bond that adatoms have with one another. The transition to 3D island formation is often driven by lattice mismatch stress, which increases with film thickness as shown in Equation (1-3). Island formation occurs because it partially relieves the mismatch strain of the system as shown by the work of Luryi and Suhir and discussed in Chapter 2. The 3D islands often form after a few monolayers (ML) of 2D growth, and this layer is called a wetting layer. The SK growth mode is commonly observed in most heteroepitaxial systems, including GoS.

Lastly, Figure 4-2 (c) depicts Volmer-Weber (VW) growth in which 3D island formation occurs without formation of a wetting layer. This situation occurs for $E_b > E_{des}$, where adatoms bond more strongly to each other than to substrate atoms. This situation occurs during growth of most metals and semiconductors on insulating materials such as amorphous SiO_2 or Si_3N_4. Understanding island nucleation behavior on these insulators is important in selective epitaxial growth (SEG).

4.2 Selective Epitaxial Growth

The SEG of Ge and GeSi has become increasingly important in a variety of advanced device applications, including high-speed HBTs[74-76] and metal-oxide semiconductor field-effect transistors (MOSFET)[77-80]. Other applications include ordered arrays of quantum dots[81-85] for photodetectors[86] and quantum cellular automata[87]. In

addition, SEG is required in the aspect ratio trapping and finite area growth defect reduction strategies for heteroepitaxy discussed in Chapter 1.

In SEG, the substrate surface contains areas of crystalline material adjacent to amorphous insulating materials. Epitaxial growth is desired on the crystalline portion of the substrate, but not on the insulating portions. Nucleation on amorphous insulators is random in nature and leads to polycrystalline or amorphous thin film growth. For successful SEG, random nucleation on the insulator must be prevented. Thus, it is important to determine the mechanisms and energetics of nucleation on the insulator responsible for optimal selectivity. The nucleation energetics can be extracted by applying atomistic nucleation theory to measurements of island densities on the insulator. The fundamentals of atomistic nucleation theory are presented next and applied to experimental results of Ge nucleation on SiO_2 to extract the energetics of the nucleation process. The energetics of Ge nucleation on SiO_2 are then used, in turn, to achieve optimal selectivity of Ge on Si versus SiO_2, and to understand the mechanisms involved in achieving SEG.

4.3 Atomistic Nucleation Theory

Atomistic nucleation theory is a rate-equation approach used to predict the energetics that are involved in the island nucleation process. Figure 4-3 graphically depicts the important atomistic processes of adsorption, desorption, surface diffusion, nucleation, and island growth that occur simultaneously on the substrate surface during deposition. Atomistic nucleation theory uses mathematically coupled rate equations to describe the surface processes and predict the nucleation density of islands as a function

of time. Measurement of the island density can be used to extract the fundamental energetics of the system such as E_{des}, E_{diff}, and E_b. The magnitude of the energetic terms can then be used to optimize the growth conditions to achieve maximum selectivity in SEG experiments.

Figure 4-3 also introduces the notation used in developing the rate equations describing the atomic processes occurring on the surface.

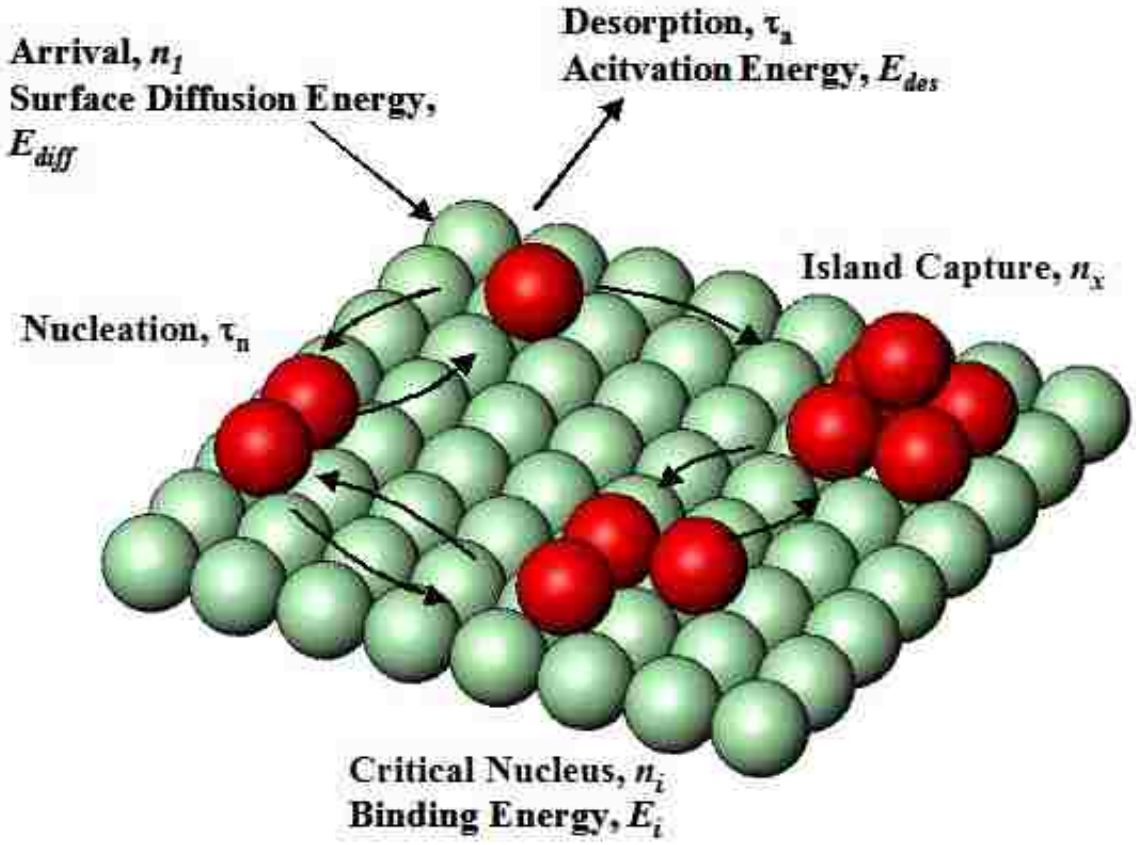


Figure 4-3. Depiction of the atomic processes occurring on a surface due to impingement of atoms from an evaporation source. The notation used in developing atomistic nucleation theory is also shown for each process.

The term n_1 represents the atoms impinging on surface from the evaporation source. These atoms undergo surface diffusion in moving from one adsorption site to another that

requires the atom to overcome an energy barrier represented by E_{diff}. Atoms can also be desorbed back into the vacuum after acquiring an energy represented by E_{des}. The characteristic time that the adatoms spend diffusing on the surface before desorbing is represented by τ_{des}. Adatoms diffusing on the surface can also collide with other adatoms on the surface and bond to each other to create an island. The rate of formation of islands on the surface is the nucleation rate and is represented by n. These small islands may not be stable at elevated temperature and can break apart into individual adatoms. Islands that decay back into adatoms are called subcritical clusters and are represented n_j, whereas larger clusters that grow by capturing adatoms are termed stable clusters and are represented by n_x. An island at the critical size, n_i, is one that will form a stable island and continue to grow upon addition of one additional adatom. These critical clusters are made up of i number of adatoms and the adatoms in the cluster have a bond energy with one another of E_i. Stable clusters continue to grow and give rise to film growth on the surface.

The kinetic processes described in Figure 4-3 are represented mathematically based on Venable's[88,89] treatment:

$$\frac{dn_1}{dt} = \Phi - \frac{n_1}{\tau_{des}} - \frac{d(n_x a_x)}{dt} \tag{4-1}$$

$$\frac{dn_j}{dt} = 0 \qquad 2 \le j \le i \tag{4-2}$$

$$\frac{dn_x}{dt} = \sigma_i D n_1 n_i \tag{4-3}$$

$$\frac{d(n_x a_x)}{dt} = (i+1)\sigma_i D n_1 n_i + \sigma_x D n_1 n_x + \Phi n_x a_x \qquad (4\text{-}4)$$

where a_x is the surface area of a stable island, σ_i and σ_x are called capture numbers and are described below, and D is the surface diffusion coefficient given by

$$D = \frac{\nu_{\parallel}}{4N_o} \exp\left(\frac{E_{des}}{k_b T}\right) \qquad (4\text{-}5)$$

in which $\nu_{||}$ is the substrate surface vibration frequency in the surface plane (~ 10^{13} s^{-1}), N_o is the surface density of adsorption sites, and T is the substrate temperature. The desorption rate, τ_{des} is given by

$$\tau_{des} = \frac{1}{\nu_{\perp}} \exp\left(\frac{E_{des}}{k_b T}\right) \qquad (4\text{-}6)$$

where $\nu_{\perp}$ is the surface vibration frequency perpendicular to the surface plane. Together, equations (4-1) to (4-4) are coupled differential equations describing the processes depicted in Figure 4-3.

Equation (4-1) describes the time rate of change for individual adatoms on the surface. The first term on the right hand side of equation (4-1) is the impingement rate of atoms from the evaporation source and is given by Equation (2-7). The second term in Equation (4-1) is the rate of desorption of adatoms from the surface, and the third term

describes the capture of adatoms by stable islands from direct impingement from the vapor source and from surface diffusion of adatoms to the island edge.

Equation (4-2) describes the time rate of change of subcritical clusters. The equation is set equal to zero with the assumption of equilibrium between subcritical clusters, so that their net rate of formation is zero. A detailed balance analysis of the subcritical clusters leads to the conclusion that only islands at the critical size, n_i, contribute to the nucleation rate of stable islands, n_x. The result is given by the Walton[90] relation describing the net rate of formation of critical clusters

$$\frac{n_i}{N_o} \approx \left(\frac{n_1}{N_o}\right)^i \frac{n_1}{N_o} \exp\left(\frac{E_i}{k_b T}\right) \tag{4-7}$$

where E_i is the binding energy of adatoms in a critical size island.

Equation (4-3) describes the nucleation rate of stable clusters. The right hand side of Equation (4-3) describes the rate that critical size clusters capture an additional adatom that is diffusing on the surface. The capture of the adatom by a critical size island then converts it into a stable growing island, n_x. Solution of the coupled Equations (4-1) through (4-3) requires a solution for the capture numbers σ_i and σ_x.

The capture of adatoms by critical and stable islands requires a model for how adatoms diffuse on the substrate surface and attach to islands. Simplifications are made by assuming that the diffusive adatom flux on the surface can be described by a 'mean' diffusion field, giving rise to the descriptive term 'mean-field theory'. The true diffusion field varies with island size, so by assuming that each island exists in an average field of diffusing species means that island-island correlations are not accounted for. However,

for large ensembles of islands, the assumption of a mean diffusion field for each island should not greatly affect the average rates described in the coupled rate equations. Solution of a 2D mean diffusive field for both critical and stable islands leads to solutions for the capture numbers in the form

$$\sigma = \frac{2\pi X K_1(X)}{K_0(X)} \tag{4-8}$$

where K_1 and K_0 are modified Bessel functions and the argument X is $(r_k/D\tau_{des})$, where r_k is the radius of the island; $r_k = r_x$ for stable islands and $r_k = r_i$ for critical size islands in the expression for σ_x and σ_i, respectively.

The 2D diffusive flux occurring on the surface due to the capture of adatoms at the edges of existing islands leads to regions of reduced adatom concentrations around the islands. The regions that are partially depleted of adatoms are called nucleation exclusion zones, and are depicted in Figure 4-4.

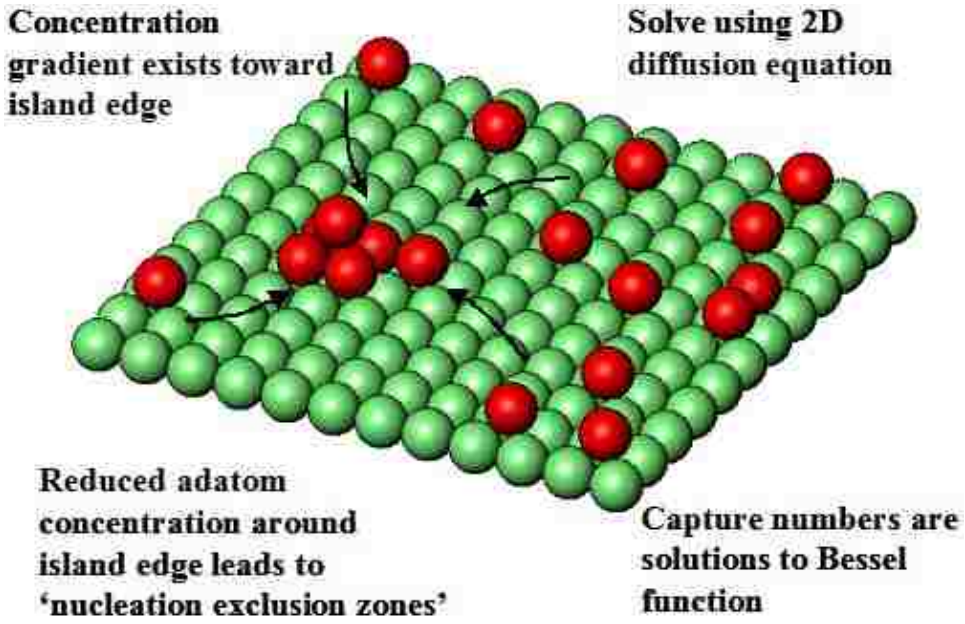


Figure 4-4. Illustration of the effect on the local adatom population due to a diffusive flux toward the island edge.

Analytical solutions of Equations (4-1) through (4-8) are made possible under conditions of steady-state nucleation for particular deposition conditions. The general solution for the maximum or saturation island density is given as

$$\frac{n_{x,\max}}{N_o} = \left(\frac{\Phi}{N_o \nu}\right)^p \exp\left(\frac{E_n}{k_b T}\right) \tag{4-9}$$

Expressions for the energy, E_n, and the exponent p are listed in Table 4-1 for the specific conditions of complete, initially incomplete, and extreme incomplete condensation.

Extreme incomplete condensation is associated with low desorption (E_{des}) and diffusion (E_{diff}) activation barriers. These low activation barriers lead to an extremely short characteristic surface diffusion length much less than the interdistance of nucleated islands. Thus, islands grow solely from direct impingement from the vapor. In

comparison, the initial incomplete regime is generally associated with high E_{des} but low E_{diff}. This regime exists when the nucleation density is sufficiently low, such that the characteristic diffusion length does not exceed the interdistance of nucleated islands, and therefore some of the diffusing adatoms desorb before reaching an island. However, once the saturation nucleation density is reached, the nucleated islands capture all diffusing adatoms. The third regime categorized as complete condensation is associated with extremely high E_{des} and/or extremely low E_{diff}, such that adatoms can diffuse until being captured by an island.

Regime	3D Islands	2D Islands
Extreme Incomplete	$p = 2i / 3$ $E_n = 2 / 3 [E_i + (i +1)E_{des} - E_{diff}]$	i $[E_i + (i +1)E_{des} - E_{diff}]$
Initially Incomplete	$p = 2i / 5$ $E_n = 2 / 3 (E_i + iE_{des})$	$i / 2$ $1 / 2 (E_i + iE_{des})$
Complete	$p = i / (i + 2.5)$ $E_n = (E_i + iE_{diff}) / (i + 2.5)$	$i / (i + 2)$ $(E_i + iE_{diff}) / (i + 2)$

Table 4-1. Expressions for the exponent p and energy E_n in Equation (4-9) that depend on the condensation regime and whether the islands are two or three-dimensional.

Depending on the regime of condensation and the island morphology described above, natural log of the saturation number density of islands can be plotted against $1/T$ to extract E_n associated with desorption (E_{des}) and diffusion (E_{diff}) of Ge as well as lateral binding energy (E_i) of adatoms in the critical nuclei. Atomistic nucleation theory has undergone a significant amount of testing since its development to determine its validity.

Nucleation theory of thin films deposited from the vapor has a long history and originated from metal nucleation studies, eventually leading to semiconductors. Early

work was focused on Au deposition onto alkali halide substrates.[91-93] While providing qualitative confirmation of the theory, early nucleation studies on alkali halide substrates were complicated by the formation of defects on the substrate caused by stray electrons emitted from the deposition source. These defects caused additional nucleation to occur on the substrate during the deposition.[94] More recently, Schmidt *et al*.[95] studied the nucleation of several metals on amorphous SiO_2 films and found that their nucleation behavior agreed with nucleation theory. In general however, metal nucleation on insulating substrates appears to be dominated by surface defects, especially at low deposition temperatures.[96-98] Following the metal-insulator studies, metal-metal and metal-semiconductor systems were studied and found to differ in nucleation energetics and behavior from insulating substrates.[99]

These early nucleation studies are examples of VW or SK growth, during which nucleation densities are measured by either SEM or TEM. With the advent of scanning tunneling microscopy (STM), nucleation and island growth are studied at the atomic level with sub-monolayer sensitivity, and much insight is gained into the fundamental processes of 2-D atomic motion on surfaces. The use of STM provides the opportunity to test nucleation theory at the atomic level. Explicit measurement of critical nucleus sizes and the flux dependence of the stable island density quantitatively validated the rate equation approach to modeling nucleation of thin films.[99-105] Complementing the STM work, Monte Carlo simulations have also confirmed that the rate equation approach is an accurately quantitative description of the nucleation process.[106] Although measurements using low-temperature STM are more precise than those inferred from SEM using

nucleation theory, the STM cannot be used on insulating substrates. Thus, we use SEM in this work to measure nucleation densities of Ge on SiO_2.

In previous studies of metal and semiconductor growth on insulators, island growth is generally observed due to low surface energy of the insulators, and this is also the case for Ge-SiO_2 at typical growth temperatures (673 to 923 K) used in our experiments. In addition, these systems are characterized by small E_{des} and E_{diff}. For example, for Ag on SiO_2, Poppa estimates the desorption energy as 0.52-0.43 eV.[107] Specifically for Ge on SiO_2, Li *et al*.[108] reported 0.44 ± 0.03 eV for an experimentally measured desorption activation energy of Ge from SiO_2. In the present study, we extend the measurement of Ge nucleation on SiO_2 over a much broader range of temperatures and deposition rates and extract the critical nucleus size, cluster binding energy, and surface diffusion energy of Ge on SiO_2 from the rate equation approach to nucleation. Preparation of the samples for nucleation experiments of Ge on SiO_2 are described next.

4.4.1 Experimental Details

For SiO_2 sample preparation, Si (001) wafers are first cleaved into narrow strips of 1 cm *w* x 5 cm *l* pieces. The Si wafers are doped with boron with a resistivity of 1 – 10 Ω-cm. The cleaved samples are cleaned in a Piranha bath consisting of 3 volumetric parts H_2SO_4 (96 wt%) to 1 part of H_2O_2 (30 wt%). The samples are subsequently dipped into a buffered oxide etch solution (20 parts 40 wt% NH_4F: 1 part 49 wt% HF) diluted in deionized (DI) water by 6:1 volumetric ratio to remove the chemical oxide. The chemical oxidation and etching process is repeated twice. The samples are dried with N_2 and then loaded into a dry oxidation furnace, in which 100 nm of oxide is grown at 1423

K. Before Ge deposition, the samples are again cleaned in Piranha and dipped into a dilute HF solution for 10 sec. The dilute HF is made by mixing 20 volumetric parts of DI water with 1 part of 49 wt % electronic grade HF solution. After the HF dip, which removes approximately 1 nm of the thermally grown SiO_2, the samples are rinsed in DI water and dried with N_2 gas. After being loaded into the deposition chamber, the samples are degassed at 873 K for 10 min. The effusion cell is set to the desired temperature and allowed to stabilize for 30 min. The substrate heater is then set to the deposition temperature and allowed to stabilize for 5 min. The shutter is subsequently opened for deposition, while the deposition time is recorded. The pressure in the chamber remains below $1x10^{-8}$ Torr during the deposition.

After deposition, the Ge nucleation density is counted *ex situ* from SEM images. The microscope is a JEOL 6400F capable of ~10 nm resolution. The samples are sputter coated with 5 nm of Au to prevent charging of the SiO_2 surface during SEM imaging and to enhance the resolution and contrast of Ge islands. Eight images are recorded across the sample in plan-view geometry to provide reliable counting statistics for nucleation densities. The island densities vary by 2 to 4 times from center to edge of the samples. Sample edges are more prone to variation due to possible contamination from cleaving and sample handling. Thus, we limit our counting to 8 locations near the center along the 5-cm strip to minimize edge effects. Figure 4-5 shows representative SEM micrographs where the island nucleation density decreases with increasing substrate temperature at a fixed flux of $4.2\ x10^{14}$ atoms cm^{-2}-s^{-1} (40 ML min^{-1}). The islands appear semicircular and are randomly distributed across the surface.

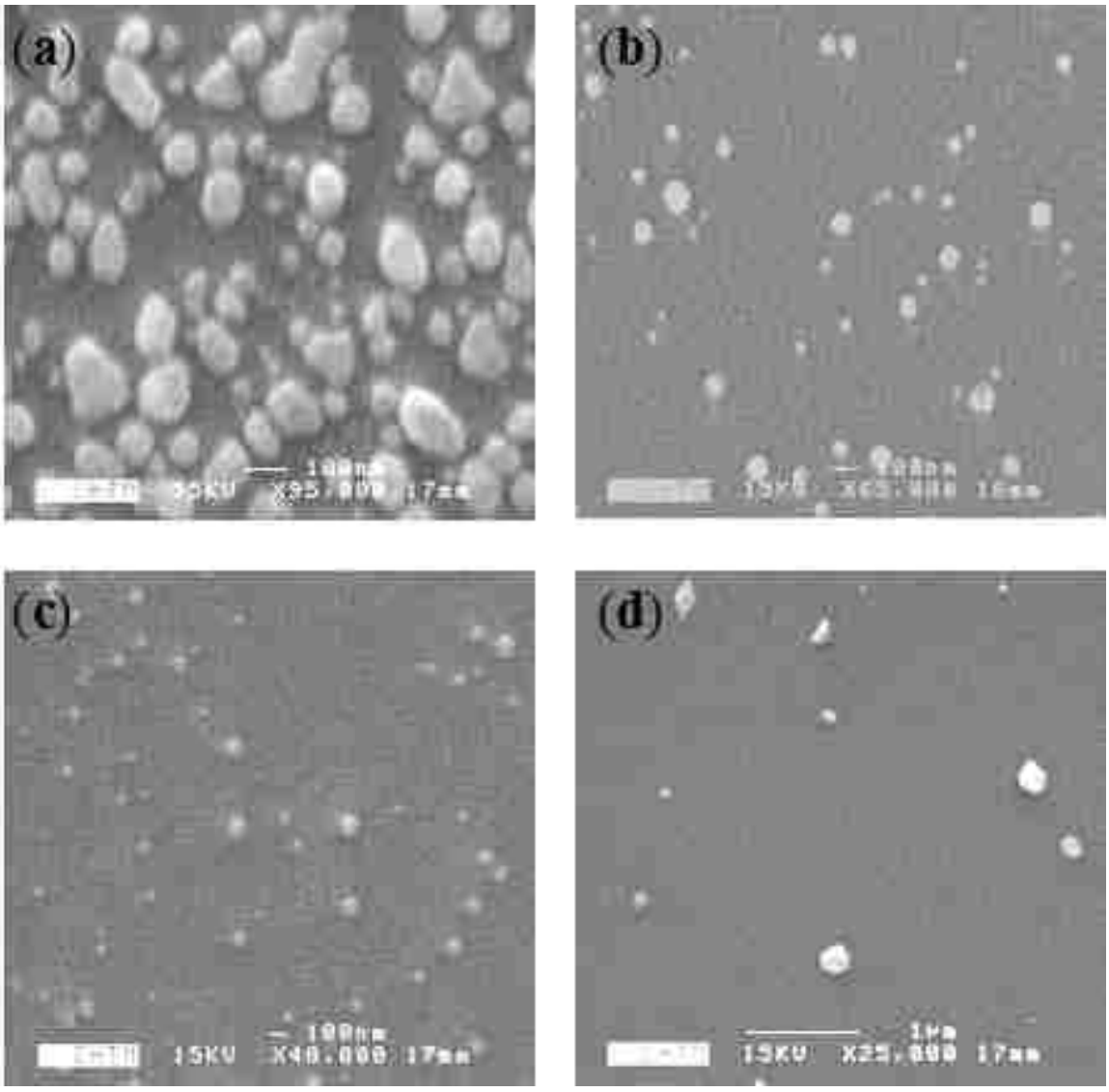


Figure 4-5. Scanning electron micrographs of Ge islands on SiO_2 at saturation island density at a flux of 4.2 x 10^{14} atoms cm^{-2}-s^{-1} (40 ML min^{-1}) with increasing substrate temperature: 4-5(a) T_{sub} = 673 K and 80 ML exposure, 4-5(b) T_{sub} = 723 K and 200 ML exposure, 4-5(c) T_{sub} = 773 K and 400 ML exposure, and 4-5(d) T_{sub} = 823 K and 800 ML exposure.

4.4.2 Results and Discussion

The number of Ge islands nucleated on the SiO_2 is a function of substrate temperature T_{sub}, deposition rate R, and time t. Nucleation density measurements are made over substrate temperatures from 673 to 973 K and deposition rates from 6.9 x 10^{14}

atoms cm^{-2}-s^{-1} (65 ML min^{-1}) to 5.1 x 10^{13} atoms cm^{-2}-s^{-1} (5 ML min^{-1}). Figure 4-6 shows the time dependence of the nucleation density at a fixed deposition rate for several substrate temperatures.

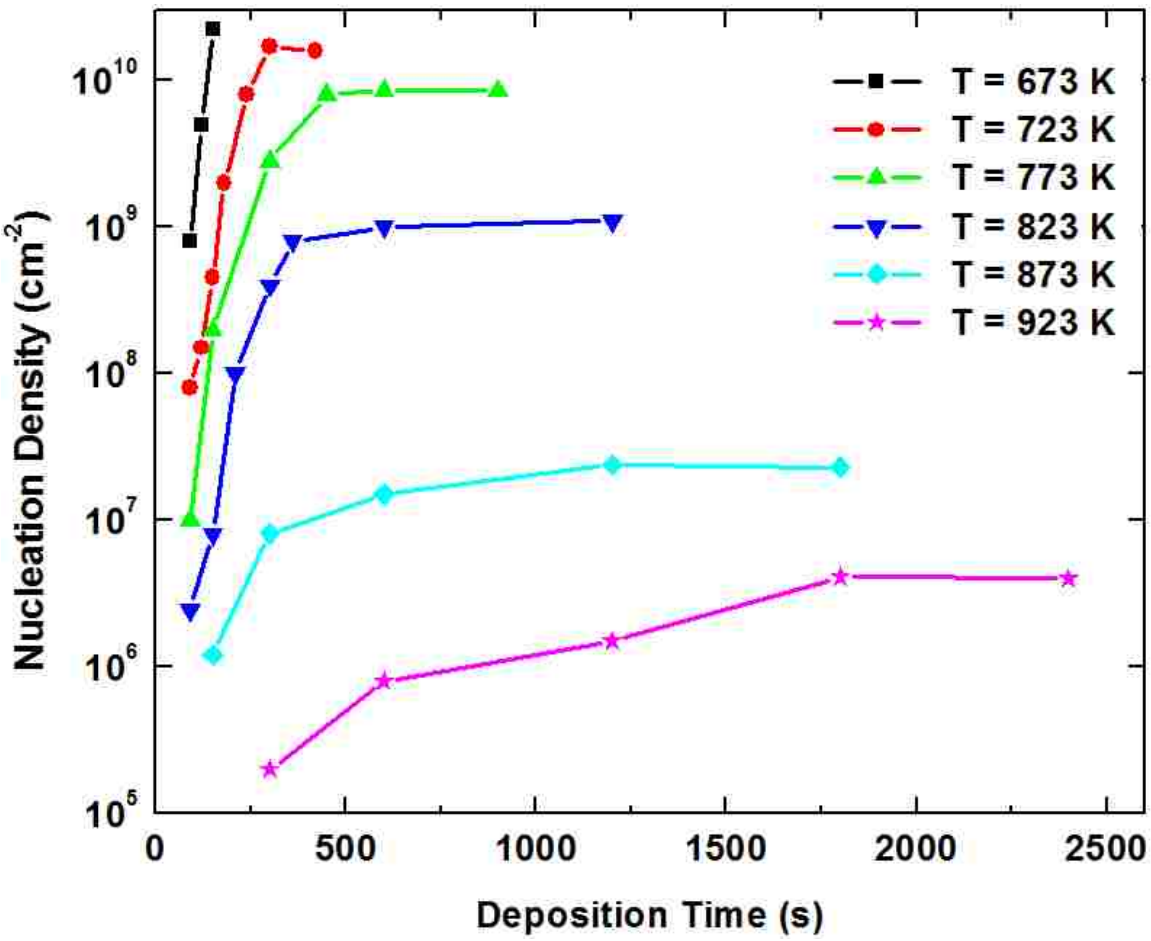


Figure 4-6. Nucleation density versus time for flux of 4.2 x 10^{14} atoms cm^{-2}-s^{-1} (40 ML min^{-1}) for several substrate temperatures. The time to reach the saturation island density increases with increasing temperature and occurs well before island coalescence except at the lowest measured substrate temperature of 673 K.

The time to reach the saturation nucleation density decreases with decreasing substrate temperature and increasing deposition rate. Qualitatively, at low temperatures, a larger number of Ge adsorbates exist on SiO_2 surface to form islands, and therefore a larger

overall nucleation density. This in turn is likely to cause the system to reach the saturation density much more quickly than at elevated temperatures. The saturation nucleation density can be described by the Equation (4-9).

Natural log of the saturation nucleation density versus $1/T_{sub}$ is shown in Figure 4-7 and found to vary by over 5 orders of magnitude.

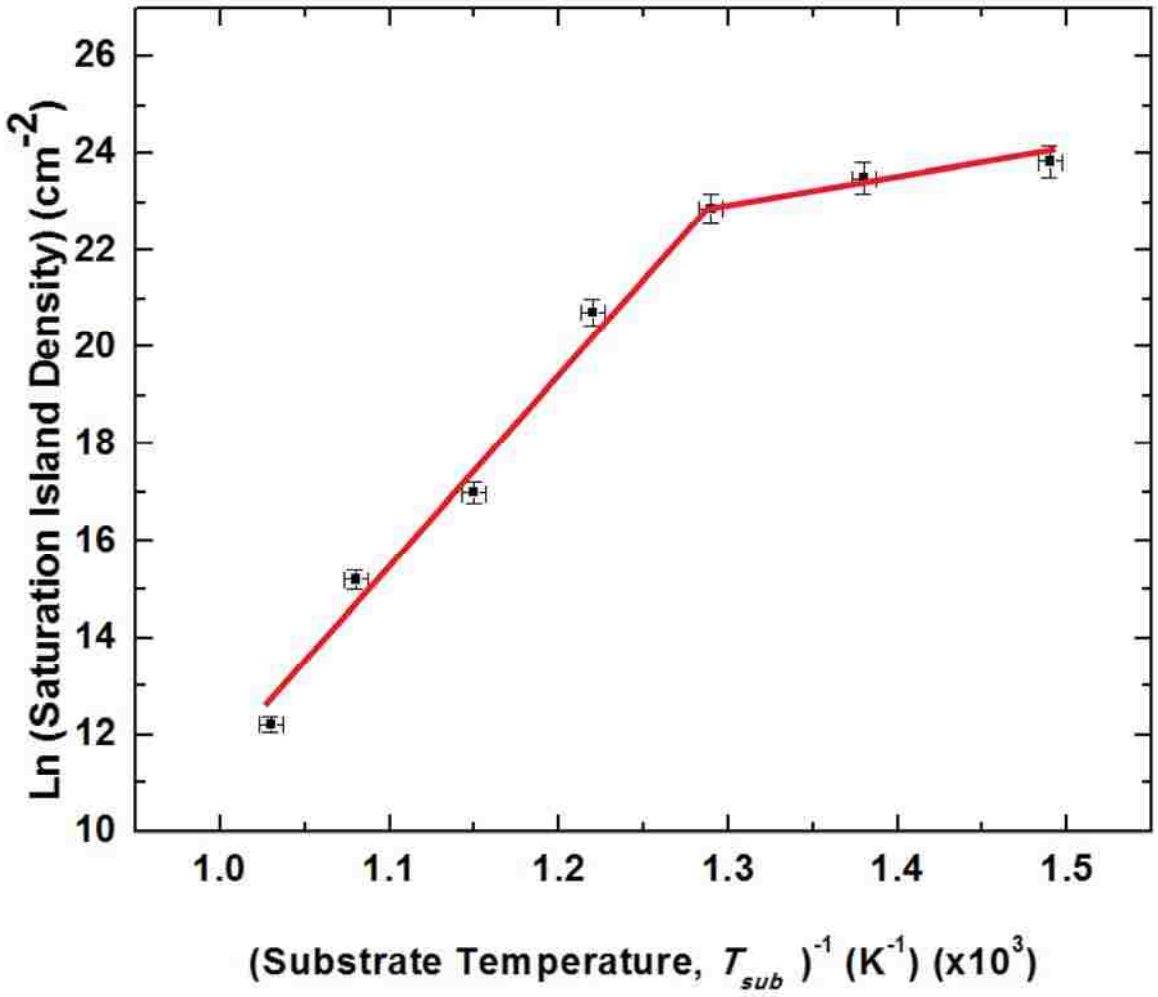


Figure 4-7. Natural log of the saturation nucleation density versus reciprocal substrate temperature. This plot reveals two distinct slopes that occur over the temperature intervals of 673 to773 K and 773 to 973 K, and this graph is used to extract the activation energies involved in the nucleation process.

Two different slopes appear in the data: one from 673 to 773 K and one from 773 to 973 K. The discontinuity in the slope may stem from a change in the critical nucleus size (i) or from a transition in the regime of Ge condensation on SiO_2. To delineate the cause of this discontinuity, the level of Ge condensation is first characterized by integral condensation coefficient (α), which is a ratio of total mass of Ge condensed to total mass of Ge impinged on the surface.

The integral condensation coefficient, α, is estimated by first measuring the island diameter for each island in a micrograph in two perpendicular directions and then calculating the arithmetic average. Next, we assume hemispherical shapes to calculate the amount of Ge condensed versus the amount impinged from the effusion cell. Figure 4-8 shows α versus t for several substrate temperatures for a fixed deposition rate.

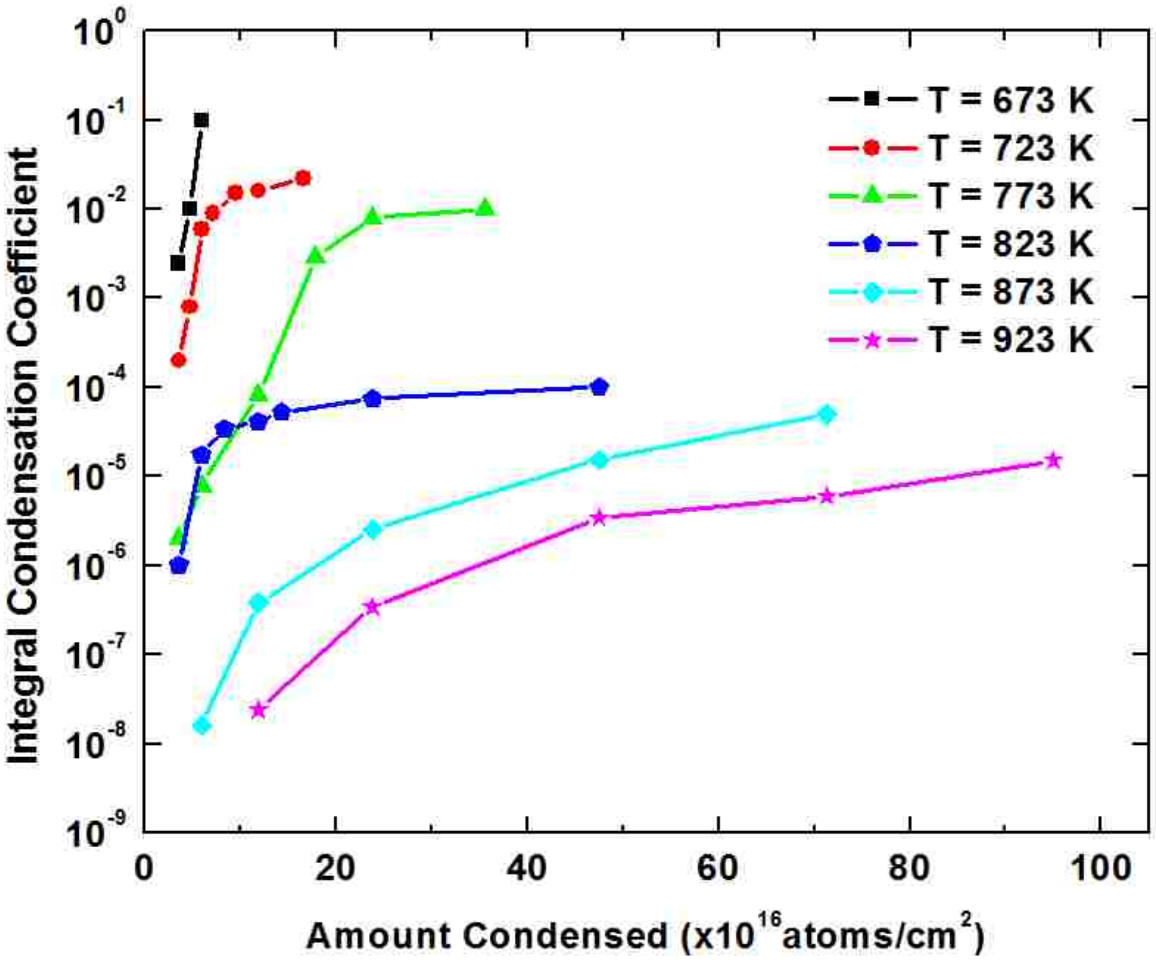


Figure 4-8. Integral condensation coefficient, α, is estimated from scanning electron micrographs and plotted against time for several substrate temperatures. Values of α are less than 0.1 even at the lowest measured substrate temperature of 673 K, and are much less than one even after reaching the saturation island density at higher temperatures. This indicates that condensation is extremely incomplete over the range of substrate temperatures investigated.

We observe that α does not exceed 0.1 even at the lowest substrate temperature of 673 K even after reaching the saturation nucleation density. From this observation, we conclude that the condensation regime is extremely incomplete over the entire experimental range. Moreover, we deduce that the slope change occurring at 673 K in Figure 4-7 is due to a change in the critical nucleus size (i).

To measure (i), natural log of saturation island density (N) is plotted versus natural log of deposition flux (R) at a fixed substrate temperature. Figure 4-9 shows this data measured at 723 and 773 K.

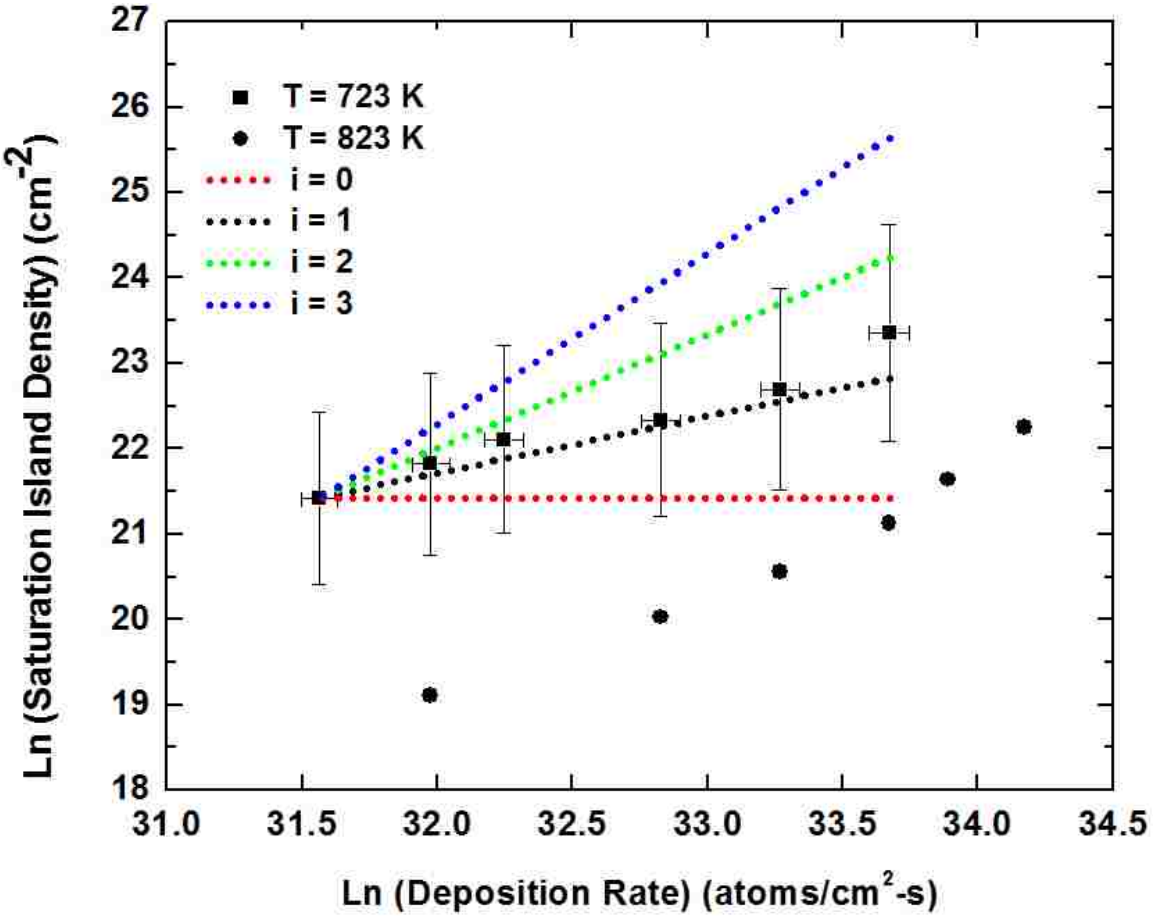


Figure 4-9. Natural log of the saturation density versus deposition rate used to determine the critical nucleus size, i, for the low and high temperature slopes shown in Figure 4-8. Broken lines indicate the slopes expected for different values of i under extreme incomplete condensation.

These substrate temperatures lie on either side of the discontinuity in slope in Figure 4-7. Linear regression is conducted on ln(N) vs. ln(R), whose slope yields the exponent p according to Equation (4-7). In the case of extreme incomplete condensation,[89]

$$p = 2i/3, \text{ and} \tag{4-10}$$

$$E_n = \frac{2}{3}\left[E_i + (i+1) E_{des} - E_{diff} \right] \tag{4-11}$$

where E_i is the binding energy of the critical nucleus relative to i isolated atoms. The linear regression yields a value of $p = 0.8 \pm 0.1$ at 723 K and $p = 1.4 \pm 0.2$ at 773 K. For the 723 K case, we calculate i to be approximately 1. However, $i = 2$ also results in a slope that traces the experimental data within the margin of experimental error. Therefore, the values of p are consistent with a range of i values from 1 to 2 at 723 K and 2 to 3 at 773 K, respectively. In the following section, we will show that E_n extracted from Figure 4-7 places a limit on i, which in turn must be consistent with E_i. That is, E_i and i are inter-dependent in Equation (4-9). As shown next, the form of E_n and its measured values for the two temperature intervals in Figure 4-7 allow us to deduce the exact value of i for both intervals. However, to determine i and E_{diff}, we first use, as an upper limit for E_i, the free-vacuum binding energy of the critical nucleus size for Ge dimers and trimers.

Measurements of free-vacuum cluster binding energies for Ge dimers and trimers have been made using a mass spectrometry technique with values of 2.65 and 6.24 eV, respectively.[109] We expect these Ge-Ge binding energies to be smaller for Ge clusters adsorbed onto SiO_2, as Ge forms bonds with the underlying substrate. Therefore, the free-vacuum binding energies represent an upper limit to the true binding energy. These binding energy estimates, along with the measured values for E_n, are used to determine the value of i for each temperature interval. For the low temperature interval (673 – 773 K), the only value of i consistent with the data is $i = 1$, leading to a result $2E_{des} - E_{diff} = 0.65 \pm 0.02$ eV. Using $E_{des} = 0.44 \pm 0.03$ eV that we had experimentally determined

using x-ray photoelectron spectroscopy, leads to a value for E_{diff} = 0.24 ± 0.05 eV. Similarly, the only possible value for *i* in the high temperature interval (773 – 973 K) is *i* = 3. Using the above values for E_{des} and E_{diff} leads to the value $E_{i=3}$ = 3.7 ± 0.1 eV for a surface adsorbed trimer. This value for $E_{i=3}$ is considerably lower than the free-vacuum binding energy of 6.24 eV. However, consider a Ge trimer with three bonds to the underlying SiO_2. Assuming that the binding energy of the free-vacuum cluster is equal to the total binding energy of the surface-adsorbed cluster, which includes three Ge-SiO_2 bonds, $3E_{des} + E_{i=3}$ = 6.24 eV. Using E_{des} = 0.44 ± 0.03 eV yields a value for $E_{i=3}$ of 4.9 ± 0.1 eV. This qualitative estimate is only meant to demonstrate the reasonableness of the calculated value for $E_{i=3}$. Due to the imprecise structure of the amorphous SiO_2 surface, and the unknown configuration of a Ge trimer adsorbed onto this surface, we cannot speculate further about the accuracy of the measured value for $E_{i=3}$.

Based on the experimentally measured E_{des} and E_{diff}, we consider the implications of the measured activation barriers on selective growth. The average distance, $\overline{X}$, that Ge adatoms migrate on the surface before desorbing is equal to[110]

$$\overline{X} = \left[\frac{1}{2 N_o^{1/2}} \exp\left(\frac{E_{des} - E_{diff}}{2 k_B T_{sub}} \right) \right] \qquad (4\text{-}12)$$

We estimate N_o to be 1 x $10^{15}$$cm^{-2}$ based on the structure and bond lengths between oxygen atoms in α-quartz[111] and assuming that each SiO_4 tetrahedron provides a potential adsorption site. Inserting the measured values for E_{des} and E_{diff} results in a migration distance of only 0.9 ± 0.3 nm at 673 K and 0.5 ± 0.2 nm at 973 K. Given these low

diffusion distances for Ge adatoms, we expect that the selective growth occurring on a patterned substrate is due to the short adatom lifetime on the oxide surface. This conclusion is a correction to our previous work in which we suggested that selective growth occurs by Ge adatom diffusion to the openings in the SiO_2 mask.

Figure 4-10 shows an oxidized Si sample with a patterned window density of 6×10^6 cm^{-2} where the windows are etched down to the Si substrate. The top micrograph represents a templated Si substrate at 673 K exposed to a Ge flux of 4.2×10^{14} atoms cm^{-2}-s^{-1} (40 ML min^{-1}) and shows extensive random nucleation on the oxide, as well as growth inside the windows.

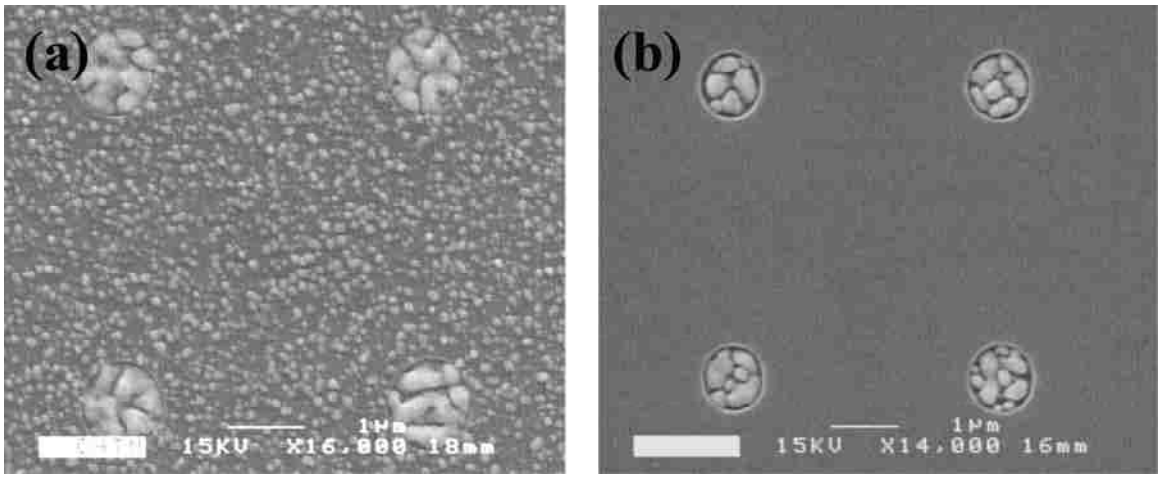


Figure 4-10. Scanning electron micrograph showing the highly selective growth achieved for a three micron separation between mask openings at 873 K, but random nucleation occurring at 723 K. Deposition flux is 4.2×10^{14} atoms cm^{-2}-s^{-1} (40 ML min^{-1}) in both images.

The sublimation energy for Ge on Si (001) has been estimated to be 4.25 eV;[73,112] therefore, we expect nearly all the Ge to stick to Si exposed inside the windows. If the characteristic diffusion length of Ge on SiO_2 were longer than the window pitch, the

rapid nucleation of Ge on Si should produce a nucleation exclusion zone (or area of reduced Ge adatom concentration) around the periphery of each opening. However, no such exclusion zone is detectable in Figure 4-10 (a), in support of the calculated short diffusion lengths for Ge on SiO_2. Additionally, the random nucleation density on the oxide is the same as that on an unpatterned sample. This result is also expected if the average surface diffusion length of Ge adatoms on the oxide is much less than the distance between openings in the oxide. Lastly, we plot the saturation nucleation density as a function of substrate temperature and deposition rate to provide a guide for deposition conditions that favor highly selective growth (Figure 4-11).

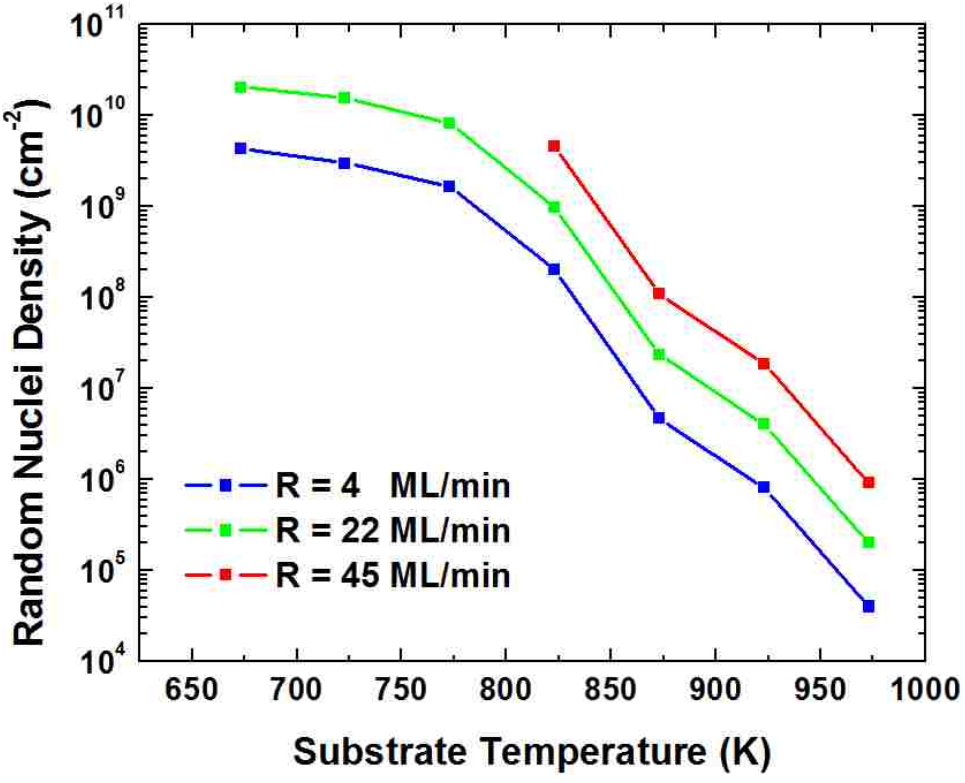


Figure 4-11. Numbers of random Ge nuclei occurring on the SiO_2 are shown versus substrate temperature for different deposition rates.

Figure 4-11 shows the number of random Ge nuclei obtained for a given substrate temperature and flux. Since random Ge nucleation is suppressed at high temperatures but not fully eliminated, it is not possible to demarcate a region of selective versus nonselective growth. Rather, Figure 4-11 can be used to choose deposition conditions that will produce a minimal number of random nuclei. Additionally, it is possible that an amount of random nucleation below the detection limit of the SEM occurs at defect sites on the mask surface. However, the observation that the random nucleation density continues to decrease precipitously without a plateau in Figure 4-11 as a function of increasing substrate temperature indicates that the defect-induced random nucleation is likely to be minimal in the temperature range explored in this work.

4.4 Conclusions of Ge Nucleation on SiO_2

The saturation nucleation density of Ge islands on SiO_2 during MBE growth is measured and used to determine the optimal growth conditions for selective growth on patterned samples. The nucleation measurements and mean-field theory are combined with our previously measured desorption activation energy to determine the size and binding energy of the critical nucleus and activation energy for surface diffusion. The small desorption and surface diffusion activation barriers lead to extremely short adatom lifetimes and diffusion lengths on the SiO_2 at elevated growth temperatures, leading to selective growth on window-patterned samples. In contrast, Ge strongly binds to Si such that the growth occurring inside the windows on patterned samples progresses mostly by direct impingement from the vapor and subsequent lateral diffusion within the holes. This result is confirmed by two observations made on the patterned samples: (1) the lack

of nucleation exclusion zones around the window openings and (2) the independence of the random Ge nucleation density occurring on the oxide surface on patterned versus unpatterned samples.

CHAPTER 5 NUCLEATION OF GERMANIUM WITHIN NANOSCALE OPENINGS IN SILICON DIOXIDE

5.1 Introduction and Background

The theory of stress reduction using nanoheteroepitaxy and the possibility to grow dislocation-free GoS is reviewed in Chapter 1. The method under current investigation to improve the GoS film quality is the nucleation of Ge islands within nanoscale windows in a thin layer of chemically grown SiO_2 and successive island coalescence over the SiO_2.

The density of small openings that form in the SiO_2 layer is greater than 10^{11} cm^{-2}, and these openings result from exposure to a Ge flux at elevated temperatures. Epitaxial Ge islands then selectively nucleate within the openings in the SiO_2. Continued growth leads to the formation of larger islands that coalescence over the remaining SiO_2 template until eventually a continuous Ge layer is formed.

Shklyaev *et al.*[81] were the first to demonstrate the technique of Ge nucleation through nanometer openings in SiO_2. Shklyaev and others have pursued this technique for quantum dot[113-116] and memory applications;[117,118] however, our group was the first to apply this method to obtain low TDD Ge films on Si.[55,58,59] Luryi and Suhir developed the theoretical analysis of Ge growth within the nanometer-sized openings in SiO_2, and its potential to produce low TDDs, as reviewed in Chapter 1.[64] The two specific requirements that must be met for dislocation-free growth of Ge on Si are as follows: 1) Ge island diameter should be less than 10 nm, and 2) Ge islands should be spaced by more than 3 nm apart.[64] Later analyses using finite element modeling of Ge islands on Si largely confirm these findings and show that Ge islands deform outward to enhance strain

relaxation.[60-62] The specific requirements for dislocation-free growth of Ge on Si are met by the process of Ge nucleation through nanometer-sized openings in chemical SiO_2.

5.2 Experimental Details

The Si substrate consists of a 2-inch wafer doped with boron with a resistivity of 1 – 10 Ω-cm. The Si wafers are cleaned for 5 min in a Piranha bath consisting of 3 volumetric parts H_2SO_4 (96 wt %) to 1 part of H_2O_2 (30 wt %) and heated to 373 K. The heated Piranha bath results in a slightly thicker oxide but a more consistent thickness compared to our previous chemical oxidation procedure done at 353 K.[58,59] The samples are subsequently dipped into a buffered oxide etch solution (20 parts 40 wt% NH_4F: 1 part 49 wt% HF) diluted in DI water by 6:1 volumetric ratio to remove the chemical oxide. The chemical oxidation is then repeated, and the wafer is rinsed in DI water and blown dry with N_2. After being loaded into the deposition chamber, the samples are degassed at 873 K for 10 min. The effusion cell temperature is set to produce a flux of 1.9×10^{14} atoms cm^{-2}-s^{-1} (19.1 ML min^{-1}) and allowed to stabilize for 30 min. The shutter is subsequently opened for deposition, while the deposition time is recorded. A total of 100 nm of Ge is deposited, and then the deposition rate is increased to 60 ML min^{-1} until a film thickness of 3.5 μm is reached. The pressure in the chamber remains below 1×10^{-8} Torr during the deposition.

Samples that undergo annealing at an early stage of Ge growth follow the same procedure described above, up to the step before the shutter is opened to begin deposition. Four samples are produced with an equivalent amount of 8, 12, 18, and 25 nm of Ge deposition, assuming all Ge sticks to the surface. A second set of samples is

then produced with identical Ge depositions, but which undergo annealing under vacuum after the deposition. For samples in which Ge islands are annealed, the shutter is subsequently closed after deposition, and the substrate temperature is raised to 1073 K for 30 min. This anneal step is previously reported to lead to Ge films free from twins upon further Ge growth at 853 K after the anneal step.[55]

Ge/SiO_2 template/Si samples are polished using a Logitech PM5 lapping/polishing machine on a Logitech Chemcloth polishing pad. The polishing solution consists of 50 parts DI water and 1 part 30 wt% H_2O_2. Afterward, the wafers are rinsed in DI water and cleaned for 10 min in a capacitively coupled plasma reactor operating at 250 watts and 1 Torr with 30 sccm O_2 flow rate.

The integration of III-V layers consisting of GaAs and AlGaAs is performed at National Renewable Energy Laboratory (NREL) and at Sandia National Laboratories (SNL). The NREL growth consists of a 10-period superlattice of GaAs and $Al_{0.2}Ga_{0.8}As$ layers. The first layer is GaAs, and each layer is 50 nm thick except for the last 100 nm thick $Al_{0.2}Ga_{0.8}As$ layer. This is followed by 1500 nm of GaAs, 200 nm of $Al_{0.2}Ga_{0.8}As$, and finally a 10 nm thick GaAs cap. The III-V growth performed at NREL is done in an atmospheric pressure metal-organic vapor phase epitaxy (MOVPE) reactor, using trimethylgallim (TMG), trimethylaluminum (TMA), and arsine delivered in H_2. The samples are first annealed at 973 K for two minutes under 1.2 Pa of arsine. The temperature is then reduced to 923 K for growth. All $Ga_{0.8}Al_{0.2}As$ layers are grown at a rate of 2.3 μm/hr and V/III inlet ratio of 70. All GaAs layers are grown at 1.8 μm/hr with V/III inlet ratio of 86. The SNL growth stack consists of 50 nm of GaAs, 100 nm of $Al_{0.2}Ga_{0.8}As$, and followed by 1000 nm of GaAs. The III-V growth performed at SNL is

done using MOVPE in a Veeco D125 system. Immediately before GaAs growth, the wafers are rinsed in DI water followed by a 30 s dip in a dilute HF solution (1 part 49 wt. % HF: 100 parts DI water). The wafers are first degassed at 373 K for 30 min and then heated to 973 K to remove Ge surface oxide. The growth precursors TMA, TMG, and arsine are delivered in an H_2 ambient. For AlGaAs growth, the deposition occurs at 923 K with partial pressures of 0.9 mTorr TMA, 2.1 mTorr TMG, and 0.4 Torr arsine. Control samples for NREL and SNL III-V growth consist of 2-inch 6° offcut Ge substrates manufactured by AXT and are Ga doped to a resistivity of 0.016-0.022 Ω-cm.

The SEM imaging is performed on an FEI Quanta 3D operating at 30 kV. The AFM imaging is done using a Park Scientific Instruments Autoprobe CP operating in non-contact mode. Both STEM and TEM images are collected on a JEOL 2010F and JEOL 2010, respectively, operating at 200 kV. The TEM samples of Ge islands and III-V films on Ge are prepared using the FIB apparatus of the FEI Quanta 3D. The composition of the annealed Ge islands is performed using Nanoprobe EDS in STEM mode on the JEOL 2010F using a 1 nm spot size. The x-ray signal is collected using an Oxford Instruments SiLi drift detector with an ultra-thin window.

Mechanical polishing is used to prepare the x-TEM samples of Ge films followed by ion milling. The pv-TEM samples are prepared by chemically removing the Si substrate in a 30 wt % solution of KOH and DI water heated to 313 K. The free-floating Ge film is then rinsed in DI water and thinned to electron transparency using a Gatan PIPS ion polisher. An Omicron SEM operating at 5 kV with a 5 nm spot size is used to collect CL images at SNL. The detector is a Gatan MonoCL2 of Cs:GaAs having a detectable wavelength range below 890 nm. Additional CL spectrum imaging

measurements at 300 K and 15.5 K are made at NREL using an SEM operating at 15 kV and 500 pA with a Si detector. Time-correlated single photon counting is employed in the collection of the time resolved PL spectra. A Ti:Sapphire laser producing 200 fs pulses at 250 kHz repetition rate is used as the excitation source. The excitation wavelength is 750 nm with average power of 0.5 mW and beam diameter of 0.5 mm. The detector is a Hamamatsu near infrared-sensitive photomultiplier tube used to collect measurements at 870 nm.

5.3 Results and Discussion

The thickness of SiO_2 chemically formed from the 100 °C Piranha solution is 1.4 nm as measured in the STEM image in Figure 5-1.

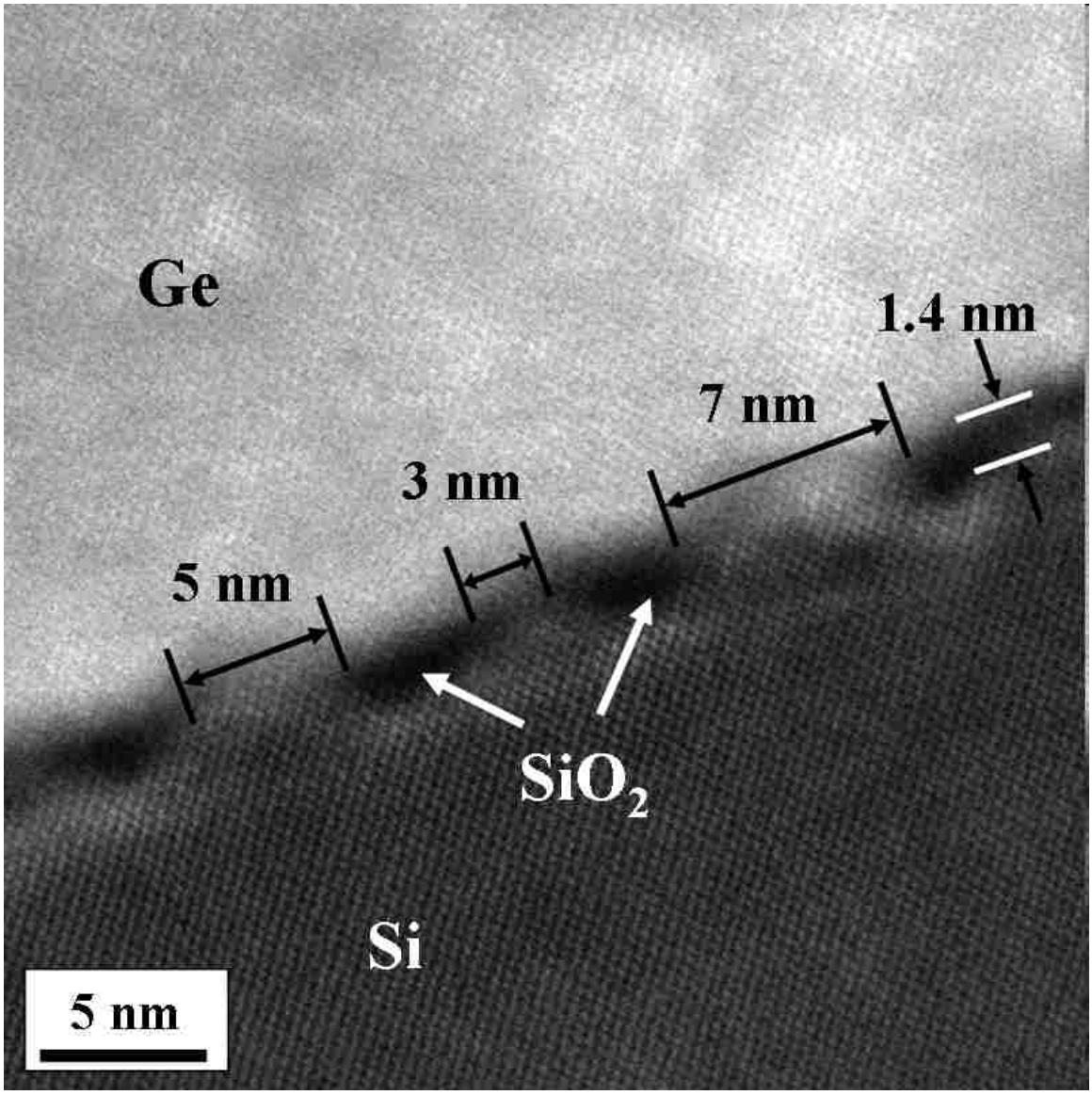


Figure 5-1. High resolution cross-sectional scanning transmission electron micrograph showing the Ge/SiO_2/Si interface. Voids of 3 to 7 nm in diameter are created in the SiO_2 where Ge subsequently nucleates and grows as islands. The islands eventually coalesce into a continuous film overgrowing the remaining oxide.

This figure shows a cross-sectional view of the Ge-Si interface after nanoscale Ge islands form within the openings in the thin SiO_2 layer and subsequently coalesce over the oxide. STEM provides elemental contrast based on atomic weight, where heavier elements scatter more electrons into the detector. Thus, epitaxial Ge appears brightest at the top of

the image, whereas Si appears darker and is shown at the bottom. Oxygen atoms contained in the remaining SiO_2 scatter the least; therefore, remaining SiO_2 appears as the dark broken line at the Ge-Si interface. The STEM image shows the high density of 3 to 7 nm wide openings in the SiO_2 and the Ge-Si epitaxial registry at the heterojunction within the oxide openings. Additionally, a thin GeSi interdiffusion layer of 2 nm is faintly visible beneath the oxide layer. In addition, EDS spectra are collected (not shown here) and further verify the elemental composition of the Si, Ge, and SiO_2 near the interface. The above interfacial architecture is maintained across the 2-inch-diameter wafer for proper scale-up of the growth technique we have developed.

5.3.1 Mechanism of Nanoscale Window Formation

The mechanism that creates openings in the oxide and allows epitaxial Ge island formation is still not completely understood. However, a sizeable body of work[119-138] has been done on the thermal decomposition of thin layers of SiO_2, substantiating some of the mechanism's elementary steps. First, the thermal decomposition of SiO_2 in an oxygen deficient atmosphere at elevated temperatures is believed to occur via the overall reaction:[139]

$$Si(s) + SiO_2(s) \rightarrow 2SiO\ (g) \qquad (5\text{-}1)$$

Tromp *et al.*[131] first showed that this reaction does not occur uniformly across the oxide surface. Rather, the reaction occurs inhomogeneously, leading to a random array of openings in the oxide. These openings then grow as Si diffuses to and reacts with SiO_2 at the periphery of the openings. Using isotopically labeled O_2^{18} with thermal desorption

mass spectroscopy , Sun *et al.*[137] demonstrated that the decomposition of the SiO_2 begins at the SiO_2-Si interface. The above observations lead us to postulate the following elementary steps to nucleate voids at the Si-SiO_2 interface:

$$SiO_2\text{–Si defect } (I) + SiO_x\ (I) \leftrightarrow SiO\ (I) \tag{5-1a}$$

$$SiO\ (I) \rightarrow SiO\ (S) \tag{5-1b}$$

$$SiO\ (S) \rightarrow SiO\ (g) \tag{5-1c}$$

where *I* stands for interface, *S* is surface, and *g* is gas phase. Equation (5-1a) represents a reaction between sub-stoichiometric oxide that exists in a thin layer at the SiO_2-Si interface [for a review see Ref. [140]] and interface defect sites. For oxides thicker than 1 monolayer, Equation (5-1b) describes SiO diffusion from the interface to the SiO_2 surface. Lastly, Equation (5-1c) describes SiO desorption from surface to vacuum. The exact defect sites where the SiO_2 decomposition begins are still unknown, but at least two possible candidates have been identified. Poindexter *et al.*[141] used electron spin resonance spectroscopy to determine that approximately 10^{12} cm^{-2} dangling bond defects (called P_{b0}) occur at the SiO_2–Si interface. Another possibility is interstitial silicon point defects that occur to minimize strain at the interface from the volume expansion during the oxidation.[142-147]

Once voids are nucleated at the SiO_2–Si interface, they grow by consumption of substrate Si. Johnson *et al.* have proposed the following model for the void growth:[145]

$$Si\ (L) \leftrightarrow Si\ (m) \tag{5-1d}$$

$$\text{Si}\ (m) \leftrightarrow \text{Si}\ (P) \tag{5-1e}$$

$$\text{Si}\ (P) + \text{O}\ (P) \leftrightarrow \text{SiO}_x\ (P) \tag{5-1f}$$

$$\text{SiO}_x\ (P) \rightarrow \text{SiO}\ (g) \tag{5-1g}$$

where *L*, *m*, and *P* represent lattice site, surface monomer, and sites at the void periphery, respectively. Equation (5-1d) describes the formation of a Si surface monomer from the lattice-site Si. In Equation (5-1e), a Si monomer diffuses to the void periphery, where it can react with O to produce SiO_x in Equation (5-1f). Lastly, Equation (5-1g) corresponds to desorption of SiO from surface to vacuum. Modeling of the void size with annealing time indicated that Si monomer formation in Equation (5-1d) is the rate-limiting step in their proposed mechanism.[145] Johnson measured an activation energy of 3.64 eV in qualitative agreement with the formation energy of Si adatoms from the Si lattice.[145]

Several researchers have also found that SiO_2 decomposition in the presence of a Ge[59,119,121,130,132,134] or Si[122,132,135] atom flux, or other metal impurities (e.g., Au, Ag, Cu, W, Ni, Pt, Ti, Mg, Al)[148,149] occurs faster and at lower temperatures than in their absence. Figure 5-2 captures this reduction in decomposition temperature upon Ge impingement for different SiO_2 thicknesses. The figure includes data taken from several studies,[119-138] including the present authors' (▲), and plots natural log of SiO_2 thickness versus inverse temperature. The dashed line (---) is a linear fit ($R^2 = 0.727$) with activation energy $E_a \sim$ 0.7 eV in the absence of a Ge flux, whereas the solid line (—) is a linear fit ($R^2 = 0.699$) with $E_a \sim 0.5$ eV in the presence of a Ge flux.

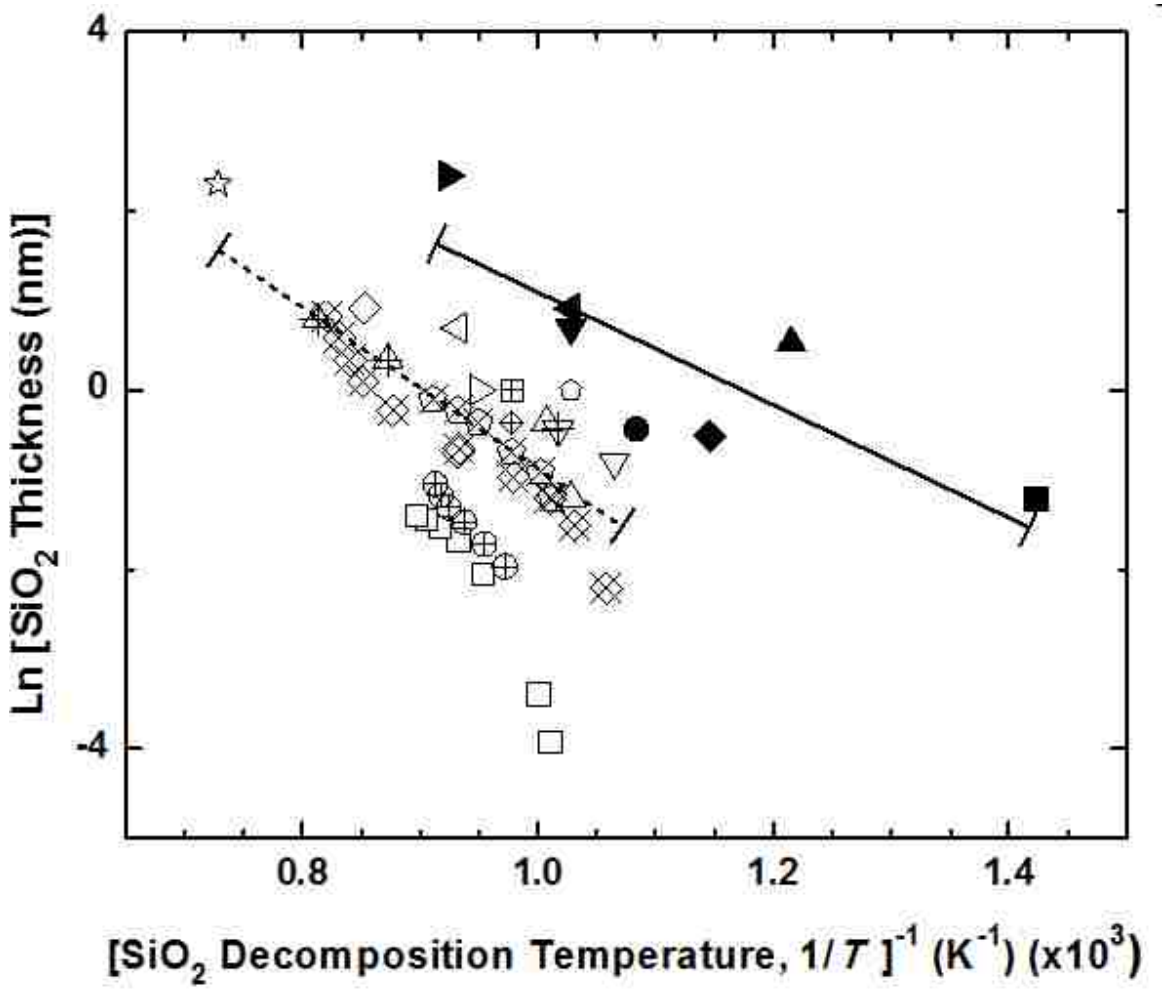


Figure 5-2. Natural log of SiO_2 thickness versus inverse temperature of the SiO_2 decomposition. The broken line is a linear fit to the data without a Ge vapor flux (open symbols). The solid line is a linear fit showing the same trend but shifted to lower temperatures in the presence of a vapor flux of Ge or Si atoms (closed symbols). Data points are referenced as follows: (■);[119] (●);[130] (▼);[134] (◀);[122] (▶);[132] (◆);[121] (□);[137] (△);[124] (▽);[133] (◇);[122] (◁);[136] (▷);[127] (☆);[131] (⬠);[128] (⊞);[150] (⊕);[125] (⟑);[123] (⟒);[120] (⟐);[129] (⊠);[138] and (⊠).[126]

Both lines indicate that the oxide decomposition temperature increases with increasing oxide thickness. However, for a given SiO_2 thickness, the decomposition occurs at lower temperatures in the presence of a Ge flux. The scatter in the data is likely the result of using different experimental methods to detect the onset of decomposition, different Si or Ge atomic fluxes, and different procedures for preparing SiO_2.

Two deductions can be made from the data shown in Figure 5-2 concerning the creation of openings in the SiO_2. First, the fact that Ge exposure lowers the observed decomposition temperature for a given SiO_2 thickness strongly suggests that Ge can also react with SiO_2. The simplest reaction between Ge and SiO_2 can be written as follows:

$$Ge\ (g) + SiO_2\ (s) \rightarrow GeO\ (g) + SiO\ (g) \qquad (5\text{-}2)$$

By directly adding Ge or Si atoms from a vapor flux, Ge or Si adatoms can diffuse to and react at defect sites at the SiO_2–Si interface, thus eliminating the need for lattice Si to be activated and diffuse to defect sites. In fact, adding atomic species of Ge or Si increases the SiO_2 decomposition rate, thus depressing the observed decomposition temperatures shown in Figure 5-2. Secondly, since supplying additional reactant species of Ge or Si increases the reaction rate, these reactants must participate in the rate-limiting reaction step. That is, the Ge or Si flux is equivalent to the formation of Si monomers in reaction (5-1d), which therefore must be the rate-limiting step in the decomposition reaction, in agreement with the findings of Johnson *et al*.[145] If either the reaction of Si with SiO_2 Equation (5-1f) or diffusion of SiO to the oxide surface Equation (5-1g) are rate-limiting, then addition of atomic Ge or Si would not increase the reaction rate and lower the observed decomposition temperature.

Last, the data in Figure 5-2 show an exponential dependence of decomposition temperature on oxide thickness, both with and without an external Si or Ge flux. Although one can attribute this trend to the energy barrier for thermally activated SiO diffusion in Equation (5-1c), the exponential dependence extends to oxide coverages that

are less than one monolayer. Since there is no bulk SiO diffusion barrier at these low coverages, SiO diffusion cannot entirely explain the exponential trend. We speculate that the exponential dependence originates from a change in reactivity at the SiO_2-Si interface as a function of oxide thickness. In regards to the change in reactivity, numerous studies have established that a structural and compositional transition layer exists at the SiO_2-Si interface.[140] Engstrom *et al*.[151] and others[152,153] have shown that the transition layer contains suboxides (i.e., Si^{+1}, Si^{+2}, and Si^{+3}) and that their concentration relative to Si^{+4} decreases with oxide thickness and higher oxidation temperatures. That is, the oxide at the SiO_2-Si interface becomes more stoichiometric with both increasing thickness and oxidation temperature. These observations may explain the increase in oxide stability with thickness for both sub-monolayer and thicker oxides, but more studies are needed to fully understand this exponential dependence.

In contrast to the deductions discussed above, there have been reports that Ge impingement on SiO_2 did not lead to SiO_2 decomposition for thicker oxide layers. Both Yun[132] and Winkenwerder[154] reported no decomposition of 10 nm thick SiO_2 in the presence of Ge flux at 810 °C and 700 °C, respectively. Li *et al*.[108] observed no decomposition for 6 nm thick SiO_2 at 700 °C. However, consistent with the observation that the SiO_2 decomposition begins at the SiO_2–Si interface, Ge must first diffuse through the oxide to the interface[137], and the reaction products, SiO and GeO, must counter-diffuse to the SiO_2 surface. Therefore, we surmise that the substrate temperatures used in the experiments of Yun,[132] Winkenwerder,[154] and Li[108] with thicker oxides are probably not high enough to readily allow Ge diffusion to the interface, especially in light of substrate temperatures required to induce SiO_2 loss in Figure 5-2. Additionally, we

expect that Si atoms can diffuse more readily through SiO_2 to the interface than the larger Ge atoms. In support of this argument, Yun[132] observed decomposition of a 10 nm SiO_2 using a Si atom flux, and a faster decomposition using both a Si and Ge flux. In addition, the sticking coefficient of Ge on SiO_2 becomes very low at higher temperatures,[54] leading to short Ge adatom lifetimes (~16 ns at 700 °C) on the SiO_2 surface before Ge desorption. This short lifetime would mean that very little Ge may actually reach the Si-SiO_2 interface for thicker oxides even at temperatures high enough to achieve Ge diffusion through the oxide.

Once the growing voids that begin at the SiO_2–Si interface have reached the SiO_2 surface and the nanoscale windows form, Ge begins to nucleate on the exposed Si. At this stage, Ge selectively grows within the voids, and eventually grows over the remaining SiO_2 upon Ge island coalescence. The whole process from void nucleation to island coalescence and film planarization is schematically depicted in Figure 5-3. Image 5-3 (a) shows the processes occurring to Ge adatoms including desorption, surface diffusion, and bulk diffusion to the Si-SiO_2 interface. Images 5-3(b-c) shows the nucleation and growth of voids from the Si-SiO_2 interface toward the SiO_2 surface. In 5-3 (d), the nucleation of Ge islands occurs within the void openings, while 5-3(e-f) depict the coalescence of islands into a continuous film and subsequent planarization. The diagonal line running through the Ge film in Figure 5-3 (e-f) represents a stacking fault and will be discussed further in a later section.

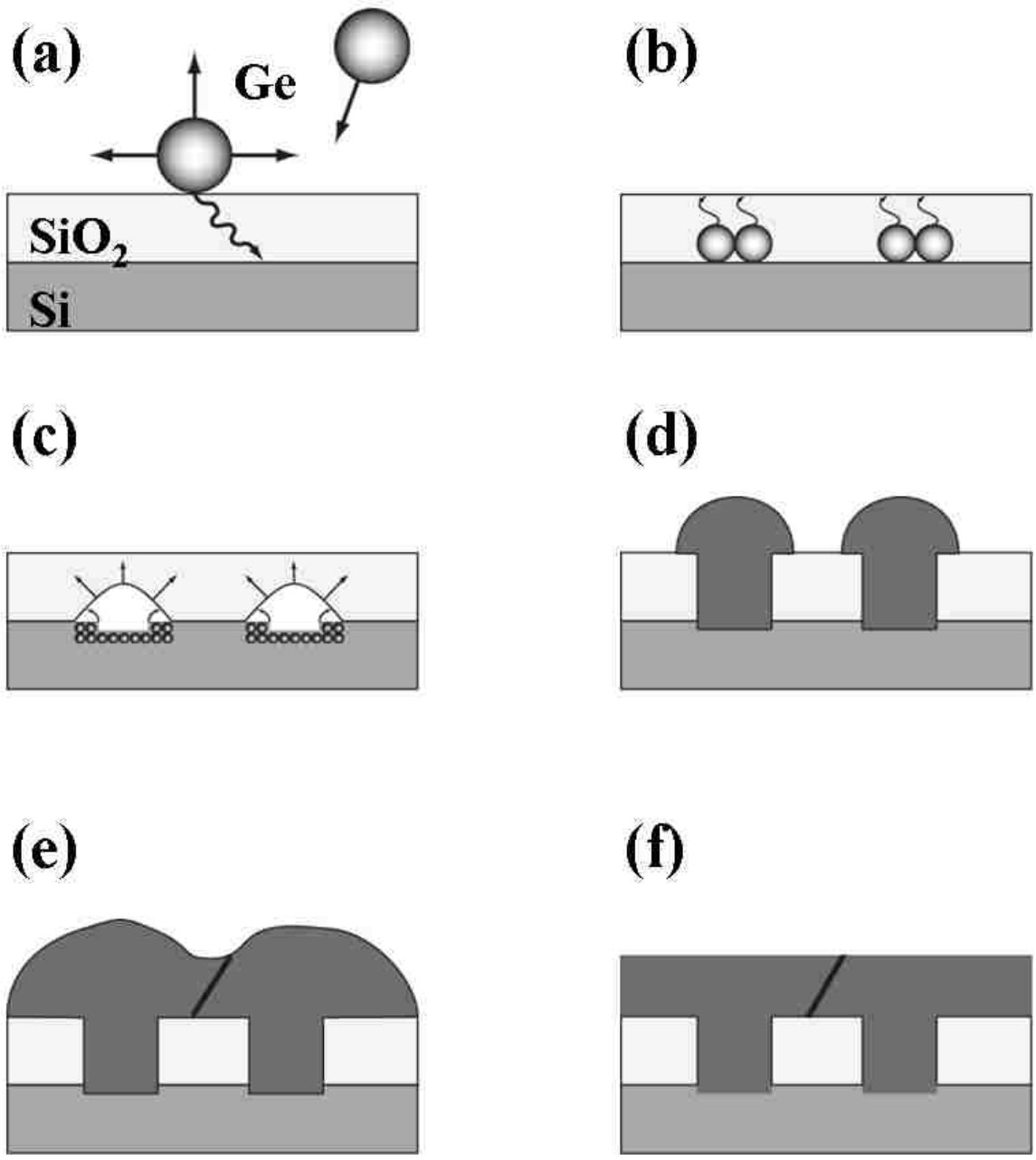


Figure 5-3. Overall depiction of the process from void nucleation and growth to Ge island coalescence and planarization. Shown in 5-3(a) are the processes occurring to Ge adatoms on the SiO_2 surface including desorption, surface diffusion, and diffusion to the Si-SiO_2 interface. Images in 5-3(b-c) show the nucleation and growth of voids from the Si-SiO_2 interface toward the SiO_2 surface. In 5-3(d), Ge selectively nucleates and grows on the newly exposed Si within the void openings. Images 5-3(e-f) show the coalescence of adjacent Ge islands resulting in a SF and subsequent film planarization using chemical-mechanical polishing.

The competition between the SiO_2 decomposition and selective deposition of Ge means that the substrate temperature is very important to simultaneously balance the SiO_2 erosion rate versus Ge growth rate. For the 1.4 nm thick SiO_2 used in this study, substrate temperatures below 550 °C are insufficient to create openings in the oxide resulting in amorphous Ge islands nucleated at the oxide surface. Likewise, at temperatures above 780 °C, the SiO_2 is completely removed before Ge islands can coalesce, leading to a large number of TDs as discussed next.

Figure 5-4 shows low-resolution, bight-field TEM images along the [110] zone axis of Ge grown on bare Si versus Ge grown on the oxidized Si. These bright-field images provide enhanced diffraction contrast of defects in the films. Figure 5-4 (a) shows that Ge on bare Si has a high density of TDs in the Ge film, while Figure 5-4 (b) shows that the Ge grown on the oxidized Si primarily contains twins. Most of the twins terminate within 200 nm from the interface, but many also propagate to the film surface. The SF density that reaches the film surface is estimated to be approximately $5x10^7$ cm^{-2} out of an estimated total of 10^9 to 10^{10} cm^{-2} near the SiO_2-Si interface, based on sampling more than 10 μm along the interface in low-resolution TEM images.

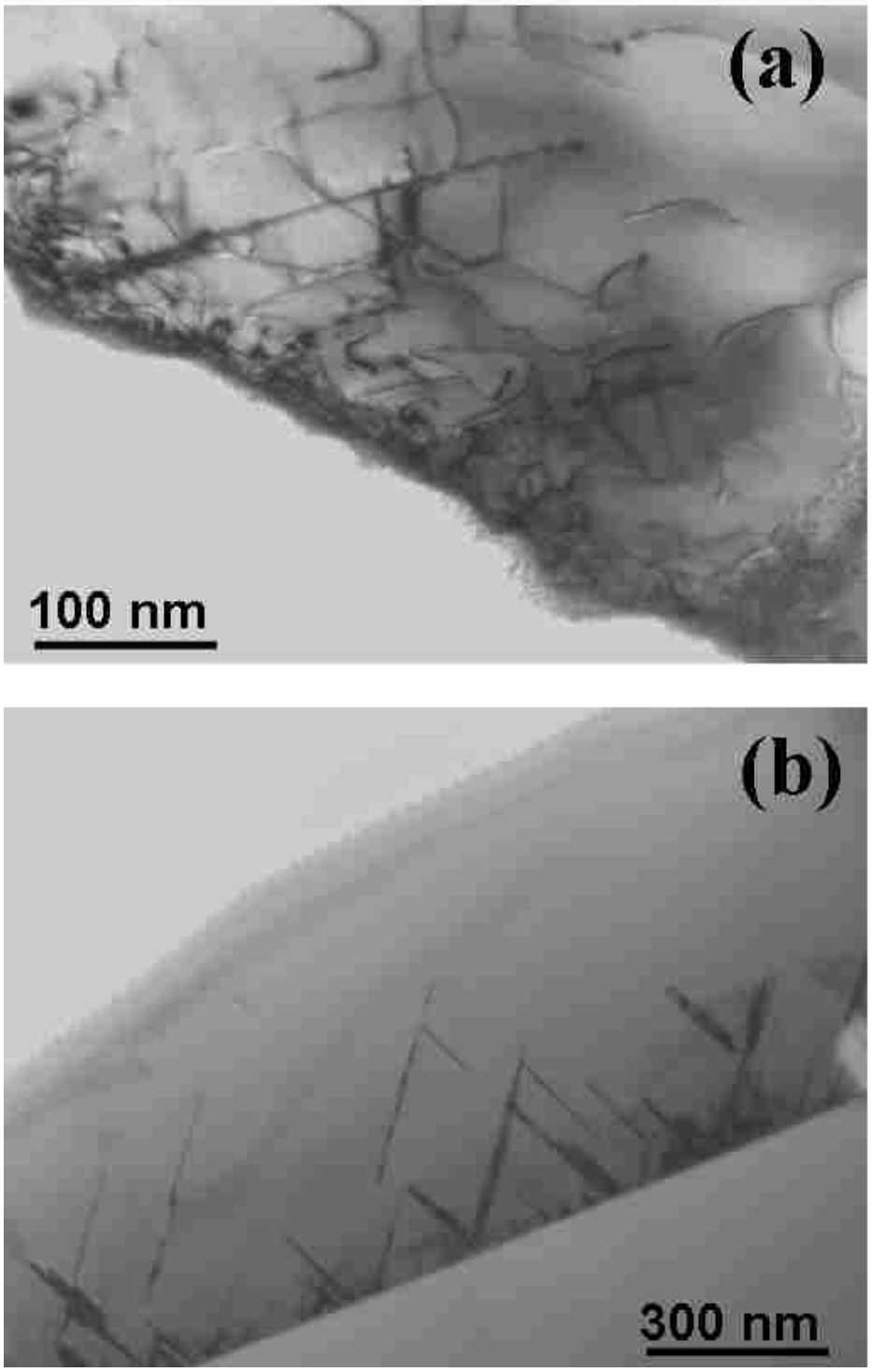


Figure 5-4. Low-resolution transmission electron micrographs, 5-4(a) Ge grown on bare Si and containing a large density of threading dislocations, and 5-4(b) Ge grown on the oxidized Si substrate and having a large density of stacking faults, many of which terminate within 200 nm of the interface.

Li *et al*.[58] previously showed that one mechanism for the SF formation is coalescence between adjacent Ge islands, and is depicted in Fig. 5-3 (e). This mechanism is well established by previous studies showing that twins may form between islands when they coalesce if the islands are slightly twisted or tilted relative to one another.[155] Another possibility is that a SF may form from a translation mismatch between the islands.[156,157] That is, the distance between islands may not be an integer multiple of lattice spacing. Therefore, a SF or a threading dislocation may form during coalescence. This would especially be the case for Ge islands nucleated on Si but separated by SiO_2 because the islands are firmly anchored to the Si substrate and are not mobile. Figure 5-5 illustrates the types of misalignment that may exist between adjacent islands on the substrate.

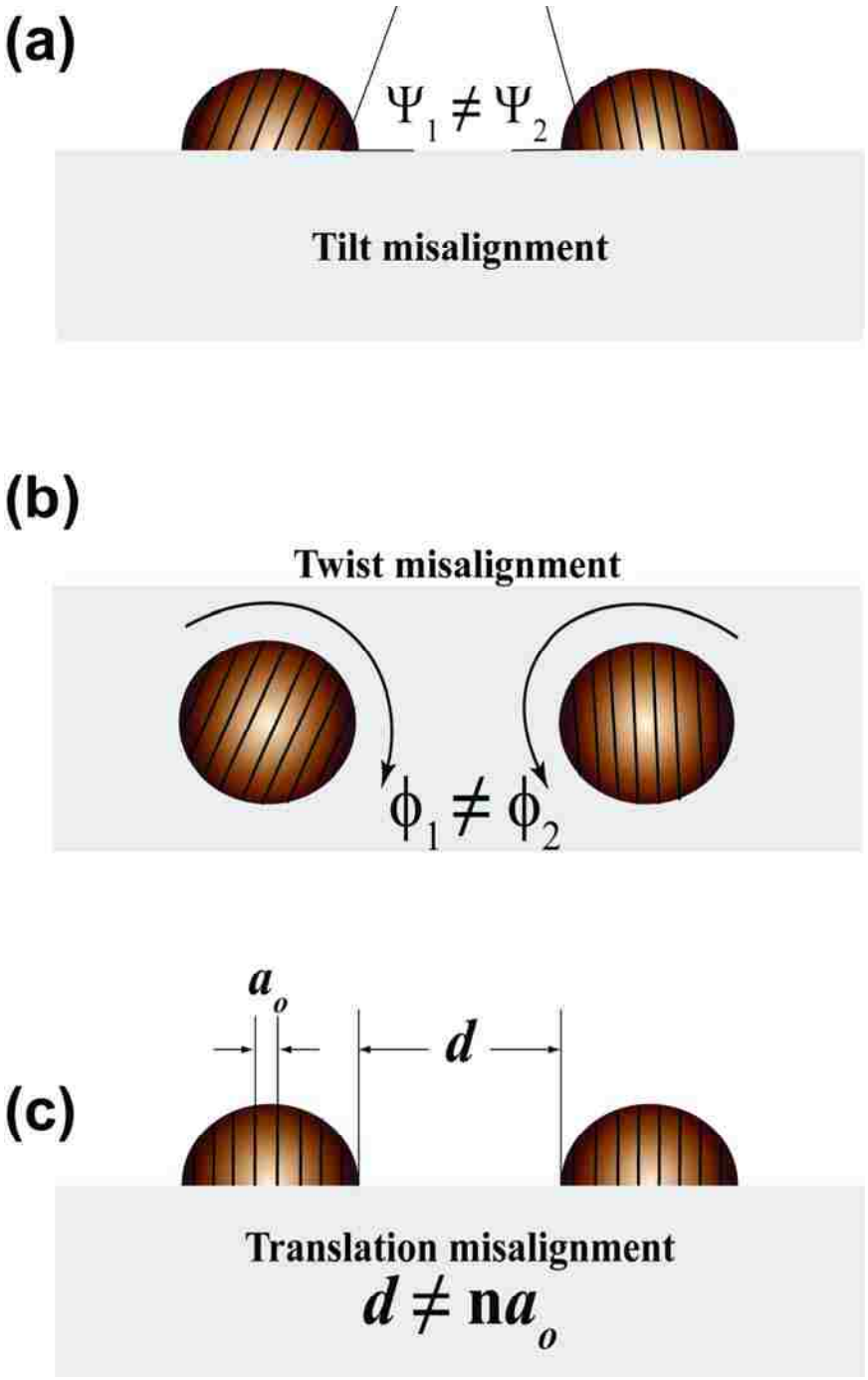


Figure 5-5. Potential misalignments of islands that can lead to defect formation upon island coalescence, 5-5(a) tilt misorientation, 5-5(b) twist misorientation, and 5-5(c) translation misalignment.

Next, a discussion is given of experiments that are performed to elucidate the origin of the twins in Ge films formed through nucleation within openings in chemical SiO_2.

5.3.2 Origin of Stacking Faults in Ge Films

The Ge films, created by the eventual coalescence of islands nucleated within nanoscale openings in chemical SiO_2, contain a large number of twins. However, the exact mechanism by which these twins form remains unknown. One possibility is that twins may result from the coalescence of Ge islands that nucleate randomly on top of the chemical SiO_2 with Ge islands that nucleate epitaxially within openings in the oxide. This may occur, for example, if Ge islands that have nucleated on SiO_2 undergo either recrystallization or reorientation upon coalescence with epitaxial Ge islands. Both processes have been observed to lead to twin/SF formation at the merging junction of islands in several different material systems.[158-164] To determine the presence of random nucleation and potential possibility of SF formation, we have measured the saturation island density at two different substrate temperatures and deposition rates and examined these measurements within the context of mean-field theory.

The results of mean-field theory show that for random nucleation, the saturation (maximum) island density varies exponentially with both substrate temperature and deposition rate.[88,89,165] For Ge islands randomly nucleating on top of thick SiO_2, we have previously observed an exponential decrease in the saturation Ge island density with increasing substrate temperature, and an increase in the island density with increasing deposition rate.[54] In contrast, the saturation island density for defect-induced nucleation is independent of temperature and deposition rate.[96] In the latter case, the saturation island density is determined solely by the density of defects at the surface of the substrate and is invariant over a wide range of deposition conditions. The saturation Ge island

density resulting from our growth technique utilizing chemical SiO_2 is expected to behave similarly to defect-induced nucleation. There are two reasons to expect this outcome. First, the number of openings that form in the SiO_2 is determined by the reaction of Ge and Si at a defect site at the Si-SiO_2 interface.[131] Second, the strong binding energy of Ge on Si should induce preferential and selective nucleation of Ge islands within the openings in the SiO_2 where Si is exposed.[73] There fore, the number of openings that form in the SiO_2 should remain constant over a temperature range sufficient to decompose the SiO_2 at the defect sites and desorb the volatile byproducts. Moreover, the number of openings should determine the saturation island density. If some of the Ge islands are nucleating both randomly on top of the chemical SiO_2 and selectively within openings in the SiO_2, then the number of randomly nucleated Ge islands on top of the SiO_2 should be greatly reduced at an elevated substrate temperature and increased at higher deposition rates. The result will be a reduction in the total island density with increasing substrate temperature, and an increase in the overall island density at higher deposition rates.

The density of Ge islands that form upon exposing the chemical SiO_2 on Si to Ge flux is examined through a series of high-resolution SEM images collected at increasing amounts of Ge deposition. Figure 5-6 (a-d) shows images taken after Ge exposures equivalent to 8, 12, 18, and 25 nm of Ge, respectively. The substrate temperature is held at 853 K, and the Ge flux is maintained at 19.1 ML/min during exposure. The density of Ge islands is measured for the samples (Set 1) shown in Figure 5-6 (a-d); higher magnification images are used in the case of relatively small Ge islands as shown in the inset of Figure 5-6 (a). Figure 5-6 (a) and (b) have island densities of $2.6 \pm 0.2 \times 10^{11}$ and

$1.4 \pm 0.2 \times 10^{11}$ cm^{-2}, respectively. This indicates that, on average, each island has coalesced with one of its neighbors between deposition of 8 and 12 nm of Ge. By analyzing the islands shown in Figure 5-6 (c) similarly for 18 nm of Ge deposition, the island density is nearly unchanged at $1.2 \pm 0.1 \times 10^{11}$ cm^{-2} indicating that islands grow without further coalescence between 12 and 18 nm of Ge deposition. Analyzing similarly for Figure 5-6 (d), in which 25 nm of Ge is deposited, the island density further decreases to $3.2 \pm 0.1 \times 10^{10}$ cm^{-2} indicating that four coalescence events per island have occurred. Therefore, we deduce that the maximum island density for these deposition conditions must occur with less than or equal to 8 nm of Ge deposition.

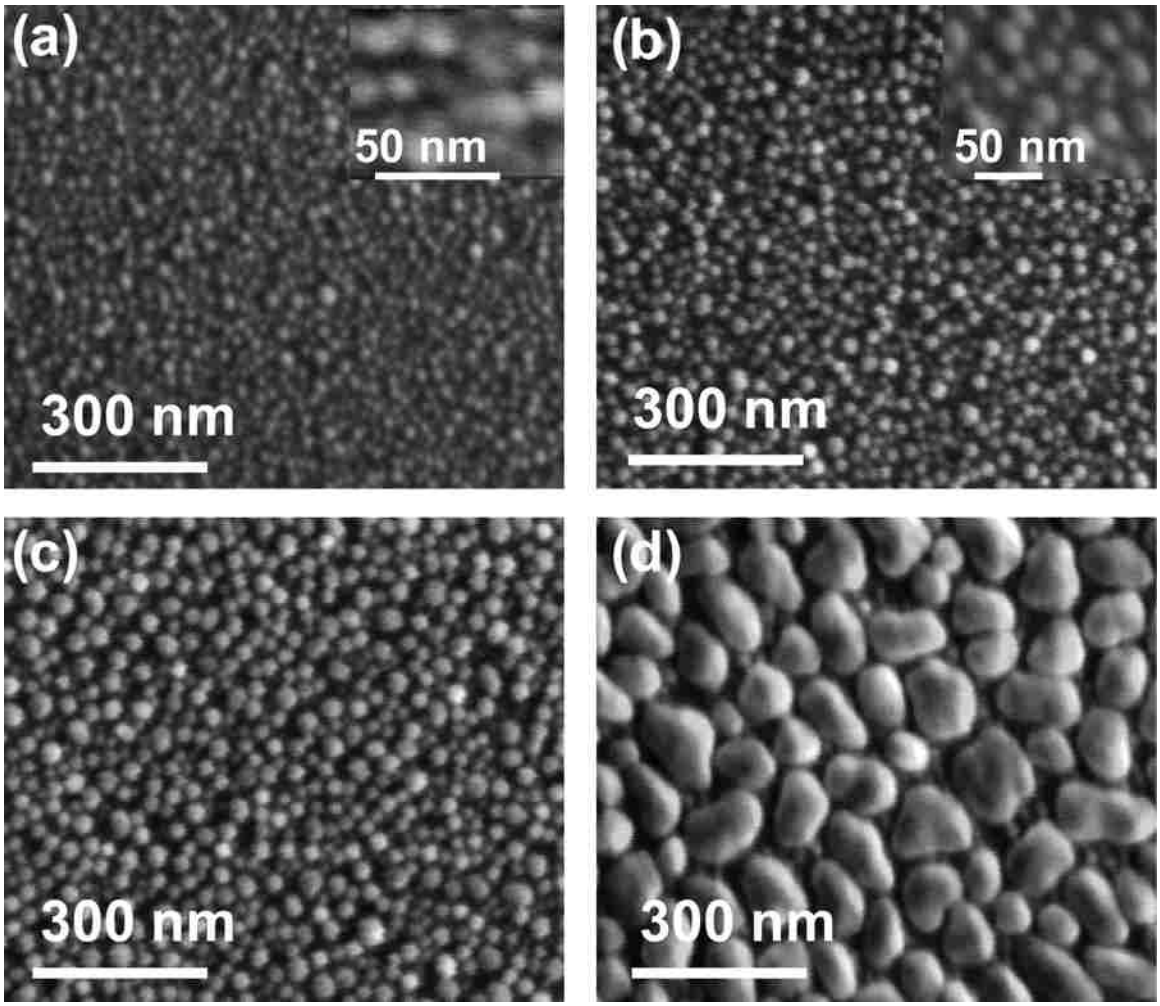


Figure 5-6. Scanning electron micrographs of Ge islands deposited within openings in chemical SiO_2. Images 5-6(a-d) have initial amounts of 8, 12, 18, and 25 nm of Ge deposition. The images track the coalescence and morphology of the islands with increasing deposition. Higher magnification images, as shown in the insets of 5-6(a-b), are used to estimate the amount of Ge contained within the islands based on the average island density and diameter.

For comparison, two additional sets of samples are prepared and imaged after the same Ge exposure levels (i.e., 8, 12, 18, and 25 nm). One set (Set 2) is made at a substrate temperature that is 70 degrees higher at 923 K and at the same deposition rate of 19.1 ML min^{-1}. The other set (Set 3) is made at the same substrate temperature of 853 K as that of the first set, but at a higher deposition rate of 60 ML min^{-1}. The set of samples

made at the higher substrate temperature (Set 2) shows the same maximum island density as Set 1 of $2.6 \pm 0.2 \times 10^{11}$ cm^{-2}, occurring at both 8 and 12 nm of Ge deposition. Island coalescence then decreases the island density to $7.1 \pm 0.1 \times 10^{10}$ cm^{-2} and $5.9 \pm 0.1 \times 10^{10}$ cm^{-2} for 18 and 25 nm of Ge deposition, respectively. These island densities are higher for the same amount of Ge deposition compared to the samples made at the lower temperature of 853 K, indicating that coalescence is suppressed at higher temperature. This can be explained by increased surface diffusion at the higher temperature, thus allowing Ge islands to achieve a greater contact angle with the surrounding SiO_2 and leading to larger spacing between Ge islands. A large contact angle of Ge islands on SiO_2 is energetically favored based on the 3.9 eV Ge-Ge binding energy compared to 0.44 eV for Ge-SiO_2.[54,73,108] Lastly, the island densities in the samples made at the higher deposition rate (Set 3) are all identical to those found in the series shown in Figure 5-6 (Set 1), with the maximum island density of $2.6 \pm 0.2 \times 10^{11}$ cm^{-2} occurring after 8 nm of deposition.

Overall, the finding is that the maximum Ge island density remains unchanged at higher substrate temperature and deposition rate. This result is consistent with selective Ge nucleation within openings in SiO_2 in the absence of random nucleation on top of the oxide. Therefore, we deduce that twins are not likely to result from random Ge island nucleation on top of the SiO_2 layer.

Another possible mechanism responsible for SF formation is that some Ge islands are nucleating in a tilted orientation to the Si substrate within openings in the SiO_2 layer. For example, an island rotated by 70.5° about a [110] direction would form a coherent

twin boundary when coalescing with a (001) oriented epitaxial island. This possibility is discussed next.

To investigate the possibility that twins arise during coalescence of twin-oriented Ge islands, an x-TEM specimen is created from the sample shown in Figure 5-6 (b). This sample is chosen to observe Ge islands that have just begun to coalescence. The x-TEM sample is oriented so that the viewing direction is along the [110] zone axis. The Ge islands in the sample are then analyzed at high-resolution to obtain lattice fringe images. The lattice fringes from the Ge islands are then Fourier transformed into diffraction patterns to obtain orientation information from individual islands. Figure 5-7 (a) shows an example of two Ge islands that have just begun to coalesce. The diffraction patterns of the Si and Ge islands are also shown as insets in the figure, and reveal that the Ge island on the left is epitaxially oriented to the Si substrate. The Ge island on the right, however, is tilted by 70.5^{o} counter-clockwise about the [110] direction with respect to the Si, putting it in a twin relationship to the Si. A coherent twin boundary has formed at the junction of the islands upon coalescence. The twin boundary is magnified in the filtered Fourier image shown in the inset of Figure 5-7 (a), at the merging point of the two islands. The dashed line marks the coherent twin boundary between the Ge islands. The (-111) and (-11-1) planes are common to both Ge islands and are marked by the solid white lines on either side of the twin boundary. Figure 5-7 (b) shows a structural model of the two Ge islands on the Si. The twin-oriented Ge island on the right is also in a twin relationship to the Si substrate, but the boundary between the Si and Ge island lies in the (100) plane, and therefore forms a $\Sigma = 3$ incoherent twin boundary. The atomic structure

of the incoherent twin boundary is obscured in the TEM image by the remaining SiO_2 template that the Ge islands have merged upon.

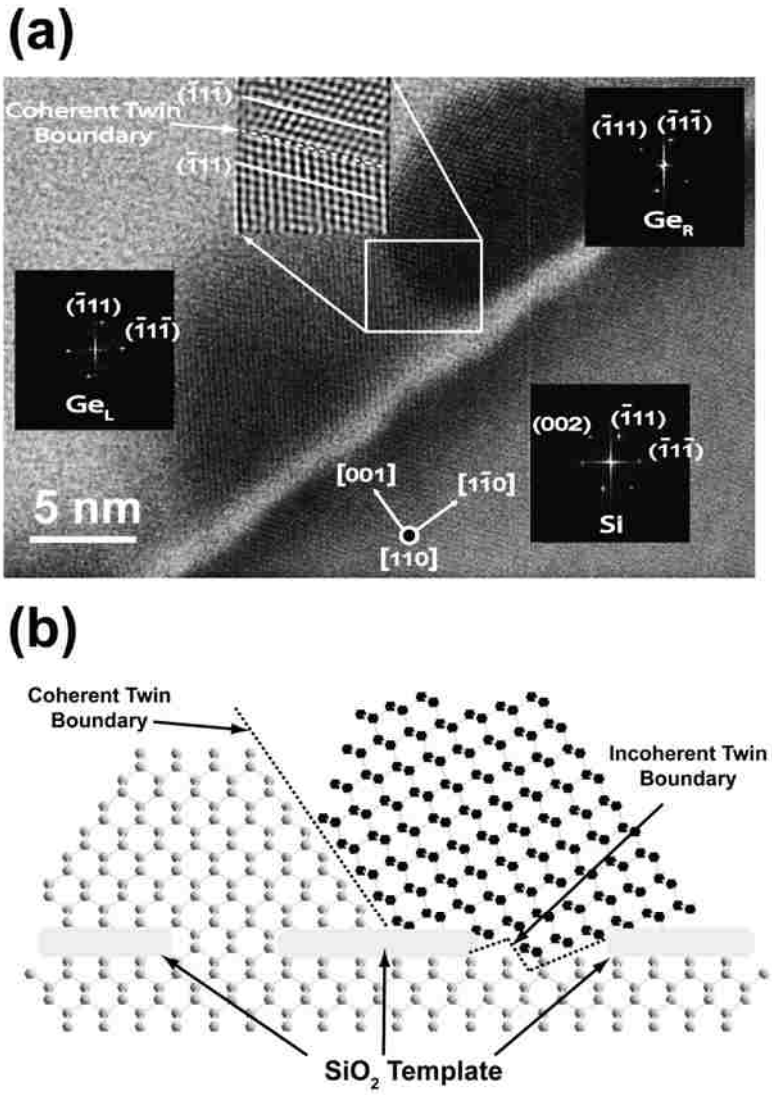


Figure 5-7. Image 5-7(a) is a high-resolution cross-sectional transmission electron microscope image of the sample with 12 nm of Ge deposition, where the Ge islands have just begun to coalescence. The Ge island on the right is nucleated in a twin relationship to the Si and has formed a coherent twin boundary at the junction with the epitaxial Ge island on the left. The twin boundary is magnified in the filtered image that is inset where the islands have merged. The diffraction patterns of the islands and substrate are also included as insets. Image 5-7(b) is a schematic drawing of the orientation of the islands corresponding to the image in Figure 5-3(a).

The Σ notation comes from the Coincident Site Lattice (CSL) model and denotes a special high-symmetry orientation relationship between two misoriented crystal lattices. The concept of the CSL model is shown in Figure 5-8. Image 5-8(a) shows a (110) plane of a diamond cubic lattice viewed along the [110] direction. Image 5-8(b) shows the same lattice in (a) but rotated by 70.5^{o} counter-clock-wise about the [110] direction. Figure 5-8 (c) shows the net result when the two lattices in 5-8(a) and 5-8(b) are translated so that they are overlapping. The two-tone blue and white lattice sites are coincident to both lattices in Figure 5-8 (a) and (b) and form the coincident site lattice. The CLS unit cell is marked with the dotted line. Sigma is defined as the reciprocal of the ratio of the CSL sites to total lattice sites within the unit cell of the CSL. The example is Figure 5-8 (c) contains a total of 12 lattice sites within the CSL unit cell. A total of 4 sites within the CSL unit cell are shared by both lattices, therefore $\Sigma = 4 / 12 = 3$. The $\Sigma = 3$ boundary is a special high-angle grain boundary known as a twin boundary. The TEM analysis reveals both twins and other misorientation boundaries between Ge islands and the Si substrate.

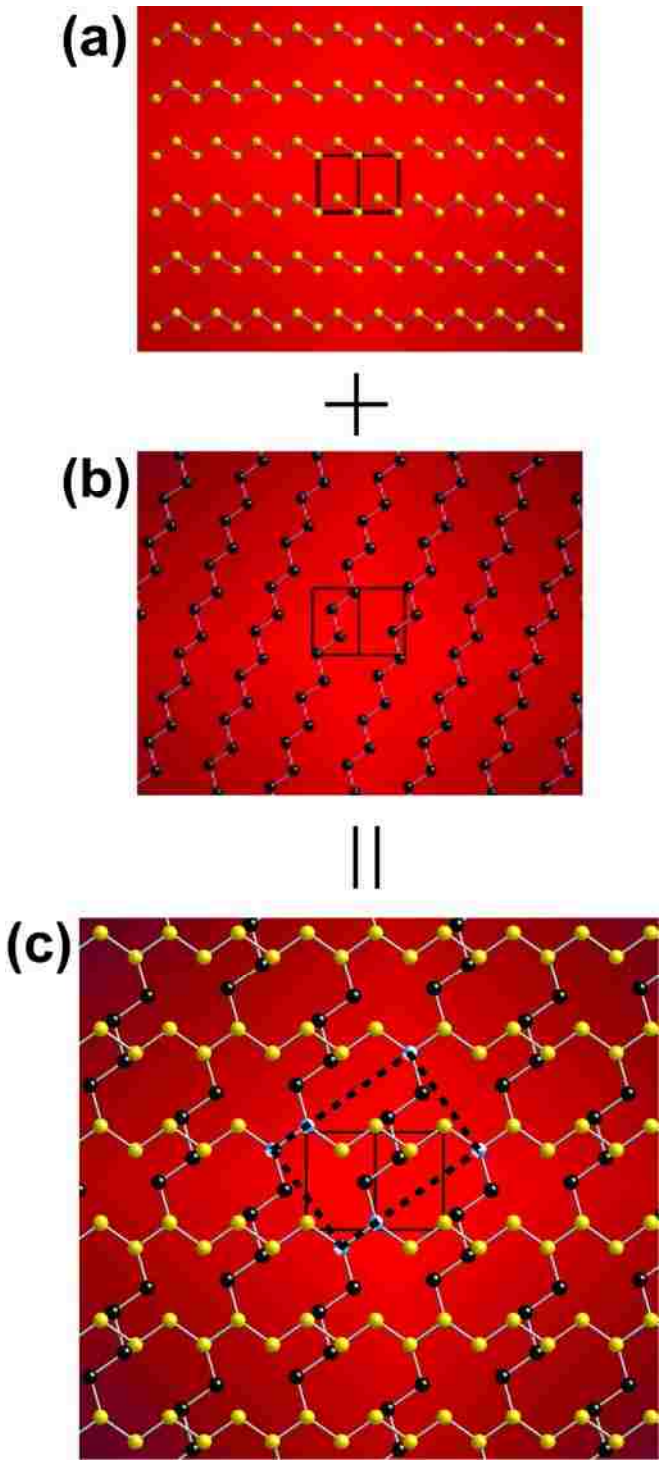


Figure 5-8. Illustration of the Coincident Site Lattice model. Image 5-8(a) shows a (110) diamond cubic lattice viewed along the [110] direction. Image 5-8(b) is the same lattice shown in 5-8(b) but rotated by 70.5 degrees counter-clock wise about the [110] direction. Image 5-8(c) shows the overlap of lattices 5-8(a) and 5-8(b) and shows the coincident sites marked in two-tone blue and white. The unit cell of the coincident site lattice is outlined with the dashed line.

Orientation analysis is applied to a total of 50 Ge islands in the sample, and a total of 8 Ge islands are found to have nucleated in twin relationships to the Si. Based on the total Ge island density of $1.4 \pm 0.2 \times 10^{11} cm^2$ in this sample, the twin/SF defect density that will result from coalescence of these twin-oriented islands is estimated to be greater than 4×10^{10} cm^{-2}. This estimate is in qualitative agreement with the TEM measured twin/SF density of approximately 5×10^{10} cm^{-2} that exists at the interface in fully coalesced Ge films, as shown in the TEM image of Figure 5-4 (b). In addition to observing 8 twin-oriented islands, 4 of the 50 islands examined at high-resolution have a small angle of tilt misorientation to the Si that ranges from 1.8 to 5.6 degrees. This indicates that approximately 2×10^{10} cm^{-2} of the total Ge islands form a low-angle grain boundary with the Si.

The reason that approximately 16 % of the Ge islands nucleate in twin relationships to the Si and 8 % nucleate with small tilt misorientation to the Si is not presently understood. The mechanistic details describing how epitaxy occurs within the confined openings that form in the SiO_2 is lacking. These details are currently being investigated using molecular dynamics simulations. Next, a method is described for planarizing GoS.

5.3.3 Planarization of Ge Films

The Ge films grown on the oxidized Si have a RMS roughness of 8 to 10 nm. This roughness is due to the 3D island growth of Ge on Si and subsequent coalescence. To prepare the films for GaAs growth, it is necessary to planarize the films using CMP. However, slurry for Ge CMP is not commercially available, so a combination of slurry and pad types is tried to obtain an optimal surface. Using a soft pad (Chemcloth made by

Logitech) in conjunction with a colloidal SiO_2 slurry (SF1 from Logitech) gives an RMS roughness of less than 1 nm but leaves a large number of shallow scratches on the Ge surface. To prevent the scratches, a solution of 1 part H_2O_2 (30 wt%) to 50 parts DI water is used in conjunction with the soft pad to produce RMS values of 0.5 nm without scratches. The Ge etch rate of the dilute peroxide is approximately 11 nm / min in bulk solution, but the etch rate is 3 to 5 times faster during the chemical polish. The soft abrasion provided by the pad in contact with raised features on the Ge surface enhances the local etch rate of the peroxide solution to produce the good planarity and surface finish of the films. Figure 5-9 (a) and (b) show AFM images of the Ge film before and after polishing, respectively. Figure 5-9 (b) shows a large number of raised lines protruding from the surface. These lines are 1 to 2 nm high and correspond to the twins that terminate at the film surface, which apparently etch at a slower rate than the surrounding material. The density of these lines is 3-to-5 $x10^7$ cm^{-2} in good agreement with TEM images. The presence of the twins in the Ge films and their termination as raised lines at the polished Ge surface have led us to investigate methods to reduce or eliminate them. We have found that annealing Ge islands leads to Ge films free from twins.[55,56]

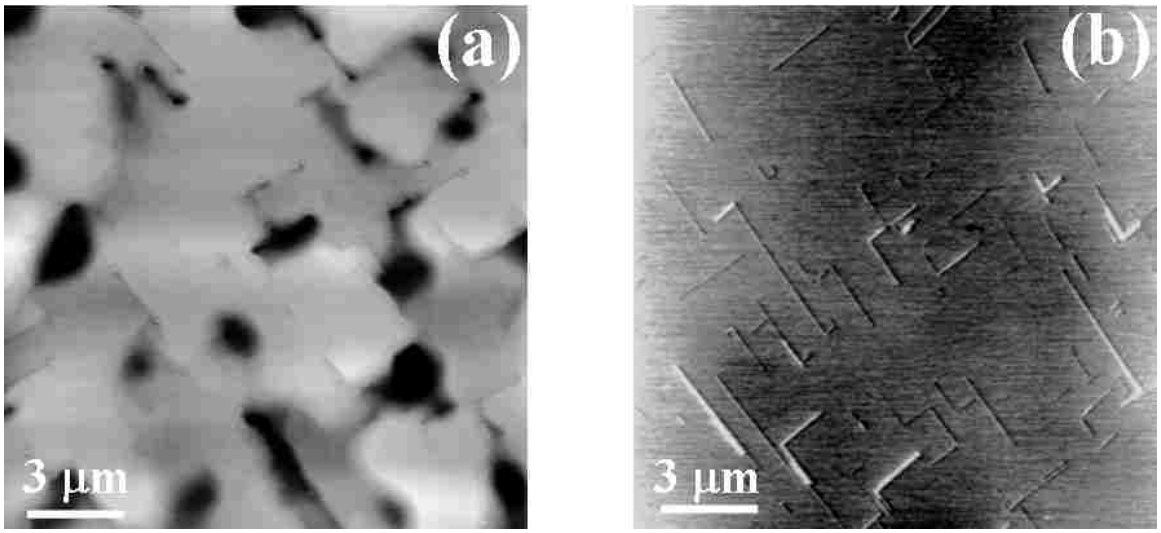


Figure 5-9. Atomic force microscope images of 5-9(a) 3 μm Ge sample grown on oxidized Si before polishing, 5-9(b) same sample after polishing with dilute H_2O_2 for 20 min. In 5-9(b), the raised lines are the result of twins that terminate at the Ge surface, and which polish at a slower rate than the surrounding material.

5.3.4 Annealing Ge Islands

Twins do not manifest themselves if an anneal step is done for 30 min at 1073 K on Ge islands before extensive coalescence has resulted in the formation of a continuous Ge film. Anneal temperatures below 1073 K for 30 min are found to be ineffective at completely removing the twins. Figure 5-10 (a-c) shows AFM images of 3 μm thick Ge films that are annealed at temperatures of 923, 1003, and 1073 K, and then planarized. In each case, the anneal step was performed for 30 min after deposition of 10 nm of Ge on the oxidized Si at 853 K, but before full Ge coalescence to form a continuous film. The density and dimensions of the SF lines decrease with increasing annealing temperature, until at 1073 K, twins are no longer detectable in AFM images.

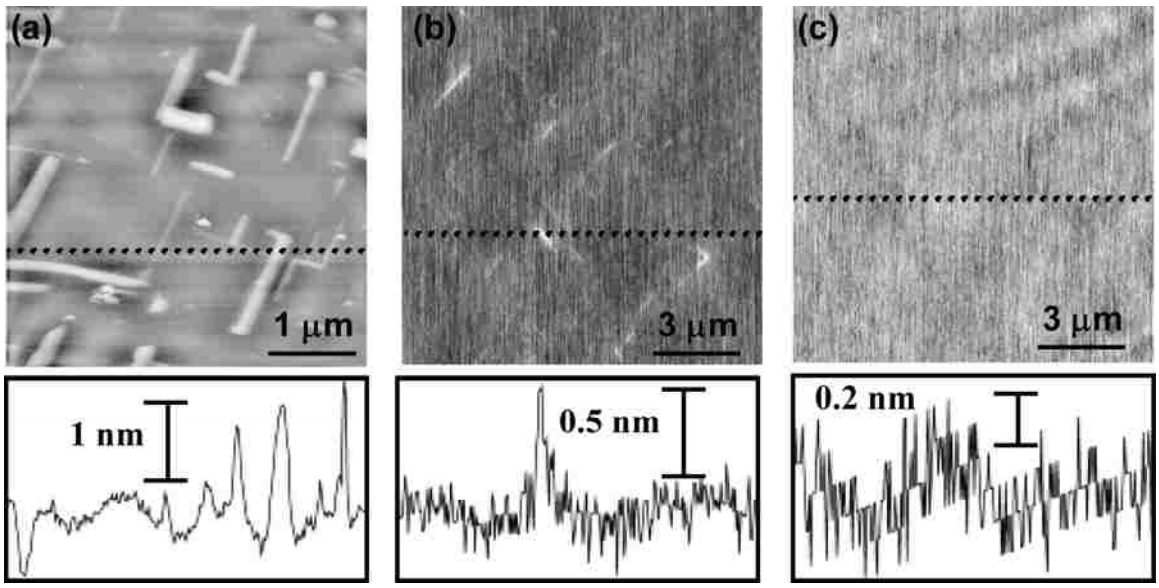


Figure 5-10. Atomic force micrographs of Ge films taken after polishing reveal the twins that terminate at the Ge surface. The images 5-10(a-c) correspond to samples that are annealed at 923, 1003, and 1073 K for 30 min after first depositing 10 nm of Ge.

Correspondingly, Figure 5-11 shows that the XRD FWHM of the (004) reflection of the Ge film decreases by a factor of 2.3 as compared to unannealed films. The FWHM of the (331) reflection (not shown) decreases even further, by a factor of 3.3. These results indicate that twins are removed, and the crystal quality of the Ge films significantly improves during the 1073 K anneal that is performed during the island stage of Ge growth.

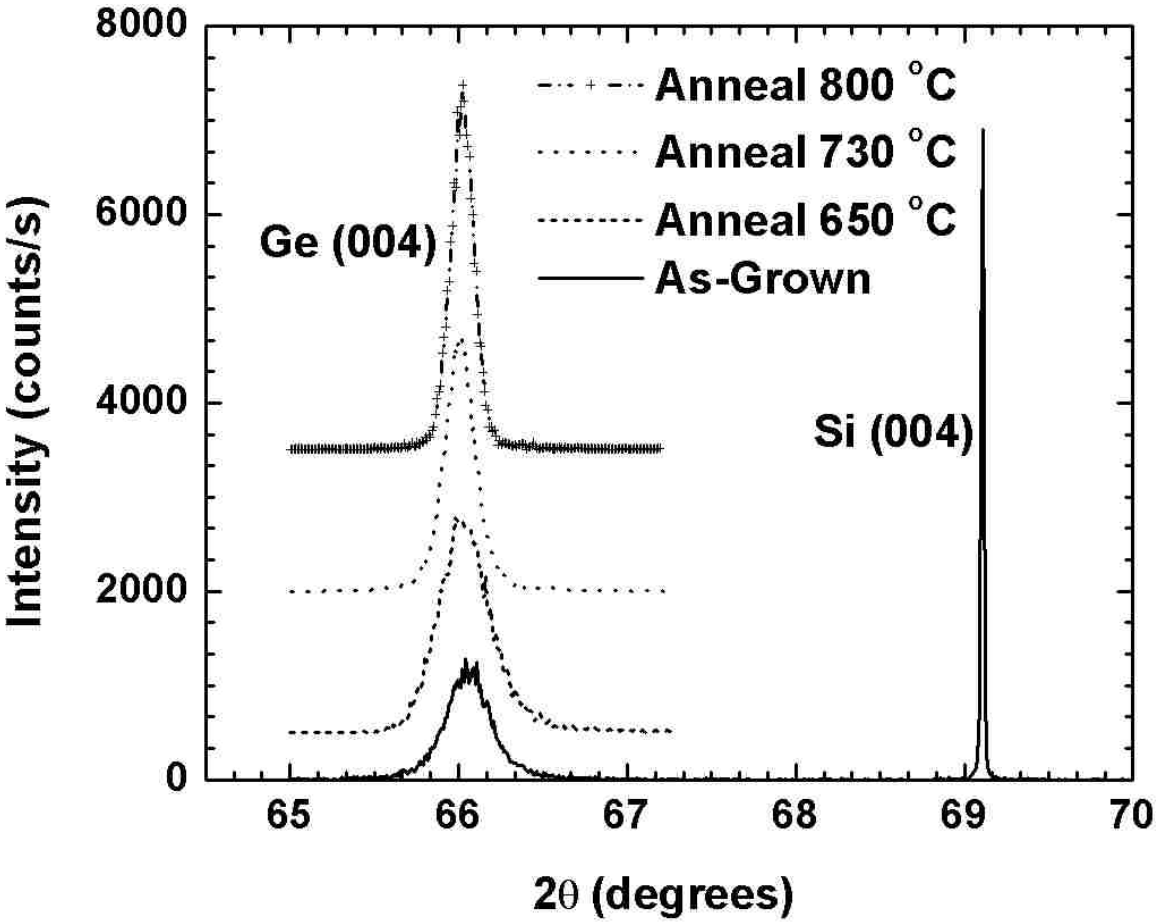


Figure 5-11. The x-ray diffraction peaks of the (004) reflection of Ge films that are unannealed (solid line), annealed at 923 (dotted line), 1003 (dashed line), and 1073 K (dot-dashed line) for 30 min after first depositing 10 nm of Ge.

Annealing at 1073 K is also done at different stages of Ge island coalescence. Two samples are created, Sample 1 with 50 nm and Sample 2 with 100 nm of Ge deposition. Significant Ge island coalescence has occurred on both samples and some islands are observed with SEM to be over 200 nm in diameter; however, the Ge islands still do not form a continuous film across the surface. The samples are then annealed at 1073 K for 30 min, followed by further Ge growth to 3 μm thickness. In both cases, twins are not observed in AFM images of the Ge films observed after polishing. In contrast, this was found *not* to be the case, if the anneal step is done after complete

coalescence of the Ge film, such that the SiO_2 template is completely covered with Ge. Complete coalescence is observed to occur in SEM images after approximately 300 nm of Ge deposition. Films annealed at 1073 K for 30 min after complete coalescence result in twins remaining in the Ge film. This result is confirmed by AFM images taken after CMP where twins reveal themselves similarly as in Figure 5-9 (b).

If twins originate from the coalescence of an epitaxial (100) Ge island and a Ge island tilted by 70.5° about the [110] direction, as suggested previously, then large islands that form as a result of multiple coalescence events should contain twins. For example, the large Ge islands in Figure 5-6 (d) have undergone several coalescence events and some of these islands will likely contain twins. Yet, we find that annealing even larger islands than these is effective in obtaining Ge films without twins. This suggests that the annealing is somehow effective at driving the twins out of the islands up to approximately 200 nm in size. Moreover, the finding that twins remain in the Ge film if annealing is done after a continuous film occurs also suggests that free surfaces are needed for twin removal. The removal of twins may arise from a combination of glide of the Shockley partial dislocations that bound the fault and atomic rearrangement during annealing. A detailed study is discussed next specifically investigating how twins are removed by annealing of Ge islands.

5.3.5 Desorption of Chemical SiO_2 During Annealing

The high temperature anneal step, in addition to removing twins from Ge islands, also likely removes any chemical SiO_2 not covered by the Ge islands. This assertion is based on observations made after annealing of a chemical SiO_2 layer on Si, under

vacuum, at 1073 K, for 30 min. Immediately after the anneal step, the sample is cooled to room temperature and coated with 100 nm Ge deposited from the effusion cell. This coating is used to prevent subsequent re-oxidation of the Si interface upon removal from the vacuum chamber. The sample is then examined in cross-section using STEM, which provides good contrast based on the atomic density of a material. The SiO_2 is less atomically dense than either Si or Ge, and therefore, it appears in STEM images as a dark layer at the interface between the Si substrate and the Ge capping layer. Figure 5-12 (a) shows that the chemical SiO_2 layer does not appear in the STEM image and indicates that the SiO_2 layer is completely desorbed upon annealing at 1073 K. Contrastingly, the STEM image of the sample shown in Figure 5-12 (b) consists of a chemical SiO_2 layer on Si that is first coated with 100 nm Ge deposited at room temperature, and then annealed at 1073 K for 30 min. The chemical SiO_2 does appear in the STEM image, in this case, indicating that the SiO_2 layer remains in place if capped before annealing. The result shown in Figure 5-12 (a) suggests that annealing a sample with Ge islands will effectively desorb the chemical SiO_2 layer that exists between the Ge islands. However, the result in Figure 5-12 (b) suggests that SiO_2 buried beneath large islands that have formed from the coalescence of smaller islands should remain intact during the anneal step.

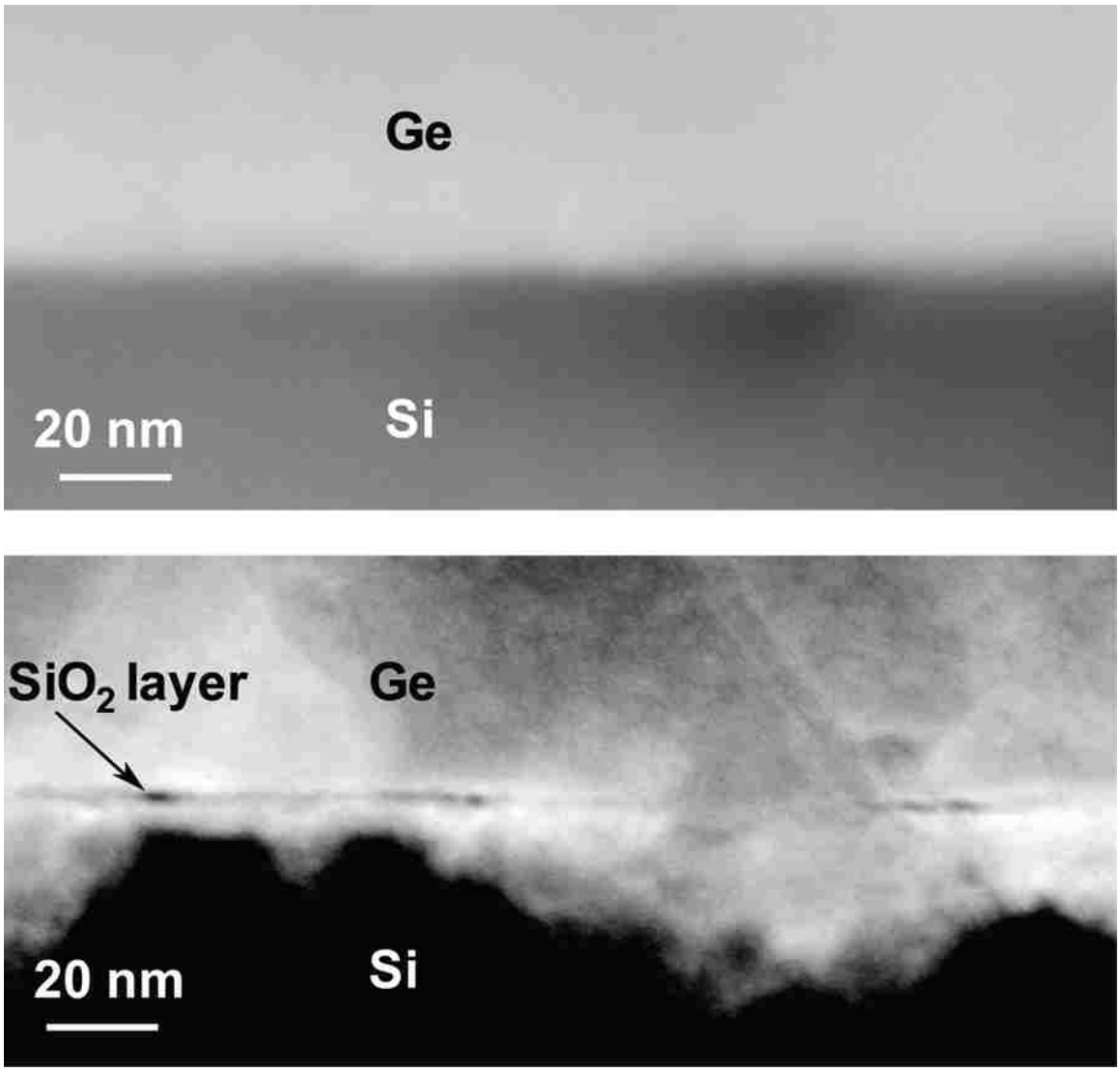


Figure 5-12. Scanning transmission electron micrograph images taken after annealing a layer of chemical SiO_2 on Si, and used to determine the stability of the oxide layer during annealing. Image 5-12(a) is taken after annealing the sample at 1073 K for 30 min under vacuum, then subsequently capped with 100 nm of Ge deposited at room temperature. The SiO_2 layer appears to have been desorbed during annealing. The sample shown in image 5-12(b) is the same as in 5-12(a), except that 100 nm of Ge is first deposited at room temperature, and followed by annealing at 1073 K for 30 min.

Subsequent Ge growth that occurs after annealing Ge islands, based on the above results, will occur directly on existing Ge islands and on freshly exposed Si where SiO_2 was desorbed in the areas between the Ge islands. The deposition occurring on the newly

exposed Si after the anneal step is, therefore, expected to lead to a large number of TDs to relieve the lattice mismatch stress between Ge grown directly on Si. The nucleation of TDs is experimentally investigated next, in addition to the mechanism of SF removal by annealing Ge islands.

5.3.6 Mechanism of Stacking Fault Removal by Annealing Ge Islands

Four samples are created with identical amounts of Ge deposition as the samples shown in Figure 5-6 (a-d). These samples are annealed at 1073 K for 30 min, in vacuum, immediately after deposition. The results are shown in the SEM images in Figure 5-13 (a-d) for 8, 12, 18, and 25 nm of deposition, respectively. The island density and morphology change considerably after annealing. The island density of $2.6 \pm 0.2 \times 10^{11}$ cm^{-2} that is present for 8 nm of Ge deposition prior to annealing, as shown in Figure 5-6 (a), is now reduced to $1.5 \pm 0.4 \times 10^{10}$ cm^{-2} in the sample shown in the SEM image in Figure 5-13 (a), taken after annealing with the same 8 nm of initial Ge deposition. The average island diameter has also increased to 18 nm. The island density for the sample shown in 5-13 (b), with 12 nm of Ge deposition has the same island density as the annealed sample with 8 nm, but the average island diameter is increased to 40 nm. The islands in 5-13 (b) have also developed square shaped facets parallel to <110> directions. The annealed sample with 18 nm of Ge deposition, shown in Figure 5-13 (c), has two sizes of islands. The small islands have approximately the same size and density as the annealed sample shown in Figure 5-13 (b). The large islands have a much lower density of $5.6 \pm 0.6 \times 10^{7}$ cm^{-2}, but their diameter is significantly larger at about 765 ± 200 nm, and a few of the islands even exceed 2 μm in diameter. The largest islands also appear to

have trenches at certain points around them, as shown in the inset of Figure 5-13 (d). The sample shown in Figure 5-13 (d), annealed after deposition of 25 nm of Ge, has the same density of large islands as the sample with 18 nm of deposition, but with an average island diameter larger than 1 μm. In addition, most of the small islands appear to have disappeared in this sample. The changes that are observed upon annealing the Ge islands are discussed next.

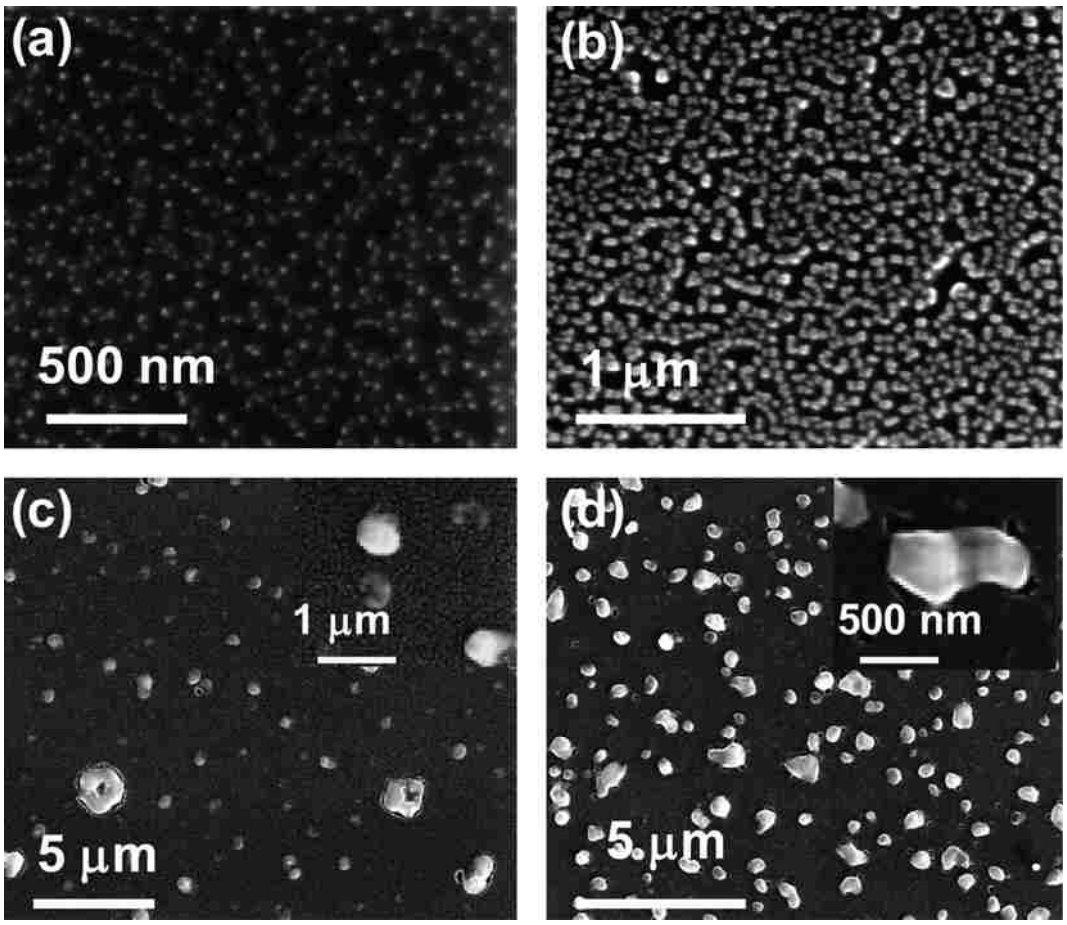


Figure 5-13. Scanning electron micrographs of Ge islands after annealing with initial deposition of 8, 12, 18, and 25 nm [images 5-12(a-d), respectively]. The islands density is reduced by a factor of 16 after annealing. Images 5-12(c-d), and insets therein, also show the formation of very large Ge islands surrounded by trenches that extend down into the Si. The density of the large islands is the same in both images.

First, there is a 16-fold decrease in the island density and a 30% increase in the average island diameter between the unannealed and annealed samples with 8 nm of Ge deposition. The amount of Ge deposited as islands is calculated for both samples to determine whether this amount of Ge is conserved. The amount of Ge contained in the islands is calculated by multiplying the island density in each sample by the average volume of an island in the sample, assuming a hemispherical island shape. The total amount of Ge in the islands of the unannealed sample in 5-6 (a) is equivalent to a uniform layer of Ge that is 1.2 nm thick per unit area. In comparison, the equivalent uniform layer of Ge for the annealed sample in 5-13 (a) is only 0.23 nm thick. However, we also know that the SiO_2 template uncovered by Ge islands is desorbed during the anneal step. This is expected to lead to the formation of a Ge wetting layer, which occurs in Ge on Si epitaxy. Assuming that a 3 monolayer thick wetting layer forms, and correcting for the area of the annealed sample where islands are present, increases the equivalent Ge thickness to 0.65 nm. This value is about half that of the unannealed sample, and the discrepancy is likely due to interdiffusion of Si-Ge that occurs during annealing. Performing the same calculation for samples 5-6 (b) and 5-13 (b), with 12 nm of Ge deposition, yields the same result. These calculations indicate that the reduction in Ge island density that occurs during annealing is due to the dissolution of Ge islands in forming a wetting layer and subsequent Si-Ge interdiffusion layer. This explanation is further confirmed by x-TEM analysis that is discussed later.

Some additional changes observed in the annealed Ge islands can be understood by comparison to previous studies of Ge on Si epitaxy. In these studies, Ge growth usually begins on a clean reconstructed Si surface. In contrast, the Si surface in our

annealing experiments already contains a pre-determined amount of Ge that is made up of islands, surrounded by the layer of chemical SiO_2. However, once the remaining SiO_2 layer is desorbed during annealing, the system then progresses toward equilibrium and should possess some features in common with Ge on Si epitaxy. For example, the smaller island density of $1.5x10^{10}$ cm^{-2} is contained in both annealed samples 5-13 (a) and 5-13(b), despite having different initial amounts of Ge deposition. This island density is within the range of 4×10^9 to 3×10^{10} cm^{-2}, commonly observed in the Stranski-Krastanov growth mode of Ge on Si.[166-168] However, this island density is also very close to the value of 1×10^{10} cm^{-2} estimated for the number of tilt misoriented Ge islands in the unannealed samples. This point will be further discussed below in the section on TEM analysis of annealed islands.

Another feature that the annealed island samples have in common with Ge-Si epitaxy is the formation of large Ge islands that are observed on samples having 18 and 25 nm of Ge deposition. These islands are not observed in the annealed samples with less deposition, and appear to require a critical amount of Ge for their formation. Figure 5-13 (c) shows that these large islands are dome-shaped and multifaceted, and surrounded by a sea of the smaller square shaped islands. This feature may be akin to the pyramid-dome-superdome transition observed with increasing Ge deposition in Ge-Si epitaxy.[169-171] Moreover, most of the large islands appear to have a trench around them that extends down into the surrounding Si. Although more extreme in the case observed here, this feature has also been observed in Ge on Si epitaxy, and has been explained as a stress-relieving effect.[168,169,172-174] The larger stress that exists at the island edges is found to be partially relieved by the formation of the trench based on Monte Carlo and finite element

modeling.[175,176] The stress at the island edge is also believed to enhance the diffusion of Si into the island, thereby creating a recessed region around the islands.[171,173,174] Next, two x-TEM samples are prepared from the annealed samples shown in Figure 5-13 (a) and (d) to further examine the Ge islands that exist after annealing.

Figure 5-14 (a) shows the x-TEM image of the sample in 5-13 (a) viewed along the [110] direction. The 4 islands in boxes are magnified in 5-14 (b-e) and the islands all appear to rest upon a GeSi alloy layer. A total of 15 islands are observed in this sample, and all possess a small amount of tilt misorientation to the Si. For example, the island in 5-14 (b) is tilted counter-clockwise about the [110] direction by about 4º, whereas the islands in 5-14 (c), (d), and (e) are tilted by 2, 5, and 3º, respectively. The dislocations located at the interface between the island and alloy layer in 5-14 (b) are pure edge type with a spacing that is approximately 5 nm. Figure 5-15 shows a high-resolution TEM image of the island in 5-14 (b) with edge dislocations marked. The spacing between the dislocations is consistent with the island misorientation being a pure tilt boundary according to Frank's equation: $\alpha = b/D$.[177] Here, α is the angle of misorientation, b is the Burgers vector of the dislocations ($b = a/2$ [110], where a is the lattice constant of Ge), and D is the spacing between the dislocations. By applying the measured dislocation spacing of 5 nm, the resulting misorientation angle is 4.6º, in close agreement with the value measured in the TEM image. The dislocation spacing in the islands shown in 5-14 (c-e) is much closer, ranging from 1.5 to 3 nm apart. This suggests that there is also a small degree of twist misorientation associated with these islands, and they form a more complicated boundary structure with the underlying Si-Ge alloy layer. Next, we discuss the composition and defect density of the Si-Ge alloy layer.

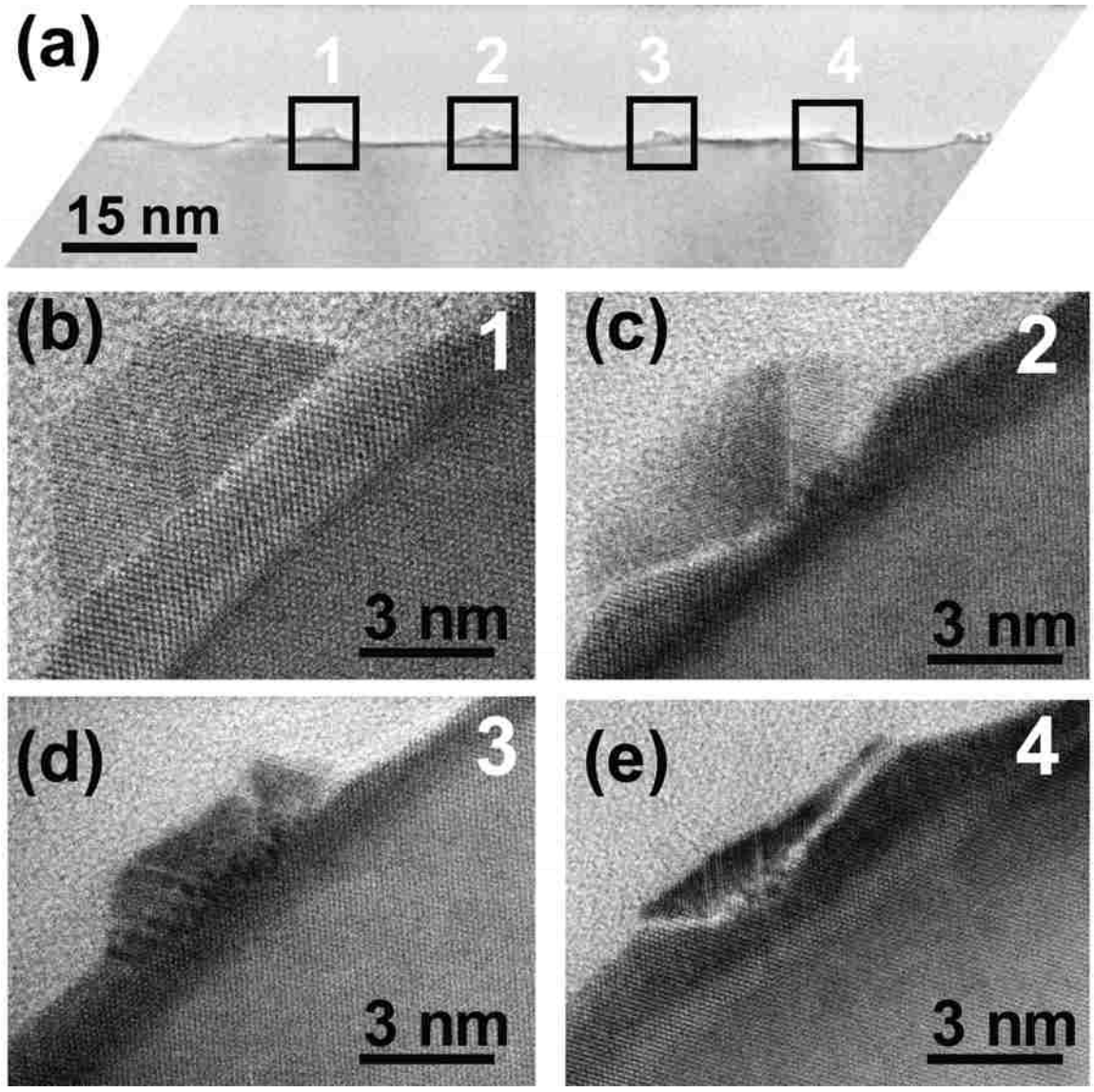


Figure 5-14. Cross-sectional transmission electron microscope images of the annealed islands with 8 nm of initial Ge deposition. Image 5-14(a) is a low-resolution image showing the morphology of the surface. Images 5-14(b-e) are high-resolution images of the islands 1 through 4 shown in image 5-14(a). The islands rest upon a Ge-Si alloy layer and are slightly misoriented with respect to the Si substrate.

We use EDS to estimate the atomic percent of Ge in the Si-Ge alloy layer, which is thickest directly beneath the islands, and also between the islands where it is thinner. The measurement was performed in STEM mode using a 1 nm probe size. A total of 10, 000 counts are collected at each point labeled 1 through 5 in Figure 5-15. The K_{GeSi}

factor used to quantify the Ge and Si composition is 1.91, and is calculated by the Oxford INCA EDS software. The Ge compositions at points labeled one through three in Figure 5-15 are 63, 44, and 12%, in turn. The Ge fraction at point four is below the detection limit of about 1 % for the EDS technique. The measurement made at point five is 25 % Ge, and is taken 2 nm below the surface and further away from the island where the alloy layer is thinner. Ten additional EDS measurements are made at 2 nm below the surface along the [110] direction.

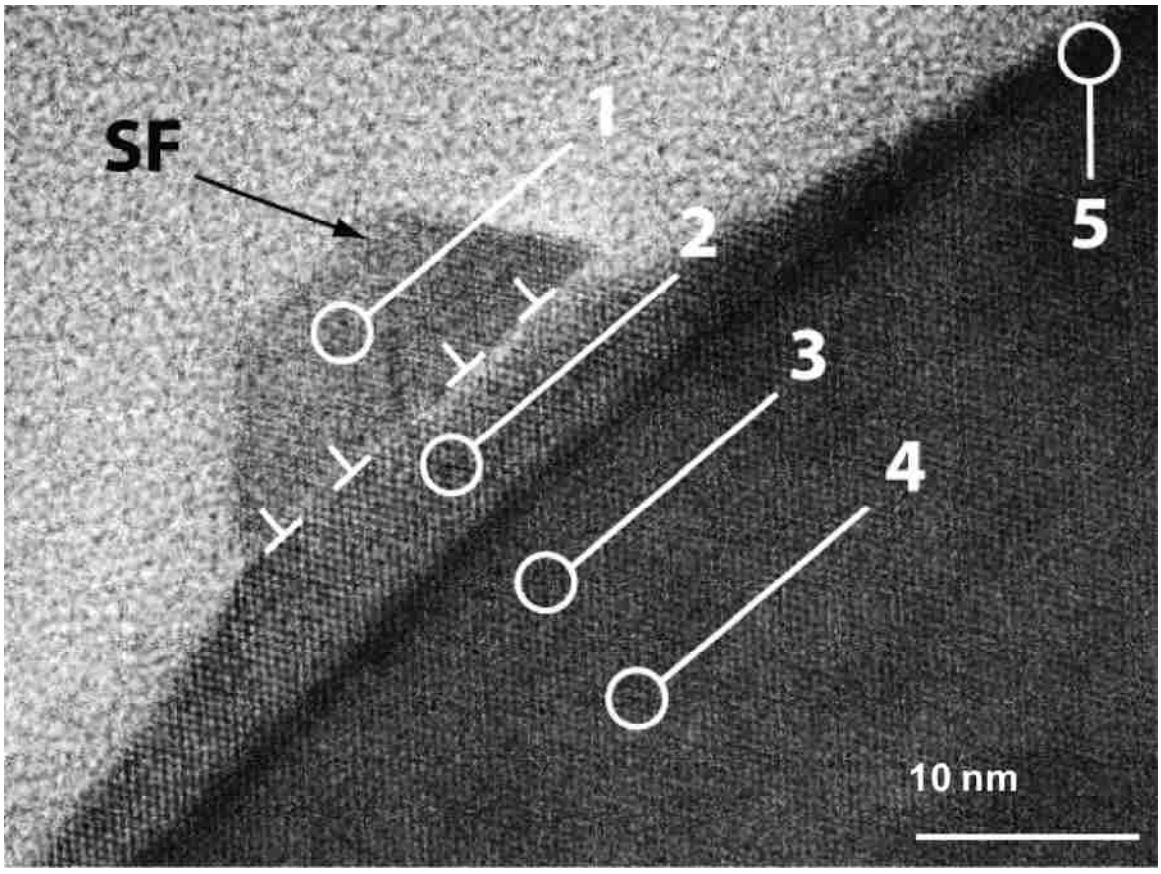


Figure 5-15. High-resolution cross-sectional transmission electron microscope image of island number 4, from Figure 5-14(a). This island is found to possess a small angle tilt boundary with the Si, with an edge dislocation spacing of 5 nm. The numbered regions correspond to locations where the composition is measured using energy dispersive spectroscopy.

These measurements are made between the islands, where the alloy layer is thinnest, and show that the average Ge content of the layer in this region is 22 ± 7 %.

The value of 63 % Ge averaged over the Ge island at point 1 is in qualitative agreement with composition of Ge-Si islands measured in the TEM using EELS. In that study, the Ge composition in the islands is reported to be 40% for growth at 973 K.[178] The measured composition of 22 % found in the thinner part of the GeSi alloy layer is also in good agreement with a finding of 28 % Ge in Ge-Si islands annealed at 1073 K.[179]

The composition of the GeSi alloy layer that exists between the Ge islands that remain after annealing is used to estimate the amount of Ge that is consumed in forming the alloy layer in this region. Assuming that the GeSi alloy layer is 2 nm thick and is composed of 22 % Ge, the equivalent thickness of pure Ge consumed is equal to 0.37 nm, after correcting for the area taken by the Ge islands. This value closely accounts for the difference observed in the amount of Ge that is contained within islands before and after annealing that was found from the earlier calculations based on the SEM images of the average island density and diameter. Therefore, it appears that the 16-fold reduction in island density observed after annealing is accounted for by dissolution of islands in forming the GeSi alloy layer.

The measurements of the composition and lattice spacing of the alloy layer are also used in conjunction to estimate the strain within the layer. Measurements of the (-11-1) lattice fringe spacing are made within the thicker part of the alloy layer that exists below the Ge islands. For example, the measured lattice fringe spacing of the layer shown at point two in Figure 5-15 is 0.318 ± 0.002 nm. This leads to a value of 35 ± 14 % Ge composition using Vegard's law and assuming complete relaxation of the layer.

This result compares favorably with the value of 44% measured using EDS and falls within the margin of error for the measurement based on (-11-1) lattice fringe spacing. The agreement between the measurements suggests that the alloy layer is fully relaxed, even though the thickness of this layer is well below experimentally measured values for the critical thickness for plastic deformation.

The reported values for the critical thickness of $Ge_{0.44}Si_{0.56}$ and $Ge_{0.22}Si_{0.78}$ on Si are 15 and 100 nm.[180] These compositions correspond to the alloy layer beneath the island shown in Figure 5-15, and for the alloy layer that exists between the islands. However, the estimated thickness of these layers is 5 and 2 nm, respectively. These layers are well below their critical thicknesses; however, it is likely that the high annealing temperature of $0.88T_m$, where T_m is the melting temperature of bulk Ge, overcomes the energy barriers to plastic deformation. The equilibrium edge dislocation spacing for relaxed layers of $Ge_{0.44}Si_{0.56}$ and $Ge_{0.22}Si_{0.78}$ on Si are 22 and 43 nm. A single dissociated dislocation was detected in the thicker part of the alloy layer beneath 2 of the 15 total islands examined in x-TEM images. There are no dislocations detected in x-TEM images taken of the thinner part of the alloy layer between the islands, but this is likely due to the limited area of sampling. Next, we discuss the large Ge islands observed after annealing the sample with 25 nm of initial Ge deposition.

The x-TEM image shown in Figure 5-16 corresponds to the sample in Figure 5-13 (d) containing large Ge islands. Orientation analysis of these islands shows that they are epitaxially aligned with the Si. They contain a large number of threading dislocations that appear to bend toward the nearest facet plane at the island surface. This can be attributed to image forces on the dislocation, and is observed in Ge on Si epitaxy.[47] In

addition, the trenches around the large Ge islands observed in the SEM images also appears to the right of the Ge island, and extends 30 nm below the Si surface. The alloy layer beneath the large islands is up to 60 nm thick, and is very uneven.

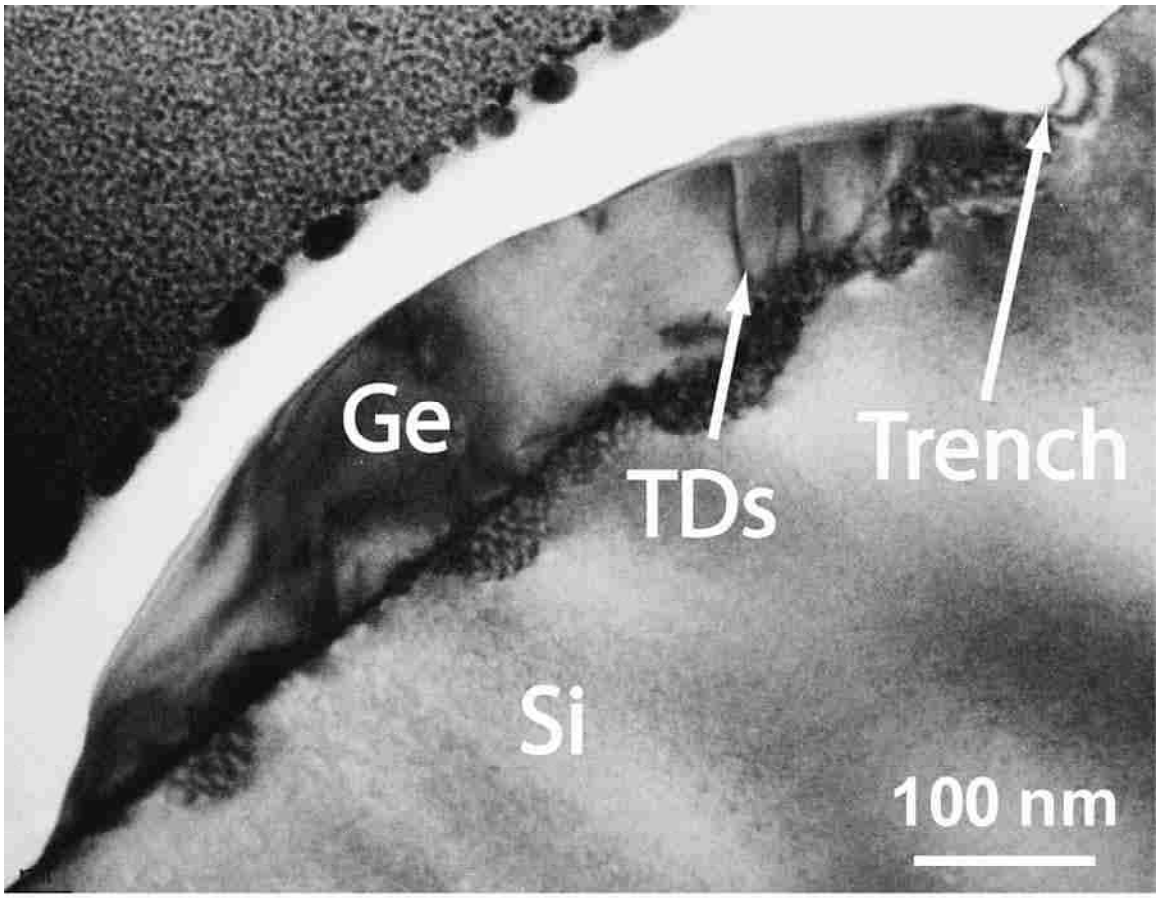


Figure 5-16. Cross-sectional transmission electron microscope image of large Ge island that forms after annealing the sample with 25 nm of initial Ge deposition. The island is epitaxially oriented to the Si and is contains threading dislocations. The trench that extends down into the Si is shown to the right of the island.

The kinetics and mechanism of the formation of these large islands is unknown. Interestingly, their density does not appear to depend on the initial size and density of the Ge islands before annealing. For example, the islands shown before annealing in Figure

5-6 (c-d) differ in both average island size and density, yet the density of the large islands is the same after annealing these samples. The large islands only differ in size, with the islands being larger in the sample having the greater amount of initial Ge deposition.

The formation of large islands in Ge -Si epitaxy has been observed and attributed to strain relaxation via dislocation nucleation and Si incorporation into Ge islands. The large trench in the Si is also attributed to stress relaxation and Si incorporation via surface diffusion, and suggests that the large islands must also contain a large percentage of Si, although the composition is not measured. In addition, the alloy layer between the large islands does not greatly differ in thickness from the sample annealed after only 8 nm of Ge deposition. It ranges from 3 to 5 nm in thickness, and shows qualitatively that most of the 25 nm of initially deposited Ge is contained in the large islands. In addition, small islands with small tilt misorientation are observed between the large islands. These small islands do not appear to differ from the ones observed in the annealed sample with only 8 nm of initial Ge deposition. It also appears that the large Ge islands, during their formation, must either consume or overgrow the small misoriented islands. The high density of twins is longer observed at the Si-Ge interface after annealing both samples with 8 and 25 nm of initial Ge deposition.

It now appears that the mechanism for the removal of twins during annealing is the dissolution of the majority of the Ge islands. However, it remains a possibility that twins are annealed out of the islands before the SiO_2 template is desorbed and Ge diffuses from the islands to the freshly exposed Si. The removal of twins by annealing has previously been reported, as well as the realignment of small misoriented islands upon annealing. To determine whether twins are removed by annealing, and to gain some

insight into the process that leads to the drastic changes in island morphology upon annealing, we have conducted the following experiment. The sample shown in Figure 5-6 (d), with 25 nm of initial Ge deposition, is capped using a spin-on-glass (SOG) polymer. The polymer is composed of methyl-siloxane and is stable at high temperatures. The sample is then annealed at 1073 K for 30 min and analyzed using x-TEM. Figure 5-17 shows the resulting sample after annealing.

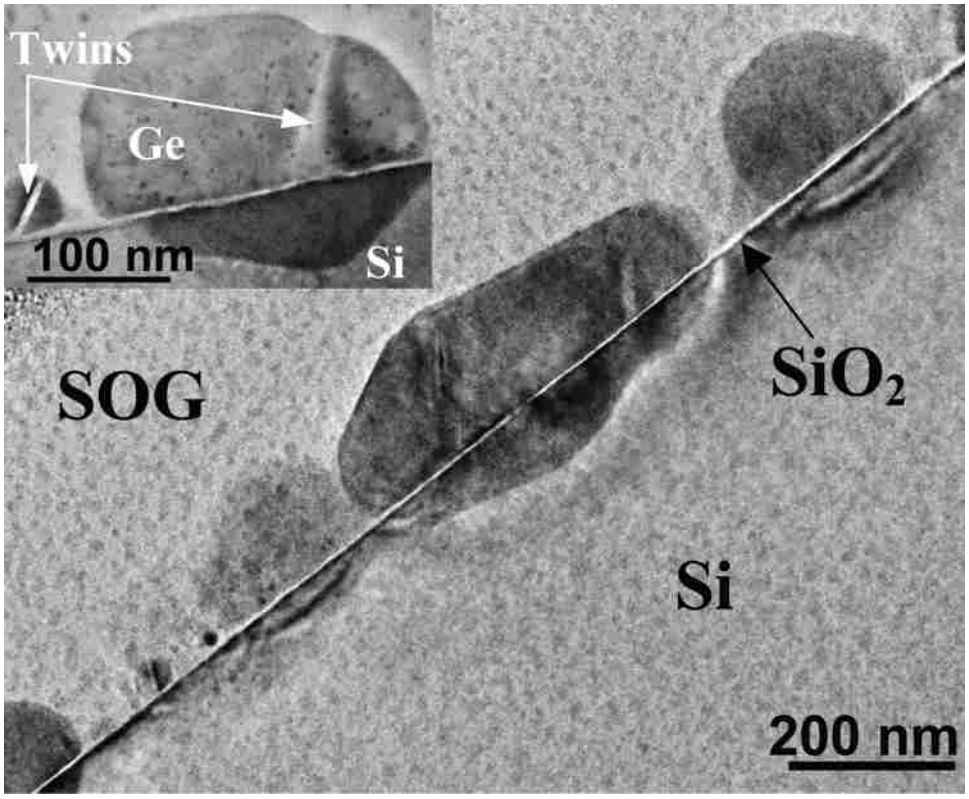


Figure 5-17. Cross-sectional transmission electron microscope image of Ge islands with 25 nm of initial Ge deposition. The islands are then capped with spin-on-glass and then annealed. Stacking faults and twins remain within the islands, and their morphology is unchanged from the pre-annealed state. The chemical SiO_2 layer is also preserved during annealing. The inset shows a close-up view of one of the islands and reveals the GeSi alloy layer formed beneath the island.

The island density and morphology is unchanged prior to annealing. In addition, twins and SFs are observed within the islands. The inset in Figure 5-17 shows the formation of a GeSi alloy layer beneath the islands. In contrast to the uneven nature of this layer observed in the uncapped annealed sample in Figure 5-17, this alloy layer in the capped samples is quite uniform and mirrors the shape of the islands themselves. Lastly, the SiO_2 template remains intact and is observed at the GeSi interface, where it has a lighter contrast than the SOG.

The result of the capped-annealed experiment demonstrates conclusively that the mechanism of SF removal is the dissolution of most of the Ge islands in forming a GeSi alloy layer during annealing. Furthermore, the result of this experiment shows that surface diffusion is the primary mode in effecting the changes in island density and morphology that take place upon annealing. Surface diffusion likely begins to transfer Ge from the islands to the surrounding Si once the SiO_2 template is desorbed.

We previously reported that the SiO_2 template is preserved during annealing if it is capped with a 100 nm thick layer of Ge[56], as the SOG capped annealing experiment also shows. Based on this observation, we assumed that the SiO_2 layer covered by Ge islands during the initial Ge deposition would be stable against desorption. However, no remaining SiO_2 is detected in any of the x-TEM images of the uncapped annealed Ge islands, including beneath any of the islands that remain exist after annealing. This observation suggests that the SiO_2 can desorb through thinner layers, or becomes uncovered during annealing.

Removal of the SiO_2 is expected to have two important effects with regard to explaining the dissolution of many of the Ge islands. First, the removal of the SiO_2 layer

will generate a large strain between the epitaxial Ge islands and the Si. Second, removal of the SiO_2 exposes the Si surface and will promote transfer of Ge by surface diffusion from the islands to the Si to form a Ge wetting layer. In addition, intermixing of Ge and Si has been observed to reduce the aspect ratio of Ge islands on Si, and even causes decay of the islands back to a nearly planar film.[166,171,181] The combination of these factors can lead to the dissolution of Ge islands upon annealing. Furthermore, as Ge transfers to the Si, the high temperature anneal should also promote relaxation of the strain that builds by plastic relaxation. This conjecture is consistent with the combination of composition and lattice fringe spacing measurements described earlier, and with the presence of dislocations that are detected within the Si-Ge alloy layer. Figure 5-18 (a-c) pictorially represents the processes that are believed to lead to the observed island morphology and Si-Ge alloy layer.

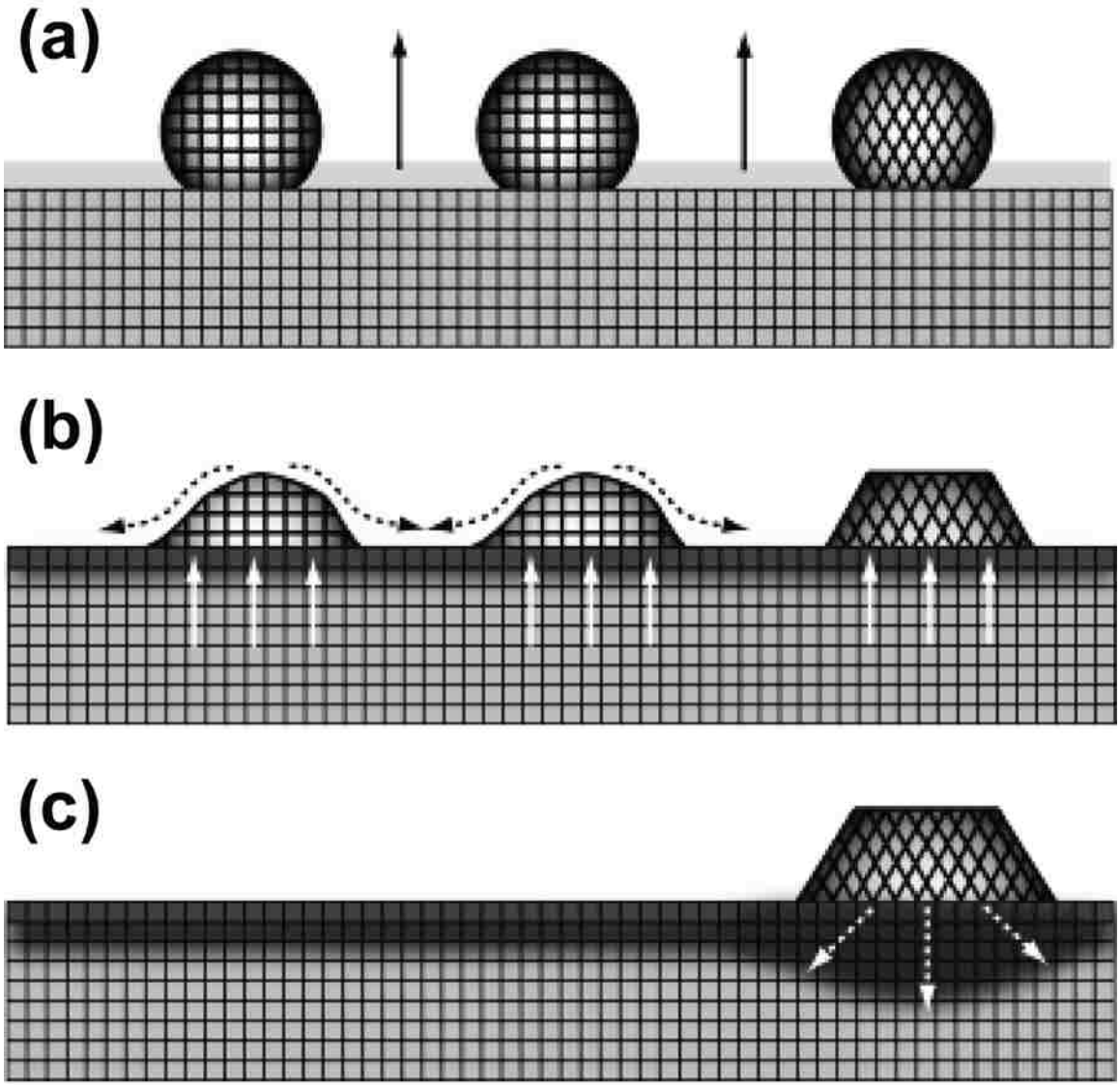


Figure 5-18. Depiction of the evolution of the Ge islands during annealing. Image 5-18(a) shows the nucleation of the Ge islands within the openings in SiO_2. The cross-hatch island indicates a tilt misorientation with respect to the Si substrate. Annealing causes desorption of the SiO_2 layer. Image 5-18(b) represents the surface diffusion taking place from the epitaxial Ge islands to the exposed Si substrate, as well as interdiffusion of Si and Ge. Ge also migrates by surface diffusion to the misoriented island. Image 5-18(c) shows the growth of the misoriented islands and the larger GeSi alloy layer that forms beneath the island.

The reason that approximately 16 % of the Ge islands nucleate in twin relationships to the Si and 8 % nucleate with small tilt misorientation to the Si is not presently understood. The mechanistic details describing how epitaxy occurs within the

confined openings that form in the SiO_2 is lacking. These details are currently being investigated using molecular dynamics simulations.

5.3.7 Conclusions of Annealing Ge Islands

We have determined the origin of the high density of twin/SF defects found in Ge films created from the nucleation and coalescence of Ge islands within small openings in SiO_2. The twins originate from the nucleation of Ge islands in twin relationships to the Si within the SiO_2 windows, and form coherent twin boundaries when merging with other Ge islands that are epitaxial to the Si. In addition to the twin oriented Ge islands, many of the Ge islands nucleate with a small misorientation angle to the Si. Annealing the Ge islands leads to the desorption of the SiO_2, and the transfer of most of the Ge in the islands to the freshly exposed Si. Intermixing then leads to the formation of a strain relaxed GeSi alloy layer, and subsequent growth results in Ge films free of twins. Dissolution of most of the Ge islands appears to be the mechanism by which twins are removed. This is confirmed by the experiments in which the initially deposited Ge islands are first capped with SOG before annealing to prevent surface diffusion and SiO_2 desorption. Subsequent analysis after annealing reveals that the twin/SF defects remain in the islands, and the islands retain their overall shape and orientation prior to annealing. In addition, some very large Ge islands are formed after annealing samples that have a critical amount of initial Ge deposition. The formation of theses large islands is not currently well understood, but the mechanism of their formation may be analogous to the shape transitions observed in pyramid-dome-superdome formations observed in Ge-Si epitaxy. The large islands found after annealing are oriented to the Si and contain

threading dislocations, in agreement with the findings of Ge-Si growth directly on Si, whereby large islands form after the nucleation of dislocations relaxes the strain buildup from the lattice mismatch. Next, we report the characterization of Ge films formed from additional growth performed after annealing Ge islands nucleated within nanoscale windows inSiO_2.

5.3.8 Characterization of Ge Films

The x-TEM image shown in Figure 5-19 is of a Ge film formed after annealing Ge islands nucleating within openings in chemical SiO_2. The image reveals the presence of a large number of TDs that exist within 200 nm of the Ge-Si interface.

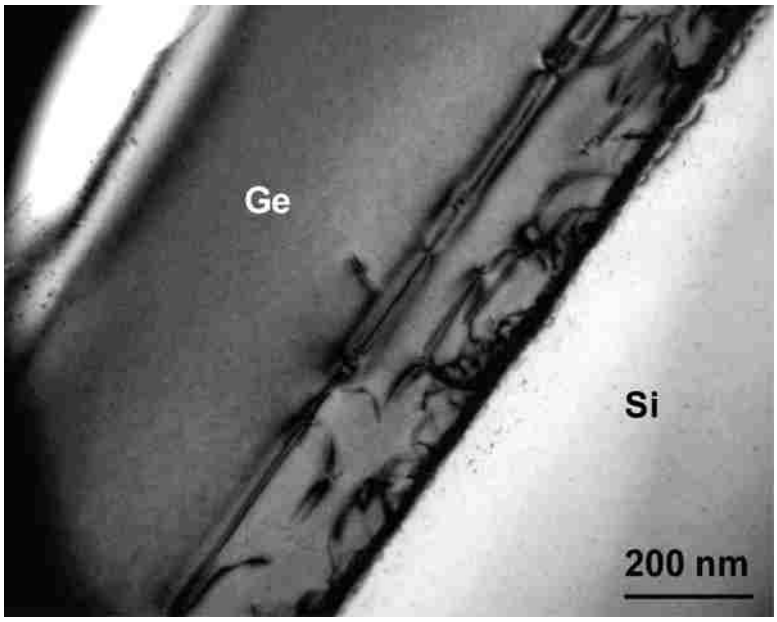


Figure 5-19. Cross-section transmission electron micrograph of a Ge-on-oxidized Si film that is annealed at 1073 K for 30 min after deposition of 10 nm Ge. A tangled network of threading dislocations now appears within 200 nm of the Ge-Si interface.

The existence of TDs at the GoS interface is in contrast to the high density of twins previously shown in Figure 5-4 to exist at the GoS interface for samples that are unannealed. Most of the dislocations terminate within a tangled network close to the Ge-Si interface, but occasionally one is seen to propagate toward the surface of the Ge. The TDD that intersects the film surface is too low to be accurately determined from the x-TEM images. However, pv-TEM images, such as that shown in Figure 5-20, consistently show that the TDD within the middle of the Ge film is 5.3×10^{7} cm^{-2}.

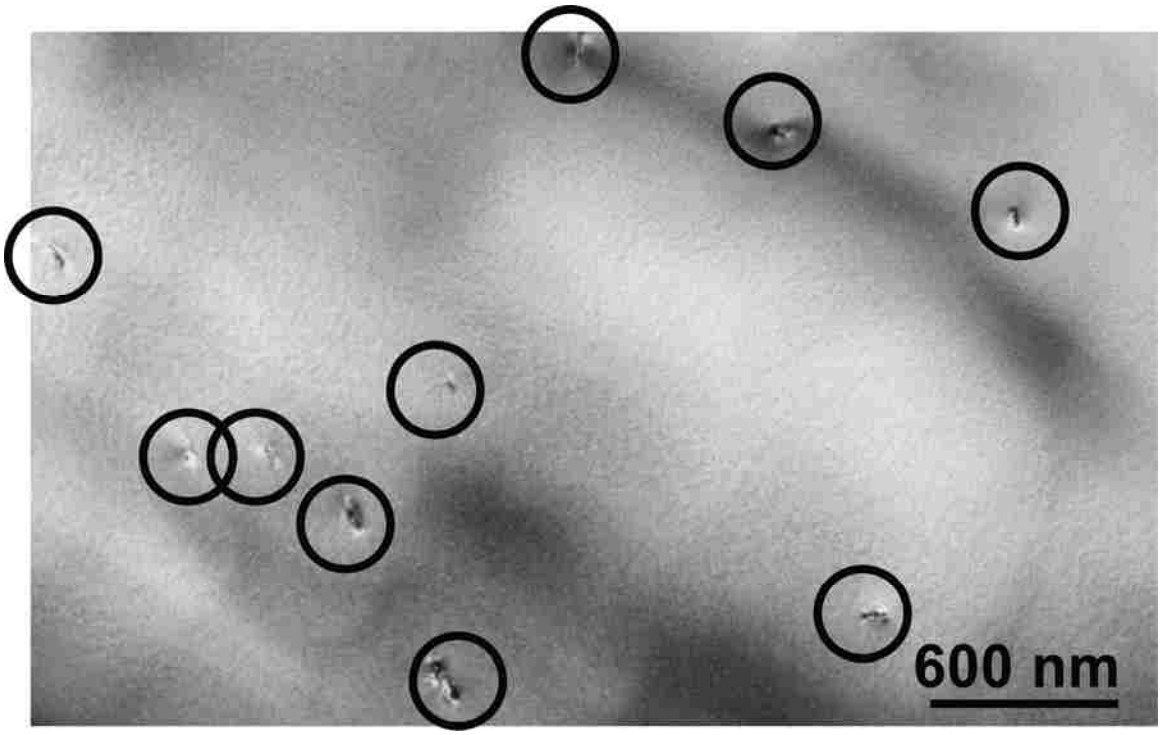


Figure 5-20. Plan-view transmission electron micrograph showing dislocations in a Ge-on-oxidized Si film that is annealed at 1073 K for 30 min after deposition of 10 nm Ge.

The TDD value obtained with pv-TEM is now compared to the TDD value obtained using EPD measurements. Figure 5-21 is an SEM image showing an annealed Ge-on-oxidized Si sample that is dipped for 30 s in a solution of 2:1:20 volumetric parts

of 49 wt. % HF: HNO_3: acetic acid. The SEM image shows that the pits are square shaped and provide good counting statistics that result in an EPD value of 5.7×10^7 cm^{-2}, highly consistent with pv-TEM images. Consequently, EPD is shown to be a technique that can provide an accurate value of the TDD in Ge films as long as the pits can be clearly resolved. This restriction puts an upper bound on the TDD of perhaps 5×10^8 cm^{-2} and complements the higher TDD densities that can be more accurately measured using TEM.

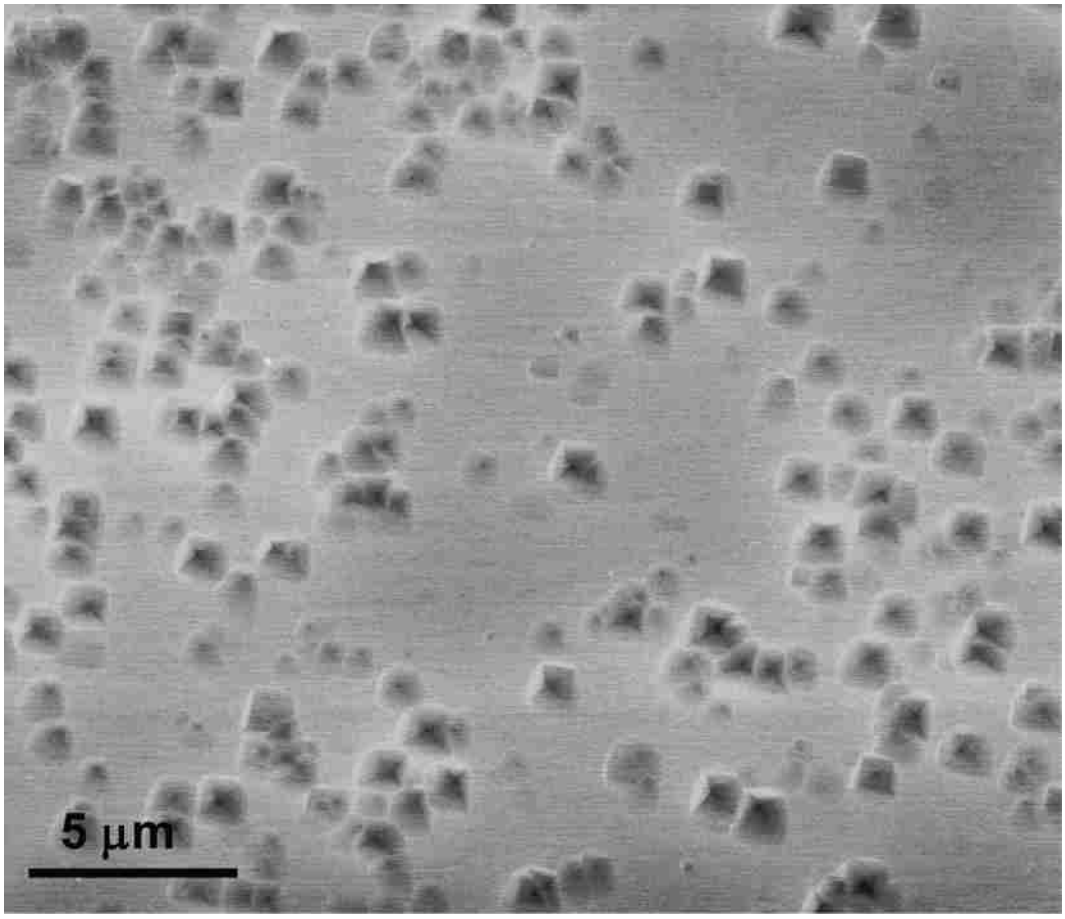


Figure 5-21. Scanning electron micrograph of annealed Ge-on-oxidized Si film etched for 30 s revealing square shaped etch pits.

The TDD in Ge films formed after the annealing step is 5×10^7 cm^{-2}. This value is comparable to well annealed Ge on Si films and is 1-2 orders of magnitude less than Ge growth on Si without annealing. The segments of misfit dislocations are much longer than in unannealed Ge on Si growth and exist mainly within a region extending 200 nm from the interface, as shown in Figure 5-19. The dislocation structure at the interface bears some resemblance to that found in graded Ge_xSi_{1-x} structures. This resemblance can be understood based on the results shown after annealing 8 nm of initial Ge deposition. The results show that growth that occurs after annealing will take place on a strain relaxed $Ge_{0.22}Si_{0.78}$ alloy layer. Fewer new dislocations will be required to relax the additional growth, allowing those dislocations to glide further before becoming blocked or entangled with one another. Next, several methods are investigated for cleaning and passivating the Ge surface after the planarization step.

5.3.9 Cleaning and Passivating the Ge Surface for III-V Growth

Previously reported methods of producing a clean Ge surface generally fall into either one of two categories: wet-chemistry methods (e.g., dilute HF, HCl, H_2O_2, and NH_4OH)[182-187] and dry chemistry methods [e.g., UV-generated ozone[188,189] or oxygen plasma exposure[190]]. In general, these methods follow the Shiraki process of preparing clean Si substrates, where the last step produces a thin oxide layer that is thermally decomposed at high temperatures.[120,190] Producing clean Ge surfaces using aqueous methods presents additional challenges because the Ge oxide is a mixture of GeO and GeO_2, with GeO_2 being water soluble.[191] In addition, both HF[187,192] and NH_4OH[190] can cause significant Ge surface roughening. Overall, previous studies of Ge surface

cleaning methods using scanning tunneling microscopy report 0.03-0.08 ML of residual carbon on the surface of the Ge, even after desorbing the Ge oxide.[183,186,190] Gan *et al*. also found that the fraction of carbon remaining after oxide desorption scales with the initial amount of carbon on the germanium oxide surface.[186] In our study, XPS spectra are collected at a take-off angle of 15º, defined here as the angle between the surface and the detector, to quantify the fraction of carbon present at the Ge surface for the following five cleaning methods: 1:10 HF-DI water, 1:10 HCl- DI water, 1:10 H_2O_2-DI water, DI water rinse, and oxygen plasma exposure.

Table 5-1 shows the surface composition for the different cleaning methods. The atomic fractions of Ge, C, Cl, and O are calculated using the atomic sensitivity factors found in Ref. 70. The fraction of C present on the surface is highest at 18% immediately after the polishing. The ratio of O to Ge is approximately 2 indicating that the germanium oxide is composed mainly of GeO_2. The polishing solution is itself a dilute H_2O_2, and after rinsing in the fresh H_2O_2 solution, the C fraction is reduced to 11%. In contrast, rinsing in DI water reduces the O-to-Ge ratio to 1.4, consistent with the water solubility of GeO_2, which leaves sub-stoichiometric germanium oxide on the surface.

Sample Preparation	Surface Composition (%)			
	Carbon	Oxygen	Germanium	Chlorine
Post-Polishing	18 ± 4	57 ± 2	25 ± 2	–
1:10 HF	14 ± 2	54 ± 1	32 ± 1	–
1:10 HCl	9 ± 2	35 ± 2	28 ± 1	28 ± 1
1:10 H_2O_2	11 ± 2	61 ± 4	28 ± 3	–
DI Rinse	12 ± 3	51 ± 2	37 ± 2	–
O_2 Plasma	6 ± 1	60 ± 1	34 ± 1	–

Table 5-1. The average and standard deviation of the chemical composition of the surface as revealed with x-ray photoelectron spectroscopy for different surface cleaning methods. The sample labeled "post polishing" has not undergone any cleaning treatment after the planarization step using dilute H_2O_2. Overall, the O_2 plasma treatment results in the lowest residual carbon contamination on the surface.

However, the surface C is 12%, nearly unchanged compared to the H_2O_2 clean. The reduction in C from 18% to 12% upon removal of GeO_2 in DI water indicates that nearly 30% of the C is contained on or near the surface of the sample after polishing. The remaining C must either be contained within the insoluble Ge oxide and at the GeO_2-Ge interface. Another possibility is that some of the residual C is from the DI water itself. The cleaning solution least effective at removing C is the dilute HF. This is in agreement with the findings of Ravillon *et al*. who found that hydrogen terminated Ge has a greater affinity for hydrocarbon contamination.[192] The most effective wet cleaning solution at reducing C contamination is the dilute HCl, which shows a 9% C concentration and a Cl terminated surface. For the *ex-situ* O_2 plasma exposure, the sample is first rinsed in DI water to remove the bulk of the surface C and the GeO_2 layer. Overall, the O_2 plasma treatment is the most effective way of reducing surface C, in agreement with the study by

Chan *et al*.[190] The C concentration is reduced to 6 %, and some of the remaining C is likely due to the exposure to the ambient air while the sample is being transferred to the XPS chamber. Therefore, the DI rinse/O_2 plasma treatment is the method adopted here to clean Ge surfaces prior to GaAs growth. Next, III-V growth on the annealed Ge films is compared to growth previously obtained on unannealed Ge films that have twins.

5.3.10 III-V Growth and Characterization on Ge

For GaAs growth on engineered Ge/Si substrates, several engineering challenges still remain, including formation of APBs and surface roughness. First, the results are presented for growth performed at SNL following the procedure given in Section 5.2. Gallium arsenide is grown on Ge substrates on both nominal and 6-degree-offcut toward [110] to determine if APBs can be eliminated with the off-cut. Samples are etched in a mixture of 10 parts 49 wt% HF to 1 part 70 wt% HNO_3 for 10 s to reveal the APBs.[193] Figure 5-22 (a) shows that an APB density of $5x10^7$ cm^{-2} exists at the surface of 1 μm thick GaAs film grown on the nominal substrate. However, no APBs are detected on the vicinal Ge substrate as shown in Figure 5-22 (b).

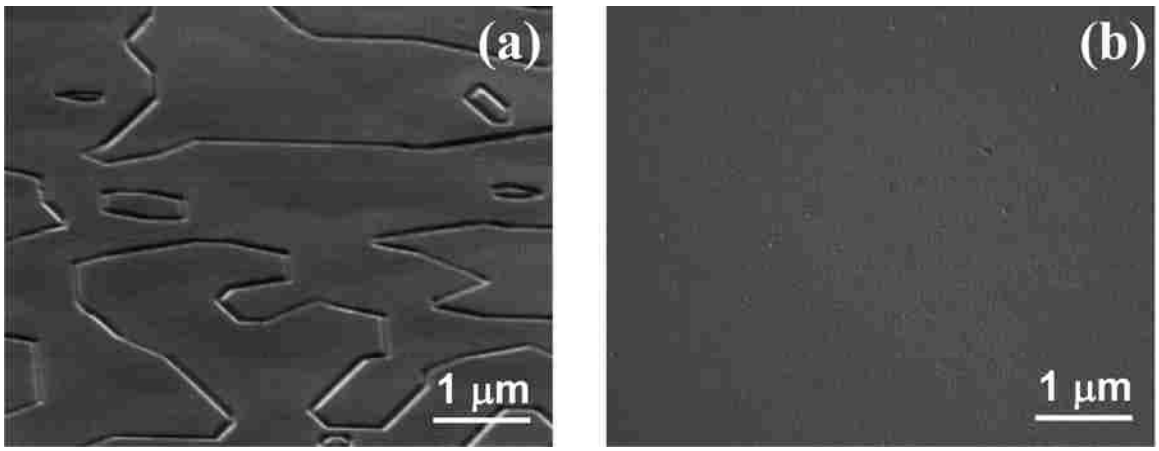


Figure 5-22. Scanning electron micrographs of the GaAs surface after etching for 5-22(a) nominal surface that reveals the antiphase boundaries in the sample, and 5-22(b) offcut 6 degrees toward [110] revealing that antiphase boundary formation is suppressed.

Figure 5-23 (a) shows an AFM image of a GaAs film grown on a 6-degree-offcut Ge substrate made by Umicore. The RMS value is 0.9 nm, and the FWHM is 49 arcsec using the (004) reflection in XRD. This is compared to GaAs grown on Ge-on-oxidized Si in the AFM image shown in Figure 5-23 (b).

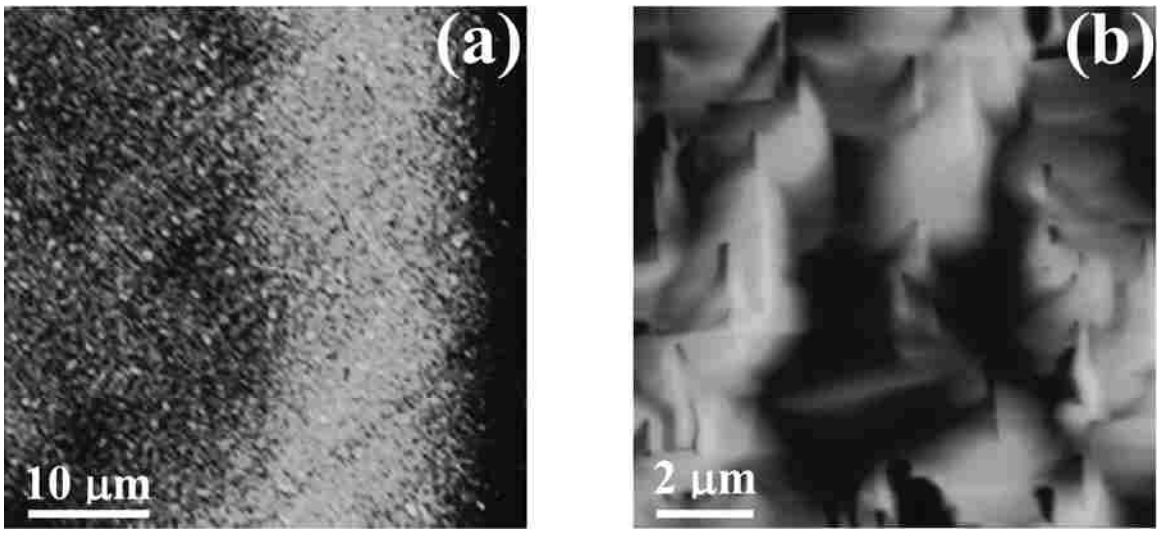


Figure 5-23. Atomic force micrographs of 5-23(a) GaAs layer grown using metal-organic chemical vapor deposition on a Ge wafer, and 5-23(b) GaAs layer grown on polished Ge-on-oxidized Si substrate. Image 5-23(b) reveals that the GaAs morphology closely follows that of the original Ge surface, showing the same raised lines due to the twins that terminate the Ge surface as seen in Figure 5-9(b).

The morphology of the GaAs closely follows that of the Ge surface, and shows the same raised lines attributed to twins in the Ge. The RMS roughness is 36 nm and the FWHM of the (006) GaAs reflection is 335 arcsec. These results suggest that the twins in the Ge either propagate into the GaAs layer, or produce APBs in the GaAs. The latter are likely due to the morphology of the twins as raised lines at the Ge surface, which would disturb the double step structure of the vicinal Ge surface.

Photoluminescence results are taken and compared in Figure 5-24 for a GaAs film grown on a GaAs substrate (····· dotted line), an offcut Umicore Ge substrate (– – dashed line), and GaAs grown on Ge-on-oxidized Si (— thick solid line).

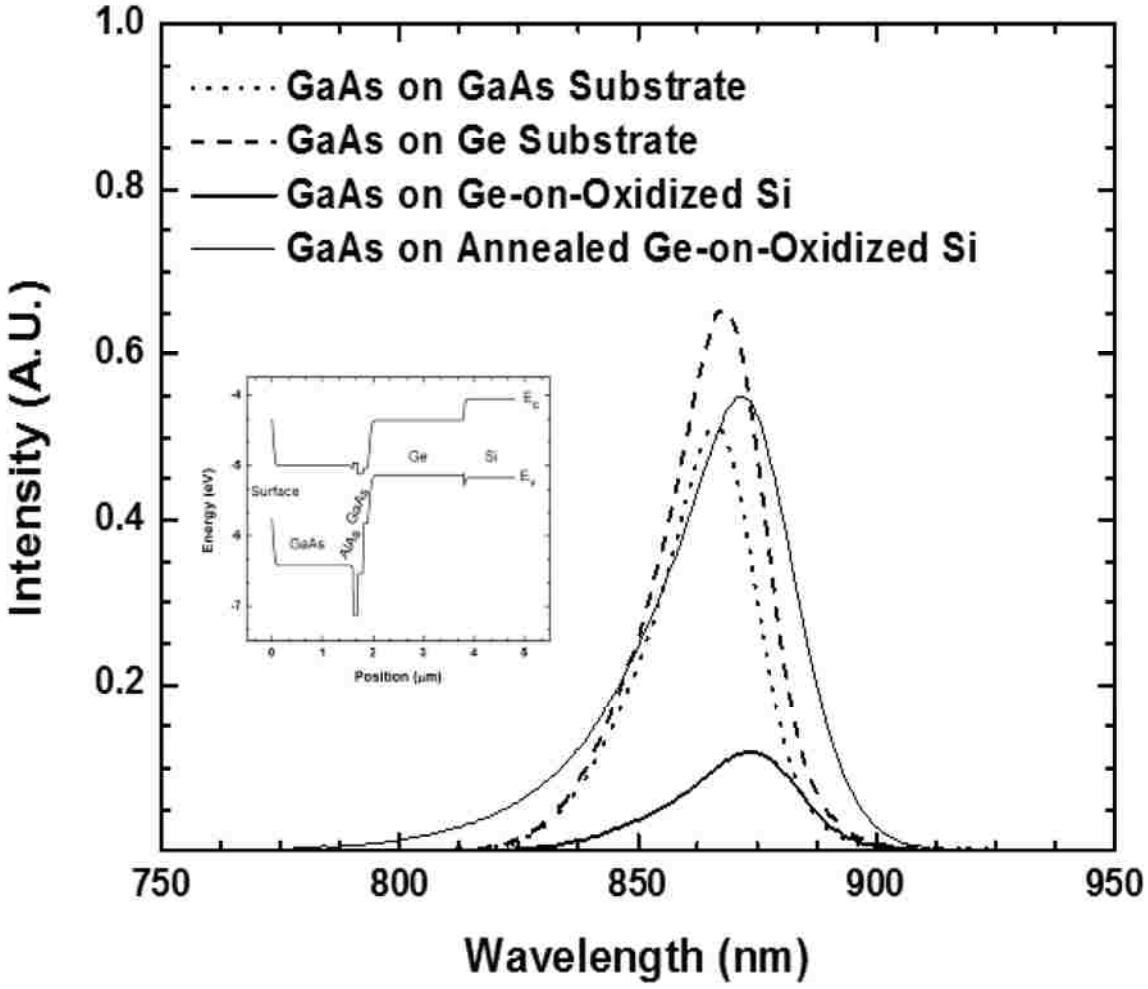


Figure 5-24. Room temperature photoluminescence spectra recorded for GaAs grown on Ge-on-oxidized Si compared to GaAs grown on a commercial Ge and GaAs wafer. The GaAs/Ge/oxidized Si sample intensity is 20-25% that of the GaAs grown on Ge and GaAs wafers. This reduced intensity is attributed to defects in the GaAs caused by the twin defect morphology of raised lines at the Ge surface. Evidence is provided by a comparison of PL intensity from GaAs grown on an annealed Ge-on-oxidized Si sample (heavy solid line) that is free of twins in the Ge. The photoluminescence intensity from this sample is comparable to GaAs grown on a GaAs substrate.

The inset in Figure 5-24 shows the energy band diagram of the test structure grown at SNL, with band energies shown relative to vacuum level. A film of GaAs grown on the Ge substrate has about 23% more intensity than GaAs grown on a GaAs substrate. This is likely due to the diffusion of Ge into the GaAs film where the Ge acts as a dopant

source providing centers for radiative recombination.[194-197] Overall, the intensity of the GaAs grown on Ge-on-oxidized Si is about one fourth that of GaAs grown on the commercial Ge substrate. Again, we attribute this reduced intensity to the twin defect morphology at the Ge surface, where twins may propagate from the Ge film into the GaAs layer, or produce APBs along the raised lines in the GaAs. Further evidence for the detrimental effect on the GaAs layer due to the SF morphology at the Ge surface is provided by the PL shown in Fig. 5-24 (— thin solid line). This sample is an annealed Ge-on-oxidized Si sample where the twins are eliminated from the Ge. The PL intensity for this sample is comparable to the structure grown on a GaAs substrate.

The image taken in Figure 5-25 (a) corresponds to an SEM image of the GaAs surface grown on Ge-on-oxidized Si, while Figure 5-25 (b) shows the corresponding CL image. The CL image shows that the radiative intensity from raised lines in the GaAs is greatly reduced compared to the surrounding regions, again confirming the detrimental effect on the GaAs layer from the twins in the Ge. However, further analysis such as TEM is needed to fully clarify the nature of the corresponding defect that is created in the GaAs.

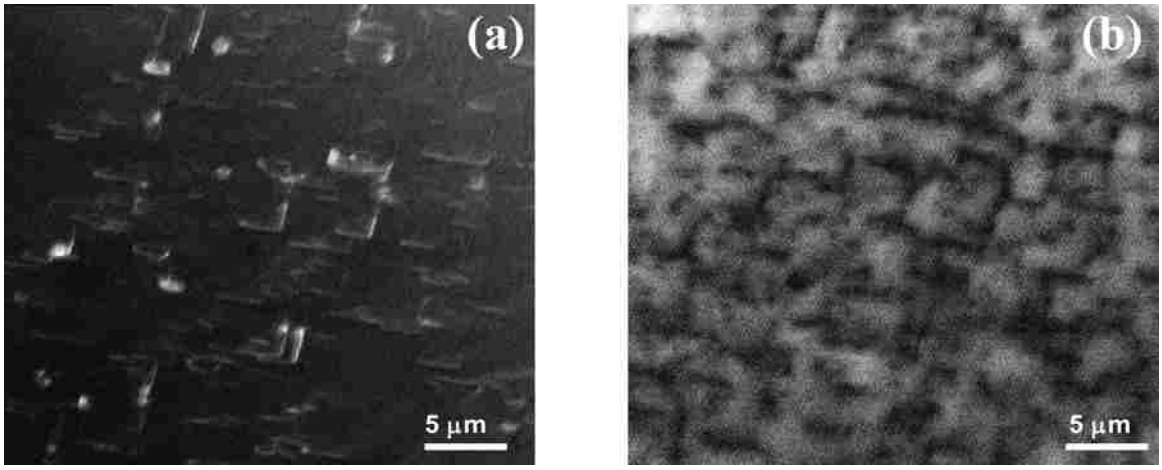


Figure 5-25. (a) Scanning electron micrographs of the GaAs on Ge-on-oxidized Si surface showing the raised lines that correspond spatially to the twins at the Ge surface, and 5-25(b) corresponding cathodoluminescence image revealing the non-radiative nature of the twin defect morphology in the GaAs layer.

The growth of III-V materials on the annealed Ge films have a much smoother surface morphology as compared to those grown on unannealed Ge-on-oxidized Si films that have twins.[55] The III-V growth on Ge films containing twins resulted in films with a root-mean-square (RMS) roughness of 36 nm.[55] In comparison, the AFM image in Figure 5-26 (a) shows the III-V structure grown at SNL on the annealed Ge-on-oxidized Si substrate that is free of twins. The RMS roughness is 3.45 nm, and the surface is similar in morphology to the same III-V structure grown on a 6^{o} offcut Ge substrate, which is shown in Figure 5-26 (b). In this case, the film RMS roughness is slightly lower at 1.35 nm.

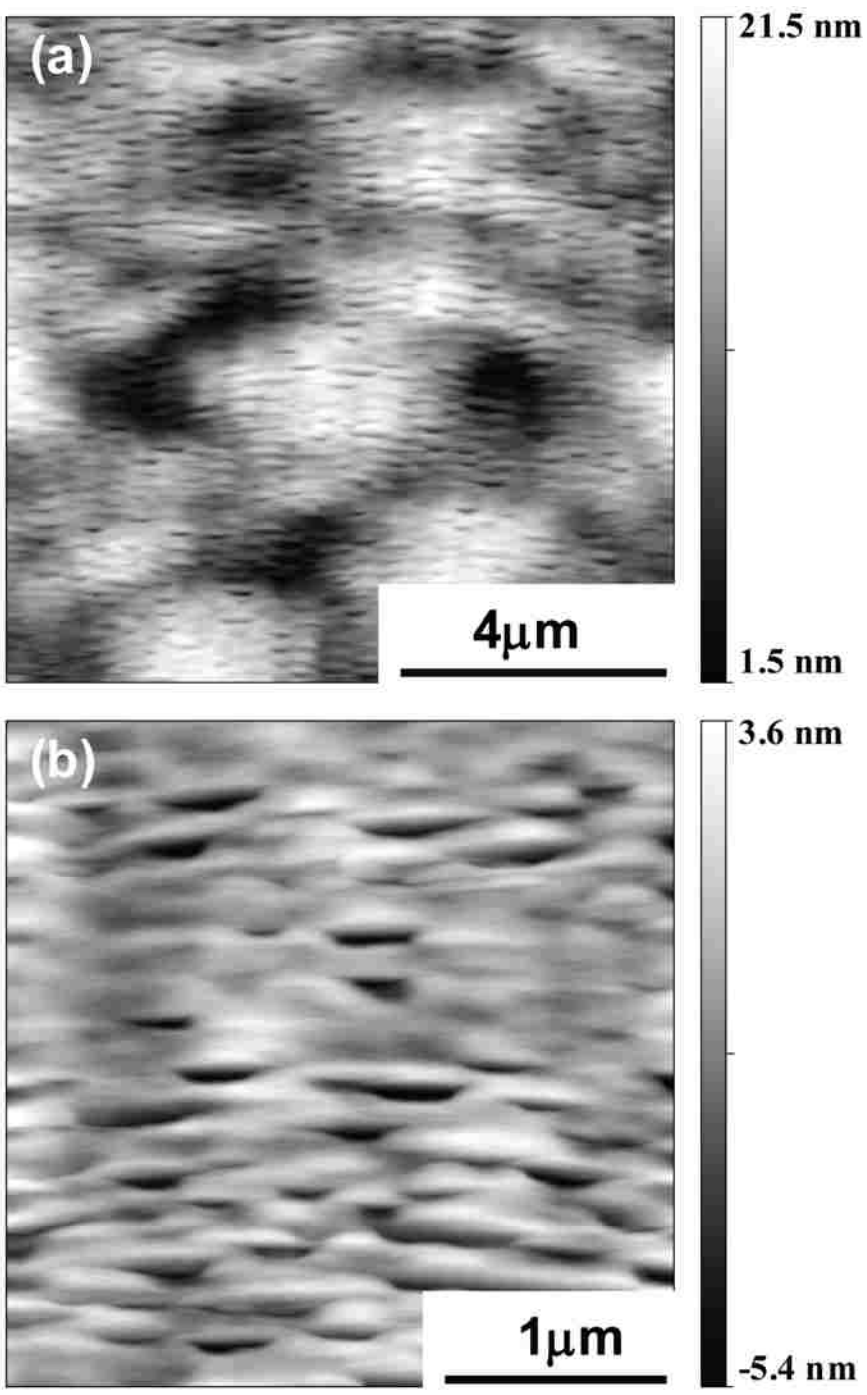


Figure 5-26. Atomic force micrographs of GaAs grown on 5-26(a) offcut Ge substrate, and 5-26(b) annealed Ge-on-oxidized Si.

A plot of the CL intensity versus energy is shown in Figure 5-27 for the III-V structure grown at SNL. The measurements are performed at NREL and are taken over an area of $100 \times 100\ \mu m^2$ at temperatures of 298 K and 15.5 K under nearly identical excitation conditions. The measurements indicate that the structure grown on the annealed Ge is comparable in intensity to that grown on the offcut Ge substrate. The III-V structure grown on the unannealed Ge sample that contains twins has an intensity only about 15 % compared to growth on the Ge substrate. This result is consistent with the previous PL intensity measurement shown in Figure 5-24 obtained for the same series of samples.[55] The III-V growth on the Ge substrate was verified to contain TDs below the detection limit of CL imaging; therefore, the fairly wide FWHM of the CL intensity peak measured at 298 K is likely due to high levels of unintentional doping. We speculate that Ge auto-doping during III-V growth is the likely culprit for the peak broadening. The low temperature measurements give a similar result but show both the excitonic transition for the annealed Ge-Si sample at 1.516 eV and a second transition at 1.496 eV. A second transition is often observed in low temperature measurements of GaAs on Si at about 19 meV below the excitonic peak.[198-200] This second peak can be attributed to the breaking of the light and heavy-hole valence band degeneracy caused by residual strain in the epilayer due to the mismatch in thermal expansion coefficient to the substrate.[198-200] However, the residual strain from thermal stress is also observed to cause a shift toward lower energy in the GaAs excitonic peak by about 25-30 meV[198-200], but this shift is not observed in the measurements shown here. Therefore, the lower energy peak is most likely due to recombination of a free electron-carbon acceptor pair.[199,200]

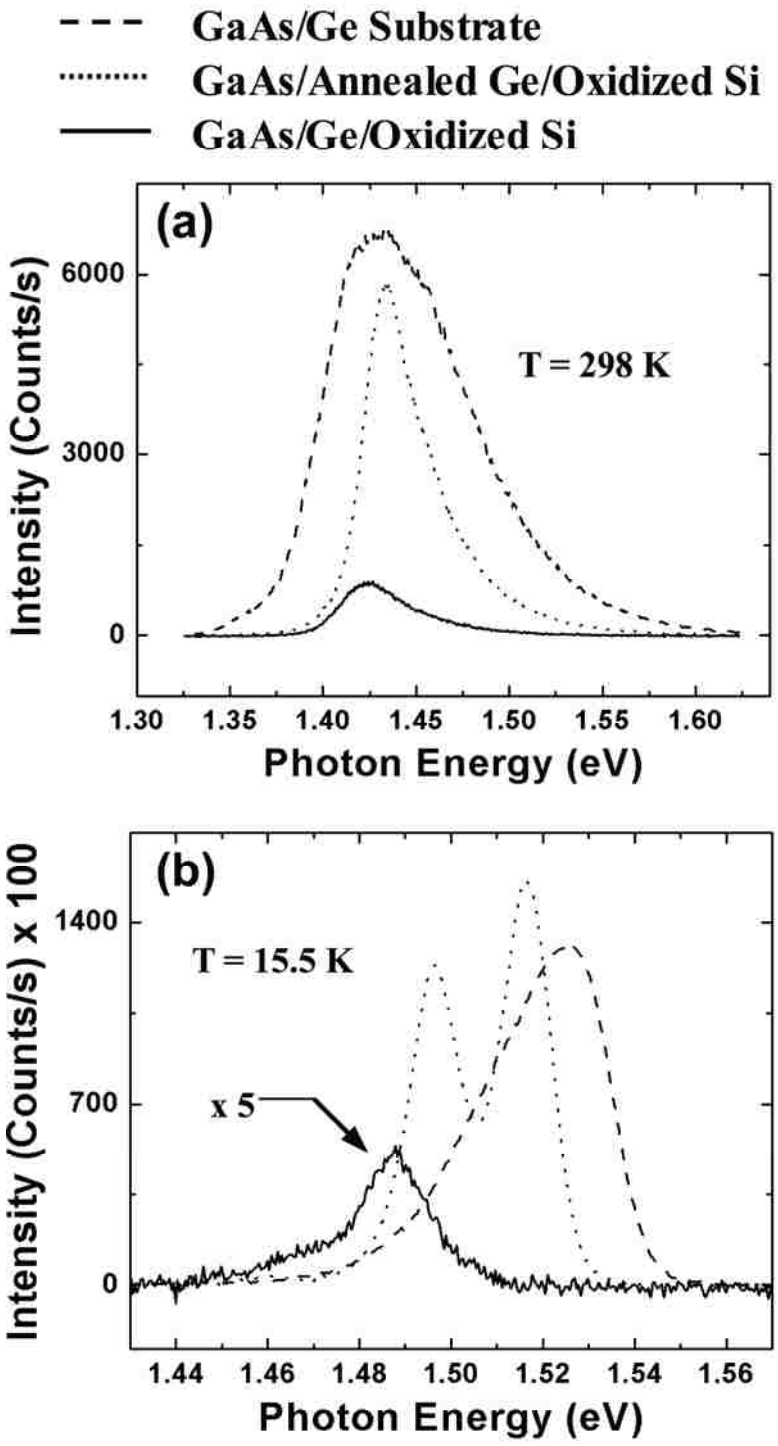


Figure 5-27. Plot of cathodoluminescence intensity versus energy taken at temperatures of 298 5-27(a) and 15.5 K 5-27(b) for GaAs on Ge substrate, and on both unannealed and annealed Ge-on-oxidized Si. The low intensity peak represented by the solid line is from GaAs on the unannealed Ge that contains twins. The higher intensity peaks given by the dotted and dashed curves are for GaAs on the annealed Ge film and Ge substrate, in turn.

A low-resolution CL image is collected and displayed in Figure 5-28 for the III-V structure grown at SNL on the annealed Ge on oxidized Si substrate.

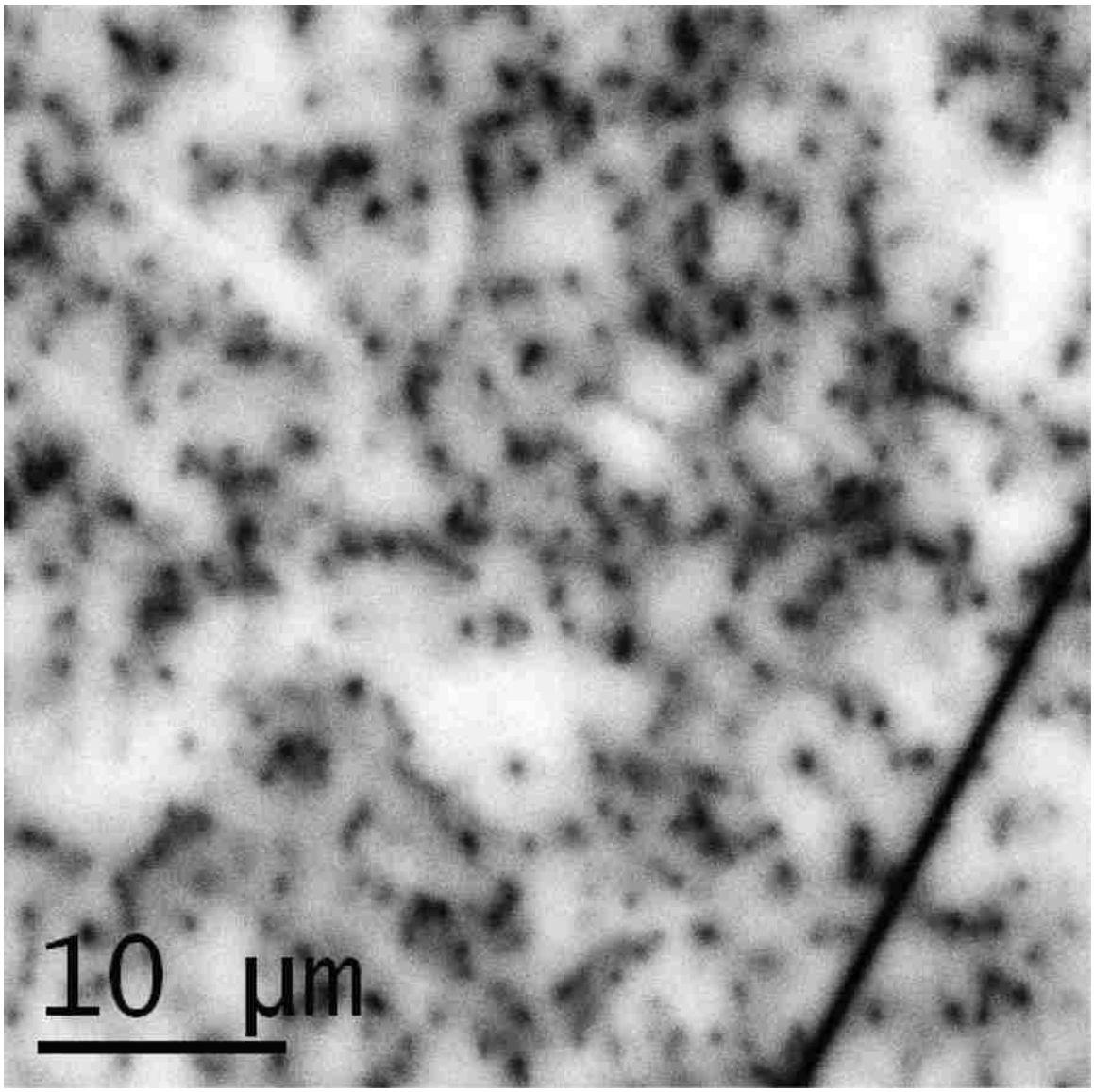


Figure 5-28. Cathodoluminescence image of GaAs grown on annealed Ge-on-oxidized Si and used to estimate the threading dislocation density in GaAs grown on annealed Ge-on-oxidized Si.

The image shows that the TDD in the GaAs films grown on the annealed Ge-Si is 2.5×10^7 cm^{-2}, or about one half the starting TDD in the Ge film. The image in Figure 5-28

shows no evidence of the SF lines found in the III-V growth on unannealed Ge shown in the CL image of Figure 5-25 (b). Low temperature (< 20 K) CL images of the same sample indicate that the many of the dislocations exist as dipole pairs separated by 200 to 300 nm. The CL intensity of the excitonic peak taken on the dislocations is reduced by 20 % compared to the background intensity. The results are now presented for the III-V structure grown at NREL that is described in Section 5.2.

The III-V structure grown at NREL is shown in the x-TEM image in Figure 5-29.

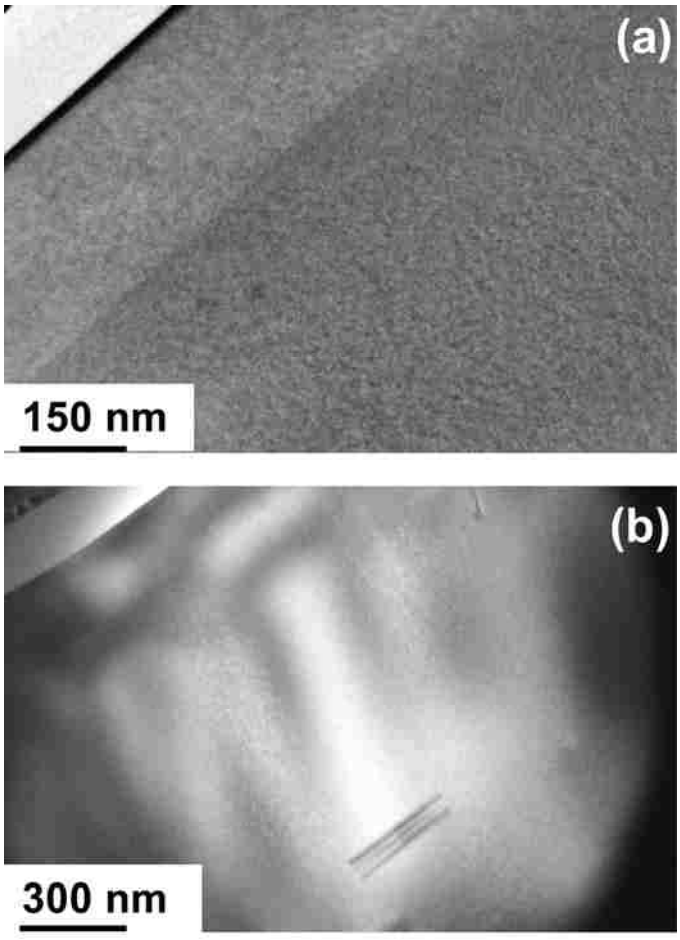


Figure 5-29. Transmission electron microscope image of National Renewable Energy Laboratory III-V structure grown on 5-29(a) Ge substrate, and 5-29(b) annealed Ge-Si substrate. No defects were detected in the sample shown in 5-28(a), while the sample in 5-29(b) contained some twin/SF defects along with a few dislocations.

This structure is grown on a GaAs, Ge, and annealed Ge-on-oxidized Si sample. The x-TEM image of Figure 5-29 (a) shows that the defect density of the NREL structure grown on the Ge substrate is below the resolution limit of the TEM. However, some twin/SF defects and a few TDs are seen in the same structure grown on annealed Ge-on-oxidized Si, and shown in Figure 5-29 (b). The defect density in the sample is estimated from TEM images to be 5×10^7 cm^{-2}.

The minority carrier lifetime of all three samples is measured using time resolved PL in conjunction with time-correlated singe photon counting. The time resolved PL kinetics shown in Figure 5-30, shifted for clarity, is similar for all three samples with expected maxima at 870 nm. However, the decay rate of the PL in the structure on annealed Ge-on-oxidized Si is much faster compared to growth on the Ge and GaAs substrates. Deconvolution is used to extract a lifetime of 67 ps for the annealed Ge sample compared to 4 to 5 ns for both Ge and GaAs substrates. Clearly, the quality of the annealed Ge must be further improved to be viable as a virtual substrate for minority carrier devices such as solar cells.

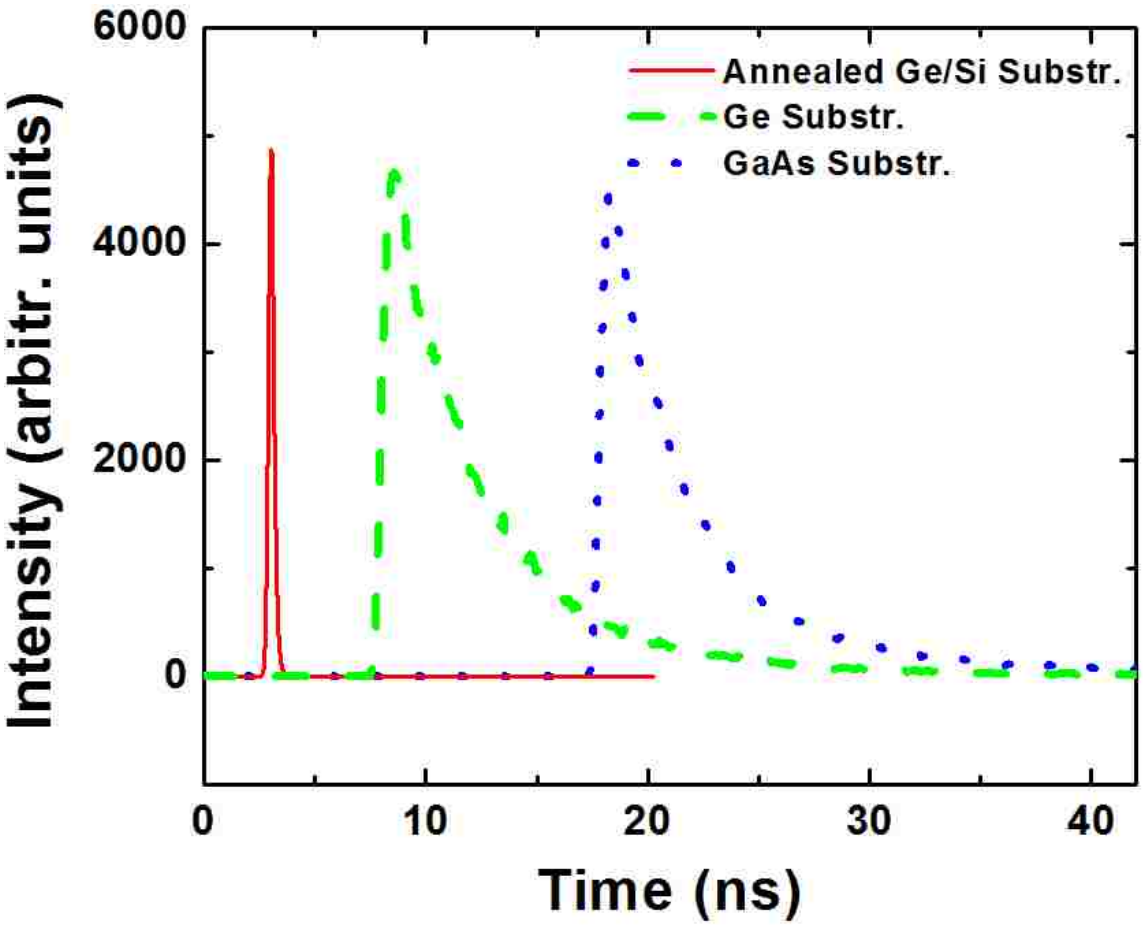


Figure 5-30. Time-resolved photoluminescence spectra of GaAs are collected and used to calculate the minority carrier lifetime. The samples measured correspond to GaAs on annealed Ge-Si (solid line), GaAs on offcut Ge substrate (dotted line), and GaAs on GaAs substrate (dashed line).

The method of nucleating nanometer sized Ge islands within openings in chemical SiO_2 inherently leads to large numbers of twins in the Ge film. However, the method of annealing the Ge islands, while effective in removing SF's from the Ge islands, results in removal of the remaining SiO_2 that exists between the islands. Further Ge growth is believed to result in the nucleation of TDs to relieve the lattice strain due to the Ge growth that occurs on the freshly exposed Si. One possible solution may be to re-oxidize the exposed Si after the high temperature anneal step, thus preventing further Ge

growth from occurring directly on Si. The re-oxidation step is then followed by preferential thermal desorption of GeO_x at 853 K, leaving SiO_2 intact.

5.3.11 Conclusions of III-V Growth on Ge

We find that annealing the Ge islands before complete coalescence over SiO_2 results in removal of the twins. Consequently, the morphology and CL intensity of III-Vs grown on the polished Ge films is greatly improved compared to films containing twins. However, the resulting Ge films now contain a density of TDs that propagate into the GaAs and lower the minority carrier lifetime by two orders of magnitude compared to similar films grown on GaAs or Ge substrates. We suspect that TDs form during later Ge growth because the anneal step that removes twins also desorbs the remaining chemical SiO_2 uncovered by Ge islands. Thus, the SiO_2 template responsible for the enhanced strain relaxation during initial Ge growth is destroyed. We propose that a second oxidation step performed after the high temperature anneal and selective sublimation of GeO_x over SiO_2 may lead to improved minority carrier lifetime in III-V grown on our Ge/SiO_2 template/Si substrates.

CHAPTER 6 STRESS INDUCED DEFECTS IN GERMANIUM GROWTH IN TRENCH PATTERNED SILICON DIOXIDE FILMS ON SILICON AND GERMANIUM SUBSTRATES

6.1 Introduction and Background

The use of trench-patterned SiO_2 films on substrates for heteroepitaxy and subsequent epitaxial lateral overgrowth (ELO) has been shown to substantially reduce the threading dislocation density in highly mismatched systems such as Ge on Si[46,48,49,201-203] and GaN on sapphire[204,205]. The reduction in defect density for Ge on Si is attributed to a combination of dislocation glide and trapping at the SiO_2 sidewalls within the narrow channels.[203,204] Previous studies show, however, that additional defects occur at the merging growth fronts of adjacent channels during ELO. The additional defects that occur from coalescence limit the area of device-quality film that can be produced with ELO. The cause of the coalescence boundary defects has been studied in several systems such as GaN[206,207] and GaAs[208,209] and is ascribed to tilting of the epitaxial layer as it grows laterally over the SiO_2. The tilt results in the formation of a low-angle grain boundary at the merging junctions of the lateral overgrowth regions.[209,210] The low-angle grain boundary is made up of a vertical wall of edge dislocations, some of which possess threading arms that terminate at the film surface.

In this study, we explore the nature and possible causes of coalescence defects in Ge on Si grown within trench-patterned SiO_2 and subsequent ELO. The coalescence defects are examined for thermally grown SiO_2 that is patterned into channels running along both [110] and [100] directions. In addition, we also examine coalescence defects in Ge homoepitaxy in which SiO_2 is deposited by chemical vapor deposition (CVD) on a

Ge on Si film and a Ge substrate and subsequently patterned into channels along the [110] direction. The epitaxially grown Ge is observed x-TEM. Finite element modeling (FEM) is used to estimate the thermal stresses in the Ge film resulting from differences in thermal expansion coefficients with the Si and SiO_2. The EPD measurements are used to characterize the overall defect density of the ELO Ge films.

6.2 Experimental Details

The (001) Si substrates used in this study are boron doped with a resistivity of 1 – 10 Ω-cm. The Si wafers are cleaned for 5 min in a Piranha bath consisting of 3 volumetric parts H_2SO_4 (96 wt %) to 1 part of H_2O_2 (30 wt %) and heated to 100 °C. The samples are subsequently dipped into a buffered oxide etch solution (20 parts 40 wt% NH_4F: 1 part 49 wt% HF) diluted in DI water by 6:1 volumetric ratio to remove the chemical oxide. Figure 6-1 (a-g) schematically depicts the sample fabrication process. Images 6-1 (a-d) show the formation of SiO_2 on the Si substrate, followed by spin coating layers of anti-reflective coating and photoresist, in turn. The SiO_2 films on Si are thermally grown in a dry O_2 oxidation furnace and patterned into 200 nm wide stripes using a combination of interferometric lithography and reactive ion etching, as depicted in Figure 6-1 (e-f). The samples are cleaned in O_2 plasma [Figure 6-1 (g)] and are subsequently re-oxidized to produce a 20 nm thick sacrificial SiO_2 layer at the bottom of the trenches. The sacrificial oxide is used to remove the damaged Si in the bottom of the SiO_2 trenches caused by the plasma etching and is removed in a dilute HF solution before Ge growth.

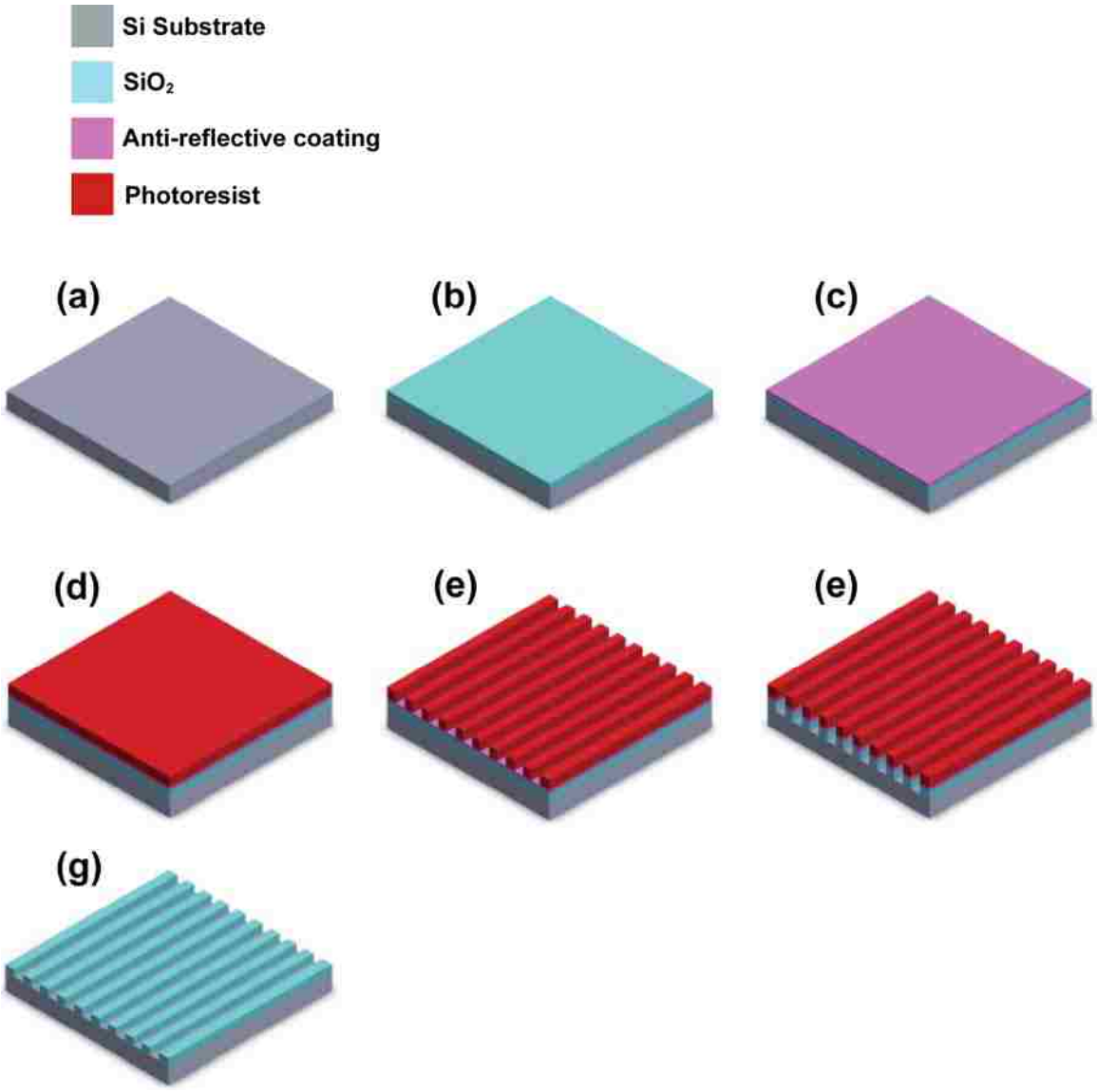


Figure 6-1. Schematic depiction of the fabrication process used to create channels of SiO_2 on the Si substrate. Images 6-1(a-d) shows the formation of SiO_2 on Si, followed by spin coating a layer of anti-reflective coating and photoresist, in turn. Images 6-1(e-f) show the exposure and development of the photoresist into channels followed pattern transfer to the SiO_2 using reactive ion etching. Lastly, image 6-1(g) shows the sample after removal of the photoresist and anti-reflective coating in O_2 plasma.

The (001) Ge substrates are 2-inch wafers with a 6° offcut manufactured by AXT and are Ga doped to a resistivity of 0.016-0.022 Ω-cm. The SiO_2 is deposited at room-temperature onto the Ge substrates using plasma-enhanced chemical vapor deposition (CVD) with SiH_4 and N_2O. The SiO_2 film on Ge is then patterned into trenches

following the same procedure used to pattern the thermally grown SiO_2 on Si substrates shown in Figure 6-1 (c-g). The Ge samples are subsequently cleaned in O_2 plasma and etched for 3 min in a solution of 50 parts DI water to 1 part 30 wt % H_2O_2 to remove approximately 30 nm of Ge from the bottom of the SiO_2 trenches. Epitaxial Ge is selectively grown within the SiO_2 trenches at 973 K and 1.1 monolayers/s.

Samples of Ge on Si are produced after following the same Si substrate pre-cleaning procedure described above. After being loaded into the deposition chamber, the samples are degassed at 873 K for 10 min. The effusion cell temperature is set to produce a flux of 1.9×10^{14} atoms cm^{-2}-s^{-1} (19.1 ML min^{-1}) and allowed to stabilize for 30 min. A total of 100 nm of Ge is deposited, and then the deposition rate is increased to 60 ML min^{-1} until a film thickness of 1.5 μm is reached. The sample is chemically polished following the Ge deposition. The Ge on Si sample then follows the same fabrication steps to produce trench patterned SiO_2 on the Ge film as outlined above for the Ge substrates.

Samples in which Ge is grown until complete coalescence takes place are planarized using CMP. The CMP is performed on a Logitech PM5 using a slurry-free dilute solution of 50 parts DI water to 1 part 30 wt % H_2O_2. The samples are prepared for x-TEM using an FEI Quanta 3D focused ion beam and examined on a JEOL 2010 operating at 200 kV. The etchant solution for EPD measurements consists of 2 parts 49 wt % HF and 1 part 0.1 M $K_2Cr_2O_7$.

6.3 Results and Discussion

Figure 6-2 shows an x-TEM image of Ge grown within the SiO_2 trenches on a Si substrate. The Ge growth is stopped before coalescence of adjacent trenches takes place in order to study the defects in the Ge prior to coalescence. The sample is coated with a SOG to planarize the sample for TEM preparation. Black lines are drawn around the SiO_2 walls to delineate the boundary between Ge, SiO_2, and the SOG in Figure 6-2. The SiO_2 walls have an undercut at their base that is caused by the 30 nm SiO_2 oxidation and dilute HF removal step. Defects in the Ge growth include threading and misfit dislocations that are confined within the trench openings. Defects are not observed in any of the regions over the SiO_2 walls where lateral Ge growth has taken place.

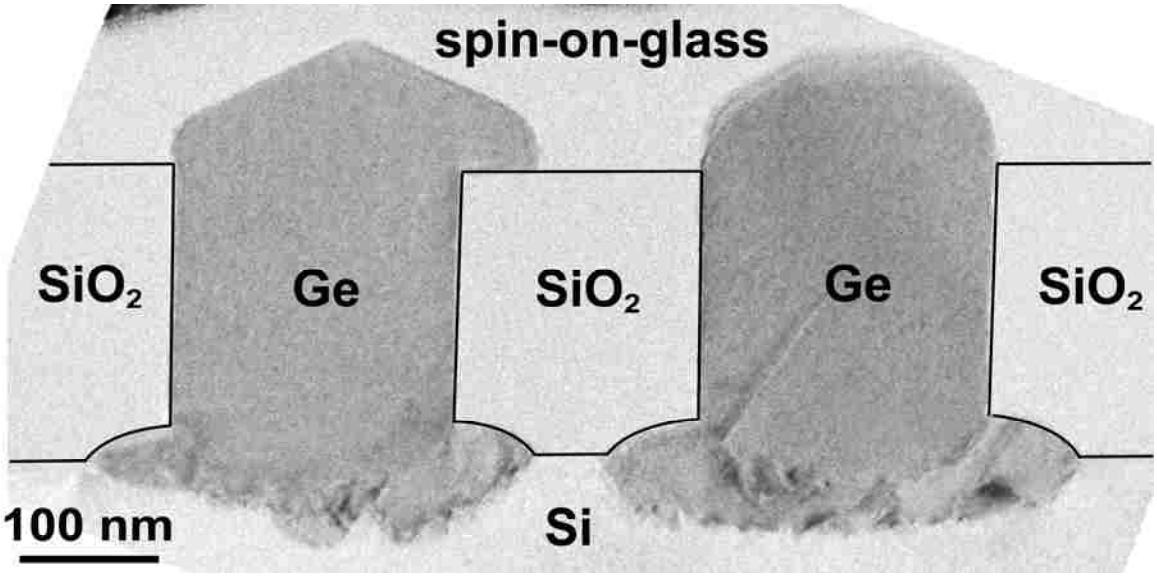


Figure 6-2. Cross-sectional transmission electron microscope image of selective growth of Ge within the SiO_2 channels patterned along the [110] direction. The Ge growth is interrupted before growth from adjacent channels coalescences.

Figure 6-3 shows an x-TEM image of Ge growth in which complete coalescence has occurred and the resulting Ge film is planarized using CMP. Figure 6-3 (a) shows

trenches patterned along the [110] direction, while Figure 6-3 (b) shows trenches running along [100]. Twins are found near the center of the SiO_2 walls in several TEM images of the coalesced samples. Additionally, threading dislocations now commonly occur near the top corners of many of the SiO_2 walls. Voids are commonly observed above the center of the SiO_2 in trenches patterned along the [100] direction, but not in the sample with trenches along [110].

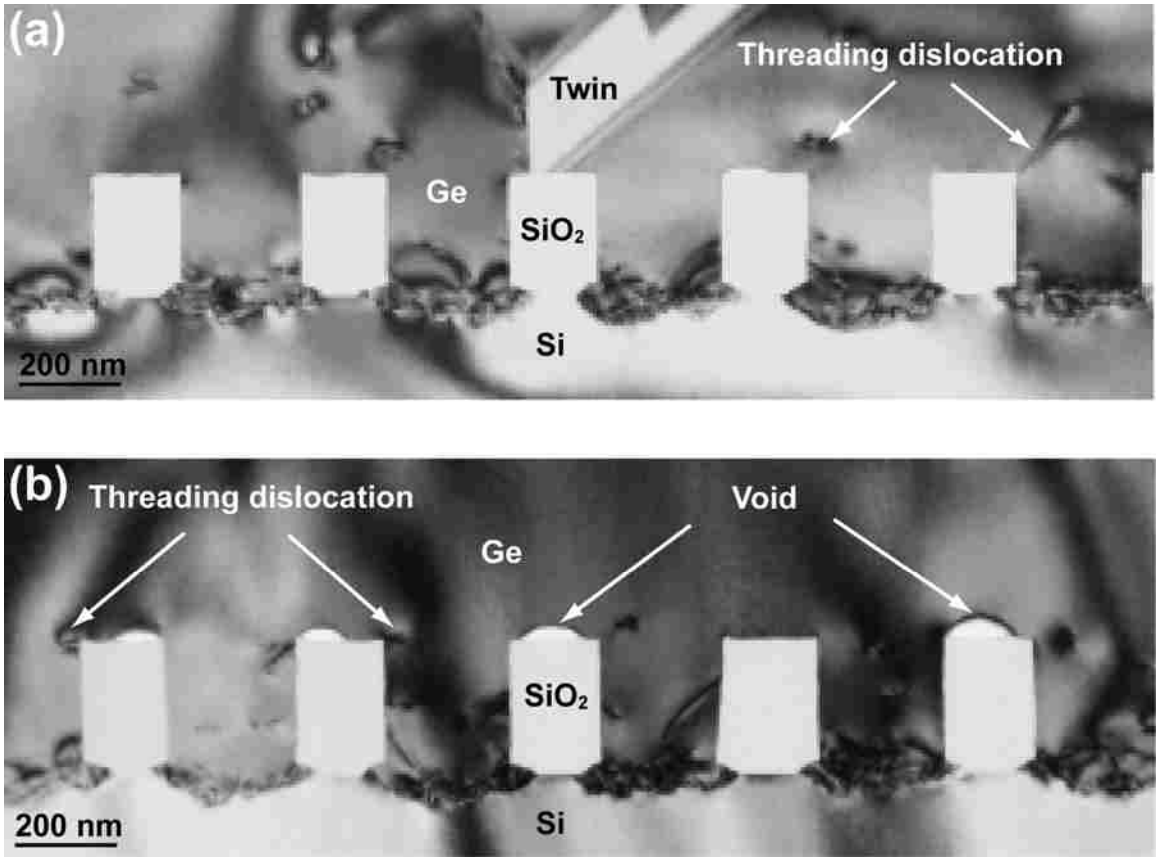


Figure 6-3. Cross-sectional transmission electron microscope images of coalesced Ge grown within SiO_2 channels along 6-3(a) the [110] direction, and 6-3(b) channels along [100] direction. Threading dislocations near the top corners of the SiO_2 walls and voids appearing over the center of the SiO_2 are marked with arrows. A twin defect appearing above the center of the SiO_2 is labeled in 6-3(a).

Previous reports of the tilt misorientation between adjacent trenches in GaN[206,210] and GaAs[209] films that are formed using growth in trench-patterned SiO_2 and subsequent ELO range from 2 to 2.8 degrees for GaN and 0.22 to 0.24 degrees for GaAs. The Ge on Si samples that are fully coalesced are analyzed with x-TEM to determine whether tilting of the Ge epilayer causes the defects appearing over the SiO_2. A series of high-resolution x-TEM images are taken 200 nm apart in a clockwise circuit around a total of 5 of the SiO_2 walls that have twins and dislocations above them. The angular orientation and lattice spacing of the (111) and (220) planes of the Ge are compared to those of the underlying Si. The angular orientation measurement is accurate to ± 0.1 degree. The result of the orientation analysis for Ge on Si shows that no net tilt occurs in the Ge within the error of the measurement. This finding is in agreement with a previous study of Ge on Si grown within SiO_2 trenches where high-resolution x-ray diffraction is used to measure the tilt of the Ge epilayer in the perpendicular direction to the trenches.[211] The authors report a tilt ranging from 0.09 to 0.16 degrees[211], consistent with the finding of less than 0.1 degree of tilt in this study. The presence of such small tilt values, in conjunction with the inconsistent formation of defects at coalescence boundaries indicates that the defects may result from local tilt misorientations rather than macroscopic tilt as observed in GaN[206,207] and GaAs[208,209] ELO films. Local tilt misorientations can result from roughness of the tops of the SiO_2 walls and the uneven nature of the faceting of adjacent Ge growth fronts as seen in Figure 6-2.

The threading dislocations observed at the upper corners of the SiO_2 trenches in coalesced samples also contribute to the defect density of the Ge film above the SiO_2. Defects that emanate from sharp corners of SiO_2 are previously observed in Si

homoepitaxy occurring in ELO films.[212-214] Stress occurring in the ELO film due to mismatch in thermal expansion coefficients of Si, Ge, and SiO_2 can become concentrated at the sharp corners.

Figure 6-4 shows an x-TEM image of a coalesced Ge film grown on the sample of Ge on Si with CVD deposited SiO_2 channels aligned with the [110] direction. The SiO_2 channels effectively block most of the threading dislocations formed from lattice mismatch at the Si/Ge interface. The voids between the Ge and CVD deposited SiO_2 are much larger than in the sample of Ge grown on Si with thermally grown SiO_2, previously shown in Figure 6-3. The voids are large enough that the upper Ge layer does not contact the SiO_2 walls where threading dislocations are observed in the sample with thermally grown oxide. The twins previously observed above the center of the thermally grown SiO_2 walls, however, are present above the center of the SiO_2 walls. The presence of twins, despite the lack of contact between Ge and SiO_2 wall, indicates that twin defect formation is caused by stress occurring from the coalescence of adjacent Ge channels.

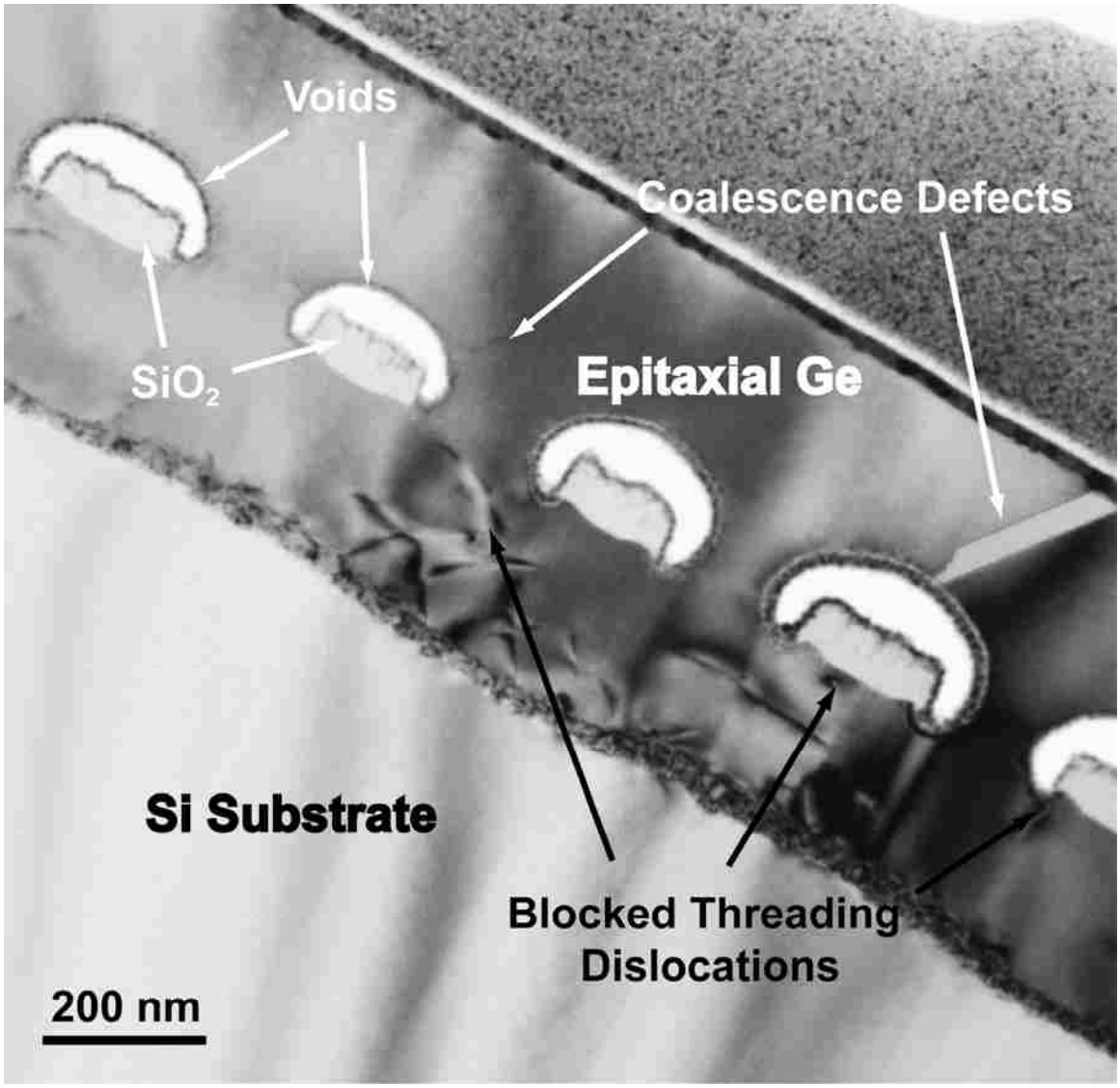


Figure 6-4. Ge growth on Ge on Si film within SiO_2 channels deposited with chemical vapor deposition and patterned into channels aligned along the [110] direction. Large voids are formed between the Ge and SiO_2 such that the upper Ge layer does not contact the SiO_2. The SiO_2 channels effectively block the threading dislocations near the Si/Ge interface from propagating into the upper Ge layer. Twins often appear over the center of the SiO_2 walls.

The coalescence defects are further studied independent of lattice mismatch using Ge substrates with CVD deposited SiO_2 that is patterned into trenches along the [110] direction. A selectively grown and fully coalesced Ge homoepitaxial film is created at a growth temperature of 973 K. The sample is then planarized and analyzed with x-TEM

and shown in Figure 6-5. The CVD deposited SiO_2 is considerably rougher than the thermally grown SiO_2. Twins are observed at the center of several of the SiO_2 walls similarly to that observed in the Ge on Si coalesced films. In contrast, however, threading dislocations are not observed at the top corners of the SiO_2 in the Ge homoepitaxial sample.

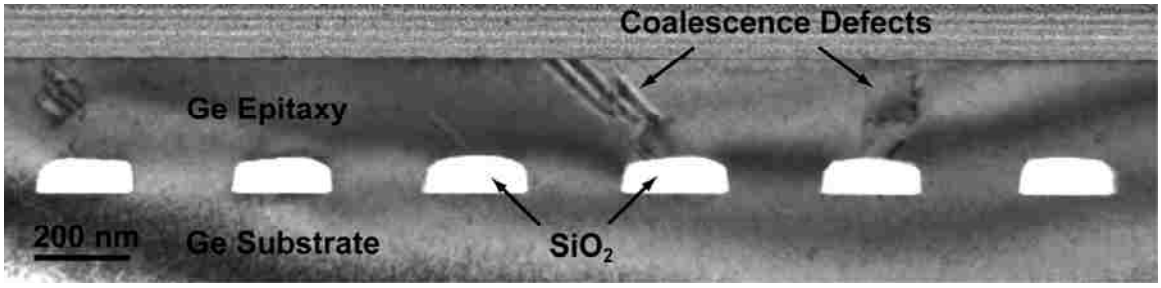


Figure 6-5. Cross-sectional transmission electron micrograph of Ge selectively and epitaxially grown within SiO_2 channels deposited using chemical vapor deposition on a Ge substrate. The SiO_2 channels are patterned along the [110] direction and marked with arrows. Twins and dislocations appear to emanate from the top center of the SiO_2 and are also marked with arrows.

The thermal stress in the coalesced samples of Ge on Si is analyzed using 2-dimensional finite element modeling (FEM), and the result is shown in Figure 6-6. The FEM results in Figure 6-6(a-c) show the thermal stress in the Ge film based on the geometry of the SiO_2 channels and a temperature excursion of 700 K. The temperature excursion corresponds to the cooling of the sample from a growth temperature of 973 K to room-temperature. The analysis in Figure 6-4 (a) shows that the maximum stress of 2.7×10^8 Pa occurs in the Ge film near the top corners of the SiO_2 walls for Ge on Si growth. The top corners of the SiO_2 walls are where the threading dislocations are observed to occur in the fully coalesced samples. Figure 6-6 (b) shows the thermal stress

in the structure of Ge coalesced over CVD deposited SiO_2 on the Ge on Si film. The maximum stress of 2.1×10^8 Pa is similar in magnitude to the Ge on Si sample. However, the Ge does not contact the corners of the SiO2 and threading dislocations are not observed in these regions in x-TEM images of this sample. Figure 6-6(c) shows that the maximum stress for the Ge growth within CVD deposited SiO_2 trenches on the Ge substrate is 1.1×10^8 Pa near the top corners of the SiO_2 walls. This value for growth on the Ge substrate is approximately half compared to Ge growth on the Si substrates and threading dislocations are not observed to emanate from the corners of the SiO_2 in the sample. The correlation between the thermal stress analysis of the FEM and the x-TEM indicate that thermal mismatch stress between the Si substrate, SiO_2 walls, and Ge film can contribute to the formation of the threading dislocations that originate at the top corners of the SiO_2 walls during cooling of the sample from growth to room-temperature.

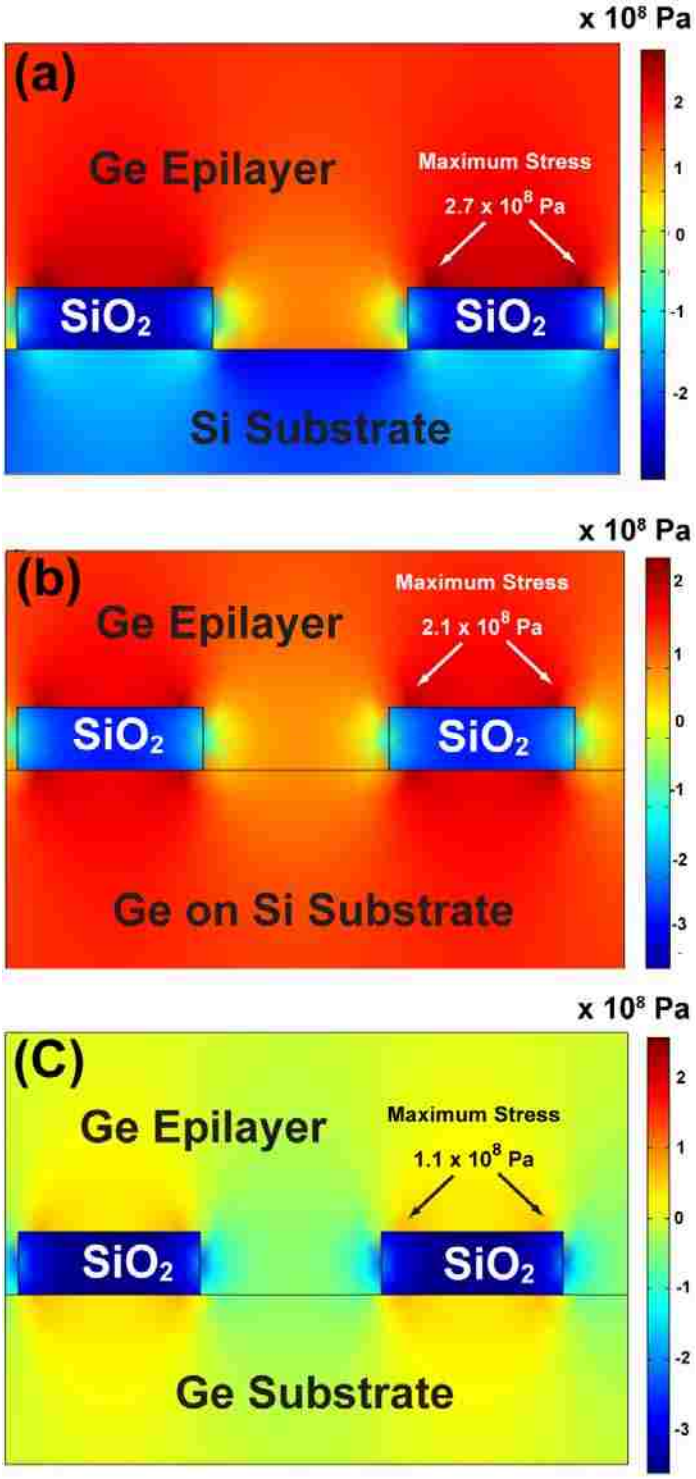


Figure 6-6. Finite element model of the thermal stress occurring from thermal expansion coefficient mismatch. Image 6-4 (a) for coalesced Ge/SiO_2/Si substrate, 6-4 (b) for coalesced Ge/SiO_2/Ge/Si substrate, and 6-4 (c) for coalesced Ge/SiO_2/Ge substrate.

The presence of twins above the center of the SiO_2 walls may be caused by either local roughness of the SiO_2 wall or translation mismatch between adjacent Ge channels. The SiO_2 roughness may induce a small local tilt misorientation in the Ge during lateral growth over the SiO_2 and cause formation of a twin defect during coalescence. Translation mismatch is shown in Figure 5-5(c) and occurs when the width of an SiO_2 wall is not an integral number of lattice spacings of Ge. A large stress can occur during coalescence over the center of the SiO_2 leading to twin defect or TD formation. The translation mismatch mechanism for twin formation appears more likely than SiO_2 roughness based on the observations shown in Figure 6-4. The Ge does not contact the SiO_2 in the sample shown in Figure 6-4 due to the large voids that appear in the Ge over the SiO_2. Therefore, the presence of twin defects over the SiO_2 in this sample is most likely due to translation mismatch rather than SiO_2 roughness. In addition, the CVD deposited SiO_2 is much rougher than the thermally grown SiO_2 as shown in Figures 6-3 and 6-4, yet the density of twins is approximately the same in samples with both types of SiO_2, as discussed next.

Lastly, etch pit densities of the coalesced samples of Ge on Si with thermally grown SiO_2 on Si and CVD deposited SiO_2 on a Ge substrate are analyzed and shown in the SEM images in Figure 6-7 (a-c). The Ge grown on Si within SiO_2 is shown in Figure 6-7 (a) for trenches along [110], (b) trenches along [100], and (c) Ge homoepitaxy within [110] SiO_2 trenches. The rectilinear and L-shaped pits aligned with <110> directions are due to twins that propagate to the film surface, whereas square or circular shaped pits are due to threading dislocations. The threading dislocation and twin defect density is 7.2×10^7 cm^{-2}, and 1.5×10^7 cm^{-2} respectively, for the sample shown in Figure 6-3 (a) with

SiO_2 trenches along [110]. The threading dislocation density is similar for the Ge on Si with [100] SiO_2 trenches, but the twin density is nearly double at 2.5×10^7 cm^{-2}. Moreover, there is a preferential alignment of the twins in the sample with channels aligned along [110]. The twins in the sample with SiO_2 trenches along [110] have a ratio of 5 to 1 for twins aligned along [110] versus the perpendicular [1-10] direction. In contrast, the sample with SiO_2 trenches along [100] contains an almost equal number of twins aligned along [110] (9.8×10^6 cm^{-2}) and [1-10] (1.5×10^7 cm^{-2}) directions.

The preferential alignment of twins in the case of channels along [110], but not [100] can be explained with reference to the {111} <110> slip system of Ge. Twins exist only on {111} planes and intersect the (100) surface along <110> directions.
Our FEM results show that large stresses exist at the edges of the Ge growth fronts during ELO over the SiO_2 walls. The overlap of the stress fields of the merging Ge growth fronts results in large stresses occurring during coalescence. Twins aligned along the [110] channel direction can relieve the greatest amount of coalescence stress in the Ge. Twins aligned with <110> directions are less efficient at relieving stress for channels along [100], which explains why there is approximately twice the number of twins formed when channels are along [100] versus [110]. In addition, twins aligned with either [110] or [1-10] relieve equal amounts of stress for channels along [100], which explains the presence of equal numbers of twins aligned along both directions in this sample.

Figure 6-7 (c) shows the sample of homoepitaxial Ge coalesced over CVD deposited SiO_2 channels along [110] on a Ge substrate. The density of twins in the sample is 1.7×10^7 cm^{-2} and is similar to the sample of Ge on Si in SiO_2 channels along

[110], despite the roughness of the CVD deposited SiO_2. The twins also show the same preferential alignment along the [110] channel direction. The inset of Figure 6-7 (c) shows that the twins exist over the center of the SiO_2 channels. The analogous results obtained for the Ge on Si and homoepitaxial Ge samples with [110] patterned channels shows that coalescence induced stress over the SiO_2 walls is the likely cause of twin defect formation in ELO growth of Ge, rather than local tilt misorientation of the Ge.

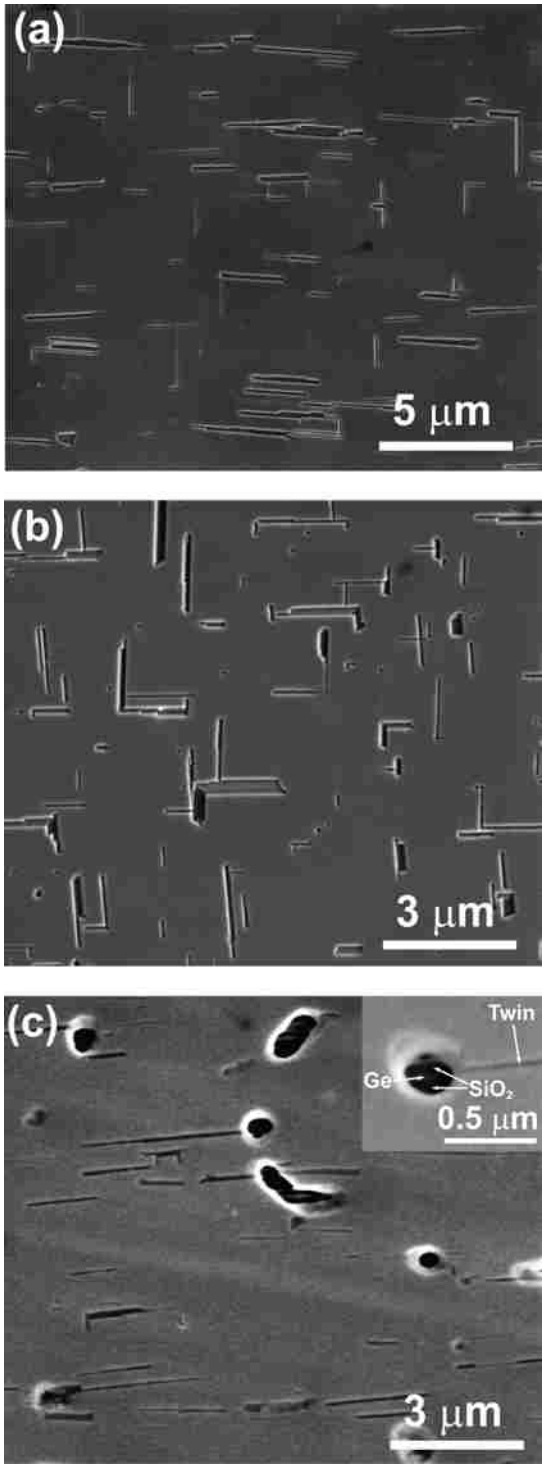


Figure 6-7. Scanning electron microscope images showing the etch pit density of the coalesced Ge in trench patterned SiO_2 channels. Image 6-7(a) shows the sample of Ge on Si with SiO_2 channels along the [110] direction. Image 6-7(b) shows the sample of Ge on Si with SiO_2 channels along the [100] direction. Image 6-7(c) shows the sample of Ge on Ge with chemical vapor deposition of SiO_2 channels along [110] direction.

6-4 Conclusions of Ge Growth in Trench Patterned SiO_2 Channels

The defects occurring in Ge films on SiO_2 patterned films on Si and Ge substrates are observed with x-TEM and EPD measurements. Threading dislocations occurring due to the lattice mismatch between Ge and Si are successfully trapped near the bottom of the SiO_2 walls. Additional defects occur after coalescence of adjacent Ge emerging from the channels in SiO_2. Threading dislocations and twins are commonly observed near the top corners and center of the SiO_2 walls, respectively. Finite element modeling is used to show that the threading dislocations occurring at the top corners of the SiO_2 walls is likely caused by thermal stress in the Ge film occurring from mismatch in thermal expansion coefficients of Ge, Si, and SiO_2. The twin defects occurring over the top center of the SiO_2 walls are likely caused by the translation mismatch between adjacent Ge channels that leads to large stresses in Ge upon coalescence over the SiO_2 walls.

CHAPTER 7. DISLOCATION BLOCKING IN GERMANIUM ON SILICON HETEROEPITAXY USING SILICON DIOXIDE LINED ETCH PITS AND EPITAXIAL LATERAL OVERGROWTH

7.1 Introduction and Background

Previous methods described to reduce the defect density in GoS using SiO_2 structures all have the disadvantage of forming additional defects during coalescence over the SiO_2. The method described in this chapter to improve the GoS film quality is the passivation of etch pits in the Ge film using SiO_2, and subsequent ELO. The GoS samples are characterized using SEM, x-TEM, and EPD measurements.

7.2 Experimental Details

The (001) Si substrate consists of a 2-inch wafer doped with boron with a resistivity of 1 – 10 Ω-cm. The Si wafers are cleaned for 5 min in a Piranha bath consisting of 3 volumetric parts H_2SO_4 (96 wt %) to 1 part of H_2O_2 (30 wt %) and heated to 100 °C. The samples are subsequently dipped into a buffered oxide etch solution (20 parts 40 wt% NH_4F: 1 part 49 wt% HF) diluted in DI water by 6:1 volumetric ratio to remove the chemical oxide. The chemical oxidation is then repeated, and the wafer is rinsed in DI water and blown dry with N_2. After being loaded into the deposition chamber, the samples are degassed at 873 K for 10 min. The effusion cell temperature is set to produce a flux of 1.9×10^{14} atoms cm^{-2}-s (19.1 ML min^{-1}) and allowed to stabilize for 30 min. A total of 100 nm of Ge is deposited, and then the deposition rate is

increased to 60 ML/min until a film thickness of 1.5 μm is reached. The sample is planarized following the Ge deposition.

The GoS wafers are polished using a Logitech PM5 lapping/polishing machine on a Logitech Chemcloth polishing pad. The polishing solution consists of 50 parts DI water and 1 part 30 wt% H_2O_2. Figure 7-1 schematically depicts the processing steps following GoS polishing. Figure 7-1 (a) shows the polished GoS sample with threading dislocations that intersect the Ge surface. Etch pits are created in the Ge using a solution of 2 parts 49 wt % HF and 1 part 0.1 M $K_2Cr_2O_7$, as shown in Figure 7-1 (b). The GoS sample with etch pits is then coated with 15 nm of SiO_2 deposited in a plasma-enhanced CVD chamber using SiH_4 and N_2O, corresponding to Figure 7-1(c). Figure 7-1 (d) depicts a 50 nm thick film of polymethyl methacrylate (PMMA) spin-coated onto the sample following the SiO_2 deposition. The PMMA flows into the etch pits and planarizes the GoS surface. Figure 7-1 (e) depicts how the PMMA and SiO_2 is etched away to the top of the etch pits using reactive ion etching with CHF_3 and O_2. The residual PMMA is removed from within the etch pits using an O_2 plasma, and depicted in Figure 7-1 (f). Lastly, Figure 7-1 (g) shows an additional 2 μm of Ge that is selectively deposited on the processed sample using MBE, followed by polishing. The SiO_2 blocks the threading dislocations from propagating into the top layer of Ge.

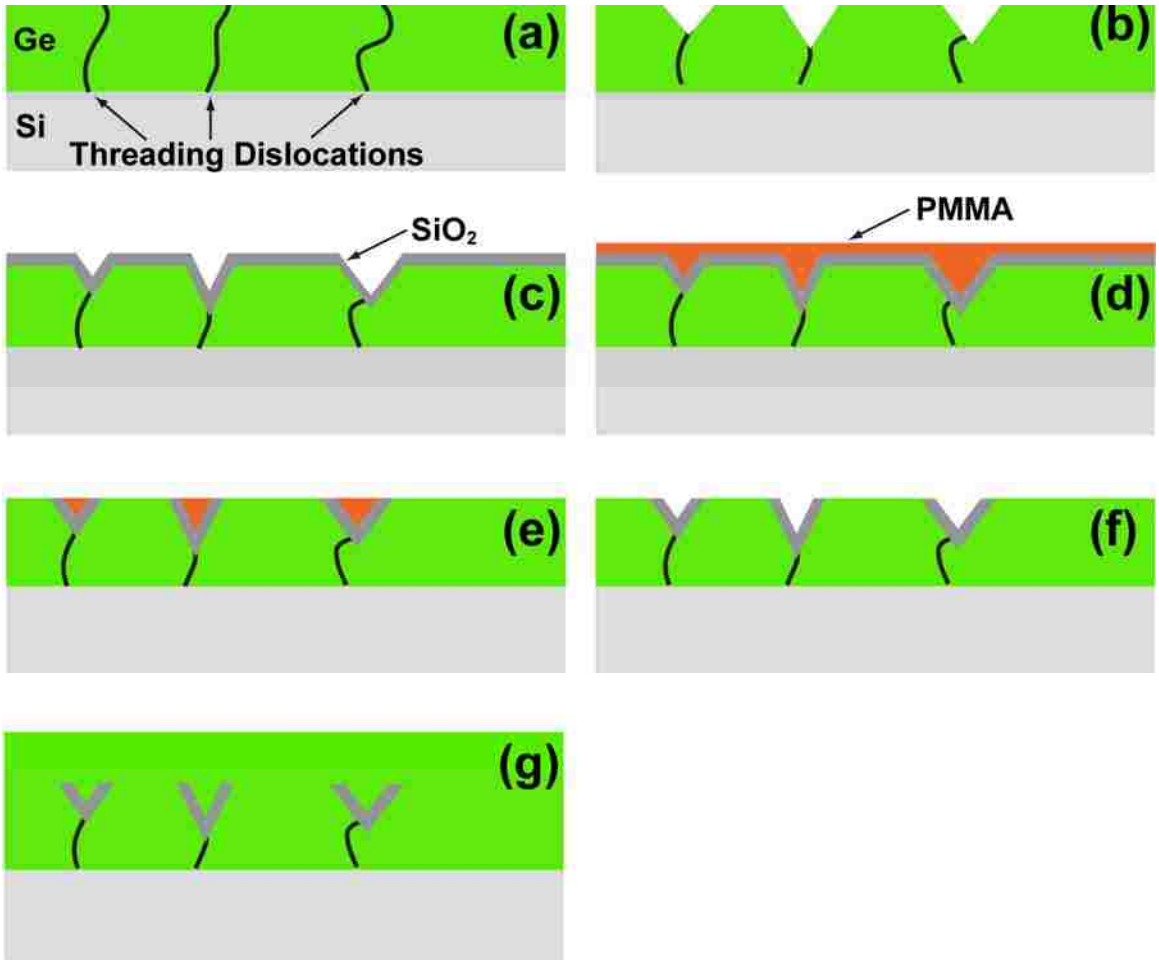


Figure 7-1. Schematic depiction of the sample fabrication process. Image 7-1(a) shows the threading dislocations terminating at the surface of the initial Ge on Si film. Image 7-1(b) shows the formation of etch pits in the surface of the Ge where the dislocations terminate. Image 7-1(c) shows the deposition of a thin layer of SiO_2. Image 7-1(d) shows a thin layer of polymethyl-methacrylate that is spin-coated onto the sample surface. Image 7-1(e) shows the sample after reactive ion etching removes the SiO_2 and polymethyl-methacrylate from the planar Ge surface. Image 7-1(f) shows removal of the residual polymethyl-methacrylate from within the etch pits. Lastly, image 7-1(g) shows the growth of a selective epitaxial lateral overgrowth layer of Ge in which the SiO_2 lined etch pits block the threading dislocations in the initial Ge film from propagating into the top Ge layer.

7.2 Results and Discussion

Figure 7-2 is an SEM image of the etch pits created in the first Ge layer grown directly on Si. The thickness of the Ge layer after formation of etch pits is approximately

500 nm and the EPD is 2.8×10^8 cm^{-2}. The etch pits range in diameter from 300 nm to 1 μm and range in depth from 30 to 100 nm. The EPD measurements are previously shown to accurately represent the dislocation density in the Ge film bases on plan-view TEM.[56]

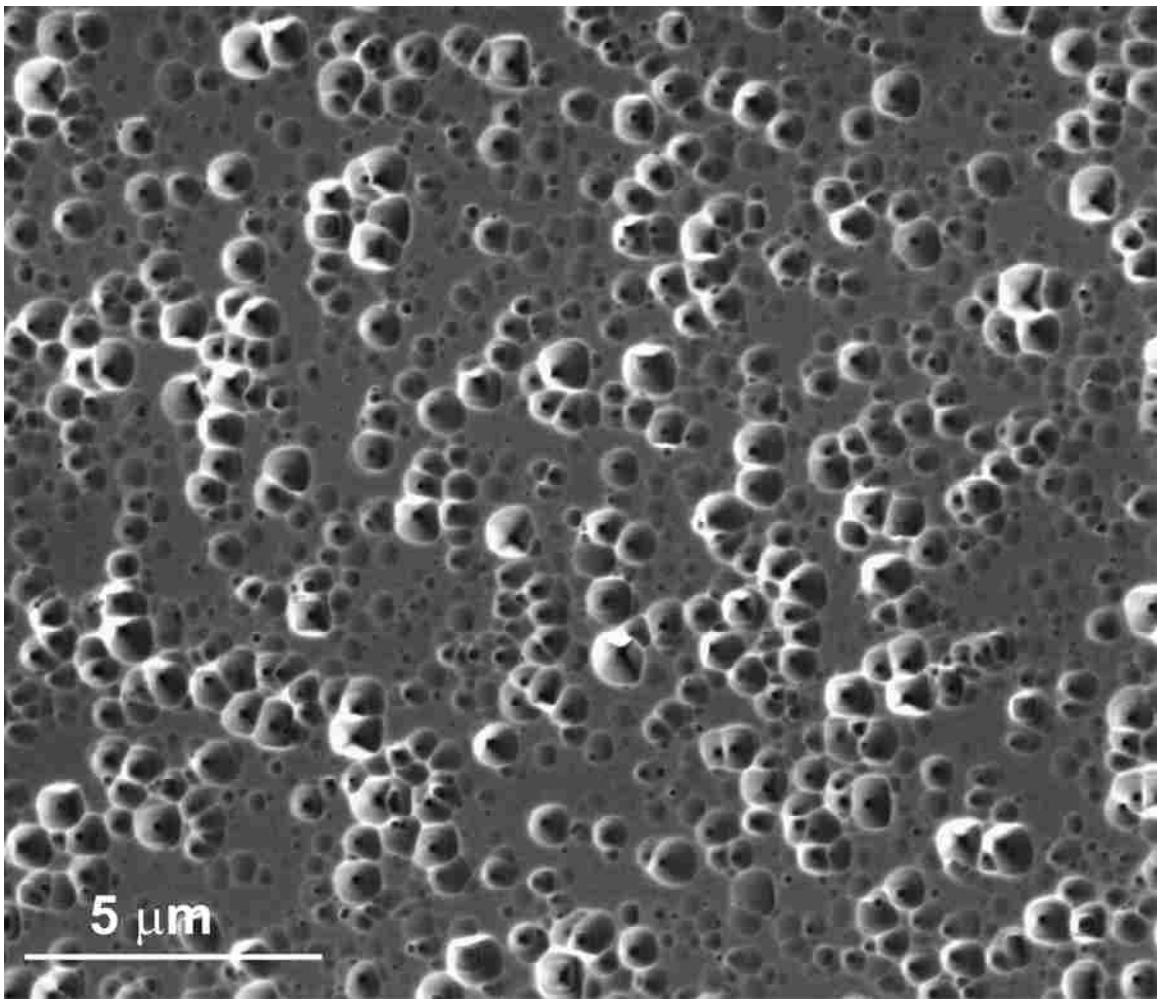


Figure 7-2. Scanning electron microscope image after etch pit formation in the initial Ge on Si film.

Figure 7-3 shows an SEM image of the sample corresponding to Figure 7-1 (f) in which the etch pits are passivated with the SiO_2. The SiO_2 lined pits show up darker than the

surrounding planar regions of the Ge surface. The deeper etch pits are lined with SiO_2 near the top of the pit, whereas shallower pits have SiO_2 only near the bottom of the pit.

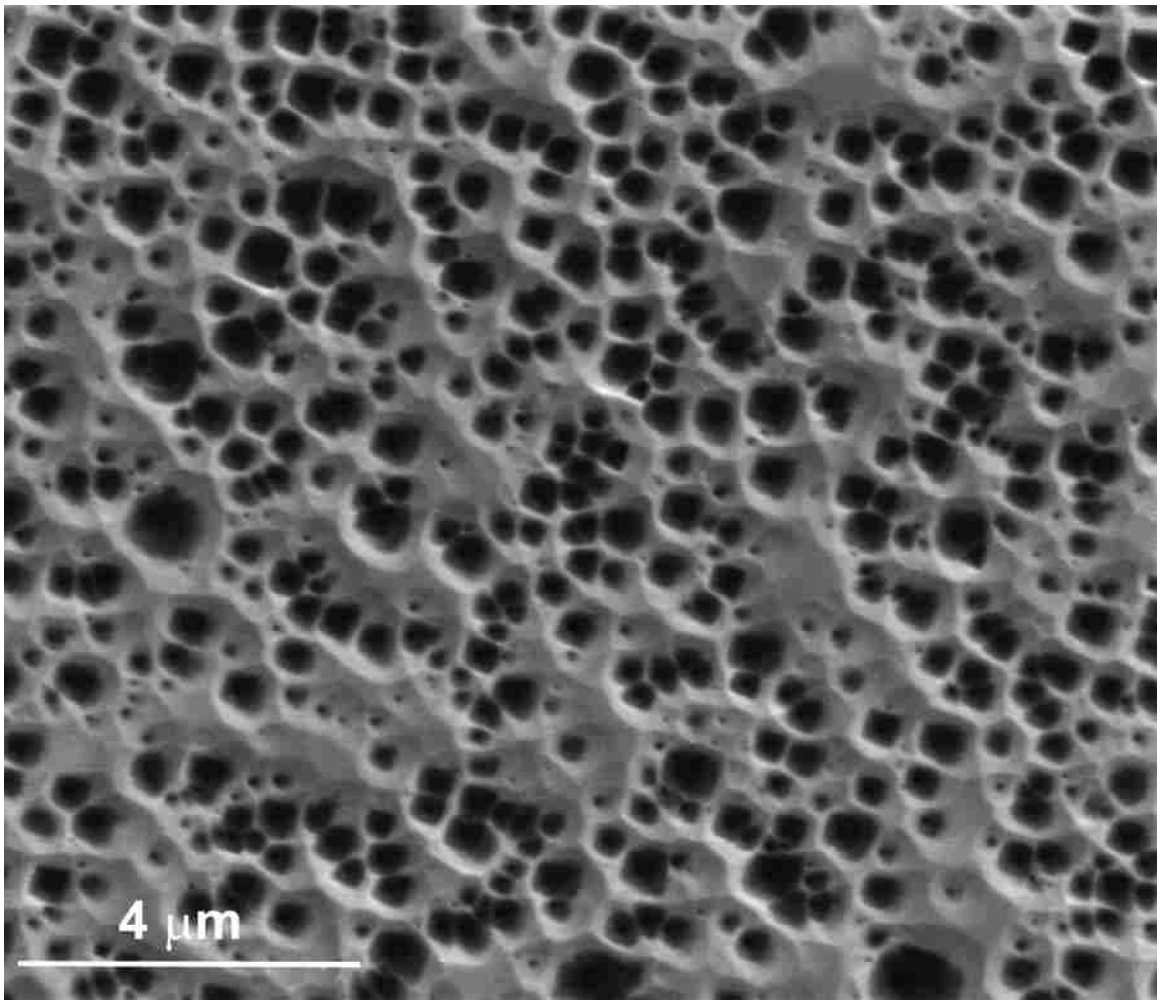


Figure 7-3. Scanning electron microscope image showing the SiO_2 lining within the Ge etch pits.

Figure 7-4 shows an x-TEM of the Ge ELO film over the SiO_2 lined etch pits. The deposition is carried out at a substrate temperature of 673 K such that Ge growth is not selective and random Ge nucleation takes place on the SiO_2. Figure 7-4 shows that the Ge nucleated on the SiO_2 lined etch pits is polycrystalline and contributes additional

defects to the upper Ge layer formed during ELO. The EPD of the resulting GoS is greater than 5×10^8 cm^{-2}. The inset in Figure 7-4 shows the threading dislocation in the lower Ge layer blocked by an SiO_2 lined etch pit. In contrast, the Ge ELO performed at higher substrate temperatures leads to much better Ge film quality.

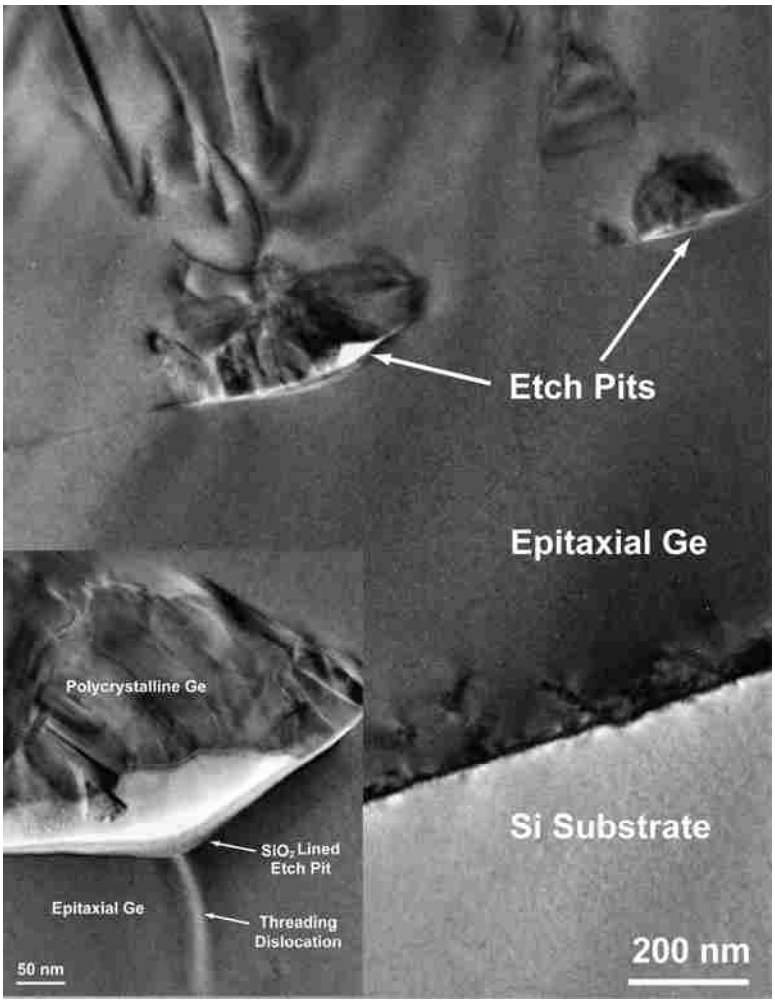


Figure 7-4. Cross-sectional transmission electron microscope image of the resulting structure after Ge epitaxial lateral overgrowth coalesces over the SiO_2 lined etch pits. The low substrate temperature results in non-selective Ge growth and polycrystalline Ge forms on the SiO_2 within the etch pits. The polycrystalline Ge leads to additional defects created in the upper Ge layer. The inset shows a close-up view of an SiO_2 lined etch pit that blocks the lower dislocation.

Figure 7-5 shows an x-TEM image where ELO growth is carried out at 973K and results in selective growth of Ge over SiO_2. The TEM image shows the epitaxial growth that takes place during ELO over the SiO_2 lined etch pits that block dislocations from below. The inset in Figure 7-5 reveals a void between the Ge and the SiO_2 lined etch pit that is formed upon Ge coalescence over the pit.

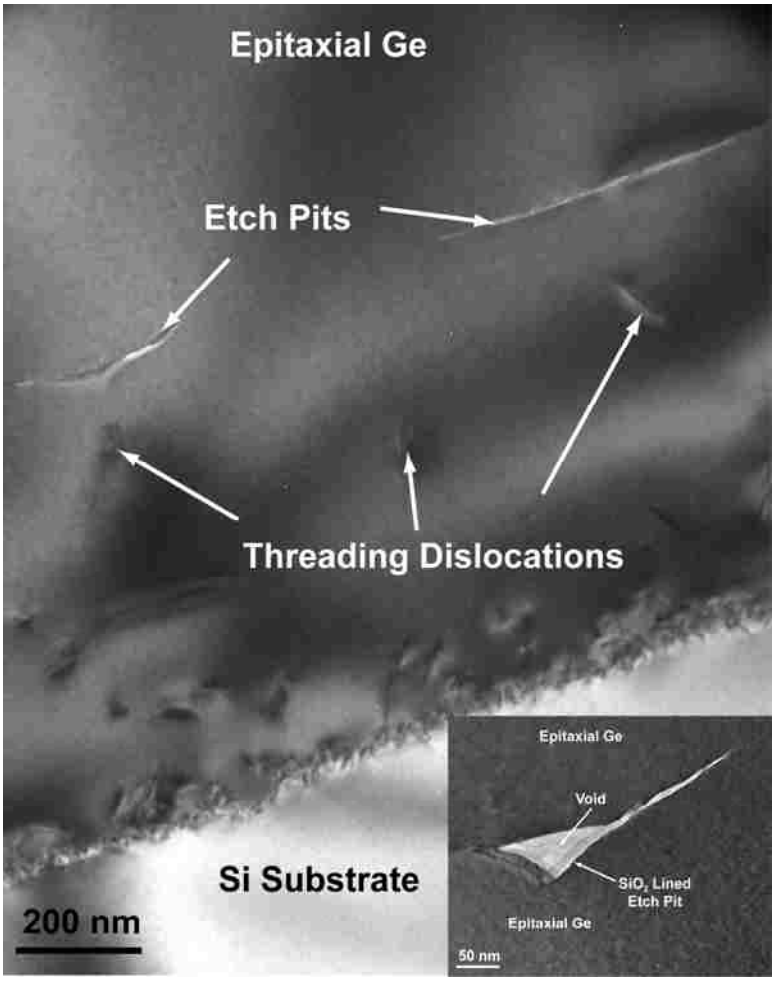


Figure 7-5. Cross-sectional transmission electron microscope image at a higher growth in which the Ge is grown selectively and laterally over the SiO_2 lined etch pits. The threading dislocations are blocked below the etch pits and the Ge overgrowth is epitaxial and high quality. The inset shows that a void is formed between the Ge and the SiO_2 over the etch pit.

Figure 7-6 shows the EPD of the resulting ELO Ge film. Twin/SF defects (rectilinear pits) and threading dislocations (square pits) are present after EPD. The density is 5.5×10^6 cm^{-2} for twin/SF defects and 3.1×10^6 cm^{-2} for threading dislocations, leading to a total defect density of 8.6×10^6 cm^{-2} in the Ge ELO film. The reduction factor in defect density is 31 for the Ge ELO layer compared to the initial GoS growth. The twin/SF defects in the Ge ELO layer likely result during coalescence of the Ge ELO layer over the SiO_2 lined etch pits. Previous studies of Ge ELO films formed over stripe-patterned SiO_2 films show the formation of twins at the merging junction of adjacent Ge growth fronts. The residual threading dislocations in the Ge ELO layer may come from etch pits that are initially very shallow and all the PMMA and SiO_2 are removed during reactive ion etching. We expect further reduction in defect density in the Ge ELO layer by further optimizing the initial GoS growth to result in fewer initial threading dislocations.

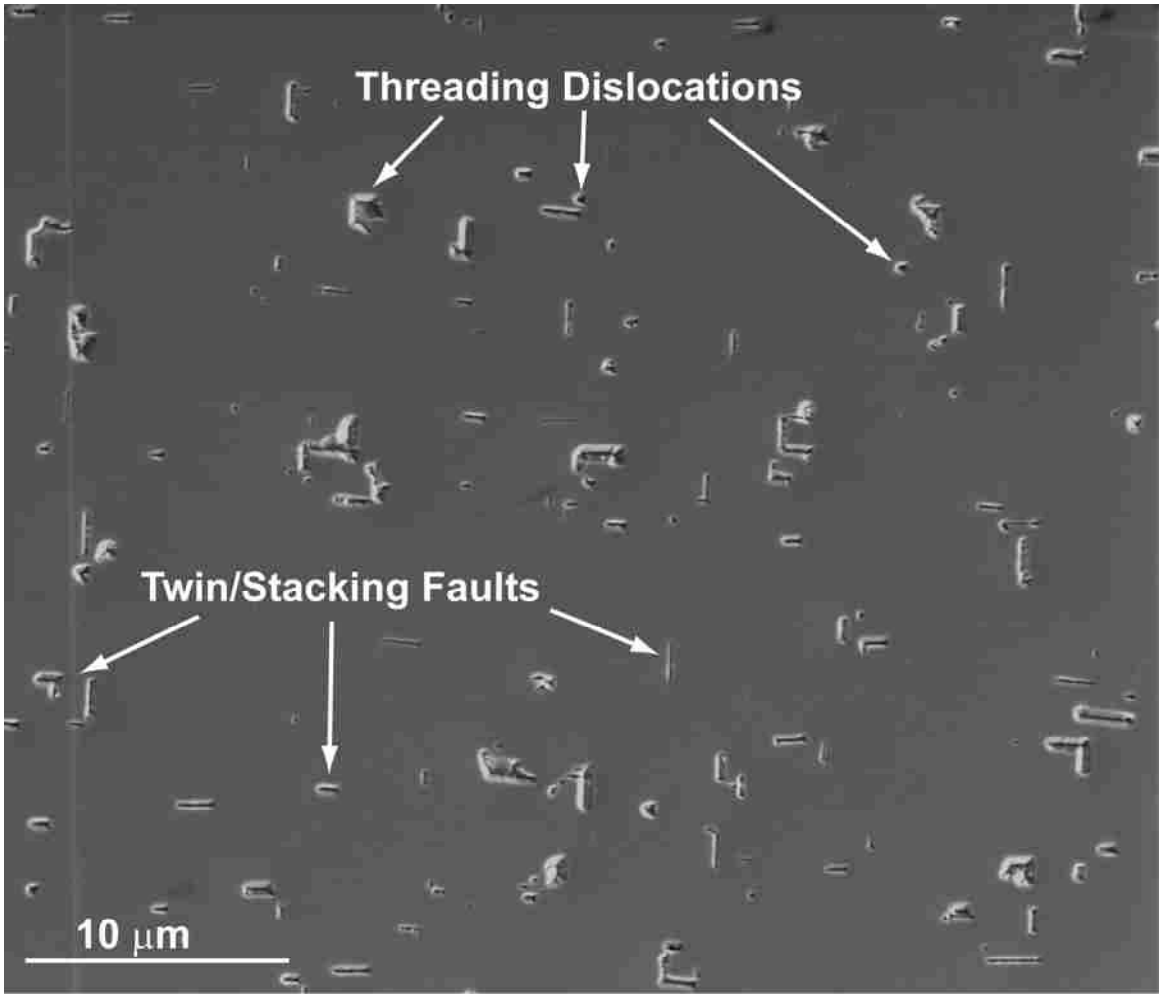


Figure 7-6. Scanning electron microscope image showing the etch pit density in the resulting Ge film selectively grown over the SiO_2 lined etch pits. The elongated pits correspond to twins or stacking faults, while square shaped pits correspond to threading dislocations.

Lastly, we performed annealing at 1073 K for 30 min on the GoS sample with SiO_2 lined etch pits. The sample is cooled to 973 K for the Ge ELO growth, polished, and then examined with EPD. We find that the sample that was annealed at high temperature prior to the Ge ELO growth has a defect density of 1.2×10^8 cm^{-2}. The reduction factor from the initial defect density is only 2.3. We believe that the high temperature anneal step leads to significant dislocation climb. The dislocations initially

blocked by the SiO_2 lined pits can climb around the obstacle and continue to propagate into the Ge ELO layer.

7.3 Conclusions for Dislocation Blocking with SiO_2 Lined Etch Pits

A significant reduction in the threading dislocation density is obtained in GoS using etch pits passivated with SiO_2 along with subsequent ELO. Twin/SF defects and TDs are found in the ELO Ge film. Twins have been observed in ELO of Ge over SiO_2 and are believed to occur upon coalesce of Ge over the SiO_2. The dislocations likely result from the shallowest etch pits in which the PMMA and SiO_2 is completely removed from the pit during reactive ion etching. Selective growth during ELO is necessary to obtain an improvement in the Ge ELO film quality. In addition, high processing temperatures after formation of the passivated etch pits in GoS leads to a high density of threading dislocations in the Ge ELO film. We speculate that the high processing temperatures allow dislocations to climb around the SiO_2 obstacles and propagate into the subsequent Ge layer.

CONCLUSIONS AND FUTURE WORK

Three different approaches are presented to eliminate, reduce, or manage defects in GoS heteroepitaxy. The first approach involves the formation of a high density of nanoscale openings in a thin layer of chemical SiO_2. Germanium selectively nucleates within the openings to form islands that grow and eventually coalesce into a continuous film. The nanoscale areas of contact between islands and substrate allows stress relaxation to occur in the Ge without the need for dislocations to form. A fraction of the Ge islands nucleate in twin relationships and slight misorientations compared to the surrounding Si and epitaxial Ge islands. The twin-oriented Ge islands cause the formation of twins upon coalescence with epitaxial Ge islands. The twins act as non-radiative recombination centers and cause significant roughness in GaAs films grown on the GoS. Annealing the Ge islands followed by additional Ge growth leads to Ge films free of twins, however, annealing the Ge islands also leads to desorption of the SiO_2 layer. Surface diffusion then transfers Ge from the epitaxial and twin-oriented Ge islands to the freshly exposed Si substrate. Dissolution of the epitaxial and twin-oriented Ge islands takes place followed by formation of a GeSi alloy layer. The dissolution of the twin-oriented Ge islands is the mechanism by which Ge films formed after additional growth are free of twins. The Ge films contain TDs, however, due to the loss of SiO_2 and the increased contact between Ge and Si. Despite the formation of TDs, the roughness of the GaAs on the annealed GoS is greatly reduced and the PL intensity matches GaAs growth on Ge and GaAs substrates. The minority carrier lifetime of GaAs on the annealed GoS, however, is nearly two orders of magnitude less than growth on a GaAs

and Ge substrate and is attributed to the TDs in the Ge film that propagate into the GaAs layer.

The second approach to reducing defects in GoS is trapping of dislocations in Ge between high aspect ratio walls of SiO_2. The method requires selective growth of Ge on Si over SiO_2. Nucleation experiments are carried out to determine the optimal deposition rate and substrate temperature to achieve selective growth using MBE. The nucleation of Ge on SiO_2 experiments lead to measurement of the important energetics of Ge nucleation on SiO_2. Measurement is made of the critical Ge island size, binding energy, and surface diffusion energy of Ge on SiO_2. The small desorption energy of Ge on SiO_2 allows selective growth to occur at high substrate temperatures and low deposition rates.

Dislocations formed from the lattice mismatch between Ge and Si are effectively trapped within the SiO_2 channels, however, additional defects form upon coalescence of adjacent Ge channels. Threading dislocations emanate from the top corners of the SiO_2 walls and twins are found over the top center of the SiO_2. Finite element analysis is done to estimate the stress in the Ge film occurring form differences in the thermal expansion coefficients between Ge, Si, and SiO_2. The FEM analysis reveals that the maximum thermal stress in the Ge film occurs at the upper corners of the SiO_2 walls where TDs are observed.

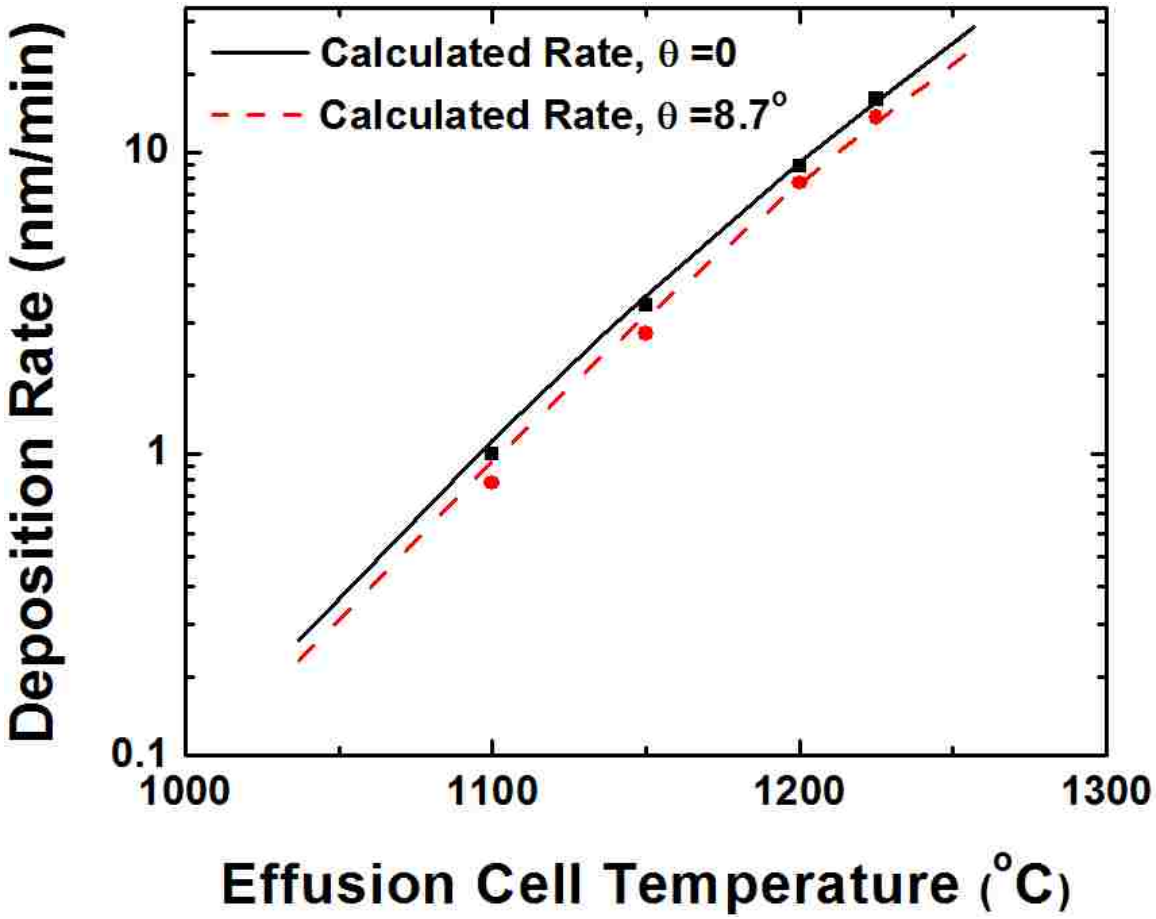
Twins are also observed to occur over the top center of the SiO_2 walls. The twin formation is best explained based on translation mismatch of adjacent Ge channels. The translation mismatch occurs because the SiO_2 walls are not an integral number of Ge lattice spacings. The translation mismatch will lead to large stresses in the Ge upon coalescence.

The third method to reduce defects in GoS is the creation of etch pits in a layer of GoS. The etch pits are lined with CVD deposited SiO_2. A second layer of Ge is then selectively grown over the SiO_2 lined etch pits. The SiO_2 blocks TDs in the lower Ge layer from propagating into the upper Ge layer. The method of blocking dislocations using SiO_2 lined etch pits is found to be the most effective method at reducing defects in GoS. Further optimization of the process could result in the commercialization of electronic devices made using GoS.

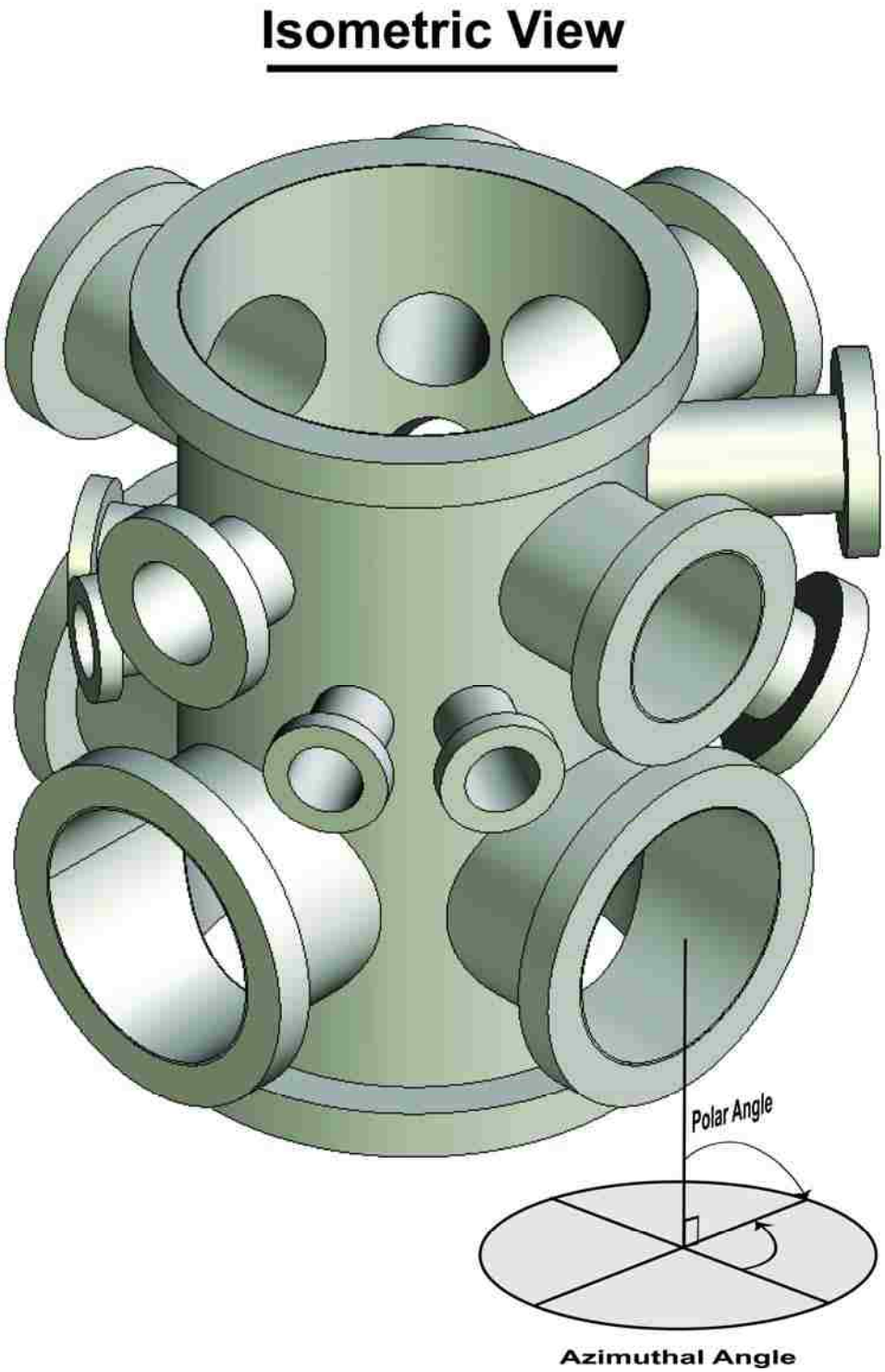
Future work should include optimization of the method of dislocation blocking using SiO_2 lined etch pits. For example, minimizing the TDD in the lower Ge layer by employing an anneal step will result in fewer etch pits in the layer. The result will be fewer defects in the subsequently grown upper Ge layer. In addition, more research on methods to alleviate stress in the Ge due to the large mismatch in thermal expansion coefficient with Si is needed. Specifically, the use of patterned SiO_2 and other methods should be systematically evaluated to determine if an increase in the GoS thickness could be achieved without the formation of cracks in the Ge. Lastly, electronic devices such as MOSFETs should be fabricated and electrically characterized on the improved GoS using etch pit dislocation blocking and compared to a control sample of GoS. The improvement of the Ge may now be sufficient for efficient operation of majority carrier devices, though not yet good enough for minority carrier device operation.

APPENDICES

APPENDIX A MBE Calculated and Measured Deposition Rates



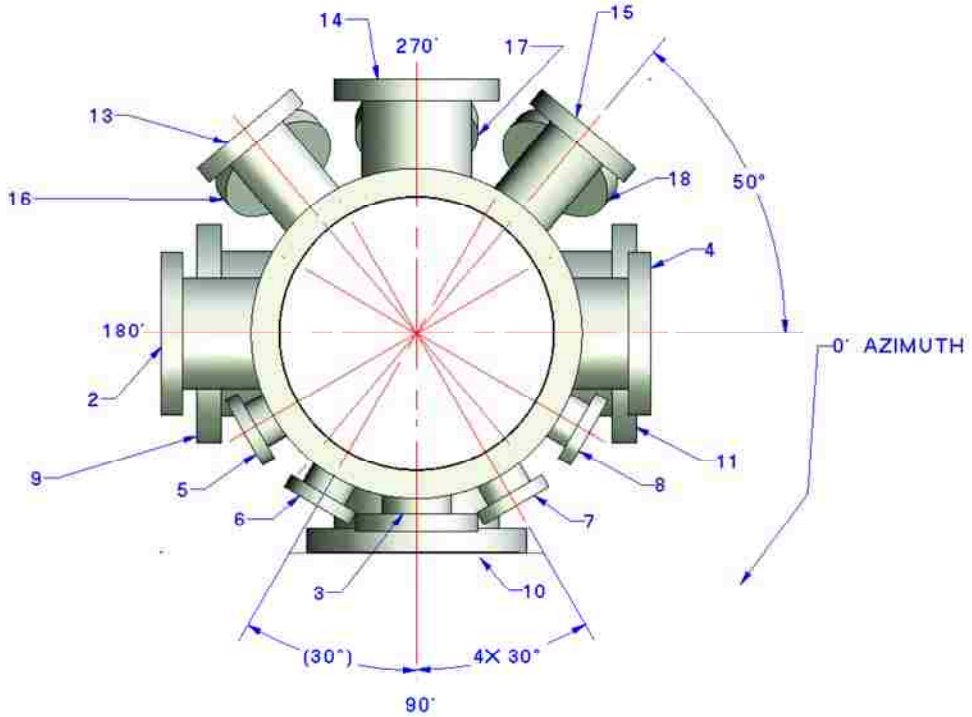
APPENDIX B MBE Chamber Design Specifications



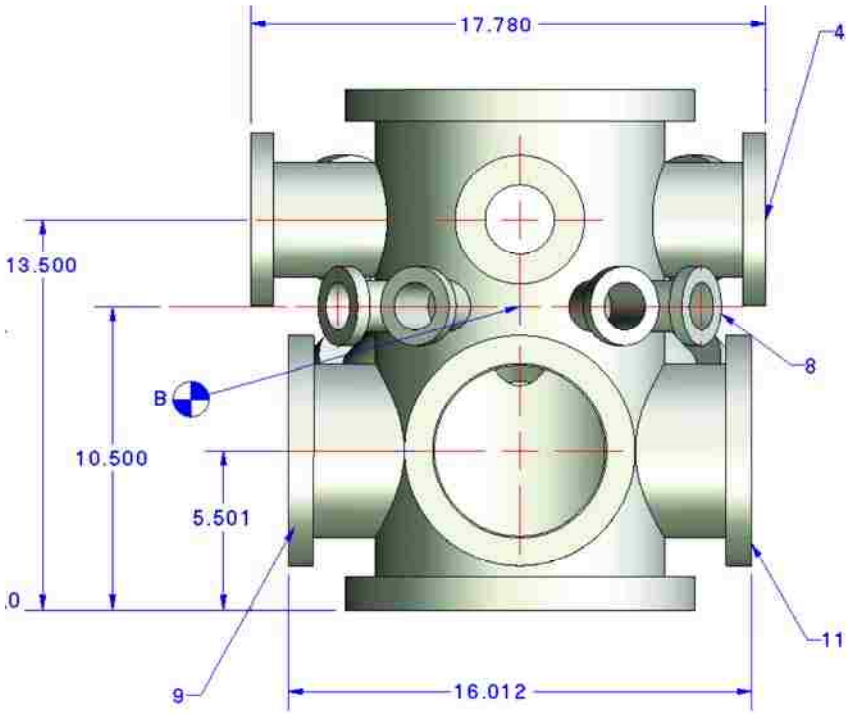
Chamber Port Specifications						
Port #	Flange Size	Tube OD	Focal Point	Focal Length	Azimuthal Angle	Polar Angle
1	12	10	A	4.5	0	0
2	6	4	A	9.28	180	90
3	4.5	2.5	A	7.25	270	90
4	6	4	A	8.5	0	90
5	2.75	1.75	B	7.25	210	90
6	2.75	1.75	B	7.25	240	90
7	2.75	1.75	B	7.25	300	90
8	2.75	1.75	B	7.25	330	90
9	8	6	C	8	180	90
10	8	6	C	8	270	90
11	8	6	C	8	0	90
12	12	10	C	5.5	0	180
13	4.5	2.5	A	9.75	230	90
14	6	4	A	9.28	270	90
15	4.5	2.5	A	9.75	310	90
16	4.5	2.5	A	10.25	230	125
17	4.5	2.5	A	10.125	270	130
18	4.5	2.5	A	10.25	310	125

All dimensions are in inches

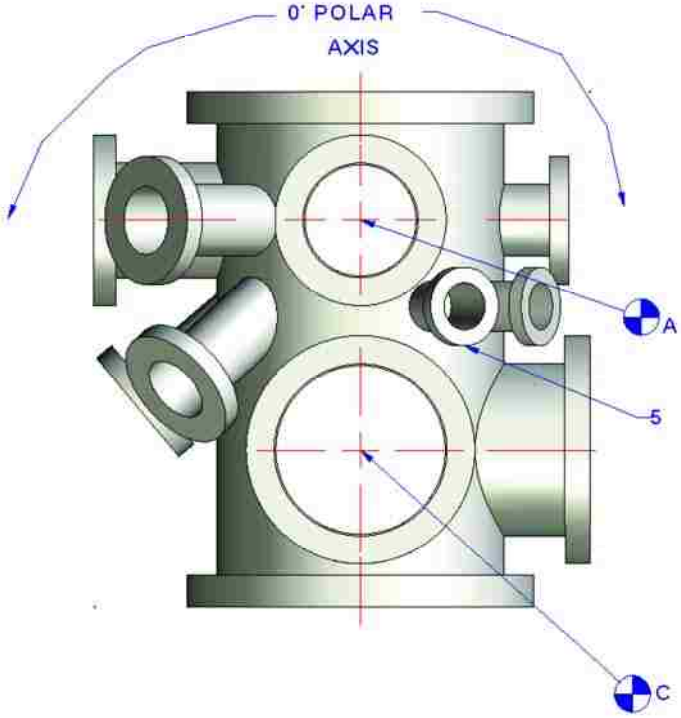
Side View 1



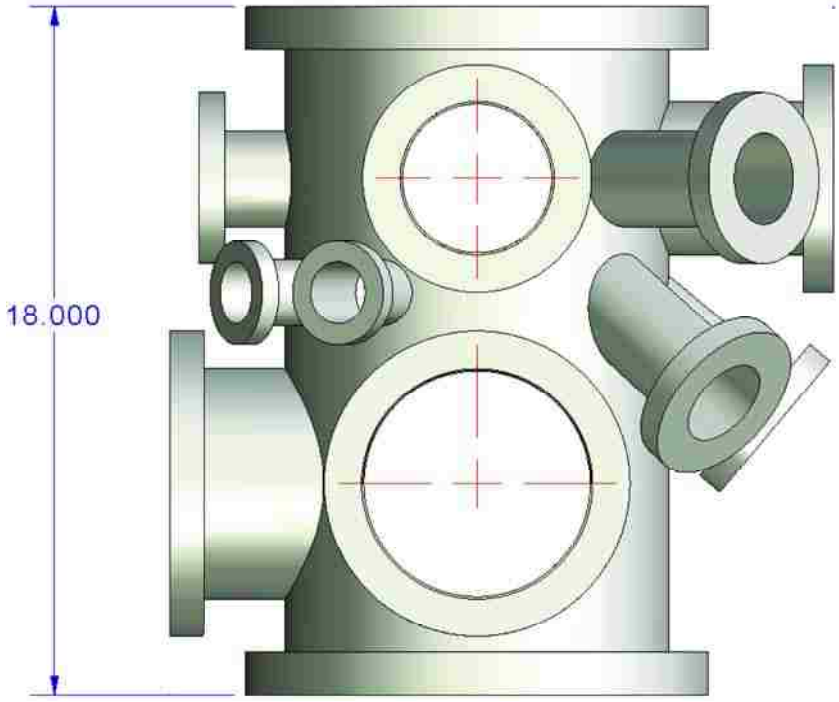
Top View



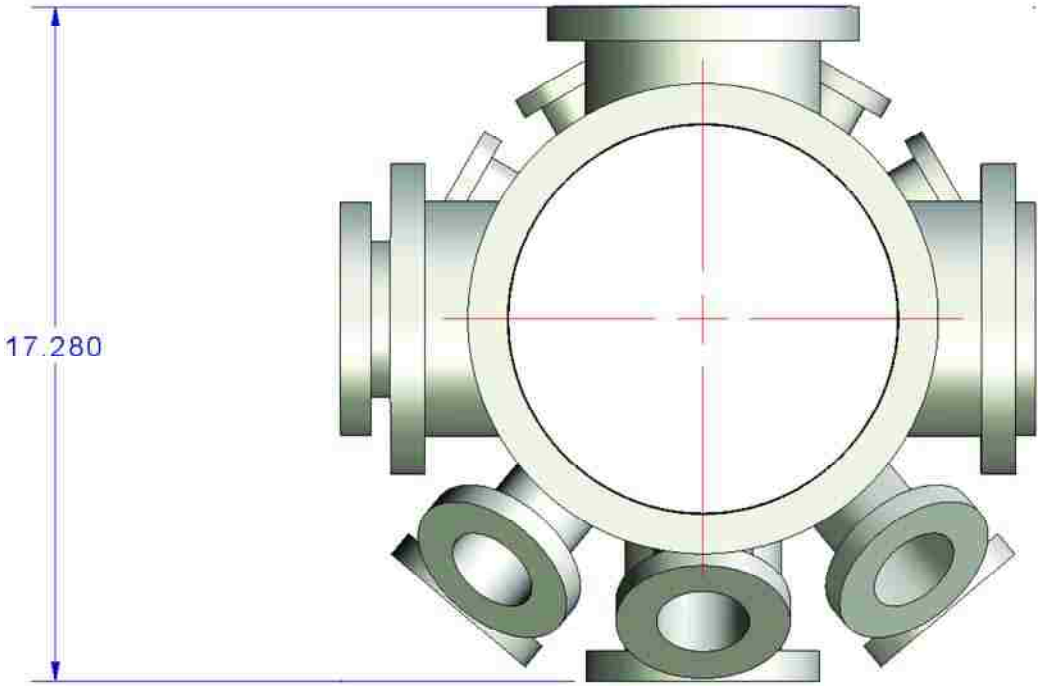
Front View



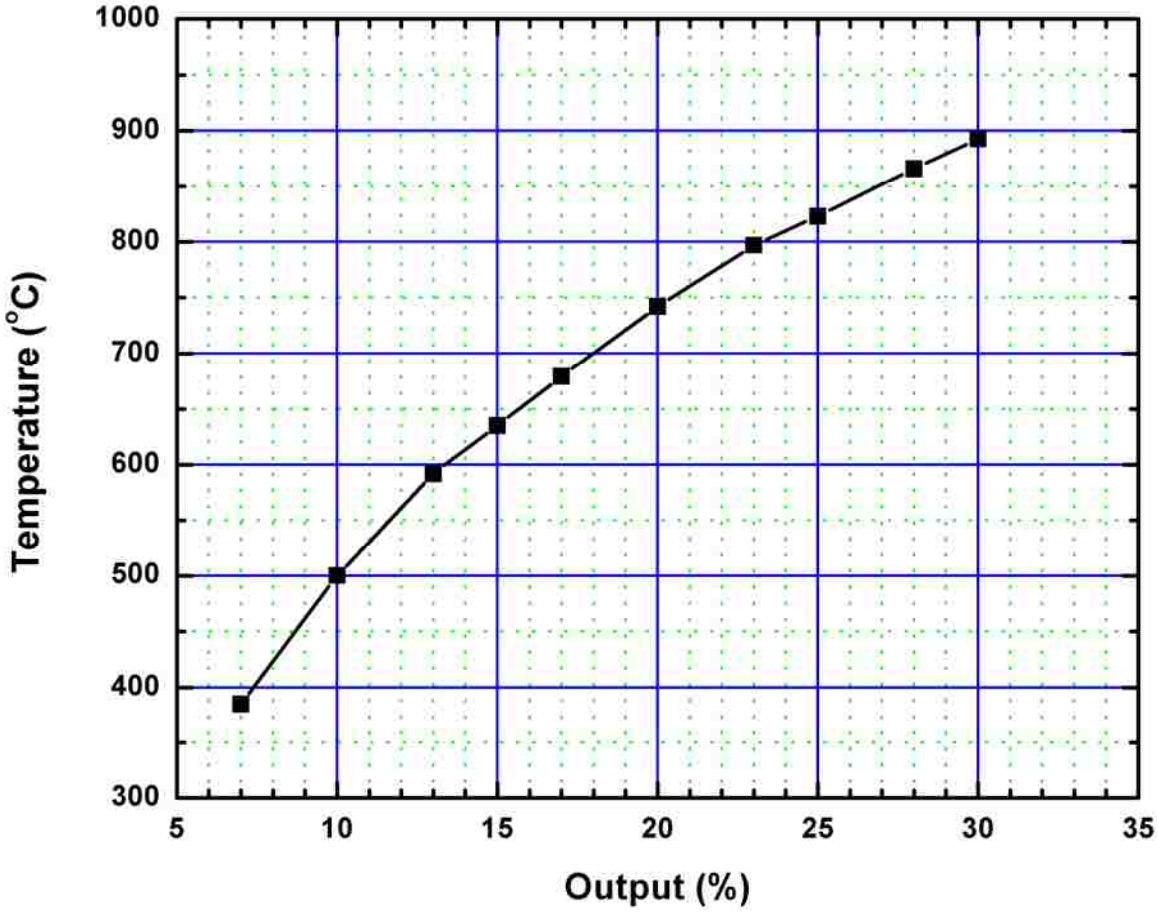
Back View



Side View 2



APPENDIX C MBE Substrate Heater Calibration



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