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Design & Evaluation of a Hybrid Switched Capacitor Circuit with Wide-Bandgap Devices for DC Grid Applications

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DESIGN & EVALUATION OF A HYBRID SWITCHED CAPACITOR CIRCUIT WITH WIDE-BANDGAP DEVICES FOR DC GRID APPLICATIONS

by

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ABSTRACT

As technologies advance, the rate at which renewable power sources, such as solar photovoltaic (PV) and wind, are being added to the power grid is increasing. Typically, PV power plants require large inverters for direct current to alternating current (DC-AC) power conversion, as well as large transformers to step up voltages to the grid voltage. Offshore wind farms and large PV power plants in remote locations often aggregate power on a DC bus in order to improve efficiency and reduce the cost of power conversion hardware within the energy complex. However, the power must still be converted to AC for integration into the grid. Research is being done to allow greater adoption of low, medium, and high voltage DC distribution, wherein DC power is used directly by loads. This has the potential for additional cost savings. To better realize this vision, however, new DC-DC converter technologies must be developed that are small, cheap and efficient at the voltages and power levels relevant to grid integration.

This project demonstrates the feasibility of a switched capacitor boost converter topology that is scalable to 10 kilovolts, and can serve as an interface between lower

voltage PV arrays and medium voltage DC (MVDC) distribution lines. In particular, this approach relies on switched capacitors, wide-bandgap (WGB) devices, and high-frequency switching to achieve high power density and high gain. As part of this work, two prototypes were constructed including a benchtop-scale prototype rated for 25W at 500 Volts and a grid-scale prototype rated for 6 kW at 10 kV. In particular, this second converter was demonstrated in hardware to deliver 2.56 kW at 10 kV DC to a resistive load with greater than 95% efficiency. Using validated models, the converter is predicted to have a CEC equivalent efficiency of 93.8%, demonstrating the feasibility of this converter for grid applications.

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ABBREVIATIONS & ACRONYMS

AC	Alternating Current
CEC	California Energy Commission
DC	Direct Current
DOE	Department of Energy
FET	Field Effect Transistor
FOM	Figure of merit
GaN	Gallium Nitride
HSCC	Hybrid switched capacitor circuit
IGBT	Insulated gate bipolar transistor
JBS	Junction Barrier Schottky
KCL	Kirchoff's Current Law
KVL	Kirchoff's Voltage Law
MPPT	Maximum Power Point Tracking
MVDC	Medium Voltage Direct Current
PV	Photovoltaic
SC	Switched capacitor
Si	Silicon
SiC	Silicon Carbide
UWBG	Ultra-wide Bandgap
WBG	Wide bandgap

I. Introduction

In this chapter, the motivation for developing advanced power electronics and thus a new topology is first reviewed. The particular value of using wide-bandgap devices is then explained. Then, the performance gaps of existing circuit topologies are explained with respect to high-gain applications. Finally, an overview of the work done under this thesis is given, and the layout of the thesis is described.

A. Motivation for High-Performance Power Electronics

Demand for renewable energy is increasing, and most of these new energy sources are coupled to an AC grid through power electronic based power converters and large bulky isolation transformers. Key institutions such as the DOE Energy Efficiency and Renewable Energy (EERE) office are targeting 100s of GW of installed photovoltaic (PV) capacity in the coming decades [1]. Despite the popularity of residential solar, the majority of PV generation and growth remains in commercial and utility-scale. A large impediment to fulfilling state and utility renewable portfolio standards is the high levelized cost of solar PV energy ($109.8/MWh) compared to other sources (e.g. a conventional coal plant at $60.4/MWh) [2]. This disparity in cost is due primarily to the high installed cost of commercial and utility-scale solar PV systems (relative to capacity factor), which currently totals between $1.77/Watt and $2.28/Watt [3]. Furthermore, inefficiency and construction costs associated with AC distribution and transmission and DC-AC conversion are motivating many, including the U.S. Department of Energy (DOE), to consider advocating direct connection of PV to DC distribution (and even DC transmission) circuits. With projected installations of renewable energy that connects to the grid through a power electronic converter, it is projected that 80% of electrical energy will pass through a power

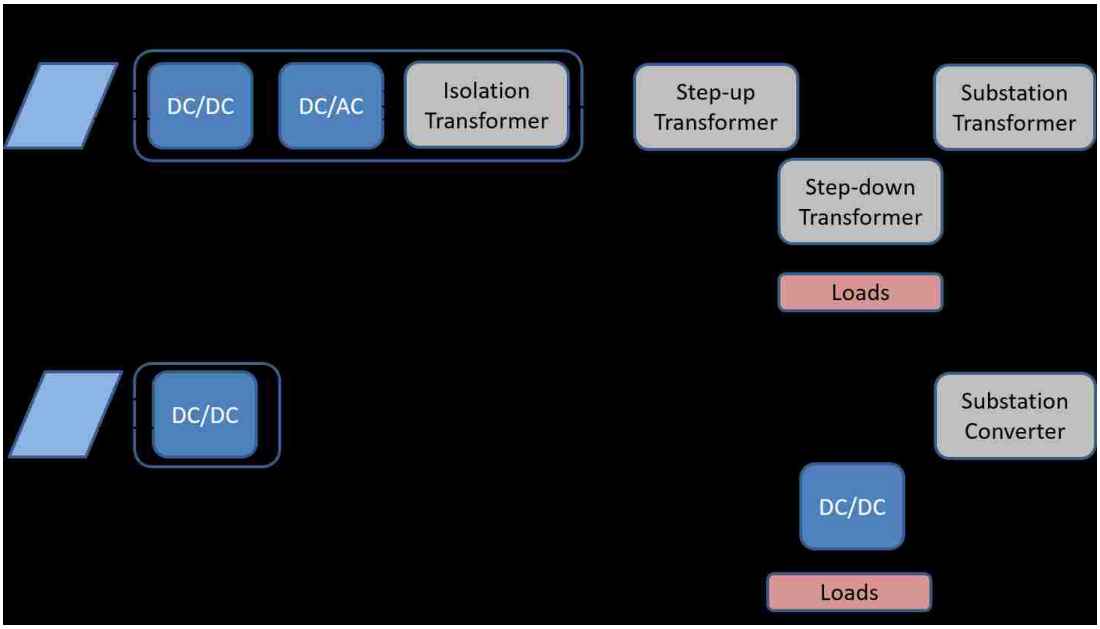

Figure 1: Typical PV AC grid integration diagram (top); Proposed PV DC grid integration (bottom)

electronic converter by 2030 [4]. Using newly developed power electronics with WBG devices can reduce power loss by 27% which equates to an approximate 8% reduction in total U.S. energy consumption.

Figure 1 compares a typical AC grid tied PV installation and a candidate MVDC grid. Typically, the PV array connects to the AC grid through an inverter at a low voltage. It may then pass through multiple other transformers to achieve distribution and transmission voltages. The proposed MVDC grid solution will allow the PV array to connect directly to a DC grid through a single DC-DC converter at a medium voltage. MVDC grids have been shown to be more efficient then AC grids that are subject to the skin effect and proximity effect and require larger conductors for the same power delivery [5]. Overall, an MVDC grid can help reduce the levelized cost of energy.

These predicted needs and benefits have motivated several institutions to set goals for power electronics performance [6]. For example, the US department of Energy Office

of Energy Efficiency and Renewable Energy (DOE/EERE) has targeted 100 W/in^3 and 98% efficiency [7]. In the recent 2014 Google/IEEE Little Box Challenge, institutions were given the challenge of designing the best inverter with specifications such as the ability to handle up to 2 kVA loads, power density greater than or equal to 50 W/in^3, 450/240 V AC-DC conversion with an efficiency of greater than 95%, conform to specific EMI standards, and many more all while undergoing testing for 100 hours. The winner, deemed by a panel of judges, received $1 million [8].

An advancement that has the potential to enable the above performance metrics is the development of new wide-bandgap semiconductor materials and devices.

B. Wide-Bandgap Devices

In contrast to conventional semiconductor materials, such as silicon and germanium, wide-bandgap materials have a larger bandgap, translating to higher breakdown voltages, lower junction capacitance, and higher operating temperature. This can enable converters that operate at higher voltage, switch faster, and have smaller thermal management systems. In particular, the performance of semiconductor materials is often characterized by various figures of merit (FOM) [6]. Figure 2 compares the breakdown voltage verses specific on-resistance for a given area of various materials; silicon, WBG, and even ultra-wide bandgap (UWBG) [6]. Higher electric fields are required to create breakdown due to the higher bandgaps. This paired with the lower on-resistance makes WBG and UWBG devices of particular interest for power conversion.

Commercial-scale and utility-scale PV inverter installations still primarily utilize silicon IGBT based power electronics that switch at low frequencies (5-15 kHz) and interface to the grid through multiple step-up transformers. IGBTs have a high on-state

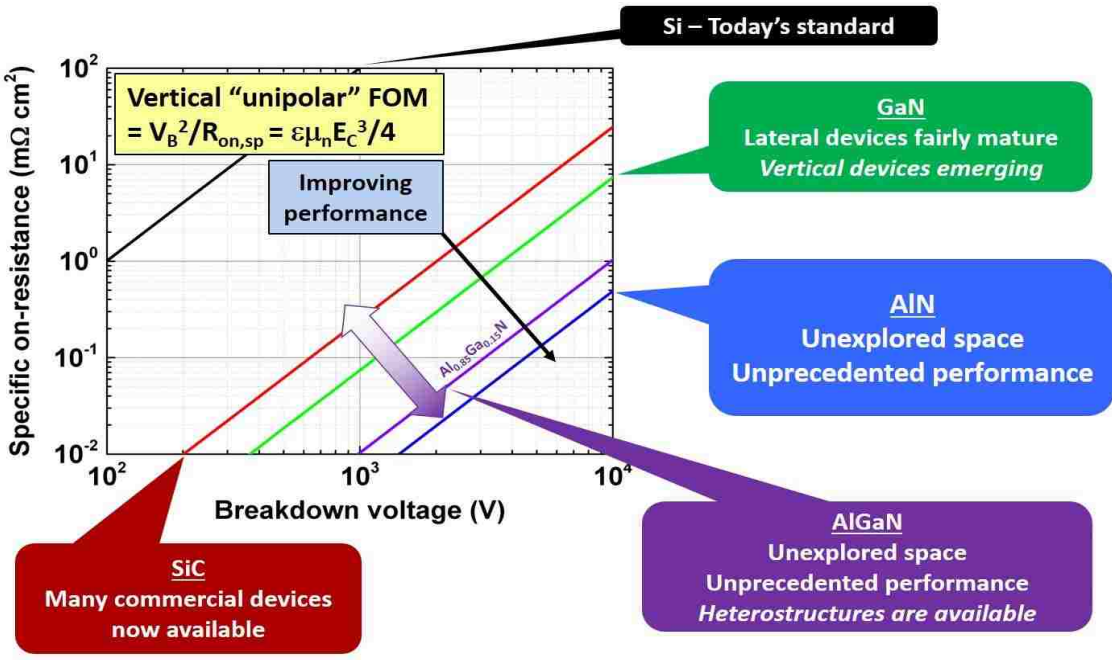

Figure 2: Vertical Unipolar FOM for several semiconductor materials; used with permission from [6]

voltage drop due to the same properties that give them their high blocking voltage. Due to a buildup of minority carriers during forward conduction, they experience a tail current when the gate signal is removed which results in a slow switching frequency. It is important to reduce parasitic inductance as inductance increases the fall time by increasing length of the tail current [9],[10]. Existing commercial PV inverters using IGBTs for switching typically average just 3.5-5.0 W/in^3, making the power electronic converter physically large and consequently a large fraction of the installed cost.

WBG devices also allow higher temperature operation which translates to less thermal management requirements. One estimate was that the heat sink size of a 10 HP electric motor drive could be reduced by 66% if WBG devices were used [11]. Due to smaller junction capacitances, these devices also operate at higher frequencies and have higher breakdown voltages. Filter components in power electronic converters scale with

the operating frequency; so, increasing frequency typically allows for smaller capacitors and inductors. For instance, the 2010 Toyota Prius was investigated in [12] where the power electronics operate at frequencies as low as 5 kHz using IGBTs. A low impedance bus was designed for use with WBG devices allowing 100 kHz operation and reducing the DC link capacitance from 888 µF using large film capacitors to 50 µF using ceramic chip capacitors. It can be found that for a specific R_{on}, when comparing WBG to Si, the smaller die size of WBG devices result in lower capacitance, which allows for quicker turn-on and turn-off times. The decreased turn-on and turn-off times lead to higher efficiencies due to less switching loss.

To realize the full potential of WBG materials and devices, the converter must be designed around the device. The benefits of WBG may not be fully exploitable by simply swapping silicon devices for WBG devices using classical converter topologies. Also, the capabilities of WBG have not been demonstrated in all device types. For example, while silicon carbide MOSFETs and GaN diodes have reached high hold-off voltage, GaN FETs remain limited to lower voltages (i.e. 650V) that are not conducive to grid applications using standard topologies.

C. Boost Converter Theory of Operation and Performance Limits

Although there are many topologies for power converters, they primarily perform one of two functions; step up (boost) or step down (buck) output voltage levels. Some applications, such as charge controllers, require a topology such as the buck-boost converter which provide step up and step down capabilities in one circuit.

The boost converter is a subset of two-level converters in which the output voltage is higher than the input voltage. The term two-level comes from the two voltage levels seen

on the inductor waveform. The classic boost converter schematic is shown in Figure 3. Normally, the switch would be a transistor, but this schematic helps illustrate the two basic states of the boost converter. The circuit is continuously switching between two states at a given frequency to maintain the desired output voltage. The ratio of the period *T* that the switch is on compared to the entire period is referred to as the duty cycle *D* and shown by (1.1). Whereas, the portion of the period that the switch is off compared to the entire period is given by (1.2).

$$D = \frac{T_{on}}{T} \tag{1.1}$$

$$D' = \frac{T_{off}}{T} = (1 - D) \tag{1.2}$$

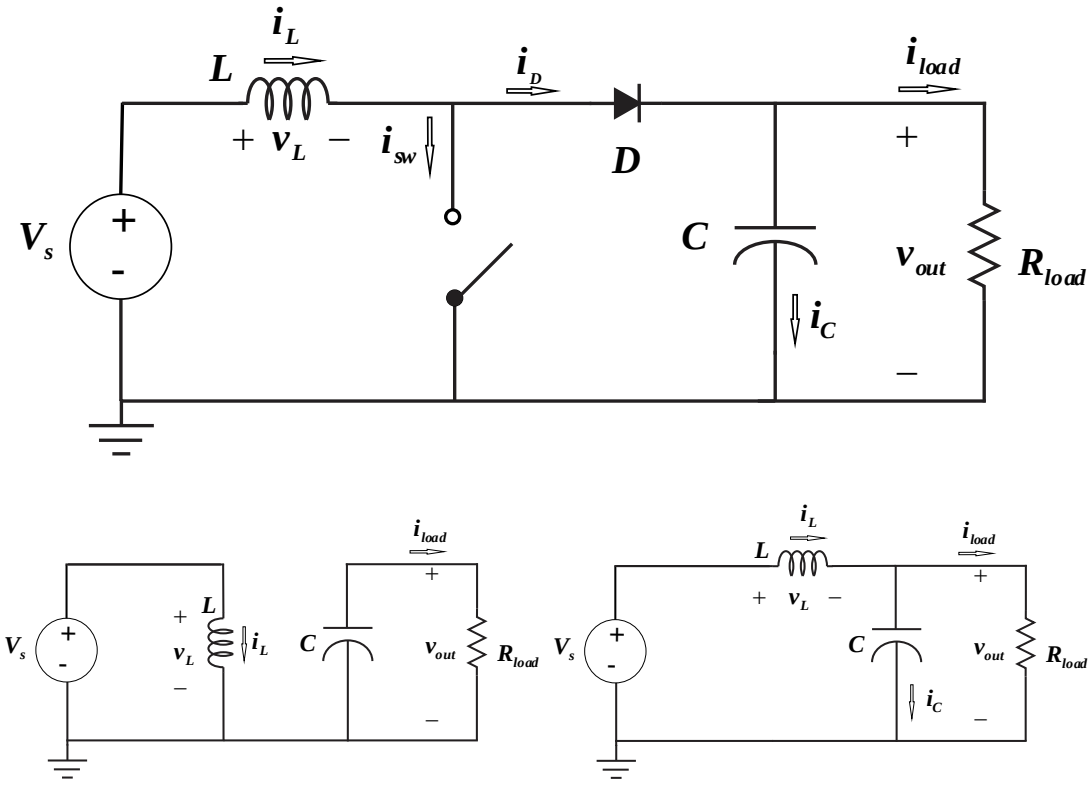

Figure 3: Boost converter schematic (top); State 1 (bottom left); State 2 (bottom right)

For DC-DC converters, the inductor is typically the primary energy-transfer element. Using the volt-second balance principle for steady-state operation and Kirchoff's voltage law (KVL), (1.3) is formed where V_s is the source voltage and V_o is the output voltage. The duty cycle is related to V_s and V_o with (1.4).

$$V_L = V_s D + (V_s - V_o)D' = 0 \tag{1.3}$$

$$D = 1 - \frac{V_s}{V_o} \tag{1.4}$$

With the switch closed, the boost converter is in state 1. A current path is created from the source, through the inductor, to ground. The voltage across the inductor is the source voltage causing the current in the inductor to increase in a ramp fashion. The increasing energy is stored in the inductors magnetic field. The change in inductor current compared to the average inductor current is also known as *inductor current ripple* and is given by (1.5) and (1.6) where f=1/T.

$$\Delta I_L = \frac{1}{L}\int_0^{DT} V_s dt \tag{1.5}$$

$$\Delta I_L = \frac{DV_s}{2Lf} \tag{1.6}$$

The source is short circuited to ground through the inductor; therefore, this state can only be maintained for a portion of the period. Although the inductor current is changing with time, an average value can be found. Using the ideal steady-state relationship equating power into and out of a system, (1.7) can be rearranged also using Ohm's law to form (1.8).

$$P_o = P_s \tag{1.7}$$

$$I_L = \frac{V_o I_o}{V_s} = \frac{V_o^2}{V_s R} = \frac{V_s}{RD'^2} \tag{1.8}$$

In order for this converter analysis to remain valid, the inductor current must remain in continuous conduction mode (CCM), meaning that the inductor current must always be greater than zero. A tradeoff is typically seen when seeking lower current ripple and smaller component size. The magnetic field in lower value inductors collapse at a higher rate when compared to larger components at the same frequency; therefore, lower value components lead to a higher ripple value. Equation (1.9) relates the minimum inductor size L_{min} to the source voltage, duty cycle, frequency, and inductor current ripple.

$$L_{min} = \frac{V_s D}{\Delta i_L f} \tag{1.9}$$

Capacitors are often sized based on their peak voltage and the maximum allowable deviation from the nominal DC voltage. The peak ripple is expressed in (1.10) as a voltage. Voltage ripple is often specified as a maximum percentage and can be found by (1.11).

$$\Delta v = \frac{V_o D}{2RCf} \tag{1.10}$$

$$\frac{\Delta v}{V_o} = \frac{D}{2RCf} \tag{1.11}$$

During state 1, the diode is reverse biased preventing the output capacitor from discharging into the left half of the circuit. Energy stored in the capacitor's electric field is used to supply the load. The switch is closed for only a fraction of the period; therefore, the output capacitor maintains its voltage level, neglecting the ripple. Inductor voltage and capacitor current are given by (1.12) and (1.13) respectively.

$$v_L = V_s \tag{1.12}$$

$$i_c = -v/R \tag{1.13}$$

While the switch is open, the boost converter is in state 2. Current will flow through the series-connected inductor and diode to supply the load while also charging the output capacitor. As time progresses the inductor's stored energy will decrease causing the current to drop again in a ramp, but with a negative slope. In this state, the inductor voltage and capacitor current are given by (1.14) and (1.15) respectively.

$$v_L = V_s - v \tag{1.14}$$

$$i_c = i_L - v/R \tag{1.15}$$

The boost converter steady-state output voltage is given by rearranging (1.4) to form (1.16).

$$V_o = \frac{V_s}{1-D} \tag{1.16}$$

Although it appears that an infinite gain may be achieved by letting the duty cycle approach 100%, a real circuit has a *critical duty cycle* for which anything greater will start to decrease gain due to various reasons including insufficient input power or an increase in switch resistance caused by a temperature increase [13], or other circuit losses. Furthermore, it is suggested that a duty cycle of no more than 80% be used due to the increased control complexity resulting from its large nonlinearity for anything greater. Taking this into consideration, the conventional boost converter has a gain limit of about 5 in practice [14].

D. High-Gain Converter Topologies

Over the years, research institutions have investigated various topologies to improve converter size, weight, and power (SWaP) metrics. A common converter used to boost voltage is the switched capacitor (SC) circuit. With this topology, capacitors are charged in parallel with a voltage source placing them at the same potential. Once charged, an active switch changes the configuration so that capacitors are then in series boosting the

voltage. High voltage gains can be achieved by adding additional capacitors but with the penalty of also adding active switches and increasing the control complexity.

In [15] a converter is presented using an autotransformer and coupled inductor on the same core along with various passive components and a single switch to achieve a full load gain of approximately 14. Although the switch only goes through two states, on and off, the converter actually transitions through three distinct modes due to the diodes as the capacitor voltages drop with the switch being off. The authors incorporated features that harvest leakage energy in one mode and deliver it to the load in another mode, to improve efficiency.

In [16] a GaN-based flying-capacitor multilevel boost converter is proposed. Only a single inductor is necessary, and voltages are balanced across flying capacitors. Diodes between each flying capacitor only conduct for a fraction of the period keeping switching conduction loss low. Since the voltages are distributed, the use of GaN transistors reduce switching loss even with high frequency switching. This circuit offers a large increase in SWaP due to its high-gain and minimal use of inductors. Although this topology offers the benefit of high-gains, the control requirements are complex due to individual switching requirements for each FET.

A high-gain topology controlled using only a single switch is discussed in [17]. This topology is referred to here as the hybrid switched capacitor circuit (HSCC). Having an input stage equivalent to a traditional boost converter, the HSCC can be controlled by a single active switch. Gains greater than the traditional boost converter can be realized through a charge pump type mechanism using diodes for switching the capacitors in various series/parallel configurations rather than an active switch, thus reducing control

complexity. In this topology, various levels of gain can be achieved, similar to [16] by increasing the number of capacitor/diode cells, referred to here as a "stage". In addition, since this circuit makes heavy use of diodes, there is a strong potential that this circuit could benefit from high voltage GaN diodes and potentially even UWBG diodes.

The HSCC will be the primary focus of this paper and is discussed in detail in the following chapter.

E. Document Layout

This work will present the design and analysis of a HSCC using WBG devices in conjunction with hardware results. Chapter II combines the fundamental analysis of a boost converter presented in Chapter 1 Section C and expands it to the HSCC. An idealized representation of how the circuit operates is visualized from Spice results. A state-space approach is also presented using an aggregated input/output behavior model in an attempt to simplify the analysis.

Before the prototypes were built, circuit simulations were performed. Chapter III focuses on the results obtained from a lower-power prototype (i.e. the "evaluation circuit") for preliminary evaluation of the concept and the grid-scale (6 kW 10 kV) bipolar HSCC prototype. Techniques for obtaining detailed models and the process for validation are also presented in this chapter.

Chapter IV details the construction and testing of the evaluation circuit. Board layout techniques are also discussed. Hardware results are presented showing graphs to show output voltage vs efficiency, output voltage vs frequency, gain vs frequency, efficiency vs frequency, duty cycle vs input voltage, and efficiency vs input voltage.

The 6 kW 10 kV bipolar HSCC prototype is presented in Chapter V. Design decisions that were made to allow flexibility with testing are explained. Various loads are tested and results are given which represent different power levels; these results were used to validate the simulation models.

Chapter VI gives a side by side comparison of hardware and simulations results. After validating the full scale HSCC model with hardware, the model was used to predict the converter's California Energy Commission (CEC) equivalent efficiency. A detailed approach is described, and the final CEC equivalent efficiency is given.

Chapter VII summarizes this project's findings and suggests future work to reach a target power density of 100 W/in^3.

The Spice models were at times altered for the circuits. The custom changes for the evaluation circuit are included in Appendix A. Appendix B shows a Spice circuit schematic for the evaluation circuit. Appendix C shows a circuit diagram that was developed in Spice and used for the full scale model.

II. HSCC Theory of Operation

The HSCC is a combination of the traditional boost converter topology and a SC circuit, which in this case includes a diode-capacitor ladder, to implement a charge pump. The gain of an idealized traditional SC circuit can be found with (2.1) where *N* represents the number of additional charge pump stages. Combining (1.15) and (2.1), the output of the idealized HSCC is determined by (2.2).

$$V_{o,CP} = (N+1)V_{s,cp} \tag{2.1}$$

$$V_{o,HSCC} = \frac{(N+1)V_s}{1-D} \tag{2.2}$$

In this topology, there is only one controlled switch, but much of the gain relies on switching within the network of diodes and capacitors in the output stage. For this circuit, each stage is characterized by the addition of two capacitors (top rail and bottom rail) and two diodes in series. A two-stage converter is shown in Figure 4. As with the classical boost converter, this simplified HSCC will be analyzed. It was observed through simulation that for an ideal HSCC, there are additional modes *m* for each additional stage. The number of modes can be identified with (2.3). An example will be analyzed further.

$$m = 2(N+1) \tag{2.3}$$

A. Two-Stage HSCC Analysis

For the two-stage HSCC, (2.3) gives 6 modes throughout one switching period. There are 3 modes with the switch ‘on’ and 3 with the switch ‘off’; see Figure 4. To help clarify simulation results, capacitors on the bottom rail (odd numbered) were made 10 times larger than the top rail (even numbered) capacitors. This helped to stabilize the lower rail during switch transitions and reduce high frequency content seen through the circuit. It also allows for the assumption that the lower rail voltages are approximately constant,

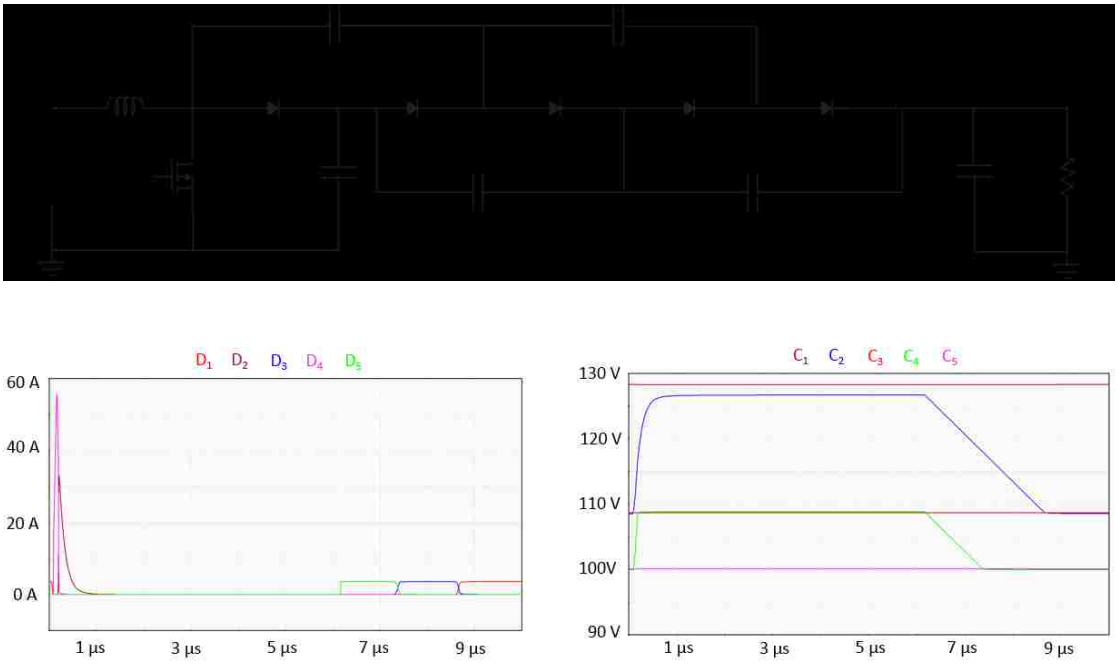

Figure 4: 2-Stage HSCC (top); Diode current profile (bottom left); Capacitor voltage (bottom right)

compared to those of the upper rail. Without loss of generality, it is assumed that all diodes turn on/off instantly and there is no overlap in their conduction times; however, this condition may be relaxed with the addition of operational modes to increase fidelity. As long as the inductor current stays positive, it behaves similar to that of the traditional boost converter in CCM. For steady-state analysis it is assumed that the voltage at the output is always greater than the input. Therefore, positive current flow into each capacitor is defined from right to left using passive sign convention. State 1 corresponds to the switch closed and the inductor charging. The diode-capacitor ladder transfers charge according to the current mode and maintains the output voltage. State 2 corresponds to the switch open and the inductor transferring its stored energy to the capacitors and load. Importance was placed on determining the diode switching and conduction pattern of the general HSCC. The

following analysis is based on Spice simulation using ideal components with no parasitics with exception to the 852 mV voltage drop built into the LTspice default diode model.

Mode 1

When entering state 1, the converter starts in mode 1; see Figure 5. The arrows show the direction of current flow. Even numbered diodes are forward biased placing the bottom rail series capacitors C_1 and C_3 in parallel with the top rail series capacitors C_2 and C_4. Although the lower rail transfers charge to the top rail, the lower rail only experiences minor fluctuations since it is always directly connected between the load and ground. Diode D_4 is the only diode conducting. As C_4 charges and reaches V_{c3}, the converter transitions to mode 2.

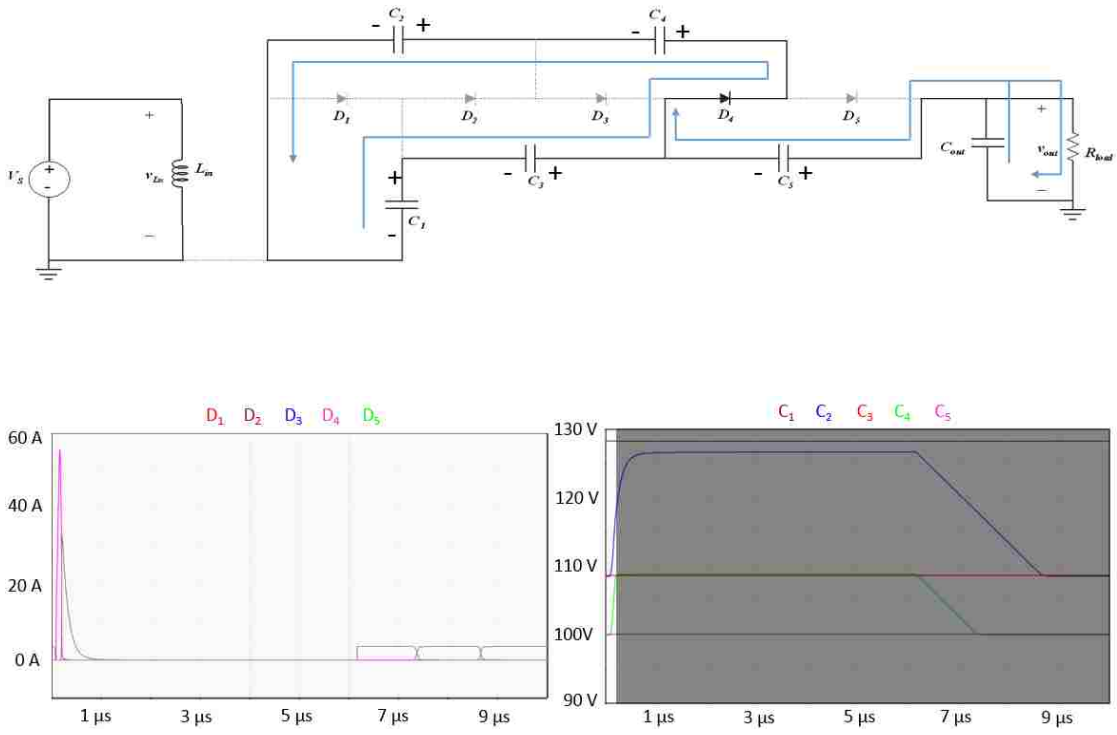

Figure 5: Mode 1 Current flow (top); Diode current (bottom left); Capacitor voltage (bottom right)

Mode 2

During mode 2, diode D_2 is conducting with capacitors C_1 and C_2 in parallel. Charge is transferred from C_1 to C_2 until V_{C2} equals V_{C1}. Figure 6 shows a representative schematic with arrows to indicate current flow. Diode current and capacitor voltage are also shown.

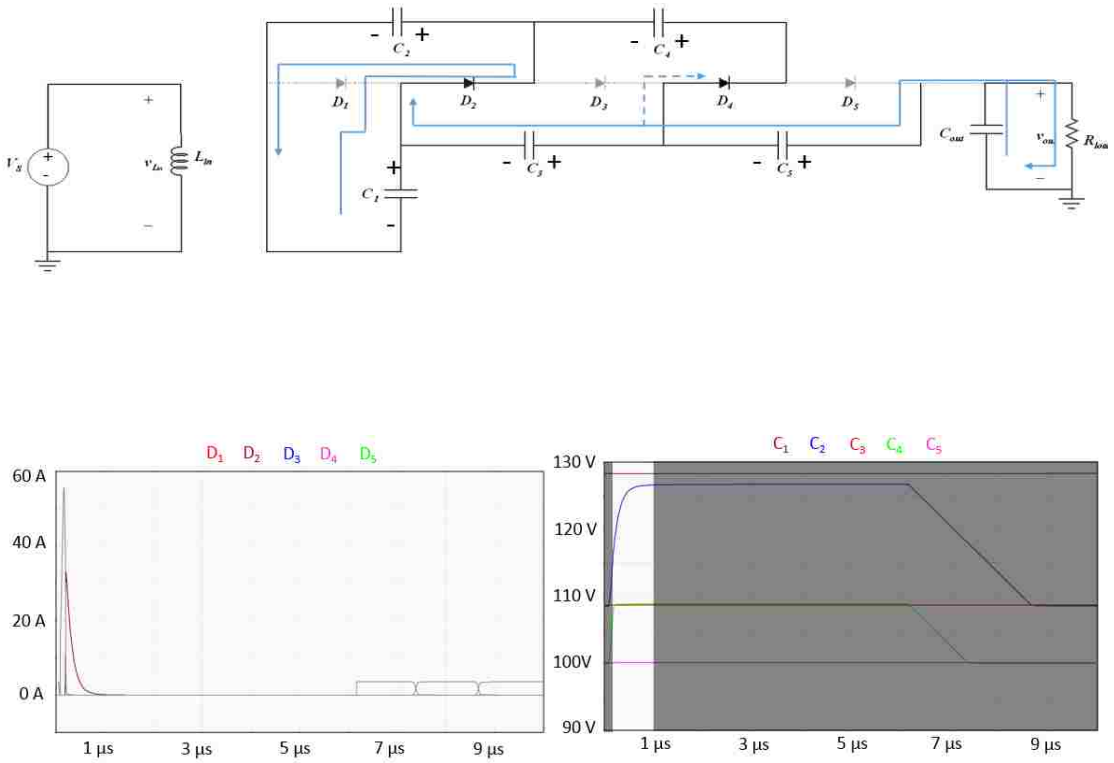

Figure 6: Mode 2 Current flow (top); Diode current (bottom left); Capacitor voltage (bottom right)

Mode 3

In mode 3, the voltage on each top and bottom rail capacitor pair (C_1/ C_2 and C_3/ C_4) are balanced resulting in no current flow. The load voltage is maintained by the capacitors on the lower rail since they have a direct connection; see Figure 7. The inductor current continues to increase until the transition to mode 4.

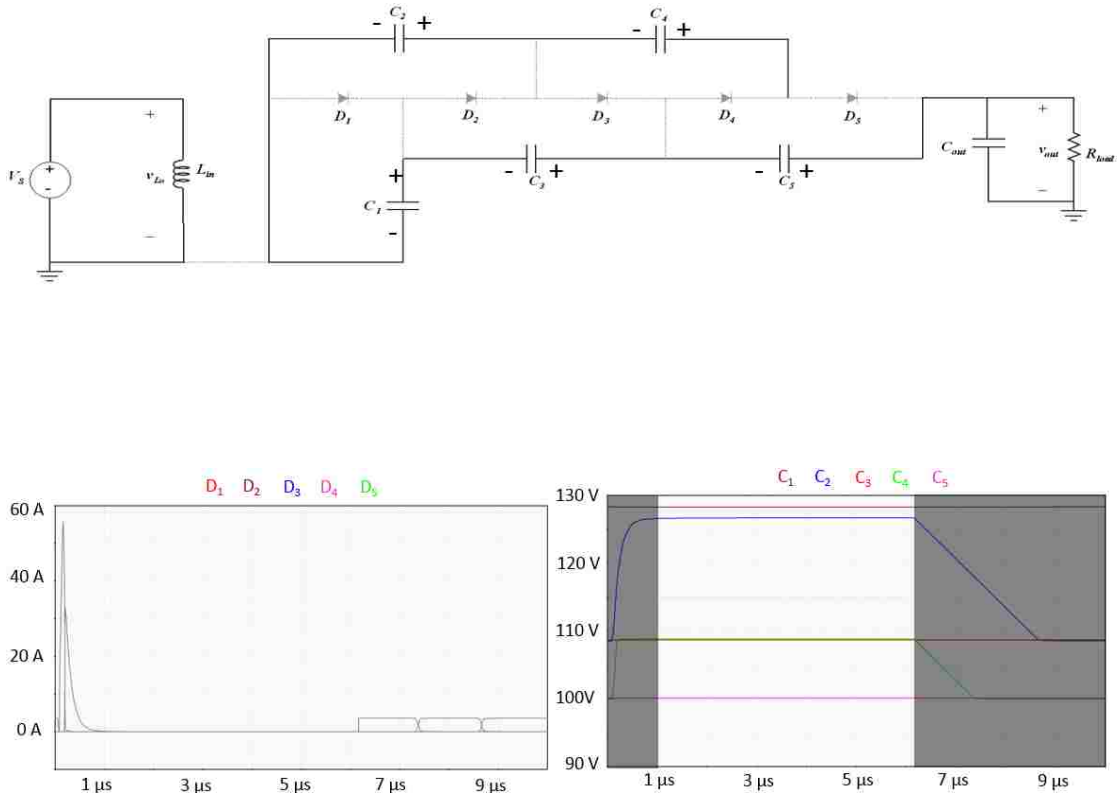

Figure 7: Mode 3 Current flow (top); Diode current (bottom left); Capacitor voltage (bottom right)

Mode 4

When the switch opens, the converter enters state 2 and mode 4; see Figure 8. Odd numbered diodes are now forward biased. The inductor is now connected to the anode of D_1 and the negative (lower potential) side of C_2. The inductor forces it's built up current through series connected C_1 and C_2, through D_5, and supplies the load. Current also branches off to charge series connected C_1, C_3, and C_5. The increase in voltage for these capacitors are very small. Top rail capacitors see a much larger voltage swing since they alternate between a connection from ground to the input inductor. It should be noted that current is flowing from the lower to higher potential through C_2 and C_4 cause the voltage in both of these capacitors to drop. As the voltage of C_4 reaches the voltage of C_5, the converter transitions into mode 5.

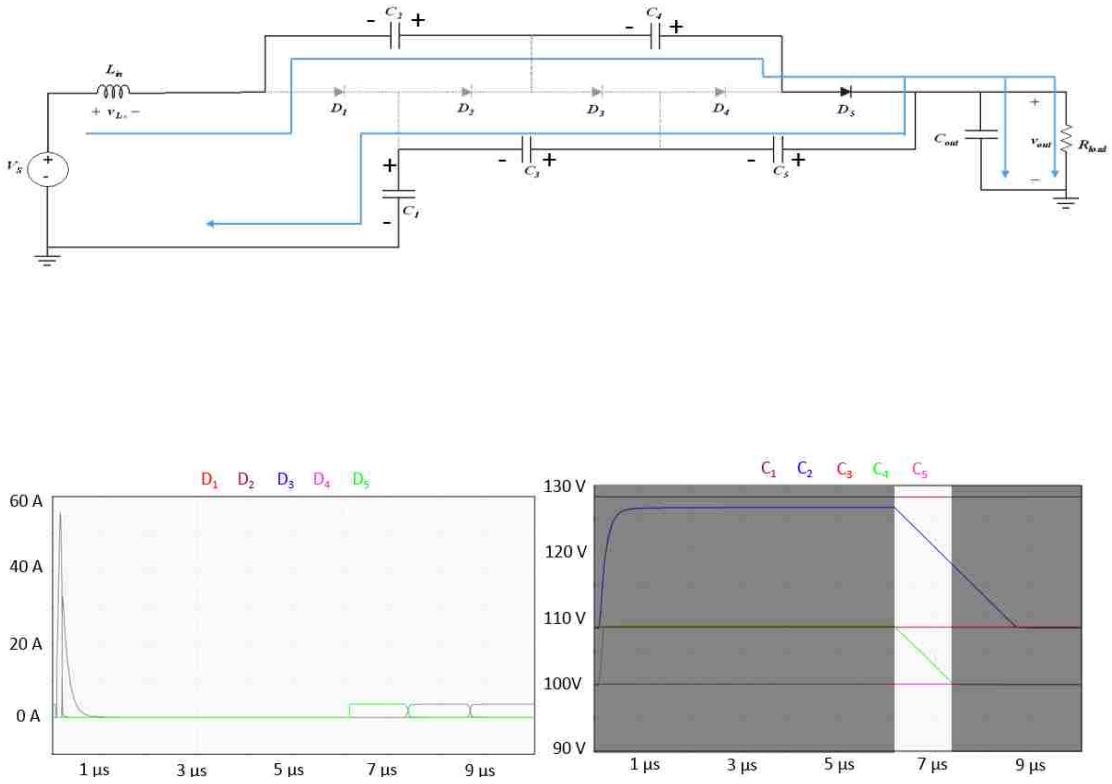

Figure 8: Mode 4 Current flow (top); Diode current (bottom left); Capacitor voltage (bottom right)

Mode 5

In mode 5, the input continues to supply the load and charge the output capacitor; see Figure 9. Diode D_3 is the only diode conducting current continues to charge C_1 and C_3. The voltage of C_2 continues to drop until it matches V_{c3}.

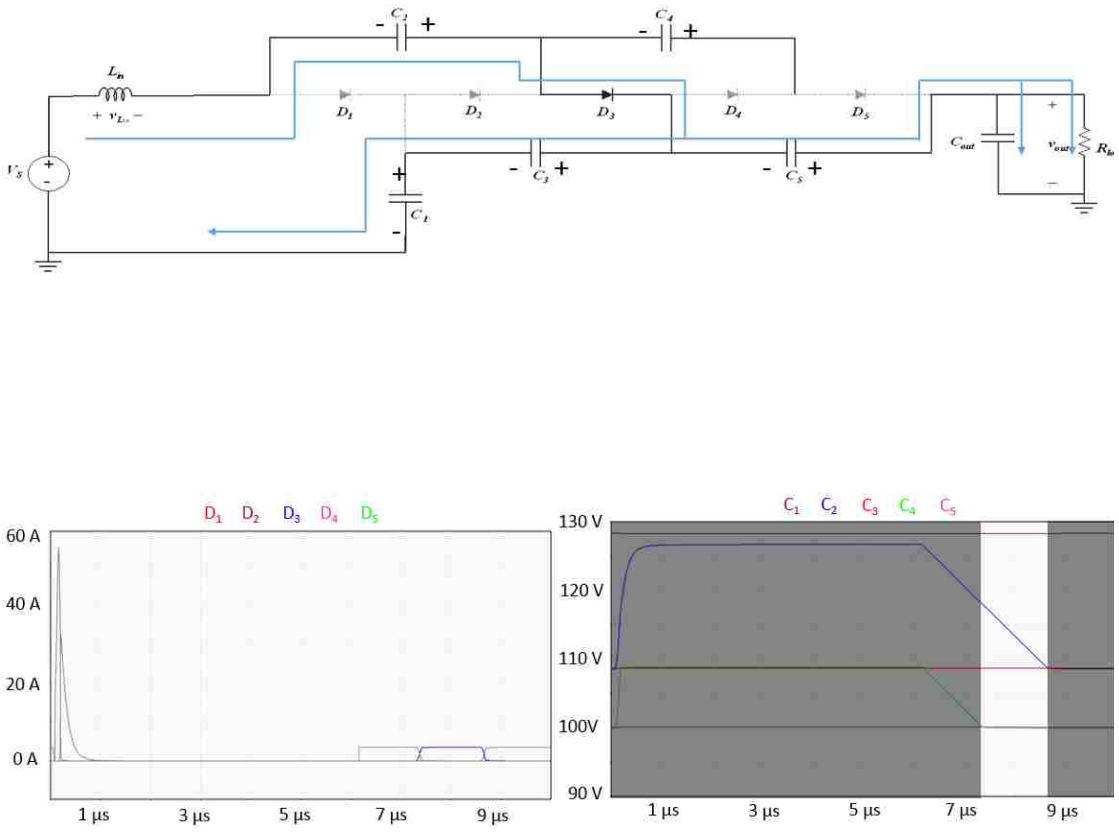

Figure 9: Mode 5 Current flow (top); Diode current (bottom left); Capacitor voltage (bottom right)

Mode 6

A majority of the input current charges C_1 during mode 6; see Figure 10. The remaining portion contributes to charging the output capacitor and supplying the load. In this mode, only D_1 is conducting.

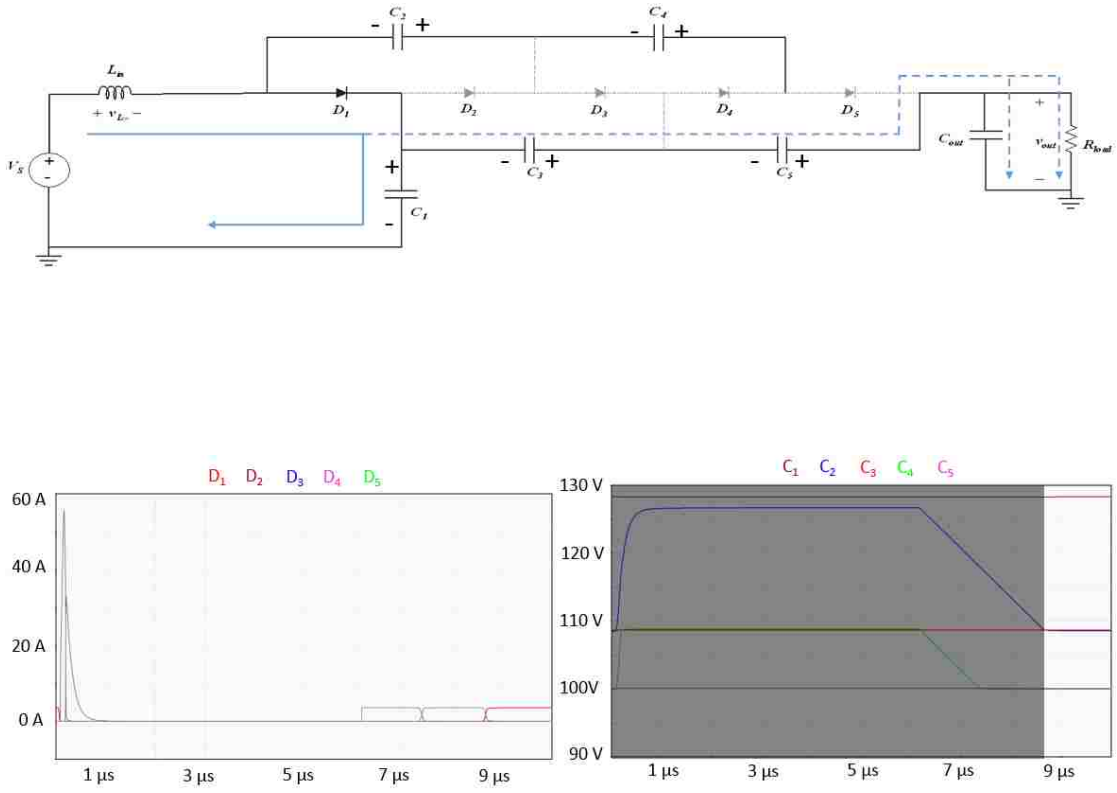

Figure 10: Mode 6 Current flow (top); Diode current (bottom left); Capacitor voltage (bottom right)

An analytical approach was taken to determine a voltage gain function dependent on the number of stages; however, the nonlinearities and complexity of the circuit make it prudent to verify the gain relationship in (2.2) in simulation. Figure 11 shows the simulated output from a traditional boost converter and a HSCC with N=1 and 2 with an input voltage of 100 and duty cycle D=50% Ideal Spice components were used, neglecting parasitics such as ESR and ESL; however, built in diode forward voltage parameters do give slightly non-ideal results. Voltages roughly match what is predicted in (2.2). For N=0, the gain is equivalent to that of a traditional boost converter, approximately 2. For N=1 and N=2, the gain is approximately 4 and 6 respectively, which approximately match simulation results.

B. Switch Mode Circuit Analysis for Boost Converter

Analysis of switch mode converters controlled by pulse-width modulation (PWM) techniques is commonly performed using the state-space averaging method. In this method, a separate circuit corresponding to each switched mode configuration is analyzed.

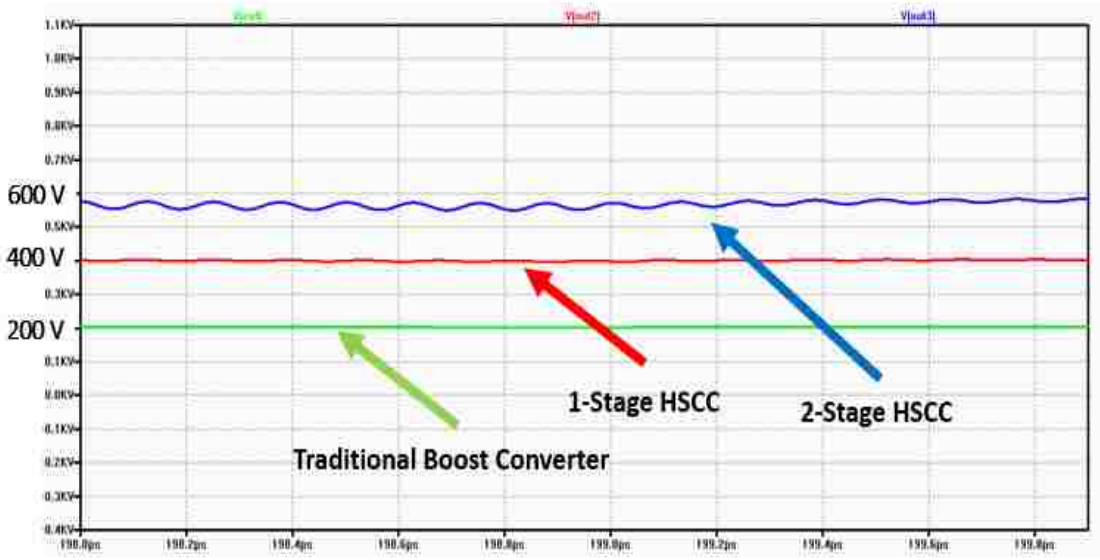

Figure 11: Comparison of output voltage for a traditional boost converter (green), 1-Stage (red), and 2-stage (blue) HSCC

Differential equations are determined for each energy storage element using KVL and KCL to represent inductor voltages and capacitor currents respectively. Equation (2.4) represents the state-space average general form where *d* represents the duty cycle, assuming a time invariant system. Matrices with the subscript "1" represent the switch "on"; whereas, the subscript "0" represent the switch "off". The A_x matrix represents the system and the input matrix is represented by B_x. System inputs during the on and off state are represented by B_1 and B_0 respectively. The output is represented by C_x. Matrix D_x is the feedthrough matrix and is often the null matrix. The state vector $\boldsymbol{x}$ contains the inductor current and capacitor voltage. The vector $\boldsymbol{u}$ contains system inputs.

$$\dot{x} = (A_1\boldsymbol{x} + B_1\boldsymbol{u})d + (A_0\boldsymbol{x} + D_0\boldsymbol{u})(1-d) \tag{2.4}$$

$$y = (C_1\boldsymbol{x} + D_1\boldsymbol{u})d + (C_0\boldsymbol{x} + D_0\boldsymbol{u})(1-d)$$

A reduced-order model is often used to simplify the analysis while still giving an understanding of how the circuit operates. Higher fidelity models may also be analyzed which include parasitics such as switch voltage drops, diode forward voltage, ESR, and ESL. Equations (2.5) and (2.6) are formed using KVL and KCL for $0 < t < DT$ and represented in state-space form by (2.7) through (2.11). The feedthrough matrix *D* is equal to the null matrix.

Switch on:
$$\frac{di_L}{dt} = \frac{(V_s - i_L r_L)}{L} \tag{2.5}$$

$$\frac{dv_C}{dt} = i_L - \frac{v_c}{CR_{load}} \tag{2.6}$$

$$A_1 = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & \frac{1}{CR_{load}} \end{bmatrix} \tag{2.7}$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{2.8}$$

$$C_1 = [0 \quad 1] \tag{2.9}$$

$$\boldsymbol{x} = \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{2.10}$$

$$\boldsymbol{u} = V_s \tag{2.11}$$

For $DT < t < T$, equations are given by (2.12) and (2.13) with state-space representation (2.10) through (2.14)

Switch off:

$$\frac{di_L}{dt} = \frac{(V_s - i_L r_L - v_C)}{L} \tag{2.12}$$

$$\frac{dv_C}{dt} = \frac{i_L}{C} - \frac{1}{CR_{load}} \tag{2.13}$$

$$A_0 = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR_{load}} \end{bmatrix} \tag{2.14}$$

$$B_0 = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{2.15}$$

$$C_0 = [0 \quad 1] \tag{2.16}$$

$$\boldsymbol{x} = \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{2.17}$$

$$\boldsymbol{u} = V_s \tag{2.18}$$

Equation (2.19) through (2.23) represents the averaged state-space form.

$$A = A_1 \mathrm{d} + A_0(1 - \mathrm{d}) = \begin{bmatrix} -\frac{r_L}{L} & \frac{d-1}{L} \\ \frac{1-d}{C} & -\frac{1}{CR_{load}} \end{bmatrix} \tag{2.19}$$

$$B = B_1 \mathrm{d} + B_0(1 - \mathrm{d}) = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{2.20}$$

$$C = C_1 \mathrm{d} + C_0(1 - \mathrm{d}) = [0 \quad 1] \tag{2.21}$$

$$\boldsymbol{x} = \begin{bmatrix} i_L \\ v_C \end{bmatrix} \tag{2.22}$$

$$\boldsymbol{u} = V_s \tag{2.23}$$

In the next section, the HSCC converter model is adapted for use with a state-space model.

B. Aggregated Input/Output Behavior

The HSCC achieves additional voltage gain through the same principle as a charge pump. In an ideal charge pump, multiple capacitors are switched from a parallel to series configuration. In one switching state with the capacitors in parallel, component voltages are equal and capacitors are charged. In the second state, capacitors are switched into a series configuration. In steady-state, charge is transferred to the output and is equivalent to the charge transferred from one capacitor to the next in one switching period [18]. Neglecting the effects of parasitics and assuming all capacitors are the same value, voltage is multiplied by the number of series connected capacitors.

In Section II Part A, diode switching behavior of the HSCC was analyzed which illustrates the complexity of the dynamic circuit behavior. Multiple modes were present for both switch states; $0 < t < DT$ and $DT < t < T$. As the number of stages *N* increase, the total number of modes increase in accordance with (2.3). The multiple modes are present

due to the forward voltage drop of the diodes; modes are changed as capacitors charge and forward bias the diode. It is necessary to predict the behavior of the HSCC with a various number of stages *N*; therefore, an even further reduced order model may be implemented by neglecting the diode forward voltage drop and treating it as an ideal diode. By neglecting the diode forward voltage drop, it can be assumed that all diodes conducting and blocking in a given conduction state do so instantly and simultaneously. In fact, this method of modeling is commonly practiced in the first stage of design to aide in understanding main features of a switching system [19].

A method for predicting converter output behavior was proposed in [20],[21] by regulating instantaneous energy stored in the converter and assuming that input power equals the sum of output power and any loss (2.24). Output voltage and load, V_C and R_{load} respectively, are user defined and used to express output power (2.25).

$$P_{in} = P_{load} + P_{loss} \tag{2.24}$$

$$P_{load} = \frac{v_c^2}{R_{load}} \tag{2.25}$$

Taking advantage of a black box approach (observing total energy stored), performance characteristics can be estimated by representing the HSCC as a simple boost converter with output capacitance of *C'*. Total energy in the HSCC can be shown by (2.26) where *N* is the number of stages and 2*N*+1 is the total number of capacitors.

$$E_{total} = \frac{1}{2} L i_L^2 + \frac{1}{2} \sum_{i=1}^{2N+1} C v_{c_i}^2 \tag{2.26}$$

To find the equivalent capacitance *C'*, equate energy stored in the capacitance in (2.26) using equation (2.27).

$$\frac{1}{2} \sum_{i=1}^{2N+1} C_{v_i}^2 = \frac{1}{2} C' v_{out}^2 \tag{2.27}$$

Expanding and reducing (2.27) gives (2.28).

$$(Cv_1^2 + Cv_2^2 + Cv_3^2 + \cdots + Cv_{2N+1}^2) = C'v_{out}^2 \tag{2.28}$$

Lower rail capacitors, C_x where *x* is odd, are connected in series between the load and ground. Assuming ideal components, the average voltage is equal across the capacitors, shown with (2.29) where all capacitor voltages have a value of v_{C_x}. The output voltage is the sum of the *N*+1 capacitor voltages along the lower rail, giving (2.30).

$$v_{C_1} = v_{C_2} = v_{C_3} = v_{C_{2N+1}} = v_{C_x} \tag{2.29}$$

$$v_{out} = v_{C_1} + v_{C_3} + \cdots + v_{C_{2N+1}} = (N+1)v_{C_x} \tag{2.30}$$

Substituting (2.29) and (2.30) into (2.28) then rearranging, an expression for the equivalent capacitance C' is obtained in (2.31). This method of simplifying a circuit for simpler analysis by using a scaling factor is similar to methods use to eliminate transformers to simplify analysis.

$$C' = \frac{2N+1}{(N+1)^2} C \tag{2.31}$$

The value for C'calculated is for the energy stored looking from the switch node to the end of the capacitor ladder and does not include the output capacitor typical in boost converters. Equation (2.32) accounts for the output capacitance by adding it to (2.31) and obtaining *C"*.

$$C'' = \frac{2N+1}{(N+1)^2} C + C_{out} \tag{2.32}$$

Replacing *C* with *C"* in (2.19), the newly formed A_1'' and A_0'' are represented by (2.33) and (2.34) respectively.

$$A_1'' = \begin{bmatrix} -\frac{r_L}{L} & 0 \\ 0 & \frac{1}{(\frac{2N+1}{(N+1)^2}C+C_{out})R_{load}} \end{bmatrix} \tag{2.33}$$

$$A_0'' = \begin{bmatrix} -\frac{r_L}{L} & -\frac{1}{L(N+1)} \\ \frac{1}{(\frac{2N+1}{(N+1)^2}C+C_{out})(N+1)} & -\frac{1}{(\frac{2N+1}{(N+1)^2}C+C_{out})R_{load}} \end{bmatrix} \tag{2.34}$$

Using (2.19), the new A" is expressed in (2.35)

$$A = A_1''\mathrm{d} + A_0''(1-\mathrm{d}) = \begin{bmatrix} -\frac{r_L}{L} & \frac{d-1}{L(N+1)} \\ \frac{1-d}{(\frac{2N+1}{(N+1)^2}C+C_{out})(N+1)} & -\frac{1}{(\frac{2N+1}{(N+1)^2}C+C_{out})R_{load}} \end{bmatrix} \tag{2.35}$$

Equations (2.20) through (2.23) are still used for B, C, $\boldsymbol{x}$, and $\boldsymbol{u}$ as they were not dependent on capacitance.

Matlab was used to plot the output of an N = 4-stage HSCC to compare the results with Spice model. Figure 12 shows the match between Spice and Matlab results with approximately 16% error. Spice simulation results were more detailed capturing more dynamics which had to do with factors such as the state-space model not including diode, capacitor, or switch losses. Nonetheless, this error is higher than expected, but a higher fidelity model is the subject of future work and may improve results.

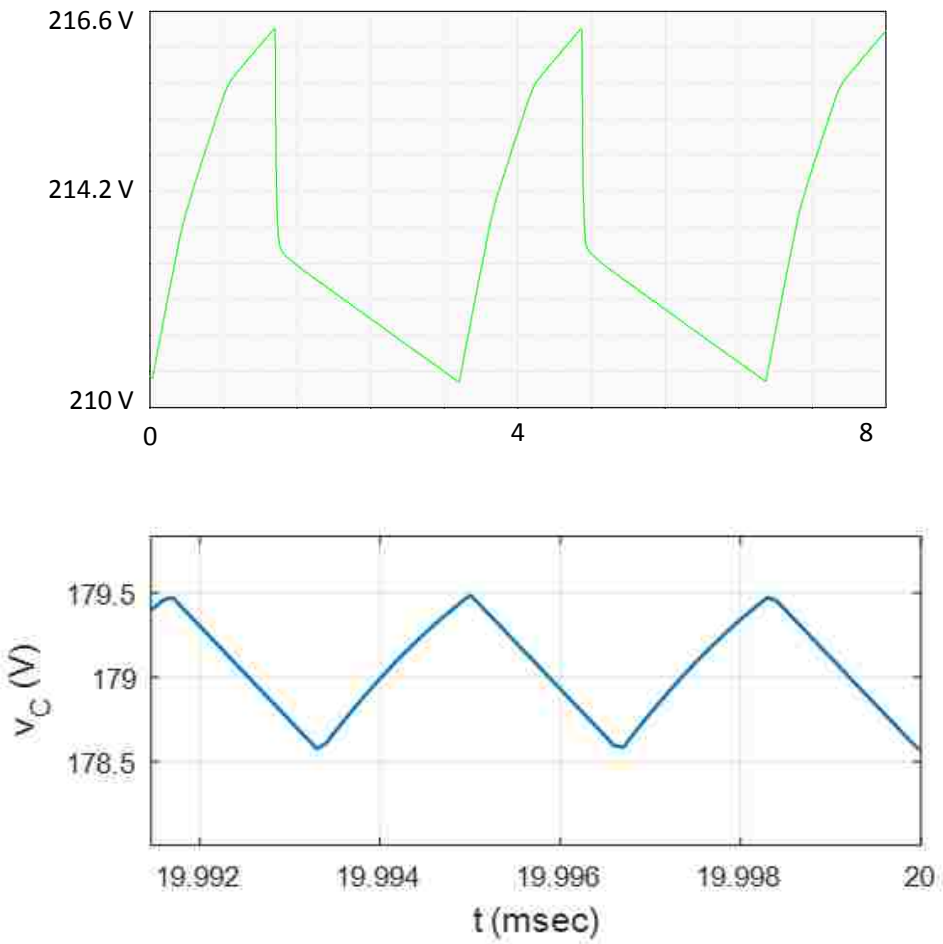

Figure 12: 4-Stage simulated HSCC (top); aggregated input/output behavioral model (bottom)

III. Modeling and Simulation of HSCC Prototypes

This section details the simulation models and results for the two prototypes. First, the 4-stage laboratory-scale HSCC design will be discussed, and the simulation results will be presented. Next, the 8-stage bipolar HSCC model and simulation results will be presented; this is the grid-scale version of what could be expected to support 6 kW at 10 kV distribution. This modified version contains a positive and negative "diode ladder" and two transistor switches. High fidelity simulations were performed to analyze circuit performance taking into account real devices to provide a closer match to actual hardware results that will be discussed in Chapter IV. For model validation, simulations were performed using a resistive load to match hardware experiments discussed in Chapter IV.

A. 4-stage laboratory scale circuit simulation

The 4-stage laboratory scale HSCC was built using a GaN FET, SiC Junction Barrier Schottky (JBS) diodes, and ceramic capacitors. Manufacturer Spice models were used for the FET (GaN Systems GS66508T-E02-MR), diodes (Rohm SCS205KGC), and 1 µF capacitors (Kemet C2220C105KCR2C). Since the capacitors are X7R dielectric multilayer ceramic chips (MLCCs), it is important to use the manufacturers C-V curve to derate their capacitance based on their expected bias voltage accordingly. In this case, Kemet's K-SIM was used. A manufacturer model was obtained for the 22 µH inductor (Vishay Dale IHLP6767GZER220M51) but measured ESR did not match the provided value; therefore, the ESR value was modified to match measured data. The schematic and models can be found in Appendix A and Appendix B respectively. Table 1 lists the parts and component values used in this circuit.

Table 1: Components used for 4-Stage evaluation HSCC

Component	Description	Manufacturer / Part Number
D_1, D_2, …	1.2 kV SiC Diode	Rohm / SCS205KGC
C_1, C_2, …	1 µF MLCC Capacitor	Kemet / C2220C105KCR2C
FET	650 V GaN FET	GaN Systems / GS66508T-E02-MR
Inductor	22 µH, 11 A SMD	Vishay Dale / IHLP6767GZER220M51

Figure 13 shows each capacitor voltage while in steady-state at f_{sw}=300 kHz. Capacitor voltages are well balanced which is important. If voltages are too far out of balance, the effective capacitance of individual stage capacitors will drift apart causing different rise/fall times and lead to the potential of diodes not switching as predicted.

Figure 14 shows the simulated node voltages. The lower rail capacitors are represented by the green, red, pink, and dark green lines starting with C_1 and moving left to C_9. The upper rail capacitors are represented by the gold, blue, teal, grey, and dark blue lines starting with C_2 and moving left to C_8. The upper rail capacitors alternate between the two lower rail capacitors the left and right of it. This happens as the switch alternates the connection of top rail capacitor C_2 between ground and the inductor.

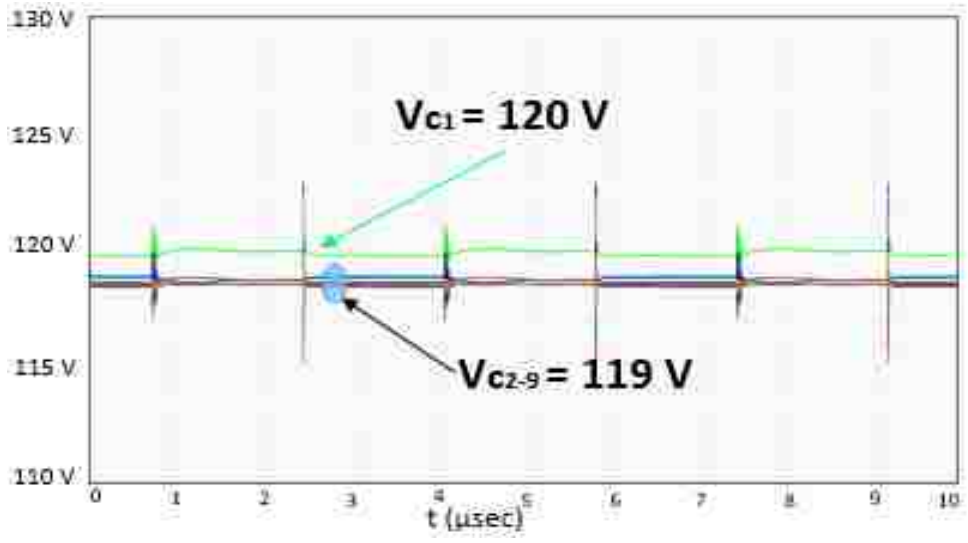

Figure 13: Simulated capacitor voltages

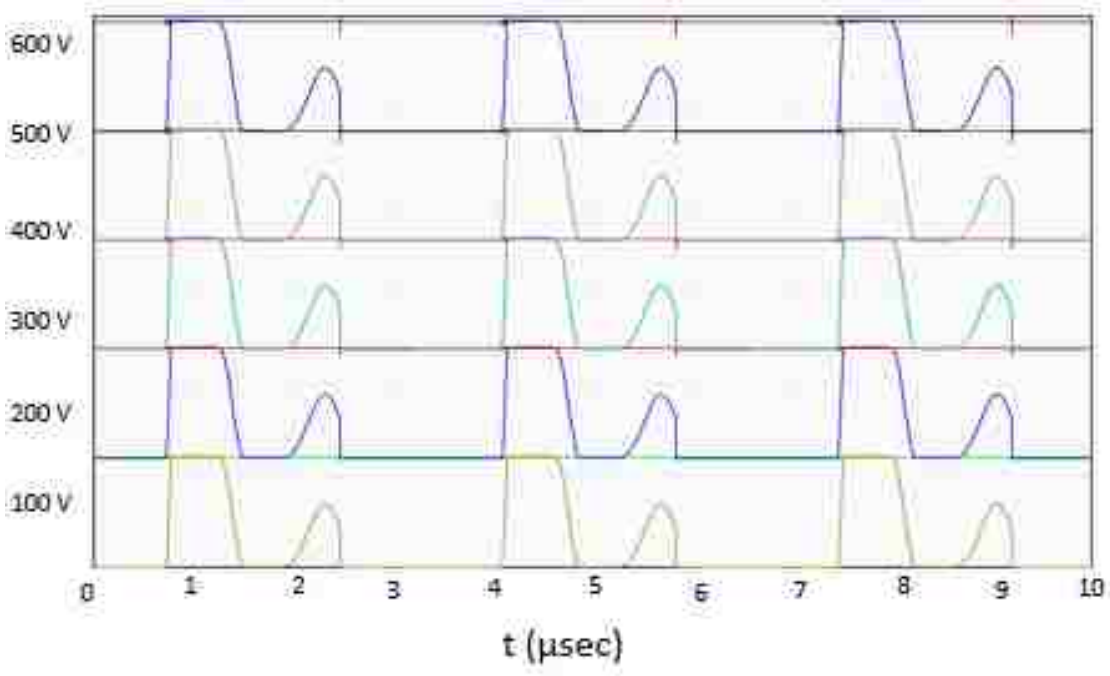

Figure 14: Simulated node voltages

Figure 15 demonstrates the switching nature of the diodes. It shows the diode voltages with the blue representing odd numbered diodes and the red representing even number diodes. As long as capacitor voltages are balanced, all diodes will be subject to equal voltages which is seen as the voltage difference of the capacitors it connects.

Figure 16 is a simulation waveform of the inductor current. Since power density is a key parameter, it is important to understand the performance of the inductor; the inductor will be the largest single item on the board and can greatly impact converter size and weight and thus the power density. The properties for the inductor current were found to be somewhat different from what would be expected for a traditional boost converter. In a traditional boost converter, if the inductor current reaches zero, it enters discontinuous conduction mode (DCM). In this converter, it is possible for there to be negative current (using passive sign convention) due to the capacitors on the top rail. During the negative

conduction mode, capacitor node voltages swing to the potential they would be at with the switch closed causing diodes to also change bias states. Load and frequency parameters determine how long and how often the converter will switch to negative conduction.

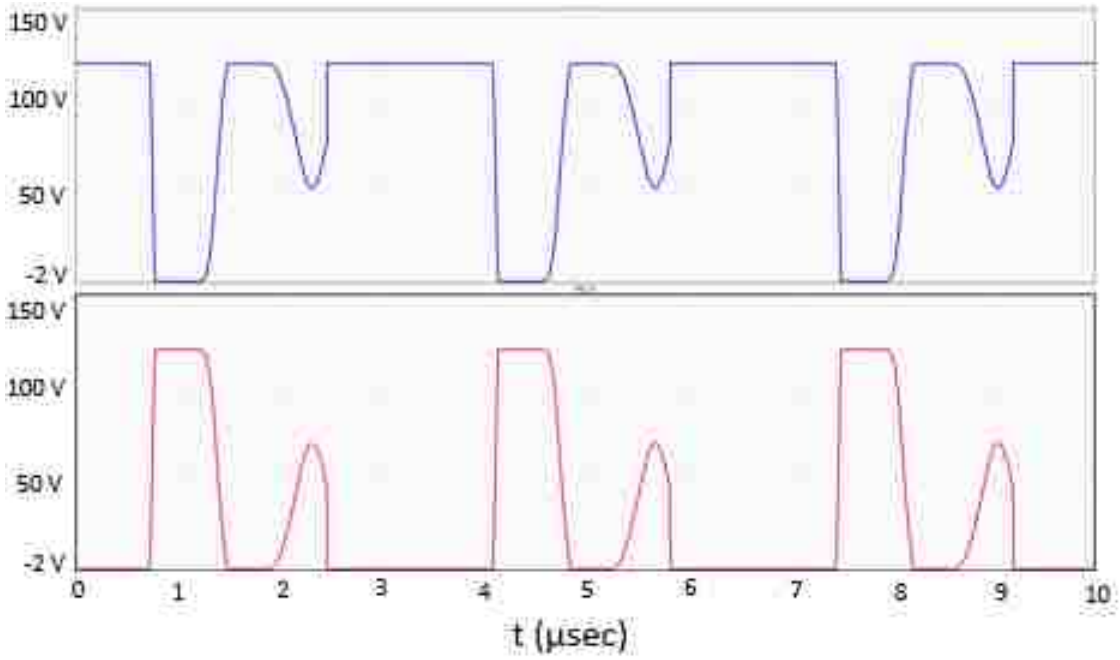

Figure 15: Simulated diode voltages

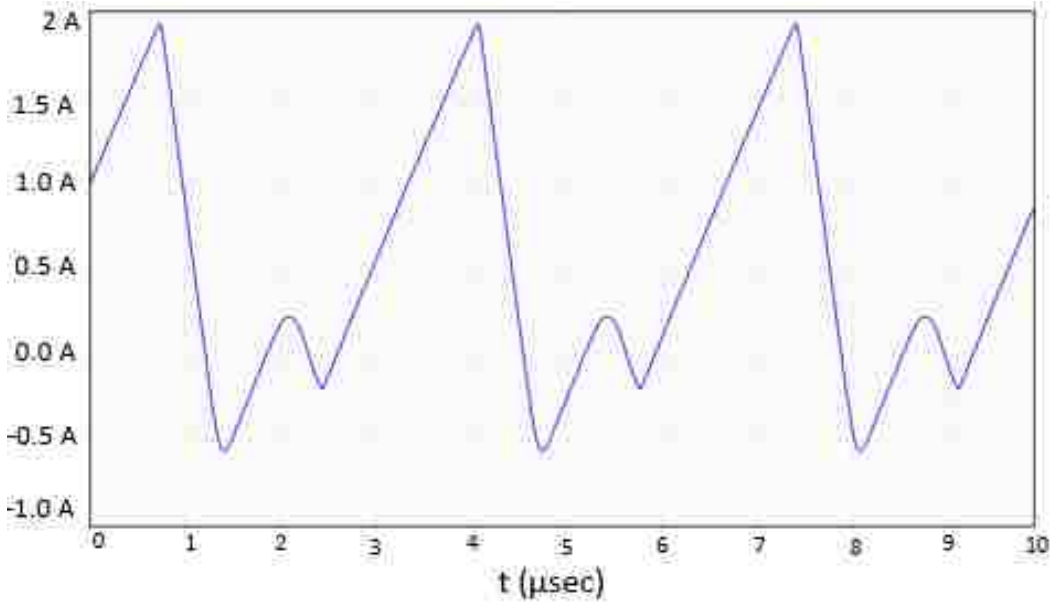

Figure 16: Simulated inductor current

B. 8-Stage full power circuit

It should be noted that the 4-stage converter model discussed in the previous Section B was validated prior to the 8-Stage simulation work discussed here and will be discussed in Chapter V. The model was modified, and these simulation results were used in the design process of an HSCC intended to operate at 10 kV and 6 kW.

To demonstrate the intended operation, simulation results are presented for a circuit with N = 8 stages. Although theoretically a 4-Stage HSCC could boost a 600 V input to 10 kV with a 70% duty cycle, component voltages would experience excess of 2.5 kV which is beyond the limits of commercial WBG devices under investigation. Diode and switch voltage ratings are the most sensitive in this application as their maximum rating is 1700 V compared to the 2000 V rating of the MLCC capacitors selected. To keep maximum component voltages at approximately 75 percent of rated (1250 V), an 8-stage HSCC was selected for the design and modeled. It was found that as additional stages are added beyond N=5-6, stage voltages become unbalanced, causing higher voltages toward the switch and tapering off nonlinearly moving toward the load.

To reduce component voltage stress, a modification to the HSCC layout previously discussed was implemented by adding a negative counterpart. This modified circuit will be referred to as a *bipolar HSCC*. The bipolar HSCC is configured by adding an additional diode-capacitor ladder that has opposite polarity and diodes flipped with anode on the right and cathode on the left. Diodes on the "bottom circuit" are oriented in the opposite direction compared to the top to allow current flow through the top half of the circuit, through the load, and back through the lower half [22]. This allows each diode-capacitor ladder to effectively see 5 kV and remain balanced as each diode-capacitor ladder will only have 4

stages (8 stages total). Figure 17 illustrates the topology of the bipolar circuit; due to space constraints, the circuit is shown with only 4 stages (as opposed to 8) for image clarity. The LTspice screenshot is available in Appendix C.

Manufacturer Spice models were used when possible to obtain the most accurate results. The positive and negative side of the circuit each used a single SiC FET (Wolfspeed C2M0045170D). SiC JBS diodes were also selected (Wolfspeed C3D10170H). Power inductors (West Coast Magnetics 320-04) rated at 57.8 µH and 32 A were necessary because of the large input current. For improved energy density, 0.1 µF X7R MLCC capacitors were used (Knowles 2220Y2K00104-KXTWS2). Table 2 summarizes the key components used for the bipolar HSCC prototype. Since the capacitors have X7R dielectric, individual stage voltages were obtained from simulation, and a C-V plot obtained from the manufacturer was used to iteratively adjust each stage's capacitance in the model accordingly; see Figure 18 for C-V plot. Since the circuit's inductance and capacitance values were low, resistance and reactance of the supply cable coming from the power supply were also included in this model. The full schematic is in Appendix C

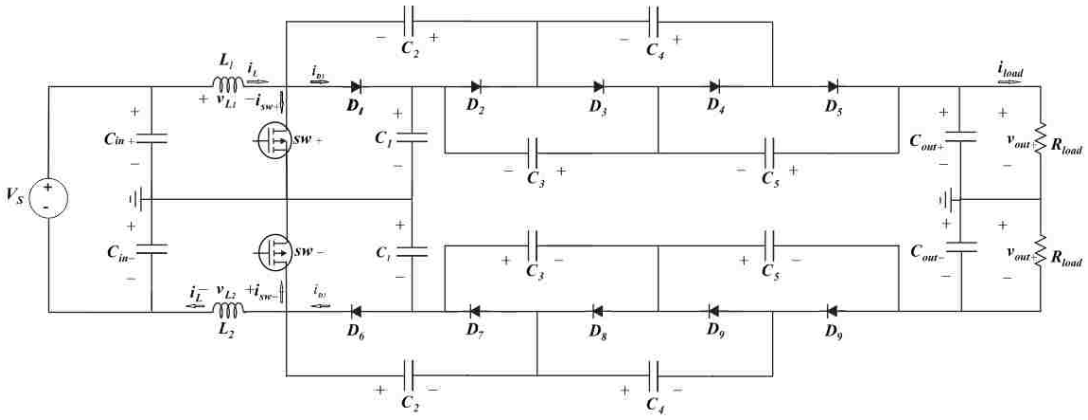

Figure 17: 4-Stage bipolar HSCC schematic

Table 2: Key components used in bipolar HSCC prototype

Component	Description	Manufacturer / Part Number
D_1, D_2, …	SiC Diode, 1.7 kV	Wolfspeed, C3D10170H
MLCC, 0.1 µF, 2 kV	Knowles	2220Y2K00104KXTWS2
SiC FET, 1.7 kV	Wolfspeed	C2M0045170D
Inductor, 58.8 µH, 32 A	West Coast Magnetics	320-04
Gate driver board	Wolfspeed	CRD-001

*These numbers include the 7-stage diode-capacitor ladder. Practical designs will likely require fewer stages and thus fewer diodes and capacitors.

Figure 18: C-V plot for Knowles 2220Y2K00140*XTWS2

Once the circuit was operational, the power levels were selected to validate hardware results and will be discussed in Chapter V. Figure 19 shows the simulated output voltage at one of the power levels. It is shown as +/- 5,045 V effectively giving a 10.09 kV

output with 600 V input and 46% duty cycle. The voltage ripple was 452 V pk-pk on each pole (9.1%). The inductor current is shown in Figure 20. Based on the loading and switching frequency of 145 kHz, similar characteristics are seen in the 8-Stage bipolar as the lower-power 4-Stage unipolar discussed in the previous section. Two switching schemes were possible; synchronous or complimentary. Simulations were performed to determine which method provided better results. Synchronous showed to be the simplest, because both gates can be triggered from a single signal. It also provided a higher overall gain in simulation, but the reason for this was not investigated extensively.

It is noted that in practice, these converters would be connected to a MVDC bus, and the MVDC bus would dictate the output voltage of the converter. The input voltage would be set by controlling the current from a PV array using a maximum power point tracking (MPPT) algorithm. To obtain performance parameters under these conditions, the resistive load could be replaced with an equivalent Thévenin source. However, the means

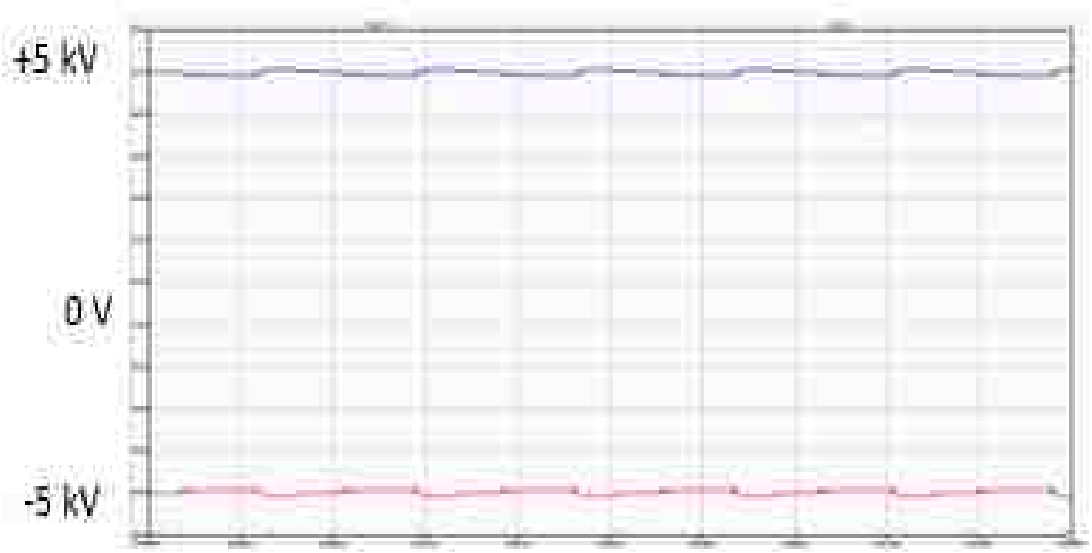

Figure 19: Simulated output voltage; Input voltage =600 V, *D*=46%, *f*=145 kHz

to test this configuration in hardware were not available; so, simulation and hardware evaluation was done using a resistive load.

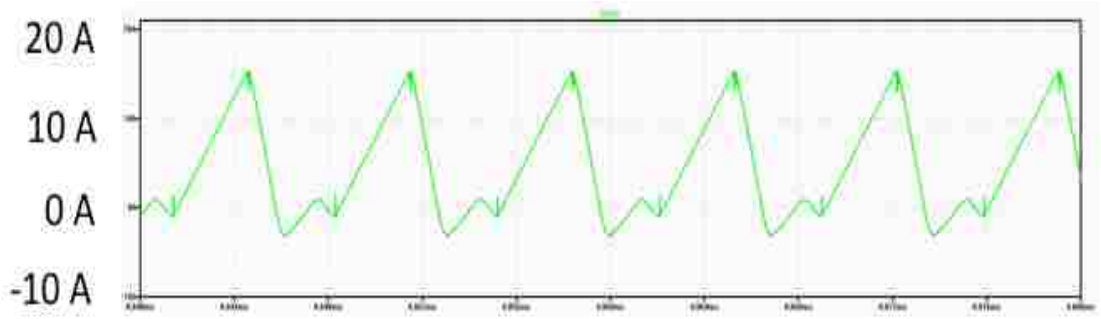

Figure 20: Simulated input inductor current; Input voltage =600 V, *D*=46%, *f*=145 kHz

IV. Hardware Validation of Evaluation Circuit

A 4-stage HSCC bench-scale prototype was designed and built to evaluate HSCC operation and allow hardware validation of simulation models. Working from the validated models, a grid-scale 10 kV 6 kW prototype was designed based on simulation results. This section discusses the hardware results for the evaluation circuit. Chapter V describes the grid-scale prototype construction and evaluation.

A. Evaluation Circuit Hardware Results

The first prototype was an attempt to investigate HSCC operation and to validate the HSCC simulation models. With it being a lower power and voltage, a GaN FET (GaN Systems GS66508T-E02-MR) was used to add the flexibility of higher frequency testing at the lower voltage levels; see Figure 21. A fixed duty cycle was supplied through an auxiliary port using an Agilent 3220A function generator. The board was laid in a configuration so that D_1 started at the input switch node and went in a straight line to D_9. Top and bottom rail capacitors were placed physically next to each other in an alternating pattern. The board connected using screw lugs to power resistors which could be connected as either 50Ω or 25Ω, by using 50Ω resistors in a single or parallel configuration. The input voltage was supplied using a BK Precision 1735A 30V/3A power supply. RMS input and output voltage and current was measured using Fluke 289, 87, 87 IV True RMS multimeters. All node voltages were recorded using Tektronix P5250A differential voltage probes and a Tektronix TDS 3014C oscilloscope. No input capacitor was added so that inductor current could be measured as the supply current. The inductor current was measured using a Tektronix TCP2020 2A RMS current clamp. Attempts were made to

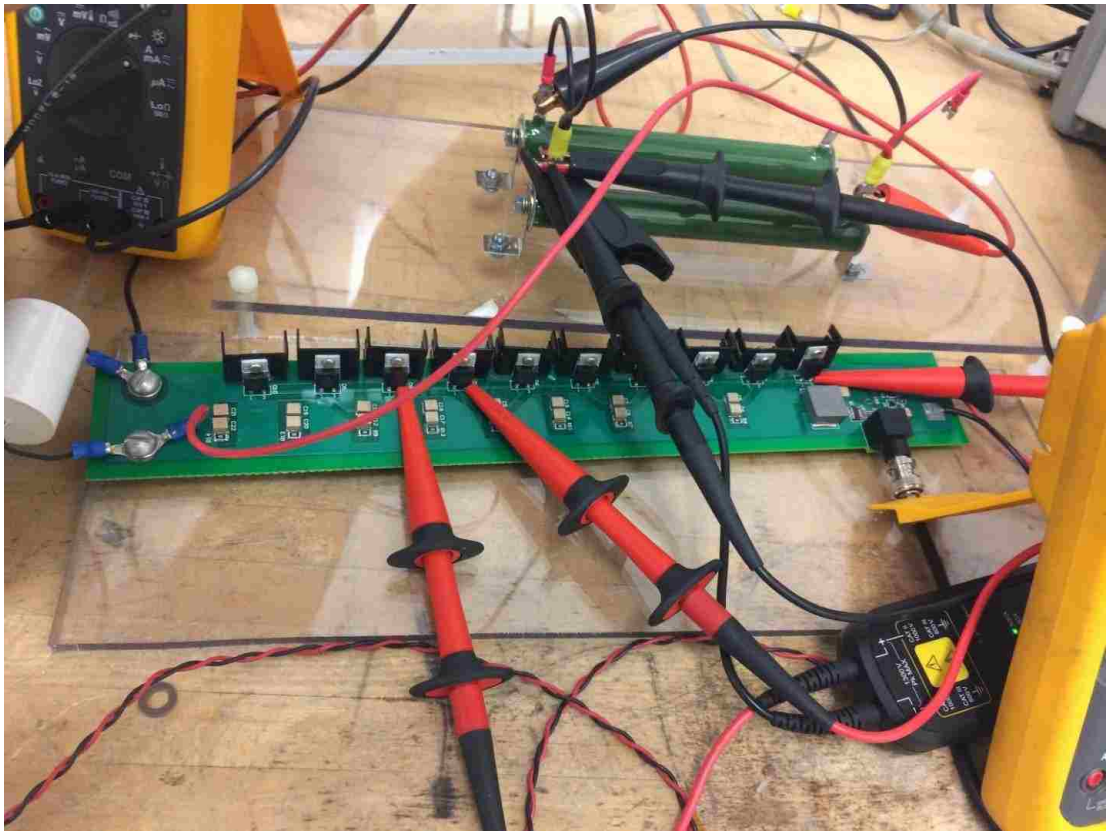

Figure 21: 4-Stage HSCC Evaluation Board

measure individual diode currents using a Rogowski coil, but due to the low current levels, there was a low signal to noise ratio which made the data unusable.

Figure 22 shows each individual capacitor voltage for 10 µs. The plot shows that even over multiple switching transitions, during steady-state, the individual capacitors are well balanced. This is important to ensuring diodes switch as predicted. Figure 23 shows each node voltage from the switch to the output. The initial boost converter stage had a gain of approximately 4.13. This gain was multiplied by (N+1) where N=4 for a total gain

of approximately 20.66. The odd numbered capacitors hold a relatively fixed voltage with respect to ground whereas the even numbered capacitors swing between node voltages.

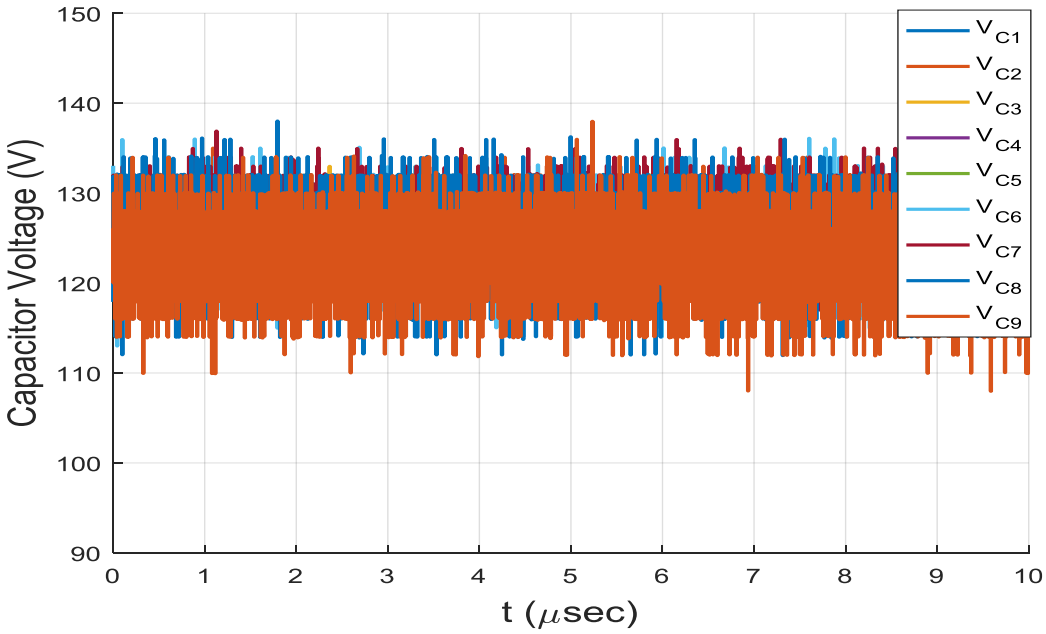

Figure 22: 4-Stage HSCC Evaluation Board measured capacitor voltages

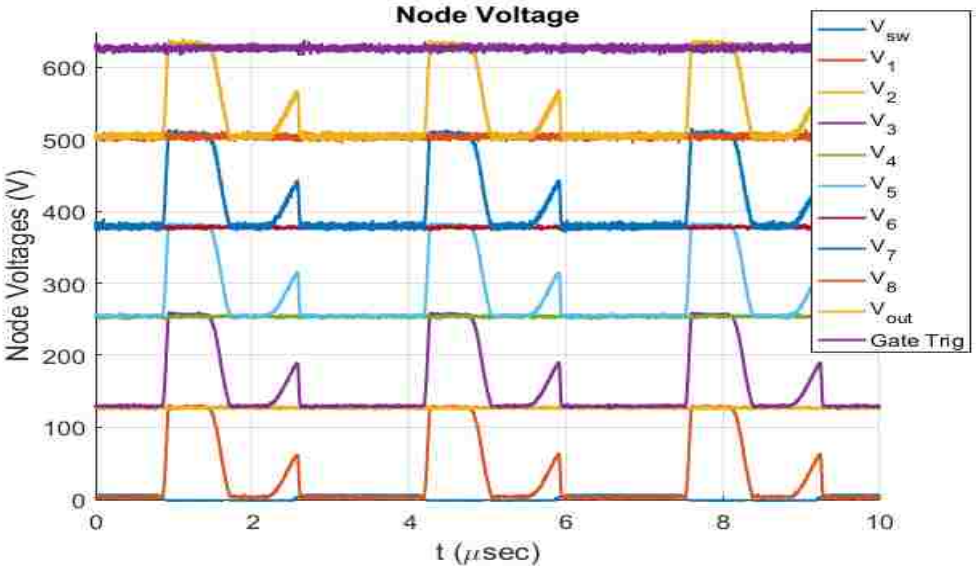

Figure 23: 4-Stage HSCC Evaluation Board measured node voltages

When the switch is ‘on’ the top rail capacitor is at the voltage of the bottom rail capacitor to its left (closer to the switch) with respect to ground. When the switch is ‘off’, the same capacitor is at the voltage of the lower rail capacitor to its right (closer to the load) with respect to ground.

Figure 24 through Figure 27 show the output voltage vs frequency, output power vs frequency, gain vs frequency, and efficiency vs frequency respectively. A constant input voltage of 30 V was supplied and the duty cycle was kept constant at 50%. The highest output power corresponded to the highest output voltage and gain; however, the efficiency was near its low at 85%. A peak efficiency of 88.1% was found at 550 kHz which was near the lowest gain; approximately 14 compared to 23. The increase in frequency may be explained by the inductor current. While increasing the frequency, there is less negative current conduction to a certain point. This is due to the reduction in the inductor ripple current which is a similar principle with a traditional boost converter; increasing the frequency provides a smaller inductor current because it doesn’t have as much time to rise or decay. The peak and minimum is closer to the average.

Figure 28 compares the effects of input voltage on duty cycle while maintaining a voltage of 550 V at 300 kHz. The frequency was chosen as an anchor point because it provided the most power. The same parameters were varied for a 25 kΩ and 50 kΩ resistive load to determine if loading affected the circuits operation. For the 25 kΩ load, the duty cycle decreased at a near linear rate of less than 1% between input voltages ranging from 25 to 30 in 1 V increments. The duty cycle using a 50 kΩ load decreased slightly more rapidly non-linearly with the largest drop of 10% going from 27 V to 28 V. The gain is

compared for both loads in Figure 29. As expected, the gain decreased for both as input voltage increased because the output voltage was kept constant.

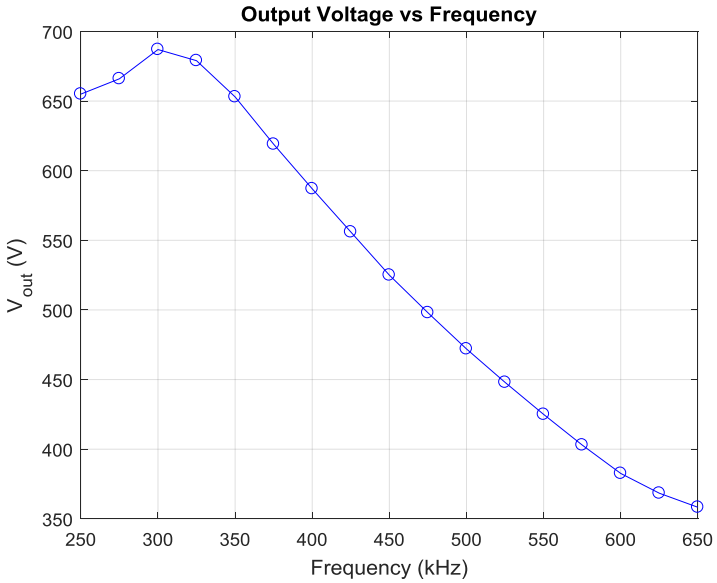

Figure 24: 4-Stage HSCC Evaluation Board test results: Output voltage vs frequency

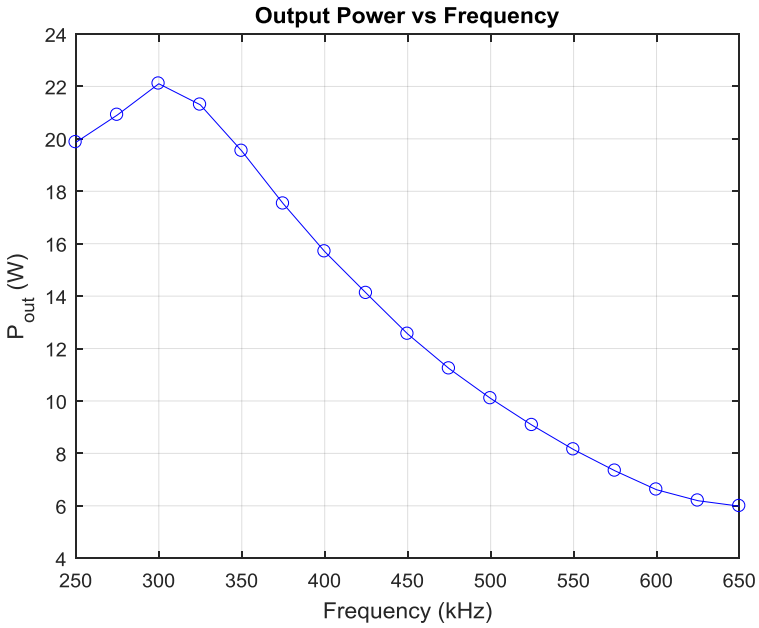

Figure 25: 4-Stage HSCC Evaluation Board test results: Output power vs frequency

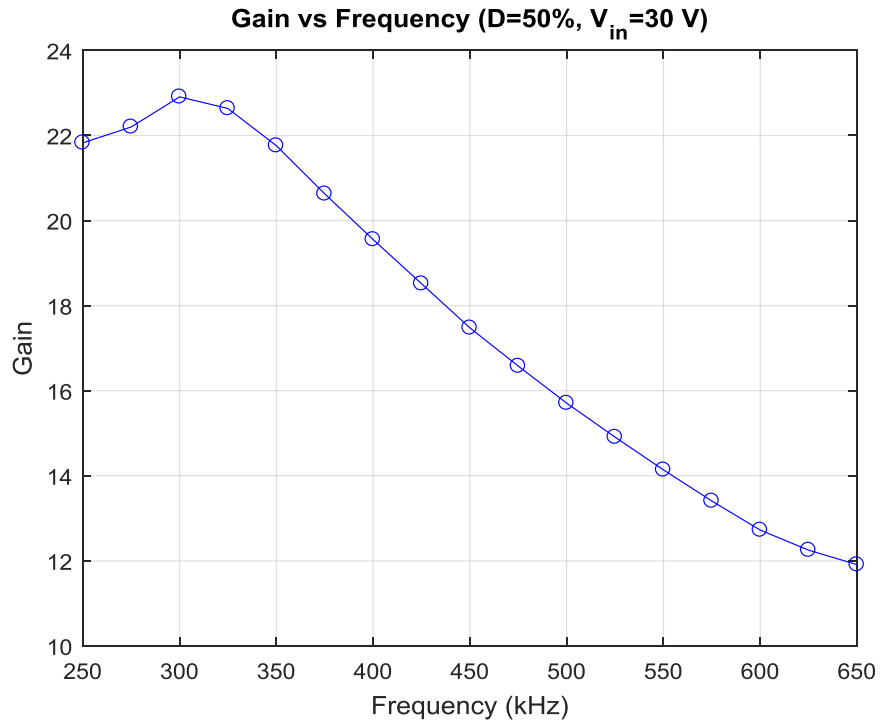

Figure 26: 4-Stage HSCC Evaluation Board test results: Gain vs frequency

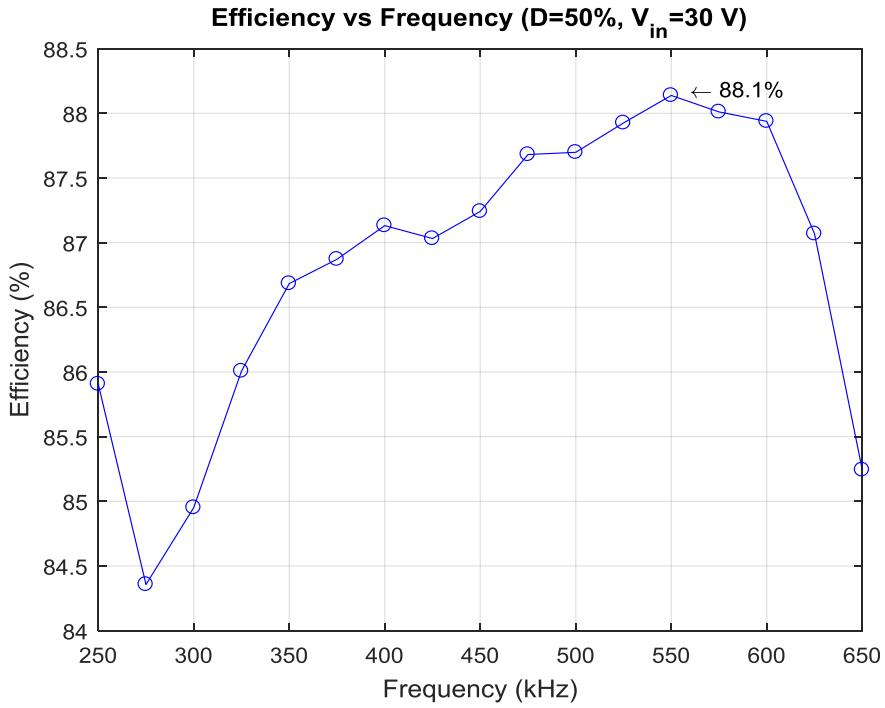

Figure 27: 4-Stage HSCC Evaluation Board test results: Efficiency vs switching frequency

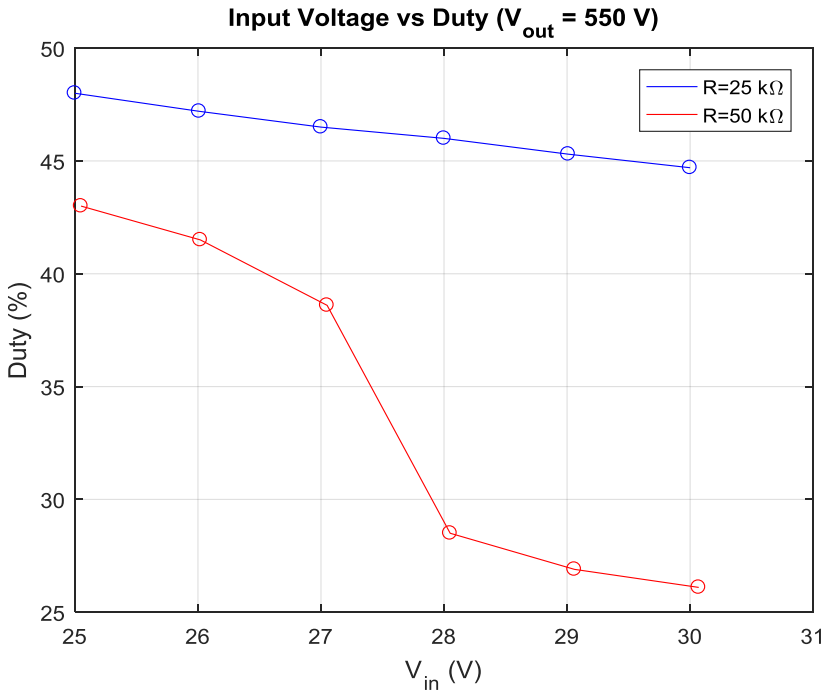

Figure 28: 4-Stage HSCC Evaluation Board test results: Duty Cycle vs input voltage

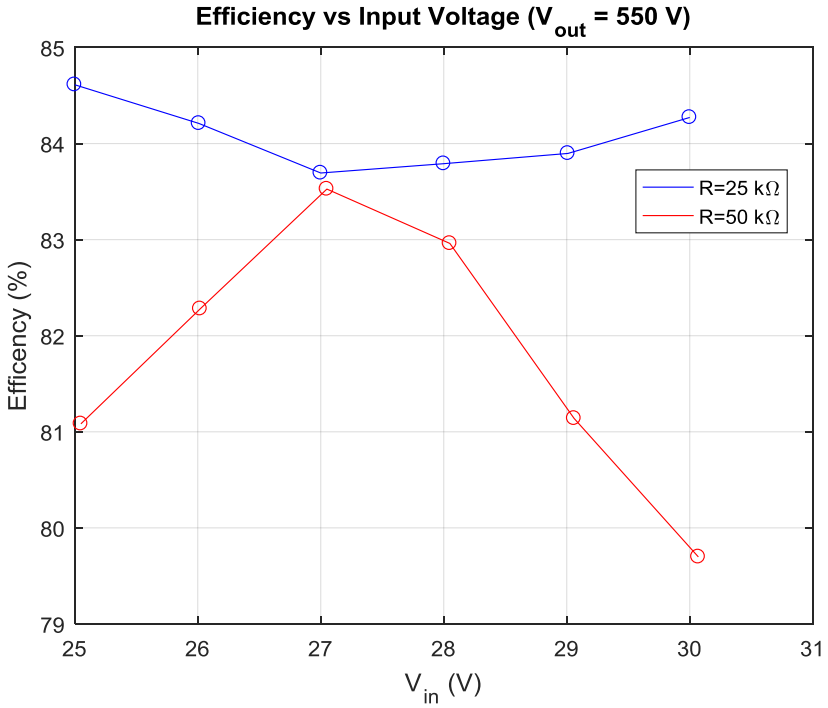

Figure 29: 4-Stage HSCC Evaluation Board test results: Efficiency vs input voltage

V. Bipolar HSCC Hardware Design and Testing Results

An 8-Stage bipolar HSCC was designed based on results found from the unipolar 4-stage HSCC. This chapter will review the design strategy and present the measured hardware results for the grid-scale prototype.

A. Bipolar HSCC Hardware Design

A prototype of the bipolar HSCC circuit was designed to operate up to 10 kV output voltage and 6 kW output power. The constructed prototype is shown in Figure 30. The inductors were sized to allow testing over a range of switching frequencies, as low as 100 kHz. The switching signal can be controlled with an open-loop PWM signal or hysteresis current control. Although hysteresis current control is more commonly used for DC-AC inverters, it is being explored as a means to directly control the input current (and thus the input power) of the HSCC. The board can be operated as a bipolar or unipolar HSCC. SiC FETS were used which have a recommend gate voltage of +24/-5 V. Each gate used a

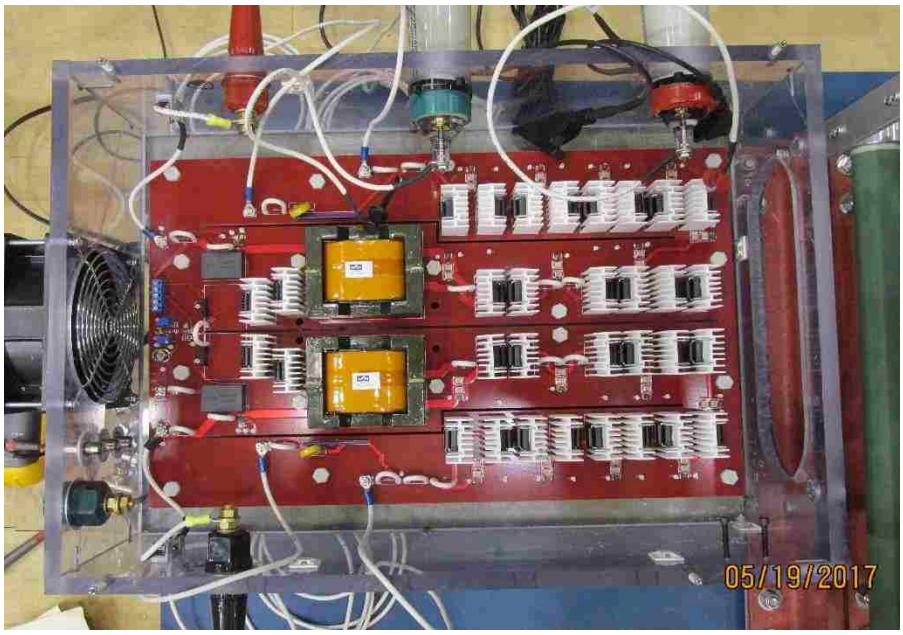

Figure 30: 6 kW 10 kV bipolar HSCC prototype

premade gate driver (Wolfspeed CRD-001). The negative polarity HSCC has an isolated source for the driver. Both gates are driven from the same signal.

A custom high-voltage resistive load, that was adjustable up to 10 kΩ, 10 kW (at 10 kV) was used for testing. High-voltage isolation and heat dissipation were important safety considerations for the design and construction of the test bed. The entire test bed was placed inside an interlocked box for protection of personnel.

For flexibility with testing, 7 stages were added to the positive side and 7 stages to the negative. Stages could easily be eliminated to allow operation with fewer stages by adding jumpers across stages. In addition, the inductors were deliberately oversized to allow a wider range of switching frequencies (down to 100 kHz). Following the preliminary phase of testing, 4 stages were selected for each pole of the converter (8 stages total), and the converter was operated at 145 kHz. These operating parameters appeared to provide the best efficiency over a wide range of operating conditions.

B. Bipolar HSCC Hardware Testing Results

The input to the bipolar HSCC prototype was connected to an Ametek / Sorenson SGI 600/8 power supply, and the output was connected to the high voltage resistor bank. Since the resistance value of the load drifted with temperature, these values were measured at the time of the experiment. For example, at a nominal 50 kΩ setting, the resistance would drift down to 44.4-47.3 kΩ. Data was collected at multiple load levels; 47.3 kΩ, 45.7 kΩ, 44.4 kΩ, 39.3 kΩ, 23.8 kΩ, 22.7 kΩ, and 16 kΩ. The RMS input and output voltages and currents were measured using Fluke digital multi-meters, and several signals were monitored by a Tektronix TDS 3054C oscilloscope. The supply was configured to supply the prototype with +/- 300V input. Measurements were taken with varying input voltage

Table 3: 8-Stage bipolar HSCC performance measurements

Operating Conditions		Hardware Results			
Input Voltage (V)	Duty cycle (*D*)	Output Voltage (V)	Output Power (W)	Efficiency (%)	Gain
330.1	0.33	5017	532	96.55	15.2
330.2	0.59	5006	1051	96.30	15.2
330.1	0.72	5004	1569	94.13	15.2
440.4	0.34	6678	975	95.88	15.2
440.2	0.66	6663	1952	95.56	15.1
530.5	0.35	8000	1440	94.98	15.1
600.1	0.46	10055	2574	95.32	16.8

and duty cycle to determine output power and other performance results that could be used to validate the simulated circuit model.

Table 3 lists measured output voltage, output power, gain, and efficiency for various input voltages and duty cycles. At each input voltage, the output voltage was held constant at that level. Duty cycle was varied to increase output power. For both voltage levels, gain stayed constant only fluctuating between 15.1 and 15.2; however, efficiency tends to decrease with increased duty cycle.

Approximately 43% of rated power was achieved with a duty cycle of $D = 0.46$. The circuit was allowed to "warm up" and reach steady-state before measurements were taken. In steady state, the RMS output voltages summed to 10.055 kV at 2.574 kW delivered to the load.

Table 3 also shows the positive and negative pole voltages. Therein, the output voltage is seen to be effectively +/-5 kV. The voltage ripple on each pole was measured to

be 477 Volts pk-pk average (9.5%). This can be mitigated with the addition of more capacitance. The average input current is 4.3 A. On the rising edge, the input current is consistent with what would be expected from a conventional boost converter. On the falling edge, the current is seen to go slightly negative. This is due to the added dynamics of the connection of the switch node to capacitor C_2; see Figure 32

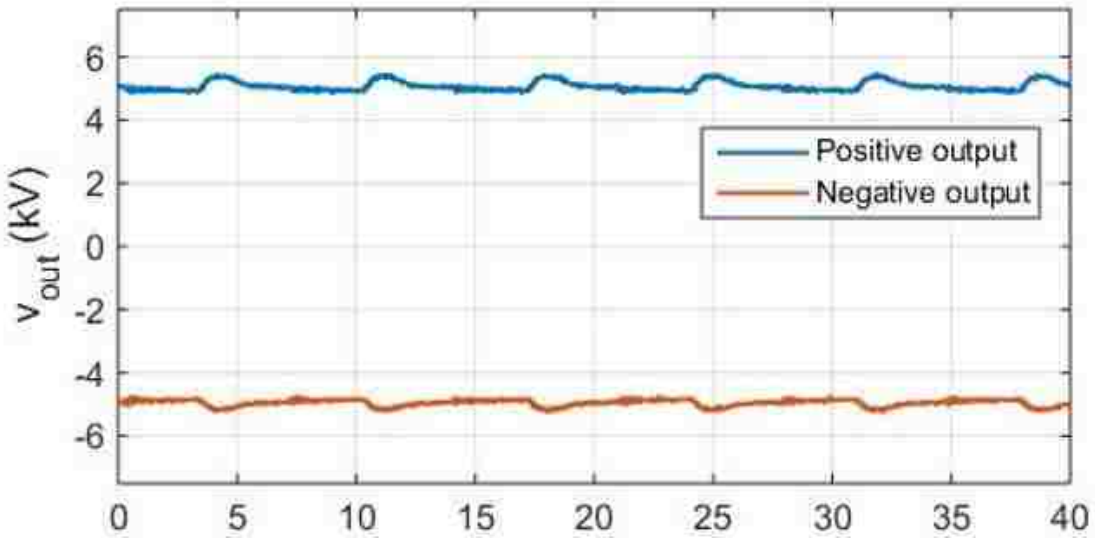

Figure 31: Output voltage of 8-Stage bipolar HSCC; 600 V input, *D*=46%, time in µs

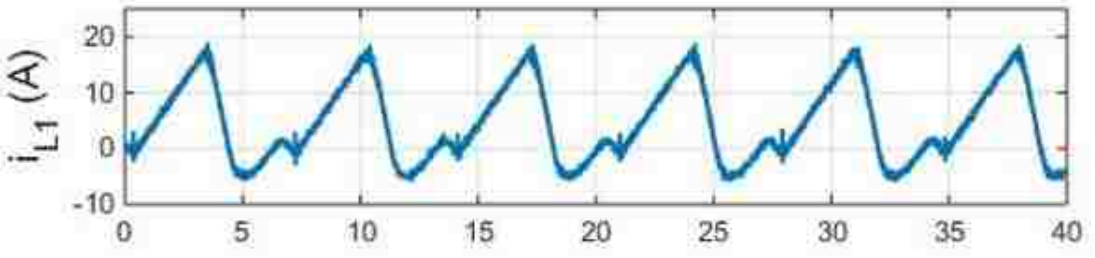

Figure 32: Inductor input current of 8-Stage bipolar HSCC; 600 V input, *D*=46%, time in µs

VI. 8-Stage HSCC Hardware and Simulation Comparison & CEC Efficiency

A benefit to having a valid circuit model for simulation is the ability to gain reliable results that you cannot test in hardware due to limiting factors. Since CEC efficiency requires operation at various input voltage and load settings not available in the lab, simulations were relied upon for this computation. The 8-stage bipolar HSCC was validated in a similar manner to the 4-Stage unipolar but achieved greater accuracy due to accounting for source impedance and both diode and FET temperature variations. This chapter will compare hardware and simulation results and discuss the method for computing the converter's equivalent CEC efficiency.

Operating parameters such as input voltage, duty cycle, and load were originally obtained from hardware testing. Data was recorded for multiple operating points. The HSCC circuit model results were compared for these same operating points tuned to give a well fit model. Table 4 shows a comparison of hardware and simulation results. The average difference between measured and predicted efficiency was approximately 1.2%.

Table 4: Experimental and Simulation Results for Converter supplying a Resistive load

Operating Conditions		Hardware Results				Simulation Results			
Input Voltage (V)	Duty Cycle (*D*)	Output Voltage (V)	Output Power (W)	Efficiency (%)	Gain	Output Voltage (V)	Output Power (W)	Efficiency (%)	Gain
330.1	0.33	5017	532	96.55	15.2	5115	553	95.10	15.5
330.2	0.59	5006	1051	96.30	15.2	5020	1058	94.53	15.2
330.1	0.72	5004	1569	94.13	15.2	4996	1566	92.43	15.1
440.4	0.34	6678	975	95.88	15.2	6708	984	95.35	15.2
440.2	0.66	6663	1952	95.56	15.1	6747	2002	94.11	15.3
530.5	0.35	8000	1440	94.98	15.1	7912	1408	95.43	14.9
600.1	0.46	10055	2574	95.32	16.8	10089	2592	93.13	16.8

The difference in measured and predicted gain was less than 0.5% showing a good fit. For most cases, the simulation efficiency was slightly below actual hardware results. Since efficiency is a key metric, this is preferred rather than simulation efficiency being higher. It would be preferable to overdesign and get a higher efficiency in hardware when testing than what was originally expected.

Converters do not perform with the same efficiency under different conditions. Factors such as loading and gain can largely affect the efficiency. For this reason, the CEC has adopted a set of test procedures for manufacturers to perform before granting the ability to connect inverters to solar systems in California. CEC inverters rated for 6 kW are typically in the range of 96-97% [23]. Although the HSCC is a DC-DC converter, not an AC-DC inverter, a modified set of test procedures was used to get a CEC equivalent efficiency for this DC-DC converter. It is expected that a similar set of test procedures would be adopted for DC-DC converters with their future use on a DC power grid.

The CEC test procedure requires testing at 6 power levels for 3 voltage levels. The weightings factors are 0.04, 0.05, 0.12, 0.21, 0.53, and 0.05 for the power levels 10%, 20%, 30%, 50%, 75%, and 100% respectively [24]. This must be done for three voltage levels, V_{NOM}, V_{MAX}, and V_{MIN}, then averaged. V_{MAX} and V_{MIN} account for the change in PV cell operating points based on seasonal variations. For this study, the assumption was made that testing would be done in Albuquerque, NM at Sandia National Laboratories Distributed Energy Technologies Laboratory (DETL) where the ability exists to connect to an actual 1 kV 6 kW PV array using SolarWorld 175 panels. Nominal operating specifications were obtained from the SolarWorld 175 datasheet [25] and was derated based on data provided therein based on Albuquerque's maximum and minimum recorded temperatures found on

www.weather.gov. Equation (5.1) is used to find the CEC efficiency. Simulation results are listed in Table 5, which also provides a final expected CEC efficiency of 93.8%.

$$\eta_{Wtd} = F_1\eta_{10} + F_2\eta_{20} + F_3\eta_{30} + F_4\eta_{50} + F_5\eta_{75} + F_6\eta_{100} \quad (5.1)$$

Table 5: Simulated CEC efficiency results

Weighting (left) for power out (right) at 10 kV out		Efficiency at V_s = 734 V	Efficiency at V_s = 794 V	Efficiency at V_s = 910 V
0.04	10 %	94.65	92.33	85.80
0.05	20 %	92.69	92.19	94.80
0.12	30 %	94.68	95.91	93.64
0.21	50 %	93.37	95.07	94.26
0.53	75 %	93.92	94.26	93.84
0.05	100 %	85.70	89.07	93.43
Weighted average		93.45	94.19	93.61
CEC efficiency 93.8%				

VII. Conclusions and Future Work

Power electronics are advancing rapidly, enabling new applications and new areas of research, especially with respect to power generation, distribution, and transmission. The DOE and other institutions are interested in the possibility of new architectures arising, including the possibility of a DC distribution network. This work presents a hybrid switched capacitor circuit (HSCC) which uses WBG devices. The HSCC is a DC-DC boost converter topology that allows higher gains than in classical DC-DC boost converters. The HSCC can be realized in a compact circuit using a diode-capacitor ladder. By using WBG devices, the circuit is capable of high-frequency switching, which allows the input inductor and capacitors to be reduced in size. In addition, the heavy reliance of this circuit on diodes makes it a potential early adoption strategy for high voltage GaN diodes and potentially even UWBG diodes.

In this work, the HSCC operation was described analytically and through Spice simulation. A low-power bench-scale prototype was built and tested to gain an understanding of key operating principles, to validate Spice models, and to set the foundation for a grid-scale 6 kW, 10 kV prototype. Both prototypes were modeled in Spice, and the models were validated against hardware experiments with approximately 1% error or less for input current, output voltage and gain. Conversion efficiency for the bipolar HSCC was within 1.2% when comparing hardware and simulation. A key metric for this converter, in addition to power density, is efficiency. The grid-scale converter was demonstrated in hardware to deliver 2.56 kW at 10 kV DC to a resistive load with greater than 95% efficiency. In addition, a modified CEC efficiency test protocol was chosen in which the converter was evaluated in simulation at a nominal, maximum, and minimum

PV array operating voltage, based on Albuquerque, NM conditions, to determine a weighted efficiency of 93.8%. These results indicate a strong potential for this converter for use in grid-scale applications.

Future work should focus on improvements to converter efficiency and power density. Eliminating the unused stages in subsequent prototypes will certainly reduce size. It is also noted that the prototype was oversized to allow for sufficient test points for data collection. The inductors were also deliberately oversized to allow a wider range of switching frequencies during the circuit performance analysis phase. Reduction of board size will remove unnecessary jumpers, eliminate unnecessary stages, and reduce trace losses. A more deliberate selection of the input inductor will reduce size and may also save in power losses. In short, the next prototype iteration should yield considerable improvement in power density.

In addition, there are several techniques that are known to increase efficiency from the reduction in switching losses such as zero-current switching (ZVS) or zero-current switching (ZCS). Employing these approaches in this circuit would be more difficult however, due to the circuit complexity.

Finally, the operation of the circuit connected to an MVDC line may introduce new dynamical complexities, requiring changes to the converter design and/or new controls approaches. This too should be investigated for future work.

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Appendix A

Device Spice Models

Capacitor: 1 µF Kemet C2220C105KCR2C

```
.SUBCKT C2220C105KCR2C 1 6
*Temp@ 30°C, Bias@ 125Vdc , Center Freq@ 316.228 kHz
* KEMET Model RLC Cerm
L1 1 2 95.90E-12
L2 2 3 1.82E-09
R1 3 4 9.90E-03
C1 4 6 772.41E-09
R2 2 5 419.40E-03
C2 5 6 25.00E-12
R3 1 6 201.30E+06
.ENDS
```

Inductor: 22 µH Vishay IHLP-6767GZ-51

```
.SUBCKT IHLPF6767GZ51
L1 N001 N003 22µ Rser=0
R1 N002 N003 .315
C1 N002 N001 38p Rser=0 Lser=0 Rpar=0 Cpar=0
R2 N004 N002 .315
.end
```

SiC Diode: Rohm Schottkey Barier Diode SCS205KG

```
* SCS205KG
* SiC Schottky Barrier Diode model
* 1200V 5A
* Model Generated by ROHM
* All Rights Reserved
* Commercial Use or Resale Restricted
* Date: 2015/11/16
*****************A C
.SUBCKT SCS205KG 1 2
.PARAM T0=25
.FUNC R1(I) {40.48m*I*EXP((TEMP-T0)/155.8)}
.FUNC I1(V) {2.102f*(EXP(V/0.02760/EXP((TEMP-T0)/405.3))-
1)*
+            EXP((TEMP-T0)/7.850*EXP((TEMP-T0)/-601.3))}
.FUNC I2(V) {TANH(V/0.1)*(710.4p*EXP(-V/198.3)*EXP((TEMP-
T0)/54.40)+
```

```
+            26.02f*EXP(-V/63.22/EXP((TEMP-T0)/178.9))*
+            EXP((TEMP-T0)/8.493*EXP((TEMP-T0)/-600)))}
V1 1 3 0
E1 3 4 VALUE={R1(MIN(MAX(I(V1)/0.5,-500k),500k))}
V2 4 5 0
C1 5 2 0.5p
G1 4 2 VALUE={0.5*(I1(MIN(MAX(V(4,2),-
5k),5))+I2(MIN(MAX(V(4,2),-5k),5)))+
+             I(V2)*(913.9*(MAX(V(4,2),0.5607)-0.5607)+
+             727.2*(1-
360.9*TANH(MIN(V(4,2),0.5607)/360.9)/1.121)**-0.4987)}
R1 4 2 1T
.ENDS SCS205KG
```

SiC FET: GaN Systems 650 V E-HEMPT GS66506T

```
* Created in LTspice Version 4.13h
*
*
          *
* GaN Systems Inc. Power Transistors
*
* LTSpice Library for GaN Transistors
*
* Version 1.27
*
*
*
************************************************************
******
************************************************************
******
*
*
* Models provided by GaN Systems Inc. are not warranted by
*
* GaN Systems Inc. as
*
* fully representing all of the specifications and
operating    *
* characteristics of the semiconductor product to which the
*
* model relates. The model describe the characteristics of
a    *
* typical device.
*
```

```
* In all cases, the current data sheet information for a
given  *
* device is the final design guideline and the only actual
*
* performance specification.
*
* Altough models can be a useful tool in evaluating device
*
* performance, they cannot model exact device performance
under *
* all conditions, nor are they intended to replace bread-
*
* boarding for final verification. GaN Systems Inc.
therefore   *
* does not assume any liability arising from their use.
*
* GaN Systems Inc. reserves the right to change models
without  *
* prior notice.
*
*
*
* This library contains models of the following GaN Systems
*
* Inc. transistors:
*
*
*
*   GS66506T
*
**********************************************************
******
*$
.subckt GS66506T gatein drainin sourcein T1
*
.param conv_aide=1
.param Rth_CasetoAmbient=0
*
.param aDi=0.25       cur={(1.3/3.6)*(0.069*75/80)*225.7/1}
slp=2.0   rpara=0.88
+      ITc=0.003           rTc=-0.0128
x0_0=0.31         x0_1=0.255
+      di_gs1={7*4.3e-5}  di_gs2={2.6e-8}
di_gs3={100*0.8}    di_gs4={80*0.23}
+      Igs1=1.42e-10       Igs2={(3.0e-010)*(5.7)/20}
Igs3=4.9     Igs4=6.83e-01
```

```
+      Igs5=-7.85e-011    Igs6=-3.30
Igs7=6.0
+      Igd1=5.49e-012      Igd2={2.6e-11*(7.5)/3}
Igd3=-3.09        Igd4=12
+      Isd1=1.7e-013       Isd2=1e-12        Isd3=0
Isd4=2.5
+      Isd5=5e-013    Isd6=10                Isd7=4.5
of1=100   of2=35
+     ff1=0.345            ff2=1.2                ff3=4.5
ff4=0.5   ff5=8    ff6=0.14
*
Rth T0 T1 {(0.35*3.6)*(15/75*80*(1+0.005*(Temp-27)))/225.7}
Cth 0 T1 {(1/3.6)*(2.4e-5*75/80)*225.7}
Rth_pkg_brd T0 0 {0.5+Rth_CasetoAmbient}
Cth_pkg T0 0 {3e-3}
*
*
bdtemp 0 T1 I = (if(v(drain,source)>0,
+     (cur*(1-ITc*(V(T1)-0+Temp-
25))*log(1.0+exp(21*(v(gate,source)-7.9+6.1-0.000*(Temp-
25))/slp))*
+    v(drain,source)/(1 +
max(x0_0+x0_1*(v(gate,source)+9.1),0.2)*v(drain,source)))*
+    v(drainin,sourcein),
+    (cur*(1-ITc*(v(T1)-0+Temp-
25))*log(1.0+exp(21*(v(gate,drain)-7.9+6.1-0.000*(Temp-
25))/slp))*
+    v(source,drain)/(1 +
max(x0_0+x0_1*(v(gate,drain)+9.1),0.2)*1.0*v(source,drain))
)*
+    v(sourcein,drainin)))
*
*Note: Internal inductors can be disabled by uncommenting
the following 3 lines and
*commenting out the next 6 lines.
*
*rd drainin drain {(3.6/4)*(0.95*rpara*(1-0*rTC*(Temp-
25)))*18.2/225.7} tc=0.0128
*rs sourcein source {(1*3.6)*(0.238*rpara*(1-0*rTc*(Temp-
25)))/225.7} tc=0.0128
*rg gatein gate {1.5}
*
rd drain3 drain {(3.6/4)*(0.95*rpara*(1-0*rTC*(Temp-
25)))*18.2/225.7} tc=0.0135
ld drainin drain3 {4.0e-10} Rser=0
rs source3 source {(1*3.6)*(0.238*rpara*(1-0*rTc*(Temp-
25)))/225.7} tc=0.0135
```

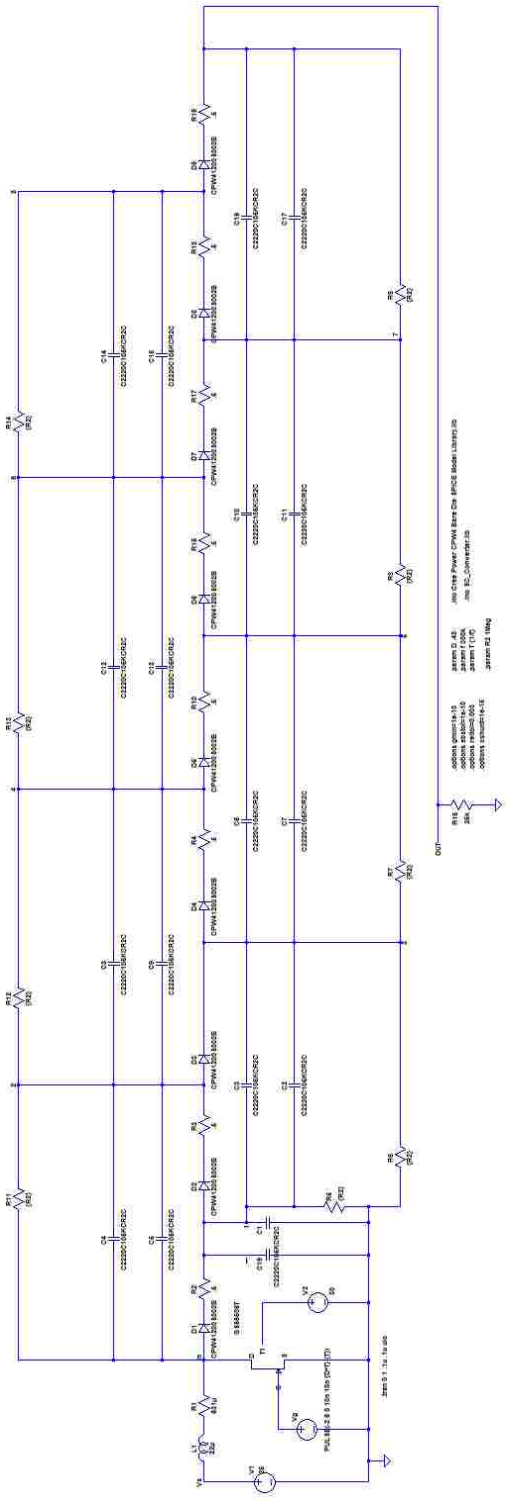
```
Ls sourcein source3 {4.0e-11} Rser=0
rg gatein gate1 {1.5}
Lg gate1 gate {1e-9} Rser=0
*
Rcsdconv drain source {1000Meg/aDi}
Rcgsconv gate source {1000Meg/aDi}
Rcgdconv gate drain {1000Meg/aDi}
*
bswitch drain2 source2 I = (if (v(drain2,source2)>0,
+    (cur*(1-ITc*(v(T1)-0+Temp-
25))*log(1.0+exp(21*(v(gate,source2)-7.9+6.1-0.00*(Temp-
25))/slp))*
+    v(drain2,source2)/(1 +
max(x0_0+x0_1*(v(gate,source2)+9.1),0.2)*v(drain2,source2))
),
+    (-cur*(1-ITc*(v(T1)-0+Temp-
25))*log(1.0+exp(21*(v(gate,drain2)-7.9+6.1-0.00*(Temp-
25))/slp))*
+    v(source2,drain2)/(1 +
max(x0_0+x0_1*(v(gate,drain2)+9.1),0.2)*1.0*v(source2,drain
2)))) )
R_drain2 drain2 drain {(1e-4)}
R_source2 source2 source {(1e-4)}
*
**
bgsdiode1 gate source1 I = (if( v(gate,source)>100,
+
     (0.2*(1*conv_aide*10.5*aDi/1077*(di_gs1*(exp(16*(100.0
)/di_gs3)-1)+di_gs2*(exp(16*
+    (100.0)/di_gs4)-1)))*(1+0.005*(Temp-
27))*(1/3.6*225.7))*(1+0.09*exp(0.051*(Temp-27))),
+
     (0.2*(1*conv_aide*10.5*aDi/1077*(di_gs1*(exp(16*(v(gat
e,source1))/di_gs3)-1)+di_gs2*
+    (exp(16*(v(gate,source1))/di_gs4)-1)))*(1+0.005*(Temp-
27)))*(1/3.6*225.7))*(1+0.09*exp(0.051*(Temp-27))))
R_source1 source1 source {(14.47/380)}
*
**
bgddiode1 gate drain1 I = (if( v(gate,drain)>25,
+
     (conv_aide*4*(0.5*aDi/1077*(di_gs1*(exp(0.3*(25.0)/di_
gs3)-1)+di_gs2*(exp(0.3*
+    (25.0)/di_gs4)-1)))*(1+0.005*(Temp-
27))*(0.2/3.6*225.7)),
```

```
+
     (conv_aide*4*(0.5*aDi/1077*((di_gs1*1)*(exp(0.3*(v(gat
e,drain1))/(di_gs3*1))-1)
+    +(di_gs2*(1))*(exp(0.3*(v(gate,drain1))/(di_gs4*1))-
1)))*(1+0.005*(Temp-27))*(0.2/3.6*225.7))))
R_drain1 drain1 drain {14.47/380}
*
bdsdiode1 drain1 source1 I = (if( v(drain1,source1)>850,
+    (0.4e-
9*conv_aide*200*(0.5*aDi/1077*(di_gs1*(exp(5*(850.0-
630+((Temp-25)/1.75))/di_gs3)-1)+1*di_gs2*(exp(5*
+    (850.0-630+((Temp-25)/1.75))/di_gs4)-
1)))*(1+0.1*(Temp-27))*(0.2/3.6*225.7)),
+    (0.4e-
9*conv_aide*200*(0.5*aDi/1077*((di_gs1*1)*(exp(5*(v(drain1,
source1)-630+((Temp-25)/1.75))/(di_gs3*1))-1)
+    +1*(di_gs2*(1))*(exp(5*(v(drain1,source1)-630+((Temp-
25)/1.75))/(di_gs4*1))-1)))*(1+0.1*(Temp-
27))*(0.2/3.6*225.7))))
*
bdsdiode2 drain1 source1 I = (if( v(drain1,source1)>750,
+    (0.1e-
3*conv_aide*200*(0.5*aDi/1077*(di_gs1*(exp(0.5*(750.0-
670)/di_gs3))))
+    *(1+0.06*exp(0.1*(Temp-27)))*(0.2/3.6*225.7)),
+    (0.1e-
3*conv_aide*200*(0.5*aDi/1077*((di_gs1)*(exp(0.5*(v(drain,s
ource)-670)/(di_gs3)))))
+    *(1+0.09*exp(0.1*(Temp-27)))*(0.2/3.6*225.7))))
*
bgddiode2 gate drain1 I = (if( v(gate,drain1)>30,
+    (conv_aide*1e-12*((0.1*di_gs1*(exp(3*(30-
4)/1))+di_gs2*
+    (exp(3*(30-4)/1))))*(1+0.005*(Temp-
25)))*(1/3.6*225.7),
+    (conv_aide*1e-12*((0.1*di_gs1*(exp(3*(v(gate,drain1)-
4)/1))+di_gs2*
+    (exp(3*(v(gate,drain1)-4)/1))))*(1+0.005*(Temp-
25)))*(1/3.6*225.7)))
****
*
C_GS  gate source   {(1.25/7*Igs1/120/2.18)*3.5*225.7}
C_GS1 gate source Q =
((1/7*10/120/2.18*1.5)*225.7*1.5*((0.5*Igs2*Igs4*log(1+exp(
ff5*0.5*(v(gate,source)-Igs3+
+                        4.6)/0.9933))-
Igs5*Igs7*log(1+exp(ff6*(v(source,drain)-Igs6)/Igs7)))))
```

```
*
C_GD   gate drain   {(0.8/17*Igd1/30/2.18)*1.5*225.7}
C_GD1  gate drain Q =
((0.7/7*1/25/2.18*0.8)*225.7*((0.5*Igs2*Igs4*log(1+exp(ff1*
6*(v(gate,drain)-Igs3+of1-50)/
+
     (Igs4*ff3)))+Igd2*Igd4*log(1+exp(0.5*ff2*(v(gate,drain
)-Igd3+of2-30)/(Igd4
+                        *ff4))))))
*
C_SD  source drain       {(2/7*Isd1/2.18)*10*225.7}
C_SD1 source drain Q =
(1/7*1/2.18*18*225.7*(4*Isd2*Isd4*log(1+exp(0.1*(v(source,d
rain)-Isd3+145)/Isd4))+
+
Isd5*Isd7*log(1+exp(1.5*(v(source,drain)-Isd6+55)/Isd7))
+                             +5.7*0.0*(0.5*2.5e-
12*0.643*log(1+exp(v(source,drain)-4.68+80))/(0.643
+                        *3.5))))
.ends
*$
```

Appendix B

4-Stage HSCC: Evaluation Circuit



Appendix C

8-Stage Bipolar HSCC: Grid Scale