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Avalanche ISFET Sensing Chip for DNA Sequencing

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DEDICATION

To my family and friends

ACKNOWLEDGMENT

My graduate student life in University of New Mexico was one of the most exciting, joyful and rewarding experience in my life. Hereby, I would like to show my best gratitude and appreciation to the people who helped me to have this great time and make a lasting impression in my life.

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ABSTRACT

DNA sequencing is a fundamental tool for biological science, aimed primarily at uncovering the genetic contributions to diseases. The first Human DNA sequence, which employed conventional fluorescent-based Sanger Sequencing method, took many years to complete at a cost of over three billion dollars. In one survey, it shows that Human Genome Project (HGP) had generated more than $67 billion in U.S. economic output, $20 billion in personal income for Americans and 310 thousand jobs in USA, only during year 2010. The HGP has increased the need for high-throughput, low cost, fast, accurate and inexpensive DNA sequence technique. This demand has forced a fundamental shift away from the conventional Sanger sequencing technique to Next Generation Sequencing (NGS) technique for genome analysis. NGS techniques provide high-throughput; low cost, user-friendly DNA sequencing and they are opening fascinating new opportunities in biomedicine. In near future, as the price of complete DNA sequencing goes further down to a few hundred dollars, we will then have DNA sequence data of millions of people. The enormous DNA sequencing data and corresponding correlation will allow us to figure out which sequences are responsible for which traits. As we relate the sequences of all

of these people to their traits, we will be able to connect the dots and learn the genetic equations that define health, longevity, and behavior.

In this dissertation, we propose a new avalanche ion-sensitive field effect transistor (A-ISFET) capable of sensing very weak pH changes during DNA synthesis. This is the first attempt to operate ISFET in avalanche mode. A-ISFET is the core of our proposed highly dense, low-cost and high-throughput DNA sequencing technique. To validate our proposed concept, we have designed, laid-out, fabricated, and successfully tested a test chip with arrays of A-ISFET using TSMC 0.25um CMOS process. Our research also includes the development of data processing circuits and system architectures for fast and efficient data processing. The test chip is used as the verification of this new DNA sequencing concept and the validation of the interfacial circuitry for the synchronization of sensing system. Each of the unit cells in the test chip is accessed through column-select and row-select signals during readout process. We design a test environment and test setup for correct readout of the sensing data from the chip through proper synchronizing signal. A specially milled and shaped structure is used to inlet and outlet the bio-chemical on the gate surface of the A-ISFET arrays. The inlet and outlet is attached to a time-controlled valve to control the flow of liquids on the surface of A-ISFET chip for test and verification of this novel DNA sensing concept. The test chip has been tested both at normal mode and at avalanche mode. Test results show that the sensitivity at avalanche mode is 6 times more than the normal mode of operation.

We have developed a model to determine the signal-to-noise ratio (SNR) of A-ISFET. The model identifies that there is an optimum bias point of A-ISFET to have maximum SNR sensitivity from the sensor. Every electronic device generates its own intrinsic noise, in addition to other induced noise from associated nearby components. We have identified different noise components of A-ISFET and have modeled their respective characteristics with bias change. Different noise components that we find in A-ISFET are thermal noise, flicker noise, shot noise, and dark current noise. This noise modeling of A-ISFET sensor will help us to understand noise sources better and to predict the sensor behavior with change of bias. Using the noise model, we can select a bias point to minimize the noise impact of A-ISFET sensor and maximize its SNR.

We also have developed a physical operation-based drain current model for A-ISFET during avalanche operation. Since A-ISFET operates in avalanche region, an accurate model for the breakdown behavior is therefore very important from both circuit design and circuit reliability point of view. The avalanche breakdown can result from impact ionization, a parasitic bipolar transistor, or the punch-through effect. Our developed model of A-ISFET drain current at avalanche region is due to impact ionization. We have validated the drain current model at avalanche through a correlation study among analytical model results, SPICE simulation results, and experimental measured results.

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CHAPTER 1
INTRODUCTION

1.1 Background

DNA stands for Deoxyribonucleic Acid. It is found inside a special area of cell called the nucleus. In 1953, Watson and Crick determined the structure of DNA. Scientists before Watson and Crick had determined the chemical composition of DNA, and that it was the hereditary material, while scientists after Watson and Crick broke the genetic code, and determined how the sequence of bases in DNA specified the sequence of amino acids in proteins. Since then, developing technology for reading this sequence was a fundamental problem in molecular and biological sensing [1]. Techniques that first enabled us to read DNA sequence was invented by Sanger in 1978. They were very costly, slow, and tedious [2]. International Human Genome Project (IHGP) did the first human DNA sequence in 2003, to improve our biological understanding, our health, and wellbeing. IHGP had used conventional Sanger sequencing method for DNA sequencing and it took around 13 years to complete the whole sequencing at a cost of over three billion dollars [3-4].

Reductions in the cost, complexity and time required to sequence large amounts of DNA have significant scientific, economic, and cultural impact [2, 5]. Attempts were made for fast DNA sequencing through conventional Sanger method with massively parallel architecture by Rothberg et.al. in 2005, however the cost remained tremendous [1, 6]. The completion of first human DNA sequencing by HGP in 2003, initiated the need for high-throughput, low cost, fast, accurate, and inexpensive DNA sequencing technologies, Next Generation Sequencing (NGS). NGS is aimed to provide low cost, fast, accurate, user friendly, point-of-care DNA sequencing to uncover details of the genetic contributions to diseases [1-2]. DNA sequencing is a fundamental tool for biological science, which determines the precise order of four bases - adenine, guanine, cytosine, and thymine within a DNA molecule [6].

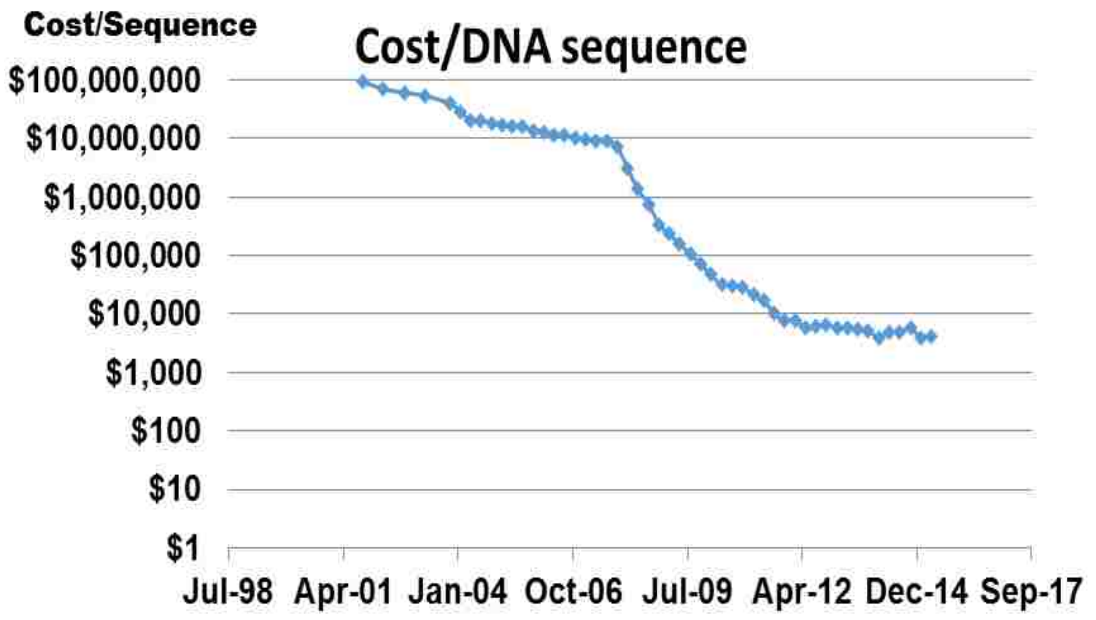

Figure 1.1: DNA Sequencing Cost per person: NHGRI [7]

In 2001, the US National Human Genome Research Institute (NHGRI) put forth a goal of achieving a "$1000 human genome", i.e. the full cost of identifying human genome sequence for less than USD$1000, as a performance milestone in low cost human genome sequencing. Figure 1.1, shows the trend in human DNA sequencing cost at sequencing centers that are funded by NHGRI [7]. We can see a huge reduction in cost per DNA sequence that results from the development and advancement of next-generation sequencing (NGS) technologies. Low cost human genome sequence will provide us easy access to genomic information to prescribe genomic personalized medicine [1].

1.1.1 Human Genome Project (HGP) : Importance of DNA sequencing

The sequencing of the human genome by HGP was the largest single undertaking in the history of biological science. It was a huge milestone in scientific achievement [4] and was coordinated by the National Institutes of Health and the U.S. Department of Energy. This massive project was carried out in 13 long years i.e. starts in 1990 and was completed in 2003. The primary objective of HGP was to determine the sequence of the human genome and to identify different genes that it contained. The HGP has discovered that there are ~20,500 human genes. It has also detailed out

the location, structure, organization, and function of those human genes. The tools and techniques that were developed and used by HGP, helped a great deal to characterize the genomes of several other important organisms used in biological research, such as mice, fruit flies, and flatworms [8].

Since the completion of HGP at 2003, there has been a significant development of genomic tools, technologies and techniques to fuel the DNA sequencing efforts forward. These developments, in many cases, are commercialized and form the foundation for a highly active and growing commercial genomics-based industry [4]. One survey shows that federal investment of $3.8 billion throughout 13 long years in HGP project had generated more than $67 billion in U.S. economic output, $20 billion in personal income for Americans and 310 thousand jobs in USA in fiscal year 2010. Literally, the HGP had initiated a "genomic revolution" by influencing renewable energy development, industrial biotechnology, agricultural biosciences, veterinary sciences, environmental science, forensic science, homeland security, and advanced studies in zoology, ecology, anthropology, and other disciplines [4]. Figure 1.2, shows the detailed structure of the functional impacts that had resulted from the sequencing of the human genome by HGP in 2003.

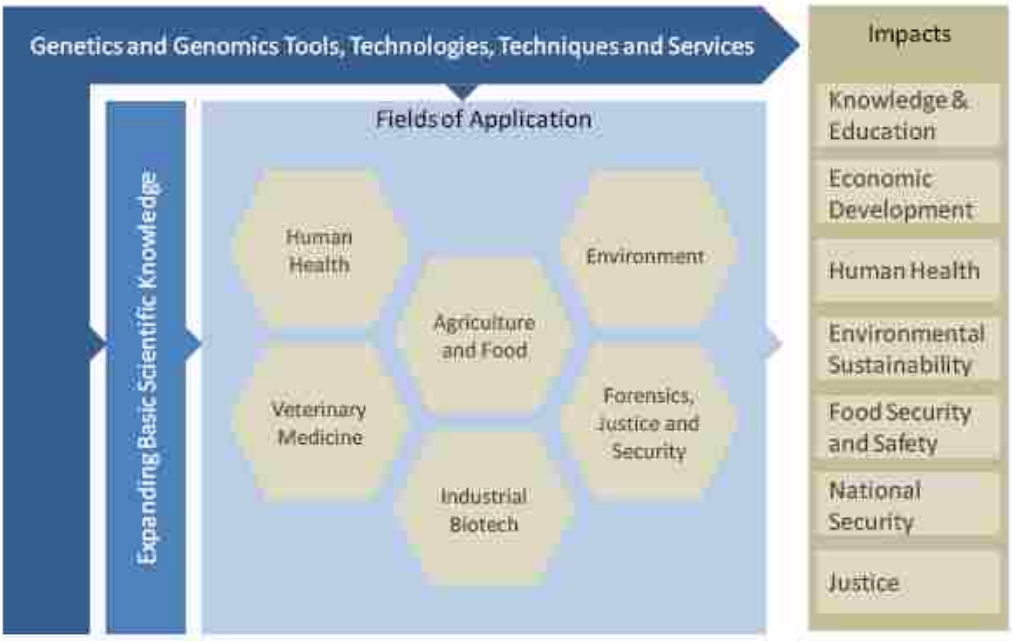

Figure 1.2: Functional Impacts Associated with DNA sequencing [4]

The development and advancement of many NGS techniques provide us fast and low cost DNA sequencing. It is now possible to complete the DNA sequence of a human for a cost of only a few thousand dollars [7] and in couple of days. In the near future, as the price of complete DNA sequencing goes further down to few hundred dollars, we may have the complete DNA sequence data for millions of people. The DNA sequencing data and corresponding correlation may allow us to figure out which sequence is responsible for which traits. As we relate the sequences of all of these people to their traits, we can connect the dots, and have an understanding of the genetic information that defines health, longevity, and behavior.

1.1.2 DNA sequencing and ISFET

IHGP had used conventional Sanger sequencing method for DNA sequencing. This conventional sequencing technique requires expensive laser to detect fluorescent tags or labels. It also needs highly precise and expensive instrumentation, specialized personnel, and very sophisticated numerical algorithms to interpret the generated data. These requirements make this sequencing process very time consuming and costly. Therefore, it is not suitable for use in mass portable point-of-care medical systems [9]. Researchers are exploring various NGS techniques that are cost efficient, fast and easy to use for DNA sequencing. These novel NGS techniques are targeted to on-site and point-of-care medical diagnostics to prescribe genomic personalized medicine. Numerous research and development on NGS has forced a fundamental shift away from the Sanger sequencing for genome analysis to different label-free, user friendly, non-optical, fast, and easy techniques [5].

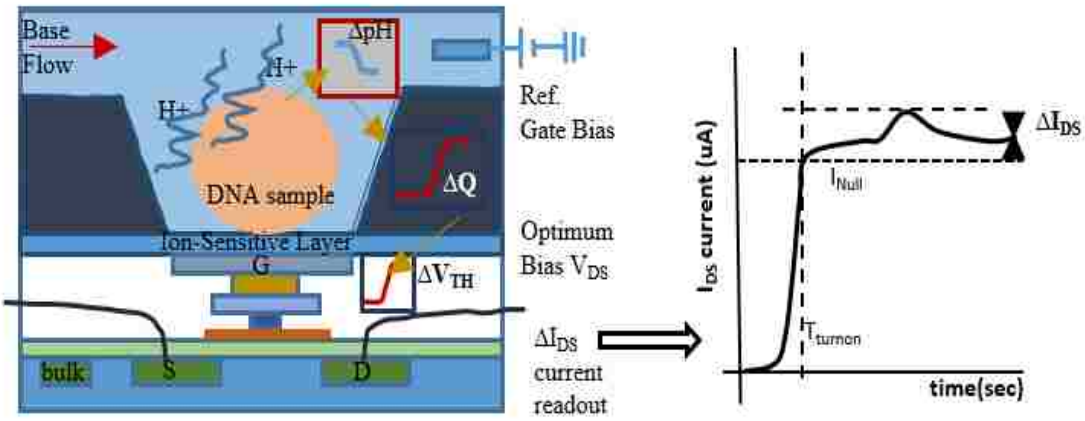

Figure 1.3: Typical ISFET sensor and its output signal

Semiconductor based, non-optical DNA sequencers are suitable for low cost and high throughput sequencing because they read a DNA sequence electronically. Moreover, they can be manufactured in high volumes at very low cost by standard complementary metal oxide semiconductor (CMOS) fabrication process [10]. Ion sensitive filed effect transistor (ISFET) [11] based electro-chemical sensor is one of the most suitable candidate for DNA sequencing in non-optical, semiconductor based techniques [12]. In addition, ISFET biosensors are also CMOS compatible, portable and label-free [12-14].

The ion sensitive gate insulator of the ISFET senses specific ion concentration and generates an interface potential at the gate (ΔV_{th}). This interface potential is proportional to pH change (ΔpH). The change in interface potential at gate, due to pH change results in a change of drain-source current, based upon the bias of ISFET [10, 13]. Figure 1.3, shows the structure of a typical ISFET sensor and the generated output signal of the sensor [10]. The gate of ISFET can be made of different ion-sensitive materials, which includes Al_2O_3, Si_3N_4, Ta_2O_5, SnO_2, and SiO_2. Our selection of gate material is based on stability, sensitivity, selectivity, long-term drift, temperature dependency, and responses time of the gate material.

1.2 Dissertation contents

This dissertation mainly focuses on the design, test and analysis of an ISFET sensing chip, which is fabricated to verify a highly sensitive NGS technique for DNA sequencing. As we are dealing with a very weak sensing signal, the ISFET chip is designed to operate in avalanche mode of operation to derive higher sensitivity from the ISFET sensor. The avalanche phenomenon is an established idea for photodetectors (APD) and is extensively used in optical communication. However, the concept of avalanche ISFET (A-ISFET) is very new and was never used for ISFET sensor. Our motivation behind this unique A-ISFET concept is to reduce DNA sequencing cost further and to increase the sensor sensitivity further. Avalanche operation of ISFET provides us enough sensitivity from a smaller sensing device and it makes the overall chip size smaller, which results further reduction in DNA sequencing cost.

We also propose a new readout technique for A-ISFET sensor, which is based on pH-to-Current conversion [13]. The conventional readout technique for ISFET is pH-to-Voltage [10, 14-17]. In pH-to-Voltage readout technique, we force a small reference current into the drain of ISFET and measure the V_{GS} voltage as the output of ISFET sensor. The proposed pH-to-Current readout technique for A-ISFET, on the other hand, forces a drain-source voltage that is close to breakdown voltage and reads the current I_{DS}, which results from the small change of interface potential at the gate (ΔV_{th}). The change in interface potential at gate (ΔV_{th}) is proportional to pH change (ΔpH). The unique circuit that we designed for pH-to-Current readout ensures the operation of ISFET in avalanche through forcing a drain to source bias voltage that is near breakdown region of the p-n junction. A-ISFET, which is designed for pH-to-Current readout, is the sensing component of our DNA sequencing chip [18]. However, the output response from A-ISFET is non-linear with pH change. This non-linear response of A-ISFET can be taken care by proper calibration and lookup table as well as through post processing of the bulk data by digital signal processing algorithm. The operation of ISFET in avalanche region gives us a very high output signal in response to a very weak signal at sensor input. This high output signal results from the multiplication of carriers due to impact ionization in depletion region of reverse bias p-n junction. A very strong reverse bias voltage in p-n junction at drain

side of A-ISFET creates a long depletion region and most of the carrier multiplication takes place there.

The completion of HGP in 2003, had initiated a strong drive for NGS techniques that are of low cost, fast, and user-friendly. Among NGS techniques, ISFET based very large scale DNA sensor-array chip is getting huge attention [10, 12, 18] for direct human genome sequencing because of, their low cost, non-optical, semi-conductor based sensing. We need to minimize the size of ISFET sensor further so that very large-scale DNA sensor-array integration is possible with lower cost. This dissertation proposes a very unique unit sensing cell with only three scalable FET transistor i.e. one is used for sensing (A-ISFET) and the rest two (MOS-FET) are for switching and synchronization. This unique and compact structure of the unit cell greatly reduces the size and fabrication cost of the sequencing chip.

We have found through mathematical analysis that the sensitivity of the ISFET is greatly dependent on the operational region, which is set by DC bias of the device. During ISFET operation with nominal voltages, we can get maximum sensitivity from the device by operating it in saturation region. SPICE simulation confirms that if we operate ISFET in avalanche region, we can achieve even more sensitivity from a tiny device i.e. ~10X more sensitivity from maximum sensitivity at normal mode of operation.

Noise is a disturbance that obscures or reduces the clarity of a signal. Every electronic device generates its own intrinsic noise, in addition to other induced noise from associated nearby components. We have identified different noise components of A-ISFET and have modeled their respective characteristics with bias change. Different noise components that we find in A-ISFET are thermal noise, flicker noise, shot noise, and dark current noise. We have developed a model to determine the signal-to-noise (SNR) ratio of A-ISFET. The model identified that there is an optimum bias point of A-ISFET to have maximum SNR sensitivity from the sensor. This noise modeling of A-ISFET sensor will help us to understand the associated noise sources better and it will provide us options to optimize the design. Using the

noise model, we can minimize the noise impact of A-ISFET sensor and maximize its Signal-to-Noise (SNR).

We have developed a physical operation-based drain current model for novel avalanche ISFET (A-ISFET). Since the A-ISFET operates in avalanche region, an accurate model for the breakdown behavior is therefore very important for both circuit design and circuit reliability point of view. The drain breakdown can result from impact ionization, a parasitic bipolar transistor, or the punch-through effect. Our model of A-ISFET drain current at avalanche region is due to impact ionization. To validate our drain current model of A-ISFET we perform a correlation study of the analytical data with SPICE simulation results, and experimental measured results.

We have designed a test chip by the TSMC's 0.25um CMOS process and laid out the chip to fabricate using the same process. Our test chip contains four different cores where each core is made of different unit cells with different dimensions and type. The available ISFET devices are of p-type and n-type with small (with W/L=2.5) and large (with W/L=24) dimensions. Each core is made of 90x95 arrays of specific type of ISFET device. The chip pad ring contains electrostatic discharge (ESD) devices to protect the transistors in the core against electrostatic charge injection during chip handling. There are total of 52 pins in the chip including four V_{DD}, four GND and several input/output signals. In this dissertation, we also designed the readout interfaces, data processing circuits and integrated the whole system for fast and efficient data processing. The test chip is used as the verification of this A-ISFET based new DNA sequencing concept and the validation of the integration and synchronization of the whole sensing system.

The fabricated chip from TSMC is found to be functional. We have created a test environment and test setup for correct readout of the sensing data from the chip through proper synchronizing signal. During test, we have accessed each of the unit cells in the test chip through column select and row select signal during readout process. A specially milled and shaped structure is used to inlet and outlet the bio-chemical on the surface of A-ISFET arrays. The inlet and outlet of the bio-chemical system is controlled by time-controlled valve, to control the flow of liquids on the

surface of A-ISFET chip for test and verification of this unique DNA sensing concept. We test the chip both at normal mode and at avalanche mode. We find that it works perfectly as a sensor both in normal mode and in avalanche mode. Test results show that the sensitivity at avalanche mode is much higher than (~6 times) the sensitivity at normal mode of operation.

1.3 Innovative aspects and Unique Contributions

This dissertation contains some novel aspects that are listed below:

- First ever operation of an ISFET in the avalanche region to derive high sensitivity from a very weak input signal and/or tiny sensing device.
- A unique pH-to-Current readout process is proposed and demonstrated to operate the sensing device in avalanche mode.
- Noise analysis of ISFET in avalanche mode is carried out to ensure optimum bias for maximum Signal-to-Noise ratio (SNR) during operation.
- A very unique, compact and tiny unit cell is designed to minimize the chip size, and cost.
- A physical operation based drain current model for ISFET at avalanche mode of operation is developed and a correlation study is performed to validate the model.
- A functional test chip is designed, laid out and tested to validate the concept of A-ISFET.

1.4 Organization of the Dissertation

In this dissertation, we are mainly concerned with analysis, design, modeling, and testing of a very new sensing device; avalanche ISFET (A- ISFET) for low cost Next Generation DNA sequencing.

Chapter 1 starts with a discussion on background and motivation toward DNA sequencing and low cost NGS techniques. It is followed by a discussion on the innovative aspects of this dissertation and the contents of the dissertation.

Chapter 2 gives us an introduction with ISFET sensor and sensitivity. It also presents a mathematical analysis on the sensitivity of ISFET based sensor. The

analysis was done in SPICE and MATLAB, for both normal modes of operation and avalanche mode of operation.

Chapter 3 identifies different noise components in A-ISFET and model their behavior with change of bias. Here, we developed a model to find an optimum bias point for A-ISFET sensor that give us maximum Signal-to-Noise ratio (SNR).

Chapter 4 models the drain current behavior of ISFET while it operates in avalanche region. We also verified the model through a correlation study with simulation, and measurement data.

Chapter 5 discusses on the design, architecture, and layout of the ISFET test chip. It also discusses on the different building blocks of the test chip and their operation. Here, we also present the findings of our literature review on state of the art ISFET sensor and DNA sequencing technique.

Chapter 6 presents the test procedure, and results of the ISFET chip. It also discusses on wire bonding, signal setup, synchronization, hardware, and other details.

Finally, in Chapter 7 we concluded the dissertation with discussions.

1.5 Discussions

In this chapter, we give a brief introduction on the dissertation, its contents and organization. It also gives us an indication on the motivation behind the research and the economic impact of the research.

CHAPTER 2

THEORY ON ISFET AND SENSITIVITY

2.1 Introduction to Sensor

A sensor is a device that is used to translate information, such as amount of ion concentration into an analytical signal, whereas, a biosensor is generally defined as an analytical device that is designed to detect or quantify a biochemical molecule such as a particular DNA sequence, pH or particular protein [19]. A successful biosensor has a high sensitive detector element that can detect very small changes in the bio-sensitive element without cross sensitivity to other irrelevant parameters, such as temperature or pressure. An ideal biosensor should neither be harmful nor deteriorate in the presence of biological substances. Ideal biosensors are fully reversible, highly reliable, highly selective, small, portable, have high signal-to-noise ratio, be immune to environmental conditions, and easy to calibrate. An actuator, on the other hand, can be defined as a transducer that converts an electrical signal or energy into a signal of another form for motors and switches [20].

Quantification of biological or biochemical processes is of the utmost importance for medical, biological and biotechnological applications. However, converting the biological information to an easily processed electronic signal is challenging due to the complexity of connecting an electronic device directly to a biological environment. Electrochemical biosensors provide us with an attractive way to analyze the content of a biological sample due to the direct conversion of a biological event to an electronic signal [21]. Figure 2.1, shows typical elements and components of electrical biosensors.

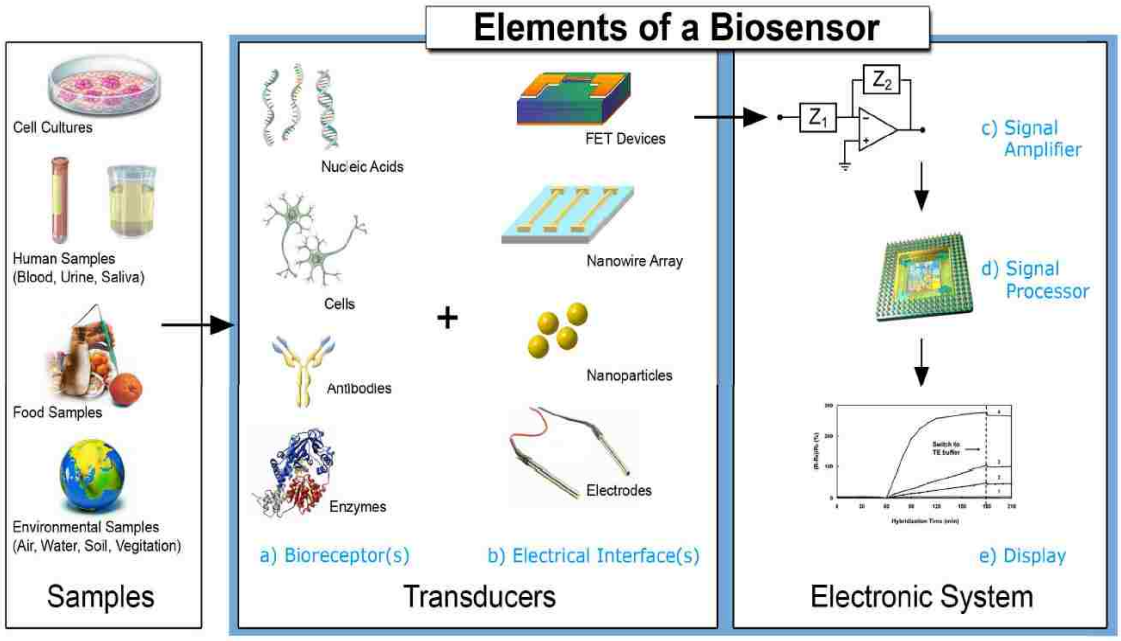

Figure 2.1: Typical elements of Electric Biosensor [21]

For a sensor, one of the most important figures of merit is the limit of detection, defined by the smallest concentration or amount of target that can be reliably sensed. Its internal noise, its drift, and its temperature [19] determine the limit of detection of sensor. However, we can improve overall sensing from a sensor through differential measurements in which a reference and a sensing element are used. Ideally, the reference element is insensitive to the analyte, but otherwise it has similar properties to the sensing element. The output signal that results from the difference between the signal of reference element and the sensing element is very robust from noise and influences [22].

This research work limits us to the electronic ion sensitive field-effect sensor, which is the basis of our A-ISFET based DNA sequencing chip. Electronic biosensors rely solely on the measurement of currents and/or voltages to detect the contents in a bio-chemical [19]. Due to their low cost, low power, and ease of miniaturization, electrical biosensors have great potential for applications, where minimizing size and cost is crucial, such as point of care diagnostics and bio-warfare agent detection.

2.1.1 Bio-Sensor: Chemical Sensors and their features

A chemical sensor is a device that transforms chemical information into an analytically useful signal. Biosensors are chemical sensors in which the recognition system uses a biochemical mechanism [23]. A biosensor needs to have three general features, which are a selective surface, a transducer, and a processor [20] as shown in Figure 2.2. The selective surface allows for a specific interaction with the target analyte, which is a compound whose composition or presence is being sought. A common method to achieve selectivity is to modify the sensor surface with immobilized receptors that bind selectively to the wanted target.

The main limitations of many chemical sensors are associated with the selectivity of the response to the target analyte compared with the response seen from potential background or contaminating compounds [25]. In a constant background, there is little need for selectivity. Generally, for a chemical sensor the background concentration changes in unknown ways due to the presence of similar chemical components or active species, temperature and pressure fluctuations.

The main types of chemical sensors developed to date rely on electrical or optical transduction technologies [25]. In this dissertation, we are mainly concerned with electrical transduction, which can be divide into amperometric type, potentiometric type or conductimetric type, depending on whether the measured signal is the current, voltage or conductance, respectively [19,25].

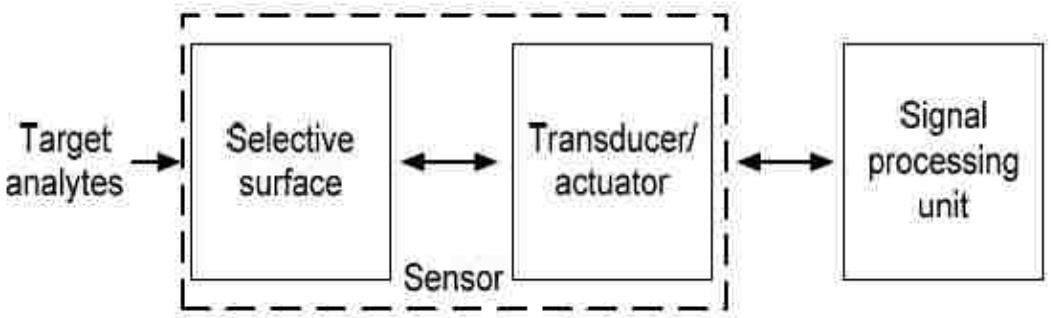

Figure 2.2: General features of a chemical sensor [20, 24]

Transducer	Mechanism	Signal	Example Sensor
Amperometric	Electron charge transfer reaction (Faraday's law)	Current: due to production or consumption of electroactive species	Oxygen, some hydrocarbons, hydrogen peroxide, fuel cells
Potentiometric	Multiphase equilibrium (Nernst Equation)	Potential: due to distribution of ionic species	Glass pH electrode, ion selective electrode
Conductomeric	Variation of resistance with composition	Conductance or resistance: due to change in resistive elements	Metal-oxide-semiconductor gas and humidity sensor, the oxide gas sensors

Table 2.1: Electrochemical Sensor Transduction Mechanisms [24]

2.1.2 Amperometric Chemical Sensor

The diagnostic analyses that are widely available are based on optical measurements. However, complicated readout instrumentation, long duration for sample pre-processing and labeling makes optical diagnostic methods expensive, time-consuming and non-portable. Electrical detection methods, on the other hand, rely on much simpler instrumentation that ensures lower cost, and easy and faster operation. Electrical detection methods also ensure label-free detection, avoidance of the influence of the label on the binding properties, and the possibility of real-time monitoring of binding interactions. In addition, micro fabrication based mass production provides the possibility of miniaturization and multiplex sensing through electrical transducers. The sensing method of our proposed DNA sequencing is based on electrical transduction in which amperometric chemical sensing is used.

An amperometric chemical sensor measures the current that results from change in electro-active species in a bio-chemical solution [21]. The sensor is made of two metal electrodes maintained at a constant potential or voltage difference. The current flow through the sensor circuit is established and is monitored by suitable

electronics and techniques. The presence of electro-active species is sensed through the variation of measured current between the electrodes.

2.2 Ion Sensitive Field Effect Transistor (ISFET)

ISFET is an electronic device that is used as an electro-chemical sensor and it works on the field effect principle, similar to that of MOSFET. ISFET was proposed and invented by Piet Bergveld over 40 years ago [26]. Since then, the original ISFET had been used in various devices including digital pH meters [27], urea detection devices [28], glucose sensors [29], and DNA image Sensors [30]. Recently, massive arrays of ISFETs are reported to use in CMOS compatible integrated circuit, to directly perform DNA sequencing of genomes [12]. This dissertation is mainly concerned with A-ISFET based DNA sequence chip where ISFET is the building block of the sensor. Many ISFET's characteristics are related to the FET behavior. Therefore, in this section fundamentals of semiconductors and FET physics will be discussed.

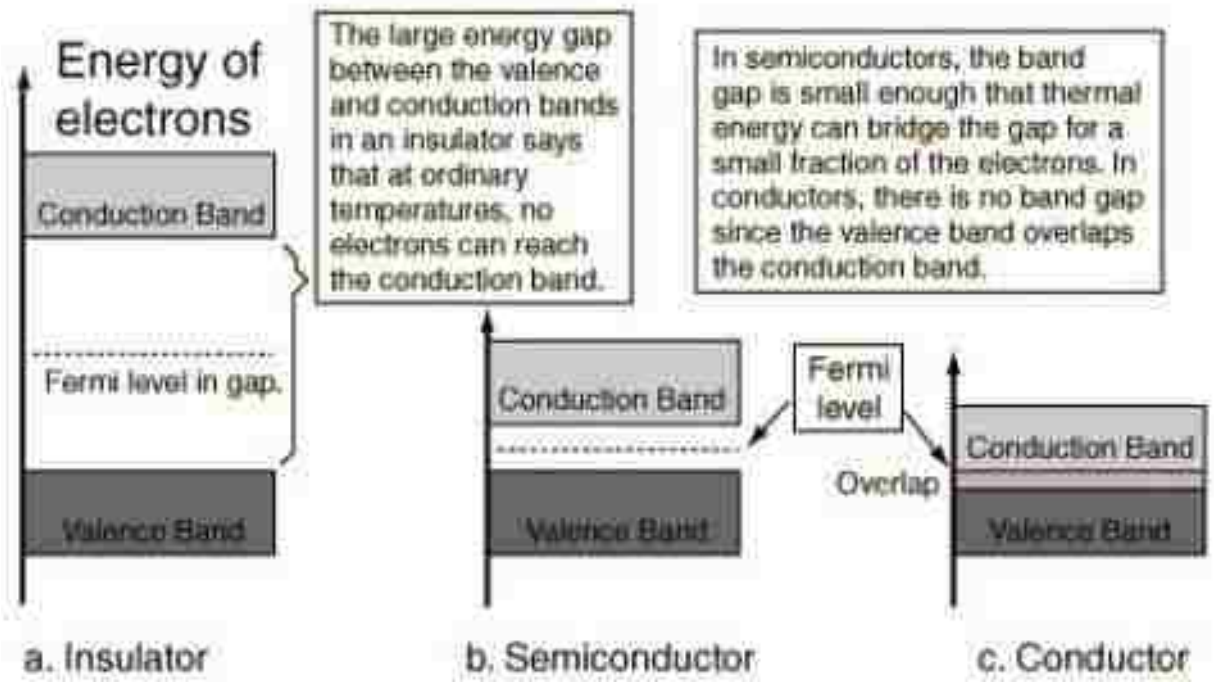

Figure 2.3: Energy band diagram of materials [31]

2.2.1 Fundamentals of Semiconductor

Materials such as metals, insulators or semiconductors have different electrical properties due to their electronic band structure. In semiconductors, there are forbidden energy states within an energy band gap E_g. Allowed energy levels form bands below and above the band gap E_g are called valence and conduction band, respectively. Typically, in a semiconductor, the energy of the band gap E_g is smaller than 2 eV and the thermal energy at room temperature can give electrons enough energy to move from the valence band to the conduction band. Insulators have a wider band gap (e.g. 9 eV for SiO_2). Therefore, in insulator electrons cannot cross the band gap at room temperature. Whereas in metals/conductors the valence band and conduction band overlaps. Figure 2.3, shows the relation of valence band and conduction band with bandgap for metal, semiconductor and insulator [31].

Based on doping, semiconductors can be classified into two types, which are intrinsic semiconductor and extrinsic semiconductor. In intrinsic semiconductors, there are no impurity atoms and electron-hole pairs are generated and destroyed by thermal generation-recombination processes. In thermal equilibrium, each electron in the conduction band forms a hole in the valence band and thus the concentration of electrons equals the concentration of holes, in intrinsic semiconductors. This is the reason for Fermi level being in middle of the band gap in intrinsic semiconductor.

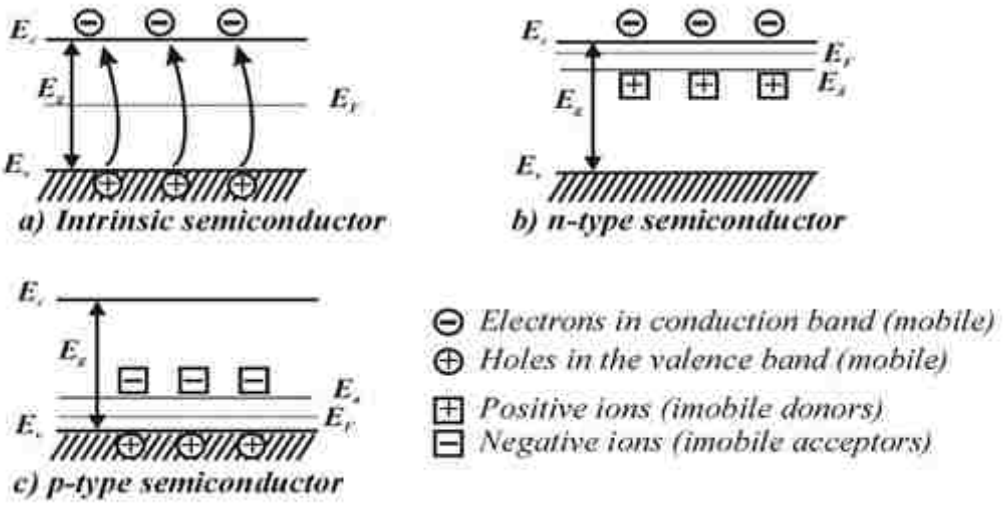

Figure 2.4: Three types of semiconductors: a) intrinsic semiconductors. B) n-type semiconductors and c) p-type semiconductors [31]

A semiconductor material that has implanted impurities is called extrinsic semiconductors. Implanted impurities form energy states within the band gap of semiconductor, which are very close to the valence or the conduction band, depending on the type of doping atoms. Doping atoms can have either three or five valence electrons. As an example, Boron has only three valence electrons and when it substitutes a silicon atom in the crystal lattice; it accepts an additional electron and becomes ionized. Therefore, boron is known as an acceptor. When boron is ionized, a positively charged hole is generated in the valence band that begins to participate in p-type conductance, whereas the boron ion stays fixed in the silicon crystal. For n-type conductance, the silicon is doped with doping atoms having five valence electrons, such as phosphorus or arsenic. The extra valence electron is donated to the lattice and a free electron is generated in the conduction band. In extrinsic semiconductor, the Fermi level is not in the middle of the band gap and it moves with variation of doping concentration in the material. In Figure 2.4, we can see the relation among valence band, conduction band, Fermi level and doping concentrations [31] of semiconductor materials.

2.2.2 MOSFET structure and Field Effect

Transistors are the semiconductor device that is extensively fabricated to make different electronic equipment. There are two types of transistors, one is current controlled bipolar junction transistor (BJT) and the other is voltage-controlled field-effect transistor (FET). In 1925, Julius E. Lilienfeld patents the basic principle of FET operation. However, in 1959 Atalla and Kahng from the Bell Labs first fabricated a metal oxide field-effect transistor (MOSFET) that works on the same principles as of FET.

The structure of an enhancement n-channel MOSFET, which has four different terminals, is shown in Figure 2.5. The terminals are drain (D), source (S), gate (G) and substrate (B). There is no conducting channel between source and drain, when the applied voltage in gate is zero. However, as we apply a positive voltage on the gate, charge carriers accumulate under the gate oxide through inversion process and conduction between drain and source begins. We can control the conductance and the amount of charge in MOSFET channel by changing the gate voltage V_{gs} [31].

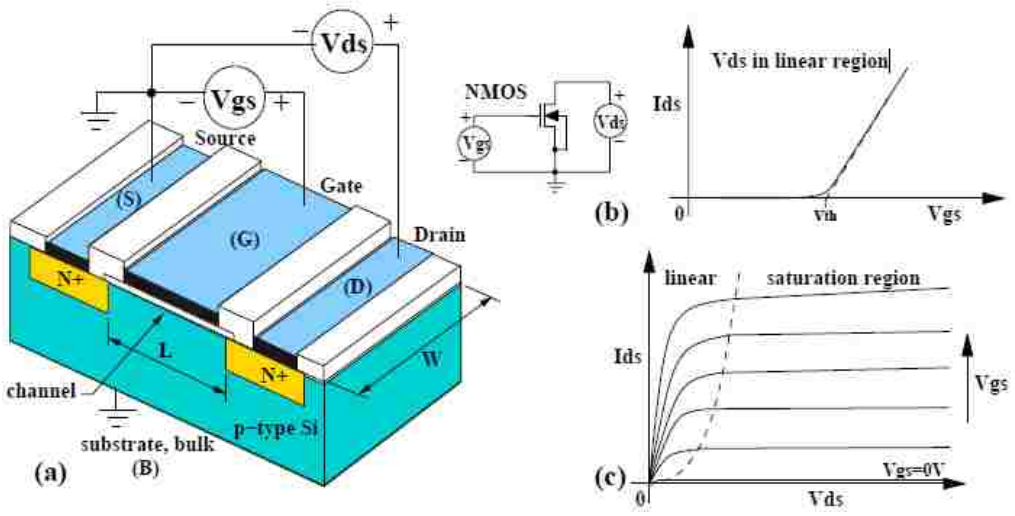

Figure 2.5: NMOS transistor and its operation with characteristics curve [32]

The type of charge carriers responsible for the conduction of the channel is opposite to the substrate. The p-type substrate inverts into n-type and an inversion layer is formed. The transfer curve and output characteristics curve of an n-channel MOSFET is also shown in Figure 2.5 [32].

One of the most important parameter of MOSFET is the threshold voltage (V_{th}), which is the minimum gate voltage required to form inversion channel under gate oxide for conduction, as shown in Figure 2.5. MOSFET has two regions of operation, the triode region and the saturation region at each fixed gate voltage. When $V_{ds} < V_{gs} - V_{th}$ and $V_{gs} > V_{th}$, MOSFET operates in triode or linear region of operation. In triode region, the channel current is linear function of drain-source voltage V_{ds}, which can be modeled as:

$$I_{ds} = \mu_n C_{ox} \frac{W}{L}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{1}{2}V_{ds}^2\right] = K_{n'} \frac{W}{L}\left[\left(V_{gs} - V_{th}\right)V_{ds} - \frac{1}{2}V_{ds}^2\right] \quad , \qquad (2.1)$$

when $V_{ds} => V_{gs} - V_{th}$ and $V_{gs} > V_{th}$, MOSFET operates in saturation region. In saturation region, the current is independent of drain-source voltage, V_{ds} and it can be modeled by:

$$I_{ds} = \mu_n C_{ox} \frac{W}{2L}\left[\left(V_{gs} - V_{th}\right)\right]^2 = K_{n'} \frac{W}{2L}\left[\left(V_{gs} - V_{th}\right)\right]^2 \quad . \qquad (2.2)$$

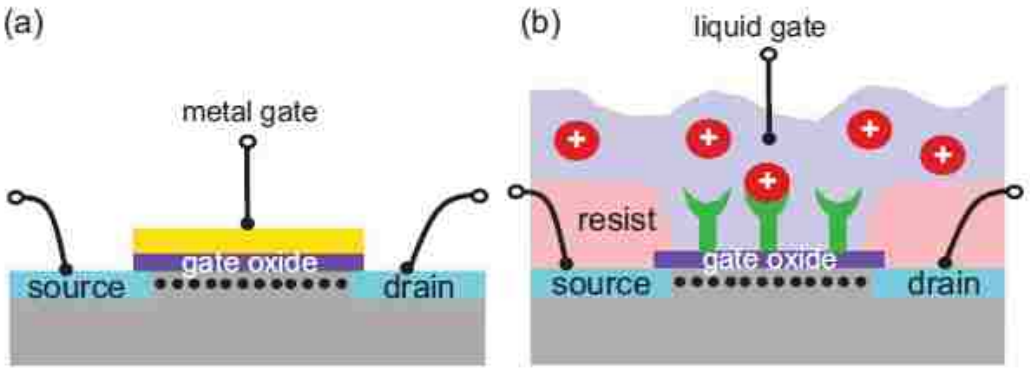

Figure 2.6: Structure of MOSFET and ISFET : Compare and Contrast [33]

2.2.3 MOSFET to ISFET

If we compare the structure and operation of ISFET with MOSFET, we find that they are very similar. ISFET is a MOSFET whose metal gate is replaced by a liquid gate, which is typically an electrode immersed in an electrolyte solution as shown in Figure 2.6. When ISFET is used as a sensor, the electrolyte is the solution under test that contains charged particles such as charged bio-molecules or protons. The gate oxide of ISFET is directly exposed to the electrolyte solution and is usually modified due to specific bindings of target species with receptors [33].

In case of MOSFET the threshold, voltage is assumed constant whereas, the threshold voltage for ISFET is dependent upon the ion concentration in electrolyte solution on the oxide layer. The threshold voltage of ISFET can be modeled as in [26]-

$$V_{th} = E_{ref} - \psi_0 + \chi_{solution} - \frac{\phi_{Si}}{q} - \frac{Q_{ox} + Q_{ss} + Q_B}{C_{ox}} + 2\phi_f \quad , \tag{2.3}$$

where, E_{ref} is the constant potential of reference electrode, ψ_o is the interface potential at solution/oxide interface, $\chi_{solution}$ is the surface dipole potential of the solvent, ϕ_{Si} is the work function of the silicon, Q_{ox}, Q_{ss} and Q_B are the oxide charge, oxide interface charge and bulk charge respectively, $2\phi_f$ is the potential for inversion of channel, and C_{ox} is the oxide capacitance /unit area.

It can be simplified as in [34] to be-

$$V_{th} = V_{th(MOS)} + V_{chem} \quad , \tag{2.4}$$

where $V_{chem} = \gamma + 2.303\alpha U_T pH$ and γ is a group of pH independent chemical potential, α is a dimensionless sensitivity parameter, and U_T = kT/q is the thermal voltage.

In an ideal case, where the highest sensitive interface material Ta_2O_5 is used on the gate, α is approximately equal to 1 and U_T at room temperature is about 26mV; we can achieve about 60mV of change in threshold voltage for every unit of pH change. Therefore, as the pH of gate liquid increase, threshold voltage of ISFET increases too. This increment of threshold voltage in ISFET causes reduced drain-source current I_{ds} for a given bias condition, shown in Figure 2.7.

We can model ISFET by combining a chemical part and a MOS transistor together, as shown in Figure 2.8. The capacitor in the chemical part is consists of two serially connected capacitors, which are Gouy-Chapman and Helmholtz capacitors [35]. This model concludes ISFET to be a standard MOS transistor with a pH sensitive oxide surface (SiO_2) that can be modeled as a capacitor.

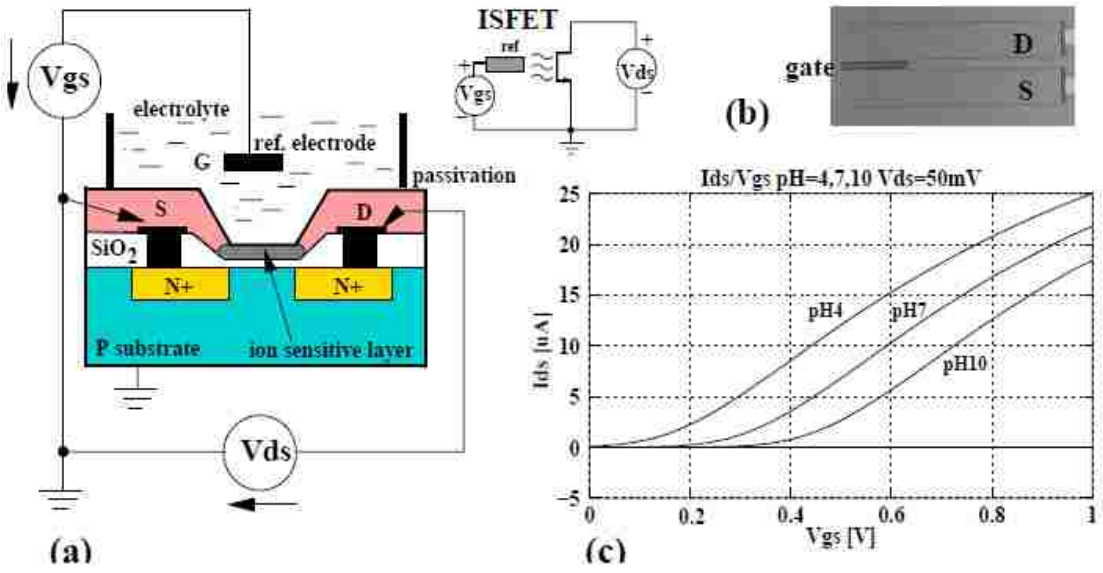

Figure 2.7: ISFET operation with transfer curve [32]

2.2.4 Sensing approaches of ISFET

ISFET can be used as an electro-chemical sensor that can directly produce electrical signal at sensor output. The electrical detection method of ISFET provides much simpler instrumentation, lower setup cost, easier and faster operation. This unique property of ISFET is the main reason for its huge popularity among researchers. Electrical detection method also ensures label-free detection approaches, avoidance of the influence of the label on the binding properties, and possibility of real-time monitoring of binding interactions. Moreover, semiconductor based ISFET sensors are compatible to standard scalable CMOS micro-fabrication. Therefore, ISFET sensors can be produced in large scale. They are also suitable for integration, and multiplex sensing.

The readout signal from ISFET sensor can be either the voltage or the current. The conventional approach is to read the voltage at the output of ISFET through pH-to-voltage conversion process as shown in Figure 2.9. In pH-to-Voltage conversion process, we force a small reference current through the channel and measure the voltage change at gate, due to ion-concentration change or chemical activity. As shown in [34], the threshold voltage of ISFET is linearly proportional to the pH of its sensing port. Therefore, ISFET sensor shows a linear response with pH change, when we use pH-to-Voltage conversion readout technique. However, it is desirable to measure and readout the threshold voltage of an ISFET at the weak inversion.

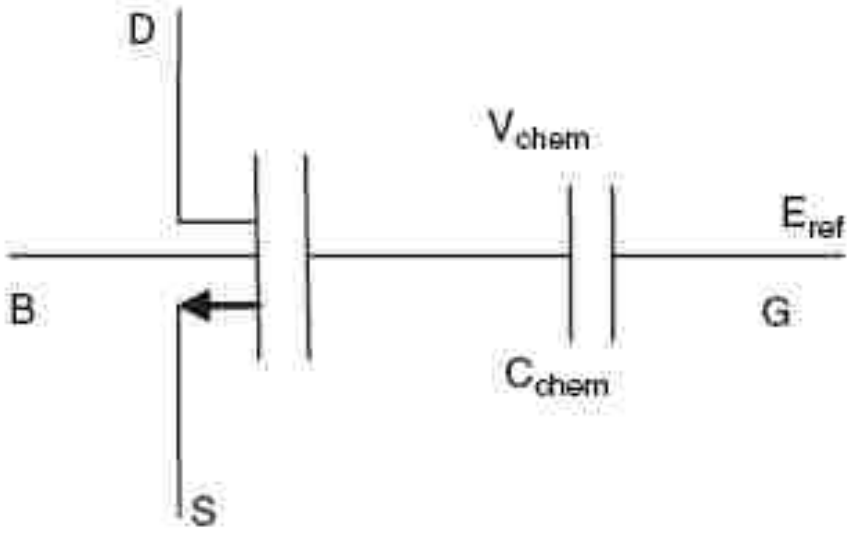

Figure 2.8 : ISFET model with respect to MOSFET [35]

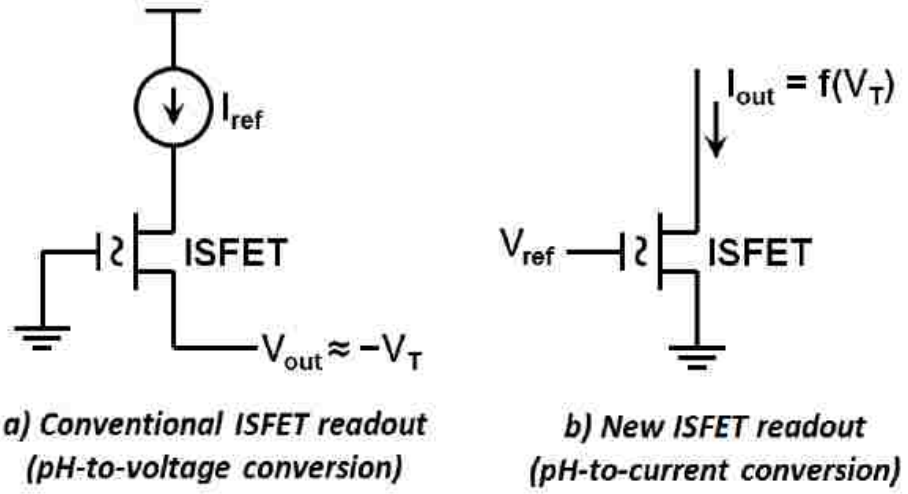

Figure 2.9: Sensing and readout principles of ISFET [18]

Our new proposed approach is to read current through a pH-to-current readout scheme shown in Figure 2.9. In this technique, we force a constant V_{ds} and measure the I_{ds} current for pH change at the gate. Although this new scheme does not provide a linear response to the pH, it allows the ISFET to operate in avalanche mode, which provides us with more sensitivity when gate signal is very weak [18]. High sensitivity of A-ISFET results from the avalanche multiplication arising from impact ionization of carries in depletion region of p-n junction when high reverse bias voltage is applied. We can address the non-linear response issue of A-ISFET through the proper calibration and lookup table as well as through post processing of the bulk data from DNA sequencing chip by complex digital signal processing algorithm.

2.2.5 CMOS compatibility of ISFET

The structure of ISFET is similar to that of MOSFET. Therefore, the fabrication of ISFET is compatible to standard CMOS process and it can be manufactured through economical scalable standard CMOS process. The gate of ISFET is made from chemical sensitive dielectric materials, which are SiO_2, Si_3N_4, Al_2O_3 or Ta_2O_5 etc. We generally select them based on their sensitivity, selectivity and long-term stability [26, 36, 37]. The standard CMOS process uses poly-silicon gate to define source and drain. Therefore, for fabricating ISFET many modified standard CMOS process is proposed [38, 39] with additional process steps. The extra

steps define the ISFET gate oxide region, formation of the gate oxide and pH sensitive insulator layers, and the formation of a window in the passivation layer to expose the ISFET sensor. When low cost fabrication is the focus, use of standard unmodified CMOS process for ISFET fabrication is the most desirable as they are the most economical option.

If an unmodified CMOS process is used to fabricate an ISFET, the poly-silicon layer must be left in the gate area for good source and drain definitions. This does not counteract the ISFET operation if an insulating pH-sensitive layer is used on top of the poly-silicon gate of standard CMOS process. Several pH-sensitive ISFET structures reported in literature [40, 41] use commercial CMOS process without any modification or post processing. In this research, our avalanche ISFET DNA sequencing chip went through standard CMOS process at TSMC and then was post-processed for well creation at MTTC of UNM.

2.2.6 ESD protection of ISFET

ISFET has very high input impedance, which makes it very sensitive to electrostatic discharge damage (ESD), similar to MOSFET. Diode networks that provide a lower impedance path between susceptible gates and the substrate can protect standard MOS devices. However, these protective networks are not available with normal ISFETs, since there is no gate conductive electrode in ISFET. There are two kind of electrostatic charge based damage in ISFET. The first type of ESD damage is destructive in nature and it damages the gate insulator. This damage of gate insulator is due to high electric field and it makes the ISFET inoperable.

The second type of ESD damage is non-destructive and it leads to a large change in threshold voltage of the device. This ESD problem of ISFET is highly reduced once the device is immersed in a solution; the conducting liquid takes away any static charge on the ISFET gate. Several ISFET electrostatic protection circuits can be found in literature consisting additional poly gate switch [42], using guard ring close to ISFET with diodes, a MOS transistor and a capacitor [43], or an ESD diode protection with the reference electrode [44] as shown in Figure 2.10.

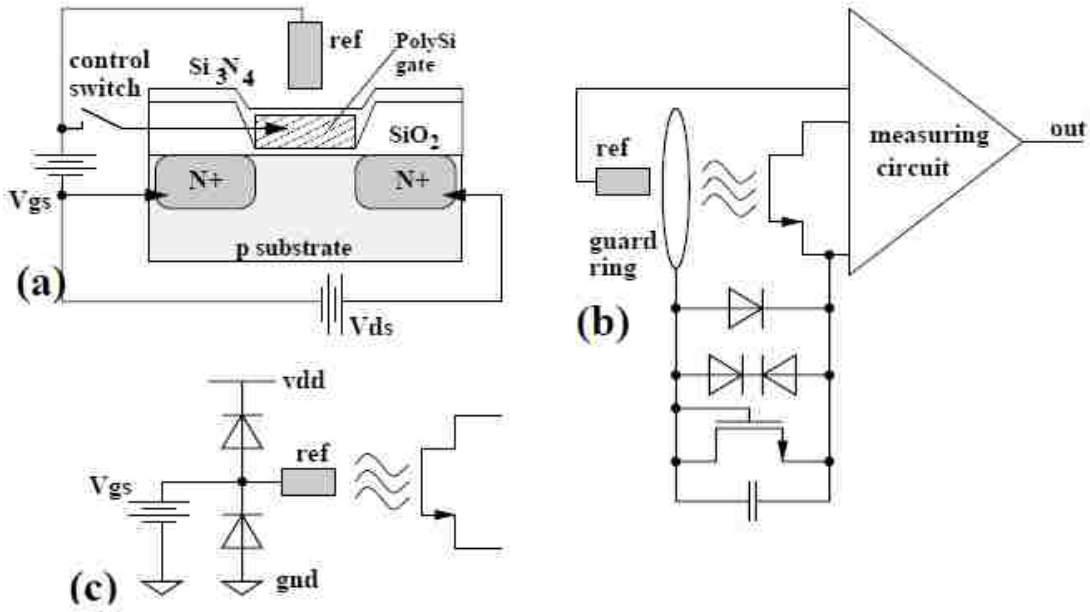

Figure 2.10: ESD protections of ISFET (a) Poly Si gate switching (b) Guard ring around ISFET gate with diode (c) Diode protection of reference electrode

2.2.7 Non-idealities of ISFET

The concept of ISFET is around 40 years old but practical applications are still emerging slowly, due to limiting factors arising from non-idealities associated with ISFET fabrication and operation. The non-idealities of ISFET can be divided into several categories, which are temperature dependence, light sensitivity and drift.

The temperature dependency of ISFET arises from the dependence of drain current on β and V_{th}. The term β is proportional to mobility of carriers in the channel whereas the mobility is an inverse function of the absolute temperature in Kelvin scale T. Therefore, ISFET has a negative temperature co-efficient from temperature dependency of β. Threshold voltage is another temperature dependent parameter of ISFET. Previously, we had seen that the threshold voltage of ISFET can be written as [26]-

$$V_{th} = V_{th(MOS)} + V_{chem} \quad , \tag{2.5}$$

where $V_{chem} = \gamma + 2.303\alpha U_T pH$, γ is a group of pH independent chemical potential, α is a dimensionless sensitivity parameter and U_T = kT/q is the thermal voltage i.e.

linear function of temperature. Therefore, we can see the threshold voltage of ISFET has positive temperature co-efficient. However, the temperature co-efficient of threshold voltage of MOSFET is negative. Therefore, this two forces work against each other and minimize the impact of temperature variation on threshold voltage of ISFET.

The light sensitivity of ISFET can be explained with that of MOSFET. Similar to MOSFET, there are two photosensitive regions in ISFET which are: reverse biased source and drain p-n junctions and ISFET channel from threshold voltage variation. Simulation results presented in [44] show that light has very minimal influence on ISFET channel and threshold voltage but parasitics reverse saturation current arising from drain-bulk and source-bulk, increases with optical radiation.

ISFET sensors are prone to drift, which is a temporal shift of the output voltage under constant conditions of temperature, pH value and buffer concentration [45]. Through drift, a sensor can show different behavior at different time and the output of sensor becomes unreliable. This drift effect of ISFET restrict its use in medical field as the accuracy required in biomedical pH sensor is very high i.e. at least 0.03pH within a measuring period of a number of hours. Reference [46] shows that an ISFET with Al_2O_3 membrane shows a drift of 0.06pH unit during first 4.5 hours and a maximum drift of 0.15pH in 24 hours.

2.3 Avalanche ISFET (A-ISFET)

The least explored region of operation for ISFET is the avalanche region. In this region, high velocity carriers are injected in the substrate of the ISFET where they are multiplied by impact ionization. This multiplication of carriers makes the device highly conductive and in a fraction of a nanosecond, a very high current start to flow. The large voltage drops across junction along with large current flow during avalanche can generate enough heat to make the ISFET device dysfunctional. However, an avalanche tolerant device can indefinitely sustain a moderate level of current while on the edge of breakdown. Generally, avalanche operation occurs when the reverse bias voltage of p-n junction approaches the breakdown voltage.

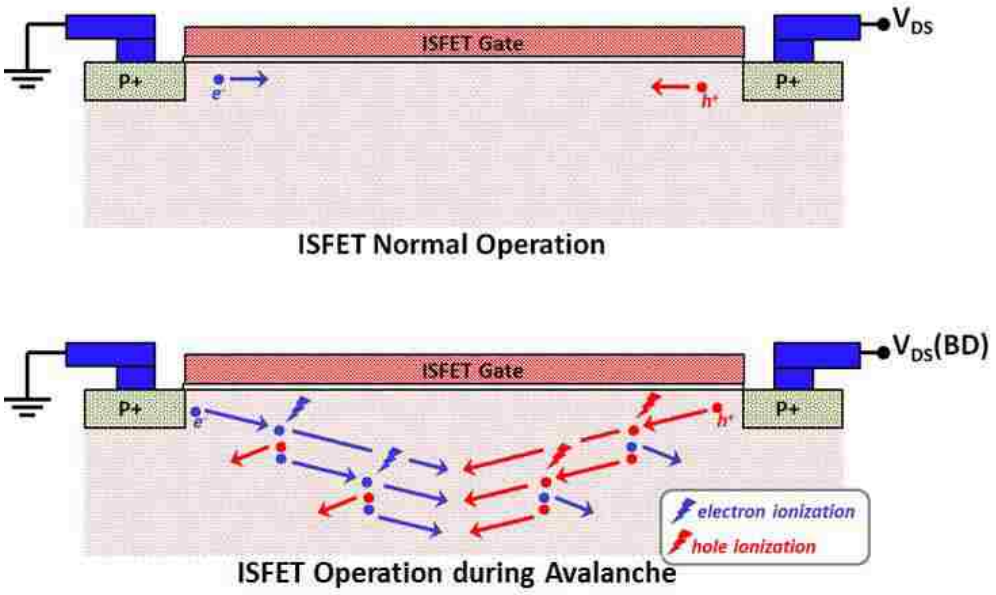

Figure 2.11: (a) An ISFET under nominal voltage (b) An ISFET under avalanche breakdown showing impact ionization. [18]

2.3.1 Structure and Bias of A-ISFET

The structure of an A-ISFET and the required bias for its avalanche operation is shown in Figure 2.11. A weak chemical signal in a normal ISFET can generate only few electrons or holes. On the other hand, in an avalanche ISFET (A-ISFET) the same weak signal results in a very large current due to carrier multiplication. The detailed phenomenon of avalanche is discussed in following section.

2.3.2 Physics of Avalanche operation

The conduction in any electronic materials results from the mobile charge carriers, which are free electrons and free holes. A fixed electron in a reverse-biased junction may break free due to its thermal energy, creating an electron-hole pair. If there is a voltage gradient in the semiconductor, the electron will move towards the positive voltage while the hole will move towards the negative voltage. However, when there is very high voltage gradient in p-n junction the free electrons move fast enough to knock a bound electron and make it free. Through this process, new

electron-hole pairs are generated. Similarly, fast moving holes can also create electron-hole pairs as shown in Figure 2.12 [47]. This secondary electron-hole pair may have high energy and can lead to collisions that can generate more electron-hole pair. This carrier creation through impact is known as carrier multiplication. Due to multiplication effect during avalanche, the current through junction increase abruptly. This abrupt increase of current through junction during avalanche might lead to device breakdown. In ISFET devices, the peak of carrier generation is commonly observed in channel near the drain area, as the depletion region width is highest there. Normally, avalanche breakdown is not desirable for electronic devices and must be avoided in order to prevent reliability issues. However, if it occurs under a controlled environment, avalanche multiplication can be extremely useful in achieving large internal gain [18].

2.3.3 Failure of A-ISFET

The main reason of A-ISFET failure is the thermal properties of silicon. If not controlled properly, during avalanche operation the junction temperature of ISFET may raise to a point, which may cause failure in metal contacts. This high operating temperature can lead to thermal destruction of the device. From reliability point of view, the operation of A-ISFET beyond rated junction temperature is not recommended.

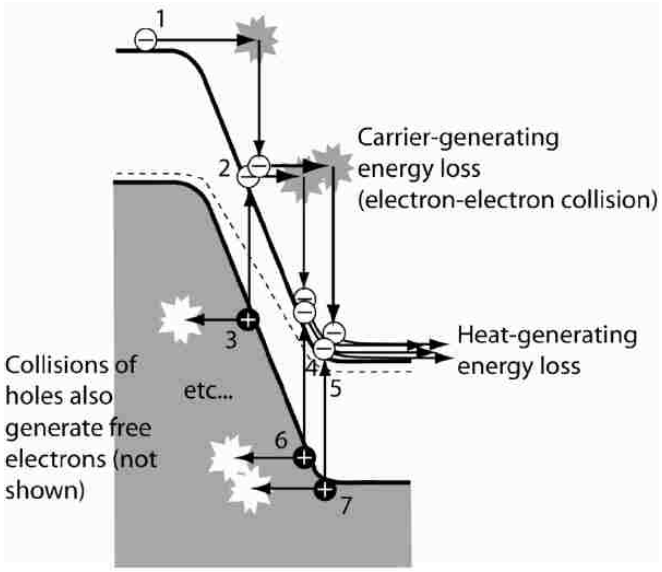

Figure 2.12: Avalanche Multiplication Process in Semiconductor [47]

Failure of A-ISFET from breakdown of the gate oxide can also be a concern as the gate-oxide is scaled down with the scaling of the CMOS process. Higher fields in the oxide increase the tunneling of carriers from the channel into the oxide. These carriers slowly degrade the quality of the oxide and lead them to failure over time. Use of high-k dielectric materials, allow us to have thicker oxide layer and to avoid oxide degradation from tunneling of carriers.

2.4 ISFET Sensor: Sensitivity

From earlier discussion, we can say that the current through drain-source of ISFET can be modeled with that of MOSFET. Similar to MOSFET, the drain-source current of ISFET strongly depends on the V_{GS} and V_{DS} bias voltages. The operating region of ISFET, based on the magnitude of bias voltages, can be differentiated into three regions, which are: i) Cut-off ii) Linear and iii) Saturation.

The following section will discuss on the ISFET operation and sensitivity at different operating region. We can define the sensitivity of an ISFET (S_{ISFET}) as the change of ISFET current due to the change of gate liquid pH i.e. ISFET ability to detect pH change [13]. It can be quantified as below -

$$S_{ISFET} = \frac{\Delta I_{DS}}{\Delta pH} = \frac{\Delta V_{GS}}{\Delta pH} . \frac{\Delta I_{DS}}{\Delta V_{GS}} = \left(\frac{\Delta V_{GS}}{\Delta pH} \right) g_m . \tag{2.6}$$

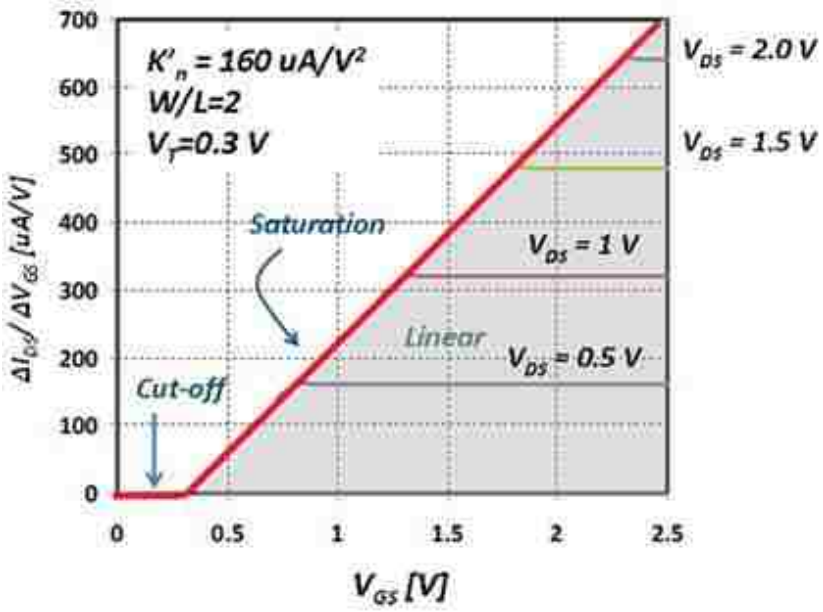

Figure 2.13: Voltage-to-current sensitivity of an ideal ISFET [13]

2.4.1 Normal Operation Mode

An ISFET operates in cutoff region when $V_{GS}<V_T$. At cutoff region of operation, both the current and change of current for ISFET is zero. Hence, this region is not suitable for operation of ISFET as sensor.

On the other hand, linear operating region of ISFET is dictated by the bias conditions $V_{DS} <V_{GS}-V_T$ and $V_{GS}>V_T$. At linear operating region, the current and change of ISFET current ($\Delta I_{DS}/\Delta V_{GS}$) can then be modeled as-

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right] = K_{n'}\frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{1}{2}V_{DS}^2\right], \quad (2.7)$$

$$\text{and } \left|\frac{dI_{DS}}{dV_{GS}}\right| = \left|\frac{dI_{DS}}{dV_T}\right| = \mu_n C_{ox}\frac{W}{L}V_{DS} = K_{n'}\frac{W}{L}V_{DS} \quad , \quad (2.8)$$

where μ_n is the mobility of electron, C_{ox} is the capacitance per unit area of the gate insulator, V_{DS} is drain to source bias voltage of ISFET, W is the channel width, L is the channel length and $K_{n'}$ is the current driving capacity of an ISFET.

Based on (2.8), we can say that the change of ISFET current at linear region is a linear function of the voltage of V_{DS} but it is independent of V_{GS} and V_T voltages.

However, at saturation region, dictated by bias conditions $V_{DS} => V_{GS}$- V_T and $V_{GS} > V_T$, ISFET current and change of ISFET current ($\Delta I_{DS}/\Delta V_{GS}$) can be modeled by:

$$I_{DS} = \mu_n C_{ox} \frac{W}{2L}[(V_{GS} - V_T)]^2 = K_{n'} \frac{W}{2L}[(V_{GS} - V_T)]^2 \quad (2.9)$$

,

$$\text{and } \left|\frac{dI_{DS}}{dV_{GS}}\right| = \left|\frac{dI_{DS}}{dV_T}\right| = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T) = K_{n'} \frac{W}{L}(V_{GS} - V_T) \quad (2.10)$$

.

Equation (2.10) shows that at saturation region the change of ISFET current is independent of the voltage of V_{GS} but it is linearly dependent on V_{GS} and V_T voltages. We can also see from (2.8) and (2.10) that the effect of threshold voltage change (i.e. pH change) on ISFET current is same as of V_{GS} voltage change.

If we use Ta_2O_5 as interface material in ISFET gate, we can achieve a threshold voltage change of around 60mV for every unit of pH change [34]. Therefore, the sensitivity variation of ideal ISFET with pH change will become as shown in Figure 2.14. We can achieve a sensitivity of around 35uA/pH for this ideal ISFET with W/L=2, V_T=0.3 V and $K_{n'}$=160uA/V^2. However, the sensitivity from a non-ideal, real ISFET is normally lower than that is shown in Figure 2.14.

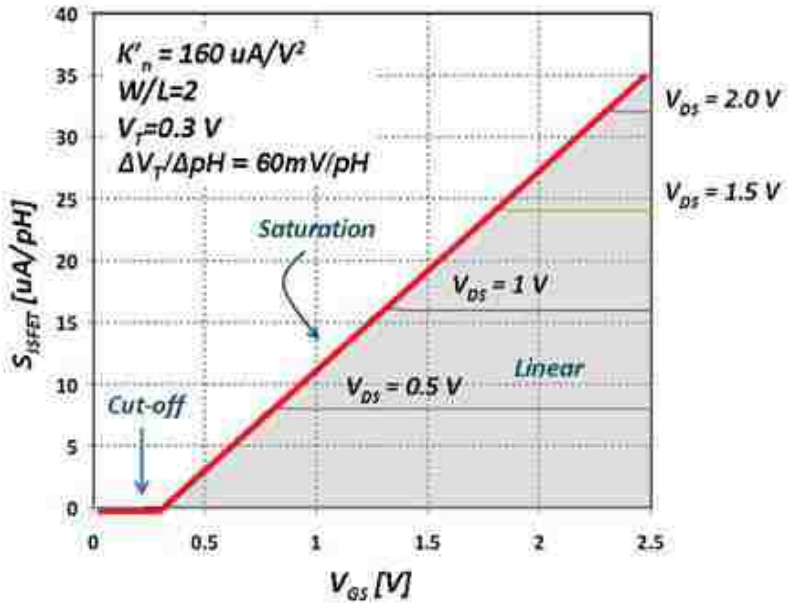

Figure 2.14: pH-to-current sensitivity of an ideal ISFET [13]

We have simulated an N-ISFET device with W/L=2 in SPICE to see its sensitivity variation with bias using TSMC's 0.25um technology model files. The sensitivity response of the short and long channel ISFETs are shown in Figure 2.15 and Figure 2.16 respectively. The sensitivity variation of long channel ISFET at saturation region follows the ideal ISFET sensitivity variation in Figure 2.14. However, the sensitivity of short channel ISFET degrades with the increase of V_{DS} voltage and it becomes saturated due drain-induced barrier lowering (DIBL) and channel length modulation effects. At high V_{GS} voltage, the sensitivity goes down due to mobility degradation of carrier in channel from carrier crowding.

The short channel effects in ISFET are due to two physical phenomena, which are: i) carrier drift characteristics in channel and ii) modification of threshold voltage. Different short channel effects in sub-micron ISFET are drain-induced barrier lowering (DIBL), channel length modulation, mobility degradation, punch-through, surface scattering, velocity saturation, impact ionization, hot electrons etc. We will discuss pros and cons of bias points A, B, C and D in Figure 2.15, below.

Bias point A: At this bias point ISFET operates in cut-off/sub-threshold region of operation. The sensitivity from ISFET in this point is quite low. But the power consumption at this point is also very low. Therefore, this point is suitable for low power applications where higher sensitivity is not an issue.

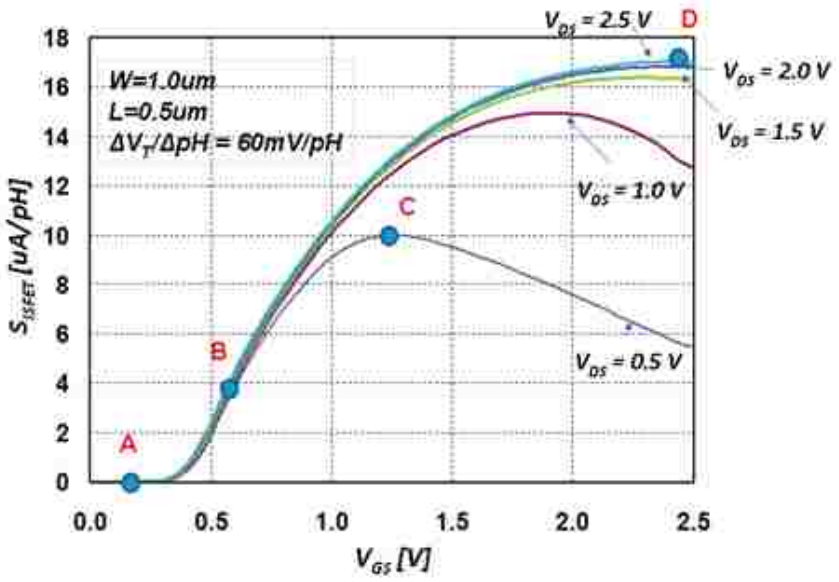

Figure 2.15: Sensitivity of a short channel ISFET with W/L=2.[13]

Bias point B: Here ISFET operates in saturation region of operation and the non-idealities due short channel effects did not take into effect. The sensitivity of ISFET around this region is a linear function of V_{GS} and hence sensitivity increases around bias point B as V_{GS} increases.

Bias point C: This point shows a local maximum of ISFET sensitivity. Beyond this bias point, the sensitivity degrades due to mobility degradation of carrier from short channel effects. We can bias ISFET to this sensitivity by applying V_{DS}= *0.5 V and* V_{GS}= *1.25V*. The pH-to-current sensitivity at point C is near 10uA/pH. This bias point gives us both high sensitivity and low power operation.

Bias point D: As we keep increasing of the voltage of V_{GS} and voltage of V_{DS}, ISFET enters into the region where short channel effects i.e. Mobility degradation, DIBL etc. becomes so significant that the sensitivity of ISFET becomes saturated or degraded. For the given TSMC's 0.25um technology node - this bias point gives us maximum sensitivity from ISFET sensor at a price of high power consumption.

Therefore, for low power operation with high sensitivity, we should operate ISFET sensor at point C with optimum voltage of V_{GS} and V_{DS}. But for application that requires higher sensitivity we have to operate ISFET at bias point D where both V_{DS} and V_{GS} are close to maximum for a given technology node.

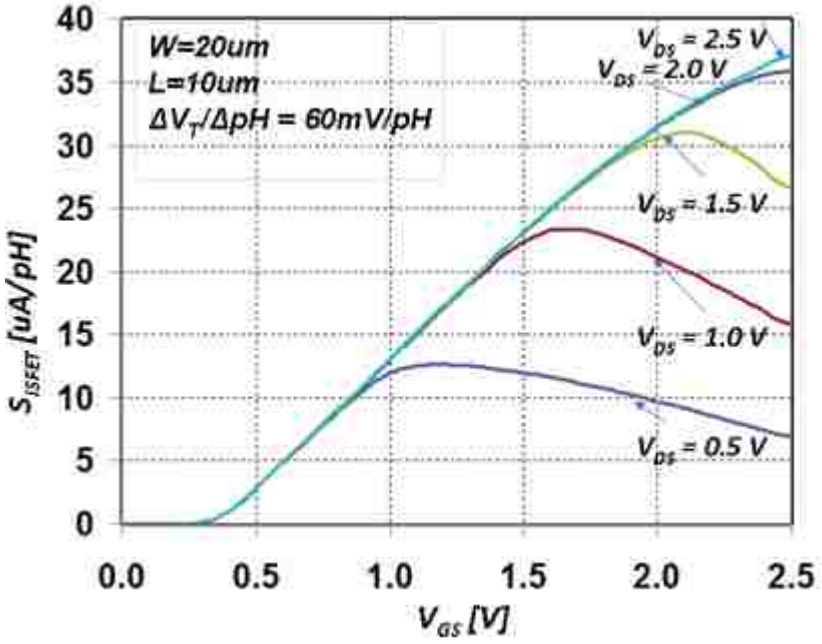

Figure 2.16: Sensitivity of a long Channel ISFET with W/L=2.[13]

2.4.2 Sensitivity of ISFET at Avalanche Mode

The electric field in FET transistor operating in saturation region, near the drain region increases significantly and causes impact ionization if we increase the drain-source bias voltage close to the breakdown voltage of the p-n junction, as shown in Figure 2.17. During avalanche region of operation, a large current originates due to impact ionization and carrier multiplication. For a n-ISFET transistor operated in saturation mode, if the generated current due to electron in channel is I_{DSsat} and we assume the ionization rates for electron and hole are equal, then current in avalanche mode can be given as [48] by-

$$I_{DS} = MI_{DSsat}, \tag{2.11}$$

$$I_{sub} = (M-1)I_{DSsat}. \tag{2.12}$$

Therefore, the sensitivity of A-ISFET is $\frac{dI_{DS}}{dV_{th}} = M\mu_n C_{ox}\frac{W}{L}\left(V_{gs}-V_{th}\right)$, which is M time higher than that in normal saturation region. Where M is avalanche multiplication factor, defined as [48]-

$$M = \left(1-\int_0^{ld}\alpha dy\right)^{-1}, \tag{2.13}$$

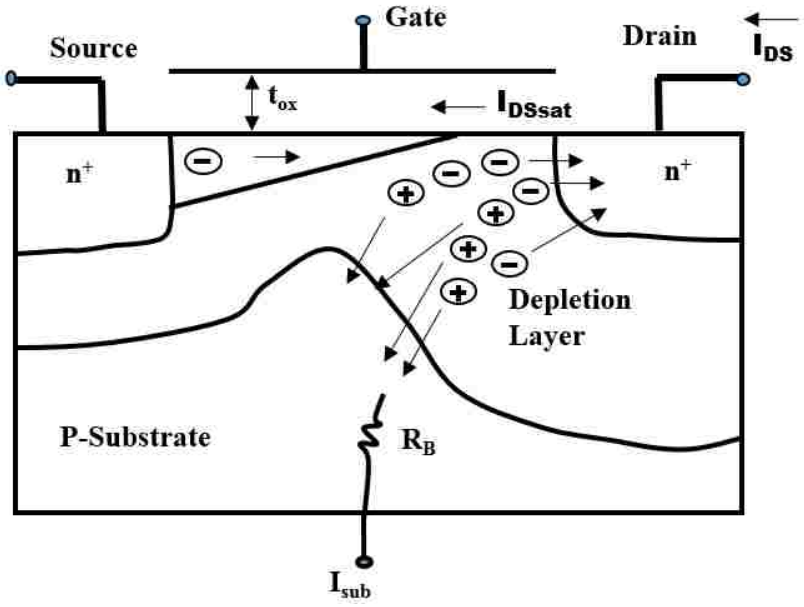

Figure 2.17: Current flow in n-channel MOSFET at avalanche [48].

Here, α is the impact ionization rate and can be approximated by $\alpha = A\exp(-B/E)$ where E is the electric field, A and B are the ionization constants, and ld is the width of the high field region where the avalanche multiplication occurs and is approximated by the empirical equation given by [49] –

$$ld = 0.22 t_{ox}^{1/3} x_j^{1/2} \quad . \tag{2.14}$$

The nominal power supply voltage of the devices manufactured by the TSMC's 0.25um CMOS process is 2.5V. Therefore, the nominal operating voltage of our ISFET chip is 2.5V. Our initial SPICE simulation result for the ISFET is shown in Figure 2.18, where the drain-source voltage goes beyond the normal operation of the device. As shown in this figure 2.18, for the same gate voltage, the device carries a much larger current when operating at close to the breakdown point than the current at the nominal voltage of 2.5V. For example, the same gate charge that can create 7.9uA of current at V_{DS}=2.5V, can create 68uA of current at V_{DS}=6.0V. This ~10X improvement in current and sensitivity is the basis for our new highly sensitive A-ISFET based sensing technology.

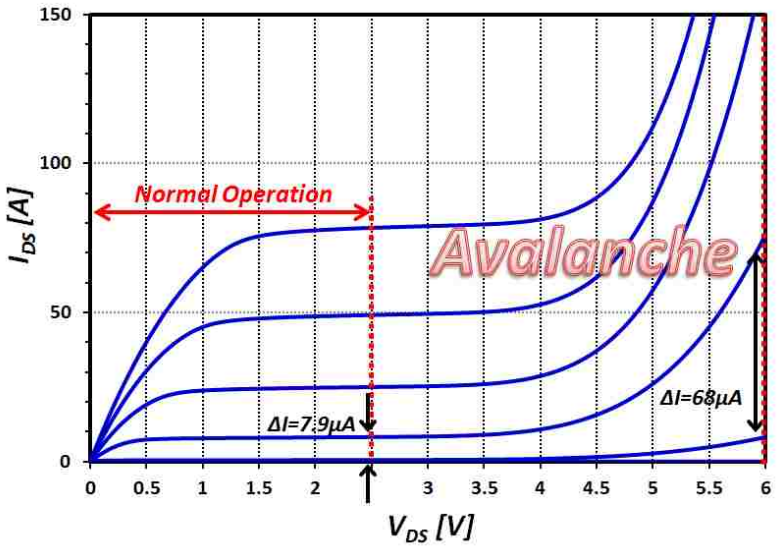

Figure 2.18: SPICE simulation showing (~10 times) higher sensitivity from ISFET device [18].

2.5 Discussions

In this chapter, we have discussed on theory and background of AISFET to have an overall idea on its structure and operation. Our mathematical analysis on ISFET had shown that for short channel ISFET the trend of transconductance is highly deviated from the transconductance trend of long channel ISFET. The analysis also shows that transconductance degrades significantly, as the devices are scaled down. However, the sensitivity of ISFET sensor is directly proportional to its transconductance; therefore, the degradation of device transconductance with scaling is a challenge for large-scale ISFET sensor array.

CHAPTER 3
NOISE ANALYSIS OF A-ISFET

3.1 Introduction to Noise

Noise is a random process. It limits the minimum signal level that a circuit can process with acceptable quality [50]. For electronic systems, especially for sensors, noise is a fundamental issue as it determines the resolution of the signal. For an example, when we are doing wireless communications, the signal is always affected by noise; the receiver must cope with and overcome noisy signals to operate properly.

The source of this noise can be classified into two categories. One is artificial external noise created by numerous noise sources from the environment, AC power lines or mechanical vibrations. Unwanted noise may enter the system together with our signal information. The effect from artificial noise can be reduced by choosing a less noisy environment or strengthen the signal power, thereby improving the signal-to-noise ratio, [51].

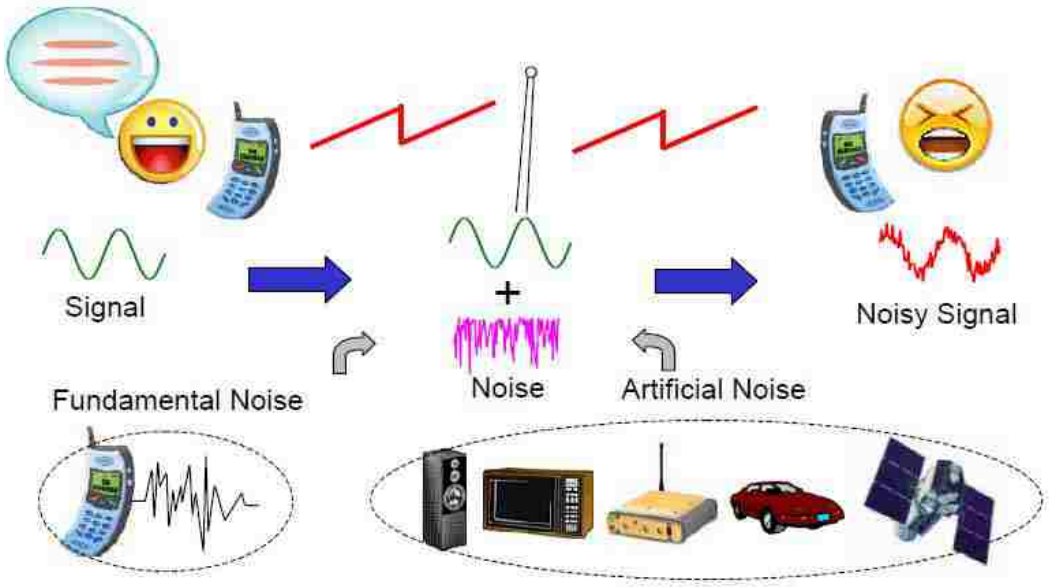

Figure 3.1: Different noise sources and their effect on signal [51]

The other sources of noise in sensor is its own intrinsic noise including induced noise from other devices operating on the same chip. The digitization and processing algorithm of signal also creates noise. These are the fundamental noises, which are created by circuits and devices. Once the design and fabrication is done, the amount of intrinsic device noise becomes fixed. Accurate modeling of noise sources in device can help us to understand the noise sources better and to optimize the design of the device with minimum noise.

Due to the randomness of noise, we need to use statistical approaches for its characterization. Generally, the average of noise current is zero; hence, the power spectral density of noise per unit frequency is used for the expression of noise. External noise sources can be removed; however, internal noise sources cannot be eliminated. It can only be minimized through careful design and operation, to improve the sensor performance.

3.2 Noise in ISFET

We have seen that an ISFET is similar to MOSFET in structural point of view. It is a voltage-controlled resistor. Therefore, thermal noise, which results from random potential fluctuations in the channel [52], in addition to other noise sources, is present in ISFET.

When we use ISFET as pH sensor, theoretically the maximum sensitivity is only 60mV/pH as dictated by Nernst equation [13]. If the noise contributions from the internal noise sources are comparable to signal generated from pH change, we cannot use sensor for our measurements. The sensor is limited by limit of detection level. Therefore, it is essential to have a better understanding of the different noise components and their mechanisms, to reduce the internal noise. Figure 3.2, shows typical spectrum of different noise component when ISFET operates at normal operating region.

In this section, different internal noise sources of ISFET are identified and modeled. The noise sources are thermal noise, flicker noise, dark current noise, shot noise and excess noise from avalanche mode of operation. The total noise of the sensor is the sum of all of the above noise components.

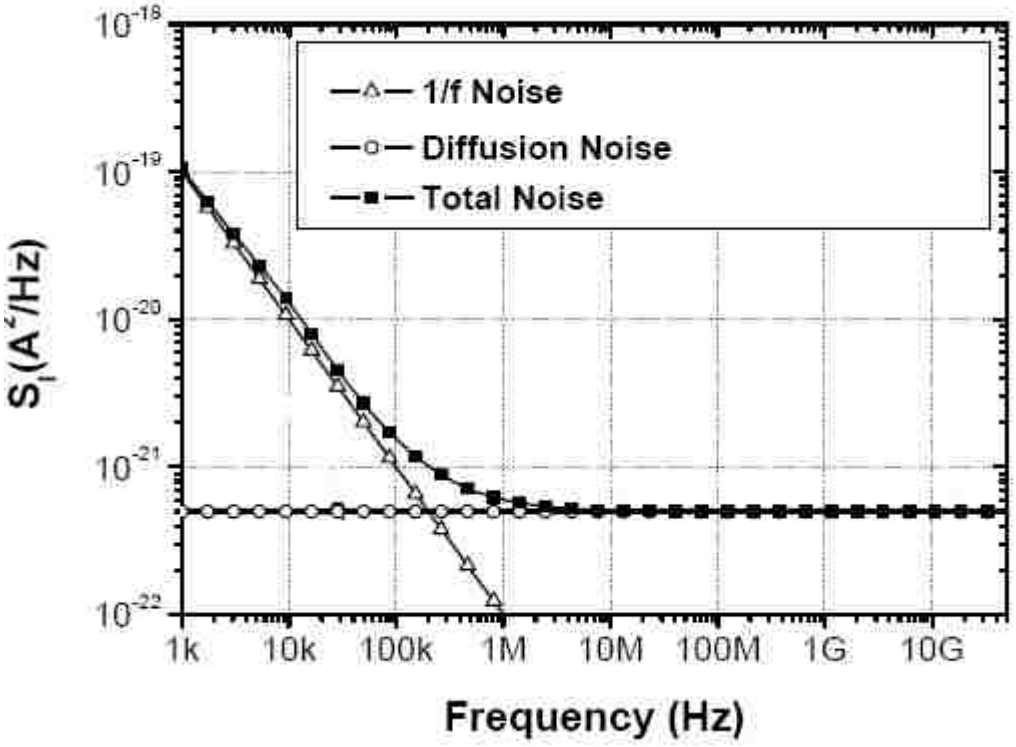

Figure 3.2: Noise spectrum of MOSFET/ISFET [51]

3.2.1 Thermal Noise/Diffusion Noise

A MOS device is a four-terminal voltage-controlled resistor; the terminals are source, drain, gate, and substrate. The voltage-controlled resistor is the FET channel connecting the source and the drain, and is controlled by a voltage applied from the gate. Thermal noise is caused by thermodynamic fluctuations of charge carriers in a material as pointed out by Nyquist [53].

A resistor with resistance R at non-zero temperature generates a thermal noise, regardless of source-drain voltage magnitude. The power spectral density (PSD) of this thermal noise in a resistance is well known by following voltage equation [50]:

$$e_n^2 = 4k_B RT\Delta f \ , \tag{3.1}$$

where k_B is the Boltzmann constant, R is the total amount of the resistance, Δf is the bandwidth, and T is the temperature of the semiconductor device. As shown in (3.1), the power spectral density of thermal noise is independent of frequency and linearly

proportional to resistance and temperature. This frequency independent property makes thermal noise a dominant noise source for high frequency RF applications. The thermal noise in the channel of ISFET in strong inversion can be modeled as [54]:

$$I_{n,t}^2 = 4k_B T g_m \gamma \ , \tag{3.2}$$

which can be modeled as gate referred voltage to be as:

$$V_{n,t}^2 = \frac{4k_B T \gamma}{g_m}, \tag{3.3}$$

where g_m is the small-signal trans-conductance at the bias of ISFET.

The conductance of the channel under the gate of A-ISFET during avalanche operation is fairly constant [48], and hence we can assume that the thermal noise is same as of the saturation / strong inversion region, during avalanche operation.

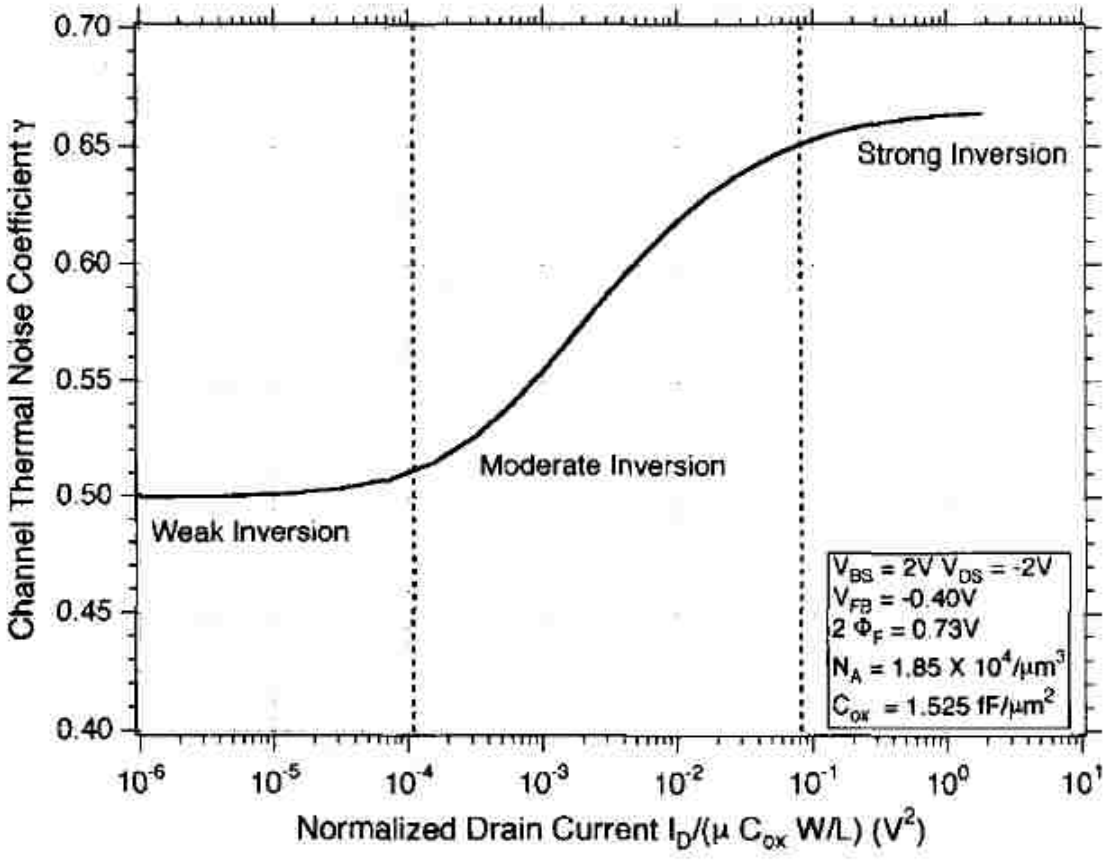

Figure 3.3: Noise coefficient γ in saturation as a function of normalized drain current. Regions of weak, moderate and strong inversion are indicated. [55]

3.2.2 Flicker Noise

Flicker noise is low-frequency noise that occurs when a direct current is flowing. Therefore, flicker noise can be regarded as being produced by a fluctuation in conductance of the channel under gate**.** Flicker noise is also known as pink noise or 1/*f* noise because its Power Spectral Density (PSD) is inversely proportional to frequency [56]. Flicker noise of a MOS transistor is assumed to originate from interfacial oxide traps. At the interface between oxide and silicon, many dangling bonds create traps. These interfacial oxide traps randomly trap and release charge in the channel.

PMOS transistors generate less flicker noise than NMOS transistors because the buried channel in PMOS transistors maintain some distance from interfacial traps [51] as shown in Figure 3.4. Flicker noise does not strongly depend on temperature. However, with scaling of device dimension flicker noise increases. A very common technique to reduce flicker noise is to increase device dimensions. Therefore, transistors for low noise applications have large gate area to suppress 1/f noise. However, this technique costs large parasitic capacitances and die area.

A typical 1/f noise model of a MOS transistor has following form (input gate referred noise).

$$V_{n,1/f}^2 = \frac{k_f}{C_{ox}WLf} \quad , \tag{3.4}$$

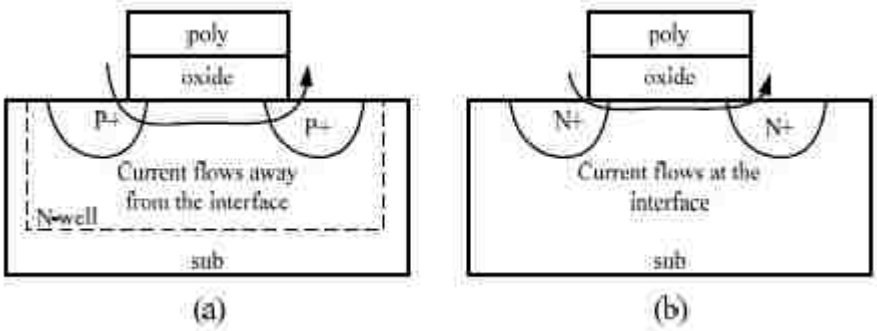

Figure 3.4: Buried channel and flicker noise: manufacturing technique to reduce flicker noise. a) buried channel: low Flicker noise b) Standard process : high flicker noise [51]

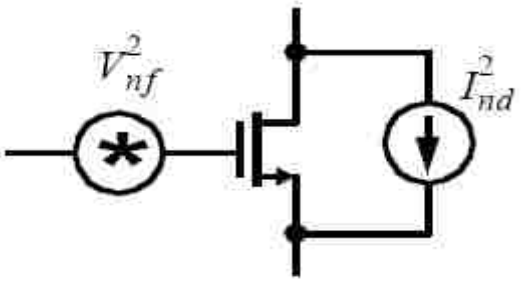

Figure 3.5: Thermal noise and Flicker noise of MOSFET [50]

where k_f is device dependent parameter, W and L are device dimensions, C_{ox} is the oxide capacitance per unit area and f is the operating frequency. Therefore, channel referred flicker noise current can be modeled as:

$$I_{n,i/f} = \frac{k_f g_m^2}{C_{ox} WLf} \ . \tag{3.5}$$

As the conductance in channel of ISFET remains same during avalanche, hence the flicker noise at avalanche could be model as that of ISFET in normal operation. Figure 3.5 shows, the channel thermal noise and gate referred flicker noise of an A-ISFET/ MOSFET.

3.2.3 Shot Noise

Shot noise is produced when charge carriers cross a potential barrier such as Schottky barriers or p-n junctions at random. The spectral density of the shot noise associated with a junction current, I_{ds} can be given by Schottky formula [57]:

$$I_{n,s}^2 = 2qI_{ds}, \tag{3.6}$$

where q is the electronic charge and I_{ds} is the dc current through junction.

Shot noise is white in nature, when ISFET operate with nominal voltage. However, this DC current is multiplied by avalanche multiplication factor, when ISFET operates in avalanche region.

During avalanche mode of operation, shot noise due to dc bias of A-ISFET can be modeled as [58]:

$$I_{n,shotDC}^2 = 2qI_{ds}B(M-1)^2F(M)\,, \tag{3.7}$$

where, q is the electron charge, I_{ds} is the saturation current of the A-ISFET, B is the bandwidth, M is the multiplication factor for avalanche, F is the excess noise factor

3.2.4 Dark Current Noise

This current is flowing through reverse biased p-n junction, when there is no chemical on the gate of the ISFET while it is operating in normal bias at saturation. At the given condition, the current through p-n junction is essentially the reverse saturation current. However, when this small reverse saturation current flows across a strong reverse biased p-n junction, we experience avalanche impact there. Due to avalanche impact and associated excess noise factor, the dark current noise can be quantified as [57,58]:

$$I_{n,darkc}^2 = 2qBI_{rev,sat}M^2F(M)\,, \tag{3.8}$$

where q is the charge of electron, B is the bandwidth, $I_{rev,sat}$ is the reverse saturation current, M is the Multiplication factor due to avalanche impact, and F is the excess noise factor due to avalanche and multiplication.

3.2.5 Avalanche Noise

Avalanche noise in semiconductor devices is associated with reverse-biased junctions. For large reverse junction voltages, the leakage current can be multiplied by the avalanche phenomenon. Carriers in the junctions gain energies in a high electrical field and then they collide with the crystal lattice. If the energy gained between collisions is large enough, then during collision another pair of carriers can be generated. This way the reverse biased current is multiplied. This is a random process and obviously, the noise source is associated with the avalanche carrier generation. The intensity of the avalanche noise is usually much larger than any other noise component. Fortunately, in case of A-ISFET, the avalanche noise exists only in the p-n junction biased with a voltage close to the breakdown voltage.

3.3 Signal-to-Noise ratio (SNR) of A-ISFET

A weak chemical signal in a normal ISFET can generate only few electrons (and holes), which results in a very-low current comparable to the device noise [18]. We can overcome this problem by operating the ISFET in avalanche region as A-ISFET. However, as we operate the device in avalanche region several non-idealities and noise sources come into play. During avalanche operation the signal power and noise power of A-ISFET becomes a function of multiplication factor, excess noise factor, temperature, load resistance, dark current, and DC bias current. In previous section, we have discussed on different noise sources in A-ISFET. Before we do the analytical formulation of signal-to-noise ratio (SNR) equation, we need to get familiar with few of the terms/concepts that are associated with avalanche operation.

3.3.1 Multiplication Factor, *M*

Avalanche multiplication is the key parameter that defines the current flow in avalanche. This multiplication comes into play from the width of depletion region and the impact ionization events in ISFET. The multiplication factor *M,* increases as the reverse bias voltage V applied to reverse bias p-n junction of ISFET approaches the junction breakdown voltage, V_b [59]:

$$M = \frac{1}{(1-(\frac{V}{V_b})^n)} \quad , \tag{3.9}$$

where n is the ideality factor of the junction.

3.3.2 Excess Noise Factor, F

All avalanche operation generates excess noise due to the statistical nature of the avalanche process. The Excess Noise Factor is generally denoted by F. It is a function of the carrier ionization ratio, k, where k is usually defined as the ratio of hole to electron ionization probabilities (k < 1). The excess noise factor can be calculated using the model developed by McIntyre, which considers the statistical nature of avalanche multiplication. The excess noise factor can be modeled as in [58]:

$$F = k_{eff} M + (1 - k_{eff})(2 - \frac{1}{M}) \ . \qquad (3.10)$$

Therefore, the lower the values of k and M, the lower the excess noise factor, F.

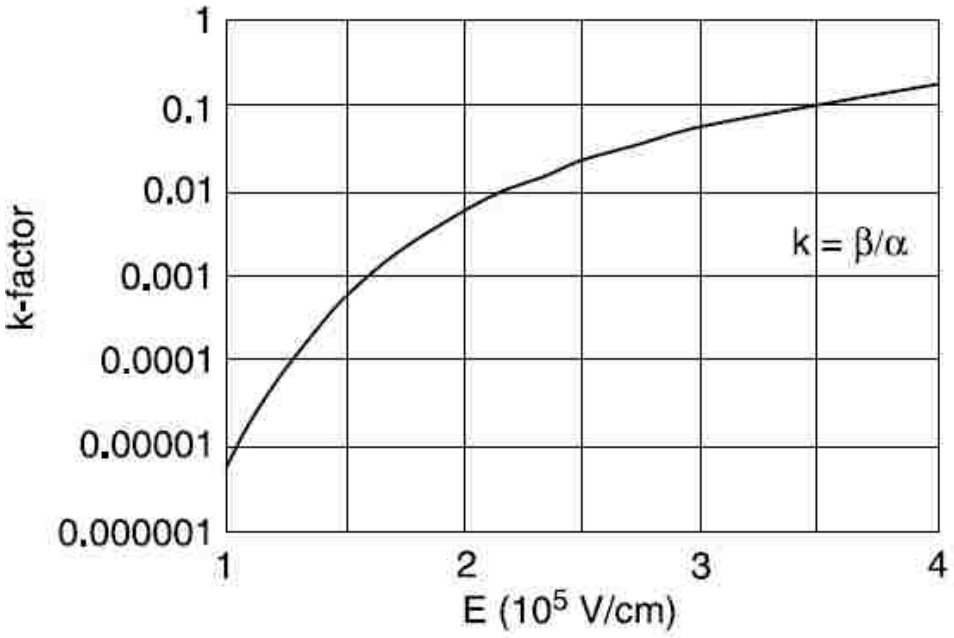

Figure 3.6: Ionization factor, k as function of electric field, during avalanche [60]

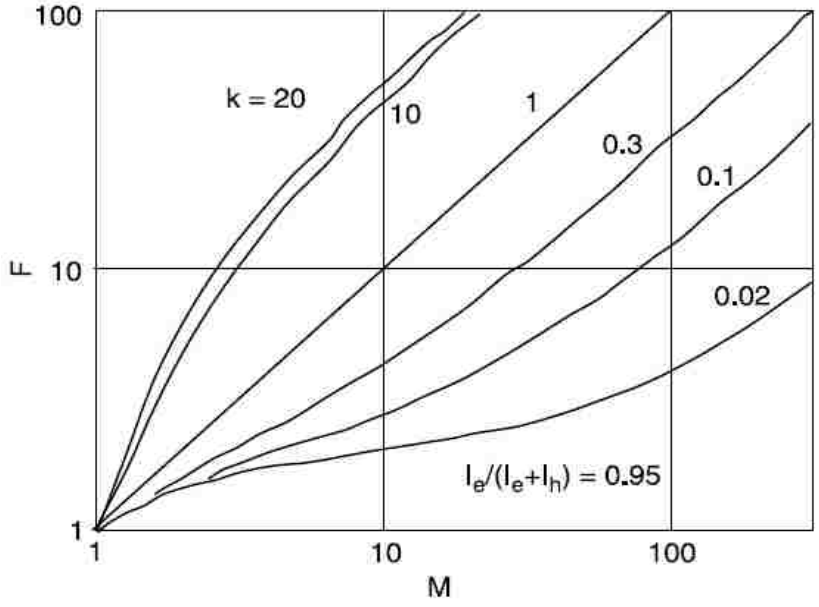

Figure 3.7: Excess noise factor as function of k and M with given electron injection ration of Ie/(Ie+Ih)=0.95 [60]

The ionization ratio k is a strong function of the electric field across ISFET structure. Since the electric field profile depends upon the doping profile, the k factor is also a function of the doping profile. An avalanche phenomenon takes place if the electric field strength in a p-n junction is higher than strength of so-called critical field at which impact ionization of carriers occurs. The electric field in a silicon p-n junction for avalanche operation ranges from 2 to $5*10^5$ V/cm and cannot exceed the value of 10^6 V/cm at which the Zener effect happens [60].

The impact ionization effect is characterized by the ionization coefficient of the average number of electron-hole pairs created by one charge carrier (electron or hole) per unit of distance (cm), during its transit in the high electric field. For most semiconductor materials (except germanium), ionization coefficients for electrons α and for holes β differ. In Si, ionization coefficients for electrons α are much higher than ionization coefficients for holes β hence an avalanche multiplication factor M_e for electrons is higher, than for holes M_h. The dependence of β/α in silicon, often called k factor, on the electric field is presented in Figure 3.6. As the electric field increases, k factor increases too.

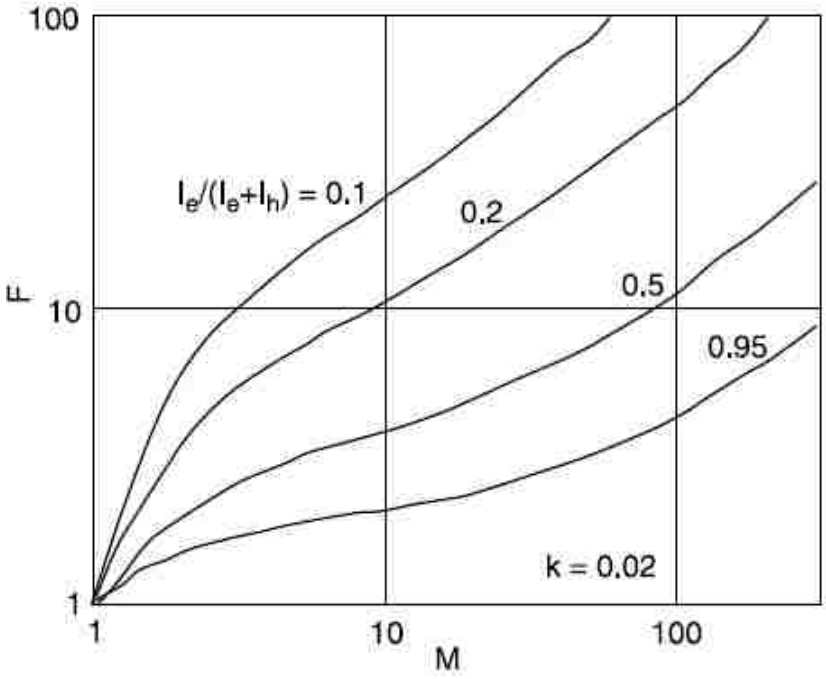

Figure 3.8: Dependence of noise factor, multiplication factor and electron injection ratio, when k=0.02 [60]

In Figure 3.7, we see the relation among multiplication factor, excess noise factor and ionization factor when electron ratio is 0.95. Here, we see that as multiplication factor increases, the excess noise factor also increases. However, with increased k factor, the increment in excess noise factor is gets larger. Figure 3.8 shows the relation among electron injection ratio, excess noise factor and avalanche multiplication factor when k=0.02 [60]. It shoes that as the electron injection ratio increases, excess noise factor decreases.

3.3.3 Model Formulation for SNR of A-ISFET

A) Simulation environment: Parameters values are -

Temperature	27 degree Celsius
Load Resistance	10k
Bandwidth	20 MHz
Small signal gate voltage	18uV

[N**ote:** gate voltage change of 59mV/pH (so small signal current is gm* v_{sig})]

DC bias current of A-ISFET @shot noise	0.25uA
Considered gm at Normal Operation	1.76mA/V
Gamma	2/3 at saturation
Dark Current	very negligible ~nA range

We are considering the current model used in reference [48] for avalanche model of A-ISFET.

B) Noise Components Considered:

1) Inversion Channel Thermal Noise at saturation. This noise is constant and has no avalanche effect [48].
2) Flicker noise in the channel under the gate oxide is also constant as the conductance and current is constant there during avalanche operation [48].

3) Dark current noise through reverse biased p-n junction can be considered to be the reverse saturation current of the p-n junction and it is very small. However, this small current has avalanche effect and hence excess noise factor is associated there.
4) Shot Noise due to DC bias of the reverse biased p-n junction is the most dominant noise component in A-ISFET as it has avalanche multiplication effect and hence excess noise factor is associated there.
5) Thermal Noise due to Load resistance is also very critical. We need to choose right load resistance to optimize the sensing of A-ISFET.

C) A-ISFET signal:

A-ISFET sensor takes a very small signal change at its input and converts it to a current proportional to trans-conductance at the given bias. From measurement of A-ISFET, we find that the trans-conductance at the given bias in avalanche is ~10mA/V. The increased value results from the avalanche multiplication factor resulting from the associated bias. Therefore, current read from A-ISFET sensor at normal operation is:

$$I_{sig} = g_m v_{sig}. \tag{3.11}$$

This current signal can be converted to equivalent power during avalanche with avalanche multiplication factor, M by the following equation:

$$I_{sig,ava}^2 = I_{sig}^2 . M^2, \tag{3.12}$$

where M is the avalanche multiplication factor.

D) A-ISFET Noise:

1) Inversion Channel thermal noise as Channel referred current noise:

$$I_{n,t}^2 = 4k_B T g_m \gamma, \tag{3.13}$$

where k_B is the Boltzmann constant, T is temperature in Kevin scale, g_m is the trans-conductance at avalanche operation and γ is the factor due to inversion. It has no avalanche impact, as conductance in inversion channel is constant.

2) Gate referred flicker noise can be given by:

$$V_{n,1/f}^2 = \frac{k_f}{C_{ox}WLf}, \tag{3.14}$$

which can be modified to channel referred current noise as:

$$I_{n,i/f} = \frac{k_f g_m^2}{C_{ox}WLf}, \tag{3.15}$$

where g_m is the transconductance at avalanche, k_f is the device noise parameter for flicker noise, C_{ox} is the oxide capacitance, f is the operating frequency, W and L are device dimensions. Flicker noise has no avalanche impact, as conductance in inversion channel is constant during avalanche operation of A-ISFET.

3) Dark current noise in p-n junction can be approximated as reverse saturation current of p-n junction, which is very small in value. However, due to strong reverse bias, there is avalanche impact and excess noise factor is there. Therefore, the A-ISFET noise from dark current can be modeled as:

$$I_{n,darkc}^2 = 2qBI_{rev,sat}M^2F(M), \tag{3.16}$$

where q is the charge of electron, B is the bandwidth, $I_{rev,sat}$ is the reverse saturation current, M is the Multiplication factor due to avalanche impact, and F is the excess noise factor due to avalanche and multiplication

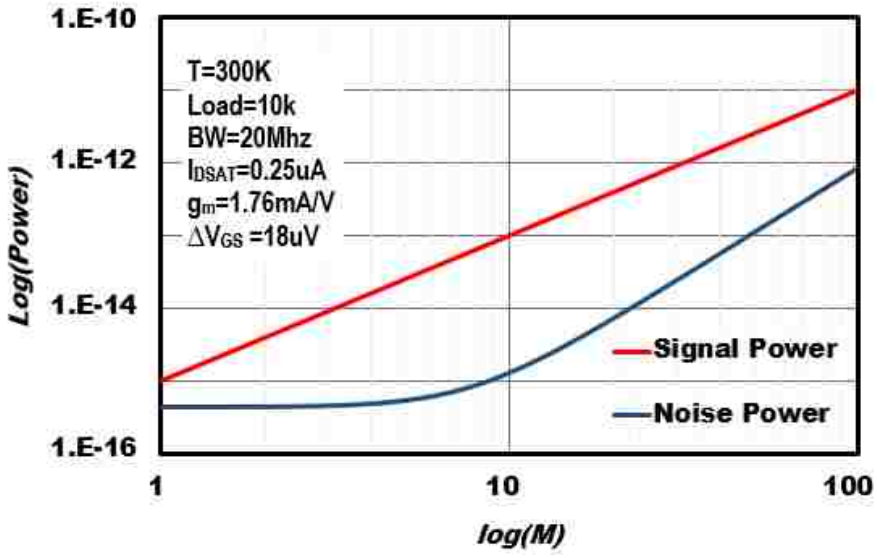

Figure 3.9. Signal power and noise power of A-ISFET as M increases

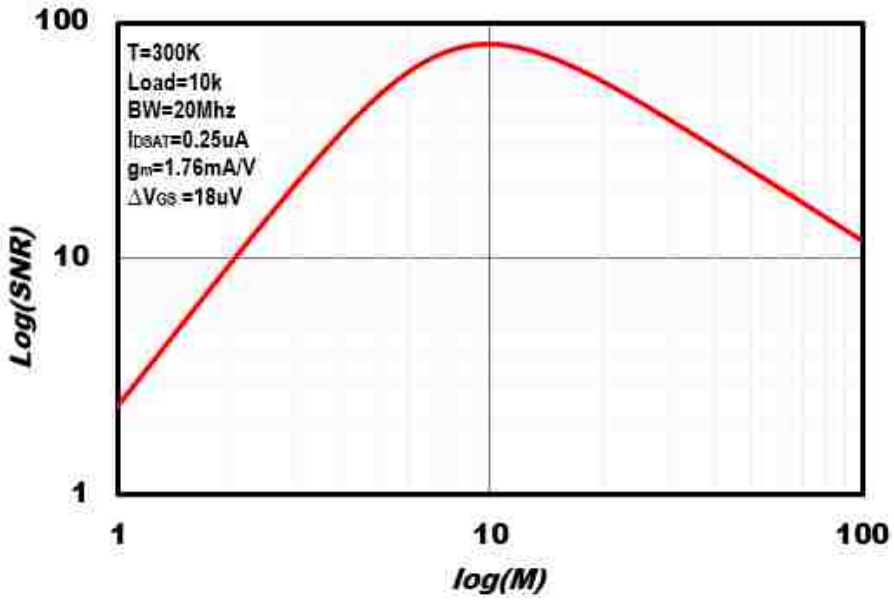

Figure 3.10: Signal-to-Noise ratio (SNR) of A-ISFET with Avalanche multiplication factor

4) Shot noise due to DC bias current of the A-ISFET is the most dominant noise component as avalanche impact and excess noise factor is associated with it. We are assuming DC bias current of 5uA for our simulation. Therefore, shot noise due to DC bias of A-ISFET can be modeled as:

$$I_{n,shotDC}^2 = 2qI_{ds}B(M-1)^2.F(M), \tag{3.17}$$

where q is the electron charge, I_{ds} is the saturation current of the A-ISFET, B is the bandwidth, M is the multiplication factor for avalanche, and F is the excess noise factor

5) We can model the thermal noise due to Load resistance as equivalent drain-source current by the following equation:

$$I_{n,Rl}^2 = 4k_BTB\frac{1}{R_L}\ , \tag{3.18}$$

where k_B is the Boltzmann constant, B is the Bandwidth, T is temperature in Kelvin scale, and R_L is the Load resistance of the sensor.

3.4 Simulation Results

Figure 3.9 illustrates the relation of signal power and noise power as the A-ISFET avalanche multiplication gain *M*, increases. It shows that after certain value of *M*, the increase in noise power is higher than that of the signal power. Therefore, there is an optimum value for *M*, where it maximizes the SNR as shown in Fig. 3.10.

The sensing quality of a sensor is directly related with its *SNR*. As the SNR of a sensor increases, the resulting error or noise in output decreases and the accuracy of the output data increases. Therefore, to ensure certain quality of sensing in a particular operation, we need to operate a sensor at least with a minimum specific SNR or allowable bit error rate (BER) in output. As an example, for PCIe 3.0 the specification for BER is 10^{-12}. However, with technology scaling, generally the signal power decreases and noise power increases. Therefore, *SNR* goes down with advancement of technology. We can conclude from Fig. 3.10 that we can derive an increased *SNR* from a scaled sensing device by operating the device with a higher multiplication factor, *M*.

In A-ISFET a change in pH of gate liquid, generates an equivalent change of threshold voltage i.e. which is equivalent to a change in gate voltage [13]. As the change in gate voltage due to pH change reduces, the output signal generated by A-ISFET sensor is also reduces. However, the generated noise from the sensor remains same. Therefore, we need to bias A-ISFET for higher *M* value to make the sensor functional by ensuring a specific level of SNR sensitivity, as shown in Fig. 3.11. As an example, for an application with required SNR of 10, we need to operate the A-ISFET sensor with M=2 for ΔV_{GS}=18uV and with M=3 for ΔV_{GS}=12uV. Whereas a ΔV_{GS}=6uV cannot achieve SNR of 10 due to overtaking of noise over power after certain value of *M*. However, if we can further reduce the noise from the sensor through careful design, fabrication, and operation, we can still use the sensor for sensing ΔV_{GS}=6uV with SNR 10.

The operating bandwidth of the sensor is also an important specification for proper operation of A-ISFET. Increasing the bandwidth increases the noise, if all other parameters are constant. The impact of bandwidth on SNR, is a contrasting scenario of Fig. 3.11. As bandwidth increases, the noise of A-ISFET sensor also increases while the signal remains the same. Therefore, we can see in Fig. 3.12, a trend of lower

SNR as operating bandwidth of A-ISFET increases. It also shows that for a given SNR, we need to operate the sensor in higher *M* factor if the operating bandwidth is higher. As an example, for an application with required SNR of 10, we need to operate the A-ISFET sensor with M=2 when operating frequency is 20 MHz and with M=5 during 100 MHz operating frequency. We can also see from Fig. 3.12 that as the operating frequency decreases, the SNR of A-ISFET sensor increases when the sensing device is biased for a particular *M* value.

From this analytical model of A-ISFET sensor, we can point out that as the reverse bias voltage increases and approaches the breakdown voltage of the junction, the multiplication factor, *M* of A-ISFET increases with bias change. However, an increased *M* results in an excess noise factor, *F* given by (10) which significantly increases the overall noise of A-ISFET after certain point. *F* is a function of ionization factor, *k.* Therefore, to minimize the excess noise impact, we need to minimize ionization factor, *k* and we also need to operate A-ISFET in avalanche, with a *M* value that ensure minimum SNR required for the given application.

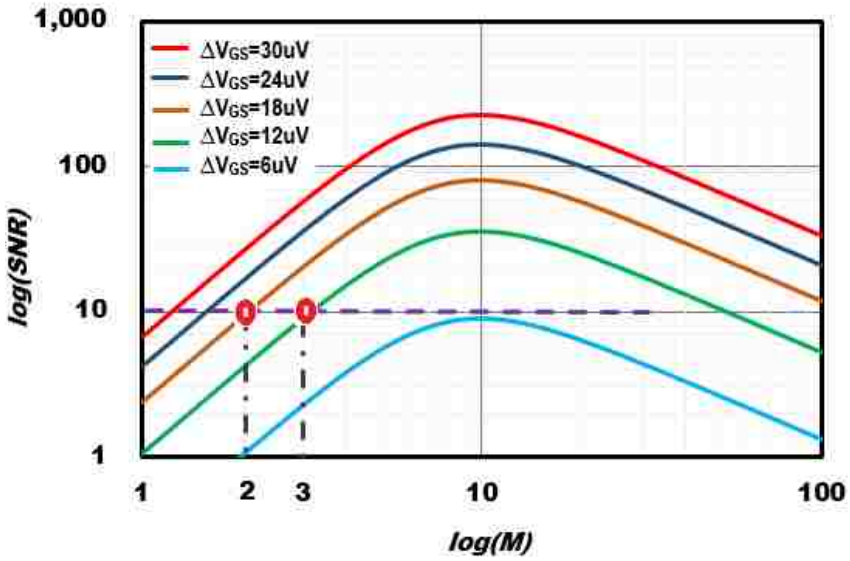

Figure 3.11. log(SNR) Vs log(M) for different amount of pH change

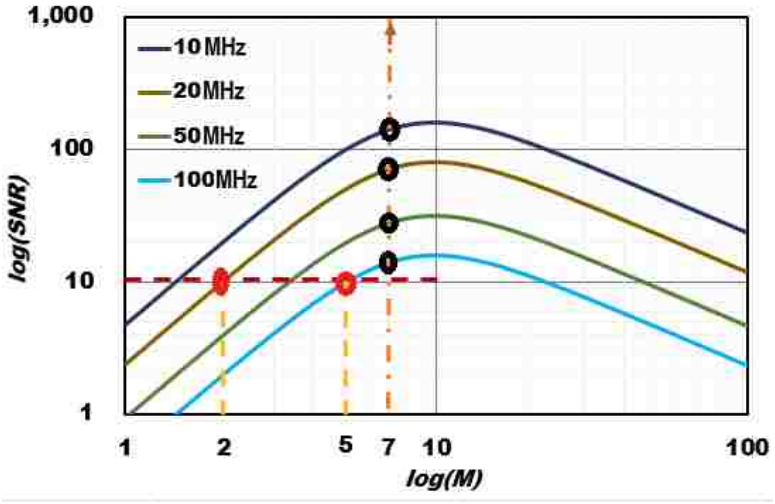

Figure 3.12. log(SNR) Vs log(M) for different bandwidth of operation

3.5 Design Suggestions to Reduce Noise of A-ISFET

We can make some design suggestions based on our analysis and reference [60]. In order to ensure the lowest possible avalanche noises and low excess noise factor an A-ISFET structure should be designed in such way that, 1) the electric field strength in the avalanche region was as low as possible (but $E > 1\times10^5$ V/cm). It ensures a low k factor. 2) the width of avalanche region should be large as possible, because it ensures more ionization impact and hence high multiplication factor with reduced noise and 3) the electron current participation in the total current injected into the avalanche region should be large as it reduces overall noise due to smaller excess noise factor. In order to achieve simultaneously high values of the multiplication factor M and low values of the F factor, we need to choose wisely the following parameters: the electric field strength, the thickness of avalanche region and the ratio of electron current to total current injected into this region.

3.6 Discussions

This chapter identifies and models the different noise components of A-ISFET. It also discusses on different parameters that are related with avalanche mode operation of ISFET. We also develop a model to find an optimum bias point to maximize the signal-to-noise (SNR) of A-ISFET sensor.

CHAPTER 4
DRAIN CURRENT MODEL OF A-ISFET

4.1 Introduction

In this chapter, a physical operation-based drain current model is developed for novel avalanche ISFET (A-ISFET). Since the A-ISFET operates in avalanche region, an accurate model for the breakdown behavior is therefore very important from both circuit design and circuit reliability point of view. The drain breakdown can result from impact ionization [61-62], a parasitic bipolar transistor [63], or the punch-through effect [64]. The model that we developed here for A-ISFET drain current at avalanche region is due to impact ionization. We also perform a correlation study to validate our model.

4.2 Model Formation Process

An ISFET is a four terminal device similar to MOSFET. The two independent variable for operation of an ISFET device is two voltage sources i.e. i) drain-source voltage, V_{DS} ii) gate-source voltage, V_{GS}. Drain-source voltage source is responsible for avalanche breakdown due to impact ionization effects whereas gate-source voltage source is responsible for determining the level of saturation current I_{DSAT0} before impact ionization during avalanche operation.

Similar to MOS device, ISFET is rated for a certain maximum reverse voltage. Operation above this maximum voltage will cause high electric fields in reversed biased p-n junctions at drain terminal of ISFET. These high electric fields create electron-hole pairs, due to impact ionization and undergoes a multiplication effect leading to increased current. The uncontrolled high reverse current flow due to impact ionization through the device may cause high power dissipation, associated temperature rise, and potentially device destruction. Therefore, the modeling of

ISFET behavior in avalanche region is very important from circuit design perspectives and system reliability point of view.

To model the behavior of A-ISFET in avalanche region of operation, we follow a two-step process. In the first step, we model the mobility degradation of carrier due to gate-source voltage while considering A-ISFET device physics into consideration. In the second step, we model the drain breakdown of ISFET due to impact ionization when drain-source voltage, V_{DS} is close to breakdown region for the reverse bias junction.

4.2.1 Mobility Degradation Effects

Among all MOSFET parameters, saturation drain current I_{DSAT0} has the strongest impact on circuit speed and it is the most important parameter that determines device performance. However, most of the models that are classically used ignore this single parameter. The classical model is no more applicable for nanoscale MOSFET that are subject to velocity saturation, mobility degradation and many other non-ideal effects. Different models are formulated to model different non-ideal short channel effects of MOSFET. Here, we follow the semi-empirical model formulated by Kai Chen et.al. [65] to model the short channel effects that degrades mobility. It considers the dependence of carrier mobility in the inversion layer on applied gate voltage, V_{GS}.

We started from an empirical inversion electron mobility model that solely dependent on device parameters of V_t, V_{GS} and T_{ox}. We used the measurement results to find out the fitting parameter to match the model with the real device behavior. The mobility model for N-ISFET electrons that we used as in [65] is:

$$\mu_{eff}\left(\frac{cm^2}{V.s}\right)=\frac{A2}{1+\left(\frac{V_{GS}+V_t}{AT_{ox}}\right)^{C2}}=\frac{A2}{1+\left(\frac{V_{GS}+V_t}{B2}\right)^{C2}} \quad . \tag{4.1}$$

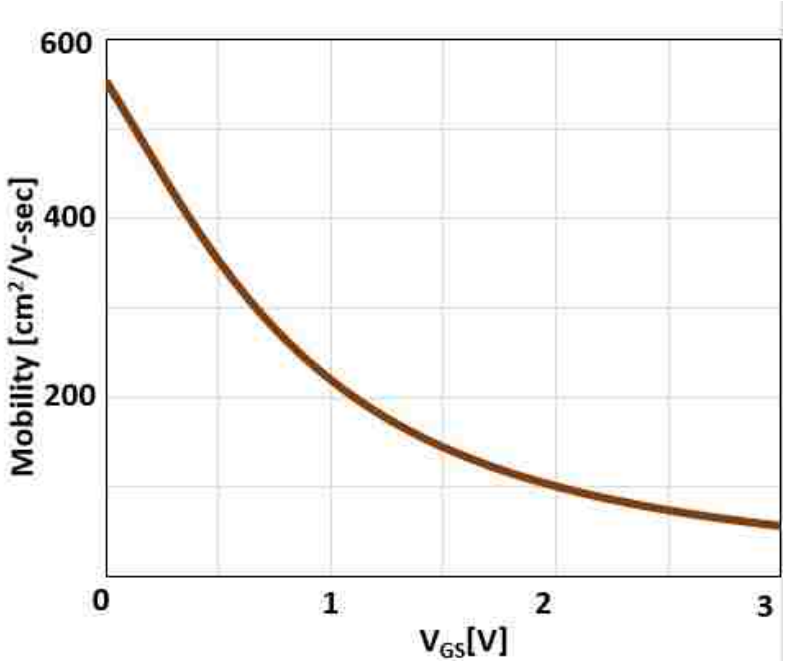

Figure 4.1: Mobility Degradation of carrier in ISFET as V_{GS} voltage changes

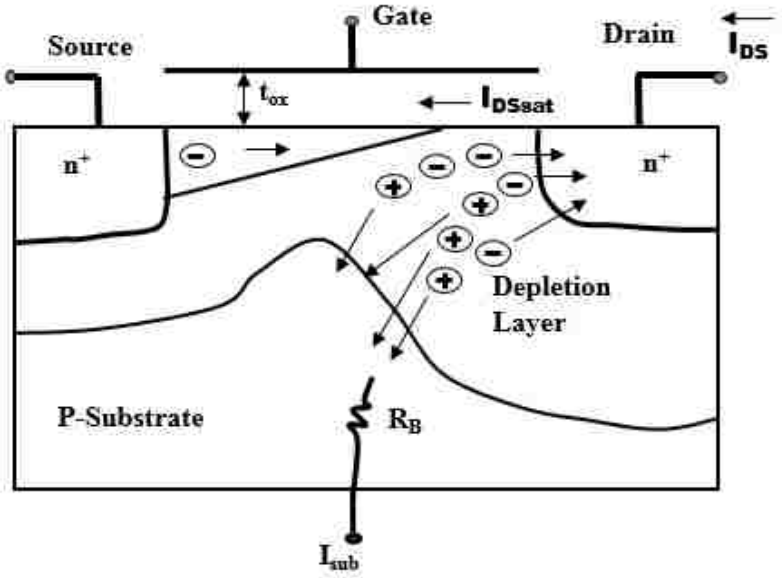

Figure 4.2: Typical Current flow in a n-channel MOSFET during avalanche[48]

Fitting parameters are *A2*=640, *B2*=0.95 and *C2*=1.85. Figure 4.1 shows the variation of mobility in our analytical model as V_{GS} voltage is changed. As shown in fig. 4.1, the maximum mobility happens to be near at sub-threshold region. However, normally the device operates at super threshold, to derive high sensitivity as discussed in Chapter 2.

After extracting the fitting parameter for mobility of carriers in N-ISFET, we derive the I_{DSAT0} for a given V_{GS} and V_t using the equation as in [65]:

$$I_{DSAT0} = k\mu_{eff}(V_{GS} - V_t)^2 \,. \tag{4.2}$$

4.2.2 Avalanche Breakdown Mechanism

For a MOS transistor, operating in avalanche mode, the electric field near the drain region increases significantly and causes impact ionization. The excess generated electron and holes, are swept into the drain substrate junction and enhanced the drain current significantly. As illustrated in Figure 4.2, if the channel current just before entering the impact ionization region is I_{DSAT} and the ionization rates for electron and hole are equal, then we can model the current of A-ISFET as [48]:

$$I_{DS} = M.I_{DSAT} \tag{4.3}$$

$$I_{sub} = (M-1)I_{DSAT} \,, \tag{4.4}$$

where I_{DSAT} is the drain current right before impact ionization, and M is the multiplication gain, given by [48]:

$$M = \frac{1}{1 - \int_0^{Ld} \alpha(x)dx} \,, \tag{4.5}$$

where Ld is the space charge boundary for electrons and α is the multiplication rate for electrons, similar to an APD.

Because the conductivity of the substrate is low, the substrate current may cause a significant voltage drop across the substrate. This voltage drops results in the body effect, which modifies the transistor biasing and increases the channel current. If the substrate resistance is R_B, the voltage drop will be:

$$V_B = I_{sub}R_B = (M-1)I_{DSAT}R_B \,, \tag{4.6}$$

The secondary effect of high current flow during avalanche is higher power dissipation, increased temperature, which eventually increases R_B, since silicon resistivity increases with temperature.

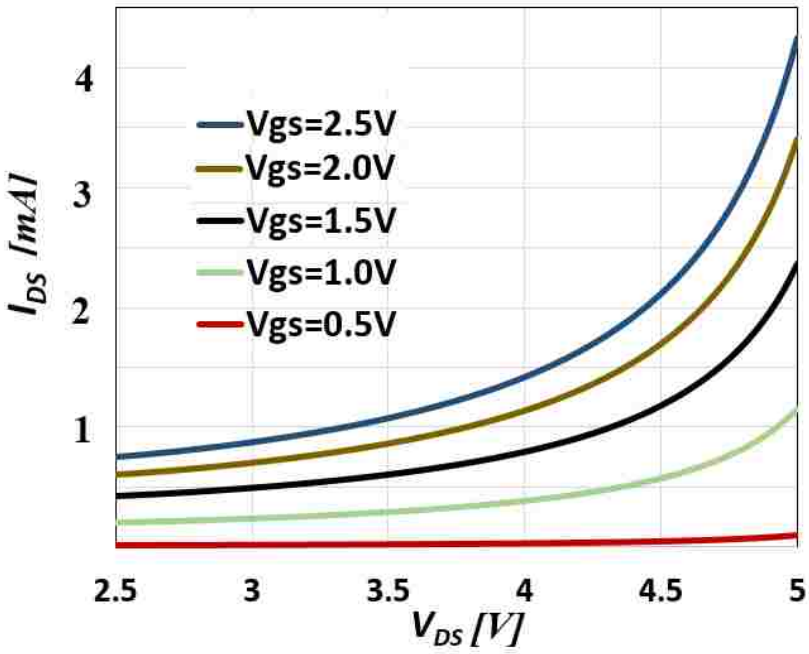

Figure 4.3: Analytical model of output Characteristics curve of A-ISFET at Avalanche region

The substrate voltage, V_B, acts as the back-gate bias and it affects a reduction in the threshold voltage; namely

$$V_T = V_{T0} - \gamma(\sqrt{(V_B + 2\Phi_B} - \sqrt{2\Phi_B} \quad , \tag{4.7}$$

where V_{TO} is the threshold voltage without substrate bias and Φ_B is the surface-inversion potential of silicon and γ is the body effect coefficient.

The reduction in threshold voltage in turn enhances the channel current. A precise calculation of the change of channel current due to V_B is possible by replacing (4.7) into the I-V equation. However, it makes the analytical form too complicated to understand.

For simplicity of analysis and physical insight, we assume that the impact of body effect on the saturation current can be modeled by:

$$I_{DSAT} = I_{DSAT0}(1 + \alpha\gamma V_B) \quad , \tag{4.8}$$

where I_{DSAT0} is the saturation channel current without body bias and α is an empirical parameter. This approximation is accurate enough for small value of V_B.

Using (4.6) for V_B, (4.8) becomes

$$I_{DSAT} = \frac{I_{DSAT0}}{1-\alpha\gamma(M-1)R_B I_{DSAT0}}. \tag{4.9}$$

Replacing (4.9) into (4.3), we have the final drain current expression for A-ISFET in the breakdown region,

$$I_{DS} = \frac{MI_{DSAT0}}{1-\alpha\gamma(M-1)R_B I_{DSAT0}} \quad . \tag{4.10}$$

To make the mathematical steps tractable in estimating the breakdown voltage, we approximate (4.5) as follows [66]:

$$\frac{1}{M} = 1-\alpha_0\left(\frac{V_{DS}-V_{Dsat}}{L_d E_0}\right)^{\tau}, \tag{4.11}$$

where E_0 is about 4.1×10^5 V/cm and α_0 is given by:

$$\alpha_0 = \frac{A}{B}L_d E_0 \exp(-\frac{B}{E_0}) \cdot \tag{4.12}$$

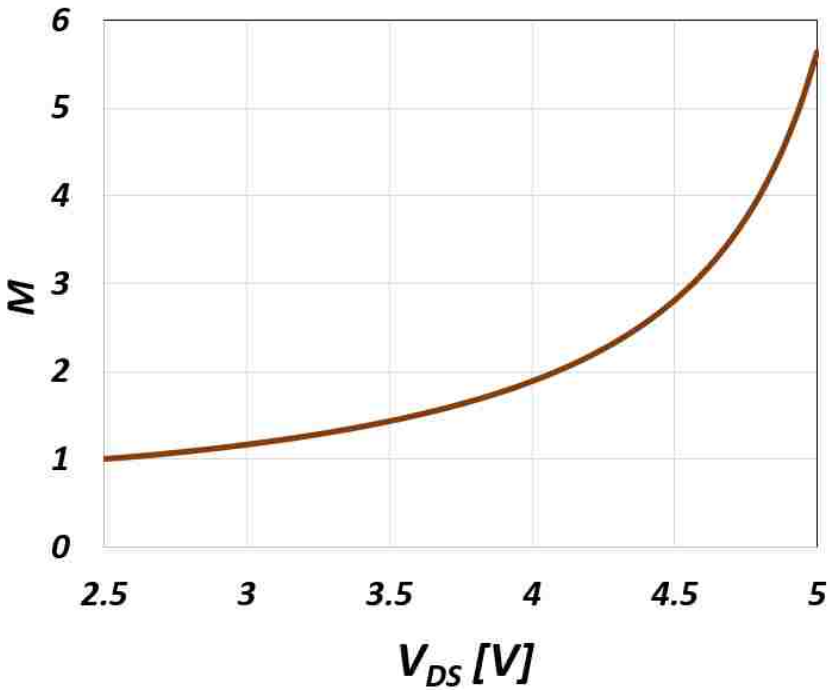

Figure 4.4: Avalanche Multiplication Factor, M when VDS voltage across channel is changed

For small value of V_{DS} (4.11) over-estimates the result of (4.5). The power index, τ and α_0 are constants for a given value of *Ld*. For finite impact multiplication factor, substituting (4.11) into (4.10), we have:

$$I_{DS} = \frac{I_{DSAT0}}{1-\alpha_0(1+\alpha\gamma R_B I_{DSAT0})(\frac{V_{DS}-V_{Dsat}}{L_d E_0})^{\tau}} \quad . \tag{4.13}$$

Then, junction breakdown is also possible when the drain voltage is given by:

$$V_{BDF} = V_{Dsat} + L_d E_0[\alpha_0(1+\alpha\gamma R_B I_{DSAT0}]^{-1/\tau} \, . \tag{4.14}$$

At this value of V_{DS} the denominator of (13) goes to zero and current becomes very large, which means that the ISFET is in breakdown.

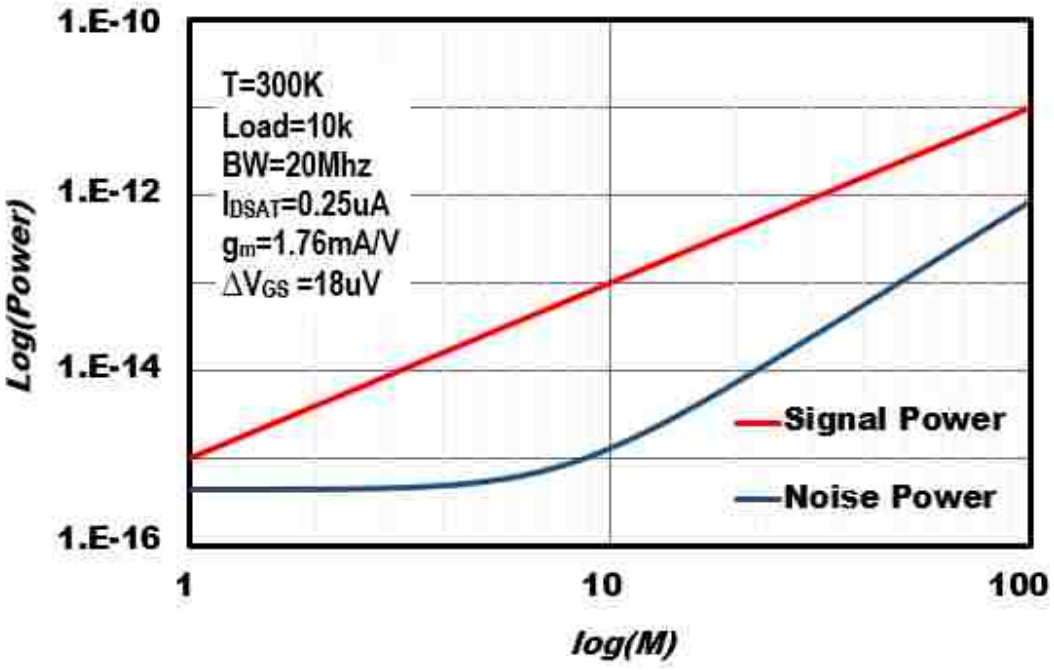

Figure 4.5: Signal power and noise power of A-ISFET as M increases

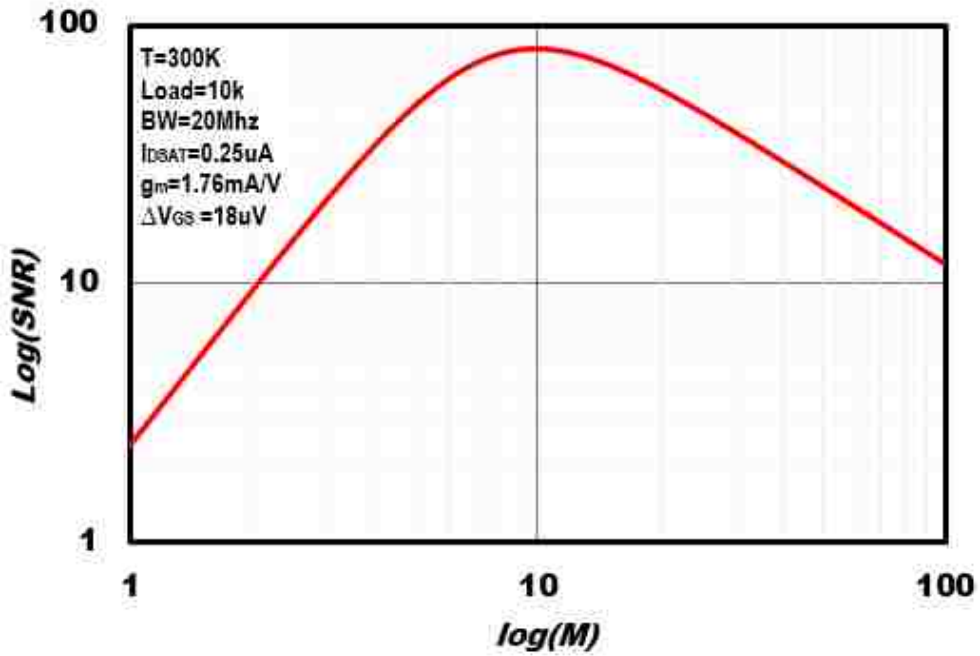

Figure 4.6: Signal-to-noise ratio of A-ISFET as M increases

4.3 Simulation Results

Fig. 4.3 illustrates the I_{DS} versus V_{DS} curve using the model that we developed here for ISFET in avalanche region. As shown in Fig. 4.3, the increase in V_{DS} voltage, results in an increase of the I_{DS} current due to increased avalanche multiplication factor, M. Fig. 4.3 also shows that as the normal voltage V_{GS} increases, the current flow through the channel also increases. However, the breakdown voltage that is required for higher V_{GS} voltage is lower. This process of avalanche breakdown is called the finite multiplication breakdown with positive feedback of the substrate current due to the impact ionization in the pinch-off region [48].

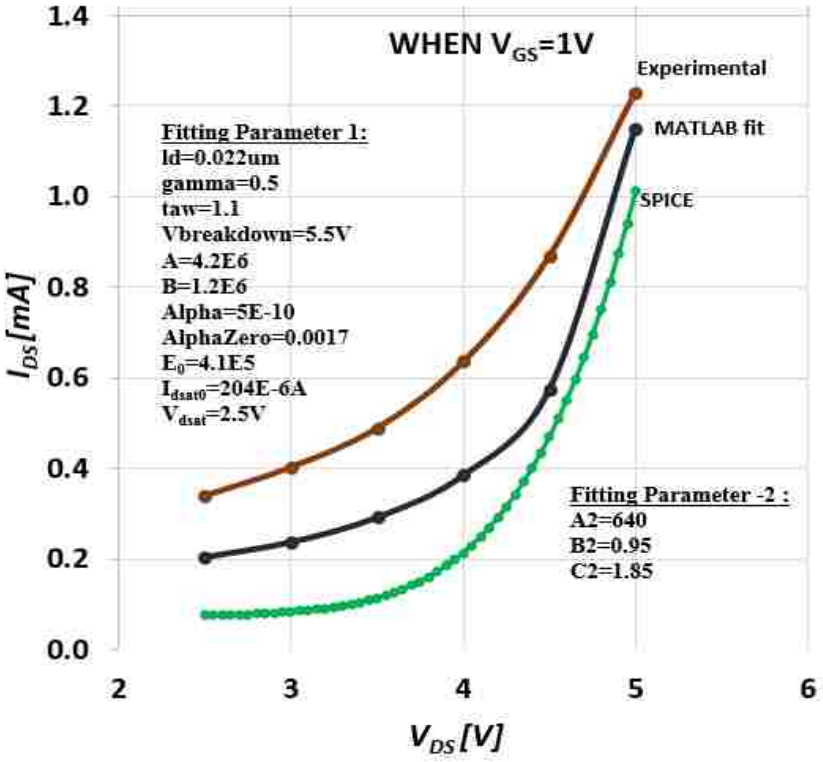

Figure 4.7: Correlation among Drain-Source Current of A-ISFET: SPICE simulation, Experimental measured, and MATLAB model.

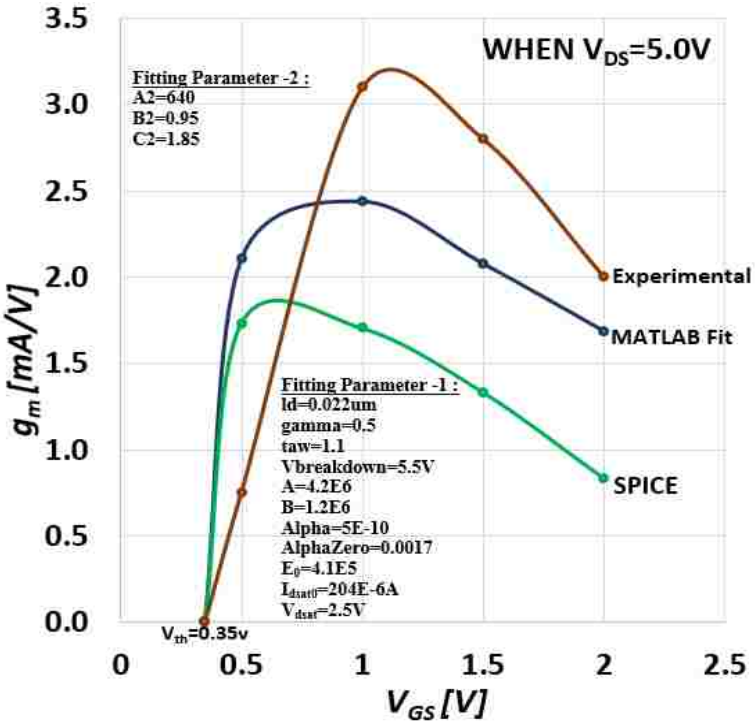

Figure 4.8: Correlation among Trans-conductance of A-ISFET at avalanche region: SPICE simulation, Experimental measured, and MATLAB modeled one.

Fig. 4.4, illustrates the relation of avalanche multiplication factor, M with drain source voltage, V_{DS}. As shown in Fig. 4.4, the value of M increases with increase of V_{DS} due to increased field across pinch off region of A-ISFET during higher V_{DS}. However as illustrated in [58] for an APD, there is a similar optimum value of M for A-ISFET that gives us maximum sensitivity from the A-ISFET sensor. In Fig. 4.5, the relation between signal power and noise power is shown, when the avalanche multiplication factor, M of A-ISFET increases. The increment in noise power overtakes the increment of signal power after certain value of multiplication factor, M. Fig. 4.6 illustrates that after certain optimum value of M factor, the sensitivity SNR of A-ISFET decreases due to increased noise contribution from higher noise factor and higher multiplication factor at avalanche region of operation.

The fitted parameters for the ionization constants A and B at avalanche region are equal to 4.2×10^6 cm^{-1} and 1.2×10^6 V/cm, respectively for short channel silicon devices [67]. The power index (τ) is determined by fitting (4.13) to the experimental measured data with Ld = 0.022 um and is found to be about 1.1.

4.4 Verification and Correlation

Fig. 4.7 illustrates the correlation of drain source current among our developed model, SPICE simulation and experimental measured results. The results are found to be of highly correlated. In finite multiplication mode, the breakdown take place when the impact multiplication factor is finite because of substrate current feedback effect. This mode of breakdown occurs when the saturation current is small and the channel current enhancement due to the substrate current is significant. Therefore, in finite multiplication mode, breakdown characteristics are governed by the channel saturation current rather than the gate bias alone, even though the saturation current is a function of the gate bias. Results plotted in Fig. 4.3 are due to this finite multiplication mode of breakdown. As in (4.14), the second term decreases with increment of V_{GS} and the breakdown voltage turns out a decrease with the gate voltage for the finite multiplication mode of breakdown. The decrease of the breakdown voltage with increment of the drain saturation current, I_{DSAT0} is governed by a number of device parameters. Reduction of the bulk resistivity will help to increase the breakdown voltage due to the finite multiplication mode of breakdown as of (4.14).

Transconductance and output resistance of MOSFET as well as ISFET are two of the most important parameters for analog applications such as sensor, current sinks, amplification stages, current sources etc. As the proposed application of A-ISFET is as sensor in DNA sequencing [18] and sensitivity of A-ISFET as pH sensor can be modeled [13]:

$$S_{ISFET} = \frac{\Delta I_{DS}}{\Delta pH} = \frac{\Delta V_{GS}}{\Delta pH} \cdot \frac{\Delta I_{DS}}{\Delta V_{GS}} = \left(\frac{\Delta V_{GS}}{\Delta pH} \right) g_m \ . \tag{4.15}$$

From eq. (4.15), we can see that the higher the transconductance g_m, the higher is the sensitivity of the A-ISFET. Fig. 4.8 illustrates the correlation of A-ISFET transconductance in avalanche region of operation when the gate-source normal voltage V_{GS} is varied. As shown in Fig. 4.8, there is a close match in variation of transconductance among measured result, SPICE simulation and analytical modeled results. We see that there is a local maximum value of transconductance for a given bias and after that point, the transconductance reduces. To maximize the sensitivity from the A-ISFET sensor we have to operate it at that particular point of bias where transconductance is maximum.

4.5 Discussions

In this chapter, we model the drain current of A-ISFET during avalanche mode of operation. We also perform a correlation study of drain current model with experimental results and SPICE simulation result. Transconductance is the device parameter that determines the sensitivity of A-ISFET sensor. Here, we also perform a correlation study of A-ISFET transconductance and found the results to be highly correlated.

CHAPTER 5

AN OVERVIEW ON TEST CHIP

5.1 Introduction

In this Chapter, we give an overview on the design and architecture of the test chip. The chapter starts with a discussion on the state of the art in literature on ISFET sensor and DNA sequencing. It will be followed by an overview on the architecture, design, layout and operation of the A-ISFET sensing chip and supporting peripheral blocks.

5.2 Literature Review

In this section, we will give a brief introduction on ISFET based sensors that are available in literature and discuss on the different challenges and suggestions related to ISFET based sensor available in literature. We will also discuss on the conventional DNA sequencing techniques as well as Next Generation Sequencing (NGS) techniques, the challenges and the potentials associated there.

5.2.1 ISFET sensor

ISFET is a special member of chemical sensor that was proposed and invented by Piet Bergveld in 1970 [11]. Since its invention, it has been recognized as a powerful sensing element and intensively demonstrated by numerous research work and publication. ISFET based sensors are very attractive because of their high-sensitivity in detection of charged analytes as well as high speed, miniaturization, scalability and low cost. There has been a drive to increase ISFET sensitivity through different technique and choosing proper DC bias of ISFET sensor is one that highly affects their sensitivity [68].

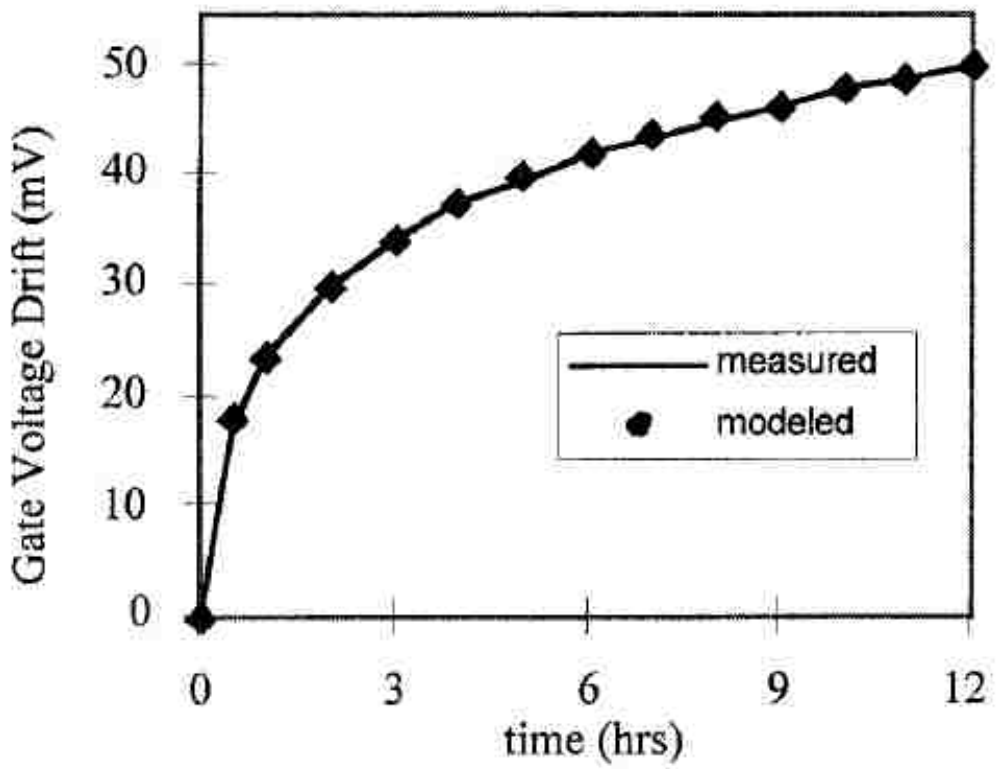

Figure 5.1: Drift in $A1_20_3$ membrane at pH=7.0 [70]

We have shown in earlier chapter that under ideal situation, ISFET can generate a theoretical maximum value of 60mV/pH unit by Nernst equation. This poor sensing margin of ISFETs is a serious threat for the stability and reliability of this device. When we use ISFET to sense a very weak signal originated from the application of few ions on the gate surface, the output signal becomes comparable to noise and pose a serious threat to the reliability of the device. Over the past few years, to obtain higher pH sensitivity and better stability, most of the metal-oxide insulators, such as Al_2O_3, Pr_2O_3, Er_2O_3, HfO_2, Ta_2O_5, and $HoTiO_3$, have been extensively investigated as sensing membranes. In [69] high sensitivity beyond Nernstian pH response from ISFET is realized using double gate FET structure. In [77], a report based on multi-finger gate ISFET shows a good pH response after going through conditioning process.

Threshold voltage instability, commonly known as drift, is another serious obstacle in developing commercially viable ISFET-based biomedical sensors. High accuracy in medical application requires very strict requirements on tolerable drift rate in ISFET. Detailed analysis of drift in $A1_2O_3$ membrane on gate is reported in

[70]. We can see that there is 50mV drift over a period of 12 hours in $A1_2O_3$ sensing membrane, as shown in Figure 5.1.

When ISFET is fabricated using low cost standard CMOS process, SiO_2 is the gate material that is used. For better sensing and drift behavior, commonly used pH-sensitive membranes on top of the gate area are Si_3N_4, Al_2O_3, SnO_2 and Ta_2O_5. These materials provide better pH sensitivity, selectivity, temperature dependence, response time and long-term stability [72, 74]. Therefore, ISFET sensors had to go through post-processing after standard CMOS fabrication process.

Another major obstacle in ISFET commercialization is the technological difficulty associated with its packaging that requires strict insulation. The strict insulation requirements can be taken care through physical separation of chemical sensitive surface from FET by including few additional process steps in fabrication [71].

An extended gate field effect transistor (EGFET) is another option for isolation of FET from the chemical environment. In EGFET, a chemically sensitive membrane is deposited at the end of signal line extended from the FET gate electrode [74-75]. EGFET has many advantages, such as light insensitivity, simple to passivate and package, the flexibility of shape of the extended gate area, disposability etc. [75, 80]. A standard CMOS compatible process flow is reported in [76] for the fabrication of extended gate ISFET.

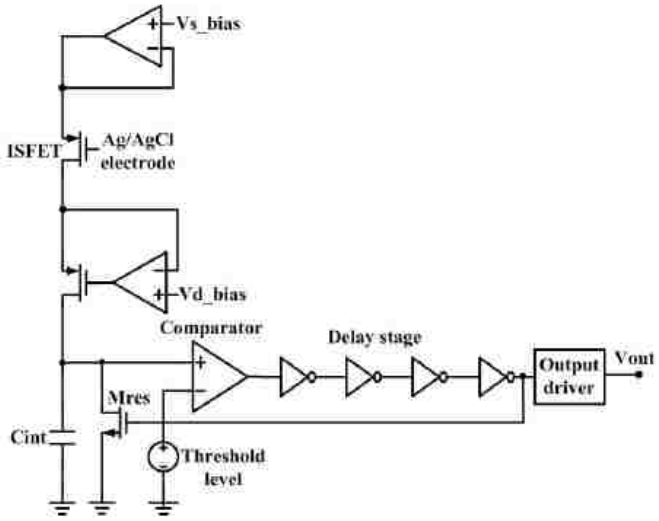

Figure 5.2: ISFET sensor for very small amount of dopamine detection [79]

The body effect in ISFET can results in a significant variation of its sensing behavior. Techniques proposed in [78] eliminate the impact of body effect on ISFET sensor output and provide 50mV/pH sensitivity.

Most of the readout techniques that are used in sensing through ISFET sensor is pH-to-Voltage readout as they provide linear response with pH change. But there are few pH-to-Current readout techniques reported in literature [79] for ISFET, where a very small amount of dopamine, in femto molar range is detected by the sensor. The ISFET sensor with readout circuit is shown in Figure 5.2. Here, the gate of an open-gate ISFET is removed and replaced by the aqueous solution whose potential is commonly set via an Ag/AgCl electrode. The exposed gate oxide is functionalized for biomolecule immobilization to have higher binding, selectivity, and sensitivity.

There is a strong driving force towards lab-on-chip based research. One of the key element in this research is CMOS compatible, scalable, low cost, non-optical ISFET. Lab-on-chip is a multidisciplinary approach to design integrated micro-scale devices for monitoring and performing biochemical assays. Their scalable and miniature size allows for controlled transport and manipulation of biological molecules and cells. Using lab-on-chip, we can do multiplex sensing by integrating CMOS-based micro-sensors onto a single platform [81-83]. Figure 5.3 shows a typical system-on-chip architecture and Figure 5.4 shows the block diagram of an ISFET based DNA sequencing system.

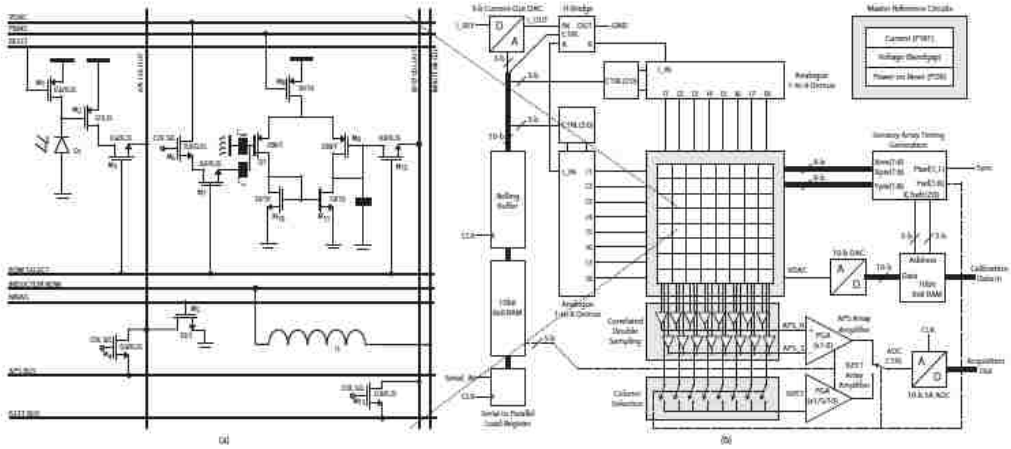

Figure 5.3: Typical system on Chip unit cell and top level architecture [82]

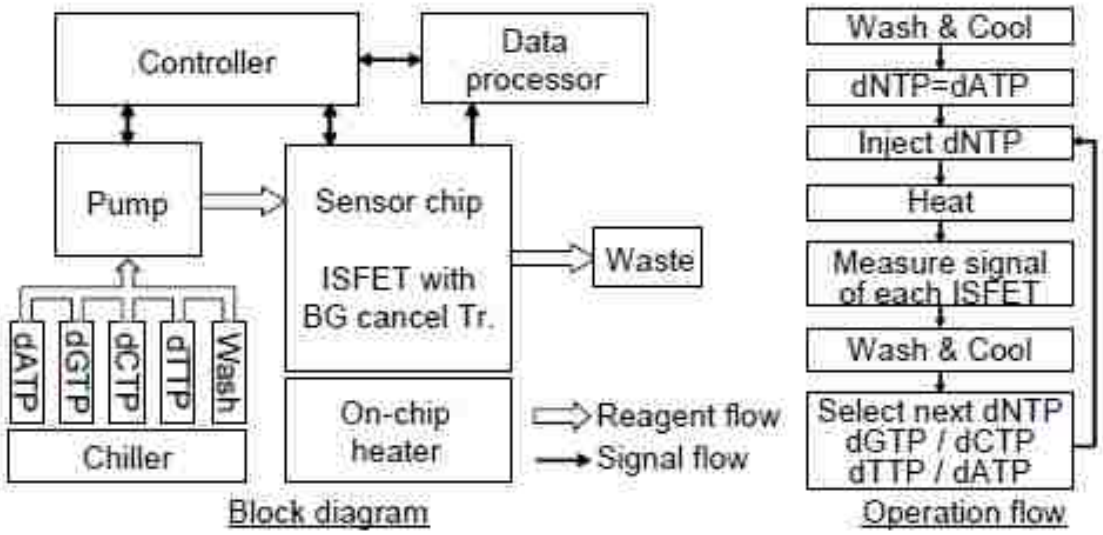

Figure 5.4: Typical ISFET based DNA sequencing system [83]

5.2.2 DNA Sequencing

Most widely used conventional DNA sequencing method is the chain termination method or Sanger method [84]. However, this conventional technique is very time consuming, optical, costly and require specialized facilities, labeling and workers [9, 85, 87]. To reduce the sequencing time through conventional Sanger method, massive parallel sequencing is an option where we can sequence tens of millions of DNA segments in a single experiment [1, 89]. However, the cost remains very high and the sequencing still needs specialized equipments and workers. These disadvantages force us to focus more on non-optical, electrical, CMOS compatible DNA sequencing process as reported in [1, 83, 90]. This thrust toward low cost, non-optical, fast, user-friendly features, and feasibility to use in point of care application provide NGS techniques [91-93] huge attention. In addition, label free NGS techniques are very popular as they provide integration of systems with high selectivity, large dynamic resolution, non-invasive, non-modification of sample, and real-time sensing [86]. There are several reports on chip based DNA sequencing [9, 87-88], which provides compressing hundreds of thousands of different DNA sequences in a tiny surface and provide us all this information on a single image. The images allow the identification of gene expressions to draw biological conclusions for applications ranging from genetic profiling to diagnosis of cancer. However, DNA microarray technology has a high variation of data quality. Therefore, to obtain

reliable results, a complex and extensive image analysis algorithm is essential before the actual DNA microarray information can be used for useful biomedical purposes [88].

There is significant development of genomics tools, technologies and techniques to fuel the NGS efforts forward. These in many cases, are commercialized and form the foundation for a highly active and growing commercial genomics-based industry as reported in [4]. As low cost DNA sequence is very critical to make sequence data widely available for true "genomic revolution", NGHRI is tracking the cost/DNA sequence from since long. In Figure 5.5, we can see a huge reduction of DNA sequence cost over past years. This cost reduction comes from extensive research and advancement in NGS over past years.

The completion of HGP in 2003 had fueled the genomic revolution and since then, there has been a tremendous growth in multi-disciplinary genomic industry. This dissertation is an effort toward further fueling the genome revolution by introducing a new low cost NGS technique. The focus behind design and fabrication of this A-ISFET based sensing chip is to introduce the concept of avalanche for ISFET to achieve high sensitivity from a device, especially when the signal is very weak and comparable with the noise of the system. In the following sections, a brief introduction on the chip architecture, layout and synchronization process has been provided.

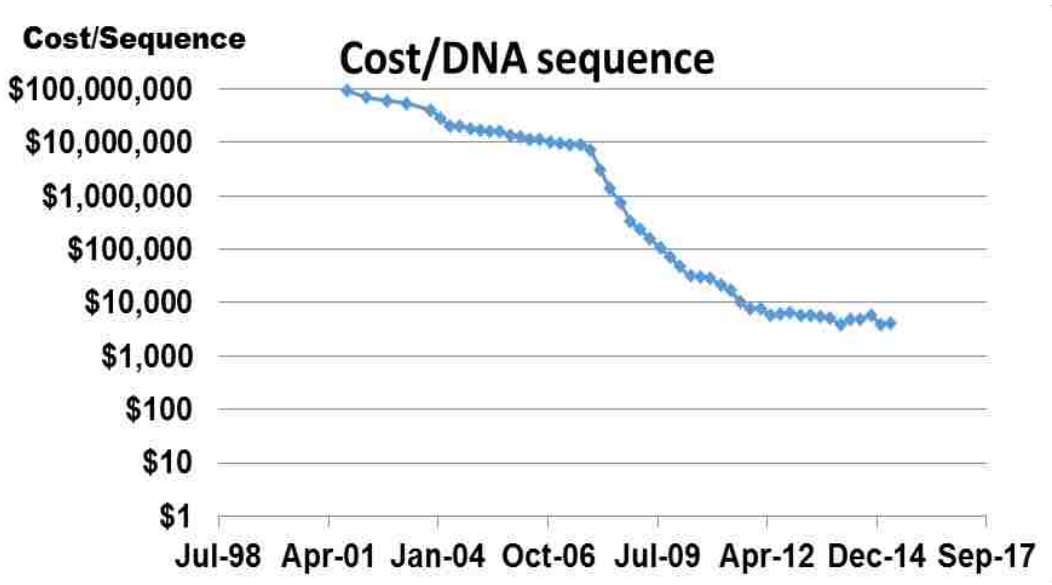

Figure 5.5: Genome Mapping Cost per person survey conducted by NHGRI [7]

5.3 Design Overview of Test Chip

5.3.1 Unit Cell

Unit cell is the main building block used to design the sensing array. The unit cell consists of one sensing transistor (ISFET) and two switching transistor for control and synchronization. The sensing chip has four different cores and each core has 90×95 unit cells. The switching/access transistors in each unit cell are used for row and column selections. They are designed large to make sure that it doesn't affect the ISFET measurements result. The structure of each unit cell and its layout is shown in the Figure 5.6.

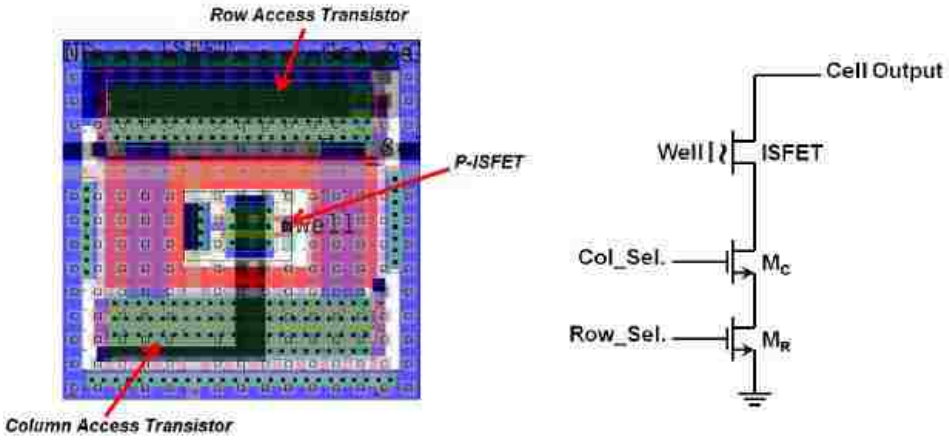

Figure 5.6: A) The layout of the unit-sensing cell - different component is outlined. B) Unit cell structure of the ISFET sensing chip with supporting column selector and row selector to access the sensing data from the cell/ well.

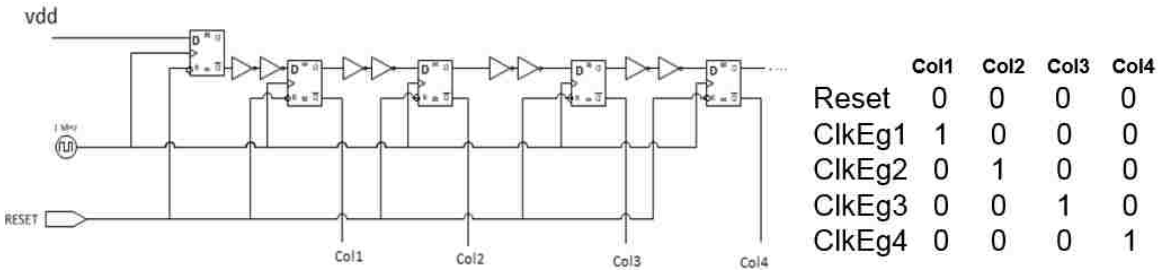

Figure 5.7: The shift register used for row and column select circuits

5.3.2 Peripheral Circuit: Column Select and Row Select

The row select and column select blocks are responsible in synchronizing the ISFET unit cell readout with clock, line sync (LSYNC), and frame sync (FSYNC) signals. We have used a special shift register to perform the row and column select as shown in Figure 5.7. Figure 5.7 also shows the sample output of the select registers with clock.

We have done a SPICE simulation on a smaller set of unit cell arrays to ensure the functionality of the row and column select circuits. The simulation results are shown in Figure 5.8. It shows that, after the reset and after each clock pulse, a column is selected where its output current is transferred to the output. This simulation confirms the functionality of the row and column select circuits as well as ISFET the unit cell with access transistors.

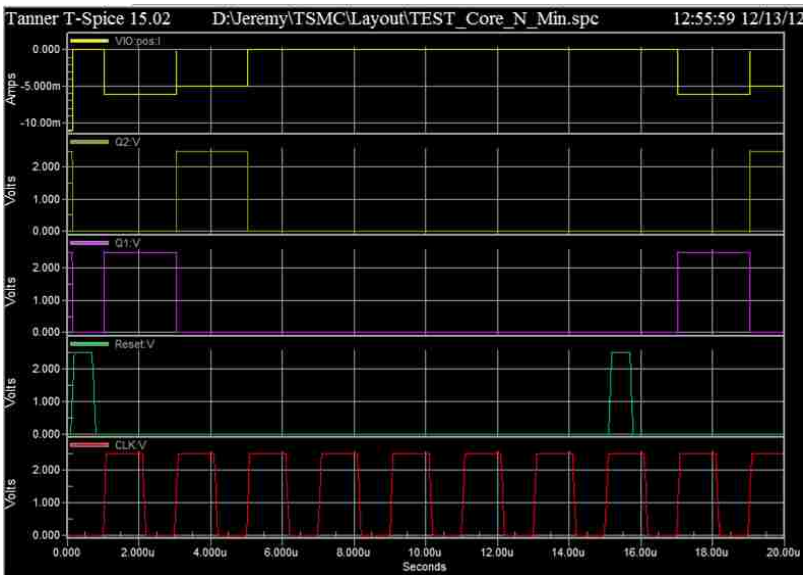

Figure 5.8: The SPICE simulation results showing the clock, reset, column select pulses and the unit cell output current.

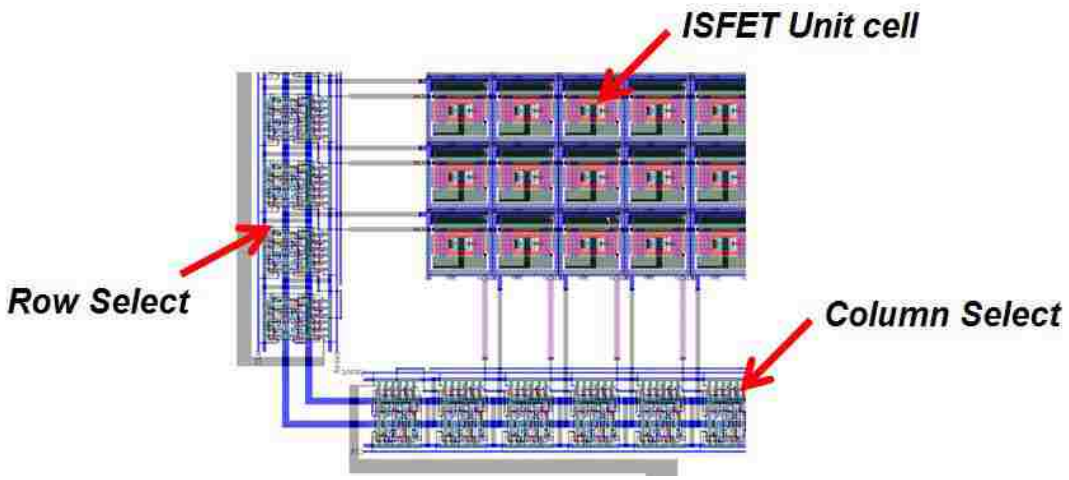

Figure 5.9: The layout of the row/column select and other supporting circuits

The layout for the row select and column select with ISFET unit cells are shown in Figure 5.9. The size of each unit cell is 16um.

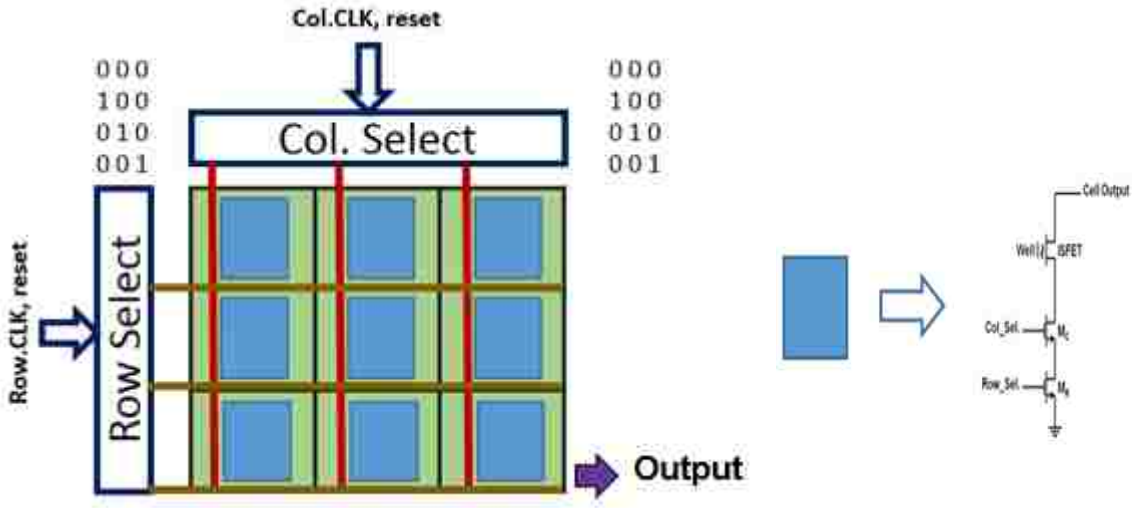

Figure 5.10: A typical architecture of a 3×3 unit sensing chip and structure of unit cell

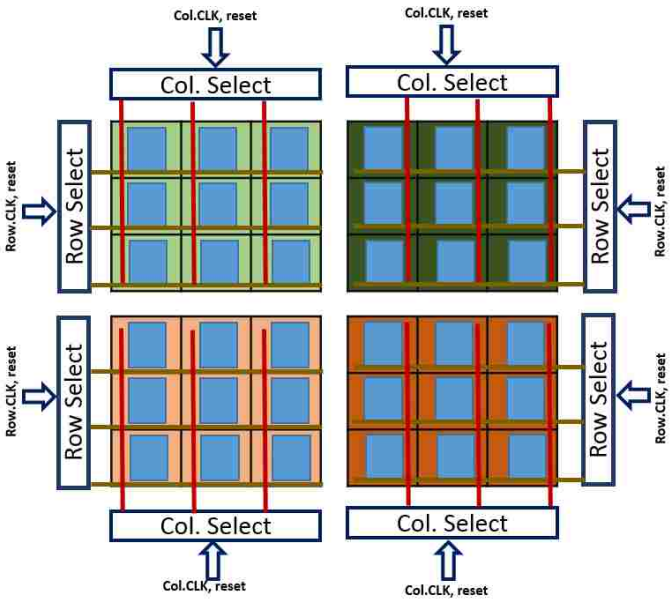

Figure 5.11: A typical 4 core sensing chip with respective column select and row select registers

5.3.3 Chip Architecture

A typical 3×3 unit sensor chip will have an architecture as shown in Figure 5.10. We can see that with change of clock the row select and column select registers are activated and change state. Upon activation of row select registers and column select registers, a particular sensor cell is activated and produces time-differentiated output from the sensor. Figure 5.11, illustrates a typical ISFET sensor chip that uses the same principle as before, while having 4 different sensing core to ensure faster readout of the sensing data. The test chip consists of four cores and each of the cores in test chip has 90×95 unit cells, which are accessed through column select and row select signal during readout process. The architecture of the test chip is shown in Figure 5.12. The access transistors are designed large to ensure that it doesn't affect the measurement results. Four sensing core contains four different unit cell specification, which includes P-ISFET and N-ISFET for both small (with W/L=2.5) and as well as large (with W/L=24) sensing transistor to check sensitivity variation. The column select register and row select register for each core has its own reset signal to synchronize the readout scheme. Figure 5.13 shows the layout of the 4 different unit cells that are used in the four core of test chip to verify the sensitivity of ISFET sensors with different device dimensions.

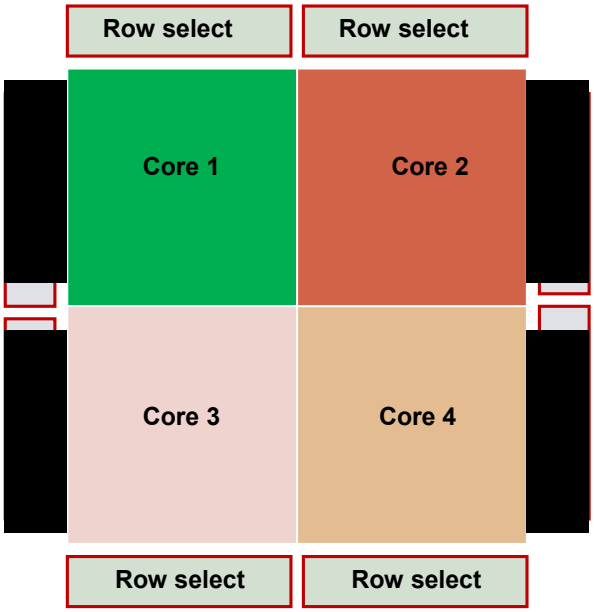

Figure 5.12: Top Level architecture and block diagram of ISFET chip

5.3.4 Layout of the Chip

We have layout the chip using TSMC's 0.25µm standard CMOS process and fabricated the chip with that process where the nominal supply voltage is 2.5V. The chip pad ring contains electrostatic discharge (ESD) devices to protect the transistors in the core against electrostatic charge injection during chip handling. The test chip has a total of 52 pins including 4 VDD, 4 GND, and several input/output signals. The layout of the chip is shown in Figure 5.14.

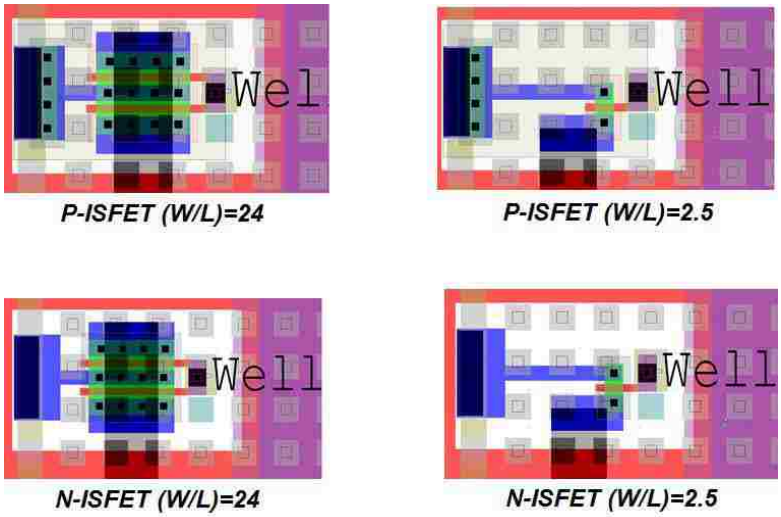

Figure 5.13: The layout of four types of ISFETs designed in the test chip

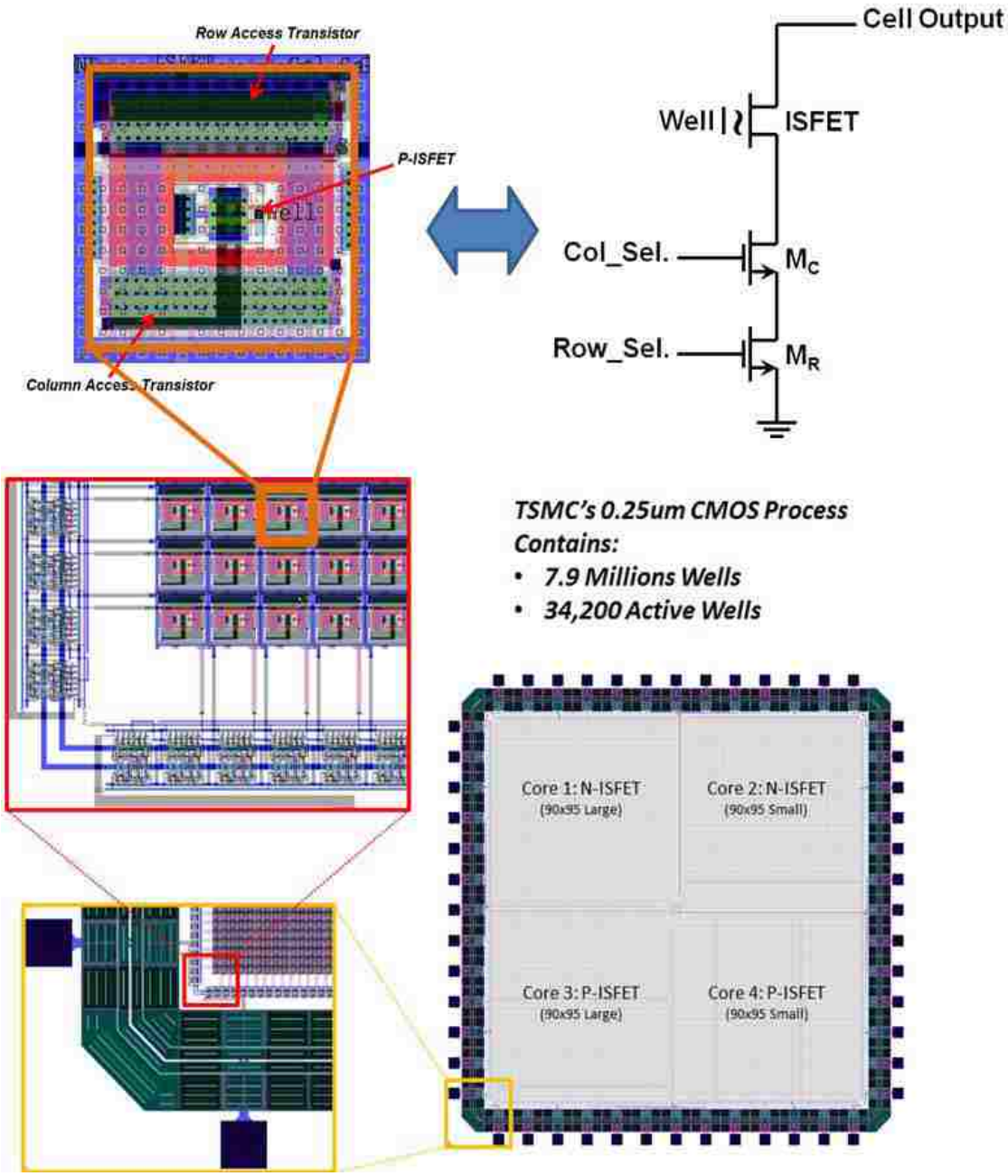

Figure 5.14: The layout of the test chip with ~35,000 arrays of A-ISFETs, including row select and column select [18]

5.3.5 EDA tools

The EDA tool that has been selected for simulation and design of the chip are TSPICE and LEDIT from Tanner EDA. Tanner EDA tools are a window based packages that are fast and powerful that can handle even a large design at the level of a chip. The only issue with using this tool is that the foundry usually does not provide the designer with the Process Design Kit (PDK). Fortunately, the simulation library of HSPICE is completely compatible with the TSPICE and it could satisfy our simulation needs without any need to modify the files. The missing component was therefore the design rule checks (DRCs) and the extraction commands that we developed at UNM. For extra verification, the final design was imported to Cadence Virtuoso to verify all the DRC rules.

5.3.6 ESD Protection

ESD protection plays a critical role in every electronic integrated circuit. The primary function of the ESD protection is to bypass accidental electrostatic charge to the VDD or VSS power rail and block it to the internal circuit that are sensitive to the discharge and can be damaged by the discharge.

There are many structures available for the ESD protection circuit and most of the process design kits come with few ready to use pre-laid out designs for the ESD protection. Unfortunately, most of the available designs cover the needs of digital circuits and are not suitable to be used for analog input/outputs. Therefore, in this project we have designed the ESD protection devices and verified their functionality through simulations and experiments as suitable for ISFET.

5.3.7 PAD

PAD is a critical part in every chip. There are two main aspects to consider in designing every PAD: mechanical and electrical properties. Mechanical consideration recommends having all the metal layers on the top of each other and have them connected using sufficient number of vias. Paying no attention to these considerations might cause the PAD peel off, while wire bonding and a failure of testing the chip.

The PAD must also be large enough to make the wire-bond and packaging the chip practical. However, in order to work at higher frequencies, the parasitic capacitance must be as low as possible that translates to having the smallest possible geometries for the PAD.

5.3.8 Well Creation

In our A-ISFET chip, we require to have a smaller well opening without violating the design rules. To achieve this goal, at the bottom of each well a smaller via is placed as shown in Figure 5.15. The well size is 375nm and the well pitch is 1.5um. Although there are 15x15 wells on top of each unit, only one well is connected to the unit cell ISFET for testing. We place a via of 360nm as it meets the design rules. After the fabrication process is complete at TSMC, the test chips have gone through post processing at the University of New Mexico, to etch the via and open the smaller wells. The SEM image of the wells after the post processing is shown in Figure 5.15. It contains 7.9 million wells, in which 34,200 wells are active with A-ISFET at the bottom. An 840nm × 840nm opening and 1.44µm pitch in the passivation layer make the wells.

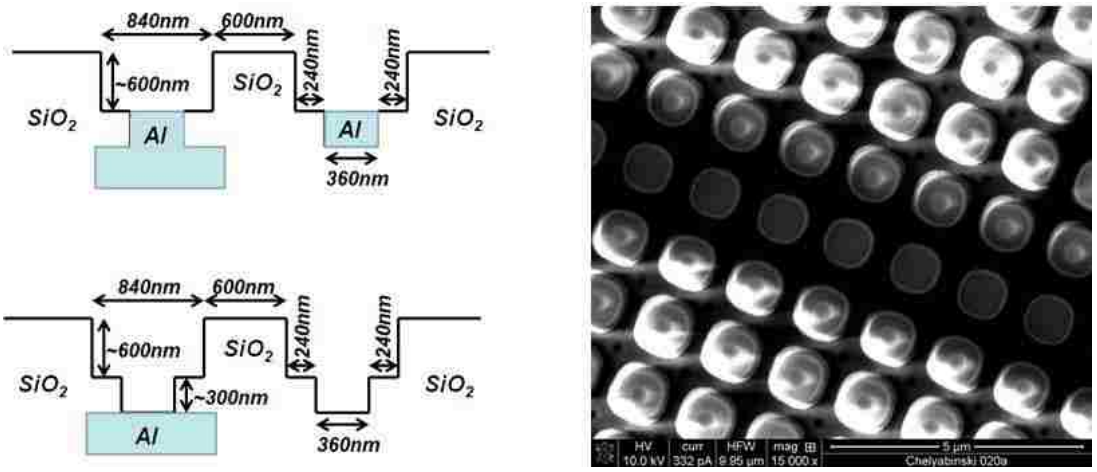

Figure 5.15: The cross section diagram of the wells structures (left) and the SEM photograph of the wells (right) [18]

5.4 Design Consideration for Full Scale Genome Sequencing

ESD protection plays a critical role in every electronic integrated circuit. The primary function of the ESD protection is to bypass accidental electrostatic charge to the V_{DD} or V_{SS} power rail and block it to the internal circuit that are sensitive to the discharge and can be damaged by the discharge.

There are many structures available for the ESD protection circuit and most of the process design kits come with few ready to use pre-laid out designs for the ESD protection. Unfortunately, most of the available designs cover the needs of digital circuits and are not suitable to be used for analog input/outputs. Therefore, in this project we have designed the ESD protection devices and verified their functionality through simulations and experiments as suitable for ISFET, described in chapter 2.

5.5 Discussions

This chapter discusses on the details architecture and design procedure of the test chip to verify the concept of A-ISFET sensor. It also discusses on the state of the art in DNA sequencing and on all electronic DNA sensor as well as the challenges that are involve with all electronic DNA sequencing.

CHAPTER 6

TEST SETUP AND EXPERIMENTAL RESULT

6.1 Introduction

In this chapter, we are going to discuss on the readout mechanism of the A-ISFET sensing chip for DNA sequencing. The discussion will also contain the integration process and noise cancellation technique to improve resolution of the sensing signal from the chip. We will conclude the chapter with test results of ISFET chip in both normal mode and avalanche mode of operation.

6.1.1 Wire Bonding

Wire bonding is the process used to provide electrical contact between the silicon chip and the external leads of the semiconductor device using very fine bonding wires. Generally, fine gold or aluminum wire is used for wire bonding. During gold ball wire bonding, a gold ball is first formed by melting the end of the wire using an electronic flame-off. This gold ball has a diameter ranging from 1.5 to 2.5 times the wire diameter.

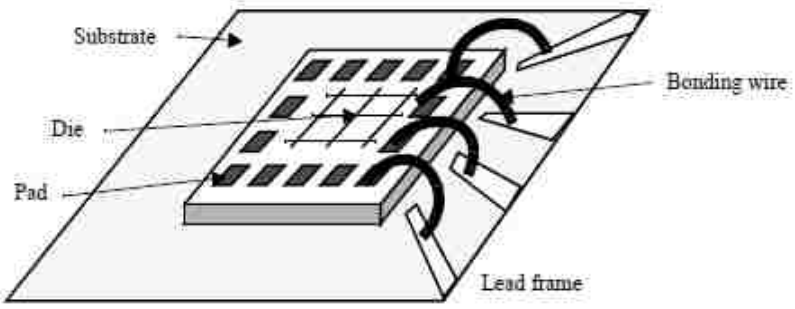

Figure 6.1: Typical wire bonding and packaging of a chip [94]

The gold ball is then brought into contact with the bond pad. Adequate pressure, heat, and ultrasonic forces are then applied to the ball for a specific amount of time, forming the initial metallurgical weld between the ball and the bond pad as well as deforming the ball bond itself into its final shape. The wire is then run to the corresponding finger of the package or substrate forming a loop between the bond pad and the package lead. Pressure and ultrasonic forces are applied to the wire to form the second bond, known as a wedge bond or stitch bond or fishtail bond. The wire bonding machine or wire bonder breaks the wire in preparation for the next wire bonding cycle by clamping the wire and raising the capillary. A typical wire bonding and packaging is shown in Figure 6.1.

6.2 Readout mechanism and Synchronization

Readout circuits are the circuit that makes the sensing data available to external world for processing. It reads a voltage or a current signal, which is modulated based upon the pH variation or threshold voltage variation at the gate of ISFET. Our sensing chip is based on pH to current readout measurement technique. We can describe the sensing process shown in Figure 6.2 - with the following process flow:

$$\text{pH}\uparrow \Rightarrow \ V_{th}\uparrow \Rightarrow \text{Ids} \downarrow \Rightarrow V_o \downarrow \text{ AND}$$

$$\text{pH} \downarrow \Rightarrow \ V_{th}\downarrow \Rightarrow \text{Ids} \uparrow \Rightarrow V_o \uparrow$$

So change of pH is transferred to a change of drain source current $I_{ds.}$ The readout circuit changes this drain-source current change to an equivalent voltage change. Operation of the readout circuit can be described by the following equation [13] -

$$V_0 = V_{ds} + R_2 * I_{ds}. \tag{6.1}$$

We can see that we can modulate the response from the readout circuit by changing the R_2 resistance as well as changing the bias voltage V_{ds} which sets the bias region of the ISFET and its current. The current can then be modulated through ISFET for a specific bias by changing the ion sensitive gate electrode to more sensitive electrode or conditioning the gate with specific binder.

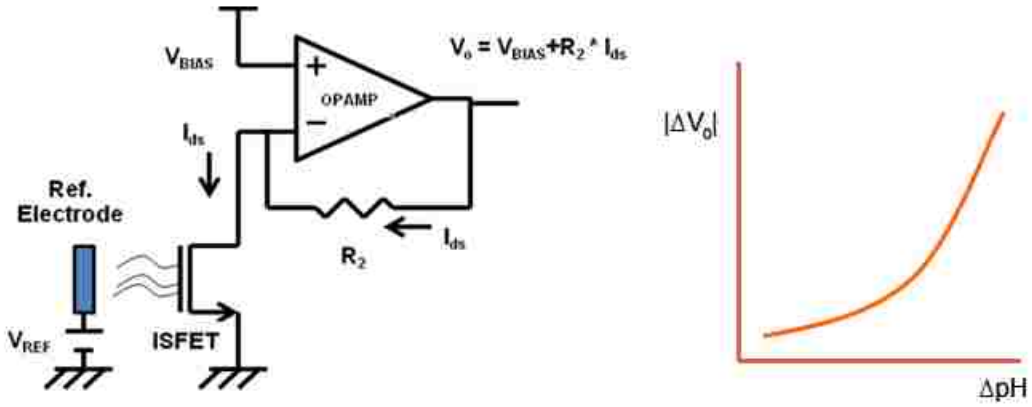

Figure 6.2: A) Circuit diagram showing the new pH to current readout concept [13] B) Shows the change in output of the readout circuit as the pH is changed.

The top level architecture of the chip with the readout scheme is shown in figure 6.3. The chip consists of four sensing core that has ISFET sensing cell with different dimension. The sensing data from each of the sensing cell is readout by the activation of the column select and row select signal for each of the core with the application of two clock signals operating at two different frequencies.

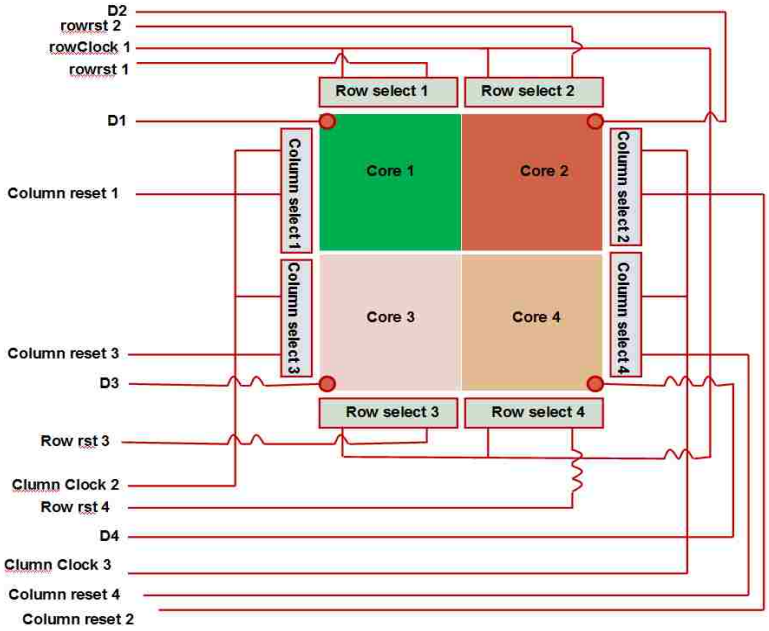

Figure 6.3: Top level architectural diagram of the ISFET sensing chip with I/O connections [13].

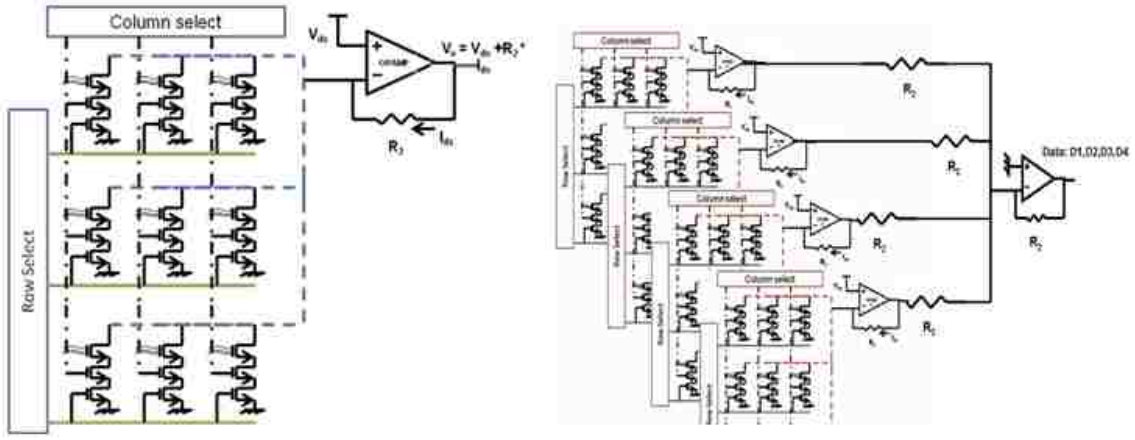

Figure 6.4: A) structure of a 3× 3 single core-sensing chip with readout circuit B) Integration of data from a typical 4-core ISFET chip in Analog domain

Using proper synchronization signal, we can readout the sensing signal from the four cores and add them together to pass through single channel to the external image grabber, shown in Figure 6.4.

The column select and row select for each core has its own reset signal and can be reset as of our requirement to synchronize the readout scheme. The timing diagram of different signals for the readout circuit and synchronization is shown in Figure 6.5. We can see that, there are four data output signal, two clock signal, and eight reset signal. Four of the reset signals are used to reset four row select registers and the other four reset signals are used to reset four column select registers during readout and synchronization. The clock frequency for row select block is faster than that of the column select block. If we want to read 20 frames in each second by the image grabber, then for the chip with 4 cores of 90×95 pixels (each) should have row select clock frequency and column select clock frequency as below.

Sample Calculation: Frequency calculation for row select, Clock 1: As time available for 1 frame = 1/20 sec. Therefore, time available for each pixel= 1/20/(90*4*95) sec =1/684000 sec.

So frequency of the clock 1 (row select) is: 0.684 MHZ

Similarly, Frequency calculation for column select, Clock 2 and Clock 3: Time available to read one row of core 1 and core 2 =1*90*90/684000 sec =9/760 sec

So the frequency of clock 2 and clock 3 (column select) = 84.4 Hz

As shown in Figure 6.4, the data signals differentiated in time domain with clock1-row, LSYNC and FSYNC are fed to the image grabber. The image of the sensing cell responses are then displayed at external window. As we are reading 20 frame in each second from the chip, the image at display shows the real time response of the pH interaction with ISFET sensor.

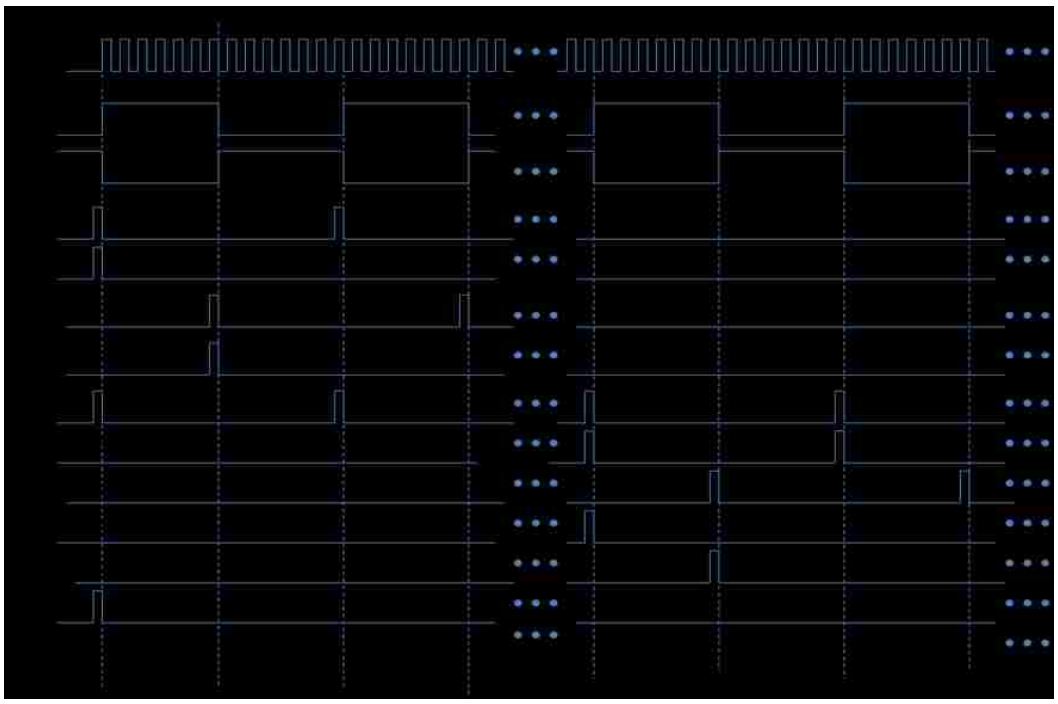

Figure 6.5: Timing diagram of the readout circuit for the ISFET chip [13].

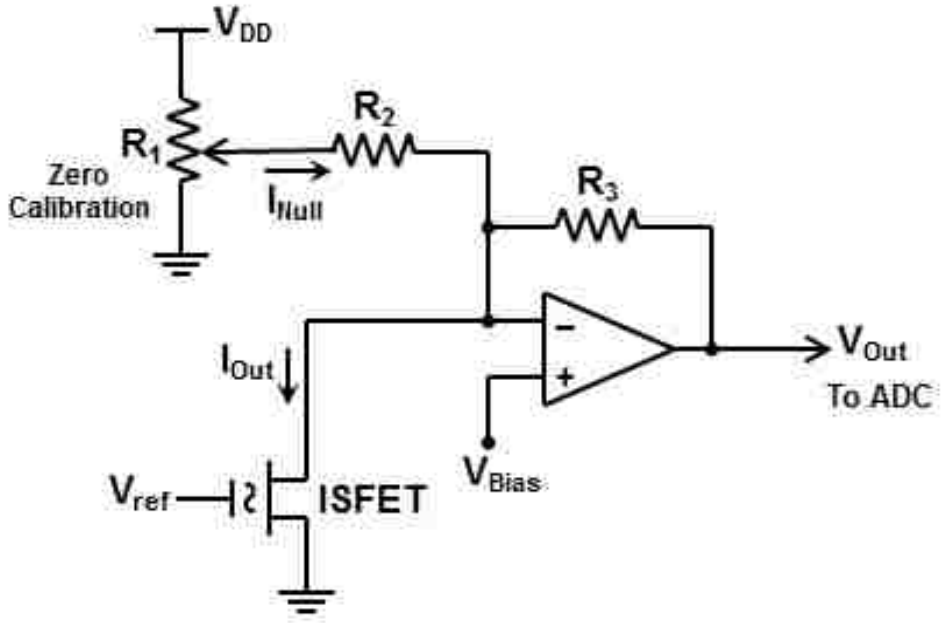

Figure 6.6: DC offset Cancellation in ISFET chip by forcing null current [18]

6.3 DC offset Cancellation Principles

We introduce a dc offset cancellation process to the readout technique to increase the resolution from the ISFET sensor. The technique is based on forcing a nulling current with a particular reference point, in our case it is pH=7. In section 6.2, we see that the output is not proportional to the sensing current; also, the signal needs to overcome a large offset to provide a significant change in output. The unique circuit technique for noise cancellation is shown in Figure 6.6. The value of required null current is dependent on the bias voltage and feedback resistance, which is given by [18]:

$$V_{out} = V_{Bias} - I_{Null}.R_3 + I_{Out}.R_3 \ . \tag{6.2}$$

$$V_{Out} = I_{Out}.R_3 \ \ \Rightarrow I_{Null} = V_{Bias} / R_3 \ . \tag{6.3}$$

The null current decreases as the value of feedback resistance in trans-conductance amplifier increases, given that the bias voltage is constant for a particular setup.

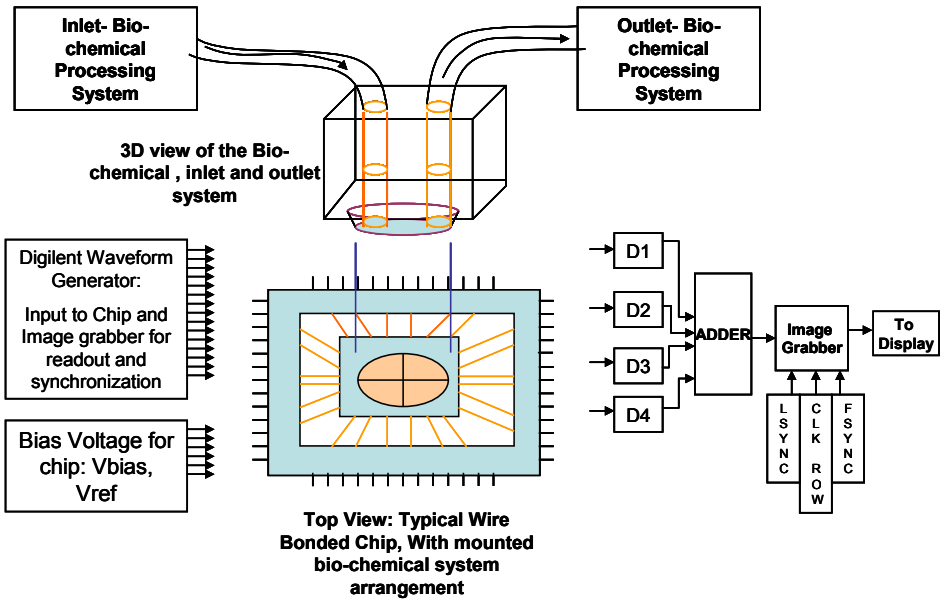

Figure 6.7: Different block for test Setup of A-ISFET sensing wire bonded chip: top mounted bio-chemical processing system, waveform generator, bias voltage generator and data processing system with image grabber [13]

6.4 Test Setup and Hardware

A cubic shaped, specially milled structure is used to inlet and outlet the bio-chemical on the gate of ISFET sensors in chip as shown in figure 6.7. The flow of bio-chemical with different pH from different reservoir is controlled by time-controlled valve by the bio-chemical processing system. We can also see from the Figure 6.7, that the mounting arrangement of the bio-chemical processing system is used to release sensing materials on top of the ISFET sensing chip. Digilent waveform generator can be used to synchronize the readout of the pH sensing data from the chip. In section 6.2, we have seen the different waveforms that are needed for the readout of the chip and for its synchronization with the external image grabber.

In addition, the bias voltage for the chip to generate pH to current signal for the readout circuit is also required. The readout circuit generates data signal - D1, D2, D3 and D4 from four different core of the chip. We then use an adder to add the four time multiplexed data signal and pass it through a single channel to the image grabber. The image grabber processes the sensing data, which are read by readout

circuit, for the external display, through the LSYNC, FSYNC and row clock signal (clk row). Figure 6.8, shows the actual setup that we use in lab for testing of the chip.

6.5 Experimental Results

In this section, we will present the result from the different experiment that we have done in the lab using this A-ISFET sensing chip. We find the chip to be fully functional and working as expected to operate. We test the chip both in normal region using nominal voltage for the CMOS process and in avalanche region with bias voltage near the breakdown region of the CMOS process.

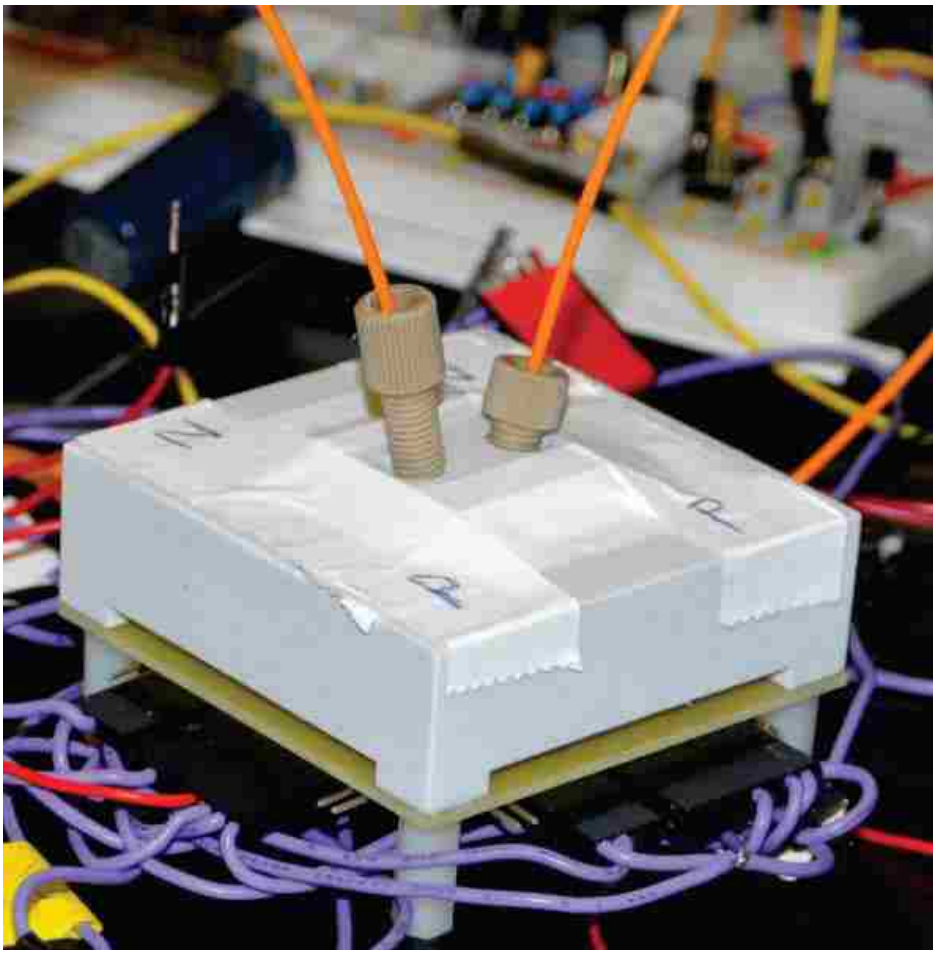

Figure 6.8: Actual lab setup for the testing of the ISFET sensing chip [13]

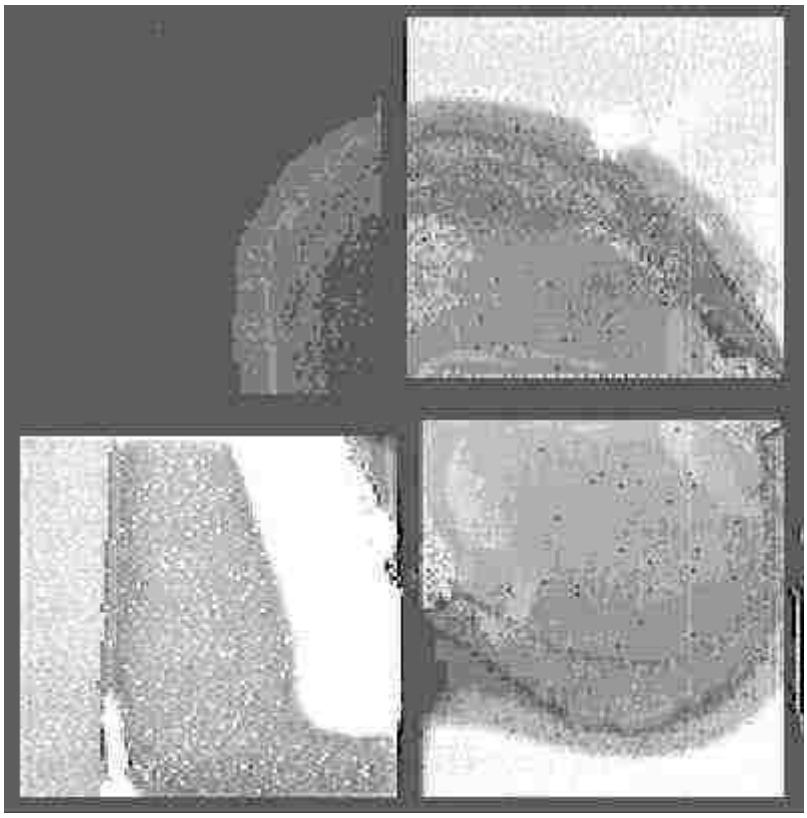

Figure 6.9: Actual test setup and wiring - implemented in lab with biochemical system's inlet and outlet [13]

Based on the experimental results, it was observed that the response of the four different cores were in the normal operational region. The response from four different cores is different as the sensitivity of the unit cell in each core is of different dimensions and parameters. However, the good thing is that the ISFET's are showing variation in response in each core and the response is in real-time as of our expectation and planning. Figure 6.9, shows the typical response that we have obtained from the ISFET chip, when operated in normal region with application of nominal voltage for the CMOS process.

Figure 6.10 shows the time domain transient response of a unit cell in ISFET chip. We can see that the response is very quick and the response reaches its peak value within 1-2 seconds. Hence, the DNA sequencing can be made possible through this technique in real-time.

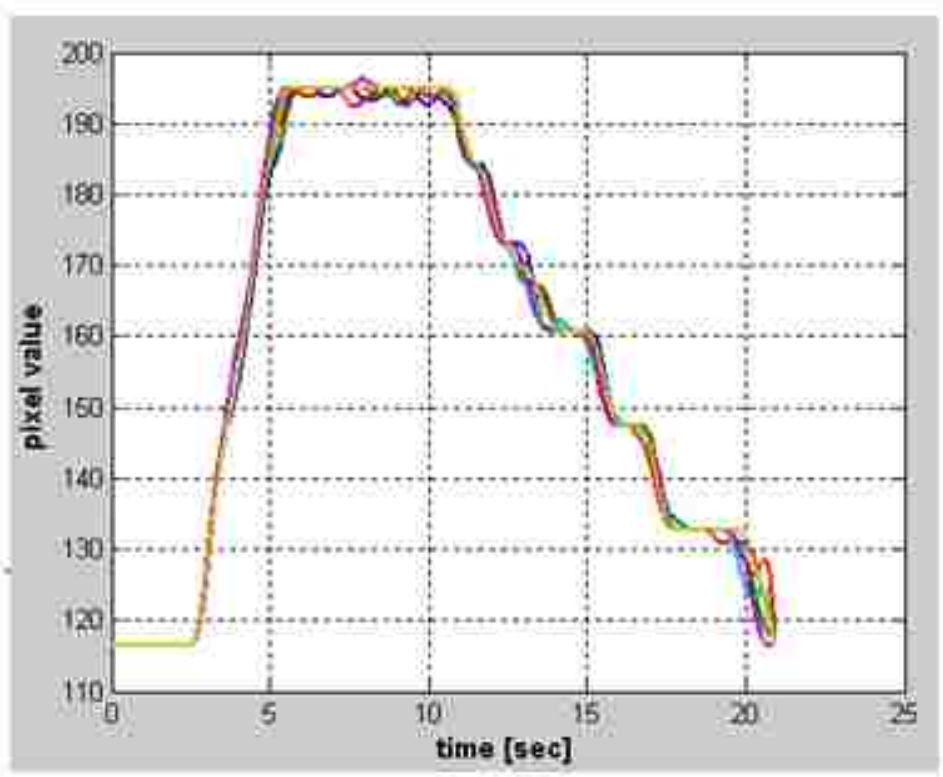

Figure 6.10: Transient response of a unit cell of the ISFET chip

We also test the chip in the avalanche region and the output is readout through the trans-impedance amplifier discussed earlier for noise cancellation null-based reading. We then convert the output signal through a 12-bit ADC. An example of the extracted image, where each pixel represents the A-ISFET signal value, is also shown in Figure 6.11. The center of the image is a drop of a test sample. In addition, each section of the image is associated to the specified core.

The values of n-type and p-type ISFETs for various pH were measured at normal (V_{DS}=2.5V) and avalanche mode (V_{DS}=5.0V). The results are illustrated in Figure 6.12. As shown earlier, the avalanche multiplication significantly improves the sensitivity of the ISFETs.

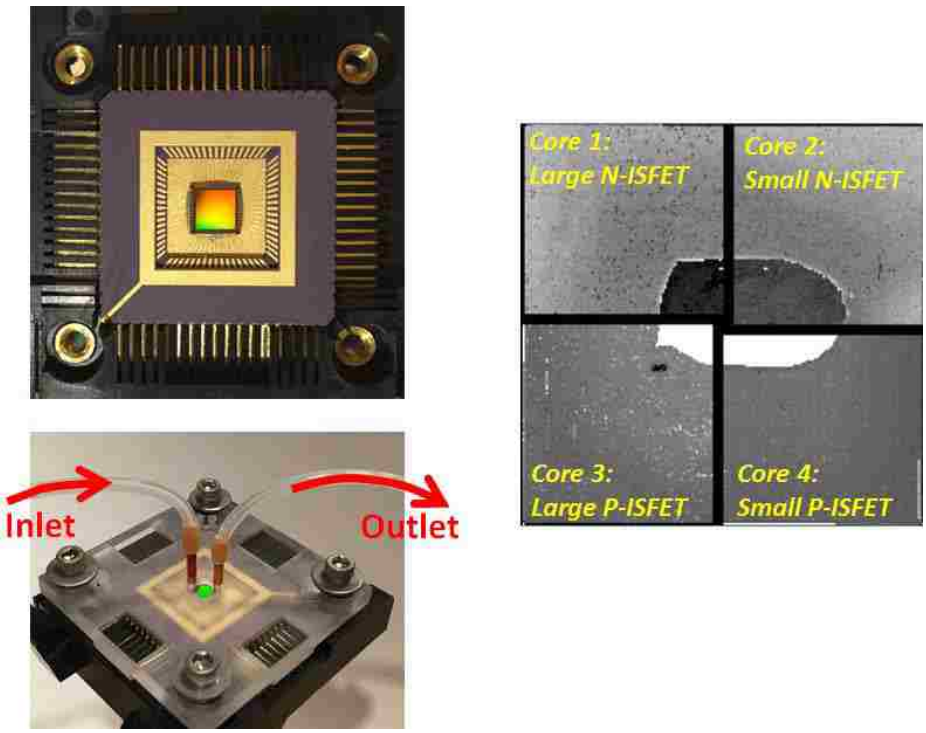

Figure 6.11: The test chip in the package and with fluidics caps. We can also see a sample image generated by A-ISFET chip. [18].

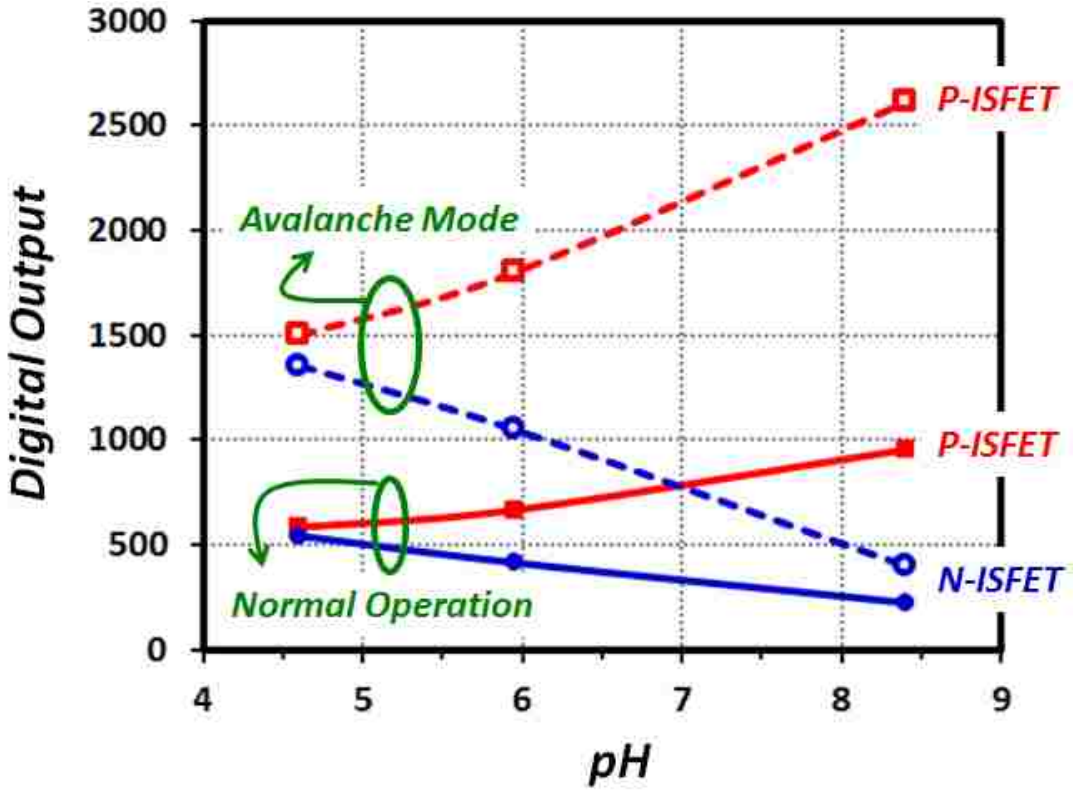

Figure 6.12: The digital output of an ISFET as a function of pH during normal operation and avalanche mode of operation [18].

To demonstrate the sensitivity of ISFET in avalanche mode versus its normal operation, one of the fabricated N-type ISFET devices with W=6µm and L=0.25µm is chosen among the devices in the test structure. The measured transconductance in normal operation as a function of V_{GS} for various V_{DS} is shown in Figure 6.13. The measured data in Figure 6.13 agrees well with the simulation data presented in [13]. As illustrated in Figure 6.13, the trans-conductance of ISFET in normal operation is maximized at 1.75mA/V when V_{GS}=1.75V and V_{DS}=2.5V.

Figure 6.14 illustrates the measured trans-conductance of the same ISFET in Figure 6.13 but operating in avalanche mode, where the V_{DS} are set beyond the 2.5V nominal voltage. This figure clearly shows the benefit of avalanche mode of operation to enhance the ISFET sensitivity. It also illustrates that the maximum multiplication gain can be achieved when V_{GS}=0.9V. For V_{DS}=6V the peak trans-conductance is 10.4mA/V (multiplication gain of about 6.0), which is consistent with the SPICE simulation results shown in chapter 2.

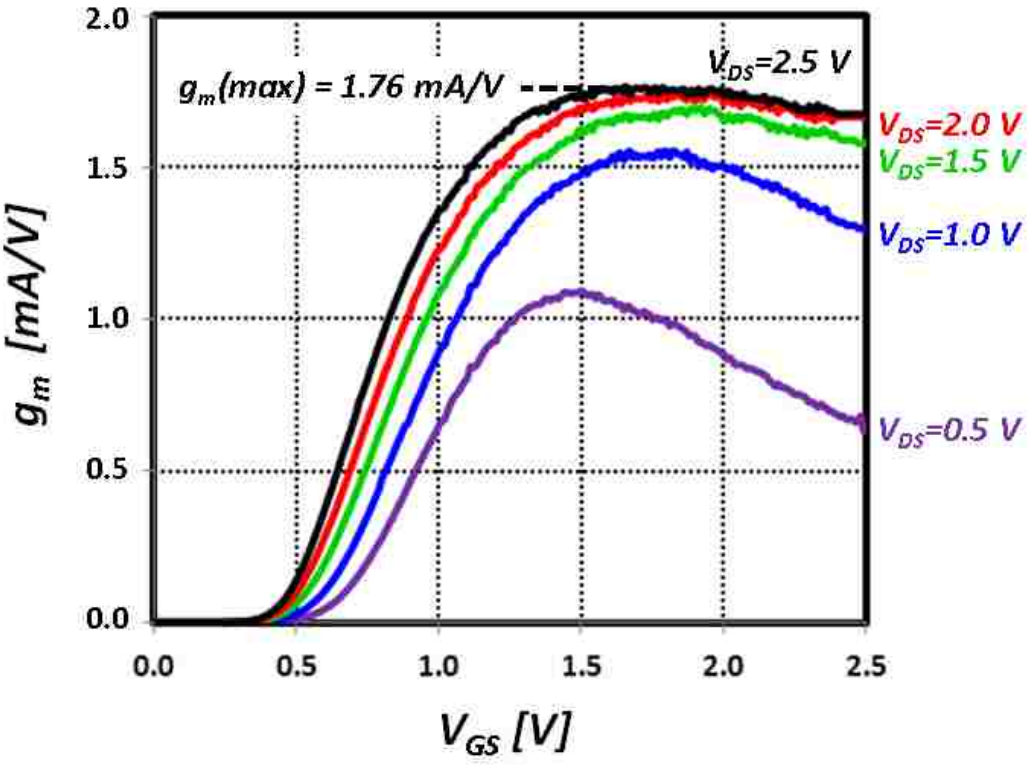

Figure 6.13: The measured ISFET trans-conductance under nominal voltages showing the maximum g_m of 1.76mA/V [18].

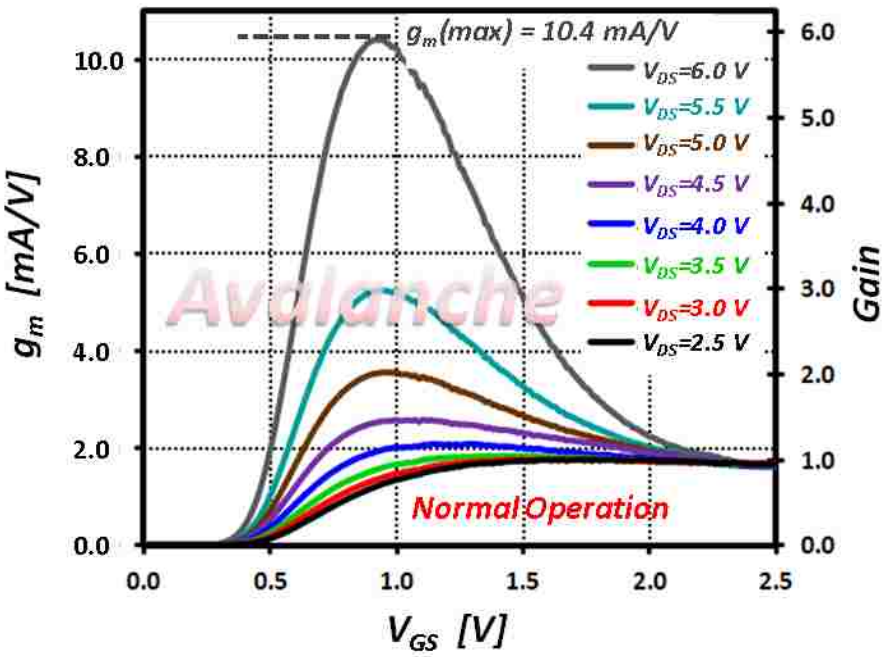

Figure 6.14: The measured ISFET trans-conductance of the same device, but under avalanche voltages, showing the maximum g_m of 10.4 mA/V [18].

Although the test result shows a high multiplication gain of 6 using an ISFET in a standard CMOS process, with fabrication process optimization (similar to an APD) the multiplication gain can be further increased.

The noise analysis will also guide us significantly in optimizing noise behavior of A-ISFET and help us to find an operating point that gives maximum signal to noise ratio (SNR).

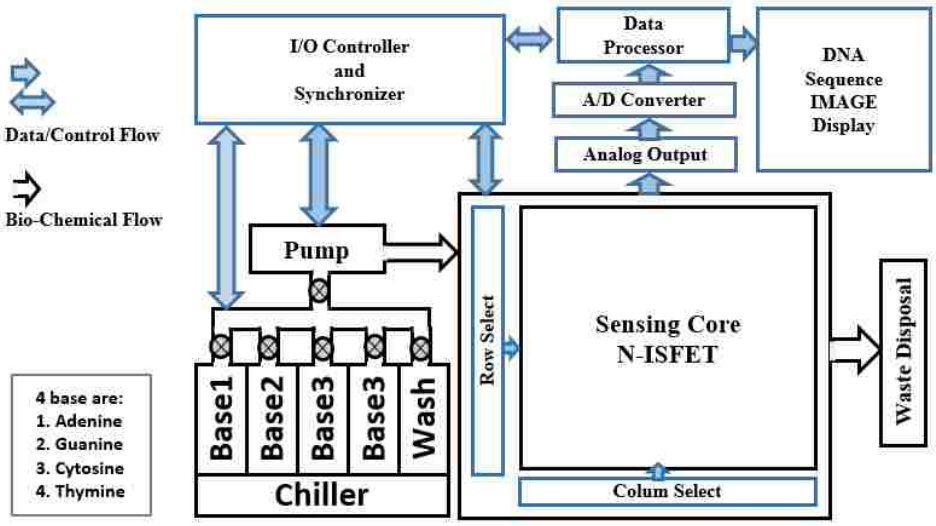

Figure 6.15: Proposed DNA sequencing system using A-ISFET chip

6.6 Proposed DNA Sequencing Procedure

The goal of this project is to come up with a design solution to overcome the high cost associated in large-scale DNA sequencing arrays. Our unique design approach helps us to improve the sensitivity from ISFET device. Therefore, we can use the same sensor at avalanche that might be limited by limit of detection parameter during normal operation. Figure 6.15 shows our proposed DNA sequencing procedure in detailed block diagram. There we can see the flow of control signal, flow of bio-chemical as well as different component that are involve in the DNA sequencing procedure. During DNA sequencing, we need to control flow of bio-chemical on DNA sequencer chip. It also needs to be initialized with right neutral solution to determine the value of background cancelling null current. The sequence of bio-chemical flow to the DNA sequencer is shown in Figure 6.16.

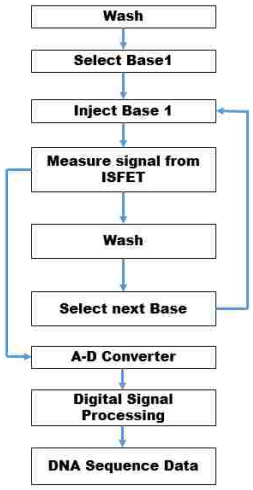

Figure.6.16.Bio-chemical process Flow Diagram for DNA sequencing

6.7 Discussions

In this chapter, the test procedure of the A-ISFET chip and the test result are discussed. The test result confirms that the transconductance during avalanche mode of operation is 6 times higher than normal mode of operation. We can increase it further by careful consideration of doping, oxide thickness and bias of A-ISFET sensor.

CHAPTER 7
CONCLUSIONS

In this dissertation, we have shown that A-ISFET is a great way to get a high sensitivity from a very small sensing device that is limited by sensitivity of the sensor. The null current based background cancellation technique ensures high resolution from the A-ISFET sensing device. Among the four different core of the A-ISFET sensing chip, the response from the N-ISFET is better as it shows better contrast. The test result also shows that N-ISFET shows a linear response with variation of pH solution at gate of ISFET input, whereas the response from the P-ISFET is nonlinear. However, we can choose either of the N-ISFET or P-ISFET device for our DNA sensing, given that we pick up a right reference point for our measurement so that we can initialize the sensor for more effective sensing within a range of pH variation. A linear response from the sensor ensures reduced post processing of the data from the sensor, whereas a non-linear response might need higher post-processing effort. The experimental results show that operation of ISFET in avalanche region can give us at least 6 times more sensitivity than the maximum sensitivity at normal region of operation with same input signal in gate of the sensor.

We further study the behavior of A-ISFET sensor from device physics, fabrication and system integration point of view to improve overall sensor performance. We have identified different noise components of A-ISFET and have modeled their respective characteristics with bias change. Different noise components that we find in A-ISFET are thermal noise, flicker noise, shot noise, and dark current noise. We have developed a model to determine the signal-to-noise (SNR) ratio of A-ISFET. The model identified that there is an optimum bias point of A-ISFET to have maximum SNR sensitivity from the sensor. Using the noise model, we can minimize the noise impact of A-ISFET sensor and maximize its SNR. The mathematical model

of SNR of the A-ISFET sensor, will extend our knowledge for quantitative understanding of the sensor, physical design issues, optimize noise and optimize DC bias.

We have also developed a physical operation-based drain current model for A-ISFET during avalanche operation. Since the A-ISFET operates in avalanche region, an accurate model for the breakdown behavior is therefore very important for both circuit design and circuit reliability point of view. Our model of A-ISFET drain current at avalanche region is due to impact ionization. To validate our drain current model of A-ISFET we perform a correlation study of the simulation data with SPICE simulation results, and experimental measured results.

Finally, we propose a DNA sequencing procedure using A-ISFET based DNA sequencing arrays. The sequencing data produced by A-ISFET sensing array have to go through extensive post processing and DSP algorithm to make accurate sequencing and prediction.

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APPENDIX A

NOISE MODEL FOR SNR SENSITIVITY OF A-ISFET

```
clc;
clear all;
close all;

for M=1:1:100

% Multiplication factor M
% k Boltzmann constant
% excess noise factor F
% keff is a function of Electric field -- E

keff=0.5;
F(M)=keff*M+(1-keff)*(2-1/M);

k=1.38064852*10^(-23); %% in SI unit joule/kelvin
T=300;
load=10000;
% it shapes the SNR curve by impacting overall noise .

q=1.6*10^-19;
f=20*10^6;
Idc=0.25*1*10^(-6);
%use for noise calculation...0.25uA current. Signal part from DC will get blocked
gm=1.76*10^(-3);
%at avalanche operation region.....use for noise calculation
gamma=2/3;
Isig=gm*18*10^(-6);
% 18uV signal

% thermal noise at Channel of ISFET
i_t_2(M)=4*k*T*gm*gamma*f;

% thermal noise from Resistance
i_2_t_2(M)=4*k*T*f/load;

% Flicker noise kf device parameter for flicker noise kf,NMOS = %2.0·10-29 AF

kf=2*10^(-29);
cox=5.3*10^(-16)/(1*10^(-6))^2;
```

```
W=5*10^(-6);
L=1*10^(-6);

i_1_f_2(M)=kf*f*gm^2/((cox)*W*L*f);

% BW should be multiplied

Ishot_2(M)=2*q*f*Idc*1*(M-1).^2*F(M);
% SHOT noise is the limiting factor - so DC bias to a very minimum DC %current value %a MUST
% Dark Current Calculation -- all dark current through pn and gets multiplied

isat=15*10^(-9);
i_d_c_2(M)=2*q*f*isat*(keff*M+(1-keff)*(2-1/M))*M.^2;

signal(M)=M.^2*Isig^2;
% noise calculation
noise(M)=Ishot_2(M)+i_t_2(M)+i_1_f_2(M)+i_2_t_2(M)+i_d_c_2(M);

figure (1);
subplot(2,2,1), loglog(1:1:M, signal(:),'r');
hold on;
subplot(2,2,1),loglog (1:1:M, noise(:),'b');
%figure (2);
subplot(2,2,2),loglog (1:1:M, i_t_2(:),'r');
hold on;
subplot(2,2,2), loglog (1:1:M, i_1_f_2(:),'b');
hold on;
subplot(2,2,2),loglog (1:1:M, Ishot_2(:),'c*');
hold on;
subplot(2,2,2),loglog (1:1:M, i_2_t_2(:),'r+');
hold on;
subplot(2,2,2),loglog (1:1:M, i_d_c_2(:),'r*');
hold on;
subplot(2,2,2), loglog(1:1:M, signal(:),'k*');
SNR(M)=signal(M)/noise(M);
%figure (3);
subplot(2,2,3),loglog (1:1:M, SNR(:))
%figure (5);
subplot(2,2,4),plot (1:1:M, F(:));

end
SNR'
```

APPENDIX B

DRAIN CURRENT MODEL OF A-ISFET AT AVALANCHE

```
close all;
clear all;
clc;

%oxide thickness
tox=0.10*10^-2;
xj=0.06*10^-2;

ld=0.22*(tox^1/3)*(xj^1/2);

E_zero=4.1*10^5;

A=42*10^5; B=12*10^5;
alpha_zero=(A/B)*ld*E_zero*exp(-B/E_zero);
taw=1.1;
r_B=100;
gamma_b=0.5;
alpha=5e-10;
vdsat=2.5;
vbrek=vdsat+(ld*E_zero*(alpha_zero)^(-1/taw));

vds=2.5:0.05:5.00;
A2=640;
B2=0.95;
C2=1.85;

nn=length(vds);
vgs=0.5:0.5:3;
kk=length(vgs);

for yy=1:1:kk

mob(yy)=A2/[1+((vgs(yy)+0.35)/B2).^C2];
bIds(yy)=(880e-6)*1/400*mob(yy)*(vgs(yy)-0.35)^2;

   for n=1:1:nn
      M(n)=(1-alpha_zero*(((vds(n)-vdsat)/(ld*E_zero))^taw))^-1;
      mm(n)=alpha_zero*(((vds(n)-vdsat)/(ld*E_zero))^taw);
      pp(n)=(vds(n)-vdsat)/(ld*E_zero);
      bb(n)=(pp(n))^taw;
```

```
        cc(n)=alpha_zero*bb(n);
        bI(yy,n)=bIds(yy)/(1-cc(n)*(1+bIds(yy)*alpha*gamma_b*r_B));
        n=n+1
    end
yy=yy+1 ;

end
plot(vds(:),bI(1,:),'b')
hold on;
plot(vds(:),bI(2,:),'r')
hold on;
plot(vds(:),bI(3,:),'c')
hold on;
plot(vds(:),bI(4,:),'g')
hold on;
plot(vds(:),bI(5,:),'v')
```

MOBILITY DEGRADATION MODEL

```
% Mobility degradation
A2=640;
B2=0.95;
C2=1.85;

vgs=-0.35:0.05:3;
kk=length(vgs);

for yy=1:1:kk
    mob(yy)=A2/[1+((vgs(yy)+0.35)/B2).^C2];
end

plot(vgs(:),mob(:))
```