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VARIATION TOLERANT ENERGY EFFICIENT DESIGN FOR
ULTRA LOW VOLTAGE DIGITAL CIRCUITS

by

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THESIS
Submitted in Partial Fulfillment of the
Requirements for the Degree of

Master of Science

Electrical Engineering

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Dedication

To my Parents.....

For their support and sacrifices

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First of all, I would like to express my special gratitude to my honorable advisor Professor Dr. Payman Zarkesh-Ha, for his endless hours of help, suggestions, ideas, advice and proper guidance throughout the whole time of my thesis. Working with Dr. Payman Zarkesh-Ha, has been a true privilege for me. His exceptional knowledge in electrical engineering area and extraordinary capability to explain difficult concepts clearly and simply has benefited me tremendously during my graduate study. He is a role model that I can always look up to. I am really thankful to him for teaching me the art of research.

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Lastly, I like to express my sincerest gratitude to Almighty God for bestowing blessings upon me.

Variation Tolerant Energy Efficient Design For Ultra Low Voltage Digital Circuits

by

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Abstract

The demand of extremely long battery life for electronic devices is the driving force for modern semiconductor industry in recent years. Supply voltage scaling offers a promising solution for this matter. To control the energy consumption and limit the power dissipation of a circuit, supply voltage should be scaled continually. Threshold voltage should also be reduced to sustain performance and reliability. This scaling of supply and threshold voltage imposes several bottlenecks in ultra-low voltage circuit design.

One of the major barriers for ultra-low voltage design is the performance deviation of digital circuit due to supply voltage variation. As technology scales, channel length, width and threshold voltage variation of the device during processing, also effect the digital circuit's characteristics. In this thesis, analytical models are derived to study the impact of process parameters and supply voltage variations on digital circuit. Based on these models, a projected 22nm process technology is used to examine the effects of device parameter

variation on ultra-low voltage digital circuit's dynamic and static behaviors. High to low propagation delay variation and noise margin (high and low) variation of an inverter are investigated. Analytical simulation results are compared with T-Spice simulation as well to verify the accuracy of the analytical models. Monte Carlo method is used on a set of 1000 samples for T-Spice simulation. Results obtained by implementing our analytical models in MATLAB are similar to the T-Spice simulation results. Both simulation results confirm that the reduction of supply voltage increases the delay and noise margin variations in an inverter circuit. Noise margin (high) variation in an inverter is more sensitive to the process related issues than noise margin (low) variation.

Another most important challenge for ultra-low voltage circuit design is to reduce the sub-threshold leakage power. A new circuit level design technique is presented in this thesis to tackle this issue. This technique allows bulk CMOS circuits to work in the sub-0.6V supply territory. The new design technique is compared with two existing leakage power reduction techniques. T-Spice simulation results suggest that, our new design can reduce the leakage power without compromising the delay of the circuit significantly. Also, our new proposed energy efficient design is more tolerant to process parameters and supply voltage variation effects. In the case of noise margin (high and low) of an inverter circuit, this new design technique is more beneficial to use than the conventional design.

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Chapter 1

Introduction

1.1 Background

As technology advances, our daily lifestyle becomes significantly dependent on the success of semiconductor industry. Computer, cell phone and other home appliances, all have complicated integrated circuits. Some of our regular use electronic devices such as modern cellular phones have functionality even more than the early decade's computers, even though their supplies comes from a battery. This passage was started in 1958, when first integrated circuit was invented. From then number of transistors on a single chip is doubled in every two or three years. In 1965, Gordon Moore showed that for any MOS transistor technology there exists a minimum cost that maximizes the number of components per integrated circuit [1]. He also predicted that as transistor dimensions are shrunk from one technology generation to the next, the minimal cost point allows doubling the number of transistors every two to three years [1]. Historically, technology scaling resulted in scaling of vertical and lateral dimensions by 0.7x each generation resulting in delay of the logic gates to be scaled by 0.7x and the integration density of logic gates to be increased by 2x [2]. Tremendous shift in the integrated circuits occurred in 1970's and 1980's, like the transitions from bipolar to PMOS, NMOS and CMOS technologies. In recent years, the number of transistors on microprocessor chips has grown at a faster rate with increasing use of on-chip cache memory, which is rising above billion–transistor

level. Ultra-modern embedded devices have continuously overcome postulated limits to technological progress. Therefore, transistors are now being manufactured with gate dimensions well below 100nm [3]. Electronic market predicts that this incredible success of the VLSI industry will be more rapid in near future.

This continuous progress of modern technologies has directed us to an era of mobile battery powered portable devices. As the success of semiconductor industry continues, extensive battery life of such popular mobile battery powered devices starts to demand more attention. The ultimate goal in design is close to having battery-less systems, because the battery contributes greatly to volume and weight. Solar power, fuel cells, and RF power are the most viable alternatives [4].One of the major challenges that circuit designers are facing in recent time is to design today's mobile battery powered electronic circuits with limited energy. And this stringent energy budget will be the major driving force for upcoming CMOS technologies. This fastest growing popularity of battery powered devices has forced the academic and industrial researchers to focus more deeply, not only just on low energy operation but also on performance and size of such devices, at the same time.

As research in ultra-low power circuit design proceeds further, supply voltage scaling becomes a more promising solution to this above mentioned power management problem. This technique gives a quadratic reduction of dynamic power. One field that is gaining interest and attraction among both corporate and scientific institutions is the concept of ultra-low power (ULP) or ultra-low energy design, which is equivalent to ultra-low voltage (ULV) design because of the relationship between power consumption or energy and voltage. This design methodology is also known as sub-threshold or near-

threshold design because the supply voltage is often lowered to values below or near the absolute value of the transistor's threshold voltage [5].

1.2 Motivation

Low power dissipation is attractive, and perhaps even essential in portable applications to have reasonable battery life and weight [4].Aggressive supply voltage scaling is the pioneer solution for soaring amount of power dissipation of an integrated circuit. However, this reduced power consumption is achieved at the expense of decreased performance. For many applications this performance reduction penalty is tolerable. For instance a significant performance penalty can be tolerated in sensor devices, energy harvesting imaging systems, and medical devices without compromising the usefulness of such devices [6]. However, for some applications performance is a critical issue. To improve performance, threshold voltage of the transistor is reduced too.

On the other hand, threshold voltage scaling results in substantial increase in the sub-threshold leakage current. As the threshold voltage decreases, sub-threshold leakage current exponentially increases [1]. Due to the substantial increase in the leakage current, the static power consumption is expected to exceed the switching component of the power consumption unless effective measures are taken to reduce the leakage power [7]. Since threshold voltage and supply voltage of a transistor are expected to be scaled regularly from one technology to another, the situation will become more deteriorated as CMOS technology proceeds further.

As number of transistors are doubled in each generation, not only billions of parasitic capacitances are charging and discharging at a high rate, but also leakage power

density is becoming extreme. Heat dissipation of modern processors is reaching the level of a hot plate. Chip temperature has reached unprecedented levels requiring expensive packaging and heat dissipation technique. Serious reliability issues arise when working at such high temperatures [1].

Another major bottleneck for ultra-low voltage operation is imposed by the process–related variation. This is mainly because leakage current strongly depends on process–related variations. For example, a slight change in sub-threshold voltage due to process variations can make severe spread in leakage current, since sub-threshold leakage current relies exponentially on threshold voltage. Fig. 1.1 shows measured I_{on} and I_{off} scatter plot for a 150nm technology [8].Even in that mature technology, there is an excessively large spread in I_{off} (100x) as compared to the 2x spread in I_{on} [9].

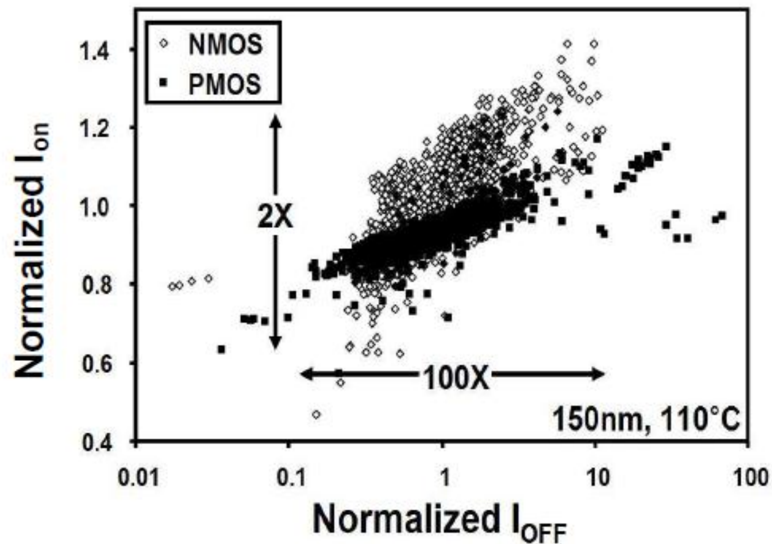

Figure 1.1: Measured I_{on} versus I_{off} scatter plot showing large spread in I_{off} for a 0.15µm technology [8]

This process related variation is predicted to increase with technology scaling. One of the main reasons of this process related variation is subwavelength lithography [9]. Extreme sensitivity to device variations in low voltage electronics has made design of such systems extremely complicated [6]. Presently used nanometer scaled circuits are fundamentally different from their predecessor technologies in that they are subject to a wide range of new effects that induce on-chip variations. The effects of variability in nanometer-scale integrated circuits cause significant deviations from the prescribed specifications for a chip. The magnitudes of these deviations, together with tight performance specifications, imply that variability is an increasingly vexing problem as technologies continue to scale [10].

Analog design was suffering from this variation issue for some time, and now it is not alone anymore; digital design is also impacted significantly in nanometer technology nodes. Process variations strongly impact different aspects of digital circuit operation. For example, in random logic, the overdrive voltage (V_{DD}-V_{th}) becomes unpredictable even for neighboring identically-sized transistors. As a result, the gate delay becomes a stochastic random variable, which complicates timing closure techniques [11-13]. Functional reliability is a major concern for circuits operating in ultra-low voltage. Yield loss probability increases and manufacturing cost due to low yield increases as a consequence. That is why it is very important to design circuit efficiently.

Another motivation for variation tolerant energy efficient design is that, the information technology industry council estimated that electricity consumption of computers in the U.S. was about 13% of the total power in 1998 with an annual growth of 2-3% [1,14].

Due to all these concerns, designing a variation tolerant, energy efficient, ultra-low voltage circuit with high yield, is the most challenging task for semiconductor industry in recent time. An ultra-low voltage circuit with lesser sub-threshold leakage current and more tolerable to process related variation facilitates competitive cost–to–performance ratio for electronic equipment.

1.3 Our Goal

- Neither the ultra-low voltage operation nor the process related variation is a new concept for CMOS logic study. Both of these topics have been addressed in several studies with high importance. But the effect of process related variability on ultra–low voltage circuit is not fully analyzed. Our primary goal is to derive analytical model to study the impact of device parameter variations on low–voltage digital circuits. A projected 22nm process technology is used to serve our purpose. For digital circuit, delay (t_{PHL}) variation and noise margin (NM_H and NM_L) variation of an inverter are considered. To analyze the effects of parameter variation, we have focused mainly on length, width, threshold voltage and supply voltage variations of a circuit.
- Our second goal is to design a more energy efficient digital logic circuit. This technique which is examined on an inverter, will not only be benefited in terms of reduced leakage power but also will be more resistant to the effects of process related variations.

1.4 Thesis Outline

This thesis is organized as follows:

- Chapter 2, presents a brief description about device and circuit characteristics at ultra-low voltage operations. Different sources of leakage current are discussed in this chapter.
- Various types of process related variability and their sources are explained in-Chapter 3.
- Then in Chapter 4, analytical models to study the effects of process parameters and supply voltage variations on digital circuit are derived. Results obtained from analytical models are compared with the T-Spice simulations in this chapter.
- We present our new design technique to reduce leakage power and parameter variation effect for digital circuit in Chapter 5. Some existing leakage power reduction techniques for digital circuits are also discussed in this chapter. Comparison results between new design and existing design techniques are presented in the latter half of Chapter 5.
- Finally, conclusions and future research directions are highlighted in Chapter 6.

Chapter 2

Ultra Low Voltage Circuit Design

2.1 Introduction

In order to increase the performance and density of transistors in an integrated circuit, CMOS devices have been scaled for more than 30 years by following Gordon More's Law. As a result, performance of microprocessors has been doubling in every two years. It is expected that for each technology generation, the delay time of a transistor will be reduced by more than 30% from its previous one. As the number of transistors on the chip becomes double, power dissipation per area increases. It is projected that by 2020, we will have one trillion transistors on a single chip [1]. Energy consumption becomes a major issue for nanometer CMOS circuits as technology progresses. To control energy consumption, supply voltage (V_{DD}) has been scaled down too in every new technologies.

The terms *low power*- and *low energy*- serves to reach the same goal, although their definitions are different. An energy efficient circuit means a low power consuming circuit also. In this paper, our main emphasis will be to reduce the power consumption of the circuit, which will in turns fulfill one of our primary goals of designing an energy efficient digital circuit.

2.2 Device and Circuit Characteristics

To minimize energy per operation and to achieve low power consumption for digital circuits V_{DD} is reduced. MOFETs then switch their operations from super-threshold ($V_{DD} > V_t$) operation in strong inversion with large gate overdrives, to near-threshold ($V_{DD} \approx V_t$) operation in weak inversion with very small overdrives, and finally into sub-threshold ($V_{DD} < V_t$) operation. Primary difference between super-threshold and sub-threshold operation is 'on' current (I_{on}). In sub-threshold region 'on' current ($I_{on\text{-}sub}$) depends exponentially on threshold voltage (V_t) and power supply voltage (V_{DD}).On the other hand, super-threshold operation 'on' current ($I_{on\text{-}super}$) is dependent on V_{th} and V_{DD} linearly (approximately).On current for super-threshold ($I_{on\text{-}super}$) in general (not considering short channel effect and channel length modulation effect) is as follows [6] :

$$I_{On-super} = \mu C_{OX}\left(\frac{W}{L}\right)\{(V_{GS} - V_t)V_{min} - \frac{{V_{min}}^2}{2}\} \tag{2.1}$$

Where $V_{min}=min\ \{(V_{GS}\text{-}V_t),\ V_{DS},\ V_{DSAT}\}$, V_{DSAT} is the drain-source voltage under velocity saturation. Now, on current for sub-threshold ($I_{on\text{-}sub}$) in general (not considering short channel effect and channel length modulation effect) is as follows [7] :

$$I_{On-sub} = \mu C_{OX}\left(\frac{W}{L}\right)(m-1){V_{TH}}^2 \exp\left(\frac{V_{GS}-V_t}{mV_{TH}}\right)\{1 - \exp\left(\frac{-V_{DS}}{V_{TH}}\right)\} \tag{2.2}$$

$$m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{\frac{\varepsilon_{si}}{W_{dm}}}{\frac{\varepsilon_{ox}}{t_{ox}}} = 1 + \frac{3t_{ox}}{W_{dm}} \tag{2.3}$$

Here, V_t is the threshold voltage, and $V_{TH} = KT/q$ is the thermal voltage. T is temperature, K is Boltzmann's constant, q is the charge of an electron. C_{ox} is the gate oxide capacitance, μ is the zero bias mobility, and m is the sub-threshold swing coefficient. W_{dm} is the maximum depletion layer width, and t_{ox} is the gate oxide thickness. C_{dm} is the capacitance of the depletion layer, and C_{ox} is the capacitance of the insulator layer, L is the

effective gate length. In long channel devices, the sub-threshold current is independent of the drain voltage for V_{DS} larger than few V_{TH} [7].

It is important to highlight the implicit V_t dependence on L in Equation (2.2) because $I_{on\text{-}sub}$ becomes very sensitive to L due to the Vt term. Vt is also dependent on V_{DS} via drain-induced barrier lowering (DIBL), which plays a role in determining the effect V_{DD} has on $I_{on\text{-}sub}$ [15].

The exponential sub-threshold $I_{on\text{-}sub}$ sensitivity to V_t drastically affects circuit behavior. First, the circuit delay and now power also depend exponentially on V_t and V_{DD}. More significantly, current matching between two FETs is exponentially dependent on any difference in V_t. For example, while a reasonable 6σ 100-mV V_t mismatch disturbs the FET current ratios by only approximately 1.17x in super-threshold operation, a similar 100-mV V_t mismatch upsets the current matching by greater than 10x in sub-threshold operation [15]. This extreme sensitivity to V_{DD} and V_t presents the most significant challenge to sub-threshold and near-threshold circuit functionality [15].

Channel length has a vital impact on sub-threshold current $I_{on\text{-}sub}$. Threshold voltage of NMOS and PMOS depends on channel length. Therefore, a minor change in gate length value due to process or temperature variation can drastically affect sub-threshold current. For short channel devices, the impact is substantial. In addition, channel length line-width variation leads to a significant disturbance in FETs drive strength matching. This creates a considerable challenge for ultra-low voltage circuit design. This problem is not so severe in the case of super-threshold operation, since current is dependent on threshold voltage either linearly or quadratically.

This drive strength mismatch effect can be reduced by increasing the gate length *L*. However, increased gate length degrades super-threshold performance, whereas sub-threshold performance is not affected as severely as super-threshold performance. This is because current can be regained with a small reduction of threshold, with no impact on the I_{on}/I_{off} ratio. More significantly, the additional capacitive loading associated with increasing gate length is significantly smaller for sub-threshold than it is for super-threshold. Sub-threshold operation at longer *L* values gives the added advantage of a steeper sub-threshold slope. Similar tradeoffs must also be considered with respect to narrow FET channel widths, *W*. However, the choice of *L* and *W* are greatly affected by the circuit application requirements [15]. Gate oxide thickness plays a key role for sub-threshold current. Reducing gate oxide thickness improves sub-threshold slope and increases sub-threshold current noticeably [15].

At the circuit level, lowering of supply voltage below sub-threshold leads to concern about noise margins, and sensitivity to process related variations. For digital CMOS logic circuits, reduction of supply voltage reduces the noise margin significantly. Minor change in process parameters makes significant variations in delay and noise margins, which causes yield loss. In analog circuits, static noise margin (SNR), circuit performance, bandwidth, and voltage swing are also degrades by supply voltage scaling. Although scaling down the threshold voltage of MOSFETs can compensate for this performance loss to some degree, the V_t scaling will results in increased power dissipation again [16]. This is one of the main bottlenecks in ultra-low voltage design. Following section gives a brief description about power consumption in a sub-threshold circuit and its sources.

2.3 Power Consumption

Today's design strategies are directed toward achieving higher speed and lower energy consumption. One of the factors which affect these parameters is power dissipation in the circuit. Due to the substantial increase in the leakage current, the static power consumption is expected to exceed the switching component of the power consumption unless effective measures are taken to reduce the leakage power [7]. Reducing power dissipation is a design goal even for non-portable devices since excessive power dissipation results in increased packaging and cooling costs as well as potential reliability problems [17]. Total power consumption in active mode for any circuit is the sum of dynamic and static power consumption. Dynamic power consumption consists of switching power and short circuit power. Therefore, the total power during active mode can be described as follows:

$$P_{Total} = P_{Dynamic} + P_{static}$$

$$= P_{Switching} + P_{Short-Circuit} + P_{static} \qquad (2.4)$$

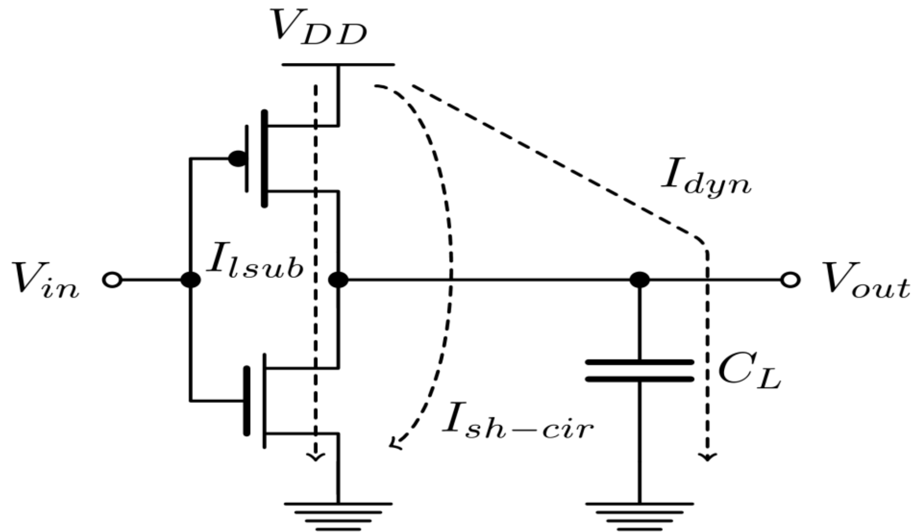

Figure 2.1: Power Consumption in an inverter [5]

Dynamic power occurs from charging and discharging of load and other parasitic capacitances of the circuit. Dynamic power can be estimated by following equation:

$$P_{Dynamic} = \alpha f C_L {V_{DD}}^2 \quad (2.5)$$

Where, f is the switching frequency, C_L is the capacitive load, V_{DD} is the supply voltage and α is the switching activity factor. Reducing any of these factors will lower the total power consumption of the circuit. Short circuit power occurs because input and output waveforms are not ideally square in real circuits; they have non-zero rise and fall time. Static power is due to non-zero current of NMOS and PMOS in off state in digital circuits or biasing current in analog circuits. $P_{Short-Circuit}$ is much smaller comparing to the other terms. Therefore, ignoring the short circuit power, the total power for active mode can be approximated as:

$$P_{Total} = \alpha f C {V_{DD}}^2 + I_{leak} * V_{DD} \quad (2.6)$$

and,

$$P_{leak} = I_{leak} * V_{DD} \quad (2.7)$$

Here, I_{leak} is the summation of all the components of the leakage currents. In the standby mode, the power dissipation is due to the standby leakage current. Different leakage mechanisms contribute to the total leakage in a device. A short description of major leakage mechanisms are described in the next section.

Leakage current (power) increases dramatically in the scaled devices. Particularly, with reduction of threshold voltage (to achieve high performance), leakage power becomes a dominant component of the total power consumption in both active and standby modes of operation. Hence, in order to suppress the power consumption in low-voltage circuits, it is necessary to reduce the leakage power in both the active and standby modes of operation. The reduction in leakage current has to be achieved using both process and circuit-level

techniques. At the process-level, the leakage current reduction can be achieved by controlling the dimensions (length, oxide thickness, junction depth, etc) and doping profile in transistors. At the circuit level, threshold voltage and leakage current of transistors can be effectively controlled by controlling the voltages of different device terminals (drain, source, gate, and body) [7].

2.4 Leakage Components

Six short-channel leakage mechanisms are illustrated in Fig. 2.2. I_1 is the reverse-bias pn junction leakage; I_2 is the sub-threshold leakage; I_3 is the oxide tunneling current; I_4 is the gate current due to hot-carrier injection; I_5 is the GIDL; and I_6 is the channel punch through current. Currents I_2, I_5 and I_6 are off-state leakage mechanisms, while I_1 and I_3 occur in both ON and OFF states. I_4 can occur in the off state, but typically it occurs during the transistor bias states in transition [18].

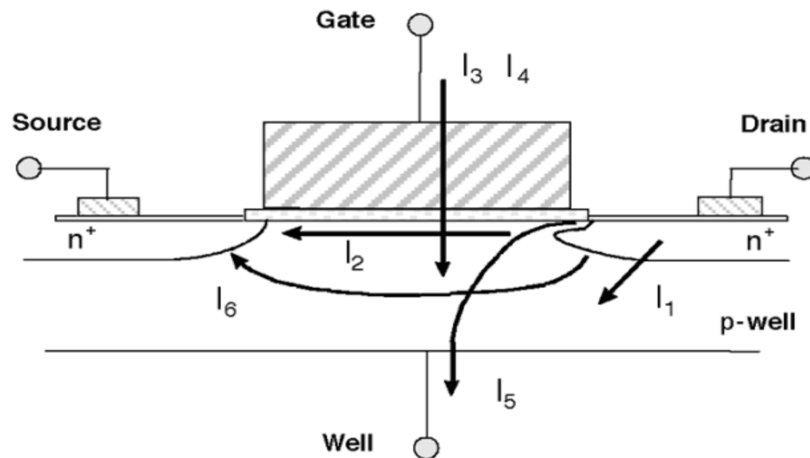

Figure 2.2 : Leakage Components in a Transistor [18]

- Minority carrier diffusion or drift near the depletion region edge and generation of electron and hole pair in the depletion region of the reversed biased junction together forms the pn junction reverse bias leakage current (I_1) in a MOSFET. I_1 is dependent on junction area and doping concentration. Band-to-Band (BTBT) tunneling dominates pn reverse junction leakage current, when heavily doped channels are used.
- Out of these six sources of leakage components, sub-threshold leakage (I_2) dominates due to the low threshold voltage. It occurs during the off sate of a MOSFET when gate-source voltage (V_{GS}) is less than threshold voltage (Vt) of the MOSFET. Sub-threshold current or the weak inversion current will be the same as of (2.2). In a short channel device, drain bias controls the threshold voltage via band bending over a significant portion of the device. As a consequence, sub-threshold current is a function of drain bias too. This effect is known as Drain Induced Barrier Lowering(DIBL).
- To get control over the gate, gate oxide thickness is reduced. This reduction of gate oxide thickness generates a high electric field across the oxide. Electrons then start to tunnel from substrate to gate and from gate to substrate. This process of tunneling through gate oxide gives rise to a leakage current known as gate oxide tunneling current (I_3).
- Due to high electric field near Si/SiO_2 interface of a short channel device, electron and holes gain sufficient energy to cross the interface potential barrier. These carriers then trapped into the oxide layer of the gate. This process is referred as hot carrier injection. The trapped hot electrons

increases the threshold voltage of a short channel device. This phenomenon is more likely for electron than hole. The current associated for this process is called the gate leakage current due to hot carrier injection (I_4).

- High field effect in the drain junction of a MOS transistor gives rise to another leakage current phenomena called Gate Induced Drain Leakage (GIDL) current (I_5). Silicon surface under the gate reaches almost same potential of p-type substrate, when the gate is biased to form an accumulation layer. Surface behaves like a p-region more heavily doped than the substrate. Depletion layer at the surface become much narrower than elsewhere, because accumulated holes are present at the surface. When the negative gate bias is large, the n+ drain region under the gate can be depleted and even inverted. This causes a dramatic increase of high field effects such as avalanche multiplication and band-to-band tunneling. As a result of all these effects, minority carriers are emitted in the drain region underneath the gate. Since the substrate is at a lower potential for minority carriers, the minority carriers that have been accumulated or formed at the drain depletion region underneath the gate are swept laterally to the substrate, completing a path for the GIDL [7].
- The depletion regions at the drain-substrate and source-substrate junctions extend into the channel in the short channel devices. The reason behind this extension is the proximity of the source and drain. The separation between the depletion boundaries decreases with the channel length as the doping is kept constant. The junctions also become closer as the reverse bias across

the junctions increases. When the combination of channel length and reverse bias leads to the merging of the depletion regions, punch through will occurred. This reduces the potential barrier for majority carrier at the source, as drain voltage increases beyond the punch through voltage (V_{PT}). More of the carriers cross the energy barrier and enter into the substrate, and the drain collects some of them. The net effect is an increase in the leakage current [7].

Sub-threshold leakage current is the largest leakage current component. It increases exponentially as a result of threshold voltage reduction. It is very important to find out an effective technique to reduce sub-threshold current. This is one of the primary concerns for ultra-low voltage design. Other than this, second most crucial concern is the variation in ultra-low voltage circuits imposed by process related issues. Next chapter will provide a details overview about effects process parameter variation in super-threshold and sub-threshold circuit design.

Chapter 3

Process Parameter Variation on Mixed Signal Circuits

3.1 Introduction

One of the effective ways of reducing both dynamic and leakage power is reducing supply voltage. However, supply voltage scaling can be achieved by sacrificing performance and efficiency of the device. The main overhead is an increased delay, as compared to circuits with nominal V_{DD}. Another vital issue for low voltage circuits is the process variability in integrated circuits, which has been previously demonstrated in several work on low voltage circuits [19-21]. Variability has been shown to be a severe limitation for sub-threshold circuits [22].

The effect of variability in nanometer-scaled circuits causes significant deviation from the prescribed specification for a chip. The magnitude of the deviations together with tight performance specifications, imply that variability is an increasingly vexing problem as technologies continue to scale. Process related variations are one-time variations that occur when a circuit is manufactured and cause process parameters to drift from their design values. These variations can impact key circuit performance characteristics: including delay, noise margin and logic threshold of digital circuits [10].

It is becoming evident that designing circuit at the nominal point, or using simple corner based approaches, are no longer viable [10]. Process variation not only effects

circuit performance but also disturbs the accuracy of leakage power estimation. Since leakage power will take significant portion of overall power consumption in the future technologies, it is important to estimate leakage power correctly. In a leakage dominant CMOS system to achieve high yields, it also becomes inevitable to identify techniques to reduce this variation and leakage power [2].

3.2 Variation Categories

Sources of variations in a circuit can be broadly categorized in to two divisions: Die-to-die (D2D) variations and Within-die (WID) variations. Figure 3.1 presents the sources of variation in a comprehensive way.

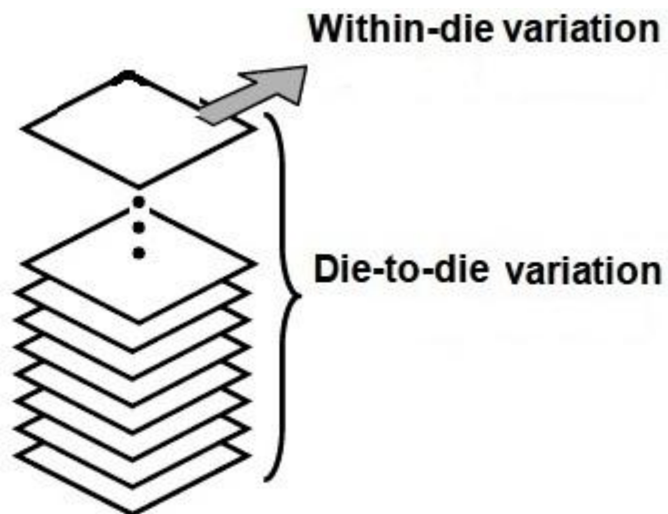

Figure 3.1: Variation categories of a circuit [2]

- **Die-to-die** variation is also known as inter-die variation or global variation. Integrated circuits are always vulnerable to this type of parameter fluctuations. Inter-die variation results from lot-to-lot, wafer-to-wafer, and

within-wafer variations. This type of variation affects every element of a chip in the same pattern. For example, die-to-die variation may cause all the transistors' gate length of a particular die to be higher than the nominal value [9]. Processing environment mainly temperature, equipment properties, wafer polishing and wafer placement are responsible for lot-to-lot and wafer-to-wafer variations. Within-wafer variation contributes to both die-to-die and within-die fluctuations. An example of within-wafer variation that can affect the die-to-die variation is the resist thickness across the wafer [23].

- **Within-die** variation is also called local or intra-die variation. Variation that occurs between two devices of the same chip is known as within-die variation. This variation creates a non-uniformity of electrical characteristics across the chip. Those parameters that vary rapidly over distances, smaller than the dimension of a die, results in within-die variations. Within-die variation may effects different devices of the same chip differently. For example, some transistors in a chip may have higher threshold voltage than others [2,23].

Within-die variation can be divided into two sub categories; random and systematic.

- **Systematic** variations are in general spatially correlated and show specific trends across the chip. Deterministic shifts of process parameters in space and time creates systematic variations on a chip. Deviations of a stepper lens is an example of such variations. It is important to note that, some of

the systematic variations on a chip are considered as random variation because of their complexity in modeling [9,24].

- **Random** variation differs randomly and independently from device to device. It is hard to model these types of variations, since sources are unknown. This type of variation changes the device behavior of a chip in a very unpredictable manner. No spatial or temporal correlation is available. One of the examples of such variation is the number of dopant atoms and their positions in a MOSFET. This effect is intrinsic and cannot be controlled externally by the manufacturing process [9,24].

Die-to-die (D2D) variations have been the prime concerns for a long time and within-die (WID) variation was neglected deliberately. However, as we entered the deep sub-micron arena, polysilicon gate length has been reduced below the wavelength of light used in optical lithography process. As a result of this complex lithography process, within-die (WID) variation has increased significantly and it is an ultimate threat for the performance of future integrated circuits. Process corners based design methodologies are no longer an effective solution for designing circuit with high accuracy [9]. In this thesis, we have given emphasis on within-die variation issue.

3.3 Sources of variation

There are several sources of variation that can deviate the performance and electrical properties of a digital circuit. In this thesis we will concentrate on variation of some of the important parameters only. We will describe primary sources of variation briefly in following subsections:

3.3.1 Random Dopant Fluctuation

The average number of dopants and their positions in a device is a random process. Still now, there is no such way to get control over the dopant atoms placement through the manufacturing process. Number of dopant atoms in a depletion region of a device is decreasing as CMOS devices are scaled down. Average number of dopant atoms in a 22nm MOSFET channel is only few tens of impurities with relatively large standard deviation. This significant amount of change in the average number of atoms varies the threshold voltages of MOSFETs in a chip enormously. Threshold voltage (V_t) of a NMOS or a PMOS depends on the number of ionized atoms in the depletion region. This fluctuation issue was anticipated long ago [9]. In earlier technologies, number of dopant atoms in a MOSFET was sufficiently large enough so that their standard deviation was not disturbing the threshold voltage deviation very much. Hence, it was not creating much problem for digital circuits but they have always been important for analog circuits [9, 24].

A pioneer work of [26-28] showed that the statistical distribution of threshold voltage variation due to random dopant fluctuation is Gaussian and its standard deviation is as follows [9]:

$$\sigma_{V_t} = \left(\sqrt[4]{2q^3 \mathcal{E}_{si} N_a \emptyset_B}\right) . \frac{t_{ox}}{\mathcal{E}_{ox}} . \frac{1}{\sqrt{3WL}} \quad (3.1)$$

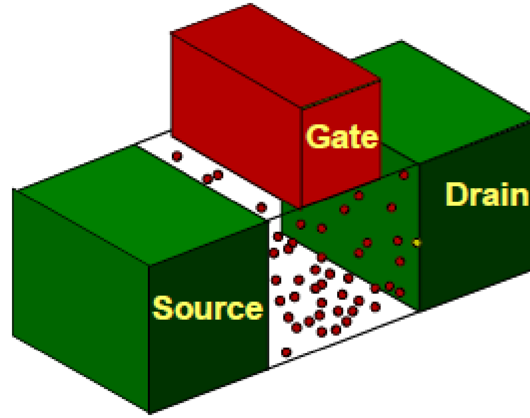

Figure 3.2 : Three-dimensional bird's-eye view of planar bulk MOSFET with randomly distributed dopants in the channel region [25]

Here q is the electron charge, $\mathcal{E}_{Si}$ and $\mathcal{E}_{ox}$ are the permittivity of the silicon and gate oxide, respectively, Na is the channel dopant concentration, $\emptyset_B$ is the difference between Fermi level and intrinsic level, t_{ox} is the gate oxide thickness, and W and L are the channel width and channel length for the transistor, respectively. Equation (3.1) implies that the threshold voltage variation is inversely proportional to the square root of effective area of the device [9]. Although it is expected from (3.1) that increasing the effective area will reduce the threshold voltage variation significantly, in practice the scenario will not be same as expected. Position of the dopant atoms will vary the threshold voltage significantly [25]. Therefore, there will be a large spread in performance and power of a device.

Figure 3.3 shows the decrease in number of dopant atoms as the channel length decreases. This decrease has been roughly proportional to $L^{1.5}$. Now a days, FETs threshold voltage variation is determined by even less than 1000 dopant atoms. Thus, it has become very tough to restrict the $\pm 3\sigma_N$ showed in figure 3.3 within a small range. That is why

random dopant fluctuation in a short channel device is getting so much attention to the designers now [9]. This variation effect is also known as “discrete dopant effect” [29].

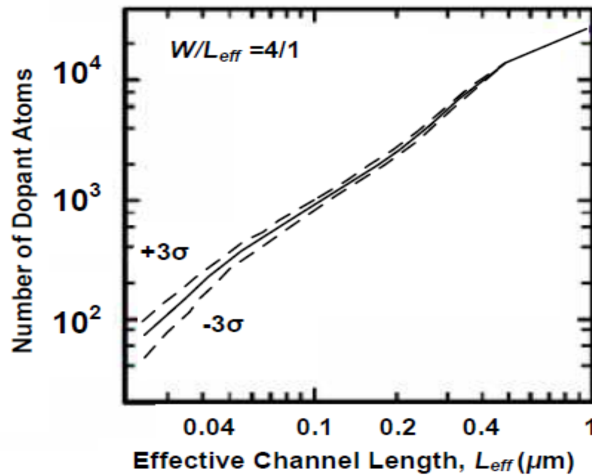

Figure 3.3: Number of dopant atoms in a depletion layer of a MOSFET vs. effective channel length [9]

3.3.2 Critical Dimension Variation

Another important process parameter that affects digital circuits is critical dimension of a device. A small variation in the device channel length or width can make a large spread in the performance and delay of a circuit. It is impossible to control this critical dimension’s variation until there is any radical change in lithography technology (e.g. Extreme Ultraviolet Lithography). Today’s technologies use feature sizes that are much smaller than the wavelength of light used in optical lithography. This results in diffraction of light, which is known as optical proximity effect (OPE). OPE is layout dependent and hence result in different critical dimension (CD) variations depending on neighboring lines as well as orientation. This makes the lithography process even more

challenging [9]. Manufacturing industries are using Optical proximity correction (OPC) and phase shift masks (PSM) to reduce this proximity effect, but still relative variation of critical dimensions are increasing [30].

Since these variations are layout dependent, they are considered as systematic intra-die variation. They have a spatial correlation across the die. The variation in transistor's channel length has direct impact on transistor's threshold voltage. The variation in threshold voltage arises due to the exponential dependence of V_t on channel length L for short channel devices, mainly due to drain induced barrier lowering (DIBL) [9]. Variations of the transistor's width (*W)* and length (*L*) directly affect its drive current, which is proportional to *W/L* [30]. Variation in the channel width (*W*) affects the threshold voltage (V_t), due to narrow channel effect. However, this effect is negligible compare to the effect of channel length variation on threshold voltage, because channel width is normally much larger than the channel length of a transistor.

3.3.3 Line Edge Roughness

Line width roughness occurs in a transistor when the width of the resist feature varies quickly over the length of the feature. When examining these variations along just one edge it is called line edge roughness (LER). LER is caused by a number of statistically fluctuating effects at these small dimensions such as shot noise (photon flux variations), statistical distributions of chemical species in the resist such as photo acid generators, the random walk nature of acid diffusion during chemical amplification, and the nonzero size of resist polymers being dissolved during development [31]. It has a direct impact on threshold voltage and channel length variation of a transistor. *Ioff /Ion* current ratio for

short channel devices also increases due to line edge roughness. It is expected to have a high threshold voltage variation due to line edge roughness in 22nm technology [9,30].

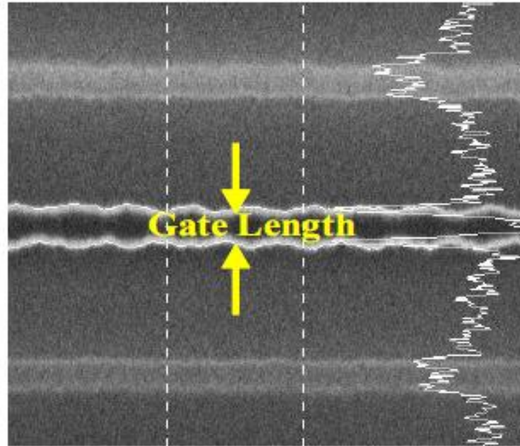

Figure 3.4 : Line edge rougness due to lithography variation [32]

3.3.4 Oxide Thickness variation

Gate oxide thickness variation during manufacturing can affect the performance and electrical properties of a circuit. However, this parameter is controlled consciously during processing. Therefore, the variation of gate oxide thickness is normally small.

3.3.5 Mobility Variation

Any variation in the mobility of hole or electron can affect the electrical properties of a transistor. Threshold voltage can be affected marginally by the mobility fluctuation. This variation can arise from several complex physical mechanisms.

3.3.6 Supply Voltage Variation

Supply voltage fluctuations are mainly caused by *IR* drop and *di/dt* noise. *IR* drop is caused by the current flow over the parasitic resistance of the power grid, whereas *di/dt*

noise is due to the parasitic inductance in combination with capacitance and resistance of the power grid and package. The superposition of both effects can not only lead to voltage drops, but also voltage overshoots. Besides fast changing power noise effects, also offsets in the voltage regulator can lead to deviations from the nominal supply voltage [30].

These are the primary sources that are responsible for performance and power variation of a mixed signal circuit. There are other sources of variations (such as temperature and interconnect) but their contributions are often negligible. Random dopant fluctuation and line edge roughness are random processes and they both have a significant effect on threshold voltage variation. For our analysis in this thesis, we will mainly focus on the impacts of threshold voltage variation, channel length and width variations and power supply voltage variation on digital circuits.

It is very important to estimate the effect of parameter variation accurately. Estimation accuracy is directly related to a company’s overall revenue. Design complexity and manufacturing cost increases due to overestimation. Conversely, an underestimation can compromise the product’s performance and overall yield [23]. To estimate the effect of variations, analytical models for digital circuit are discussed in Chapter 4.

Chapter 4

Analytical Models

4.1 Introduction

An important issue for low voltage circuits is the process variability in integrated circuits, which has been previously demonstrated in several works on low-voltage circuits. These variations can impact many key circuit performance characteristics. For digital circuits, affected parameters include: delay, noise margin and logic switching threshold of the circuit. As a result, properly analyzing the effect of process related variations on digital circuit has become the most demanding concern. To do so, an analytical model is required and a closed-form model for device variability is derived in this chapter to enable first order estimation of some fundamental circuit parameters. This analysis can be extended to develop models for the impact of variations on any circuit's parameters. To estimate the variation of device parameters, we will start with a device variation map to understand the effects properly.

4.2 Device Variation Map

For the first time, Bernstein *et al.* used experimental and measured data to illustrate a color map of device variations on I-V characteristics plot in a 65nm CMOS device as shown in Figure 4.1 [6]. The background color in the figure is indexed to the magnitude of device current variation actually observed in DC hardware characterization of the device,

operated at the specific drain-source voltage (V_{DS}), drain-source currents (I_{DS}) and implied gate-source voltage (V_{GS}) point on the plot. The red shading indicates regions of the highest device current variation, and blue shading shows areas of the lowest device current variations. The device variation map shown in Figure 4.1, is a very useful tool in understanding the impact of device variations on various circuit topologies. In this section, we develop analytical models to construct such a device variation map for any given technology node [6].

4.2.1 Assumptions

In the IC fabrication process, all device parameters are subject to deviations from their nominal values. Statistical models have been developed for transistor parameters, such as threshold voltage (ΔV_t), effective channel length (ΔL_{eff}) and device width (ΔW).In this study, we only considered these parameters as variables, but methods can be extended to any additional variables as well [6].

4.2.2 Derivations

In general the drain-source current, I_{DS} of a transistor is represented by:

$$I_{DS} = f\,(V_t, L, W) \tag{4.1}$$

Where V_t is the threshold voltage, L is the device length and W is the device width. Function f can be any analytical model that describes the device characteristics, such as alpha-power law model, unified model, or MOSFET transregional model, where it covers all regions of operations including the sub-threshold region [6].

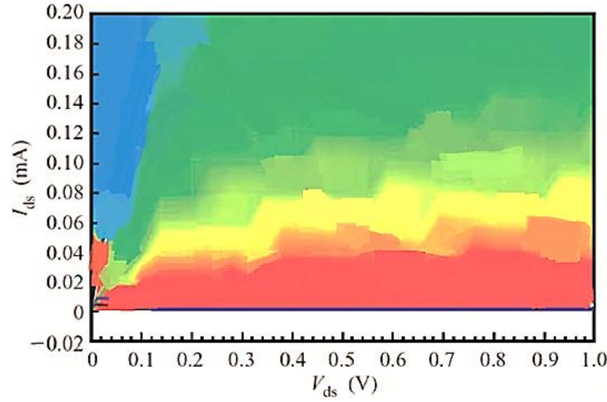

Figure 4.1. Device variation map on a 65nm NMOS I-V characteristics using experimental data [6]

Assuming that device variations are small compared to their nominal values and that they can be approximated by Gaussian distribution, the device current variation can be derived by taking partial derivative as shown below:

$$\Delta I_{DS} = \sqrt{(\frac{\partial f}{\partial V_t})^2 \Delta {V_t}^2 + (\frac{\partial f}{\partial L})^2 \Delta L^2 + (\frac{\partial f}{\partial W})^2 \Delta W^2} \quad (4.2)$$

where each term represents the contribution of variation to the associated device parameter. To simplify the derivation, the unified model is used here to represent the transistor drain-source current, I_{DS} :

$$I_{DS} = K_n^{'} \left(\frac{W}{L}\right)\left((V_{GS}\text{-}V_t)V_{min}\text{-}\frac{V_{min}^2}{2}\right)(1+\lambda V_{DS}) \quad (4.3)$$

where $V_{min}=min\{(V_{GS}\text{-}V_t),V_{DS},V_{DSAT}\}$, V_{DSAT} is the drain-source voltage under velocity saturation, K_n' is the device trans conductance, λ is the channel length modulation factor and *(W/L)* is the device aspect ratio. From partial derivative equation in (4.2) the device current variation can be derived and simplified as [6]:

$$\frac{\Delta I_{DS}}{I_{DS}} = \sqrt{(\frac{2\Delta V_t}{2(V_{GS}\text{-}V_t)V_{min}})^2+(\frac{\Delta L}{L})^2+(\frac{\Delta W}{W})^2} \quad (4.4)$$

The analytical model represented in (4.4) is the key element in generating the device

variation map shown in Figure 4.1. An example of the device variation map for a projected 22nm CMOS is shown in Figure 4.2, where it clearly agrees with the device variation map shown in Figure 4.1 [2].

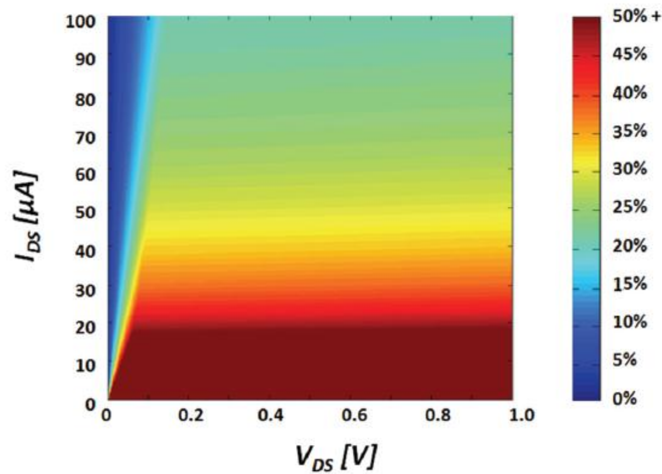

Figure 4.2. Projected Device Variation map for PTM's 22nm NMOS Device [6]

4.3 Low Voltage digital circuits under device variations

The analytical model for the device variation map derived and demonstrated in Section 4.1 is one of the main components for analyzing the impact of device variations for electronic circuits. By examining the I-V trajectory space for an NMOS circuit in electronic circuit over the device variation map, one can predict the impact of device variations under different conditions [6].

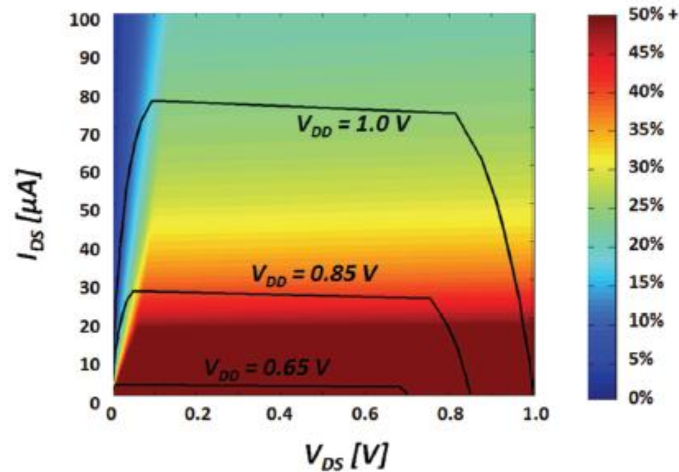

Figure 4.3. The I-V trajectory of an NMOS in an inverter under different supply voltages using PTM's 22nm device parameters [6]

For example, Figure 4.3 illustrates the I-V trajectory of a NMOS in an inverter under different supply voltages for the PTM's 22nm CMOS technology, as described in Table 4.1. Clearly, the impact of device variations is more severe in inverters with lower supply voltages, because the device spent a larger portion of the trajectory in the high (red) variation region [6].

Device	V_t	K'	V_{DSAT}	λ	(W/L)
NMOS	0.37 V	97.5 µA/V^2	0.24 V	0.06 V^{-1}	100
PMOS	0.25 V	12.0 µA/V^2	0.75 V	0.1 V^{-1}	200

Device	% ΔV_t	% ΔW	% ΔL_{eff}	% ΔV_{DD}
NMOS	4%	1.2%	2.5%	5%
PMOS	4%	1.2%	2.5%	5%

Table 4.1 : The PTM'S 22nm CMOS Device Parameters [6]

4.3.1 Propagation Delay

4.3.1.1 Ideal Square Wave (rise time=0)

To quantify the impact of parameter variations on digital circuit, we start with the high-to-low propagation delay of an inverter. All parameter values of the inverter are based on table 4.1. We will analyze both the super-threshold and sub-threshold region of operations of the inverter. It is important to note that, our main interest in this thesis project is to model a simple and accurate delay variation model that can help us to discover different design compromises, rather than modeling the propagation delay accurately. Therefore, our models will be simplified but not too precise. To simplify the analysis we use unified model for current equation. Similar analysis can be done for low-to-high propagation delay of the inverter also. In the following sections operating region of NMOS is determined based on the PTM's 22nm CMOS technology parameters but the derived equations for different operating regions of NMOS are universal and can be used for other technologies as well by identifying the proper region of operation.

A. Super-threshold circuit ($V_{DD} \geq V_t$)

Considering a perfect square wave as an input signal in the gate (V_G=V_{DD}), the propagation delay (t_{pHL}) of an inverter can be expressed by the following equation:

$$t_{pHL} = \frac{C_L V_{DD}}{2 I_{ON}} \tag{4.5}$$

where,

$$I_{on} = k_n' \left(\frac{W}{L}\right)_n \{(V_{GS} - V_{t,n})V_{min} - \frac{V_{min}^2}{2}\} \tag{4.6}$$

and

$$V_{min} = min\{(V_{GS}\text{-}V_{t,n}), V_{DS}, V_{DSAT}\}$$

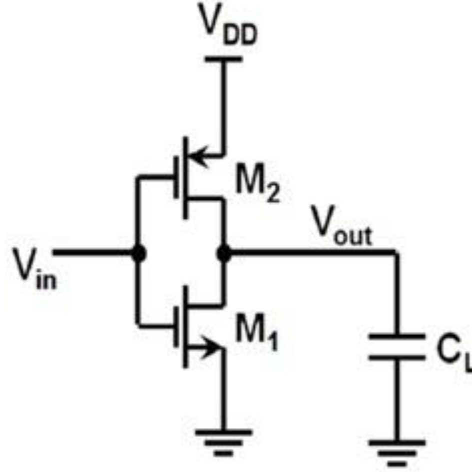

Figure 4.4. An Inverter circuit [6]

(i) For V_{DD} = 0.62V to 1V

NMOS will be in velocity saturation region, because $V_{DSAT,n} < V_{GS}-V_{t,n} < V_{DS}$. So, t_{pHL} will be –

$$t_{pHL} = \frac{C_L V_{DD}}{2k_n'\left(\frac{W}{L}\right)_n \{(V_{GS}-V_{t,n})V_{DSAT,n} - \frac{(V_{DSAT,n})^2}{2}\}}$$

$$= \frac{C_L V_{DD}}{2k_n'\left(\frac{W}{L}\right)_n \{(V_{DD}-V_{t,n})V_{DSAT,n} - \frac{(V_{DSAT,n})^2}{2}\}} \quad (4.7)$$

Now by taking partial derivatives of equation (4.7) with respect to $V_{DD}, V_{t,n}, L$ and W, we can find the effect of each parameters individually:

(a) $$\frac{\partial t_{pHL}}{\partial V_{DD}} = \frac{-C_L(V_{DSAT,n}V_{t,n} + \frac{(V_{DSAT,n})^2}{2})}{2k_n'\left(\frac{W}{L}\right)_n\left(V_{DD}V_{DSAT,n} - V_{DSAT,n}V_{t,n} - \frac{(V_{DSAT,n})^2}{2}\right)^2}$$

(b) $$\frac{\partial t_{pHL}}{\partial V_{t,n}} = \frac{C_L V_{DD} V_{DSAT,n}}{2k_n'\left(\frac{W}{L}\right)_n\left(V_{DD}V_{DSAT,n} - V_{DSAT,n}V_{t,n} - \frac{(V_{DSAT,n})^2}{2}\right)^2}$$

(c) $\frac{\partial t_{pHL}}{\partial L} = \frac{C_L V_{DD}}{2k_n'(W)_n\left(V_{DD}V_{DSAT,n} - V_{DSAT,n}V_{t,n} - \frac{(V_{DSAT,n})^2}{2}\right)}$

(d) $\frac{\partial t_{pHL}}{\partial W} = \frac{-C_L V_{DD} L}{2k_n'(W^2)_n\left(V_{DD}V_{DSAT,n} - V_{DSAT,n}V_{t,n} - \frac{(V_{DSAT,n})^2}{2}\right)}$

Assuming that the variations of device parameters are small compared to their nominal values and they can be approximated by the Gaussian distribution, the inverter delay variation can be derived by as shown below:

$$\Delta t_{pHL} = \sqrt{\left(\frac{\partial t_{pHL}}{\partial V_{DD}}\right)^2 \Delta V_{DD}{}^2 + \left(\frac{\partial t_{pHL}}{\partial V_t}\right)^2 \Delta V_{t,n}{}^2 + \left(\frac{\partial t_{pHL}}{\partial L}\right)^2 \Delta L^2 + \left(\frac{\partial t_{pHL}}{\partial W}\right)^2 \Delta W^2} \quad (4.8)$$

From partial derivative equation in (4.8) the inverter delay variation can be derived and simplified as :

$$\frac{\Delta t_{pHL}}{t_{pHL}} = \sqrt{\left(\frac{V_{DSAT,n}+2V_{t,n}}{2V_{DD}\text{-}2V_{t,n}-V_{DSAT,n}} . \frac{\Delta V_{DD}}{V_{DD}}\right)^2 + \left(\frac{2\Delta V_{tn}}{2V_{DD}\text{-}2V_{t,n}-V_{DSAT,n}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2} \quad (4.9)$$

In addition, the variation of low-to-high propagation delay can be modeled by an equation analogous to (4.9). Using the device parameters for 22nm technology node given in Table 4.1 and the analytical model in (4.9), the plot of delay variation components versus supply voltage is illustrated in Figure 4.5. As expected, reducing supply voltage results in a very large delay variation. However, the analytical model shown in (4.9) provides the contribution of each variability component, separately. Figure 4.5 shows that, for analytical model presented in (4.9), V_{DD} and V_t are dominant source of uncertainty, especially when supply voltage is reduced below 0.8V. According to Figure 4.5, the impacts of channel length and device width variations on delay of digital circuits are negligible. For V_{DD} = 0.62V, total variation is around 25%, where V_{DD} variation contributes mostly by 22%. L and W variations contributes only 2.5% and 1.2%, respectively. 4% V_t variation

can make around 15% delay variation for an inverter circuit.

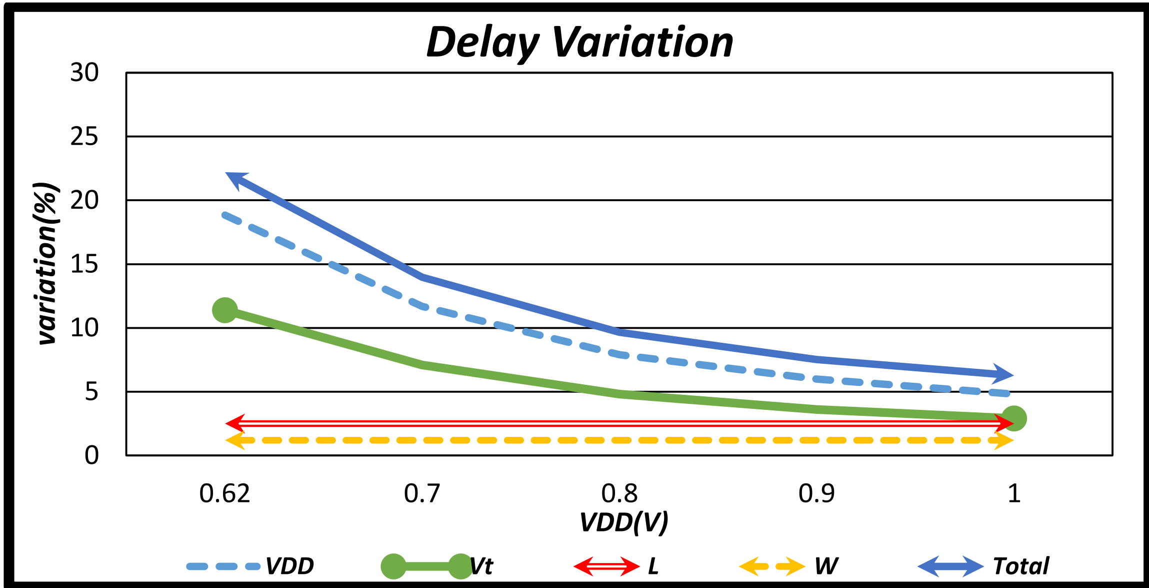

Figure 4.5. Delay variation versus supply voltage for an inverter in PTM's 22nm technology node. (Velocity saturation)

(ii) For V_{DD} = 0.37V to 0.61V

NMOS will be in saturation region, because V_{GS}-$V_{t,n}$ < $V_{DSAT,}n$ < V_{DS}. Therefore, t_{pHL} will be:

$$t_{pHL} = \frac{C_L V_{DD}}{k_n'\left(\frac{W}{L}\right)_n (V_{GS}-V_{t,n})^2}$$

$$= \frac{C_L V_{DD}}{k_n'\left(\frac{W}{L}\right)_n (V_{DD}-V_{t,n})^2} \qquad (4.10)$$

Now by taking partial derivatives of equation (4.10) with respect to $V_{DD}, V_{t,n}, L$ and W we can find out the effect of each parameters individually:

$$(a)\ \frac{\partial t_{pHL}}{\partial V_{DD}} = \frac{-C_L(V_{DD}+V_{t,n})}{k_n'\left(\frac{W}{L}\right)_n (V_{DD}-V_{t,n})^3}$$

$$(b)\ \frac{\partial t_{pHL}}{\partial V_{t,n}} = \frac{2C_L V_{DD}}{k_n'\left(\frac{W}{L}\right)_n \left(V_{DD} - V_{t,n}\right)^3}$$

$$(c)\frac{\partial t_{pHL}}{\partial L} = \frac{C_L V_{DD}}{k_n'(W)_n\left(V_{DD} - V_{t,n}\right)^2}$$

$$(d)\frac{\partial t_{pHL}}{\partial W} = \frac{-C_L V_{DD} L}{k_n'(W^2)_n\left(V_{DD} - V_{t,n}\right)^2}$$

Like previous case, assuming that the variation of device parameters are small compared to their nominal values and they can be approximated by the Gaussian distribution, the inverter delay variation can be derived by as shown below:

$$\Delta t_{pHL} = \sqrt{(\frac{\partial t_{pHL}}{\partial \mathrm{V_{DD}}})^2 \Delta \mathrm{V_{DD}}^2 + (\frac{\partial t_{pHL}}{\partial \mathrm{V_t}})^2 \Delta \mathrm{V_{t,n}}^2 + (\frac{\partial t_{pHL}}{\partial \mathrm{L}})^2 \Delta \mathrm{L}^2 + (\frac{\partial t_{pHL}}{\partial \mathrm{W}})^2 \Delta \mathrm{W}^2} \quad (4.11)$$

From partial derivative equation in (4.11) the inverter delay variation can be derived and simplified as:

$$\frac{\Delta t_{pHL}}{t_{pHL}} = \sqrt{(\frac{\mathrm{V_{DD}+V_{t,n}}}{\mathrm{V_{DD}\text{-}V_{t,n}}} . \frac{\Delta \mathrm{V_{DD}}}{\mathrm{V_{DD}}})^2 + (\frac{2\Delta \mathrm{V_{tn}}}{\mathrm{V_{DD}\text{-}V_{t,n}}})^2 + (\frac{\Delta \mathrm{L}}{\mathrm{L}})^2 + (\frac{\Delta \mathrm{W}}{\mathrm{W}})^2} \quad (4.12)$$

Plot of delay variation components versus supply voltage is illustrated in Figure 4.6. Like the model of (4.9), reducing supply voltage results in a very large delay variation. Figure 4.6 show that from analytical model presented in (4.12), V_{DD} and V_t are dominant source of uncertainty, again. According to figure 4.6, the impacts of channel length and device width variations are negligible on delay variation in this case too. For $V_{DD} < 0.5$V, total variation is no more tolerable; because the overall variation becomes more than 50%. Near threshold voltage overall variation is even more than 100%. For V_{DD}=0.4V total variation is 161%, where V_{DD} variation contributes mostly by 128%. L and W variations

contributes only 2.5% and 1.2% respectively. V_t variation can effect as much as around 100% delay variation for an inverter circuit.

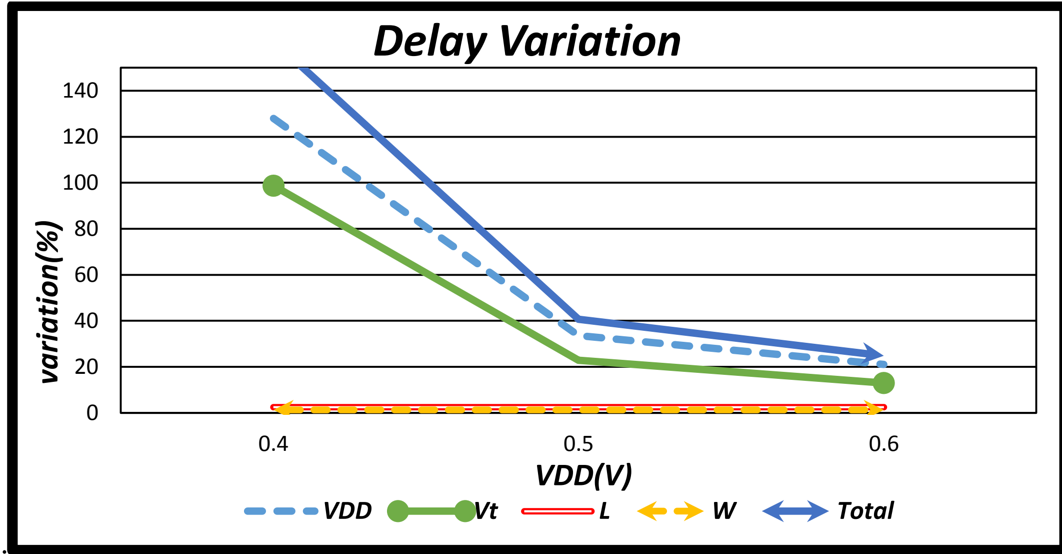

Figure 4.6. Delay variation versus supply voltage for an inverter in PTM's 22nm technology node. (Saturation)

B. Sub-threshold circuit ($V_{DD} < V_t$)

When the supply voltage is less than the threshold voltage, transistor operates in sub-threshold region and current that passes through the transistor is called 'off current' or 'leakage current'. This off current is also known as sub-threshold conduction current. In a sub-threshold circuit, this leakage current is the driving force of logic circuit functionality. Considering a perfect square wave as an input signal in the gate, propagation delay (t_{pHL}) of an inverter operating in the sub-threshold region can be expressed by the following equation:

$$t_{pHL} = \frac{C_L V_{DD}}{2 I_{ON}} \quad (4.13)$$

where, $$I_{ON} = k_n' \left(\frac{W}{L}\right)(m-1){V_{TH}}^2 \exp\left(\frac{V_{GS}-V_{t,n}}{mV_{TH}}\right)\{1-\exp\left(\frac{-V_{DS}}{V_{TH}}\right)\} \quad (4.14)$$

Since, $V_{DS} \gg V_{TH}$, $\exp\left(\frac{-V_{DS}}{V_{TH}}\right) \approx 0$. Therefore,

$$t_{pHL} \approx \frac{C_L V_{DD}}{2k_n'\left(\frac{W}{L}\right)_n (m-1){V_{TH}}^2 \exp\left(\frac{V_{DD}-V_{t,n}}{mV_{TH}}\right)} \quad (4.15)$$

Now taking partial derivatives of equation (4.15) with respect to the process parameters, we can find the followings:

$$(a) \frac{\partial t_{pHL}}{\partial V_{DD}} = \frac{C_L(1-\frac{V_{DD}}{mV_{TH}})}{2k_n'\left(\frac{W}{L}\right)_n (m-1){V_{TH}}^2 \exp\left(\frac{V_{DD}-V_{t,n}}{mV_{TH}}\right)}$$

$$(b) \frac{\partial t_{pHL}}{\partial V_{t,n}} = \frac{-C_L V_{DD}(\frac{1}{mV_{TH}})}{2k_n'\left(\frac{W}{L}\right)_n (m-1){V_{TH}}^2 \exp\left(\frac{V_{DD}-V_{t,n}}{mV_{TH}}\right)}$$

$$(c) \frac{\partial t_{pHL}}{\partial L} = \frac{C_L V_{DD}}{2k_n'(W)_n (m-1){V_{TH}}^2 \exp\left(\frac{V_{DD}-V_{t,n}}{mV_{TH}}\right)}$$

$$(d) \frac{\partial t_{pHL}}{\partial W} = \frac{-C_L V_{DD}.L}{2k_n'(W^2)_n (m-1){V_{TH}}^2 \exp\left(\frac{V_{DD}-V_{t,n}}{mV_{TH}}\right)}$$

Assuming like the other cases, that the variation of device parameters are small compared to their nominal values and they can be approximated by the Gaussian distribution, the inverter delay variation can be derived and simplified as:

$$\frac{\Delta t_{pHL}}{t_{pHL}} = \sqrt{\{(1-\frac{V_{DD}}{mV_{TH}}).\frac{\Delta V_{DD}}{V_{DD}}\}^2 + (\frac{\Delta V_{t,n}}{mV_{TH}})^2 + (\frac{\Delta L}{L})^2 + (\frac{\Delta W}{W})^2} \quad (4.16)$$

Plot of delay variation components versus supply voltage in the sub-threshold circuit is illustrated in Figure 4.7. Unlike the models of (4.9) and (4.12), reducing supply

voltage results in a reduction of overall delay variation. Figure 4.7 shows that, for analytical model presented in (4.16), V_t is the dominant source of delay variation. From Figure 4.7, the impacts of channel length and device width variations are negligible for delay variation and their contributions do not change with the supply voltage. For V_{DD}=0.3V, total delay variation is 31%, whereas for V_{DD}=0.09V variation is 25%. Delay variation in an inverter due to threshold voltage (V_t) variation is constant for the sub-threshold operation and it is fixed at 25%. However, delay variation due to V_{DD} variation changes; 5% of V_{DD} variation can create 20% delay variation for an inverter when supply voltage is 0.3V and 2.5% when supply voltage is 0.1V.

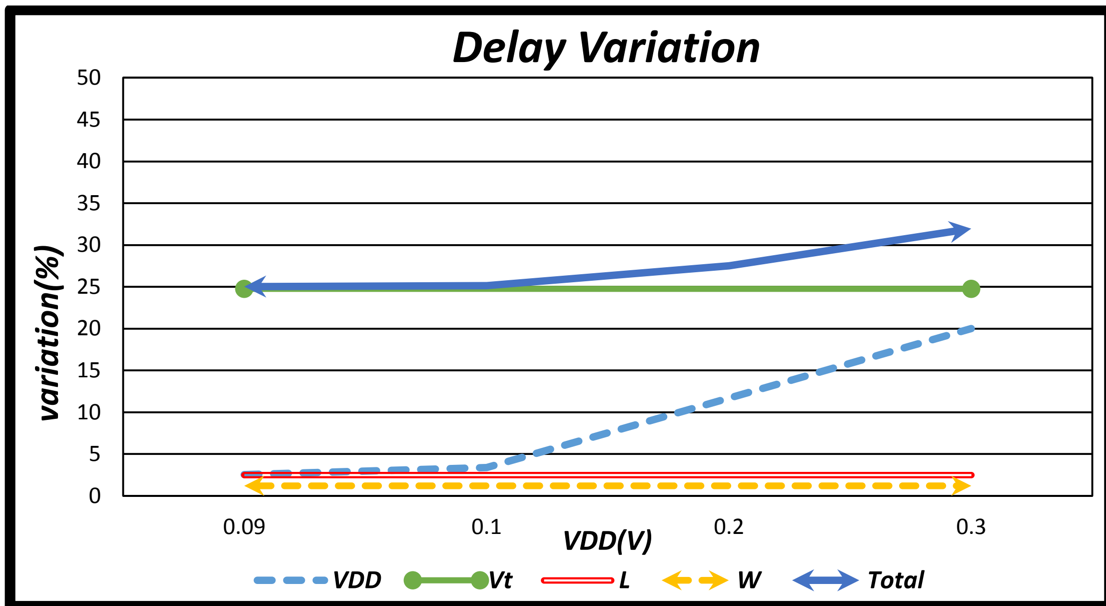

Figure 4.7. Delay variation versus supply voltage for an inverter in PTM's 22nm technology node. (Sub-threshold)

4.3.1.2 Non-ideal Square Wave (rise time≠0)

In last section, we have considered a step input signal in the gate of an inverter. However, in real circuit this assumption is not exactly correct. The dynamics of switching in a practical circuit is much more complicated and the input has a finite rise or fall times. Therefore, it is important to consider the impact of input slope on delay variation. Delay of an inverter is significantly disturbed by the finite input slew.

Since we are considering a finite input slope at the gate of an inverter, the gate voltage can be modeled as [9]:

$$V_G = \frac{t}{T_r} V_{DD} \tag{4.17}$$

where, T_r is the rise time and $0 \le t \le T_r$. Now, considering load capacitance as C_L and current through NMOS as I_n, input or output characteristics of an inverter is governed by the following differential equation [9]:

$$C_L \frac{dV_{out}}{dt} \approx -I_n \tag{4.18}$$

A. Super-threshold circuit ($V_{DD} \geq V_t$)

(i) For V_{DD} = 0.62V to 1V

In this regime NMOS is in velocity saturation region, because $V_{DSAT,n} < V_{GS}$-$V_{t,n}$ $< V_{DS}$. So, current through NMOS, I_n will be –

$$I_n = k_n' \left(\frac{W}{L}\right)_n \{\left(\frac{t}{T_r} V_{DD} - V_{t,n}\right) V_{DSAT,n} - \frac{V_{DSAT,n}{}^2}{2}\}$$

Equation (4.18) can be rewritten as –

$$\int_{V_{DD}}^{V_{out}(t)} dV_{out} = -\int_0^t \frac{k_n'}{C_L}\left(\frac{W}{L}\right)_n \left\{\left(\frac{t}{T_r}V_{DD} - V_{t,n}\right)V_{DSAT,n} - \frac{V_{DSAT,n}^{\ 2}}{2}\right\} dt \qquad (4.19)$$

Considering that the rise time, T_r is in picosecond range (result obtained from T-Spice simulation) and after simplifying (4.19), we obtain:

$$V_{out}(t) = V_{DD} - \frac{T_r k_n'}{V_{DSAT,n}V_{DD}C_L}\left(\frac{W}{L}\right)_n \{\left(\frac{t}{T_r}V_{DD} - V_{t,n}\right)V_{DSAT,n} - \frac{V_{DSAT,n}^{\ 2}}{2}\}^2 \qquad (4.20)$$

At $t = t_{pHL}$, $V_{out}(t)=V_{DD}/2$, hence (4.20) becomes-

$$\frac{t_{pHL}V_{DD}V_{DSAT,n}}{T_r} - V_{DSAT,n}V_{t,n} - \frac{V_{DSAT,n}^{\ 2}}{2} = \sqrt{\frac{V_{DD}^{\ 2}V_{DSAT,n}C_L}{T_r k_n'\left(\frac{W}{L}\right)_n}}$$

$$\Longrightarrow t_{pHL} = \frac{V_{t,n}T_r}{V_{DD}} + \frac{V_{DSAT,n}T_r}{2V_{DD}} + \sqrt{\frac{T_r C_L}{V_{DSAT,n}k_n'\left(\frac{W}{L}\right)_n}} \qquad (4.21)$$

Assuming that the variations of device parameters are small compared to their nominal values and they can be approximated by the Gaussian distribution, the inverter delay variation can be derived and simplified as:

$$\frac{\Delta t_{pHL}}{t_{pHL}} = \sqrt{\frac{(\frac{\partial t_{pHL}}{\partial V_{DD}})^2 \Delta V_{DD}^{\ 2} + (\frac{\partial t_{pHL}}{\partial V_t})^2 \Delta V_{t,n}^{\ 2} + (\frac{\partial t_{pHL}}{\partial L})^2 \Delta L^2 + (\frac{\partial t_{pHL}}{\partial W})^2 \Delta W^2}{[\frac{V_{t,n}T_r}{V_{DD}} + \frac{V_{DSAT,n}T_r}{2V_{DD}} + \sqrt{\frac{T_r C_L}{V_{DSAT,n}k_n'(\frac{W}{L})_n}}]^2}} \qquad (4.22)$$

Here,

$$(a)\frac{\partial t_{pHL}}{\partial V_{DD}} * \Delta V_{DD} = [\frac{-1}{V_{DD}}\left(\frac{V_{t,n}T_r}{V_{DD}} + \frac{V_{DSAT,n}T_r}{2V_{DD}}\right)] * \Delta V_{DD}$$

$$(b)\frac{\partial t_{pHL}}{\partial V_{t,n}} * \Delta V_{t,n} = \frac{T_r}{V_{DD}} * \Delta V_{t,n}$$

$$(c)\,\frac{\partial t_{pHL}}{\partial L} * \Delta L = \frac{1}{2}\sqrt{\frac{T_r C_L}{V_{DSAT,n} k_n{}'(W)_n (L)_n}} * \Delta L$$

$$(d)\,\frac{\partial t_{pHL}}{\partial W} * \Delta W = \frac{-1}{2}\sqrt{\frac{T_r C_L L}{V_{DSAT,n} k_n{}'(W)_n{}^3}} * \Delta W$$

The plot of delay variation components versus supply voltage is illustrated in Figure 4.8. In this example it is assumed that the input rise time is 1ps. Reducing supply voltage results in an increased delay variation. It is clear from Figure 4.8 that, for analytical model presented in (4.22), V_{DD} and V_t are dominant source of uncertainty. Impact of channel length and device width variations are negligible on delay variation in digital circuits. For V_{DD}=0.62V, total variation is around 2.2% where V_{DD} variation contributes mostly by 1.7%. L and W variations contributes only 0.95% and 0.46% respectively. V_t variation can make around 1% delay variation for an inverter circuit.

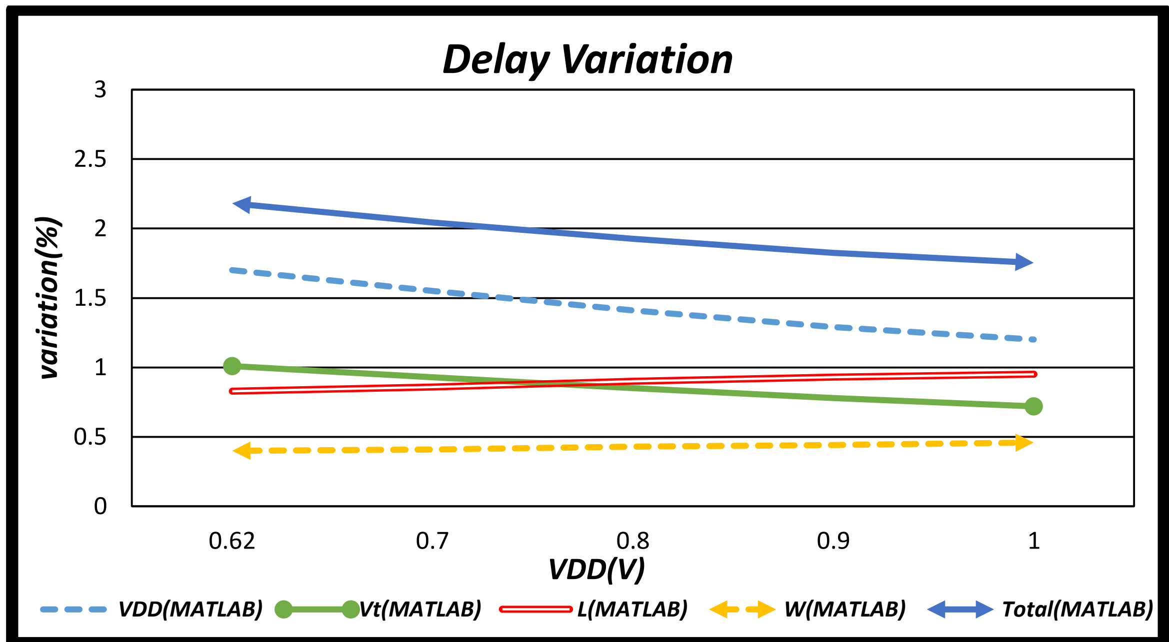

Figure 4.8. Delay variation versus supply voltage for an inverter in PTM's 22nm technology node. (Velocity saturation)

	Variation (%)									
Supply	**MATLAB**					**T-Spice**				
V_{DD}(V)	**V_{DD}**	**V_t**	**L**	**W**	**Total**	**V_{DD}**	**V_t**	**L**	**W**	**Total**
0.62	1.7	1.01	0.83	0.4	2.182	1.73	2.2	1.95	0.25	3.42
0.7	1.55	0.93	0.86	0.41	2.043	1.43	1.86	1.93	0.24	3.047
0.8	1.41	0.85	0.9	0.43	1.925	1.6	1.66	1.97	0.3	3.047
0.9	1.29	0.78	0.93	0.44	1.825	1.64	1.35	1.88	0.3	2.852
1	1.2	0.72	0.95	0.46	1.753	2	1.3	1.95	0.3	3.096

Table 4.2 : Comparison of T-Spice and MATLAB simulation results for Delay variation

(Velocity Saturation)

Results found by implying the analytical model equation in MATLAB is compared with the actual delay variation of an inverter found from T-Spice simulation. In T-Spice simulation we have used 'monte carlo' method on 1000 samples. In a real integrated circuit one inverter can drive multiple inverters of different sizes. In our T-Spice analysis, we have considered one inverter is driving another inverter of same size. And we focused on the second inverter to find the delay variation. Table 4.2 presents the results of both simulations. They are very much similar. Form Figure 4.9, we can see that, the total variation in T-Spice simulation is very close to the closed form equation developed here and implemented into MATLAB. According to T-Spice simulation, total variation for 1V supply voltage is 3.1%; from MATLAB simulation total variation for same supply voltage is 1.75%. There is only 1%-1.5% difference in both results. Therefore we can conclude by stating that our analytical model expressed by (4.22) is accurate enough to estimate the delay variation of an inverter correctly.

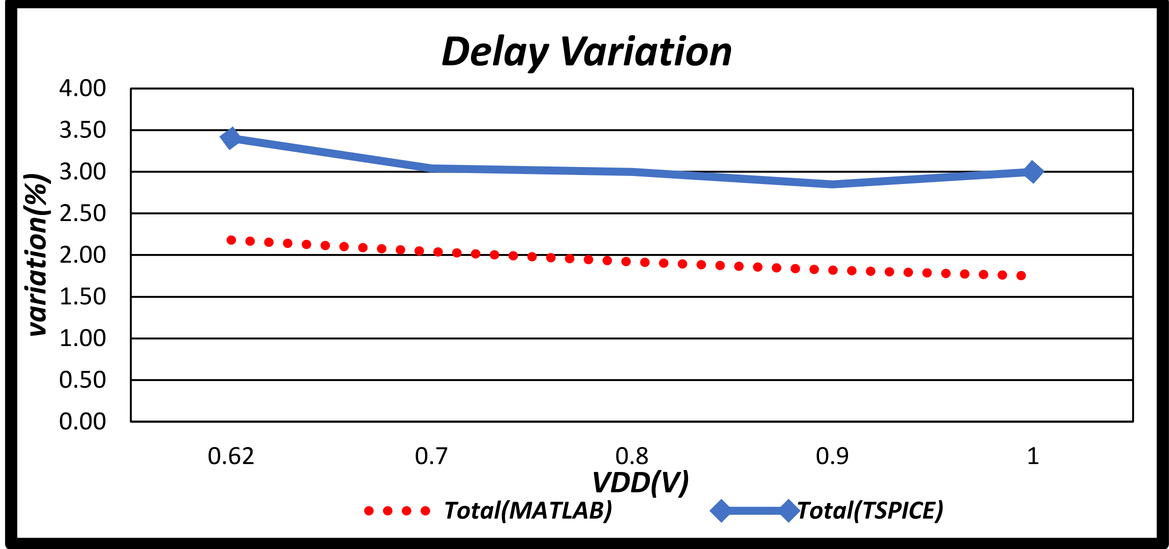

Figure 4.9. Delay variation comparison for an inverter. (Velocity Saturation)

(ii) For V_{DD} = 0.37V to 0.61V

NMOS will be in saturation region, because V_{GS}-$V_{t,n} < V_{DSAT},n < V_{DS}$. Therefore, current through NMOS, I_n will be –

$$I_n = \frac{k_n{}'}{2}\left(\frac{W}{L}\right)_n \left(\frac{t}{T_r}V_{DD} - V_{t,n}\right)^2$$

Equation (4.18) can be rewritten as –

$$\int_{V_{DD}}^{V_{out}(t)} dV_{out} = -\int_0^t \frac{k_n{}'}{2C_L}\left(\frac{W}{L}\right)_n \left(\frac{t}{T_r}V_{DD} - V_{t,n}\right)^2 dt \qquad (4.23)$$

Again, rise time, T_r will be in picosecond range (result obtained from T-Spice simulation). Based on that, after doing some simplifications (4.23) can be written as-

$$V_{out}(t) = V_{DD} - \frac{k_n{}'}{6C_L}\left(\frac{W}{L}\right)_n \frac{T_r}{V_{DD}}\left(\frac{t}{T_r}V_{DD} - V_{t,n}\right)^3 \qquad (4.24)$$

At $t = t_{pHL}$, , $V_{out}(t)$=V_{DD}/2, hence (4.24) becomes-

$$\left(\frac{t_{pHL}}{T_r}V_{DD} - V_{t,n}\right)^3 = \frac{3{V_{DD}}^2 C_L}{T_r {k_n}' \left(\frac{W}{L}\right)_n}$$

$$\Longrightarrow t_{pHL} = \left(\frac{3{T_r}^2 C_L}{{k_n}'\left(\frac{W}{L}\right)_n V_{DD}}\right)^{\frac{1}{3}} + \frac{V_{t,n}T_r}{V_{DD}} \tag{4.25}$$

Like other cases, the inverter delay variation can be derived and simplified as:

$$\frac{\Delta t_{pHL}}{t_{pHL}} = \sqrt{\frac{(\frac{\partial t_{pHL}}{\partial \mathrm{V_{DD}}})^2 \Delta \mathrm{V_{DD}}^2 + (\frac{\partial t_{pHL}}{\partial \mathrm{V_{t,n}}})^2 \Delta \mathrm{V_{t,n}}^2 + (\frac{\partial \mathrm{T_{pHL}}}{\partial \mathrm{L}})^2 \Delta \mathrm{L}^2 + (\frac{\partial t_{pHL}}{\partial \mathrm{W}})^2 \Delta \mathrm{W}^2}{[(\frac{3{T_r}^2 C_L}{{k_n}'(\frac{W}{L})_n V_{DD}})^{\frac{1}{3}} + \frac{V_{t,n}T_r}{V_{DD}}]^2}} \tag{4.26}$$

Here,

$$(a)\,\frac{\partial t_{pHL}}{\partial V_{DD}} * \Delta V_{DD} = \{-\frac{V_{t,n}T_r}{{V_{DD}}^2} - (\frac{{T_r}^2 C_L}{9\,{k_n}'\left(\frac{W}{L}\right)_n {V_{DD}}^4})^{\frac{1}{3}}\} * \Delta V_{DD}$$

$$(b)\,\frac{\partial t_{pHL}}{\partial V_{t,n}} * \Delta V_{t,n} = \frac{T_r}{V_{DD}} * \Delta V_{t,n}$$

$$(c)\,\frac{\partial t_{pHL}}{\partial L} * \Delta L = (\frac{{T_r}^2 C_L}{9\,V_{DD}{k_n}'W_n{L_n}^2})^{\frac{1}{3}} * \Delta L$$

$$(d)\,\frac{\partial t_{pHL}}{\partial W} * \Delta W = -(\frac{{T_r}^2 C_L.L}{9\,V_{DD}{k_n}'{W_n}^4})^{\frac{1}{3}} * \Delta W$$

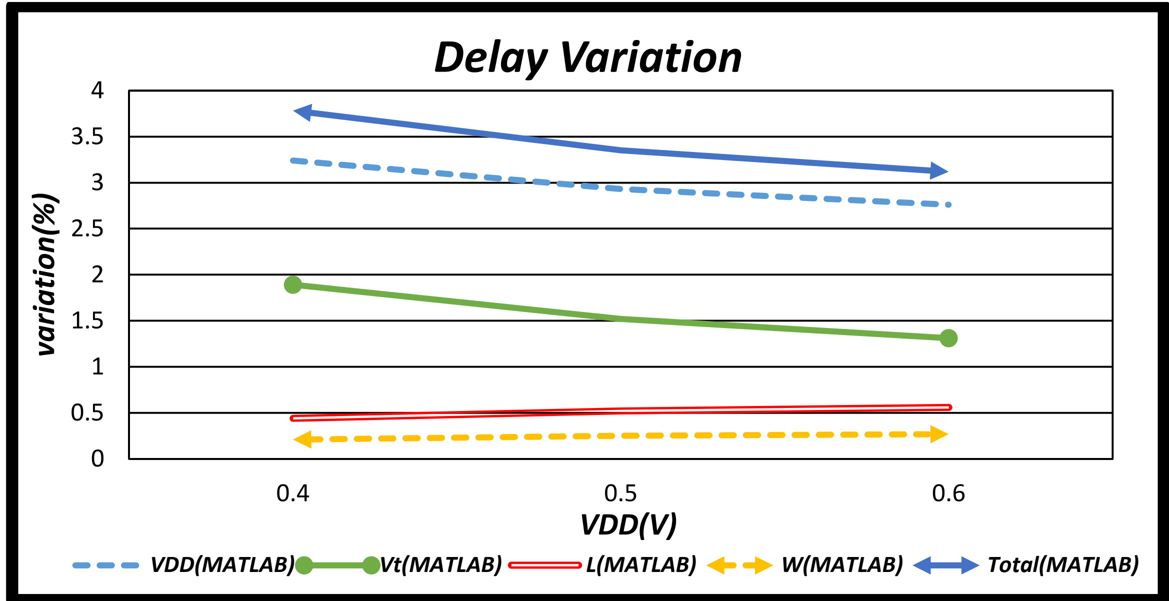

Figure 4.10. Delay variation versus supply voltage for an inverter in PTM's 22nm technology node. (Saturation)

The plot of delay variation components versus supply voltage is illustrated in Figure 4.10. Reducing supply voltage results in an increased delay variation. For analytical model presented in (4.26), V_{DD} and V_t are dominant source of delay variation. Impact of channel length and device width variations are negligible on delay variation in digital circuits.

	Variation (%)									
Supply	MATLAB					T-Spice				
V_{DD}(V)	V_{DD}	V_t	L	W	Total	V_{DD}	V_t	L	W	Total
0.4	3.24	1.89	0.44	0.21	3.783	5.24	6.11	3.17	0.36	8.658
0.5	2.93	1.52	0.52	0.25	3.351	2.5	3.4	2.3	0.25	4.81
0.6	2.76	1.31	0.56	0.27	3.118	1.73	2.2	1.95	0.25	3.42

Table 4.3 : Comparison of T-Spice and MATLAB simulation results for Delay variation (Saturation)

Simulation results of MATLAB and T-Spice can be found in table 4.3. They are very much similar. Also from figure 4.11, we can see that, the total delay variation using T-Spice simulation is very close to the results from our closed form model implemented into MATLAB. According to T-Spice simulation, total variation for 0.6V supply voltage

is 3.42 %; from MATLAB simulation total variation for same supply voltage is 3.12%. There is almost 5% difference in estimated total variation result and T-Spice result for V_{DD}=0.4V. From T-Spice result, we can see that, effect of channel length variation is not negligible. This is only major difference between analytical and T-Spice simulation results. 2.5% of channel length variation during processing can vary delay of an inverter by 3.17% when V_{DD}=0.4V.

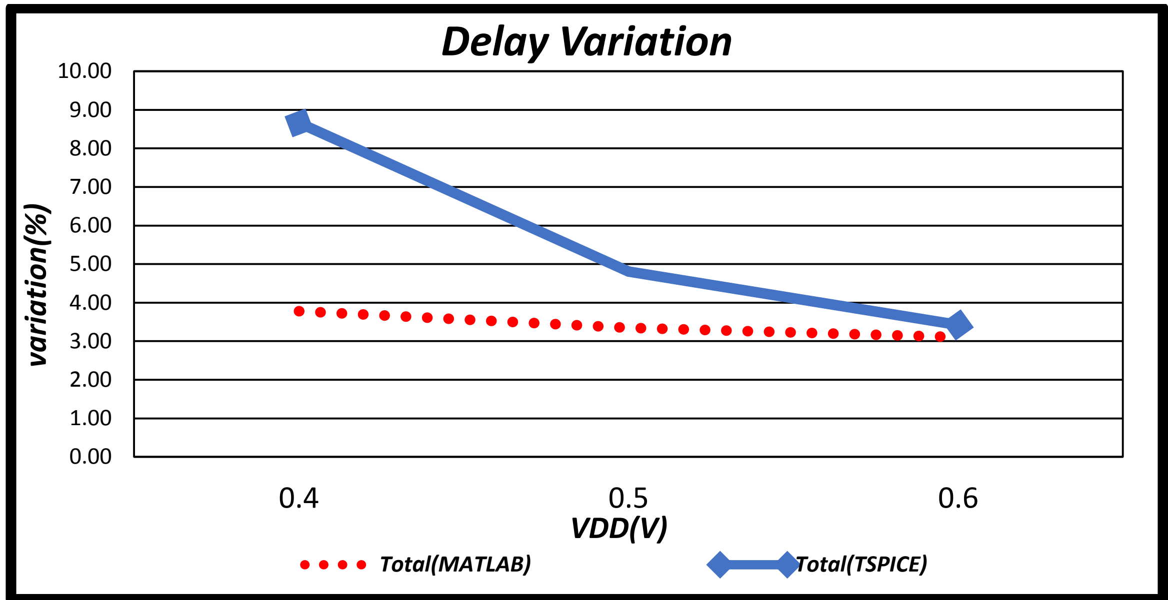

Figure 4.11. Delay variation comparison for an inverter. (Saturation)

B. Sub-threshold circuit (V_{DD}<V_t)

In this regime NMOS will be in cutoff region, because $V_{GS} < V_{t,n}$. Therefore, current through NMOS, will be –

$$I_n = k_n' \left(\frac{W}{L}\right)_n (m-1).V_{TH}^2 \exp\left(\frac{\frac{t}{T_r}V_{DD} - V_{t,n}}{mV_{TH}}\right)$$

where, m is the sub-threshold swing coefficient and V_{TH} is the thermal voltage. Then, (4.18) will be as follows –

$$\int_{V_{DD}}^{V_{out}(t)} dV_{out} = -\int_0^t \frac{k_n'}{C_L}\left(\frac{W}{L}\right)_n (m-1).V_{TH}^2 \exp\left(\frac{\frac{t}{T_r}V_{DD}-V_{t,n}}{mV_{TH}}\right) dt \qquad (4.27)$$

Rise time (T_r) will be in picosecond range (Result obtained from T-Spice simulation). After doing some simplifications (4.27) can be written as-

$$V_{out}(t) = V_{DD} - \frac{k_n'}{C_L}\left(\frac{W}{L}\right)_n (m-1).V_{TH}^2 \exp\left(\frac{\frac{t}{T_r}V_{DD}-V_{t,n}}{mV_{TH}}\right)\frac{mV_{TH}T_r}{V_{DD}} \qquad (4.28)$$

At $t = t_{pHL}$, $V_{out}(t)=V_{DD}/2$, hence (4.28) becomes-

$$\frac{\frac{t_{pHL}}{T_r}V_{DD} - V_{t,n}}{mV_{TH}} = \ln\left(\frac{C_L V_{DD}^2}{2\,k_n'\left(\frac{W}{L}\right)_n m(m-1).V_{TH}^3 T_r}\right)$$

$$\Rightarrow t_{pHL} = \frac{V_{t,n}T_r}{V_{DD}} + \frac{mV_{TH}T_r}{V_{DD}} \ln\left(\frac{C_L V_{DD}^2}{2\,k_n'\left(\frac{W}{L}\right)_n m(m-1).V_{TH}^3 T_r}\right) \qquad (4.29)$$

Let, variation of device parameters are small compared to their nominal values and they can be approximated by the Gaussian distribution, the inverter delay variation can be derived and simplified as:

$$\frac{\Delta T_{PHL}}{T_{PHL}} = \sqrt{\frac{\left(\frac{\partial T_{pHL}}{\partial V_{DD}}\right)^2 \Delta V_{DD}^2 + \left(\frac{\partial T_{pHL}}{\partial V_t}\right)^2 \Delta V_{t,n}^2 + \left(\frac{\partial T_{pHL}}{\partial L}\right)^2 \Delta L^2 + \left(\frac{\partial T_{pHL}}{\partial W}\right)^2 \Delta W^2}{\left[\frac{V_{t,n}T_r}{V_{DD}} + \frac{mV_{TH}T_r}{V_{DD}} \ln\left(\frac{C_L V_{DD}^2}{2\,k_n'\left(\frac{W}{L}\right)_n m(m-1).V_{TH}^3 T_r}\right)\right]^2}} \qquad (4.30)$$

Here,

$$(a)\, \frac{\partial T_{pHL}}{\partial V_{DD}} * \Delta V_{DD} = \{-\frac{V_{t,n}T_r}{V_{DD}^2} - \ln\left(\frac{C_L V_{DD}^2}{2\,k_n'\left(\frac{W}{L}\right)_n m(m-1).V_{TH}^3 T_r}\right)\frac{mV_{TH}T_r}{V_{DD}^2} + \frac{2mV_{TH}T_r}{V_{DD}^2}\} * \Delta V_{DD}$$

$$(b)\, \frac{\partial T_{pHL}}{\partial V_{t,n}} * \Delta V_{t,n} = \frac{T_r}{V_{DD}} * \Delta V_{t,n}$$

$$(c)\frac{\partial T_{pHL}}{\partial L} * \Delta L = \frac{mV_{TH}T_r}{V_{DD}L_n} * \Delta L$$

$$(d)\frac{\partial T_{pHL}}{\partial W} * \Delta W = \frac{-mV_{TH}T_r}{V_{DD}W_n} * \Delta W$$

The plot of delay variation components versus supply voltage is illustrated in Figure 4.12. Reducing supply voltage results in an increased delay variation. It is important to note that, for analytical model showed in (4.30), V_{DD} and V_t are dominant source of delay variation. However, for V_{DD} less than 0.2V, threshold voltage, V_t variation contribution is maximum. For V_{DD} =0.3V, delay variation due to V_{DD} variation and V_t variations are 4.13% and 2.16%, respectively. On the other hand for V_{DD} =0.09V, delay variation due to V_{DD} variation and V_t variations are 2.94% and 5.1%, respectively. Impacts of channel length and device width variations are negligible on delay variation of digital circuits. Delay variation due to V_{DD} variation decreases with the reduction of supply voltage.

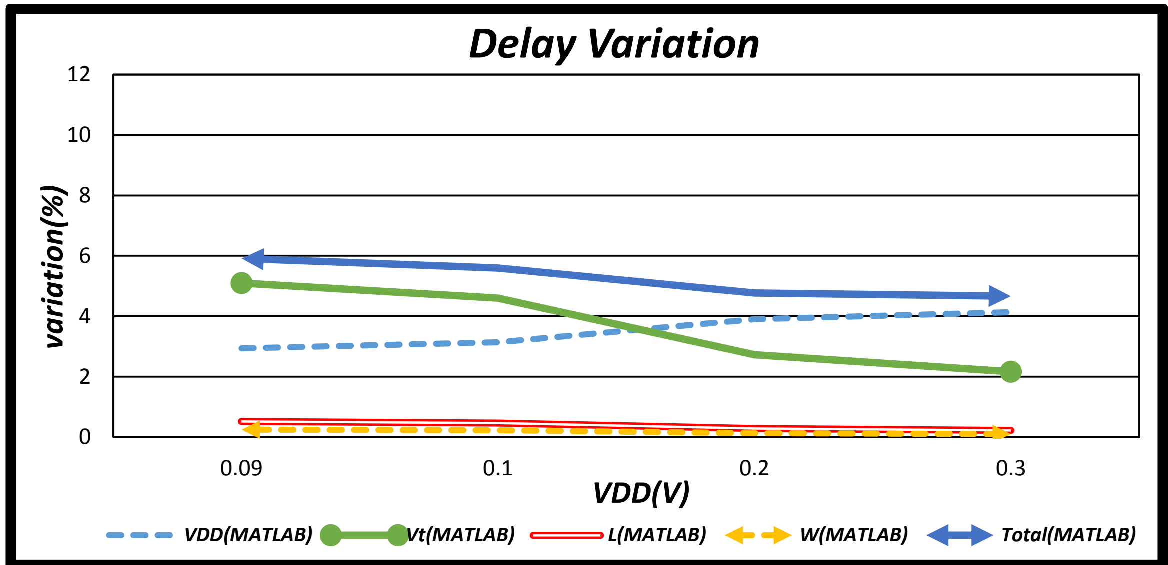

Figure 4.12. Delay variation versus supply voltage for an inverter in PTM's 22nm technology node. (Sub-threshold region)

	Variation (%)									
Supply	**MATLAB**					**T-Spice**				
V_{DD}(V)	**V_{DD}**	**V_t**	**L**	**W**	**Total**	**V_{DD}**	**V_t**	**L**	**W**	**Total**
0.09	2.94	5.1	0.52	0.25	5.92	7.45	22.78	11.86	1	26.76
0.1	3.14	4.6	0.46	0.22	5.6	3.7	17.11	4.6	1	18.127
0.2	3.9	2.73	0.28	0.13	4.77	6.31	11.76	3.9	0.33	13.908
0.3	4.13	2.16	0.22	0.1	4.67	7.12	10.1	4.02	0.34	12.999

Table 4.4 : Comparison of T-Spice and MATLAB simulation results for Delay variation (Sub-threshold)

Simulation results of MATLAB and T-Spice are presented in table 4.4. They both have the same trends. As the supply voltage reduces delay variation due to threshold voltage variation increases and thus threshold voltage variation becomes the dominant factor in both cases. However, for T-Spice simulation magnitude of this variation is much higher than the MATLAB simulation. Simulation of analytical model with MATLAB shows that, total variation due to V_{DD}, L, W and V_t variations will increase from 4.67% to 5.92% when V_{DD} reduces from 0.3V to 0.09V. But for the same range of supply voltage, actual delay variation (according to T-Spice simulation) will rise from 12.99% to 26.76%. This means that our analytical model will have deviations from actual delay variation. And this is understandable because we have not considered the DIBL and other short channel effects in our analytical model. These DIBL and other short channel effects become severe when device operate in the sub-threshold region particularly. Nevertheless, difference between two simulation results are still in a reasonable range.

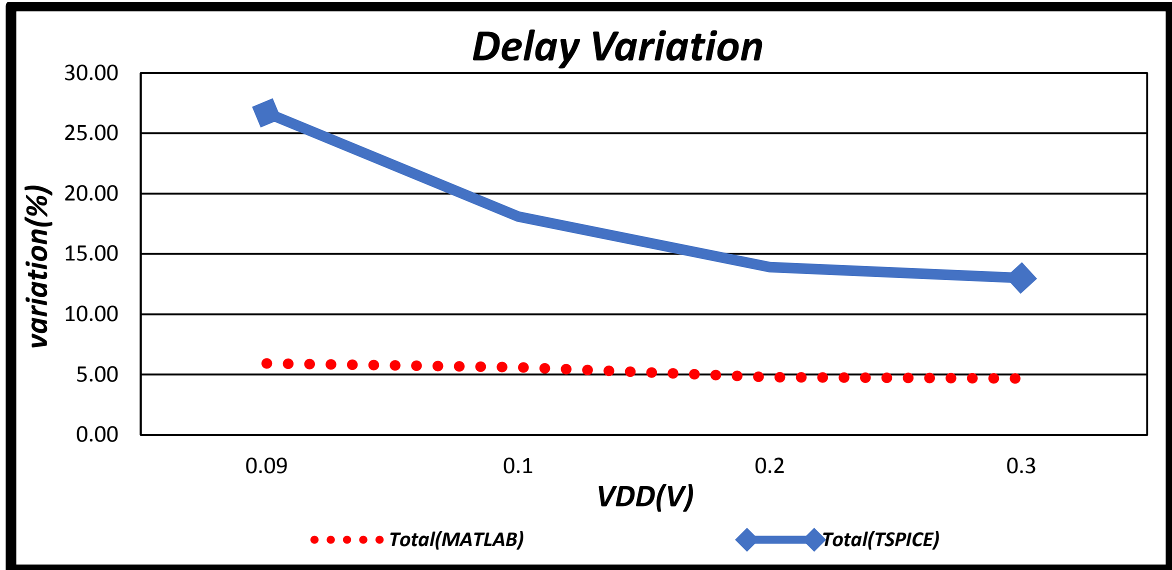

Figure 4.13. Delay variation comparison for an inverter.(Sub-threshold region)

4.3.1.3 Effect of input rise time in delay variation

Simulation results of section 4.3.1.1 and 4.3.1.2 found by implementing our analytical models in MATLAB implies that input rise time plays a vital role in delay variation of an inverter. As the rise time of the gate input becomes zero, delay variation turn out to be intolerable. Figure 4.14 illustrates the effect of input rise time on delay variation in term of T-Spice simulation. For our comparison we chose two types of inputs. One having a zero rise time (square wave) for gate input voltage and another one having a rise time of 10ps (linear input) for gate input voltage of an inverter. First one is based on theoretical assumption and the second one is more practical in a real integrated circuit. Form figure 4.14 we can see that, as the input voltage at the gate of an inverter becomes sharper, delay (t_{pHL}) variation goes too high. For higher rise time values of gate input voltage, delay variation of an inverter is very less. For a square wave input delay variation is 350% when supply voltage of the inverter is 0.5V. For V_{DD}=0.8V, delay variation for square input is 250%. On the other hand

delay variation for liner input (Tr =10ps) varies in between 3.95% to 6.13%. For 0.8V supply, delay variation due to process and supply voltage variation is only 3.95% and for 0.6V supply voltage delay variation of an inverter is only 4.51%

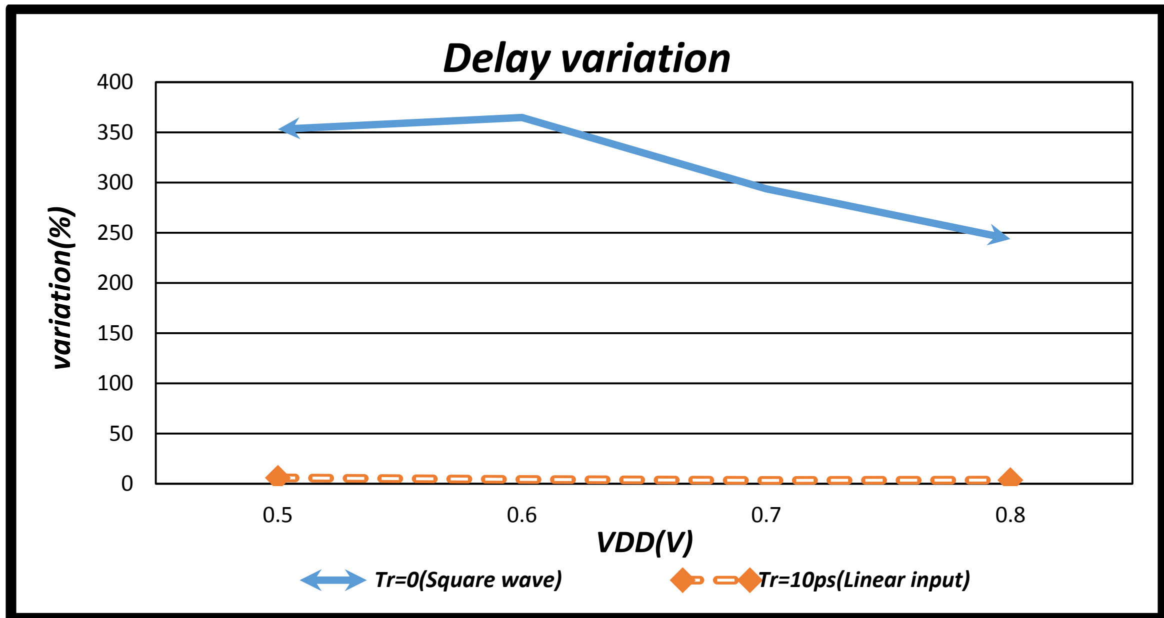

Figure 4.14: Effects of rise time on delay (t_{pHL}) variation

4.3.2. Nosie Margin:

Unwanted signals, such as noise, must be addressed in any system of logic, particularly in ultralow-power CMOS. The noise margin is the difference between a valid output logic level and an input level at which the data of a ‘‘victim’’ circuit will be corrupted. (A victim circuit is one that is subject to noise from an external source.) [15]

Region	Input Voltage V_I	Output Voltage V_o	NMOS Transistor	PMOS Transistor
1	$V_I \le V_{t,n}$	$V_{OH} = V_{DD}$	Cutoff	Linear
2	$V_{t,n} < V_I \le V_o + V_{t,p}$	High	Saturation	Linear
3	$V_o + V_{t,n} < V_I \le (V_{DD} + V_{t,p})$	Low	Linear	Saturation
4	$V_I \ge (V_{DD} + V_{t,p})$	$V_{OL} = 0$	Linear	Cutoff

Table 4.5: Operational region of transistors in an inverter ($V_{DD} \ge V_t$)

A crucial way to investigate the impact of device parameter variations in the digital circuit is to analyze the noise margin variations; both NM_L and NM_H. Operational region of a transistor in an inverter for super-threshold region of operation case ($V_{DD} \ge V_t$), is given in the above table.

4.3.2.1 Noise Margin (Low State) variation

A. Super-threshold:

Equating currents for saturated NMOS transistor and linear PMOS transistor of Region 2 gives us the following equation:

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n \left(V_{in}-V_{t,n}\right)^2 = \frac{k_p'}{2}\left(\frac{W}{L}\right)_p \left[2\left(V_{DD}-V_{in}-|V_{t,p}|\right)(V_{DD}-V_{out})-(V_{DD}-V_{out})^2\right] \quad (4.31)$$

To find the lower logic threshold of input (V_{iL}), derivation condition $\left(\frac{\partial V_{out}}{\partial V_{in}}\right) = -1$ has to be evaluated for equation (4.31); which leads us to:

$$k_n'\left(\frac{W}{L}\right)_n \left(V_{in}-V_{t,n}\right) = k_p'\left(\frac{W}{L}\right)_p \{V_{out}-V_{DD} + \left(V_{DD}-V_{in}-|V_{t,p}|\right)\left(-\frac{\partial V_{out}}{\partial V_{in}}\right) -(V_{DD}-V_{out})(-\frac{\partial V_{out}}{\partial V_{in}})\}$$

$$\Rightarrow V_{in}\text{-}V_{t,n} = \frac{k_p'\left(\frac{W}{L}\right)_p}{k_n'\left(\frac{W}{L}\right)_n}(2V_{out}\text{-}V_{DD}\text{-}V_{in}\text{-}|V_{t,p}|)$$

Let, $V_{in} = V_{iL}$ and $V_{out} = V_{OH} = V_{DD}$, then

$$V_{iL}\text{-}V_{t,n} = \frac{k_p'\left(\frac{W}{L}\right)_p}{k_n'\left(\frac{W}{L}\right)_n}(V_{DD}\text{-}V_{iL}\text{-}|V_{t,p}|)$$

$$\Rightarrow V_{iL} = \frac{V_{t,n}\frac{k_n'\left(\frac{W}{L}\right)_n}{k_p'\left(\frac{W}{L}\right)_p}+V_{DD}-|V_{t,p}|}{1+\frac{k_n'\left(\frac{W}{L}\right)_n}{k_p'\left(\frac{W}{L}\right)_p}} \tag{4.32}$$

Using (4.32) and parameter values of table 4.1 we can find the V_{iL} values of table 4.6.It is important to note that, when $V_{DD} \leq 0.6V$, then $V_{GS} < V_t$ .Therefore, (4.31) does not hold anymore. Both NMOS and PMOS are turned off. Therefore, inverter operates in sub-threshold region instead of super-threshold region.

V_{DD}(V)	V_{iL} (V)
0.4	0.326
0.5	0.346
0.6	0.366
0.7	0.386
0.8	0.406
0.9	0.425
1	0.445

Table 4.6 : V_{iL} values of an inverter(Super-threshold region)

Let, $V_{OL} = 0.$ Then the Noise margin (Low State), NM_L can be written as follows:

$$NM_L = V_{iL}\text{-}V_{0L} = V_{iL}$$

$$NM_L = \frac{V_{t,n}K_R+V_{DD}-|V_{t,p}|}{1+K_R} \tag{4.33}$$

Here,

$$K_R = \frac{K_n'}{K_p'} * \frac{(\frac{W}{L})_n}{(\frac{W}{L})_p}$$

Assuming that the variation of the device parameters are small compare to their nominal values and they can be approximated by Gaussian distribution, NM_L variation can be derived by taking the partial derivative and the equation is as following:

$$\frac{\Delta NM_L}{NM_L} = \sqrt{\frac{(\frac{\partial NM_L}{\partial V_{DD}})^2 * \Delta V_{DD}{}^2 + \left(\frac{\partial NM_L}{\partial V_t}\right)^2 * \Delta V_t{}^2 + \left(\frac{\partial NM_L}{\partial L}\right)^2 * \Delta L^2 + \left(\frac{\partial NM_L}{\partial W}\right)^2 * \Delta W^2}{(\frac{V_{DD} - |V_{Tp}| + V_{tn} * K_R}{1 + K_R})^2}} \tag{4.34}$$

Where,

(a) $\frac{\partial NM_L}{\partial V_{DD}} * \Delta V_{DD} = \frac{1}{1+K_R} * \Delta V_{DD}$

(b) $$\frac{\partial NM_L}{\partial V_t} * \Delta V_t = \sqrt{\left(\frac{\partial NM_L}{\partial V_{t,p}} * \Delta V_{t,p}\right)^2 + \left(\frac{\partial NM_L}{\partial V_{t,n}} * \Delta V_{t,n}\right)^2}$$

$$= \sqrt{\left(\frac{-1}{1 + K_R} * \Delta V_{t,p}\right)^2 + \left(\frac{K_R}{1 + K_R} * \Delta V_{t,n}\right)^2}$$

(c) $$\frac{\partial NM_L}{\partial L} * \Delta L = \sqrt{\left(\frac{\partial NM_L}{\partial L_n} * \Delta L_n\right)^2 + \left(\frac{\partial NM_L}{\partial L_p} * \Delta L_p\right)^2}$$

$$= \sqrt{\left(\frac{\frac{K_R(V_{DD} - |V_{t,p}| - V_{t,n})}{L_n}}{(1 + K_R)^2} * \Delta L_n\right)^2 + \left(\frac{\frac{K_R(V_{t,n} + |V_{t,p}| - V_{DD})}{L_p}}{(1 + K_R)^2} * \Delta L_p\right)^2}$$

(d) $$\frac{\partial NM_L}{\partial W} * \Delta W = \sqrt{\left(\frac{\partial NM_L}{\partial W_n} * \Delta W_n\right)^2 + \left(\frac{\partial NM_L}{\partial W_p} * \Delta W_p\right)^2}$$

$$= \sqrt{\left(\frac{\frac{K_R(V_{t,n} + |V_{t,p}| - V_{DD})}{W_n}}{(1 + K_R)^2} * \Delta W_n\right)^2 + \left(\frac{\frac{K_R(V_{DD} - |V_{t,p}| - V_{t,n})}{W_p}}{(1 + K_R)^2} * \Delta W_p\right)^2}$$

In Figure 4.15 noise margin (low state) variation components versus supply voltage is illustrated. Reducing supply voltage results in a less noise margin (low) variation. Total noise margin (low) variation increases from 3.54% to 3.6% as supply voltage reduces from

1V to 0.7V. V_t variation is the dominant source of noise margin (low) variation. For V_{DD} =0.7V, noise margin (low) variation due to V_t variation is 3.12% where total variation due all parameter variation is 3.6%. Noise margin (low) variation due to V_{DD} variation decreases with the reduction of supply voltage.

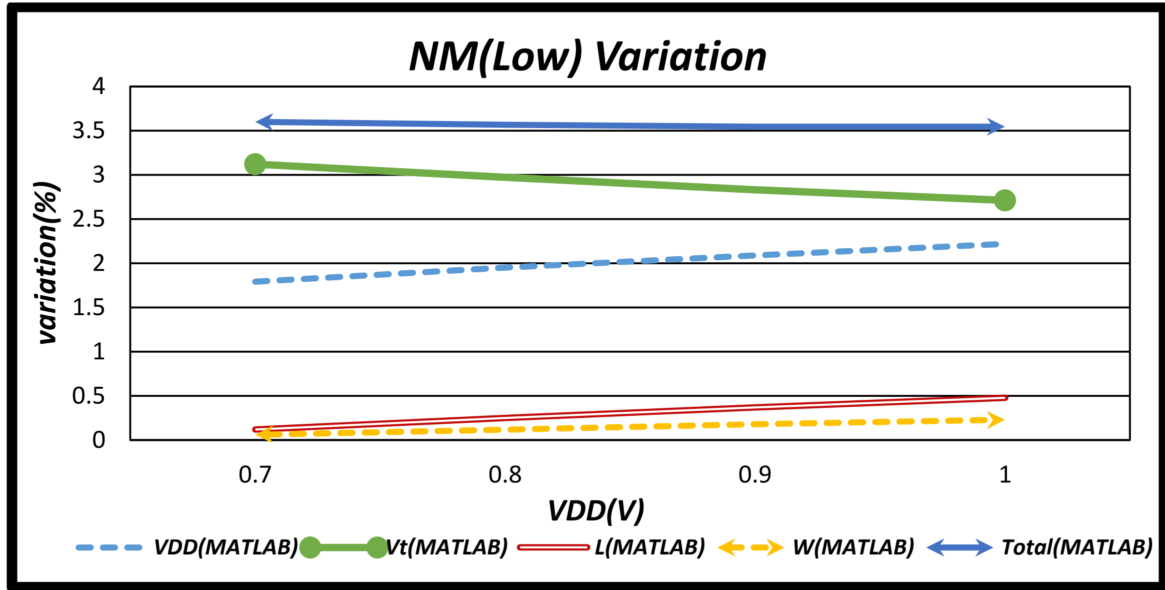

Figure 4.15. Noise Margin (Low State) variation versus supply voltage for an inverter in PTM's 22nm technology node. (Super-threshold region)

Table 4.7 shows simulation results of MATLAB and T-Spice for noise margin (Low state) variation. They both have the same trends. We have already seen form figure 4.14 that, reduced supply voltage has almost constant noise margin variation; T-Spice simulation also supports this result. Total variation in T-Spice simulation reduces from 3.59% to 2.96% as supply voltage reduces from 1V to 0.7V. This means that our analytical model will have a good estimation of noise margin (low) variation. Only differences between two simulation results are in the effect of channel length variation. It has slightly higher values in T-Spice simulation than the predicted ones. However, the difference is very small.

	Variation (%)									
Supply	**MATLAB**					**T-SPICE**				
V_{DD}(V)	**V_{DD}**	**V_t**	**L**	**W**	**Total**	**V_{DD}**	**V_t**	**L**	**W**	**Total**
0.7	1.79	3.12	0.12	0.06	3.6	2.34	1.11	1.43	0.06	2.959
0.8	1.95	2.97	0.25	0.12	3.56	1.8	1.32	1.78	0.08	2.856
0.9	2.09	2.83	0.37	0.18	3.54	1.5	1.52	2.15	0.13	3.033
1	2.22	2.71	0.48	0.23	3.54	1.5	1.78	2.73	0.18	3.592

Table 4.7 : Comparison of T-Spice and MATLAB simulation results for Noise Margin(low state) variation (Super-threshold)

Comparison of T-Spice and MATLAB simulations for total variation is showed in the following figure.

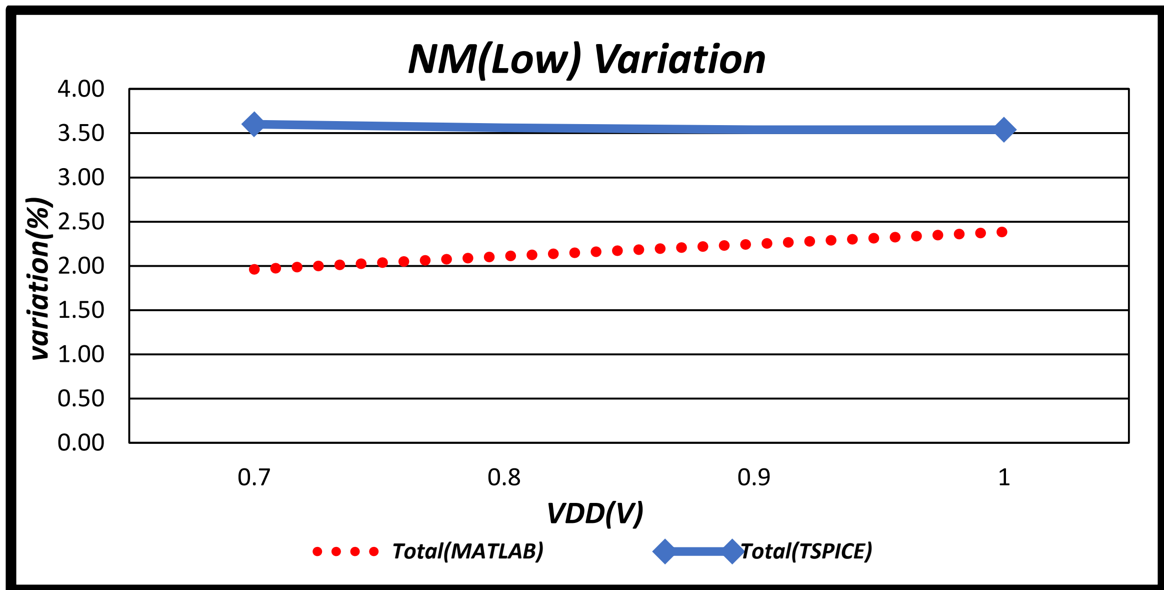

Figure 4.16. Noise margin (Low State) variation comparison for an inverter. (Super-threshold)

B. Sub-threshold

From the discussion of last section, we came to know that, for $V_{DD} \leq 0.6V$, inverter operates in the sub-threshold region. Because both NMOS and PMOS have V_{iL} less than 0.37V and as a result $V_{GS} \leq V_{t,n}, V_{t,p}$.Equating currents for NMOS and PMOS transistors operating in the sub-threshold region and not considering DIBL effect gives us the

following equation:

$$k_n'\left(\frac{W}{L}\right)_n(m-1)V_{TH}{}^2\exp\left(\frac{V_{in}-V_{t,n}}{mV_{TH}}\right)\{1\text{-}\exp\left(\frac{-V_{out}}{V_{TH}}\right)\}=k_p'\left(\frac{W}{L}\right)_p(m-1)V_{TH}{}^2\exp\left(\frac{V_{DD}-V_{in}-|V_{t,p}|}{mV_{TH}}\right)\{1\text{-}\exp\left(\frac{-V_{DD}+V_{out}}{V_{TH}}\right)\}$$

To find the lower logic threshold of input (V_{iL}), derivation condition $(dV_{out}/\,dV_{in}) = -1$ has to be evaluated for above equation; which leads us to:

$$\exp\left(\frac{V_{in}-V_{t,n}}{mV_{TH}}\right)\{\exp\left(\frac{-V_{out}}{V_{TH}}\right)\frac{1}{V_{TH}}\frac{\partial V_{out}}{\partial V_{in}}\}+\{1\text{-}\exp\left(\frac{-V_{out}}{V_{TH}}\right)\}\exp\left(\frac{V_{in}-V_{t,n}}{mV_{TH}}\right)\frac{1}{mV_{TH}} =$$
$$\frac{k_p'\left(\frac{W}{L}\right)_p}{k_n'\left(\frac{W}{L}\right)_n}[\exp\left(\frac{V_{DD}-V_{in}-|V_{t,p}|}{mV_{TH}}\right)\left(-\frac{1}{mV_{TH}}\right)\{1-\exp\left(\frac{-V_{DD}+V_{out}}{V_{TH}}\right)\}+\exp\left(\frac{V_{DD}-V_{in}-|V_{t,p}|}{mV_{TH}}\right)\{-\exp\left(\frac{-V_{DD}+V_{out}}{V_{TH}}\right)\frac{1}{V_{TH}}\frac{\partial V_{out}}{\partial V_{in}}\}]$$

Let, $V_{in} = V_{iL}$ and $V_{out} = V_{OH} = V_{DD}$, then

$$\frac{-1}{V_{TH}}\exp\left(\frac{V_{IL}-V_{t,n}-mV_{DD}}{mV_{TH}}\right)+\exp\left(\frac{V_{iL}-V_{t,n}}{mV_{TH}}\right)\frac{1}{mV_{TH}}-\frac{1}{mV_{TH}}\exp\left(\frac{V_{IL}-V_{t,n}-mV_{DD}}{mV_{TH}}\right) = \frac{k_p'\left(\frac{W}{L}\right)_p}{k_n'\left(\frac{W}{L}\right)_n}\exp\left(\frac{V_{DD}-V_{iL}-|V_{t,p}|}{mV_{TH}}\right)\frac{1}{V_{TH}} \quad (4.35)$$

Now, $\exp\left(\frac{V_{IL}-V_{t,n}-mV_{DD}}{mV_{TH}}\right) \approx 0$, therefore (4.35) can be written as:

$$exp\left(\frac{V_{iL}-V_{t,n}}{mV_{TH}}\right)\frac{1}{mV_{TH}} = \frac{k_p'\left(\frac{W}{L}\right)_p}{k_n'\left(\frac{W}{L}\right)_n}exp\left(\frac{V_{DD}-V_{iL}-|V_{t,p}|}{mV_{TH}}\right)\frac{1}{V_{TH}}$$

$$\Rightarrow V_{iL} = \frac{V_{DD}+V_{t,n}-|V_{t,p}|+mV_{TH}\ln\{\frac{mk_p'\left(\frac{W}{L}\right)_p}{k_n'\left(\frac{W}{L}\right)_n}\}}{2}$$

$$\approx \frac{V_{DD}+V_{t,n}-|V_{t,p}|}{2} \quad (4.36)$$

Assuming $V_{OL} = 0,$ Noise margin (Low State), NM_L can be written as follows:

$$NM_L=V_{iL}\text{-}V_{OL}=V_{iL}$$

$$NM_L = \frac{V_{DD}+V_{t,n}-|V_{t,p}|}{2} \quad (4.37)$$

Here,

$$K_R = \frac{K_p'}{K_n'} * \frac{(\frac{W}{L})_p}{(\frac{W}{L})_n}$$

Assuming that the variation of the device parameters are small compare to their nominal values and they can be approximated by Gaussian distribution, device NM_L variation can be derived by taking the partial derivative and the equation is as following:

$$\frac{\Delta NM_L}{NM_L} = \sqrt{\frac{(\frac{\partial NM_L}{\partial V_{DD}})^2 * \Delta V_{DD}^2 + \left(\frac{\partial NM_L}{\partial V_t}\right)^2 * \Delta V_t^2 + \left(\frac{\partial NM_L}{\partial L}\right)^2 * \Delta L^2 + \left(\frac{\partial NM_L}{\partial W}\right)^2 * \Delta W^2}{(\frac{V_{DD}+V_{t,n}-|V_{t,p}|}{2})^2}} \quad (4.38)$$

Where,

(a) $\frac{\partial NM_L}{\partial V_{DD}} * \Delta V_{DD} = \frac{1}{2} * \Delta V_{DD}$

(b) $$\frac{\partial NM_L}{\partial V_t} * \Delta V_t = \sqrt{\left(\frac{\partial NM_L}{\partial V_{t,p}} * \Delta V_{t,p}\right)^2 + \left(\frac{\partial NM_L}{\partial V_{t,n}} * \Delta V_{t,n}\right)^2}$$
$$= \sqrt{\left(\frac{-1}{2} * \Delta V_{t,p}\right)^2 + \left(\frac{1}{2} * \Delta V_{t,n}\right)^2}$$

Figure 4.17 illustrates noise margin (low state) variation components versus supply voltage based on the analytical model of (4.38). Reducing supply voltage results in a higher noise margin (low) variation. Total noise margin (low) variation increases from 5.1% to 7.16% as supply voltage reduces from 0.6V to 0.2V. Effect of V_t variation on noise margin becomes severe when supply voltages reduces below 0.3V. For V_{DD} =0.6V, noise margin (low) variation due to V_{DD} variation is 4.37% and due to V_t variation is 2.6%. But For V_{DD} =0.2V, noise margin (low) variation due to V_{DD} and V_t variations are 3.5%.and 6.25%, respectively. Noise margin (low) variation due to V_{DD} variation decreases with the reduction of supply voltage.

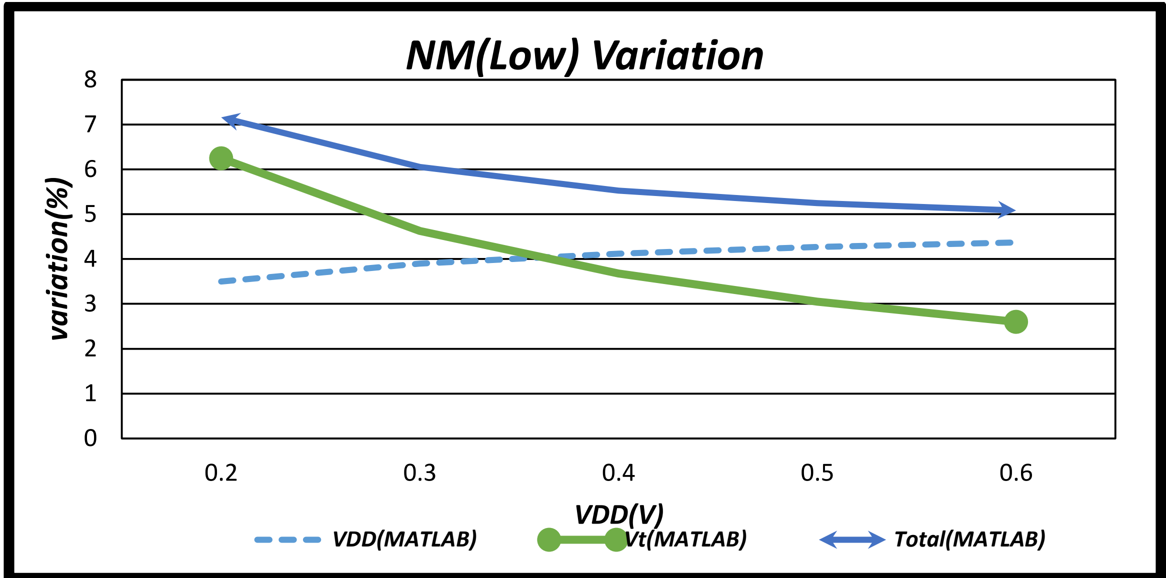

Figure 4.17. Noise Margin (Low State) variation versus supply voltage for an inverter in PTM's 22nm technology node. (Sub-threshold region)

Table 4.9 shows simulation results of MATLAB and T-Spice for noise margin (Low state) variation. They both have the same trends of increment as supply voltage goes lower. Both of the simulation results agree that V_t and V_{DD} variations are the primary sources of noise margin (low) variation of an inverter that is operating in the sub-threshold region. However, T-Spice simulation increases from 2. 7% to 3.35% only as supply voltage reduces from 0.6V to 0.2V. But MATLAB results on the other hand has a sharper incremental pattern (from 5.1% to 7.16%) as the supply voltage reduces from 0.6V to 0.2V.

Supply VDD	Variation (%)					
	MATLAB			TSPICE		
	VDD	V_t	Total	VDD	V_t	Total
0.2	3.5	6.25	7.1633	3.27	0.73	3.3505
0.3	3.9	4.63	6.0537	4.23	0.53	4.2631
0.4	4.12	3.68	5.5242	4.14	0.48	4.1677
0.5	4.27	3.05	5.2474	3.94	0.6	3.9854
0.6	4.37	2.6	5.085	2.6	0.84	2.7323

Table 4.8 : Comparison of T-Spice and MATLAB simulation results for Noise Margin (Low State)

Since overall variation result for MATLAB simulation is no more than 2x of the T-Spice simulation result, so we can state that, our analytical model for estimating noise margin (low state) variation is correct. Comparison of T-Spice and MATLAB simulations for total variation is showed in the following figure.

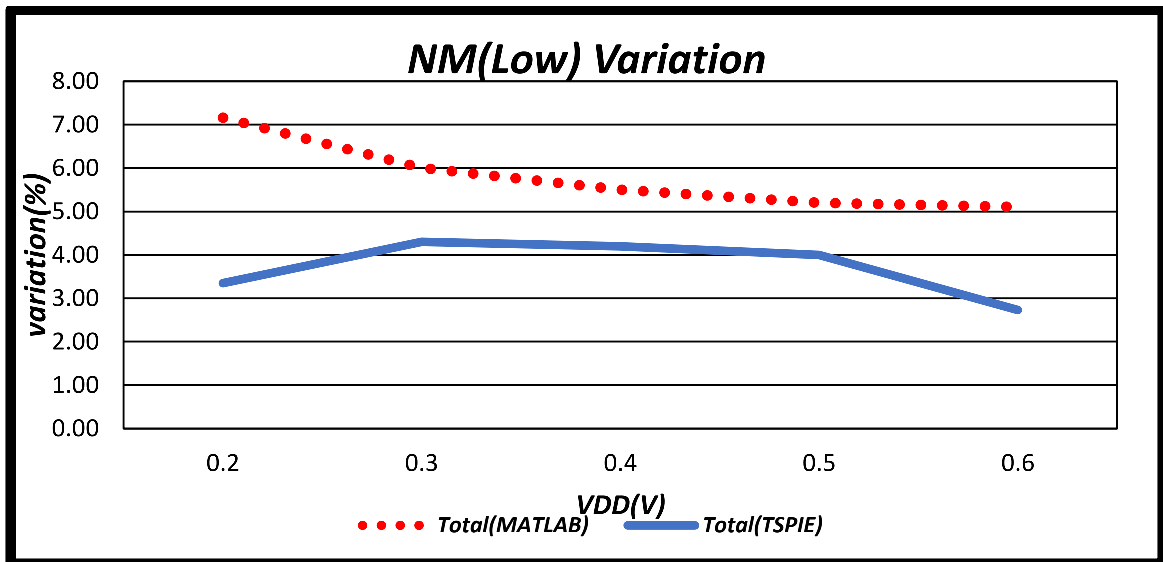

Figure 4.18. Noise Margin (Low State) variation comparison for an inverter. (Sub-threshold)

4.3.2.2. Noise Margin (High State) variation

A. Super-threshold:

Equating currents for saturated PMOS transistor and linear NMOS transistor of Region 3 of table 4.5 gives us the following equation:

$$\frac{k_n'}{2}\left(\frac{W}{L}\right)_n \left[2\left(V_{IH}\text{-}V_{t,n}\right)V_{out}\text{-}V_{out}^{2}\right]=\frac{k_p'}{2}\left(\frac{W}{L}\right)_p \left(V_{DD}\text{-}V_{IH}\text{-}|V_{t,p}|\right)^{2} \tag{4.39}$$

To find the lower logic threshold of input (V_{iL}), derivation condition $(\frac{\partial V_{out}}{\partial V_{in}}) = -1$ has to be evaluated for equation (4.39);which leads us to the following equation:

$$k_n'\left(\frac{W}{L}\right)_n \{V_{out}+\left(V_{in}\text{-}V_{t,n}\right)\frac{\partial V_{out}}{\partial V_{in}} - V_{out}\frac{\partial V_{out}}{\partial V_{in}}\} = k_p'\left(\frac{W}{L}\right)_p \{\left(V_{DD}\text{-}V_{in}\text{-}\left|V_{t,p}\right|\right)(\text{-}1)\}$$

$$\Longrightarrow 2V_{out}\text{-}V_{in}+V_{t,n} = \frac{k_p'\left(\frac{W}{L}\right)_p}{k_n'\left(\frac{W}{L}\right)_n}(V_{in}+\left|V_{t,p}\right|\text{-}V_{DD})$$

Let, $V_{in} = V_{iH}$ and $V_{out} = V_{OL} = GND\ (0)$, then

$$V_{iH}\text{-}V_{t,n} = \frac{k_p'\left(\frac{W}{L}\right)_p}{k_n'\left(\frac{W}{L}\right)_n}(V_{DD}\text{-}V_{iH}\text{-}\left|V_{t,p}\right|)$$

$$\Longrightarrow V_{iH} = \frac{V_{t,n}\frac{k_n'\left(\frac{W}{L}\right)_n}{k_p'\left(\frac{W}{L}\right)_p}+V_{DD}-|V_{t,p}|}{1+\frac{k_n'\left(\frac{W}{L}\right)_n}{k_p'\left(\frac{W}{L}\right)_p}} \tag{4.40}$$

It is important to note that equation (4.32) and equation (4.0) are identical. That means V_{iH} and V_{iL} are same point in the voltage transfer characteristics curve of an inverter. Using equation (4.40) and parameter values of table 4.1 we can find the V_{iH} values of table 4.10.And again, when $V_{DD} \leq 0.6V$, then $V_{GS} < V_t$ .So equation (4.40) does not hold anymore. Both NMOS and PMOS are turned off. Therefore, inverter operates in sub-threshold region instead of super-threshold region.

V_{DD}(V)	V_{iH} (V)
0.4	0.326
0.5	0.346
0.6	0.366
0.7	0.386
0.8	0.406
0.9	0.425
1	0.445

Table 4.9 : V_{iH} values of an inverter(Super-threshold region)

Let, $V_{OH} = V_{DD}$. Hence, Noise margin (High State), NM_H can be written as follows:

$$NM_H = V_{OH} - V_{iH}$$

$$NM_H = \frac{V_{DD}K_R - V_{t,n}K_R + |V_{t,p}|}{1+K_R} \quad (4.41)$$

Here,

$$K_R = \frac{K_n'}{K_p'} * \frac{(\frac{W}{L})_n}{(\frac{W}{L})_p}$$

Assuming that the variation of the device parameters are small compare to their nominal values and they can be approximated by Gaussian distribution, device NM_H variation can be derived by taking the partial derivative and the equation is as following:

$$\frac{\Delta NM_H}{NM_H} = \sqrt{\frac{(\frac{\partial NM_H}{\partial V_{DD}})^2 * \Delta V_{DD}{}^2 + \left(\frac{\partial NM_H}{\partial V_t}\right)^2 * \Delta V_t{}^2 + \left(\frac{\partial NM_H}{\partial L}\right)^2 * \Delta L^2 + \left(\frac{\partial NM_H}{\partial W}\right)^2 * \Delta W^2}{(\frac{V_{DD}K_R + |V_{t,p}| - V_{t,n}K_R}{1+K_R})^2}} \quad (4.42)$$

Where,

(a) $\frac{\partial NM_H}{\partial V_{DD}} * \Delta V_{DD} = \frac{K_R}{1+K_R} * \Delta V_{DD}$

(b) $\frac{\partial NM_H}{\partial V_t} * \Delta V_t = \sqrt{\left(\frac{\partial NM_H}{\partial V_{t,p}} * \Delta V_{t,p}\right)^2 + \left(\frac{\partial NM_H}{\partial V_{t,n}} * \Delta V_{t,n}\right)^2}$

$= \sqrt{\left(\frac{1}{1+K_R} * \Delta V_{t,p}\right)^2 + \left(\frac{-K_R}{1+K_R} * \Delta V_{t,n}\right)^2}$

(c) $\frac{\partial NM_H}{\partial L} * \Delta L = \sqrt{\left(\frac{\partial NM_H}{\partial L_n} * \Delta L_n\right)^2 + \left(\frac{\partial NM_H}{\partial L_p} * \Delta L_p\right)^2}$

$$= \sqrt{\left(\frac{\frac{K_R(V_{t,n} + |V_{t,p}| - V_{DD})}{L_n}}{(1 + K_R)^2} * \Delta L_n\right)^2 + \left(\frac{\frac{K_R(V_{DD} - |V_{t,p}| - V_{t,n})}{L_p}}{(1 + K_R)^2} * \Delta L_p\right)^2}$$

(d) $$\frac{\partial NM_H}{\partial W} * \Delta W = \sqrt{\left(\frac{\partial NM_H}{\partial W_n} * \Delta W_n\right)^2 + \left(\frac{\partial NM_H}{\partial W_p} * \Delta W_p\right)^2}$$

$$= \sqrt{\left(\frac{\frac{K_R(V_{DD} - |V_{t,p}| - V_{t,n})}{W_n}}{(1 + K_R)^2} * \Delta W_n\right)^2 + \left(\frac{\frac{K_R(V_{t,n} + |V_{t,p}| - V_{DD})}{W_p}}{(1 + K_R)^2} * \Delta W_p\right)^2}$$

In Figure 4.19 noise margin (high state) variation components versus supply voltage is illustrated. Total NM_H variation due to process related issues, increases as the supply voltage reduces. NM_H variation increases from 7.56% to 9.72% when V_{DD} reduces from 1V to 0.7V.Following table illustrates the individual contribution of each parameter variation on overall NM_H variation. It is clear from the table that, V_{DD} variation and V_t variations play key roles in overall NM_H variation. NM_H variation due to both of them increases as V_{DD} increases. For V_{DD} =0.8V, V_{DD} variation contribution is roughly 3x more than the contribution of V_t variation. Like delay variation, contribution of L and W variations are not so important and they are less than 1% when V_{DD} varies in between 0.7V and 1V range. For V_{DD}= 1V, NM_H variations due to V_t variation is 2.17% and for V_{DD} =0.7V, it is 3.83%. For same voltages NM_H variation due to V_{DD} variations are 7.23% and 8.94%, respectively.

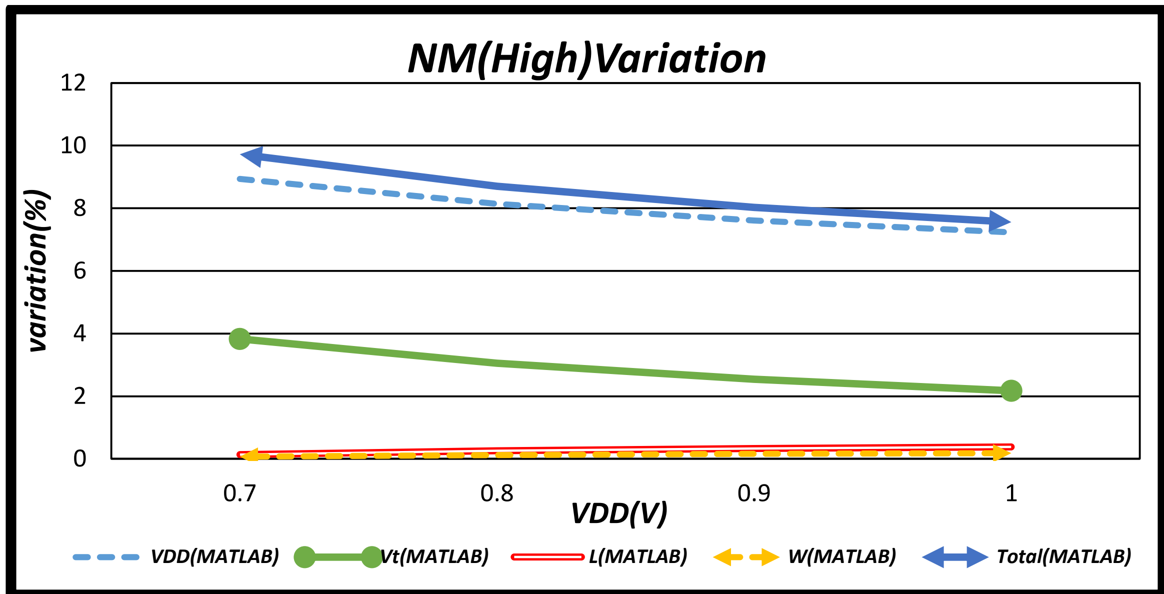

Figure 4.19. Noise margin (High State) variation comparison for an inverter. (Super-threshold region)

Table 4.11 below shows simulation results of MATLAB and T-Spice for noise margin (High state) variation. They both have very close results. We have already seen form figure 4.14 that, reduced supply voltage has higher impact on noise margin variation; T-Spice simulation also supports this result. Total variation in T-Spice simulation increases from 6.94% to 10.22% as supply voltage reduces from 0.9V to 0.7V. However, for 1V supply voltage, total variation is 10.4% in T-Spice simulation. Both simulations confirm that maximum noise margin (high state) variation will be around 10%.This means that our analytical model is close enough to estimate noise margin (high) variation correctly. Only differences between two simulation results are in the effects of channel length and width variations. They both have higher values in T-Spice simulation than the predicted ones.

	Variation (%)									
Supply	MATLAB					T-SPICE				
V_{DD}(V)	V_{DD}	V_t	L	W	Total	V_{DD}	V_t	L	W	Total
0.7	8.94	3.83	0.14	0.07	9.727	5.42	2.4	7.44	3.74	10.221
0.8	8.14	3.05	0.26	0.12	8.697	8.78	2.13	3.13	1.57	9.6895
0.9	7.61	2.54	0.33	0.16	8.031	5.1	3.26	3	1.63	6.94
1	7.24	2.17	0.38	0.18	7.56	4.44	2.27	6.48	6.36	10.4

Table 4.10 : Comparison of T-Spice and MATLAB simulation results for Noise Margin (high state) variation (Super-threshold region)

Comparison of T-Spice and MATLAB simulations for total variation is showed in the following figure.

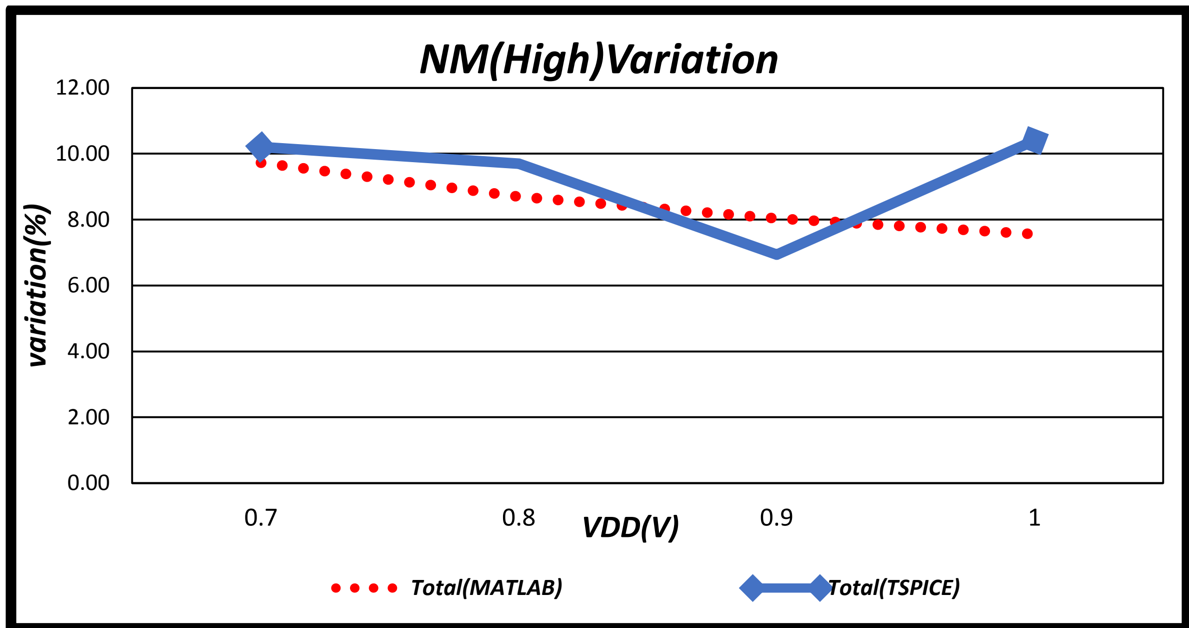

Figure 4.20. Noise margin (High State) variation comparison for an inverter. (Super-threshold region)

B. Sub-threshold

Equating currents for NMOS and PMOS transistors operating in the sub-threshold region and not considering DIBL effect gives us the following equation:

$$k_n'\left(\frac{W}{L}\right)_n (m-1)V_{TH}{}^2\exp\left(\frac{V_{in}-V_{t,n}}{mV_{TH}}\right)\{1\text{-}\exp\left(\frac{-V_{out}}{V_{TH}}\right)\}=k_p'\left(\frac{W}{L}\right)_p (m-1)V_{TH}{}^2\exp\left(\frac{V_{DD}-V_{in}-|V_{t,p}|}{mV_{TH}}\right)\{1\text{-}\exp\left(\frac{-V_{DD}+V_{out}}{V_{TH}}\right)\}$$

To find the lower logic threshold of input (V_{iL}), derivation condition $(\frac{\partial V_{out}}{\partial V_{in}}) = -1$ has to be evaluated for above equation; which gives us the following equation:

$$\exp(\frac{V_{in} - V_{t,n}}{mV_{TH}}) \{\exp(\frac{-V_{out}}{V_{TH}})\frac{1}{V_{TH}}\frac{\partial V_{out}}{\partial V_{in}}\} + \{1\text{-}\exp(\frac{-V_{out}}{V_{TH}})\}\exp(\frac{V_{in} - V_{t,n}}{mV_{TH}})\frac{1}{mV_{TH}} =$$

$$\frac{k_p'(\frac{W}{L})_p}{k_n'(\frac{W}{L})_n}[\exp(\frac{V_{DD}-V_{in}-|V_{t,p}|}{mV_{TH}})(-\frac{1}{mV_{TH}})\{1-\exp(\frac{-V_{DD}+V_{out}}{V_{TH}})\}+\exp(\frac{V_{DD}-V_{in}-|V_{t,p}|}{mV_{TH}})\{-\exp(\frac{-V_{DD}+V_{out}}{V_{TH}})\frac{1}{V_{TH}}\frac{\partial V_{out}}{\partial V_{in}}\}]$$

Let, $V_{in} = V_{iH}$ and $V_{out} = V_{OL} = GND(0)$, then

$$\frac{-1}{V_{TH}}\exp\left(\frac{V_{iH}-V_{t,n}}{mV_{TH}}\right) = \frac{k_p'(\frac{W}{L})_p}{k_n'(\frac{W}{L})_n}[-\exp\left(\frac{V_{DD}-V_{iH}-|V_{t,p}|}{mV_{TH}}\right)\frac{1}{mV_{TH}} + \exp\left(\frac{V_{DD}-V_{iH}-|V_{t,p}|-mV_{DD}}{mV_{TH}}\right)\frac{1}{mV_{TH}} + \exp\left(\frac{V_{DD}-V_{iH}-|V_{t,p}|-mV_{DD}}{mV_{TH}}\right)\frac{1}{V_{TH}}]$$

Now, $\exp\left(\frac{V_{DD}-V_{iH}-|V_{t,p}|-mV_{DD}}{mV_{TH}}\right) \approx 0$,then :

$$\exp\left(\frac{V_{iH} - V_{t,n}}{mV_{TH}}\right)\frac{1}{V_{TH}} = \frac{k_p'\left(\frac{W}{L}\right)_p}{k_n'\left(\frac{W}{L}\right)_n}\exp\left(\frac{V_{DD} - V_{iH} - |V_{t,p}|}{mV_{TH}}\right)\frac{1}{mV_{TH}}$$

$$\Rightarrow V_{iH} = \frac{V_{DD}+V_{t,n}-|V_{t,p}|+mV_{TH}\ln\{\frac{k_p'\left(\frac{W}{L}\right)_p}{mk_n'\left(\frac{W}{L}\right)_n}\}}{2}$$

$$\approx \frac{V_{DD}+V_{t,n}-|V_{t,p}|}{2} \quad (4.43)$$

Assuming, $V_{OH} = V_{DD}$, Noise margin (Low State), NM_H can be written as follows:

$$NM_H = V_{OH} - V_{iH}$$

$$NM_H = \frac{V_{DD}-V_{t,n}+|V_{t,p}|}{2} \quad (4.44)$$

where,

$$K_R = \frac{K_p'}{K_n'} * \frac{(\frac{W}{L})_p}{(\frac{W}{L})_n}$$

Assuming that the variation of the device parameters are small compare to their nominal values and they can be approximated by Gaussian distribution, device NM_H variation can be derived by taking the partial derivative and the simplified equation is:

$$\frac{\Delta NM_H}{NM_H} = \sqrt{\frac{(\frac{\partial NM_L}{\partial V_{DD}})^2 * \Delta V_{DD}{}^2 + \left(\frac{\partial NM_L}{\partial V_T}\right)^2 * \Delta V_T{}^2 + \left(\frac{\partial NM_L}{\partial L}\right)^2 * \Delta L^2 + \left(\frac{\partial NM_L}{\partial W}\right)^2 * \Delta W^2}{(\frac{V_{DD} - V_{t,n} + |V_{t,p}|}{2})^2}} \quad (4.45)$$

Where,

(a) $\frac{\partial NM_H}{\partial V_{DD}} * \Delta V_{DD} \quad = \quad \frac{1}{2} * \Delta V_{DD}$

(b) $\frac{\partial NM_H}{\partial V_t} * \Delta V_t \quad = \sqrt{\left(\frac{\partial NM_L}{\partial V_{t,p}} * \Delta V_{t,p}\right)^2 + \left(\frac{\partial NM_L}{\partial V_{t,n}} * \Delta V_{t,n}\right)^2}$

$$= \sqrt{\left(\frac{1}{2} * \Delta V_{t,p}\right)^2 + \left(\frac{-1}{2} * \Delta V_{t,n}\right)^2}$$

Figure 4.21 shows the noise margin (high state) variation components versus supply voltage based on the analytical model of (4.45). Reducing supply voltage results in a higher noise margin (low) variation. Total noise margin (high) variation increases from 5.7% to 9.6% as supply voltage reduces from 0.6V to 0.09V. Effect of V_t variation on noise margin becomes severe when supply voltages reduces below 0.6V. Effect of V_{DD} variation on noise margin is almost constant at 4.7%. For V_{DD} =0.6V, noise margin(high) variation due to V_{DD} variation is 4.89% and due to V_t variation is 2.31%. But For V_{DD} =0.09V, noise margin (high) variation due to V_{DD} and V_t variations are 4.68%.and 8.36% respectively. Other parameters effects are very nominal and cannot change the overall variation significantly.

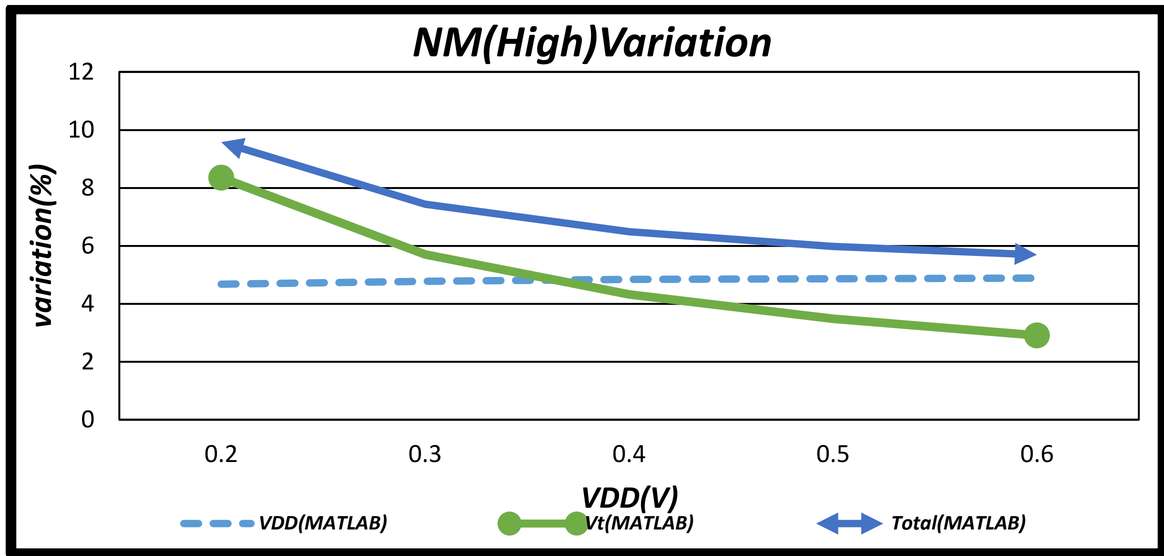

Figure 4.21. Noise Margin (High State) variation versus supply voltage for an inverter in PTM's 22nm technology node. (Sub-threshold region)

Simulation results of MATLAB and T-Spice for noise margin (High state) variation are presented on table 4.13 below. Although overall variation increases with the reduced supply voltage for both cases but their magnitudes are not equal. We can see that, V_t and V_{DD} variations are the major sources of concern for noise margin (high) in both simulations. Impact of process parameters variation effect in T-Spice simulation is approximately 2x than the analytical model. For V_{DD} =0.2V, analytical model's estimation for total variation is 9.58%, where T-Spice simulation tells us that actual variation due to the deviation in the process parameters will be 26.17%. This is because our analytical model is a simplified version and has ignored some short channel effects (DIBL, gate tunneling etc.)

	Variation(%)					
Supply	**MATLAB**			**TSPICE**		
VDD	**VDD**	**V_t**	**Total**	**VDD**	**V_t**	**Total**
0.2	4.68	8.36	9.581	22	14.2	26.174
0.3	4.78	5.7	7.439	12.4	8.7	15.148
0.4	4.84	4.32	6.488	11.5	4.01	12.179
0.5	4.87	3.48	5.986	6.87	6.01	9.1278
0.6	4.89	2.91	5.69	8.67	6	10.544

Table 4.11 : Comparison of T-Spice and MATLAB simulation results for Noise Margin (High state) variation (Sub-threshold)

Comparison of T-Spice and MATLAB simulations for total variation is illustrated in the following figure.

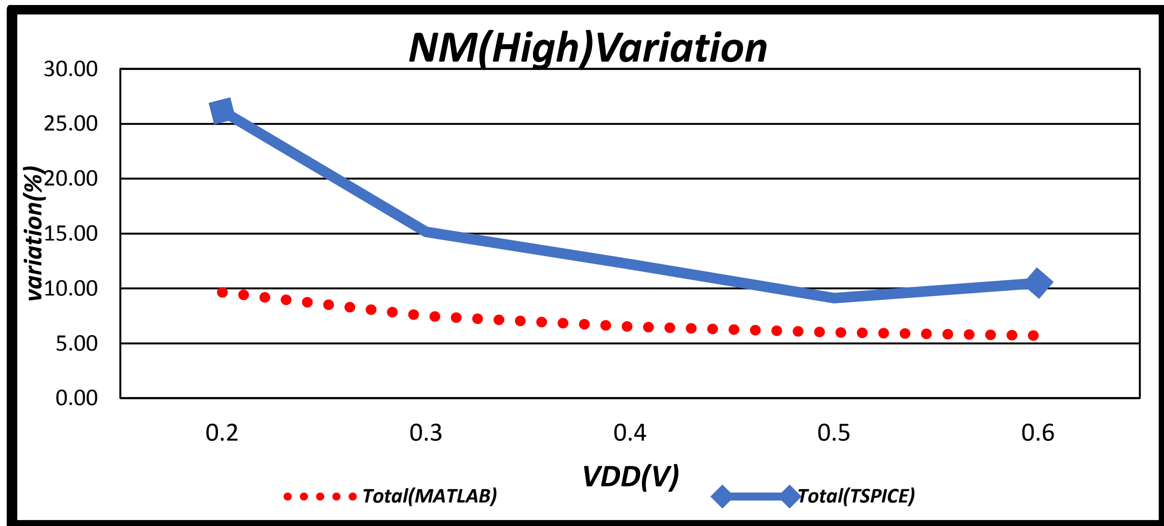

Figure 4.22. Noise Margin (High State) variation comparison (Sub-threshold Region)

It is very important to note that, for digital circuit we have not extended our analysis beyond V_{DD}=0.09V for delay variation. It is because, below 0.09V supply voltage, delay variation becomes more than 100% in T-Spice simulation and our analytical model is not able to predict that value. Therefore our analytical model for delay variation is valid when

supply voltage is 0.9V or higher. For noise margin (high and low state) variation, scenario is even worse. For T-Spice simulation, voltage transfer characteristic curve (VTC) is not accurate and it is not possible to find V_{iH} (High input logic threshold) value from the T-Spice simulation when supply voltage is reduced below 0.2V. So in this thesis paper, noise margin (high and low state) analytical models are valid when supply voltage is 0.2V and above. Noise margin (high and low) values are showed in chapter 5.

By analyzing the results that are presented in this chapter, we can say that, our analytical models are correct and they can estimate the impacts of parameter variations on digital circuits correctly. The analytical models results are not exactly same of the T-Spice simulation results but the difference is within a tolerable range. And this difference is because of ignoring some complex effects during modeling. These simple analytical models will not only estimate the overall variation in a circuit but will also provide the contribution of each variability component separately.

Effect of parameter variation is becoming more and more severe in digital circuit as technology progresses. Main reason for this problem is the leakage current, which is increasing radically for digital circuits. So in chapter 5 will mainly focus on digital circuits. We will discuss about some existing leakage power reduction techniques first, and then we will propose a new technique to solve this vexing problem.

Chapter 5

Ultra Low Voltage Circuit Design Technique

5.1 Introduction

From chapter 4, we can see that, variation in digital circuits is becoming severe for ultra-low voltage operation. This variation is occurring due to substantial increase in leakage current in the circuit. Supply voltage is scaled when downsizing the technology feature size in order to maintain constant field scaling. As a result performance of a digital circuit decreases. To maintain the performance, threshold voltage is also scaled accordingly. Since leakage current is exponentially dependent on threshold voltage; this reduction increases leakage current dramatically. A very small change in the threshold voltage or supply voltage or critical dimensions of the device during processing can change leakage current by a huge amount. As a result, delay or other static behavior parameters of a circuit can vary significantly.

Several circuit level techniques have been developed so far to reduce the leakage current and its variation effect for ultra-low voltage circuit. In this chapter, we will first describe two popular and simple techniques (Dynamic Threshold CMOS and Transistor Stacking) to reduce leakage current in an inverter circuit. Then we will propose our new technique to reduce leakage current in ultra-low voltage circuit. Since these circuits reduce the leakage current, they will also reduce leakage power too. These circuits can be

considered as energy efficient circuit as well. We will then compare our new design technique with these two existing techniques in terms of delay and noise margin (high and low sates) variations.

5.2 Dynamic Threshold CMOS (DTCMOS)

In a dynamic threshold CMOS logic circuit threshold voltage is varied dynamically. Body of the transistor is tied up with the gate. This scheme uses body biasing technique to adaptively change the threshold voltage. In this approach, we will explain the mechanism by considering NMOS transistor's threshold voltage conditions only. Similar analysis can be done for PMOS too.

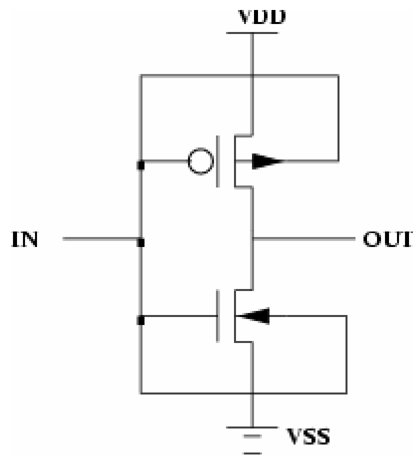

Figure 5.1: Schematic of DTCMOS inverter [7]

This concept of changing threshold voltage dynamically relies on the connection between substrate and gate. During the ON state of the transistor threshold voltage ($V_{t,n}$) is low; and maintain a high threshold voltage ($V_{t,n}$) during OFF state. Threshold voltage of NMOS can be explained by the following equation:

$$V_{t,n} = V_{t,n0} + \gamma(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}) \quad (5.1)$$

where $V_{t,n0}$ is the threshold voltage for $V_{SB} = 0$, ϕ_F is the substrate Fermi potential, and γ is the body-effect coefficient. When gate has an input of V_{DD} (ON state of active mode), then source-body biasing voltage V_{SB} becomes negative. Therefore, threshold voltage $V_{t,n}$ reduces which increases the drive current for NMOS during the ON state and reduces the delay. This process is also known as forward body biasing technique. On the other hand, when gate input voltage is $0V$ (OFF state of active mode or standby mode of a transistor) then source-body biasing is voltage V_{SB} becomes $0V$. As a result, threshold voltage during off state remains higher than ON state.

DTMOS can be developed in bulk technologies by using triple wells. To reduce parasitic components some sort of ‘doping engineering’ is needed .More benefits can be found for DTMOS when partially depleted Silicon-on-Insulator (SOI) devices are used. Excellent DC inverter characteristics down to 0.2V and good ring oscillator performance down to 0.3V are achieved using this method. The supply voltage of DTMOS is limited by the diode built in potential in bulk silicon technology. The *pn* diode between source and body should be reverse biased. Hence, this technique is only suitable for ultra-low voltage (0.6V and below) circuits in bulk CMOS [7].

5.3 Transistor Stacking:

Sub-threshold leakage current flowing through a stack of series connected transistors reduces when more than one transistor in the stack is turned off. This effect is known as the “stacking effect” [7]. In a transistor stacking technique, two transistors are

used to replace one. Therefore, for an inverter circuit there will be two NMOS and two PMOS. An inverter with stack of transistors is shown in Figure 5.2.

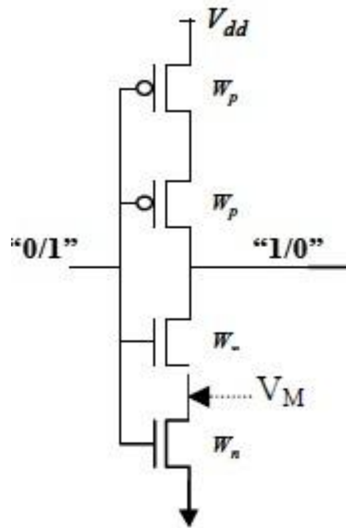

Figure 5.2: Schematic of an inverter with transistor stack [2]

Let say input to the inverter gate is *0V* (OFF state of active mode or standby mode of transistor) both NMOS transistors are in cut-off region. Voltage at the intermediate node (V_M) is positive due to small drain current. This has several advantages, First of all, gate source voltage of top NMOS transistor (V_{GS1}) is negative and hence sub-threshold current reduces substantially. Secondly, source to body potential (V_{SB1}) becomes positive. This process is known as reverse body biasing technique. As a result, threshold voltage increases and thus reduces sub-threshold leakage current drastically. The leakage of a two transistor stack is an order of magnitude less than leakage in a single transistor [7].

Both of these leakage reduction mechanisms discussed above have some limitations. DTCMOS is good when transistor is ON. At that case, threshold voltage is reduced and hence delay is improved further. But it cannot give much improvement in terms of static power, because threshold voltage is not increased for OFF state. On the other

hand, transistor stack technique gives better reduction of sub-threshold leakage power during OFF state. But during ON state, the threshold voltage increases because of forward body biasing of the top NMOS transistor. Because of all these reasons, delay in an inverter increases by a large amount. PMOS transistors also follows the similar mechanism in stack transistors inverter. To overcome these issues, we have proposed a new circuit level technique in the following section.

5.4 Transistor Stacking with DTCMOS (New Design)

In our proposed design, we have combined basic principles of both transistor stack and dynamic threshold CMOS. Instead of stacking with basic NMOS and PMOS, we have replaced them with dynamic threshold NMOS and PMOS in the stack transistor circuit. Schematic of our new design is give below:

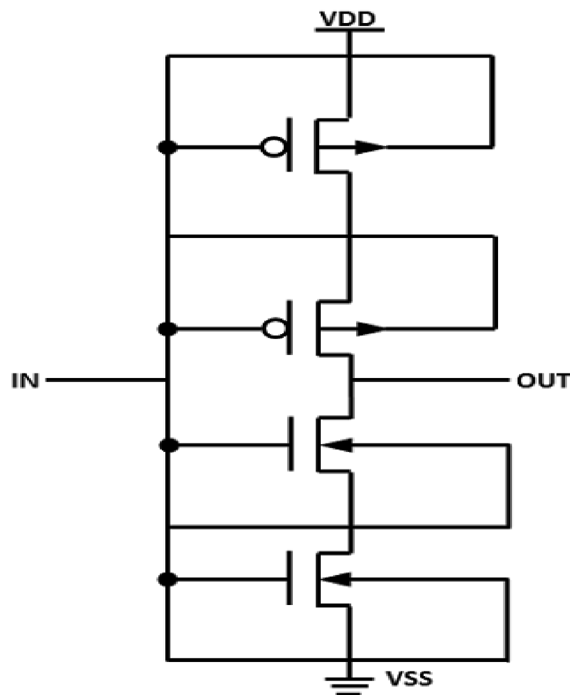

Figure 5.3: Schematic of an inverter with DTCMOS transistor stack

For our analysis let us start with the NMOS network. When input voltage is *0V* at the gate, both NMOS transistors are turned off. Like normal transistor stack, intermediate node of two NMOS transistors will have a positive voltage. And as a result of reduced gate to source voltage and increased source to body potential, leakage current will be reduced by a large amount in our new design. However, as input becomes (V_{DD}) during the ON state, this design follows the DTCMOS circuit technique. Source to body potential (V_{SB}) becomes negative. Thus threshold voltage will be reduced and we will have less delay in our circuit. Same analysis is true for PMOS too. Therefore it is expected that our proposed new design will have better leakage management than original DTCMOS inverter and will be much faster than the original stack transistor inverter circuit. Simulations results will be presented in the following section. The *pn* diode between source and body should be reverse biased. Hence, this technique is only suitable for ultra-low voltage (0.6V and below) circuits in bulk CMOS.

5.5 Simulation Results

In order to verify our new design's effectiveness, we have compared it with the existing leakage reduction techniques that are discussed in section 5.1 and 5.2.Along with them we have also considered a standard inverter model (existing technique) that we have used earlier in chapter4 for analytical versus T-Spice model comparison. We have compared them in terms of delay (t_{pHL}) and leakage power. In addition to find out a variation tolerant energy efficient design, we have considered the delay and noise margin (high and low state both) variation too. All the results in this section are based on T-Spice simulation. Parameter values are chosen based on PTM's 22nm technology that are given in Table 4.1.

5.5.1 Delay Comparison (t_{pHL})

Plot of delay versus supply voltage is presented in the following figure and table 5.1. From figure 5.4 we can see that, as supply voltage decreases, delay increases. Delay are in nano-second range. Above 0.2 V supply voltage all three techniques, stack transistor, DTCMOS and new design have almost same delay. Below 0.2V supply voltage DTCMOS have the least delay where delay for basic stack transistor has the highest. For 0.1V supply voltage delay for stack transistor (10.73nS) is approximately 3x than the DTCMOS (3.6nS).As expected delay for our new technique settles in between them with 8.64nS.

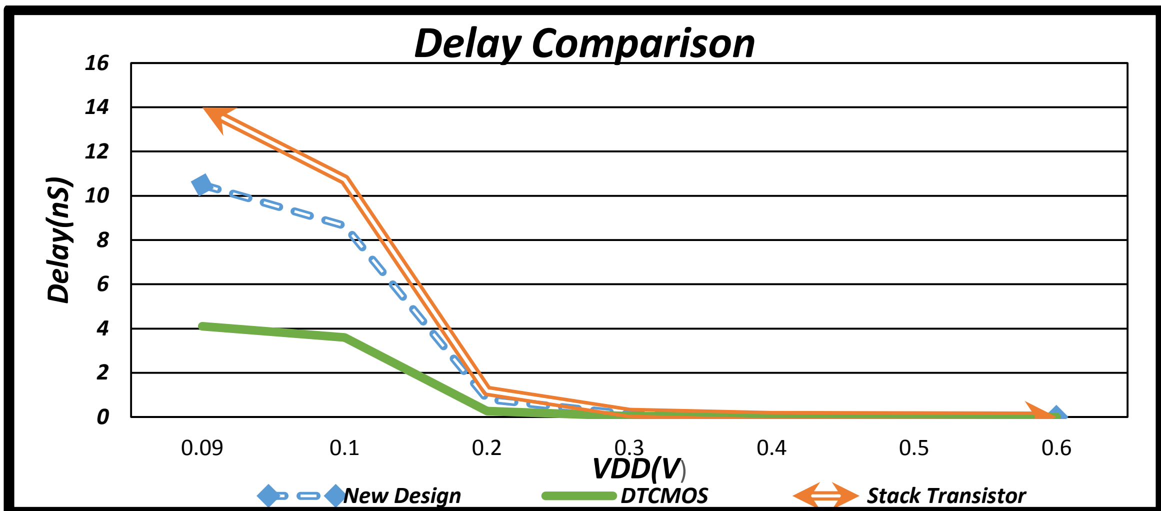

Figure 5.4: Delay (t_{pHL}) comparison for different leakage reduction techniques

From Table 5.1, low-to-high propagation delay values that we have estimated by our analytical model are close to the T-Spice simulation results. For 0.1Vsupply voltage MATLAB simulation results shows delay will 1.4nS. For T-Spice simulation this result is just 3.7ns higher. Also it is important to note that, delay increases for new design and stack transistor technique than the existing design.

Delay (nS)					
V_{DD}(V)	**MATLAB**	**Existing Design**	**New Design**	**DTCMOS**	**Stack Transistor**
0.09	1.93	6	10.5	4.1	14
0.1	1.4	5.1	8.64	3.6	10.73
0.2	0.12	0.437	0.81	0.274	1.18
0.3	0.02	0.06	0.12	0.037	0.177
0.4	0.012	0.015	0.035	0.011	0.046
0.5	0.008	0.007	0.018	0.006	0.022
0.6	0.007	0.005	0.012	0.004	0.014

Table 5.1: Delay (t_{pHL}) values of an inverter for different circuit techniques

5.5.2 Leakage Power and Energy Comparison

It is expected that for a fixed threshold voltage, reduction of supply voltage will provide less leakage power. Plot of leakage power versus supply voltage agrees with this theoretical assumption. Figure 5.5 shows that, as supply voltage decreases, leakage power also decreases in all circuit techniques. Leakage power is in nano-watt range. T-Spice simulation tells that, DTCMOS is not suitable for reducing sub-threshold leakage power. It is also mentioned earlier in our discussion. On the other hand, as expected from the theory, transistor stack and new design both provides a significant amount of leakage power reduction compare to the existing design. For V_{DD}=0.6V, leakage power for transistor stack and new design technique are only around 43.45nW, but for DTCMOS techniques this amount is 389.65nW. In conventional design it is 400.45nW which means our new design can reduce leakage power by around 9x than the conventional design. For V_{DD}=0.09V, our proposed new design has 2.2x reduced leakage power than DTCMOS and conventional design technique.

It is expected that in new CMOS technologies, static power will exceed the dynamic power [7]. Dynamic energy per input cycle will be same for all design techniques ($E_{dynamic}$

$= C_L * V_{DD}^2$). Now input signal period (T) for all design techniques is assumed to be same and duty cycle is 50%. The design technique that has lowest leakage power will have the lowest leakage energy per cycle also. Therefore we can say that, our new design will consume least leakage energy per cycle and hence it the most energy efficient circuit design with higher speed.

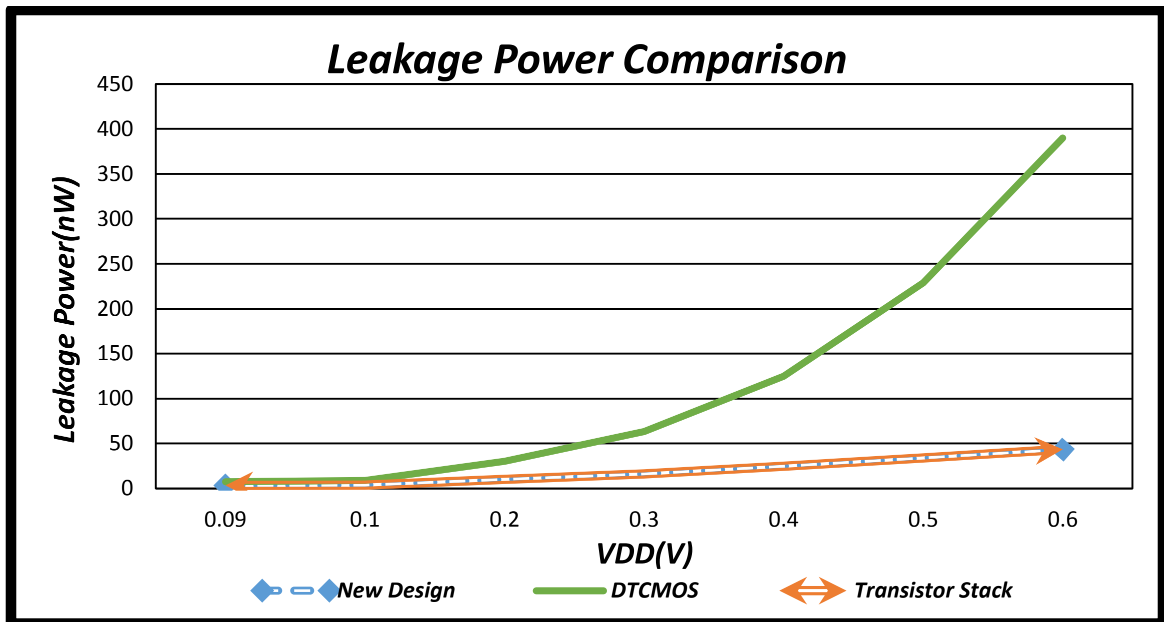

Figure 5.5: Leakage Power comparison for different leakage reduction techniques

More detail of the simulation results for leakage power per transition comparison is illustrated in table 5.2.

Leakage Power (nW)				
V_{DD} (V)	Existing Design	New Design	DTCMOS	Transistor Stack
0.09	7.15	3.23	7.35	3.23
0.1	8.55	3.65	8.8	3.65
0.2	29.8	10.1	30.3	10.1
0.3	63.15	16.25	63.15	16.25
0.4	124.68	24.675	124.68	24.675
0.5	228.6	33.75	228.6	33.75
0.6	400.45	43.3	389.65	43.45

Table 5.2: Leakage Power of an inverter for different circuit techniques

5.5.3 Delay (t_{pHL}) variation comparison

It was one of our goals of this paper to find out a variation tolerant design for ultra-low voltage digital circuits. Figure 5.6 demonstrates delay variation comparison versus supply voltage. From figure 5.6, we can find that, delay (t_{pHL}) variation increase as supply voltage reduces. Our proposed new design is more tolerant to delay variation that occurs due to the result of parameter variations. For 0.09V supply voltage our proposed design has 18% high to low propagation delay variation. It is 8.7% less than the existing design. Both DTCMOS and transistor stacking techniques have almost 23% delay variation. For supply voltage of 0.08V, our new design has a delay variation of only 21%, where all other design techniques have delay variation of more than 100%. Existing design technique has the variation of about 470%.

During high-to-low propagation delay of an inverter, pull-up Network (PUN) has leakage current flowing through the PMOS side that also contributes to the delay variation. For our proposed design, $I_{on,n}/I_{off,p}$ ratio is much higher than the $I_{on,n}/I_{off,p}$ ratios of other two designs (DTCMOS and transistor stack) and existing design techniques. It is stated earlier in chapter 1 that, $I_{off,}$ variation is extreme in recent technologies due to its exponential dependency on supply and threshold voltage variations. Therefore, delay variations in DTCMOS and transistor stack design techniques are higher than our proposed design. From 0.1V to 0.6V supply DTCMOS and our proposed new design have same effects on delay variation due to parameter deviations.

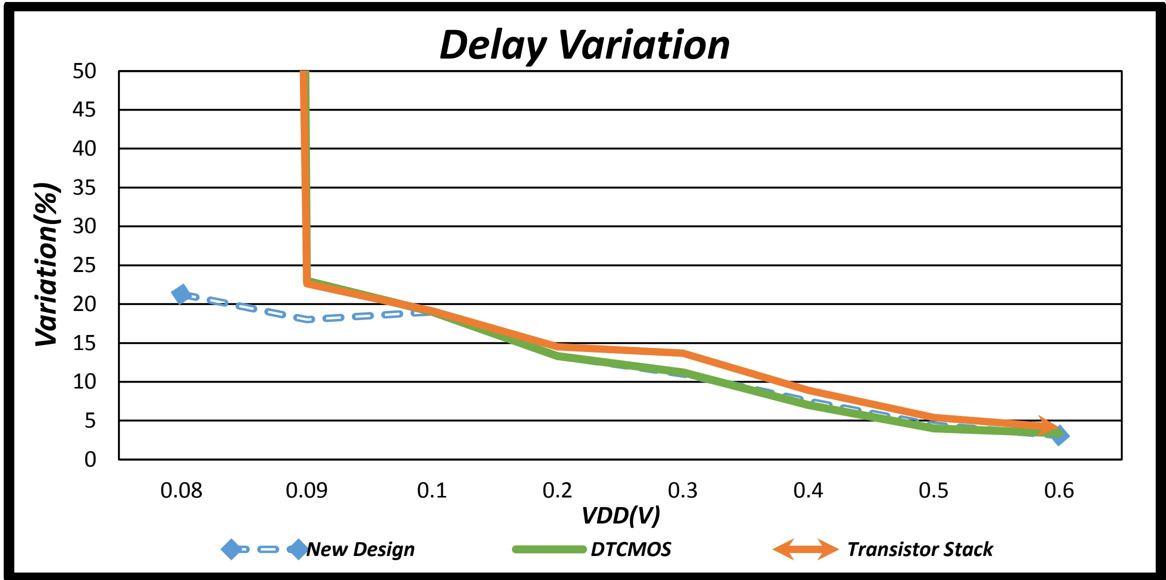

Figure 5.6: Delay (t_{pHL}) variation comparison for different leakage reduction techniques

More detail of the simulation results for delay (t_{pHL}) variation comparison is illustrated in table 5.3.

Delay variation (%)				
V_{DD}(V)	Existing Design	New Design	DTCMOS	Stack
0.08	470	21	3000	1000
0.09	26.7	18	23	22.6
0.1	18.1	19	19	19.1
0.2	13.9	13.3	13.32	14.5
0.3	13	11	11.21	13.7
0.4	8.658	7.5	7	8.9
0.5	4.81	4.4	4	5.4
0.6	3.42	3.11	3.4	4.15

Table 5.3: Delay (t_{pHL}) variation comparison for different leakage reduction techniques

5.5.4 Noise Margin (Low state) comparison

Plot of noise margin (low sate) values versus supply voltage is presented in the following Figure and table 5.4. From Figure 5.7 we can see that, as supply voltage decreases, noise margin (low) value decreases. Noise margins are in mili volt range. All three techniques, stack transistor, DTCMOS and new design have almost same noise margin when V_{DD} is less than 0.3V. Above 0.3V supply voltage DTCMOS have the least noise margin (low) value, where basic stack transistor has the highest. For 0.6V supply voltage noise margin (low) for stack transistor is 268mV, DTCMOS has 223mV only. For our new technique noise margin (low) is 255mV for 0.6V supply.

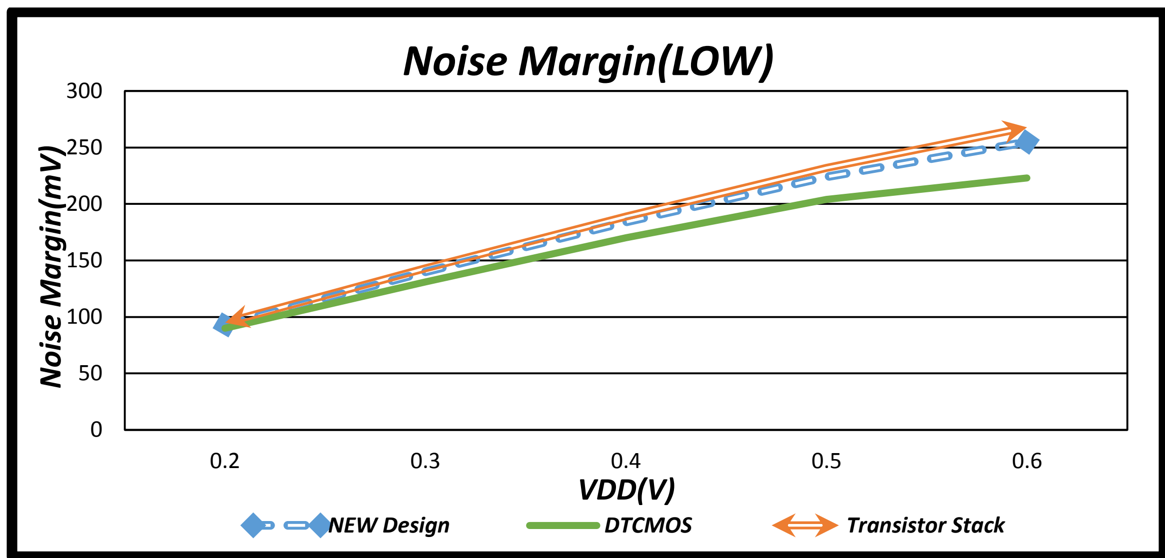

Figure 5.7: Noise Margin (Low State) comparison for different leakage reduction techniques

From table 5.4, we can see that, noise margin (low) values are overestimated in our analytical model. Both new design and transistor stack has higher values than the existing design. But it is opposite for DTCMOS.

NM LOW(mV)					
V_{DD}(V)	MATLAB	Existing Design	NEW DESIGN	DTCMOS	Transistor Stack
0.2	160	91	93	90	95
0.3	210	133	140	131	143
0.4	260	172	184	170	189
0.5	310	209	224	204	232
0.6	360	237	255	223	268

Table 5.4: Noise margin (Low State) comparison for different leakage reduction techniques

5.5.5 Noise Margin (High state) comparison

Plot of noise margin (high sate) values versus supply voltage is presented in the following figure and table 5.5. From figure 5.8 we can see that, as supply voltage decreases, noise margin (high) value decreases too. Noise margins are in mili volt range like noise margin (low) values. All three techniques, stack transistor, DTCMOS and new design have almost same noise margin. Above 0.2V supply voltage DTCMOS have the least noise margin (high) value where basic stack transistor and new design have the highest. For 0.6V supply voltage noise margin (high) for stack transistor is 192mV, DTCMOS has 172mV only. For our new technique noise margin (high) is 188mV for 0.6V supply.

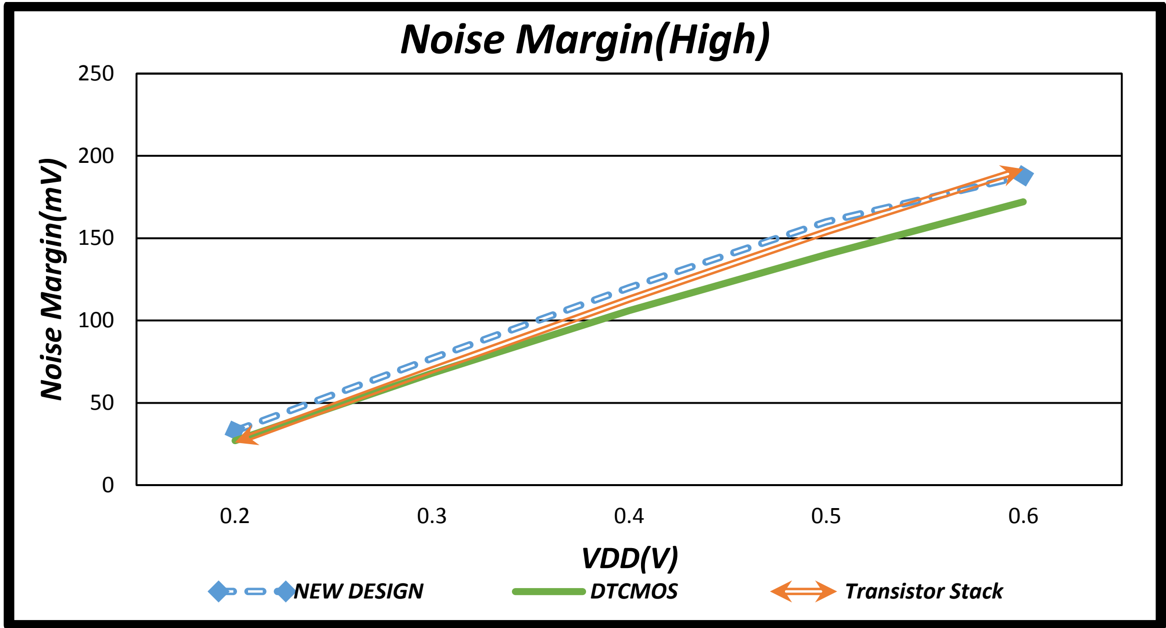

Figure 5.8: Noise Margin (High State) comparison for different leakage reduction techniques

From table 5.5, we can see that, noise margin (high) values are overestimated in our analytical model.

NM HIGH (mV)					
V_{DD}(V)	MATLAB	Existing Design	NEW DESIGN	DTCMOS W/L=100	Stack (W/L=100)
0.2	40	20	33	27	26
0.3	90	61	77	68	70
0.4	140	99	120	106	113
0.5	190	132	160	140	154
0.6	240	160	188	172	192

Table 5.5: Noise margin (High State) comparison for different leakage reduction techniques

5.5.6 Noise Margin (Low State) variation comparison

It was one of our goals of this thesis to find out a variation tolerant design for ultra-low voltage digital circuits. As a part of it, figure 5.9 illustrates noise margin (low) variation comparison versus supply voltage. From figure 5.6, we can find that, noise margin (low) variation changes slightly as supply voltage reduces. Our proposed new design is tolerant to noise margin (low) variation that occurs due to the result of parameter variations. Noise margin (low) variation in original design is not so substantial. It just increases from 2.97% to 3.41% as supply voltages reduces form 0.6V to 0.2V. All of these techniques provide approximately same result which is close to existing design. For 0.2V supply voltage our proposed design has 3.63% total noise margin (low) variation due to process parameters and supply voltage variation effects.

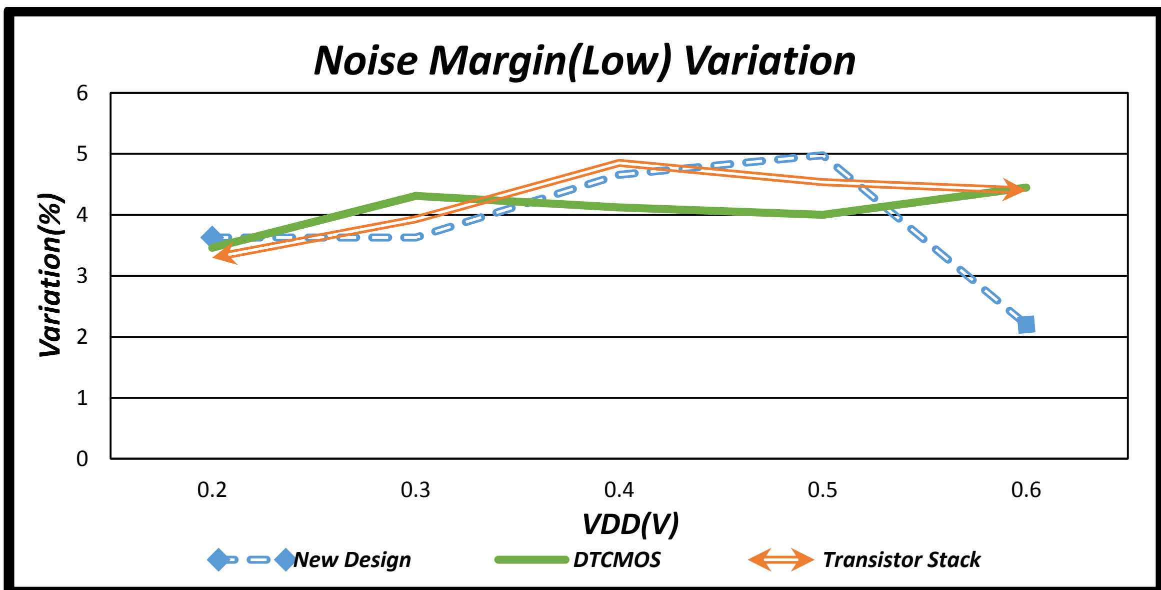

Figure 5.9: Noise Margin (Low State) variation comparison for different leakage reduction techniques

More detail of the simulation results for noise margin (Low State) variation comparison is illustrated in table 5.6.

NM (Low) variation (%)				
V_{DD}(V)	Existing Design	NEW DESIGN	DTCMOS	Stack
0.2	3.35	3.63	3.46	3.3
0.3	4.26	3.63	4.31	3.93
0.4	4.16	4.66	4.12	4.85
0.5	3.98	4.98	4	4.54
0.6	2.73	2.2	4.45	4.4

Table 5.6: Noise Margin (Low State) variation comparison for different leakage reduction techniques

5.5.7 Noise Margin (High State) variation comparison

Figure 5.6 demonstrates noise margin (high) variation comparison versus supply voltage. From figure 5.10, we can find that, noise margin (high) variation increase as supply voltage reduces. Our proposed new design is more tolerant to noise margin (high) variation that occurs due to the result of process and supply voltage parameter variations. For 0.2V supply voltage our proposed design has 16.2% noise margin (high) variation. It is 14.8% less than the existing design. Both DTCMOS and transistor stacking techniques have higher variation. For same supply voltage total variation in DTCMOS circuit is 26.8% which is 10.6% higher than our proposed design. And for transistor stack this variation amount is 21.64% which is 5.44% more than our new proposed design.

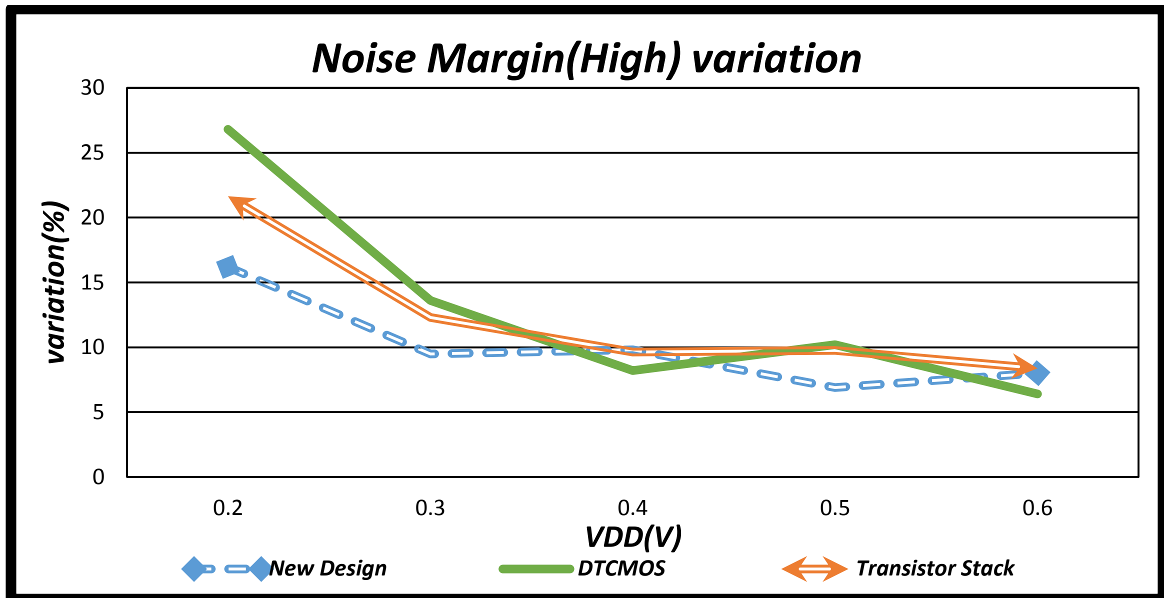

Figure 5.10: Noise Margin (High State) variation comparison for different leakage reduction techniques

More detail of the simulation results for noise margin (High State) variation comparison can be found in the following table.

NM (High) variation (%)				
V_{DD}(V)	Existing Design	NEW DESIGN	DTCMOS	Transistor Stack
0.2	26	16.2	26.8	21.64
0.3	15	9.5	13.6	12.3
0.4	12	9.8	8.21	9.63
0.5	9	6.9	10.2	9.76
0.6	10	8	6.4	8.37

Table 5.7: Noise Margin (High State) variation comparison for different leakage reduction techniques

In summary, our proposed new design is far better than DTCMOS in terms of power and energy efficiency of an inverter. It has also better noise margin (both high and low sate). But we have to compromise for circuit delay which is very less in DTCMOS inverter.

Transistor stacking technique has shown very close performance to our proposed new design technique in terms of noise margin (both high and low state) and leakage power efficiency but it has a very high delay compare to our new design technique. Moreover, our proposed design technique is more variation tolerant than other two circuit level techniques. In case of noise margin (high state) and propagation delay variation due to process parameters and supply voltage variations, our proposed design is more beneficial to use. Our proposed new design can minimize the effects of parameter variations on noise margin (high state) by around 10% for V_{DD}=0.2V and high-to-low propagation delay by 8.7% for V_{DD}=0.09V. For V_{DD}=0.08V our proposed design has around 450% of reduced delay variation.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

Due to aggressive scaling of transistors, severe issues have risen for CMOS technology in recent times. It is becoming nearly impossible to achieve Gordon Moore's law of doubling integration capacity in every 18 to 24 months. Power and energy consumptions are becoming extremely large as more transistors are packed in the same area. Ultra-low voltage circuit design is one of the most promising solutions for energy constrained systems with rigid energy budget. Supply voltages are scaled to reduce power consumption and to maintain constant electric field for CMOS scaling. This results in a significant performance penalty. Threshold voltage of a device is scaled accordingly to boost the performance. Therefore, increased impact of process parameter variations and increased sub-threshold leakage current has become emerging concerns.

This increased impact of process parameters and supply voltage variations have created a severe bottleneck for ultra-low voltage digital circuit design. Although this issue is well known and has been mentioned in several studies but it is yet to be fully analyzed. To reduce the yield loss and production cost, it is necessary to estimate the variation effect on digital circuit's static and dynamic characteristics properly. In this thesis, we have derived some closed form analytical models to estimate the delay and noise margin

variations of a digital circuit. Simulation results obtained by implementing our closed form analytical models in MATLAB are compared with the T-Spice simulation results that are based on PTM's (Predictive Technology Model) 22nm process technology standard. Results found from both simulations are close enough to claim that these closed form analytical models can estimate delay and noise margin variation of a digital circuit accurately.

In chapter 5, a new circuit level technique was proposed to mitigate the effects of process parameters and supply voltage variations on a digital circuit's performance and robustness and also to reduce leakage energy of the circuit. Again delay and noise margin of an inverter are taken into account as circuit's characteristics. This new proposed digital circuit (inverter) design technique not only reduces the process and supply voltage variation effects but also reduces sub-threshold leakage power consumption without increasing the delay of a circuit substantially. This proposed technique is compared with two existing energy efficient circuit design techniques (Transistor stack and Dynamic Threshold CMOS) and T-Spice simulation results infer that the proposed technique is more variation tolerant. New design provides minimum amount of leakage energy for any supply voltage. Transistor stack technique also provides same amount of leakage energy but delay penalty is much higher compare to our proposed design. This new technique can reduce within die delay variation of an inverter by 8.7% for 0.9V supply voltage and noise margin (high) variation by 10% when supply voltage is 0.2V. For V_{DD}=0.8V, all circuit design techniques except our proposed new design has delay variation of more than 100% where our new design provides only 21% of delay variation. It also offers better performance than

DTCMOS and existing design technique in terms of noise margin of the circuit. However, there is an extra area requirement for this design, and design complexity is also higher.

6.2 Future Work

The closed form analytical models that are derived in this thesis are based on the major process parameters (Channel length, width and threshold voltage) and supply voltage variations. In reality, CMOS technologies has more sensitive parameters (e.g. oxide thickness and etc.) other than the ones aforementioned and can affect circuit performance severely. Also, to simplify our models we have ignored DIBL, Gate tunneling and other short channel effects. This closed form analytical model's concept can be extended further by including all other short channel effects and other process parameters to find the effects of process variation on low voltage digital circuit more accurately. It is important to note that, we have just focused on inverter circuit in this thesis. Similar techniques can be applied to analyze other digital circuits such as NAND, NOR and etc. This 22nm CMOS technology is still a vast area of research. These analytical models are very effective tools in designing and making crucial decisions for low and ultra-low voltage digital circuits.

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