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LARGE-AREA, WAFER-SCALE EPITAXIAL GROWTH OF GERMANIUM ON SILICON AND INTEGRATION OF HIGH-PERFORMANCE TRANSISTORS

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LARGE-AREA, WAFER-SCALE EPITAXIAL GROWTH OF GERMANIUM ON SILICON AND INTEGRATION OF HIGH-PERFORMANCE TRANSISTORS

BY

SWAPNADIP GHOSH

B.Tech University of Kalyani, India

DISSERTATION

Submitted in Partial Fulfillment of the
Requirements for the Degree of

**Doctor of Philosophy
Engineering**

The University of New Mexico
Albuquerque, New Mexico
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DEDICATION

I dedicate this work, first and foremost, to my beautiful wife, Sudakshina Das. Her support and understanding of all the late evenings and weekends spend studying and working in the lab has allowed me to fulfill my research goals for this work. Without the sacrifices she made in allowing me to pursue my dreams, none of this work would have been possible. She has been the best friend, supporter, and partner I could have asked for.

Second, this work is dedicated to my parents Parimal Ghosh, and Aruna Ghosh for their support and encouragement to fulfill my potential and pursue my dreams. I hope I have made them proud of my accomplishments and will continue to do so in my future endeavors.

Third, I also dedicate this work to my extended family and friends for their encouragement and understanding when I was often absent from family functions, both mentally and physically.

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I wholeheartedly acknowledge my research advisor, Sang Han, in the accomplishment of this work. He has been a dedicated teacher, mentor, and friend to me throughout graduate school, and I know he will continue to be so in the future. I also thank him for the long hours spent teaching me the art of technical writing.

I wish to thank my dissertation committee for taking the time to read my dissertation and provide me with feedback on my research. They are all excellent teachers and I have greatly enjoyed and benefited from attending their courses.

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ABSTRACT

Building on a unique two-step, simple MBE growth technique, we have investigated possible dislocation locking mechanisms by dopant impurities, coupled with artificially introduced oxygen. In the case of n-type Ge grown on Si, our materials characterization indicates that the dislocation density (DD) can reach the $\sim10^5$ cm^{-2} level, compared to p-type and undoped Ge on Si (GoS). We note that our Ge film covers the entire underlying Si substrate at the wafer scale without mesas or limited-area growth. In this presentation, we will focus on the use of n-type impurity (phosphorus) diffusing from the Si substrate and the introduction of O at the Ge-Si interface. The O is introduced by growing a thin chemical SiO$_2$ layer on top of the Si substrate before Ge epitaxy begins. Z-contrast cross-sectional TEM images suggest the presence of oxygen precipitates in n-type Ge, whereas these precipitates appear absent in p-type Ge. These oxygen precipitates are known to lock the dislocations. Supporting the argument of precipitate formation, the TEM shows fringes due to various phase boundaries that exist at the precipitate/Ge-crystal interface. We speculate that the formation of phosphorus (P) segregation resulting from slow diffusion of P through precipitates at the precipitate/Ge-crystal interface facilitates dislocation locking. Impurity segregations in turn suppress O

concentration in n-type Ge indicating reduced magnitude of DD that appears on the top surface of n-Ge compared to p-Ge film. The O concentrations (10^{17} to 10^{18} cm^{-3}) in the n- and p-type GoS films are measured using secondary ionization mass spectroscopy. We also demonstrate the technique to improve the Ge epitaxial quality by inserting air-gapped, SiO_2-based nanoscale templates within epitaxially grown Ge on Si. We have shown that the template simultaneously filters threading dislocations propagating from Ge-Si interface and relieves the film stress caused by the TEC mismatch. The finite element modeling stress simulation shows that the oval air gaps around the SiO_2 template can reduce the thermal stress by 50% and help reduce the DD. We have then compared the structural and electrical characteristics of n-type Ge films with its p-type counter parts. In n-type Ge, the DD decreases from ~10^9cm^{-2} near the Ge-Si interface to ~10^5 cm^{-2} at the film surface. In contrast, we observe 5×10^7 cm^{-2} TDD at the film surface in p-type Ge. The full width at half-maximum for our n-type Ge(004) XRD peak is ~70% narrower than that of p-type Ge. As a stringent test of the dislocation reduction, we have also fabricated and characterized high-carrier-mobility MOSFETs on GoS substrates. We also report p- and n-MOSFETs with μ_{eff} of 401 and 940 cm^2/V-s and a subthreshold slope of 100 and 200 mV/decade, respectively. These effective mobilities show an exceptional 82 and 30% improvement over that of conventional Si channel MOSFETs. We also investigate the optical quality of ultra-low DD GoS film by measuring photoluminescence (PL). The n-type Ge PL main peak shows pronounced tensile-strain ($\times0.8\%$) than that of p-type which is an indicator of direct BG shrinking at the Γ band-edge. Going beyond epitaxial engineering and device fabrication, we have also recently demonstrated a scalable path to create a 2D array of Ge quantum dots (QDs) on

responsive SiGe substrates based on elastic mechanical deformation and subsequent SiGe compositional redistribution, coupled with MBE growth. For large-scale manufacturing of single-electron transistors, we have also demonstrated that a spatially structured elastic compressive stress to the SiGe substrate with thermally annealing leads to a compositional redistribution of Si and Ge in the near-surface region of SiGe substrates, forming a 2D array of Ge-depleted nanoscale regions. Based on these latest findings, we have also begun to chart a future direction for my research group, where one can explore new advanced device architectures, such as Si-compatible, optically actuated, Ge-quantum dot-based field effect transistors.

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CHAPTER 1 INTRODUCTION

1.1   MOSFET Scaling Benefits

Compact integrated circuits (ICs) are the heart of present

technology. Over last few decades, we have seen a phenomenal progress in terms of the

integration of ICs. For instance, to realize denser ICs on a chip, our presnt technology

offers ultra-low-scale-integration (ULSI) instead of very-large-scale-integration (VLSI).

Over the past 50 years, Moore's law, first stated in 1965, has been considered to be

sacrosanct for all VLSI people which simply described that the number of transistors on a

chip to double about every two years [1]. This remarkable progress in integration has

been realized by continual downscaling of the gate-length in metal-oxide-semiconductor

field-effect transistors (MOSFETs). To abide by Moore's law, the physical dimensions

of MOSFETs have been downscaled using constant field scaling approach where the

MOSFETs not only become smaller over this years but they also become inexpensive,

power efficient, become faster, and enable more logic functions per unit area of a

die. The large density, by integrating more and more devices/chip allows technologist to

offer superior performance from ICs at reduced cost per function as shown in Figure 1.1.
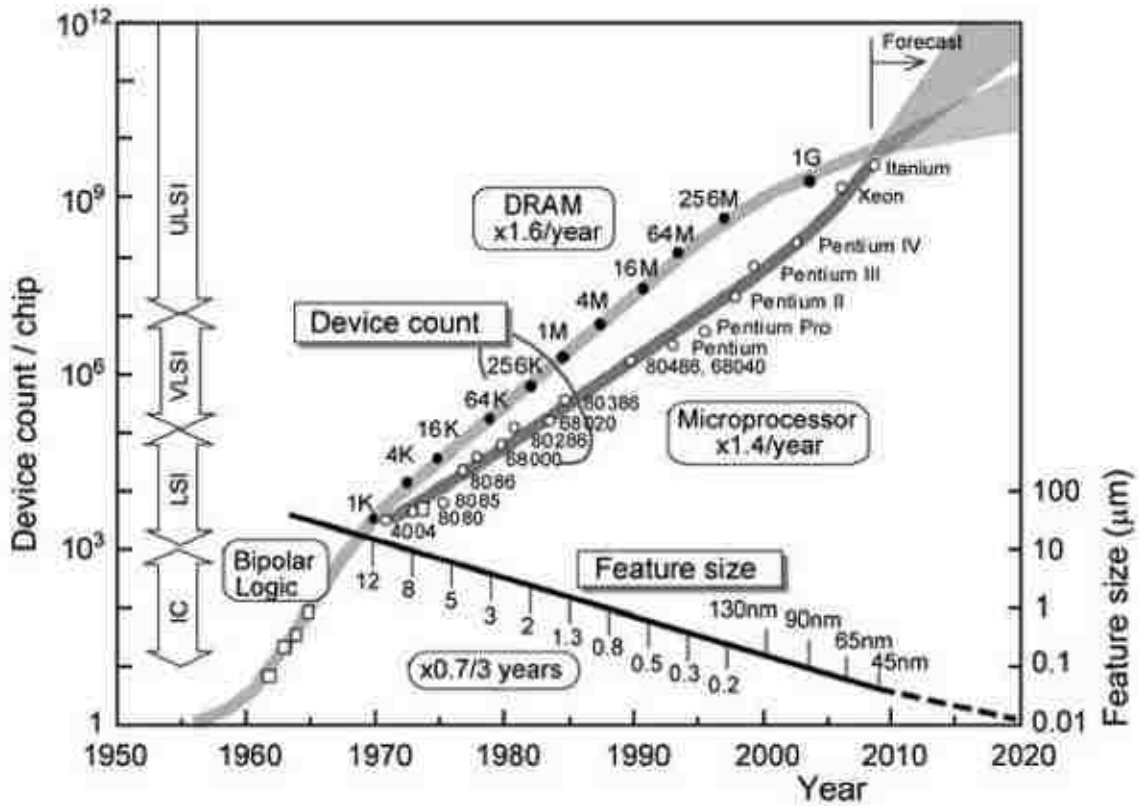
Figure 3.1. Trends in device count/chip and feature size of MOS device, as a function of the year of production [2].

1.2   Beyond Scaling

We mention in our previous section that the scalability is the main reason of the tremendous success in complmentary metal-oxide-semiconductor (CMOS) compatible Silicon (Si) based IC technologies. According to Moore's law, shrinkage in physical dimensions of transistors boost device performance. Based on constant-field scaling approach,upon the physical dimension of transistor by *S* (scaling factor), the depletion width has to be shrunk by *S* to ensure normal device performance. The doping density increases with reducing depletion width, and applied voltage at the transistor terminal reduces by factor *S* to maintain constant-field since

$$depletion\ width \sim \sqrt{(doping\ density) \bullet (applied\ voltage)}$$

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As a result, the direct consequence of constant-field scaling is three-folds: first, increased

component density by a factor of S^2 ; second, increased speed of a transistor by a factor of

S because of the reduced transit time of carriers in transistors and capacitance RC delay;

third, power-density of the component remains constant.

However, constant-field scaling approach fails as physical

dimensions of the transistors shrink further to 100 nms[3] because the applied voltage can

not be scaled anymore by a factor of S with continuously shrinking dimensions because

of constraint on the threshold bias to avoid increasing standby power during "off" state of

transistors. Considering impossibility of continuously scaling applied voltage with

shrinking dimensions, for the first time in 2005 [4], a constant-voltage scaling approach

was proposed to overcome this challenge. The following table 1-1 shows performance

parameters of transistor based on constant-voltage scaling,

Table 1-1: Transistor parameters scaling based on constant-voltage scaling

Regular Parameters	Scaled Parameters
W, L, t_{OX}, X_j	Scaled by S
V_{dd}, V_t	Do not scale
N_a, N_d	$S^2 N_a, S^2 N_d$
$I_{d, sat}$	$S I_{d,sat}$
P_{ds}	$S P_{ds}$

For simplicity, we consider an example of n-MOSFET, and corresponding schematic is

shown in Fig. 1.2.
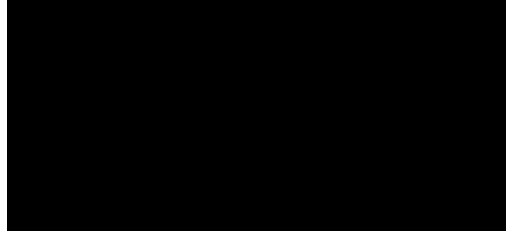
Figure 1.2: Schematic of n-MOSFET

In case of n-MOSFETs, electrons are the major carriers in the inversion channel. Considering a channel length of L, and electron velocity of v, the transit time (t) for carriers from source to drain is $t = L/v$. The transit time for carriers is becoming smaller with shorter L, considering that v approaches to v_{sat} in small channel length transistor. Essentially this means that the transistors speed always increases with shrinking physical dimension of transistors. Besides benefiting speed, however, the saturation current density and power density go up with shorter channel length of transistors. The direct consequence of increasing power density is significant heat dissipation, prohibits further increase in the clock speed of transistors.

Researchers have realized that further increase in the clock speed can not be only improved through scaling, and time has arrived to reconsider a complete new device architecture or reexamine different material platform that can offer higher clock speed than that of Si. For instance, transistors built on SiGe substrate can offer an intrinsic speed of 500 GHz [5] compared to 100 GHz [6] on Si platform, and transistors fabricated on material such as InP can offer intrinsic speed of 1000 GHz [7]. The speed bottleneck is also depended on propagation delay through passive interconnects. Several ideas have been proposed to replace aluminum-based (electric conduction) and SiO_2 (electric insulation) interconnects by Cu-based and low-k dielectric materials (such as

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doped SiO_2). Another efficient approach to reduce propagation delay is to use optical interconnects instead of electric interconnects. In this retrospect, Si-based photonics allows designing of interconnects extremely efficient, and potentially a strong contender in next generation device architecture.

1.3   Emerging CMOS Technology Roadmap
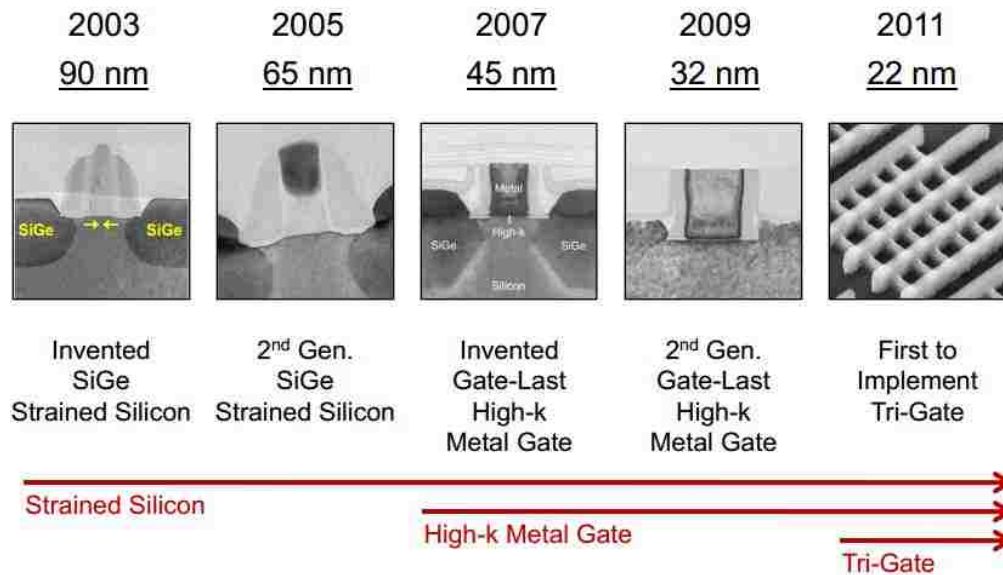
Figure 1.3: Intel Si-Transistors Scaling and Roadmap until 2012 [8].

Over the past decade or so, various novel processes and design architectures are being introduced into fabrication of advanced Si-MOSFETs in order to maintain the historical 17% improvement per year. Figure 1.3 shows evaluation of advanced Si-based transistors roadmap proposed by Intel in 2012 [8]. As the physical dimension of gate-length starting to shrink such as 90 nm, 60 nm, Intel introduced strained-Si instead of bulk-Si substrate in their MOSFETs. Intel put too much effort in introducing strained-Si in this technology nodes because to get benefit from increasing carrier mobility (and thus improving ON current) by strain engineering. To achieve their

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goal to produce strained-Si based transistors in a large-manufacturing scale [9,10], Intel

adopted uniaxial-strain induced process in their sub-100 nm logic-technology nodes. A

major invention occurred in 2007 when Intel for the first time introduced High-k

dielectric as gate oxide, and gate-last technique instead of conventional SiO_2, and gate-

first technique in their transistor fabrication processes. The main reason behind adopting

high-k gate dielectric was to maintain oxide thickness at low gate leakage current. Later

in 2011, Intel has revolutionized their design of transistors by putting tri-gate geometry in

22-nm-node transistors for the very first time. However, scaling beyond 22-nm or 10-

nm-node would probably require a complete new device architecture or a new material

platform altogether.
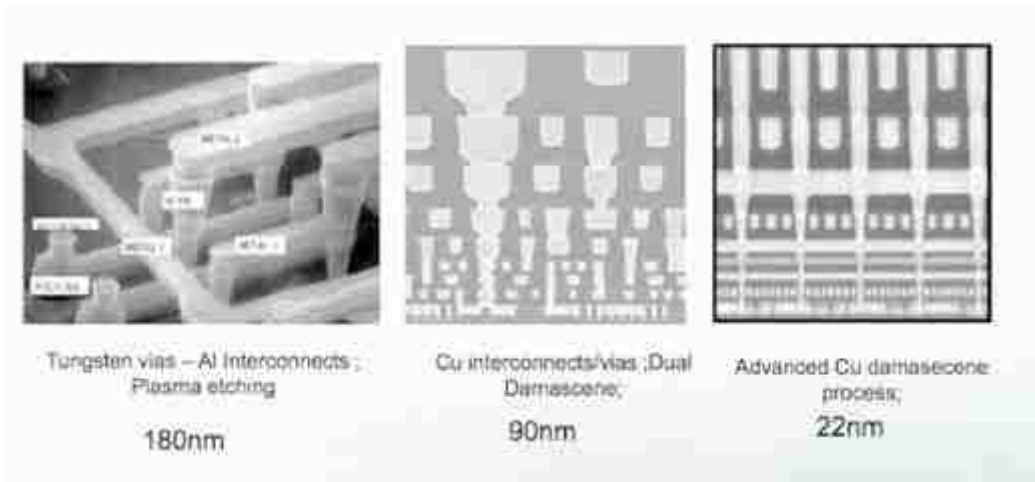
Figure 1.4: Evolution of Metallization [8]

As the speed of transistors becoming higher with shrinking

transistors geometry, it is becoming incredibly important to maintain the speed through

back-end metal lines that interconnect these transistors. Figure 1.4 shows an evaluation

of back-end metallization schemes that have been taken place over these years with

shrinking dimensions of transistors, such as 180 nm to 22 nm. Before 180 nm nodes,

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mostly the metallization schemes used Al interconnects through SiO_2 vias. However, we notice Al interconnects through W vias were used at 180 nm nodes to minimized RC delay between transistors. This invention opened up a new path for metal interconnects, however faced tremendous mechanical stability. In comparison to 180 nm nodes, IBM revolutionized assembly of interconnects at 90 nm nodes by introducing Cu interconnects/vias thorugh dual damascence. This allowed IBM to demonstrate an assembly of interconnects upto 9 layers at 90 nm node technology. Since then, this Cu interconnects/vias have been matured to integrate in 22 nm node technology which allowed Intel to assembly more than 9 layers of interconnects. Hence, the 22 nm nodes with several layers of interconnects allowed chips to perform complex logic functions efficiently than before. However, beyond 22 nm or so on, the density of transistors and number of interconnects that are going to exist in a chip will be incredibly large. As a direct consequence of large number of interconnects, the time delay among transistors will be a critical issue. It is entirely possible that scaling beyond 22-nm or 10-nm-node would probably require a complete new interconnect platform. Presently, Intel and others are speculating to make use of optical interconnects instead of traditional electric interconnects. Si-based photonics can potentially provide a good platform for optical interconnects which can perform efficiently with smaller footprint of transistors.
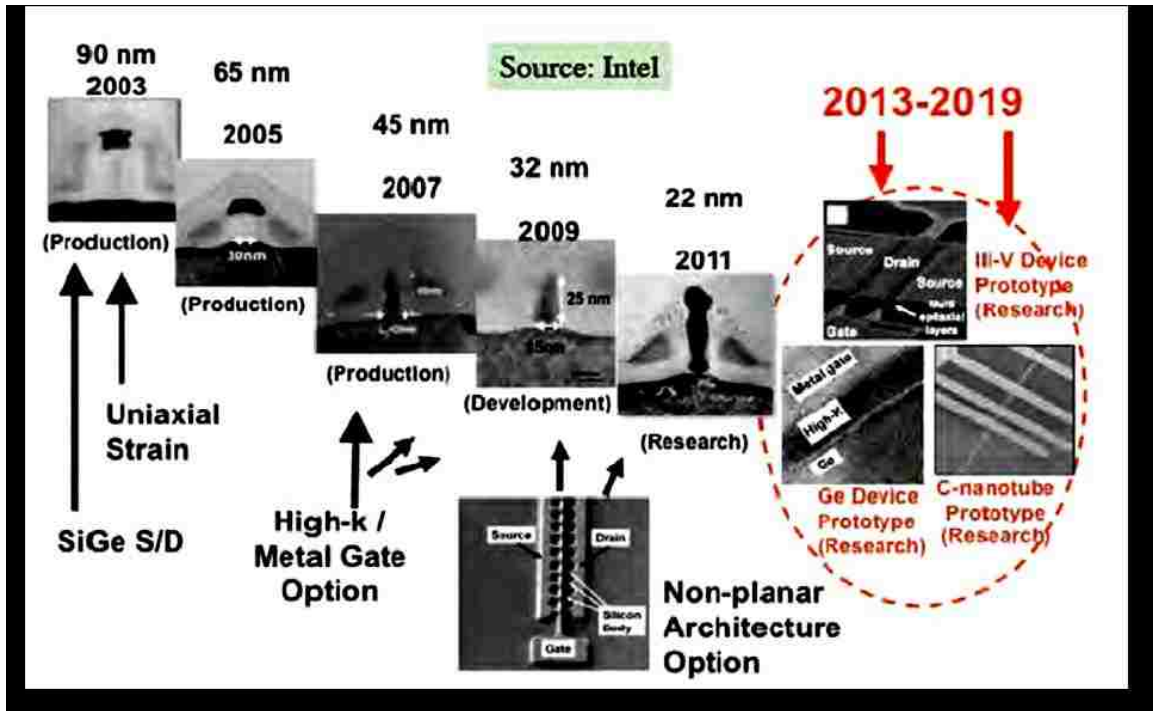
Figure 1.5: MOSFET Transistor Scaling and Roadmap [9]

Scaling beyond 22 nm or smaller will probably require total structural changes in the transistors designing or probably require to use a higher carrier mobility materials such as Germanium or III-V semiconductors than that of Si. Figure 1.5 shows a roadmap predicted by ITRS on scaling of MOSFETs and its architectures. With smaller nodes, not only transistors start to use High-k dielectrics as a gate oxide also the architecture of transistors moved from planar to non-planar. For instance, ultra-thin body FETs or multi-gate FETs architectures are considered as potential replacement for bulk-MOSFETs because of their inherent superior electrostatic integrity [10-12]. Another promising alternative is to use higher-carrier mobility channel materials such as Ge which possess four and two times larger holes and electron mobility than that of Si counterpart [13-16]. The roadmap also predicts about three major materials platform that potentially can complement existing Si-based technology, are Ge, III-V semiconductors such as GaAs, InP, InAs etc [17-19], and carbon-nanotubes [20-21].

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1.4   The Promise of Silicon Photonics

"As newer, faster microprocessors roll out, the copper connections that feed those processors within computers and servers will prove inadequate to handle the crushing tides of data."(*Paniccia & Koehl, 2006*).

Electronics is the technology of controlling the flow of electrons whereas photonics is the technology of controlling electrons whereas photonics is the technology of controlling the flow of photons. Electronics and photonics have been joined together in semiconductor optoelectronic devices where photons generate mobile electrons, and electrons generate and control the flow of photons generate and control the flow of photons. The compatibility of semiconductor optoelectronic devices and electronic devices has, in recent years, led to substantive advances in both technologies. Semiconductors are used as optical detectors, sources (LEDs and lasers), amplifiers, waveguides, modulators, sensors, and nonlinear optical To meet challenges in high-density data communication systems, real-time sensing/detection, and high-speed control/actuation, it has become necessary to develop a new compactly integrated optolectronics platform that can potentially capable of handling large speed-bandwidth requirements. One of the most studied systems of optoelectronics is the Si photonics system. The Si-based photonics system studies the principles and technologies of merging electronics and photonics into the silicon platform. It is considered a more efficient and lower cost optical solution for high density data communications in optical fiber system and computer system. It is expected that a successful monolithic integration of silicon based nanophotonic devices and microelectronic devices will lead to a more

significant "micro optoelectronics revolution" than the well-known "microelectronics "revolution".
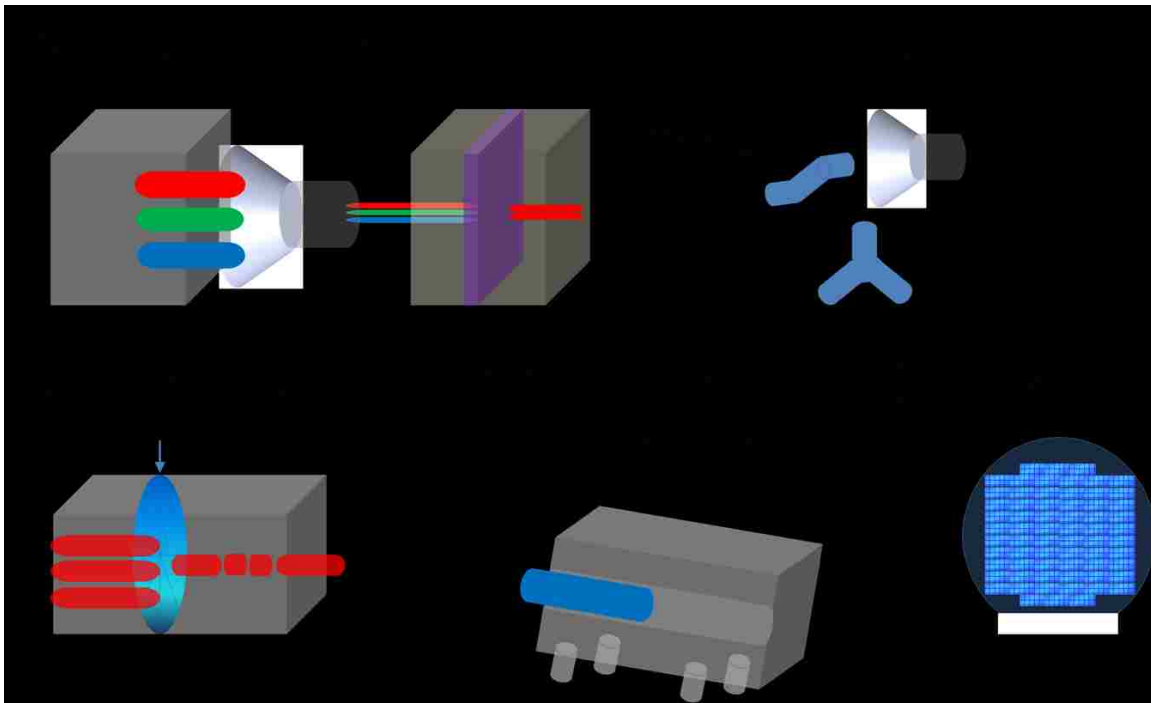
Figure 1.6: Components for Siliconization [22]

Si photonics offers a promising platform where optics and electronics can be integrated monolithically using conventional CMOS processing [23]. Figure 1.6 shows few examples of source, detector, modulator etc. that can built on Si photonics platform. There are some exclusive features that a Si platform can offer compared to it electronics counterpart.

First, photons will be transmitting information in a Si photonics platform. There are many benefits of optical communications: 1) high-speed or bandwidth can be achieved owing to short RC delay; as different wavelength photons don't interact with each other, so multiple wavelengths can co-exist in a communication channel resulting in large information carriage. This technique is called wavelength-

division-multiplexing (WDM). For instance, Luctera corporation demonstrated the capability of Si photonics device by showing performance from a four-channel WDM transceiver [24] ; 2) optical fiber offers low-attenuation which can be used for long-distance communication; 3) optical fibers are low-cost transmission medium mostly based on silica and polymer materials which are inexpensive compared to traditional metal lines.

Second, optical interconnects among chip-to-chip or device-to-device can be totally deployed at different levels using Si photonics platform. The propagation delay between circuits or chips is mostly dominated by RC delay. Once the optical interconnects are deployed and activated, the RC delay issue no longer exists, and the speed will no longer be limited by scaling. For instance, the propagation delay of optical interconnects, which are not subjected to RC delay, is the gate delay, which decreases with physical dimension. Besides very short propagation delay, optical interconnects also provides large capacity/unit area by employing dense WDM technique, which succeeds in the optical fiber systems [25].

Third, Si photonics is a perfect platform where electronic and photonic components can be integrated using hybrid integration scheme. The integration itself is a challenging task, and needs careful designing of each component, which is a subpart of this large Si photonics platform. The major components of this platform are optical devices (both active and passive) such as LASER, modulator, filters, waveguides, and electronic devices such as Si CMOS circuitry. For instance, Si is an ideal material for passive components in the optical interconnects, owing to its transparency in the wavelength range of 1.1 μm to 7 μm. The function of Si-based optical interconnects is not limited by the most useable near infrared (NIR) communication wavelength of 1.3μm

to 1.55 µm. Beside optical interconnects, owing to large refractive index difference between Si and SiO_2 as a core and cladding materials (Si~3.6 and SiO_2~ 1.5), Si platform can be used to design a compact waveguide for propagating optical information between components. Although Si is a good choice for designing passive components, however, it is not an ideal choice for active application such as photodetection, generation, and electrooptic modulation. Intrinsic Si without further material engineering, lacks in electrooptic effect (Pockel effect) because of its centrosymmetric crystal structure [26,27]. Additionally, Si is not an efficient photodetector due to its transparency at NIR wavelengths. In comparison, SiG based devices can create electrooptic modulation, and photodetection more efficiently than Silicon. The band-gap (BG) of SiGe can be artificially engineered to produce optical modulation, which is which is based on Franz-Keldysh (FK) effect [28]. Also, tensile-strained engineering scheme can be used to capture photogenerated carriers more efficiently using SiGe based devices [29, 30].

1.5   Why Germanium?

Previous sections somehow capture the idea that there is a significant need for finding devices built from new materials, which potentially can perform faster than that of devices fabricated using existing Si CMOS technology. The major reason of finding new materials platform is two-fold: first, the devices would not be limited by scaling, and second, the new material would complement Silicon. Among many materials, Ge is one of such promising material that have shown enormous promise. Germanium possesses many advantages compared to its counterpart Silicon. The lattice electron and hole mobility (μ_n and μ_p) are 3900 and 1900 cm^2/V-s for Ge, compared to 1400 and 470 cm^2/V-s for Si. In other words, the electron and hole bulk

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mobility of Ge is 2.75 and 4 times than that of Si [31]. The direct consequence of high lattice mobility is large surface mobility that Ge provides. As a result, owing to large bulk and surface mobility, the transistors fabricated from Ge shows high speed. Besides outstanding mobility of Ge, the electron and hole mobility in Ge are more symmetric compared to Si. This leads to smaller footprint area in Ge-based pMOS in a CMOS inverter cell, compared to Si-based pMOS.
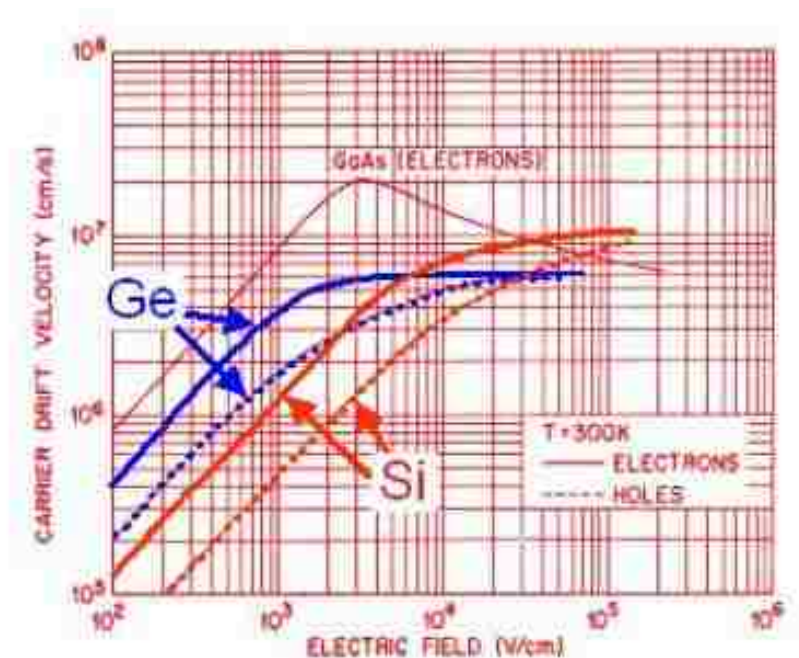
Figure 1.7: Carrier drift velocity (cm/s) as a function of electric field (V/cm) [31]

Beside larger bulk carrier mobility compared to Si, Ge also shows a significant improvement over Si in its ballistic limit. An electron in a ultra short channel device operated under ballistic limit, is no longer dependent on scattering, and the saturation drain current ($I_{d,sat}$) is no longer influenced by saturation velocity (v_{sat}) of electron. Rather in short channel devices, the $I_{d,sat}$ now depends only on thermal injection velocity (v_{inj}) [32-34]. For instance, lets look at the case for standard MOSFET. Figure 1.8 shows a band diagram of a source side of MOSFET.

Figure 1.8: Band-diagram from source side to drain side under ballistic limit.

The drain to source drive current under ballistic limit can be calculated based on following set of equations, which are derived from the band-diagram shown above. The equations are as follows,

$$I_{ds} = w \times Q_{inv} \times v_{inj};$$
$$and \qquad\qquad (1\text{-}1)$$
$$\frac{C_{load} \times V_{ds}}{I_{ds}} = \frac{L_g \times V_{ds}}{(V_{ds} - V_{th}) \times v_{inj}}$$

$$(1\text{-}2)$$

and,

$$v_{inj} \propto \mu_{low\text{-}field} \propto \tau_0$$
$$and \qquad\qquad (1\text{-}3)$$
$$\tau_0 = \frac{r_0}{1 + r_0}$$

where I_{ds} = drain to source current, w = gate length, Q_{inv} = inversion charge density in a channel, v_{inj} = injection velocity at source end, C_{load} = load capacitance, V_{ds} = drain to source voltage, L_g = gate length, V_{th} = threshold voltage, $\mu_{low\text{-}field}$ = low-field electron mobility, τ_0 = mean time between scattering events, and r_0 = reflection coefficient. Based on eqns. 1.1 and 1.2, the drive current and delay in channel of MOSFET is a function of

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v_{inj}, which is directly proportional to $\mu_{low\text{-}field}$ and τ_0. The eqn. 1-3 shows that τ_0 can be explained in terms of r_0. In the first order of ballistic limit, Ge channel has larger $\mu_{low\text{-}field}$ and smaller r_0 than that of channel of Si MOSFETs. Consequently, the Ge-based ballistic MOSFETs have larger injection velocity, channel mobility, and smaller gate delay compared to Si-based ballistic MOSFETs.

The band gap is an especially important property because it determines the emission and/or absorption wavelength of devices made from these materials such as light-emitting diodes (LEDs), solar cells, lasers, and detectors. Ge, like Si, is an indirect BG semiconductor material. Like Si, the band structure of Ge shows that the conduction band (CB) minimum occurs at the L valley. In comparison, the III-V materials such as GaAs, InP etc. exhibits direct BG properties where the CB minimum occurs at Γ valley, instead of L valley. Owing to its direct BG properties, III-V materials are considered for fabricating active components such as integrated light sources and photodetectors as compared to Si or Ge. Despite its indirect band alignments, the CB of Ge at the Γ valley ($E_{\Gamma1}$) is only 136 meV higher than the L valley (E_g) with respect to VB maximum, as shown in figure 1.9 [35]. The energy difference between Γ and L valley can be further reduced by introducing uniaxial or biaxial tensile strain in Ge. The direct gap shrinks faster than indirect gap with applied tensile stress in Ge. Therefore, optoelectronics properties of Ge can be possibly enhanced by utilizing strain engineering, which greatly helps to modify the band structure of Ge.
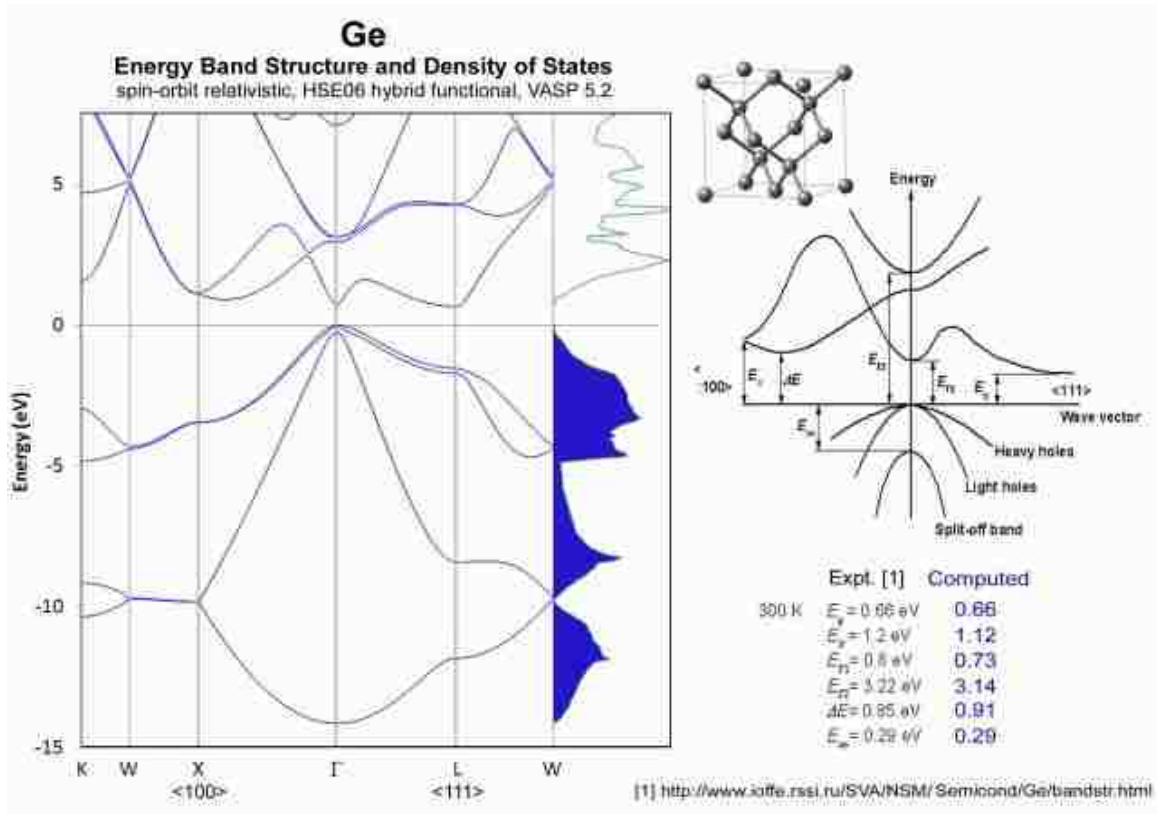
Figure 1.9: Computed energy band structure and density of states at equilibrium of elemental Germanium [35]

Strain modification in Ge can be performed in several ways. The widely known method of introducing tensile stress in Ge layer is to grow Ge on Si substrate. Owing to the thermal expansion coefficient difference between the Ge film and the Si substrate will lead to about 0.2% thermally induced tensile strain after cooling down from typical growth temperature (>650∘C) to room temperature. Based on energy difference vs tensile strain % calculation reported in [36], the 0.2% thermal induced strain can decrease the energy difference between Γ and L valley from 136 to about 110 meV. Another strategy that has been adapted by [37] to further shrink for the energy difference between $E_{\Gamma l}$ and E_g is to dope Ge with n-type dopnats, which fill electrons into the L valleys up to the level of the Γ valley. Recently, few groups have exercised an alternative approach to convert Ge

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a direct BG semiconductor by introducing tin (Sn) into the Ge [38]. The direct BG of GeSn

alloys vary between 0.61 and 0.35 eV with Sn concentrations between 6 and 15%.

Furthermore, GeSn alloys exhibits higher carrier mobility than that of Ge, which makes it

a promising material for optoelectronic applications.

1.6   Importance of Heteroepitaxy of Ge-on-Si

Single-crystal growth of a semiconductor material on another, as

known as Heteroepitaxy, is extremely important for the development of various devices

and systems, and its applications are ranging from electronics, photonics, and all the way

up to biomedical imaging. There are three important features associated to heteroepitaxy:

substrate engineering, heterojunction devices, and device integration. Figure 1.10 shows

some of the semiconductor materials, and their corresponding electronic properties

such as BG, and lattice constants, which make   them   interesting   for   device

applications. The BG of a material is an important parameter because it determines the

emission wavelength for a photonic device such as light-emitting diode, lasers etc.

However, owing to different BG and lattice constants of materials, in most cases, growth

of materials require mismatched heteroepitaxy.   Intelligent substrate engineering

practices allow us to epitaxially grow certain materials that are unavailable in the form of

large-area, high-quality, single-crystal wafers. Few widely available substrates are Si,

GaAs, InP, 6H-SiC, 4H-SiC, and sapphire (α-Al$_2$O$_3$) that are available with acceptable

quality. Among these, only selected low-index crystal orientations are available for

commercial use: Si (001), Si (111), GaAs (001), InP (001), 6H-SiC (0001), 4H-

SiC (0001), and sapphire (0001). For instance, ternary and quaternary alloys can

potentially have some interesting applications, although producing those alloys require

rationality in choosing one of these regular substrates with chemical and crystallographic compatibility. Another instance is GaN heteroepitaxially grown on SiC or sapphire substrates because of GaN has the optimized BG for emitting blue and violet wavelengths. Beside necessity, materials cost also a reason to practice substrate engineering. For instance, owing to cheaper cost and availability of Si compared to GaAs, there is a huge push in adapting Si-based platform for future photonics applications instead of GaAs-based platform, which is better suitable for photonics.

Several heterojunction devices including laser diodes, high-luminescence light-emitting diodes, strained layer superlattice (SLS) lasers and detectors, and high-frequency transistors would not have existed without heteroepitaxy. Heterojunction devices also took a giant leap with the development of SiGe heterojunction transistors such as heterojunction bipolar transistor (HBT). Heteroepitaxial growth modes including Stranski–Krastanov (SK) or Volmer–Weber (VW) allows us to fabricate quantum dot devices, including lasers and single-electron transistors.

Another area in which heteroepitaxy made or making tremendous contribution is integrated circuits (ICs). Each heteroepitaxial platform offers unique advantage over other systems. For instance, group-IV based heteroepitaxial systems are efficient in applications such as high-density digital circuits, sensors, high-power electronics, high-frequency amplifiers. In comparison, III-V based heteroepitaxial systems are actively used in applications such as optoelectronic devices including light-emitting diodes and lasers, modulators, and detectors. . Heteroepitaxy can be used to

integrate the applications of several niche materials onto a single chip, leading to a substantial reduction in cost, size, and weight.
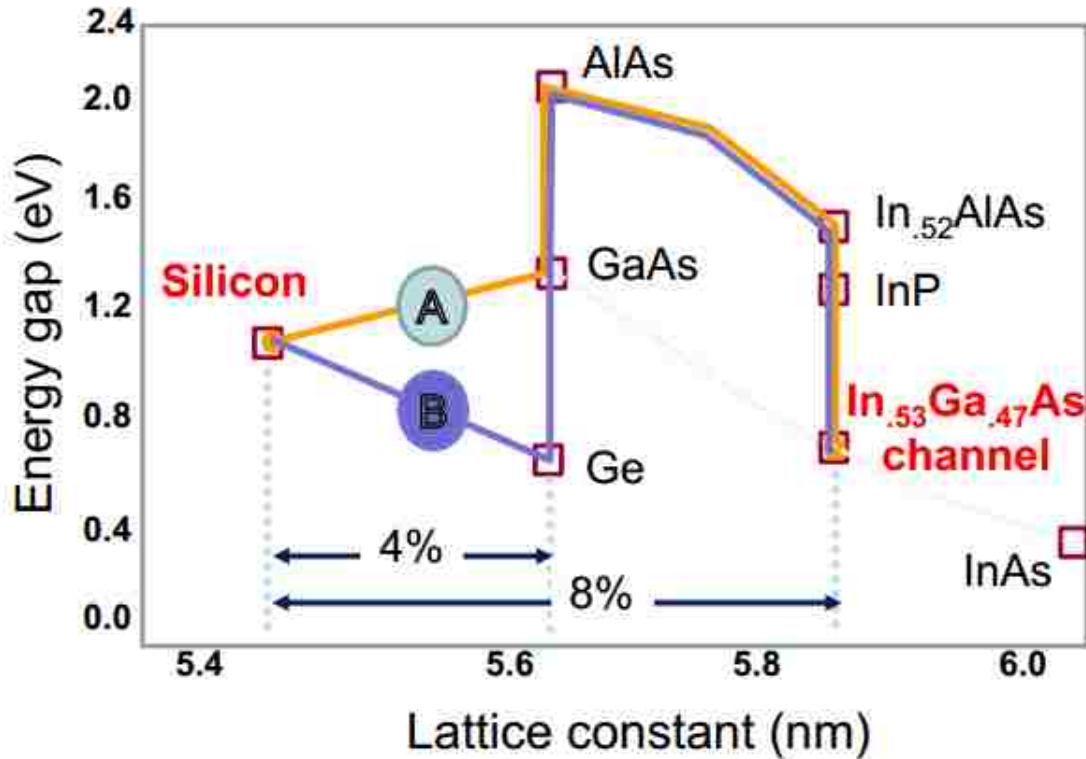
Figure 1.10. Energy gap versus lattice constant for many important semiconductors[39] Especially important is the Ge-GaAs-AlAs system that is widely researched due to the similarity of the lattice constants of the materials.

Lets turn our attention to one of the most studied systems of heteroepitaxy, which is SiGe system, especially epitaxial Ge on Si (GoS) system. This GoS system offers several applications including high-frequency HBT, and strained Si devices. The HBT is widely popular in radio-frequency telecommunications and high-bandwidth instrumentation. The strained Si devices leverage strain during heteroepitaxial process to enhance mobility in CMOS field-effect transistors [40]. Unlike Si, another outstanding property of Ge is that Ge is closely lattice-matched to several III-V group materials such as GaAs and AlAs, as shown in Figure 1.10. In previous sub-sections, we

have talked about how lattice mismatch in turn can be disadvantageous because it leads to the formation of defects in the material that degrade its electronic properties. Herein, I present few applications of Ge-based heteroepitaxial system, and these applications are devised using a platform where Si, Ge, and GaAs are main components.

The first application is near-infrared (NIR) avalanche photo-detectors (APD) [41]. By virtue of the emission wavelength of Ge, this is optimized to an eye-safe spectral region of around 1,500 nm, allowing Ge-based APDs to be safely deployed throughout human environments. Several potential applications including motion sensors, fi re detectors, and light detection and ranging (LIDAR) control systems for automobiles, where Ge-based APDs can be used. In addition, APDs are widely used in high-bit-rate, long-haul fiber communication systems. Ge/Si based APDs offer ~5–10 dB better sensitivity due to their internal multiplication gain 59 compared to photodetectors based on p-i-n junctions. Owing to an excellent optical absorption of Ge around 1500 nm spectral regions combined with the outstanding carrier multiplication properties of Si, the Ge/Si APDs is one of the most efficient class of photodetectors, shown in Fig. 1.11. In The large electric-field gain region of Si enables photocarriers from the Ge absorption layer to undergo a series of impact ionization processes, which in turn amplifies the photocurrent and improves sensitivity of APDs.

The second application is Ge-Si based optoelectronics. Optoelectronics such as semiconductor lasers and detectors can be used for optical interconnects for chip-to-chip communication with a large bandwidth. Having optoelectronics monolithically integrated with Si CMOS can achieve lower cost, lighter weight, and greater speed than having separate chips performing separate functions and

interconnected with Cu wires [42]. Figure 1.12 shows an example LED devices fabricated from GoS substrate. Previous reports have shown that tensile strained n+ Ge is capable of behaving as a direct BG material, owing to its direct gap shrinkage because of tensile strain and filling up *L* valley with extrinsic electrons coming from n-type dopants. The MIT group in past has shown that a net gain can be achieved with 0.25% tensile strained Ge with n-type doping concentrations ranging from 10^{19} to 10^{20} cm^{-3}.
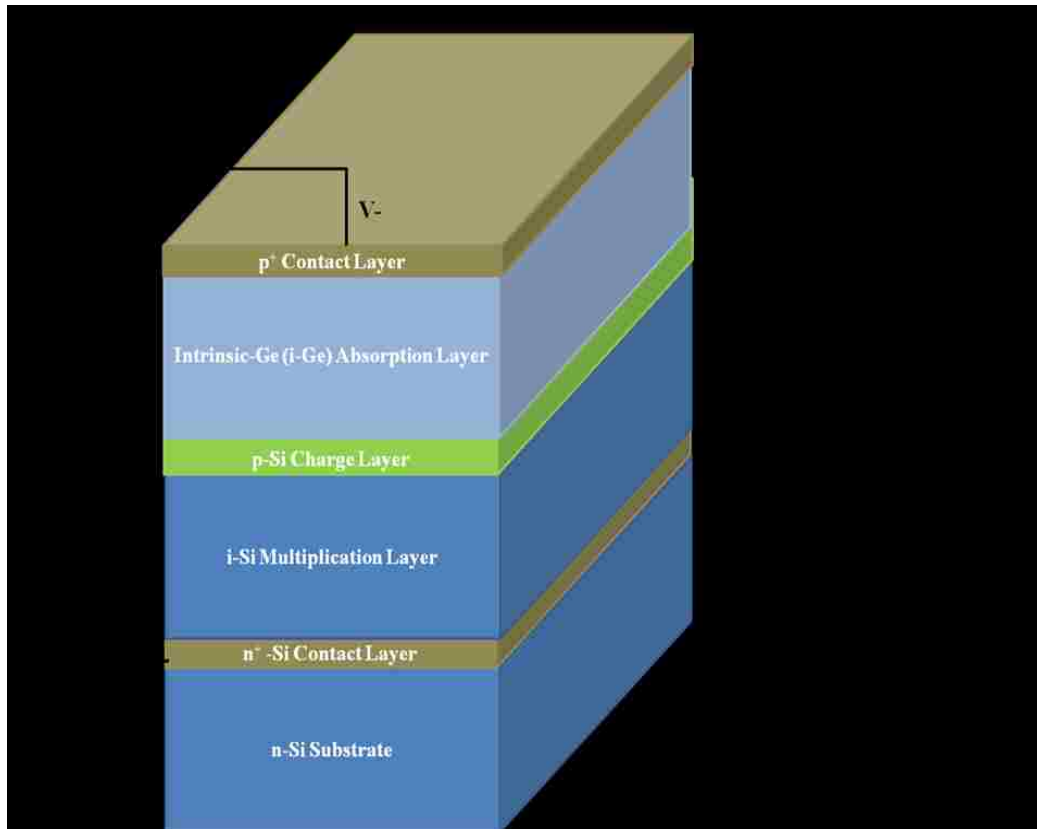
Figure 1.11. Near-infrared avalanche photodetector fabricated from Germanium on Si substrate utilizing a Ge based absorption layer and a Si based carrier multiplication layer.
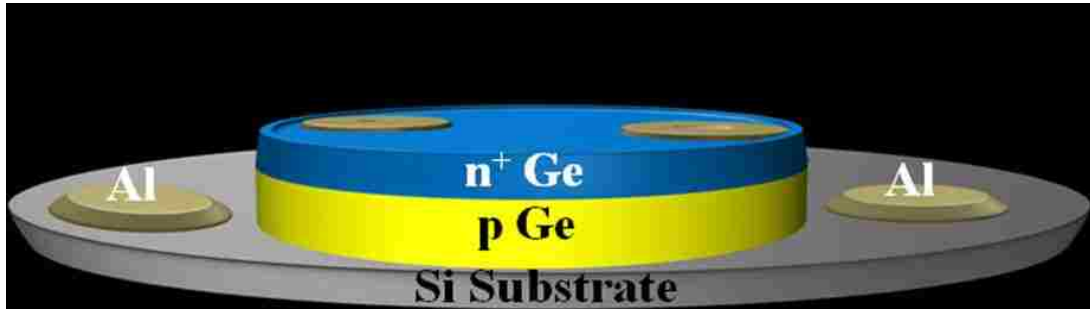
Figure 1.12. Light emitting diode fabricated from Germanium on Si substrate utilizing a Ge based absorption layer and a Si based carrier multiplication layer. In this case Ge based devices can be used as a source.

In order to achieve faster computing speeds[43,44], it is imperative to have shorter gate length transistors. Silicon based CMOS electronics continue to approach scaling limit with shrinking physical gate length of the transistors. To avoid this scaling problem, a solution is to fabricate Ge-based pMOS and GaAs-based nMOS transistors on Si platform[45-48]. As stated previously, Ge has four times larger hole mobilities compared to Si. Likewise, GaAs has an electron mobility of 8500 compared to 1350 cm^2 V^{-1}-s^{-1} for Si. Therefore, future CMOS design will utilize Ge pMOS and GaAs nMOS transistors to achieve much greater switching speeds, as shown in Figure 1.13.
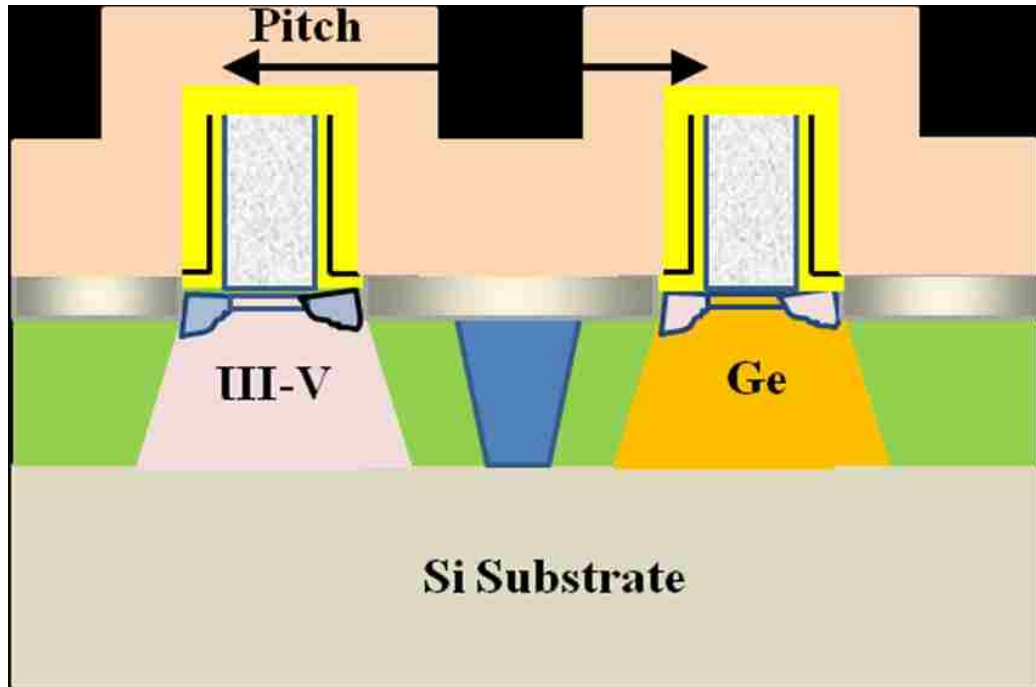
Figure 1.13. High mobility complementary metal-oxide-semiconductor transistors utilizing a Ge based p-metal oxide semiconductor and III-V n-metal oxide semiconductor structure on Si substrate.

Germanium is potential candidate that can be used as a bridge between III-V semiconductors epitaxially growing on Si substrate. In such cases, GoS can serve as a virtual substrate for integrating III-V heteroepitaxial layers onto Si. There are several optoelectronics application that one can think of using III-V layers that are grown onto Si. An example of a III-V based optoelectronics device integrated onto a virtual substrate is multijunction (MJ) solar cells,[49-56],[57-58], shown in Figs. 1.14. A schematic of a triple-junction solar cell is depicted in Figure 1.14. Solar energy is abundant on earth, and MJ solar cells are very efficient in converting this solar energy into useable electricity. The MJ solar cells find use in space applications, but could also be useful for terrestrial applications if their cost per watt can be reduced. Especially in

MJ solar cells, par of the higher cost is because of using Ge substrate. Herein, using Si substrate to grow high quality thin film of Ge can play a significant role in reducing the overall cost of MJ solar cells. Owing to abundance in Si substrate, this GoS 'virtual substrates' could replace the more expensive Ge substrates. Beside cost reduction, using Si, which is mechanically stronger and less brittle than Ge, would provide easiness in processing steps and obtaining higher yield. Also, using virtual substrates would reduce the overall weight of solar cells that are intended to be used for space applications. Another application where Ge interlayer can play a significant role is growing ternanry or quarternary III-V compound semiconductors onto cheap Si substrates. This would enable us to monolithically integrate optoelectronics with Si based CMOS technologies. Figure 1.15 shows a schematic of ternary III-V allows integrated onto Si substarte [59]. This stack consists of an interlayer of Ge between Si substrate and GaAs buffer, which is lattice matched to Ge. We note that the buffer layer of GaAs is used for subsequently growing a thick InGaAs layer.
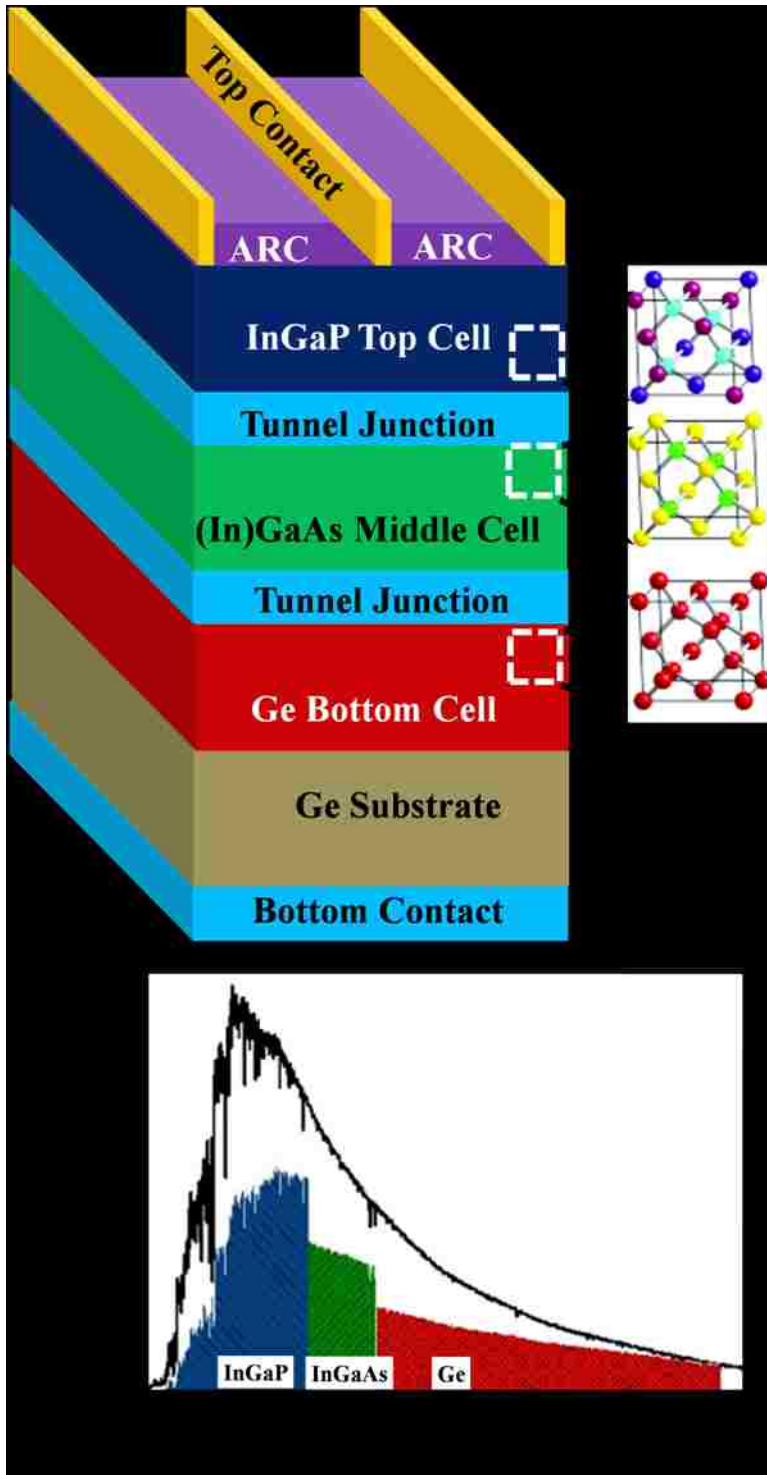
Figure 1.14 Schematic of a triple junction solar cell. The cell consists of a series of layers in order of largest to smallest bandgap from top to bottom. Each layer collects a range of the solar spectrum shown in the inset at the lower right. The III-V layers are closely lattice matched to one another and to the Ge substrate.
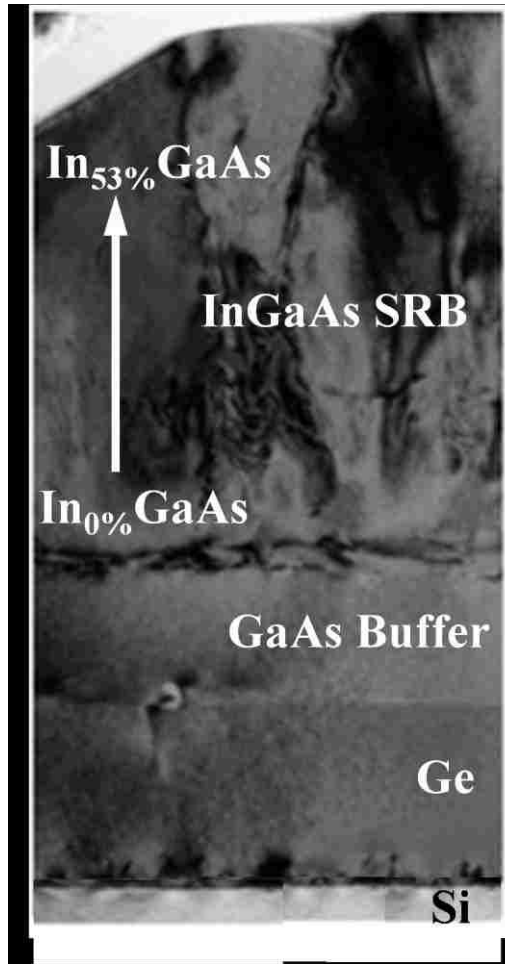
Figure 1.15. Ternary III-V alloys integrated on GoS virtual substrate. The Ge is used as a buffer layer in between GaAs buffer and underlying Si substrate [59].

1.7   Barriers to High-Quality Epitaxial Ge on Si

Heteroepitaxial growth frequently represents a growth where materials of different lattice constants are grown in a stacked order. The epitaxial layer usually has a relaxed lattice constant that is different from that of the substrate. Therefore, the lattice mismatch strain can be defined as

$$f = \frac{a_s - a_e}{a_s} \tag{1-4}$$

where a_s and a_e are the substrate and epitaxial layer lattice constants, respectively. The absolute magnitude of the lattice mismatch may vary from 1 to 10 % depending on the properties of grown materials. Interestingly, mismatch with $f > 0$ represents tensile where as $f < 0$ represents compressive strain. This section is going to deal with various important aspects of mismatched heteroepitaxial growth: the critical layer thickness, lattice relaxation and the introduction of dislocation defects and the dynamics of dislocation reactions.

In the case of heteroepitaxial growth of Ge layer on Si substrate, the mismatch strain is almost 4.2%, and compressive in nature. GoS system also shows a 116% thermal mismatch because of the different thermal expansion coefficients of Ge and Si. The lattice mismatch results in threading dislocations (TD) with a density on the order of 10^9-10^{10} cm^{-2}, while the thermal strain can lead to microcracks in Ge films as the sample cools from a growth temperature of 853 K to room temperature. The TDs directly influence the electronic properties of epitaxial layer. For instance, to achieve a minority carrier lifetime in III-V films on GoS that is comparable to that of lattice-matched III-V growth on Ge and GaAs substrates [60,61], it is extremely important to have a that the threading dislocation densities (TDD) in the Ge films must be less than 10^6 cm^{-2}.

Now lets turn our attention to various aspects of mismatched growth and dislocation dynamics. If there is a lattice mismatch between the epitaxial layer and substrate such as 4.2% in case of Ge and Si, the initial growth will be coherently strained to match the atomic spacings of the Si substrate in the plane of the Ge/Si interface. Figure 1.16 depicts this situation, where the epitaxial layer of Ge has a larger lattice constant than the Si substrate ($a_e > a_s$ and $f < 0$). We assume that the

substrate is sufficiently thick enough so that it remains unstrained by the growth of the epitaxial layer. We also assume that the unstrained substrate crystal is cubic with a lattice constant a_s. The pseudo-morphic initial layer of Ge matches the Si lattice constant in the plane of the interface ($a = a_s$), and therefore experiences in-plane biaxial compression. Considering the definition of mismatch, the lattice relaxation only occurs at in-plane, and given by,

$$\varepsilon_P = f - \partial \qquad (1\text{-}5)$$

where ∂ is the lattice relaxation. In comparison, the pseudomorphic layer shows no lattice relaxation. Therefore, the out-of-plane strain ($\varepsilon_\perp$), which is also perpendicular to interface, is given by,

$$\varepsilon_\perp = \frac{2C_{12}}{C_{11}} \varepsilon_\parallel \qquad (1\text{-}6)$$

where C_{12} and C_{11} are elastic constants of Ge.
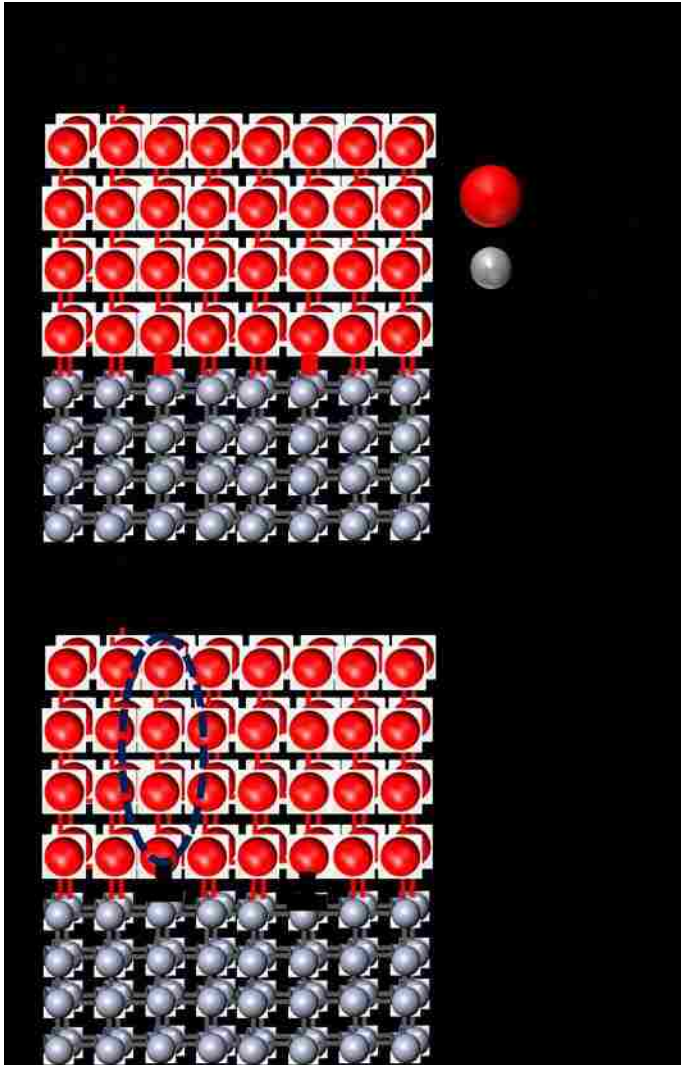
Figure 1.16. Image (a) shows the pseudomorphic growth of Ge on Si. Image 1.16(b) shows the nucleation of a misfit dislocation to relieve the stress at larger Ge thickness.

The strain energy in the epitaxial layer increases with increasing thickness of Ge. Beyond certain thickness of epitaxial layer, the strain energy becomes uncontrollably larger, and it becomes energetically favorable to introduce of misfit dislocations to relax some of the strain. The thickness at which this misfit dislocations form is called the critical layer thickness. There are various ways one can interpret

critical layer thickness. For instance, the Matthews and Blakeslee model [62] and Matthews energy calculation model are used often to calculate the critical layer thickness. Based on the consideration of energy, the strain in the epitaxial layer equals to the mismatch strain at the critical thickness. Matthews in critical thickness calculation starts with calculating aerial strain energy in pseudomorphic layer with an in-plane-strain of $\varepsilon_{\parallel}$. The aerial strain energy (E_e) is given by,

$$E_e = 2G\frac{(1+v)}{(1-v)}h\varepsilon_{\parallel}^2 \tag{1-7}$$

where G is the shear modulus and v is the Poisson ratio. Figure 1.16 (b) shows an example of growth for Ge on Si. The aerial energy associated with a square array of misfit dislocations with average separation S is

$$E_d = \frac{1}{S}\frac{Gb^2(1-v\cos^2\alpha)[\ln(R/b)+1]}{2\pi(1-v)} \tag{1-5}$$

where α is the angle between the Burgers vector and the line vector for the dislocations, b is the length of the Burgers vector, and R is the cutoff radius for the determination of the dislocation line energy. The cut-off radius is considered as $R=min\ (S,\ h)$. Matthews assumed R is equal to the film thickness, h. Also, the average spacing between dislocations can be written as,

$$S = \frac{b\cos\alpha\cos\phi}{f\text{-}\varepsilon_{\parallel}} \tag{1-7}$$

where ϕ is the angle between the interface and the normal to the slip plane. The total energy of the system is equal to $E_e + E_d$. The minimum total energy at equilibrium can be found from the condition,

$$\frac{\partial(E_e + E_d)}{\partial \varepsilon_{//}} = 0 \tag{1-8}$$

Solving the eqn. (1-7) gives the in-plane strain at minimum energy, or the equilibrium strain

$$\varepsilon_{\|}(eq) = \frac{f}{|f|} \frac{b(1 - v\cos^2 \alpha)[\ln(h/b) + 1]}{8\pi h(1 + v)\cos \lambda} \tag{1-9}$$

Now, to determine the critical layer thickness for the onset of dislocation nucleation, Matthews used this condition where the thickness for which $\varepsilon_{//}(eq) = f$. Solving,

$$h_c = \frac{b(1 - v\cos^2 \alpha)[\ln(h_c/b) + 1]}{8\pi|f|(1 + v)\cos \lambda} \tag{1-10}$$

Beside Matthews, van der Merwe [63] also developed an alternative expression for the critical layer thickness by equating the strain energy in a pseudomorphic film to the interfacial energy of a network of misfit dislocations. The critical layer thickness that van der Merwe found, can be expressed as,

$$h_c = \left(\frac{1}{8\pi^2}\right)\left(\frac{1 - v}{1 + v}\right)\frac{a_s}{|f|} \tag{1-11}$$

where a_s is the lattice constant of the substrate. Both Matthew's and van der Merwe's models predict a critical thickness value of about 3 nm for GoS. However, often experimentally observed values of critical thickness for GoS differ by ten times from predicted thickness of 3nm.

Other than Matthews, van der Merwe, People and Bean[64] also derived an alternative expression for the critical thickness of GoS. It turns out that the critical thickness that is calculated based on People and Bean [64] is in much better agreement with their experimentally observed values. People and Bean considered that strain energy in

the pseudomorphic layer is equal to the energy of a dense network of misfit dislocations

at the interface with a spacing of

$$S = 2\sqrt{2}a_s \qquad (1\text{-}12)$$

The calculated areal energy density of this misfit dislocation array is given by,

$$E_d \approx \frac{Gb^2}{8\pi\sqrt{2}a_s} \qquad (1\text{-}13)$$

Now, setting Equations (1-6) and (1-13) equal to each other and solving for the thickness,

they estimated the critical thickness to be

$$h_c = \left(\frac{1+v}{1-v}\right)\left(\frac{1}{16\pi\sqrt{2}}\right)\left(\frac{b^2}{a_f}\right)\left[\left(\frac{1}{f^2}\right)\ln\left(\frac{h_c}{b}\right)\right] \qquad (1\text{-}14)$$

People and Bean used this expression to calculate the critical layer thickness for GoS

with the lattice mismatch strain of $f = -0.04x$, where x being the molar fraction in the Si$_{1-x}$Ge material system. The People and Bean value for critical thickness is very close to

experimentally observed value for critical thickness. We notice that the critical thickness

for GoS is only a few nanometers. Considering this small length of critical layer

thickness, it is likely that threading dislocations form in the Ge layer that has a thickness

in the range of micrometers.

Another type of defects that primarily can be seen while growing

III-V s on Ge layer is known as anti phase boundary (APB) domains. Figure 1.17 shows

a schematic of APB defects.   This starts with the formation of Ga-Ga(group-III) or As-

As (group-V) bonds along the APB.   There are two distinct possibilities of forming

APBs. First, APBs form if an incomplete initial monolayer of either Ga or As forms on

the surface of the monovalent material such as Si or Ge. In almost all cases, the GaAs

growth starts with an As overpressure to create a monolayer of As on the monovalent semiconductor surface. Owing to the larger vapor pressure of As than that of Ga, the excess As readily desorbs from an As monolayer. In comparison, Ga can aggregate on the surface and form droplets. Second, APBs form at single height atomic steps of monovalent material if either Ga or As atoms try to settle over this atomic step. The single step atomic heights normally exist on single crystalline monovalent substrates due to a small unintentional angle of miscut relative to the crystal orientation. It is known that using a substrate intentionally offcut by greater than 4 degrees toward a [110] direction can suppress APBs. Figure1.18 shows that how large offcut angle favors the reconstruction of the surface into atomic steps of double height [65], which eventually helps to suppress APBs. To summarize, we note that there are several material related issues one need to consider carefully, namely lattice and thermal mismatch, and APBs, while growing epitaxial layer of Ge on Si substrate. To achieve a high-quality film of Ge, sufficient engineering techniques must be employed to overcome these technical challenges.
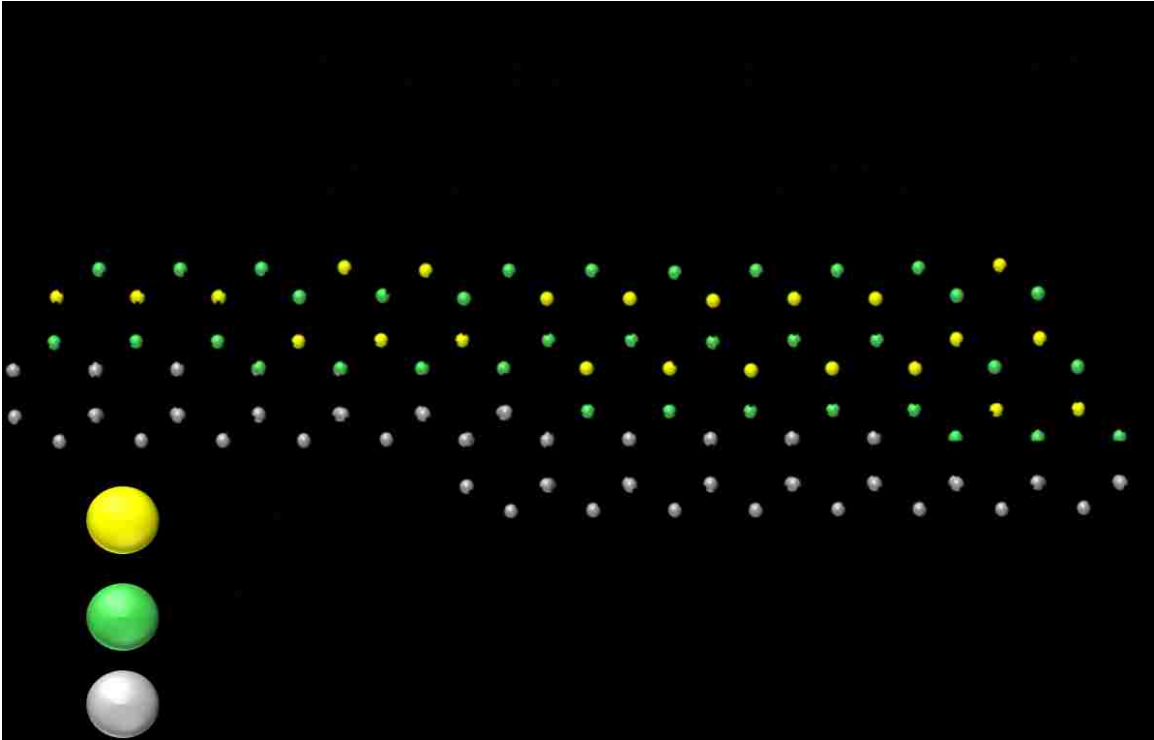
Figure 1.17. Antiphase domain boundary that occurs from the epitaxial growth of a III-V semiconductor on group-IV materials such as Ge or Si in the presence of single height atomic steps.
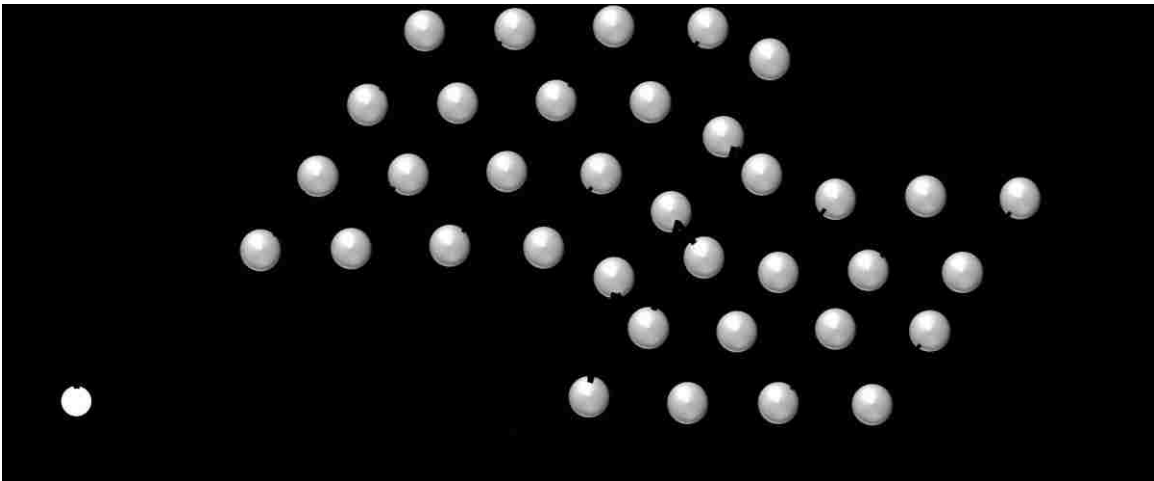
Figure 1.18. Rendition of the double height step reconstruction that occurs on substrates offcut by several degrees toward the [110] direction. The morphology suppresses the formation of anti-site defects occurring in zinc-blende epitaxy on diamond cubic materials.

1.8   Previous Approaches to Reduce Threading Dislocations in Heteroepitaxy

1.8.1 Growth of High Quality Relaxed Ge Layers Using Compositional Grading

Since the 70's, compositional grading has been used to grow high quality layer of III-V semiconductor compounds [66]. Later, similar approach has been practiced for growing GoS, where graded $Si_{1-x}Ge_x$ is used between the the Si substrate and the final epitaxial layer of Ge. A careful choice in molar fraction in $Si_{1-x}Ge_x$ is need to achieve high-quality Ge layer. Otherwise, graded SiGe layer with a large Ge content produces high crosshatch surface roughening in the graded layer along with a large TDD [67]. A chemical mechanical polishing (CMP) step is used to further reduce the TDD in the final Ge layer. Using this technique, the graded $Si_{1-x}Ge_x$ layer is grown up to Ge content with x=0.5 before removing 500 nm using CMP. This technique does produce Ge film that is suitable for device fabrication [68], however, the CMP step adds up complexity to the whole process.

1.8.2 Two Step CVD Growth With Low Temperature Buffer Layer

Colace et al [69] proposed an idea of growing moderate quality Ge layers using a two-step chemical vapor deposition (CVD) method. Using this method, a thin, low-temperature buffer of Ge layer is grown followed by a thick, high temperature layer of Ge grown on top. Since the initial Ge layer is grown at low-temperature, and the hydrogen gas that being used in CVD process acted as a surfactant, the first layer can be grown beyond the critical thickness for the Stranski Krastanov (SK) growth mode. The final layer that is grown at high-temperature showed a significantly less dislocation density [70]. The low-temperature buffer layer has two-fold advantages: first, the final Ge

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film consists of small number of dislocations; second, the Ge layer shows a tremendously low surface roughness. Later, multiple annealing steps are added in this two-step growth process to further reduce the TDD [70].

1.8.3 Multiple Hydrogen Annealing for Heteroepitaxy

Stanford group demonstrated an alternative technique of growing high-quality Ge layer on Si (100) substrate using a CVD process known as Multiple Hydrogen Annealing for Heteroepitaxy (MHAH) [71-73]. Figure 1.19 shows a Ge film that is grown using MHAH process shows consists of very few threading dislocations reaching to the surface. The process steps are following: the growth starts with a hydrogen bake followed by 200nm layer of Ge grown using GeH_4 at 400ºC for 15 mins. A thermal annealing for 60 mins at 825ºC is introduced before further growth. After annealing, a second 200nm layer of Ge is grown using GeH_4 at 400ºC for 15 mins.
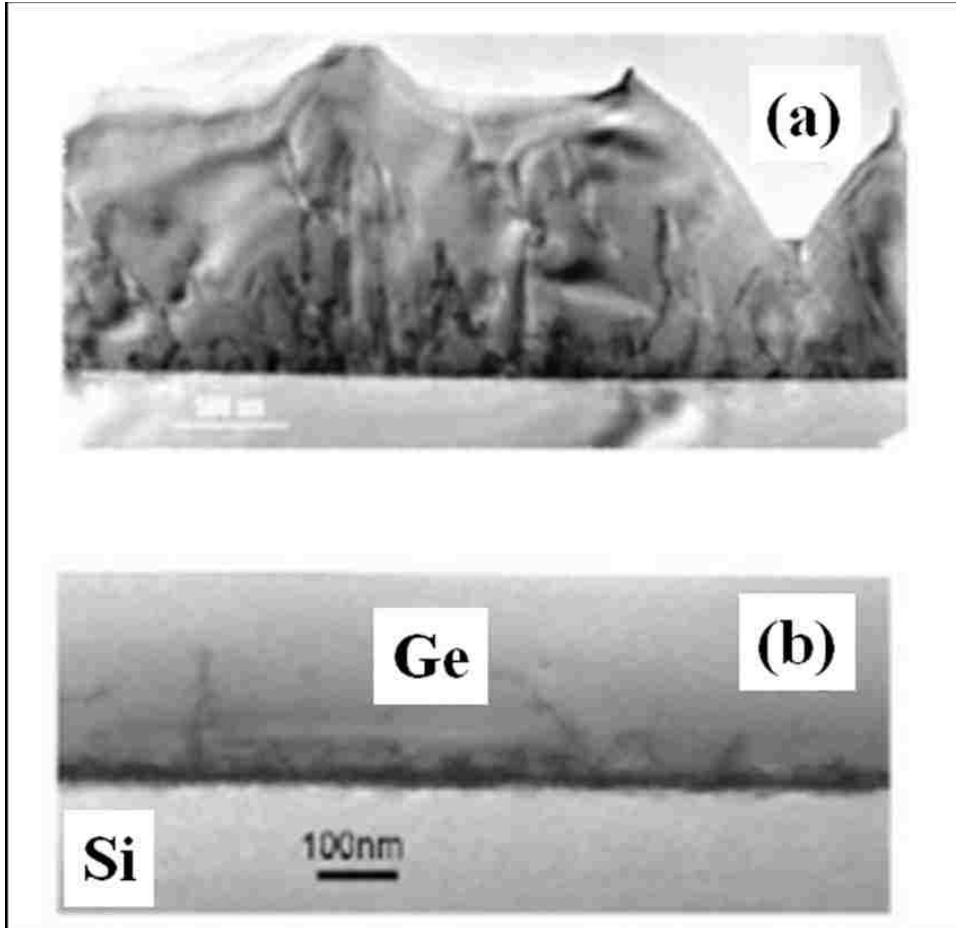
Figure 1.19: (a) Cross-sectional TEM image of unannealed GoS layer. Misfit dislocations can b visible in the TEM image. (b) Cross-sectional TEM image of GoS layer grown using MHAH method. Dislocations are mostly confined at the Ge/Si interface [71-73].

Another annealing for 60 mins at 825°C is performed after the second layer of Ge is grown. The characterization on Ge film reveals low TDD. The usefulness of the Ge film is further tested by fabricating electrical devices such as GoS MOSFET's [72] and photodetectors [74].

1.8.4 Heteroepitaxy using Super Lattice Structures (SLS)

An alternative technique of producing a low-TDD film in heteroepitaxy is the use of a SLS [75-77]. This technique makes use of overlapping of strain fields that are associated with a pseudomorphically grown SLS and strain fields

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associated with TDs. The strain fields either show positive or negative signs. Based on signs, the SLS may either attract or repel dislocation. For example, a compressive strain field generating from the SLS repels a compressive strain field associated with a TD. In contrast, a tensile strain field generating from the SLS attracts a TD associated with a compressive strain field. Figure 1.20 shows an example of a threading dislocation being bent due to the interaction with a strained $Al_{0.3}Ga_{0.7}As$ layer on a GaAs film. Although SLS shows promises, however, SLSs are not successful in greatly reducing the TDD in heteroepitaxy by more than a factor of two or three.
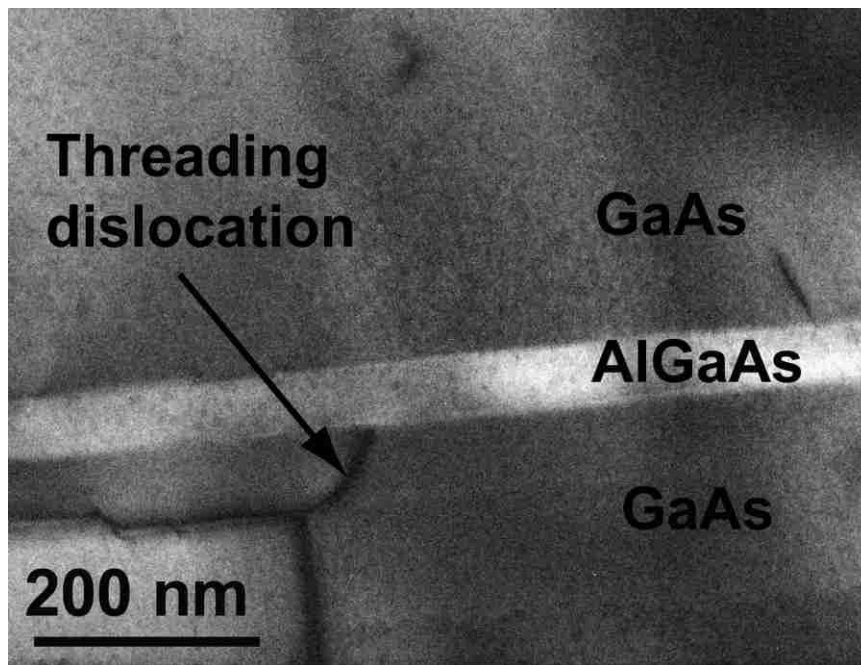
Figure 1.20: The principal of strained layer defect filtering is illustrated in the transmission electron microscope image of an $Al_{0.3}Ga_{0.7}As$-GaAs structure. The stress field of the $Al_{0.3}Ga_{0.7}As$ layer repels the stress field associated with the threading dislocation and bends it into the (001) growth plane.

1.8.5 Heteroepitaxy using Aspect Ratio Trapping (ART) Method

An alternative method of producing a high-quality GoS film is aspect ratio trapping (ART) method [78-81]. This particular method makes use of finite

growth areas that are created on the substrate using a combination of lithography and etching techniques to create high-aspect-ratio walls of dielectric material such as SiO_2. After the creation of wall, the substrate is subjected to impingement of Ge atoms. Heteroepitaxial growth then selectively takes place in between these high-aspect-ratio walls. The limited growth area within the openings allows TDs to glide short distances before being terminated by the high-aspect-ratio walls of the SiO_2. A cross-sectional TEM view of aspect ratio trapping within trenches is shown in Figure 1.21.
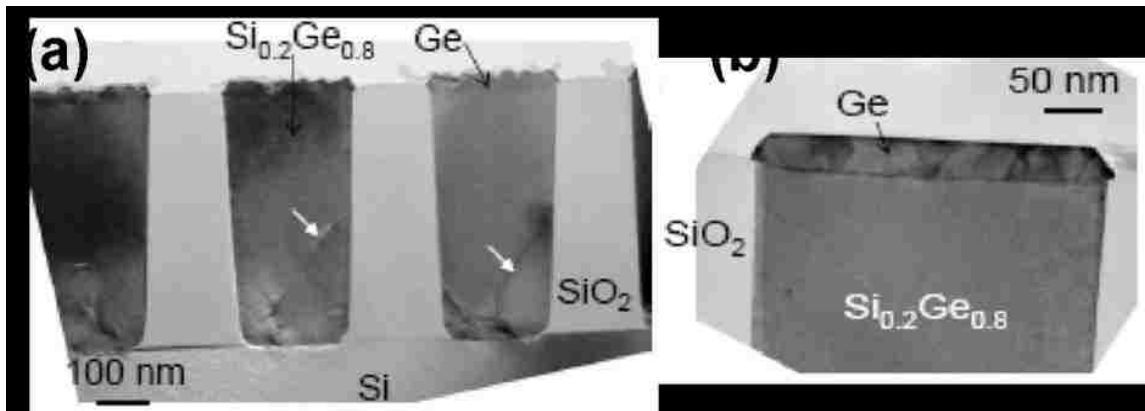
Figure 1.21: Heteroepitaxial growth selectively takes place within the patterned trenches and traps threading dislocations between the SiO_2 walls leading to high-quality material near the tops of the trenches. Coalescence of adjacent trenches, however, can lead to the nucleation of additional defects. In addition, the mask material itself may induce defects as the epitaxial film grows laterally over the mask regions[78-81].

The event termed as coalescence occurs if the growth continues above the pattern features. In the case for coalescence the growth fronts from adjacent openings merge together. This process leads to a continuous film that can be used device fabrication, owing to the coalescence of adjacent trenches. However, the event of coalescence has negative impact on growth. Literatures show that the regions where the coalescence occurs possess a large TDD [81-83]. Aspect ratio trapping promises to be a method of

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producing high-quality GoS, although it has drawback of producing only finite regions of device quality material. In contrast to previously mentioned approaches, in an effort to reduce TDDs over a large-area, we use nanoheteroepitaxy technique as an alternative approach to achieving low TDD [84-89].

1.9 Selective Growth using Nanoheteroepitaxy

Several literatures show that Ge can be grown epitaxially on Si substrate that has been patterned with oxide. Theoretical analysis claims that Ge grown selectively on Si undergoes elastic relaxation, which gives rise to low TDDs. Unfortunately, experimental results do not corroborate to theoretical results and most cases a very high TDDs being recorded [90-93]. These sets of experiments do reveal an interesting fact, which tells that the window size used for Ge growth can be carefully engineered to achieve low TDD [90-93]. It has been found that the Ge film quality improves with reducing window size. The distance misfit dislocations have to travel to reach to the edge of the window decreases with reducing window size. Hence, the probability of misfits to interact and multiply decreases significantly with reducing window size. For example, fig. 1.22 shows an example of Ge growth taking place on Si within windows in SiO_2 that are only a few nanometers in diameter. We notice that Ge forms a mushroom shape over the SiO_2 layer. Ge relaxes their strain by deforming outward over the SiO_2 layer [90-93].

A theory of lattice mismatch strain in nanoheteroepitaxy was first reported by Luryi and Suhir [94]. Their research showed that the critical thickness of Ge that is grown in lattice-mismatched condition depends on the island diameter. Luryi and

Suhir [94] starts the analysis by calculating the in-plane stress in the epitaxial deposit using this expression, which is given by,

$$\sigma_{\parallel} = f \frac{E}{1-v} \chi(y,z) \exp(-2\pi/2l) \qquad (1\text{-}15)$$

where E is Young's modulus, the z-axis is perpendicular to the substrate, and the y-axis lies in the plane of the interface, along the center of the seed pad, and

$$\chi(y,z) = \begin{cases} 1 - \dfrac{\cosh(ky)}{\cosh(kl)} & z \le h_e \\ 1 & z \ge h_e \end{cases} \qquad (1\text{-}16)$$
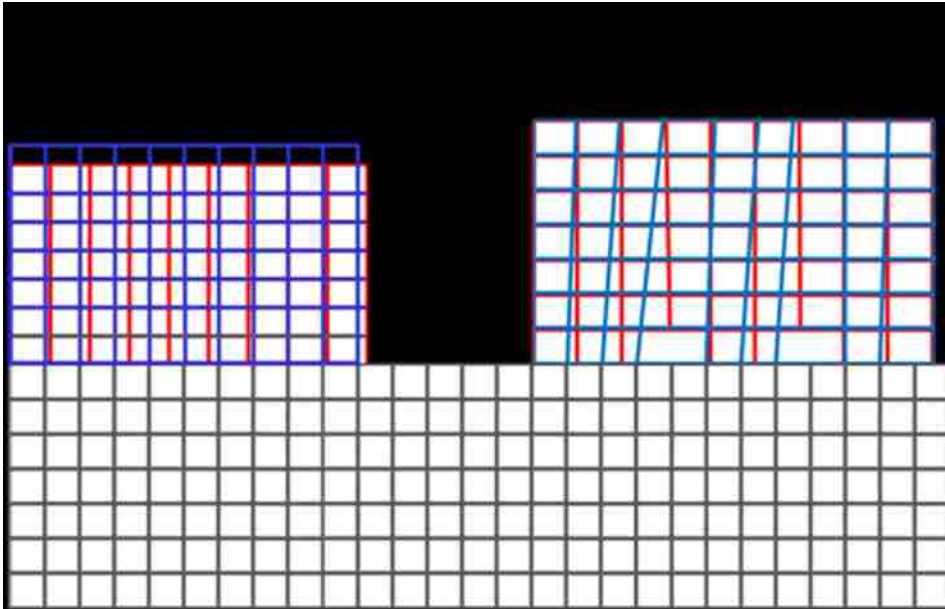
Figure 1.22: Finite element model showing the deformation of lattice planes occurring in the tensile strained heteroepitaxial island and within the compressively stained substrate.

where h_e is the effective range for the stress in the z-direction, to be determined below, and the interfacial compliance parameter k is given by

$$k = \left[\frac{3}{2} \left(\frac{1-\nu}{1+\nu} \right) \right]^{1/2} \frac{1}{h_e} \equiv \frac{\zeta}{h_e} \qquad (1\text{-}17)$$

The strain energy density per unit volume is

$$\omega(y, z) = \frac{1-\nu}{E} \sigma_\parallel^2 \qquad (1\text{-}18)$$

and is maximum at $y = 0$. The strain energy per unit area is found by integrating over the thickness of the epitaxial deposit and is maximum at $y = 0$, which is

$$E_s = \int_0^h \omega(0, z) = \frac{E}{1-\nu} f^2 h_e^2 \qquad (1\text{-}19)$$

The right-hand side of Equation (1-19) defines the characteristic thickness h_e, which is then given implicitly by

$$h_e = h \left\{ \left[1 - \sec h \left(\frac{\zeta l}{h_e} \right) \right]^2 \left[1 - \exp(-\pi h / l) \frac{l}{\pi h} \right] \right\} = h \left[\phi \left(\frac{l}{h} \right) \right]^2 \qquad (1\text{-}20)$$

The right-hand side of this equation defines the reduction factor $\phi(l/h)$. For $l \gg h$, $h_e \approx h$, and for $l \ll h$,

$$h_e \approx \frac{1}{h} \left[1 - \sec h(\zeta \pi) \right]^2 \qquad (1\text{-}21)$$

The strain energy per unit area from Equation (1-18) is used in conjunction with an energy calculation for the critical thickness to find the critical layer thickness for an island of radius l. The result is

$$h_c^{\ l} = h_c[\phi(l/h_c^{\ l})f]$$
(1-22)

where Matthew's calculation for the critical thickness, Equation (1-8), is inserted into Equation 1-21 to yield

$$h_c^{\ l} = \frac{b(1-\nu\cos^2\alpha)[\ln(h_c^{\ l}/b)+1]}{8\pi\left|\phi(l/h_c^{\ l})f\right|(1+\nu)\cos\lambda}$$
(1-23)

The critical thickness is shown in Figure 1-13 as a function of lattice mismatch, with the island diameter $2l$ as a parameter. Matthew's calculation for the critical thickness, which assumed a planar film, corresponds to $2l \to \infty$.
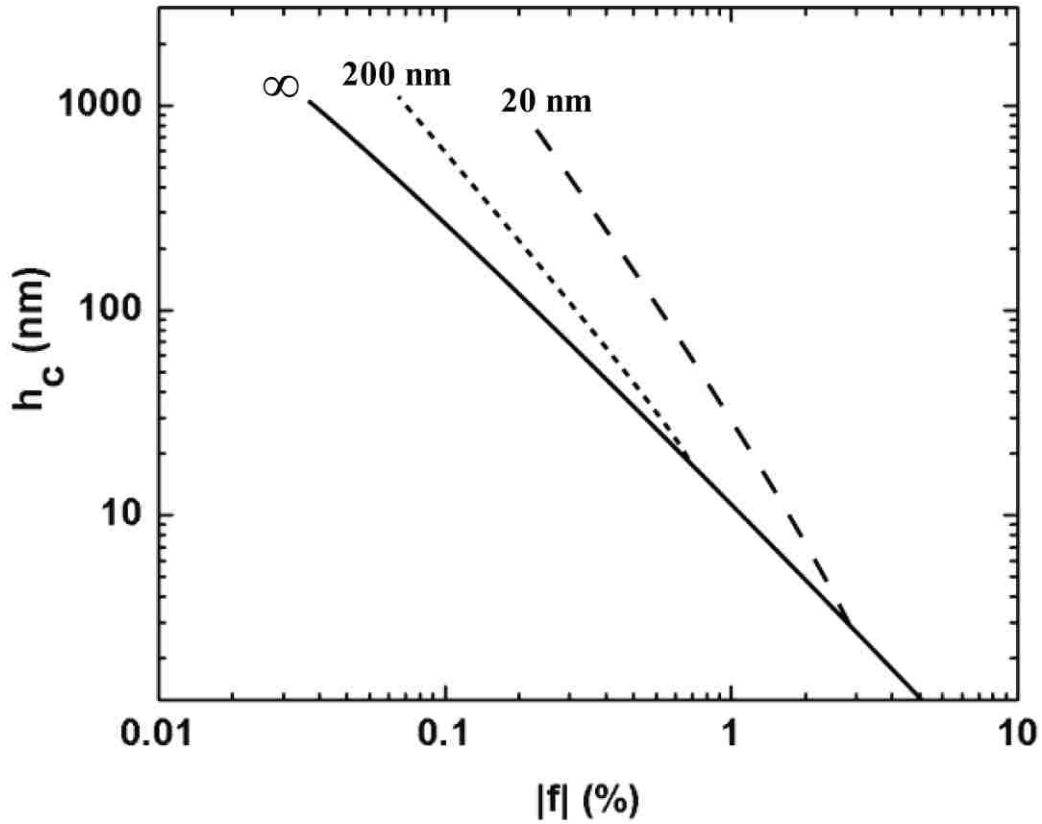
Figure 1.23: Critical thickness versus lattice mismatch based on Matthew's total energy calculation [42] The solid line is Matthew's result for a planar film in contact with the substrate. The dotted and dashed lines represent an island of 200 and 20 nm, respectively, in contact with the substrate based on Luryi and Suhir's model [95]

For nanometer-scale islands, the critical thickness can be increased significantly.

Additionally, for a given mismatch, there is a critical island diameter for which the

critical thickness diverges to infinity. For GoS, this island diameter is approximately 10

nm, and is shown in Figure 1-14.

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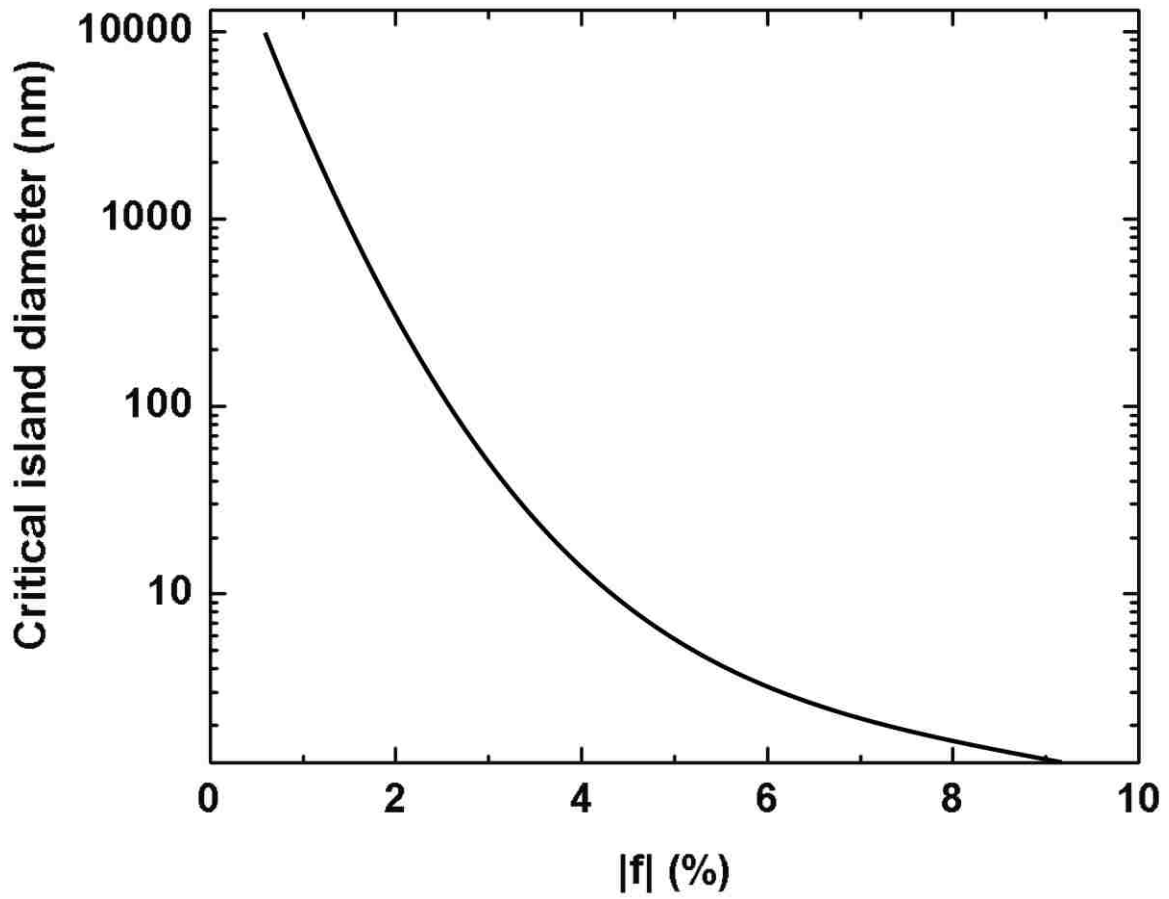
Figure 1.24: Critical island diameter versus lattice mismatch.[19] Island diameters below the solid line have infinite critical thickness for a given mismatch and will relax without the formation of dislocations [95]

CHAPTER 2 Epitaxial Growth and Molecular Beam Epitaxy

2.1 Epitaxial Growth

2.1 Theory of Crystal Growth

An epitaxy is the term that often synonymous to layer-by-layer deposition of material. The purpose of epitaxy is to extend the crystalline substrate in a planar manner. The molecular exchanges between a source and the substrate surface are the driving force behind the deposition process. When mobile atoms/molecules from a source vapor are deposited on the substrate surface, they are termed as adatoms. These adatoms freely move on the surface until they are captured into the crystal structure of the substrate. Epitaxial growth starts owing to the planar incorporation of adatoms on the surface of the substrate. However, the mobility or movement of adatoms on the surface of substrate is always associated to its migration distance, λ, which is an average distance an adatom travels before being fully captured by the crystal structure of the substrate. This migration distance is dependent on various parameters of growth. The two most important parameters are the chemical species of the source vapor and the temperature of the substrate. For example, the migration distance of Ge is greater than that of Si due to the difference in chemical bond strength that exists between Ge and Si. The migration distance also depends on the energy barriers between the adjacent surface capture sites. For instance, often temperature of substrate is raised during growth. Because the kinetic energy of the adatom increase with raised substrate temperature making it easier for adatoms to overcome these energy barriers and increase the migration distance as well.

Another parameter that influences the growth morphology is the crystallographic orientation of the substrate. The migration distance is shorter in closer packed crystal planes due to its lower energy barrier than that of wider packed crystal. If we consider common crystallographic planes, and associated migration distances, then the migration distance increases in the order (100)<(110)<(111) planes [96].
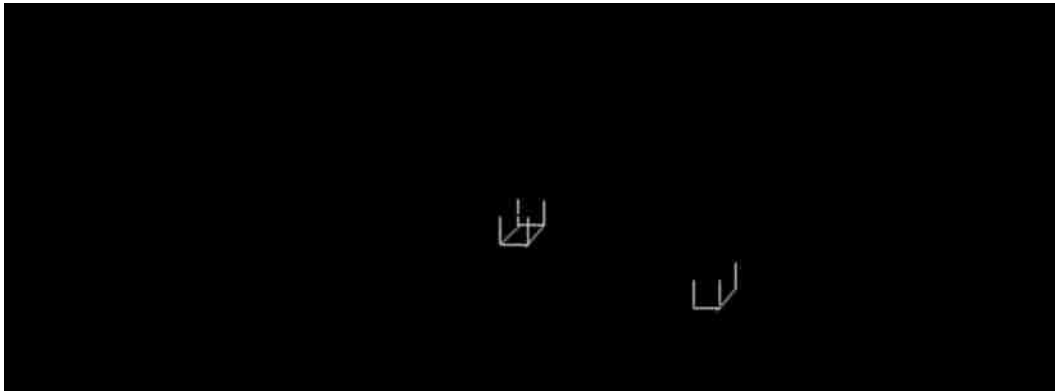
Figure 2.1: The Terrace-Ledge-Kink model of a crystalline surface. This schematic illustrates few important features and bonding sites for adatoms [96].

The Si substrates are vicinal in nature, which means that the surface is not completely flat but consists of many terraces separated by atomic steps as shown in fig. 2.1. These terraces often adjoin to each other to form layer-by-layer growth if the adatom migration distance is greater than the width of terrace [97]. A temporary rebonding of two surface dangling bonds often constructs a dimer. Figure 2.1 shows a single step having an upper terrace with dimerisation parallel to its edge is referred to as, S_A, with the terrace above it labeled as T_A. A single step with upper terrace of dimerisation perpendicular to its edge is referred to as, S_B, and terrace as T_B. Lets assume a situation where the potential well associated with the surface step is deeper than a surface site away from a step. For this specific case, when the adatom loses its kinetic energy then it incorporates into the

surface step and is named a ledge atom shown in fig. 2.1. In summary, the sites for adatom incorporation are (from most preferential to least) given as: bulk vacancy, surface vacancy, ledge vacancy, kink vacancy and step vacancy.

2.2   Form Islanding to Surface Roughness

2.2.1   Three Growth Modes

In this section, we will try to understand the underlying physics of the process that governs nucleation and growth. Before we jump to the discussion of Ge growth on Si substrate it is important to understand the physics of nucleation. We start the discussion by choosing a classic problem, where a droplet of radius r is in contact with vapor. Figure 2.2 shows a rendition of this situation [98]. We can consider the droplet and surrounding vapor molecules as a system. The system can be defined by solving for its change in free energy, which described by,

$$\Delta G = \frac{4}{3}\pi r^3 \Delta G_V + 4\pi r^2 \gamma \qquad (2\text{-}1)$$

where ΔG_v is the change in free energy per unit volume and γ is the free energy change per unit surface [19]. Now ΔG_v can be defined as,

$$\Delta G_V = \frac{kT}{\Omega}ln(\frac{P_V}{P_S}) = \frac{kT}{\Omega}ln(1+S)$$

$$where \qquad (2\text{-}2)$$

$$S = \frac{(P_V - P_S)}{P_S}$$

where k= Boltzmann constant, T= temperature in kelvin, P_V= actual pressure in gas phase, P_S= saturated vapor pressure at equilibrium, Ω= atomic volume (volume per atom), and S= supersaturation. There are three possibilities, if, $P > P_S$, then the system is supersaturated or if $P = P_S$, then the system is at equilibrium, or $P < P_S$, then the system is
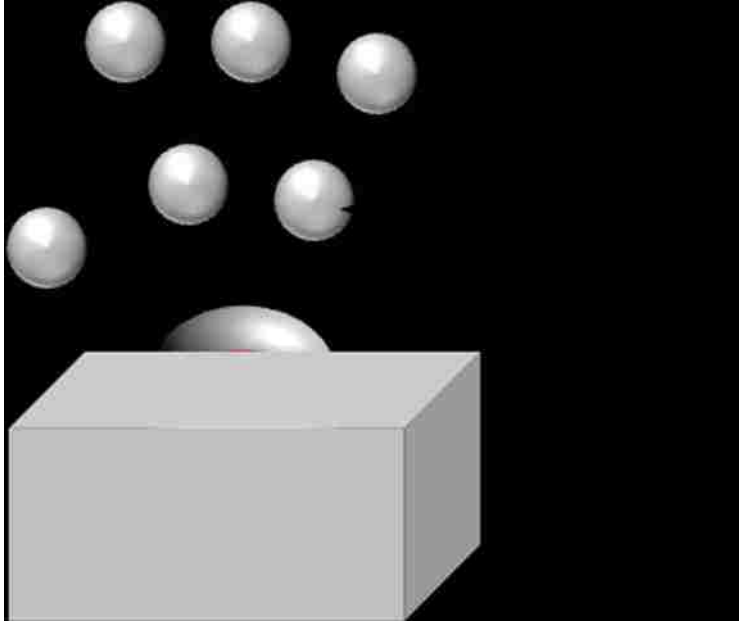
Figure 2.2: Schematic of a system where vapor molecules are in contact with a droplet.

undersaturated. The change in free energy, ΔG, has two components, surface energy, and volume energy, respectively. The presence of surface energy always creates an activation barrier to nucleation of condensed phases. Figure 2.3 shows a plot of activation energy, E, as a function of nucleation size. Figure 2.3 also shows that for small r, the surface energy term dominates, and once the critical nucleus is formed then the volume energy term starts to dominate. The E^* represents the activation barrier to nucleation. The three different growth modes are the result of this activation barrier. These three growth modes are, island growth mode or Volmer-Weber growth (VW), layer growth mode or Frank Van der Merwe (FVM), and Stanski-Krastanov (SK) growth (a combination of layer and island growth) [98]. Herein, we provide a brief description of the island growth, and the layer growth mode. SK growth will be described in greater details in context of Ge/Si system. The change in free energy, ΔG, during nucleation of heterogeneous systems (B nucleation on A) can be described by this following equation,

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$$\Delta G = \gamma_{BV} - \gamma_{AV} - \gamma_{AB} \qquad (2\text{-}3)$$

where, γ_{AV}, γ_{BV}, and γ_{AB} represent the change in surface energy between substrate (A) and total volume (V), the change in surface energy between growth material (B) and total volume(V), and the change in free energy between growth material (B) and substrate (A), respectively.
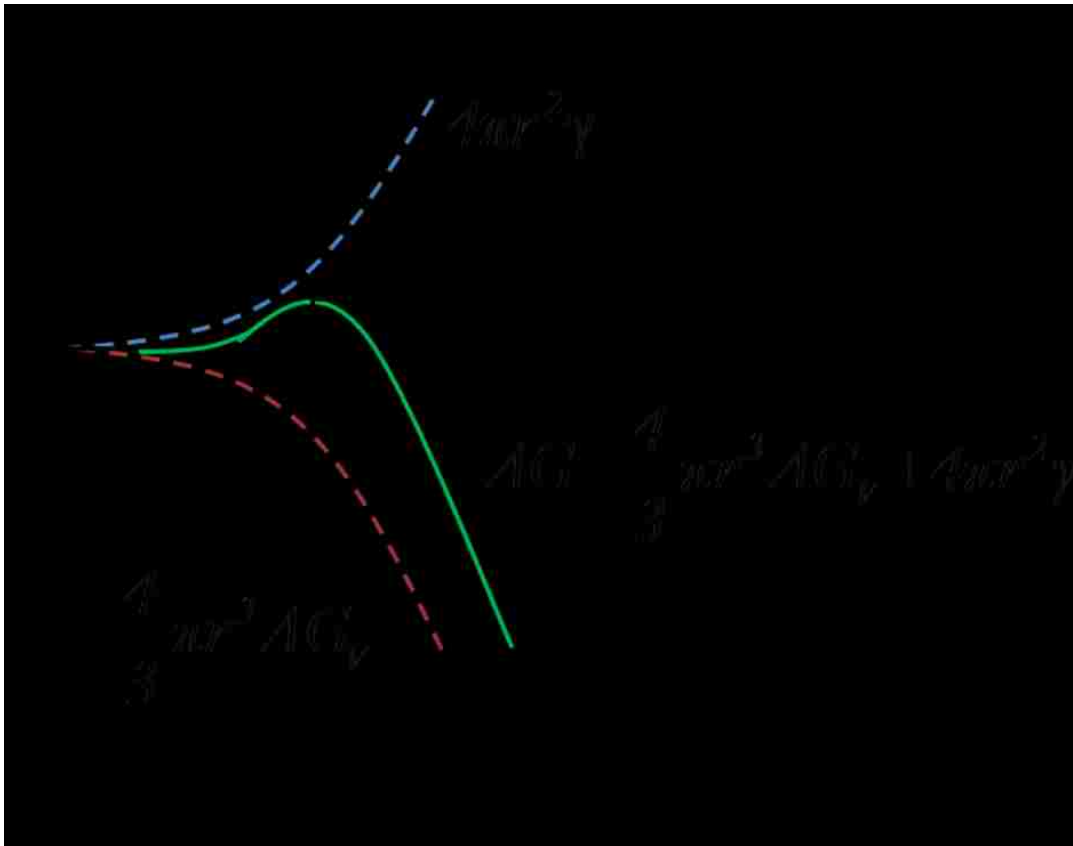
Figure 2.3: A plot showing activation energy for nucleation (*E*) as a function of nucleation size (*r*)[73].

2.2.2 Island Growth Mode or Volmer-Weber growth (VW) mode:

During an island growth mode, the smallest stable clusters nucleate on the substrate and grow in three dimensions (3D) to form islands. In this case for

island or VW growth mode, the deposited atoms are more strongly bound to each other than to the substrate. An example of this type of growth mode is typically a deposition of metal on insulators. Figure 2.4 (a) shows a schematic of the VW growth mode [98]. In this VW mode, the growing layer wants to minimize its interface energy
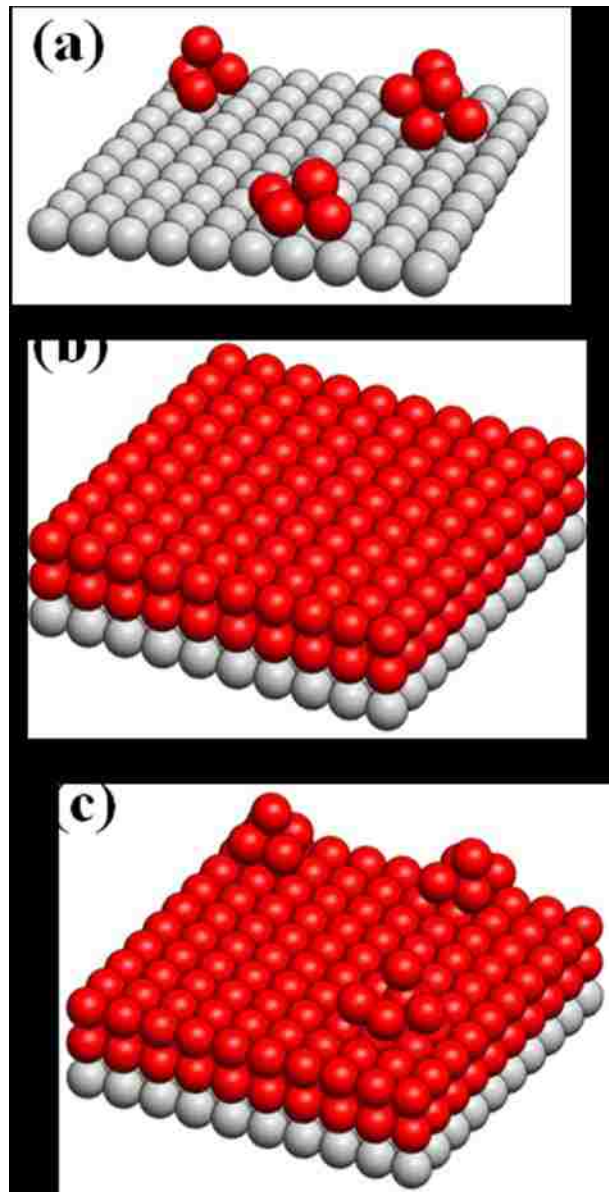
Figure 2.4: The three modes of epitaxy, (a) Volmer-Weber growth , (b) Frank-van der Mere, (c) Stranski-Krastanov.

and its own surface energy by forming "islands" on the surface. In order to favor island growth on surface, the following condition must hold true, and can be described by,

$$\gamma_{AV} < \gamma_{BV} + \gamma_{AB} \qquad (2\text{-}4)$$

Using 2-3 and 2-4, we obtain that ΔG is >0 and thus the system wants to minimize the surface energy by forming islands on substrate surface.

2.2.3 Layer Growth Mode or Frank Van der Merwe (FVM) Mode:

During a layer growth mode, the smallest stable clusters grow in two dimensions (2D), resulting in the formation of planar sheets. In this case for layer or FVM growth mode, the deposited atoms are more strongly bound to the substrate than each other. An example of this type of growth mode is typically a single crystal epitaxial growth of semiconductor films. Figure 2.4 (b) shows a schematic of the FVM growth mode [98]. In this FVM mode, the growing layer reduces thesurface energy, and wets the surface completely. As a result, a smooth layer on layer growth occurs. In order to favor layer-by-layer growth on surface, the following condition must hold true, and can be written as,

$$\gamma_{AV} > \gamma_{BV} + \gamma_{AB} \qquad (2\text{-}5)$$

Using 2-3 and 2-5, we obtain that ΔG is <0 and thus the system wants to minimize the surface energy by forming layers on substrate surface.

2.2.4 Stranski-Krastanov (SK) Growth Mode:

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Figure 2.4 (c) shows a schematic of the SK growth mode [99]. The balance of forces changes during the growth of first few layers in SK growth mode. The epitaxial layers consists of a continuous, smooth film that usually has properties that differ from the bulk. We also note that based on eqns. 2-3-2-5, the balance of charges changes during the SK growth if the materials (epitaxial layer and substrate) have a large lattice mismatch and the strain associated. The balance of charges depends on the surface and the interfaces of materials and also the initial condensation process influences the film structure. As we learn from previous section that the growth process always starts with nucleation process followed by a continuous film growth. By definition, nucleation refers to the initial few steps of film growth where sufficient number of vapor atoms or molecules condenses on the substrate. Once the nucleation stage ends, a uniform distribution of small, highly mobile clusters or islands start to form on the substrate surface while the substrate is subjected to vapor flux. Islanding happens during the SK growth to relieve the misfit strain without forming dislocations. The size and density of clusters start to increase until the islands begin to coalesce. This particular event is termed as coalescence phenomenon. The density of islands decreases during coalescence allowing further nucleation to occur. The coalescence continues until all unfilled channels, voids are filled, and this results to a continuous film. .

A Ge/Si heteroepitaxial growth system is a perfect example of the SK growth mode. As mentioned earlier that SK growth mode is a combination of the island and layer growth modes. The lattice mismatch between Ge and Si influences the balance of forces during the SK growth. Typically, the range of lattice mismatch that supports SK growth is between $3\% < \varepsilon < 7\%$ [99]. An initial adsorbate-wetting layer of

characteristic thickness forms during the SK growth. However, once one or more monolayers equivalent amount of growth materials get deposited on to substrate, the subsequent layer growth becomes unfavorable and island growth starts to occur to relieve the misfit strain. When the islands formation becomes favorable, then a transition from 2D to 3D islands, known as the SK-transition, begins to occur [99]. The final epitaxial layer consists of uncoalesced 3D islands with persisting wetting layer. Figure 2.4 (c) shows a schematic of islands and a wetting layer. The wetting layer is exaggerated in this image to highlight the SK growth mechanism. Here are few examples of heteroepitaxial systems that follow the SK growth model: Ge/Si, InAs/GaAs, PbSe/PbTe, CdSe/ZnSe, PTCDA/Ag. Researchers also have demonstrated that the SK growth mechanism can be used to grow self-assembled quantum dots (QDs) [100].

2.3   Molecular Beam Epitaxy

One of the most used and reliable epitaxial growth systems is Molecular beam epitaxy (MBE) system. The MBE system comprises of several important engineering parts including an ultra-high-vacuum (UHV) chamber in which the growth takes place. The growth involves the impingement of atomic or molecular flux onto a heated single-crystal substrate where the epitaxial layers grow [101]. The source flux originates from Knudsen cells or gas-source crackers. Shutters and valves that are attached to the cell are used to turn on and off the flux, providing an atomic layer abruptness. Often MBE employs a number of in situ characterization tools based on electron or ion beams for feedback and control of growth process. Several heteroepitaxial systems can be grown using MBE technique, including III-V and II-VI

semiconductors; Si, Ge, and $Si_{1-x}Ge_x$ alloys; and SiC and $Si_{1-x-y}Ge_xC_y$ alloys. There are few area where MBE proves unsuccessful, namely III-phosphides, and their alloys involving As and P. Also, MBE systems are expensive, and maintainace costs are very high.

An MBE reactor involves a number of source cells arranged radially in front of a heated substrate holder. Figure 2.5 shows an image of the MBE deposition system used in this work. The deposition chamber is connected to an entrance load lock that is pumped with a turbomolecular pump operating at 240 L/s. The load lock is vented with pure N_2 gas and the pressure is monitored with a thermocouple (TC) and cold-cathode gauge for measuring low and high vacuum, respectively. The deposition chamber is pumped with a 500 L/s turbo pump and a 400L/s ion pump that produce a base pressure of 5×10^{10} Torr, which is measured with an ion gauge. The effusion cell has a dual-filament with a double-walled pyrolytic
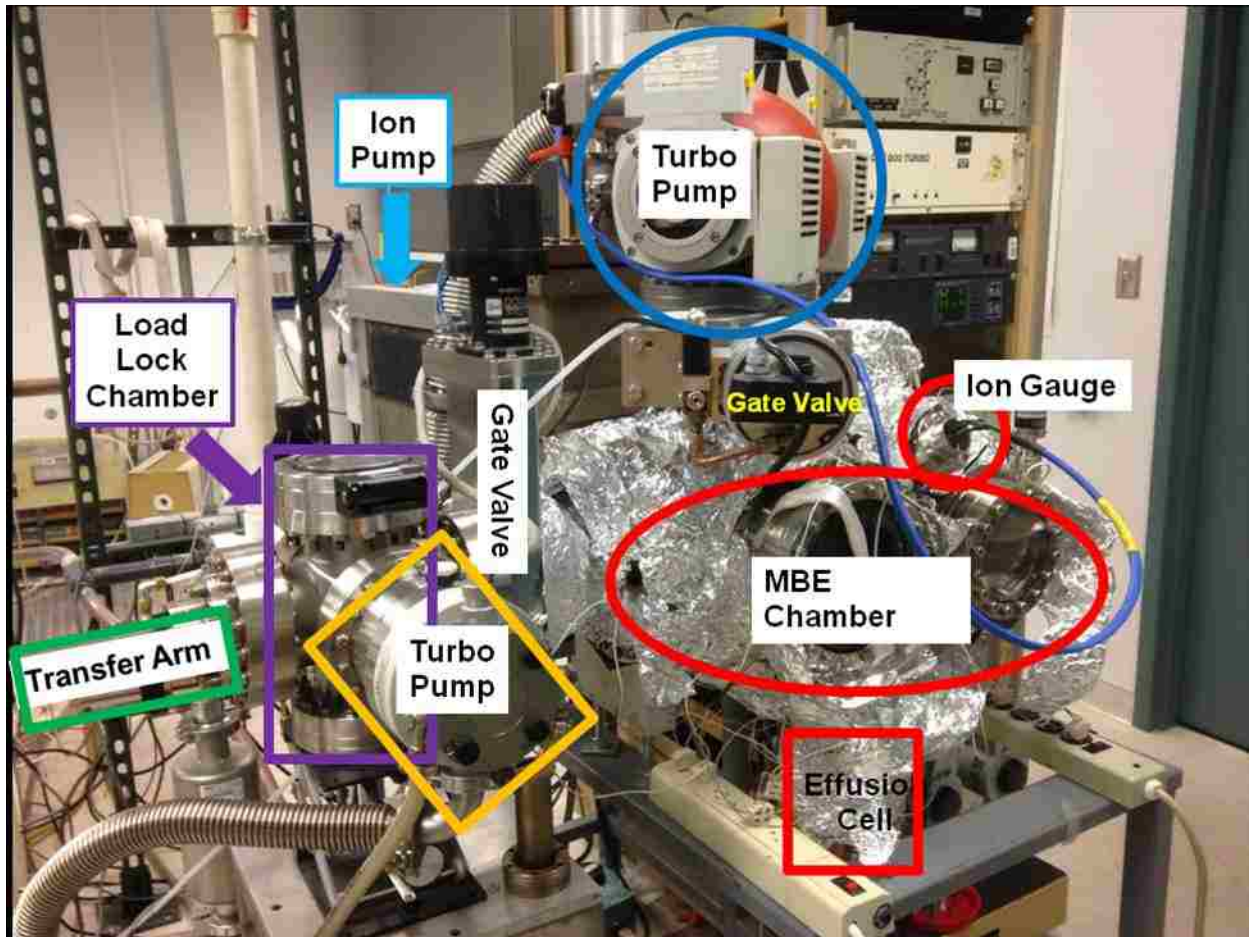
Figure 2.5: The molecular beam epitaxy vacuum chamber system used in this work with major components labeled.

boron nitride (PBN) crucible filled with Ge source material of 99.9999 % purity. The effusion cell temperature is measured using two TCs placed near the outside of the PBN crucible. The deposition rate is measured at a point on the sample that is perpendicular to the source at several substrate temperatures, where $\theta = 0$.

Lets try to understand how MBE evaporation work. The evaporation starts from source cell. First, the mean free path for an evaporated atom or molecule need to be estimated assuming that all other particles in the system are at rest. Let's consider that the velocity of evaporated particle is c, and all particles have a round

cross section with diameter σ. Any two particles that cross each other in a distance of σ or less will collide. Therefore, collision cross section of each particle can be written as $\pi\sigma^2$ and collision frequency of single particle can be written as $c\pi\sigma^2 dt$. If there are N particles in a volume, then the collision frequency will be, $Nc\pi\sigma^2 dt$. The mean free path of a particle can be written as,

$$\lambda = c/ Nc\pi\sigma^2 = (N\pi\sigma^2)^{-1} \tag{2-5}$$

However, a more realistic calculation of the mean free path can be made assuming that all particles are in motion. Based on this, the modified mean free path for an evaporated particle can be written as,

$$\lambda = (N\pi\sigma^2 * 1.414)^{-1} = kT/(1.414 * \pi\sigma^2 P) \tag{2-6}$$

where P is the pressure of MBE chamber. For example, typical values of σ range from 2 to 5 Å, so that λ is about 10^3 cm at a pressure of 10^{-5} torr.

The effusion cells or Knudsen cells are one of the simplest source cells being used in a MBE system. The flux of atoms from effusion cell is calculated based on kinetic theory of gases [102]. The evaporation rate from a surface area A_e can be written as,

$$\frac{dN_e}{dt} = \frac{A_e P}{\sqrt{2\pi kTm}} \tag{2-7}$$

where P is the equilibrium vapor pressure, T is effusion cell temperature in Kelvin and and m is the mass of the vapor or evaporant. The effusion rate can also be written in following manner,

$$\frac{dN_e}{dt} = \frac{A_e P}{\sqrt{2\pi kTM / N_A}} \tag{2-8}$$
$$where\ m = M / N_A$$

where M is weight of the molecular species and N_A is the avagadro's number. By plugging in value of N_A, the equation becomes more comprehensible, can be written as,

$$\frac{dN_e}{dt} = 3.51 \times 10^{22} \frac{A_e P}{\sqrt{MT}}$$

(2-9)

We note that P or equilibrium vapor pressure is greatly dependent on temperature of the effusion cell. Now, let us turn our attention to the substrate surface. The flux of evaporant that is arriving at the heated substrate surface based on evaporation or effusion rate, can be

$$J = \frac{\cos\theta}{\pi R^2} \frac{dN_e}{dt}$$

(2-10)

where R is the distance between effusion cell and substrate heater, and θ is the angle between the beam axis and the normal to the substrate. The evaporation model outlined above assumes that evaporation occurs at mouth of the effusion cell. Unfortunately, the evaporation rate falls off over time, subsequently beam profile also changes its shape over time. The use of tapered effusion cells can mitigate this effect to some extent. A useful application of Equation (2-7) is the calculation of the time required to coat a surface with gas molecules. For the time to complete one monolayer coverage on a surface containing 10^{15} atoms cm^{-2}, the use of Equation (2-7) yields

$$\tau_c = \frac{10^{15}}{3.513 \times 10^{22}} \frac{(MT)^{1/2}}{P} = 2.85 \times 10^{-8} \frac{(MT)^{1/2}}{P} \sec$$

(2-11)

In air at atmospheric pressure and ambient temperature, a surface will acquire a monolayer of gas in 3.5 nanoseconds, assuming all impinging atoms stick to the surface. At a pressure of 10^{-10} torr, the surface will remain uncoated for 7.3 hours. These calculations demonstrate the importance of ultra-high vacuum background pressures when film purity is important.

2.4 Selective Epitaxial Growth

The SEG of Ge and GeSi has become increasingly important in a variety of advanced device applications, including high-speed HBTs [103-105] and metal-oxide semiconductor field-effect transistors (MOSFET) [106,107]. Other applications include ordered arrays of quantum dots [108-112] for photodetectors [113] and quantum cellular automata [114]. In addition, SEG is required in the aspect ratio trapping and finite area growth defect reduction strategies for heteroepitaxy discussed in Chapter 1.

In SEG, the substrate surface contains areas of crystalline material adjacent to amorphous insulating materials. Epitaxial growth is desired on the crystalline portion of the substrate, but not on the insulating portions. Nucleation on amorphous insulators is random in nature and leads to polycrystalline or amorphous thin film growth. For successful SEG, random nucleation on the insulator must be prevented. Thus, it is important to determine the mechanisms and energetics of nucleation on the insulator responsible for optimal selectivity. The nucleation energetics can be extracted by applying atomistic nucleation theory to measurements of island densities on the insulator. The fundamentals of atomistic nucleation theory are presented next and applied to experimental results of Ge nucleation on SiO_2 to extract the energetics of the nucleation process. The energetics of Ge nucleation on SiO_2 are then used, in turn, to achieve optimal selectivity of Ge on Si versus SiO_2, and to understand the mechanisms involved in achieving SEG.

2.5 Heterogeneous Atomistic Nucleation Theory

Heterogeneous nucleation is the process that is more relevant to the case of heteroepitaxy. The nucleation rate greatly depends on surface types. Typically,

heterogeneous nucleation can be studied using two different models, such as, a macroscopic model , and atomistic model [115-117]. The macroscopic model is frequently used to study homogenous nucleation on surface, and can also be used to study heterogeneous nucleation. The macroscopic model takes consideration of surface free energies and balance of forces to determine the nucleation rate. In contrast, atomistic model uses a rate-equation approach to predict the energetics that are involved in the island nucleation process. The atomistic nucleation theory is directly applicable to nuclei containing as few as two atoms. Through this discussion of atomistic model theory, nucleation will be used as a tool to predict growth of nuclei on a substrate as in the case of heteroepitaxy. In addition, this model will be used to further predict nucleation of new clusters of epitaxial material on top of an wetting layer (second-layer nucleation) during a SK growth.

The atomistic model for heterogeneous nucleation assumes that atoms arrive at a flat surface with an impingement flux of R (atoms per unit area per unit time). Based on incident flux, we assume that concentration of adatoms (per unit area) on the surface equal to n_1. This gives rise to unstable clusters of two or more atoms on the surface. However, there will also be stable clusters beside unstable clusters. These unstable clusters are constantly shrinking to reduce free energy of their system, and subsequently large clusters are constantly forming by growing. We assume that critical clusters have i atoms, and stable clusters have an average of w_x atoms in each cluster. Not to mention that here $w_x > i$, because all clusters containing more than i atoms will be stable. We also assume that n_x and n_j denote the concentration of stable clusters and unstable clusters of w_x atoms and j atoms each, respectively. Figure 2.6 shows an image

of   interaction   of   the   adatoms   and   surface   clusters.
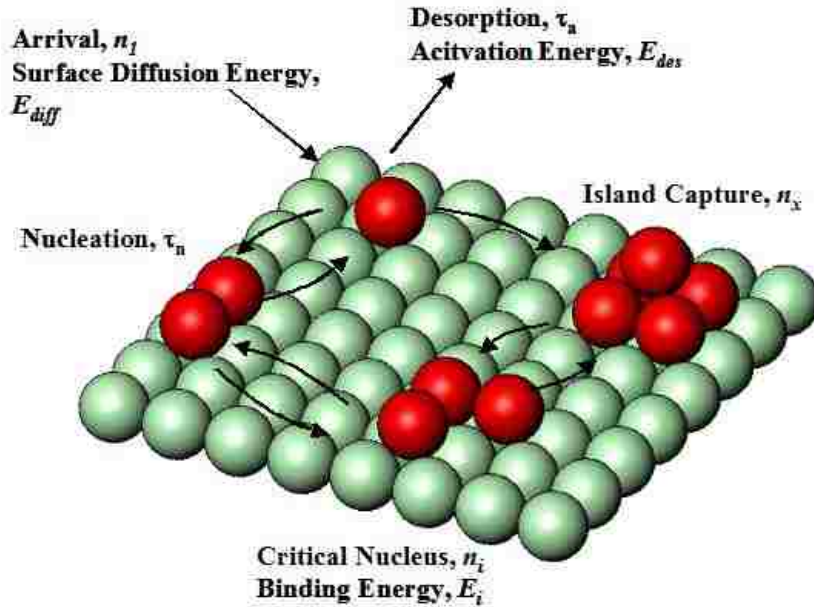
Figure 2.6: Depiction of the atomic processes occurring on a surface due to impingement of atoms from an evaporation source. The notation used in developing atomistic nucleation theory is also shown for each process [95].

Adatoms once arrive on the surface may have three possibilities:

reevaporate (with a time constant τ_a), combine with other adatoms or unstable clusters or

being captured by a critical cluster (nucleation, with a time constant τ_n), or being

captured by a stable cluster (with a time constant τ_c). Therefore, the rate equations for

this system are represented mathematically by, based on Stowell and Hutchinson [118,119]

$$\frac{dn_1}{dt} = R - \frac{n_1}{\tau_e} - \frac{d(n_x w_x)}{dt} \qquad (2\text{-}12)$$

$$\frac{dn_j}{dt} = 0 \qquad 2 \le j \le i \qquad (2\text{-}13)$$

$$\frac{dn_x}{dt} = \sigma_i D n_1 n_i - 2 n_x \frac{dZ}{dt} \qquad (2\text{-}14)$$

Equation (2-12) denotes the time rate of change of the adatom concentration, in which the

first term represents condensation, second term represents reevaporation or desorption,

and third term represents diffusive capture by stable clusters. Equation (2-13) denotes the time rate of change of unstable clusters is zero. This means that populations of subcrtical or unstable clusters are constant with time. However, this is true if the growth happens near equilibrium. Equation (2-14) describes that the time rate of change of the concentration of stable clusters, in which the first term represents the formation of new stable clusters (with concentration n_1) by the diffusive capture of adatoms (with population n_i). Here, D is the surface diffusion constant of adatoms and σ_i is the capture number for the critical-size clusters. The second term in Equation (2-14) denotes the coalescence of stable clusters, in which Z is the fraction of the surface covered by stable clusters. The range for Z is $0 \leq Z \leq 1$.

In this section, we will develop a model to predict nucleation rate. Equations (2-12) and (2-14) are coupled through

$$\frac{d(n_x w_x)}{dt} = (i+1)\sigma_i Dn_1 n_i + \sigma_x Dn_1 n_x + Rn_x w_x$$

$$= \frac{n_1}{\tau_n} + \frac{n_1}{\tau_c} + RZ \tag{2-15}$$

Moreover, in steady state, right side of eqn. (2-12) can be assigned to zero.

$$n_1 = R\tau(1-Z) \tag{2-16}$$

where $\tau^{-1} = \tau_c^{-1} + \tau_n^{-1} + \tau_a^{-1}$, and $\tau_c^{-1} = \sigma_x Dn_x$.

Now, based on number of atoms in the stable clusters, the substrate coverage Z is can be expressed by,

$$\frac{dZ}{dt} = N_a^{-1} \frac{d(n_x w_x)}{dt} \tag{2-17}$$

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where N_a denotes the areal density of atoms in the stable clusters. The relationship between the populations of critical clusters and adatoms can be expressed by,

$$\frac{n_i}{N_0} = \left(\frac{n_i}{N_0}\right)^i C_i \exp\left(\frac{E_i}{kT}\right) \qquad (2\text{-}18)$$

where N_0 is the atomic density in the substrate crystal, E_i is the free energy change in critical size cluster, and C_i is a constant. Based on eqns. (2-12) through (2-18), we obtain an expression for the normalized saturation density of stable nuclei, which can be written as,

$$\frac{n_x}{N_0} = C\eta \left(\frac{R}{N_0 v}\right)^q \exp\left[\frac{E_n}{(i+2)kT}\right] \qquad (2\text{-}19)$$

where C and η are constants and v is the surface vibration frequency ($\sim 10^{11}$ to 10^{13} s^{-1}). Finally, the nucleation rate can be written as,

$$J = \sigma_i D n_1 n_i \qquad (2\text{-}20)$$

Expressions for the energy, E_n, and the exponent q are listed in Table 2-1 for three specific conditions: complete, initially incomplete, and extreme incomplete condensation. Now, the E_n comprises of three parts: lateral binding energy (E_i), desorption activation barrier (E_{des}), and diffusion (E_{diff}) activation barrier.

Table 2-1. Expressions for the exponent p and energy E_n in Equation (2-19) that depend on the condensation regime and whether the islands are two or three-dimensional [95]

Regime	3D Islands	2D Islands
Extreme Incomplete	$p = 2i / 3$ $E_n = 2/3 [E_i + (i +1)E_{des} - E_{diff}]$	i $[E_i + (i +1)E_{des} - E_{diff}]$
Initially Incomplete	$p = 2i / 5$ $E_n = 2/3 (E_i + iE_{des})$	$i / 2$ $1/2 (E_i + iE_{des})$
Complete	$p = i/ (i + 2.5)$ $E_n = (E_i + iE_{diff}) / (i + 2.5)$	$i /(i + 2)$ $(E_i + iE_{diff}) / (i + 2)$

.

Based on the activation barrier height, we can determine the regime of condensation. For example, extreme incomplete condensation regime represents low E_{des} and E_{diff} activation barriers. Because of these low activation barriers, the characteristic surface diffusion length is much less than the interdistance of nucleated islands in the case for extreme incomplete condensation. The example of such regime is islands formation only from impingement from the vapor. In comparison, the initial incomplete and complete regimes are associated with high E_{des} but low $E_{diff,}$ and high E_{des} and/or extremely low $E_{diff,}$ respectively. The example of initial complete regime is when the nucleation density is sufficiently low. The characteristic diffusion length does not exceed the interdistance of nucleated islands in the initial complete regime, resulting in desorption of adatoms before being captured by a stable island. Complete condensation regime represents the case when the nucleated islands capture all diffusing adatoms. This regime also suggests that the saturation nucleation density is reached. The natural log of the saturation number density of islands can be plotted against $1/T$ from eqn. (2-19). This step is required to further extract values of E_{des} and E_{diff}. These values of activation

barriers can be totally correlated to the regime of condensation and the island morphology that is present on the substrate surface. Previous members of our group, *Li et al.,* and *Leonhardt et al.* work have shown that how atomistic nucleation theory can be applied to Ge on SiO_2 system. Specifically for Ge on SiO_2, Li *et al.*[120] reported 0.44 ± 0.03 eV for an experimentally measured desorption activation energy of Ge from SiO_2. Later, *Leonhardt et al.* [84] reported the measurement of Ge nucleation on SiO_2 over a much broader range of temperatures and deposition rates. Nucleation density and energetics of Ge on SiO_2 are described next.

2.6   Nucleation Density and of Energetics of Ge on SiO_2

From the discussion in previous section on the atomistic nucleation theory, we realize that a thorough understanding of this atomistic model of nucleation of Ge adatoms on SiO_2 surface can be used later to predict a SEG behavior of Ge on Si substrate. This section will give the details about the nucleation density and energetics of islands of Ge deposited on SiO_2 surface. This discussion is based on the work from *Leonhardt et al.* [85] Details of the SiO_2 sample preparation and Ge deposition can be found in this literature. A 100-nm thick SiO_2 is grown on Si substrate ($1 - 10$ Ω-cm), and a MBE growth process is used to deposit Ge. The pressure in the chamber remains below 1×10^{-8} Torr during the deposition. Multiple samples have been produced to get a better statistical estimate. Finally, all these samples are characterized using scanning electron microscopy (SEM). The Ge islands are semicircular in shape and are randomly distributed across the surface.

The following discussions on nucleation and energatics have two main goals. First, by measuring the saturation nucleation density of Ge islands on SiO_2 as a function of substrate temperature sets up a platform to determine the optimal growth conditions for selective growth on patterned SiO_2 samples. Second, the nucleation measurements as a function of substrate temperature helps to estimate desorption activation energy of adatoms, which is going to be useful to determine the size of the critical nucleus and the condensation regime in which Ge growth takes place.

Here are the two key results based on the nucleation measurements. Figure 4-6 shows a plot of natural log of the saturation nucleation density versus $1/T_{sub}$. The figure shows that the saturation nucleation density vares by over 5 orders of magnitude across this temperature range. We identify two different slopes in the data: one from 673 to 773 K and one from 773 to 973 K. We speculate that the discontinuity in the slope originates from a change in the critical nucleus size (*i*) or from a transition in the regime of Ge condensation on SiO_2. Later, to confirm the cause of this discontinuity, an experiment is performed where the integral condensation coefficient is characterized as a function of amount of Ge condensed on the surface. The integral condensation coefficient is characterized by measuring a ratio of total mass of Ge condensed to total mass of Ge impinged on the surface. From this experiment, a conclusion has been made on what causing this discontinuity in the slope. It appears that the condensation regime, which is extremely incomplete, influences the entire experimental range.
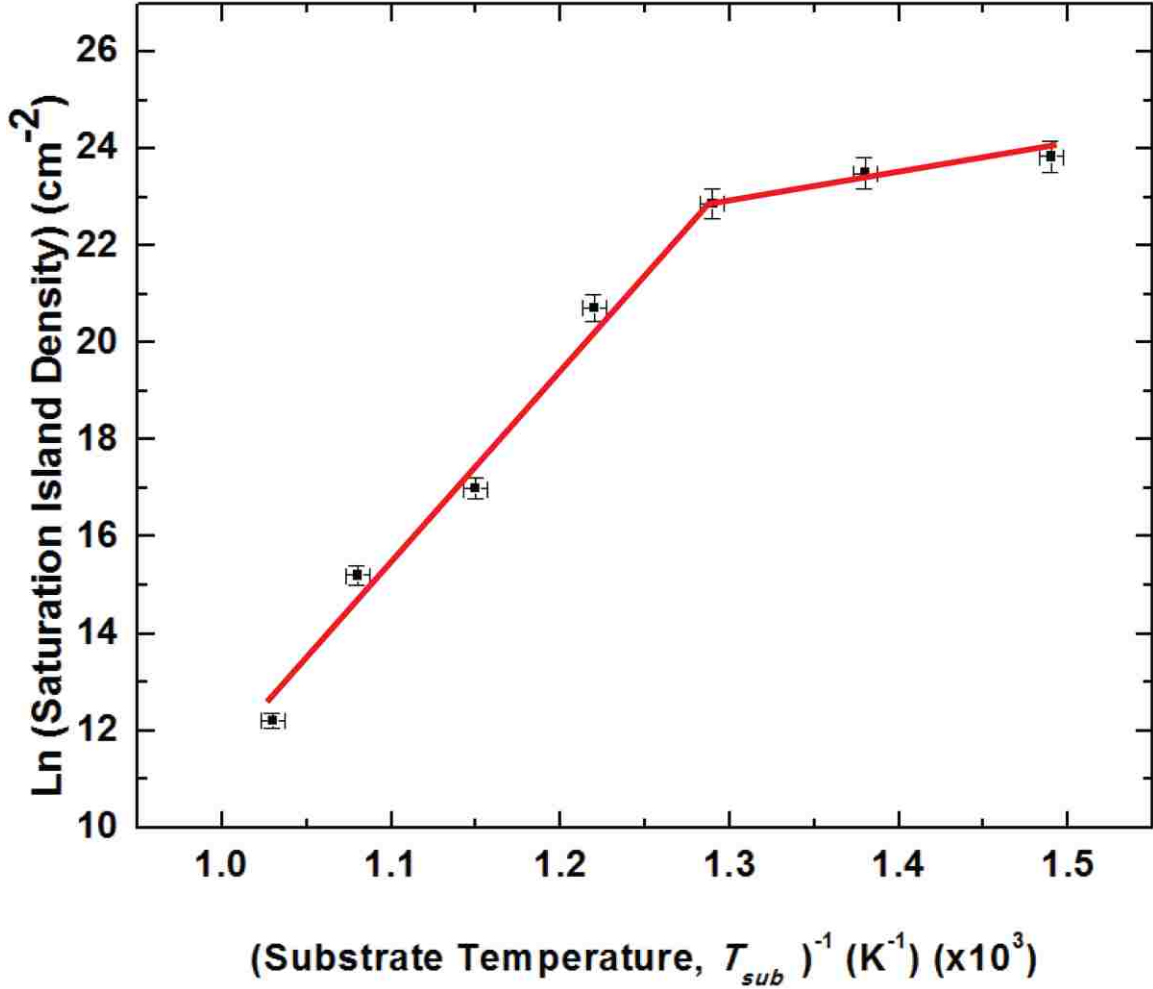
Figure 2.7: Natural log of the saturation nucleation density versus reciprocal substrate temperature. This plot reveals two distinct slopes that occur over the temperature intervals of 673 to773 K and 773 to 973 K, and this graph is used to extract the activation energies involved in the nucleation process (taken from) [95].

In the case of extreme incomplete condensation,[121]

$$p = 2i/3 \text{, and} \tag{2-21}$$

$$E_n = \frac{2}{3}\Big[E_i + (i+1)E_{des} - E_{diff} \Big] \tag{2-22}$$

where E_i is the binding energy of the critical nucleus relative to i isolated atoms. Based on previous discussions, herein we provide only the important findings about nucleation density and activation barriers that are associated to Ge islands on SiO_2. The linear

regression yields a value of $p = 0.8 \pm 0.1$ at 723 K and $p = 1.4 \pm 0.2$ at 773 K, shown in

fig. 2.7. Not going in to details, fig. (2.7) also yields a value of $2E_{des} - E_{diff} = 0.65 \pm 0.02$

eV for the low temperature interval (673 – 773 K). Based on x-ray photoelectron

spectroscopy, which helps to estimate $E_{des} = 0.44 \pm 0.03$ eV, leads to a value for $E_{diff} =$

0.24 ± 0.05 eV. Similarly, the values for E_{des} and E_{diff} arealso found for the high

temperature interval (773 – 923 K). The values of E_{des} and E_{diff} can be used to estimate

activation barriers for the selective growth. First, the average distance, X, that Ge

adatoms migrate on the surface before desorbing is calculated based on this equation [122]

$$\overline{X} = \left[\frac{1}{2N_\circ^{\frac{1}{2}}} \exp\left(\frac{E_{des} - E_{diff}}{2k_B T_{sub}} \right) \right] \tag{2-23}$$

Based on eqn. (2-23), we measure the values for E_{des} and E_{diff} results in a migration

distance of only 0.9 ± 0.3 nm at 673 K and 0.5 ± 0.2 nm at 973 K, assuming $N_o = 1$ x

10^{15} cm^{-2}. This is an important finding. The measured diffusion distance is small for Ge

adatoms on SiO$_2$, and we speculate that the the short adatom lifetime on the oxide

surface ultimately governs the selective growth of Ge on SiO$_2$ surface.

CHAPTER 3 FUNDAMENTALS OF CHARACTERIZATION TECHNIQUES

Material Characterizations:

3.1   X-Ray Diffraction:

In this section we will discuss the instrumental analysis technique known as x-ray diffraction (XRD). This is one of the oldest forms of non-destructive x-ray crystallography. The purpose of the single-crystal XRD technique is to determine the molecular structure of single-crystal. This can be divided into three subsets that are actually process in determining the structure of the crystal. The first step is to analyze the dimensions of the crystalline lattice. This involves determining the unit cell dimensions, and the positions of the atoms in the lattice that are directly related to the bond length and angles of the atom to atom. Step two involves determining the structure of the crystalline lattice from the information that is gathered from step one. The third step involves comparing of spectra for crystal identification. The first part of the XRD is a x-ray tube, this is where x-rays are created by a cathode ray tube dislodging electrons from a specified target such as molybdenum. The strong attack of electrons produce x-ray then head toward crystal holder through a collimator. The crystal holder is a part of a diffractometer that keeps the crystal in a fixed position allowing the x-rays to interact with the crystal. The x-rays are either reflected or refracted against the crystalline lattice. The angle of incidence of x-rays against the crystalline lattice defines the spectrums produced. The third and final part of XRD is x-ray detector. This is where the diffracted x-rays can be seen as spots against the detector. The spectrum is determined by the spots, which should have seen as deflection of x-rays of the crystalline lattice. Figure 3.1(a) shows a 3D view of the XRD set-up. Beginning of the x-ray tube denoted here is a

micro-focus x-ray tube, where the target material produces x-rays. The x-rays are then directed to sample holder through a pinhole collimator. The sample is sat on the sample holder allowing x-rays to interact with the crystal lattice. Once the x-rays are out of the crystal then it reaches to the x-ray detector, denoted as
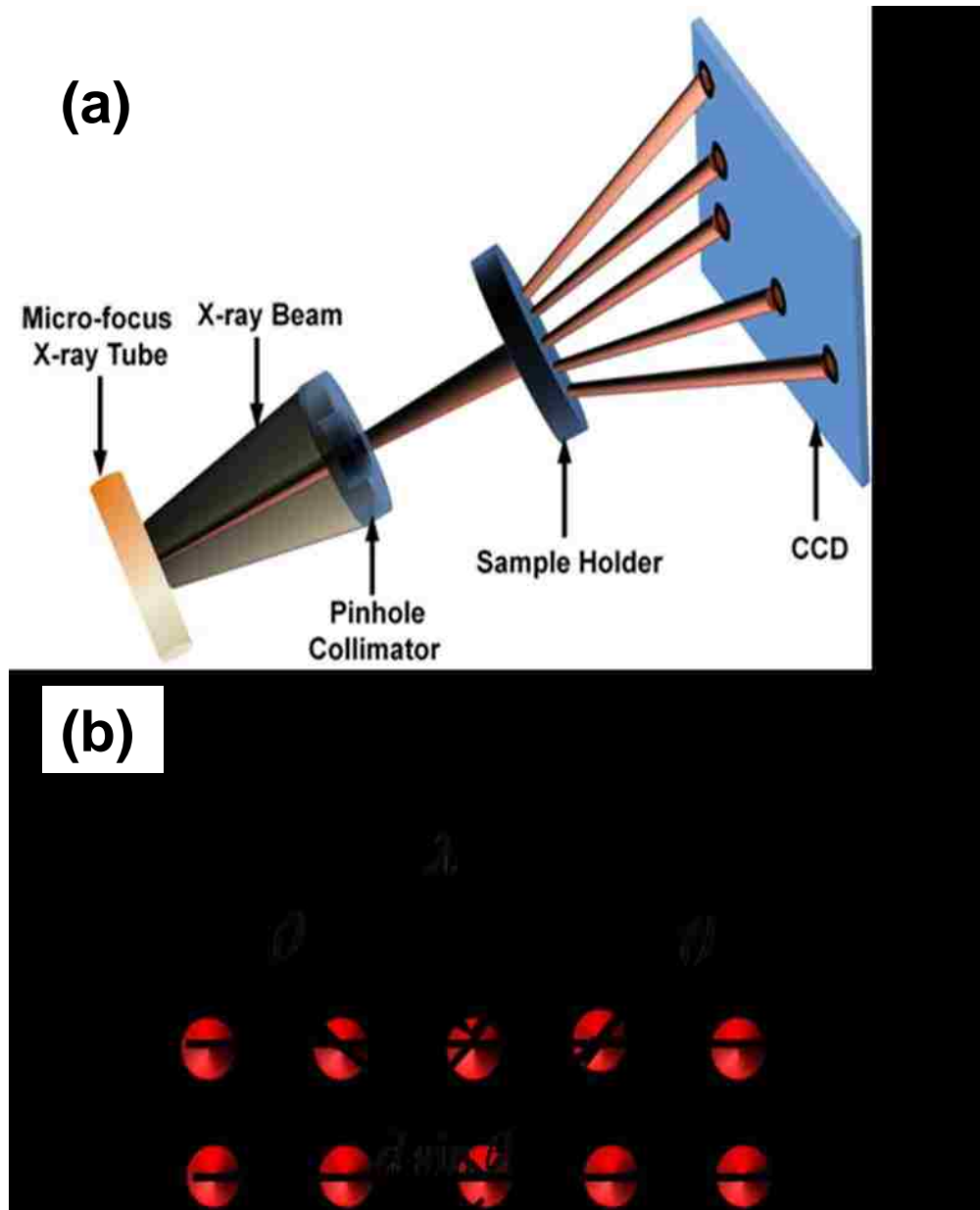
Figure 3.1: (a) A 3D view of x-ray diffraction set-up. The x-ray is being generated from a x-ray tube, passing through pinhole collimator, and sample, and ultimately hitting the CCD screen. The diffraction spots are generated on the screen. (b) a schematic showing how x-ray interact with atoms in a crystal.

charge coupled device (CCD). The diffraction spots can be seen on the CCD detector screen, shown in fig. 3.1.

Figure 3.1(b) shows a schematic of x-rays that are interacting with the atoms in the crystal. The interplanar distance is in the order of wavelength of x-rays. Figure 3.1 (b) shows two incident x-rays parallel to one another make an angle θ with respect to plane of the atoms. When x-ray 1 and 2 reflect, they will interfere constructively when they travel a total distance that differs by a whole number multiple of their wavelength; that is when the two waves are fully in-phase. In order for x-rays to properly diffracted, the angle of incidence of x-rays against the atoms in the crystal must satisfy Bragg law, which can be expressed by,

$$2d \sin \theta = \lambda_0 \ . \qquad (3\text{-}1)$$

where d = lattice interplanar spacing of the crystal, θ = x-ray incidence angle (Bragg angle), and λ_0 = wavelength of the characteristic x-rays.

3.2   X-ray Photoelectron Spectroscopy:

The technique that we are going to describe in this section is x-ray photoelectron spectroscopy (XPS). The development of XPS is credited to Dr. Kai Siegban, a Swedish physicist and his team. Dr. Kai Siegban was able to record the first high-resolution XPS spectrum in 1954, his paper on the findings of his research and development was published in 1967, and in 1969 the first XPS instrument was produced in the Unites States. In 1981, he received the Nobel Prize in physics for his work in the development of XPS. The technique work based on the following phenomenon of the photoelectric effect. Figure 3.2 shows the flow of energy described by the photoelectric

effect. In this technique, the incoming x-ray impact the surface of the sample, and cause core electrons to ionize and emit photoelectrons. The electro analyzer in an XPS detects electron binding energy (BE). In XPS, the data is generated by comparing the number of photoelectrons detected from the surface to the BE of the electrons detected. Binding energy of electrons is calculated by the subtracting the energy of the incoming
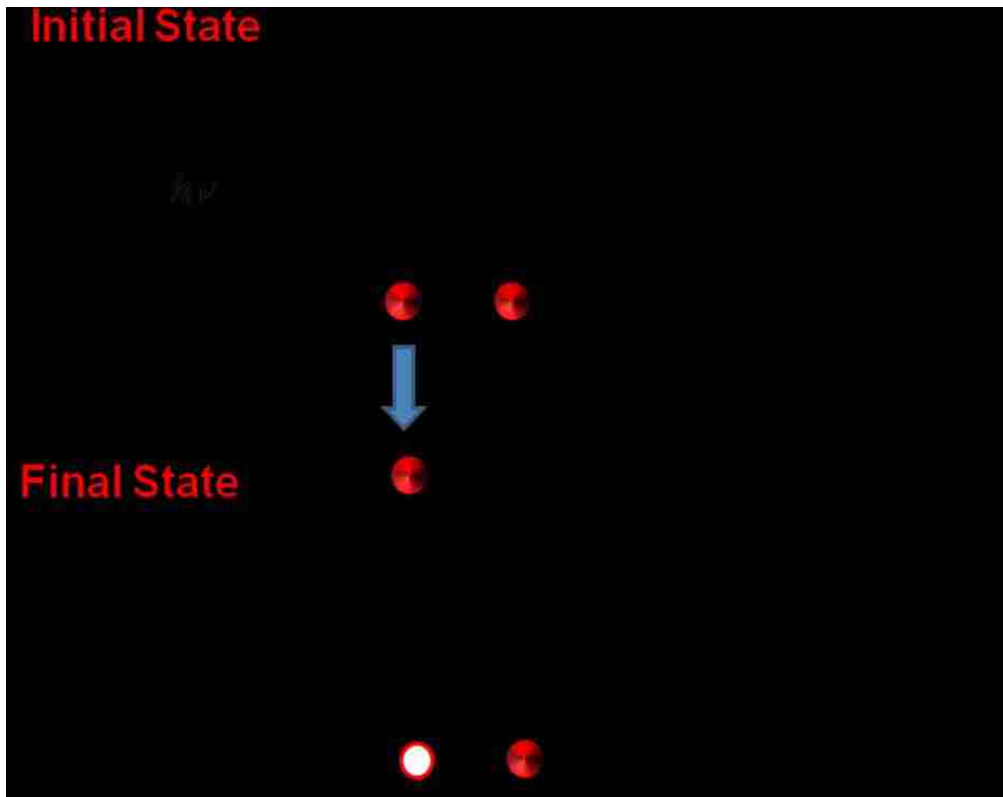
Figure 3.2: A schematic illustrating a phenomenon called photoelectric effect, which is the key for x-ray photoelectron spectroscopy.

photons from the kinetic energy (KE)of the photoelectrons emitted. The binding energy can be expressed by,

$$E_{binding} = E_{photon} + (E_{kinetic} + \phi) \qquad (3\text{-}2)$$

The following describes how a XPS system works. A focused beam of x-rays is used to irradiate the surface of a sample, which causes electron from the top layer of the surface

(top 1 to 10 nm) to release photo-emitted electrons. These photo-emitted electrons are then analyzed by electron analyzer. Figure 3.3 shows a real life picture of a XPS system located in our CHTM laboratory. The instrumentation of XPS system includes a x-ray emission source, electroanalyzer, electron multiplier, ion gun, vacuum system, electronic controls, and computer control system. The
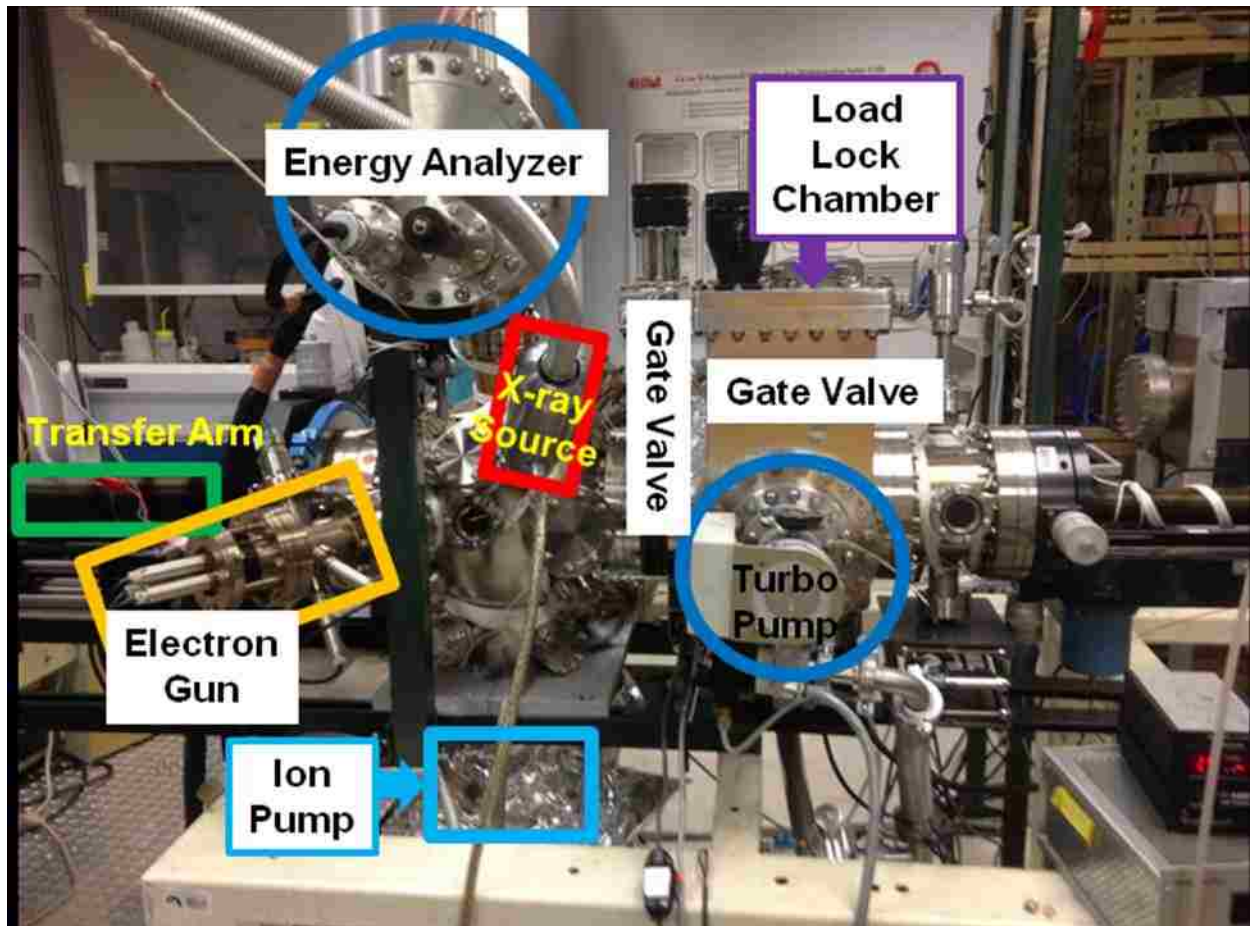
Figure 3.3: An experimental set-up of x-ray photoelectron spectroscopy system.

advantages of the XPS system include relatively simple spectrum produced from XPS system, high accuracy in identifying samples, good resolution, and non destructive. The limitations of the XPS system include samples must endure ultra high vacuum, cannot see elements smaller than Li, and sample area must be small (10 μm).

3.3   Scanning Electron Microscopy:

The scanning electron microscopy (SEM) is a technique that is used for measuring the thickness of films and surface topography. The SEM uses a beam of electron to form an image of the sample surface. Figure 3.4shows a cut-out 3D view of SEM tool. The top most part of the tool is a thermionic electron gun, which generates a beam of electron that interacts with the sample located at the bottom of the tool. The generated electrons are attracted toward a positive anode, and the charged beam is simply pass through a hole that is located right in the middle of the anode. The electron beam is focused using a series of electromagnetic lenses denoted as condenser lens. These lenses are not simple glass lenses; rather they are electromagnetic lenses, which uses electric and magnetic fields to manipulate a path of charged electron beam. The focused beam of electrons then interacts with the sample or specimen through elastic and inelastic collisions processes. The elastic collisions produce backscattered electrons (BE) coming from the surface and from deeper within the sample. The BE electrons are basically reflected electrons. The inelastic collisions produce secondary electrons (SE) coming from the top surface of the sample. Now the BE and SE electrons head toward a positively charged detector, known as faraday cage. Later these collected electrons are used to create an image on the screen. This is extremely important to understand why this called scanning electron microscope. The primary beam of electrons actually scans over the surface of the sample, and based on its incoming energy, this scanning beam excites a volume on the sample. Later, the SE that are generated from the entire volume

reach to detector, and contribute the image formation. Usually, the electron beam diameter is on the order of 1 to 2 nm.
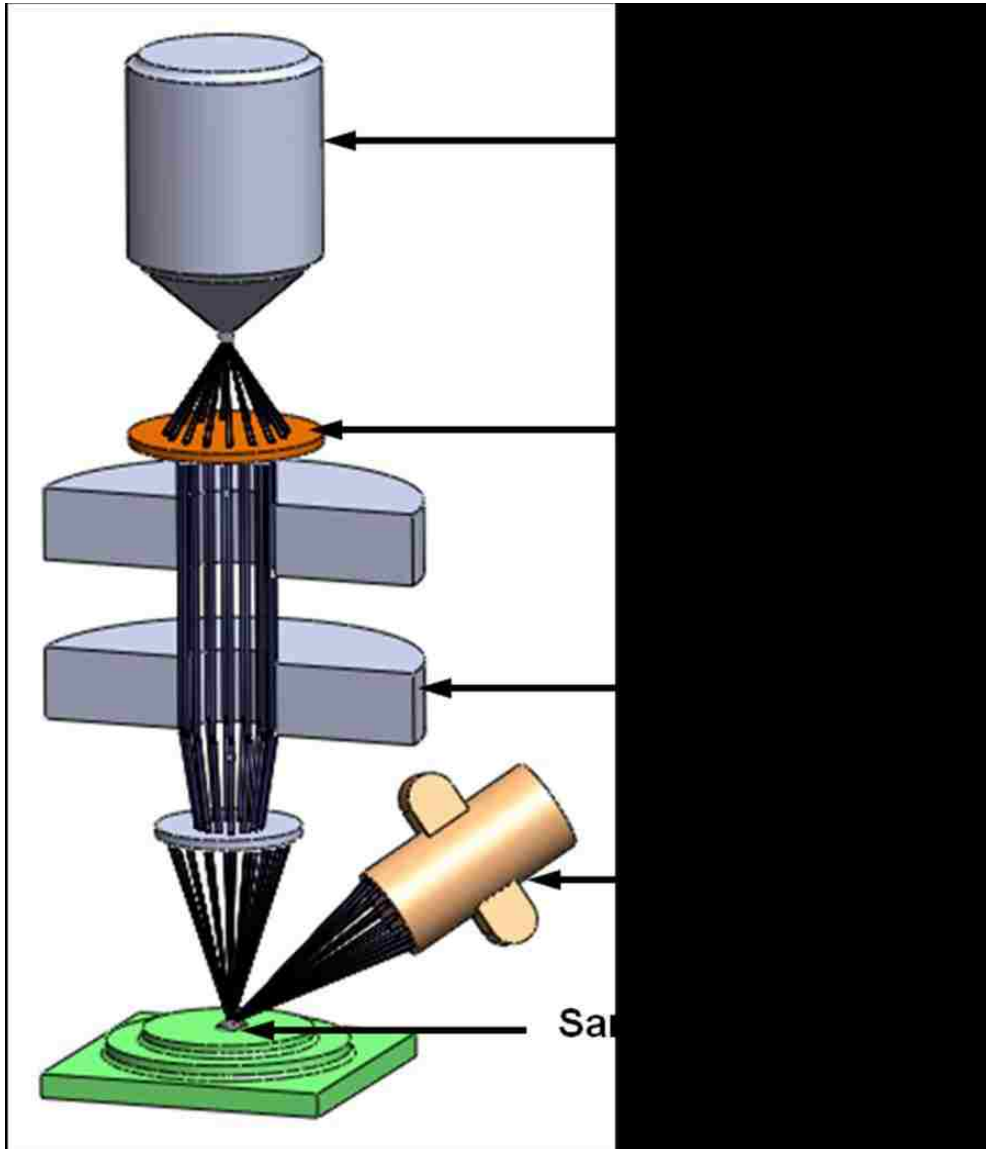
Figure 3.4: A 3D cut-out view of scanning electron microscope.

3.4   Focused Ion Beam:

The goal of the focused ion beam (FIB) in-situ lift-out method is to prepare a thin, electron transparent membrane to be imaged using a high-resolution TEM machine. An advantage of FIB method is that the specimen can be prepared from the starting bulk sample. The FIB instrument is very analogous to a SEM. Figure 3.5 shows a cut-out 3D view of a FIB instrument. This consists of a vacuum chamber, a liquid metal ion source (mostly Ga ions), an ion column, a sample stage, detectors, gas delivery system. The liquid metal ion source (LMIS) makes use of ion-assisted sputtering to etch materials from the sample. There are various reasons why Gallium mostly used for LMIS in FIB instruments: low melting point, low volatility, low vapor pressure, excellent vacuum, mechanical, and electrical properties, and excellent emission characteristics. A typical accelerating voltage in a FIB instrument ranges from 1 to 30 keV. The ion column consists of two lenses; the condenser lens and the objective lens. A series of apertures defines the probe size and provides a range of ion currents typically on the order of 10 pA to 30 nA. The functionalities such as beam deflection, alignment, and stigmation correction are mostly performed using cylindrical octopole lenses. A special kind of FIB system is dual-beam FIB instrument, which allows sample preparation, imaging, and analysis to be accomplished in one tool. The dual beam, which consists of ion beam and the electron beam provides flexibility in 3D structural analysis. We use this dual beam FIB to prepare our samples for TEM imaging.
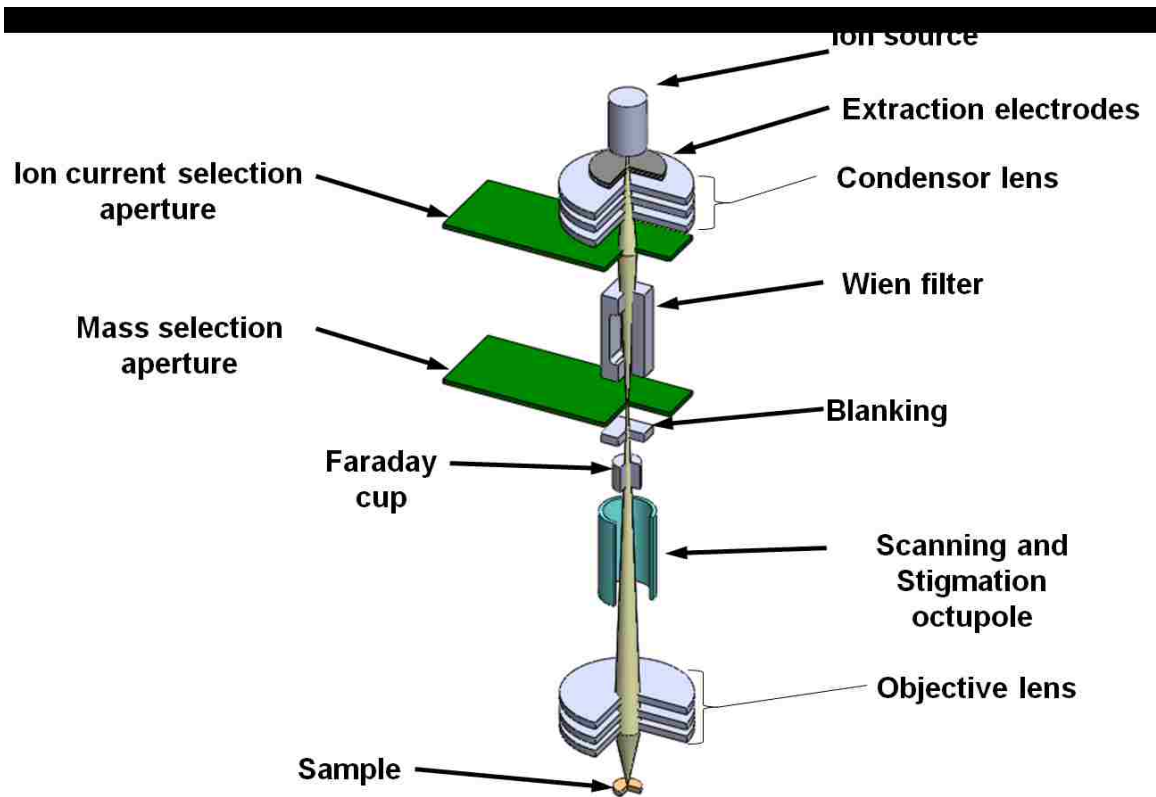
Figure 3.5: A 3D cut-out view of focused ion beam instrument.

3.5   Transmission Electron Microscopy:

Transmission electron microscope, also known as TEM, is a microscope uses electron as a source to see a very small sample in a very high resolution with magnitudes of nanometers. The TEM allows us to image lattice fringes of crystalline sample. There are various modes in which a TEM instrument can be operated, such as dark and bright field imaging mode, phase contrast mode etc. The TEM instrument uses electrons as a source because electron has a shorter wavelength, and with shorted wavelength corresponds to higher resolution. The beam of electrons goes through a very thin sample, and generates a shadow image of the sample with high resolution. Figure 3.6 shows a cut-out 3D view of TEM instrument. The first component

of the TEM instrument is a electron gun, that shoots electrons to the column of a TEM instrument. The instrument is always operated under vacuum to avoid any systematic fault. The beam of electrons first hit the first condenser lens that determines the size of the range of electrons that hits the sample. After that the beam goes through a second condenser lens that controls the size of the spot on the sample.
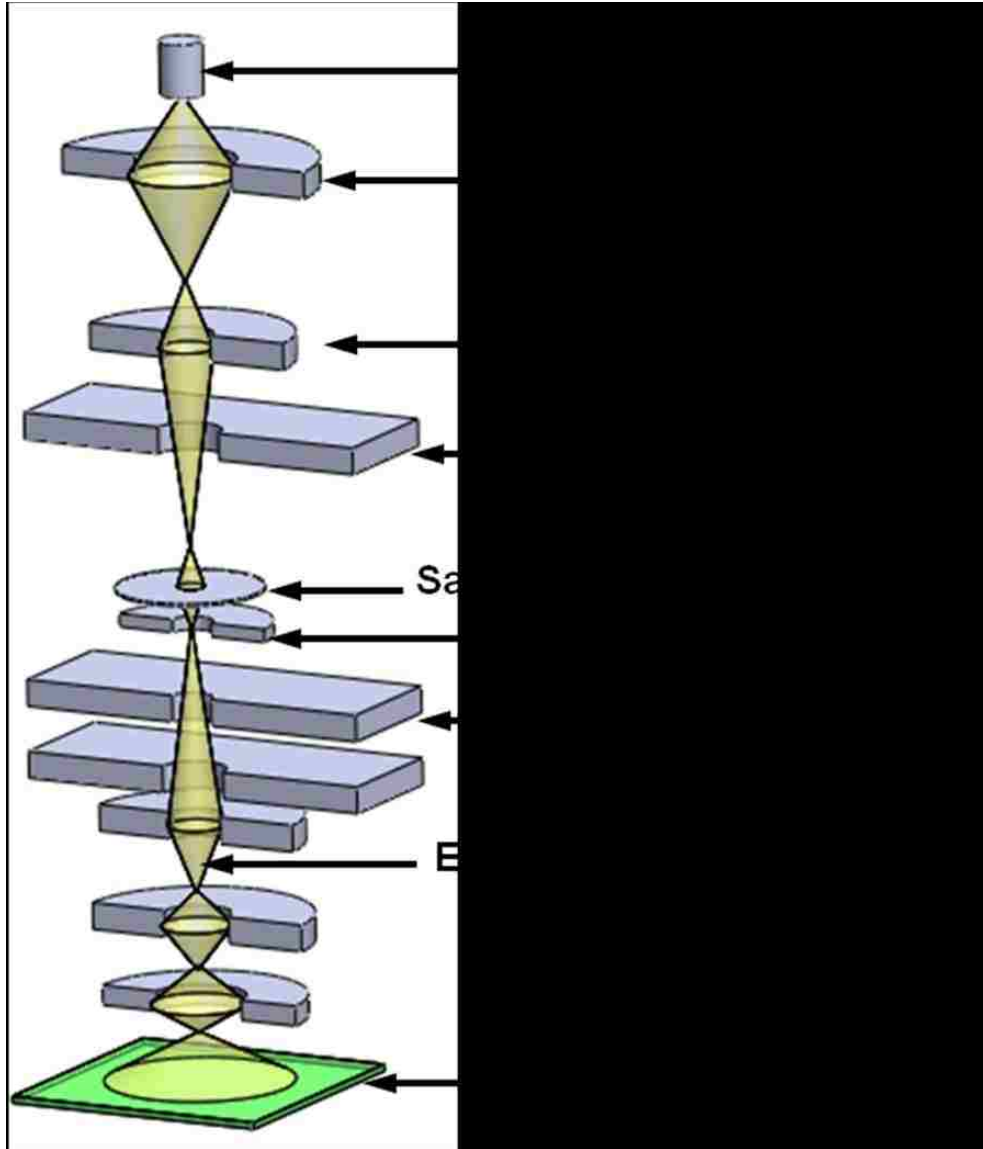
Figure 3.6: A 3D cut-out view of transmission electron microscope instrument.

The condenser aperture blocks stray electrons that do not goes through the TEM column. Basically, the beam width of electron beam is controlled through condenser aperture. After that the beam hits the sample, which is placed on the sample holder. The first thing that happens when a beam hits the sample is scattering from the surface of sample. There are two processes involve with scattering: elastic scattering, and inelastic scattering. However, part of the beam that does not scatter by the sample transmits through the sample. The first component that those transmitted electrons see is objective aperture. The aperture basically filters out the scattered electrons that are not needed for imaging. The transmitted beam now goes through an objective lens followed by projective lens, and hits the fluorescent phosphor screen at the bottom of the instrument. Once the electrons hit the screen it generates a dark and bright image of the sample on the screen.

TEM offers several advantages over other microscopy tools. The TEM provides most powerful magnification. The TEM allows us to obtain high quality and detailed image of a sample. Also, TEM provides qualitative information of the sample such as elements or structural information of the sample. However, there are few disadvantages. First, TEM is very large and expensive equipment. Usually, the sample preparation is very long, tedious, and complicated process because it may include such as dehydration, sputtering, and coating of non-conductive materials, cryofixation etc.

3.6   Energy Dispersive Spectroscopy

Various types of scattering and reflection occur once a primary beam of electrons irradiate a sample surface. Various types include backscattered electrons, secondary electrons, and auger electrons are generated during this process.

Beside these processes, another process also occurs where x-rays are generated within the sample due to inelastic scattering by electrons with the sample surface. Figure 3.7 shows a schematic of energy dispersive microscopy (EDS) technique. Using EDS, these x-rays are collected into a Si-Li drift detector. The detector typically converts the x-rays into an electronic signal. The depth in the sample from which these x-rays are usually generated ranges from 1 to 3 µm. The numbers of x-rays that reach to the detector totally influence the accuracy and detectability of this method. A higher resolution can be obtained through this method with shorter probe size. However, with shorter probe size, the current also becomes smaller. A large collection time window is necessary to obtain sufficient amount of x-rays with this smaller current. In contrast, larger current can sometime burn out the sample, and defeats the purpose. In EDS, the optimum probe size and numbers of count are usually 1 nm and 10000, respectively. With optimized probe size, and counting, the detection limit of EDS can be as small as 1 atomic percent.
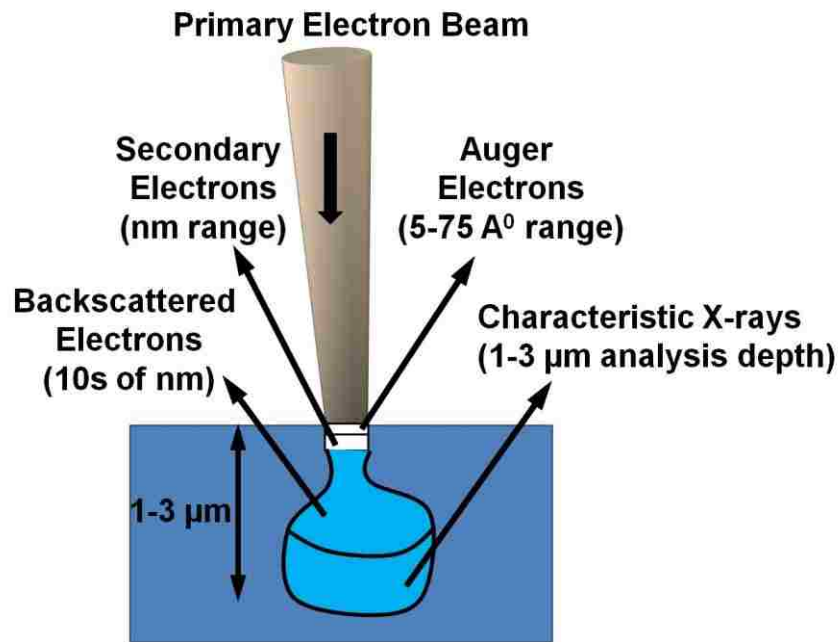
Figure 3.7: A schematic of energy dispersive microscopy technique.

3.7   Secondary Ion Mass Spectroscopy:

Secondary ion mass spectrometry (SIMS) focuses on secondary ions that are being emitted from the surface of the sample as well as the mass analysis of the charged particles. SIMS belongs to a group of analytical method known as ion spectroscopic techniques. Instrument such as SIMS produces ions, and separate those ions according to their mass and charge ratio. SIMS is the most highly developed method in compared to other existing instrumentation method. SIMS has two main uses: in material science, and in surface science. SIMS contains three sub-analytical methods, such as static SIMS, dynamic SIMS, and imaging SIMS. Each one of these sub-analytical method has a high effectiveness for observing trace elements, isotopes, and atomic monolayers. Now, lets take a look how can SIMS be used? Secondary ion mass spectrometry has two main uses: first, to obtain spatial and depth resolution depending upon which sub-analytical method that we use; second, we can compose both organic and inorganic solids usually within the outer region of the sample. The data that can be obtained include mass specs, ion images, depth profiling, 3D imaging of ions. The theory behind SIMS is very simple. The sample is prepared under vacuum, and a primary ion beam irradiates the surface with the energy levels between 3 to 20 keV. High energy levels produced by the beam can have either a positive or negative charge. Bombardment of primary ions produces monoatomic and polyatomic particles. The production of these particles is known as sputtering. Figure 3.8 shows a schematic of SIMS method. The components that are being shown in the figure include a primary ion beam, generated positive and negative ions known as secondary ions, electrons, mass analyzer, and detector. The secondary ions are analyzed using a mass analyzer, and then being sent to

detector which produces analytical information such as mass spectrum, depth profiling, ion imaging etc. The analytical signal arises from primary ions passing energy to target atoms on the surface. Later, energized atoms recoil (collide) with more atoms in a cascading process. As a result, the sputtered material comes off the sample surface.
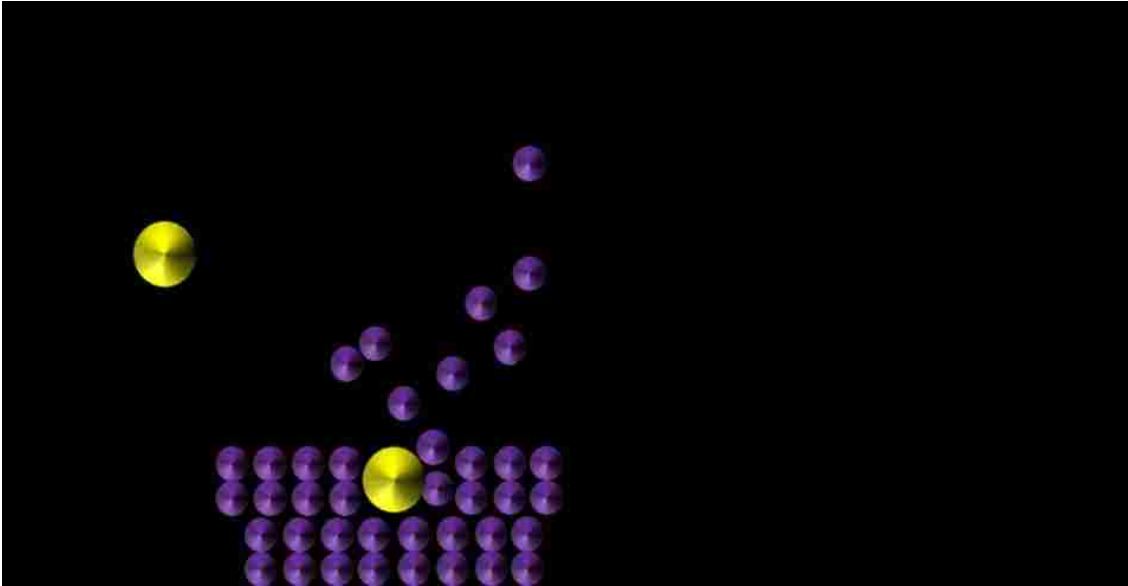
Figure 3.7: A schematic diagram of secondary ion mass spectrometry method. The primary ion beam is shown in yellow, and secondary ions are shown in purple. Postive and negative ions and electrons are being produced during this process.

3.8   Etch Pit Density:

Etch pit density (EPD) measurement technique is a kind of crystallographic etching method that is often used to evaluate total dislocation densities in bulk or heteroepitaxial semiconductors. The total density of etch pits on the surface usually correspond to total threading dislocation density (TDD) of the heteroepitaxial layer. When a heteroepitaxial layer is subjected to etching regent such as HF, the etch rate around dislocations can be reduced or enhanced. Because of the difference in etch

rate in dislocations compared to rest area in heteroepitaxial layer, hillocks or pits form around dislocation. These pits can be easily identified under SEM imaging mode, and aerial density of EPD can be calculated. Most commonly investigated etch pits are threading dislocations, stacking faults etc. To obtain better understanding regarding defects, however, it is extremely important to investigate those defects using a traditional technique such as TEM.
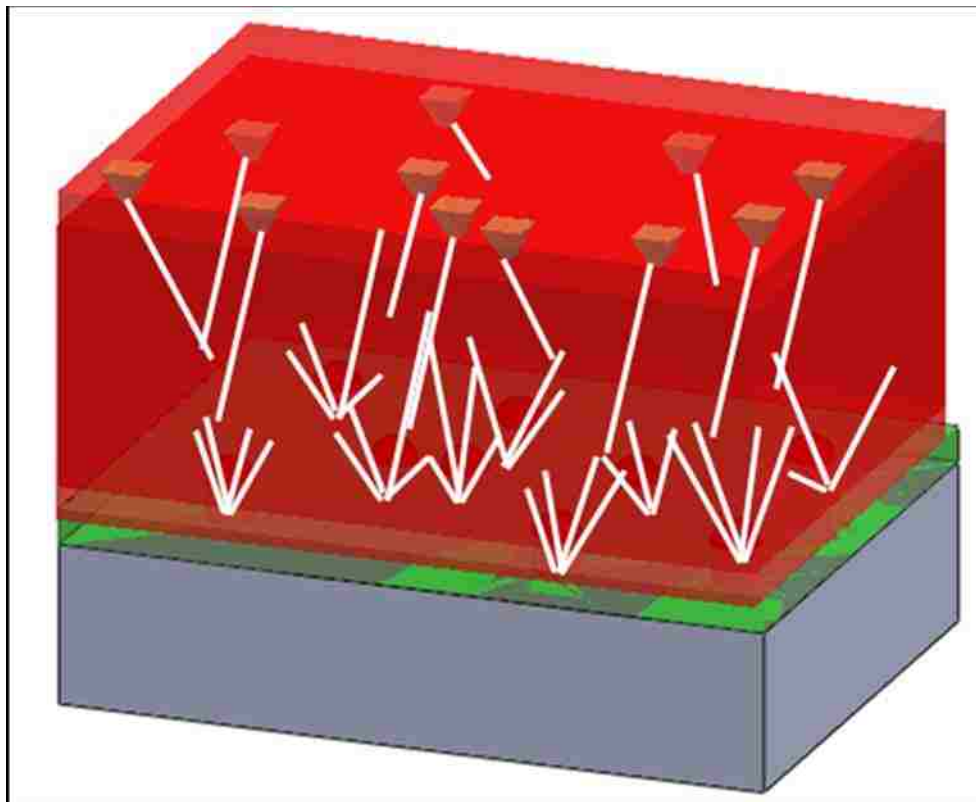
Figure 3.8: A 3D view of heteroepitaxial layer involving etch pits. These pits correspond to threading defects or stressed region in the epitaxial layer. EPD allows us to count the density of threading dislocation in a large area.

3.9   Photoluminescence:

Photoluminescence (PL) spectroscopy is a technique to probe electronic structures of materials. This technique is contactless and nondestructive. PL

measurements at different temperatures or different wavelengths or different intensities allow us to obtain a very detailed information about the electronic materials. The PL intensity and spectrum are strong functions of various important properties of the material. First, the spectral distribution of PL can provide information regarding the bandgap of the electronic material. The spectral width of PL is a strong function of composition of the electronic material. Second, PL spectrum also allows us to probe impurity levels and defects types in the electronic material. Usually, PL spectrums at low sample temperatures (e.g 10K, 4K etc) can provide wealth of information regarding the spectral peaks associated to impurities. In this manner, PL enables us to detect if the impurities in the material have been doped intentionally or unintentionally. Third, the quality of PL spectrum is directly associated to recombination centers. There are two types of recombination centers in electronic materials: radiative and non-radiative. The distinguishable PL peaks allow us to determine the nature of recombination centers in the electronic material at a certain wavelength.

3.10   Interferometric Lithography:

Interferometric lithography (IL) is a patterning technique that uses constructive and destructive interferences to generate periodic arrays of feature sizes. It is being projected by industry that less than 20 nm of feature size can be attained using IL technique. Figure 3.9 shows 3D view of the IL set-up. The IL components involve a coherent ultra-violet light source that emits laser with a certain wavelength such as 355 nm. The laser beam passes through series of beam expander and pin hole. A portion of laser beam gets reflected by mirror and then hits the sample surface, whereas, the other

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portion of laser beam directly falls onto sample surface. An interference pattern is created owing to the interference between reflected and unreflected parts of the beam. This interference pattern ultimately gets translated onto a photoresist (PR) film that is being spun on the surface of the sample. The interference changes the solubility of PR, and results to a periodic patterning on PR. The IL allows us to obtain various types of periodic features ranging from lines to squares to dots. The feature size and interdistance between features are strong function of wavelength, intensity, and angle of exposure of incmoming light beam. The relationship can be expressed by,

$$d = \frac{\lambda_0}{2 \sin \theta} \qquad (3\text{-}3)$$

where d is the pitch of the feature, λ_0 is the wavelength of the light source, and θ is the angle of reflection from the plane mirror.
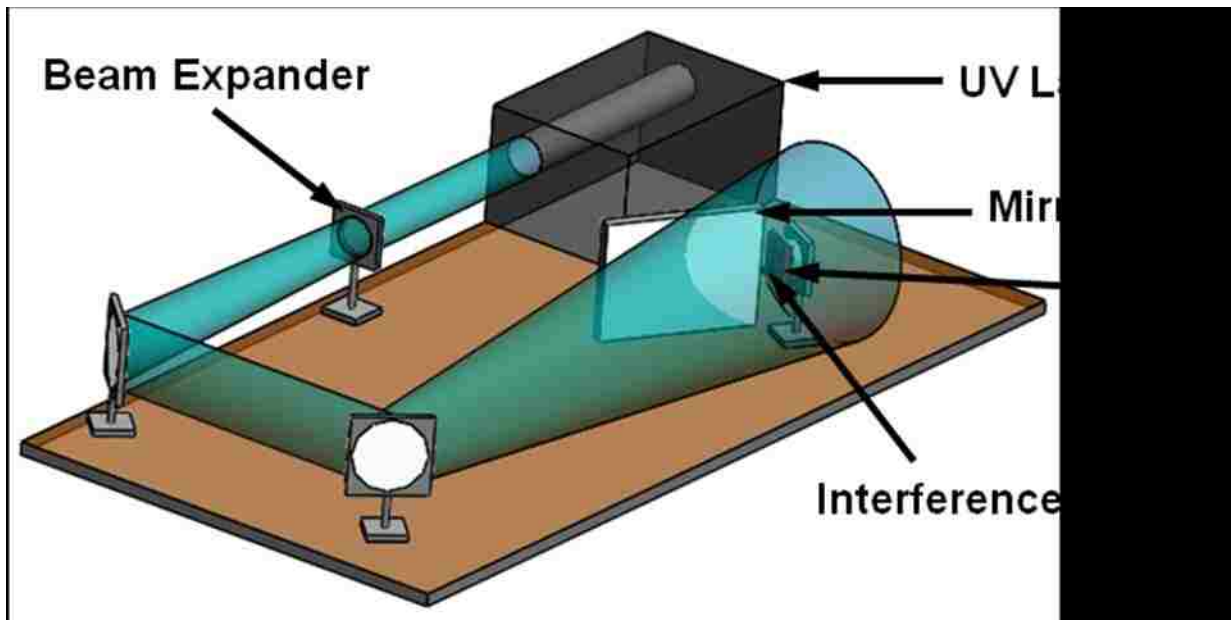
Figure 3.9: A 3D view of the interferometric lithography experimental setup and operating principle.

Carrier Transport Characterizations:

3.11   Hall Measurement:

In this section, we are going to discuss a phenomenon known as Hall Effect. In order to understand Hall Effect we have to recall following principle. An electric charge moving through a magnetic field that electric charge will feel a force as a result of that magnetic field. Figure 3.10 (a) shows a sheet of material in which the Hall Effect is present. Suppose an electron is moving from right to left through the conductor, shown in fig. 3.10. Now the conductor lies in a magnetic field B, which is pointed upward with respect to the plane of the conductor. The electron experiences a magnetic force because of this magnetic field, and the direction of this magnetic force is determined by right hand rule. The magnetic force will cause the electrons to travel closer to one side than the other. This will create a negative charge on one side and positive charge on the other side, shown in fig. 3.10 (b).
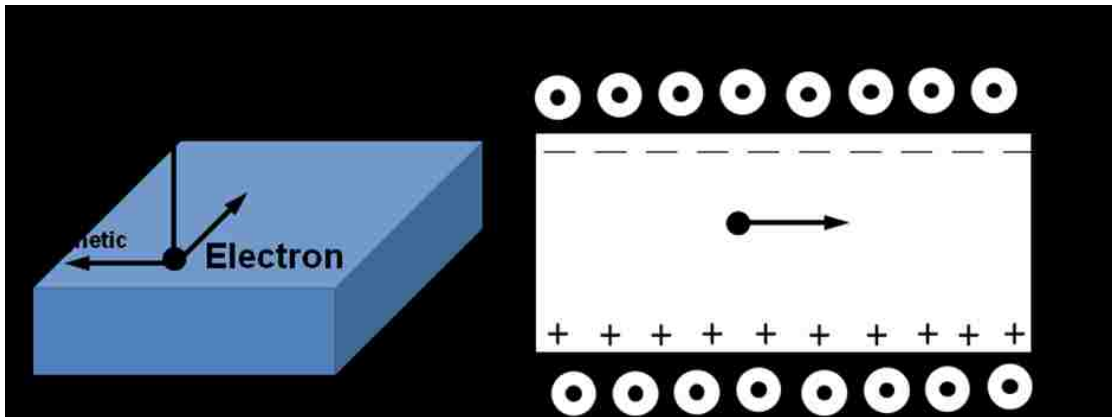
Figure 3.10: (a) A moving electron on the conductor that experiences a magnetic field B. (b) A separation of charges occur because of the moving electrons under magnetic force. A Hall voltage is generated because of this effect.

This separation of charge will create a voltage difference which is known as Hall emf. This voltage builds up until the electric field produces an electric force on charge that is

equal and opposite to the magnetic force. This effect is known as the Hall Effect. The derivation for the Hall voltage is given in the following,

$$F_{magnetic}=F_{electric} \Rightarrow qV_DB=qE_H$$
$$\Rightarrow E_H=V_DB$$
Since
$$V=Ed$$
$$\Rightarrow V_H=\varepsilon_H=E_Hd=V_DBd$$
$$\Rightarrow \varepsilon_H=V_DBd=Hall\ emf$$

(3-4)

where $B=$ magnetic field, $V_D=$ drift velocity, and $E_H=$ hall electric field, and $d=$ width of the conductor.

3.12   Capacitance-Voltage Measurements:

In this section, we are going to discuss about the experimental method of capacitance-voltage (C-V) characteristics MOS devices.   This C-V characteristic is a fast and reliable method in the determination of electronic quality of MOS devices. One of such reliable and accurate way of measuring C-V characteristic of a MOS device is split C-V method. Figure 3.11 shows an experimental set-up for the C-V characteristic.   The experimental setup includes a computer controlled   system of instruments designed to make quasistatic and high-frequency (1 MHz) C-V measurements on MOS capacitors. The C-V set-up includes a a Keithley 595 quasistatic C-V Meter for low-frequency C-V measurements and Keithley 590 C-V analyzer for high frequency C-V measurements. The set-up also includes Keithley 230 programmable voltage Source to apply voltage and Keithley 5951 remote input coupler to control the communication between the instruments and the computer. The communication between the computer

and instruments are achieved through general purpose interface bus (GPIB). A Software

package is used in order to control the instruments, and also for data collection and
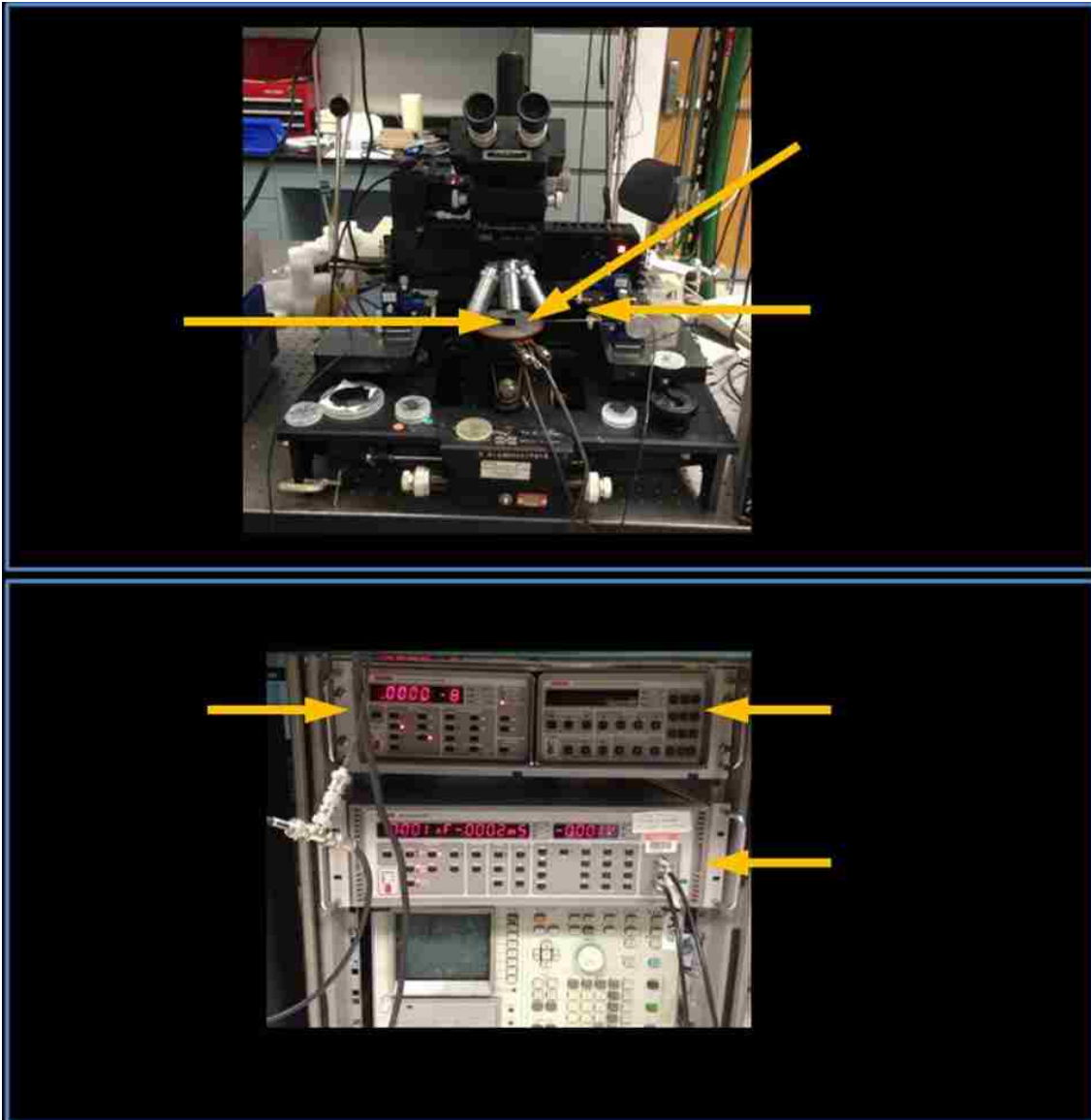
Figure 3.11: An experimental set-up of capacitance-voltage measurement system.

acquisition. Once the instruments are properly placed in a way the measurement should

take place, a C-V measurement is performed on a MOS device. The C-V measurement

on MOS devices provide information on the dielectric constant of gate dielectric, doping

concentration and flat band voltage values of the semiconductor. The doping concentration and flat band voltage are determined from the high frequency C-V curves. The C-V characteristic also can provide information regarding the effective oxide charge density, and the density of interface defect states (D_{it}). The interface defect states are calculated based on the results obtained from quasistatic and high-frequency measurements.

3.13 Current-Voltage Measurements:

A current-voltage (I-$V)$ measurement is a task to obtain current vs. voltage or resistance characteristics of a device. This is a fundamental characteristic for various devices such as transistors. To perform I-V measurement, it is usually required to combine many instruments such as voltage source, current source, current meter, switch, voltmeter, device under test (DUT) etc. Two different types of I-V measurements are performed using the set-up, such as forward I-V and transfer I-V characteristics. In forward I-V measurement, a drain-to-source (I_{ds}) current is measured as a function of drain-to-source (V_{ds}) voltage, keeping gate-to-source (V_{gs}) voltage fixed. In contrary, during transfer I-V measurement, a drain-to-source (I_{ds}) current is measured as a function of gate-to-source (V_{gs}) voltage, keeping drain-to-source (V_{ds}) voltage fixed. Figure 3.12 shows a schematic of the I-V measurement set-up, and corresponding ports for V_{ds}, V_{gs}, and I_{ds} are also shown in this figure.

A proper care has to be taken during I-V measurements such as keeping the DUT and all the cables are in a dark and noise free environment. This will allow us to measure a low-magnitude of current. For this type of sensitive and low

current measurement, we have used tri-axial cable which has capability to compensate the charging of cable. For accurate measurements, we have performed all of these I-V measurements in a probe station. The probe station consists of four probes which are capable of handling tri-axial cable. The probe station includes a chuck, which is connected to a heater to provide the capability of temperature dependent measurement. The complete setup is enclosed by a shielded metal cabinet which is connected to vacuum pumps. Using this type of cabinet, we obtain isolation from the outside acoustic noise, light and all other kind of disturbance while measurements are going on.
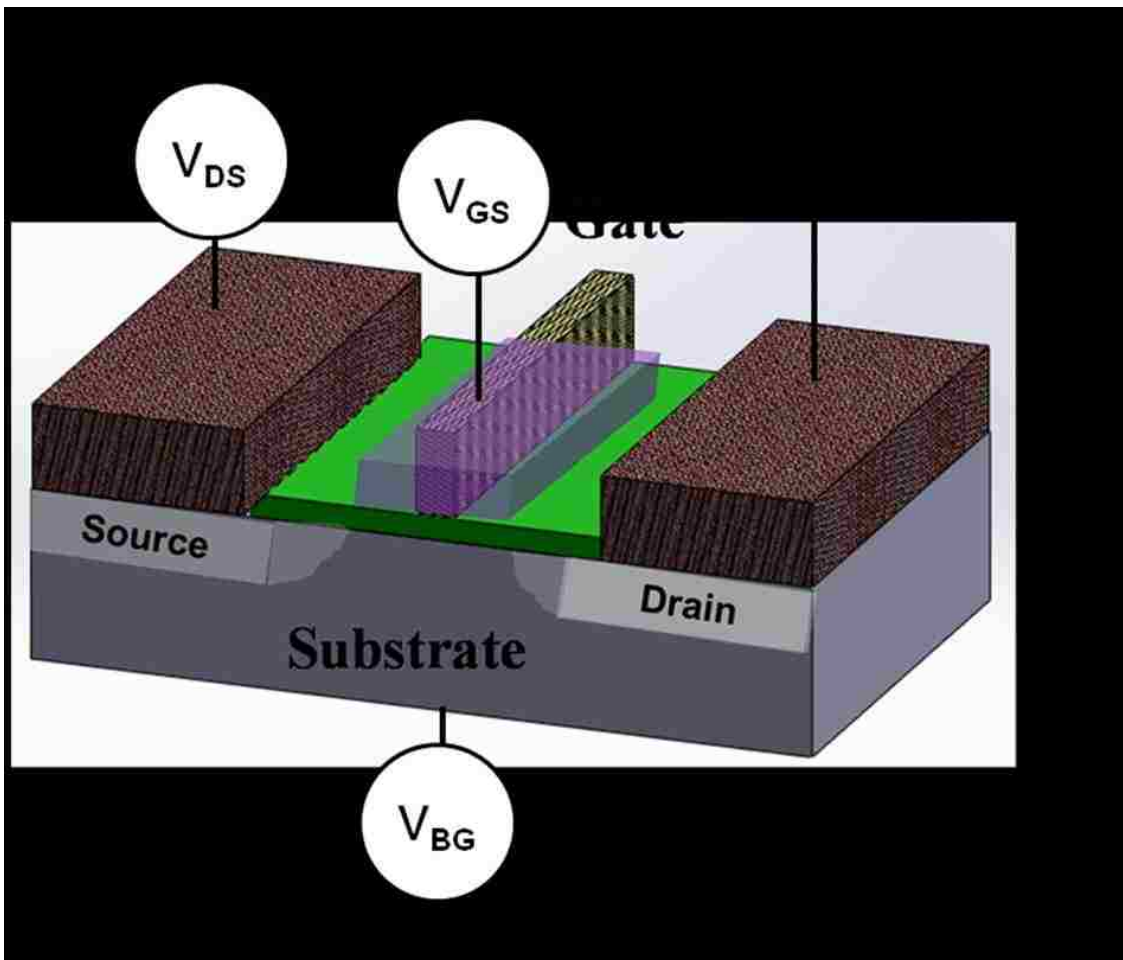
Figure 3.12: Schematic of electrical characterization of a field effect transistor device. Four probes are used, one for back gate, one for top gate and other two for source and drain contacts.

CHAPTER 4 Ultra-Low-Dislocation-Density, Wafer-Scale, Epitaxial Ge-on-Si

4.1   Introduction and Background

Chapter 1 of this dissertation has discussed about the theory of nanoheteroepitaxy and its potential as a growth method for very-low-dislocation density film of GoS. The growth method that we have developed to improve the GoS film quality is based on the nucleation of Ge islands in the nanoscale opening in a thin layer of chemically grown SiO_2 layer followed by successive coalescence of Ge islands over the layer of SiO_2. These nanoscale openings in SiO_2 layer particularly depend on the Ge flux and the temperature of the substrate heater. Based on this parameters, the density of opening that form in the SiO_2 layer can range from 10^{10} to 10^{11} cm^{-2}. Once these openings form, the selective growth of Ge starts when Ge islands selectively nucleate within the openings, and anchor to underlying Si substrate. Upon further growth via impingement of Ge flux onto Si substrate, a continuous film of Ge starts to form over the remaining SiO_2 template. The modified growth process that is developed in our lab, however, requires a thermal annealing step before Ge islands coalesce over the SiO_2 template. This step is intended for stacking faults (SFs) removal from Ge layer. To further eliminate dislocations that stem at the Ge-Si interface, we make use of dislocation locking mechanism by dopant impurities, coupled with artificially introduced oxygen. This modified growth technique leads to a ultra-low-dislocation-density (ULDD) film of GoS.

Our modified growth technique based on nanoheteroepitaxy follows two specific requirements: first, Ge island diameter should be less than 10 nm, and second, Ge islands should be spaced by more than 3 nm apart [94]. Interestingly enough, a well optimized process of Ge nucleation through nanometer-sized openings in

chemical SiO_2 takes care of these specific requirements that allow us to grow a ULDD film of GoS.

4.2   Experimental Details

Germanium is grown by molecular beam epitaxy (MBE). Details of the growth parameters including flux and substrate heater calibration are described elsewhere [89]. Si(100) substrates used in this study have a resistivity approximately in the range of 1-10 Ω-cm. The Si substrates are cleaned and chemically oxidized for 5 min in a Piranha bath consisting of 3 volumetric parts of H_2SO_4 (96 wt %) and 1 part of H_2O_2 (30 wt %) and heated to 373 K. The samples are subsequently dipped into a buffered oxide etch solution (20 parts 40 wt% NH_4F: 1 part 49 wt% HF) diluted in deionized (DI) water by 6:1 volumetric ratio to remove the chemical oxide. The chemical oxidation is then repeated, and the wafer is rinsed in DI water and blown dry with N_2. The final chemical oxidation step results in a SiO_2 layer of 1.4 nm thickness [89]. After being loaded into the deposition chamber, the samples are degassed at 873 K for 10 min. The effusion cell temperature is set at 1393 K to produce a flux of 7.6 x10^{13} atoms/ cm^2-s (7.6 ML/min) and allowed to stabilize for 30 min before the shutter is opened for deposition. The pressure in the growth chamber remains below 2 x 10^{-8} Pa during the deposition period.

By varying the deposition conditions and number of thermal annealing cycles, we have produced four different samples with different TDDs (Samples A – D). For Sample A, a 5-nm-equivalent amount of Ge is initially deposited, using the touchdown technique. We define the equivalent amount as the thickness of a continuous Ge film that would have resulted if Ge uniformly covered the substrate surface without

forming 3D islands. After the initial growth and while the shutter remains closed, the substrate temperature is raised to 1123 K for 30 min in order to remove stacking faults (SFs) and dislocations from partially coalesced Ge islands [123]. The substrate temperature is then reduced to 873 K and allowed to stabilize for 10 min before the shutter is opened for further deposition at 7.6 ML/min. This second phase of the growth starts with depositing a 100-nm-equivalent amount of Ge. Then, the effusion cell temperature is set at 1473 K to produce an increased flux of 5.1×10^{14} atoms/cm^2-s (51 ML/min) until the final thickness of the film is approximately 1 µm. This film is then annealed at 1073 K for 30 min.

Ge/SiO$_2$ template/Si samples are polished using a Logitech PM5 lapping/polishing machine on a Logitech Chemcloth polishing pad. The polishing solution consists of 50 parts DI water and 1 part 30 wt% H$_2$O$_2$. Afterward, the wafers are rinsed in DI water and cleaned for 10 min in a capacitively coupled plasma reactor operating at 250 watts and 1 Torr with 30 sccm O$_2$ flow rate.

Sample is characterized using etch pit density (EPD) and X-ray diffraction (XRD). For etch pit density measurements, the samples are immersed for 2 min in an etch solution that consists of 2 volumetric parts of 49 wt % HF and 1 part of 0.1 M K$_2$Cr$_2$O$_7$. The revealed etch pits are then imaged by an FEI Quanta 3D scanning electron microscope (SEM) operating at 15 keV for the electron beam energy. Our previous work, using plan-view transmission electron microscopy (TEM), shows that EPD measurements quantitatively represent the dislocation density in the Ge film [89]. The XRD technique is used to qualitatively determine the crystallinity of Ge films. We use a Phillips MRD X-ray diffractometer equipped with Cu K_α line at 0.154 nm. This line

provides sufficient resolution to measure the interatomic distances of Ge epilayer. We use the full width at half maximum (FWHM) of (004) and (331) diffraction peaks as an indicator of Ge film crystallinity and defect level.

4.3   Growth Results and Discussion

There are three main steps associated to our modified growth scheme for GoS. They are as follows: selective growth of Ge in nanoscale openings in chemical SiO_2, SF removal by annealing Ge islands, and dislocation locking by oxide precipitates and impurities. In next few sections of this chapter, we will discuss each one of these steps in detail.

4.3.1   Selective Growth of Ge in Nanoscale Openings in Chemical SiO_2

The first step of our growth process is to grow Ge selectively in the nanoscale openings in chemical SiO_2 layer. A sizeable body of work [124-132] has been performed to understand the mechanism, which creates openings in the oxide and allows epitaxial Ge island formation. Unfortunately, this mechanism is not completely understood. Several research groups have performed extensive studies on decomposition of SiO_2 in the presence of a Ge [124, 126, 133, 134, 135] or Si [127, 133, 136] atom flux, or other metal impurities (e.g., Au, Ag, Cu, W, Ni, Pt, Ti, Mg, Al) [137,138]. The outcome of their research leads to a conclusion that decomposition of SiO_2 occurs faster and at lower temperatures with the presence of flux than in their absence. Figure 4.1 shows that the temperature for decomposition reduces with Ge impingement for different SiO_2 thicknesses. The data in this figure is an accumulation of data taken from several studies, [124-132] including the study performed by our group(▲). Figure (4.1) shows a plot of natural log of SiO_2

thickness as a function of inverse temperature. The calculated activation energy (E_a) obtained from the dashed line (---) and the solid line (—) are ~ 0.7 eV and 0.5 eV , respectively, in the absence and presence of a Ge flux.
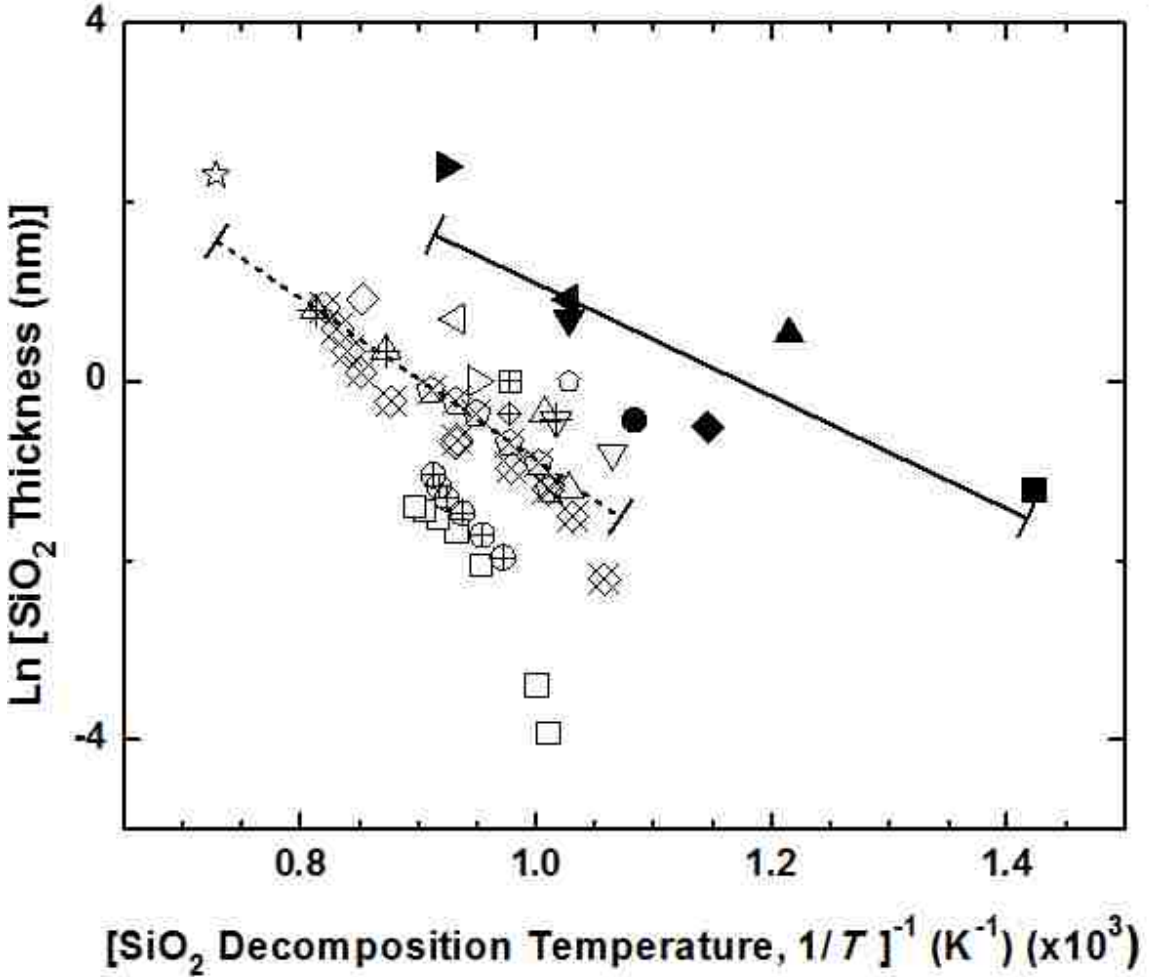
Figure 4.1: Natural log of SiO_2 thickness versus inverse temperature of the SiO_2 decomposition. The broken line is a linear fit to the data without a Ge vapor flux (open symbols). The solid line is a linear fit showing the same trend but shifted to lower temperatures in the presence of a vapor flux of Ge or Si atoms (closed symbols). Data points are referenced as follows: (■);[124](●);[133] (▼);[135] (◄);[127](►);[133](Λ);[126] (∀);[140] (8);[129](X);[134](M)[127] (Ξ);[139] (χ);[132] (ψ);[132](□); [132](⊐);[141] (/); [130](:);[128] (E);[125](O);[132](□);[139]and (Π) [131](taken from PhD thesis of Darin L [95])

Both lines indicate that for a given SiO_2 thickness, the decomposition occurs at lower temperatures in the presence of a Ge flux. We can make two deductions from fig. 4.1.

First, the evidence of decreasing decomposition temperature with the presence of Ge flux strongly suggests that Ge react swith SiO_2 layer. The reaction step can be expressed by,

$$Ge\ (g) + SiO_2\ (s) \rightarrow GeO\ (g) + SiO\ (g) \qquad (4\text{-}1)$$
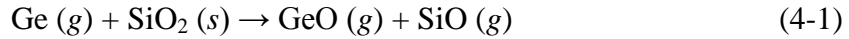
where g refers to gas phase, and s refers to solid phase. The eqn. (4-1) suggests that Ge from the vapor flux can diffuse to and react at defect sites at the SiO_2–Si interface, producing two gas phase species such as GeO and SiO. In fact, adding atomic species of Ge or Si increases the SiO_2 decomposition rate, thus depressing the observed decomposition temperatures shown in fig. 4.1. Basically,this reaction is rate-limiting in nature, and the additional reactant species such as Ge must participate in this reaction. The incorporation of Ge increases the reaction rate. We speculate that adding the Ge or Si flux is equivalent to the formation of Si monomers in reaction, and the main cause behind in increasing reaction rate and lower decomposition temperature.

This speculation is in agreement with the findings of Johnson *et al.*[142] Second, fig. 4.1 also shows an exponential dependence of decomposition temperature as a function of oxide thickness, both with and without an external Si or Ge flux. We speculate that the exponential dependence stems from a change in reactivity at the SiO_2-Si interface with varying oxide thickness. Various studies [143] have done to understand this mechanism in regards to the change in reactivity. Engstrom *et al.*[144] and others[145,146] have reported that a transition layer exists at SiO_2-Si interface, and contains suboxides (i.e., Si^{+1}, Si^{+2}, and Si^{+3}). They also have shown that the concentration of suboxiedes relative to Si^{+4} decreases with oxide thickness and increasing oxidation temperatures. These studies suggest that the oxide at the SiO_2-Si interface becomes more stable with both increasing thickness and oxidation temperature. These observations lead to conclusion that a

optimal thickness of SiO_2 is required to have selective growth. For instance, Both Yun [147]and Winkenwerder [148] reported no decomposition of 10 nm thick SiO_2 in the presence of Ge flux at 810 °C and 700 °C, respectively, and Li *et al.*[85] observed no decomposition for 6 nm thick SiO_2 at 700 °C. We speculate that Ge adatoms have to spend enough time diffusing in with increasing and more stable SiO_2, independent of decomposition temeprature. This leads to conclusion that [84] a short Ge adatom lifetimes (~16 ns at 700 °C) on the SiO_2 surface before Ge desorption playa an important role for opening nanoscale window in SiO_2 layer.

Herein, fig. 4.2 shows acomplete process flow from void nucleation to right before island coalescence. Image 4.2 (a) shows the SiO_2 layer (green) that is chemically grown on Si substrate. Image 4.2 (b) shows the processes occurring to Ge adatoms impinging on SiO_2 layer, and nanoscale openings at the Si-SiO_2 interface. Images 4.2 (c) shows the nucleation of Ge adatoms (red) through the nanoscale voids at the Si-SiO_2 interface. Figure 4.2 (c) also shows few diagonal line running through the Ge islands, which represents a stacking fault and will be discussed further in a later section. This whole process is dubbed as "touchdown" method.
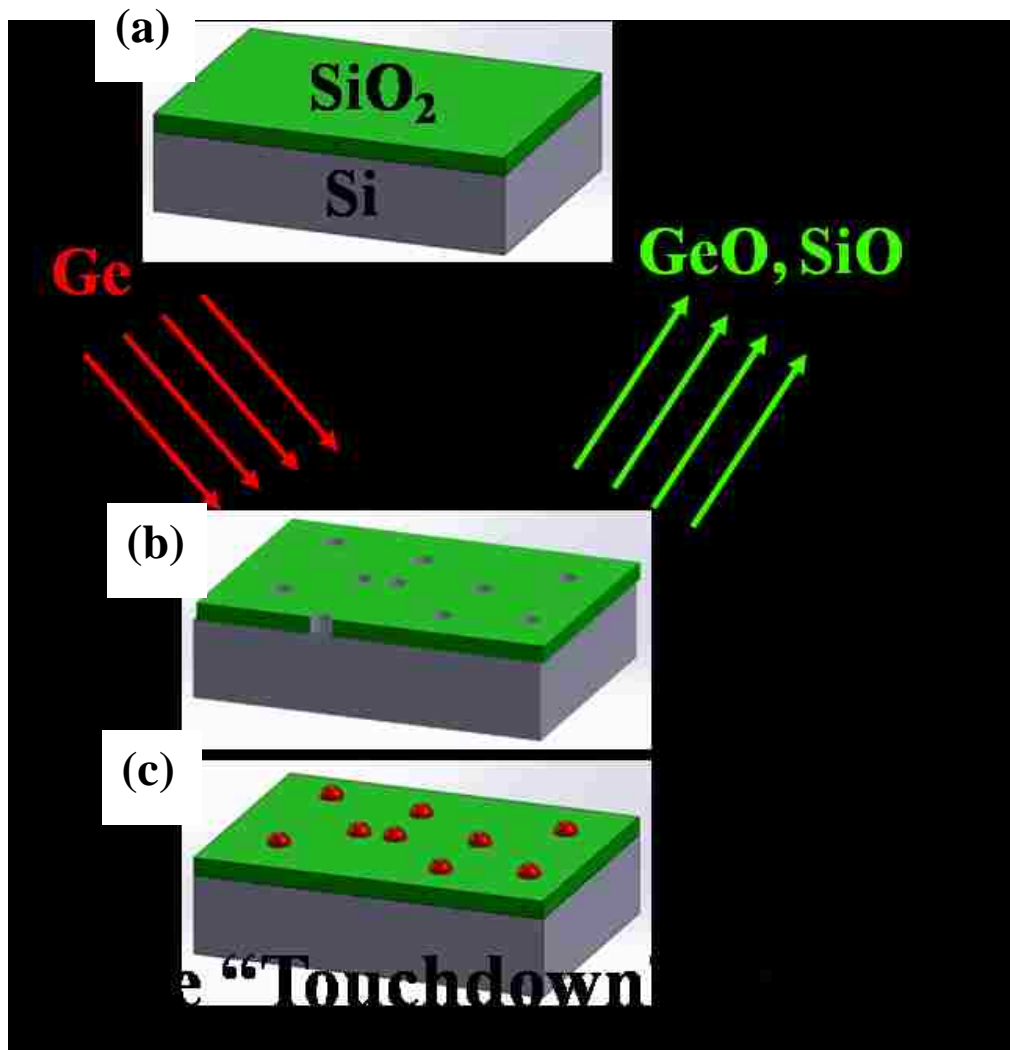
Figure 4.2: A schematic illustrating the process from void nucleation and growth to Ge island formation. Shown in 4.2(a) is a surface of Si substrate with chemically grown oxide on it. Images in 4.2(b) show the process of void formation in the Si-SiO$_2$ interface toward the SiO$_2$ surface. In 4.2(c), Ge selectively nucleates and grows on the newly exposed Si within the void openings

Figure 4.3 shows a cross-sectional TEM image of nanoscale openings in SiO$_2$ layer that is

formed via touchdown method. The thickness of chmically grown SiO$_2$ layer using the

100 °C Piranha solution is 1.4 nm.
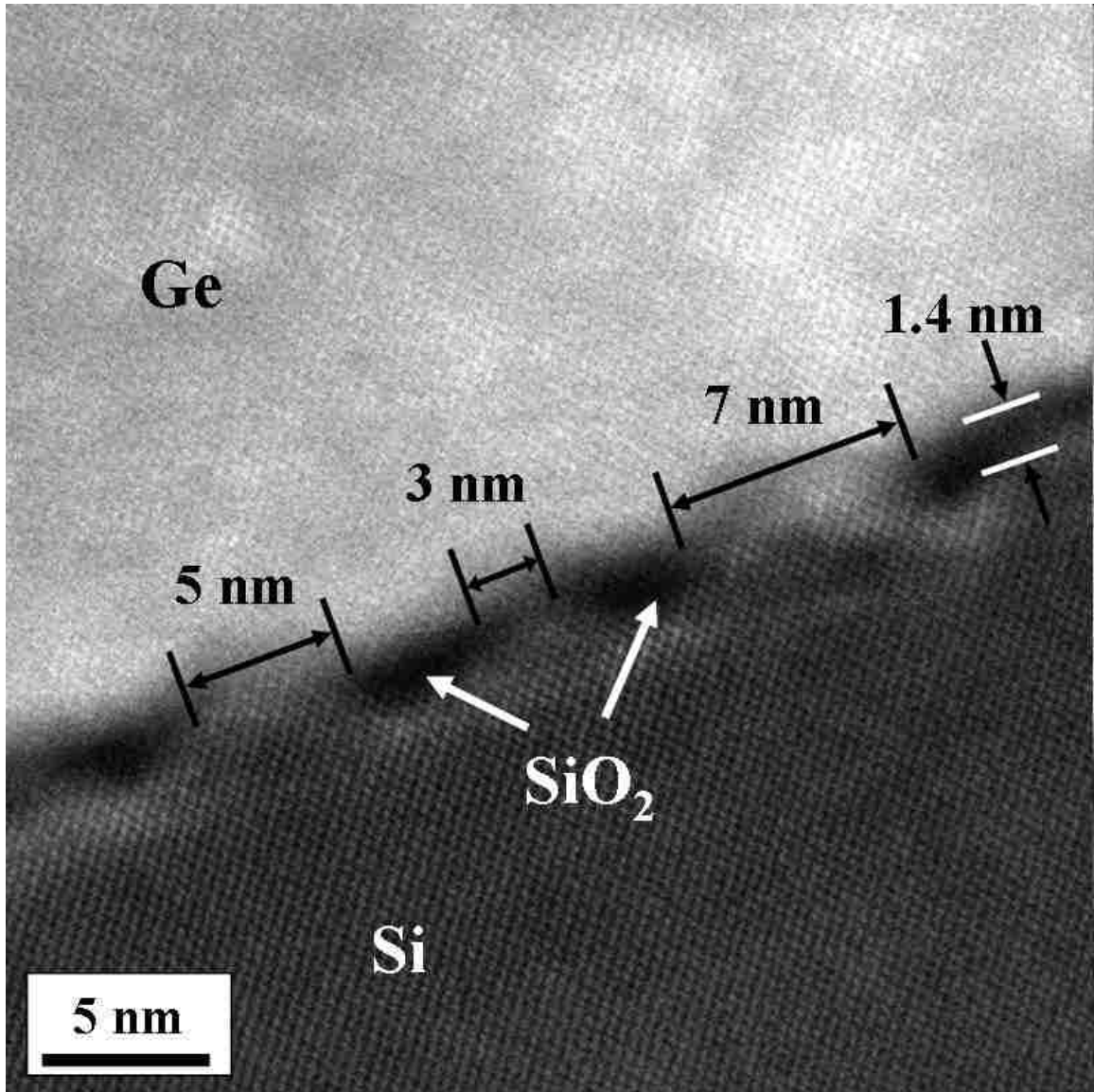
Figure 4.3: High resolution cross-sectional transmission electron micrograph showing the Ge/SiO$_2$/Si interface. Voids of 3 to 7 nm in diameter are created in the SiO$_2$ where Ge subsequently nucleates and grows as islands (taken from PhD thesis of Darin L [95]).

This figure also shows few nanoscale islands of Ge that exist at the the Ge-Si interface.

To understand the mechanism of touchdown method, we let those Ge islands coalesce in

this particular experiment. As a result, this figure shows a thin layer of Ge on top of Si

substrate instead of only islands of Ge. Based on STEM, which provides elemental

contrast based on atomic weight, Ge appears brighter and Si appears darker. The STEM

image shows the high density of 3 to 7 nm wide openings in the SiO_2. This figure also reveals the lattice fringes of Ge, which is in epitaxial registry at the heterojunction within the oxide openings. This "touchdown" method enables us to grow epitaxial layer of Ge on Si substrate on a 2-inch-diameter wafer-scale.

Figure 4.4 (a-b) show bight-field TEM images along the [110] zone axis of Ge directly grown on Si and Ge grown on the oxidized Si using "touchdown" method. Figure 4.4 (a) shows that direct growth of Ge on Si produces a high density of TDs in the Ge film. In contrst, fig. 4.4 (b) shows that the Ge grown on the oxidized Si using "touchdown" scheme has almost very few TDs, however, the Ge film mostly contains SFs or twins. We estimate that the density of SFs that reach to the film surface is approximately$5x10^7$ cm^{-2} . We speculate that SFs form due to translation mismatch between the islands[149,150]. The translation mismatch occurs for two reasons, they are: first, the inter-distance between islands may not be an integer multiple of lattice spacing, causing mismatch; second, these islands that are anchored to Si substrate may exist in a twist relationship from ach other. Therefore, a SF or a threading dislocation may form during coalescence of Ge islands on Si substrate. A detailed study on SFs formation, and twin relationship is provided in the next section.
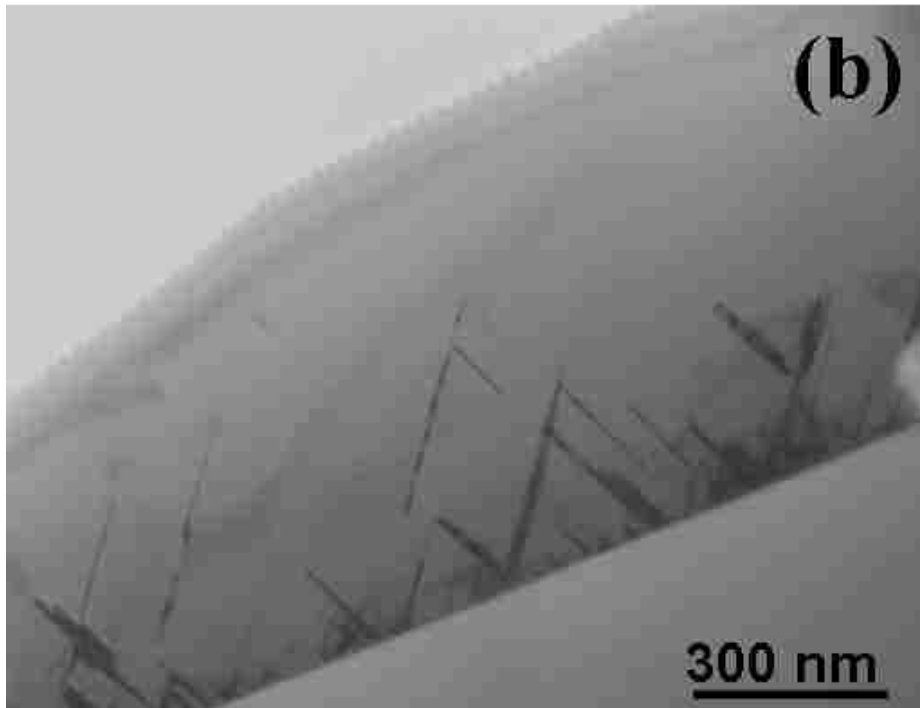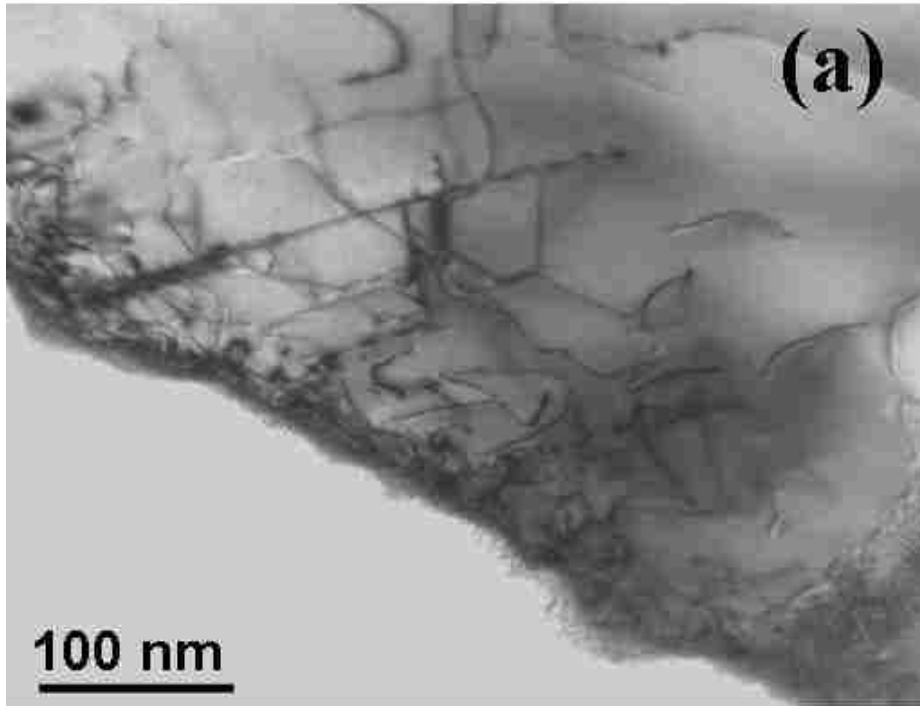
Figure 4.4: Low-resolution transmission electron micrographs, 4.4(a) Ge grown directly on on Si substrate leading to a large density of threading dislocations, and 4.4(b) Ge grown on chemically oxidized Si substrate through touchdown method and having a large density of stacking faults, many of which terminate within 200 nm of the interface (taken from PhD thesis of Darin L [95]).

4.3.2 Mechanism of Stacking Fault Removal by Annealing Ge Islands

The significance of selective growth through nanoscale openings of SiO_2 is described in details in the previous section. We note that the desnity of TDs reduces siginificantly in the Ge film that is grown via "touchdown" methods compared to the Ge film that is grown directly on Si. However, the Ge film that is grown via "touchdown" method tends to show SFs in the order of $5x10^7$ cm^{-2} . We speculate that this SFs form because of coalescence Ge islands in the presence of chemical oxides. In this section, we will try to understand in details why those SFs from in the Ge films. Also, we will discuss about the method of removing these SFs from Ge film. These SFs or twins can form in the Ge film by few possible mechanisms. One possible mechanism by which these twin form is that when randomly nucleated Ge islands on top of SiO_2 coalescence with another Ge islands that nucleated epitaxially within openings in the oxide. Previous research from our group has shown that this mechanism is not the best one to describe the possible reason behind the formation of SFs. The details are given in this literatures [84,86] . Based on the conclusion from this literature, we can thererefore negelect the possible mechanism, which states that twins are not likely to result from random Ge island nucleation on top of the SiO_2 layer.

In contrst, the other possible mechanism states that these SFs form because majority of these Ge islands are in a tilted orientation from one another while they nucleate within openings in the SiO_2 layer. We start this discussion by showing an x-TEM image of an individual island, shown in fig. 4.5. This sample is chosen for our study because these Ge islands are on the verge of coalescence. The x-TEM sample is oriented in the direction along [110] zone axis in order for viewing the lattice fringes of

Ge islands. Figure 4.5 (a) shows the lattice fringes and corresponding fourier

transformed diffractioin patterns (insets) of these islands. This figure shows that the left

Ge island is epitaxially registerd to Si substrate, whereas the right island is tilted at 70.5°

counter-clockwise about the [110] direction with respect to the Si substrate. As a result,

these two islands are presently in a twin relationship to the Si. The direct consequence of

this type of twin relationship is the formation of coherent twin boundary upon

coalescence. A magnified view of filtered Fourier image of the twin boundary is shown

in the inset of fig. 4.5 (a). Figure 4.5 (b) shows a schematic model of the two Ge islands

on the Si. The atomic arrangement in the left island is perfectly registered to Si substrate.

In comparison, the atomic arrangement in the right island is in a twin relationship to the

Si substrate. The boundary between the Si and Ge island that lies in the (100) plane is

termed as incoherent twin boundary. This type of twin boundary is commonly observed

during heterogenous nucleation. A coherent twin boundary forms at the merging

interface of two Ge islands, and captured in the structural model. The SFs or twins in the

Ge film mostly from because of coalescence of Ge islands that are in a twin relationship

with one another.
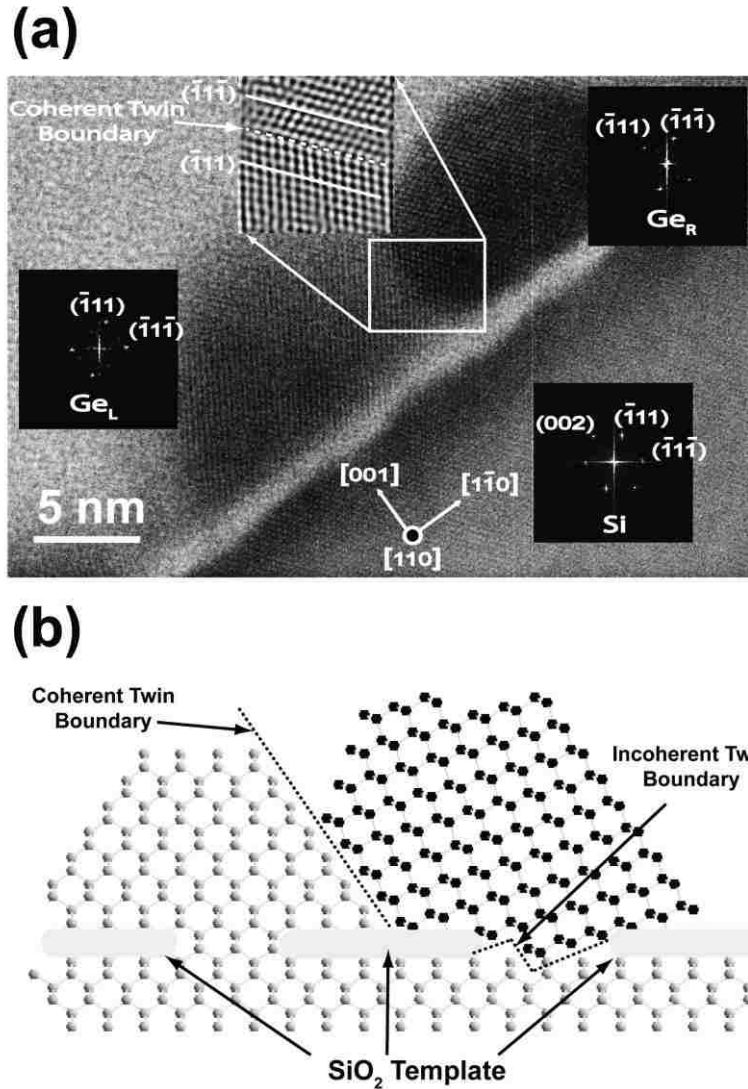
Figure 4.5: (a) a high-resolution cross-sectional transmission electron microscope image of 12-nm of Ge deposited on Si substrate sample, where the Ge islands have just started to coalescence. A Ge island which is nucleated in a twin relationship to the underlying Si, shown in the right. This has led to a coherent twin boundary at the junction with the epitaxial Ge island on the left. The magnified filtered image of twin boundary is shown in the inset. The diffraction patterns of the islands and substrate are also included as insets. (b) a schematic illustrating a coherent and incoherent twin boundary (taken from PhD thesis of Darin L[95]).

We observe that a significant amount of SFs exist in the Ge film

that is grown via "touchdown" method. The most efficient way of removing these SFs is

to anneal the Ge islands before coalescence begins. Herein, we show a plot of four

different Ge islands samples, where three sample are annealed at different temperatures, and one sample is unannealed. The thermal annealing is performed for 30 minutes. Figure 4.6 shows that the XRD FWHM of the (004) narrows with increasing annealing temperature of Ge film. The Ge film that is annealed at 1073K has a FWHM that is 0.4 times as compared to unannealed films. Also, The FWHM of the (331) reflection (not shown) decreases even further, by a factor of 3.3. Based on (004) and (331) results, we can conclude that thermal annealing step is required to remove SFs from the Ge film.
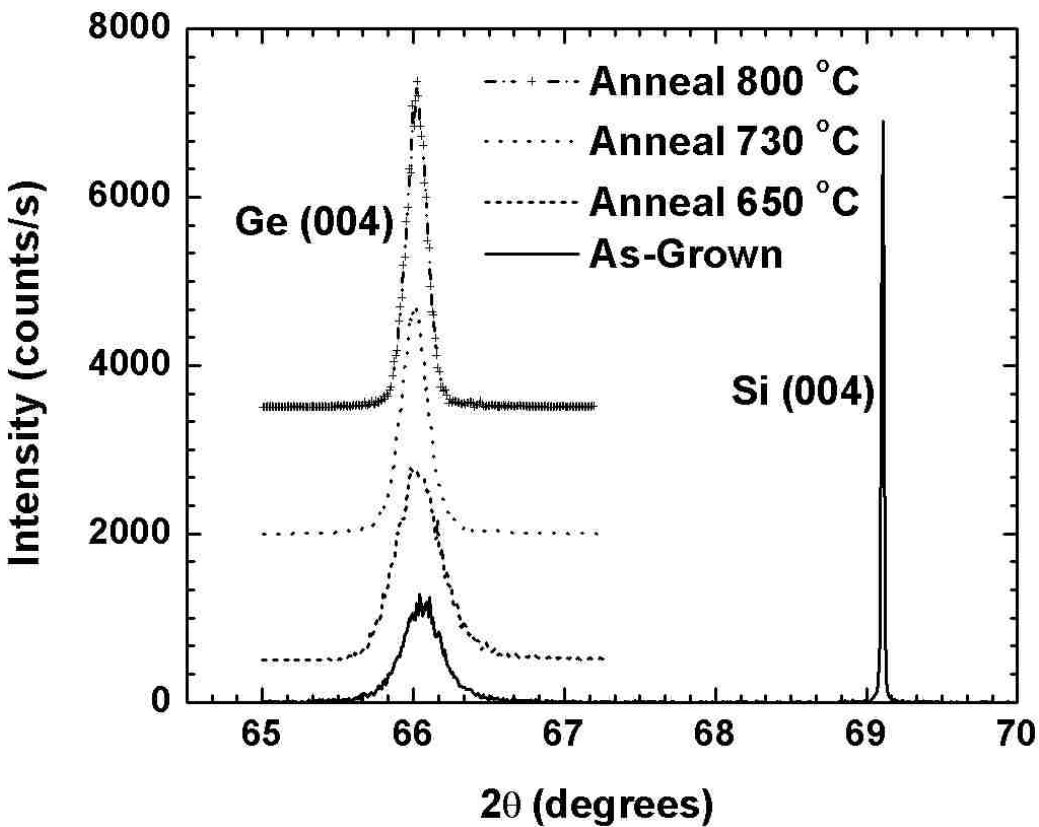
Figure 4.6: The x-ray diffraction peaks of the (004) reflection of Ge films that are (bottom to top) unannealed (solid line), annealed at 923 (dotted line), 1003 (dashed line), and 1073 K (dot-dashed line) (taken from PhD thesis of Darin L [95]).

We have determined the origin of the high density of twin/SF defects found in Ge films created from the nucleation and coalescence of Ge islands

within small openings in SiO_2. The twins originate from the nucleation of Ge islands in twin relationships to the Si within the SiO_2 windows, and form coherent twin boundaries when merging with other Ge islands that are epitaxial to the Si. In addition to the twin oriented Ge islands, many of the Ge islands nucleate with a small misorientation angle to the Si. Annealing the Ge islands leads to the desorption of the SiO_2, and the transfer of most of the Ge in the islands to the freshly exposed Si. Intermixing then leads to the formation of a strain relaxed GeSi alloy layer, and subsequent growth results in Ge films free of twins. Dissolution of most of the Ge islands appears to be the mechanism by which twins are removed. This is confirmed by the experiments in which the initially deposited Ge islands are first capped with SOG before annealing to prevent surface diffusion and SiO_2 desorption. Subsequent analysis after annealing reveals that the twin/SF defects remain in the islands, and the islands retain their overall shape and orientation prior to annealing.

In addition, some very large Ge islands are formed after annealing samples that have a critical amount of initial Ge deposition. The formation of theses large islands is not currently well understood, but the mechanism of their formation may be analogous to the shape transitions observed in pyramid-dome-superdome formations observed in Ge-Si epitaxy. The large islands found after annealing are oriented to the Si and contain threading dislocations, in agreement with the findings of Ge-Si growth directly on Si, whereby large islands form after the nucleation of dislocations relaxes the strain buildup from the lattice mismatch. Next, we report the characterization of Ge films formed from additional growth performed after annealing Ge islands nucleated within nanoscale windows inSiO_2.

4.3.3   Mechanism of Dislocation Locking by Impurities and Oxide Precipitates

We have seen so far that TDs and SFs are originated during epitaxial growth of GoS. Implementing growth method such as "touchdown" makes use of nanoheteroepitaxy technique to trap most of the threading decfects that originate at the Ge-Si interface. Also, in our modified growth method, we thermally anneal the Ge islands just before their coalescence. The TEM images qualitatively show the effectiveness of "touchdown" technique and thermal annealing step in Ge layer. The modified growth technique is promising, although, we observe that siginificant density of TDs still exist in the Ge film. In this section, we will describe about a unique approach that has been added in our growth method to reduce the density of threading defects in the Ge film. Building on a unique two-step, simple MBE growth technique, therefore, we have investigated possible dislocation locking mechanisms by dopant impurities, coupled with artificially introduced oxygen. In the case of n-type Ge grown on Si, our materials characterization indicates that the TDD can reach the ultra-low $\sim 10^5$ cm^{-2} level, compared to p-type and undoped Ge on Si (GoS). We investigate n-type GoS using transmission electron microscopy (TEM) and x-ray diffraction (XRD) to support its outstanding crystallinity. We note that our Ge film covers the entire underlying Si substrate at the wafer scale without mesas or limited-area growth.

In this section, we will focus on the use of n-type impurities (phosphorus) diffusing from the Si substrate and the introduction of oxygen at the Ge-Si interface. The oxygen is introduced by growing a thin chemical SiO_2 layer on top of the Si substrate before Ge epitaxy begins. We speculate that the P segregation facilitates dislocation locking at the oxide precipitate/Ge-crystal interface, which is located near to

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the actual Ge-Si interface. Figure 4.7 show a complete process flow of growth that occurs on n-type Si substrate. In contrast, B segregations at the oxide precipitate/Ge-crystal interface is not a stable process, and does not lead to dislocation locking. Figure 4.8 shows a complete process flow of growth that occurs on p-type Si substrate. Figure 4.8 illustrates that the dislocation locking mechanism is absent in Ge growth on p-type Si substrate. We analyze the effectiveness of the oxide precipitates and dopant segregation in filtering TDs in the Ge layer. In addition, we examine the effects of impurities in oxygen diffusion through the Ge layer by performing secondary ion microscopy spectroscopy (SIMS) analysis.

Herein, we presnt the experimental section, which consists of growth, SEM, TEM, XRD results of n-type and p-type Ge films. Ge is grown on n- and p-type Si(100) (resistivity > 1-3 Ω-cm) using MBE. The growth, annealing, and polishing steps are described in detail in experimental method section before.   We characterize the Ge film quality, using XRD and etch pit density (EPD).   The full-width-at-half-maximum (FWHM) of XRD diffraction peaks is used to qualitatively determine the crystallinity of Ge films. Figures 4.9 (a-b) show the Ge(004), Si(004), and Ge(331) peaks for n- and p-type GoS substrates. FWHM of Ge(004) peak is 100 and 300 arcsec for n- and p-type Ge, suggesting high level of crystallinity. The FWHM values of Ge(004) and Ge(331) peaks for n-type are narrower by 0.3 and 0.38 of than that of p-type, indicating the pronounced crystal quality of n-type than p-type. The Ge(331) FWHM particularly points to a considerable reduction in stacking faults for n-type compared to p-type. Figures 1(a)–(b) (inset) show a SEM images (25 μm $\times$ 25 μm) of etch pits created on n- and p-GoS samples.
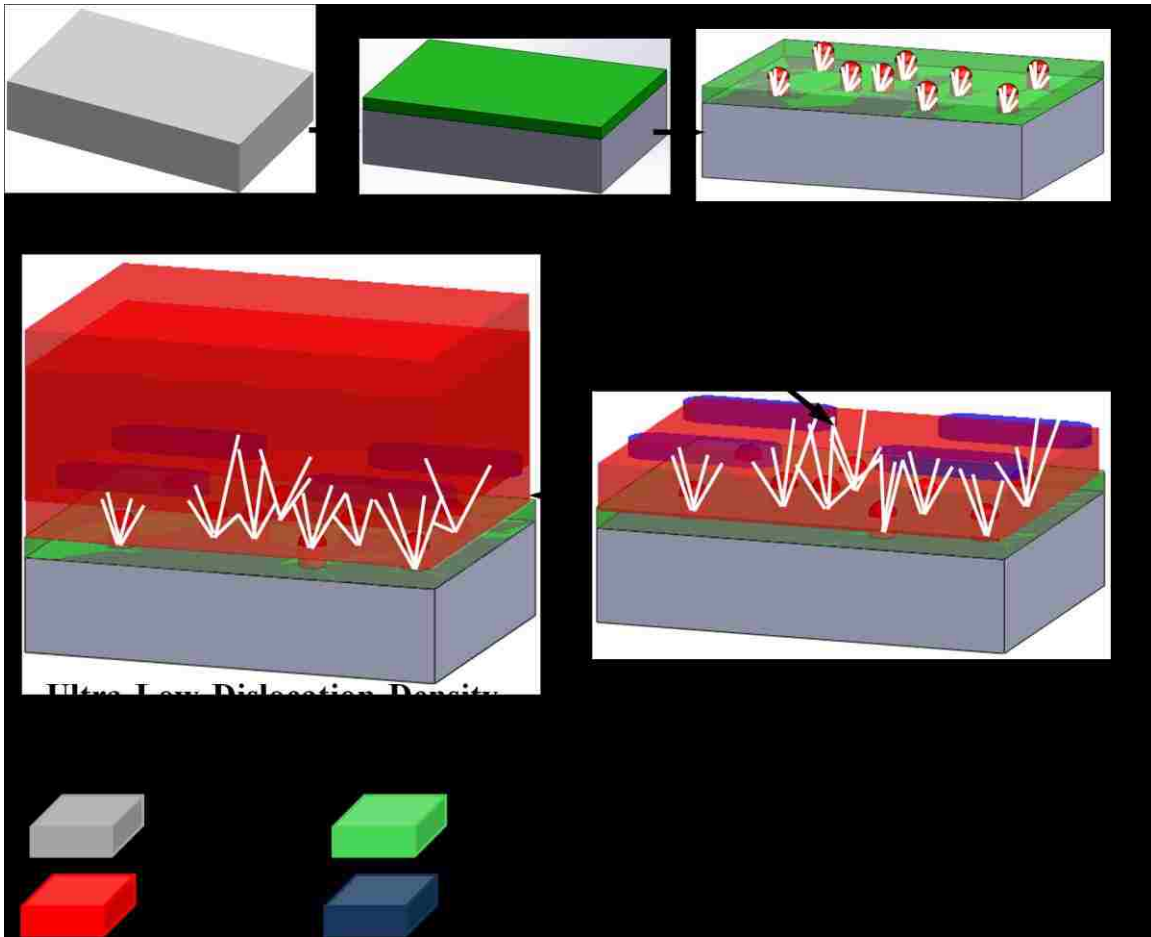
Figure 4.7: Dislocation locking by oxide precipitates and phosphorus impurities in Ge growth on n-type Si susbtarte**.** The precipitate blocks are shown by dark blue colors. The final Ge film surface shows no defects.

These etch pits reveal TDDs of 1×10^5, 5×10^7 cm^{-2}, respectively.

We statistically estimate on EPD based on the results from 5 wafers of each dopant type

and 4 different areas on each wafer. Our previous work, using plan-view TEM, shows

that EPD measurements quantitatively represent the dislocation density in the Ge film [89].
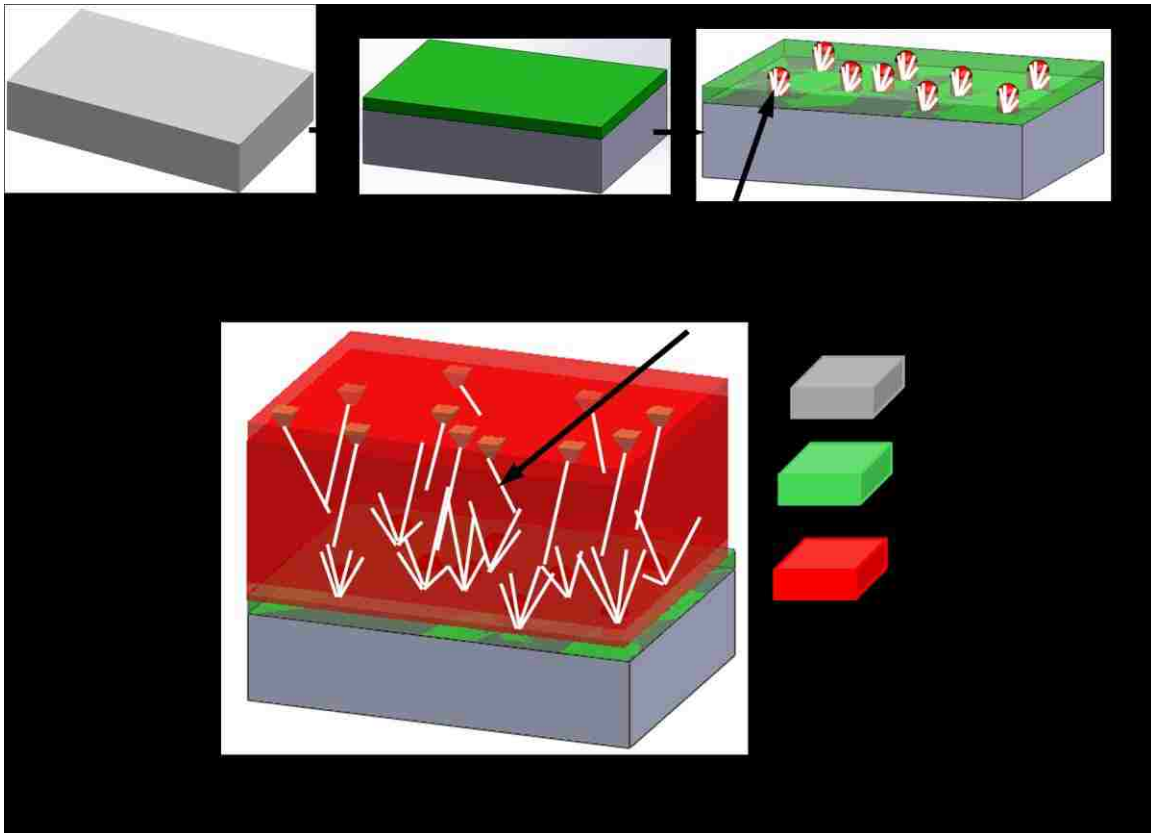
Figure 4.8: No Dislocation locking by oxide precipitates and born impurities in Ge growth on p-type Si substarte. The precipitates are missing in this growth process. The dark cross mark on the schematic represents that this particular step is missing from the entire growth process. The final Ge film surface show a significant density of threading defects.

The Figure 4.10 shows a high-resolution TEM (HRTEM) image of the n-type GoS. The HRTEM shows few 10-20 nm white platelet shaped features in the vicinity of the Ge-Si interface, and those platelets are positioned along [110] direction, which is along the TEM zone axis. Note that the dimension of this region is on the order of 10 to 20 nm, which is much greater than 5 to 7-nm SiO_2 patches created during our
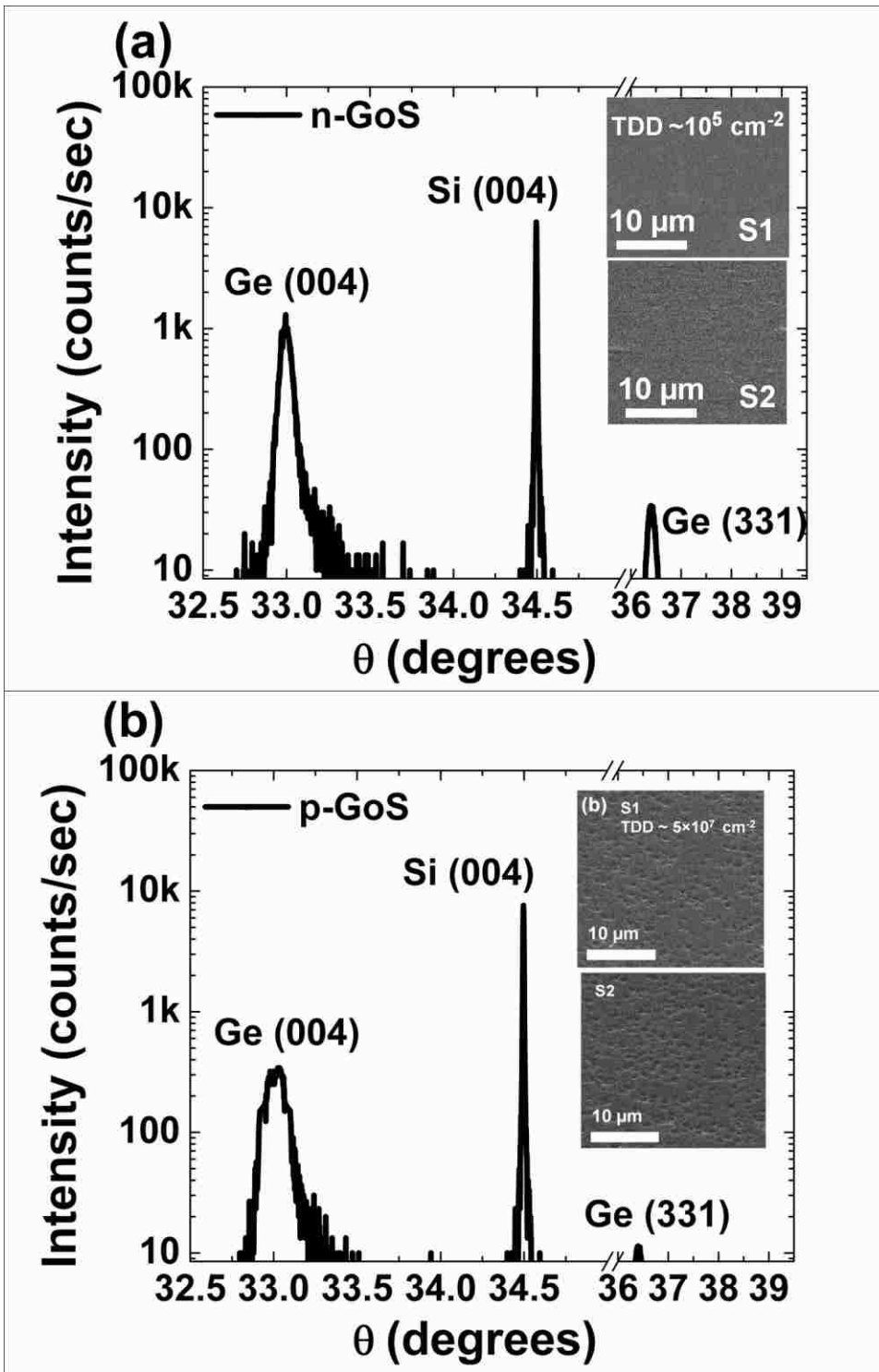
Figure 4.9: (a) XRD intensity of Ge(004), Si(004), and Ge(331) peaks for n-type GoS substrate. (Inset) SEM images of etch pits on n-type surface. (b) XRD intensity of Ge(004), Si(004), and Ge(331) peaks for p-type GoS substrate. (Inset) SEM images of etch pits on p-type surface.

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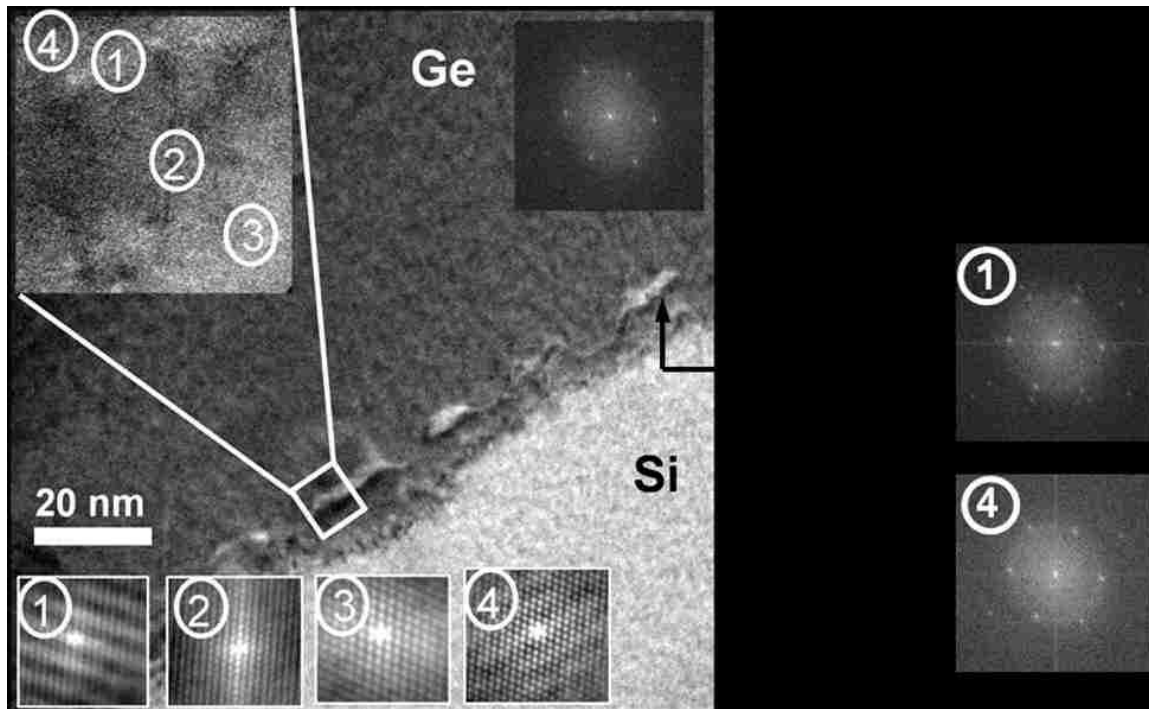
Figure 4.10 : The TEM characterization show TDD on the order of ~ 10^5 cm^{-2}. Oxide precipitates tend to lock dislocations.

typical MBE growth. The fast fourier transform (FFT) pattern of an individual platelet reveals weak spots around periphery, suggests polycrystalline nature of corresponding platelet. The FFT pattern is extracted using digital micrograph software. These weak spots marked inside the dashed circles could only arise from the oxide precipitates that are shaped as platelets. The platelet shaped oxide precipitate formation study has been previously observed on CZ grown Si at the temperature regime of 650-900°C . The growth and subsequent annealing temperatures in our MBE process matches with the temperature range associated to the precipitate formation. The precipitate density in the Ge layer is approximately 8×10^9 cm^{-2}, and this magnitude is on the same order of magnitude of dislocation density, which forms at the Ge-Si interface. Figure 4.10 also

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shows a FFT pattern of relaxed-Ge, the coincidence of the spots indexed (110) in the

cubic crystal phase of Ge supports that the Ge that is located on and around those

precipitates is relaxed. The cross-sectional TEM image reveals that the threading defects

and stacking faults (SFs) are greatly reduced, and the result supports the EPD

measurements, which shows that n-type GoS has cumulative dislocation density of

approximately 10^5 cm^{-2} level. The inset shows a magnified view at and around of a

discrete locked-dislocation region with subsections marked by 1 to 4. The corresponding

spatial auto-correlation images show both long-range ordering as well as lack of ordering,

depending on the subsection. The long-range ordering is absent in subsection 1, likely

due to O precipitation around the dislocations, whereas subsections 2, 3 and 4 show long-

range ordering and high-level crystallinity. Figure 4.11 shows a HRTEM image of the p-

type GoS.
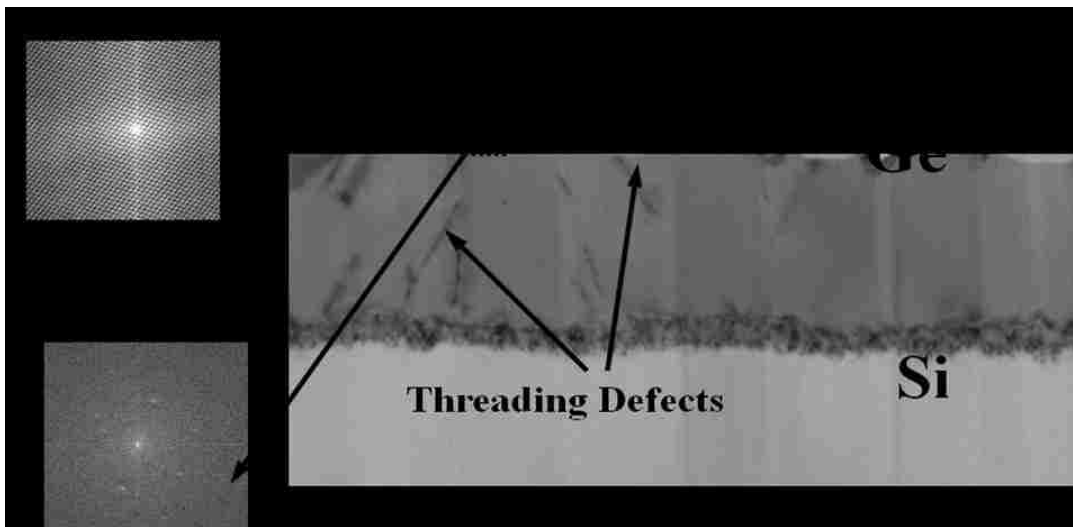
Figure 4.11 : The TEM characterization show TDD on the order of ~ 5x10^7 cm^{-2}. Oxide precipitates is absent in this p-type GoS, and no locking mechanism occurs in this type of growth.

In contrast to n-type, p-type GoS does not have any presence of precipitates at the vicinity of Ge-Si interface. As a result, the threading defects and other dislocation can freely propagate to the Ge surface, and clearly shown in the TEM image. There are no oxide precipitates formed near at the Ge-Si interface. As a result, dislocations don't interact with precipitates or impurities in Ge layer. The direct consequence is that the dislocation locking is totally absent in this growth process. Therefore, the dislocation locking is more pronounced in n-type which facilitates formation of oxide precipitates, terminates threading dislocations propagating from the Ge-Si interface. The dislocation density in n-type Ge is 500 times less than that of p-type Ge. One possible mechanism for the ultra-low dislocation density is that n-type impurities segregate at least 10 times more to oxide precipitate/Ge crystal interface than that of p-type impurities. Hence n-type impurity and oxide precipitates platelets are more easily introduced into Ge layer than p-type impurities. Ultimately, these precipitates that are integrated into Ge crystals lock dislocations.

Based on previous results from TEM images, we notice that precipitates only from in n-type Ge epilayer. Therefore, we will only consider the case for n-type GoS for further study to demonstrate why precipitates form and their implications in dislocation locking mechanism. Figure 4.12 (a) shows a magnified view of an oxide precipitate that forms in a n-type Ge epilayer. Figure 4.12 (b) shows a oxide precipitate that is terminating a defect lines, ans stopping its propagation further. The marked region in this fig. 4.12 (a) shows a single precipitate along [110] direction. Supporting the argument of precipitate formation, the marked region shows fringe due to various phase boundary that exists at the precipitate/Ge crystal interface. The presence of

O particles causes lattice distortions in Ge due to difference of particle size and

crystallographic structure between O precipitates and Ge atoms. We note that the atomic

radius of O is smaller in a Ge lattice leads to a tensile stress. Dislocation defects also

create a compressive stress field due to extra row of atoms that is inserted into the crystal.

These two opposite stresses attract each other, and as a result the O precipitates form at

and around the dislocations. Based on TEM, the
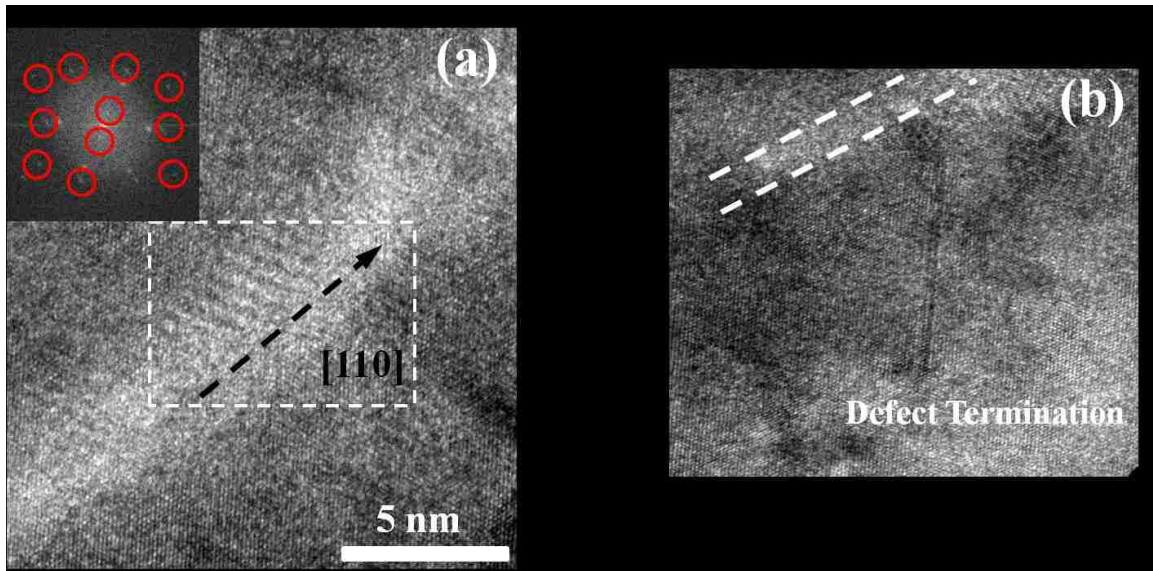
Figure 4.12: (a) A magnified view of a oxide precipitate region in a n-type Ge epilayer.
Inset shows a FFT image of oxide precipitate. Extra set of weak diffraction spots are
observed, that arise from polycrytallinity of oxide precipitate. (b) A magnified view of
oxide precipitate which is terminating a defect lines.

precipitate dimensions are in the order of 10-20 nm, which is larger than the critical

radius (ref) dimension above which dislocation bowing mechanism is favored. The

strength for dislocation bowing can be written as,

$$\tau = \frac{Gb}{L-2r}$$

(4-2)

where τ is material strength, G is the shear modulus, b is the

magnitude of the Burgers vector, L is the distance between pinning points, and r is the

precipitate phase particle radius. Hence, we propose a mechanism where O precipitates, attracted toward dislocation coupled with dislocation bowing facilitates a unique method of locking dislocation. In addition, extra set of weak diffraction spots, shown at the inset of fig. 4.12 (a), can also be used as supporting evidence for oxide precipitate. The estimated percentage of oxide precipitate is .04-.08 vol%, which is calculated from the area of precipitate over the total observed area of the sample, assuming uniform thickness. To estimate the atomic composition of Si, Ge and O at and around the precipitate, we show a series of nano-probe energy dispersive spectroscopy (EDX) images (fig. 4.13 (a-c)) that are taken right at the Ge-Si interface, at the precipitate and at slightly above the precipitate in the Ge epilayer. We notice that the concentration of O is considerable at the interface and precipitates; however, their concentration drops precipitously in the Ge epilayer above the precipitate.
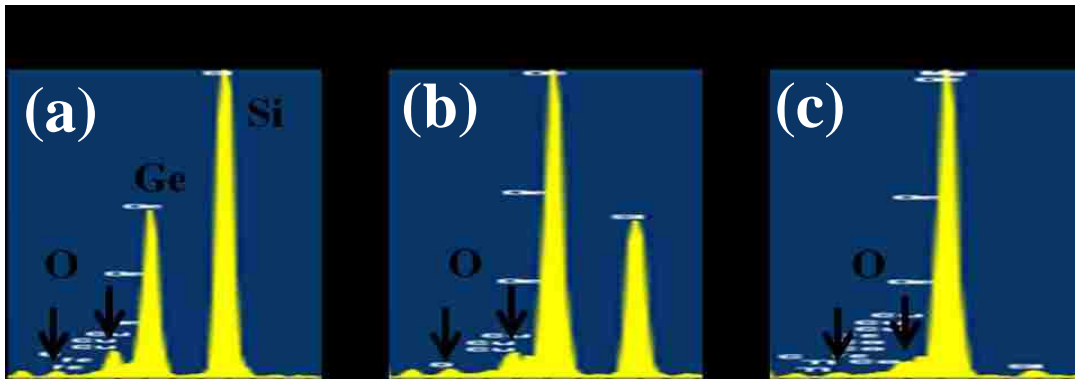
Figure 4.13: A series of nano-probe EDX images, (a) right at Ge-Si interface, (b)at oxide precipitate-Ge-crytsal interface, and (c) at slightly abovethe oxide precipitate.

Building upon the nano-probe EDX and TEM results on oxide precipitates in the n-type Ge epilayer, to strengthen our claim on obtaining ultra-low-dislocation-density Ge film based upon dislocation locking, we propose two coupled mechanism that facilitates dislocation locking. Firstly, we perform SIMS analysis to

show the atomic composition of Si, Ge and O as a function of distance from Ge-Si interface. Figure 4.14 shows SIMS spectrums of n-type and p-type GoS substrates. We note that two distinct peaks of O and a sharp peak of P can be observed in n-type GoS. The first sharp peak of O corresponds to O that can be found in the nano-scale patches of chemical SiO_2 which is located at the Ge-Si interface. The shoulder O peak corresponds to oxide precipitates. The sharp P peak also coincides with the shoulder
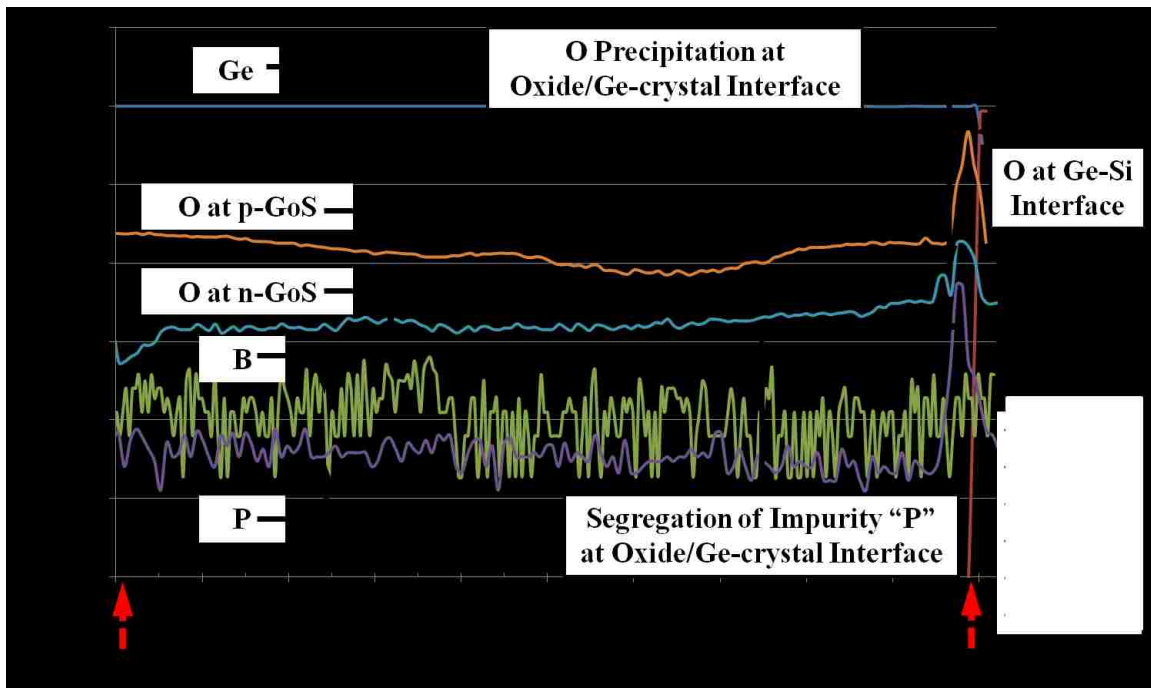
Figure 4.14: SIMS spectrums of n-type and p-type GoS substrates. The blue line represents concentration of Ge in GoS substrate, which is maximum. The O concentration for p- and n-type GoS substrates are shown here. The O concentration in p-type is higher than that of in n-type, causing more defects in the p-type GoS substrate.

peak of O. As seen from the SIMS, these two peaks are approximately 25-30 nm away from the Ge-Si interface, and cross-sectional HRTEM result also supports SIMS measurement. We speculate the sharp drop of P peak due to n-type impurity such as P has larger dopant segerate coefficient (k_0) than that of B. The k_0 can be written as,

$$k_0 = C_{Ge}/C_{oxide\text{-}precipitate} \tag{4-3}$$

Based on SIMS data, the n-type dopant has $k_{0,P}=15$ in precipitate/Ge interface compared to p-type dopant which has $k_{0,B}=0.2$. This indicates that P is more likely to be introduced into the Ge crystal via dopant segregation compared to B into Ge crystal. Additionally, concentration of B remains almost constant throughout the Ge layer, and close to 8×10^{16} cm^{-3} at the surface, which is close to 1×10^{17} cm^{-3} concentration obtained from Hall measurements. In contrast, the concentration of P drops in the vicinity of Ge-Si interface due to segregation, and settles to 1×10^{16} cm^{-3} at the surface, whereas Hall measurements show a P concentration of 5×10^{16} cm^{-3}. Based on segregation coefficients ($k_{0,P}>1$ and $k_{0,B}<1$) values obtained from SIMS analysis, we can say that P diffuses extremely slowly in oxide precipitates compared to B. As a matter of fact, we speculate that diffusion distance for P through a monolayer thick oxide precipitate should be an order of magnitude slower than that of diffusion distance for B. To verify our understanding on diffusion distance of impurities, we run a very simple experiment where we grow certain thicknesses of n- and p-type GoS keeping the growth time constant for both experiments which is 60 min. We observe that the growth rate for n-type GoS is 2.5×10^{-8} cm/sec compared to 1×10^{-8} cm/sec for p-type GoS. According to *R. N. Hall et al.*, we obtain values of segregation constants (K) for P and B in Ge crystal, and they are 0.1 and 10, respectively. Additionally, according to *Christense et al.*, , under vacuum annealing range at 825-850°C, the diffusivity (D_P or D_B) for P and B are 4×10^{-16} and 8×10^{-16} cm^2/sec, respectively. We can estimate the diffusion distance (d), which can be written as,

$$d = \text{growth rate}/D_P \text{ or } D_B \tag{4-4}$$

of 1.6×10^{-8} cm and 6×10^{-8} cm, for P and B, respectively. We note that the diffusion

distance for P through a oxide precipitate monolayer is approximately 4 times smaller

than that of B. Based on calculation of segregation coefficients and diffusion distances

for two different impurities, we can conclusively tell that P tends to preferentially

segregate along the precipitate/Ge-crystal interface, whereas B likes to deplete at

precipitate/Ge-crystal interface. Figure 4.15 shows a schematic where segregation of P

atoms occur at the oxide-Ge interface. where as no segregation of B atoms occur at the
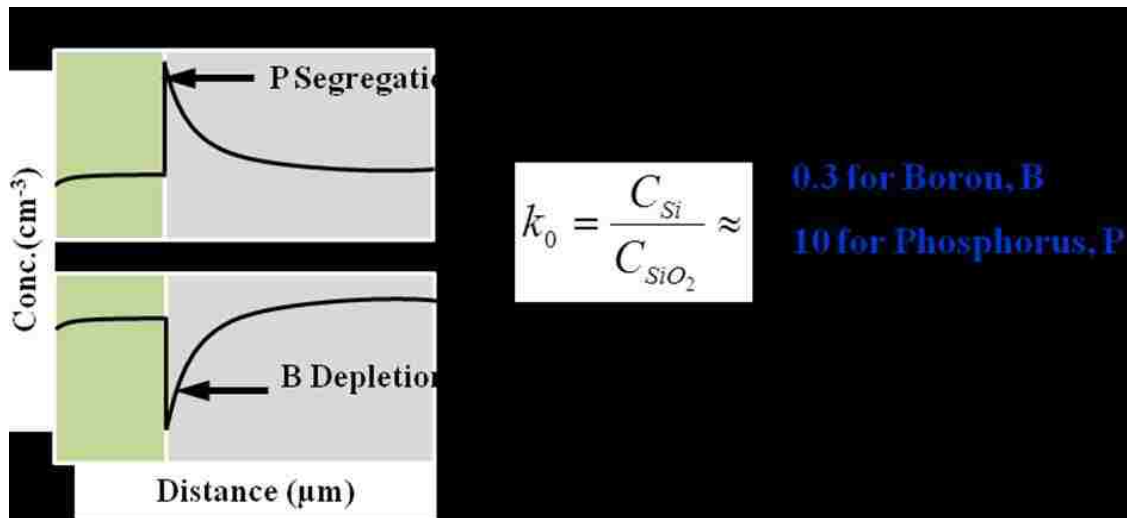
oxide-Ge interface.

Figure 4.15: Phosphorus atoms preferentially segregate at oxide-Ge interface. In contrst, B atoms don't segregate at the oxide-Ge inetrface. The phosphorus segregation results to dislocation locking at the Ge epilayer.

This argument can be supported through SIMS results, which shows that B maintains a

constant level of concentration away from the precipitate/Ge-crystal interface. Thus,

proposed mechanism for dislocation locking is herein where preferential segregation of P

helps to form a complex precipitate-dopant matrix which captures dislocations, and

subsequently rest of the dislocations simply bowed at the precipitate interface. In comparison, B dopant unable to form such complex precipitate-dopant matrix, and major portions of dislocations that are stemming at the Ge-Si interface subsequently propagate upward. Additionally, O concentration in n-type Ge film drops continuously right after precipitate-dopant interface, and the magnitude of O concentration on the surface of Ge for n-type is approximately 50 times smaller than that of in p-type GoS. We note that O incorporation leading to stacking fault formation during Ge(001) epitaxy. Figure 4.16 depicts a characteristic hexa-ring (six-atom ring) in the diamond lattice structure of Ge, represented by atom numbers 1, 2, 3, 4, 5, and 6. In a defect-free growth condition, where incorporation of three-atom nuclei (4, 3, 7; 4, 5, 8) in the [001] direction occurs, often satisfies the requirement for three-dimensional periodicity of the hexa-ring pattern. In the {111} plane that comprises the three-atom nucleus is bonded covalently to two atoms above and below the plane. However, incorporation of O during epitaxy results in the formation of a Ge–O–Ge bonding in the hexa-ring pattern, and subsequently perturbs the stacking sequence of {111} planes. The disruption in stacking sequence can be attributed to the presence of O, forming only two bonds with the adjacent Ge atoms in the lattice. This loss of stacking sequence in the {111} plane yields SFs, which subsequently propagate along [001] and intersects with Ge surface along [110]. This type of similar mechanism is shown in [151] which describes about the solid-phase epitaxial growth of Si. The device performance is very sensitive to the presence of SFs and dislocations since they contribute in the rise to dark currents which is unwanted elements in photodetectors or they give rise to large threshold currents in laser diode. Therefore, it's imperative to grow a film that can provide very low-dislocation-density. This pronounced reduction of

O concentration on the surface through dislocation locking yields an ultra-low-dislocation-density n-type GoS film that has TDD of 10^5 cm^{-2}.
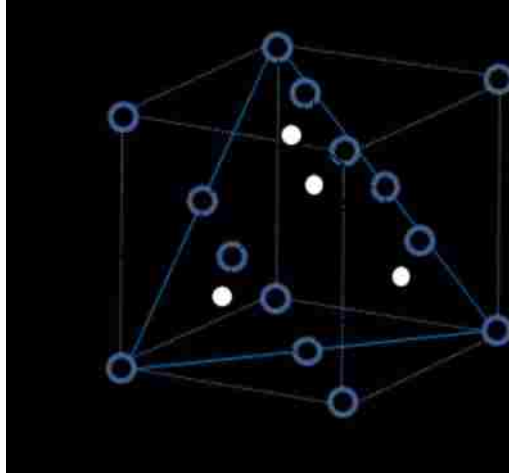
Figure 4.16: a characteristic hexa-ring (six-atom ring) in the diamond lattice structure of Ge, represented by atom numbers 1, 2, 3, 4, 5, and 6 [151].

4.4   Plan-view Characterization of Ge Films

Previous sections of this chapter describe the mechanisms of our modified growth approach for GoS. We notice that n-type GoS has better epitaxial quality than that of p-type GoS. We also performed an in-depth investigation, which reveals that introduction of oxide precipitates coupled with impurties help to lock dislocations in n-type GoS. In contrast, the p-type GoS does not show any oxide precipitates forming near the Ge-Si interface.   Most of the dislocations terminate within a tangled network close to the Ge-Si interface in the case for n-type GoS, whre as majority of dislocations propagate toward the surface of the Ge in p-type GoS. The x-TEM tool though provide enough information about dislocations, however, plan-view TEM (PV-TEM) is the best tool in order to count number of dislocations that intersects the film surface. Herein, pv-TEM image, such as that shown in fig. 4.17, show that the TDD for n-type Ge film is approximately 1 x 10^5

cm^{-2}. For better statistical estimation, we have captured four pv-TEM images from four

different parts of the sample.
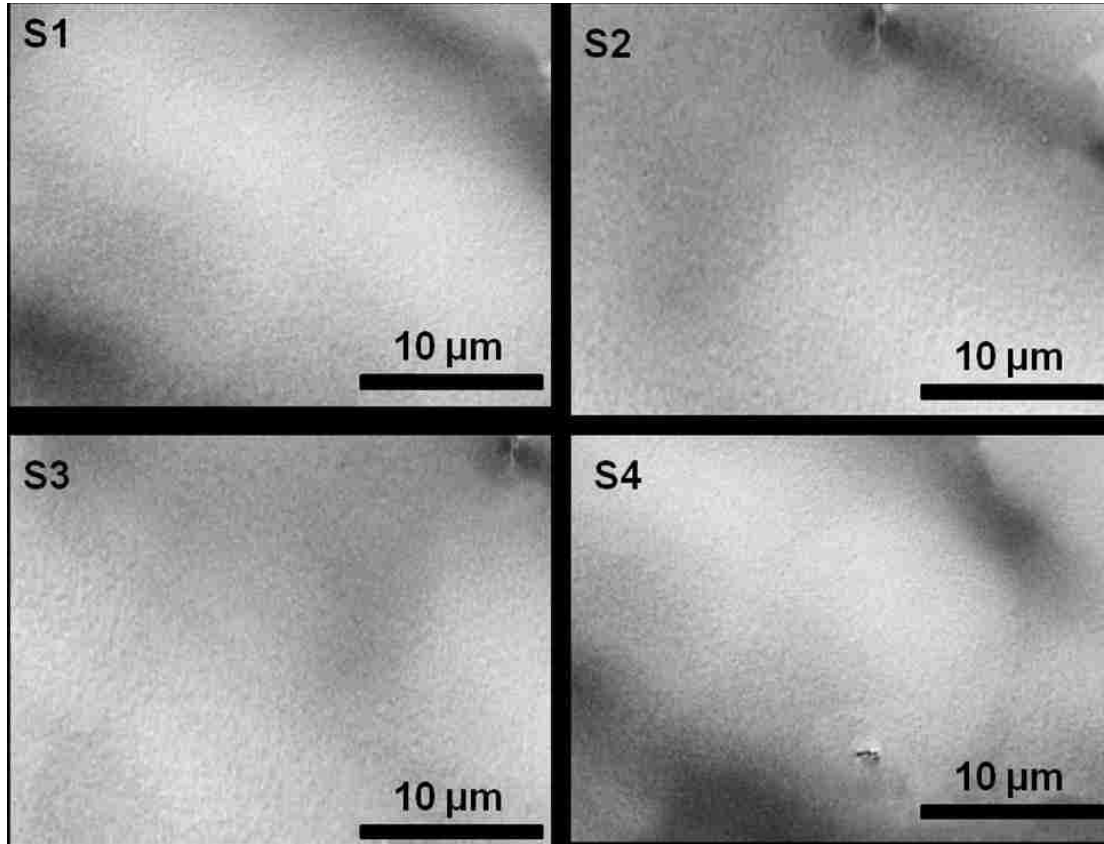
Figure 4.17: Plan-view transmission electron micrograph images showing almost no
dislocations in a n-type GoS film. S1, S2, S3 and S4 show four different parts of the
sample. This enables us to get a good statistical estimation about the total TDD.

In contrast to n-type GoS film, the p-type GoS film shows dislocation pproximately 5 x

10^7 cm^{-2}, shown in fig. 4.18. The TDD number that we have obtained from pv-TEM

images are very much in agreement to the TDD numbers that we have obtained from

EPD measurements.
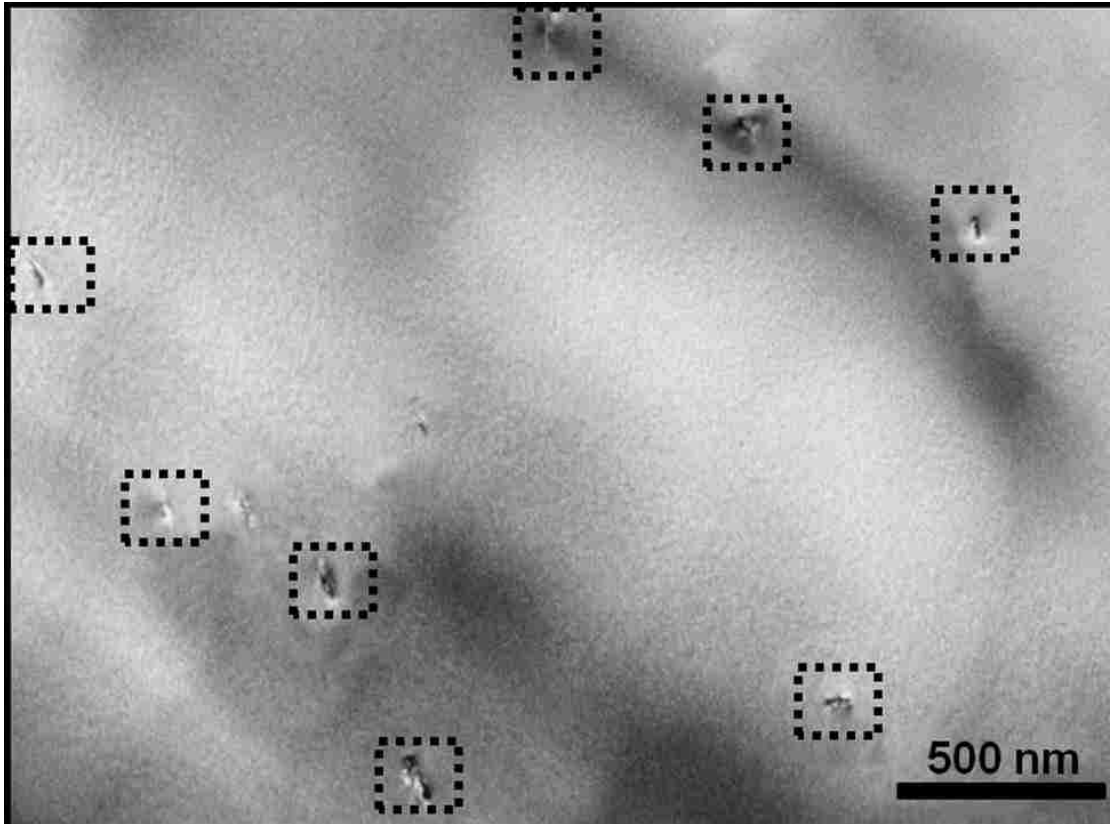
Figure 4.18: Plan-view transmission electron micrograph showing dislocations in a p-type GoS film.

CHAPTER 5 Investigation on Thermal Stress Stress Relief in Ge-on-Si using air-gapped SiO$_2$ nanotemplates

5.1   Introduction and Background:

We demonstrate that SiO$_2$ nanotemplates embedded in epitaxial Ge grown on Si relieve the stress caused by the thermal expansion mismatch between Ge and Si. The templates also filter threading dislocations propagating from the underlying Ge-Si interface, reducing the density from 9.8×10^8 to 1.6×10^7 cm^{-2}. However, we observe that twin defects form upon Ge coalescence over the template, and the density is approximately 2.8×10^7 cm^{-2}. The coalescence occurs without direct contact with SiO$_2$, leaving a void between Ge and SiO$_2$ that further reduces the thermal stress. The stress obtained from finite element modeling corroborates the experimental observation.

High-quality Ge heteroepitaxially grown on Si proves advantageous in many applications, including near infrared photodetectors [152], high-mobility transistors integrated on Si substrates, and virtual substrates for III-V multijunction solar cells. Growing low-dislocation-density Ge on Si (GoS) and subsequently integrating III-V layers presents two significant engineering challenges: lattice and thermal expansion coefficient mismatch. The materials engineering solutions to circumvent the lattice mismatch include post-growth annealing [153], graded buffer layers[154], selective epitaxial overgrowth (SEG) [155], and aspect ratio trapping (ART) [156]. The ART technique, in particular, utilizes high-aspect-ratio holes or trenches etched through dielectric films to trap dislocations, greatly reducing the dislocation density. A noteworthy advantage of ART technique is that it avoids the thick buffer and high thermal budget typical of other heteroepitaxial techniques, making it more suitable for

integration with Si complementary metal oxide semiconductor (CMOS) process. However, one shortcoming of ART is that it has been demonstrated to be effective only for small holes or narrow strips with dimensions less than 1 μm [157].

We focus on the use of SiO_2-based templates with nanoscale channels placed on the epilayer of GoS followed by Ge SEG. The template simultaneously filters threading dislocations (TDs) propagating from the Ge-Si interface and relieves the film stress caused by the thermal expansion coefficient mismatch between Ge and Si. We analyze the effectiveness of the template in filtering TDs in the lower Ge layer. In addition, we examine the existence and potential causes of defects stemming from the coalescence of adjacent Ge growing out of the template channels over the SiO_2 template. Lastly, we investigate the effects of template geometry on thermal stress, using finite element modeling (FEM).

5.2   Experimental Details:

The Ge is grown using molecular beam epitaxy (MBE). The 5-cm diameter Si (001) substrates used in this study are boron doped with a resistivity of 1-10 Ω-cm. The Si substrates are cleaned and chemically oxidized for 5 min in piranha bath consisting of 3 volumetric parts of H_2SO_4 (96 wt %) and 1 part of H_2O_2 (30 wt %) and heated at 373 K. The samples are subsequently dipped into a buffered oxide etch solution (20 parts 40 wt % NH_4F: 1 part 49 wt % HF) diluted in deionized (DI) water by 6:1 volumetric ratio to remove the chemical oxide. The chemical oxidation is then repeated, and the wafer is rinsed in DI water and blown dry with N_2. The final chemical oxidation step is previously shown to result in a chemical oxide layer of 1.4 nm thickness[85,88,158].

After being loaded into the deposition chamber, the samples are degassed at 853 K for 10 min. The effusion cell temperature is set to produce a flux of 6.7 x 10^{14} atoms $cm^{-2} s^{-1}$ (64 ML/min) and allowed to stabilize for 30 min. The substrate temperature is then increased to 1073 K for 30 min to remove the chemical oxide. Next, 1 µm of Ge is deposited after lowering and stabilizing the substrate temperature to 853 K. The pressure in the chamber remains below 1.3 x 10^{-6} Pa during the deposition. The GoS samples are polished using a Logitech PM5 lapping/polishing machine on a Logitech chemcloth polishing pad. The polishing solution consists of 50 parts of DI water and 1 part of 30 wt % H_2O_2. A 60 nm thick SiO_2 layer is deposited on GoS by plasma enhanced chemical vapor deposition (PECVD) using SiH_4 and N_2O. The SiO_2 is patterned into trenches along the [110] direction using interferometric lithography[159-165] and reactive ion etching. The SiO_2 trench width and pitch are 200 and 400 nm, respectively. The patterned sample is again transferred to the deposition chamber for SEG, where an additional 1 µm of Ge is deposited. The GoS samples are characterized using cross-sectional transmission electron microscopy (x-TEM), scanning electron microscopy (SEM), and etch pit density (EPD) measurements.

5.3 Results and Discussions:

Figure 5.1 shows x-TEM images of the structure containing the SiO_2 nanotemplate. In Figure 5.1(a), the estimated threading dislocation density (TDD) below the oxide template is 9×10^{10} cm^{-2}. We note that this relatively high TDD in the lower Ge epilayer is chosen as the baseline solely for the purpose of demonstrating of TD
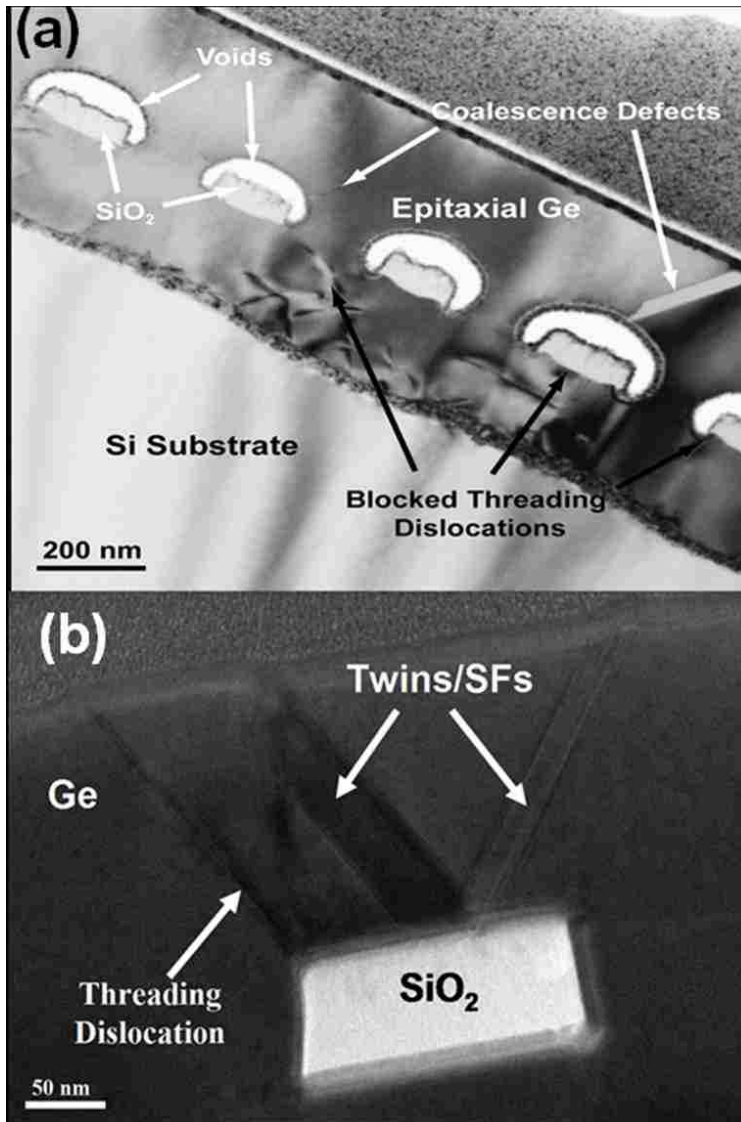
Figure 5.1: TEM images of (a) Ge forms a void over the SiO_2 template while epitaxially grown on GoS. The template filters threading dislocations. (b) Ge grown in direct contact with the template over GoS [166].

filtering. Most TDs are blocked by the oxide walls and do not propagate into the upper

SEG Ge layer. Figure 5.1(a) also shows that voids (or air gaps) form around the

sidewalls and top of the oxide template during Ge SEG at 923K. In contrast, Figure 1(b)

shows that voids do not form over the oxide template during Ge SEG at 853K. However,

twins and stacking faults are present in both TEM images irrespective of formation of

voids over the oxide template.

The EPD of the GoS substrate and the Ge epilayer coalesced over

the SiO_2 template on GoS is shown in the SEM images of Figure 5.2(a-b). The square

shaped pits shown in Figure 5.2(a) correspond to TDs with a density of 1.1×10^8 cm^{-2} that

intersects the film surface. The TDD in Figure 5.2(b) is 1.6×10^7 cm^{-2}. The rectilinear

pits correspond to twins and stacking faults (SF) aligned with [110] that propagate to the

film surface. The density of twins/SFs in the sample is 2.8×10^7 cm^{-2}. The twins also

show the same preferential alignment along the [110] oxide template. The large circular

openings are due to incomplete coalescence of the Ge SEG. The large opening shown in

the inset of Figure 5.2(b) reveals the location of a twin defect that exists directly over top

center of the SiO_2.

5.4   Mechanism of Thermal Stress Reduction using Air-gap

The results displayed in Figures 5.1 and 5.2 show that twins/SFs

form during coalescence independent of void formation. We consider three possible

mechanisms responsible for the twin/SF formation. First, the atomic scale roughness of

the SiO_2 surface may lead to local misorientation of the Ge during lateral growth over the

oxide template. Second, coalescence defects may form due to translation misalignment

as depicted in Figure 5.3. That is, the width of the SiO_2 template walls may not be an

integer multiple of Ge lattice spacing. Therefore, adjacent Ge growing out of channels
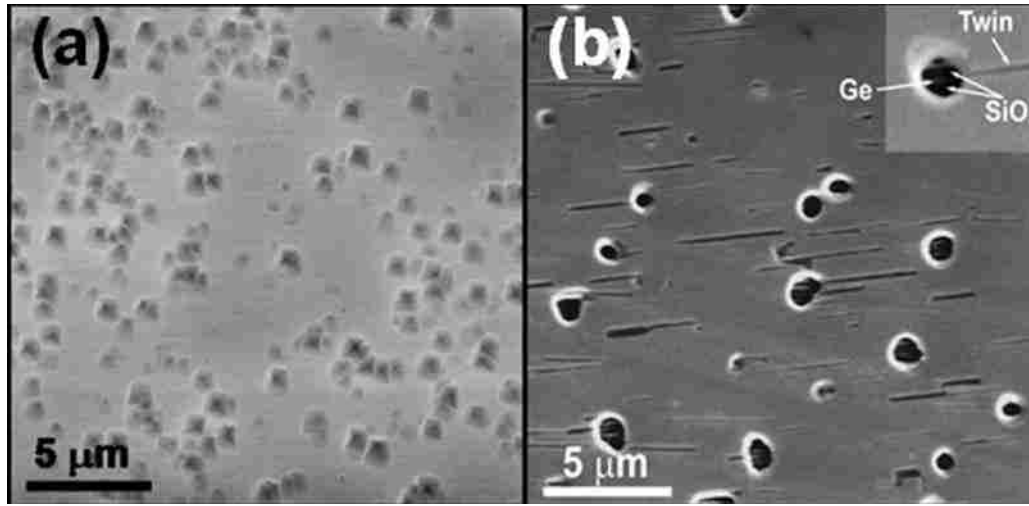
Figure 5.2: (a) Scanning electron micrograph of annealed GoS film etched for 30 s revealing square shaped etch pits. (b) Scanning electron micrograph of epitaxial Ge film grown via SiO2 trenches on GoS film etched for 30 s revealing etch pits [166].

will no longer be in registry to each other as they grow laterally over the SiO$_2$, leading to defect formation during coalescence. This mechanism is well established by previous studies showing that twins form during coalescence when translation mismatch exists between islands[167-170]. Third, thermal stress in the Ge epilayer is caused by the difference in thermal expansion coefficient (TEC) of Si, Ge, and SiO$_2$. The thermal stress induces a varying Ge lattice constant in the underlying GoS, especially adjacent to SiO$_2$, thereby leading to translational mismatch during subsequent lateral overgrowth.

5.5   Finite Element Modeling of Air-gapped Templates:

We eliminate the first mechanism based on results shown in Figure 5.1(a), in which twin defects form during Ge coalescence without contact with SiO$_2$. Next, we use FEM to investigate the effects of SiO$_2$ template and Ge morphology on the

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thermal stress in the samples. Figure 5.4(a) shows the thermal stress due to 600K

temperature excursion and growth of 2 µm of GoS without SiO_2 template. The TEC of
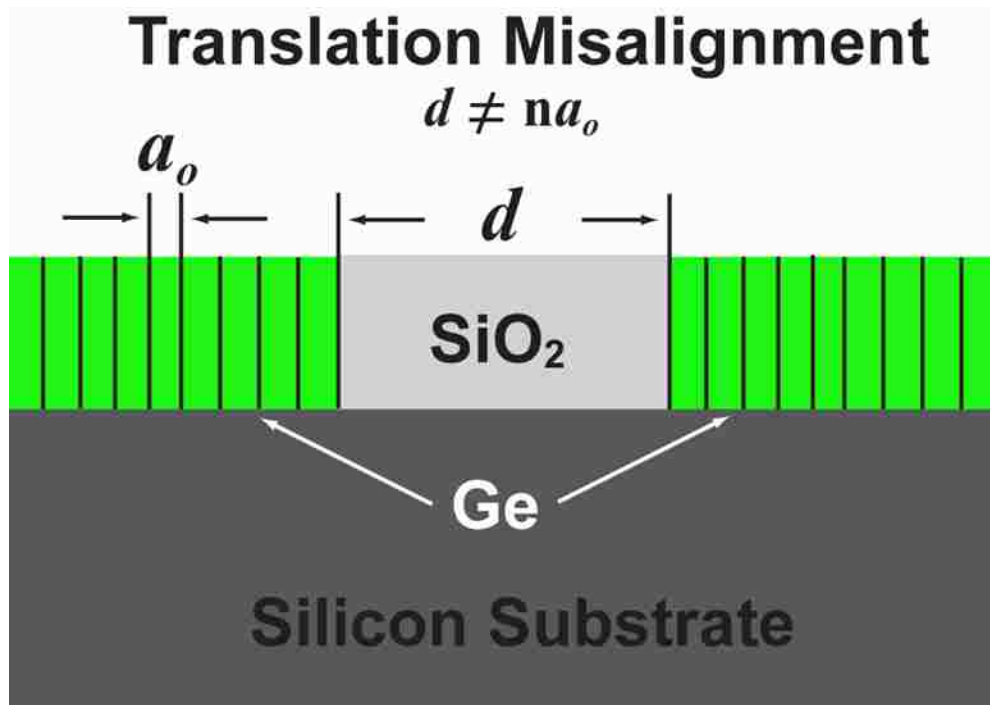
Figure 5.3: Potential misalignment of Ge islands that leads to defect formation upon coalescence [166].

Ge is that of Si, hence the resulting tensile stress in Ge is uniformly distributed and up

approximately twice to 3×10^8 Pa. Figure 5.4(b) corresponds to the structure shown in

Figure 5.1(a) in which Ge forms a void over the SiO_2 template. The results show that

maximum tensile stress of $\sim 1.6 \times 10^8$ Pa occurs in the Ge facing the top corners of the

SiO_2 template, indicated by arrows. These high stress regions are where twin defects are

observed in Figure 5.1(a). Figure 5.4(c) corresponds to the structure shown in Figure

5.1(b) in which Ge grows laterally in contact with the SiO_2. The maximum stress of

$\sim 1.8 \times 10^8$ Pa occurs in the Ge near the top corners of the SiO_2 template (indicated by

arrows). The high stress regions of Figure 5.4(c) correspond to the location of TDs

emanating from the top left corner of the SiO$_2$ wall shown in Figure 5.1(b). Comparing

Figure 5.4(a) with that of 5.4(b-c) shows that the stress in the Ge epilayer is no longer
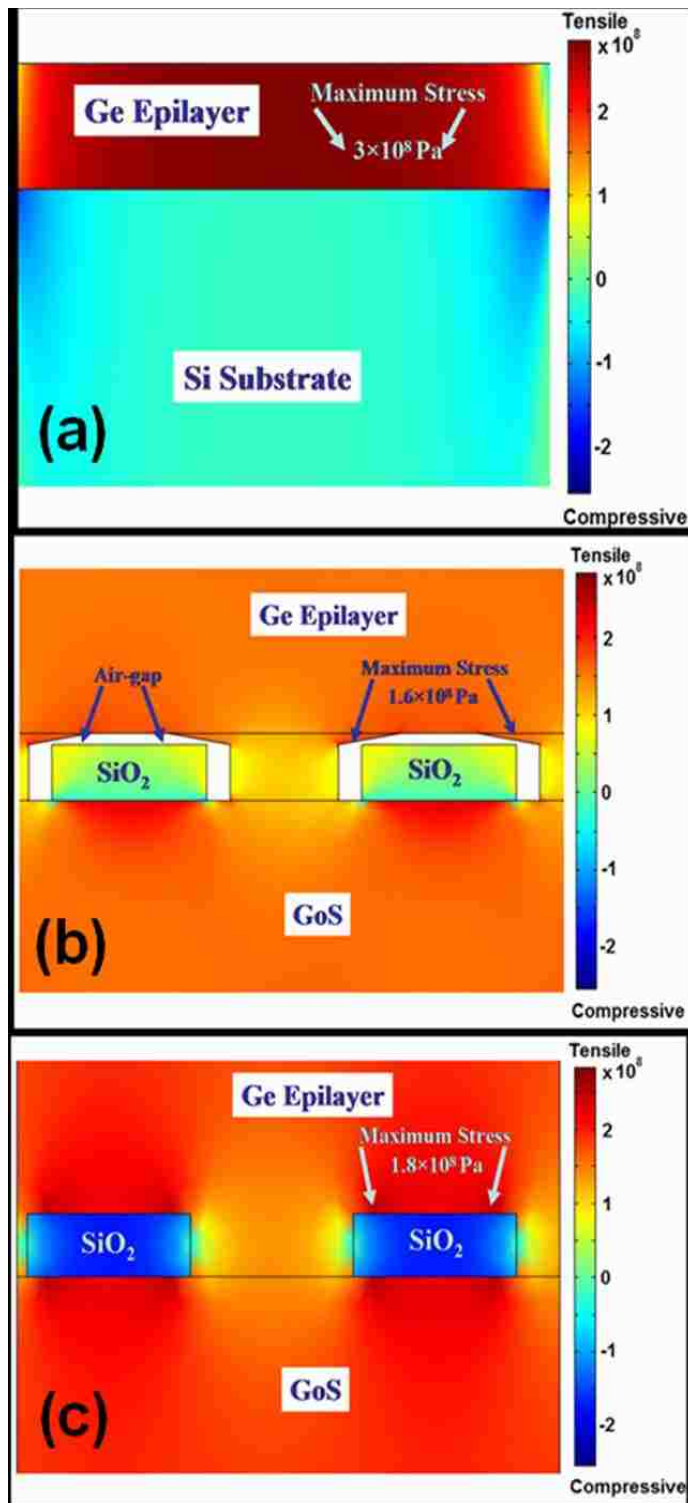
Figure 5.4: FEM simulation images of (a) epitaxial Ge grown directly on underlying Si substarte (b) Ge forms a void over the SiO_2 template while epitaxially grown on GoS (c) Ge grown laterally in contact with the SiO_2 template over GoS.

uniform due to the presence of SiO_2 template. The non- uniformity of the stress field due to template is a potential source of translational mismatch as described earlier. Figure 5.4(b) also shows that the magnitude of stress field in the Ge epilayer above the air-gapped SiO_2 template is less than that underneath the SiO_2 template. In comparison, Figure 5.4(c) shows that the magnitude of the stress field in the Ge epilayer in direct contact with the SiO_2 above the SiO_2 template and that underneath the SiO_2 template are approximately equivalent. These results indicate that the structure in which Ge epilayer forms void over the SiO_2 template imparts less thermal mismatch stress than the structure in which Ge epilayer grows in direct contact with the SiO_2 template.

5.6   Conclusions:

In summary, an air-gapped SiO_2 nanotemplate structure is considered to reduce the thermal stress caused by TEC mismatch between Ge and Si and to simultaneously filter the TDs. A FEM stress modeling further corroborates this stress relief mechanism. The total defect density in the coalesced Ge film, which consists of TDs and a combination of twins and SFs, is about 2.8×10^7 cm^{-2}. The use of SiO_2 template in combination with SEG reduces the threading dislocation density (TDD) above the SiO_2 template by nearly 2 orders of magnitude compared to the Ge layer beneath the template. However, twins and SFs form during Ge coalescence over the SiO_2 template. Based on the TEM images, the likely mechanism for twin/SF formation is the translational misalignment of Ge growing out of adjacent template channels and coalescing over the SiO_2 template, compounded by the thermal mismatch stress.

CHAPTER 6 High-Speed Transistors on Ge-on-Si Substrates

6.1   Introduction

Improving effective carrier mobility, instead of continuously miniaturizing device dimensions, can be an alternate path to advance the performance of integrated circuit transistors. For instance, the use of strained channel and change in channel direction[171,172] have been shown to enhance the carrier mobility. Another approach is to use high carrier mobility materials, such as Ge [173,174], $In_{0.53}Ga_{0.47}As$[175], and InP [176] for the transistor channel. Among these materials, Ge has been extensively studied due to its hole mobility four times higher and electron mobility two times higher than those of Si[177]. In addition, a thin layer of Ge can be used as a buffer to integrate III-V channel materials to achieve high electron mobility[178,179]. Hence, Ge and III-V materials epitaxially grown on Si have emerged as a promising candidate for the next generation of high-mobility field-effect transistors[180].

While the superior carrier mobility in Ge is recognized, the use of epitaxially grown Ge-on-Si (GoS) wafer-scale substrates for high-mobility transistors has not been commercially demonstrated because of the difficulty in achieving Ge of sufficient quality. This is primarily due to the 4.2 % lattice mismatch and 116% thermal expansion coefficient mismatch between Ge and Si. The former can result in threading dislocation densities (TDD) on the order of 10^7-10^9 cm^{-2}, while the latter can lead to microcracks in Ge films or their delamination as the wafer cools from an elevated growth temperature (e.g., 853 K) to room temperature. Various methods exist to reduce the defect density in GoS substrates, including graded Ge_xSi_{1-x} buffer layers[181], thermal cyclical annealing[182], strained-layer blocking[183], small-area mesas[184], and aspect ratio trapping[185]. These methods have had varying degrees of success, while presenting new

integration challenges, such as the need to use very thick buffer layers, high temperature processing steps, or limited area growth.

In addition to the existing materials engineering issues around heteroepitaxy, the device integration also poses difficult challenges. For instance, maximizing Schottky barrier height (SBH), minimizing reverse leakage current, and minimizing their variation over large area are critical for fabricating low-power transistors[186]. Previous studies have revealed that SBH depends on the forward bias ideality factor[186], choice of Schottky metal[187], influence of surface damage[188], and material quality[189]. Dimoulas *et al.* [190] have reported a strong Fermi-level pinning by the charge neutrality levels close to the valence band edge of Ge. Such strong Fermi-level pinning leads to the formation of low resistance Ohmic contacts on p-type Ge, irrespective of metal work functions. To unpin the Fermi-level, Zhou *et al.* [191] reported a fabrication of Schottky contact on p-type Ge by inserting a thin Al_2O_3 layer between the metal and p-Ge. However, less is known about the properties of dielectric layers required to unpin the Fermi-level in the case of metal and heteroepitaxially grown p-type GoS, where dislocations in the heteroepitaxial Ge propagate to the metal-Ge interface. In consideration of these dislocations, our goal was to develop a detailed understanding of how the thin dielectric layers would relieve the Fermi-level pinning and affect the metal-GoS Schottky barrier properties.

In comparison to previous studies on FETs based on Schottky gate contact on Ge-channel on SiGe or Si substrates[192], we have investigated the electrical characteristics of p-channel metal semiconductor field effect transistors (MESFETs) fabricated on GoS virtual substrates. We note that our Ge film covers the entire

underlying Si substrate at the wafer scale without mesas or limited-area growth. We have developed a method to improve the GoS film quality by the nucleation of Ge islands within nanoscale windows in a thin layer of chemically grown SiO_2 and successive island coalescence over the SiO_2[193,194], dubbed as "touchdown" method. The details of the touchdown technique are provided in our previous work[193,194]. In this study, we have created samples with varying threading dislocation densities (TDDs) ranging from low-10^7 to high-10^8 cm^{-2} by changing the growth parameters of the touchdown method. The purpose was to determine how the dislocation density affects the device performance of MESFETs fabricated from our GoS substrates. The reason for such characterization is that dislocations and point defects that are present in the Ge film as well as at the Ge/Si interface act as scattering and/or recombination centers for charge carriers. These defects degrade the device performance and raise the issue of long-term reliability. Here, we report the impact of dislocation density and the thin dielectric layer on the performance of high-hole-mobility p-channel MESFETs fabricated on our GoS substrates, and we demonstrate the quality of relaxed Ge epilayer grown by the touchdown method.

6.2 Germanium Growth on Silicon

Germanium is grown by molecular beam epitaxy (MBE). Details of the growth parameters including flux and substrate heater calibration are described elsewhere[195]. Si(100) substrates used in this study are semi-insulating (SI) with a resistivity greater than 1000 Ω-cm. The reason for using SI-Si substrates is to minimize the leakage current through the Si substrate during pinch-off operation of MESFETs. The SI-Si substrates are cleaned and chemically oxidized for 5 min in a Piranha bath

consisting of 3 volumetric parts of H_2SO_4 (96 wt %) and 1 part of H_2O_2 (30 wt %) and heated to 373 K. The samples are subsequently dipped into a buffered oxide etch solution (20 parts 40 wt% NH_4F: 1 part 49 wt% HF) diluted in deionized (DI) water by 6:1 volumetric ratio to remove the chemical oxide. The chemical oxidation is then repeated, and the wafer is rinsed in DI water and blown dry with N_2. The final chemical oxidation step results in a SiO_2 layer of 1.4 nm thickness [25]. After being loaded into the deposition chamber, the samples are degassed at 873 K for 10 min. The effusion cell temperature is set at 1393 K to produce a flux of 7.6 x10^{13} atoms/ cm^2-s (7.6 ML/min) and allowed to stabilize for 30 min before the shutter is opened for deposition. The pressure in the growth chamber remains below 2 x 10^{-8} Pa during the deposition period.

By varying the deposition conditions and number of thermal annealing cycles, we have produced four different samples with different TDDs (Samples A – D). For Sample A, a 5-nm-equivalent amount of Ge is initially deposited, using the touchdown technique. We define the equivalent amount as the thickness of a continuous Ge film that would have resulted if Ge uniformly covered the substrate surface without forming 3D islands. After the initial growth and while the shutter remains closed, the substrate temperature is raised to 1123 K for 30 min in order to remove stacking faults (SFs) and dislocations from partially coalesced Ge islands[194]. The substrate temperature is then reduced to 873 K and allowed to stabilize for 10 min before the shutter is opened for further deposition at 7.6 ML/min. This second phase of the growth starts with depositing a 100-nm-equivalent amount of Ge. Then, the effusion cell temperature is set at 1473 K to produce an increased flux of 5.1×10^{14} atoms/cm^2-s (51 ML/min) until the

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final thickness of the film is approximately 1 μm. This film is then annealed at 1073 K for 30 min.

For Sample B, a 25-nm-equivalent amount of Ge is first deposited until Ge is fully coalesced into a continuous film, using the touchdown technique. While the shutter is closed, the substrate temperature is raised to 1023 K for 30 min to glide out the dislocations. The substrate temperature is then reduced to 873 K and allowed to stabilize for 10 min before the shutter is opened to deposit 150 nm of Ge. The effusion cell temperature is then set to 1473 K to achieve approximately 1 μm of final film thickness. For Sample C, the substrate temperature is set to 873 K and allowed to stabilize for 10 min before the shutter is opened to deposit an approximate 1-μm-equivalent amount of Ge, using the touchdown technique. This film is then annealed at 1073 K for 30 min.   For Sample D, a 1-μm-equivalent amount of Ge is deposited directly on Si substrate without the touchdown technique.   No post-growth annealing is performed on Sample D.

After the growth, all GoS samples are polished using a Logitech PM5 lapping/polishing machine on a Logitech Chemcloth polishing pad. The polishing solution consists of 50 parts of DI water and 1 part of 30 wt. % H_2O_2. The final thickness of these samples is approximately 270 nm after polishing.

Samples A-D are characterized using etch pit density (EPD) and X-ray diffraction (XRD). For etch pit density measurements, the samples are immersed for 2 min in an etch solution that consists of 2 volumetric parts of 49 wt % HF and 1 part of 0.1 M $K_2Cr_2O_7$. The revealed etch pits are then imaged by an FEI Quanta 3D scanning electron microscope (SEM) operating at 15 keV for the electron beam energy. Our

previous work, using plan-view transmission electron microscopy (TEM), shows that

EPD measurements quantitatively represent the dislocation density in the Ge film[195]. The

XRD technique is used to qualitatively determine the crystallinity of Ge films. We use a

Phillips MRD X-ray diffractometer equipped with Cu K_α line at 0.154 nm. This line

provides sufficient resolution to measure the interatomic distances of Ge epilayer. We

use the full width at half maximum (FWHM) of (004) and (331) diffraction peaks as an

indicator of Ge film crystallinity and defect level.

6.3   Materials Characterization

Prior to device fabrication, we characterized the Ge film quality,

using EPD and XRD. Figures 6.1(a) – (d) are a series of SEM images of etch pits created

on Samples A-D. These etch pits reveal TDDs of 2×10^7, 5×10^7, 7×10^7 and 2×10^8 cm^{-2},

respectively. Consistent with the EPD measurements, Figures 6.2(a) – (d) show the (004)

diffraction peaks of Ge and Si from Samples A-D. The full-width-at-half-maximum

(FWHM) of Ge(004) peak for Sample A is narrower than that of Sample D by 72%.

Similarly, the FWHM of the (331) reflection (not shown) for Sample A is narrower than

that of D by 67%. These results indicate that stacking faults (SFs) are largely removed in

Sample A, and the crystal quality of the Ge films significantly improves during the

1123K anneal that is performed before the island coalescence stage of Ge growth. Based

on the materials characterization, we expect the best device performance from Sample A

and progressively lessening performance from Sample A to Sample D.

6.4   Metal-Semiconductor Field Effect Transistors Fabrication

Figure 6.3 shows a schematic diagram of the MESFET architecture

with the dimensions provided for convenience. The 270-nm-thick Ge epilayer consists of

two regions: a 100-nm-thick buffer layer, where most of the dislocations reside, and the
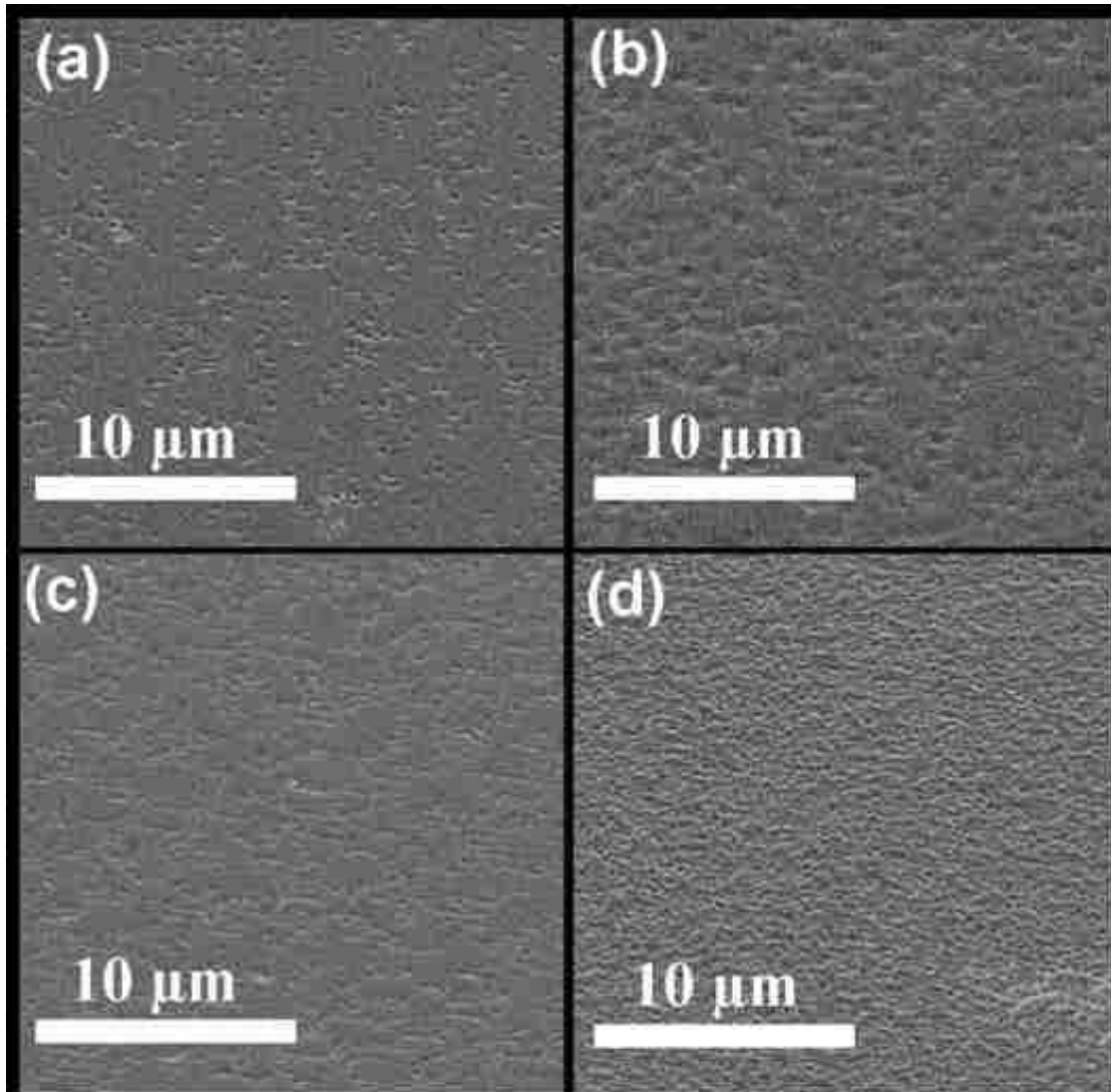
Figure 6.1: Scanning electron micrograph images of etch pits formed in the Ge film epitaxially grown on SI-Si film (a) with dislocation density of $2x10^7$ cm^{-2} (Sample A) (b) with dislocation density of $5x10^7$ cm^{-2} (Sample B) (c) with dislocation density of $7x10^7$ cm^{-2}

following 170-nm-chick layer being used as the channel. The channel region is doped to

p-type (5×10^{16} cm^{-3}) during the molecular beam epitaxy (MBE) growth.

Mesa isolation, which defines the total device width of 600 μm, is

done, using reactive ion etching (RIE) in a CHF$_3$/O$_2$ plasma. The CHF$_3$/O$_2$ plasma is

sustained with gas flow rates of 90 sccm/5 sccm and 120 W RF power at the chamber

pressure   of   75
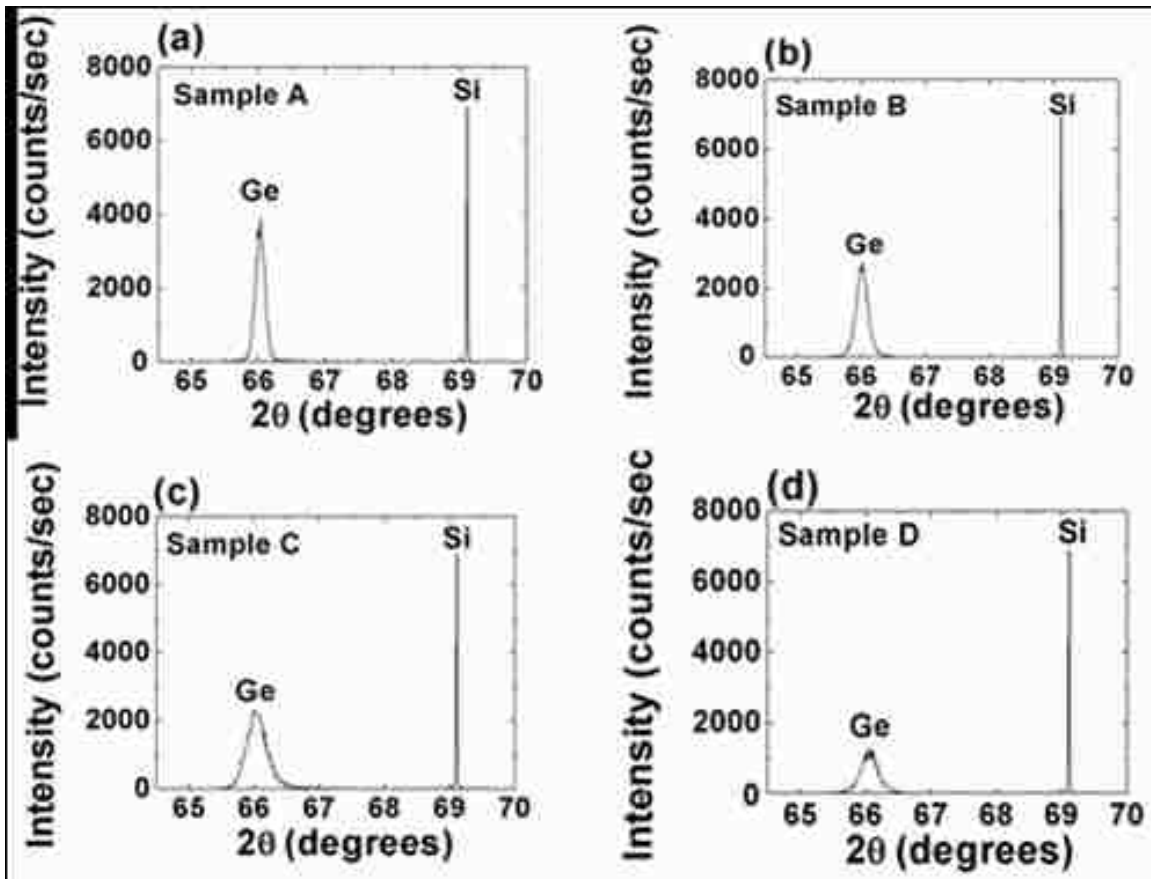
Figure 6.4: X-ray diffraction peaks of the (004) reflection of Ge films that are grown on SI-Si substrates under different growth conditions. Four different TDD samples are shown: (a) 2×10^7 cm^{-2} (Sample A), (b) 5×10^7 cm^{-2} (Sample B) (c) 7×10^7 cm^{-2} (Sample C), and (d) 2×10^8 cm^{-2} (Sample D).

mT. Under these operating conditions, the magnitude of self-bias on the substrate platen

is 95 V, and the etch rate is approximately 25 nm/min. The etching is performed in such

a way that the mesa wall is etched with an approximately 15° slope from the surface normal, instead of a vertical profile, allowing for the conformal deposition of gate metal on the mesa and along the mesa wall.

Following the mesa etching, the source and drain regions are defined by lithography. Ohmic contacts are formed by depositing 100 nm of Ti on source and drain regions using e-beam evaporator. To reduce the contact resistivity, rapid thermal annealing (RTA) is performed in a Ti metallization scheme at 450 °C for 30 s. The source–drain spacing is approximately 6.5 μm.
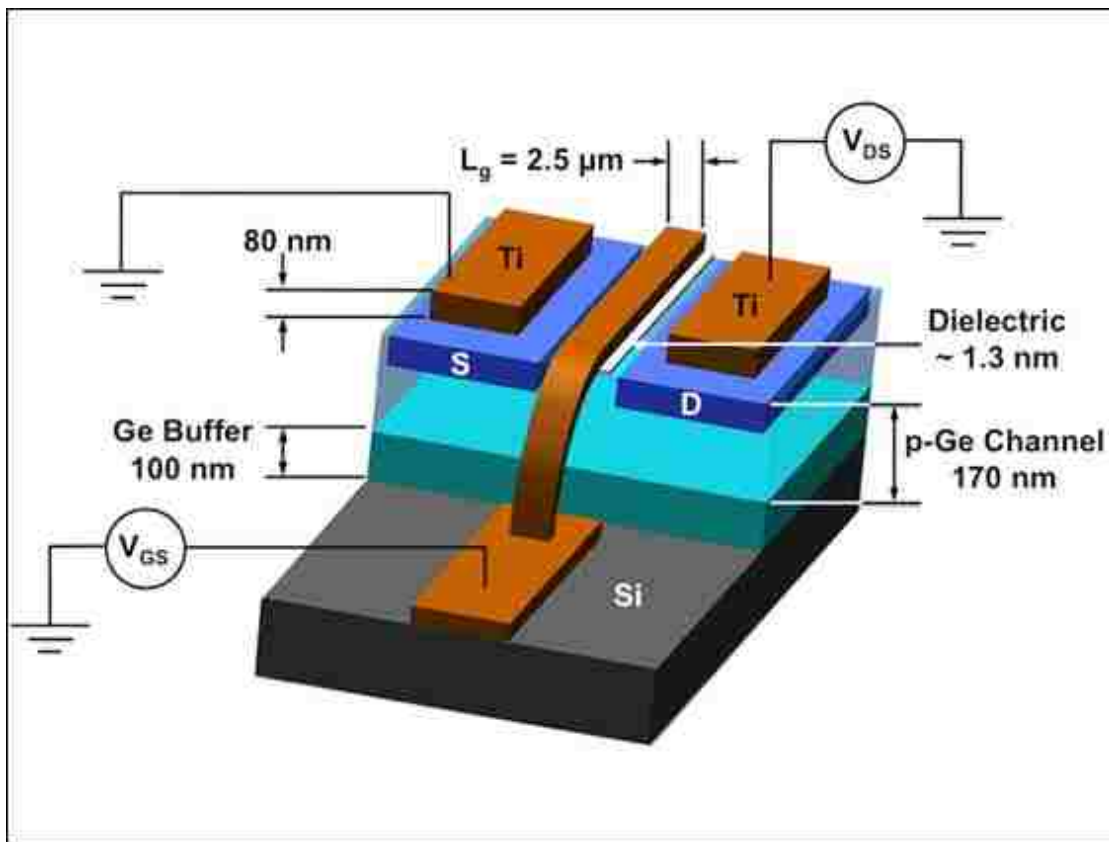
Figure 6.3: Schematic diagram of p-channel MESFETs with 2.5-μm gate length fabricated on epitaxially grown Ge on SI-Si substrates, using a 200 mm Si compatible process flow.

Finally, a T-shaped 2.5-µm-long gate region is defined by lithography. To unpin the Fermi level, we first deposit a thin dielectric layer (0.5 to 2 nm) on Ge and then deposit 80 nm of Ti to create the Schottky gate. Our fabrication thus follows a gate-last process flow. We have studied three different dielectric layers (SiO_2, Al_2O_3 and HfO_2) on each sample (Samples A-D). After the Ti/dielectric/p-GoS gate stack is completed, a forming gas (H_2/N_2 = 1:10) anneal is carried out at 370 $^{\circ}$C for 20 min. This forming gas anneal treatment is intended to reduce the abnormal flat-band voltage (V_{FB}) shift that often originates from the radiation charging during Ti evaporation[196]. These MESFETs allow mobility measurements to be made under operational conditions in a wide range of vertical electric fields applied to the Schottky gate.

6.5 Effect of Dislocations and Dielectric Layers on Electrical Characteristics

6.5.1. Hole Mobility in Ge Epilayer

Following the EPD and XRD materials characterization of Ge epilayer grown on Si, we have performed room-temperature Hall measurements under a magnetic field of 0.7 T, using the Van-der-Pauw geometry. We solder indium dots to the GoS substrates to create Ohmic contacts. Figure 6.4(a) shows the resulting room-temperature hole mobility plotted as a function of net carrier concentration in these films. In typical semiconductors where the ionized impurity scattering is the only scattering mechanism, the mobility decreases as the net carrier concentration increases. In our films, however, the mobility shows two regimes [Fig. 4(a)]. These two regimes are separated by a dashed line in Fig. 6.4(a). In Regime I, the mobility decreases with increasing carrier concentration, indicating that impurity scattering dominates in this

regime. In Regime II, the mobility increases with increasing carrier concentration. This latter trend can be attributed to dislocation scattering, and it has also been shown in epitaxially grown GaN[197].

For devices where holes are the majority carrier, the hole scattering is possible if the dislocations are p-type in nature[198]. The p-type dislocation lines become positively charged, and a space charge region is formed around them. The electric field surrounding the space charge region scatters holes traveling across the dislocations, thus reducing the mobility. Similarly, the dislocation-induced scattering of electrons has also been studied experimentally and theoretically in n-type Ge substrates[199]. The hole mobility accounting for the dislocation scattering can be expressed by [200]

$$\mu_{disl} = \frac{30\sqrt{2\pi}\varepsilon^2 d^2 (kT)^{3/2}}{N_{disl} e^3 (1\text{-}f)^2 \lambda_d \sqrt{m}} \, , \tag{6-1}$$

where ε is the dielectric constant of the epilayer, d is the distance between dislocation centers, k is the Boltzmann constant, T is the substrate temperature, N_{disl} is the density of dislocations, e is the unit charge, f is the occupation rate of the ionized dislocation centers of p-type, λ_d is the Debye screening length, and m is the mass of the charge carrier. λ_d in turn is given by

$$\lambda_d = (\frac{\varepsilon kT}{e^2 n})^{1/2} \, , \tag{6-2}$$

where n is the net carrier concentration. In comparison, the hole mobility accounting for the ionized impurity scattering can be expressed by

$$\mu_I = \mu_{min} + \frac{\mu_{max}\text{-}\mu_{min}}{1 + (\frac{n}{N_r})^\alpha} \, , \tag{6-3}$$

where μ_{min}, μ_{max}, α, and N_r are the minimum mobility at high carrier concentration, the maximum mobility at low carrier concentration, a unitless fitting parameter, and the density of states within the valence band.

The final mobility term is subsequently expressed by

$$1/\mu = 1/\mu_I + 1/\mu_{disl} \qquad , \qquad\qquad (6\text{-}4)$$

where μ_I is the mobility contribution from ionized impurity scattering, and μ_{disl} is the mobility contribution from dislocation-induced scattering. According to Fig 4(a), the window in which ionized impurity scattering dominates (Regime I) narrows, going from Sample A to Sample D. Conversely, the window in which dislocation-induced scattering

dominates (Regime II) widens, going from Sample A to Sample D. The relatively large
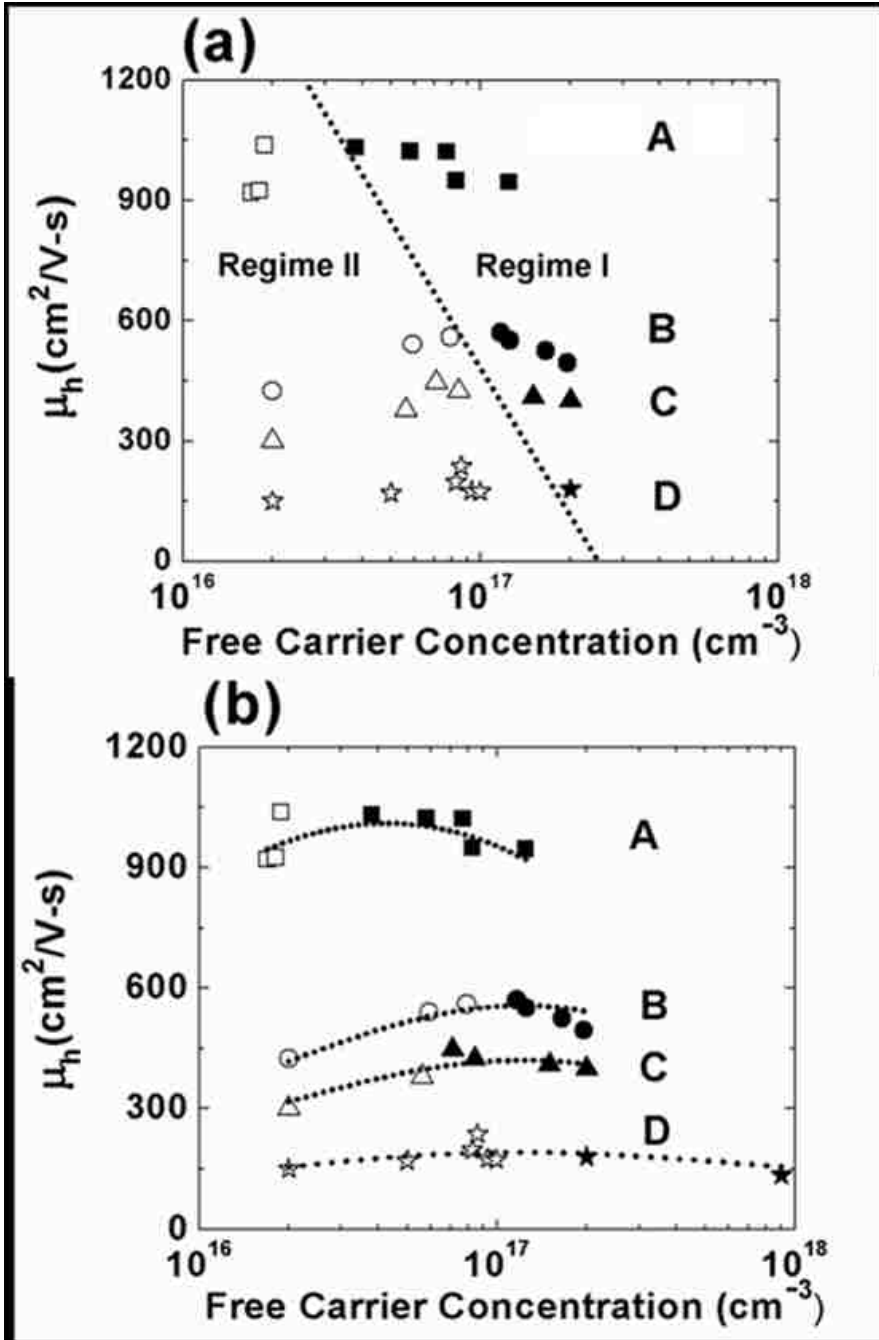
Figure 6.4: (a) Hole mobility (μ_h) as a function of net free carrier concentration in p-GoS films. Two types of symbols are used to represent the specific transport characteristics of four different p-GoS samples. The open symbols are used to represent Regime II for Samples A-D, where the mobility is largely determined by dislocation scattering. The solid symbols are used to represent Regime I for Samples A-D, where the mobility is largely determined by ionized impurity scattering. (b) shows the comparison between experimental data and analytical model for the mobility. The model tracks the

experimentally measured mobility (Regime I and II) very well for Sample A, but the goodness of fit decreases with increasing TDD.

impurity scattering window for Sample A reflects its low TDD compared to the other three samples.

Figure 6.4(b) shows both theoretically calculated and experimentally measured hole mobilities. The dotted lines trace the hole mobility, calculated from Eqs. (6-1)-(6-4), as a function of free carrier concentration (n) ranging from 1.0×10^{16} to 1.0×10^{18} cm^{-3}. For Sample A, we set $N_{disl} = 2 \times 10^7$ cm^{-2}, $N_r = 1.6 \times 10^{17}$ cm^{-3}, and $\alpha = 0.7$, while varying d and f. The best fit results from $d = 2.236$ μm and $f = 0.94$. The theoretical and experimental results agree well for Sample A with the goodness of fit R^2 at 0.9, whereas the goodness of fit deteriorates for Samples B-D. We speculate that this disagreement stems from the inaccurate estimation of f. The comparison between model and experiment in Fig. 6.4(b) leads to two important observations: (i) f increases with increasing N_{disl} and (ii) in Regime II, μ increases much more sensitively with increasing n for Sample A than Samples B-D. The increasing occupancy rate (f) can be attributed to the increasing number of active deep acceptor levels within the Ge band gap. The Coulombic potential of the ionized threading dislocation cores increases with these increasing deep acceptor levels. The increasing potential around the dislocation core interferes with the movement of Fermi-level, and it is reasonable to expect that the likelihood of Fermi-level pinning increases with increasing N_{disl}. We can deduce from observation (ii) that the amount of doping density that is needed to compensate for the increasing amount of charges around dislocation cores increases with increasing N_{disl}. As a result, the transition from dislocation-induced scattering Regime II to ionized-impurity-scattering Regime I occurs over a wider window

of n with increasing N_{disl}. That is, the mobility (μ) becomes less sensitive to n as N_{disl}

increases.
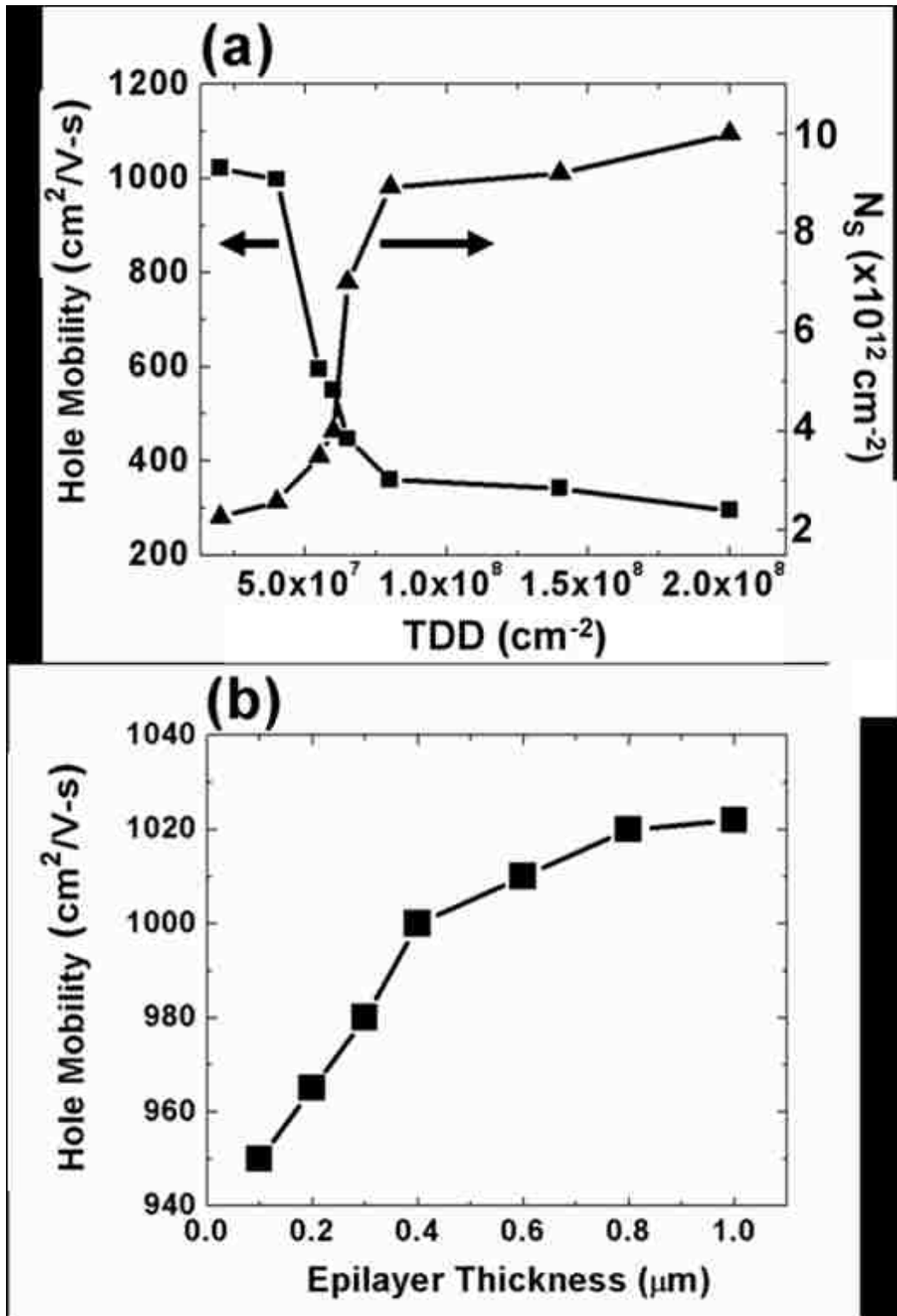
Figure 6.5: (a) Hole mobility (μh) and sheet-carrier density (NS) measured by Hall measurement at room temperature as a function of dislocation density. (b) The hole mobility (μh) measured as a function of the epilayer thickness.

Figure 6.5(a) shows the hole mobility and sheet carrier density as a function of defect density at 300 K for Samples A – D. We note that the mobility values of 1020, 650, 450 and 300 cm^2/V-s for Samples A – D correspond to sheet carrier densities (N_S) of 2.5×10^{12}, 4.0×10^{12}, 7.0×10^{12} and 2.0×10^{13} cm^{-2}, respectively. The sheet carrier density increases by almost an order of magnitude for Sample D compared to Sample A, while the Hall coefficient ($R_S = [qN_S]^{-1}$) decreases by almost an order of magnitude for Sample D compared to Sample A. This suggests that the dislocations originating from the Ge-Si interface substantially contribute to the sheet carrier density with increasing N_{disl} from Sample A to D.

Figure 6.5(b) shows the hole mobility as a function of Ge epilayer thickness for Sample A. The mobility is measured with samples of different Ge film thickness. With increasing thickness, the mobility empirically follows an exponential form given by

$$\mu(\text{d})=\mu_{\text{sat}}[1\text{-exp(-d}/\gamma)],\qquad\qquad(6\text{-}5)$$

and settles to a value of 1020 cm^2/V-s (μ_{sat}) at approximately 1 µm away from Ge-Si interface. In this fit, d is epilayer thickness and γ is the characteristic length over which the mobility increases from the Ge-Si interface. This γ correlates very well with the characteristic length over which the TDD decreases (~1 µm) from the Ge-Si interface[201]. Our previous work [201] shows that the minority carrier lifetime in the Ge epilayer also rises to its maximum value approximately 1 µm from the Ge-Si interface.

6.5.2. Current-Voltage Characteristics of Metal-Semiconductor Schottky Contact

Schottky barrier is essential for fabricating MESFETs. However, Ohmic behavior is often observed on p-type Ge Schottky diodes [190,191] regardless of the difference in metal work functions. This Ohmic response stems from Fermi level pinning[191]. In order to unpin the Fermi level and attain Schottky characteristics from p-type Ge, a thin (~1 nm) dielectric layer can be inserted between the metal and Ge[191]. The interfacial dielectric layer act as a dangling bond terminator at the Ge surface and consequently reduces the surface charge trap density, which originally pinned the Fermi level. By inserting a dielectric layer, the current-voltage (*J-V*) characteristics change from quasi-Ohmic to rectifying for p-type Schottky diodes.

To determine the optimum dielectric layer thickness, we have measured the room temperature *J-V* characteristics on Ti/SiO$_2$/GoS samples, in which the SiO$_2$ thickness is varied from 0.5 to 2 nm. Figure 6.6(a) shows that the ON/OFF ratio or the forward-to-reverse current density ratio on the aforementioned gate stack increases with increasing SiO$_2$ thickness, but reaches a constant level of approximately 50 as the SiO$_2$ thickness exceeds 1.3 nm. We deduce from Fig. 6.6(a) that the SiO$_2$ layer effectively unpins the Fermi level as the thickness exceeds 1.3 nm and that the *J-V* characteristics transition from quasi-Ohmic to rectifying.

Following the SiO$_2$ thickness optimization, we have investigated how different dielectric layers (i.e., SiO$_2$, Al$_2$O$_3$, and HfO$_2$) affect the *J-V* characteristics. For due comparison, the thickness of the dielectric layer is kept constant at 1.3 nm. Figure 6.6(b) shows the room temperature *J-V* characteristics of the Schottky diodes fabricated from Ti

gate and p-type GoS substrates. We have tested the three different dielectric layers (i.e.,
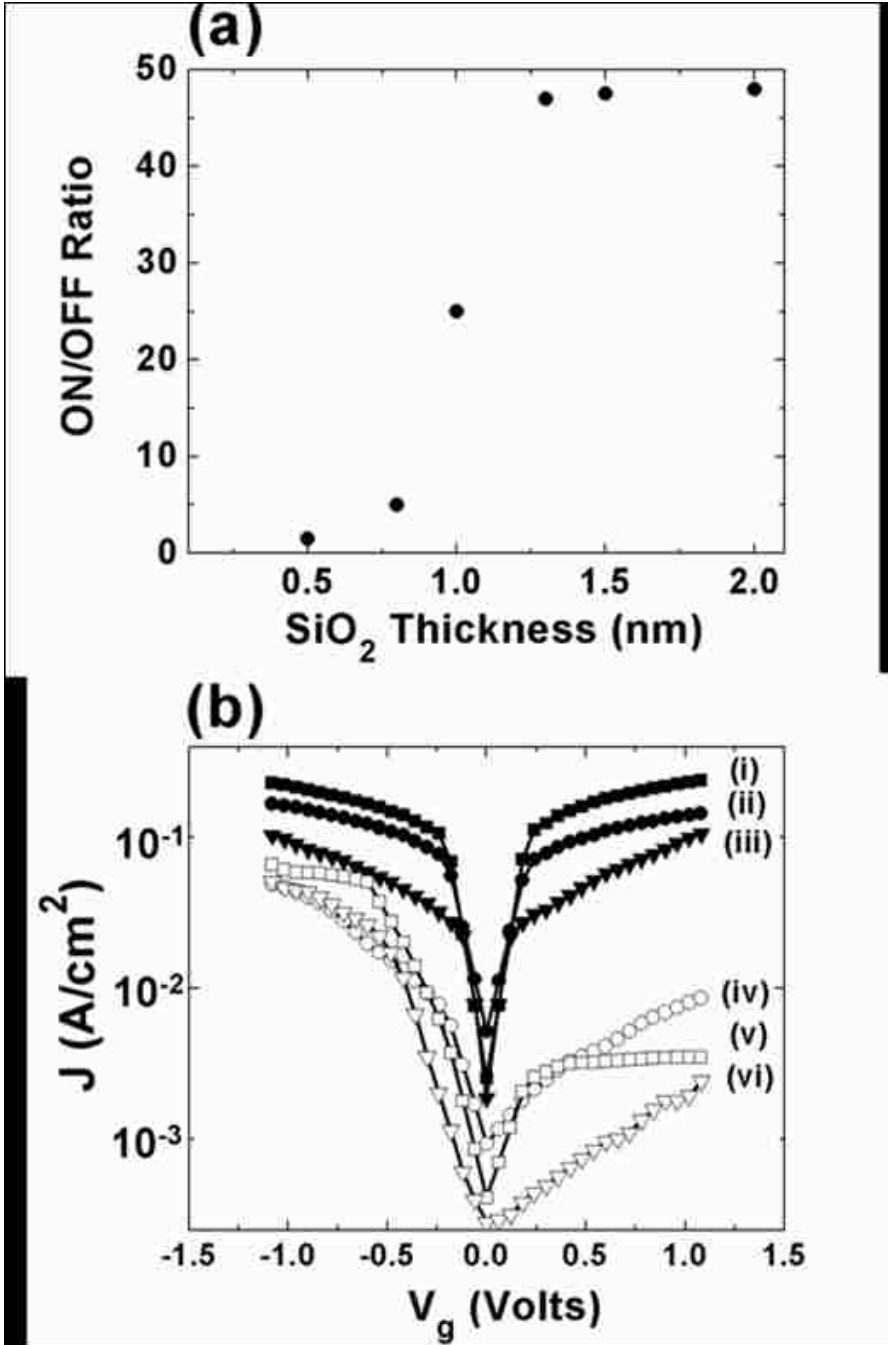
Figure 6.6: (a) The room temperature ON/OFF ratio (forward to reverse current density ratio) from Ti/SiO$_2$/p-GoS Schottky diode stack on Sample A as a function of varying SiO$_2$ thickness. (b) Forward-bias and reverse-bias Schottky characteristics with three different dielectric layers (i.e., SiO$_2$, Al$_2$O$_3$ and HfO$_2$). (i)-(iii) represent Schottky characteristics from Sample D, and (iv)-(vi) represent Schottky characteristics from Sample A.

SiO$_2$, Al$_2$O$_3$, and HfO$_2$) for GoS samples grown by four different methods (Sample A –

D). For the purpose of clarity, Figure 6.6(b) plots results from only Sample A and D.

Independent of the dielectric layer, Sample D does not exhibit the rectifying behavior of

typical Schottky diodes, and a large reverse leakage current density (J_S) exists with all

three dielectric layers (i-iii). For Sample D, which has the highest TDD amongst the four

samples, the forward-to-reverse current density ratio is approximately unity, clearly

showing Ohmic J-V characteristics instead of Schottky diode characteristics.

In contrast, Sample A, which has the lowest TDD amongst the four

samples, shows the rectifying Schottky diode characteristics. Compared to Sample D, the

forward current density with all three dielectric layers (iv-vi) shows a slight decrease in

magnitude, whereas the reverse leakage current density (J_S) shows a more strongly

pronounced decrease. That is, the decrease in dislocation density significantly improves

the reverse current characteristics. With the clear improvement in the reverse leakage

current, HfO$_2$ (vi) shows the best reverse Schottky characteristics amongst the three

dielectric layers, where the ON/OFF current ratio is approximately 250 with the reverse

bias (V_g) at 0.25V. This dislocation-density-dependent reverse leakage current density

(J_S) can be described by [197]

$$J_S = \frac{I_S}{A_e(1-\pi r^2 [TDD])} = A^* T^2 exp(-\sqrt{\zeta}\delta) exp(\frac{-q\phi_{bo}}{kT}) \quad , \qquad (6\text{-}6)$$

where I_S, A_e, r, [TDD], A^*, T, ζ, δ, q, ϕ_{b0}, and k denote reverse leakage current, metal-

semiconductor interface area, effective radius of a cylinder surrounding each threading

dislocation, threading dislocation density per unit area, Richardson constant (40.8 for

Ge), temperature (300 K), dielectric layer barrier height, interfacial dielectric layer

thickness, unit charge, effective Schottky barrier height (~0.3517 eV), and Boltzmann constant, respectively. The $\exp(-\sqrt{\varsigma}\delta)$ term represents the tunneling probability through the dielectric layer.

Noting that HfO_2 provides the best reverse leakage current characteristics amongst the three dielectric layers, we focus on comparing the *J-V* characteristic of Schottky diodes fabricated from Sample A and D [case (iii) and (vi)], where HfO_2 is inserted as the dielectric interfacial layer. At reverse bias of approximately 0.25V, the corresponding J_S of Sample A and D is 2×10^{-4} and 3.9×10^{-2} A/cm^2. For Eq. (6), I_S and J_S are experimentally measured, A_e is fixed at 400 µm × 2.5 µm, and *[TDD]* is 2×10^7 and 2×10^8 cm^{-2} for Sample A and D, respectively. Based on these values, the effective radius *r* is 1.2 µm to 380 nm for Sample A and D. This suggests that in Sample D, the interdistance between cylindrical dislocation cores is shorter than that in Sample A. The proximity of dislocation cores and the electric field around the cores in turn render the tunneling probability for Sample D greater than that of Sample A. In addition to the electric field, dislocations introduce trap states near the valence band edge for p-type Ge film, and the holes can tunnel through these trap states making the tunneling probability larger for Sample D than Sample A. Based on Eq. (6-6), we extract the tunneling probability for Sample A and D to be 1.26×10^{-3} and 0.13. That is, the tunneling probability is approximately two orders of magnitude greater in Sample D than in Sample A. This explains why Schottky diodes from Sample A show a smaller reverse leakage current density and a greater ON/OFF ratio than Schottky diodes from Sample D.

6.5.3. *C-V* Characterization and Interface Trap Density

While a low TDD and the use of a thin HfO_2 layer render Schottky diode characteristics for the Ti-Ge interface, we have further characterized the interface by *C-V* measurements to estimate the interfacial trap density (D_{it}). A decrease in D_{it} resulting from the decrease in TDD and the use of a thin dielectric layer between metal and semiconductor can be used as another indicator of improving metal-semiconductor interface. Defects strongly affect the electrical characteristics of metal-semiconductor interface, in particular, the *C-V* characteristics of the junction[202]. Therefore, the *C-V* characteristics provide a very convenient means of detecting and characterizing a low concentration of defects (e.g., deep traps) [203].

The gate-to-channel capacitance is measured on the Ti/dielectric/GoS stack, using the split *C-V* technique. Figure 6.7(a) shows a cross-sectional transmission electron microscopy (XTEM) image of the Ti/dielectric/GoS stack on Sample A, where the physical thickness of the dielectric layer is approximately 1.3 nm. The crystalline Ge layer is shown at the bottom part of Fig. 6.7(a). Based on XRD measurements (not shown here), the substrate has a residual tensile strain of 0.27%. The residual tensile strain is largely a result of the 116 % mismatch in thermal expansion coefficients of Ge and Si. This tensile strain is expected to enhance the hole mobility. Figure 6.7(b) shows a z-contrast scanning-TEM (STEM) image of the Ge and Si interface. The irregular boundary at the Ge-Si interface suggests Ge-Si interdiffusion, which increases with the number of annealing steps. The interdiffusion helps reduce the stress stemming from the lattice mismatch[204].
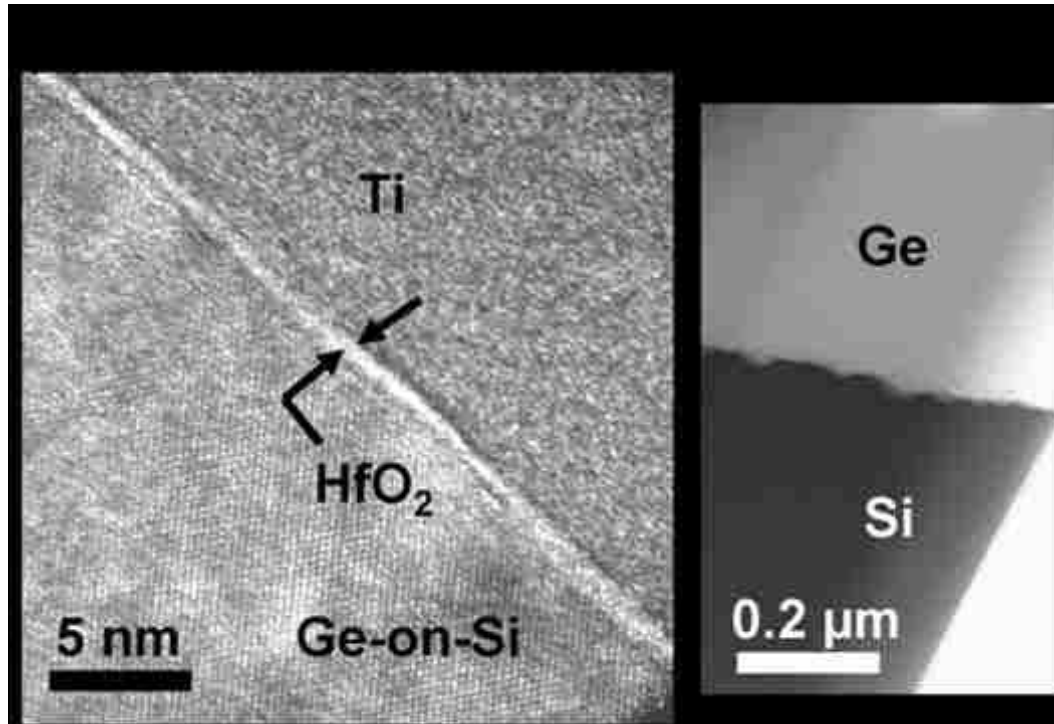
Figure 6.7: (a) High-resolution, cross-sectional TEM image of Ti/1.3-nm HfO$_2$/p-GoS stack and (b) corresponding STEM image.

To complement the reverse leakage current measurements, we compare the *C-V* characteristics from the three different dielectric layers with varying TDDs. Figure 6.8(a) shows the *C-V* characteristics of Ti/1.3 nm-SiO$_2$/p-GoS stack for Samples A-D. All *C-V* measurements are performed at 100 kHz, except for the quasi-static *C-V* measurement. For Sample A, we observe a minor peak near the gate bias of 0 V. We also note that the capacitance shows a peak at the forward gate bias of approximately -0.8 V, and the capacitance decreases with increasing forward bias ($V_{gs} < -0.8$ V) instead of remaining constant. These *C-V* characteristics suggest the presence of a large density of surface states despite the lowest TDD for Sample A[205]. Furthermore, with increasing TDD, the ratio between forward-bias and reverse-bias capacitances decreases: 7.9, 3.3, 1.1 and 0.87 for Samples A-D, respectively. In fact, the *C-V*

characteristics progressively deteriorate going from Sample A to Sample D because of

the   increasing
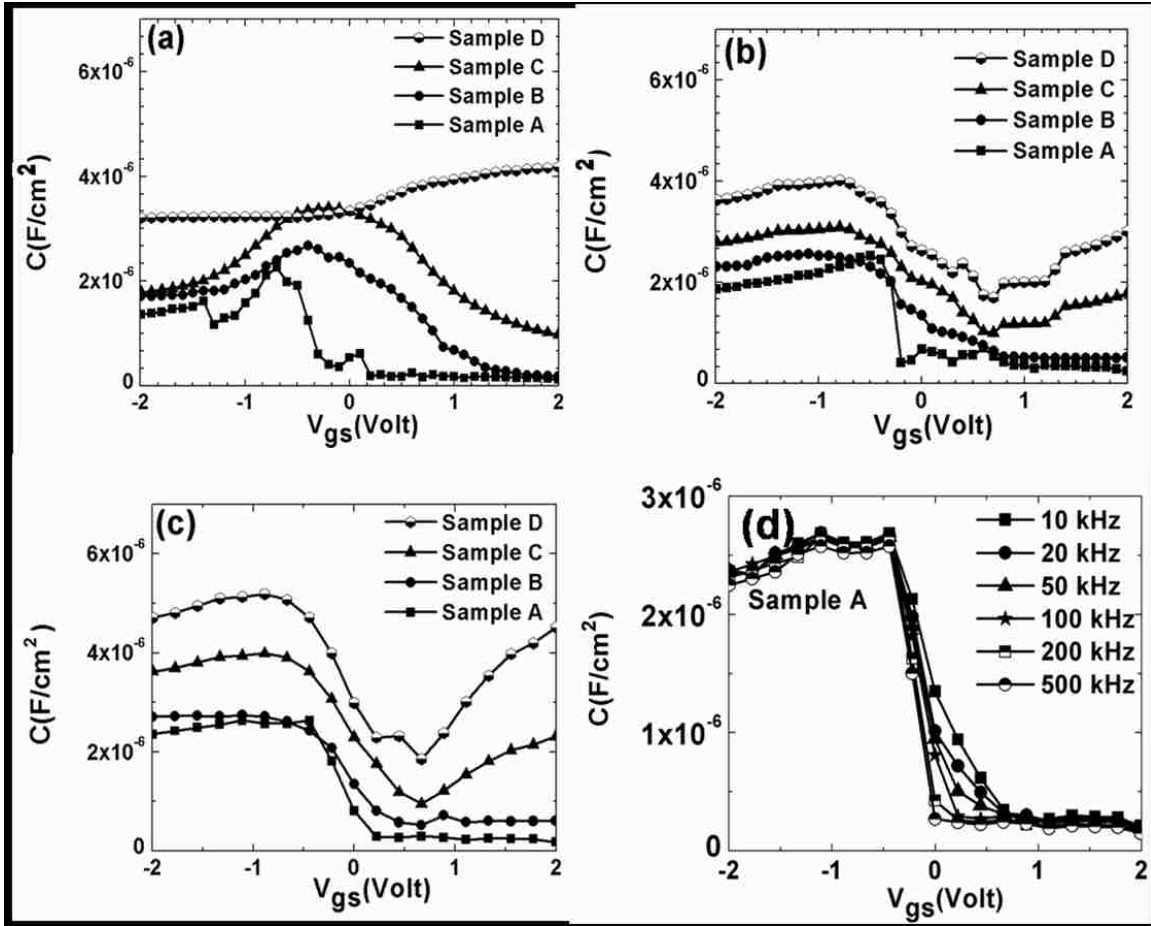
Figure 6.8: C-V characteristics of Ti/1.3-nm dielectric/p-GoS Schottky contacts for Samples A-D with three different dielectric layers: (a) SiO_2, (b) Al_2O_3, and (c) HfO_2. The C-V characteristics are obtained using split C-V technique. The C_{HF} is obtained at 100 kHz.

TDD. In particular, Sample D shows a quasi-Ohmic response with the largest leakage

current. The above observations follow typical metal-semiconductor *C-V* characteristics,

transitioning from Schottky to Ohmic with an increasing number of defect centers on the

semiconductor surface.

Figure 6.8(b) and 6.8(c) show the *C-V* characteristics of Ti/1.3 nm-Al$_2$O$_3$/p-GoS and Ti/1.3 nm-HfO$_2$/p-GoS Schottky contacts, respectively, for Samples A – D. In the case of Al$_2$O$_3$ on Sample A, the capacitance abruptly increases for V_{gs} < -0.4 V, and the decrease in forward-bias capacitance for V_{gs} < -0.8 V is less pronounced than that for the SiO$_2$ case. In addition, the ratio between forward-bias and reverse-bias capacitances is improved by replacing SiO$_2$ with Al$_2$O$_3$: 10.8, 15.5, 2.43 and 1.76 for Samples A – D. However, the best *C-V* characteristics are obtained when HfO$_2$ is inserted between metal and p-GoS. In a sharp contrast to SiO$_2$ and Al$_2$O$_3$, Fig. 8(c) does not shows peaks or an abrupt increase in the capacitance with forward bias. The ratio between forward-bias and reverse-bias capacitances is further improved: 13.8, 16.8, 2.75 and 2.13 for Samples A – D. The absence of peaks and abrupt increase indicates that HfO$_2$ effectively passivates the surface states.

Figure 6.8(d) additionally shows frequency-dependent *C-V* responses (10 kHz to 500 kHz) for the Ti/1.3 nm-HfO$_2$/p-GoS Schottky contacts. The *C-V* characteristics for the forward gate bias in the range of -0.3 to -2 V represent accumulation of holes at the HfO$_2$/p-GoS interface. The accumulation capacitance is not sensitive to frequency and shows small dispersion (<5%/decade). In contrast, the multi-frequency *C-V* responses in the gate bias region of 0 to 0.8 V exhibit typical characteristics of interfacial defects at the HfO$_2$/Ge interface. In this range of gate bias, the measured capacitance is strongly sensitive to ac signal frequency. However, the frequency dispersion is considerably larger in the range of 10 to 50 kHz, compared to the higher range of 100 to 500 kHz, indicating that slow interfacial trap states are present near the conduction band edge.

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To assess how forming gas anneal (FGA) further reduces the surface states, we have prepared Ti/1.3 nm-SiO$_2$/p-GoS, Ti/1.3 nm-Al$_2$O$_3$/p-GoS, and Ti/1.3 nm-HfO$_2$/p-GoS stacks with the lowest TDD (Sample A) and measured their C-V characteristics with and without the FGA step. Based on the high-frequency and quasi-static C-V measurements, the interfacial trap density (D_{it}) [206] is then estimated for the metal-dielectric-semiconductor stacks. The unidirectional quasi-static capacitance per unit area (C_{QS}) is measured based on

$$C_{QS} = I \bigg/ \left(\frac{\partial V}{\partial t} \right),$$

(6-7)

where I is the measured current, and $\partial V/\partial t$ is the ramp rate of V_{gs} maintained at 0.1 V/s. The unidirectional quasi-static capacitance (C_{QS}) extracted from Eq. (6-7), with and without FGA, is 2.5×10^{-6} and 4.1×10^{-6} F/cm^2 for SiO$_2$, 2.2×10^{-6} and 3.2×10^{-6} F/cm^2 for Al$_2$O$_3$, and 2.3×10^{-6} and 3.1×10^{-6} F/cm^2 for HfO$_2$, respectively. The high-frequency capacitance (C_{HF}) is measured at 100 kHz, with and without FGA: 1.7×10^{-6} and 1.9×10^{-6} F/cm^2 for SiO$_2$, 2.0×10^{-6} and 2.4×10^{-6} F/cm^2 for Al$_2$O$_3$, and 2.2×10^{-6} and 2.7×10^{-6} F/cm^2 for HfO$_2$, respectively.

The interfacial trap density (D_{it}) is then calculated from C_{QS} and C_{HF} for all three dielectrics by

$$D_{it} = \frac{C_{OX}}{q} \left\{ \frac{\left(C_{QS}/C_{OX} \right)}{\left[1 - \left(C_{QS}/C_{OX} \right) \right]} - \frac{\left(C_{HF}/C_{OX} \right)}{\left[1 - \left(C_{HF}/C_{OX} \right) \right]} \right\},$$

(6-8)

where C_{OX} is the equivalent oxide capacitance per unit area, q is the unit charge, and C_{HF} is the high-frequency capacitance per unit area. Figure 6.9(a) shows D_{it} as a function of Ge energy within its bandgap (BG) with SiO$_2$, Al$_2$O$_3$, or HfO$_2$ before and after FGA at 350 ºC for 15 min. Based on Eq. (8), the as-deposited D_{it} levels are approximately

5×10^{13}, 1.3×10^{13}, and 8×10^{12} cm^{-2} eV^{-1} for SiO_2, Al_2O_3, and HfO_2, respectively, on p-type GoS. After the FGA, the D_{it} level decreases by approximately a factor of 5 to 1×10^{13}, 3×10^{12}, and 1.6×10^{12} cm^{-2} eV^{-1}.
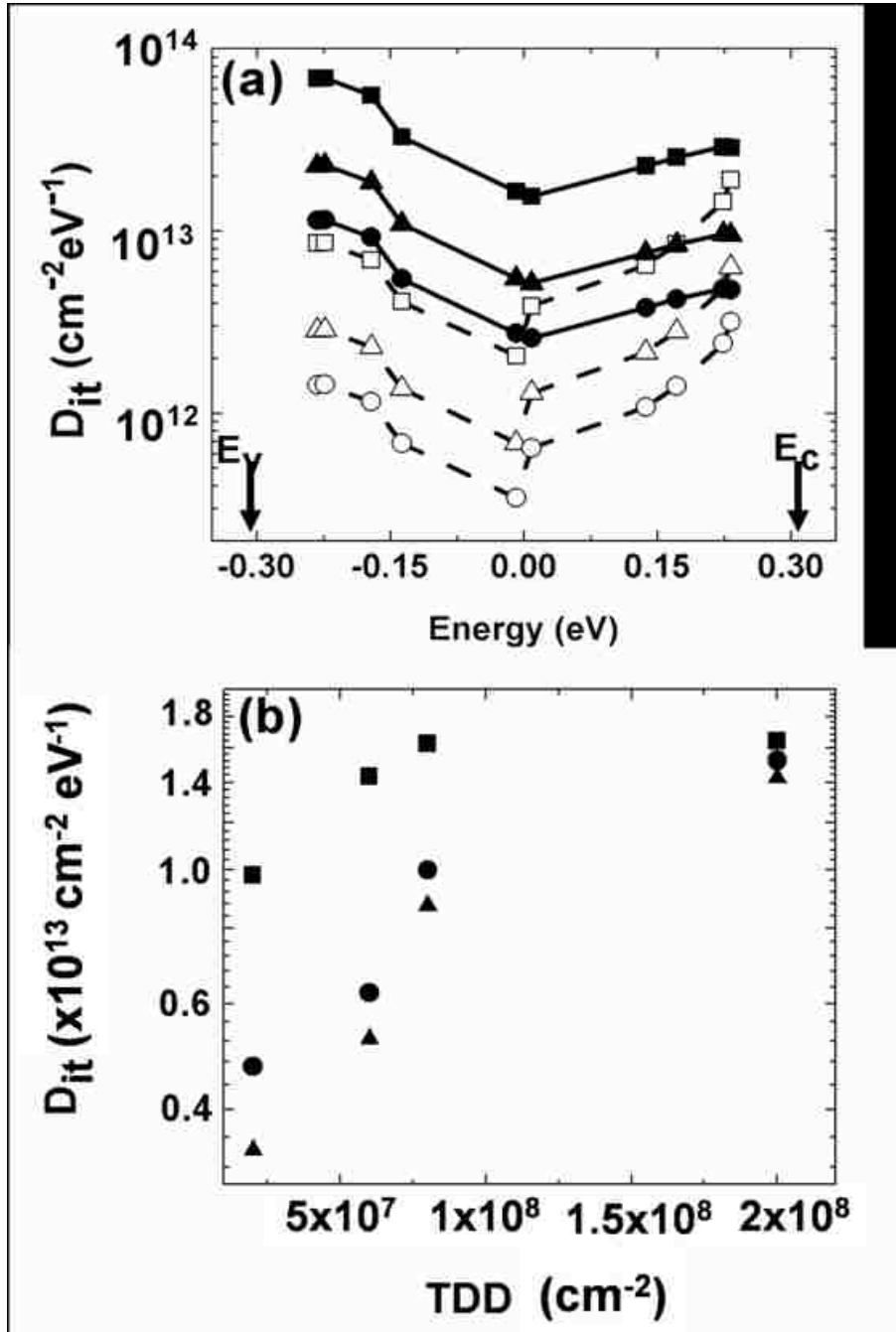
Figure 6.9: (a) Dit as a function of Ge energy surface potential before and after FGA at 350 ∘C for 15 min. The energy surface potential axis is labeled with the convention that

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0.0 V represents the mid-gap position (Ei), -0.33 V represents the VB edge and 0.33 V represents the CB edge. D_{it} levels for three different dielectric layers are shown in the image. (b) Near-VB-edge D_{it} as a function of defect density for SiO_2, Al_2O_3 and HfO_2.

The horizontal axis in Fig. 6.9(a) corresponds to the energy. The energy label follows the convention that 0 V represents the mid-gap position (E_i), while a positive energy samples the upper half of the BG toward the conduction band (CB) edge (E_C), and a negative value explores the lower half of the BG toward the valence band (VB) edge (E_V). However, energy calculations are often subject to errors due to several parameters, such as doping and interface charge nonuniformities. Considering these unknown variables that can introduce errors into calculations, the mid-level D_{it} distributions within the BG should be interpreted qualitatively. Fig. 6.9(a) shows that in all three dielectric cases, the lower-half D_{it} (near the VB edge) values are greater than the mid-level D_{it} values (mid-gap position). The minimum D_{it} values obtained from SiO_2, Al_2O_3, and HfO_2 for with and without FGA are 3×10^{12} and 1.5×10^{13}, 1×10^{12} and 5×10^{12}, and 6×10^{11} and 3×10^{12} $cm^{-2}\,eV^{-1}$, respectively. The minimum D_{it} shown at the mid-gap for all three samples indicates that their impurity densities are approximately equal. Therefore, we deduce that the overall decrease in experimentally obtained D_{it} for both un-annealed and FGA samples is strictly because of different dielectric layers. In each group, the D_{it} near the VB edge decreases, as the dielectric layer changes from SiO_2 to Al_2O_3 to HfO_2. We attribute this decrease in D_{it} to the decrease in unpassivated bonds per unit area at the dielectric/Ge interface, as the dielectric layer changes from SiO_2 to Al_2O_3 to HfO_2. Since the unpassivated bonds can cause hole scattering, one can expect the hole mobility to improve as the dielectric layer changes from SiO_2 to Al_2O_3 to HfO_2, and our later results with MESFETs will show that the greatest hole mobility is obtained

with Ti/1.3 nm-HfO$_2$/p-channel GoS MESFETs fabricated from epitaxially grown Ge on SI-Si substrates. We have also observed that after FGA, relatively higher D_{it} exits at the upper-half of the band gap; a similar observation is made in metal-oxide-semiconductor capacitors by other investigators[207]. These characteristics can be attributed to a greater number of filled-acceptor states that are always present in the upper-half of the band gap close to E_C edge. Thus, the decrease in D_{it} is less pronounced with decreasing TDD near the CB, compared to the decrease in D_{it} near the VB.

Figure 6.9(b) shows near-VB edge D_{it} for a range of TDD values after FGA with SiO$_2$, Al$_2$O$_3$ and HfO$_2$. We observe that a large near-VB edge D_{it} exists in a large TDD sample such as 2×10^8 cm^{-2} (Sample D) in all three dielectrics. In fact, with the large TDD, the D_{it} values from all three dielectric layers converge to a relatively constant level of 1.6×10^{13} cm^{-2} eV^{-1}. In contrast to the large TDD range, the near-VB edge D_{it} values corresponding to the low TDD show a clear improvement with the use of HfO$_2$. For Sample A with 2×10^7 cm^{-2} TDD, in particular, the Ti/1.3 nm-HfO$_2$/p-GoS stack exhibits 2 and 5 fold improvement in near-VB edge D_{it}, compared to Ti/1.3 nm-Al$_2$O$_3$/p-GoS and Ti/1.3 nm-SiO$_2$/p-GoS stacks.

6.5.4. *J-V Characteristics and External Transconductance of MESFETs*

Based on the Schottky *J-V* characteristics as well as *C-V* and D_{it} profiles discussed above, the use of HfO$_2$ as an insertion layer between gate metal and p-GoS improves the electrical performance of the metal-semiconductor interface. Therefore, for the MESFET device characterization, we have strictly used HfO$_2$ and considered four different TDDs (Samples A-D). Figure 6.10 shows the *J$_{ds}$–V$_{ds}$*

characteristics of our MESFETs operated in enhancement mode at room temperature for

Samples A-D. The gate bias is scanned from 0 to -0.5 V by 0.1 V steps. For Sample A,

the J_{ds} is approximately 5×10^{-3} A/cm^2 at zero gate bias (V_{gs} = 0 V), indicating that the

channel is essentially pinched off.   In comparison, the increasing TDD
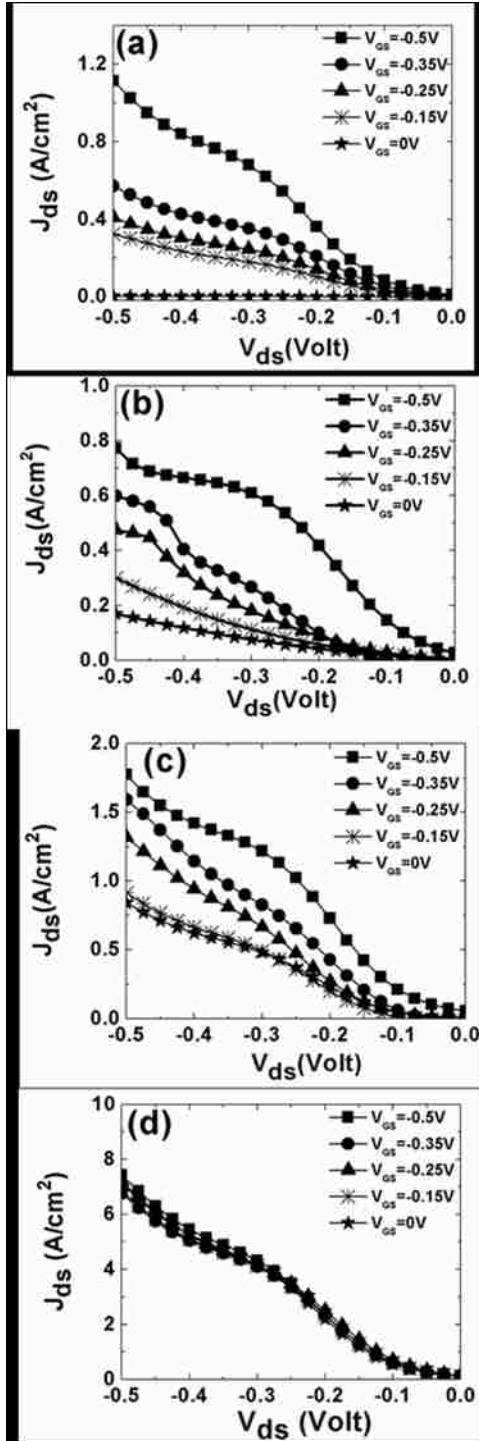
Figure 6.10: Figures 6.10 (a-d) correspond to the $J_{ds} - V_{ds}$ characteristics obtained from four different TDD samples (Samples A-D). The gate bias is increased from 0 to -0.5 V at 0.1 V steps.

leads to increasing J_{ds} at zero gate bias by a factor of 40, 160, and 1400, for Samples B-D, indicating that the channel cannot be pinched off when the dislocation density is high. This deteriorating performance can be explained by the VB edge shift with increasing TDD. As the TDD increases, an increasing number of defect states near the VB edge lead to Fermi level pinning and a large positive shift in the threshold voltage (V_{th}), which subsequently cause an overall increase in J_{ds} and loss of V_{gs} dependence.

At a forward bias of $V_{ds} = $ -0.5 V, the J_{ds} is approximately 1.2, 0.8, 1.8, and 7 A/cm^2 for Samples A-D, respectively. Overall, the saturation current density increases with increasing TDD. While we report J_{ds} at $V_{ds} = $ -0.5V, we note that J_{ds} does not fully saturate for all four samples. In fact, with increasing TDD, the continuous rise in J_{ds} becomes more pronounced, and the J_{ds}–V_{ds} slope in the saturation region becomes steeper. We attribute the imperfect saturation in J_{ds} to the increasing total magnitude of electric field surrounding the dislocation network with increasing TDD, behaving as an additional load and a leakage current path[208].

To further analyze the transfer J-V characteristics, the gate bias (V_{gs}) is scanned from 0 to -0.5V by 0.1 V steps, while V_{ds} is kept constant at -0.5 V for Samples A-D. Figure 6.11(a) shows normalized $\bar{J}_{ds}$ vs. V_{gs} measured at 300 K. The drain current is normalized to J_{ds} at $V_{gs} = 0$ V. The normalization is done intentionally in order to qualitatively capture how dislocations affect J_{ds}. For Sample A, $\bar{J}_{ds}$ ranges from 1 to approximately 23, as V_{gs} varies from 0 to -0.5. In comparison, the variation in $\bar{J}_{ds}$ becomes less sensitive to V_{gs} for Samples B-D. In the case of Sample D, $\bar{J}_{ds}$ becomes virtually independent of V_{gs} and remains constant, showing that the forward and transfer

characteristics of MESFETs significantly deteriorate with increasing TDD. The inset in
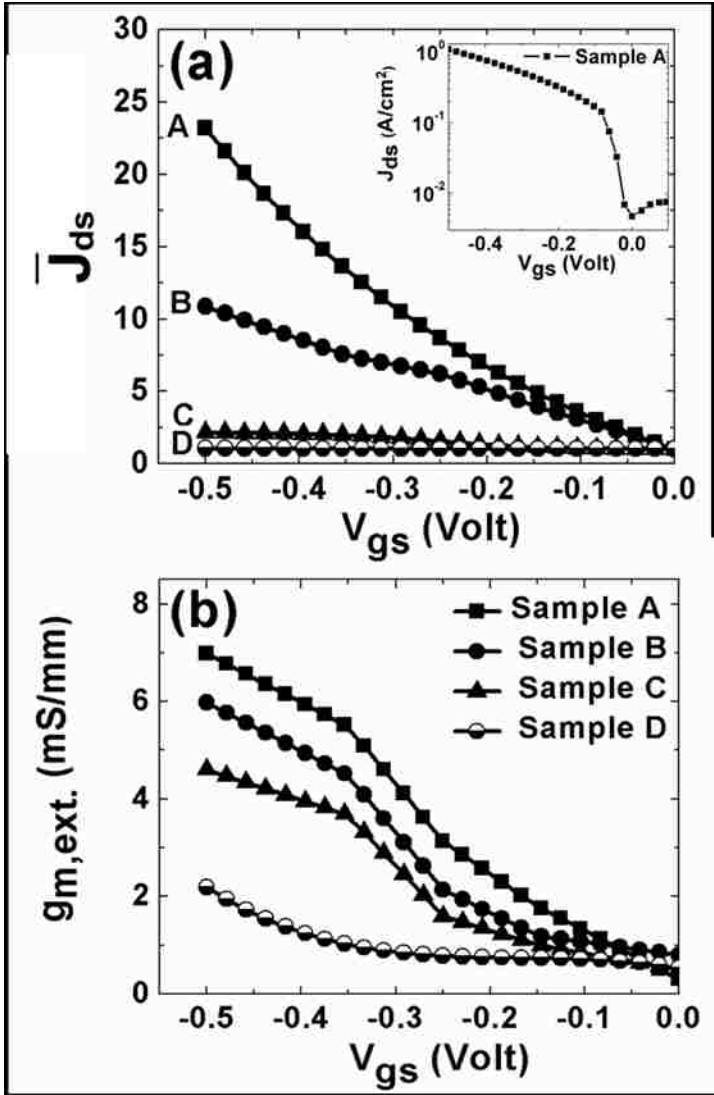
Figure 6.11: (a) Normalized vs. V_{gs}. Inset shows $J_{ds} - V_{gs}$ characteristics obtained from Sample A with HfO_2 interfacial layer. (b) $g_{m,ext}$ vs. V_{gs} for Samples A-D. V_{ds} is biased at -0.4 V to be in the saturation region. These measurements are performed at 300 K.

 Fig. 11(a) further shows the transfer characteristics in absolute current density J_{ds} vs. V_{gs}

for our MESFETs fabricated from Sample A with HfO_2 interfacial layer. J_{ds} ranges from

1.2 to approximately 4×10^{-3} A/cm^2, as V_{gs} varies from -0.5 to 0.2 V, while V_{ds} is kept

constant at -0.5 V. The transfer curve for Sample A follows $I_{ds}^{1/2}$ dependency, as the

applied V_{gs} varies from -0.5 to 0.2 V.   The forward J_{ds} or ON current density with

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negative V_{gs} shows a steep subthreshold swing in the linear regime, whereas the reverse J_{ds} or OFF current density with positive V_{gs} shows a very low drain current density.

As a measure of characterizing transistor speed, we have extracted the external transconductance ($g_{m,ext}$) from J_{ds}-V_{gs} characteristics of MESFETs for Samples A-D. Figure 6.11(b) shows that the $g_{m,ext}$ peak value reaches approximately 7 mS/mm for Sample A. This peak value decreases by a factor of 0.86, 0.64 and 0.29, respectively, for Samples B-D. This result is another evidence that dislocations behave as scattering as well as recombination centers for charge carriers and slow down the carrier response to changes in V_{gs}.

While the hole mobility from Hall measurements is a good indicator of carrier transport in the epilayer, the room-temperature, low-field, effective hole mobility ($\mu_{h,eff}$) is a more representative indicator of transistor performance. Figure 6.12 shows $\mu_{h,eff}$, extracted from J_{ds}-V_{ds} measurements, as a function of the effective electric field E_{eff}. The effective hole mobility of MESFETs fabricated from Sample D is omitted from the analysis because these devices cease to work as transistors due to its large TDD. The low-field condition is satisfied in the regime where J_{ds} responds linearly to V_{ds} (-0.25 To 0V). In this linear regime, $|V_{ds}| < |V_{dsat}|$, where V_{dsat} is approximately V_{gs}-V_{th}. When the channel for hole transport is not pinched off in the linear regime, the low-field $\mu_{h,eff}$ can be calculated by the following equation,

$$\mu_{h,eff} = \left\{ \left(\frac{L_g h}{\varepsilon_s W} \right) \left(\frac{1}{V_{gs} - V_{th}} \right) \left(\frac{\partial I_d}{\partial V_d} \bigg|_{V_g} \right) \right\} \quad , \tag{9}$$

where L_g and W are the gate length (2.5 µm) and width (~ 400 µm), h is the channel depth (~ 170 nm), ε_s is the channel permittivity (16.2 for Ge), V_{gs} is the applied
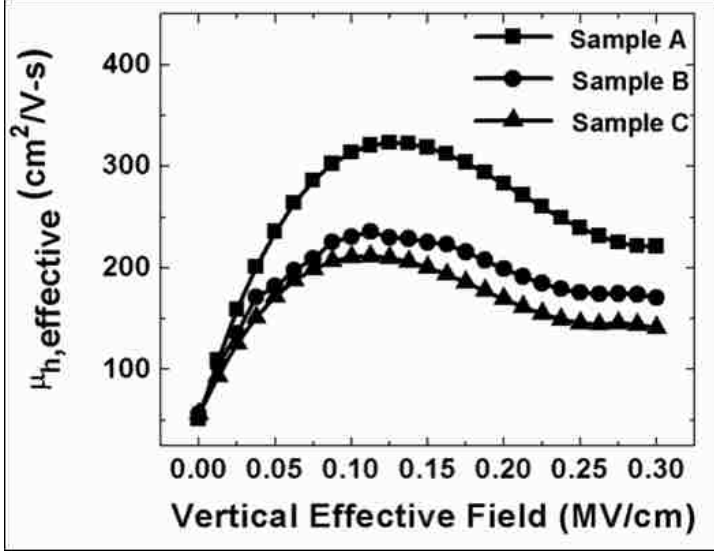
Figure 6.12: Effective hole mobility as a function of vertical electric field.

gate-bias, V_{th} is the threshold voltage, and $\left. \left(\partial I_d / \partial V_d \right) \right|_{V_g}$ corresponds to the slope from the J_{ds}-V_{ds} characteristic curve. The use of $\mu_{h,eff}$ measured against E_{eff} make it easy to compare with Si properties and standard *universal mobility*[209]. The low-field used for this comparison is 0.1 MV/cm. Consistent with the $\bar{J}_{ds}$-V_{gs} results, Figure 12 shows that $\mu_{h,eff}$ increases with decreasing TDD. The peak effective hole mobility measured from MESFETs fabricated on Sample A is approximately 307 cm^2/V-s, compared to 225 and 200 cm^2/V-s measured on Sample B and C. The effective peak mobility from Sample A exceeds bulk-Si universal mobility as well as recently reported values from $Si_{0.6}Ge_{0.4}$/SOI [38], relaxed Ge [28], and strained Ge [28] by a factor of 2.8, 1.75, 2.05 and 1.23, respectively.

Finally, in order to investigate the temperature dependent microwave performance of the GoS p-type MESFETs, the cut-off frequency (f_T) is calculated from $g_{m,ext}$ and L_g as

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a function of temperature. The cut-off frequency directly governs the MESFET speed;
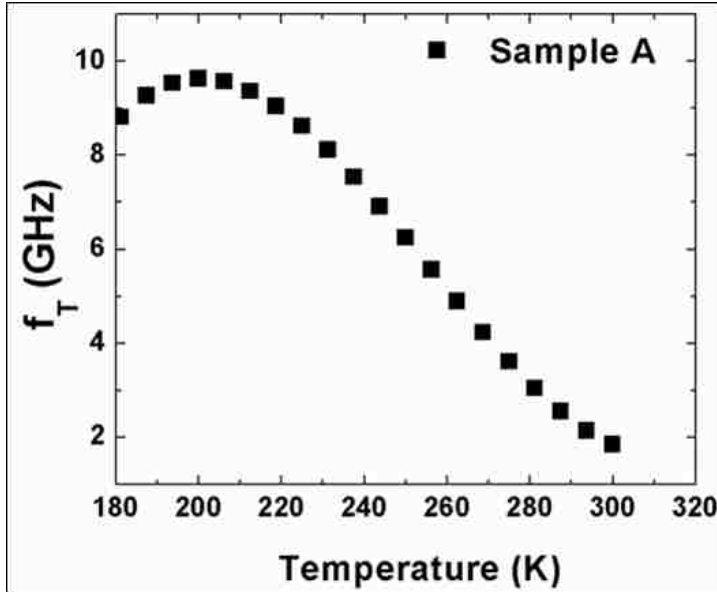
Figure 6.13: Cut-off frequency as a function of operating temperature at V_{ds} = -0.5 V.

the device speed increases with increasing f_T. Figure 6.13 shows f_T of MESFETs fabricated on Sample A with the thin HfO$_2$ dielectric layer and 2.5 μm gate length. f_T is approximately 10 GHz at 200K and 2 GHz at 300K. This decrease in f_T with increasing temperature can be attributed to the increasing number of trap charges at the elevated temperature, and subsequently the increasing emission of charges from the traps into the channel.

6.6   Conclusions

We have fabricated metal-semiconductor Schottky contacts as well as MESFETs on p-type Ge epitaxially grown on Si (GoS). The Ge film is grown at the wafer scale without mesas or limited-area growth. The electrical characteristics of these devices are analyzed with varying threading dislocation density (TDD), ranging from 2×10^7 to 2×10^8 cm^{-2}. In addition to the effect of threading dislocations on the electrical characteristics,

we have explored three different dielectric layers (SiO_2, Al_2O_3, and HfO_2) inserted between Ti and Ge to determine which dielectric layer unpins the Fermi level more effectively.

The Hall-measurements reveal that the hole mobility in Ge is 1020 cm^2/V-s with the low TDD samples. The hole mobility shows strong dependence on both TDD and the sheet charge carrier density. In general, the mobility decreases with increasing TDD. We also observe that when the dislocation-induced charge carrier scattering predominantly governs the mobility, the mobility increases with increasing sheet charge carrier density. This window of dislocation-induced scattering narrows as the TDD decreases.

For metal-gated Schottky contacts on GoS, the *J-V* electrical characteristics show that the use of thin (~1.3 nm) dielectric layer effectively unpins the Fermi level and that HfO_2 dielectric layer with the lowest TDD (2×10^7 cm^{-2}) shows the best ON/OFF current density ratio amongst the four different TDD samples. Furthermore, the use of HfO_2 improves the *C-V* characteristics and interfacial trap density (D_{it}) by lowering the unpassivated bonds per unit area that exist at the dielectric/Ge interface. In particular, the near-VB edge D_{it} value decreases with decreasing TDD.

The forward and transfer *J-V* characteristics of MESFETs show that the channel can be effectively pinched off with low TDD devices. However, we observe imperfect saturation in the forward J_{ds}-V_{ds} response, which can be attributed to the dislocation network that acts as an additional load and leakage path for the current. With the lowest TDD and use of HfO_2, the external transconductance extracted from transfer J_{ds}-V_{gs}

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measurements is 7 mS/mm, and the corresponding peak effective mobility is 307 cm^2/V-s. These values compare well with previously reported values.

6.7   Metal-Oxide-Semiconductor Field Effect Transistors

Using high-carrier-mobility materials, such as Ge, InGaAs, and InP, is a viable path to fabricate CMOS transistors with improved performance[210].In particular, Ge has been extensively studied due to its high hole mobility(×4 of Si).A thin layer of Ge buffer can also be used to integrate III-V channel materials on Si to achieve high electron mobility. These high-mobility materials have been epitaxially integrated on Si to reduce the material cost and ensure compatibility with the current Si IC manufacturing. However, growing high-quality films has been a considerable engineering challenge. Herein, we have epitaxially grown low-defect density, continuous Ge films on Si at the wafer scale without mesas or limited-area, using a simple two-step molecular beam epitaxy (MBE) technique[194] We have further tested the electrical film quality by fabricating and characterizing p- and n-MOSFETs.

6.8   Material Growth and Characterization:

Ge-on-Si (GoS) substrates have not been broadly used for commercial device applications due to significant engineering challenges in growing high-quality, low-defect-density Ge epilayer. However, a variety of methods exists today to reduce the defect density in GoS: e.g., graded Ge_xSi_{1-x}buffer layer [60] and epitaxial necking [82,152].These methods have had varying degrees of success, but they often require thick buffer layers, high temperature processing steps, or limited-area epitaxy. In particular, the epitaxial necking technique requires high-aspect-ratio dielectric windows

to terminate defects propagating from the Ge-Si interface. In comparison, we have implemented a simple two-step MBE growth technique in our laboratory[194].This self-templating growth begins with creating 5-7 nm diameter windows in a 1.4-nm-thick chemical SiO_2 on Si by Ge molecular beam exposure. This step is followed by selective nucleation of Ge islands on Si exposed within the nanoscale windows. Successive lateral growth and coalescence over the SiO_2 form a continuous Ge film covering the entire substrate. This technique is further improved by adding an annealing step during partial coalescence of Ge islands[2]that removes most of the stacking faults in the film. A similar approach was developed later by Nakamura *et al*[211].

Ge is grown on n- and p-type Si(100) ($\rho>$ 1-3 Ω-cm). Our improved growth procedure is described in a recent publication[212]. The film thickness after growth is approximately 1.3 µm and polished down to 1 µm for specular finish. Prior to device fabrication, we characterize the Ge film quality, using X-ray diffraction (XRD) and etch pit density (EPD). Figure 6.14(a) shows the Ge(004), Si(004), and Ge(331) diffraction peaks for our n- and p-type GoS substrates. The FWHM of Ge(004) peak measured from the 1-µm-thick Ge film is 100 and 230 arcsec for n- and p-type Ge, indicating high level of crystallinity. The FWHM values of Ge(004) and Ge(331)peaks for n-type are ×0.3 and ×0.38 of p-type, suggesting that then-type crystal quality is significantly better than p-type. The Ge(331) FWHM particularly points to a considerable reduction in stacking faults for n-type compared to p-type[2].These FWHM values compare well with the work by Ikeda *et al*[213], who achieved FWHM of 490 and 720 arcsec for Ge(004) peak at θ and 2$\theta$from a 390-nm-thick film.
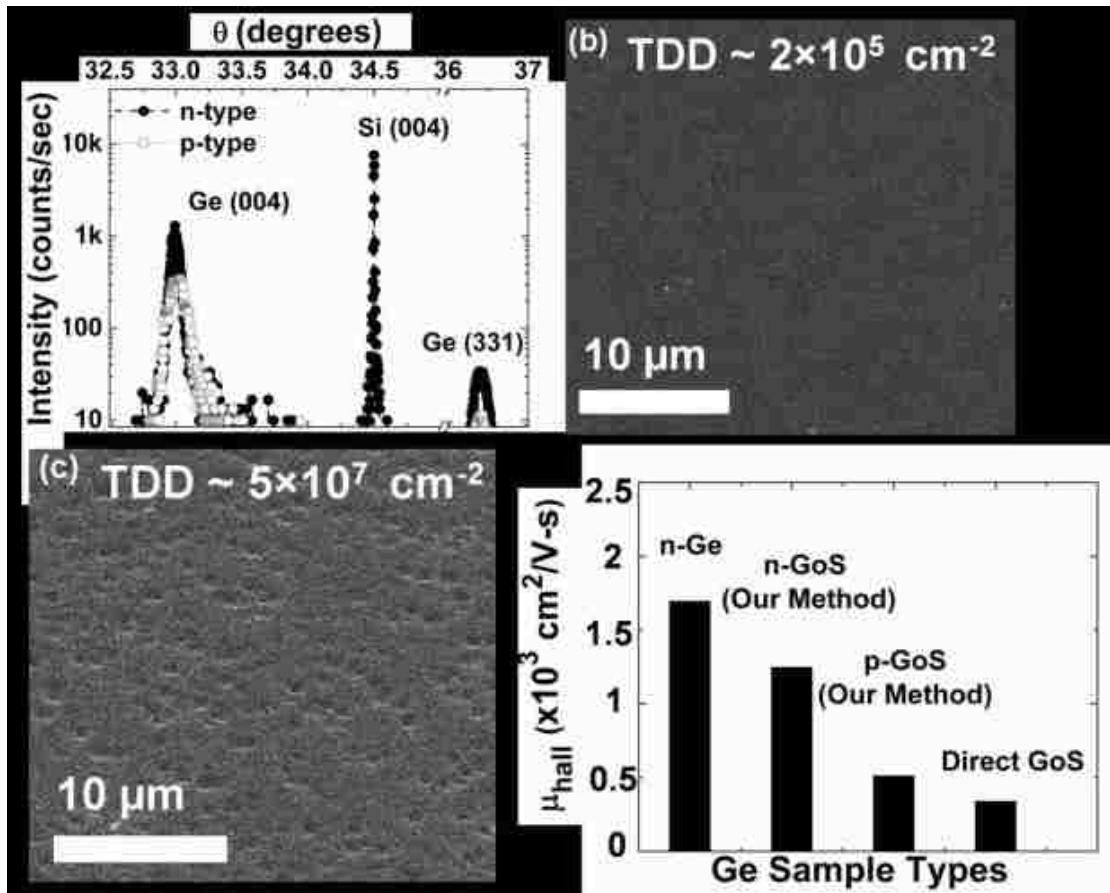
Figure 6.14:(a) XRD intensity of Ge(004), Si(004), and Ge(331) peaks. (b) SEM images of etch pits on n-type surface. (c) SEM images of etch pits on p-type surface. (d) Majority carrier mobility in Ge substrate and GoS substrates. n-Ge (100) wafer, purchased from MTI corporation, has a As doping level of 5×10^{16} cm^{-3}.

Figures 6.14(b)–(c) show SEM images of etch pits created on n- and p-type Ge surfaces over 25×25 μm^2 region. For a statistically reliable estimate on EPD, we sample 5 wafers of each dopant type and 4 different areas on each wafer. The EPD is $\sim 2 \times 10^5$ and $\sim 5 \times 10^7$ cm^{-2} for n- and p-type GoS. For the basis of comparison, when Ge is grown directly on Si without Ge-Si interfacial engineering, a typical EPD is on the order of 5×10^8 cm^{-2}. The EPD measurements quantitatively represent the threading dislocation density (TDD) in the Ge film. Consistent with XRD and EPD measurements, Figure 1(d)

shows the room-temperature (RT) Hall mobility (μ_{hall}) from n-type Ge wafer, n- and p-type GoS, and Ge grown directly on Si without Ge-Si interfacial engineering, all with the same background doping level of 5×10^{16} cm^{-3}: 1600, 1250, 550, and 250cm^2/V-s. The EPD and Hall measurements support that the dislocations originating from the Ge-Si interface strongly influence the mobility, which progressively decreases with increasing TDD.

6.9 Device Fabrication:

MOS capacitors are first fabricated on GoS and Ge substrates. After native oxide removal[214],we grow GeO$_2$ at 550 ºC for 15 min under 1 atm dry O$_2$ by rapid thermal oxidation. The next step is plasma-assisted thermal nitridation at 300 to 400 ºC for 10 min under 600 mTorr of NH$_3$with 150 W of RF power to convert GeO$_2$ to GeO$_x$N$_y$ (oxynitrides).Compared to N$_2$O or NO, the use of NH$_3$ leads to better N incorporation into the oxynitride film[214].HfO$_2$ is then deposited at RT by Hf e-beam evaporation in the presence of atomic O that promotes oxidation at low temperatures. A T-shaped 2.5-µm-long gate region is defined by lithography and deposition of 100-nm-thick Ti in a gate-first process flow. The backside contact is made with sputter-coated Al. After fabricating the Ti/HfO$_2$/GeO$_x$N$_y$/Ge gate stack, a forming gas (H$_2$/N$_2$ = 1:10) anneal is carried out at 370 ºC for 20 min. The source and drain regions are defined by lithography and heavy doping with B and P spin-on dopants (SODs) for p- and n-MOSFETs, avoiding ion implantation. The drive-in diffusion of P or B dopants follows two steps: furnace thermal annealing at 800 ºC for 30 min and rapid thermal annealing (RTA) at 850 ºC for 30 s. The residual SODs are then removed in a NH$_4$F solution, and

O_2 plasma is used to further clean the Ge surface. To ensure that heavy doping can be achieved by SODs, we have diffused B and P separately into n-type GoS

and measured the substrate resistivity. The same step is repeated for p-type GoS. Table 6-1 lists the dopant concentration estimated from sheet resistance. The counter-doping increases sheet resistance in both types of GoS substrates, indicating that the heavy dopant diffusion is achieved. Ohmic contacts are formed by depositing Ti on source and drain regions, using e-beam evaporation and RTA at 450 ºC for 30 s. The source–drain spacing is approximately 6.5 µm.

Table 6-1: Dopant concentration based on sheet resistance.

Dopant Type	GoS Type	Sheet Resistance ($\Omega/\square$)	Dopant Concentration (cm^{-3})
B	n-Ge	160	4×10^{18}
B	p-Ge	2	2.5×10^{19}
P	n-Ge	8	2×10^{19}
P	p-Ge	105	6×10^{18}

6.10   Results and Discussion:

Figure 6.15(a) shows a cross-sectional TEM image of the gate stack with 5-nm-thick HfO_2 and 8-nm-thick GeO_xN_y. The oxynitride is known to provide good surface passivation for Ge[214]. The TEM image shows that the GoS-GeO_xN_y interface is not sharply defined. We attribute this roughness to the ion bombardment that occurs in the RF plasma during the nitridation step. We expect that using down-stream

plasma would minimize the ion-induced roughening. While further optimization can be conducted, the primary goal of this study was to test our material quality by fabricating MOS structures on the GoS substrates.

To maximize the N content, we compare the intensities of N1s, O1s, and Ge3d X-ray photoelectron spectroscopy (XPS) peaks from samples nitridated at
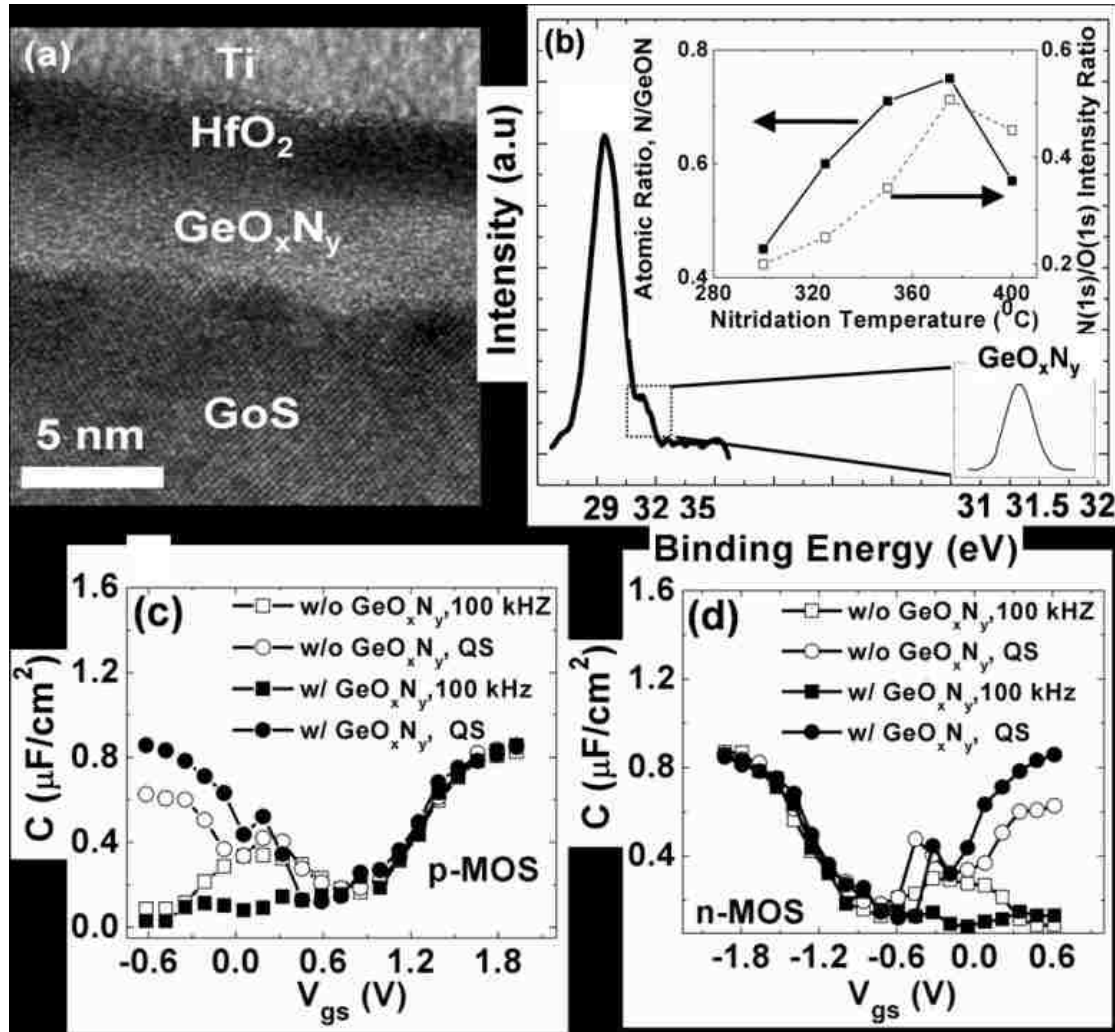
Figure 6.15 :(a) High-resolution, cross-sectional TEM image of Ti/5-nm HfO2/8-nm GeOxNy/GoS stack. (b) XPS Ge3d peak with a shoulder corresponding to the oxidation state of Ge in GeOxNy. (Inset) N/Ge and N/O ratios are used to compare the N content in the GeOxNy layer formed at different nitridation temperatures. (c) and (d) C-V characteristics of p- and n-MOS with and without GeOxNy.

different temperatures. Figure 6.15(b) shows the main Ge3d peak at 29.5 eV and a shoulder at 31.5 eV assigned to the oxidation state of Ge in GeO_xN_y. Using Gaussian deconvolution and appropriate sensitivity factors, the inset of Fig. 2(b) qualitatively shows atomic ratios of N/GeO_xN_y and N/O as a function of nitridation temperature. The maximum N incorporation is achieved at 375 °C at which we expect the best electrical performance[214]. To assess the effectiveness of oxynitride passivation, we compare the *C-V* characteristics of p- and n-MOS capacitors with and without GeO_xN_y. *C-V* measurements are performed at high-frequency (HF) at 100 kHz and under quasi-static (QS) condition. Without GeO_xN_y, Figs. 6.15(c) and (d) both show a noticeable peak at $V_{gs}\sim$ 0V.In comparison, the *C-V* characteristics of p- and n-MOS improve with GeO_xN_y, where Figs. 2(c) and (d) do not show peaks or an abrupt increase in the forward-bias capacitance. In both types, however, kinks appear near inversion during QS scans even after performing various thermal anneals on our MOS stacks, suggesting the presence of slow interface states[215].To complement the *C-V* measurements, we have measured the reverse leakage current density of p- and n-MOS with the GeO_xN_y layer: $\sim 1\times10^{-3}$ and $\sim 7\times10^{-3}$ A/cm^2.We attribute the higher leakage current in n-MOS to the larger TDD in p-type Ge.Based on HF and QS measurements, the interfacial trap density (D_{it}) is estimated from C_{QS} and C_{HF} by

$$D_{it}=\frac{C_{OX}}{q}\left\{\frac{\left(C_{QS}/C_{OX}\right)}{\left[1-\left(C_{QS}/C_{OX}\right)\right]}-\frac{\left(C_{HF}/C_{OX}\right)}{\left[1-\left(C_{HF}/C_{OX}\right)\right]}\right\},$$ where C_{OX} is the equivalent oxide capacitance/unit area, q is the unit charge, C_{HF} is the high-frequency capacitance/unit area, and C_{QS} is unidirectional quasi-static capacitance/unit area. C_{QS} is measured based on $C_{QS}=I/\left(\partial V/\partial t\right)$, where *I* is the measured current, and $\partial V/\partial t$ is the ramp rate of V_{gs} at 0.1 V/s. Based on the

C-V measurements, the minimum D_{it} for the MOS stack is 6×10^{12} and 2×10^{13} cm^{-2} eV^{-1} at RT for p- and n-MOS. We note that p-MOS fabricated on n-Ge has lower D_{it} than that of n-MOS fabricated on p-Ge. However, the TDD ratio between p- and n-GoS ($>10^2$) does not equate to the ratio between the D_{it} for the n- and p-MOS stacks (>3). This suggests that the interfacial roughening at GeO$_x$N$_y$-Ge interface, along with TDD, may contribute to D_{it}. While our previous work [212] shows that TDD influences the magnitude of D_{it}, the direct correlation between TDD and D_{it} cannot be made in this case because the impurity type is different for the two gate stacks.

6.11   Effective Mobility of MOSFETs

An important parameter for MOSFETs performance is threshold voltage (V_{th}). Typically a plot of linear drain current (I_{ds}) vs. gate voltage (V_{gs}) is used to calculate V_{th}. The measured V_{th} for p-MOSFETs on Ge, p- and n-MOSFETs on GoS are -0.25, -0.15, and 0.1V, respectively. Figure 6.16(a) shows I_{ds}-$V_{gs,}$ plotted in logarithmic scale. Based on the slope from I_{ds}-$V_{gs,}$, we can also calculate MOSFET subthreshold slope (SS),expressed by: $SS = \left(\dfrac{d(log_{10}I_{ds})}{d(V_{gs})} \right)^{-1}$ .In our I_{ds}-V_{gs} characteristics, the V_{gs} is scanned from -1.2 to 1.2V by 0.1 V steps, while V_{ds} is kept constant at -0.5 V for p-MOS and +0.5 V for n-MOS. For GoS substrates, the ON current (I_{ds}) in the linear regime shows a subthreshold swing (SS) of 100 and 200 mV/decade for p- and n-MOSFETs.

Complementing Hall measurements, Figure 6.16(b) shows the RT low-field, effective hole and electron mobilities ($\mu_{h,eff}$ and $\mu_{e,eff}$) extracted from *C-V* and I_{ds}-V_{gs} measurements, as a function of effective electric field E_{eff}. The effective mobility (μ_{eff}) can be obtained from $\mu_{eff} = \left(\dfrac{L}{W} \right) \left(\dfrac{I_{ds}(V_{gs})}{V_{ds}Q_{inv}(V_{gs})} \right)$ by measuring I_{ds} in the linear region,

where $Q_{inv}=C_{ox}(V_{gs}-V_{th})$. The low-field condition (0.05 MV/cm in our case) is satisfied in the regime where I_{ds} responds linearly to V_{ds} (-0.25 to 0 V). Figure 6.16(b) shows that the peak $\mu_{h,eff}$ is ~400 cm^2/V-s, whereas the peak $\mu_{e,eff}$ is ~950 cm^2/V-s. $\mu_{h,eff}$ and $\mu_{e,eff}$ show 82 and 30 % improvement over Si MOSFETs, and $\mu_{h,eff}$ shows enhancement by a factor of 2.67 and 1.61 over the mobilities in relaxed and strained Ge[216].
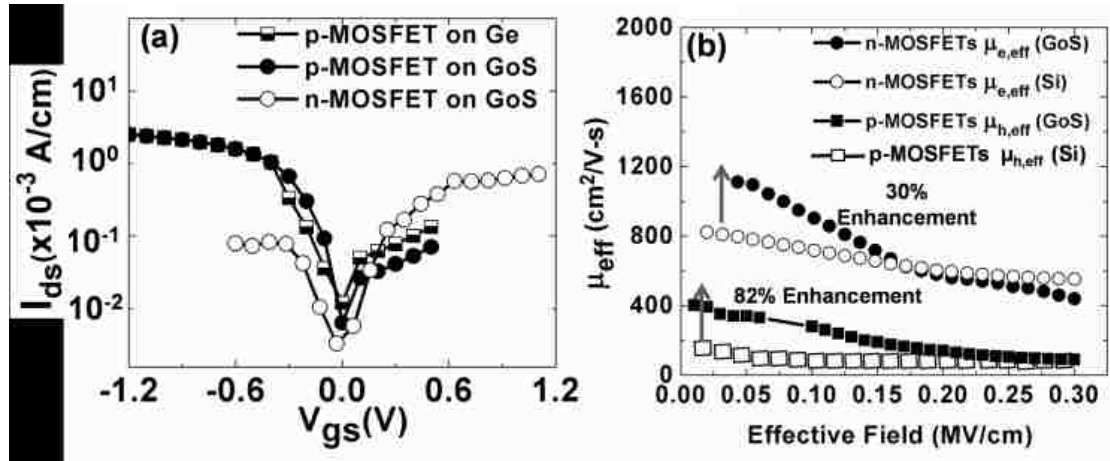
Figure 5.16: (a) Subthreshold slope of p-MOSFETs fabricated on n-Ge and n-GoS, and n-MOSFETS fabricated on p-GoS: 80, 100, and 200 mV/decade. (b) $\mu_{h,eff}$ and $\mu_{e,eff}$ for p- and n-MOSFETs as a function of electric field.

6.12   Conclusions

We have grown high-quality continuous Ge films on Si at the wafer scale. As a rigorous test of the Ge material quality, MOSFETs are fabricated and characterized on these GoS substrates, using Ti/HfO$_2$/GeO$_x$N$_y$/Ge gate stack. The low-field effective carrier mobility in p- and n-MOSFETs on GoS shows 82 and 30 % improvement over that of Si-channel-based MOSFETs and compares well with other MOSFETs fabricated on relaxed and strained Ge. We observe that the p-MOSFET performance is superior to that of n-MOSFETs, reflecting the low TDD in n-Ge than in p-Ge.

CHAPTER 7:

FUTURE DIRECTION: Creating a Responsive SiGe Substrate to Form 2D Array of Ge Quantum Dots Using Stress-induced Near-surface Compositional Redistribution

My research goal was two-fold, first, to establish materials engineering solutions to grow ultralow-dislocation-density epitaxial Ge on Si (GoS) at the wafer-scale and second to use the engineered substrates to fabricate working devices as a rigorous test of our scientific understanding. High-quality GoS substrates enable numerous applications, including high-mobility transistors, low-cost multijunction solar cells, and infrared photodetectors. However, the fundamental engineering challenge hindering broad commercial use of GoS substrates still remains to be lattice and thermal expansion coefficient mismatch. Over the past two decades, many engineering solutions have emerged to overcome this challenge, including graded buffer layer, cyclic thermal annealing, and aspect ratio trapping. In comparison, through my dissertation work, I have provided a path to reduce both dislocations and thermal stress in Ge at the wafer scale as a single continuous film by improving a molecular beam epitaxy (MBE) growth technique used in our laboratory. To test the quality of these films, I have fabricated and characterized both p- and n-channel MOSFETs for high-mobility transistor applications. Going beyond epitaxial engineering and device fabrication, I have also recently demonstrated a scalable path to create a 2D array of Ge quantum dots (QDs) on responsive SiGe substrates based on elastic mechanical deformation and subsequent SiGe compositional redistribution, coupled with MBE growth. In this chapter, I'll discuss

about the experimental approach that I have taken to demonstrate the feasibility of creating 2D array of Ge QDs on SiGe substrate.

7.1   Introduction:

Fabrication of long-range, periodic, self-assembled germanium (Ge) quantum dots (QDs) on Si or SiGe substrates have opened up an exciting opportunity in the field of nano-/micro-electronics, high-density patterned media for data storage, optoelectronics, and nanosensor arrays [217-219]. Due to the discrete nature of the confined states in QDs, the confinement of carriers is expected to improve multi-fold in QDs, result in a substantial increment in the luminescence efficiency [220,221]. Development of such uniform, periodic Ge QDs on Si or SiGe substrates would make it possible to combine the optical and electronic components on the same substrate using the existing Si CMOS technology. A variety of methods of fabricating of Ge QDs on Si substrates have been reported, such as [222], Ge dot registry with a trench pattern[223], pattern created by Ga ion implantation where Ga clusters acted as nucleation sites for Ge dot formation [224], and lithography/reactive ion etching-created pits lead to patterned Ge dots [225,226]. While these previous methods have attracted researchers due to their requirement of having limited substrate pre-processing, however, these approaches often fall short in fabricating device-quality ordering of Ge QDs where maintaining periodicity of QDs is the key.

7.2   Proposed Mechanism of Fabricating Long-Range, Periodic QDs of Ge

Herein, we propose a unique method of fabricating 2D array of QDs of Ge on a SiGe substrate. We use simulation to predict and experiment to demonstrate the compositional redistribution of Si and Ge in the near-surface region of

Si$_{0.8}$Ge$_{0.2}$ substrates by applying a spatially structured compressive stress to the substrate and thermally annealing the substrate under stress. The primary advantage of the proposed approach is that a single, reusable template is used to induce the compositional variation for multiple substrates. The compositional redistribution of Ge is predicted under purely elastic deformation, using a lattice kinetic Monte-Carlo simulation that accounts for the influence of composition, temperature, and stress on the diffusion kinetics of Ge in SiGe alloy. Atomistic stress field in a SiGe slab is computed using the Tersoff empirical potential and static relaxation. This compositional variation in turn can be used to selectively grow a 2D array of Ge quantum dots upon Ge exposure using molecular beam epitaxy (MBE). Figure 7.1 shows a schematic of the process flow for 2D array of Ge QDs formation. Figure 7.1 (a) shows a schematic of a 2D array of indentors and a bulk SiGe substrate before they are in contact with each other. Figure 7.1 (b) illustrates an assembly of the system including a mechaniucal press, a 2D array of indentors and a bulk SiGe substrate once they are in contact. The mechanical press exerts elastic compressive stress to near-surface of SiGe substrate through these indentors. Now this assembly is annealed at high temperature. Once the annealing step is performed, the system is subjected to cooling down. Figure 7.1 (c) shows that the 2D array of indentors are now withdrawn from the surface of SiGe substrate, leading to patterned residual tensile sress and Ge depletion in the near-surface of SiGe substrate. Finally, the stress-patterned surface of SiGe is subjected to Ge beam in a MBE chamber. Based on the stress magnitude and compositional variation that exist on the near-surface of SiGe substrate, a 2D array of QDs of Ge start to form on the SiGe substrate.
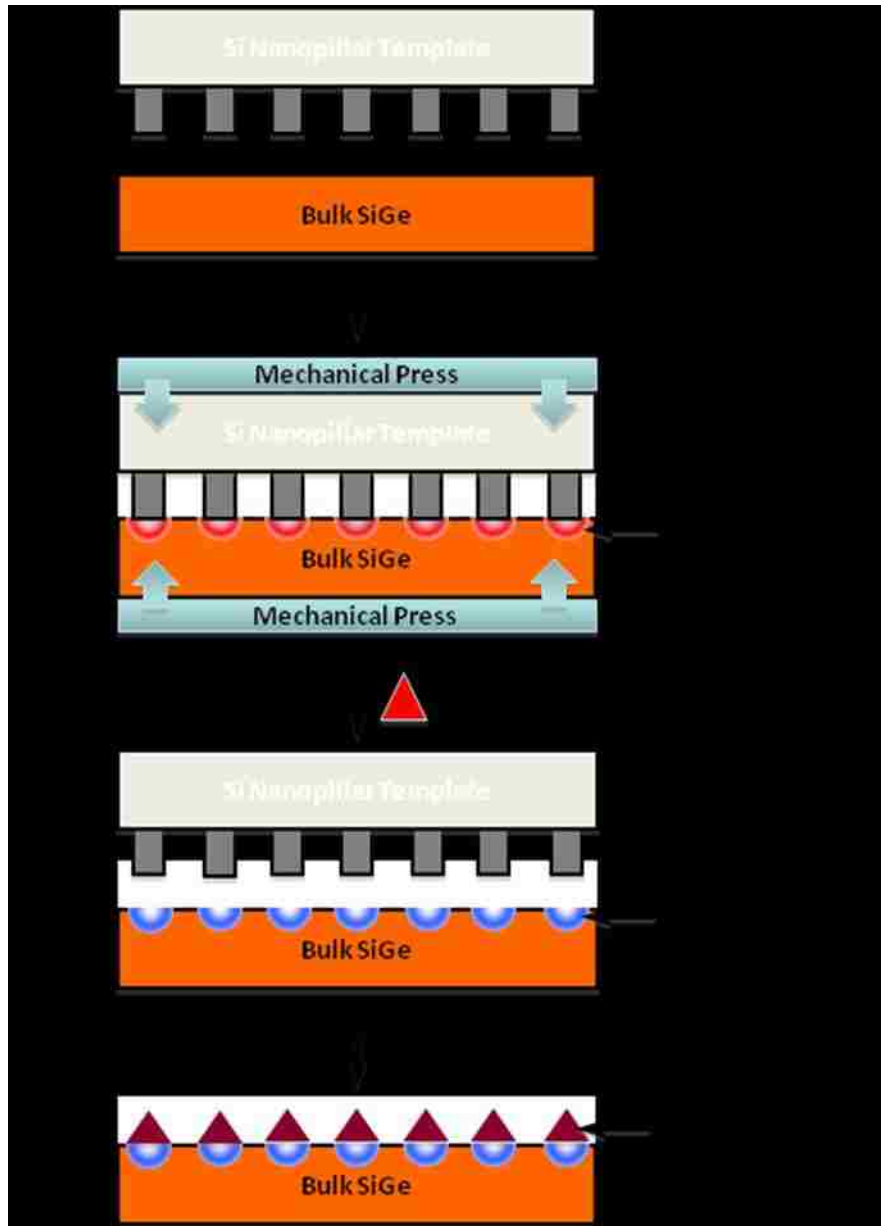
Figure 7.1:(a) A schematic of a 2D array of indentors and a bulk SiGe substrate before they are in contact with each other. (b) an assembly of the system including a mechaniucal press,a 2D array of indentors and a bulk SiGe substrate once they are in contact. The mechanical press exerts elastic compressive stress to near-surface of SiGe substrate through these indentors. (c) this system is now annealed at high temperature. Once the annealing is performed, the 2D array of indentors are withdrawn from the surface of SiGe substrate, leading to patterned residual tensile sress and Ge depletion in the near-surface of SiGe substrate. (d) once this stress-patterned is subjected to Ge beam in a MBE chamber, a 2D array of QDs of Ge start to form on the SiGe substrate.

To complement the computational prediction, the compressive stress is applied by pressing a 2D array of Si indenters against the $Si_{0.8}Ge_{0.2}$ substrate. Hertz contact model is used to calculate the compressive stress applied to the $Si_{0.8}Ge_{0.2}$ substrate under the Si nanopillars. We observe that the magnitude of compressive stress and annealing temperature determine the nature of deformation (elastic or plastic) in the $Si_{0.8}Ge_{0.2}$ substrate. Corresponding energy dispersive x-ray spectroscopy (EDS) shows that the compositional redistribution of Si and Ge in the near-surface region of $Si_{0.8}Ge_{0.2}$ substrates results from elastic deformation within a thermal annealing temperature range of 950 to 1000 °C and an applied stress range of 15 to 18 GPa. Based on nano-probe EDS, the elastically deformed compressed region shows near-complete Ge depletion and Si enrichment in atomic concentration. However, the temperature and stress exceeding the aforementioned ranges result in plastic deformation with no compositional variation. The plastic deformation depth is ~30 nm according to scanning transmission electron microscope images. We attribute the plastic deformation to (1) the localized pressure applied to the substrate under the contact area, (2) the near-surface substrate stiffness at substrate temperature, and (3) the tensile biaxial stress under the compressed region due to different thermal expansion rates of Si vs. $Si_{0.8}Ge_{0.2}$.

7.3   Experimental Details:

For the $Si_{1-x}Ge_x$ substrate, we have chosen x = 0.2 because to obtain maximum lateral variation in the surface strain that will enable us to induce maximum possible stresses during the stress transfer process without plastic relaxation via formation of misfit dislocations. The 2D array of Si indenters, dimension of 80 nm in diameter and 420 nm in pitch, are fabricated by interferometric lithography (IL) [227-231]

and conventional dry etching. The IL method allows fabricating a 2D array of sub-wavelength size features, using light interference at ultra-violet (UV) wavelengths range. The mechanical press comprises two Molybdenum (Mo) plates. These Mo plates are intentionally made recessed in order to hold the Si pillars and $Si_{0.8}Ge_{0.2}$ substrate. Tungsten coated stainless steel screws are used to hold and compress the Molybdenum plates together. We apply externally a precise amount of torque that is desired onto the screws. This will provide the pressure (or compressive stress) that is needed for creating periodic indentation onto the near-surface of the $Si_{0.8}Ge_{0.2}$ substrate. The p-type doped $Si_{0.8}Ge_{0.2}$ substrate is bought commercially. The doping type and doping density is verified though Hall measurement experiment. The x-ray diffraction (XRD) technique is used to qualitatively determine the full-width half-max (FWHM) of $Si_{0.8}Ge_{0.2}$ substrate. We use a Phillips MRD X-ray diffractometer equipped with Cu K_α line at 0.154 nm. We determine FWHM of 30 arcsec of (004) diffraction peak as an indicator of crystallinity of $Si_{0.8}Ge_{0.2}$ substrate.

This 2D array of Si indenters and $Si_{0.8}Ge_{0.2}$ substrate is compressively pressed together using the mechanical press, shown in Fig. 7.1(c). Once the mechanical press is properly assembled, we place this into a furnace at ambient temperature. Then, the furnace is elevated to high temperature (range from 900°C to 1000°C) to initiate thermal annealing process for three hours. Experiments are categorized into two broad sets: (1) in the first set of experiments, each sample subjects to different torque; however, the annealing temperature is kept constant for every samples. (2) in the second set of experiments, each sample subjects to different annealing temperature; however, the applied torque is kept constant for every samples. After three

hours of steady state thermal annealing, the furnace is brought to room temperature where the press is then pulled out and set to equilibrate with surrounding room temperature. Thereafter, the indented $Si_{0.8}Ge_{0.2}$ substrate surface is imaged by SEM performed on a FEI Quanta 3D operating at 15 keV for the electron beam energy. Finally, the indented substrate surface is characterized using cross-sectional and scanning transmission electron microscopy (XTEM and STEM) in conjunction with nano-probe EDS. We use EDS to quantitatively estimate the compositional redistributions of Si and Ge atoms at the near-surface of the $Si_{0.8}Ge_{0.2}$ substrate.

7.4   Analytical Contact Model:

In this paper, we restrict our attention to nano-indentation method using 2D array of Si indenters that imparts compressive stress onto $Si_{0.8}Ge_{0.2}$ substrate. And, our aim is to determine a quantitative relationship between imparted compressive stress under the indenters and external loading torque that is applied through the screws. Based on the magnitude of external torque, this yields deformation (elastic or plastic) in $Si_{0.8}Ge_{0.2}$ substrate. We assume that the volume of the contact nano-indenter remains constant during adhesion and associated deformation. When the compressive stress is applied on the $Si_{0.8}Ge_{0.2}$ substrate, the system is no longer remain a simple system rather become a strongly coupled system [232]. As a consequence of strong coupling, the complex model can no longer be described using a simple mass and spring model, instead of this strong coupling though the direct contact between Si nano-indenter and $Si_{0.8}Ge_{0.2}$ substrate is modeled using the Hertz contact model [233,234]. Considering a nano-indenter radius (R) ~ 80 nm, which is larger compared with the indentation depth that occurs on $Si_{0.8}Ge_{0.2}$ substrate, we can treat the $Si_{0.8}Ge_{0.2}$ substrate that is under indentation is

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experiencing simple compression, neglecting the lateral deflection. The pressure p, which is applied on the $Si_{0.8}Ge_{0.2}$ substrate, is written as,

$$p = \frac{1}{3\pi} \cdot \left(\frac{f^2}{f_0^2} - 1 \right) \cdot \frac{K_N}{R} \tag{7-1}$$

and,

$$\frac{f^2}{f_0^2} = \frac{2E_r}{K_N} \sqrt{\frac{A}{\pi}} + 1 \tag{7-2}$$

Where f = resonance frequency of the coupled system where a nano-indenter is in contact with $Si_{0.8}Ge_{0.2}$ substrate, f_0 = resonance frequency of the free standing nano-indenter, E_r = reduced elastic modulus of the contact, K_N = Si indenter stiffness, A = contact area. These values of f and f_0 are not obtained easily through our experiments, however, the ratio can be determined easily using other parameters those are available, and shown in Eq. (2). The reduced elastic modulus of the contact, E_r, can be calculated, taking into account the Young modulus and the Poisson ratio of the pillar (E and v for the Si pillar) and the $Si_{0.8}Ge_{0.2}$ substrate (E_i and v_i for the $Si_{0.8}Ge_{0.2}$ substrate), $\frac{1}{E_r} = \frac{1-v^2}{E} + \frac{1-v_i^2}{E_i}$.

Considering E = 162 GPa for the Si pillar and E_i = 126 GPa for the $Si_{0.8}Ge_{0.2}$ substrate for computations, a reduced elastic modulus of E_r = 75.54 GPa is obtained. In order to estimate A, we assume both a circular contact area with radius r and a deformation depth h, which is much smaller than the radius of curvature R of an individual Si pillar (see Fig. 7.3(a)). Thus is good approximation, h is described by $h \cong r^2/2R$. The elastic deformation depth as well as contact area will be shown in detail while we analyze the cross-sectional TEM image of corresponding indentation zone.

7.5   Applied Compressive Stress vs. External Torque

Figure 7.2 (a) shows a 2D view of a Si indentor pressing against the surface eof $Si_{0.8}Ge_{0.2}$ substrate. Figure 7.2 (b) shows a graphical representation of calculated elastic compressive stress in units of GPa (shown in left-vertical axis) on near-surface of $Si_{0.8}Ge_{0.2}$ substrate as a function of external torque (N-m) and corresponding deformation depth in units of nm (shown in right-vertical axis) as a function of external torque. The analytically obtained compressive stress can be approximated using the following equation, $T=(C.D.P.A)/(\# \ of \ screws)$, where T= externally applied torque (N-m), C = torque coefficient (0.36 in our case), D = nominal screw diameter (0.00635 m), P = compressive pressure (GPa), and A = contact area (m^2), respectively. However, the deformation depth is a non-linear function of externally applied torque. The applied torque as a function of deformation depth can be approximated using the relationship $T\infty$ $h^{1.5}$, assuming that the deformation-torque curve follows the Hertz contact model. To demonstrate the efficacy of stress transfer onto the $Si_{0.8}Ge_{0.2}$ substrate though 2D array of Si indenters, we conduct two different set of experiments: 1) where we vary compressive stress from 8 to 20 GPa, and 2) where we vary annealing temperature from 900˚C to 1000 ˚C. Each experiment has run for 3 hours. The goal for performing this broad set of experiments to estimate a range of compressive stress and annealing temperature that is required for obtaining elastic compression which is imparted by the 2D array of Si indenters at the near-surface of $Si_{0.8}Ge_{0.2}$ substrate.
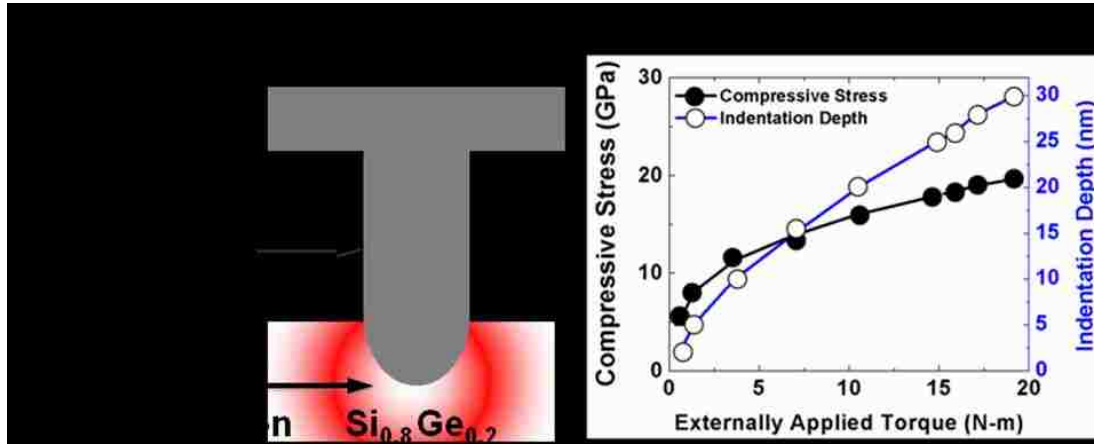
Figure 7.2:(a) A 2D view of the assembly consisting of a single indentor and a bulk SiGe substrate. The mechanical press exerts elastic compressive stress to the surface of SiGe substrate through indentors. (b) a plot of elastic compressive stress under each indentor as a function of torque being applied to each screw of mechanical press.

7.6   Effect of Compressive Stress and Temperatures in Indentation:

Figure 7.3 shows set of scanning electron microscopy (SEM) images of the surfaces of the $Si_{0.8}Ge_{0.2}$ substrates as a function of externally torque and annealing temperature. The torque and temperature are shown in horizontal and vertical axis, respectively. We observe that SEM images start to reveal visible indentation spots on $Si_{0.8}Ge_{0.2}$ substrates with increasing compressive stress from 8 to 20 GPa, and increasing annealing temperature from 900 to 1000 ˚C. For instance, we observe two different features in Fig. 7.3, and they are outlined by black dotted and solid circles. We speculate that the dotted circle represents a Si leftover, which is a residue from the 2D array of Si indenters that has made contact with the substrate during compression. We speculate that, either elastically or plastically deformed region exists underneath each Si leftover, outlined by the dotted circle. In contrast, the solid circle shows a plastically deformed region.
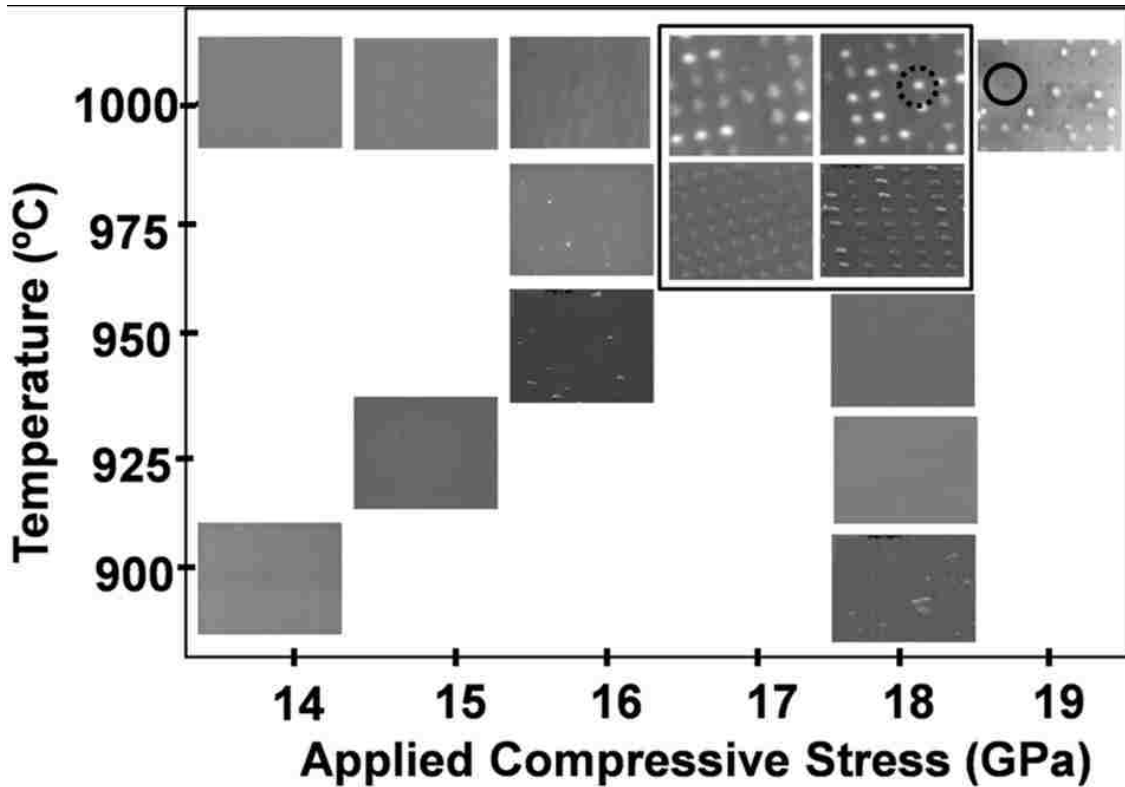
Figure 7.3: set of scanning electron microscopy (SEM) images of the surfaces of the $Si_{0.8}Ge_{0.2}$ substrates as a function of externally torque and annealing temperature.

The top image of Fig. 7.4 (L) shows a SEM image of a 2D array of Si indentors that are being withdrawn from the SiGe surface after the thermal annealing is completed. The top image of Fig. 7.4 (R) is a 3D rendition of a 2D array of Si indentors. The bottom image of Fig. 7.4 (L) shows a SEM image of the surface of $Si_{0.8}Ge_{0.2}$ substrate fter completion of thermal annealing step. The bottom image of Fig. 7.4 (R) is a 3D rendition of a 2D array of Si leftovers on SiGe surface. We observe that an array of Si leftovers present on the surface of $Si_{0.8}Ge_{0.2}$ substrate. We note that a compressive stress of 17 GPa and an annealing temperature of 1000 °C is used for this experiment. We choose this particular case because the substrate surface comprises of Si leftovers. Due to adhesion between Si indenters and corresponding

substrate during thermal annealing, that result in forming leftover of Si onto the $Si_{0.8}Ge_{0.2}$ substrate. Further EDS compositional details on Si leftovers, and compressive regions underneath leftovers through in-depth XTEM characterization are given in next few paragraphs.
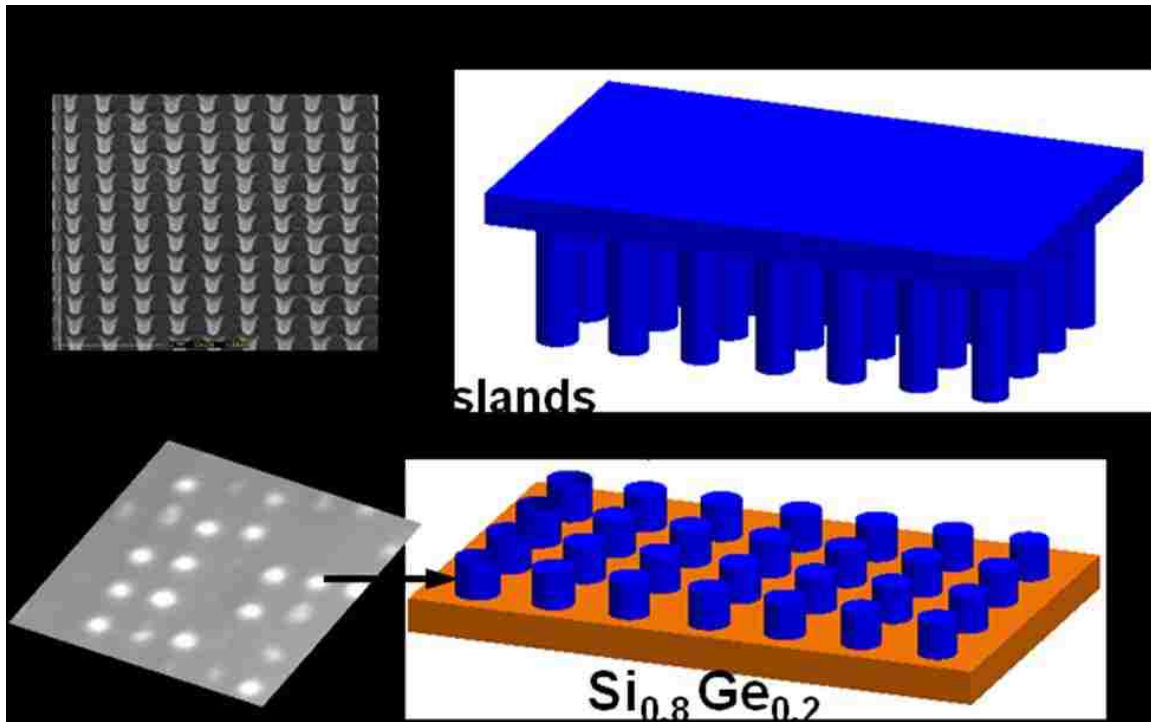
Figure 7.4: (L) SEM images of a 2D array of Si indentors and a 2D array of Si leftovers on the surface of SiGe substrate. (b) 3D rendition of a 2D array of Si indentors, and Si leftovers on SiGe surface.

7.7   EDX Calibration for Quantitative Compositional Analysis:

Before we proceed into characterizing the compositional variation on $Si_{0.8}Ge_{0.2}$ substrate as a function of applied compressive stress, it's necessary to characterize Si indenters, and unmodified, $Si_{0.8}Ge_{0.2}$ substrate through EDS. The parameters that will be used to characterize both of these samples will be set-up as calibration parameters and will be used later while characterizing the stress-

patterned $Si_{0.8}Ge_{0.2}$ substrate. Figure 7.5 shows the calibration parameters where atomic percentages of Si and Ge (in vertical axis) are plotted as a function of incident electron beam energy. We notice that, the atomic percentage of Si and Ge compositions in $Si_{0.8}Ge_{0.2}$ substrate is a strong function of incident electron beam energy. The atomic percentage ratio of 0.8:0.2 between Si and Ge is obtained with 6 KeV. Henceforth, to characterize, we use 6 KeV while performing EDS through XTEM. In $Si_{0.8}Ge_{0.2}$ substrate, the EDS spectra has two peaks: GeL (1.1 KeV) and SiK (1.7 KeV). The compositional percentages of GeL and SiK are approximately 19.92% and 80.08%, respectively.
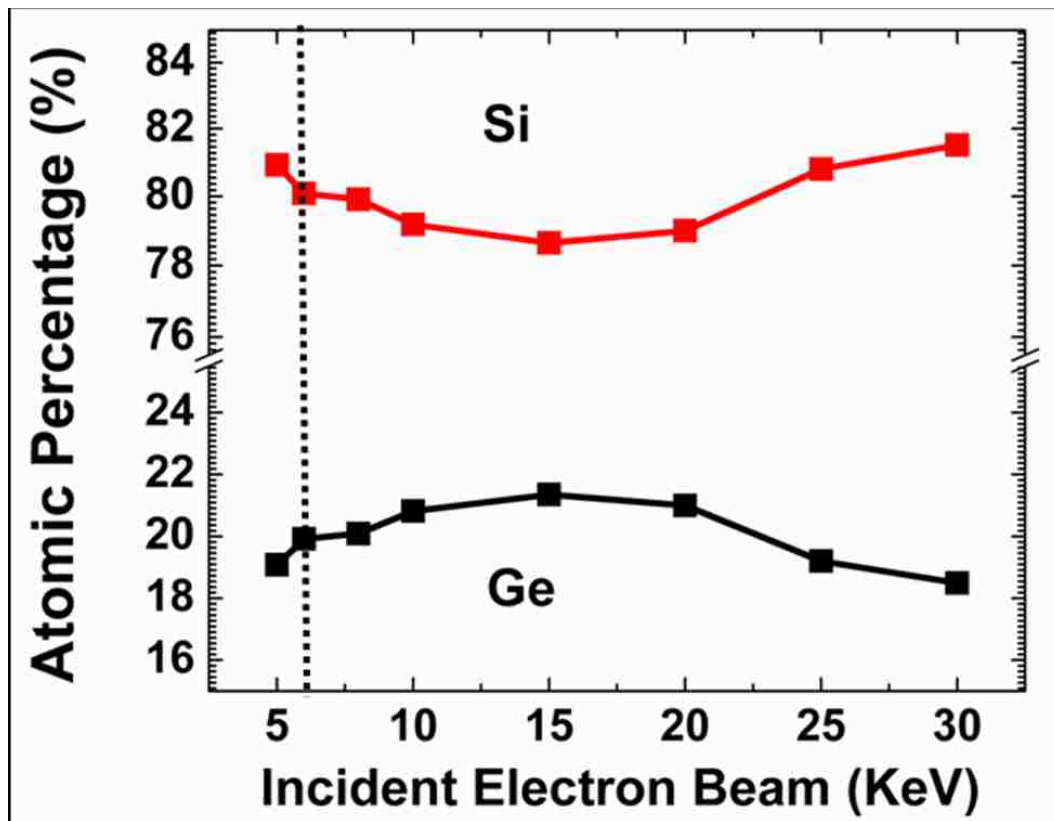
Figure 7.5: the calibration parameters where atomic percentages of Si and Ge (in vertical axis) are plotted as a function of incident electron beam energy. The optimum atomic percentage ratio of 0.8:0.2 between Si and Ge is obtained with 6 KeV.

7.8   Deformation and Characterizations:

Previously we have mentioned that imparted elastic compressive stress onto $Si_{0.8}Ge_{0.2}$ substrate in turn creates compositional variation. Herein we turn our focus on XTEM investigation of elastically deformed region in $Si_{0.8}Ge_{0.2}$ substrate and corresponding atomic compositional variation in the substrate through EDS. Figure 7.6 (a) shows a stack of Si leftover and $Si_{0.8}Ge_{0.2}$ substrate. The substrate is compressively stressed, and elastically deformed. The irregular shaped Si leftover is a part from Si indenter that is used for applying elastic compressive stress onto $Si_{0.8}Ge_{0.2}$ substrate. We note that, the elastically deformed region in the corresponding substrate shows no dislocation or fault lines. According to our hypothesis, we should observe compositional variation in this elastically deformed region of the substrate. Figure 7.6 (b) shows atomic percentage of Si and Ge atoms at the near-surface of $Si_{0.8}Ge_{0.2}$ substrate as a function of positions (P1 to P45) on the corresponding substrate. The inset of Fig. 4 (b) shows a XTEM image of $Si_{0.8}Ge_{0.2}$ substrate that comprises two such elastically compressed regions, and marked EDS positions starting from P1 to P45 on the corresponding substrate. Figure 7.6 (b) shows two, near-complete depletion regions of Ge atoms, marked by positions 12-14, and 32-34, respectively. In contrast, this corresponding regions show near-complete enrichment of Si atoms. This is expected based on our theoretical prediction. We note that, Ge atom is larger in size than Si atom, and they are randomly distributed in the $Si_{0.8}Ge_{0.2}$ substrate initially. Once the elastic compressive stress is imparted onto the near-surface of the substrate, the Ge atoms tend to move out from the compressed region, results in near-complete depletion of Ge atoms in those regions. The elastic

compressive stress that is acted onto the substrate employs an elastic deformation, also results to near-complete enrichment of Si atoms underneath the indented region. Therefore, with suitable amount of compressive stress, and correct annealing temperature, we experimentally demonstrate a near surface compositional variation in the $Si_{0.8}Ge_{0.2}$ substrate that in turn can be used to fabricate 2D array of Ge QDs. We expect to obtain an increasing atomic percentage of Ge at the near-surface of the substrate away from the compressed region. According to our EDS investigation, however, we don't observe such variation in atomic percentage of Ge. We attribute this to the large inter-distance between two elastically compressed regions, in other words, to the inter-distance between two Si indenters.

In contrast to elastic deformation that results in compositional variation, Fig. 7.6 (c) shows a XTEM image of $Si_{0.8}Ge_{0.2}$ substrate which is plastically deformed. Figure 7.6 (c) also shows a magnified view of a plastically deformed region which is outlined by white-dotted box. The stack consists of a Si leftover and $Si_{0.8}Ge_{0.2}$ substrate is shown here. Like before, the irregular shaped feature is Si leftover, however, in this particular case presents plastic deformation. The XTEM image shows that few dislocation lines and stacking faults exist at the near-surface of the substrate. The plastic deformation depth is approximately 30 nm. According to our hypothesis, we should not observe compositional variation in this plastically deformed region of the substrate. Figure 7.6 (d) shows atomic percentage of Si and Ge atoms at the near-surface of $Si_{0.8}Ge_{0.2}$ substrate as a function of positions (P1 to P20) on the corresponding substrate. The inset of Fig. 7.6 (d) shows a XTEM image

of $Si_{0.8}Ge_{0.2}$ substrate that comprises one such plastically compressed region, and marked EDS positions starting from P1 to P20 on the corresponding substrate. Figure
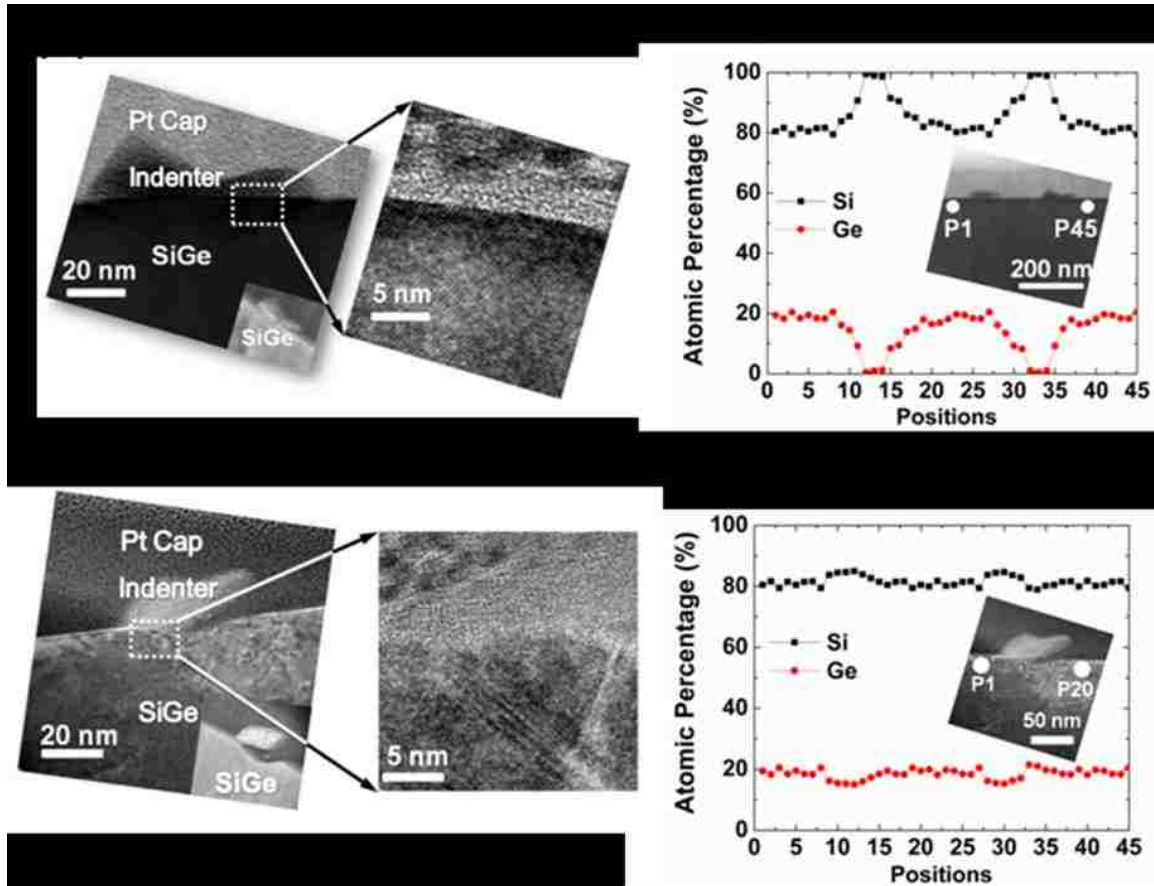
Figure 7.6 (a) cross-sectionaal transmission electron microscope image of stack including a Si leftover and SiGe substrate. This case corresponds to elastic deformation where no physical deformation happens on the SiGe surface after indentation. A magnified view of the TEM image of the interface between indentor and SiGe surface is also being shown here. (b) atomic percentage of Si and Ge atoms at the near-surface of $Si_{0.8}Ge_{0.2}$ substrate as a function of positions (P1 to P45) on the corresponding substrate. This plot represents that a compositional variation has occurred due to elastic compressive stress. (c) cross-sectionaal transmission electron microscope image of stack including a Si leftover and SiGe substrate. This case corresponds to plastic deformation where physical deformation happens on the SiGe surface after indentation. A magnified view of the TEM image of the interface between indentor and SiGe surface is also being shown here. A fault line can be seen from the magnified TEM image. (b) atomic percentage of Si and Ge atoms at the near-surface of $Si_{0.8}Ge_{0.2}$ substrate as a function of positions (P1 to P45) on the corresponding substrate. This plot represents that no compositional variation has resulted due to plastic compressive stress.

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7.6 (d) shows none of such near-complete depletion or near-complete enrichment regions of Ge or Si atoms. This is also in agreement with our hypothesis. The compressive stress that is acted onto the corresponding substrate exceeds the elastic compression limit, and the elastic strain energy is ultimately released via forming dislocations or stacking faults. Since the substrate is no longer experiencing elastic compressive stress, segregation of Ge and Si atoms does not occur at the near-surface of corresponding substrate. Therefore, we observe that the compositional variation is completely obscured under plastic deformation.

7.9 Conclusions:

Applying a spatially structured compressive stress to $Si_{0.8}Ge_{0.2}$ substrate and thermally annealing the substrate under elastic deformation cause compositional redistribution. The compressed regions show either elastic or plastic deformations. The elastically deformed regions show near-complete Ge depletion and Si enrichment. The plastically deformed regions do not show compositional redistribution. Atomistic simulations corroborate experimental results and provide a means to optimize the stress, temperature, and press geometry to achieve compositional redistribution. This compositional variation in turn can be used to selectively grow a 2D array of Ge quantum dots upon Ge exposure using molecular beam epitaxy (MBE).

Conclusions:

8.1   Summary of My Research and Future Work:

My research goal was two-fold, first, to establish materials engineering solutions to grow ultralow-dislocation-density epitaxial Ge on Si (GoS) at the wafer-scale and second to use the engineered substrates to fabricate working devices as a rigorous test of our scientific understanding. High-quality GoS substrates enable numerous applications, including high-mobility transistors, low-cost multijunction solar cells, and infrared photodetectors. However, the fundamental engineering challenge hindering broad commercial use of GoS substrates still remains to be lattice and thermal expansion coefficient mismatch. Over the past two decades, many engineering solutions have emerged to overcome this challenge, including graded buffer layer, cyclic thermal annealing, and aspect ratio trapping. In comparison, through my dissertation work, I have provided a path to reduce both dislocations and thermal stress in Ge at the wafer scale as a single continuous film by improving a molecular beam epitaxy (MBE) growth technique used in our laboratory. To test the quality of these films, I have fabricated and characterized both p- and n-channel MOSFETs for high-mobility transistor applications. Going beyond epitaxial engineering and device fabrication, I have also recently demonstrated a scalable path to create a 2D array of Ge quantum dots (QDs) on responsive SiGe substrates based on elastic mechanical deformation and subsequent SiGe compositional redistribution, coupled with MBE growth.

Herein I provide the approach that I have taken throughout my dissertation work. To improve our MBE growth technique, I made use of dislocation removal from partially coalesced Ge islands[1-3] and dislocation locking by oxygen

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precipitates. These two methods rely on the ease of dislocation glide during the initial stage of Ge island coalescence and the use of chemical SiO_2 to facilitate oxygen precipitate formation in the Ge epilayer, respectively. To rigorously test the Ge material quality, I took an approach of fabricating devices of technical relevance today. In particular, I first chose to fabricate high-mobility, Schottky-barrier-controlled p-MESFETs, whose performance is much more sensitive to the defect level in the entire Ge film and the Ge-Si interface, compared to MOSFETs. However, I also fabricated high-mobility p- and n-MOSFETs with competitive performance that would have a more immediate technical impact. Following materials engineering and device fabrication, I proceeded to pursue the next-generation device architectures, such as single-electron transistors based on Ge quantum dots, which can exploit my scientific understanding. In the case of Ge quantum dots, precisely positioning Ge quantum dots over a large wafer-scale area is one of the significant engineering challenges. As a part solution to this engineering challenge, I took an approach of using a mechanical imprint that consists of a 2D array of nanoscale Si pillars that press against the SiGe substrate. Upon elastic compression and thermal annealing, Ge preferentially migrates out of the compressed region, and subsequent Ge beam exposure with annealing is expected to form a 2D array of quantum dots on Ge-depleted regions. To complement my experimental work, I have also employed a finite element method to analyze GoS architecture, film stress, and dislocation reduction. These approaches illustrate that I have performed an entire spectrum of materials research, starting from epitaxial growth and characterization, to device fabrication and characterization, to modeling and analysis.

Herein I provide my scientific progress that I have made through my dissertation work. By increasing our understanding of dislocation glide during island coalescence and revealing impurity-dependent, dislocation locking mechanism by oxygen precipitates, I was able to achieve an ultra-low dislocation density of $\sim 10^5$ cm^{-2} in wafer-scale Ge epilayer. Furthermore, I have demonstrated competitive device performance from high-carrier-mobility transistors (MESFETs and MOSFETs) fabricated on GoS substrates. The key results include the effective mobility (μ_{eff}) from p- and n-MOSFETs with an exceptional 82 and 30% improvement over that of conventional Si channels. For large-scale manufacturing of single-electron transistors, I have also demonstrated that a spatially structured elastic compressive stress to the SiGe substrate with thermally annealing leads to a compositional redistribution of Si and Ge in the near-surface region of SiGe substrates, forming a 2D array of Ge-depleted nanoscale regions. Based on these latest findings, I have also begun to chart a future direction for my research group, where one can explore new advanced device architectures, such as Si-compatible, optically actuated, Ge-quantum dot-based field effect transistors.

Herein I provide few siginificant research results of my PhD work, and their broader scientific impact. I summarize my research by four main milestones: (1) sub-10^5 cm^{-2} dislocation density in Ge epilayer, providing a basis for Si-compatible, Ge-based photonic devices; (2) μ_{eff} and cut-off frequency in p-MESFETs exceeding 300 cm^2/V-s and 9 GHz , which would enable fast switches as well as low-power, read-only memory devices; (3) p- and n-MOSFETs with μ_{eff} of 401 and 940 cm^2/V-s and a subthreshold slope of 100 and 200 mV/decade, respectively, further supporting the material quality of GoS substrates and their potential use in high-carrier-mobility CMOS

devices; and (4) nanoscale 2D array of Ge depletion in SiGe substrates, providing a platform to create a 2D array of Ge quantum dots for the next-generation quantum computing research.

I believe there are three main directions in which my future research can go. Firstly, this research will address the feasibility of fabricating MOSFETs on wafer-scale germanium on silicon virtual substrate, and the outcome of this research will open up possibility of using this virtual substrate for next generation CMOS technology. Secondarily, sub-10^5 cm^{-2} dislocation density in Ge epilayer can open up possibility of uaing Ge-on-Si for next generation Si-compatible, Ge-based photonic devices. Third, a scalable path to create a 2D array of Ge quantum dots (QDs) on responsive SiGe substrates will enable us to build devices in nanoscales, such as single electron transistors, high-sensitive QD-based photodetectors. Moreover this will build a platform that can be useful to build devices for next-generation high-performance computing.

APPENDICES

APPENDIX A MBE Calculated and Measured Deposition Rates
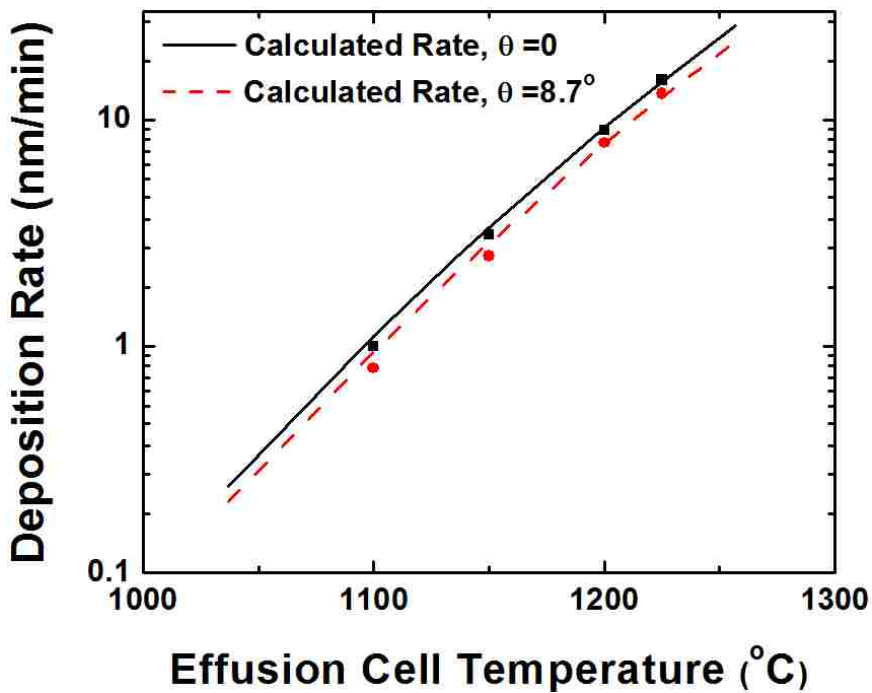
APPENDIX B MBE Substrate Heater Calibration
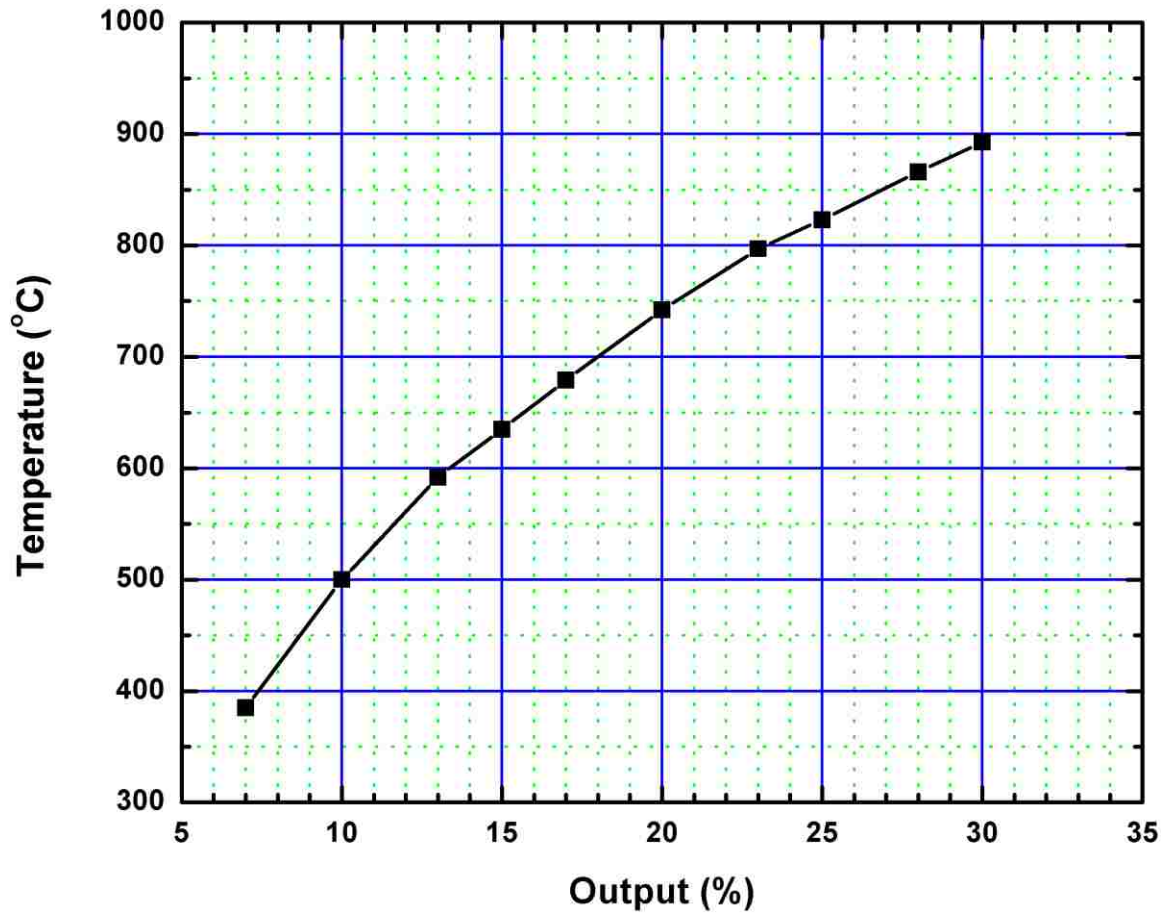
APPENDIX C Finite Element Modelling Using COMSOL Multiphysics

Finite element modeling based on a commercial software package COMSOL is used to calculate the thermal stress occurring in the epitaxial Ge due to differences in thermal expansion coefficients among Ge, Si, and SiO_2. The COMSOL tool performs continuum stress simulation using finite element methods. The simulation results, comparing Ge grown on Si with and without SiO_2 templates, show that the nanoscale templates can effectively reduce the thermal stress. The resulting stress results obtained using the simulation model corroborate the experimental observations. The simulation results suggest that the SiO_2 nanotemplates can reduce the stress caused by the thermal expansion coefficient mismatch, while simultaneously reducing the lattice-mismatch-induced dislocations in Ge grown on Si.
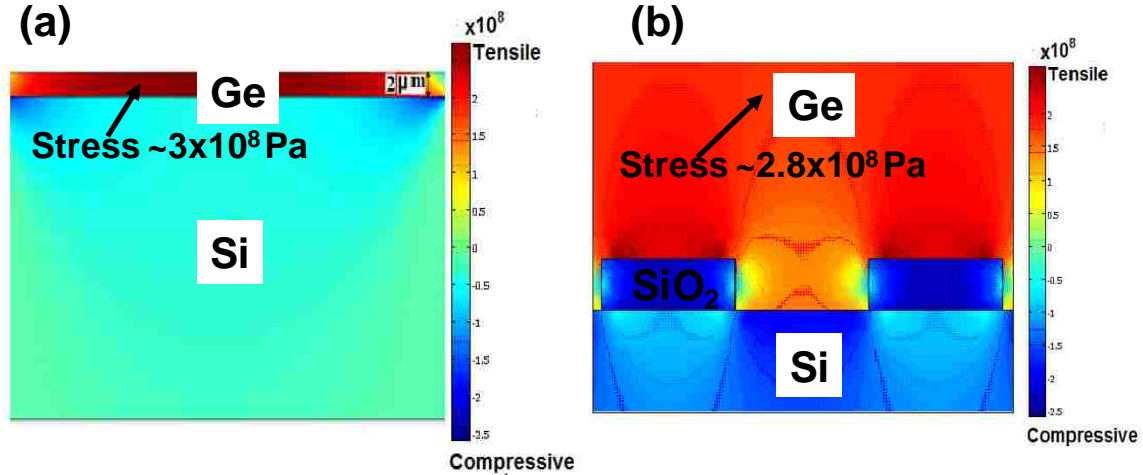
AppxC 1:(a) Simulated in-plane stress in directly grown epi-Ge on Si. In-plane biaxial tensile stress ~$3x10^8$ Pa. Ge is tensilystressed due to thermal expansion coefficient mismatch. (b) Simulated in-plane stress of epi-Ge grown within 200 nm by 200 nm SiO_2 trenches on Si. In-plane biaxial tensile stress ~$2.8x10^8$ Pa
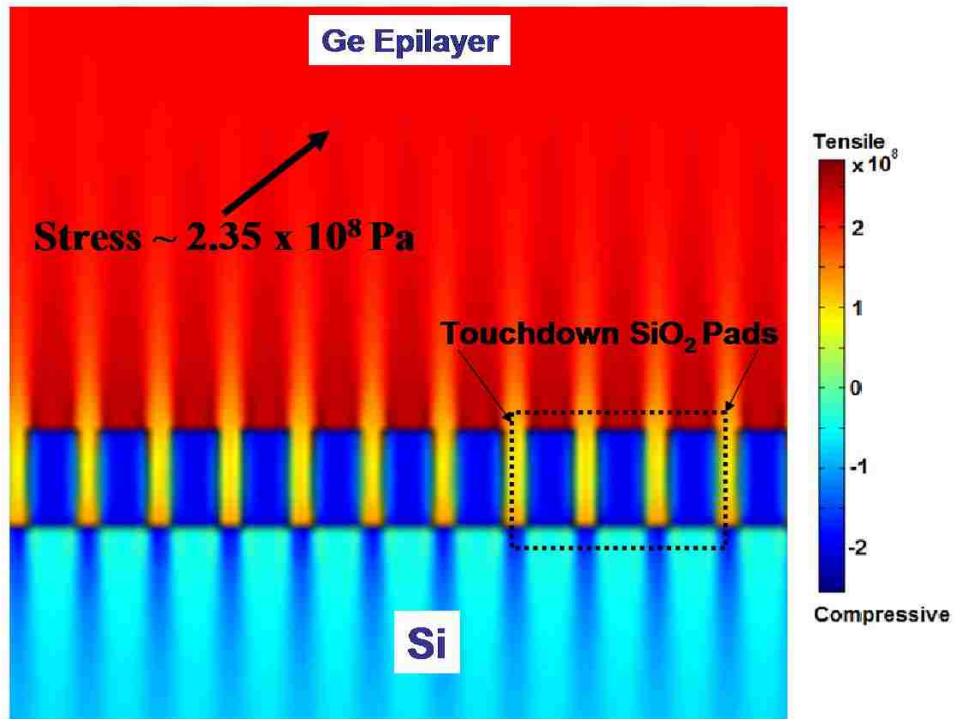
AppxC2: Finite Element Simulation of Epitaxial Ge grown on Si using Touchdown method
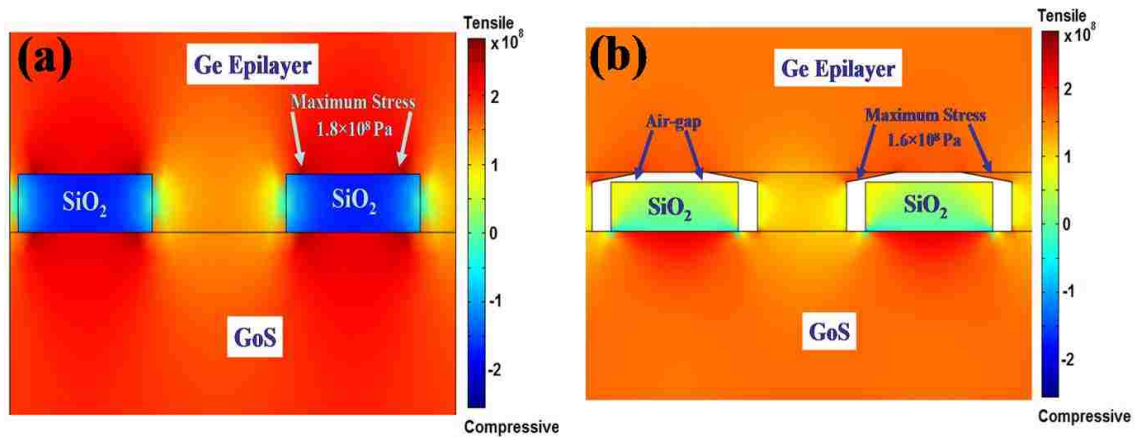
AppxC3: (a) Simulated stress in epi-Ge grown via SiO_2 nanotemplates fabricated on Ge-on-Si. Corner-induced-stress is observed above the nanotemplates. (b) Resulting stress of epi-Ge grown via SiO_2 nanotemplates fabricated on Ge-on-Si. Void/air-gap forms while merging. Corner stress is not observed. Twins form due to coalescence

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APPENDIX D Photoluminescnce Characterization of Ge-on-Si Films

We also investigate the optical quality of ultra-low dislocation density Ge-on-Si film by measuring room-temperature photoluminescence (PL). The n-type Ge PL main peak shows pronounced tensile-strain ($\times 0.8\%$) than that of p-type, which is an indicator of direct bandgapshrinkingat the Γ band-edge.

AppxD1: Room-temprature photoluminescence of n-GoS shows pronounced direct band-to-band transition at 1850 nm (0.67 eV). The n-GoS has ultra-low dislocation density, approximately in the range of 1×10^5 cm^{-2}. In contrast, the p-GoS shows less photoluminescence intensity, because p-GoS consists of large dislocation desnity, approximately in the range of 5×10^7 cm^{-2}.

We also investigate the optical quality of ultra-low dislocation density n-GoS film by measuring temperature dependent photoluminescence (PL) spectras. The intensity of PL at 1850 nm from n-GoS increases with decrasing operating temperature, indicating an outstanding optical quality of Ge film.
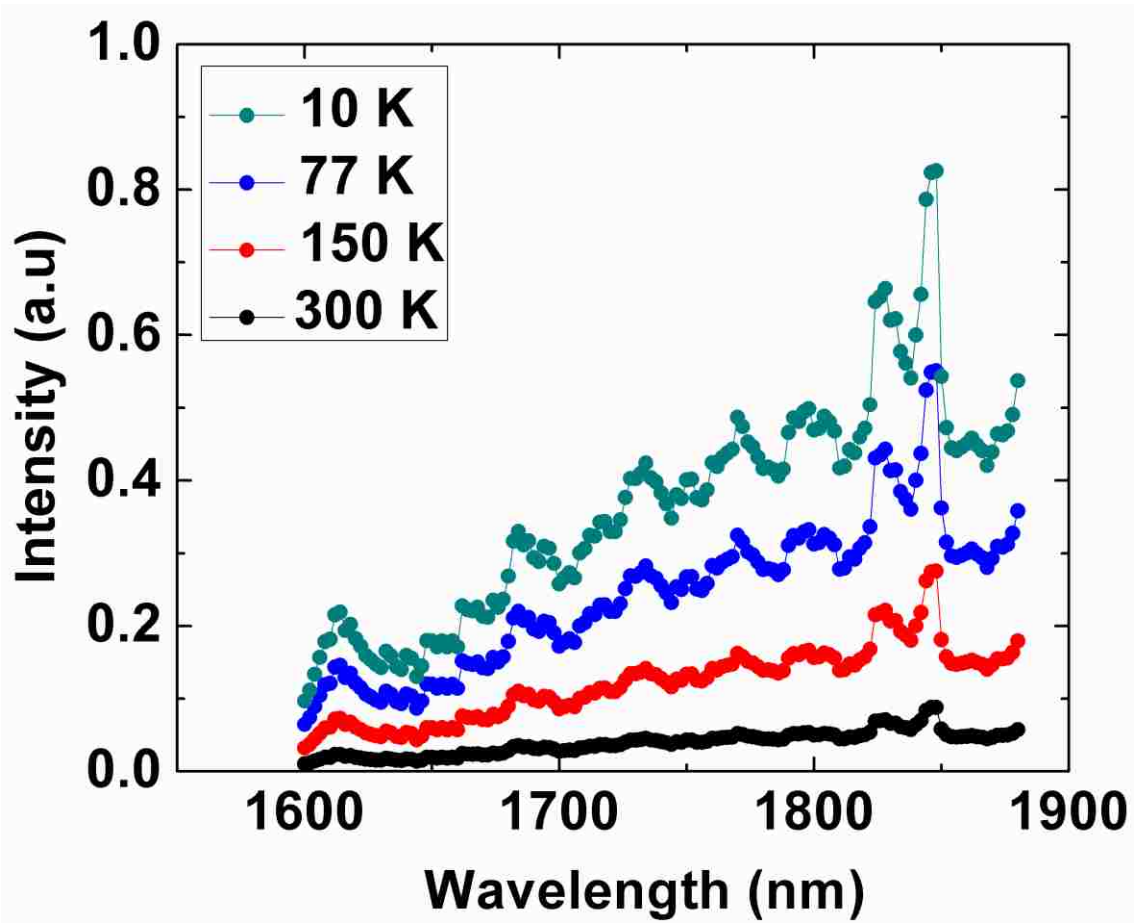
AppxD2: Temperature dependent photoluminescence spectrum of n-GoS.

APPENDIX D Symmetry-Breaking Nanostructures on Crystalline Silicon for Enhanced Light-Trapping in Thin Film Solar Cells

Crystalline silicon (c-Si) solar cells are expected to continue their large market share in the photovoltaics (PV) industry.[1] The c-Si wafers used in these solar cells are typically $100 - 300$ μm in thickness and constitute approximately 40% of the total module cost.[2] A viable solution to reduce the cost is to use thin c-Si films of $1 - 10$ μm in thickness. However, the optical absorption in thin c-Si films is much less than that of thick films, and highly efficient light trapping is necessary to achieve the comparable level of efficiency of the thick films.

Various light-trapping schemes exist today to enhance light absorption. These schemes include light scattering by nanoparticles,[2-5] random surface corrugation,[6] nanorod arrays,[7-15] and diffraction gratings.[16-24] When metal/dielectric nanoparticles are placed on thin films, light is efficiently scattered into the underlying films at the resonance frequencies. However, the metal nanoparticles strongly absorb light, when placed on weakly absorbing photoactive films.[3] This loss limits the light trapping efficiency. Random surface roughening is another cost-effective manufacturing method to efficiently scatter light into the films. Compared to the random surface features, the light trapping can further improve by introducing periodic nanostructures, such as nanorod arrays or diffraction gratings. While nanorod-based solar cells can have strong light absorption, the surface recombination of charge carriers becomes a significant challenge because of a large surface-to-volume ratio.[11] In comparison, diffraction gratings can have a relatively small surface area while efficiently trapping the light. Based on the comparison of various light trapping schemes, metal-free, periodic, light-

trapping nanostructures with a small surface area would provide an ideal solution to achieve high efficiency in thin film solar cells.

Han *et al.* recently reported that proper symmetry-breaking in periodic nanostructures enhances light-trapping.[16] This improvement can reduce the c-Si solar cell thickness by two orders of magnitude, while achieving the same efficiency as thick flat c-Si films with an antireflection coating. However, fabricating such structures in a scalable, cost-effective, manufacturable manner remains elusive.[18, 25, 26] In this work, we introduce a new approach to systematically break the symmetry in inverted nanopyramid arrays. The fabrication relies on simple, low-cost, wet etching process steps, and does not rely on the use of off-cut Si wafers. [27, 28 27, 28 27, 28 27, 28 27, 28 27, 28 27, 28 27, 28] This method also provides a convenient platform to rapidly canvass through a large range of geometries and study the effect of symmetry-breaking on light trapping. We note that our light-trapping structures inherently minimize parasitic losses. Our approach eliminates the need for metal nanostructures for light scattering and therefore reduces metal loss. In addition, the total increase in surface area is either comparable to the microscale inverted pyramids or much less than that of nanorod arrays. These advantages make the symmetry-breaking nanostructure exceptionally suitable for high-efficiency solar cells.

Figure 1 illustrates our approach to break the symmetry in inverted nanopyramid arrays with each symmetry group denoted by the Schönflies notation. The top row of Fig. 1 shows a variety of etch templates represented by white mask with perforation. The open windows in the template are defined by lithography and dry etching. Interferometric or nanoimprint lithography can be used to define the submicron windows.

The exposed underlying c-Si is then etched in an alkaline solution to create the inverted nanopyramids shown in the bottom row of Fig. 1.

In Figure 1, we use a square lattice with C_{4v} symmetry with its side parallel to the [110] direction as the basis of comparison.[17] The first level of symmetry-breaking can be achieved by rotating the etch template and therefore the side of the square lattice around the [001] axis from the [110] direction. This lattice rotation effectively results in each inverted nanopyramid rotated around its own apex. Consequently, the mirror symmetry is completely broken while the 4-fold rotational symmetry is preserved. In addition to the rotation, the symmetry can be further broken by arranging the etch windows in non-square-lattice patterns. The possible two-dimensional non-square lattices are rectangular, triangular, centered-rectangular, and oblique lattices.[29] With the previously described sequence of symmetry-breaking, we can reduce the symmetry of inverted nanopyramid arrays down to C_2.

To fabricate symmetry-breaking inverted nanopyramids on c-Si, we use p-type Si(001) wafers with a resistivity of 1-10 Ω-cm. The etch template, going from top to bottom of its stack, is comprised of photoresist, anti-reflection coating (ARC), and SiO_2. The SiO_2 layer is thermally grown on c-Si prior to lithography. Then, a 70-nm-thick ARC layer and a 500-nm-thick photoresist (PR) film are sequentially spin-coated on SiO_2/Si. In our current effort, we make use of interferometric lithography (IL) to pattern the etch windows. The etch windows can be circular or elliptical as shown in Fig. 2 whose major and minor axes are 730 and 540 nm. The pitch varies from 670 to 1000 nm (Figs. 2 and 3). After the PR is developed, reactive ion etching in CHF_3/O_2 plasma is used to create the windows in the SiO_2 layer.

The fully developed PR/ARC/SiO$_2$ stack serves as a wet etch mask. A 20 wt% KOH solution is used to define the inverted nanopyramids into the underlying c-Si. This anisotropic etching step leaves flat unetched areas between the inverted pyramids (Fig. 3), which reduce light trapping.[17] To minimize the unetched areas, we use a solution mixture of HNO$_3$ and HF (300:1) to further etch the c-Si isotropically.[30] We then apply acetone rinse to remove the PR. A buffered oxide etch solution is subsequently used to remove the ARC/SiO$_2$ layer from the patterned surface, revealing an array of inverted nanopyramids. The nanopyramids are imaged either intermittently between the process steps or at the end of fabrication by an FEI Quanta 3D scanning electron microscope (SEM) operating at 15 keV electron beam energy. Figures 2(a) – (b) are a series of SEM images of the inverted nanopyramid arrays obtained from a rotated oblique lattice, where the angle between the two lattice vectors is 97º. The side of the lattice is rotated around [001] axis approximately by 22.5º from the [110] direction. The outer set in (a) shows a partially etched surface under the SiO$_2$ template after 70-second anisotropic etching. The inset in Fig. 2(a) shows a de-magnified view of the surface after 90-second anisotropic etching, and the bird's eye view of this surface is shown in Fig. 2(b).

Figure 3(a)-(c) show our fabricated inverted nanopyramid arrays with C$_{4v}$, C$_4$, and C$_2$ symmetry, respectively. The C$_4$ and the C$_2$ structures are obtained by rotating the square and rectangular template lattices according to our scheme in Fig. 1. The rotation angle is approximately 22.5^o. This angle is chosen to be one half of 45° to further reduce the symmetry from C$_{4v}$ or C$_{2v}$, either of which results from 0 and 45° rotations. We note that the unetched flat area in Fig. 3(b) is reduced to that in Fig. 3(c) by extending the isotropic etching time. Further isotropic etching completely removes these unetched

regions. The resulting inverted nanopyramids show a long-range order over 2.5 cm $\times$ 2.5 cm substrates, and the insets in Fig. 3 show the uniformity in a de-magnified view. Overall, we have achieved systematic symmetry-breaking in inverted nanopyramid arrays on c-Si(001) surfaces with scalable lithography and simple wet etching.

To quantitatively estimate the level of enhanced light trapping by our symmetry-breaking scheme, we have calculated optical absorption in c-Si for inverted nanopyramid arrays of C_{4v}, C_4, and C_2 symmetries for normally incident light. Figure 4(a) shows that, overall, our systematic symmetry-breaking along the $C_{4v} \rightarrow C_4 \rightarrow C_2$ sequence increases the absorption in c-Si. In this calculation, the inverted nanopyramids are etched into a 2-μm-thick c-Si film, and a 60-nm-thick Si_3N_4 conformal coating with 1.9 refractive index is used for anti-reflection. The reason for choosing the thickness of 2 μm is to assess how effectively our symmetry-breaking nanopyramids would trap the light for thin c-Si solar cells as a potential replacement for thick c-Si solar cells. The simulated c-Si film has a 717-nm-thick SiO_2 film and a 150-nm-thick Ag layer on the backside as a reflector. For the described configuration, the optical calculations match well with the experimental results for C_{4v} symmetry demonstrated in a previous study.[17] For the C_4 and C_2 structures, the simulated inverted nanopyramids are rotated by 22.5$^{\text{o}}$ resulting in structures that correspond to our experimental results in Fig. 3 (b) and (c). The C_{4v} and C_4 structures exhibit absorption that is independent of the polarization of incident light due to their 4-fold rotational symmetry. This degeneracy is lifted for the C_2 structure by breaking the 4-fold rotational symmetry. This results in enhanced absorption over the *broad* useful sunlight spectrum through the increased number of resonances for unpolarized light.

In Fig. 4(a), each structure is optimized to have maximum performance by varying the periodicity. The performance is characterized by the ultimate efficiency η,[31] which is defined as the maximum efficiency of a photovoltaic cell as the temperature approaches 0 K when each photon with energy greater than the band gap produces one electron-hole pair:

$$\eta = \frac{\int_0^{\lambda_g} I(\lambda)A(\lambda)\frac{\lambda}{\lambda_g}d\lambda}{\int_0^{\infty} I(\lambda)d\lambda} \quad , \tag{1}$$

where I is the AM1.5G solar spectrum,[32] A is the absorptance in c-Si, λ is the wavelength, and λ_g is the wavelength corresponding to the band gap. The optimized periodicity is 700 nm for both C_{4v} and C_4 symmetry inverted nanopyramid arrays. Figure 4(b) shows the efficiency map of the structures for various combinations of periodicities from 500 to 1000 nm in the x and y directions. The angle between the x-axis and the [110] direction is fixed at 22.5°. This map shows that the maximum efficiency occurs when the periodicities are 800 and 900 nm in the x and y directions, respectively. This optimum structure is similar to our experimental structure in Fig. 3(c). The optimum periodicities show that, for maximum light trapping with inverted nanopyramids, the symmetry should be broken from C_4 to C_2 but not by a great degree of change in periodicity from that of C_4. The optimum ultimate efficiencies obtained for C_{4v} (not shown in the map), C_4, and C_2 symmetry inverted nanopyramids are 0.337, 0.350, and 0.362, respectively. This implies that, if a solar cell with C_{4v} inverted nanopyramids has a 25% photovoltaic efficiency at the cell level, the C_2 symmetry structures would provide a 26.9% efficiency.

In conclusion, we have introduced a simple method to systematically break the symmetry on c-Si(001) surface for enhanced optical absorption in solar photovoltaics.

This method uses cost-effective, manufacturable, wet etching steps, and does not rely on off-cut wafers. The symmetry of inverted nanopyramids can be reduced by rotating the etch template about the [001] axis and using five different lattice types. Following this approach, the symmetry is reduced from C_{4v} to C_4 to C_2. Our calculations demonstrate that, as the symmetry of the inverted nanopyramids is broken in the $C_{4v} \rightarrow C_4 \rightarrow C_2$ sequence, the photovoltaic efficiency increases along the path. We are currently working towards integrating our symmetry-breaking structures into c-Si solar cells according to the design provided by the US National Renewable Energy Laboratory. We expect that our method of symmetry-breaking will be useful not only for light trapping, but also for spectrally tuned light absorption and emission. Our symmetry-breaking approach is also broadly applicable to other optical material systems, such as organic photovoltaics and optoelectronic devices. That is, our symmetry-breaking scheme provides a versatile experimental platform to study the effect of nanostructure symmetries on various optical phenomena.

ACKNOWLEDGMENT

Figure 1. Schematic approach to systematically break the symmetry by rotating the etch template and arranging the openings in various lattice types. Top figures show the etch template rotated about the [001] axis. The flat region on the right side of each c-Si wafer indicates the [110] direction. Subsequent etching in an alkaline solution defines inverted nanopyramids on c-Si (001) surfaces (bottom figures). The resulting symmetries are labeled in Schönflies notation.
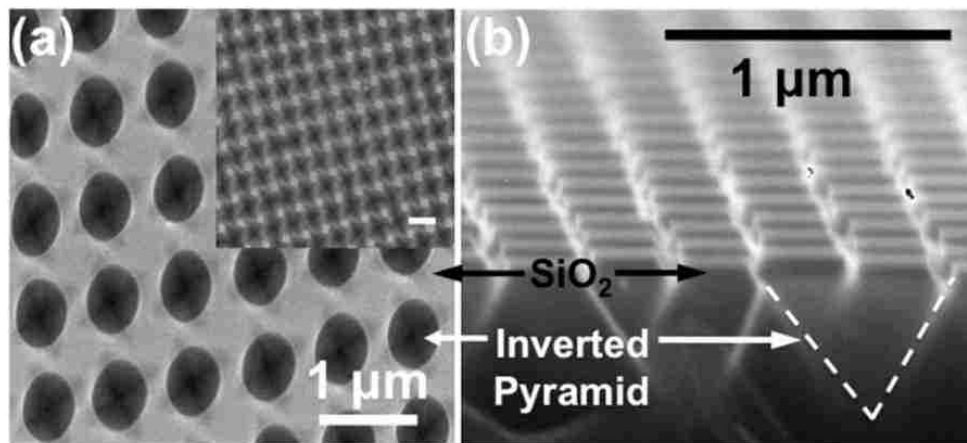
Figure 2. (a) Plan view and (b) bird's eye view scanning electron micrographs of symmetry-breaking inverted nanopyramid arrays. These structures are obtained from an oblique lattice whose side is rotated by approximately 22.5° around [001] axis. The angle between the two lattice vectors is approximately 97°.
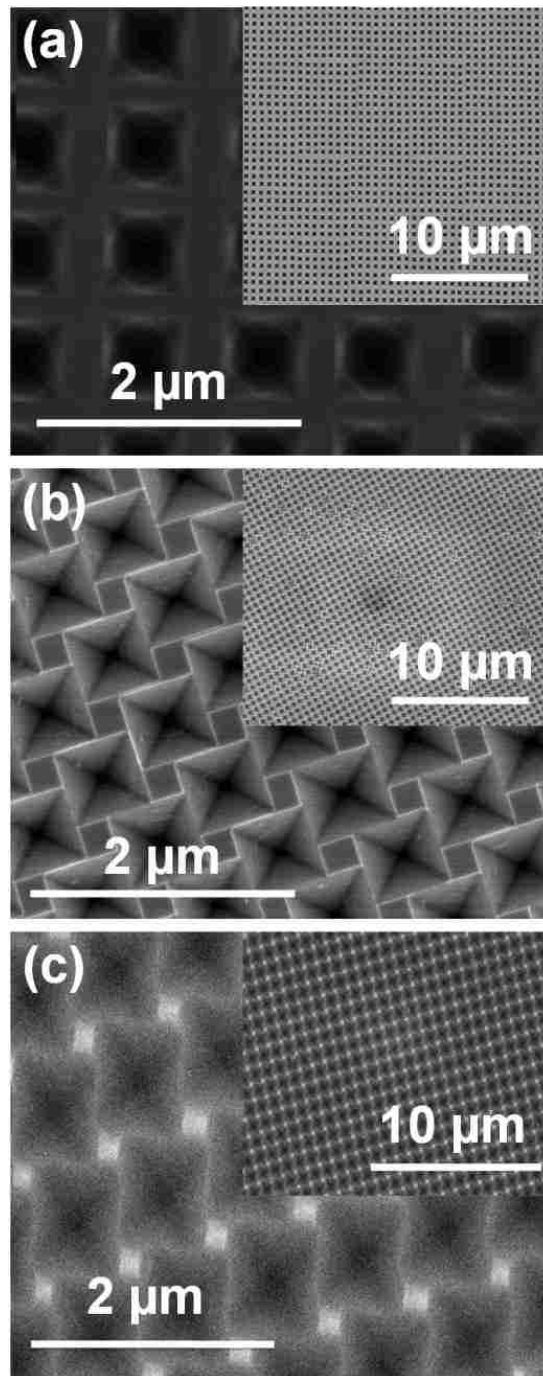
Figure 3. Scanning electron micrographs of the inverted nanopyramid arrays with (a) C_{4v}, (b) C_4, and (c) C_2 symmetry. The insets are a de-magnified view of each structure. These structures are obtained after anisotropic etching of (a) 70 seconds and (b,c) 105 seconds and, subsequently, isotropic etching of (a) 0 seconds, (b) 3 seconds, and (c) 12 seconds. In (b) and (c), each pyramid is rotated by approximately 22.5° around its own apex from [110] direction.
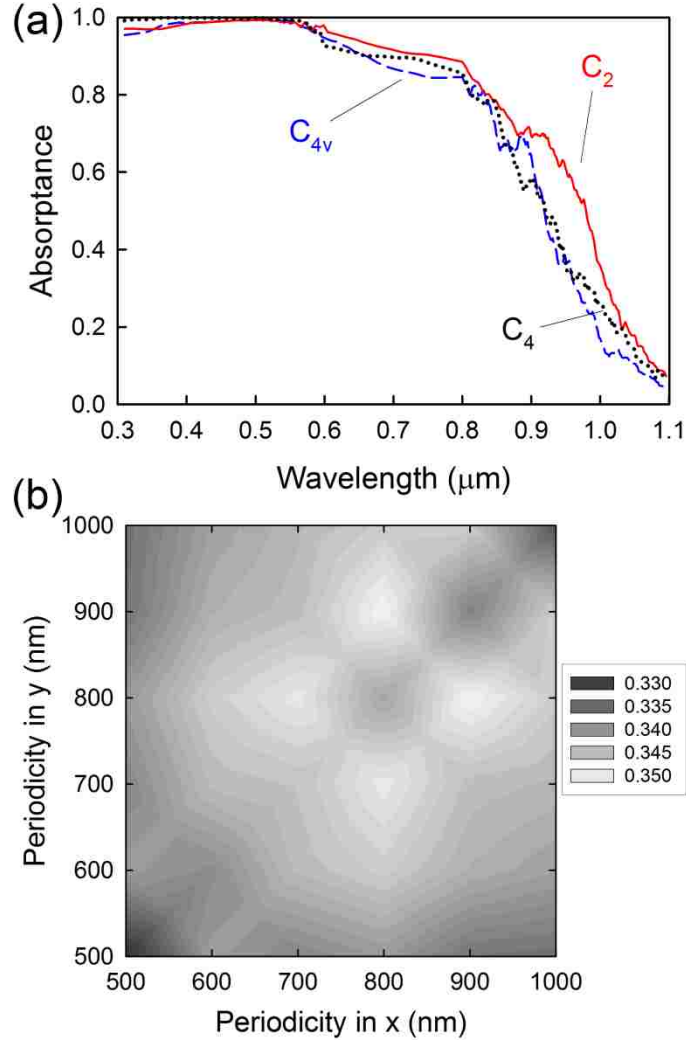
Figure 4. (a) Calculated absorptance spectrum in c-Si for the inverted nanopyramid arrays of C_{4v} (dashed), C_4 (dotted), and C_2 (solid line) symmetry. For C_4 and C_2, one side of the square lattice is rotated about the [001] axis by 22.5^o from the [110] direction. For maximum efficiency, the array periodicity is 700 nm for C_{4v} and C_4 and 800 nm $\times$ 900 nm for C_2. (b) Calculated ultimate efficiency for the inverted nanopyramid arrays with various periodicities in x and y directions, where the angle between x-axis and [110] direction is 22.5^o. Transfer matrix method is used for the calculations.[33]

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