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THERMOMECHANICAL STRESS ANALYSIS OF PACKAGING OPTIONS FOR VCSEL ARRAYS

BY

JAMES P. ROSPRIM

B.S.M.E. , RENSSELAER POLYTECHNIC INSTITUTE , 2014

THESIS

Submitted in Partial Fulfillment of the
Requirements for the Degree of

Master of Science in Mechanical Engineering

The University of New Mexico
Albuquerque, New Mexico

July, 2016

Dedication

To all my greatest Loves sacrificed in the pursuit of this achievement, Sleep, Appetite, Hobbies, Social Interactions, and Peace of Mind.

Acknowledgements

First and foremost, I would like to thank my parents, David and Susan, for their continuous support and love. I would like to thank the entire TriLumina staff for their mentorship and guidance. In particular, I would like to thank Rich Carson, Mial Warren, Kirk Otis, Tom Wilcox, and Dave Robinson for their assistance in my professional development.

Special thanks to my committee members, Dr. Chris Hall, Dr. Yu-Lin Shen, and Dr. Mial Warren for their support and advisement as I finish this chapter of my academic career.

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Abstract

This work was conducted to examine the mechanical stress occurring within Vertical Cavity Surface Emitting Lasers (VCSEL) due to packaging deformation under Continuous Wave (CW) operation. The modeling of a VCSEL device in this thesis utilized finite element analysis methodology to examine the viability and optimization of packaging options from a mechanical standpoint. Previous works have analyzed the resulting thermal stress within a single VCSEL structure, or from the standpoint of optical alignment. However, little to no work has been conducted to examine VCSEL arrays and device packaging from a mechanical stress perspective. This thesis demonstrates the resulting stress within the VCSEL array device at temperature extremes necessary for qualification in industry. Stress is found to be below documented fracture levels for two sub-mount packaging arrangements. The second sub-mount design includes copper through vias and proved to increase the overall stress in the package. Analysis of a VCSEL device bonded directly to a printed circuit board (PCB) found the use of plated through vias within the PCB to most viable. While package deformation induced larger stresses than previous designs, the VCSEL die and solder connections remained below fracture and shear failure levels. This thesis further demonstrates the most significant and cost effective method to

reduce stress in any packaging variation is through depositing solder onto the sub-mount rather than the VCSEL die.

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Abbreviations

VCSEL	Vertical Cavity Surface Emitting Laser
DBR	Distributed Bragg Reflector
LI	Light Output Power vs. Injection Current
FEA	Finite Element Analysis
AEC	Automotive Electronics Council
PCB	Printed Circuit Board
CTE	Coefficient of Thermal Expansion
CW	Continuous Wave
GaAs	Gallium Arsenide
AlGaAs	Aluminum Gallium Arsenide
AlN	Aluminum Nitride
Au(80)Sn(20)	Gold (80 % by weight) Tin (20 % by weight)
SoS	Solder on Sub-mount

1 Introduction

1.1 VCSEL Technology Overview

Vertical Cavity Surface Emitting Laser's, or VCSEL's are micro-cavity lasers that emit light in a direction normal to the wafer surface. A VCSEL structure consists of distributed Bragg reflector (DBR) mirrors on either side of a light-emitting layer, called the active region. This layer is a thin semiconductor of high optical gain, and is on the order of 1 micron or less in thickness. One DBR mirror side consists of p-doped mirrors while the other is n-doped. This allows electrical current to be injected through the DBR mirrors, forming the laser diode. These mirrors consist of multiple quarter-wave layers of semiconductor materials of differing compositions (typically $Al_xGa_{1-x}As$ or AlAs). They consist of an alternating sequence of high and low refractive index layers to produce reflectivity's greater than 99% [1]. The geometric structure of a single VCSEL can be seen below in Figure 1.1.

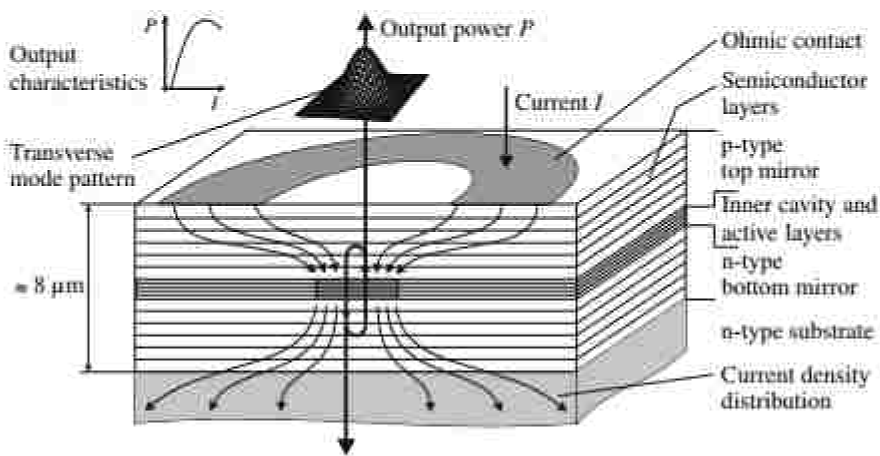
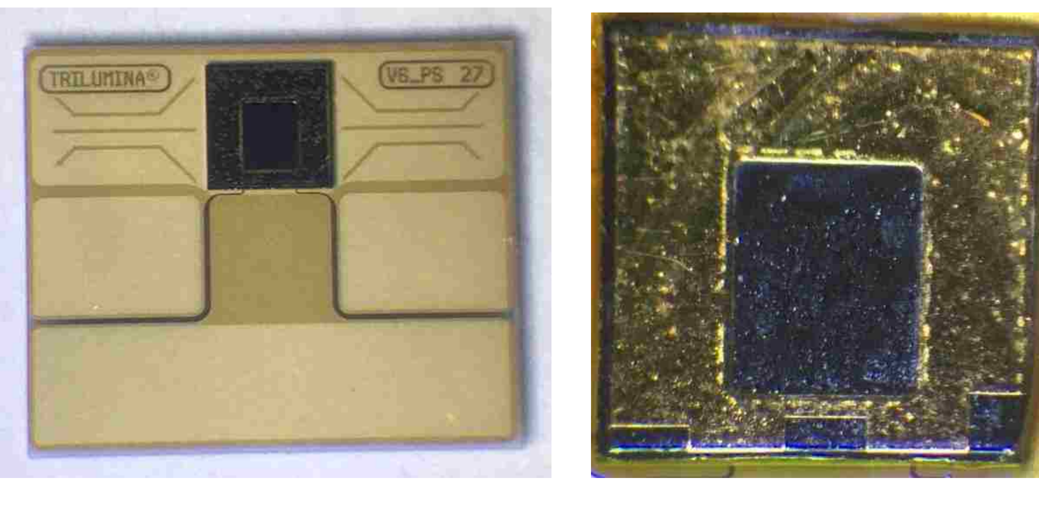


Figure 1.1 – VCSEL Layer Structure [2]

The advantages that VCSEL's hold over alternative light emitters and edge-emitting lasers include narrow beam divergence, circular beam shape, low power consumption, high modulation bandwidth, and easy polarization control [1]. Because the cavity length is small, high packing density can be achieved in designing devices using multiple VCSEL's. This also allows for large reductions in fabrication costs and testing at the wafer level, as wafers are able to yield more devices.

VCSEL devices are packaged in various ways depending on the specific application or design requirements. Figure 1.2 provides an example of one such packaging configuration in which a VCSEL die is bonded to a sub-mount. This packaging will be analyzed in this work for an Aluminum Nitride (AlN) sub-mount and a VCSEL die of proportional size.



a) Die on Sub-mount Assembly *b) Die with Au Plating*

Figure 1.2 – VCSEL Die on Sub-mount Package[1]

This packaging method is common as the coefficient of thermal expansion (CTE) material property typically matches close to that of the VCSEL device. This matching reduces the stress caused by deformation within the package under thermal loading.

[1] Packaging of actual TriLumina © VCSEL array

1.2 VCSEL Thermal Characteristics

The most recognized limitation to VCSEL performance is the thermal behavior [2]. Heating induced in the structure can cause thermally dependent behaviors and, thus, must be addressed as both a design and performance concern. This dependence is most notably seen in VCSEL's Optical Power vs. Injection Current (LI) characteristics. The device exhibits temperature dependent threshold current and optical power limitations such as injection current increases. This is known as the thermal rollover effect, whereas injection current rises, device temperature increases, limiting the maximum optical output power.

Heat generation for current driven VCSEL devices occurs through three sources. The first and most dominant heating source is from Joule heating due to current injection through resistive mirrors. The second source is due to optical free carrier absorption in doped layers, which is caused by photon reabsorbtion in the semiconductor. The third source is through non-radiative recombinations. It can be assumed that approximately 85% of the total heating occurs in the active region, with 10% occurring in the p-type DBR mirrors and 5% occurring in the n-type DBR mirrors due to Joule heating [2] [3].

1.3 Thesis Motivation

The use of VCSEL technology across multiple industries and for varying applications requires packaging solutions that are scalable, cost effective, and reliable. Devices used in varying industries need to perform in a wide range of environmental temperatures. This range coupled with the internal heating effects of VCSEL's requires packaging considerations to optimize device performance while reducing mechanical deformation caused by thermal effects. In addition, these packaging considerations need take into account the manufacturability of VCSEL devices and the tradeoffs between performance optimization/deformation reduction and cost per device.

The goal of this work is to explore alternative packaging options for VCSEL devices in an effort to quantify and potentially reduce packaging deformation from thermal stresses at the temperature extremes necessary for many industry qualifications. The feasibility of these packaging design alternatives as related to mechanical deformation and failure mechanisms is examined from both a performance and reliability standpoint, as well as a manufacturability and cost perspective.

1.4 Thesis Approach

FEA models for the different packaging options are constructed using Solidworks® Simulation tool. Internal device heating will be incorporated into the simulations from empirical data taken from operating VCSEL devices of similar geometry. Environmental temperature boundary conditions will be applied to the models to account for the range of temperatures in which functioning devices will be required to operate. The resulting stress induced in the device packages will be compared to values found in literature to examine yielding, fracture potential, and shear failure potential. These results will be consolidated to understand the feasibility of packaging alternatives and analyzed from a cost-benefit standpoint.

1.5 Thesis Overview

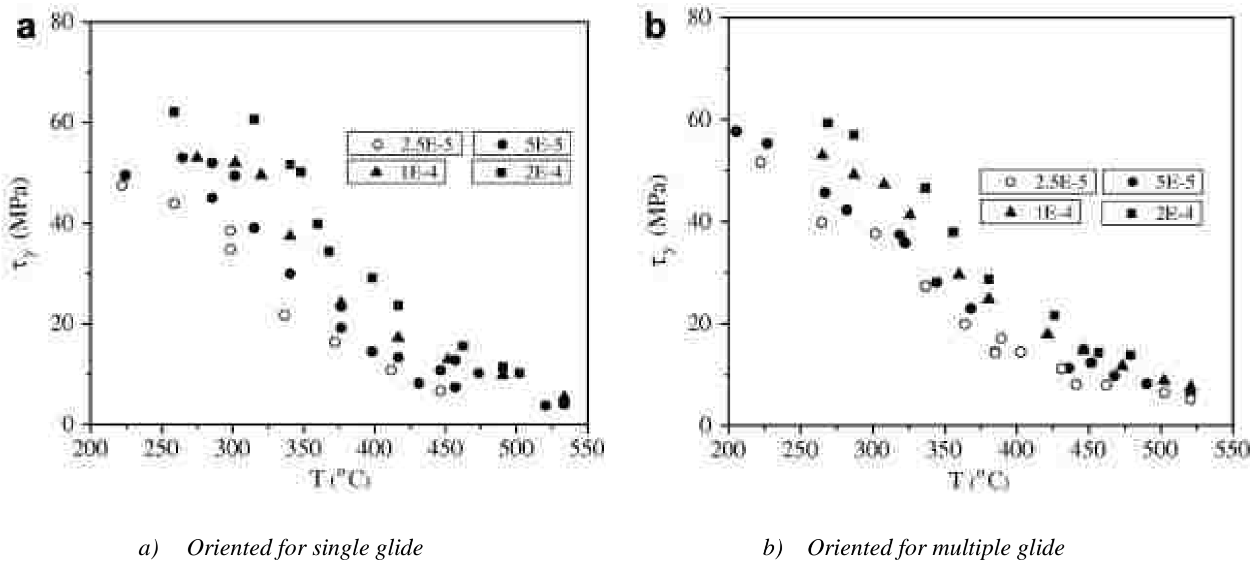
In Chapter 2, a literature review will be presented discussing previous work in semiconductor laser packaging. In Chapter 3, residual stress that occurs in the devices post flip chip bonding to a sub-mount will be quantified. VCSEL device component variables such as sub-mount gold thickness and solder deposition method will be varied in an effort to reduce this residual stress. In Chapter 4 the packaging structure and changing device component variables will again be examined, but from an operational standpoint as opposed to manufacturing. The resulting thermal stress in the device in operation will be

quantified as internal heat generation from the device and ambient temperatures drive thermal stress. Chapter 5, will again, examine stresses from internal device heating, with the inclusion of copper through vias within the sub-mount. In Chapter 6, packaging of a VCSEL device directly on a printed circuit board (PCB) will be analyzed for design feasibility and reliability. Varying PCB designs will as well be examined to reduce thermal stress in the operating VCSEL device. Chapter 7 will take into account all previous findings on design efficiency and feasibility and examine the cost benefit tradeoffs of such designs. Because these devices will be studied for practical consumer applications, rather than purely theoretical, the tradeoff between cost and device functionality is of importance.

2 Literature Review

2.1 Failure Mechanisms in Semiconductor Packaging Materials

At the lower temperature regimes in which operational VCSEL devices will be used, the semiconductor material exhibits brittle material properties. The driving failure mechanism is, therefore, cracking, or fracture deformation, as opposed to plastically yielding. Experiments to find the yield and ultimate strengths of semiconductor materials have been extensive. A series of papers presented by Wang *et al*. reported yield and fracture values of undoped single crystal GaAs. These works explored the temperature and strain rate dependence on yield stress in the brittle regime (T < 400 °C). The figures below from this work show the yield stress dependence on temperature for various strain rates [4].



a) Oriented for single glide　　*b) Oriented for multiple glide*

Figure 2.1 – GaAs Yield Stress Temperature Dependence [4]

This yield resulted in fracture and breakage of the material as opposed to plastic deformation of the material. Experiments conducted by Suzuki *et al.* and Swaminathan and Copley gained insight to yield strength of GaAs over temperature as well. Figure 2.3 describes the experimental results.

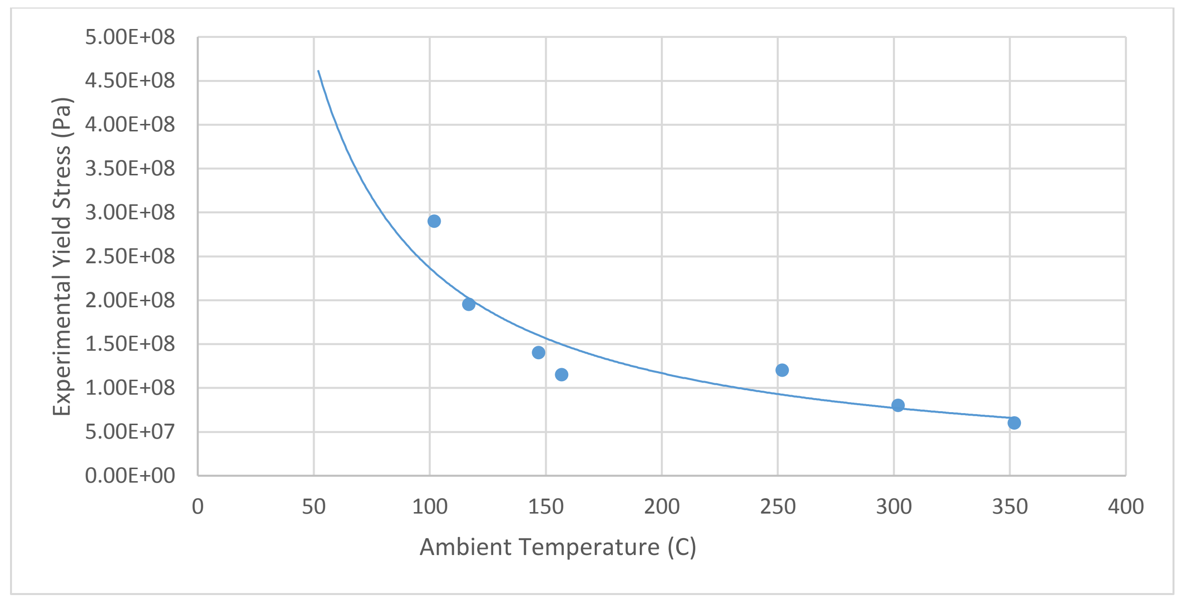


Figure 2.2 – Literature Yield Strength Values over Temperature [5] [6]

For the purposes of this study, an averaged value of 2.7 GPa will be assumed as the fracture strength of the semiconductor VCSEL material [7]. This value is in agreement with the previously mentioned studies and is taken from literature [8] [9].

Au(80)Sn(20) solder is ideal for many packaging applications as it has high strength and does not undergo stress relaxation at normal temperatures. This solder does not incur plastic deformation, and thus does not quickly degrade from fatigue or thermal cycling [10]. Figure 2.3 below shows the schematic for the stress-strain curve.

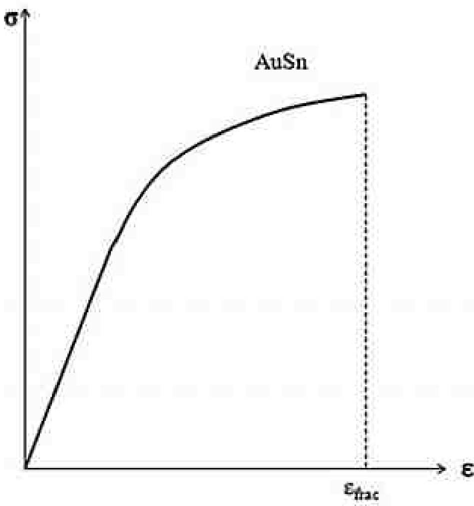


Figure 2.3 – Au(80)Sn(20) Stress Strain Curve Diagram [10]

Data provided by the manufacturer states the tensile strength of the Au(80)Sn(20) solder to be 275 MPa [11]. Similarly, Olsen and Berg found the ultimate tensile strength of various solder alloys across a wide temperature range. This work can be seen below in Figure 2.4.

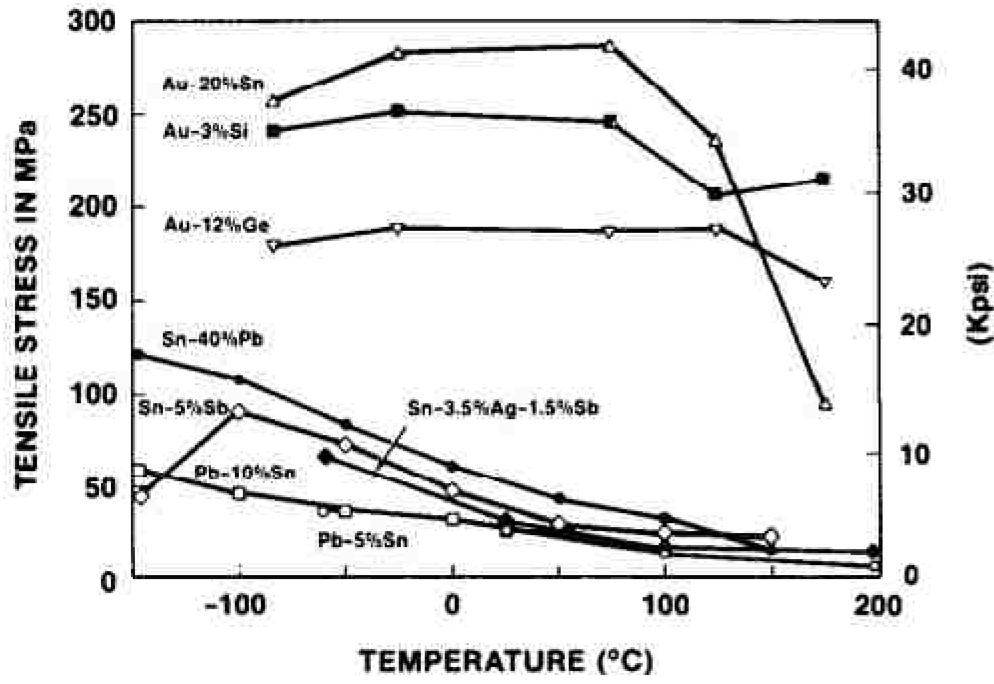


Figure 2.4 – Ultimate Tensile Strength Results – Olsen and Berg [12]

A value of 275 MPa will be used as a benchmark for the solder shear failure of the Au(80)Sn(20) interconnects and 217 MPa as the yield strength in which plastic deformation occurs [11].

2.2 Thermally Induced Stress in Layered Structures

Early work performed for modeling thermal stress in bimetallic strip structures was conducted by Timoshenko [13]. This model assumed two layers behaved like beams and were capable of both axial and bending deformation. This work led to an analytical solution for the maximum normal stress in the two metal structures, with the assumption that the stress was uniformly distributed across the length. It does not, however, provide information on stress distribution, shear stresses, or transverse stresses.

In 1949, Aleck utilized the variational principal in two-dimensional theory of elasticity to find an approximate solution for induced stresses due to a uniform change in temperature of a thin rectangular substrate clamped along an edge [14]. Aleck's method was used by Zeyfang in 1971 to study an elastic plate of finite length bonded to a rigid infinite body. He determined for long plates, the stress has a uniform component valid for the center of the plate and a non-uniform component valid for the edges [15].

Further research was conducted in 1962 by Taylor and Yuan to study the axial stresses from cooling of high-temperature bonding operations due to CTE mismatch. An elastic, one dimensional model was used to predict tensile stress locations in shear-constrained brittle strips [16]. This work was expanded upon by Chen and Nelson to include other physical conditions and geometries. Several models were developed for thermal stress in bonded joints [17].

2.3 Die and Substrate Work

The mechanical deformation of die-substrate assemblies has been addressed in a number of studies. Suhir developed models for stress distributions and curvature of bi-material and tri-material assemblies to analyze stress in elastic thin films. Suhir's analytical model is an extension of the Timoshenko model. The structure of a tri-material assembly can be seen below.

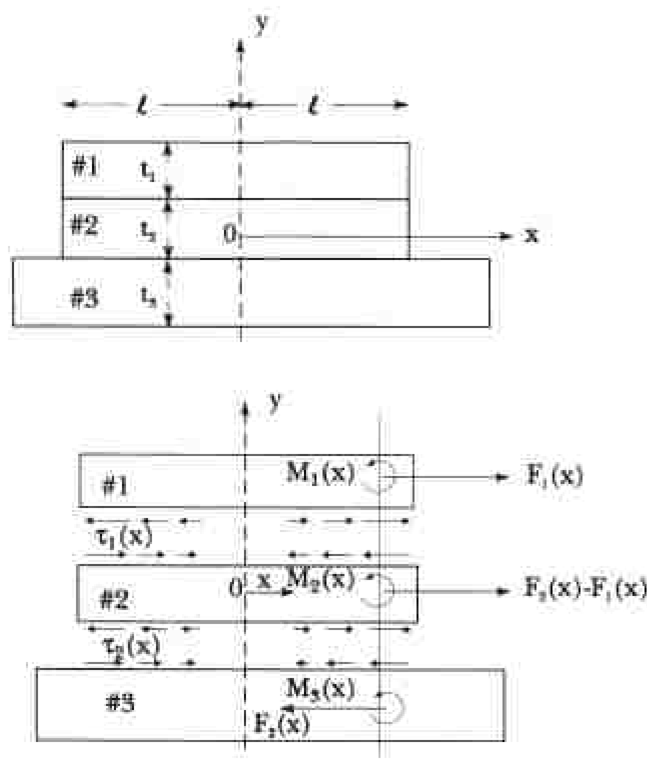


Figure 2.5 – Suhir's Stress Analysis Diagram for Elastic Thin Films [18] [19]

This model describes the displacements of the materials to be calculated as follows.

$$u_1^-(x) = \alpha_1 \Delta T x - \lambda_1 \int_0^x F_1(\zeta) d\zeta + \kappa_1 \tau_1(x) + \frac{t_1}{2} \int_0^x \frac{d\zeta}{r(\zeta)} \qquad (2.1)$$

$$u_2^+(x) = \alpha_2 \Delta T x + \lambda_2 \int_0^x [F_1(\zeta) - F_2(\zeta)] d\zeta - \kappa_2 \tau_1(x) - \frac{t_2}{2} \int_0^x \frac{d\zeta}{r(\zeta)} \qquad (2.2)$$

$$u_2^-(x) = \alpha_2 \Delta T x + \lambda_2 \int_0^x [F_1(\zeta) - F_2(\zeta)] d\zeta + \kappa_2 \tau_2(x) + \frac{t_2}{2} \int_0^x \frac{d\zeta}{r(\zeta)} \qquad (2.3)$$

$$u_3^+(x) = \alpha_3 \Delta T x + \lambda_3 \int_0^x F_2(\zeta) d\zeta - \kappa_3 \tau_2(x) - \frac{t_3}{2} \int_0^x \frac{d\zeta}{r(\zeta)} \qquad (2.4)$$

These equations include the axial and interfacial compliances for the layers, $\lambda_i = (1 - v_i)/E_i t_i$ and $\kappa_i = t_i/3G_i$, $i = 1,2,3$ respectively. $F_i\,(x)$ are the in-plane forces acting on the layers, τ_i is the shearing stress, t_i is the thickness, E_i is the elastic modulus, G_i is the

shear modulus, v_i is Poissons ratio, α_i is the coefficient of thermal expansion, l is the half length of the structure, r is the radius of curvature of the composite structure, ζ is a spatial variable, and ΔT is the melting point minus the given temperature. In the above equations, the first term accounts for the unrestricted thermal expansion in the layers, the second terms are due to the forces in a given cross sectional location x. The assumption is made here that the forces are constant over the thickness. The third term accounts for the non-uniform shearing force distribution in the direction normal to the materials interface. The fourth term results from the bending in the structure. Additionally, the bending moments shown in Figure 2.5 are described as follows.

$$M_i = -D_i/r(x) \quad (2.5)$$

They are related to D_i, the flexural rigidities by

$$D_i = E_i t_i^3/12(1 - v_i^2) \quad (2.6)$$

This model is effective in the preliminary determination of whether the ultimate strength of the die is able to accommodate a particular die attachment. Suhir, as well, presented models that examined failure modes in adhesively bonded/soldered assemblies. These modes included fracturing or cracking of the die or substrate at the midpoint or corners of the interface, cohesive failure of the bonding material, and adhesive failure of the bonding material [20] [19].

2.4 Optoelectronic Device Qualification Temperatures

Qualification of operating temperatures for optoelectronic devices vary across different industries depending on the environment and intended use. Table 2-1 describes typical temperature range requirements for different industries.

Table 2-1 – Typical Industry Optoelectronic Device Temperature Range Standards

Industry	Standard Minimum	Standard Maximum
Commercial	0 °C	70 °C
Industrial	-40 °C	185 °C
Automotive	-40 °C	150 °C
Military	-55 °C	125 °C

The AEC (Automotive Electronics Council) standards define the qualification requirements and reference test conditions for qualification of microcircuits and discrete semiconductors. The AEC-Q100 specifies various 'grades' for temperature qualification. Table 2-2 includes the temperature ranges for each grade [21].

Table 2-2 – AEC-Q100 Temperature Qualification Grades

Grade	Ambient Operating Temperature Range
0	-40 °C to +150 °C
1	-40 °C to +125 °C
2	-40 °C to +105 °C
3	-40 °C to +85 °C

The temperature extremes used in this thesis are -30 °C and 140 °C. This range was chosen as it falls within qualification standards, and due to equipment limitations.

2.5 Conclusion

In examining failure mechanisms within VCSEL packaging, both brittle and ductile material must be considered. Taken from literature, the benchmark value for brittle fracture used in this work for the VCSEL device is 2.7 GPa. The ductile property of the solder

connections indicate shear stress to be the driving failure mechanism. A benchmark value of 275 MPa is used, and is taken directly from the manufacturer. Previous works have examined thermally induced stress in multilayer structures as well as die on sub-mount packaging configurations. However, little to no work has been conducted for VCSEL array devices or for varying sub-mount designs.

3 VCSEL Package Model: Manufacturing Residual Stress

3.1 Motivation

The packaging process of VCSEL array devices is of particular concern to reliability and operational success. One method employs a flip-chip bonding process in which the laser is thermo-mechanically bonded to a substrate using solder deposited on the VCSEL. This bonding process results in deformation of the device and can create residual stress during the cooling step of the process. Packaging stress was found to reduce the temperature threshold for the triggering of plastic deformation, and reduces the density power threshold for failure by Martin-Martin *et al*. [22]. Voids produced during the bonding process are known to increase device operating temperature as well as thermal and mechanical stress failures [23] [24].

Reducing this residual stress is of importance to increase device reliability and laser performance as it will mitigate the propagation of void deformations that may occur during the bonding process. The residual packaging stress post bonding will be quantified for the current device packaging[2]. Additionally, packaging variables of solder deposition and sub-mount gold thickness will be examined in an effort to reduce residual packaging stress in the VCSEL device.

[2] Packaging used for current TriLumina Corp.© devices.

3.2 Theory

Hard solders, such as Au(80)Sn(20) used in this work, are advantageous in packaging applications because of their high melting point and high strengths. Due to high yield strength (23 °C-275MPa, 100 °C-217MPa, 150 °C-165MPa) [12], the eutectic is free from thermal fatigue, which results in elastic deformation rather than plastic. Due to this high yield stress of the eutectic solder at room temperature, the residual stress post bonding is of less concern that that within the VCSEL laser structure. Crack formation, shearing stress, and peeling stress can occur due to stress developed during the bonding process and subsequent device use can propagate these and result in reduced performance or device failures. As the eutectic Au(80)Sn(20) solder is high strength, much of the stress will be transferred to the VCSEL device and not relieved by plastic deformation that occurs in soft solders.

For the purposes of this work, it is assumed the materials are isotropic. The governing equation for thermal diffusion is

$$\rho C_p u(\Delta T) = \nabla(k\nabla T) + Q \tag{3.1}$$

in which ρ is the density, k is thermal conductivity, and C_p is the heat capacity at constant pressure. Q is the heat source, and in the case of this chapter, represents the temperatures imposed on the package by the flip chip bonders heated plate and die attach tool.

A common means by which to combine complex stresses into a uni-axial stress is calculating the von Mises equivalent stress. Shown in equation form, it can be described as

$$\sigma_{VM} = \left(\frac{(\sigma_1 - \sigma_2)^2 + (\sigma_2 - \sigma_3)^2 + (\sigma_3 - \sigma_1)^2}{2}\right)^{1/2} \tag{3.2}$$

This value uses the resulting principal stresses (σ_i) to represent a critical value of the distortional energy stored in an isotropic material. The von Mises stress is traditionally used to examine plastic yielding, where the critical value being compared to represents the onset of plastic yielding. For the purposes of this study, the von Mises stress will be used to understand the uni-axial stresses occurring within the VCSEL package, and to better resolve the effects from changing design parameters.

Figure 3.1 shows the eutectic phase diagram for the Au(80)Sn(20) solder used in this work.

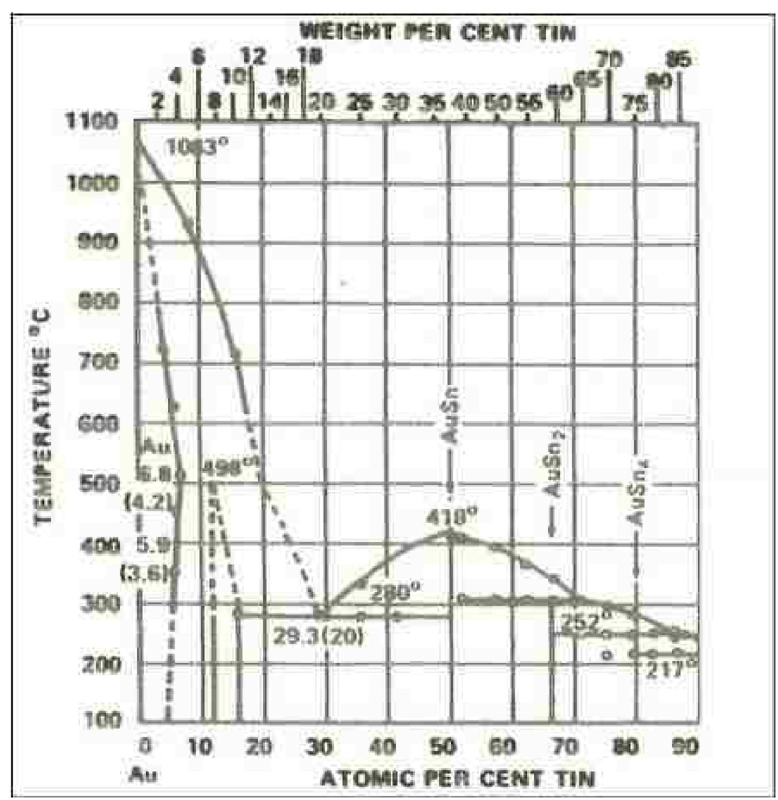


Figure 3.1 - Au(80)Sn(20) Phase Diagram [25] [11]

It can be seen that the reflow temperature of Au(80)Sn(20) eutectic solder is approximately 280 °C.

3.3 Model Development

The material properties for this study and subsequent chapters are detailed in Table 3-1.

Table 3-1 – Thermal Simulation Material Properties [22] [26] [27] [28]

Material	Modeled As	Density (g/cm^3)	Specific Heat (J/kg*K)	Thermal Conductivity (W/m*K)	CTE 10e-6 (1/K)	Elastic Modulus (Pa)
GaAs	Linear Elastic	5.3	$303 + .081T$ [2]	$-9.19 + .00317T + 16100T^{-1}$ [3]	5.8	$8.85e10 - 9.65e6T$ [2]
Al(x)GaAs	Linear Elastic	4.31	$479 + .0624T - 6.57e6T^{-2}$ [3]	$-22.7 + .00816T + 2.95e4T^{-1}$ [3]	5.39	$8.42e10 - 2.56e6T$ [2]
Au Plating	Elastic Plastic	19.282	128	315	14.4	3.5e10
Au(80)Sn(20) Solder	Linear Elastic	14.7	150	57.3	16	6.8e10
AlN	Linear Elastic	3.255	740	319	3.48	3.3e11
FR4	Linear Elastic	1200	880	.25	22	1.2e10
Copper	Linear Elastic	8900	390	390	24	1.1e11

For the FEA analysis of a VCSEL die flip chip bonded to a gold plated substrate, a number of assumptions were made. Primarily, the die consists of 400 VCSEL mesas with a pitch of 80 μm. This simplified model is used for ease of computation as the geometric

[3] Thermal Dependence Equations from [22]

layouts of functional VCSEL parts include various sized gold plating and pitches. Appendix A.1 gives the detailed geometric cross section, indicating material specifications and dimensions.

The thermal and mechanical properties of the multiple epitaxial layers that make up the AlGaAs structure are averaged through the structure as including the individual layers would increase the computational load significantly. The simulations were conducted on one half of the fully assembled part, with the appropriately imposed symmetric conditions included in the model. A virtual wall is imposed on the bottom of the sub mount to simulate the flip-chip bonder's heated bed. The temperature boundary conditions imposed on the top surface of the die and the bottom surface of the sub-mount follow the temperature profiles shown in Figure 3.2.

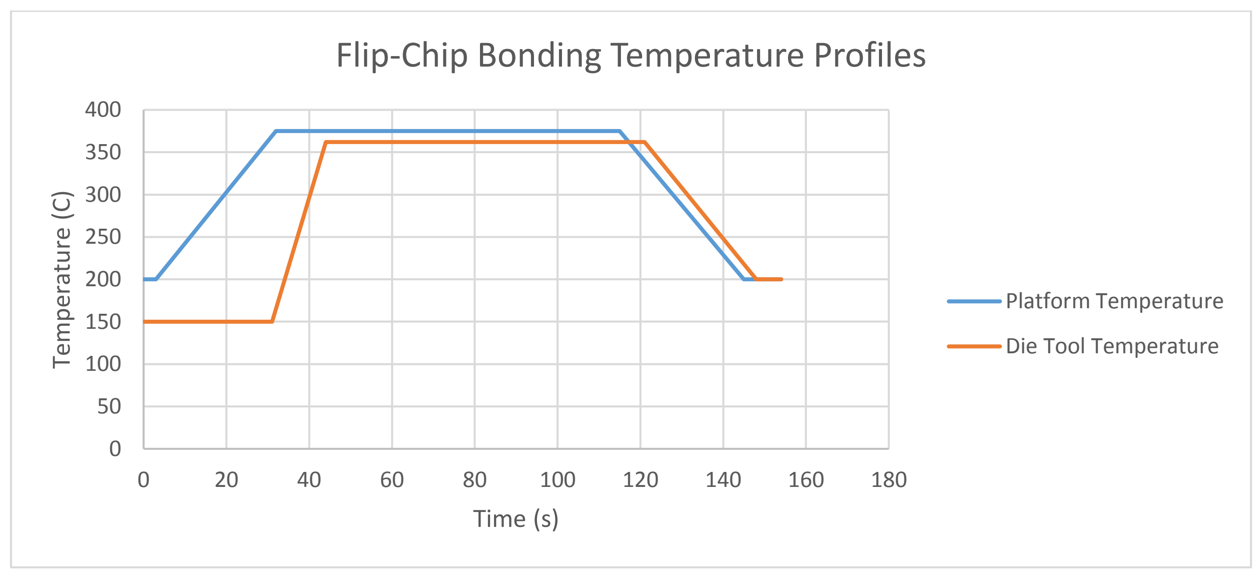


Figure 3.2 – VCSEL Flip-Chip Bonding Temperature Profiles

The die attach tool's geometry is a 2x2 mm square with a center hole to enable pressure suction. Parts used for numerous applications will include micro lenses or a silicon nitride anti-reflection coating on the top of the GaAs chip exposed to the ambient environment, and is aligned to the active VCSEL mesas. An outer perimeter of stand-off metal is added

to ensure there is no contact during the bonding process. Thus, heat transfer and pressure applied by the die attach tool will only be applied to this outer perimeter of the GaAs chip.

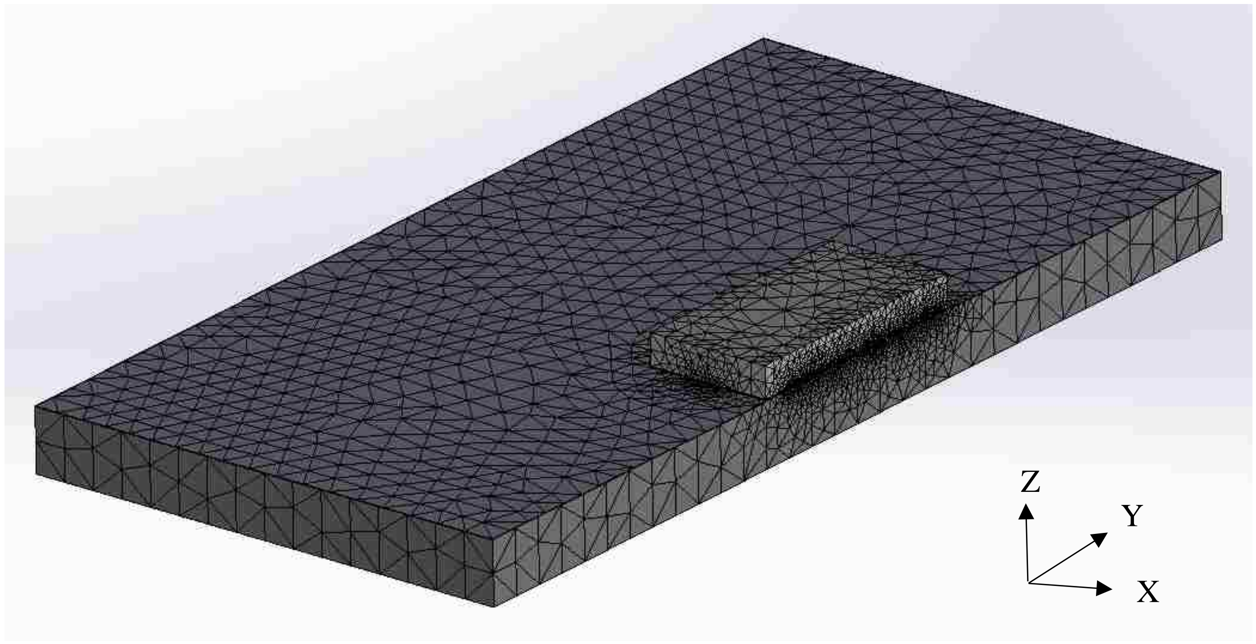


Figure 3.3 – Simulation Mesh of VCSEL Package

The half model mesh contains 31867 nodes and 125248 elements. Due to the complexity of the geometry, mesh controls were applied to the AlGaAs component and the sub-mount gold. A minimal element size of 0.005 um and a maximum of 250 um were applied to this and subsequent models with an element growth ration of 1.5. The mesh can be visualized in Figure 3.3.

3.4 Simulation Development

Post bonding residual stress will first be quantified as the packaged chip is removed and returned to ambient temperature. A nonlinear analysis is run in which the temperatures on both the GaAs chip and sub-mount are returned to a temperature of 25 °C. The stress

free temperature is prescribed to be 280 °C, the reflow temperature of the Au(80)Sn(20) eutectic solder. During the bonding process, this temperature marks the moment the device is treated as a rigid, connected package. It should be noted that residual stress from early stages of VCSEL device manufacturing, such as solder deposition by physical vapor deposition processes at elevated temperatures, is not included in the simulations.

To quantify stresses occurring during the flip chip bonding process, and to examine methods to reduce this stress, two parameters will be varied. The first parameter will be the sub-mount gold thickness (and subsequent deeper indentation) for the solder on mesa deposition method. This method involves depositing solder bumps onto the VCSEL die, and can be seen in the mask layout in Figure 3.4 where the red outlines describe the solder.

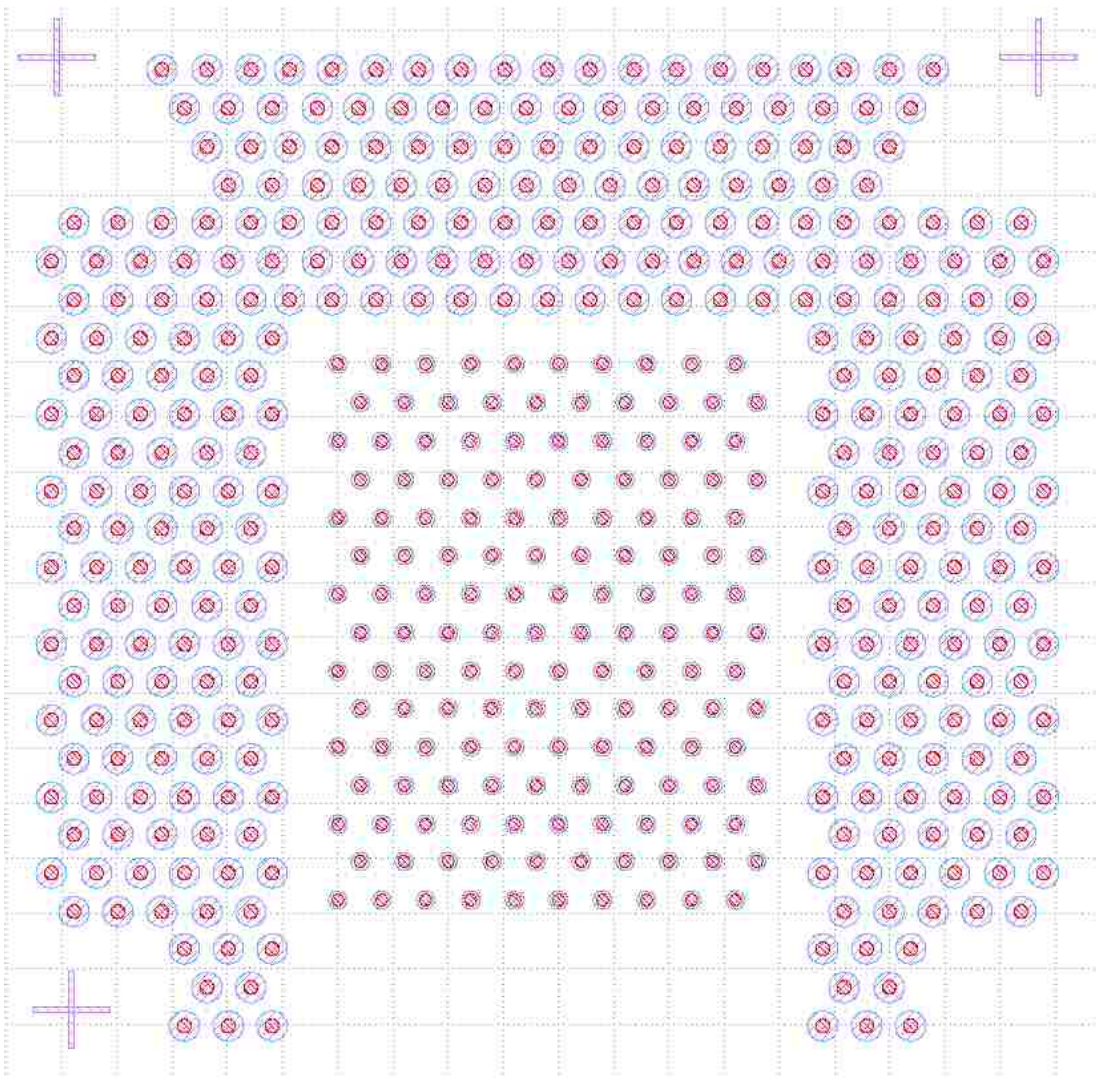


Figure 3.4 – Solder on Mesa Layout (VCSEL device)[4]

The geometric cross section can be visualized below in Figure 3.5 for a single mesa.

[4] Layout for actual TriLumina Corp. © device

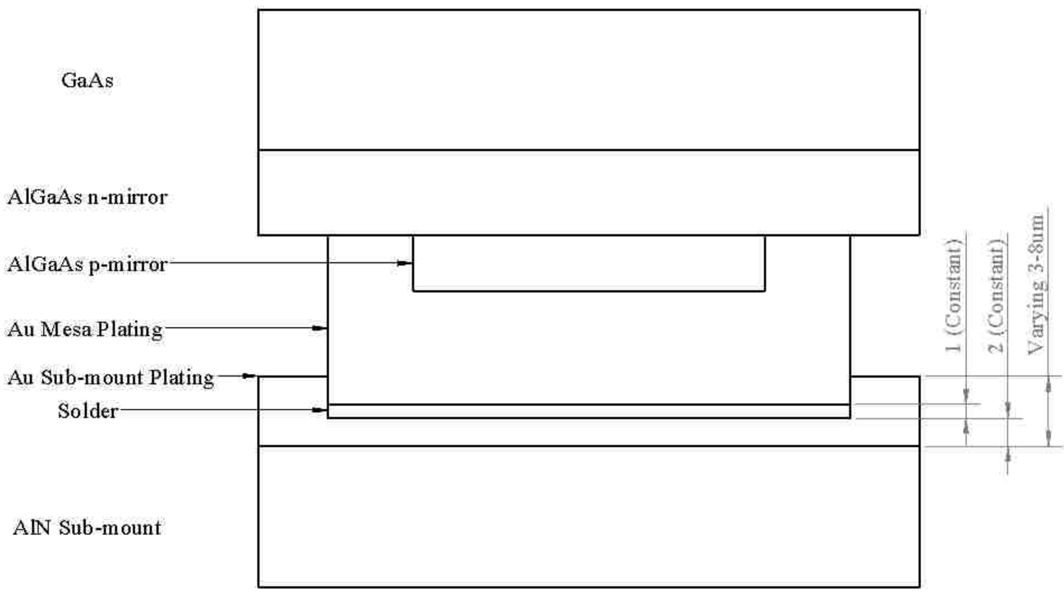


Figure 3.5 – Solder on Mesa Packaging Design

The second parameter to be examined is a solder on sub-mount (SoS) deposition method in which the Au(80)Sn(20) eutectic solder is deposited onto the sub-mount wafer as opposed to the VCSEL wafer. This will encase the mesas and sit above the gold as the solder is not specifically aligned to the mesas, but generally deposited in the overall area. In this case, a solder thickness of 3 um is used while varying the sub-mount gold thickness. The third case will examine the effect of increasing the thickness of the solder on sub-mount deposition method. The thickness of the sub-mount gold will be chosen based on the results of the previous experiment to use a thickness most advantageous to reducing the residual stress in the package. This can be seen in Figure 3.6.

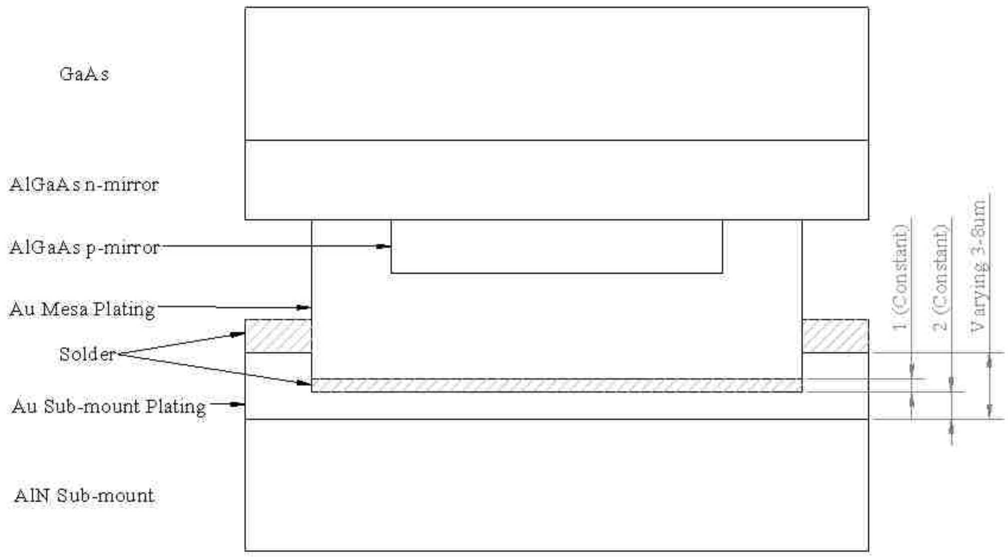


Figure 3.6 – Solder on Sub-mount Packaging Design

A symmetric boundary condition is applied to the inner face (+X direction), and the center point on the bottom face of the AlN sub-mount is fixed.

3.5 Results

The package undergoes compressive strain during cooling due to CTE mismatch between components in the package. The resulting residual stress can be seen for the package and individual components in Figure 3.7 and Figure 3.8, respectively, for a sub-mount gold height of 8 um.

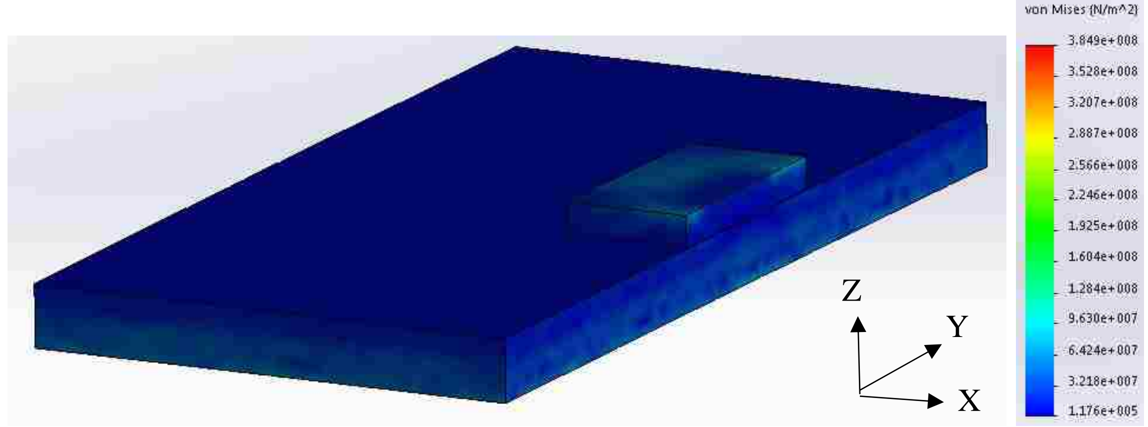
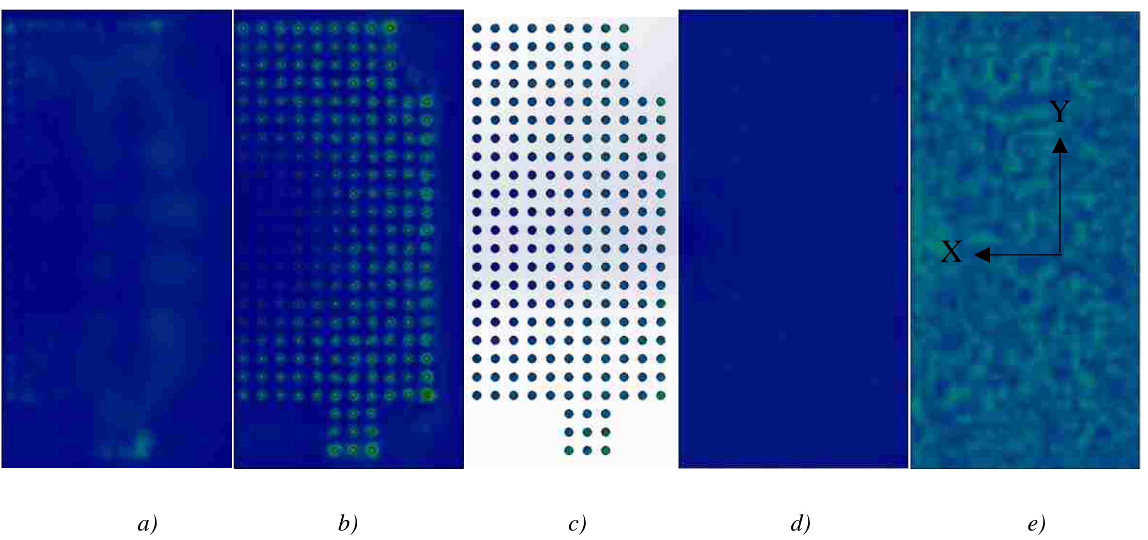


Figure 3.7 – von Mises Residual Stress Profile Solder on Mesa



a) b) c) d) e)

Figure 3.8 – von Mises Residual Stress Profile Solder on Mesa for a) GaAs b) AlGaAs c) Au Plating d) Au(80)Sn(20) Solder and Sub-mount Gold e) AlN

The maximum stress can be seen to occur in the outer VCSEL mesa structures of the array in the n-mirror DBR layers. These large values of the thermally induced stresses due to CTE mismatch in the package are in line with similar research such as Ikeda *et al.* which found compressive stress from cooling of AlGaAs/GaAs lasers to reach a maximum of 3 GPa [29]. For the varying sub-mount gold heights, the following results can be seen for the maximum and average von Mises stress in the individual components of interest, namely

the GaAs die, the AlGaAs DBR mirror components, and the AlN sub-mount. Additionally, the influence of a solder on sub-mount packaging configuration is plotted for comparison.

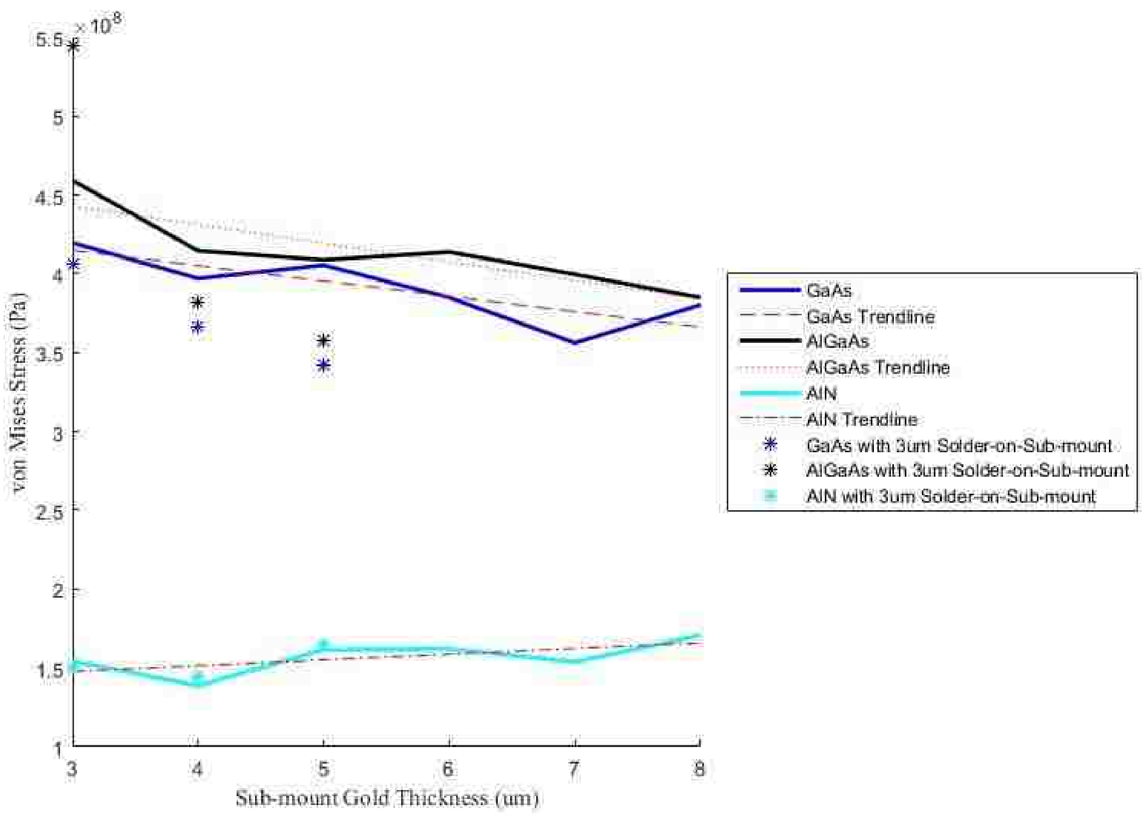


Figure 3.9 – Max von Mises Residual Stress vs Sub-mount Gold Thickness

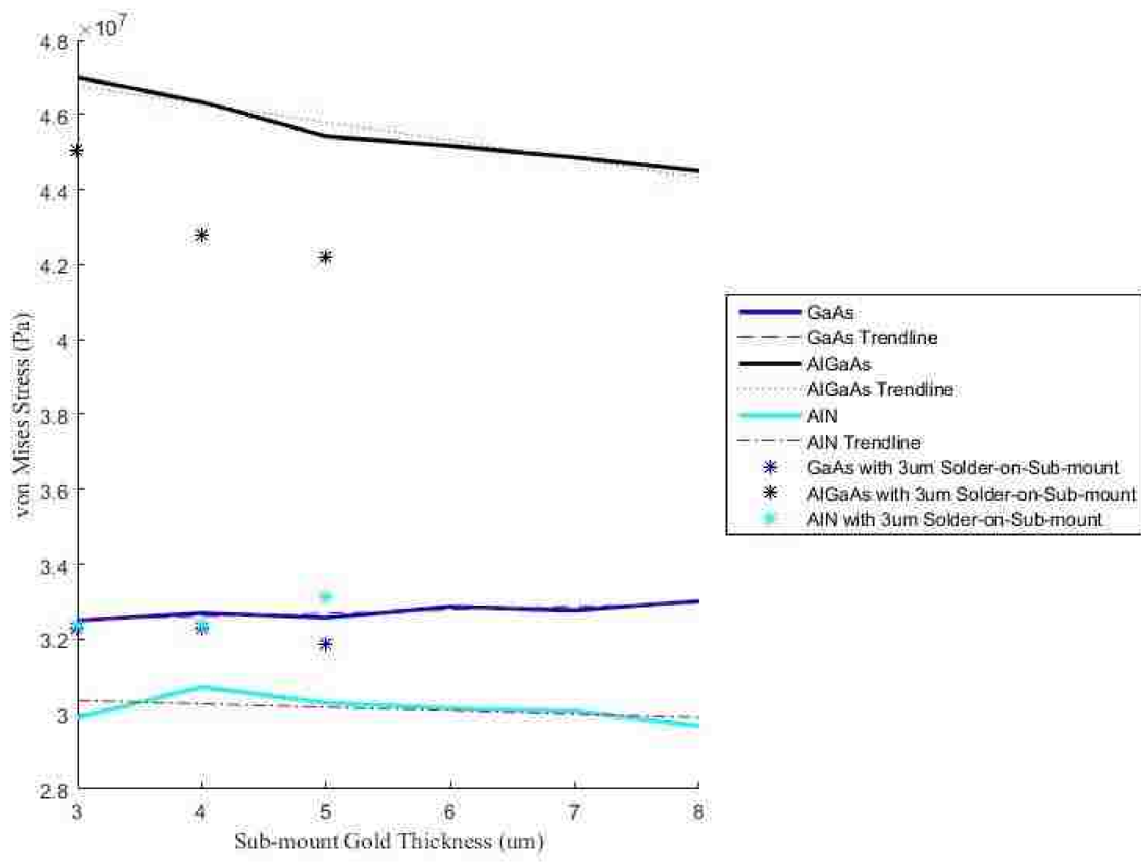


Figure 3.10 – Average von Mises Residual Stress vs Sub-mount Gold Thickness

As was seen in Figure 3.8 (b), the concentration of residual stress within the VCSEL AlGaAs component is in the outer mesas. This is shown in Figure 3.11 for the AlGaAs DBR structures with 8 um of sub-mount gold, the lowest average stress level simulated.

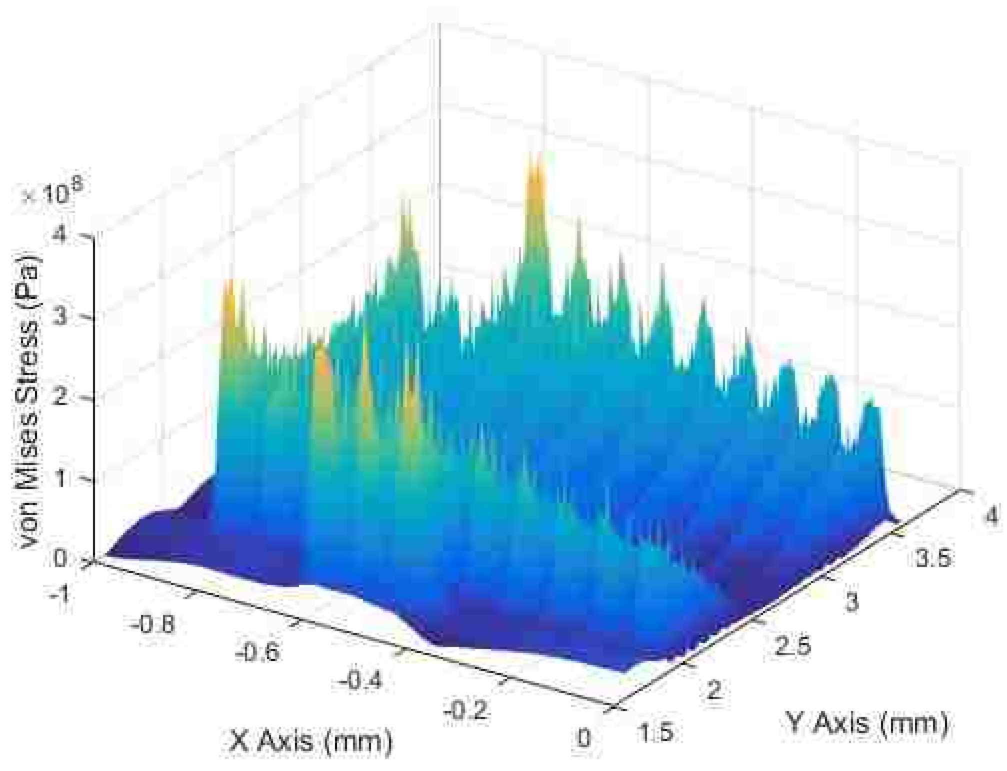


Figure 3.11 – AlGaAs von Mises Residual Stress Plot, 8um Sub-mount Gold

3.6 Conclusions

In observing the residual stress post bonding for VCSEL array packaging to a sub-mount, the simulations performed show the highest residual von Mises stress concentrated in the AlGaAs DBR mirror pairs. This concentration was seen to be predominantly within the outer mesa structures of the array. As the inner mesa structures are active VCSELS, it is of less concern that this high concentration occurs in mesa structures used explicitly for structural and electrical purposes. The location of active VCSEL mesas is described in the next chapter in Figure 4.2. The highest residual stress within the package occurred with the smallest height of gold on the sub-mount, approximately 460 MPa within the outer AlGaAs mesa structures.

The residual stress was shown to decrease in the AlGaAs DBR components and AlN sub-mount as sub-mount gold thickness was increased. Thus, increasing this gold thickness would aid in reducing residual stress from die bonding. It should be noted that these results do not account for the relaxation that occurs due to creep. For the purposes of packaging design comparison and optimization, only the residual stress when cooled to room temperature are examined to understand peak stress levels attained before relaxation.

It has been shown that the maximum residual stress resulting from the die boding process occurs in inactive mesa structures. Additionally, to reduce this residual stress in an effort to mitigate void and crack deformation, the addition of extra sub-mount gold is found to be advantageous. Utilizing a solder on sub-mount deposition method in which extra solder covers the gold mesa plating is shown to reduce the package deformation from CTE mismatch and lower the residual stress from die bonding.

Reducing the residual stress in the VCSEL can be accomplished by choosing a solder material with a lower melting temperature. Reducing the temperature difference to room temperature, or ‘zero strain’ temperature would minimize stress. The tradeoff for VCSEL devices comes from the need for a higher temperature solder. Die on sub-mount assemblies are typically integrated into larger assemblies, which use lower temperature solders. Thus, higher temperature solders are necessary to ensure the bonded connections of the VCSEL to a sub-mount do not reflow. Due to the AlGaAs component being modeled as a solid, some residual stress is not accounted for in this work. The dissimilar materials of the epitaxial layers would account for some additional residual stress given the CTE difference between them.

4 Mechanical Analysis of VCSEL Package Under CW Operations

4.1 Motivation

Under pulsed and CW operation, VCSEL devices undergo thermo-mechanical loads due to the three primary heating mechanisms described in Chapter 1. In addition to limiting optical output power of the devices, these loads induce deformation in the package as well as strain and fatigue damage in the contact joints [18]. Shear stress of the solder connecting joints will be computed and compared to literature values to ensure failure will not occur at the contact joints.

It is of interest to examine whether the thermal stresses from internal heating within an operational VCSEL device in varying ambient temperatures is sufficient to cause fracture deformation in the components, and cause failure in the solder joints due to shear stress. Because a hard solder is used in this analysis, the shear failure mechanism is of interest for connection failure. Shear failure in these joints will result in overall structure degradation in the package. Finding the principal stresses in the VCSEL package allows for comparison to fracture strength for the laser materials found in literature. As mentioned previously, the thermomechanical failure mechanism from chip substrate assemblies is fracturing of the laser die material or failure of the solder attach material.

Increasing the sub-mount gold will be examined to understand its influence on overall package temperature dissipation and stress reduction. Finally, the alternate solder on sub-mount packaging configuration previously described in Figure 3.6 will be examined for similar results in heat dissipation and stress reduction.

4.2 Theory

As mentioned in the previous chapter, the assumption is made that materials used in this study are isotropic. Additionally, for CW operations, a further assumption is made that internal heat generation within the VCSEL device exhibits steady flow conditions. The governing equations for isotropic thermal stress can be described as

$$k\delta_{ij}\frac{\partial}{\partial x_i}\left(\frac{\partial T}{\partial x_j}\right) = \rho C_v \frac{\partial T}{\partial t} - W \tag{4.1}$$

$$G u_{i,\mu\mu} + (\lambda + G) u_{\mu,\mu i} = -X_i + \beta \frac{\partial T}{\partial x_i} \tag{4.2}$$

$$\sigma_{ij} = \lambda \epsilon_{\mu\mu}\delta_{ij} + 2G\epsilon_{ij} - \beta\delta_{ij}(T - T_0) \tag{4.3}$$

where

$$\beta = \frac{\alpha E}{1 - 2\nu} \tag{4.4}$$

$$\lambda = \frac{E\nu}{(1+\nu)(1-2\nu)} \tag{4.5}$$

$$G = \frac{E}{2(1+\nu)} \tag{4.6}$$

in which W is the heat generation per unit time per unit volume, X_i is the body force components per unit volume, x_i are the space coordinates, u_i are the components of the displacement vector, β_{ij} is the thermal moduli, σ_{ij} are the components of the stress tensor, ϵ_{ij} are the components of the strain tensor. Additionally, α is the thermal coefficient of

linear expansion, k is the thermal conductivity, E is Young's Modulus, v is Poisson's ratio, λ is Lame's constant, G is the shear modulus, and δ_{ij} is the Kronecker delta [18]. For the case in which it is assumed heat flow is steady (see Equation 4.7), Equations 4.1 and 4.2 can be re-written as Equations 4.8 and 4.9, respectively.

$$\frac{\partial T}{\partial t} = 0 \tag{4.7}$$

$$\nabla^2 T = \frac{\rho C_v}{k}\frac{\partial T}{\partial t} - \frac{W}{k} \tag{4.8}$$

$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 v}{\partial x\,\partial y} + \frac{\partial^2 w}{\partial x\,\partial z} + (1-2v)\nabla^2 u + \frac{X_x}{(\lambda+G)} = 2(1+v)\alpha\frac{\partial T}{\partial x} \tag{4.9a}$$

$$\frac{\partial^2 v}{\partial y^2} + \frac{\partial^2 u}{\partial x\,\partial y} + \frac{\partial^2 w}{\partial y\,\partial z} + (1-2v)\nabla^2 v + \frac{X_y}{(\lambda+G)} = 2(1+v)\alpha\frac{\partial T}{\partial y} \tag{4.9b}$$

$$\frac{\partial^2 w}{\partial z^2} + \frac{\partial^2 u}{\partial x\,\partial z} + \frac{\partial^2 v}{\partial y\,\partial z} + (1-2v)\nabla^2 w + \frac{X_z}{(\lambda+G)} = 2(1+v)\alpha\frac{\partial T}{\partial z} \tag{4.9c}$$

Equation 4.3 can as well be rewritten using the strain-displacement relations seen below.

$$\epsilon_x = \frac{\partial u}{\partial x} \tag{4.10a}$$

$$\epsilon_y = \frac{\partial v}{\partial y} \tag{4.10b}$$

$$\epsilon_z = \frac{\partial w}{\partial z} \qquad (4.10c)$$

$$\gamma_{xy} = \frac{\partial u}{\partial y} + \frac{\partial v}{\partial x} \qquad (4.11a)$$

$$\gamma_{yz} = \frac{\partial v}{\partial z} + \frac{\partial w}{\partial y} \qquad (4.11b)$$

$$\gamma_{zx} = \frac{\partial w}{\partial x} + \frac{\partial u}{\partial z} \qquad (4.11c)$$

Equation 4.3 is then expanded to

$$\sigma_x = \frac{\lambda}{v}\left[(1-v)\frac{\partial u}{\partial x} + v\left(\frac{\partial u}{\partial y} + \frac{\partial w}{\partial z}\right)\right] - \beta(T - T_0) \qquad (4.12a)$$

$$\sigma_y = \frac{\lambda}{v}\left[(1-v)\frac{\partial v}{\partial y} + v\left(\frac{\partial w}{\partial z} + \frac{\partial u}{\partial x}\right)\right] - \beta(T - T_0) \qquad (4.12b)$$

$$\sigma_z = \frac{\lambda}{v}\left[(1-v)\frac{\partial w}{\partial z} + v\left(\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y}\right)\right] - \beta(T - T_0) \qquad (4.12c)$$

and further resolved into shear stress as

$$\tau_{xy} = G\left(\frac{\partial u}{\partial y} + \frac{\partial v}{\partial x}\right) \qquad (4.13a)$$

$$\tau_{yz} = G\left(\frac{\partial v}{\partial z} + \frac{\partial w}{\partial y}\right) \qquad (4.13b)$$

$$\tau_{zx} = G\left(\frac{\partial w}{\partial x} + \frac{\partial u}{\partial z}\right) \tag{4.13c}$$

where

$$\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} \tag{4.14}$$

These equations describe the normal stress and strains that are a result of the changing displacement components (u, v, w) in the x, y, and z directions, body forces, and temperature difference from a stress free state.

The above governing equations are incorporated into FEA software by calculating strain at the nodal points within the meshed model. These equations are condensed into nodal matrices as seen in Equation 4.15.

$$\varepsilon = \begin{bmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \\ \gamma_{xy} \\ \gamma_{yz} \\ \gamma_{xz} \end{bmatrix} = \begin{bmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \\ 2\varepsilon_{xy} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{xz} \end{bmatrix} = \begin{bmatrix} \partial u/\partial x \\ \partial v/\partial y \\ \partial w/\partial z \\ \partial u/\partial y + \partial v/\partial x \\ \partial v/\partial z + \partial w/\partial y \\ \partial u/\partial z + \partial w/\partial x \end{bmatrix} \tag{4.15}$$

Thermal strain using the temperature at each node (T), the stress free reference temperature (T_0), and the coefficient of thermal expansion vector (**α**) can be expressed as

$$\varepsilon_{th} = \boldsymbol{\alpha}(T - T_0) = [\alpha \quad \alpha \quad \alpha \quad 0 \quad 0 \quad 0]^T (T - T_0) \tag{4.16}$$

Using Hooke's Law, the stress can be found from

$$\boldsymbol{\sigma} = \boldsymbol{C}(\boldsymbol{\varepsilon} - \boldsymbol{\varepsilon}_{th}) \tag{4.17}$$

$$\boldsymbol{C} = \frac{E}{(1+v)(1-2v)} \qquad (4.18)$$

in which C is the stiffness matrix, E is Young's Modulus, and v is the Poisson ratio. A more detailed description of the constitutive equations used in the FEA analysis can be found in Appendix B.

4.3 Model Development

The model geometry is similar to that of the package used in analyzing the deformation response of the manufacturing flip-chip process described in Appendix A.1, and heat generation is prescribed to the interface between the n-mirror and p-mirror DBR solids. The interface used in lieu of a solid model of the active region can be visualized below in Figure 4.1.

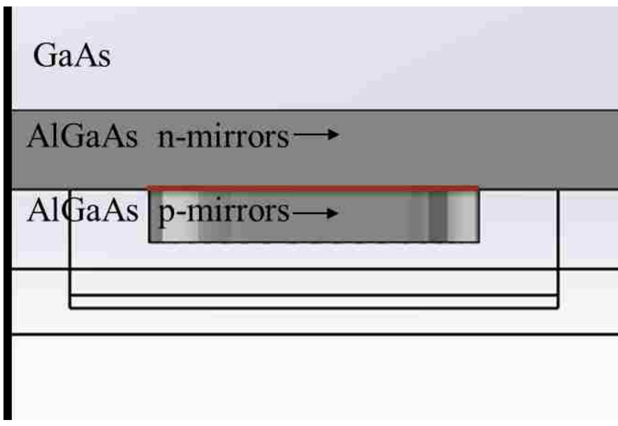


Figure 4.1 – Internal Heat Generation Location, Single VCSEL Mesa

This simulates heat generation from the active region, rather than modeling a separate solid with a thickness on the order of tenths of a micron. The device is structured to have only 150 VCSEL mesas actively generating light (75 for the half scale model), with the

surrounding mesas acting as structural support. The active VCSEL mesas are highlighted in Figure 4.2.

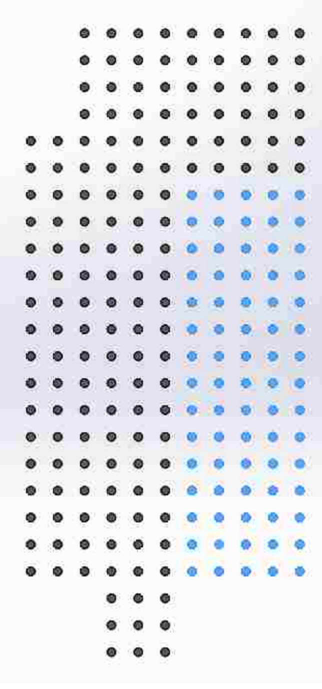


Figure 4.2 – Active VCSEL Mesa's

4.4 Simulation Development

The active region heat power used in the simulation is based on empirical data from a VCSEL package of similar geometry to accurately depict the optical power run-off over time due to heating within the device. These were run at continuous wave (CW) operation with an input current of 1 Amp. Testing over an extended period of time was conducted in a thermal oven run at 90° C. The data from these experiments can be seen below in Figure 4.3.

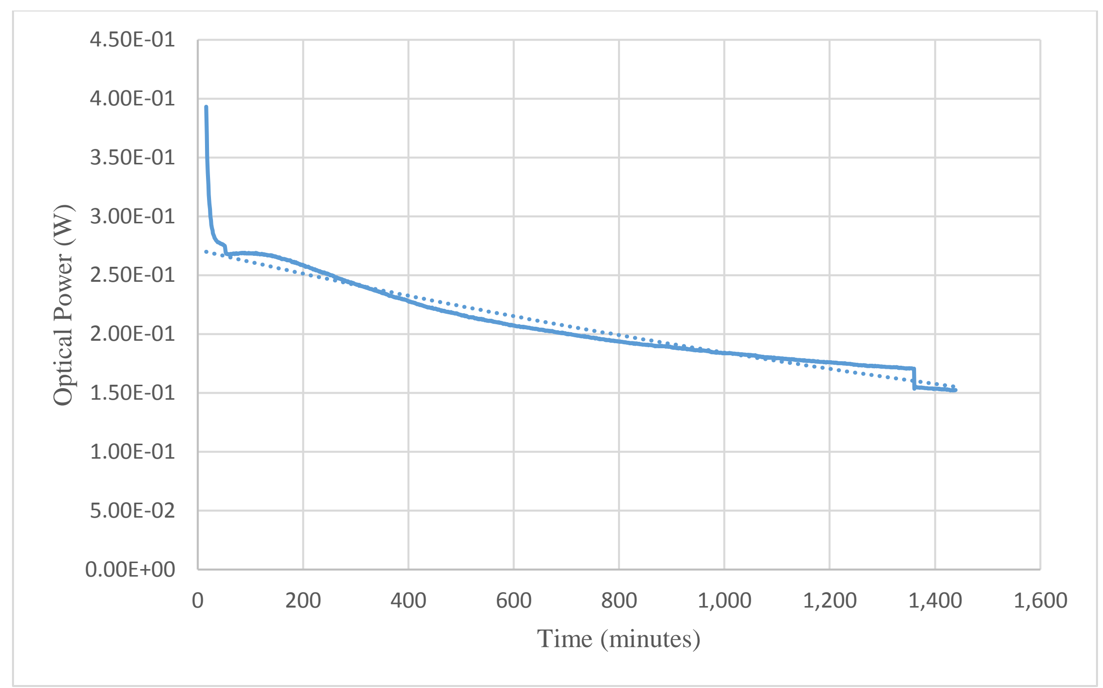


Figure 4.3 – CW Operation VCSEL Package Test

The thermal power can be found using the general assumption

$$Power_{input} = Power_{optical} + Power_{thermal} \quad (4.19)$$

For the two environmental temperature conditions, the steady state optical power output is assumed to be 0.172 W based on conducted experiments. Using Equation 4.20, the thermal power prescribed to the active region is 1.6W. The environmental temperature is prescribed to the bottom of the AlN sub-mount, simulating the heatsink the package is on to be at the ambient temperature. The nonlinear simulations are run with 25°C as the zero strain temperature. The assumption is made that relaxation effects have reduced the residual stress from bonding to a negligibly small size.

4.5 Results

Using the assumption that the zero strain temperature is 25°C, the von Mises stress at each layer can be seen below in Figure 4.6 for a sub-mount gold thickness of 8 μm and an ambient temperature of 140 °C.

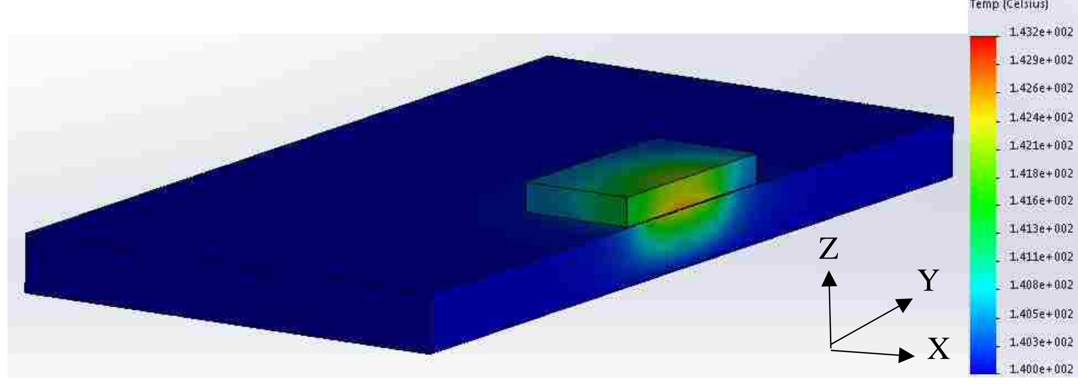


Figure 4.4 – Temperature Profile at 1.6W Heat Generation, Sub-mount Au Thickness 8um, Ambient 140°C

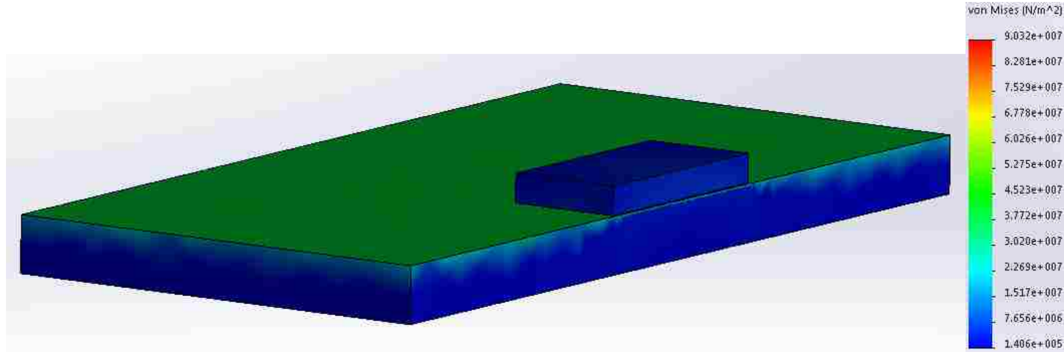
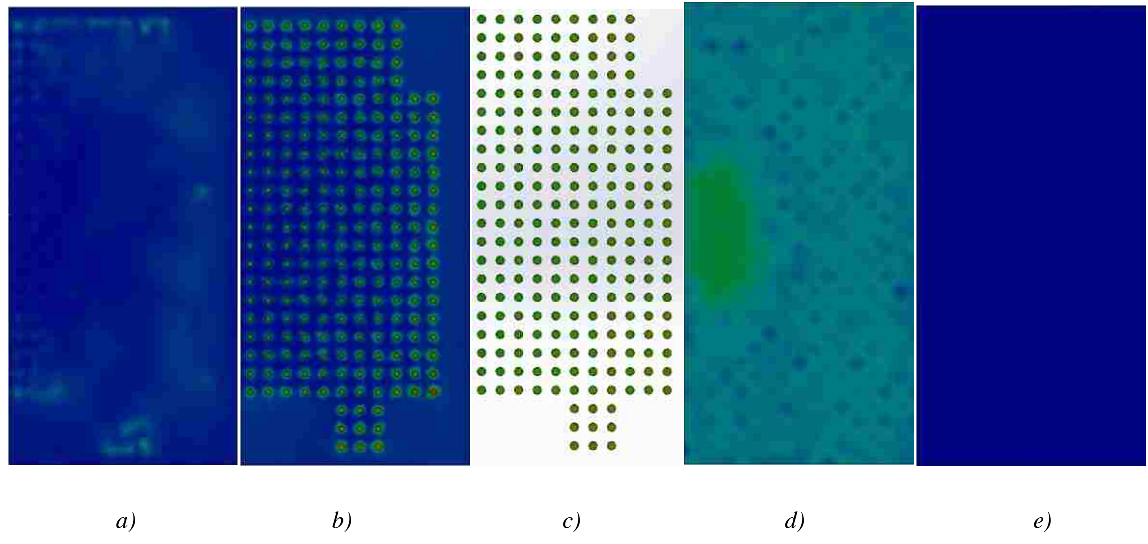


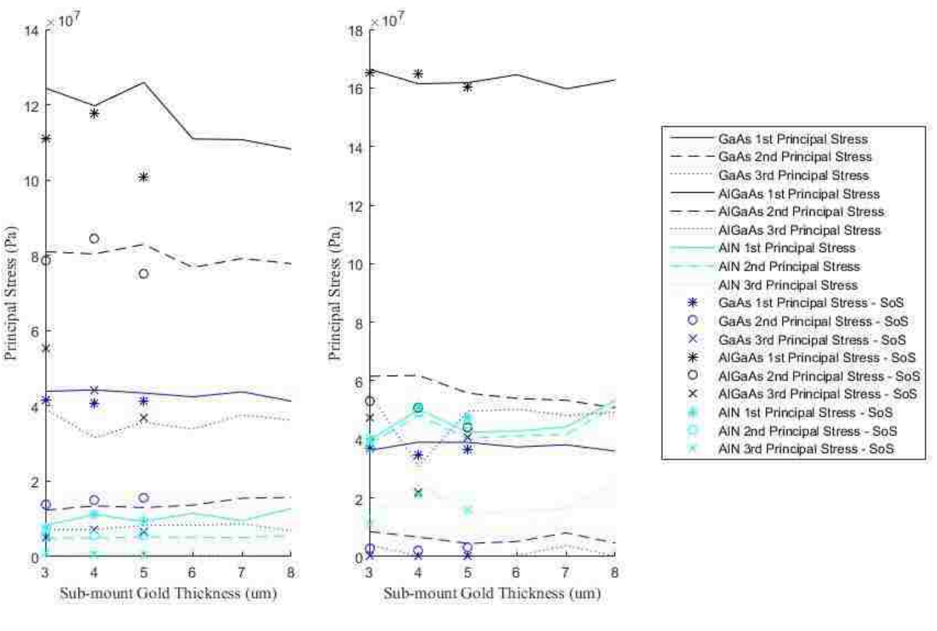
Figure 4.5 – von Mises Stress Profile at 1.6W Heat Generation, Ambient 140°C



a) *b)* *c)* *d)* *e)*

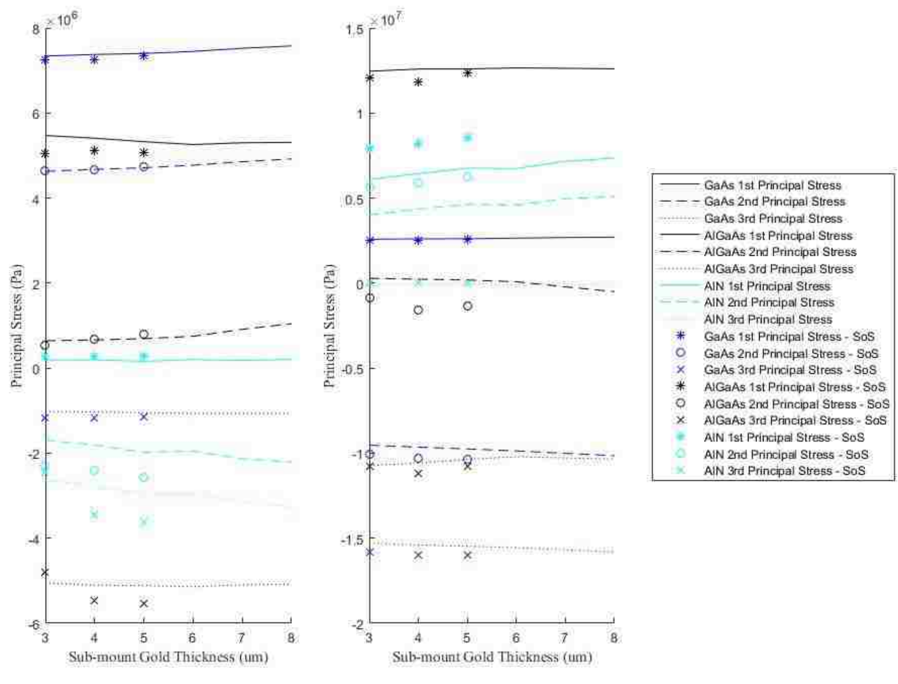
Figure 4.6 – von Mises Stress Profile for a) GaAs b) AlGaAs c) Au Plating d) Sub-mount Gold e) AlN

The maximum principal stresses occurring in the package can be seen below in Figure 4.7 for the components of concern as the sub-mount gold thickness is increased and a solder on sub-mount deposition packaging approach is taken.



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 4.7 – Maximum Operational Principal Stress vs. Sub-mount Gold



b) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

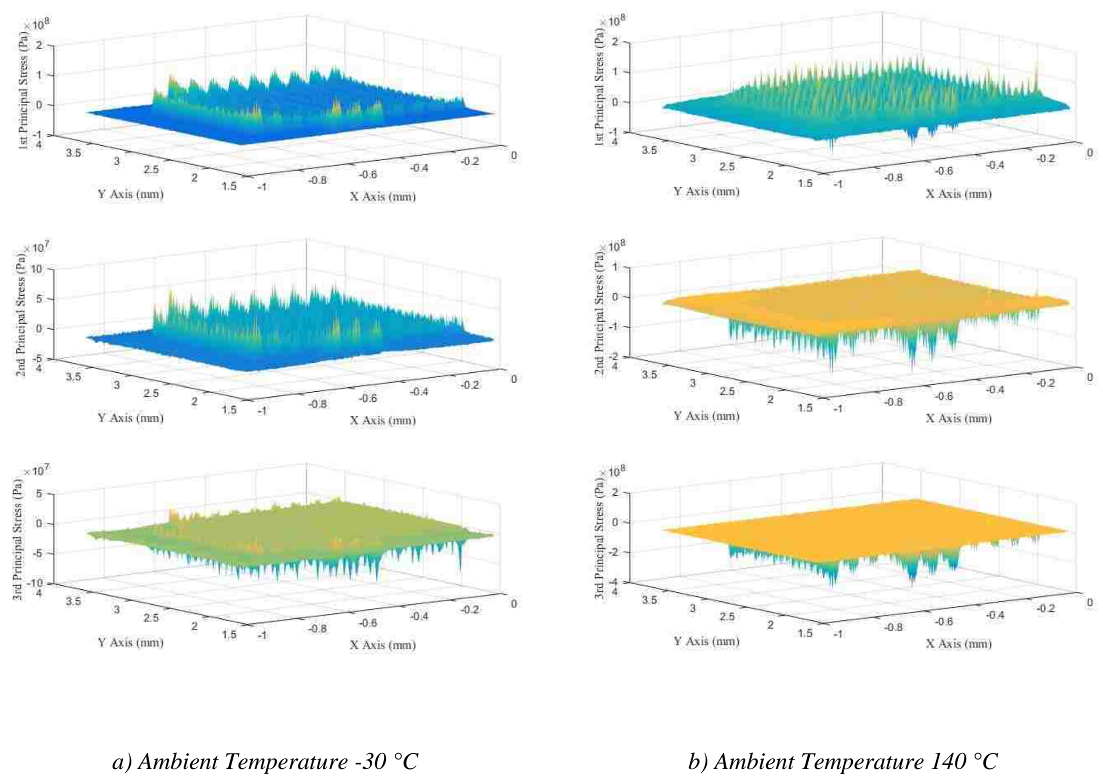
Figure 4.8 – Average Operational Principal Stress vs. Sub-mount Gold

The directionality of the normal and shear stresses is described in Table 4-1.

Table 4-1 – Principal and Shear Stress Directionality

Stress	Model Orientation	Axes	Stress Directionality
Normal Stress X σ_x		Z X	
Normal Stress Y σ_y		Z Y	
Normal Stress Z σ_z		Z X	
XZ Shear τ_{xz}		Z X	
YZ Shear τ_{yz}		Z Y	

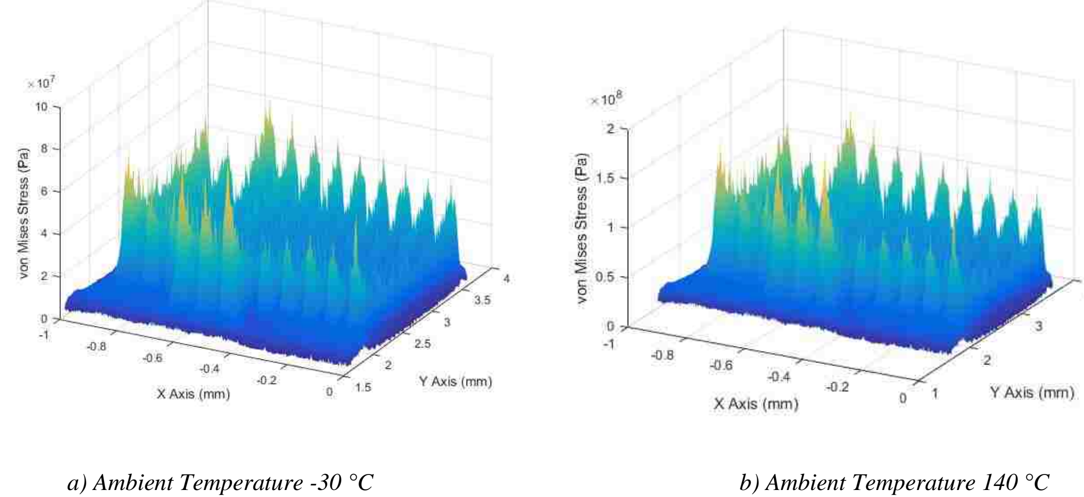
It can be seen that the effect of increasing the sub-mount gold is marginally effective in altering the average principal stresses. The maximum principal stress within the VCSEL device occur consistently in the AlGaAs component for both temperature extremes. These maximum principal stress remains below the fracture level of 2.7 GPa, as do the maximum principal stresses of the GaAs component. It can be seen that increasing the sub-mount gold is slightly effective at reducing these maximum stresses. Figure 4.9 below presents a visualization of the principal stresses within the AlGaAs VCSEL component to describe the location and magnitude at the temperature extremes.



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 4.9 – AlGaAs Principal Stresses, Sub-mount Au Thickness 5um, Solder on Sub-mount

The largest principal stresses documented in the above figures primarily occur in the outer AlGaAs mesa structures and can be further visualized in Figure 4.10 for the von Mises stress. As these are structural mesas rather than active light emitting mesas, the device performance is predicted to remain reliable. This is further supported by Figure 4.8 which describes the average principal stresses within the components being far below fracture level.

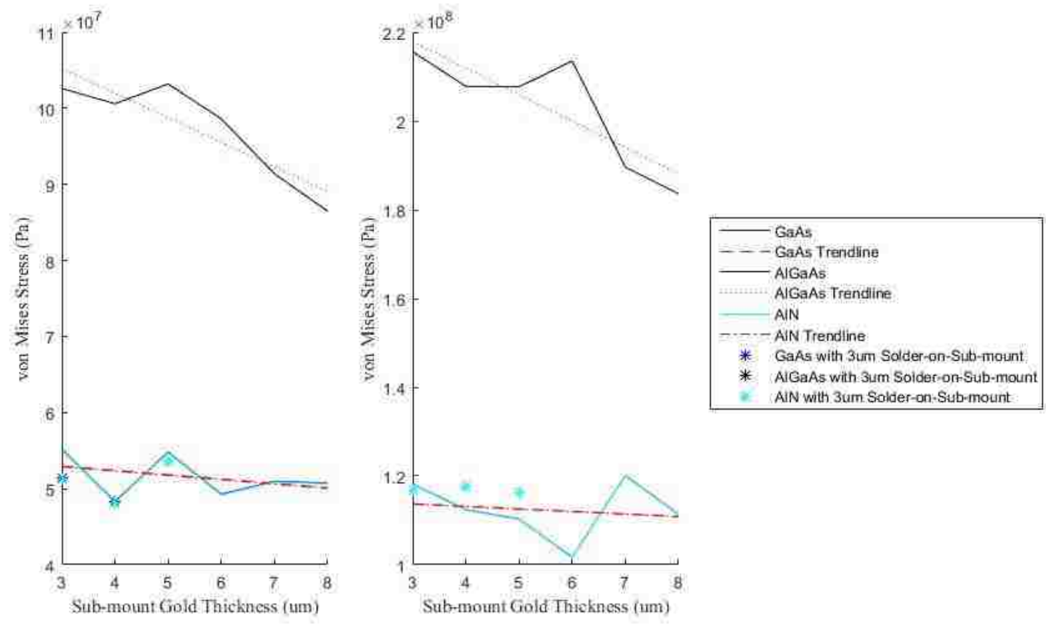


a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 4.10 - Operational von Mises Stress in AlGaAs Components, Sub-mount Au Thickness 8um

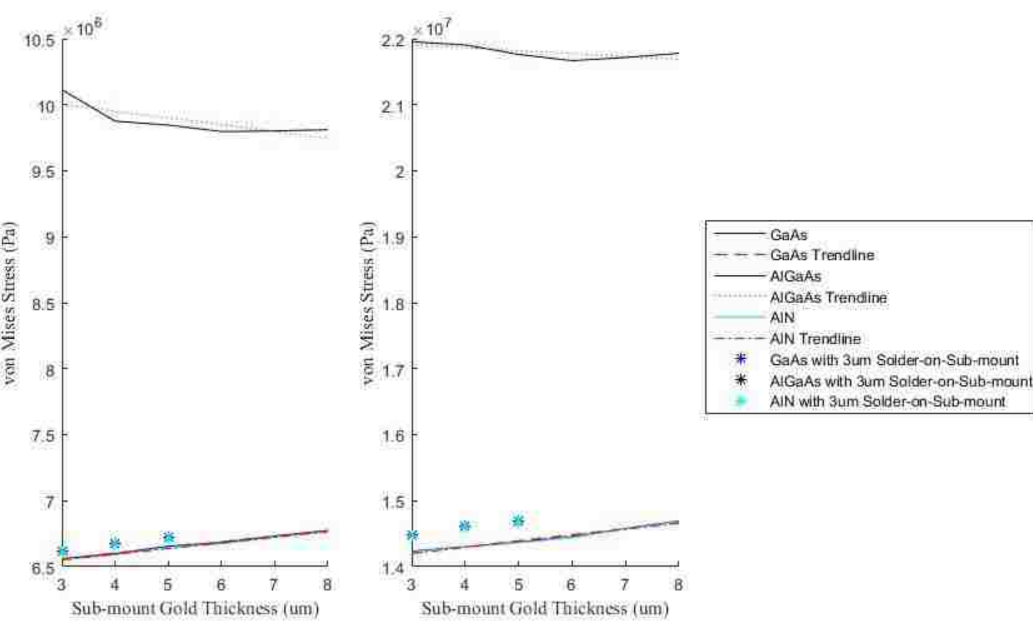
The adoption of a solder on sub-mount approach results in a slight reduction of the maximum principal stress within the GaAs die. Additionally, solder on sub-mount reduces the maximum principal stress in the AlGaAs component at both temperatures, but is seen to be more effective at -30 °C. This is due to the extra solder along the sides of the mesas providing resistance to the concave deformation that occurs.

The following figures detail the von Mises and shear stresses in the package for varying sub-mount gold thicknesses.



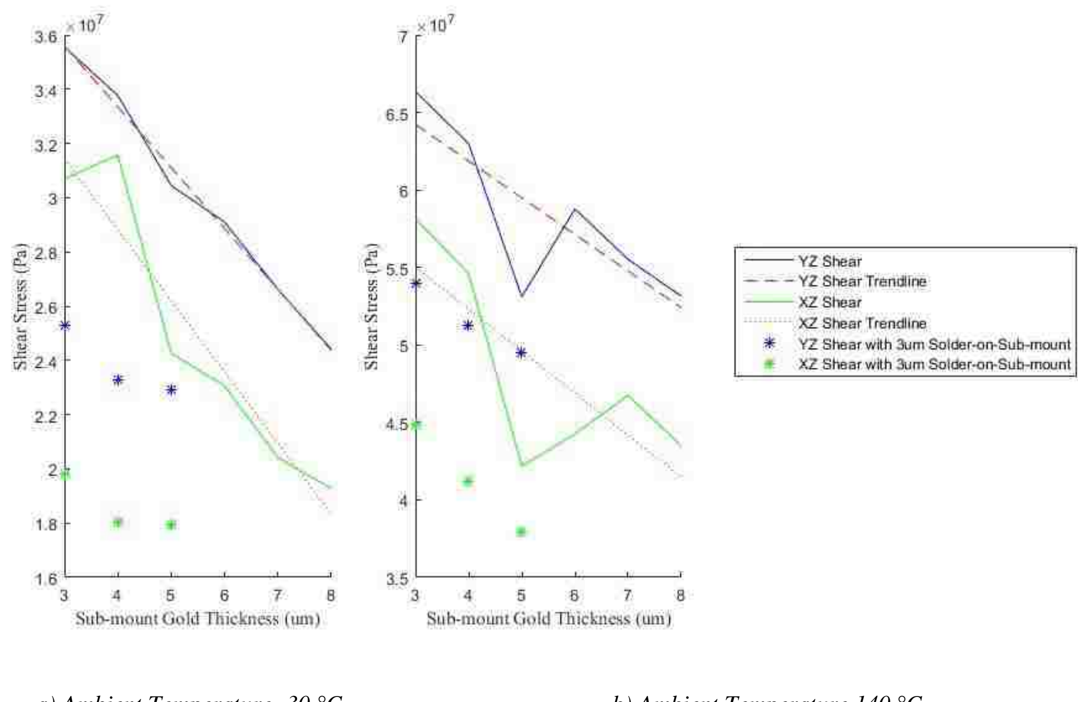
c) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 4.11 – Maximum von Mises Operational Stress vs Sub-mount Gold Thickness



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

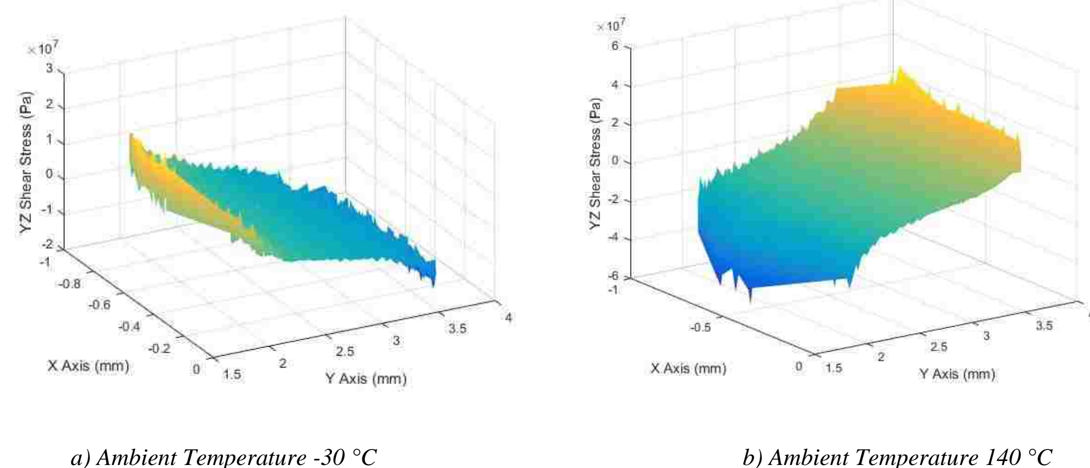
Figure 4.12 – Average von Mises Operational Stress vs Sub-mount Gold Thickness



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

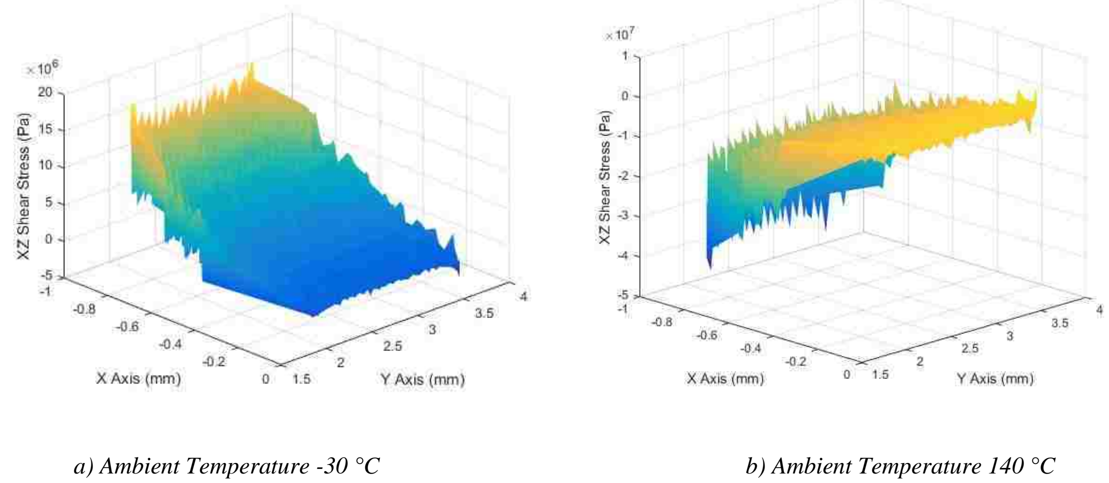
Figure 4.13 – Max Operational Shear Stress Au(80)Sn(20) Solder vs Sub-mount Gold Thickness

Shear stress within the solder interconnect joints is seen to be reduced as sub-mount gold is increased. At both temperature extremes, the shear stress is seen to remain well below the benchmark failure level of approximately 275 MPa. Additionally, no plastic yielding is predicted to occur as the shear stress values remain below 217 MPa. This is true for both temperature extremes. These maximum shear stresses are seen to occur in the outer regions as seen in Figure 4.14 and Figure 4.15, similar to the locations of the maximum principal stresses. The solder on sub-mount design configuration is shown to significantly reduce both stress within the AlGaAs mesa structures, and the shear stress in the Au(80)Sn(20) eutectic solder interconnects.



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 4.14 - Operational Max YZ Shear Stress in Solder, Sub-mount Au Thickness 8um



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 4.15 – Operational Max XZ Shear Stress in Solder, Sub-mount Au Thickness 8um

At -30 °C, the shear stress is in tension while at 140 °C they are in compression within the solder interconnects. For cold ambient temperature, the CTE mismatch between package components causes a concave deformation in the AlN and GaAs/AlGaAs die, and hot temperatures result in convex deformation as illustrated in Figure 4.16.

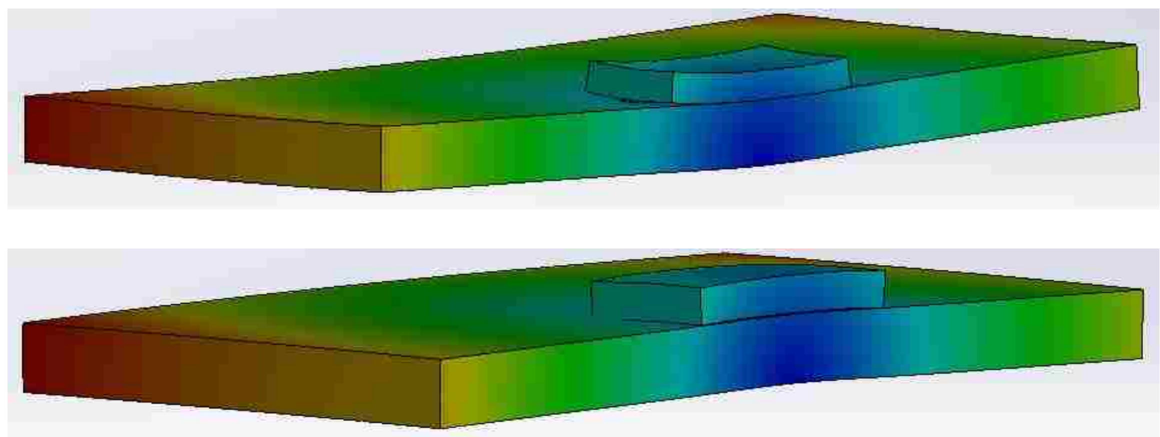


Figure 4.16 – Package deformation for -30°C Ambient (top), and 140°C Ambient (bottom)[5]

The lateral shear stresses (YZ) occur predominantly in the solder interfaces at the top and bottom of the VCSEL array (+/- Y Axis), and focused toward the outer edges (- X Axis). Similarly, the longitudinal shear stresses (XZ) are larger in the outer solder interfaces.

4.6 Conclusion

For the temperature extremes of -30 and 140 °C, the GaAs and AlGaAs components of the laser array remain in the brittle regime (T≤400°C). It was shown that the maximum principal stress at these extremes and across various packaging designs would not exceed the benchmark 2.7 GPa, indicating the VCSEL die components would not reach a stress level that would induce brittle fracture. The maximum principal stresses, as well occur in outer AlGaAs mesa structures, indicating the resulting maximum stress from package deformation occurs away from the light emitting mesas. Additionally, the potential for shear failure in the solder interconnects is not of concern for this packaging configuration at the temperature extremes of interest. Plastic yielding is as well seen to remain below the benchmark of 217 MPa for the solder connections.

[5] Deformation graphs exaggerated for shape clarification

The addition of thicker gold on the sub-mount is shown to marginally influence the stresses in the GaAs and AlGaAs components under CW operational heating. Table 4-2 describes the resulting changes in stress per micron of additional sub-mount gold.

Table 4-2 – Percent Stress Change Results

Analysis Component	Temperature Extreme	Solder on Sub-mount Thickness (μm)	Average % Change in Stress per 1 μm Sub-mount Gold	
			AlGaAs Component	
Max von Mises	-30	0	-2.62 %	
		3	-50.10 %	
	140	0	-2.47 %	
		3	-44.48 %	
Average von Mises	-30	0	-0.50 %	
		3	-32.98 %	
	140	0	-0.13 %	
		3	-33.34 %	
Maximum 1st Principal	-30	0	-0.5 %	
		3	-5.41 %	
	140	0	0.08 %	
		3	0.06 %	
Maximum 2nd Principal	-30	0	0.67 %	
		3	-1.26 %	
	140	0	1.46 %	
		3	-8.78 %	
Maximum 3rd Principal	-30	0	0.4 %	
		3	14.11 %	
	140	0	0.16 %	
		3	-10.34 %	
			YZ Shear	XZ Shear
Max Shear Stress	-30	0	-5.23 %	-6.19 %
		3	-28.22 %	-34.82 %
	140	0	-3.32 %	-4.20 %
		3	-14.65 %	-19.13 %

Table 4-2 describes the stress reduction in the AlGaAs, as the largest maximum stresses occur in this component within the package.

For a VCSEL array die bonded to an isotropic sub-mount, it was shown that increasing the sub-mount gold has minimal influence, and does not significantly help reduce the resulting stress in the AlGaAs component where the largest are seen to occur. It does, however, provide benefit to reducing the shear stress in the solder interconnects. An approximate 5 % reduction in shear stress is seen to occur per additional micron of sub-mount gold. The utilization of a solder on sub-mount packaging approach reduces both the principal stresses in the components as well as the shear stress in the solder interconnects. The addition of this elastic layer is most influential at lower temperatures, preventing tensile deformation as the package deforms. It is, therefore, advantageous to adopt a solder on sub-mount packaging approach while increasing the sub-mount gold, if economically feasible.

5 Alternative Sub-mount Packaging Analysis

5.1 Motivation

Thermal management of VCSEL packaging is critical to the performance and reliability of these devices. One method to improve the efficiency of this dissipation away from the die is the inclusion of copper through vias into the sub-mount. In addition to thermal considerations, alternative electrical connective methods can be employed with this packaging design. Common methods to achieve electric connectivity in semiconductor packaging involves wire bonding or leadless chip carrier solutions. These provide a means by which a die on substrate assembly can be interfaced to circuit boards or other packaging, but still include the thermal resistance of a sub-mount.

By including through vias directly in the sub-mount, multiple processing steps can be eliminated in the manufacturing and assembly of the device otherwise involved with wire bonding. In addition to being able to solder the sub-mount directly to electronic components rather than through an additional packaging interface, this approach provides a better thermal conduit to dispense heat away from the VCSEL device. Thus, it is of interest to quantify the thermal and mechanical outcome of including copper through vias directly into the sub-mount design.

5.2 Model Development

The overall dimensions of the substrate remain the same as the Chapter 4 analysis, and can be found in Appendix A.1. A 5 x 5 grid of copper through vias is centered in the

AlN sub-mount, with diameters of 0.4 mm and pitch of 0.4 mm. The symmetric half model can be visualized below in Figure 5.1. The copper material properties are included in

.

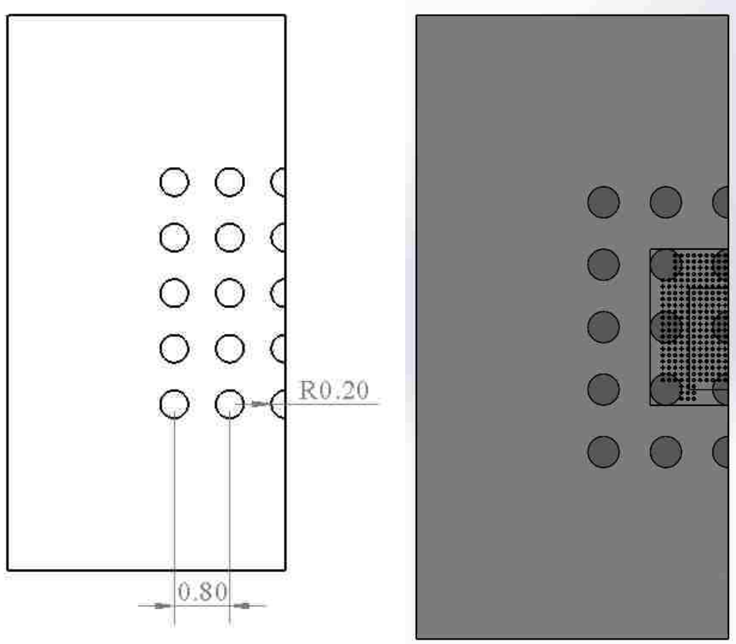


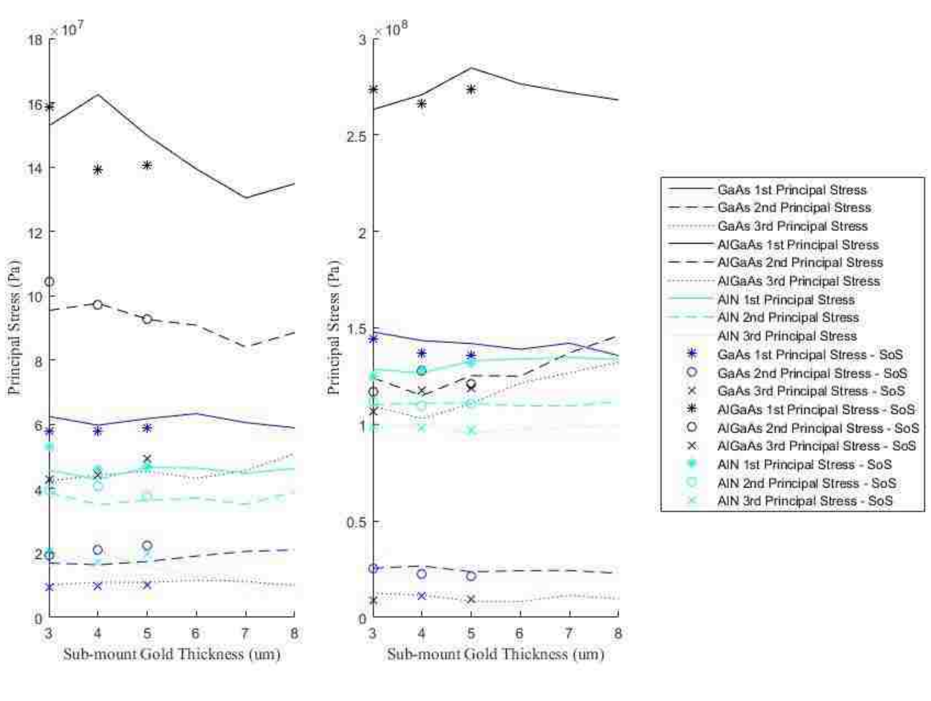
Figure 5.1 – Copper Through Via Sub-mount Design

5.3 Simulation Development

Similar to the simulation development in Chapter 4, the ambient temperature extremes are prescribed to the bottom of the sub-mount. This simulates the assumption that the heatsink typically used in a VCSEL assembly is at the ambient temperature. Total internal heat generation of 1.6 W is set at the interface of the n-mirror and p-mirror AlGaAs structure of the 150 active mesas, as was previously illustrated in Figure 4.1.

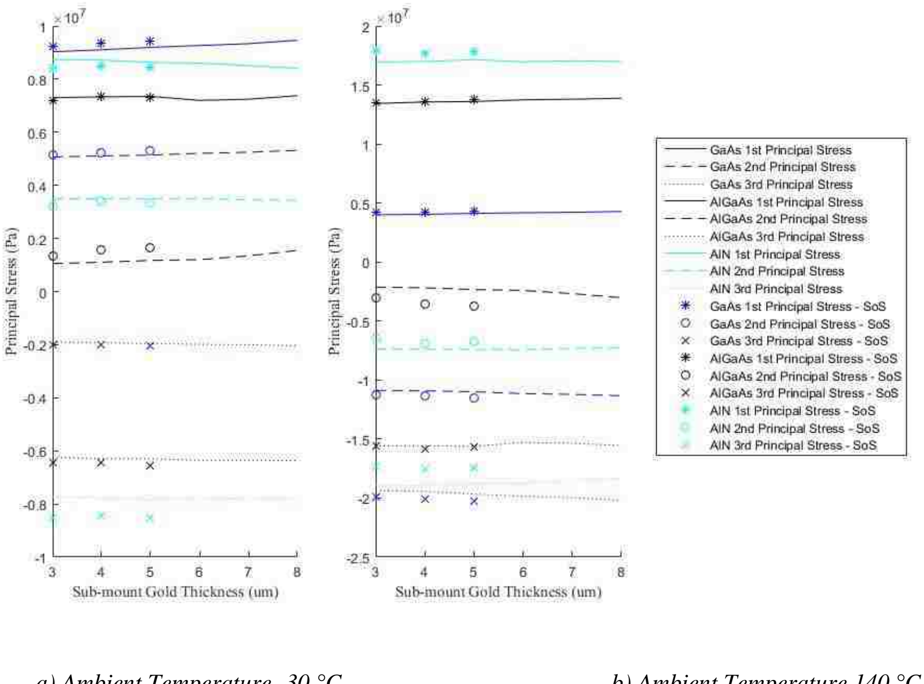
5.4 Results and Discussion

The results of the principal stresses in the assembly components for the die on sub-mount packaging assembly utilizing copper through vias follow closely to the design without vias. The maximum principal stress again occurs in the AlGaAs component. At both temperature extremes, the maximum stress does not exceed 2.7 GPa for the VCSEL device components. This can be seen below in Figure 5.2.



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

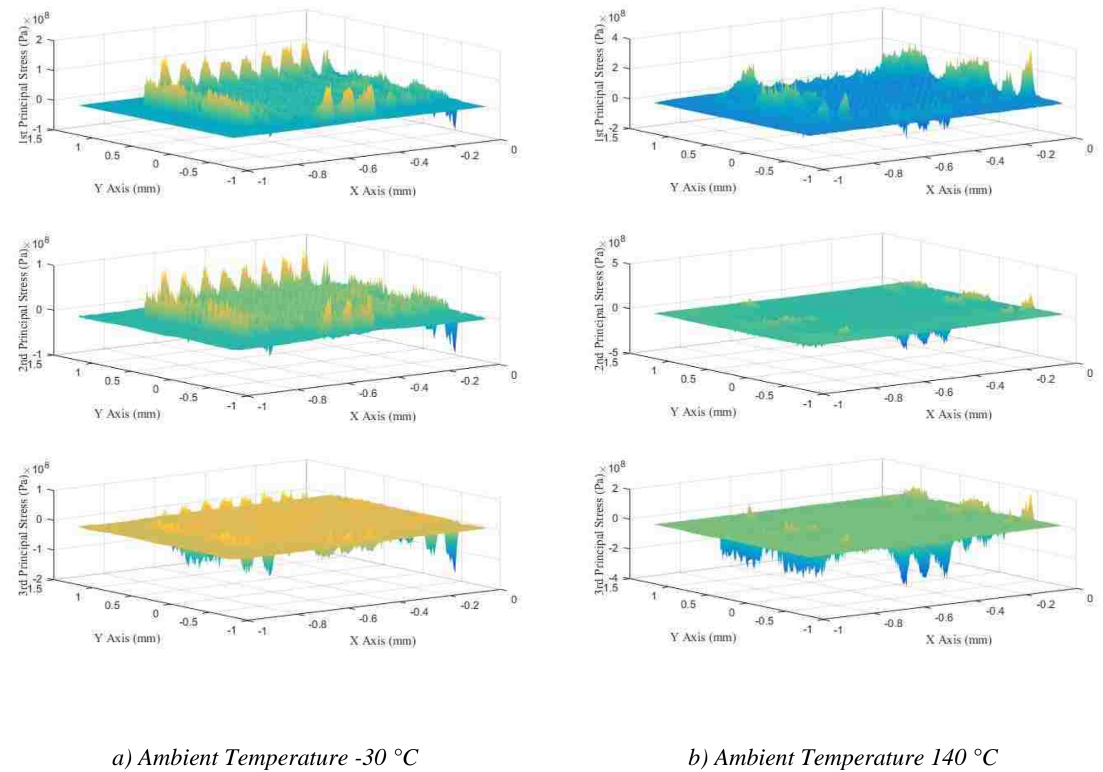
Figure 5.2 – Maximum Operational Principal Stress vs Sub-mount Gold (Sub-mount Via Design)



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

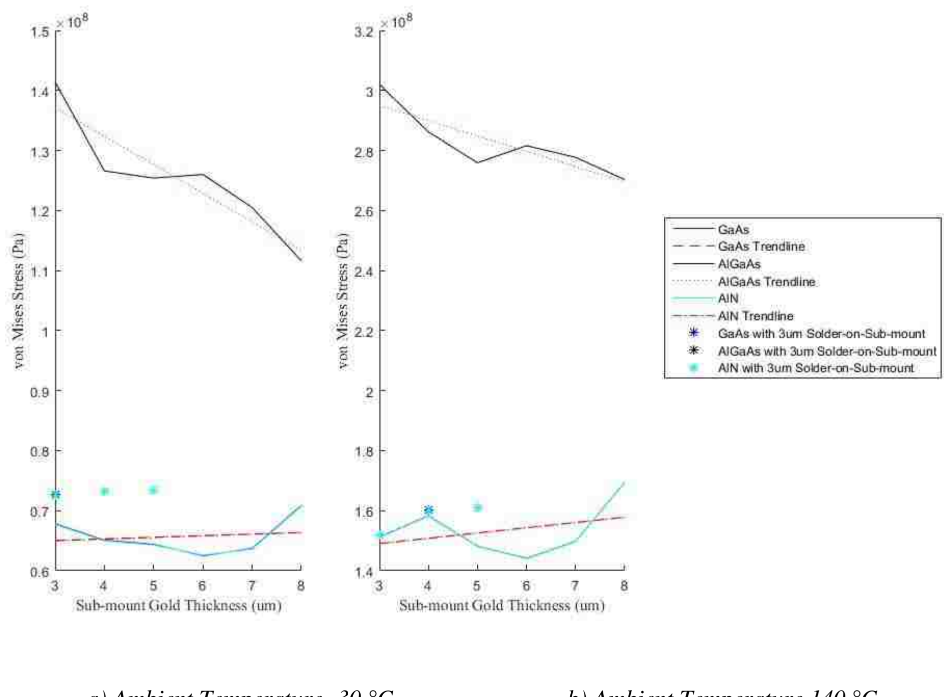
Figure 5.3 – Average Operational Principal Stress vs Sub-mount Gold (Sub-mount Via Design)

The average principal stresses are higher than for the packaging design without through vias in the sub-mount. The largest maximum principal stress occurs in the AlGaAs structure, and remains below the fracture level of 2.7 GPa. A visualization of the corresponding locations for these maximum principal stresses can be seen below in Figure 5.4 for the AlGaAs component.



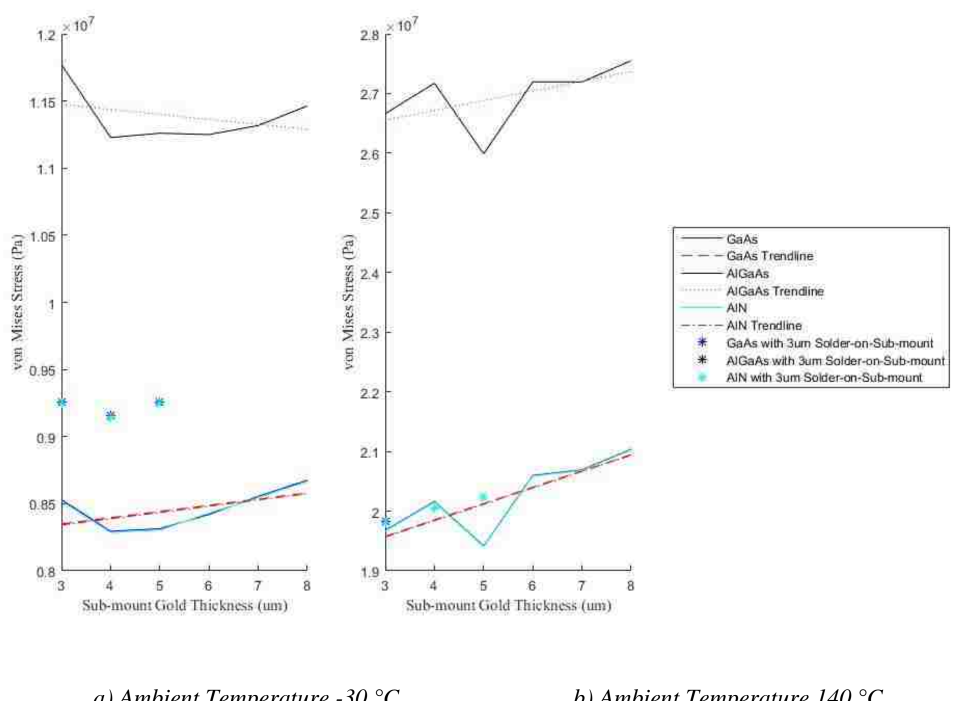
a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 5.4 – AlGaAs Principal Stresses, Sub-mount Au Thickness 5um, Solder on Sub-mount (Sub-mount Via Design)



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

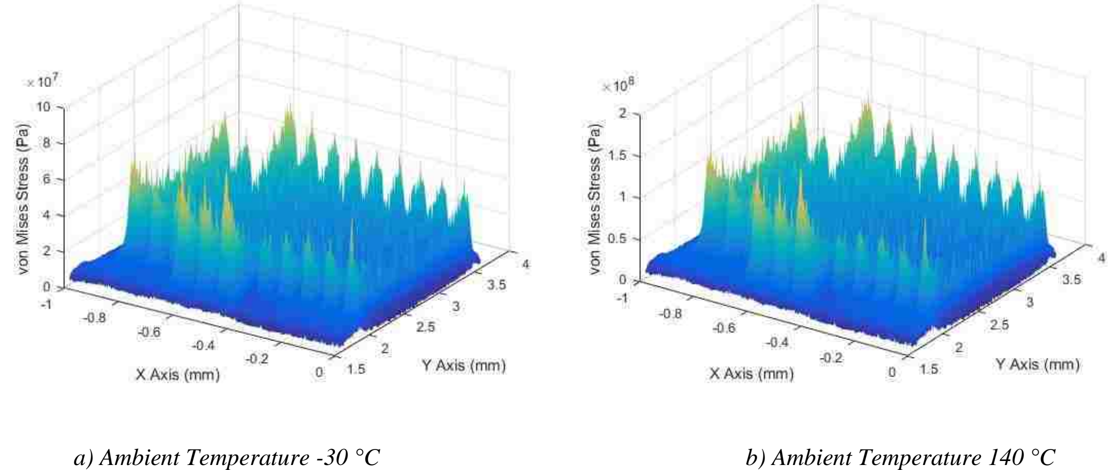
Figure 5.5 – Maximum von Mises Operational Stress vs Sub-mount Gold Thickness (Through Via Sub-mount)



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 5.6 –Average von Mises Operational Stress vs Sub-mount Gold Thickness (Through Via Sub-mount)

These maximum principal stresses occur in the outer AlGaAs mesas, similar to the results in the previous chapter. This can be visualized below in Figure 5.7. It should be noted that stress within the sub-mount increases significantly due to the inclusion of the copper material with a much larger CTE than AlN.

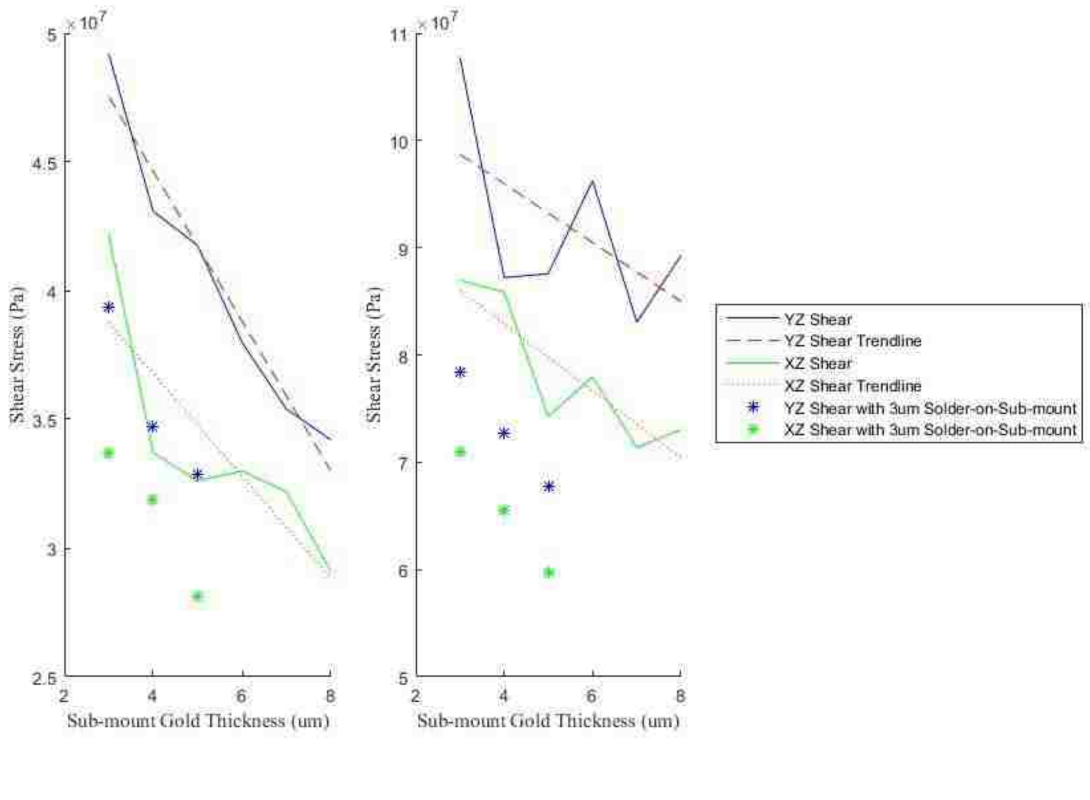


a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 5.7 – Operational von Mises Stress in AlGaAs Components, Sub-mount Au Thickness 8um (Through Via Sub-mount)

The addition of sub-mount gold is seen to have minimal influence on reducing the average principal stresses occuring in the package. As for an isotropic sub-mount, the maximum principal stress can be seen to be reduced with the increase in sub-mount gold. Employing a solder on sub-mount packaging approach as well is seen to reduce the maximum principal stress in the VCSEL device. This is especially evident at the lower temperature extreme, where the solder prevents concave deformation.

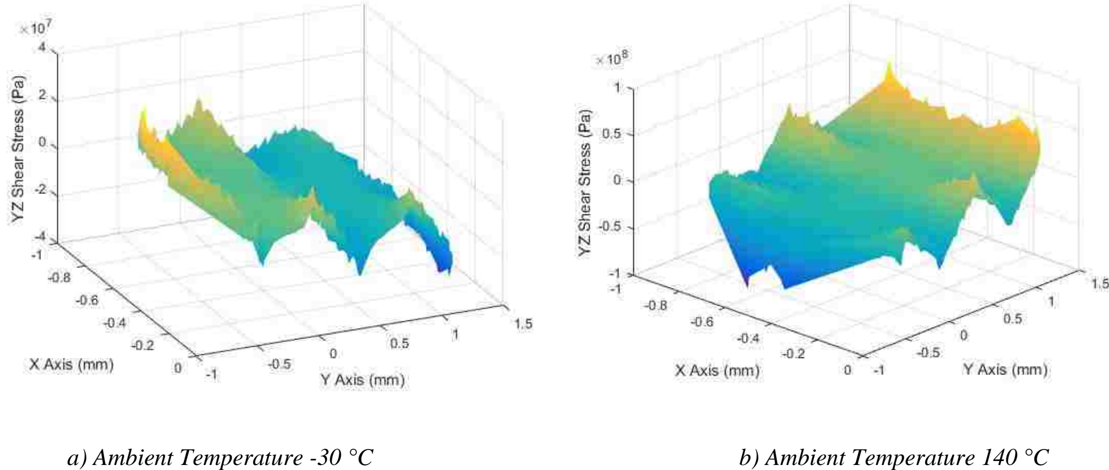
Figure 5.8 below describes the YZ and XZ shear stresses at the temperature extremes.



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

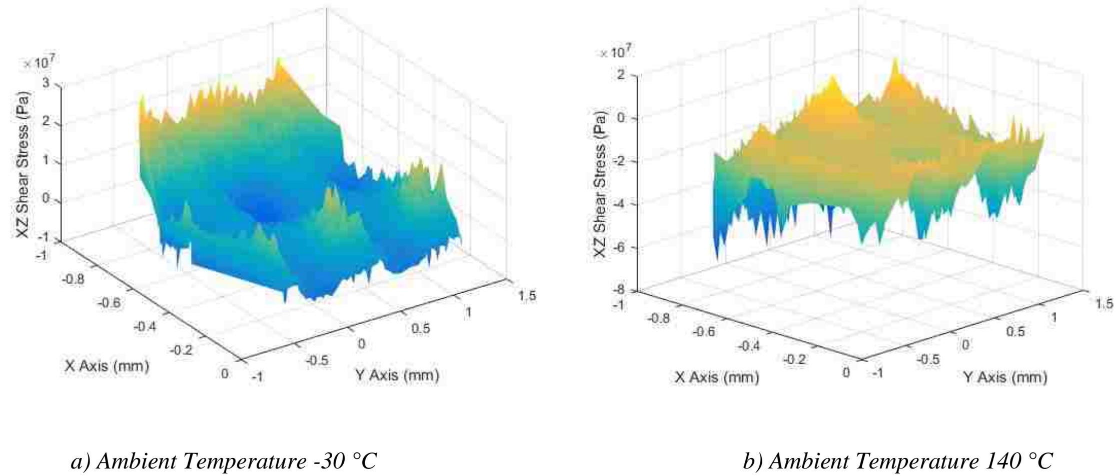
Figure 5.8 – Max Operational Shear Stress Au(80)Sn(20) Solder vs Sub-mount Gold Thickness (Through Via Sub-mount)

At both temperature extremes, shear failure is seen to not occur as the maximum values within the solder interconnects remain below 275 MPa. Additionally, these values do not exceed the benchmark for plastic yielding of 217 MPa. The shear stresses can be visualized below in Figure 5.9 and Figure 5.10 for the solder interconnect components at the temperature extremes.



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 5.9 – Operational YZ Shear Stress in Solder, Sub-mount Au Thickness 8um (Through Via Sub-mount)



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 5.10 – Operational XZ Shear Stress in Solder, Sub-mount Au Thickness 8um (Through Via Sub-mount)

Shear stress for the solder interconnects corresponding to the light emitting VCSEL mesas is found to be more pronounced than for an isotropic sub-mount.

Increasing the sub-mount gold is seen to be advantageous to reducing shear stress. Additionally, a solder on sub-mount assembly approach further reduces these stresses. It can be seen that for the -30 °C temperature extreme, the outer longitudinal solder interconnections (+/- Y direction) are in tension. At the 140 °C extreme, the outer latitudinal solder interconnects (+/- X direction) are in compression.

The inclusion of copper through vias aids in drawing heat away from the device. Because VCSEL functionality is temperature dependent, under normal operating conditions the temperature rise in the device would be less than simulated. This would, in turn, reduce the stresses occurring within the VCSEL device to less than those simulated.

5.5 Conclusion

The inclusion of copper through vias in the AlN sub-mount was shown to increase the principal stresses in the VCSEL package components more than without vias. It was seen that the maximum principal stress occurred in the AlGaAs component, specifically in the outer mesa structures. This stress location is consistent with the previous findings for an isotropic sub-mount. The maximum principal stresses at both temperatures remained below the fracture level of 2.7 GPa. Additionally, the shear stresses were found to remain below the shear failure level of 275 MPa for both temperature extremes, and remain below the benchmark of 217 MPa for plastic yielding. As in the previous chapter, the locations of these maximum shear stresses occur in the solder connections corresponding to inactive VCSEL mesas.

While this packaging configuration was shown to increase the maximum and average principal stresses in the VCSEL components as well as the maximum shear stress in the solder connections relative to the isotropic sub-mount design, the addition of sub-mount gold and solder on sub-mount approach were seen to assist in the reduction of these stresses.

Table 5-1 describes the average change in stress per micron of sub-mount gold for the temperature extremes, and for different solder on sub-mount configurations.

Table 5-1 – Percent Stress Change Results, Solder on Sub-mount

Analysis Component	Temperature Extreme	Solder on Sub-mount Thickness (µm)	Average % Change in Stress per 1 µm Sub-mount Gold	
			AlGaAs Components	
Max von Mises	-30	0	-3.51 %	
		3	-44.09 %	
	140	0	-1.75 %	
		3	-45.16 %	
Average von Mises	-30	0	-0.44 %	
		3	-19.29 %	
	140	0	0.56 %	
		3	-24.70 %	
Maximum 1st Principal	-30	0	0.45 %	
		3	-2.82 %	
	140	0	-0.06 %	
		3	-0.25 %	
Maximum 2nd Principal	-30	0	0.27 %	
		3	1.49 %	
	140	0	-0.05 %	
		3	0.26 %	
Maximum 3rd Principal	-30	0	-0.58 %	
		3	1.59 %	
	140	0	-0.59 %	
		3	3.11 %	
			YZ Shear	XZ Shear
Max Shear Stress	-30	0	-5.08 %	-5.17 %
		3	-20.24 %	-13.08 %
	140	0	-2.85 %	-2.67 %
		3	-22.15 %	-20.57 %

While these percentage reductions are significant, this packaging assembly is shown to be less advantageous than using a sub-mount without through vias under these simulation parameters. They do indicate the addition of sub-mount gold and adoption of a solder on sub-mount packaging approach to be advantageous to reducing stress in the package.

6 VCSEL Die and PCB Analysis

6.1 Motivation

Currently, the packaging process for flip-chip bonding VCSEL array devices onto an intermediate sub-mount requires extra processing steps and can be costly both in terms of time and material. One scalable alternative to using an intermediate material in electronic packaging applications is directly interfacing to a PCB. Integrating optical interconnects at the PCB level have advantages over electrical interconnects such as increased bandwidth, lower power consumption, and minimization of electromagnetic interference effects. This concept has been explored in previous works by Happel *et al*. and Cho *et al*., among others [30] [31].

For purposes of resource efficiency and reliability, packaging alternatives to current die on substrate designs will be examined to explore feasibility of integrating VCSEL array devices directly to PCB electronics. Three PCB boards will be simulated to understand the optimum design for effective VCSEL performance.

6.2 Model Development

The VCSEL array geometry is kept consistent with previous simulations with the addition of a 40x40 mm FR4 PCB. The corresponding dimensioned assembly drawing can be seen in Appendix A.2. The PCB is assumed to be a four-layer board of varying properties. Design 1 does not include through-hole vias, Design 2 includes plated through-hole vias, and Design 3 includes copper filled through-hole vias. These can be seen in Appendix A.3. The FR4 material properties for the PCB board are described in

.

The sub-mount gold is kept constant at 5 um in thickness, and the packaging design utilizing solder deposited on the VCSEL mesas is used as previously illustrated in Figure 3.5. It is necessary to keep these variables constant in an effort to isolate the results of a VCSEL device bonded to a PCB.

6.3 Simulation Development

A nonlinear analysis using the prescribed heat generation of 1.6W at the AlGaAs DBR mirror interface of the active 150 elements, similar to Chapters 4 and 5, is performed for the two temperature extremes and PCB designs. The outer corners of the PCB are fixed and the ambient temperature is prescribed to the outer edges.

The mesh properties are outlined in Table 6-1.

Table 6-1 – VCSEL PCB Simulation Mesh Properties

	Nodes	Elements
PCB Design 1	42455	174991
PCB Design 2	52579	225406
PCB Design 3	54993	241194

The temperature profiles in devices bonded to PCB boards would vary from simulated results as the internal heat generated by the device is temperature dependent and would vary from the 1.6W used. However, for the purposes of comparison, the prescribed internal heating taken from empirical data at 90 °C is used as a constant for steady state analysis, as it was in the previous chapters.

6.4 Results

For the nonlinear analysis, the heat can be seen to be most effectively dissipated through the PCB board Design 3, with copper filled through vias. The figures below illustrate the temperature profiles in the assembly for the three designs, as well as the resulting heat flux through the bottom copper pad on the PCB's.

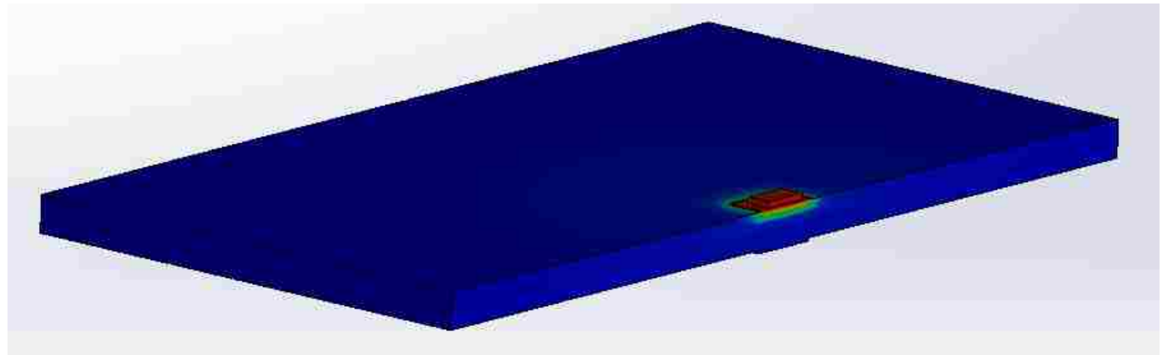


Figure 6.1 – Temperature Profile PCB Design 1

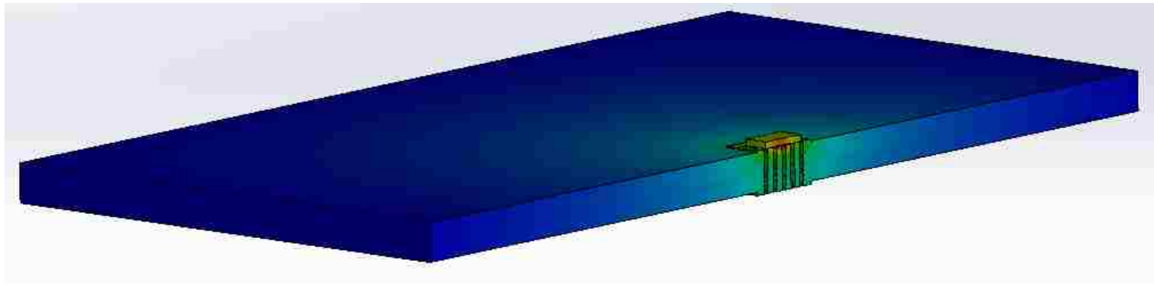


Figure 6.2 – Temperature Profile PCB Design 2

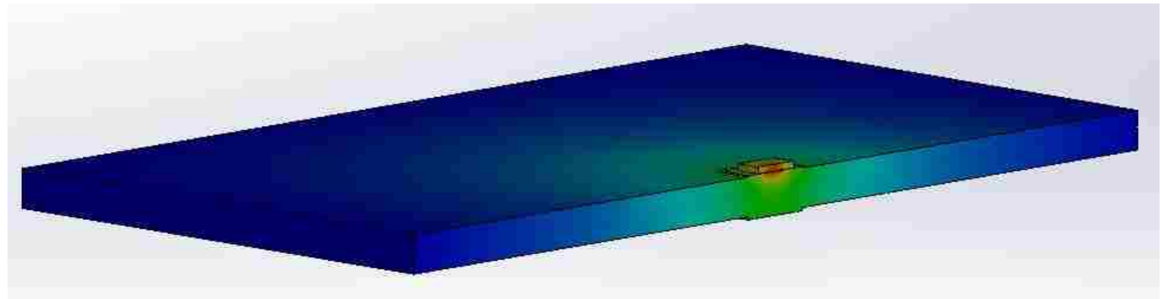


Figure 6.3 – Temperature Profile PCB Design 3

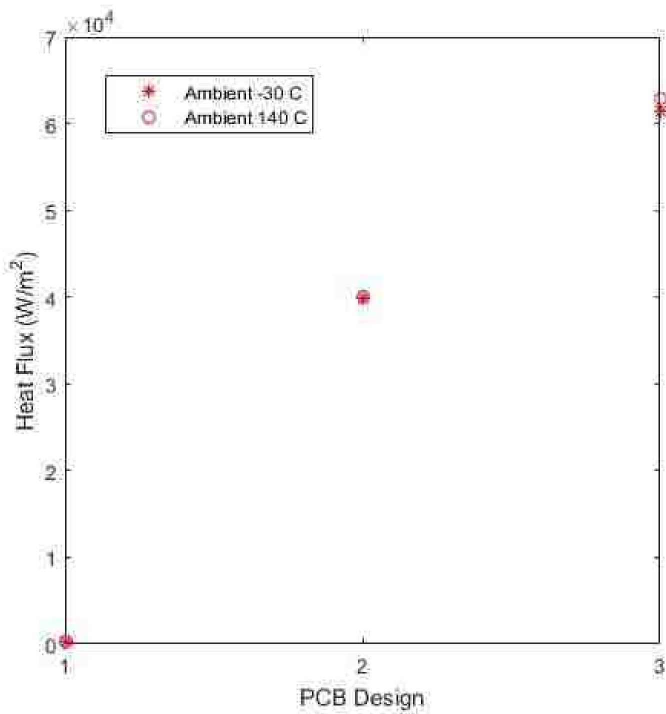
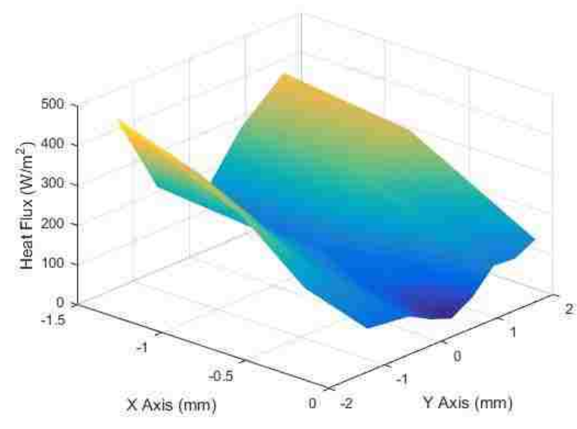
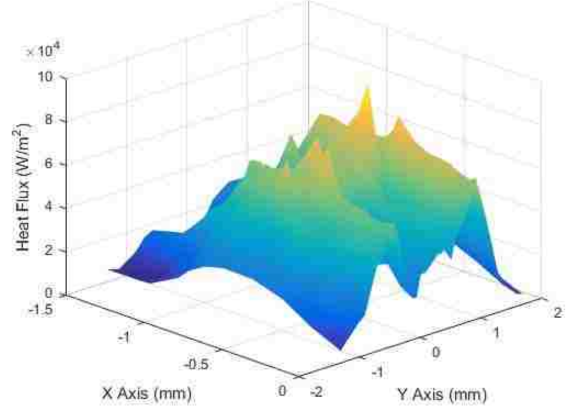


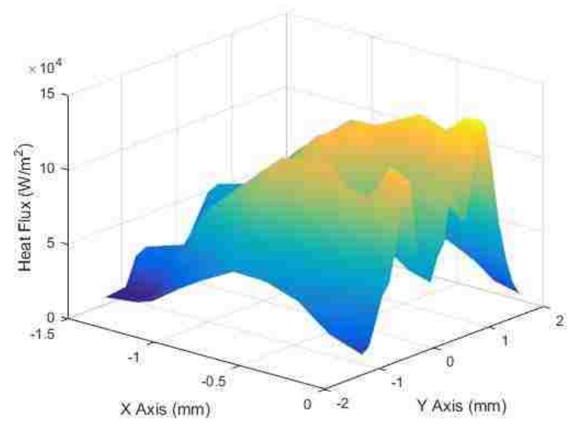
Figure 6.4 – Heat Flux Through Bottom of PCB



a) Heat Flux PCB Design 1



b) Heat Flux PCB Design 2

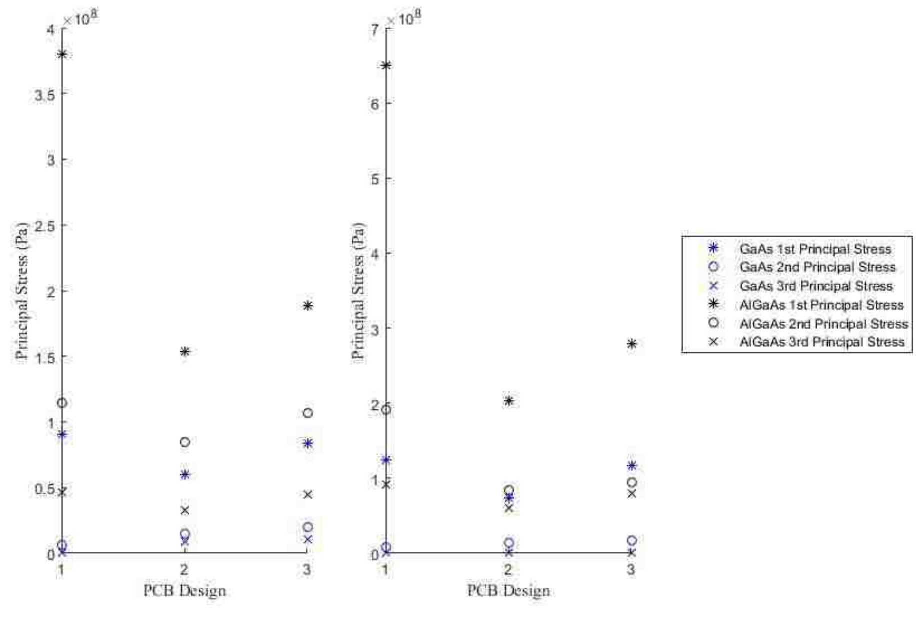


c) Heat Flux PCB Design 3

Figure 6.5 – Heat Flux Profiles Through Bottom of PCB

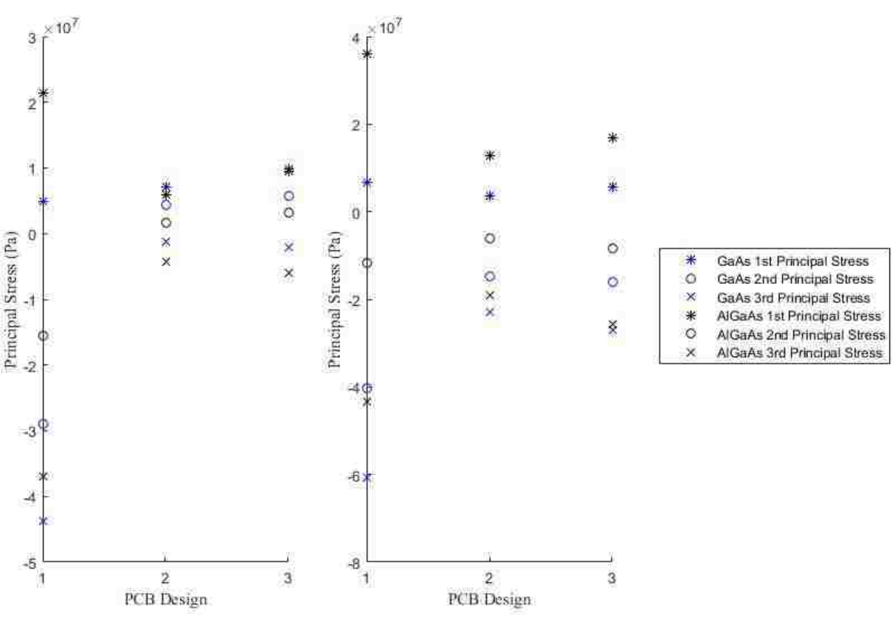
It can be observed that PCB Design 3 provides the best resulting heat flux through the bottom of the PCB copper pad and away from the VCSEL device as seen in Figure 6.4 and Figure 6.5. This is essential for thermal management if this packaging configuration is to be considered. The heat flux through the pad is indicative of the heat directed into a heatsink. PCB Designs 2 and 3 result in a heat flux approximately two orders of magnitude greater than Design 1.

Below, the resultant maximum and average principal stresses can be seen for the varying PCB designs.



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

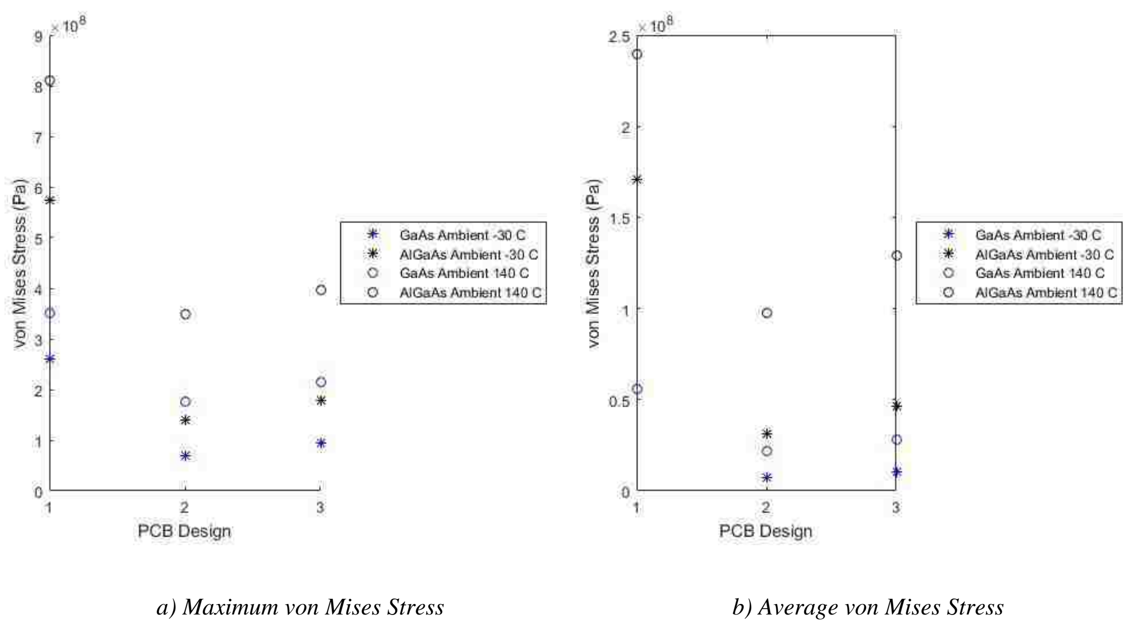
Figure 6.6 – Maximum Principal Stress for Varying PCB Designs



a) Ambient Temperature -30 °C *b) Ambient Temperature 140 °C*

Figure 6.7 – Average Principal Stress for Varying PCB Designs

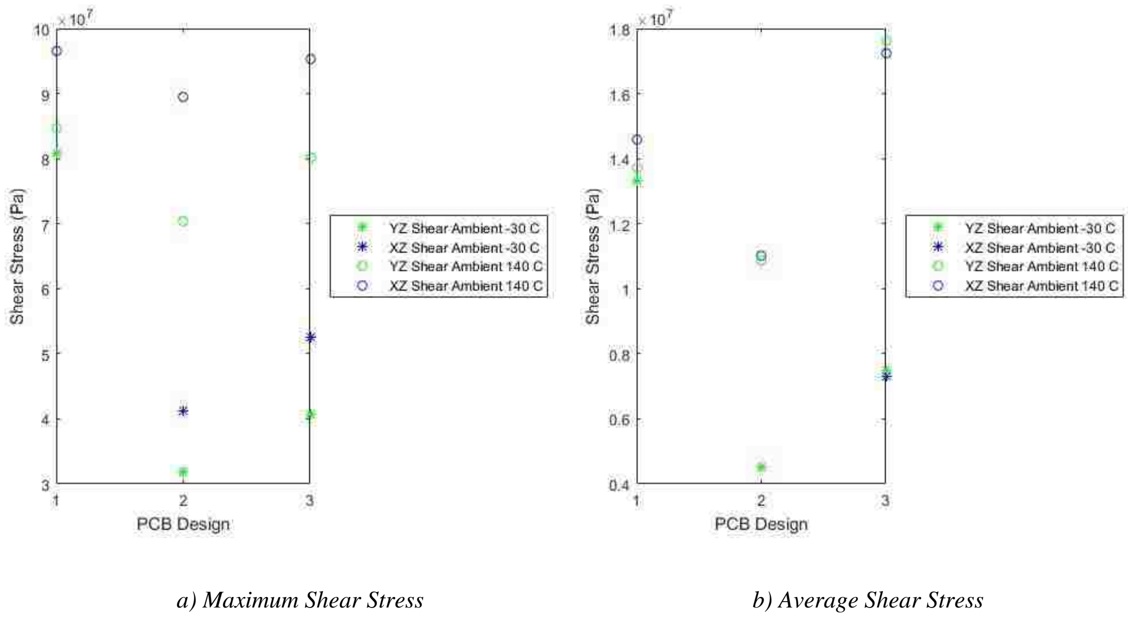
The maximum principal stresses occurring in the laser components at the temperature extremes all fall below the fracture level for the varying PCB designs. The largest maximum principal stresses occur using PCB Design 1, while Design 2 is seen to induce the lowest in the VCSEL device. This can, as well, be seen in the von Mises stress in Figure 6.8.



a) Maximum von Mises Stress *b) Average von Mises Stress*

Figure 6.8 – von Mises Stress for Varying PCB Designs

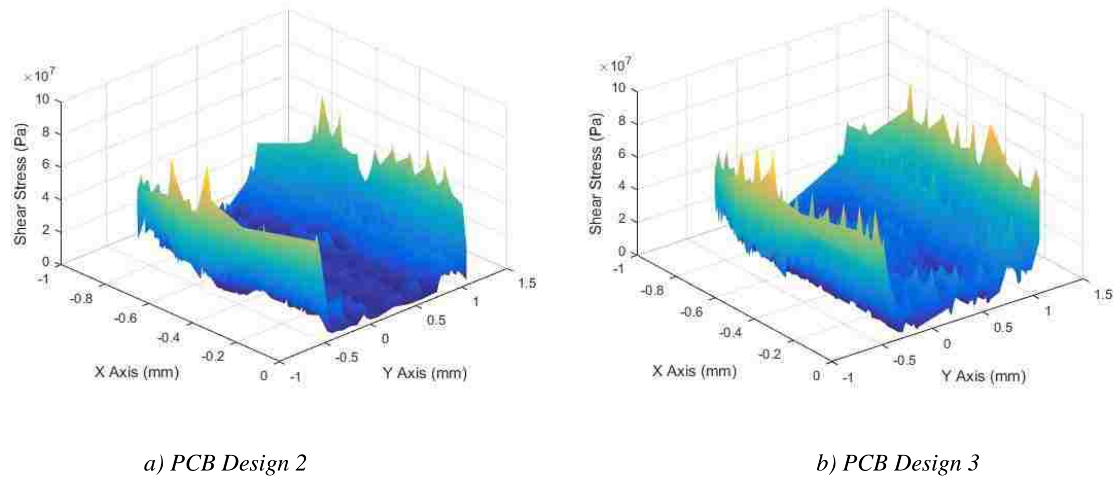
The shear stresses in the solder interconnections do not exceed failure level of 275 MPa for both temperature extremes for any of the three PCB designs. These results are described below in Figure 6.9. This shows that when implementing a VCSEL device bonded directly to a PCB, neither shear failure nor plastic deformation will occur in the solder connections.



a) Maximum Shear Stress *b) Average Shear Stress*

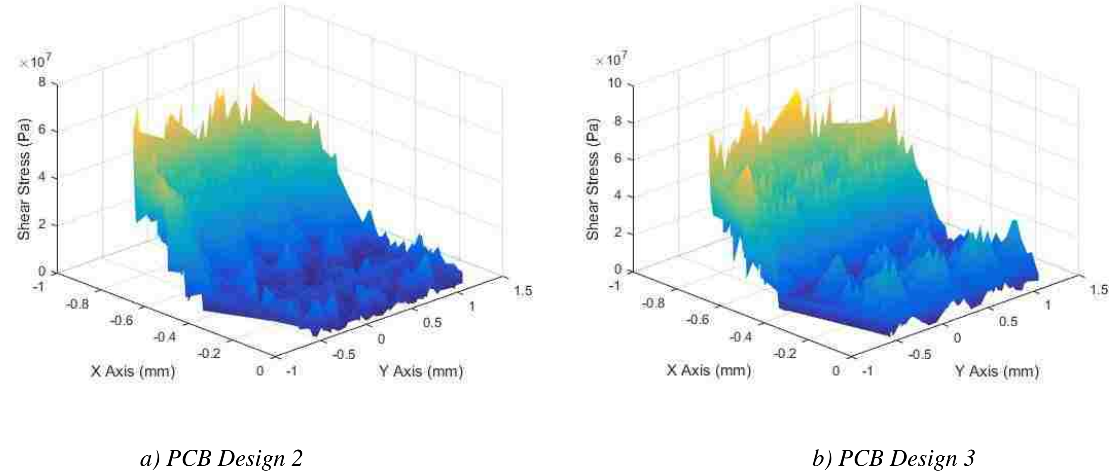
Figure 6.9 – Solder Connection Shear Stress for Varying PCB Designs

The location of the maximum induced shear stresses can be visualized below in Figure 6.10 and Figure 6.11 for the solder connections for PCB Designs 2 and 3. Not only are the largest shear stresses near the edges more uniform, the stresses in the connections corresponding to the active VCSEL mesas are greater.



a) PCB Design 2 *b) PCB Design 3*

Figure 6.10 – YZ Shear Stress in AlGaAs Component at 140 °C



a) PCB Design 2 *b) PCB Design 3*

Figure 6.11 – XZ Shear Stress in AlGaAs Component at 140 °C

6.5 Conclusion

In examining three PCB designs, it was found that the VCSEL device with an internal heat generation of 1.6 W would not be susceptible to fracturing as the stresses induced from CTE mismatch within the package remain below the fracture strength of 2.7 GPa. These maximum principal stresses are, however, significantly larger than the die on sub-mount packaging configurations. PCB Design 1 was found to produce the largest stresses, while PCB Design 2 was found to be the optimum of the three designs. At both ambient temperature extremes, the maximum shear stress, seen to occur in the outer solder connections, remain below the benchmark for shear failure. Plastic deformation as well would not take place in the solder connections for any of the three designs.

The packaging alternative of a VCSEL die directly bonded to a PCB is shown to have considerable potential as package deformation is seen to not cause damage within the VCSEL die or solder interconnections. Of the three designs, PCB Design 2 was found to produce the best results for this potential packaging configuration.

7 Cost Benefit Analysis of VCSEL Packaging Options

7.1 Motivation

In addition to mechanical and thermal tradeoffs in packaging design, cost plays a significant role for VCSEL devices in a commercial setting. As manufacturing is scaled up for VCSEL devices, the cost per device becomes a critical aspect in design considerations. These costs directly affect the scalability and profitability of producing these devices. A balance is needed between finding effective packaging configurations that reduce costs and performance/reliability of the devices. An overview of associated costs for these different packaging alternatives will be analyzed to understand the feasibility as related to large scale manufacturing efforts of these devices. In addition, this analysis will examine potentially advantageous avenues for further research efforts to improve costs without sacrificing performance.

7.2 Methodology

Initial costs at the wafer level are used to set a baseline, and are based on current manufacturing estimates and vendor quotes[6]. These costs are based on processing methods at the wafer level as is the industry standard. Semiconductor wafers can be processed in a variety of sizes ranging from 1-inch to 11.5-inches in diameter. It is assumed for the purposes of this study that a 4-inch wafer is used, although larger wafer sizes will increase

[6] Initial baseline costs courtesy of Tom Wilcox and TriLumina Corp© manufacturing data.

the number of devices per wafer, and thus reduce the cost per device. A wafer of this size can be seen below in Figure 7.1.

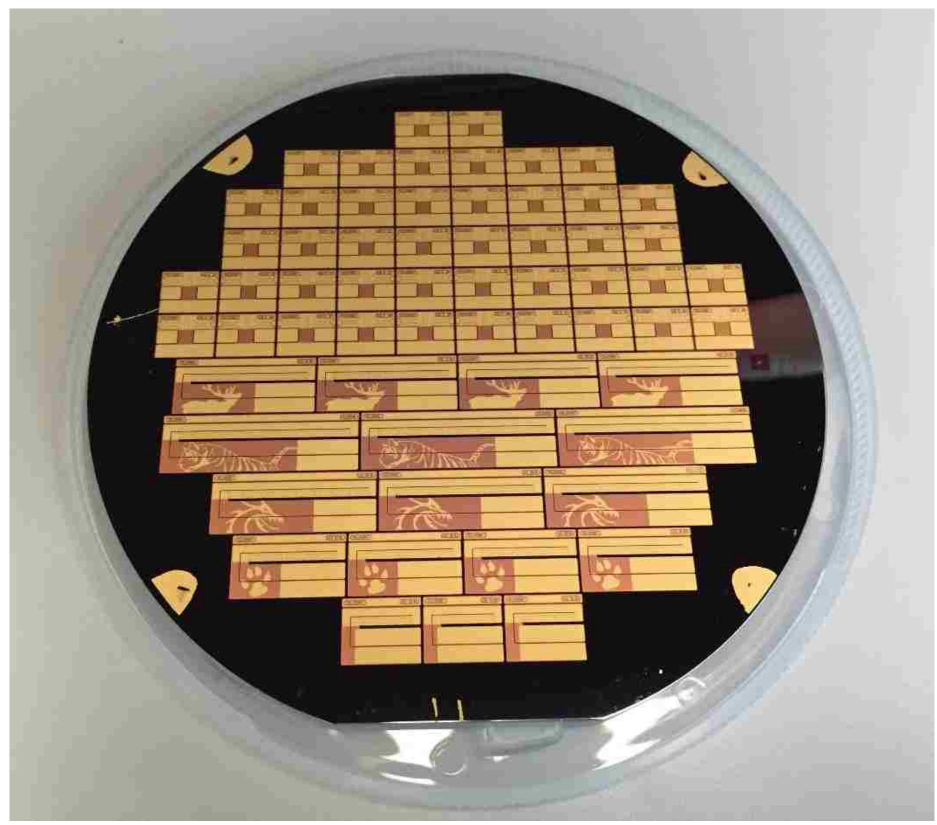


Figure 7.1 – 4 Inch Sub-mount Wafer (Varying Sized Sub-mounts)

It is initially estimated that 1412 individual VCSEL devices can fit on one wafer, and 117 sub-mounts can be produced from one wafer. This estimate is for the same VCSEL die and sub-mount size used in this work.

7.3 Cost / Benefit Analysis

For increasing additional gold on the sub-mount, an approximate price of $260.00 per wafer is used for 4 um in thickness. While additional costs and processes are involved

in plating the sub-mounts, it is assumed the greatest cost factor is the electroplated sub-mount gold amount used. Per wafer, at the current manufacturing processing rate used in obtaining these cost values, the addition of an extra micron of gold would cost $65.00. This results in an approximate cost increase of $0.56 per device for a reduction in stress. Table 7-1 shows the cost benefit tradeoff for die on sub-mount packaging configurations.

Table 7-1 – Cost Benefit Table, Additional Sub-mount Gold

Cost	Benefit				
	Reduction in Max Stress for AlGaAs Component	Reduction in Average Stress for AlGaAs Component	Reduction in Maximum Principal Stress for AlGaAs Component	Reduction in YZ Shear Stress	Reduction in XZ Shear Stress
$0.56 per μm	Isotropic Sub-mount				
	2.59 %	0.13 %	0.21 %	4.28 %	5.2 %
	Sub-mount with Through Vias				
	2.63 %	0.06 %	-0.19%	3.97 %	3.92 %

While scaling up operations and reducing device footprint size will reduce this per-device cost, the current packaging configuration shows a significant increase in cost for minimal mechanical stress improvements.

The cost and processing methods to deposit solder on either the VCSEL wafer or the sub-mount wafer is identical. Therefore, the solder on sub-mount packaging approach can produce significant stress reduction in the package for no additional cost. Mechanical benefits to stress reduction in the 30, 40, and 50% range with no additional packaging costs is advantageous for overall device performance and reliability. Table 7-2 provides an overall view of the benefits from switching to a solder on sub-mount packaging approach.

Table 7-2 – Cost Benefit Table, Solder on Sub-mount

Cost	Benefit				
	Reduction in Max Stress for AlGaAs Component	Reduction in Average Stress for AlGaAs Component	Reduction in Maximum Principal Stress for AlGaAs Component	Reduction in YZ Shear Stress	Reduction in XZ Shear Stress
$0.00	Isotropic Sub-mount				
	47.29 %	33.16 %	2.7 %	21.44 %	26.98 %
	Sub-mount with Through Vias				
	44.63 %	21.9 %	1.54 %	21.2 %	16.83 %

The benefit of adopting a packaging approach using PCB's effectively eliminates costs associated with building sub-mounts. While this approach was seen to be of some benefit in regard to lower stress within the components and shear stress, the potential to fully eliminate an intermediate sub-mount for the overall package of these VCSEL devices drastically reduces costs. This warrants further development of VCSEL on PCB packaging options.

7.4 Conclusion

The mechanical stress reduction can be seen to occur through the increase in sub-mount gold, or adopting a solder on sub-mount packaging approach provided an overall packaging benefit through mitigating void or crack propagation, inducing brittle fracture within the VCSEL die material, and reducing shear stress in the solder interconnect joints. However, these packaging improvements must still be economically feasible when viewed from a scalable operating perspective. It was found that using current manufacturing techniques and prices for gold deposition and solder deposition, that marginal mechanical benefit can be accomplished for $0.56 a device per um of extra gold on the sub-mounts.

This is a significant rise in per unit cost, especially for large operations where cost reduction is critical. Adding sub-mount gold was found to provide a reduction of approximately 4.74 % (isotropic sub-mount) and 3.95 % (sub-mount with through vias) to the shear stresses in the solder interconnect joints.

Utilizing a solder on sub-mount approach was seen to provide significant reductions in shear stress for no additional costs. As solder deposition methods and costs do not vary between which wafer is used (VCSEL wafer or sub-mount), simply altering the deposition process is seen to provide an approximately 24.21 % reduction in maximum stress within an isotropic sub-mount and 19.02 % for a sub-mount with through vias.

8 Conclusions and Recommendations

In this work, the residual stress was first quantified for the flip chip bonding process used to package the VCSEL device to a sub-mount. The mechanical results of internal device heating from CW operation was analyzed for two die on substrate assemblies. The first being a simple gold plated isotropic sub-mount, and the second a substrate with copper through vias. Additionally, a packaging configuration involving the VCSEL die directly mounted to a four-layer PCB board was analyzed for practicality under CW operation. Packaging parameters such as increasing the sub-mount gold thickness and adding a full solder layer to the sub-mount were varied to examine their effect on the operational stress in the VCSEL die components and solder connection interfaces. For each study -30 °C and 140 °C were used for the ambient temperature conditions. These are consistent with industry qualification standards for semiconductor devices.

The residual stress for a VCSEL array after flip-chip bonding to a sub-mount was analyzed in Chapter 3. It was found that the highest residual von Mises stresses were concentrated in the AlGaAs DBR component, specifically the outer mesa structures of the array. The highest residual stress within the package occurred with the smallest height of gold on the sub-mount, approximately 4.6e8 Pa within the outer AlGaAs mesa structures. As the sub-mount gold thickness was increased, the residual stress in the AlGaAs DBR components and AlN sub-mount decreased. Utilizing a solder on sub-mount deposition method in which extra solder covers the gold is shown to reduce the package deformation from CTE mismatch and lower the residual stress from die bonding.

Stress induced from CW operation of a VCSEL die bonded to an isotropic sub-mount is examined in Chapter 4. The maximum principal stresses at the temperature extremes of concern were found to remain below the fracture benchmark of 2.7 GPa within the VCSEL device. At both temperatures, the shear stress within the solder interconnects was found to remain below the failure level of 275 MPa. The addition of sub-mount gold was found to result in minimal changes to the maximum principal stresses within the VCSEL device, and approximately 5% reduction in shear stress within the solder interconnects. Adopting

a solder on sub-mount packaging approach was shown to have a minimal effect in reducing the average principal stresses in the VCSEL components, but did aid in reducing the maximum principal stress, especially at the lower temperature extreme. Solder on sub-mount had significant influence on the sear stress in the solder interconnects. This reduction was found to be approximately 26% in the YZ plane and 27% in the XZ plane.

The inclusion of copper through vias in the sub-mount were shown to increase the maximum principal stresses in the package components more so than an isotropic sub-mount design. As with the isotropic sub-mount, the largest principal stresses were seen to occur in the outer mesa structures of the array. This packaging configuration resulted in the maximum principal stresses remaining below the fracture strength of 2.7 GPa at the temperature extremes. Additionally, the shear stress in the solder interconnections remained below the shear failure level of 275 MPa at the temperature extremes, although larger than those induced with an isotropic sub-mount. Increasing the sub-mount gold was found to marginally help in reducing the average principal stresses, but aided in reducing the maximum principal stress in the VCSEL device slightly. Additional sub-mount gold was found to reduce the maximum shear stress in the solder interconnections by approximately 5%. The adoption of a solder on sub-mount packaging approach was found to be beneficial in reducing both the maximum principal stress in the VCSEL device and the shear stress in the solder connections. The benefit of this approach is most evident in the shear stress, for which a reduction of approximately 20% and 16% were found for the YZ and XZ shears, respectfully.

In examining three types of PCB designs in Chapter 6, it was found that using a PCB with plated through vias is most advantageous for lower stress within the VCSEL components. As with previous sub-mount designs, the location of the maximum principal stresses was seen to occur in the outer AlGaAs mesas. The plated through-hole PCB design would be best if considering applications with VCSEL on PCB, but further optimization to reduce stress in the die and solder connections would be required. This design minimizes the contact to the copper, which has a CTE significantly larger than the semiconductor material. A potential alternative to copper would be solder to fill the vias, in an effort to

more closely match CTE's. The VCSEL device bonded directly to a PCB shows potential for further investigation into this packaging option.

Across these studies of varying packaging options for VCSEL's, it has been shown that increasing the sub-mount gold is advantageous in reducing residual manufacturing stress and CW operational stress within the VCSEL die. The increase in gold was seen to provide a more significant reduction in shear stress for the solder interconnects. Utilizing a solder on sub-mount approach provides the greatest reduction in stress by introducing an additional elastic layer to the overall package and providing additional support to the protruding mesa structures and solder connections. Especially at lower temperatures, the solder around the side of the mesas hinders concave deformation of the package, reducing the stresses in the mesas. From a cost-benefit analysis, the use of a solder on sub-mount approach is most advantageous as no additional cost is associated with it. The addition of thicker sub-mount gold was shown to include a cost increase of approximately $0.56 per micron for current device designs.

It was found that increasing the sub-mount gold was marginally effective in reducing the stress within the VCSEL device, and was observed to have a significant impact in reducing the shear stress in the solder connections. The addition of the thicker gold added a more robust ductile layer that surrounded both the mesa and the solder. As the thickness was increased, the more this layer could plastically yield and absorb the stress in the solder. The AlGaAs mesas were already surrounded by a fair amount of gold, and thus the benefit of additional gold plastically yielding from the sub-mount is marginal. Adopting the solder on sub-mount approach allows an additional elastic layer to surround the mesa structures. This layer acts as a buffer, aiding in providing resistance to the deformation occurring in the package. Because the AlGaAs mesas deform slightly less from the surrounding solder, the stress is reduced within the structure as well as the bonded solder connection. For the varying packaging designs, the PCB's were seen to induce the largest principle and shear stresses. Of the three designs, PCB Design 1 was found to perform the worst. This is due to more significant heat build-up within the VCSEL from the lack of thermal conduits to pull heat away. PCB Design 2 was found to perform better than 3. This can be attributed to the smaller amount of copper in contact with the VCSEL die. The CTE material

properties of the VCSEL die and PCB materials are more poorly matched than for a sub-mount. This drives greater stress within the VCSEL and shear stress within the solder for PCB configurations. The conclusion of CTE mismatch with copper driving greater stresses is consistent for the sub-mount analysis as well. The sub-mount that included copper through vias induced greater principle and shear stresses.

The assumption is made in this work that the DBR mirrors are modeled as solids rather than the many epitaxial layers. Further analysis can be conducted using a higher fidelity model in which the many layers are included in the VCSEL array. This would undoubtedly increase the stress within the VCSEL mesas as work from Martin-Martin *et al*. and Anaya *et al*. show the largest stresses occurring in a single VCSEL mesa modeled with DBR mirror components occur at the interfaces to the active region [22] [27]. The varying CTE properties of the layers would induce further stress in the VCSEL from the thermal loading. However, because the epitaxial layers are lattice matched, the AlGaAs component is a single crystal structure. This gives credit to the assumption of modeling the DBR mirrors as solids.

Through this work, it is recommended that a solder on sub-mount packaging approach be employed to reduce not only residual stress in the VCSEL device from flip chip bonding, but component stress and solder interconnect shear stress as well. Additionally, the use of copper through vias in the sub-mount design is not recommended, as the larger stress within the package could propagate void deformations or micro-cracks. The VCSEL packaging alternative to a sub-mount for a die directly bonded to a PCB was found to be promising. Fracture was not seen to occur within the VCSEL device for any of the designs. A PCB design in which plated through holes are used was seen to be the most advantageous. Because this is a new approach to packaging, it is recommended that further research be conducted to understand the feasibility and reliability of packaging a VCSEL device directly to a PCB.

List of Appendices

Appendix A – Dimensioned Drawings

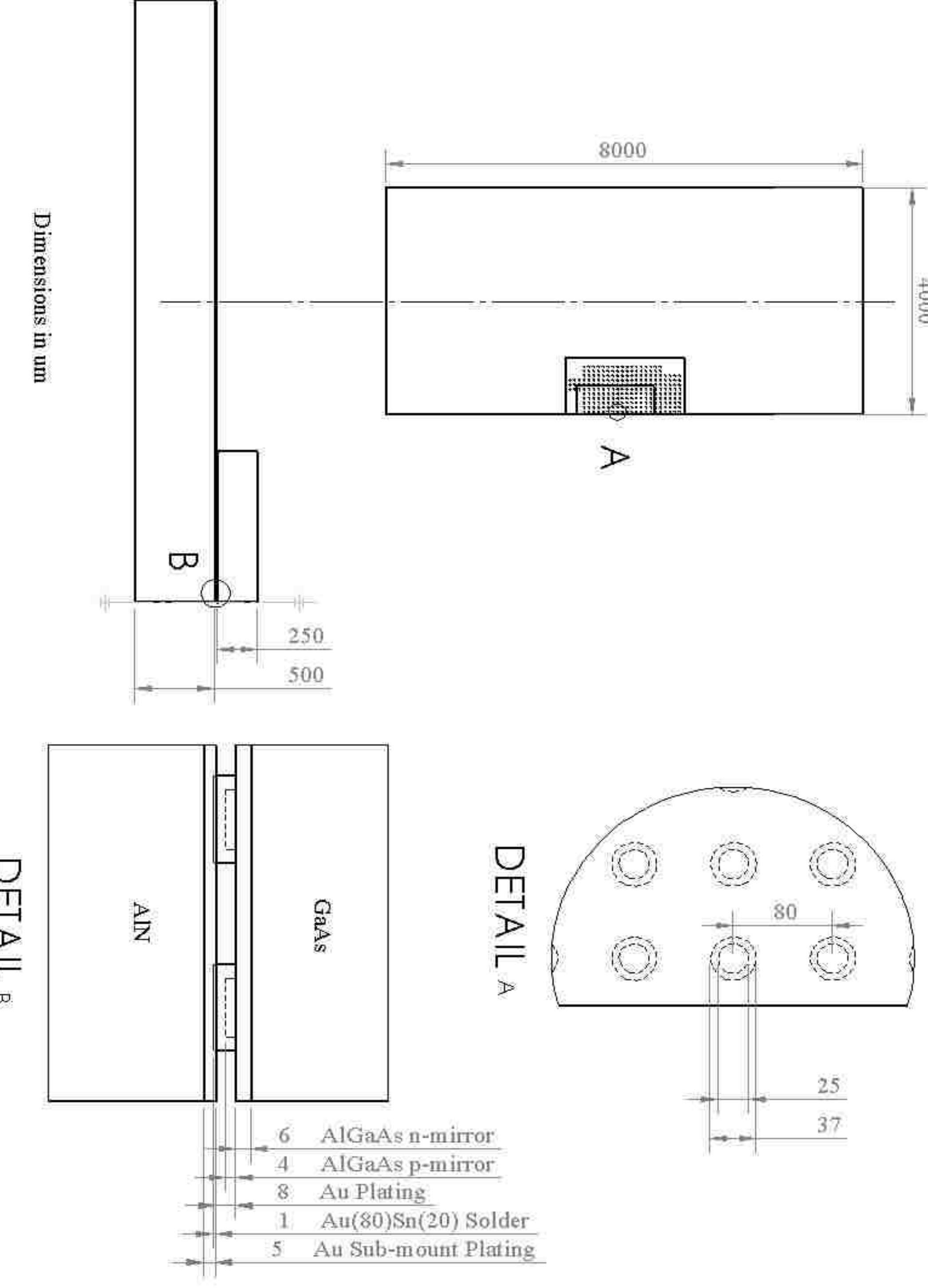
Appendix A.1 – AlN Sub-mount

Appendix A.2 – PCB

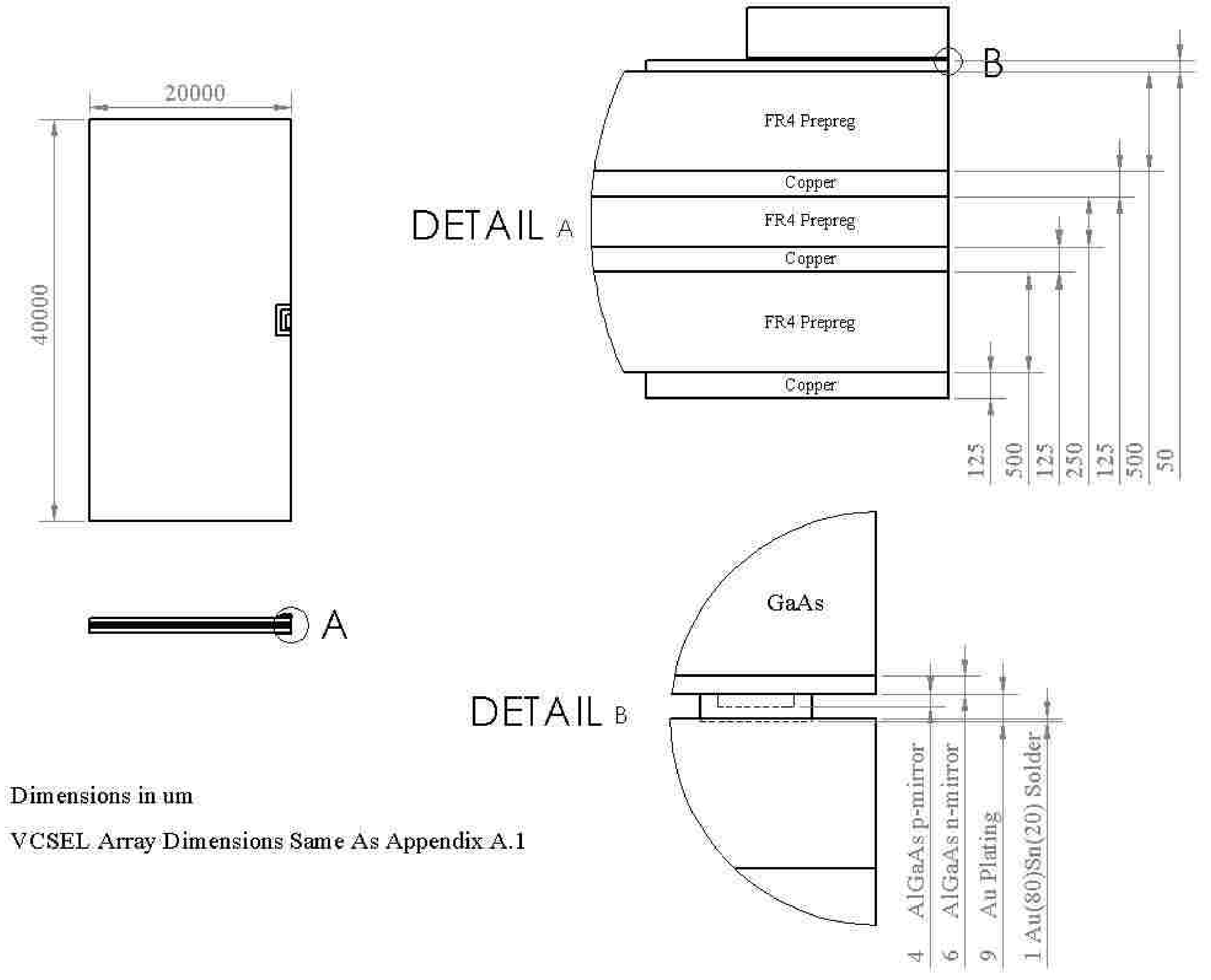
Appendix A.3 – Varying PCB Designs

Appendix B – Finite Element Analysis Theory

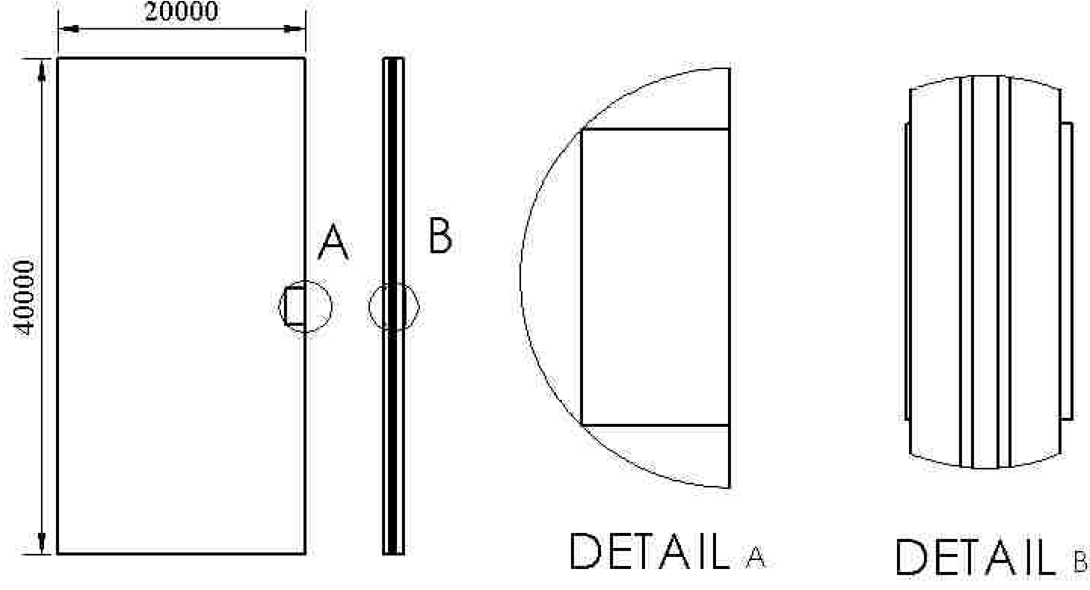
Appendix A.1



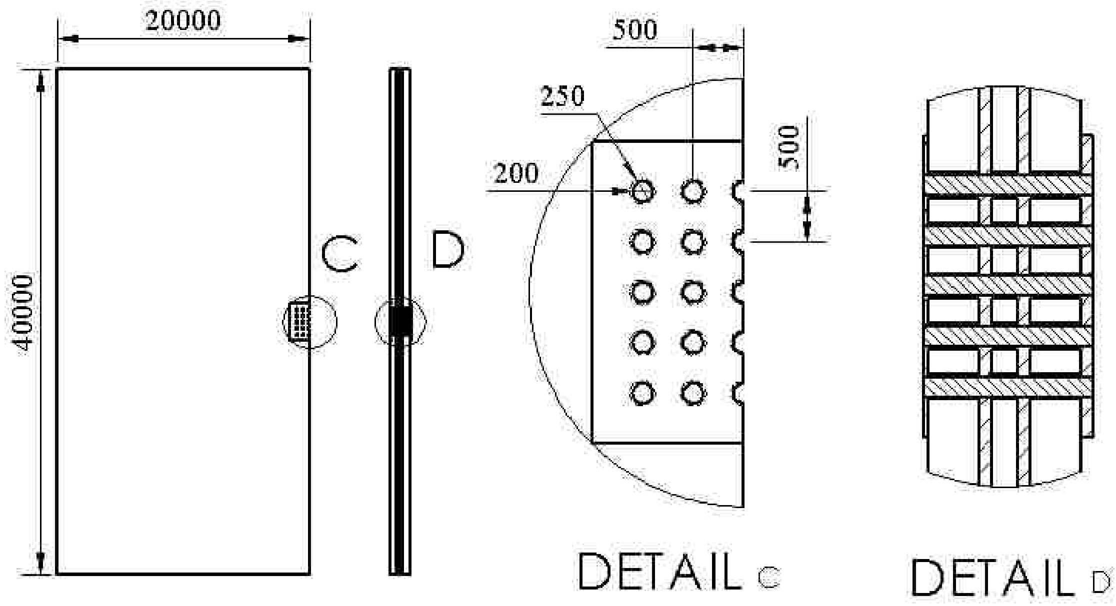
Appendix A.2



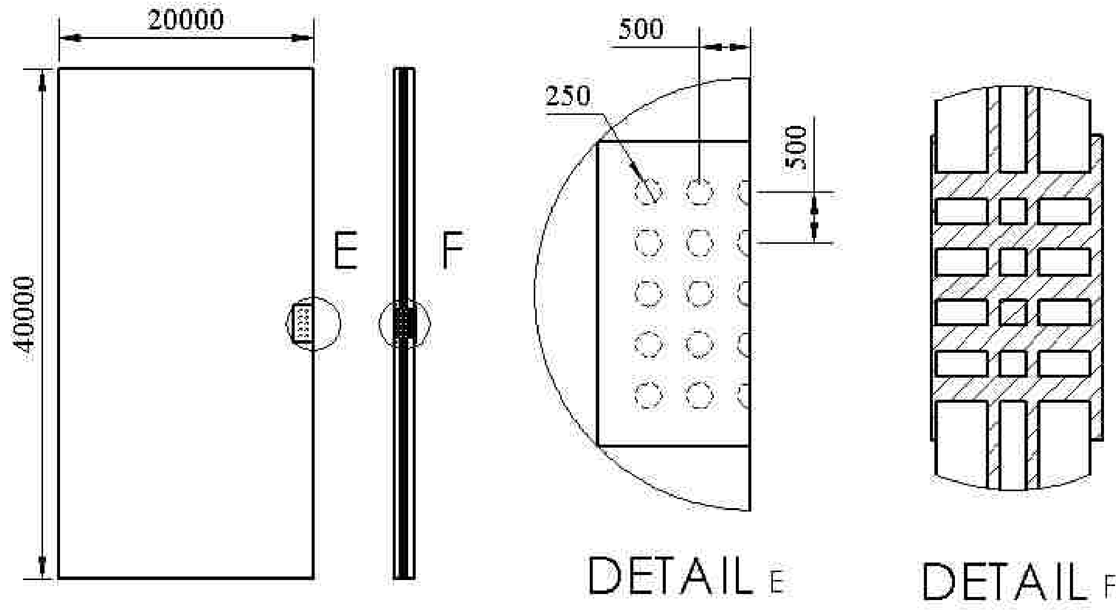
Appendix A.3



PCB Design 1



PCB Design 2



PCB Design 3

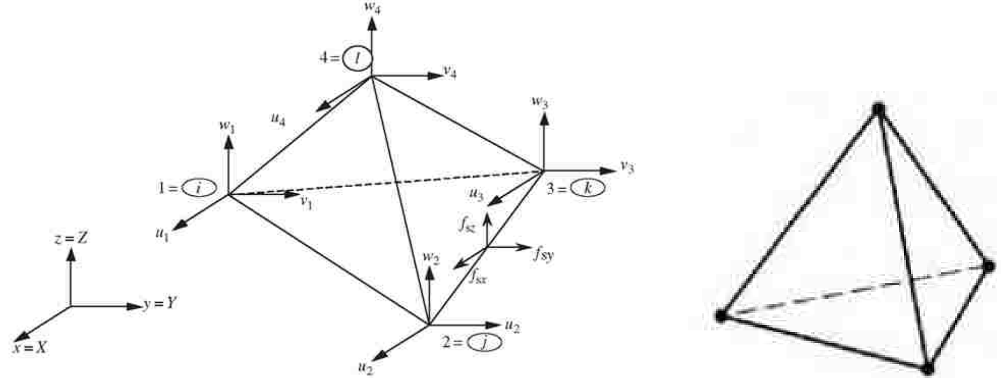
Appendix B

Using finite element analysis to understand displacement reactions in a system due to varying loads involves a number of steps. First, a set of elements connected at nodes must be defined for the geometry. For each of these elements, a stiffness matrix, $K^{(e)}$, and a force vector, $f^{(e)}$, must be computed. These element contributions are then assembled into a global system and can be seen written in the form

$$[K]\{U\} = \{f\}$$

where U is the system displacement vector. The global system is then modified by imposing essential (displacements) boundary constraints. From there, the above equation is solved to find a, the system global displacement vector. Finally, for each element the stresses and strains are computed and evaluated.

The structure defined for the simulations used in Solidworks® are linear tetrahedral solid elements. The figures below show the geometric design of these elements [32].



Each element has four nodes, each with three translational degrees of freedom (designated u,v, and w) giving each element 12 degrees of freedom. The nodes of a tetrahedral element can be designated 1, 2, 3, and 4. The nodal displacement vector can then be described as

$$d_e = \begin{Bmatrix} u_1 \\ v_1 \\ w_1 \\ u_2 \\ v_2 \\ w_2 \\ u_3 \\ v_3 \\ w_3 \\ u_4 \\ v_4 \\ w_4 \end{Bmatrix}$$

The matrix of the shape function can, as well be described as

$$N = \begin{bmatrix} N_1 & 0 & 0 & N_2 & 0 & 0 & N_3 & 0 & 0 & N_4 & 0 & 0 \\ 0 & N_1 & 0 & 0 & N_2 & 0 & 0 & N_3 & 0 & 0 & N_4 & 0 \\ 0 & 0 & N_1 & 0 & 0 & N_2 & 0 & 0 & N_3 & 0 & 0 & N_4 \end{bmatrix}$$

The shape functions are derived from the volumes

$$N_1 = \frac{V_{P234}}{V_{1234}}, \quad N_2 = \frac{V_{P134}}{V_{1234}}, \quad N_3 = \frac{V_{P124}}{V_{1234}}, \quad N_4 = \frac{V_{P123}}{V_{1234}}$$

The Cartesian coordinates can be found using the volume coordinates from

$$x = N_1 x_1 + N_2 x_2 + N_3 x_3 + N_4 x_4$$

$$y = N_1 y_1 + N_2 y_2 + N_3 y_3 + N_4 y_4$$

$$z = N_1 z_1 + N_2 z_2 + N_3 z_3 + N_4 z_4$$

Expressed in matrix form, this equation is

$$\begin{Bmatrix} 1 \\ x \\ y \\ z \end{Bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ x_1 & x_2 & x_3 & x_4 \\ y_1 & y_2 & y_3 & y_4 \\ z_1 & z_2 & z_3 & z_4 \end{bmatrix} \begin{Bmatrix} N_1 \\ N_2 \\ N_3 \\ N_4 \end{Bmatrix}$$

Rearranged, this equation then yields

$$\begin{Bmatrix} N_1 \\ N_2 \\ N_3 \\ N_4 \end{Bmatrix} = \frac{1}{6V} \begin{bmatrix} a_1 & b_1 & c_1 & d_1 \\ a_2 & b_2 & c_2 & d_2 \\ a_3 & b_3 & c_3 & d_3 \\ a_4 & b_4 & c_4 & d_4 \end{bmatrix} \begin{Bmatrix} 1 \\ x \\ y \\ z \end{Bmatrix}$$

where

$$a_i = det\begin{bmatrix} x_j & y_j & z_j \\ x_k & y_k & z_k \\ x_l & y_l & z_l \end{bmatrix}, b_i = -det\begin{bmatrix} 1 & y_j & z_j \\ 1 & y_k & z_k \\ 1 & y_l & z_l \end{bmatrix}, c_i = -det\begin{bmatrix} y_j & 1 & z_j \\ y_k & 1 & z_k \\ y_l & 1 & z_l \end{bmatrix}, d_i = -det\begin{bmatrix} y_j & z_j & 1 \\ y_k & z_k & 1 \\ y_l & z_l & 1 \end{bmatrix}$$

and i varies from 1 to 4, and j,k, and l are determined in a cyclic permutation. Thus, the shape function can be expressed as

$$N_i = \frac{1}{6V}(a_i + b_i x + c_i y + d_i z)$$

After the shape functions are constructed, the strain energy term in local coordinates can be shown as

$$\Pi = \frac{1}{2}\int_{Ve} {d_e}^T B^T cBd_e dV = \frac{1}{2}{d_e}^T\left(\int_{Ve} B^T cBdV\right)d_e$$

which can be simplified to

$$\Pi = \frac{1}{2}{d_e}^T k_e d_e$$

in which B is the strain matrix and k_e is the stiffness matrix. The formulas for these are seen below

$$B = LN = \begin{bmatrix} \frac{\partial}{\partial x} & 0 & 0 \\ 0 & \frac{\partial}{\partial y} & 0 \\ 0 & 0 & \frac{\partial}{\partial z} \\ 0 & \frac{\partial}{\partial z} & \frac{\partial}{\partial y} \\ \frac{\partial}{\partial z} & 0 & \frac{\partial}{\partial x} \\ \frac{\partial}{\partial y} & \frac{\partial}{\partial x} & 0 \end{bmatrix} N$$

$$k_e = \int_{Ve} B^T cBdV$$

The shape function is also used to find the nodal force vector for the element and can be expressed by adding the nodal forces from the body and surface, as seen below.

$$f_e = \int_{Ve} [N]^T f_b dV + \int_{Se} [N]^T f_s dS$$

These equations are then transformed to global Cartesian coordinates above. These fundamental equations are the underlying logic of FEA in Solidworks® used to conduct simulation analyses.

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