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Thermo-Mechanical Reliability and Electrical Performance of Indium Interconnects and Under Bump Metallization

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THERMO-MECHANICAL RELIABILITY AND ELECTRICAL PERFORMANCE OF INDIUM INTERCONNECTS AND UNDER BUMP METALLIZATION

By

Jon-Claude Leger

B.S., Mechanical Engineering, University of New Mexico, 2013

THESIS

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ABSTRACT

This thesis presents reliability analysis of indium interconnects and Under Bump Metallization (UBM) in flip chip devices. Flip chip assemblies with the use of bump interconnections are frequently used, especially in high density, three-dimensional electronic devices. Currently there are many methods for interconnect bumping, all of which require UBM. The UBM is required for interconnection, diffusion resistance and quality electrical contact between substrate and device. Bonded silicon test vehicles were comprised of Indium bumps and three UBM compositions: Ti/Ni/Au (200Å/1000Å/500Å), Ti/Ni (200Å/1000Å), Ni (1000Å). UBM and indium were deposited by evaporation and exposed to unbiased accelerated temperature cycling (-55°C to 125°C, 15°C/min ramp rate). Finite Element Analysis (FEA) simulations were used to gain understanding of non-linear strain behavior of indium interconnects during temperature cycling. Experimental testing coupled with FEA simulations facilitated cycle-to-failure calculations. FEA results show plastic strain concentrations within indium bump below failure limits. It has been demonstrated that fabrication of Ti/Ni/Au, Ti/Ni, and Ni UBM stacks performed reliably within infant mortality failure region.

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CHAPTER 1 Introduction

1.1 Statement of Research

The electronic device industry has become increasingly miniaturized, while still seeking to achieve high performing and high reliability devices. In order to fabricate these advanced electronic assemblies, flip chip interconnections are most commonly used. Within the interconnection bump structure (commonly solder material) is an Under Bump Metallization (UBM). UBM is an intermediate multilayer thin film stack that provides electrical and mechanical connection between interconnect bump and substrate bond pad. UBM is essential for electrical connection path, diffusion barrier and solder wettability between bump and substrate bond pad.

This thesis aims to define, test and evaluate three UBM stacks Ti/Ni/Au(200Å/1000Å/500Å), Ti/Ni(200Å/1000Å) and Ni(1000Å) for use with indium bumped flip chip devices. Test samples are exposed to accelerated temperature cycling (-55°C to 125°C, 15°C/min. ramp rate, 10 minute dwell at extremes) and interconnect quality is evaluated using various electrical and mechanical analysis methodologies. In addition to experimental testing, numerical finite element models are generated in an effort to better understand failure modes and cycle-to-failure estimations.

1.2 Objective of Research

The primary objectives of this research are to quantify UBM and indium interconnects compatibility and to predict early life failures due to accelerated temperature cycling (ATC). Indium interconnects are gaining popularity in multiple high performing application environments, and reliability prediction is not completely understood. Further

understanding of rate-temperature behavior of indium interconnects provides the microelectronics industry with guidance for high-reliability device design.

1.3 Methods of Research

This work investigates three UBM stack compositions within a double-sided silicon based device containing tungsten bond pads and non-reflowed indium interconnection bumps. In order to evaluate indium bump and UBM performance, electrical continuity and resistance measurements are monitored. Electrical performance is quantified by resistance measurements of various 2D and 3D electrical structures within the indium bump array. In addition to the physical test methods described above, Finite Element Analysis (FEA) models were generated to simulate thermo-mechanical response during ATC. Equivalent plastic strain values are also used in Coffin Manson fatigue life calculations to estimate cycle-to-failure.

1.4 Structure of Thesis

This thesis contains six chapters. Chapter 1 introduces research intent and methods for analysis. Chapter 2 is a literature review of topics relevant to this work. Chapter 2 topics include chip to wafer interconnections methods, indium interconnects, UBM principles and reliability research of indium solder joints.

Chapter 3 is a review of thermal testing standards used for device qualification of surface mount bump interconnections. This chapter presents methods and parameters to be considered when exposing electronic devices to accelerated thermal cycling/shock envir`onments. Fatigue models for use in cycle-to-failure predictions are also presented.

Chapter 4 outlines experimental methods for test sample generation. The later portion of this chapter describes experimental processes for electrical, environmental and adhesion testing.

Chapter 5 presents results of accelerated temperature cycling, Finite Element Analysis simulations and fatigue life estimations.

Chapter 6 summarizes this thesis and suggests future work.

CHAPTER 2 Review: Chip to Wafer Interconnections

2.1 Introduction

In the past 50 years, semiconductor manufacturing has seen great advances due to device size reduction and improved processing technologies. Moore's Law is frequently cited as predicting IC device density to double every 2 years[1]. This prediction is helpful for researchers and industry to develop solutions to meet cutting edge technological needs. To further develop predictions, the International Technology Roadmap for Semiconductors (ITRS) is compiled by international associations. The ITRS provides a 15 year outlook for the semiconductor industry as a guidance tool for technology development. The ITRS:2012 Update predicts 3-D interconnects reliability as a process integration difficulty in the near term of 2011-2018[1]. While 3-D interconnects are vital to overall device functionality, interconnect reliability is of more concern for extended operational life. ITRS 2012 predicts reliability to be one of the five most critical challenges for interconnect technologies [1]. Table 1 summarizes the five difficulties in semiconductor interconnects as reported by the ITRS. Current research and development of high performing devices requires new material combinations for interconnection structures. Furthermore, compatibility of multi-material combinations at electrical junctions must be considered. In order to address reliability concerns, interconnection structures must be subjected to electrical, thermal and mechanical testing. Coupling thermomechanical testing along with electrical performance provides strong evaluation methods of how flip chip devices will perform under various environmental conditions.

Material	Reliability	Metrology
• New Materials • Improve conductivity • Reduce dielectric permittivity	• Longer Life Devices • Analyze thermo-mechanical and electrical exposure • Model behavior • Detect failure mechanisms	• Control Interconnect Features • Improve circuit performance • Reduce feature size

Table 1: Difficulties in semiconductor interconnects for near term [1].

2.2 Interconnects Overview

Wire bonding and flip chip are the two primary methods of chip to wafer interconnection [2]. Each method provides favorable characteristics as well as limitations. Both methods involve direct electrical and mechanical connection of upper die onto lower carrier substrate. Wire bonding is a common industry proven process. In this method, upper die is attached to carrier substrate face up, with bond pads oriented outwards. Connection is created by thin gauge wires, bonded electrically and mechanically between upper die bond pads and lower substrate metallization. Flip chip bonding eliminates thin gauge wires and employs metallic bump structures for connection of die and substrate. Bumps can be formed on die, substrate or both. In a flip chip process, connections are created at each solder bump location. Bump attachment is achieved by thermal reflow, thermo-compression or thermosonic force, face down onto carrier substrate (hence, the term flip chip). Flip chip bonding is rapidly becoming a preferred method of interconnection due to device requirements of smaller geometry, increased input/output (I/O) density and increased performance.

2.2.1 Wire Bonding

Wire bonding can be described as a "single-point-unit operation", with each bond individually produced [3]. It is generally suited for low cost, low speed and larger packaged devices. Thin gauge metallic wires as small as 15µm in diameter, commonly aluminum, copper, silver or gold, are routed from upper die bond pads to lower carrier metallization pads. Bond attachment is created by the application of force, heat and/or ultrasonic energy [4]. This bonding process is repeated for every contact pad on the device. Single point bonding for devices with high I/O can become unmanageable for manual techniques. Automated bond tools with vision system capabilities are available for large device processing. A simplified schematic of a wire bonded device is included in Figure 1 below:
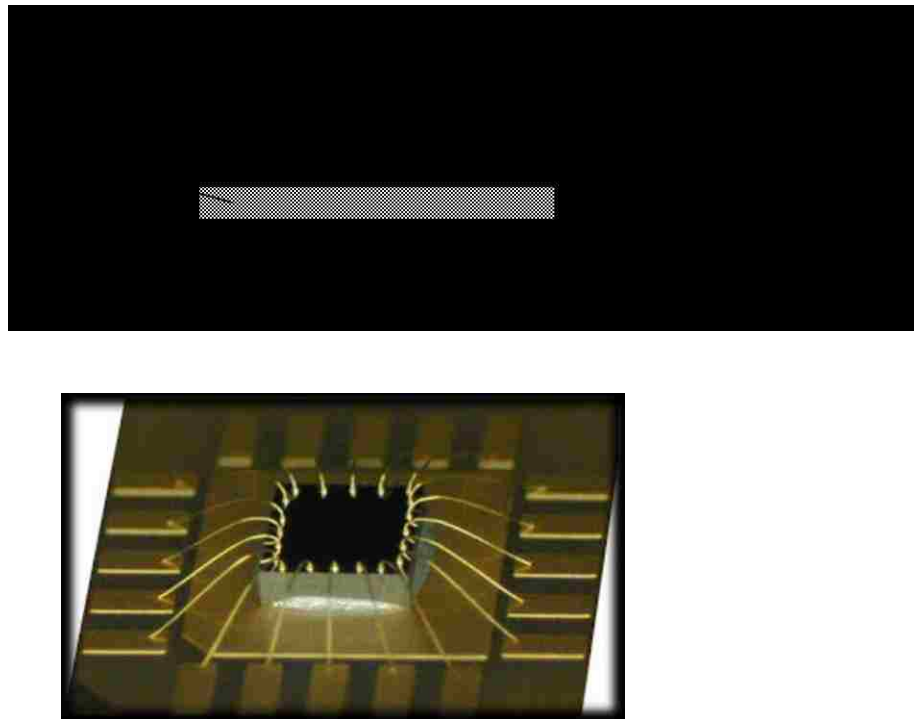
Figure 1: Wire bonded device. Schematic representation and functional device [5].

Wire bonding is a well-defined process that has proven effective for use in the packaging industry for several decades. Manual bonding operations allow process flexibility during device development. The second primary advantage of wire bonding is visual inspection at connection sites. This allows for device troubleshooting and failure mitigation. This technology is not without limitations that prevent its use in certain technologies. The first limitation of wire bonding is the high inductance due to the physical wire connection. Metallic properties and wire length contribute to increased inductance and reduces device signal speed. High performance devices requiring accelerated signal processing are many times not candidates for wire bonding. The second primary limitation of a wire bonded device is limited I/O density. Bond pad sites are limited to the external perimeter of device substrate and therefore inner device area is unused. Industry trends point to small area devices and therefore eliminates wire bonding for these application. A comparison of wire bonding technologies is shown in Table 2 below.

Wire Bonding	
Advantages	*Disadvantages*
Industry proven	Electrical performance
Process flexibility	Not suited for high I/O
Visual inspection of bond sites	Bonds are formed individually

Table 2: Wire bonding technology comparison.

2.2.2 Flip Chip Bonding

Flip chip is a generic term describing a method used to bond electronic devices. Bonding creates electrical connection between upper die and lower carrier substrate. Typically, solder bumps are deposited onto upper die and then mated to lower wafer substrate. IBM pioneered this technology in the early 1960's for use in computing hardware, with a process called controlled collapse chip connection, or C4 [6, 7]. Flip chip interconnect

technologies have since evolved and improved greatly in the last five decades. In more recent years, device pad pitch has steadily decreased from 40µm in 2004 to 25µm in 2013 for HP technology nodes[8]. Device miniaturization has driven flip chip technology to improve interconnection structures. Solder bumps are a preferred interconnection structure, providing quality electrical connection, wettability and highly repeatable processing. Flip chip processing with solder bumps can be characterized by four primary steps: wafer preparation, solder bump formation, flip attachment and finalized underfill. Generic solder bump processing begins with deposition of an under bump metallization (UBM) onto wafer bonding sites. UBM is a necessary interface that promotes solder adhesion/wettability, limits metallic diffusion and anchors solder bumps to device substrate. After UBM deposition is complete, solder bumps can be formed on top of the UBM. Solder bump formation can be achieved in multiple ways, the most common being vacuum evaporation. After successful solder bump formation, dicing of a complete wafer can occur. Once diced a single upper die is flipped, aligned and bonded face down onto the lower substrate. Bonding mechanisms can either be heated reflow or thermo-compression force. Many materials are present in a flip chip bonded device including: substrate material, metallic bond sites, UBM and solder metals. Variations in material properties such as coefficient of thermal expansion (CTE) can create fatigue in interconnect sites during operational thermal environmental exposure. To limit or prevent such fatigue an underfill process is used. During underfill a nonconductive epoxy is dispensed around the perimeter of the upper die to fill voids around all solder interconnections. This epoxy serves two functions; it provides structural reinforcement to individual bumps and limits the mismatch of CTE throughout the device. In depth

discussion of flip chip processing methods is included in the later portion of Chapter 2. A simplified schematic of a flip chip device is shown in Figure 2 along with a single flip chip mounted transistor[9].

Flip chip processing has become the standard device methodology for high performing devices due to numerous advantages over wire-bonding, namely high packing density and improved electrical characteristics. Electrical advantages include shorter signal paths and reduced inductance and capacitance of connections. Bond site availability within device perimeter allows designers to reduce area and height of a completed package. Thermal management is another key area for long lasting assemblies. Flip chip components dissipate heat better through the back of the die, which thus reduces stresses caused by residual heat. Flip chip processing is well suited for large scale production in established facilities. This is due to high capital cost for equipment and processing operators. Table 3 summarizes the primary advantages and disadvantages of flip chip bonding.
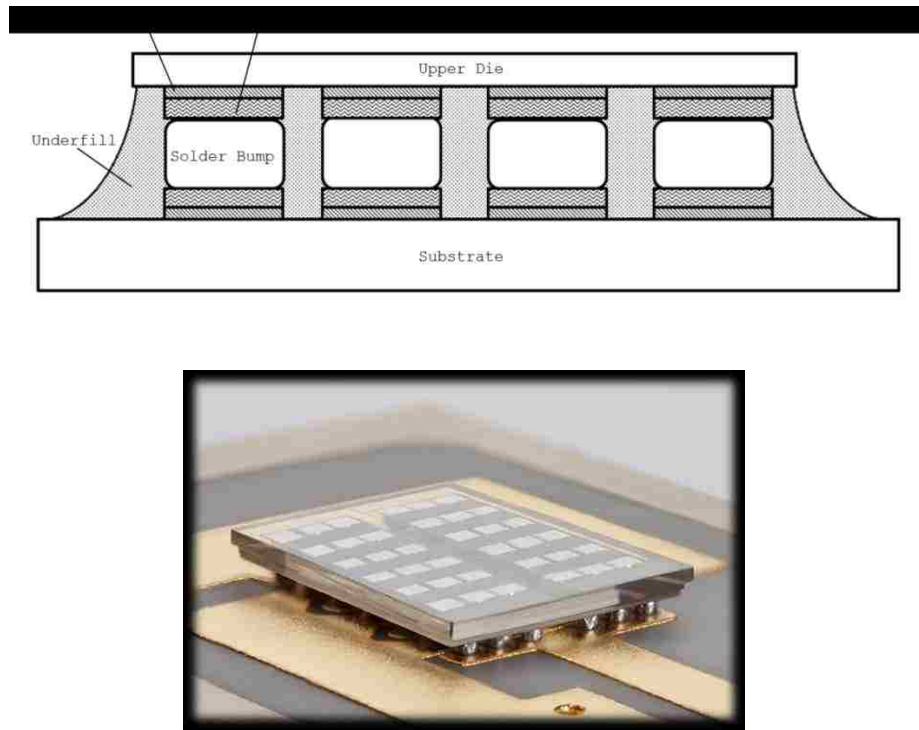
Figure 2: Flip Chip Device. Upper: Schematic, Lower: Flip Chip power device[9].

Flip Chip Bonding	
Advantages	*Disadvantages*
High packaging density	Additional processing
In-area array interconnects	Difficult inspection of interconnections
Electrical and thermal performance	High cost for low volume
Lower cost for high volume	
High reliability	

Table 3: Flip Chip technology comparison.

2.3 Under Bump Metallization (UBM) for Flip Chip Devices

In its simplest form a solder bump interconnection is comprised of a multi-layer UBM, solder bump and metallic bond pad [10]. The primary function of UBM is to join the metal bond pad and the solder bump. In addition to mechanical and electrical connection, UBM provides diffusion resistance and solder wettable characteristics.

2.3.1 UBM Principles

Flip chip devices with UBM and solder bump interconnections are found in a wide variety of electronic based packaging such as portable consumer devices, computing hardware and military technology. Devices with metallic bond pads are not solderable, therefore require deposition of a UBM. A quality UBM is essential for the reliability of the entire package. A simplified schematic of solder bump interconnect and a cross-section scanning electron microscope (SEM) image is shown in Figure 3 below:
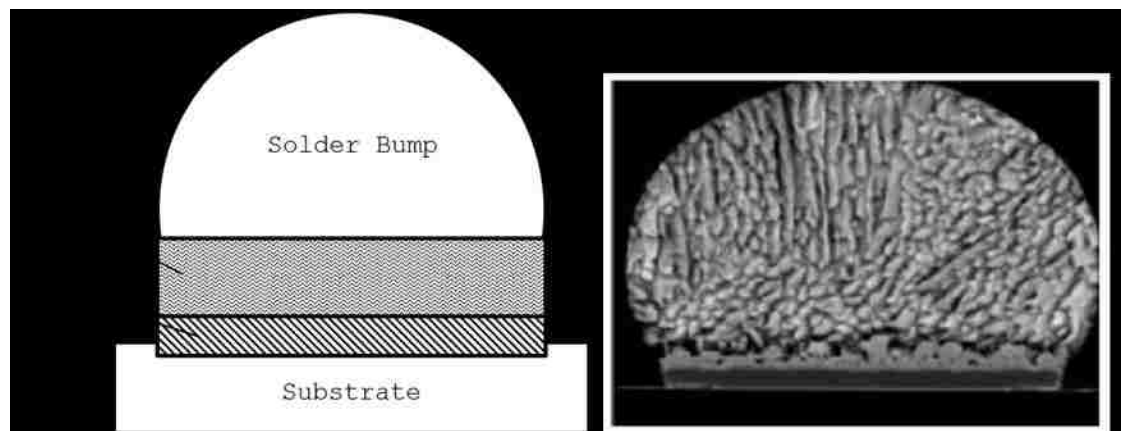
Figure 3: Solder bump structure. Right: SEM image (Sn bump, NiCu UBM [8])

Bond pad metals typically form an insulating oxide layer when exposed to air. This native oxide creates an unfavorable surface for solder bump adhesion and eventual electrical connection. Deposition of a UBM onto bond pads prevents oxide formation and

prepares for quality interconnects. The multi-purpose UBM must adhere to metal bond pad, intermediate passivation layer and also solder bump metal while acting as a diffusion barrier between bump metal and bond pad metal. In addition, low resistance electrical contact is required from UBM material. To meet these fundamental requirements multiple metal layers are usually deposited successively to create a UBM stack.

Properties of UBM [11]

Adhesion

- Quality adhesion of UBM to bond pad metallization, surrounding passivation layer and solder bump metal. The role of UBM is to be a compatible interface for all material present and to ensure that devices will remain bonded through processing and operational life.

Diffusion barrier

- Diffusion barrier between solder and bond pad metal. Diffusion interactions cause reliability issues.

The purpose of a diffusion barrier layer in IC fabrication is to prevent or limit the chemical interaction of two adjoining metals. When metals interact by diffusion, new phases can be formed, thus creating unpredictable electrical and structural connections. Barrier layer materials must be stable in the presence of all device metallurgy. Also, maintaining good electrical conductivity ($\sim 200 \mu\Omega$-cm)[12] is essential. Diffusion barriers are commonly categorized into three types: passive, sacrificial and stuffed.

Passive barriers are non-reactive to either joined metal materials. Metals with corresponding nitrides are ideal diffusion barriers. For example, Titanium nitride (TiN) is commonly used since it possesses strong atomic bonds, chemical inertness and excellent electrical conductivity.

Sacrificial barriers limit diffusion for a certain period of time. Barrier material diffuses with joined metals at various rates and is consumed throughout the device lifetime. Slower diffusion rates perform as better barrier layers. The disadvantage with sacrificial barriers is that layer consumption can be difficult to predict and therefore creates reliability issues.

Stuffed barriers physically block diffusion paths at grain boundary sites. Typically, stuffed barrier materials are introduced during deposition of another barrier metal layer. Titanium tungsten (TiW) deposited in a nitrogen environment is an actively used stuffed barrier [12]. The nitrogen introduction fills grain boundary diffusion paths and makes them inoperable.

Solder wettability

- Final top layer of UBM must be solder wettable.

Solder wettability is described as the ability of a surface to readily accept melted solder to create a continuous layered material. This defines the physical joint necessary for solder interconnections. In flip chip packaging, wettability is influenced by surface properties of UBM material and solder alloy proportions [13].

Oxide barrier

- UBM must not be readily oxidized during processing.

Oxides act as insulators and are undesirable for electrical contacts. Oxides on metal bond pads must be removed prior to UBM deposition. In addition, the UBM structure must not readily oxidize or solder wettability will be compromised. A common metal used in UBM structures is gold (Au) due to its corrosion resistance and electrical conductivity.

Thermal compatibility

- UBM must not create stress on solder bump, bond pad metallization or substrate due to mismatch of coefficient of thermal expansion (CTE).

2.3.2 UBM Composition by Layer

Most UBM contain multiple metal layers. These layers and corresponding functions are summarized in Table 4 below [11]:

UBM Layer	Function	Metals Used	Thickness
Adhesion & diffusion barrier	Joining of bond pad metal with passivation layer Prevent diffusion interaction of bond pad and solder metals	Cr, Ti, TiW, Ni, Pd, Mo	0.15 - 0.2 μm
Solder wettable layer	Improves ability of melted solder to create a reliable joint	Cu, Ni, Pd	1 - 5 μm
Oxidation barrier layer	Prevents UBM structure from oxidation	Au	0.05 - 0.1 μm

Table 4: UBM function and composition by layer.

2.3.3 UBM Deposition Techniques

In order to ensure a quality bond, oxide formed on pad connections must be removed before UBM can be deposited. Oxide removal techniques include dry etching, plasma etching or a wet chemical bath. For typical aluminum bond pads, oxide layer is milled using a focused ion beam. Ion bombardment of oxide layer prepares the surface for subsequent physical sputtering. Next UBM can be deposited in vacuum by sputtering,

evaporation or can be chemically plated. The most common physical vapor deposition method is multi-metal vacuum evaporation.

2.4 Processing after UBM Deposition

2.4.1 Interconnect Bump Formation

Flip chip processing relies heavily on interconnect bump formation. An understanding of processing methods is essential in UBM and bump interaction analysis. This section includes a brief overview of traditional bump fabrication methods, which occur after UBM deposition has completed.

Evaporation

IBM's C4 technology pioneered sequential evaporation of metallic layers[14]. In this process, UBM and solder material (Pb or Sn based) is evaporated through a metal mask (commonly molybdenum) onto a complete wafer's surface. The metal mask defines solder deposition geometry and area covered. The evaporation process occurs at elevated temperatures under vacuum in order vaporize deposition material. First, thin-film layers of UBM are evaporated on device bond pads. Next, solder or other material can be evaporated through the metal mask openings generated in the previous UBM deposition step. Sequential evaporation requires precise alignment of mask and wafer surface.

Lift-off Technique

Lift-off processing is a commonly used method for feature patterning of desired material using sacrificial photoresist (PR). An additive processing methodology creates structures of desired materials in openings in PR. This process begins with a layer of light

responsive PR deposited on the entire wafer. Next, openings are made in PR layer to define metallization and corresponding solder bump geometry. UBM and solder bump material is then deposited in previously defined openings to cover the entire wafer. Finally, unwanted PR and other unneeded metallization are washed away. Only UBM and solder bump material deposited in openings created in previous steps will remain. More details pertinent to this technique for use with indium interconnect material are included in a following section.

Printing Solder Paste

In this method solder bumps are created by printing a solder paste mixture through a stencil or screen mask. The solder paste is a mixture of solder powder, flux and other organic material [14]. The most common applications of this technique are in low cost consumer and automobile electronics, specifically by Delco Electronics [2]. This method is not suitable for fine pitch applications due to limitation of solder paste and stencil geometry. Another limitation of this process is the potential for high void population and therefore reliability concerns[14].

Electroplating

Electroplating is a deposition process using electrical current to create metallic coatings on photolithographic defined structures. To begin, UBM is deposited as a blanket film forming solder bump defining structures and ground connection for electrical plating. PR is then deposited and patterned with various openings. The wafer, acting as the cathode, is now plated in a chemical solution with electrical current applied. After plating is complete, PR is stripped and UBM is etched resulting in non-reflowed solder bumps.

Anisotropic Conductive Films

Anisotropic conductive films (ACF) composed of conductive polymers are an alternative to solder bumped flip chip connection structure. The mechanism of attachment and conductivity is due to metallic conductive particles held within a filler polymer. The lower substrate and upper die are mated and electrical connections are created at bond pad locations. Common electrically conductive particles are silver and nickel (Ag, Ni). Filler polymer materials vary due to device requirements. ACF have limitations for use in high-density packaging applications due to poor contact resistance and inability to connect devices with low I/O pitch (<50µm) [15]. ACF with finer alignment of conductive polymers in the Z-axis may help to address inability to achieve low pitch devices[16].

2.4.2 Trends in Flip Chip Bonding

IBM's Flip Chip C4 technology was first patented in 1969 [17]. Since then the flip chip industry has seen many improvements such as increase in device density, material compatibility and improved processing techniques. The flip chip industry will be expected to keep pace with markets in memory, mobile phones and electronics.

In order to improve process integration research institutions are finding alternative methods of successful solder bumping. Since the early 1990's significant patents have been submitted with the intent of improving the solder bump and flip chip process. Common trends from research and development institutions point to improved processing at the bump level as well as overall device performance. Bump processing creates

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challenges with photoresist incompatibility and has driven exploration of additional buffer layers within metallization structures[18].

Strict requirements in the flip chip industry will drive device pitch dimensions smaller and smaller. This prediction, in agreement with ITRS forecasting, will facilitate growth in flip chip methodologies compared to wire bonding interconnect methods. Fine pitch flip chip devices have applications in devices from high performing military assemblies to small consumer electronics. No matter the device application, cost effectiveness will be a consistent area of interest for the microelectronics industry. Key solutions for next generation flip chip devices include reducing processing time and improving microbumping dependability.

2.5 Indium Interconnects

In the previous sections concepts related to flip chip electronic devices have been described using conventional solder material. Experimental analysis in this thesis was completed using pure indium as interconnect material. Pure indium is not considered a true solder alloy material and will be defined as an interconnection material from this point on.

Mechanical and electrical interaction of indium joint and UBM is a key component of this thesis. The fundamentals of indium for use as an interconnect material are discussed below.

2.5.1 Indium Overview

Physical Properties

Indium is classified as a soft metal and is commonly used for low temperature flip chip die attachment[19]. When used for die attach, indium offers many advantages over common solder alloys such as ductility at extremely low temperatures, high thermal conductivity and compensation for mismatched coefficient of thermal expansion (CTE) between dissimilar materials.

The crystal structure of pure indium is a face-centered tetragonal (FCT), with lattice constants of a=0.32525 nm, c=0.49465 nm[20]. Indium behaves viscoplastically at high and low temperature extremes. Viscoplasticity is defined as the deformation of the material being dependent on the rate in which an external load is applied. For electronic interconnects, viscoplastic response is caused by repeated environmental/operational thermal excursions. Thermal excursions can be classified as the wide range and repeated temperature cycles an electronic assembly is exposed to. Indium has a relatively low melting point (156.6°C, 429.6K), and forms quality bonds even at room temperature. Indium has superior performance in low temperature applications compared to its Sn-Pb counterparts due to high ductility behavior. Indium's ductility is advantageous during temperature changes and compensates for different CTE between mated materials, a common reliability issue in three dimensional electronic assemblies.

Indium Physical Properties	
Density	7.30 g/cc
Elastic Modulus	12.74 GPa (20°C in tension)
CTE	24.8 ppm/°C
Melting Point	156.6°C

Table 4: Indium Material Properties[20].

2.5.2 Indium Bump Fabrication

Indium bumps are most commonly formed by evaporation or electroplating[21]. Evaporation generates uniform coverage of bumps but can be costly due to the need for advanced processing tools. Electroplating is a simpler and less expensive process but uniform bump height can be difficult to acheive. Indium deposition by evaporation and lift-off is used exclusively in this thesis and therefore is included in more detail. Electroplating techniques are not discussed. Figure 4 shows process flow for evaporating indium bumps followed by lift-off.

STEP 1: Pad metallization is defined by photolithography.

STEP 2: Photoresist, commonly negative type, is spun onto wafer surface creating a thick layer. A soft bake at elevated temperatures follows.

STEP 3: Photoresist is exposed and developed. Crucial undercut profile is created due to developer interaction with photoresist.

STEP 4: Solder bump evaporation and underlying UBM materials are deposited by evaporation. UBM deposition is not shown in STEP 4. Interconnect material can now be sequentially evaporated onto all surface of the wafer.

STEP 5: A solvent is used to wash away all the PR and deposited material on top of the thick photoresist layer. The only material remaining is the target UBM and interconnect bump.
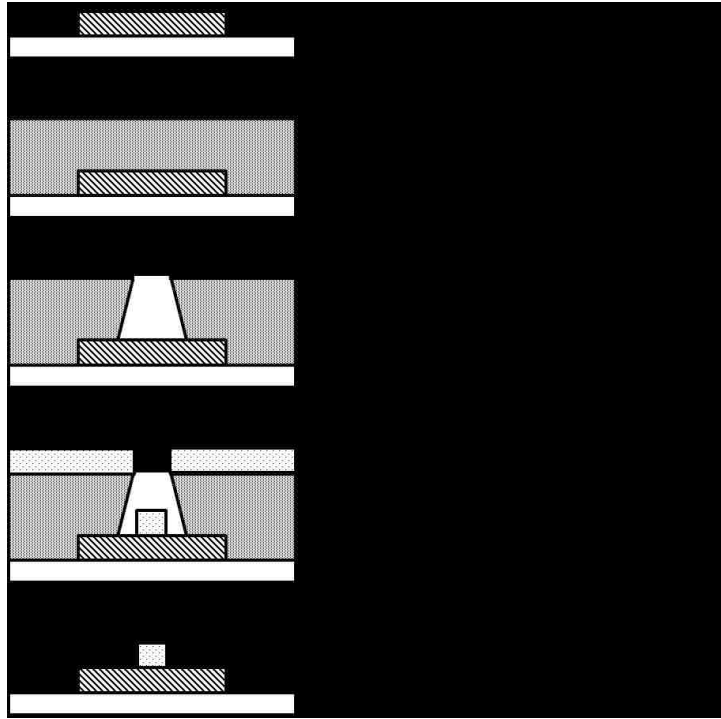
Figure 4: Process Flow: Indium evaporation followed by lift-off

2.5.3 Trends in Indium Interconnect Technologies

Indium bumping is a common interconnection method used in high density focal plane array (FPA) detection systems. FPAs are actively used in military and medical imaging applications. Military FPA systems are subjected to extreme operational conditions and require high reliable indium connections to ensure operation. It has been demonstrated that reliability of an indium solder joint is directly proportional to its height[21]. Therefore, taller bumps typically are suited for longer operating life. Life cycle predictions are not easily formulated and many factors affect operating life. For example, thermal cycling during device operation can induce fatigue in indium bumps. Fatigue and other accumulated affects adversely determine how long a device will operate before failure. Fatigue studies using indium interconnects have been reported for room temperature conditions most notably by Darveaux [22]. Results have shown constitutive

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relations applicable to shear and thermal cycling exposure of indium bumped electronic assemblies. Reliability testing and information for indium interconnects at extreme temperatures is needed for advanced indium technologies.

2.6 Indium Reliability Research

Extensive research efforts from Robert Darveaux have gained acceptance in failure analysis of solder joints. Darveaux's work includes experimental shear testing at room temperature and finite element simulation of solder joint crack growth [22, 23]. Simulation work has investigated interconnect size and pad metallization interactions. Increased emphasis on interconnect reliability has given way to improved finite element analysis simulation. Using detailed geometry models of flip chip devices and temperature cycling conditions, joint failures can be simulated. Coupling simulation and design provides the most comprehensive analysis of joint fatigue life.
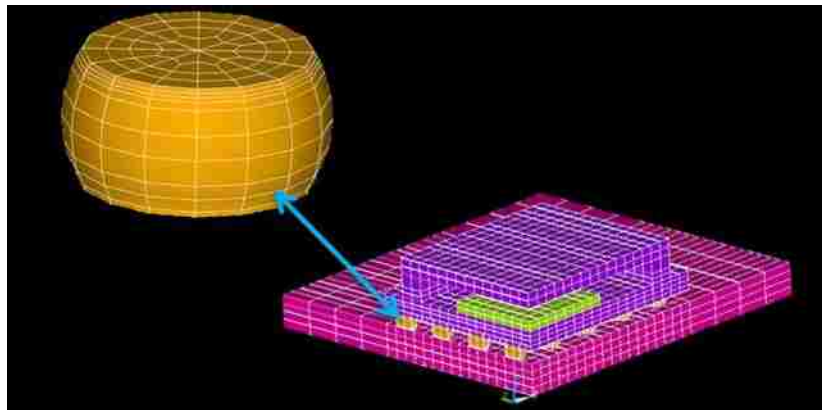
Figure 5: Solder joint and device assembly model. Darveaux[23].

International reliability research is actively published by French defense and space company Sofradir. This research and development facility manufactures infrared (IR) detection systems used primarily in military and space applications. Military IR detectors

operate in the most extreme environments and commonly use indium interconnects. Reliability requirements are strict, demanding 10-15 years of operational life. In order to quantify device performance using indium joining materials Sofradir performs continuous reliability cycling. This type of cycling can induce years of accelerated stress in monitored testing experiments. Sofradir has demonstrated that IR FPA detectors have been continuously cycled for up for 17,500 cycles without failures[24]. Results like this show that temperature cycling of indium bumped devices can prove difficult and time intensive.

2.7 Summary- Process Flow of Completed Device

Up to this point, Chapter 2 has reviewed chip-to-wafer interconnects, UBM principles and indium interconnect material. Each of the previously mentioned principles are essential for device fabrication, but combined they define the overall process flow for an operational device. For simplicity, flip chip processing can be characterized by four primary steps: wafer preparation, interconnect bump formation, flip attachment and finalized underfill. A summary of each step is included below.

2.7.1 Wafer Preparation

During wafer preparation, photolithography and chemical processes are used to fabricate electronic structures on a wafer of semiconductor material. These structures combined to make up electrical contacts for ultimate device operation.

2.7.2 Interconnect Bump Formation

Interconnect bump formation begins with deposition of a under bump metallization (UBM) onto device bond pads. UBM contains adhesion, interconnect wettability and

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diffusion barrier/non-oxidation layers between bond pads and interconnection structures [11]. Upon completion of UBM deposition, interconnect bump material is deposited on top of the UBM. Deposition of interconnect material can be achieved in many ways. The method of deposition depends on device parameters such as bump pitch, cost and interconnect material composition. The most common deposition method is evaporation. In a simplified procedure, previously processed wafers are inserted into a vacuum chamber along with desired UBM and interconnect materials. Material evaporation occurs at elevated temperatures in order to vaporize and scatter atoms onto all surfaces of the wafer. Deposition accumulates on wafer surface in the form of thin films. Multiple layers of metals and alloys can be deposited sequentially while remaining under vacuum, an added benefit in reducing oxide growth. Evaporation processing provides reliable metallurgical control of layer thickness and is highly repeatable [2]. One limitation of evaporation is its inability to cover drastic changes in surface topography or step coverage. This limitation is most commonly addressed with the use of liftoff techniques, as described in a previous section.

2.7.3 Flip Attachment

After interconnect bumps have been formed, wafers are diced and prepared for flip chip attach. A flip chip bonder is used to handle, place and bond the upper die to lower substrate. The accuracy of the tool defines controllability of a flip-chip attach process. It is a common standard for the desired tool accuracy to be greater than 16 percent of the bump pitch [11]. Using optical alignment techniques, die and substrate will be mated via interconnect bump structures. Bonding mechanisms include thermal reflow, compression or thermosonic force. This finalized bonded sample is now available for underfill.

2.7.4 Finalized Underfill

An underfill step is performed to encapsulate the voids between multiple interconnect bump sites, commonly in an array orientation. A non-conductive liquid epoxy, known as underfill, is used to enhance structural support and provide thermal benefits. Underfill helps to bridge the differences of CTE present in a multi-material package. Underfill encapsulation is a crucial step for the reliability of the entire device.

A simplified representation of a typical underfill filled sample is included in Figure 6.
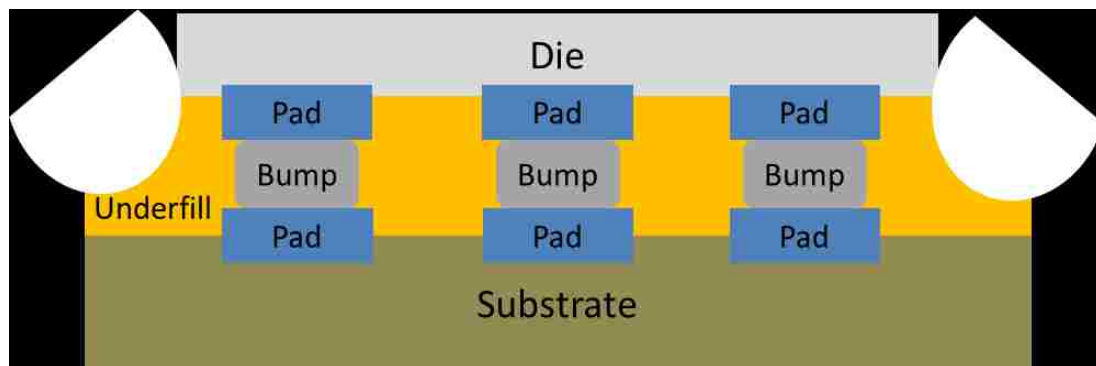
Figure 6: Simplified schematic of underfilled device.

CHAPTER 3 Performance Test Methods: Surface Mounted Devices

3.1 Reliability Prediction

Device lifetime is difficult to predict for multi-material electronic assemblies. Complexity of material interactions and operational behavior due to thermo-mechanical and electrical exposure create challenges for reliability engineers. A common graphical prediction model is known as the bathtub curve, which depicts operational life versus time. The bathtub curve, shown in Figure 7, is divided into three regions. The first downward sloping region is known as early failure or "infant mortality". This period is representative of early failing devices that decrease over time, leaving more robust devices entering the second region. This middle period remains flat and represents normal operational life. In this region failure rates are nearly constant. The third region of the bathtub curve is the end of life or "wearout" period. Devices entering this period begin to experience failures at an increasing rate. Electronic failures are caused by thermal stresses, degradation of electrical components and overall fatigue. Reliability testing methods include mechanical shock, temperature cycling/shock, electrical burn-in and various environmental exposures. The most common testing method for electronics assembly is through accelerated life testing by temperature cycling.
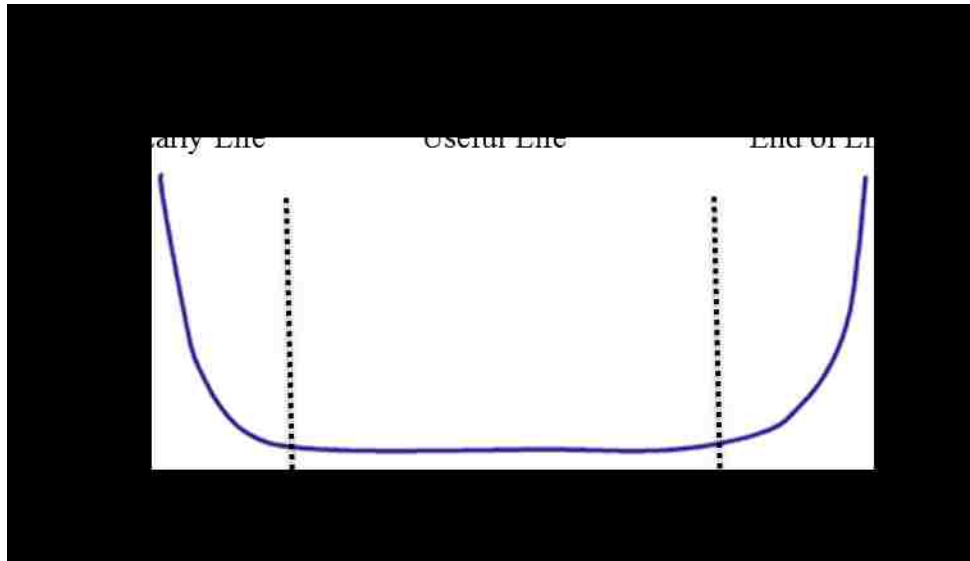
Figure 7: Reliability "bathtub curve" model.

In this thesis, temperature cycling is used as the primary evaluation criterion for device lifetime. Using rigorous temperature cycling, early life failures are examined. Early life failures are extremely undesirable for product development. This indicates defects during the manufacturing process and requires costly and necessary design iterations. Figure 8 summarizes motivation for reliability analysis of devices within the early life region. Fatigue modeling for early life failure is presented in the following section.
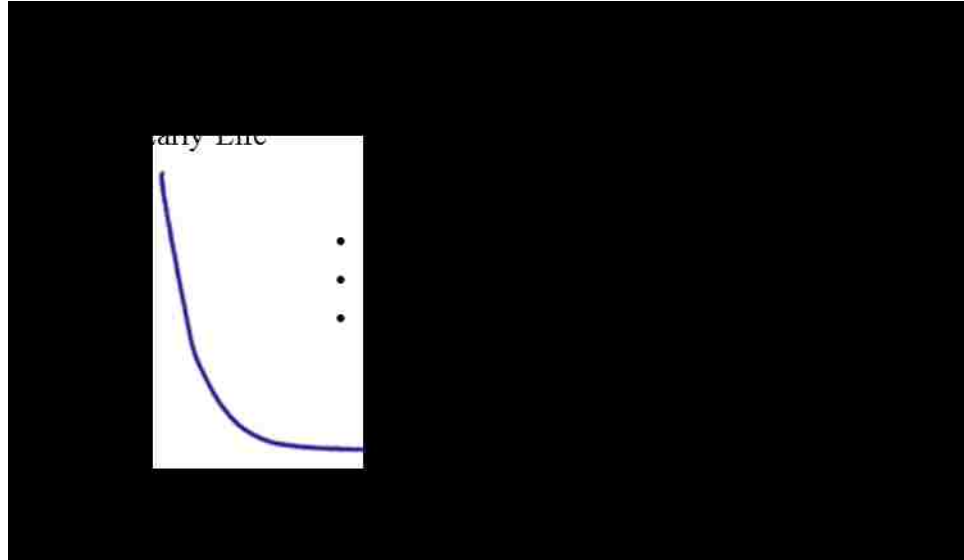
Figure 8: Early failure life region of "bathtub curve."

3.2 Fatigue Reliability Models

Reliability is defined as the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels [25]. Electrical device reliability is dependent on material interactions, mechanical loads and electrical interfaces. Damage mechanisms and failure modes are extensive for surface mount interconnects. The primary damage mechanism investigated in this thesis is deformation, caused by differences of CTE between substrate and interconnect bump. A secondary damage mechanism is brittle intermetallic phase formation due to temperature cycling.

Approach to fatigue modeling

Numerical and constitutive models can be effective in predicting number of cycles to failures (N_f) in devices exposed to accelerated thermal environmental conditions. In order to predict accurately four primary steps are employed[26].

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Step 1: Define theoretical and/or constitutive equation with accompanying assumptions.

Step 2: Generate geometry model and input constitutive equation into FEA software.

Step 3: Using FEA results, calculate median cycle to failure, N_f.

Step 4: Validate FEA results and N_f with experimental temperature cycling data.

Coffin-Manson Model

The Coffin-Manson fatigue life prediction is widely referenced in the literature and is applicable for life prediction within the range of Low Cycle Fatigue (LCF). LCF is defined as the range of 100 and 10,000 thermal cycles[27]. This fatigue model predicts median cycle to failure using the following relation

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon_f}\right)^{1/c} \tag{1}$$

where N_f = median cycle to failure, $\Delta\gamma$ = cyclic shear strain range, $2\varepsilon_f$ = fatigue ductility coefficient, c = fatigue ductility exponent. Fatigue ductility exponent, c is further defined below:

$$c = -0.422 - 6 \times 10^{-4}T_m + 1.74 \times 10^{-2}\ln\left(1 + \frac{360}{t_d}\right)$$

where T_m = mean cyclic solder joint temperature, t_d = half cycle dwell time (min).

Anand Model

The Anand Viscoplastic Model has gained acceptance in the electronics industry for calculating plastic strain rate ($\dot{\varepsilon}_p$) of interconnects and solder joints. This model is used for modeling rate-dependent deformation, including creep and plastic strain. Plastic strain calculations are based on material dislocation deformation due to thermal cycling.

Inelastic or plastic strain rate is found using the following expressions[43]:

$$\dot{\varepsilon}_p = A \, exp\left(\frac{-Q}{RT}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \tag{2}$$

$$\dot{s} = h(\sigma, s, T)\dot{\varepsilon}_p$$

$$\dot{s} = \left\{h_0\left|1 - \frac{s}{s^*}\right|^a \cdot sign\left(1 - \frac{s}{s^*}\right)\right\} \cdot \dot{\varepsilon}_p \, ; \quad a > 1 \tag{3}$$

Where $h(\sigma, s, T)$ is related to the dynamic hardening and recovery processes. The variable h_o is the hardening constant, a is the strain rate sensitivity of hardening process and s^* is the saturation value of internal state variable s.

The evolution equation for saturation value s^* is provided below:

$$s^* = \hat{s}\left[\frac{\dot{\varepsilon}_p}{A} exp\left(\frac{Q}{RT}\right)\right]^n \tag{4}$$

Where $\hat{s}$ is a coefficient and n is the strain rate sensitivity of the saturation value of deformation resistance. For $s < s^*$ Equation 3 can be written as

$$ds = h_o\left(1 - \frac{s}{s^*}\right)^a d\varepsilon_p \tag{5}$$

and then integrated to define

$$s = s^* - \left[(s^* - s_o)^{1-a} + (a - 1)\{(h_o)(s^*)^{-a}\}\varepsilon_p\right]^{\frac{1}{1-a}} \tag{6}$$

Further developments of these fatigue models, as related to experimental samples, are discussed in Chapter 5.

3.3 Introduction to Testing Standards

Failures of electronic assemblies are heavily dependent on material composition and operational conditions. Multiple materials are contained within electronic devices, such as thin film metals and insulating structures. Material complexity means that expansion and/or contraction between varying materials occurs as a result of thermal environmental exposure. This effect is due to varying values in CTE between different materials. For example, under-the-hood automobile electronics must withstand constant elevated temperatures around 140°C. Repeated exposure to thermal environmental conditions increases failure rate. Studies of environmental failure have shown that 55% of all military aircraft electronic failures are linked to elevated temperature exposure and thermal cycling[28]. Reliability research continues to prove that electronic interconnects are the most failure prone structure of an electronic assembly. Many testing standards are actively used in the electronic industry to evaluate reliability of electrical interconnects. Detailed descriptions of thermal cycling and thermal shock standards are included in the following sections. A summary of test standards reviewed in this thesis is found in Table 5.

3.3.1 Thermal Cycling

The Institute of Printed Circuits (IPC) defines thermal cycling as exposure of assemblies to cyclic temperature changes where the rate of temperature change is slow enough to avoid thermal shock (typically less than or equal to 20°C/min.)[29].

JEDEC Test Method A104E[30], a thermal cycling standard, recommends the use of multi-chamber cycling systems for evaluating electrical interconnection structures. This testing method is used to examine the ability of interconnections to endure thermo-mechanical stress when exposed to cyclic high and low temperatures. Convection chambers are the primary apparatus approved by this test standard. Test Method A104E emphasizes ramp rate and soak time as vital parameters for testing. These terms are defined below.

> *Ramp Rate:* The rate of temperature increase or decrease per unit of time, commonly expressed in (°C/min.)

> *Dwell Time:* The total time the sample is within a specified range of each nominal temperature extreme.

Test Method A104E defines that transient thermal gradients must be avoided within test devices. In order to avoid such gradients, ramp rate must be adjusted according to thermal mass of the device. Devices with large mass require slower ramp rates. Commonly used ramp rates are between 10°C/min. and 14°C/min. Dwell times are application specific, but common standards are 10 and 20 minutes.

3.3.2 Thermal Shock

The IPC defines thermal shock as exposure of electronic assemblies to rapid temperature changes causing transient temperature gradients, warpages, and stresses within the part and/or assembly. Typically the defining factor of thermal shock is ramp rate, defined as 20°C/min. or greater.

The two primary testing standards for thermal shock of electrical devices are MIL-STD-202 Method 107[31] and JEDEC Test Method A106[32]. Both standards describe test parameters for determining the resistance of a device to extreme alternating high and low temperature exposures. MIL-STD-202 states that thermal shock can cause cracking or delamination of finishes, leakage of filling materials and changes in resistance due to mechanical displacement of conductors or insulating materials. Typically environmental chambers or liquid baths are employed to achieve thermal shock conditions. For liquid bath immersion, a solution containing water and alcohol is acceptable and preferred. Measurements are recommended to be taken before the first cycle and after final completion of all desired cycles. In situ measurements are not recommended.

JEDEC Test Method A106 [32] is exclusively a liquid bath immersion method. This test method emphasizes liquid circulation in order to achieve desired temperature zones. Perfluorocarbon is cited as the recommended fluid for all test conditions. Hermeticity examination and/or electrical measurements are cited as the evaluation criterion for failure. A summary of all thermal cycling and thermal shock standards are presented in Table 5 below:

Institution	Standard	Type	Year	Thermal Medium	Test Condition	T Min (°C)	T Max (°C)	Dwell (mins)	Ramp (°C/min)
JEDEC	JESD22-A106B	Thermal Shock	2011	Liquid Bath	A	-40	85	-	-
				Liquid Bath	B	0	100	-	-
				Liquid Bath	C	-55	125	-	-
				Liquid Bath	D	-65	150	-	-
Dept. of Defense	MIL-STD-202G	Thermal Shock	2013	Air	A	-55	85	< 5	-
				Air	B	-65	125	< 5	-
				Air	C	-65	200	< 5	-
				Air	D	-65	350	< 5	-
				Air	E	-65	500	< 5	-
				Air	F	-65	150	< 5	-
				Liquid Bath	A	0	100	0.5 - 5	-
				Liquid Bath	B	-65	125	0.5 - 5	-
				Liquid Bath	C	-65	150	0.5 - 5	-
				Liquid Bath	D	-65	200	0.5 - 5	-
Dept. of Defense	MIL-STD-883J	Thermal Shock	2013	Liquid Bath	A	0	100	< 5	-
				Liquid Bath	B	-55	125	< 5	-
				Liquid Bath	C	-65	150	< 5	-
Dept. of Defense	MIL-STD-883J	Thermal Cycle	2013	Air	A	-55	85	> 10	-
				Air	B	-55	125	> 10	-
				Air	C	-65	150	> 10	-
				Air	D	-65	200	> 10	-
				Air	E	-65	300	> 10	-
				Air	F	-65	175	> 10	-
JEDEC	JESD22-A104E	Thermal Cycle	2014	Air	A	-55	85	< 15	10-14
				Air	B	-55	125	< 15	10-14
			`	Air	C	-65	150	< 15	10-14
				Air	G	-40	125	< 15	10-14
				Air	H	-55	150	< 15	10-14
				Air	I	-40	115	< 15	10-14
				Air	J	0	100	< 15	10-14
				Air	K	0	125	< 15	10-14
				Air	L	-55	110	< 15	10-14
				Air	M	-40	150	< 15	10-14
				Air	N	-40	85	< 15	10-14
				Air	R	-25	125	< 15	10-14
				Air	T	-40	100	< 15	10-14
IPC	9701	Thermal Cycle	2006	Air	TC1	0	100	10	< 20
				Air	TC2	-25	100	10	< 20
				Air	TC3	-40	125	10	< 20
				Air	TC4	-55	125	10	< 20
				Air	TC5	-55	100	10	< 20

Table 5: Thermal Shock and Thermal Cycling Test Standards [25, 30, 31, 34].

3.4 Reliability Prediction Using Environmental Testing

Temperature cycling coupled with electrical measurement testing is an effective method for monitoring early failures of semiconductor devices. As introduced in section 3.1, a common failure trend is known as the bathtub curve. This curve predicts higher failure rates during the initial life cycle of a device. Depending on environment testing method employed, thermal shock or thermal cycling, device lifetime can estimated. Thermal shock creates unrealistic environmental conditions that may initiate failures in the early life region. Typically thermal shock testing is used for analysis of extreme operating

conditions. Thermal shock testing may result in failures of all samples during bathtub model's early life region. A better method is thermal cycling. This less extreme technique introduces normal operational stresses at an accelerated rate, thus saving testing time. Using thermal cycling for reliability prediction provides superior insight into device performance during early life period. Experimental testing conditions used in this thesis are presented in the following chapter.

CHAPTER 4 Experimental Setups and Testing Procedures

4.1 Introduction

This chapter presents experimental techniques used to generate and temperature cycle UBM samples. The first part of this chapter defines sample generation methods. The later portion of this chapter describes testing methods and detailed experimental setups. Figure 9 shows experimental procedure process flow for UBM reliability assessment.
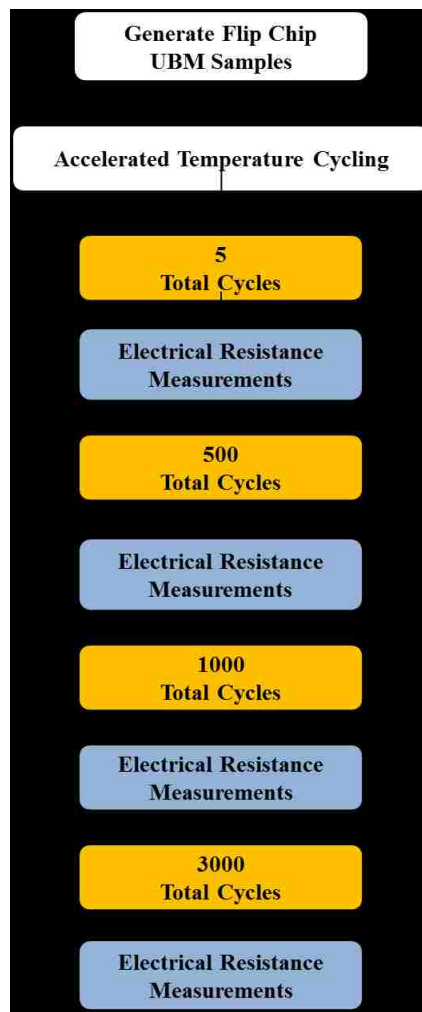

Figure 9: Experimental procedure process flow.

4.2 Test Characterization Vehicle

The test vehicle examined in this thesis was a silicon on silicon device with multiple four-point test measurement structures. Test structures include daisy chains, serpentines and kelvins, all accessible for probing at the outer edge of the device, shown in Figure 10. Daisy chains are comprised of multiple two and three-dimensional wiring schemes through indium bump array. Serpentine structures monitor open contacts and characterize via resistance. Kelvin structures characterize single indium interconnect, used for contact resistance calculations.
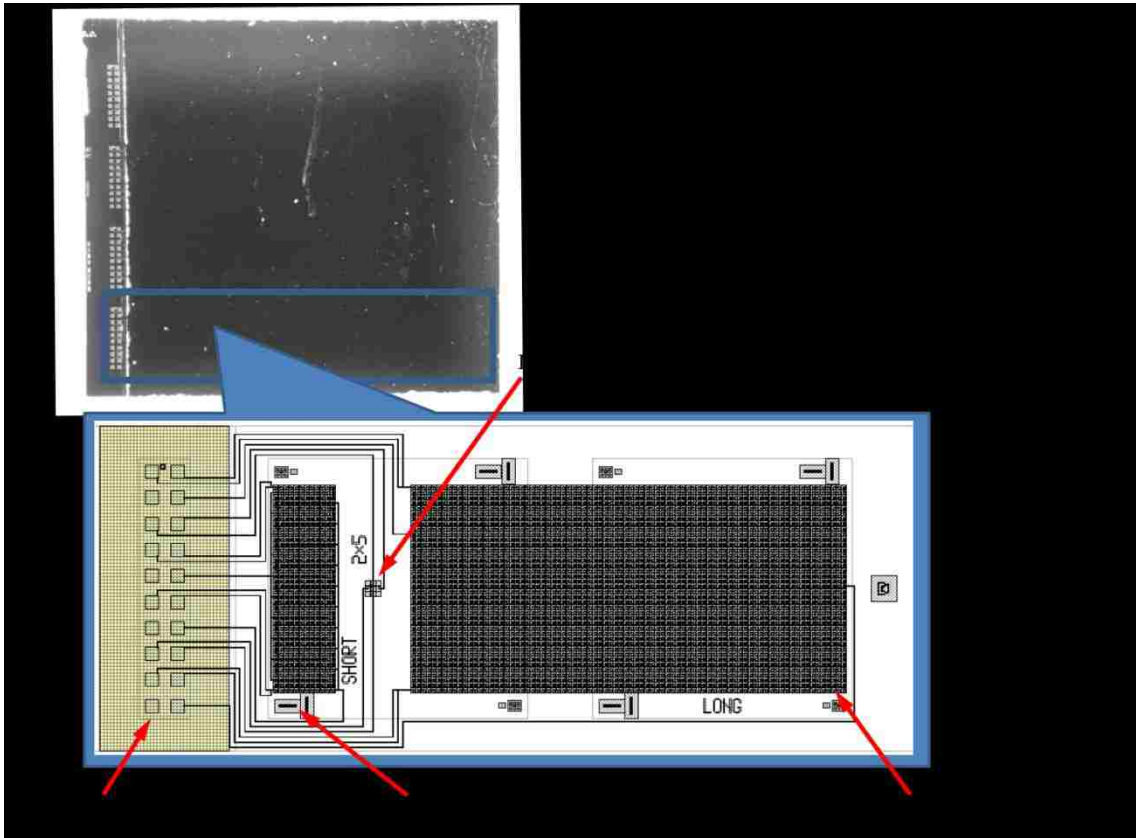

Figure 10: UBM Test Vehicle.

4.3 UBM Sample Generation

100 bonded, die-level samples were generated for this thesis. Processing of the samples occurred on 6 inch (150mm) wafers and required multiple steps and tooling all found in a standard semiconductor fabrication facility. A simplified schematic view of a typical sample is included below. Individual samples were roughly 12mm x 12mm with over 6,000 indium bump interconnections per sample. Multiple electrical structures are present in each sample, allowing for flexibility in electrical characterization testing.
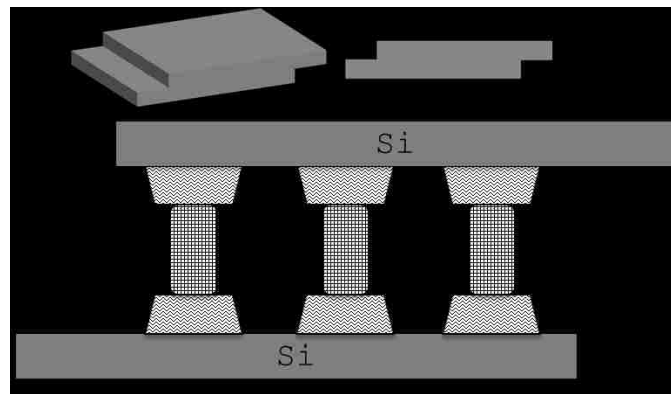

Figure 11: Simplified schematic of bonded sample.

A detailed image of a typical sample is shown in Figure 12. This image shows a top and bottom view of a sample. Top view shows four electrical test pads available for resistance monitoring of indium interconnection structures contained in center area. Bottom view shows dark colored epoxy underfill material.

Figure 12: Typical bonded UBM sample, (Left) Top view. (Right) Bottom view.

4.3.1 Metallization

Under bump metallization was deposited via evaporation. Wafers were inserted in a vacuum chamber system where elevated temperatures evaporated and deposit metal material. Multi-layer UBM required sequential evaporation steps of each metal. The three UBM metal stacks examined in this work include: Ti/Ni/Au, Ti/Ni and Ni. Corresponding UBM metal thicknesses are organized in Table 6.

ID	UBM	Thickness (nm)
UBM 2	Ti/Ni/Au	20/100/50
UBM 3	Ti/Ni	20/100
UBM 4	Ni	100

Table 6: UBM sample material composition and thickness.

4.3.2 Indium Interconnections

The liftoff of indium metal produces pillars of uniform height and pitch. A generic liftoff process was discussed in Section 2.5.2. Identical processing was implemented for test sample generation. Indium bumps fabricated for UBM test samples were 20x20µm, 6µm

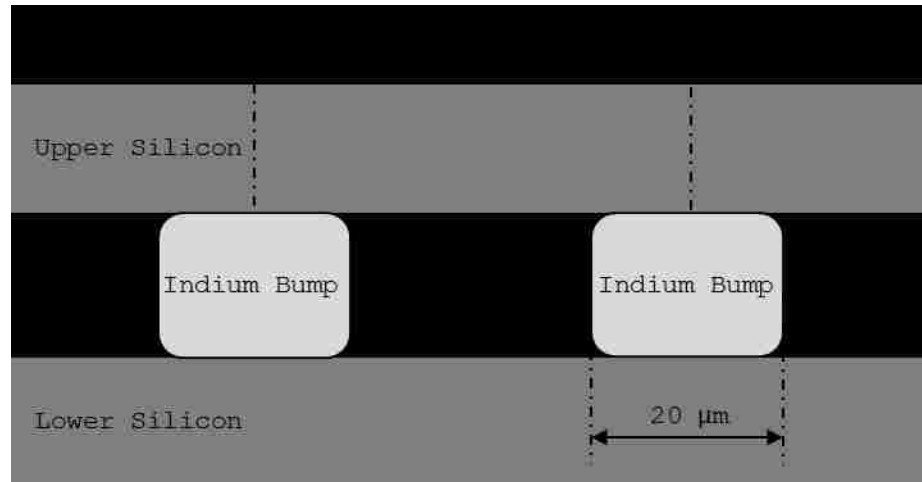tall and 40µm pitch, center-to-center distance. Figure 13 defines key dimensions of test samples.

<div align="center">

Figure 13: Two dimensional schematic. Internal dimensions of UBM samples.

</div>

4.3.3 Dicing

Up to this point, fabrication processing has occurred at the wafer level. Indium bump evaporation and liftoff indicate the end of wafer-level processing. Dicing, or sometimes called singulation, separates small die from a larger wafer. Multiple die were generated from one single wafer. For this study, roughly 40 die were separated from a single 6 inch (150mm) wafer.

4.3.4 Bonding

Accurate pick and place bonding ensures quality electronic contact and continuity. This was an essential process for sample fabrication. Bonding was done on a Karl Suss FC150 bonder. Non-reflowed compression bonding was achieved with bonding force of 15kgf (147N) for 15 seconds, ramp to force of 30 seconds. Bonding tool is shown in Figure 14.
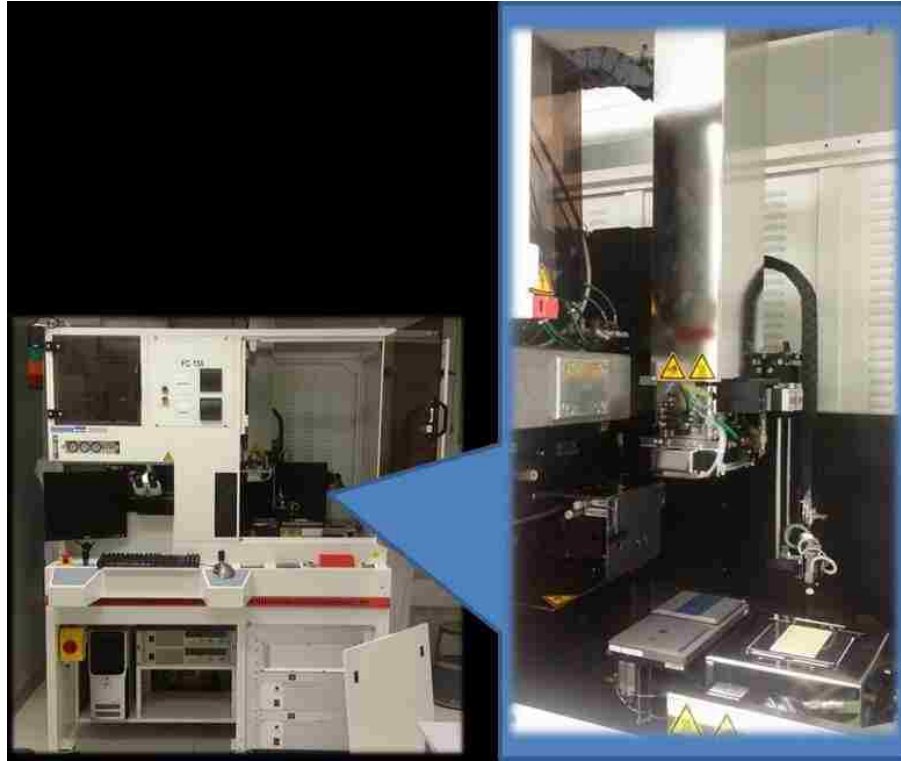
Figure 14: High accuracy pick and place bonding tool.

4.3.6 Epoxy Encapsulation-Underfill

Upon completion of bonding, an underfill process is performed to improve reliability of the entire device. A total of 100 samples were bonded and available for analysis. 50 samples were underfilled and 50 were left non-filled. The motivation to generate underfilled and non-filled samples was to further analyze behavior of indium interconnect degradation with and without the benefits of an underfill epoxy. The underfill process was done manually with the use of an electronic fluid dispense (EFD) tool. Dispense conditions were 21 psi positive pressure using a 25 Gauge (0.5144mm outer diameter) needle. Substrate temperature was elevated to 80°C using a hot plate. Substrate heating was employed to aid in capillary flow of epoxy. Upon completion of underfill dispense, samples were cured at 150°C for 30 minutes in a convection oven. Low viscosity epoxy,

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Chipcoat U8443-14, from Namics Corporation was selected for its superior capillary flow in narrow gaps[35]. Material Properties are provided in Table 7.

CHIPCOAT U8443-14 Underfill Epoxy		
Item	**-**	**Unit**
Filler Content	50	wt%
Color	Black	-
Viscosity	10	Pa.s
Tg (TMA)	135	°C
CTE	42	ppm/°C
Bending Modulus	6.5	GPa
Bending Strength	110	MPa

Table 7: Underfill Epoxy Material Properties.

Underfill Coverage Verification

Narrow gaps present in UBM samples proved difficult to underfill using conventional epoxies. CHIPCOAT U8443-14 provides excellent filling characteristics for gaps under 10 μm. Staggered geometry of bonded samples, as seen in Figure 11, allows for underfill process to occur on bottom side of sample, leaving top side bond pads untouched. Infrared imaging of non-filled and underfilled samples provided validation of epoxy fill coverage within entire 12 x 12mm die. Epoxy material appears as dark areas in right image. Figure 15 shows two samples imaged side by side. The left sample is underfilled; right sample is non-filled. Dark perimeter defines complete epoxy material coverage and a quality encapsulation process.
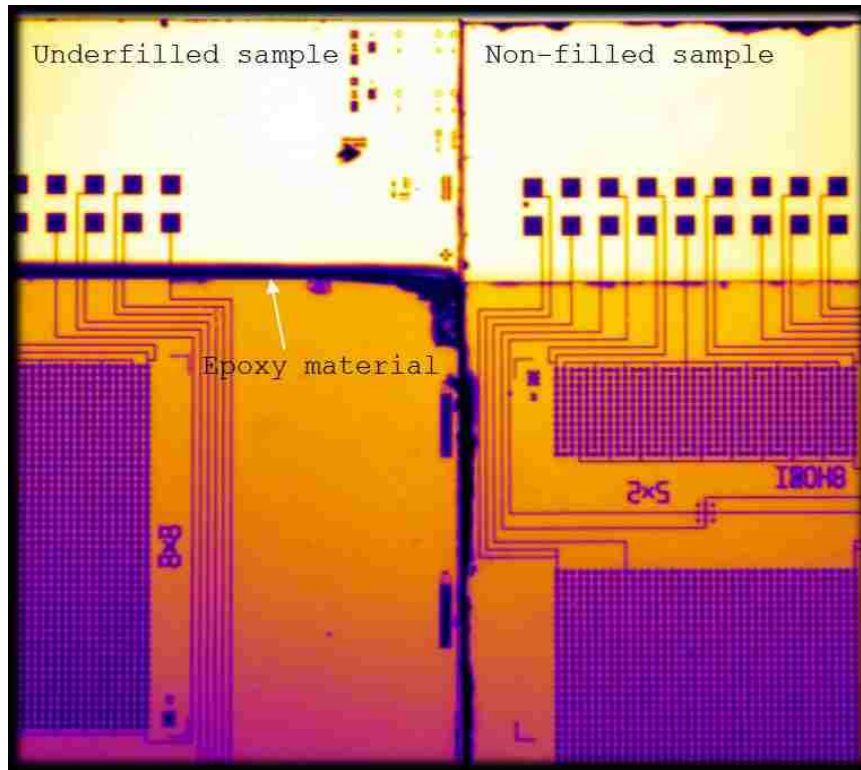
Figure 15: IR inspection of underfilled sample.

4.4 Testing Conditions

4.4.1 Electrical Resistance Measurement System

Preliminary electrical screening was used to identify known good die prior to temperature cycling exposure. Electrical screening was conducted on a manual probe station and MATLAB controlled switch/measure unit, seen in Figure 16. Resistance values of various kelvin, daisy chain and serpentine structures were measured. Data collected was used to eliminate outliers and establish reference values for tracking of samples throughout temperature cycling. The benchtop probe station is comprised of the following subsystems, shown below.

- Control computer (A)

- Agilent switch/measure unit (B)

- Multi-pin probe card (C)
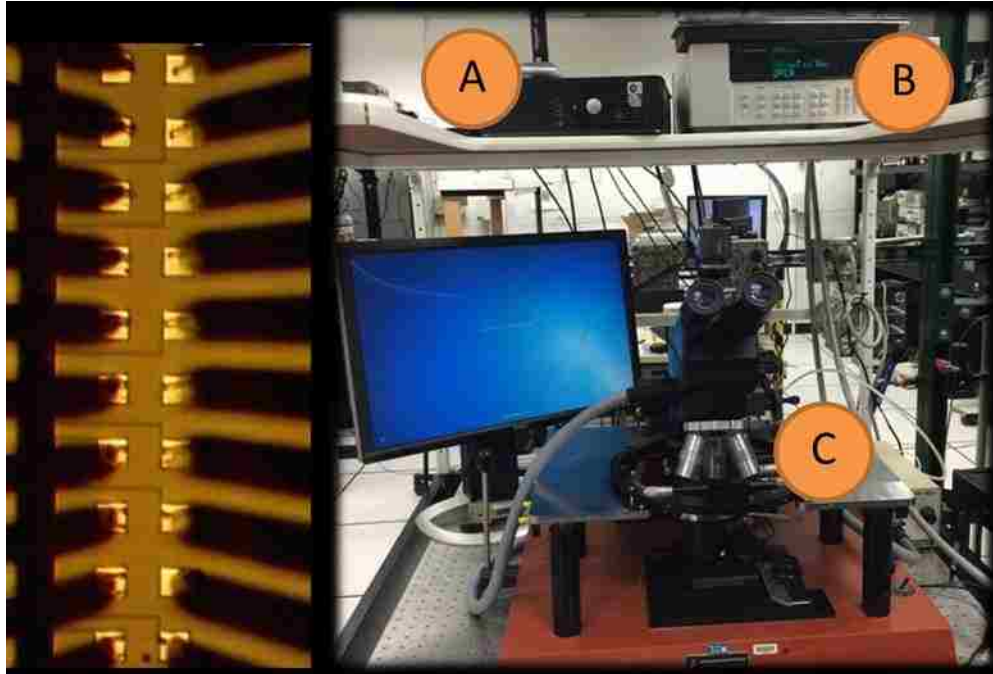
Figure 16: Manual probe station system
Left: Test pads as seen through microscope. Right: Probe station testing system.

The control computer interfaces with the switch/measure unit to sweep through pre-defined measurement schemes corresponding to test structures within UBM samples. A single touchdown of probes, as shown in Figure 16 at Left, contacts twenty test pads and measures resistance values of various structures. This measurement system allowed for accurate and repeatable testing of multiple samples. Resistance resolution of 0.001Ω was achieved using this system. User interface for data acquisition was access through a graphical input window shown below.
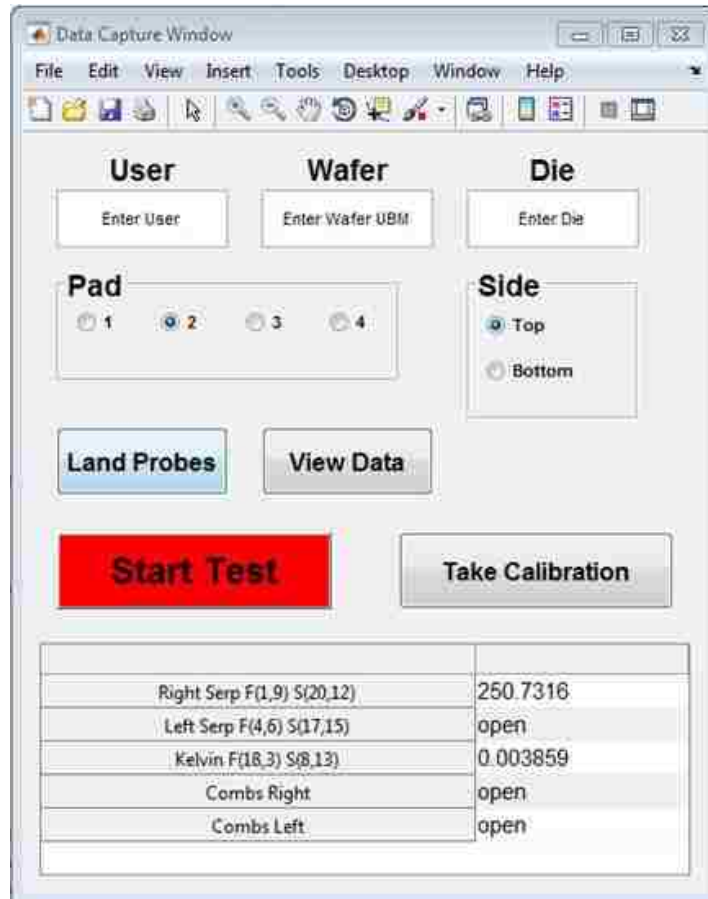
Figure 17: Data acquisition user interface.

4.4.2 Thermal Conditions and Temperature Cycling Equipment

Thermal Conditions

Temperature cycling testing was done from -55°C to 125°C with ramp rate of 15°C/min. and dwell time of 10 minutes at each temperature extreme, consulting with JEDEC A104E[30] and Military Standards 883J[34]. 3000 cycles of total thermal exposure was defined, intending to expose samples to more rigorous conditions seen in true operation. Furthermore, reliability of indium interconnects and accompanying UBM can be validated through early life failures. If devices are able to withstand early life failures confidence is gained that longer life operation is achievable. Profile of one complete

temperature cycle is shown in Figure 18. Cycled parts were removed from temperature cycling chamber and tested at intervals of 500, 1000 and 3000 cycles.
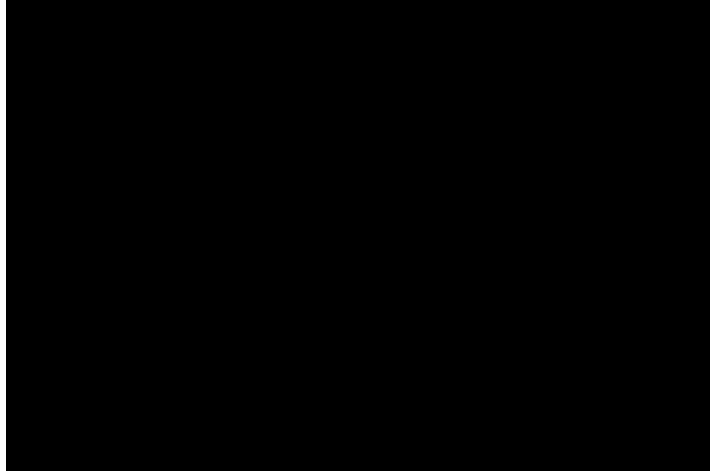
Figure 18: Temperature profile for one cycle.

Failure Criterion

Resistance increase is a common monitoring parameter for overall degradation of an interconnect structure. Resistance values will increase as a result of crack initiation, intermetallic compound formation or other thermal induced fatigue. Industry wide specification of interconnect failure criterion was adopted for this analysis. IPC 9701A/JEDEC-9702 define failed interconnects as exhibiting a 20% increase in resistance[36].

Temperature Cycling Equipment

Temperature cycling was conducted in a Tenny Environment TSJR air-to-air chamber. This equipment was selected for its ability to meet ramp rate specifications and internal chamber volume able to accommodate 100 samples.

Figure 19: Temperature cycling chamber. *TSJR by Tenny Environment*.

CHAPTER 5 Results

5.1 Accelerated Temperature Cycling (ATC)

5.1.1 ATC Overview

Temperature cycling accelerates fatigue within electronics devices. Within an entire assembly, interconnection bumps are of most concern for failure[37]. Expansion and contraction between interconnect bump, substrate and upper die caused by changes in temperature, creates plastic strain. Accumulated plastic strain adversely effects device operational lifetime. To further understand interconnect behavior resulting from changes in temperature, rigorous unbiased ATC was performed. Detailed sample tracking and resistance measurements of interconnect structures was collected at various intervals of cycling.

Temperature cycling (-55°C to 125°C, ramp rate of 15°C/min., 10 minute dwell at extremes) was performed on 100 bonded UBM samples for 3000 cycles. Thermal conditions were defined by consulting JEDEC A104E[30] and MIL-STD 883J[34] test standards. Temperature profile of one UBM sample is shown in Figure 20. Thermocouple monitoring demonstrated accurate ramp rate requirements as defined by JEDEC Standards[30]. Test Method A104E emphasizes ramp rate adjustment based on thermal mass of samples. Test samples used in this research possess low thermal mass and therefore can withstand fast ramp times. Temperature profile shown is not representative of 10 minute dwell times.
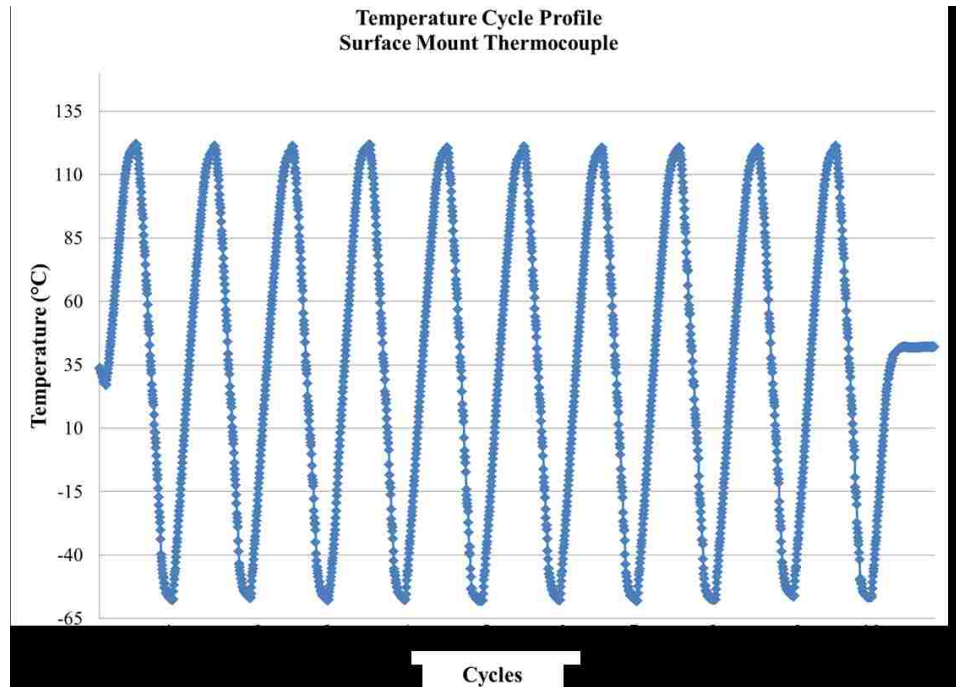
Figure 20: Thermocouple verification. Temperature profile of ATC conditions.

5.1.2 Electrical Resistance Measurements

Electrical resistance of serpentine structures was measured on all samples at various intervals of temperature cycling. Serpentine structures were selected for characterization because routing of electrical continuity provides optimal sampling of indium interconnects degradation. A single serpentine structure has 970 indium interconnections electrically in series. Data was collected for all 100 samples at intervals of 5, 500, 1000 and 3000 cycles. Failure criterion was predefined as 20% increase in resistance by IPC 9701A/JEDEC-9702 standards[36]. Serpentine resistances of 100 samples were measured four times. All measurements were conducted at room temperature.

Considerable amount of in-chamber temperature cycling was used to expose samples to harsh thermal conditions. Upon completion of 3,000 cycles, all samples had been exposed to 500 total hours at each temperature extreme. This totaled approximately 42

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days (1000 hours) of dwell time exposure at -55°C and 125°C. 42 days of total exposure does not include intermediate temperature exposure during ramps of cooling and heating.

	Cumulative Cycle Intervals				Dwell Time	
Temperature	5	500	1000	3000	Total	
125°C	0.83 hrs	82.5 hrs	83.3 hrs	333.3 hrs	500 hrs	21 days
-55°C	0.83 hrs	82.5 hrs	83.3 hrs	500 hrs	500 hrs	21 days

Table 8: Thermal dwell time exposure summary.

No failures were detected after completion of 3,000 cycles. Results show a trend of decreasing resistance over cycling within all UBM stacks examined. Figure 21 shows an overall summary of all UBM samples measured. Measurements presented are of serpentine structure. Figure 21 is organized by UBM stack and underfill or non-filled designation. Group means are represented by horizontal lines.
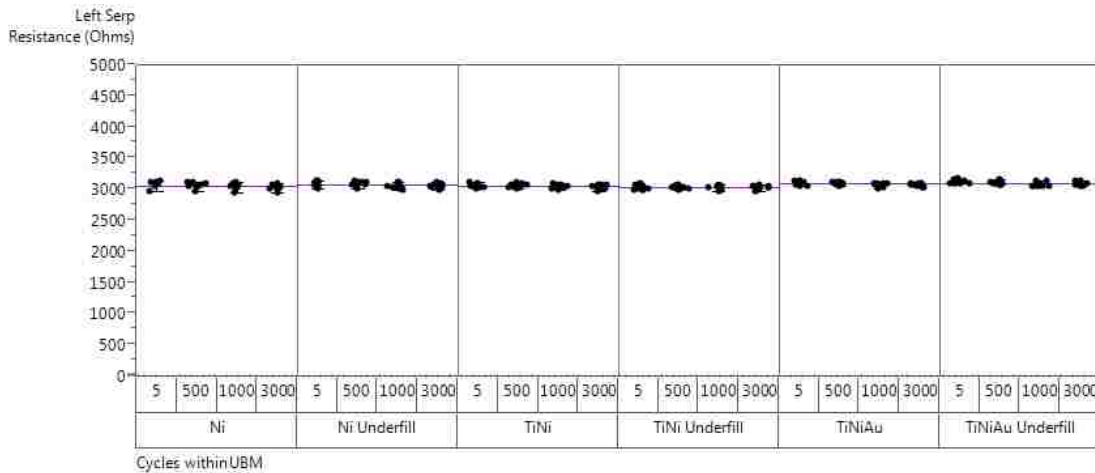
Figure 21: Resistances measurements of all UBM samples.

Further analysis of electrical resistance measurements is included below. It has been demonstrated that a decreasing resistance trend is present within each UBM sample set. Non-filled samples showed similar interconnect performance compared with underfilled samples.

Figure 22: Detailed variability chart of serpentine resistance.

Figure 23: Mean serpentine resistance by UBM and underfill condition.

Figure 24: Mean serpentine resistance by cycle.

Figure 25: Mean resistance UBM and cycle interactions.

5.1.3 ATC Discussion

Upon analysis of electrical testing data, it can be concluded that absences of failures is due to matched CTE values of silicon on silicon samples. The composition of CTE matched samples do not experience the damaging deformation effe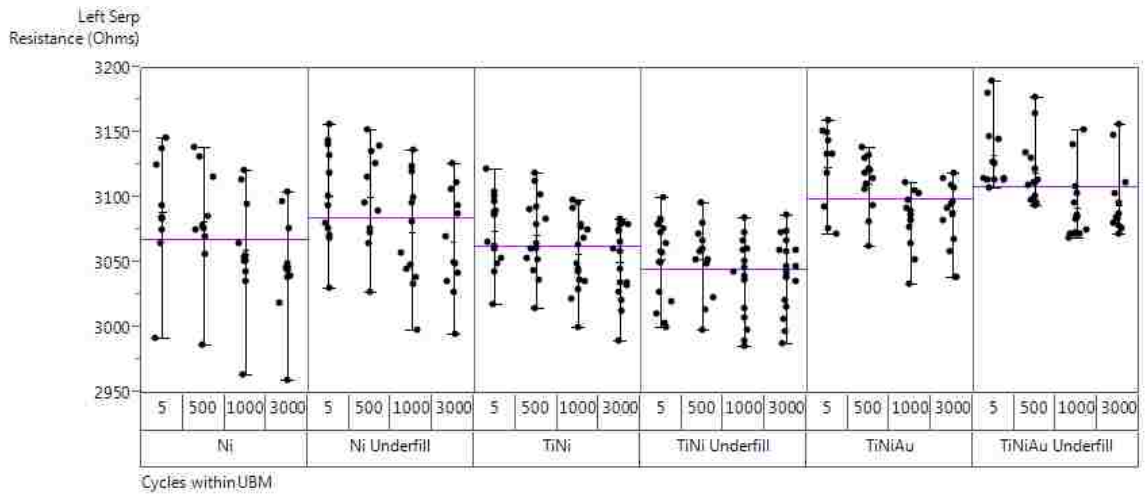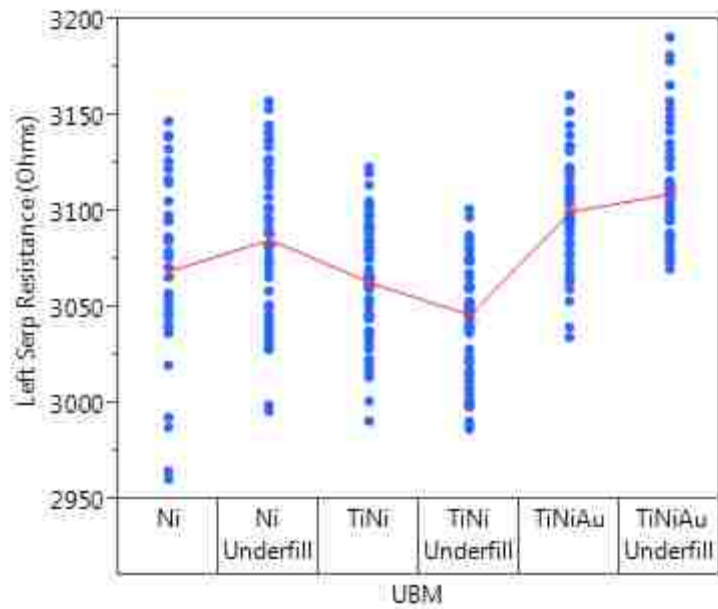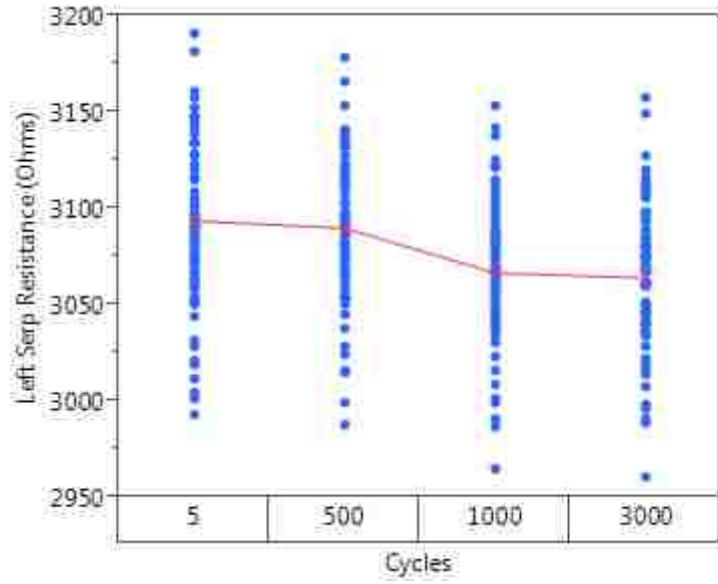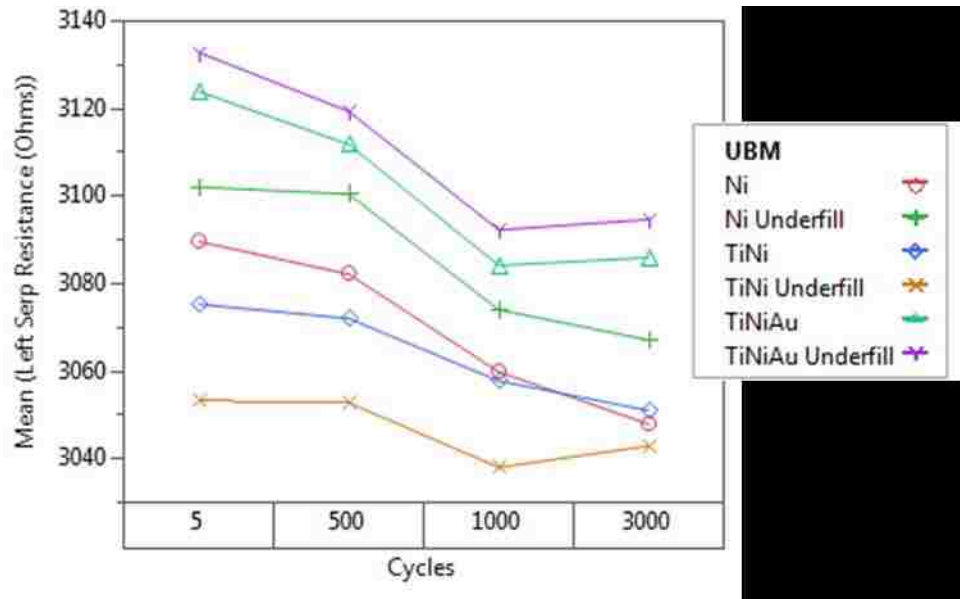cts commonly observed in temperature cycling. High quality processing methods of indium bump formation and bonding are also considered explanations for high yield sample set. Electrical testing measurements showed a trend of decreasing resistance, 2.52% decrease, in all samples through 3,000 cycles. Failure criterion, 20% increase in resistance, was not met and interconnects degradation was not observed. Further analysis of reliability methodologies pointed towards what is known as the burn-in effect[38]. Burn-in is a screening method to minimize early failure rates in semiconductor devices. During burn-in accelerated stresses are induced within samples and random failures are eliminated from the infant mortality region. In this thesis burn-in effects do not identify infant mortality failures. Confidence in sample operation without failure through "infant mortality" region is achieved.

5.1.4 Measurement System Variation Analysis

Resistance measurements are a key element of sample tracking and UBM/interconnect quality monitoring. A measurement system gauge study was used to assess capability of probe station. The intent of this analysis was to verify measuring techniques to be consistent and accurate between test samples.

Variation analysis was defined according to the Automotive Industry Action Group (AIAG) guidelines. Three randomly selected UBM bonded samples were measured over six consecutive days at random times. Resistance measurements were logged and used in

percent variance calculations. AIAG's Systems Analysis Reference Manual states that a measurement system is acceptable if the percentage of variance between samples is less than 10% [39].

Results show that probe station test system demonstrated a high degree of repeatability and reproducibility. Three randomly selected samples were analyzed by measuring the same serpentine structure on each sample. Analysis shows a mean percent variance of 1.24. This is within the limits of acceptability as defined by AIAG standards. Variation analysis data is summarized below:

Right Serp Resistance	31	252.32	251.99	252.20	252.34	252.10	252.25	0.02	−0.03%
Right Serp Resistance	16	264.14	263.80	263.99	263.99	263.90	263.91	0.01	−0.09%
Right Serp Resistance	24	247.97	247.65	247.86	247.86	247.73	247.87	0.01	−0.04%

Table 9: Probe station system variation analysis data.

System variation throughout the six day testing period is presented in the following three plots. Resistance measurement values along with percent change are charted below in Figures 26-28.

Ti/Ni/Au   UBM Die 31

Resistance ▬▬ **% Change**
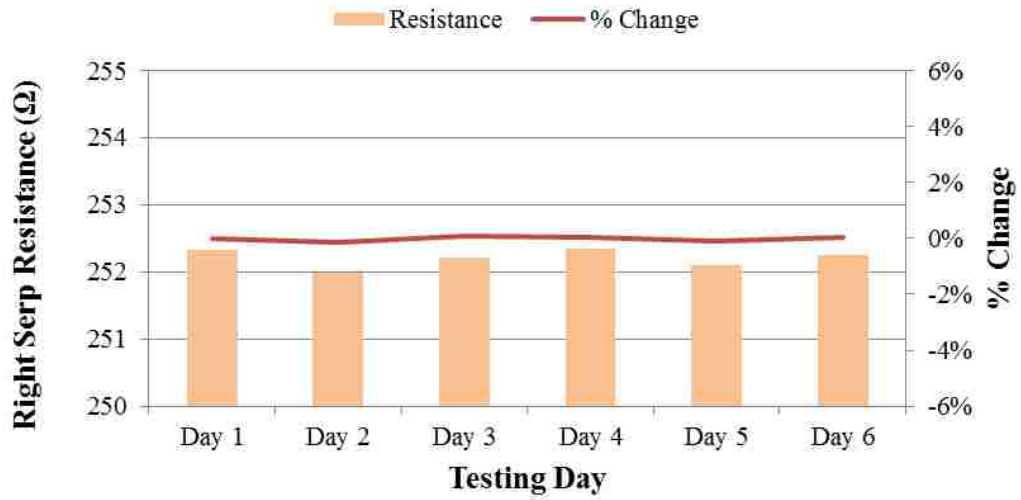
Figure 26: System variation measurements, TiNiAu UBM.

Ti/Ni   UBM Die 16

Resistance ▬▬ **% Change**
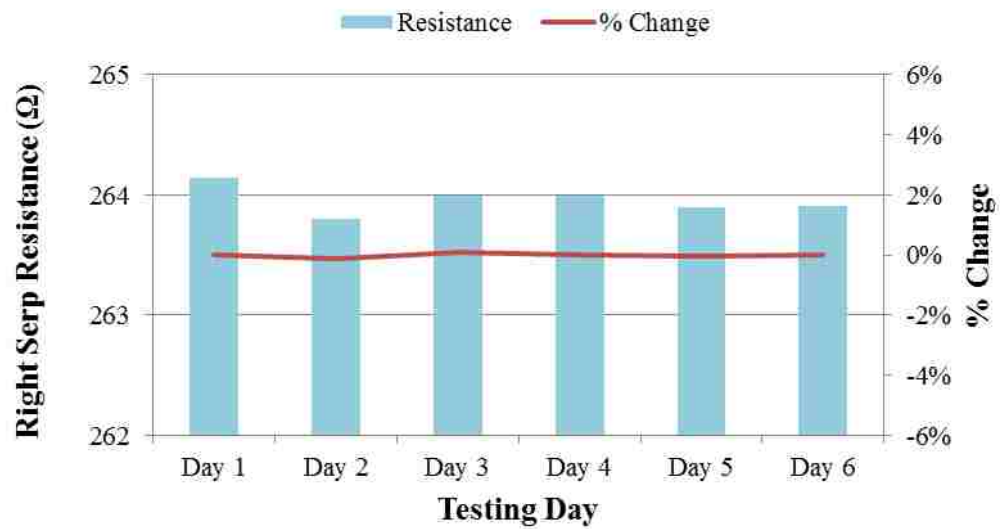
Figure 27: System variation measurements, Ti/Ni UBM.
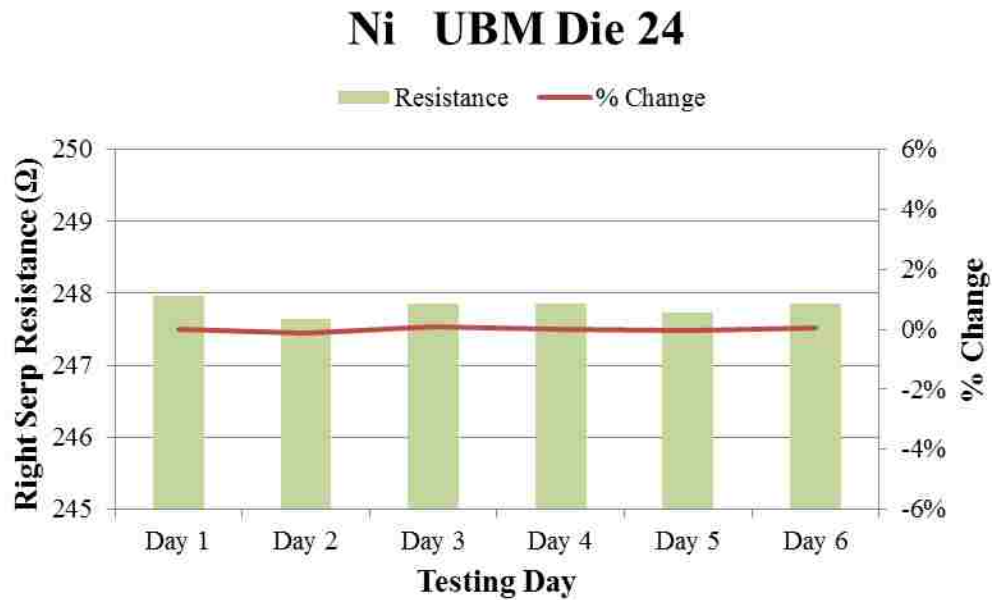
Figure 28: System variation measurements, Ni UBM.

5.2 Finite Element Analysis (FEA) - Single Indium Interconnect

5.2.1 FEA Model Creation and Mesh Parameters

FEA simulations are now presented to further understand behavior of the test samples when exposed to accelerated temperature cycling. All results presented in this section were calculated using ANSYS 15.0. The two dimensional plane strain model used for this analysis was comprised of two silicon substrates, indium bump and underfill epoxy material (Chipcoat U8443-14). Dimensions were representative of actual generated samples. Indium bump dimensions are defined in Figure 14 (20x20μm, 6μm tall). Silicon substrates were modeled 675μm tall. Underfill material is assumed to completely surround indium bump. Indium and underfill material were modeled as visco-plastic

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solids. Silicon bodies were modeled as elastic substrates. Non-filled and underfilled mesh element models are shown in Figure 29.
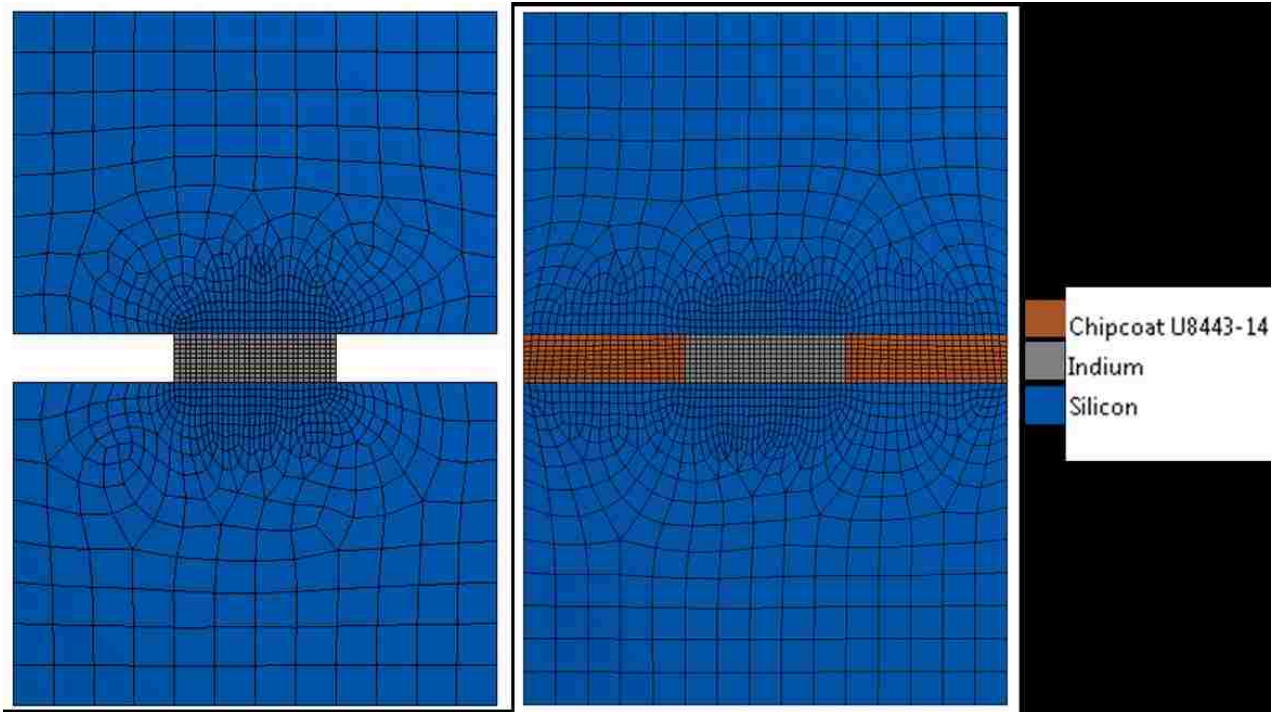
Figure 29: ANSYS mesh element model with material definitions.

Interactions between indium and underfill are the areas of most interest, therefore biasing techniques were used to reduce element density in non-critical areas. Edge sizing and mapped face meshing techniques were also employed to refine elements near material boundaries.

5.2.2 Engineering Data

Non-linear FEA simulation was used to calculate viscoplastic strain due to temperature cycling in a single indium interconnect. This analysis utilized ANSYS 15.0 software along with Anand parameters for pure indium material. Material properties used for simulations are organized in Table 10[20, 35, 40] .

Material	Density (g/cm^3)	CTE $(ppm/°C)$	Young's Modulus (GPa)	Poisson's Ratio	Conductivity $(W/m\,K)$
Silicon	2.3	2.49	112	0.28	105
Underfill Epoxy	1.5	42.0	6.5	0.4	-
Indium	7.3	24.8	12.7	0.45	83.7

Table 10: Material properties used in ANSYS simulation.

The Anand Viscoplastic Model has been presented in Chapter 3 of this thesis and has been reviewed extensively in the literature[41]. The primary governing equations are included below[43].

$$\dot{\varepsilon}_p = A\,exp\left(\frac{-Q}{RT}\right)\left[\sinh\left(\xi\frac{\sigma}{s}\right)\right]^{\frac{1}{m}} \tag{2}$$

$$s = s^* - \left[(s^* - s_o)^{1-a} + (a-1)\{(h_o)(s^*)^{-a}\}\varepsilon_p\right]^{\frac{1}{1-a}} \tag{6}$$

This model is used for modeling rate-dependent deformation, including creep and plastic strain. When properly applied, the Anand Model calculates plastic strain values throughout simulated temperature cycling. Plastic strain calculations are based on material dislocation deformation due to thermal cycling. Input values of pure indium and variable definitions are summarized below. ANSYS simulations couple these input variables and thermal conditions to calculate plastic strain values for indium material.

	s_o (Mpa)	Q/R (K)	A $(1/s)$	ξ	m	h_0 (MPa)	s^* (MPa)	n	a
Pure In	28.3	9369.7	2.33E8	49.97	0.2985	0.0	28.3	0.0	1.0

Table 11: Anand parameters of pure indium, Pure In [34, 35].

where

s_o = initial value of deformation resistance

$Q/R = Q$: activation energy, R: universal gas constant

$A =$ pre-exponential factor

$\xi =$ stress multiplier

$m =$ strain rate sensitivity of stress

$h_o =$ hardening/softening constant

$s^* =$ coefficient for deformation resistance saturation value

$n =$ strain rate sensitivity of saturation (deformation resistance) value

$a =$ strain rate sensitivity of hardening or softening

5.2.3 Viscoplastic Strain ANSYS Results

Equivalent plastic strain (EQPS) simulation for one cycle is shown in Figure 30. Contour plot of underfilled case shows maximum strain concentrations at outer corners of indium bump. Non-filled model results in lower EQPS values and negligible strain at bump center. Underfill material has a large CTE value compared to silicon or indium, therefore introduces plastic strain due expansion and contraction with changes in temperature.
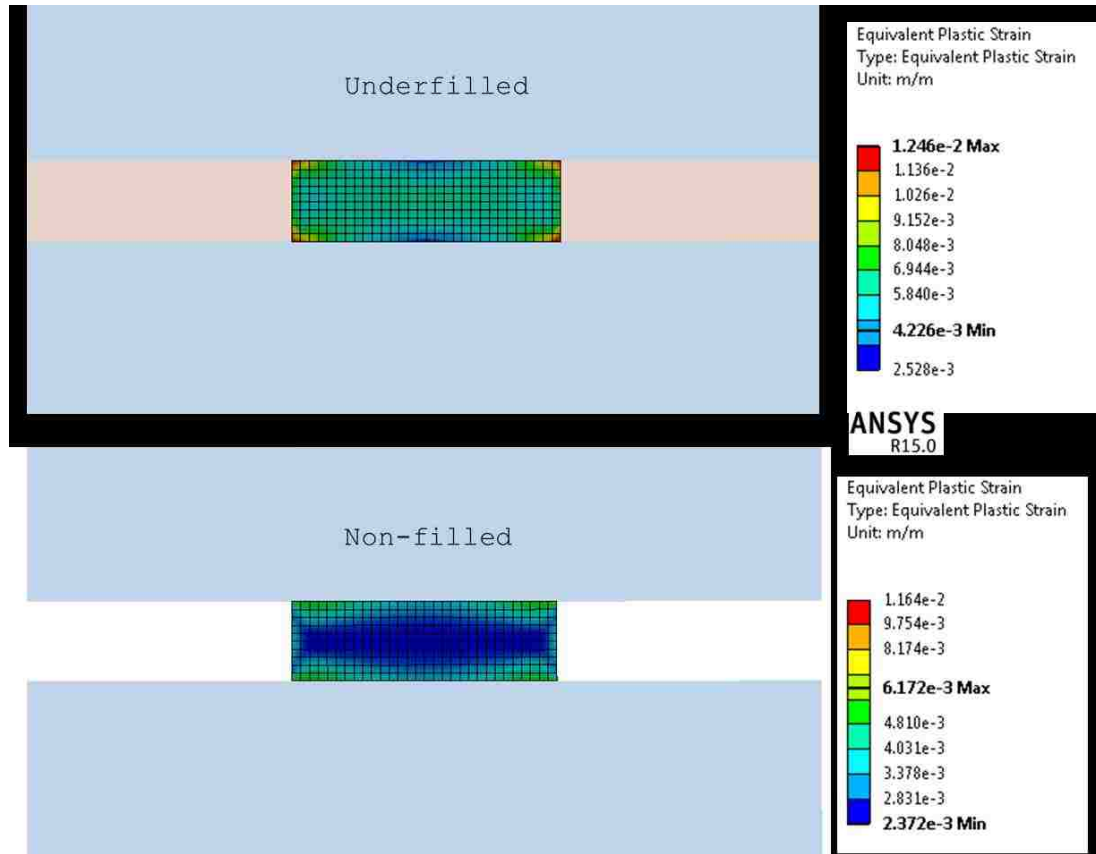
Figure 30: Maximum EQPS, single temperature cycle completion.

5.2.4 Mesh Convergence

Mesh convergence is a validation method used to verify FEA results to be accurate of realistic experimental conditions. To perform a convergence study multiple mesh sizing are used to monitor solution behavior. First, a coarse mesh of large element size is solved. Next, multiple intermediate mesh element dimensions are examined. If the contour plots of each solution are similar, mesh convergence is achieved. Element sizing examined for this convergence study were 1.2µm, 0.6 µm, 0.17 µm and 0.12 µm shown in Figure 31. Mesh convergence is achieved and results presented in the previous section are valid simulation parameters.
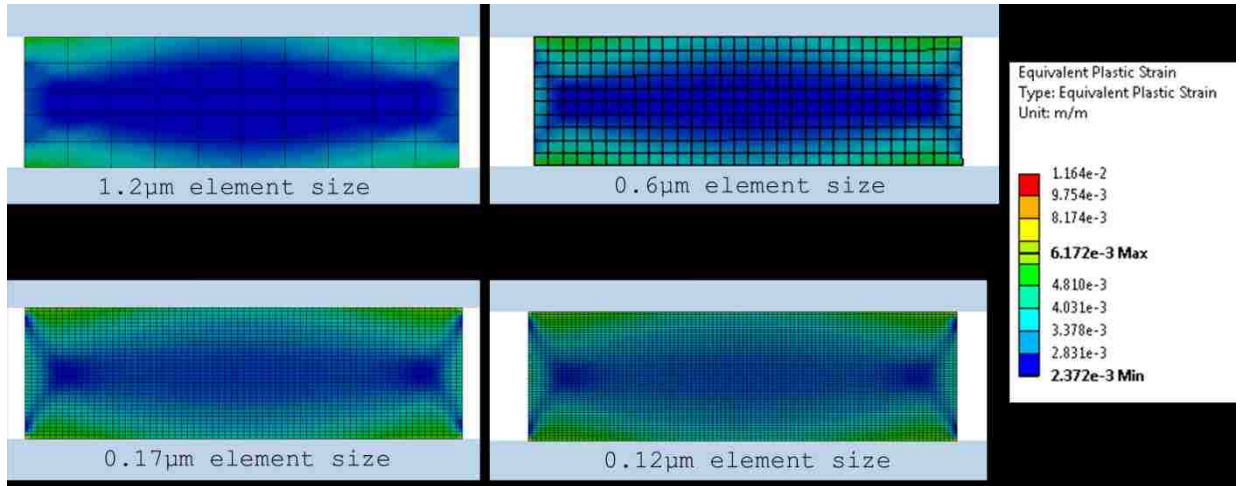
Figure 31: Mesh convergence study.

5.2.5 Verification of FEA Simulation

To verify ANSYS EQPS simulations a simplified thermal strain calculation was performed. Thermal strain for a two material assembly can be defined in Equation 7[44]:

$$\varepsilon = \Delta\alpha\Delta T \qquad (7)$$

where $\Delta\alpha$ = difference of Coefficient of Thermal Expansion $\left(\frac{ppm}{°C}\right)$

ΔT = change in temperature (°C)

Using Equation 7 along with CTE values of indium and silicon from Table 10 determines thermal strain, ε. The difference of CTE between indium and silicon was found to be $22.31\frac{ppm}{°C}$. Change in temperature, as defined by ATC conditions and FEA simulations, was 180°C. Using these values yields $\varepsilon = 4.01 \times 10^{-3}$. The strain level found using ANSYS simulation for non-filled condition, at locations away from the corners and adjacent to the interface with silicon, was consistent with this value.

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Numerical calculation compared to ANSYS result provides verification of strain behavior using these analysis techniques.

5.3 Fatigue Life Prediction

5.3.1 Coffin Manson Model

The Coffin Manson equation is a popular cycle-to-failure estimation, especially for leadless solder joint interconnections[27]. Conventional use of this equation uses cyclic strain range along with variables defined by thermal conditions. The simplified Coffin Manson relationship is presented again

$$N_f = \frac{1}{2}\left[\frac{\Delta\gamma}{2\varepsilon_f}\right]^{\frac{1}{c}}$$ (1)

where $\qquad$ N_f = cycles to failure

$\Delta\gamma$ = cyclic strain range (treated as maximum EQPS in one full cycle)

ε_f = fatigue ductility coefficient, $\left(2\varepsilon_f' \approx 0.65\right)$ [42]

c = fatigue ductility exponent

Fatigue ductility exponent is defined below:

$$c = -0.442 + -6 \times 10^{-4}T_m + 1.74 \times 10^{-2}\ln\left(1 + \frac{360}{t_d}\right)$$

Where $\qquad$ T_m = mean cyclic solder joint temperature (°C)

t_d = cycle dwell time (min)

Coffin Manson equation predicts failures to occur near 4,600 and 23,000 cycles for underfilled and non-filled samples, respectively. Cycle-to-failure estimations are substantially different between samples. Plastic strain is directly related to fatigue damage initiation and ultimate failure. Minor EQPS contributions from non-filled case means that fatigue damage is slow and thus longer predicted life cycle. Numerical values used for failure predictions are organized below.
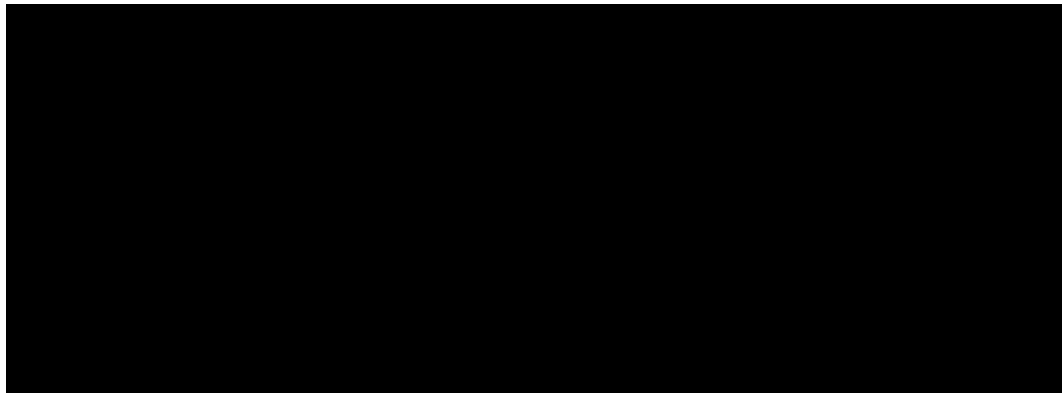

Table 12: Parameters used for cycle-to-failure estimation, underfilled and non-filled.

CHAPTER 6 Conclusions

In this chapter conclusions are made about the reliability of Under Bump Metallization (UBM) and indium interconnects within the early life (infant mortality) region of accelerated temperature cycling (-55°C to 125°C). The first part of this chapter discusses experimental accelerated temperature cycling (ATC) results. Next, FEA simulation results and their applications in fatigue life predictions are summarized. Additionally, contributions to reliability engineering of indium bumped flip chip devices are described. This chapter and thesis concludes with suggestions for future work.

6.1 Research Summary and Conclusions

Techniques for reliability characterization of early life failures of flip chip indium interconnected devices have been demonstrated. Results show that infant mortalities due to accelerated temperature cycling are not detected by electrical resistance measurements. It can be concluded that device metallization combinations do not present reliability concerns during early life, for temperature extremes examined.

Experimental Testing

100 double sided silicon based devices with indium interconnections were generated for experimental analysis. Samples contained three different UBM stacks (TiNiAu, TiNi, Ni). Electrical measurement test structures were present within every device. Test structures included daisy chains, serpentines and four-point kelvins, all accessible for

probing at the outer edge of device. These structures allowed for tracking of continuity and resistance of interconnects when exposed to aggressive ATC.

Unbiased ATC was used to analyze indium interconnect reliability. Thermal conditions were defined by consulting JEDEC A104E[30] and MIL-STD 883J[34] test standards. Samples were exposed to a total of 3,000 thermal excursions (-55°C to 125°C, 15°C/min. ramp rate, 10 minute dwell at extremes). Temperature cycling occurred in an air-to-air environmental chamber, out-of-chamber resistance measurements were collected at intervals of 5, 500, 1000 and 3,000 cycles.

Resistance fluctuations were used as monitoring parameters for overall degradation of interconnect structures. Failure criterion was defined as a 20% increase in resistance from Test Standard JEDEC-9702[36].

No failures were detected after completion of 3,000 cycles. Results show a trend of decreasing resistance through cycling within all UBM stacks examined. Both underfilled and non-filled samples demonstrated resistance decreases throughout temperature cycling.

Experimental Testing Conclusions

Early failures within test samples were not detected using experimental conditions previously discussed. Conclusions are summarized below.

1) CTE values of silicon-on-silicon test vehicles are matched. Thermal induced fatigue is not significant to initiate common failure mode of interconnects, such as crack propagation, shear stress.

2) For all three UBM metallization stacks, resistance did not increase during accelerated temperature cycling.

3) Confidence in device performance during early life failure region of the bathtub curve was achieved. Quality device processing and yield screening reduced probability for infant mortalities.

4) Addition of underfill epoxy to test samples does not change failure resistance during early life region.

FEA Simulation and Fatigue Life Prediction

A single bump two-dimensional plane strain ANSYS model was used for non-linear viscoplastic strain analysis. Two models were examined: underfilled and non-filled conditions. Simulation parameters were representative of experimental temperature cycling. The Anand Viscoplastic model was used in ANSYS simulations to calculate plastic strain rate of indium bump material. Maximum equivalent plastic strain (EQPS) values were computed and then used in a Coffin Manson cycle-to-failure equation. Cycle-to-failure (N_f) of non-filled and underfilled samples was examined.

ANSYS simulations calculated maximum EQPS values of 1.24% and 0.62% for underfilled and non-filled samples, respectively. Using these results, Coffin Manson equation predicted failures to occur near 4.6E+03 and 2.3E+04 cycles for underfilled and non-filled samples, respectively. Plastic strain accumulation remains slow for both simulation models.

FEA Simulation and Fatigue Life Prediction Conclusions

By using finite element analysis simulations and fatigue life equations, cycle-to-failure lifetime was estimated. Maximum equivalent plastic strain (EQPS) within a single indium interconnect was calculated using Anand parameters input into ANSYS software. ANSYS simulations were representative of ATC conditions. The results of fatigue life prediction are summarized below:

1) Simulation results show thermal induced plastic strain concentrations near outer corners of indium bump for underfilled samples. Non-filled simulations show significantly less EQPS due to CTE equivalence of lower and upper silicon.

2) Cycle-to-failure estimation using Coffin Manson equations predicted failures at 4,606 and 23,337 for underfilled and non-filled simulations, respectively. Large differences in predicted values are due to large CTE value of epoxy underfill material, compared to indium and silicon.

3) Local CTE mismatch of silicon and indium are present but are not able to overcome global CTE equivalence of silicon on silicon device. Expansion and contraction of upper and lower silicon negate significant plastic strain accumulation.

Contribution to Reliability Engineering

Rate-temperature fatigue modeling of indium interconnects is actively examined by researchers. Material complexities of three-dimensional assemblies create great challenges for experimental and simulation research. This thesis utilized experimental thermo-mechanical techniques and finite element analysis to gain understanding of indium behavior resulting from extreme temperature exposure. Test samples generated

for this work were examined for early life failure detection. This work presents methods to couple experimental temeperature cycling with simulation predictions for device perfomance validation.

6.2 Suggestions for Future Work

Upon completion of this research, future work has been identified which could lead to further reliability analysis of early life failures in flip chip devices. The two primary areas of future work are identified: experimental testing and simulation design.

The experimental test environment is a research proven analysis tool for thermo-mechanical reliability prediction. Early life failures are detrimental to high reliability components. To accelerate thermal environmental stresses, temperature cycling was completed for 3,000 cycles without failures. The next research step is to extend cycling conditions for longer intervals. By doing so, fatigue accumulation can be further monitored by electrical resistance measurements. The identified continuation of this work is presented below.

- Expose samples to extended cycling conditions. In the current work, early life failures are examined through completion of 3,000 cycles. No failures were detected during testing. If longer cyle exposure is executed, failures from thermal induced fatigue may initiate.
- Cross-section samples for high resolution imaging and elemental mapping. Cross section analysis provides enhanced monitoring of potential failures. Scanning Electron Microscopy is effective for monitoring intermetallic formation and

interconnect crack propagation. Element mapping can aid in observing diffusion of metals into unwanted regions.

Simulation based design is a powerful engineering tool when testing conditions are extreme or costly to perform. By using finite element models of electronic components subjected to environmental conditions failure mitigation can be achieved.

- Higher fidelty FEA model of array of indium interconnections. Improved modeling will incorporate cumulative strain accumulation due to multiple interconnection structures.
- Further analysis of rate-temperature effects of underfill epoxy material. Considerable differences in cycle-to-failure results would arise from improved EQPS calculations.

REFERENCES

1.   International Technology Roadmap for Semiconductors, *ITRS Roadmap 2012 Overview*, in *2012 Update*. 2012.

2.   Jaeger, R.C., *Introduction to Microelectronic Fabrication: Volume 5 of Modular Series on Solid State Devices (2nd Edition)*. Vol. 5. 1988: Addison-Wesley

3.   Elenius, P., Levine,L, *Comparing Flip-Chip and Wire-Bond Interconnection Technologies.* Chip Scale Review, 2000.

4.   A. C. Fischer, N.R., G. Stemme, J. G. Korvink, *Unconventional Applications of Wire Bonding Create Opportunities for Microsystem Integration.* Journal of Micromechanics and Microengineering 2013.

5.   Yihui Wang, *Wire Bonding*, in *Chip with ball wire bonding*. 2009. August 21, 2014; Availabe from: http://wirebonding.blogspot.com/2009_11_01_archive.html.

6.   Paul A Totta, S.K., *Microelectronics Packaging Handbook*. Chip-To-Package Interconnections, ed. R.R. Tummala. 1997: Springer US.

7.   Totta, P., *History of Flip Chip and Area Array Technology*, in *Area Array Interconnection Handbook*, K. Puttlitz and P. Totta, Editors. 2001, Springer US. p. 1-35.

8.   Wolf, J., *Flip chip bumping technology-Status and update.* 2006.

9.   Institut, F.B. *Packaging of GaN power transistors*. 2015 April 30, 2015; Available from: http://www.fbh-berlin.com/publications/frequent/03-power-electronics/topic-power-electronics.

10.   Puttlitz, K.J. and P. Totta, *Area Array Interconnection Handbook*. 2001: Kluwer Academic Publishers.

11.   Jittinorasett, S., *UBM Formation on Single Die Dice for Flip Chip Applications*, in *Department of Electrical Engineering*. 1999, Virginia Polytechnic Institute and State University: Blacksburg, Virginia.

12.   Wolf, S., *Silicon Processing for the VLSI Era, Vol. 2: Process Integration*. Vol. 2. 1990: Lattice Press.

13.   Dusek, M., *Wettabillity - SnPb and Lead-free Solders*. Materials Centre National Physical Laboratory.

14.   Sung K Kang, P.G., Da-Yuan Shih, *An Overview of Pb-free, Flip-Chip Wafer Bumping Technologies*. 2008, IBM

15.   Gasse, A., et al. *Assessment of advanced anisotropic conductive films for flip-chip interconnection based on Z axis conductors*. in *Nuclear Science Symposium Conference Record, 2003 IEEE*. 2003.

16.   Sun, M., *Conductivity of conductive polymer for flip chip bonding and BGA socket.* Microelectronics Journal, 2001. p. 197-203.

17.   Miller, L.F., *Method of joining a component to a substrate*. 1969, Google Patents.

18.   Degani, Y. and D.P. Kossives, *Flip chip bump bonding*. 2001, Google Patents.

19.   Chang, R.W. and C.P.M.E. University of Maryland, *Influence of Cryogenic Temperature and Microstructure on Fatigue Failure of Indium Solder Joint*. 2008: University of Maryland, College Park.

20.   Indium Corporation. *Physical Constants of Pure Indium*. 2015 [cited 2015 February 17]; Available from: http://www.indium.com/metals/indium/physical-constants/.

21.   Henini, M., *Handbook of Infrared Detection Technologies*. 2002: Elsevier.

22.   Darveaux, R. and I. Turlik. *Shear deformation of indium solder joints*. in *Thermal Phenomena in Electronic Systems, 1990. I-THERM II., InterSociety Conference on*. 1990.

23.   Darveaux, R. *Effect of simulation methodology on solder joint crack growth correlation*. in *Electronic Components; Technology Conference, 2000. 2000 Proceedings. 50th*. 2000.

24.   Breniere, X., *Uniting IR detectors for tactical and space applications: a continuous cycle for reliability.* SPIE Proceedings 2009. 7298: p. 12.

25.   IPC, *Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments*, in *IPC-SM-785*. 1992.

26.   Lee, W.W., *Solder joint fatigue models: review and applicability to chip scale packages.* Microelectronics Reliability, 1999. 40: p. 231-244.

27.   Pang, J.H.L., *Lead Free Solder: Mechanics and Reliability*. Theory on Mechanics of Solder Materials. 2012, Springer Science Business Media.

28.   Steinberg, D.S., *Vibration Analysis for Electronic Equipment*. 1988: Wiley.

29.   IPC, *IPC-9701*, in *Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments*. 2002, IPC: Northbrook, Illinois.

30.   JEDEC, *JEDEC Standard*, *Temperature Cycling*, in *Test Method A104E*. 2014, JEDEC Solid State Technology Association: Arlington, VA.

31.   Department of Defense, *Test Method Standard Microcircuits-Thermal Shock*, in *MIL_STD-202 Thermal Shock*. 1984.

32.   JEDEC, *JEDEC Standard*, in *Thermal Shock-JESD22-A106B*. 2004, JEDEC Solid State Technology Association: Arlington, VA.

33. JEDEC, *JEDEC Standard*, in *Thermal Shock-JESD22-A106C*. 2004, JEDEC Solid State Technology Associsation: Arlington, VA.

34. Department of Defense, *Test Method Standard Microcircuits*, in *MIL-STD-883J-Thermal Shock*. 2013.

35. Namics Corporation. *Flip Chip Underfill(UF)*. 2015 [cited 2015 May 11,2015]; Available from: https://www.namics.co.jp/e/product/chipcoat01.html.

36. IPC/JEDEC, *Monotonic Bend Characterization of Board-Level Interconnects*, in *Test Board Daisy-Chain Links*. 2004, Solid State Technology Association.

37. Steinberg, D.S., *Preventing thermal cycling and vibration failures in electronic equipment*. 2001: J. Wiley.

38. Taeho, K., K. Way, and W.T.K. Chien, *Burn-in effect on yield.* Electronics Packaging Manufacturing, IEEE Transactions on, 2000. 23(4): p. 293-299.

39. AIAG, *Measurement Systems Analysis, Reference Manual, 3rd. ed.* 2003, Automotive Industry Action Group Southfield, Michigan.

40. MatWeb. *Material Property Data, Silicon Si*. 2015 [cited 2015 May 31]; Available from: http://www.matweb.com/search/DataSheet.aspx?MatGUID=7d1b56e9e0c54ac5bb9cd433a0991e27&ckck=1.

41. Johnson, Z.E., *A Compilation of Anand Parameters for Selected SnPb and Pb-free Solder Alloys.* University of Minnesota. 2012.

42. Lee, O., Y. Park, and D. Kim, *Reliability estimation of solder joints under thermal fatigue with varying parameters by using FORM and MCS.* Journal of Mechanical Science and Technology, 2008. 22(4): p. 683-688.

43. Motalab, M. et al. *Determination of Anand constants for SAC Solders using Stress- Strain or Creep Data.2012, Center for Advanced Vehicle Electronics, Auburn University.*

44.   R.E. Taylor, CINDAS Data Series on Materials Properties, *Thermal Expansion of Solids*, Vol 1-4, ASM International, 1998.