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Richard Johnson

Richard William Johnson
Candidate

Mechanical Engineering
Department

This thesis is approved, and it is acceptable in quality and form for publication:

Approved by the Thesis Committee:

Dr. Yu-Lin Shen , Chairperson

Dr. Peter Vorobieff

Dr. Zyad Leseman

Numerical Analysis of TSV/Micro-bump Deformation due to Chip Misalignment and Thermal Processing in 3D IC Packages

By

RICHARD WILLIAM JOHNSON

BACHELOR OF SCIENCE

THESIS

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Numerical Analysis of TSV/Micro-bump Deformation due to Chip Misalignment and Thermal Processing in 3D IC Packages

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Richard William Johnson

B.S., Mechanical Engineering, University of New Mexico, 2006

M.S., Mechanical Engineering, University of New Mexico, 2012

Abstract

Three-dimensional (3D) stacking of integrated circuits (ICs) is an enabling technology in the advancement of the microelectronics industry. 3D stacking enables increased device density per volume and improved electrical performance through short vertical interconnect paths. Mechanical reliability of 3D IC packages is critical due to the widespread use of electronic devices. Misalignment induced shear deformation of the through-silicon vias (TSV) and solder micro-bumps are simulated through an applied shearing action. Thermal effects due to coefficient of thermal expansion (CTE) mismatch during processing are also studied to provide trends of stress and deformation fields. Reliability of the 3D chip stack, TSV and solder micro-bump are assessed by examining local stresses and the buildup of plastic strain through series of parametric two-dimensional (2D) and 3D finite element method (FEM) simulations. A special case when the solder joint is transformed into an intermetallic compound is also examined. Misalignment induced shearing strongly influences stresses and deformation in and around the micro-bump. Thermal CTE mismatches influence stresses and deformation in the entire 3D chip stack and in the TSV far away from the joint. Shortcomings of the 2D plane strain model for examining CTE mismatch and measuring buildup of plastic strain in the joint are also discussed.

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Chapter 1 Introduction

In 1965, Gordon Moore, the director of research and development at Fairchild Semiconductor, predicted the number of components per IC to double every two years [1]. Moore thought that this trend would hold constant over the next ten years, Figure 1, based on trends from the invention of the transistor through 1965 [1]. Amazingly, over the next forty years Moore's prediction has held remarkable true [2].

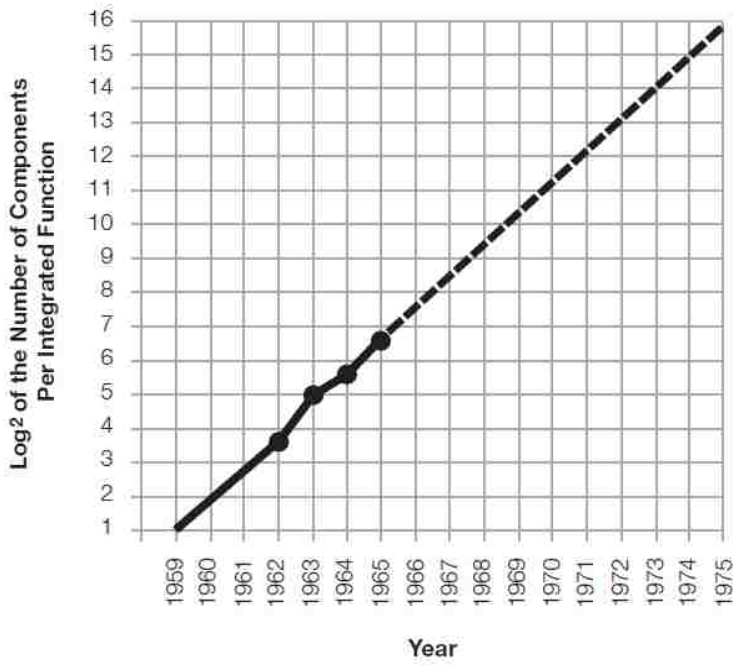

Figure 1: Moore's original prediction of the doubling of components per IC published in *Electronics,* 1965 [1].

Over the past two decades, from 1990 to 2010, the number of components on memory devices increased from 1 million to 1 billion [2]. This increase has occurred at a

remarkable rate. Until now, chip manufacturers have been able to follow Moore's prediction by increasing the density of components in 2D IC packages. The microelectronics industry has not only succeeded in increasing density, but also the functionality of 2D ICs by reducing the lateral chip dimensions resulting in many new applications [3]. These approaches have pushed the performance of the IC forward, but have not addressed the subsequent complexity of electrical interconnects, which is exacerbated by the increase in component density, Figure 2(a). As the physical limits, or at least economical considerations, of miniaturization are approached, industry is looking to 3D IC packaging as the new direction [2]. An emerging technology that enables the continued advancement of microelectronics devices, in both electrical performance and reduced size, is the 3D IC. The 3D IC with vertical TSV interconnects is a key enabling technology that can further the advancement of microelectronics devices, Figure 2(b). Unique advantages include the increase of device density per volume, utilization of short vertical interconnection for improved electrical performance, and the capability of integrating multiple functions into a single package [2-4]. The signal path between stacked silicon chips is provided by the TSV and not by complex external wire bonds. Multiple levels of interconnects are required to connect the 2D chip with the outside world which in turn dwarf the size of the actual device layer [3]. Parasitic electrical losses, due to interconnect resistance and capacitance, are reduced by the short vertical interconnects resulting in higher signal speed and reduced power consumption [5].

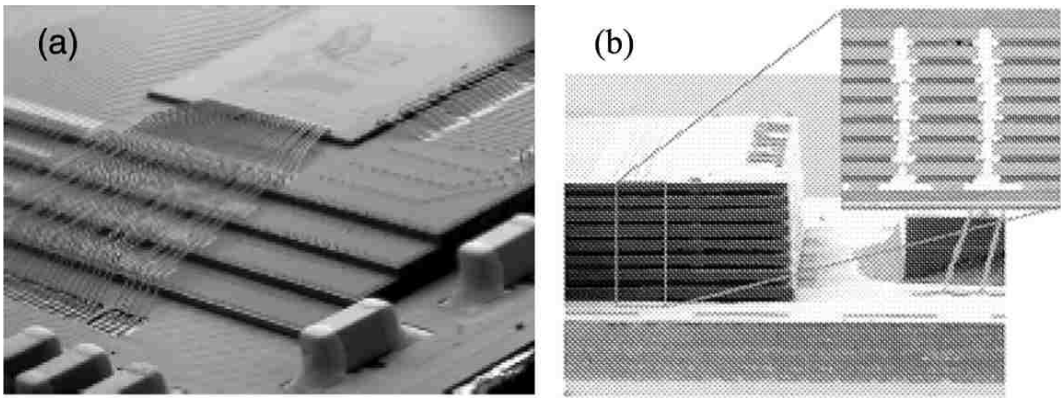

Figure 2: (a) Stacked package of 2D planer ICs with interconnect wires shown. (b) 3D IC package with TSV electrical interconnects [3]

After a number of years exploring 3D IC technology, industry is pushing the 3D IC to the market. Commercial products utilizing 3D IC and TSVs are starting to appear. Developments in 3D IC and TSV interconnect technology are being made at a frantic pace by universities, research institutions and by many of the major semiconductor companies including Samsung, IBM, Intel, Nokia, and St-Ericsson [3, 6-7]. Many industry experts predict that this year will be the debut of 3D ICs with TSV technology [6]. Micron, a manufacturer of memory, with a consortium that includes IBM, has announced a hybrid Memory Cube (HMC) that claims to increase performance 15 times, reduce power consumption by 70% all within 90% less space, Figure 3 [8]. While these claims seem overly optimistic, the numbers point to the innovative promise that chip manufacturers hope for in the 3D IC and TSV.

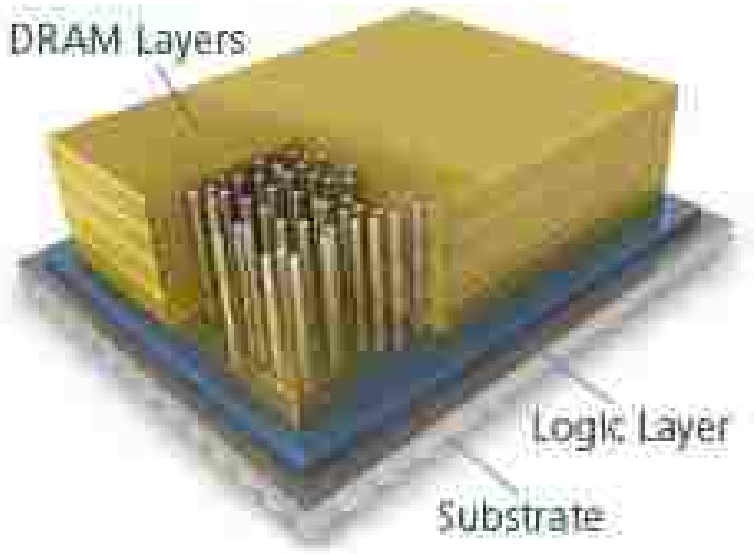

Figure 3: Hybrid Memory Cube (HMC) a high-density memory system using 3D IC packaging and TSV interconnect technology [8].

In 2011, Samsung announced the development of a 32 gigabyte (GB) double data rate-3 (DDR3) memory using 3D IC and TSV technology, Figure 4. Samsung's claims were more modest than IBM with a 70% increase in speed and 30% decrease in power consumption [9]. Some products using 3D IC technology with TSV interconnects may already be available to the consumer.

Figure 4: Samsung's 32 gigabyte DDR3 memory module with 3D TSV packaging technology [9].

It has been reported that IBM has already been manufacturing the 3D IC for consumer electronics devices utilizing low density TSV interconnects [6]. It is clear that the 3D IC with TSV interconnects is the next major innovation in the microelectronics industry. It is also interesting to ask how Moore's law will hold as industry embraces this enabling technology in a move to 3D.

Chapter 2 Literature Review on Thermo-Mechanical Issues in 3D ICs

Figure 5 shows a schematic of stacked Si chips containing copper (Cu) TSVs. In current technology the diameter of individual micro-bumps between chips is on the order of 10 to 20 μm [2]. The joint can also exist in the form of Cu pillars. Larger solder bumps are used for joining the packaging substrate and the chip stack. Underfill material may be applied, and there are adjacent support and heat conducting structures not explicitly depicted in Figure 5.

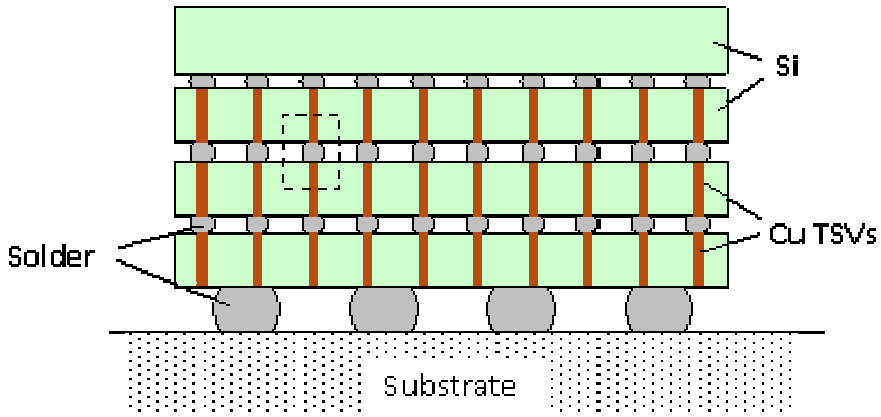

Figure 5: Representative 3D integration scheme showing vertical stacking of Si chips containing copper TSVs. The schematic is not to scale, and the possible underfill material and other peripheral structures are not included.

Very little experimental data is currently available for the reliability of the 3D IC [2]. The focus of research has been numerical modeling of the thermo-mechanical behavior of 3D ICs. Successful implementation of the 3D IC will rely upon the control of thermo-mechanical stresses in the Cu TSV and surrounding Si [10]. Another important issue that

needs to be addressed affecting the 3D IC is chip misalignment. Alignment of TSVs among several stacked chips is non trivial [2]. The effects of chip misalignment have not been systematically studied. It is known that by introducing TSVs into a Si substrate, warpage will occur due to CTE mismatch and internal stresses [2]. As the number of chip stacks increases this problem is only exacerbated. Warpage of the chip stack causes difficulty in alignment but also results in a shearing action [2]. Simulations cooling a 3D IC package show chip warpage; a phenomenon verified experimentally [11].

Joule heating has also been identified as a major problem facing the 3D IC [2]. Removing heat from ICs has been of great concern since the invention of the transistor, a fact reiterated by Moore in his 1965 paper [1]. Joule heating occurs from currents flowing through non-ideal, or resistive, circuitry of the IC. These losses are often referred to as I^2R losses in electronics, where I is the current and R is the resistance of the circuit. In the Si chip, heat is generated in the transistor, the contact metallization, the multi-layered interconnect and in the solder joints [2]. As much as 50% of the power in microprocessors is dissipated through electrical losses in interconnects [3]. Since the total heating is a function of the number of devices and interconnects, heat generation in a 3D IC can be larger by the number of chips stacks that of a 2D counterpart [2]. Heat dissipation in the 3D IC presents the new set of challenges. Due to the reasons for 3D stacking, the thermal issues become more serious [12]. In the 2D IC package, the heat transfer path is relatively thin. Since 3D packages are no longer planar, heat transfer must now occur through a layering of dielectric materials with typically poor values of thermal conduction [2]. Heating in the 3D IC is extremely serious and must be efficiently managed to control chip performance, and mitigate the possibility of damage [2].

Due to the large CTE mismatch between the Cu TSV and Si chip, thermal stress induced failure is an important issue [13]. The CTE of Cu is approximately five times larger than that of the surrounding Si. As a result, thermal stresses form when the chip stack heats or cools. Thermal stresses exist at room temperature since the IC is annealed at a temperature around 250 °C [13-17]. As the chip stack heats or cools during processing and operation, significant stresses exist in and around the TSV Si interface. Some of the thermo-mechanical issues readily identified are cracking of the Si chip, cracking of the TSV and interfacial delamination [12]. Experimental results using X-ray microdiffraction, show high shear and hydrostatic stresses that can lead to debonding, cracking, as well as plastic damages [10]. Many of the thermo-mechanical studies of TSVs are limited to free standing wafers and not an integrated package [11]. It is shown that thermal stresses in the TSV are actually lower in the IC package then in a stand alone wafer [11] Since more realistic geometry is simulated in the 3D package, possible underfill and the effect of neighboring TSVs, the results from these studies offer better thermo-mechanical predictions.

A number of numerical studies have examined the effect of TSV geometry to identify potential failure sites and mechanisms [5, 10-25]. Thermo-mechanical stresses can cause interfacial debonding, cracking of Si and plastic deformation in the Cu TSV and solder joint, which can lead to ductile failure [26]. Optimization of the 3D IC is essential to avoid short fatigue life in the TSV interconnect [18]. In general, fast temperature changes cause fracture at the TSV Si interface while repeated thermal cycling, due to the buildup of plastic strain, results in ductile failures [22, 26]. Rapid thermal cycling of the TSV limits the inelastic deformation of the TSV through strain rate hardening [22]. Geometry

and materials selection strongly influence the durability of the 3D IC [18, 12]. The properties and thickness of the underfill layer are the most important factors influencing the reliability of the solder joint [18]. Underfill acts as a buffer against thermal strains in the 3D IC package [13]. The TSV diameter is the most influential parameter determining the reliability of the Cu TSV and thus surrounding Si [13, 18]. The strength of the TSV and chip is dependant upon the TSV pattern and density [2].

Stresses in the Si chip substrate are known to affect the electron mobility and thus the performance of the IC [10, 13]. The region near the TSV where electron mobility of devices could be degraded is called the "keep away zone" [13]. A number of studies have considered the effects of die thickness, TSV diameter, micro-bump diameter, TSV height, underfill thickness and overall spacing of interconnects on the stresses in the 3D IC [13, 18, 20]. It is critial to understand the stress distributions near the surface of the Si where devices are typically located [13, 20]. Measurements, using X-ray mircodiffraction, of stress/strain near the Cu TSV and Si interface indicate a "keep out zone" of approximately 17 μm, which corresponds to the radius beyond which the strain is essentially zero [10]. It is reported that a 7% change in the electron mobility results from a 100 MPa stress in the Si chip [13]. 3D modeling is needed to capture the nature of the stress field near the Si surface around the TSV [20]. As was seen as a primary influence on the reliability of the Cu TSV, the diameter of the micro-bump greatly influences the "keep away zone" [13].

It is important to model plastic deformation of metals in device structures to more accurately predict stress distributions and damages [21]. Allowing plastic deformation limits the buildup of unrealistically high stresses in ductile materials. Better physical

models, taking into account the microstructure, are also needed to improve the reliability of computed stresses in the 3D IC [3].

Chapter 3 Two-Dimensional Analyses[1]

3.1 Introduction

As mentioned in Chapter 2, an important challenge in 3D ICs is the accurate alignment of the chip stack, which can be exacerbated by chip warpage. Misalignment of chips inevitably subjects the micro-bumps to shear deformation [2]. The behavior of the bonding layer between already-stacked chips is in fact one of the most difficult issues during subsequent bonding processes [27].

In recent years, intensive research efforts on thermal stress related issues in TSV structures have been reported [5, 10-25]. The effect of chip alignment, on the other hand, has not been systematically studied. The present chapter is thus devoted to misalignment-induced mechanical deformation in and around the TSV/micro-bump. Numerical analyses on a model joint structure (Figure 6, perceived as a representative area segment of the chip stack in Figure 5) are conducted using FEM. The 2D model uses an idealized layout to capture the basic physical features of the Si chip, TSV, solder material and underfill (when existent) under misalignment-induced shear. Three-dimensional simulations will be the focus of Chapter 4. We seek to parametrically explore the trend of stress and deformation fields as affected by the geometry and material. The specific objectives include:

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[1] Compiled from a journal paper submitted to Microelectronics Reliability, accepted April 2012 [26].

- To examine how the local TSV/micro-bump assembly responds mechanically to the overall shear loading.
- To study the effect of solder thickness in the micro-bump and its damage implications.
- To compare the deformation characteristics with and without underfill between chips.
- To compare the evolution of stress and deformation fields caused by mechanical shear and thermal loading.

3.2 Numerical Model

3.2.1 Model Description

Figure 6 shows the FEM model geometry. The simulation domain ABCD may be viewed conceptually as a representative area segment highlighted by the dashed rectangle in Figure 5 The model is symmetric about the center vertical and horizontal lines, with an overall dimensions of AB = 100 μm and AC = 100 μm. The copper TSVs in the upper and lower Si chips are connected through a micro-bump (also referred to as "joint" in this thesis) of thickness (H) 20 μm and diameter (w) 20 μm. The micro-bump is assumed to have straight side walls and a Cu-solder-Cu structure. The solder thickness h is varied in the study between 5, 10 and 20 μm, the last case being that there is no Cu material in the micro-bump. In actual devices, if a prolonged post-soldering annealing is carried out, the solder layer may be transformed entirely into an intermetallic material [2]. Therefore, in

one particular case of the present modeling, we replace the entire 5 μm-thick solder by an intermetallic material. Outside of the micro-bump and between the chips, there is a possible underfill layer as depicted in Figure 6. The influence of underfill in the bonded chip structure is specifically studied. The TSV diameter (d) is taken to be 10 μm.

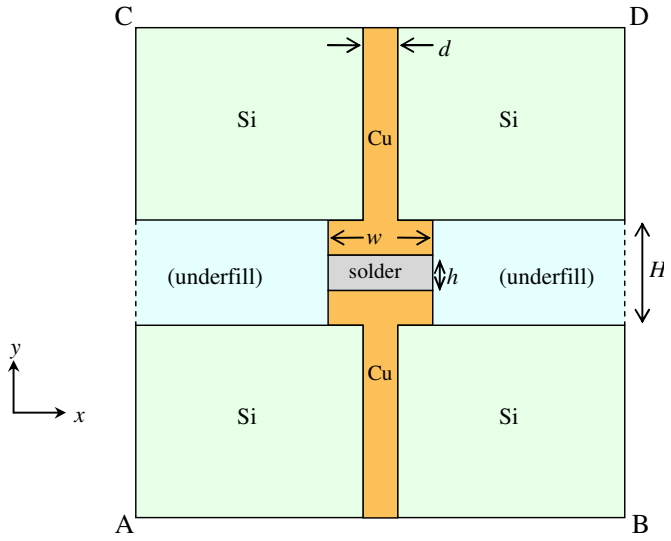


Figure 6: Material layout used in the finite element modeling. The domain ABCD is perceived to be a representative area segment highlighted in Figure 5. In its un-deformed configuration, the structure is symmetric about the center vertical line (centerline along the Cu TSVs) and center horizontal line (middle cut through the solder). The fixed dimensions used in the modeling are: AB = AC = 100 μm, H = 20 μm, d = 10 μm, w = 20 μm. Different solder thicknesses h are considered.

Misalignment-induced shear deformation is modeled through a prescribed shear action under the plane strain condition. The bottom boundary AB is taken to be stationary, while the top boundary CD is displaced along the x-direction for up to 1 μm (presumably the misalignment distance). The left and right boundaries are not constrained. Note that the current loading mode and boundary conditions do not give rise to a strict periodic deformation field representative of a true composite structure with repeated unit cells.

However, since the main deformation action is centered around the micro-bump region, which is reasonably away from the boundaries of the model, key deformation features can still be obtained from the current approach. Moreover, by comparing results from the various scenarios within the present modeling framework, useful trends about overall mechanical response, local deformation and damage propensity can be obtained. We also note that the present modeling focuses only on a representative micro-bump and its vicinity inside a chip stack, Figure 5, so the misalignment effect on the packaging substrate is excluded from the investigation.

For gaining insight on how deformation caused by overall shear differs from that caused by thermal expansion mismatch, we also consider pure thermal loading using the same model depicted in Figure 6. A cooling history from 250 to 20°C is simulated, where 250°C is taken to be the stress-free temperature [13-17]. During thermal loading the left boundary AC is prohibited to displace in the *x*-direction but tangential movement of its nodal points is allowed. The bottom boundary is prohibited to displace in the *y*-direction but tangential movement of its nodal points is allowed. The top (CD) and right (BD) boundaries are constrained to remain horizontal and vertical, respectively, but otherwise can adjust their positions. The boundary conditions thus ensure that the domain ABCD is a true unit cell of the periodic composite structure in the x-y plane [28], although the 2D plane strain condition is still imposed.

The finite element program Abaqus (Version 6.10, Dassault Systemes Simulia Corp., Providence, RI, USA) is employed for the computation. The model contains a total of 10,000 four-noded elements, with a finer mesh size around the center (joint) region. An assessment of numerical convergence led to mesh refinement around the joint in the

regions of high strain gradient. The material properties used as input parameters in the modeling are listed in Table 1. The Si, underfill and intermetallic materials are assumed to isotropic, linearly elastic solids [28-30]. Specifically, the intermetallic properties are based on those of the Cu_6Sn_5 phase [30]. Copper is taken to be isotropic elastic-plastic with linear strain hardening, with its plastic yielding following the von Mises criterion and incremental flow theory. Its plastic yielding behavior is based on experimental measurement of a 1 μm-thick passivated Cu film [31]. The solder material, taken to be the Sn–1.0Ag–0.1Cu alloy [26], is also treated as an isotropic elastic-plastic solid. Its plastic response follows the slow-rate experimental stress-strain curve with an initial yield strength of 20 MPa; the flow strength increases to a peak value of 36 MPa at the plastic strain of 0.15, beyond which a perfectly plastic behavior is assumed [32,33]. For simplicity no other contact or dielectric layers are included in the model, and all interfaces are assumed to be perfectly bonded. It is worth mentioning that, for the underfill material, there is a large variation of mechanical properties across its glass transition temperature (T_g). The initial portion of the cooling process from 250 to 20°C considered in this study is likely to be above the underfill T_g. In our preliminary analysis, a reduced underfill elastic modulus from 7.0 GPa to 0.04 GPa [29] over the temperature range of 100 to 110°C was tested (above the conceived T_g the low modulus of 0.04 GPa was maintained). This exercise showed that plastic deformation in solder is moderately enhanced, but the overall stress and deformation fields in the entire structure remained very similar to the cases without the T_g consideration. Therefore, constant underfill properties are used in the present work.

Table 1: Material properties used in the finite element modeling (E: Young's modulus, ν: Poisson's ratio, α: coefficient of thermal expansion, σ_y: yield strength, H: plastic linear hardening slope). In addition to the listed temperature-independent material properties, a linear temperature dependence is specifically taken into account for Cu, with its values at 250°C being E: 105.8 GPa, ν: 0.3, α: 18.6×10^{-6}/K, σ_y: 121.3 MPa and H: 8.6 GPa.

	Cu	Solder	Si	Underfill	Cu_6Sn_5
E (GPa)	110	47	130	7.0	134
ν	0.3	0.36	0.28	0.33	0.28
α (10^{-6}/K)	17.0	22.5	3.1	32.0	16.0
σ_y (MPa)	155	20	--	--	--
H (GPa)	17.8	Non-linear (see text)	--	--	--

3.2.2 Model Validation

Due to the idealized model configuration, no attempt was made to quantitatively correlate the numerical prediction with an actual experiment on the 3D package. Rather, we seek to validate the model in a qualitative manner, by comparing the plastic deformation field with experimentally observed damage path in an actual solder joint [34,35]. It is known that solder joint failure can occur at the joint boundary (along the intermetallic layer), which can be explained by the weak interfacial strength or the brittle nature of the intermetallic. However, a commonly observed failure pattern in real-life and laboratory shear-tested solder joints is that cracking appears close to, but not at, the interface between the solder and bond material. An example is illustrated in Figure 7(a), which shows a cross section of a scanning electron microscopy image of a Sn-based

solder bump after being repeatedly sheared by way of thermal cycling [36]. Failure was found to be near the interface between solder and Si chip.

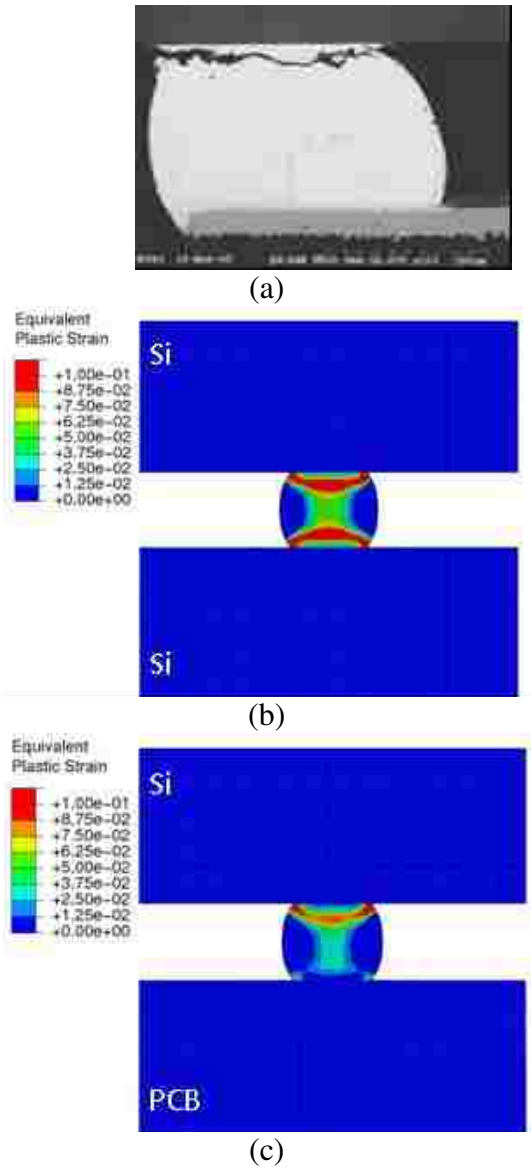


Figure 7: (a) Experimentally observed cracking in a Sn-3Ag-0.5Cu solder ball after thermal cycling between -40 and 125°C for 500 cycles [31]. (b) and (c): Contour plots of equivalent plastic strain in the solder joint after 10 cycles of shear deformation if (b) both the upper and lower substrates are Si, and (c) the upper and lower substrates are Si and printed circuit board (PCB), respectively.

The model depicted in Figure 7 is used for the benchmark calculation. In particular, the entire bump is taken to be the Sn-based solder and made into a bump shape. No underfill is used and the TSV is replaced by Si. Figure 7(b) shows the contour plot of equivalent plastic strain after 10 cycles of shear deformation between displacements 0 and 1 μm. Highly non-uniform plastic deformation has occurred in the solder. Distinct bands of concentrated plastic deformation have developed close to, but not at, the interface between solder and Si substrate. Accumulation of local plasticity will thus lead to damage initiation and eventual failure. This likely failure path along the localized plastic band is consistent with experimental observation.

We now consider a case where the upper substrate is still Si but the lower substrate is a printed circuit board (assumed to be a homogeneous material with Young's modulus 22 GPa and Poisson's ratio 0.28). The assembly is subjected to the same cyclic shear deformation, and the contour plot of equivalent plastic strain is shown in Figure 7(c). The concentrated deformation band appears only near the interface between solder and the upper substrate. Apparently the stiffness of the substrate material plays an important role in affecting the deformation inside the solder joint. The more compliant lower substrate, in comparison with the upper substrate, tends to deform more easily under the applied shear, so it has a greater tendency to deform with the solder. It can be deduced from Figure 7(c) that damage initiation in solder is more likely to take place near the interface with the upper substrate (Si chip). We note that, in Figure 7(a), the actual crack in the solder bump is also on the Si chip side (the other side is the more compliant organic-based circuit board) [34].

3.3 Results and Discussion

Numerical results in the forms of contour plots and overall mechanical response are now presented. Special attention is devoted to the comparison of results with the different model features. The cases where a soft solder exists in the micro-bump is considered first.

3.3.1 Overall Shear Response

Figure 8(a)-(c) show the distribution of shear stress σ_{xy} generated in the chip/joint structure when the applied shear displacement reaches 1 μm, for the solder thicknesses of 20, 10 and 5 μm, respectively, in the case of no underfill. It can be seen that the shear stress is largely carried by the joint area, and its distorted shape is apparent. The magnitude of σ_{xy} inside the solder region is not large (limited to about 20 MPa) due to its highly plastic nature. In the cases with thinner solder regions (or thicker Cu layers in the joint, Figure 8(b) and (c)), the shear stress in the Cu regions sandwiching the solder is actually greater (close to 30 MPa). Only small regions in the Si chips, near the four corners of the joint, are under relatively high shear stress.

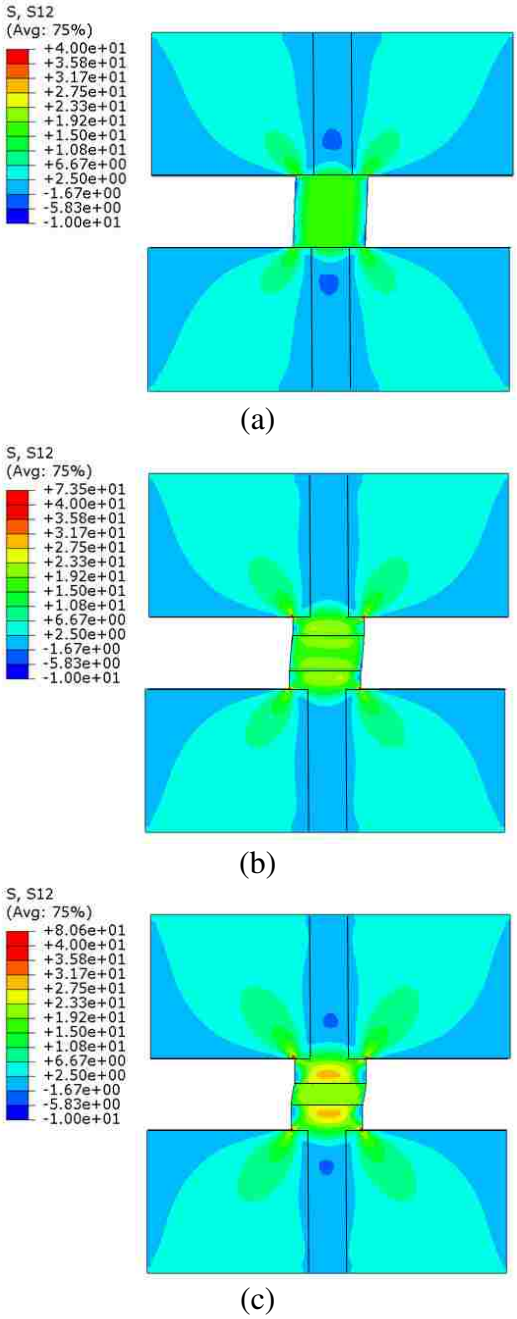


Figure 8: Contour plots of shear stress σ_{xy} (MPa) at the maximum applied shear displacement of 1 μm, for solder thicknesses of (a) 20 μm, (b) 10 μm and (c) 5 μm, in the case without underfill.

A similar set of contour plots of shear stress σ_{xy}, but for models with the underfill, is shown in Figure 9. Here the same overall applied shear displacement is seen to generate much higher shear stresses, compared to the case without underfill. A thinner solder region generally results in higher shear stresses in the surrounding area including Si. Note that in Figure 9(c) where the solder thickness is 5 μm, the shear stress in the adjacent underfill can attain a value of 150 MPa, which brings about the possibility of local debonding between the underfill and micro-bump.

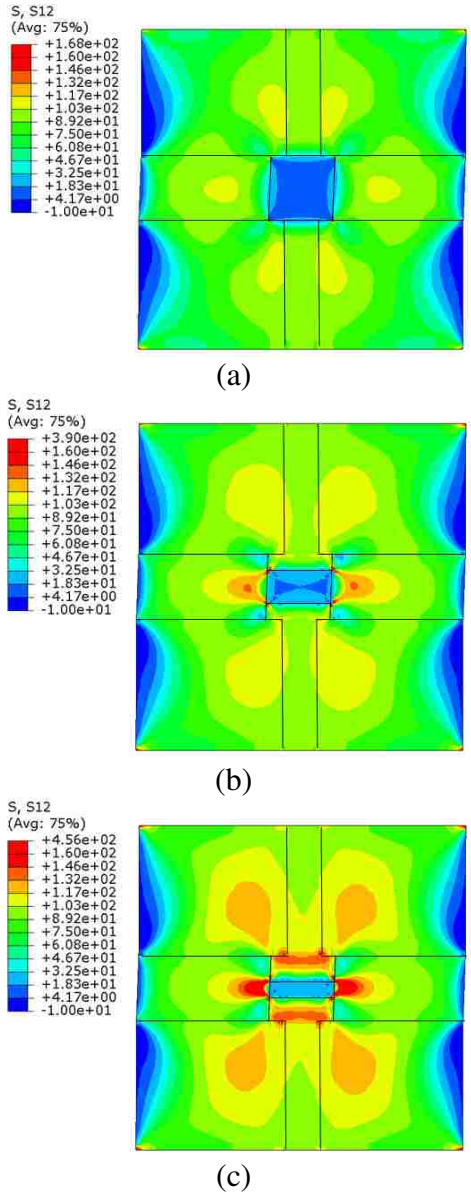
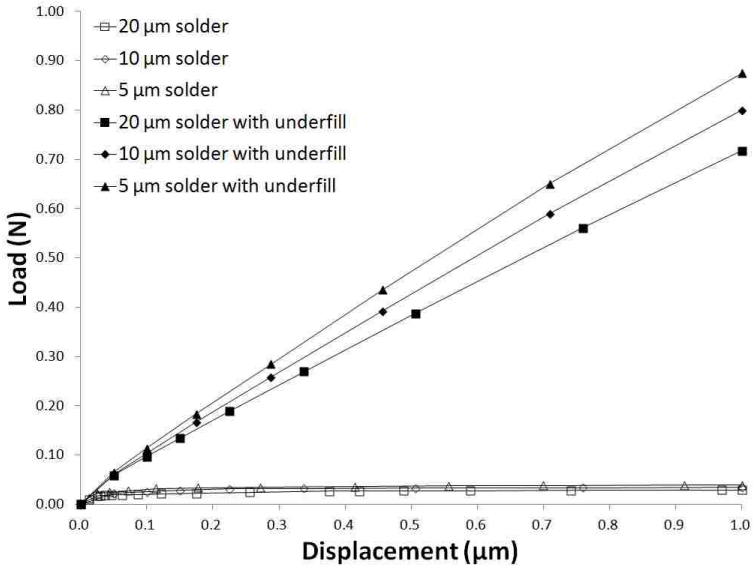


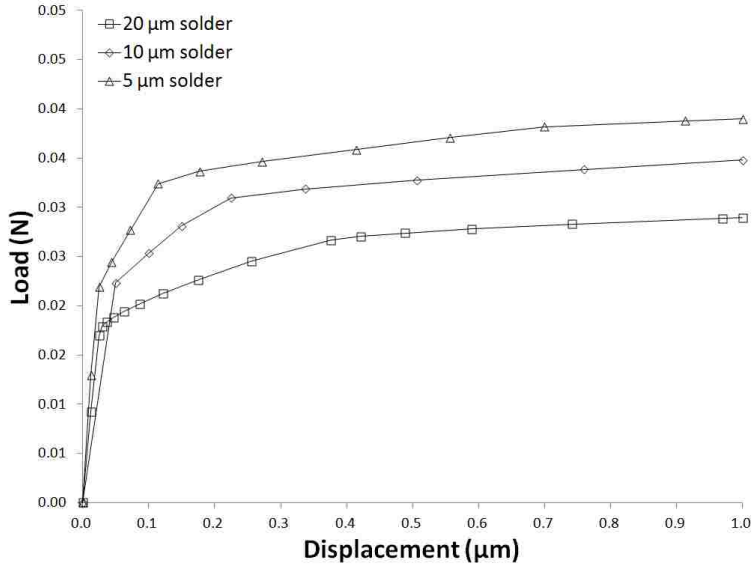
Figure 9: Contour plots of shear stress σ_{xy} (MPa) at the maximum applied shear displacement of 1 µm, for solder region thicknesses of (a) 20 µm, (b) 10 µm and (c) 5 µm, in the case with underfill.

Figure 10(a) shows the overall shear force-displacement curves corresponding to all six conditions (with and without underfill, each with three different solder thicknesses). The models containing underfill display a much greater strength than those without

underfill. Figure 10(b) shows the overall shear force-displacement curve without underfill at an enlarged scale. The shape of the load force-displacement curve is representative of an elastic-plastic material. The high strength in underfilled stack suggests that the joint can better resist misalignment induced shear deformation from a global standpoint. However, the risk of local damage may become higher owing to the high local stresses as illustrated by the stress distribution in Figure 9. The shear response in Figure 10 also shows that, in both cases with and without underfill, the overall shear force becomes greater as the solder region of the micro-bump becomes thinner.



(a)



(b)

Figure 10: Load-displacement curves up to the applied shear displacement of 1 µm (a) with and without underfill, (b) without underfill, each with three different solder region thicknesses (5, 10 and 20 µm).

It is worth pointing out that the current numerical model does not include any on-chip interconnect and dielectric materials. Rather, only Si and Cu TSV are used to represent

the chip structure. It is expected that the deformation field "spreading" to the chip region will affect the interconnect and dielectric materials. However, since their modulus values are generally no greater than that of Si, the stresses carried by Si observed in the present modeling should serve as an upper bound for the stresses in the interconnect structure.

Plastic Deformation in Micro-bump, Figure 11(a)-(c) show the contour plots of equivalent plastic strain at the maximum applied shear displacement of 1 μm, for the solder thicknesses of 20, 10 and 5 μm, respectively, in the case of no underfill. Although the shear stress levels are comparable in solders of different thicknesses, Figure 8, a significant variation of the plastic strain field exists. In Figure 11(a) and (b), strong deformation bands near the solder-Cu interfaces are evident, which is similar to that in Figure 7. This observation also suggests that the side wall of the joint, bulged or straight, does not play a major role in affecting the plastic deformation pattern. The highly non-uniform deformation becomes less apparent as the solder region thickness is made smaller, Figure 11(c). This is because the entire thin layer is now under severe constraint by the long interfaces relative to the thickness dimension [29]. Generally speaking, the same overall horizontal shift is now born by the soft material with a reduced thickness, so a higher strain level is seen in Figure 11(c). Note also that, for all solder thicknesses considered, neither the Cu TSV nor the Cu region inside the micro-bump shows any notable plasticity during the deformation.

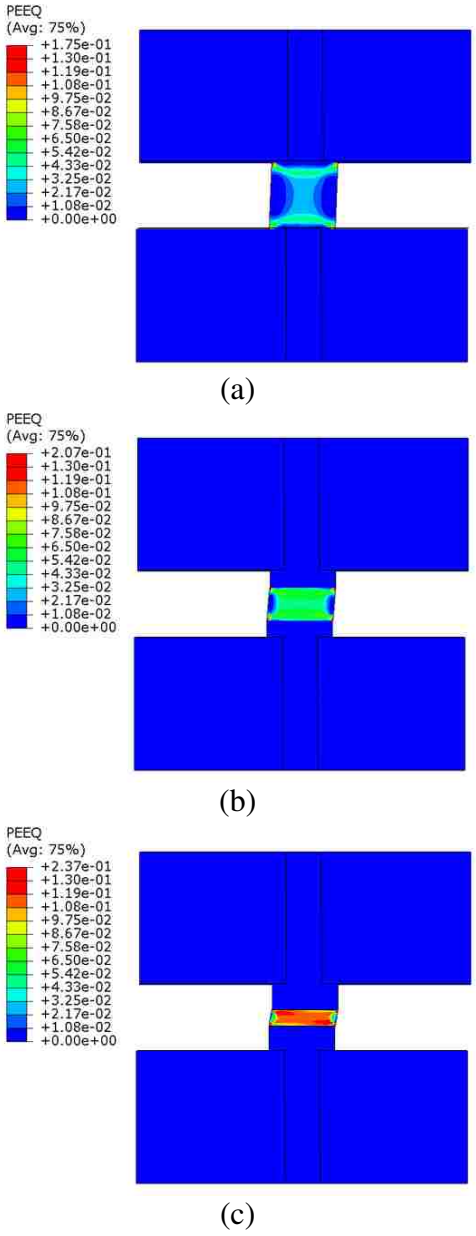


Figure 11: Contour plots of equivalent plastic strain at the maximum applied shear displacement of 1 µm, for solder thicknesses of (a) 20 µm, (b) 10 µm and (c) 5 µm, in the case without underfill.

If underfill is present in the model, plastic deformation takes up a different form as shown in Figure 12(a)-(c). It can be seen that there is no banded deformation structure in all solder regions. Relatively high plastic strains exist near the interface regions adjacent

to the Cu and underfill. The plastic strain value generally increases with decreasing solder thickness. The underfill material is much more compliant than Si and Cu, the presence of which, however, is able to affect the plastic deformation pattern in solder to a significant extent.

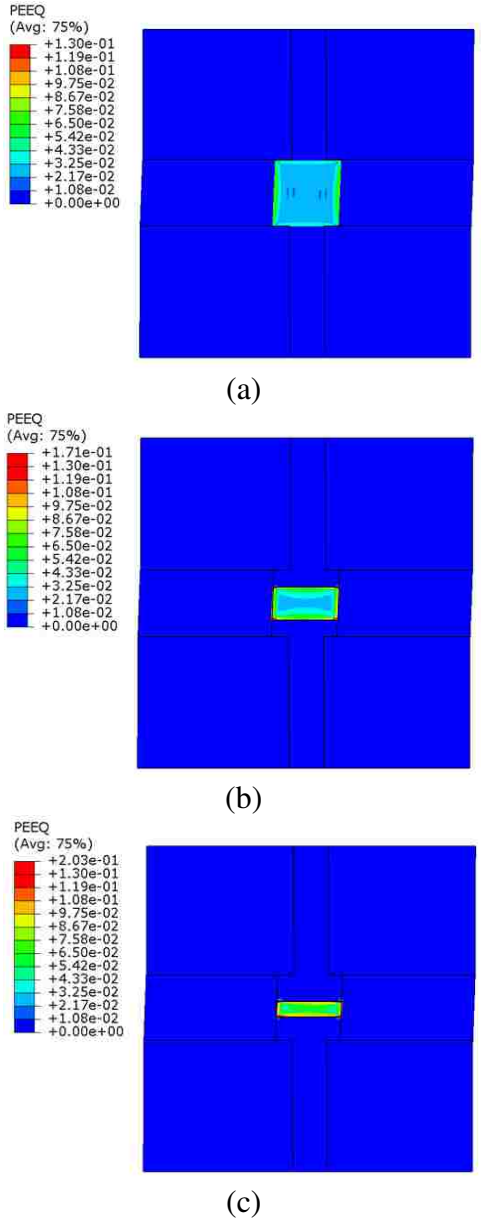


Figure 12: Contour plots of equivalent plastic strain at the maximum applied shear displacement of 1 μm, for solder thicknesses of (a) 20 μm, (b) 10 μm and (c) 5 μm, in the case with underfill.

For gaining quantitative insight into solder plasticity influenced by its thickness and underfill, the equivalent plastic strain values were averaged over the solder area during the deformation history. Figure 13 shows the variations of this averaged plastic strain with the applied shear displacement, up to 1 μm, for both the cases with and without underfill, each with three solder thicknesses (20, 10 and 5 μm). It can be seen that solder is in its elastic state (zero plastic strain) when the applied shear is very small. Once plastic yielding starts, different solder thicknesses with or without underfill, give rise to very different average plastic strains. The accumulation of plasticity is much faster in thin solders, which suggests their higher tendency for damage initiation. Among the six curves in Figure 13, the highest and lowest both correspond to the case without underfill (the thinnest and thickest solders, respectively). The 10 μm-thick solder shows nearly identical evolution of average plastic strain with and without underfill. Taking into account the overall shear response, Figure 10, and solder plastic strain, Figure 13, the case of thinnest solder without underfill poses the highest concern for shear induced micro-bump failure.

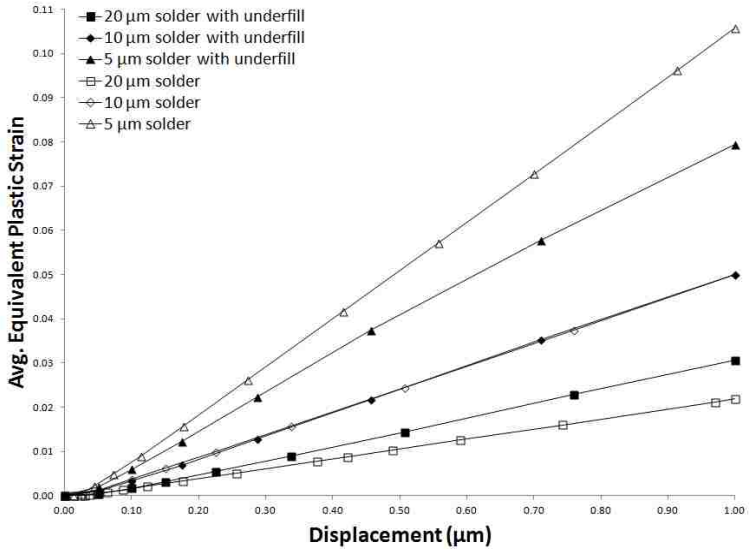


Figure 13: Equivalent plastic strains, averaged over the solder region, as a function of the applied shear displacement up to 1 μm, for the cases without and with underfill, each with three different solder thicknesses (5, 10 and 20 μm).

3.3.2 Replacement of Solder by Intermetallic

When the solder region in an actual micro-bump is thin, the reaction between solder alloy and copper may transform the entire solder into an intermetallic compound layer during the post-soldering annealing process [3]. We therefore consider one special case in the present modeling, by taking the 5 μm-thick solder region as an intermetallic layer. Figure 14(a) and (b) show the σ_{xy} shear stress contours at the maximum applied shear displacement, for the cases without and with underfill, respectively. It is evident that, with the stiff brittle material at the center of the joint, the greatest local stress now appears in the intermetallic itself in both cases. The maximum shear stress in the intermetallic is slightly higher when underfill does not exist, Figure 14(a). However, the underfill bonding the two Si chips in Figure 14(b) aids in the resistance to shear, as was

manifested by the overall load-displacement response shown in Figure 15. Here the underfill-containing chip stack shows a much greater shear force during deformation. At the maximum shear displacement of 1 μm, the overall shear force is seen to be more than twice that without the underfill.

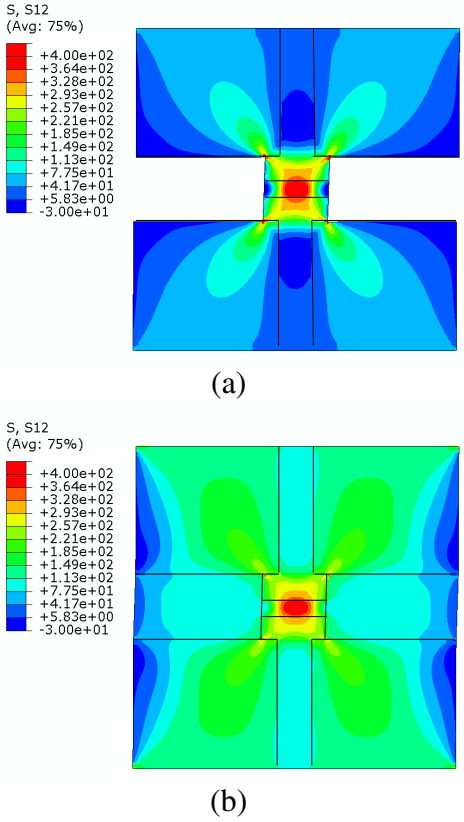


Figure 14: Contour plots of shear stress σ_{xy} (MPa) at the maximum applied shear displacement of 1 μm, for the cases (a) without and (b) with underfill, if the 5 μm-thick solder is converted entirely into intermetallic.

By comparing the shear force magnitudes in Figure 15 and Figure 10 at the same displacement, it is clear that the "intermetallic joint" offers a higher resistance to shear deformation than the "solder joint." However, consideration of the local stress features is

also important. By comparing Figure 14(b) with Figure 9(c) (same thickness of intermetallic and solder), the local shear stress σ_{xy} in the underfill adjacent to the micro-bump is found to be lower if solder is completely replaced by intermetallic (approximately 100 vs. 150 MPa). The risk of failure caused by the underfill is thus reduced, but the high stress in intermetallic itself reaches nearly 400 MPa, Figure 14(b).

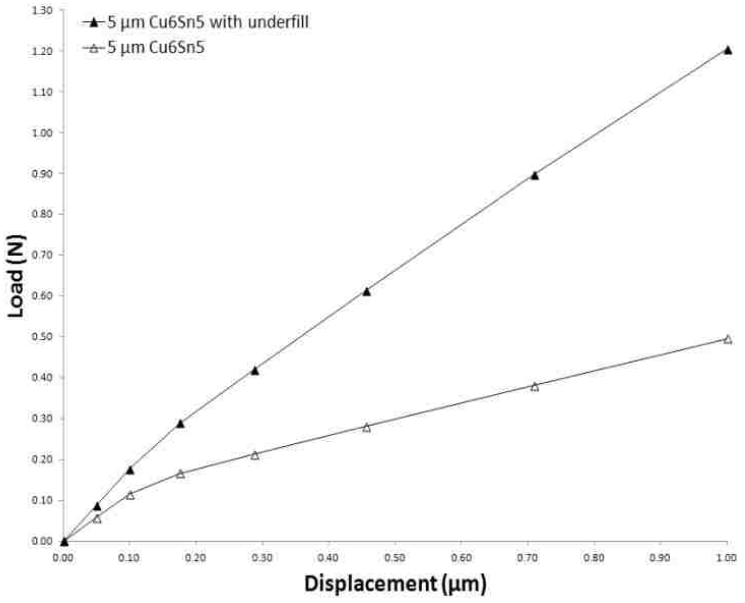
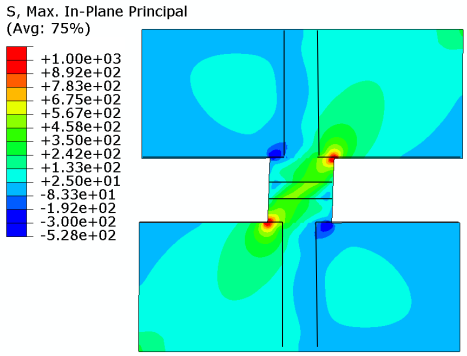


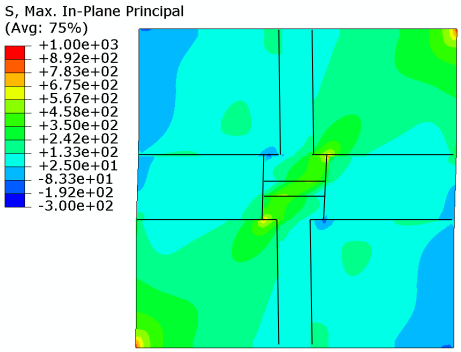
Figure 15: The overall load-displacement curves at the maximum applied shear displacement of 1 µm, for the cases without and with underfill, if the 5 µm-thick solder is converted entirely into intermetallic.

The maximum principal stress field also deserves attention here. Figure 16(a) and (b) show the contour plots of maximum in-plane principal stress for the cases without and with underfill, respectively, at the maximum deformation. It can be seen that the tensile stress can reach beyond 400 MPa in a certain portion of the intermetallic in both cases. As a consequence, failure initiated at the intermetallic is of concern. In addition, high

tensile stresses are also observed in some parts of the Si near the joint corners, which may have implications for the mechanical integrity of Si itself. The same concern applies also to the on-chip interconnect and dielectric structures. Although they are not explicitly included in the present analysis, existence of the high tensile stress implies potential damage such as dielectric cracking and interfacial debonding.



(a)



(b)

Figure 16: Contour plots of maximum in-plane principal stress (MPa) at the maximum applied shear displacement of 1 μm, if the 5 μm-thick solder is converted entirely into intermetallic, for the cases (a) without and (b) with underfill.

Figure 17(a) and (b) show the contour plots of equivalent plastic strain at the maximum shear displacement, for the cases without and with underfill, respectively. With the thin solder region replaced by the stiff intermetallic, the Cu region directly above and

below the intermetallic is now under a greater extent of deformation and plastic yielding has occurred. Therefore, the concern of permanent deformation caused by misalignment still exists for intermetallic joints, except that plasticity is now in copper rather than solder as in previous considerations. Plastic deformation may spread into the TSV as observed in Figure 17(b).

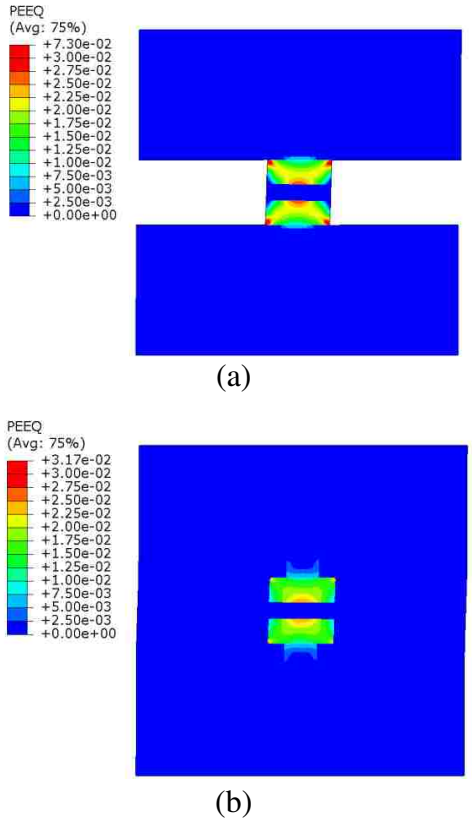


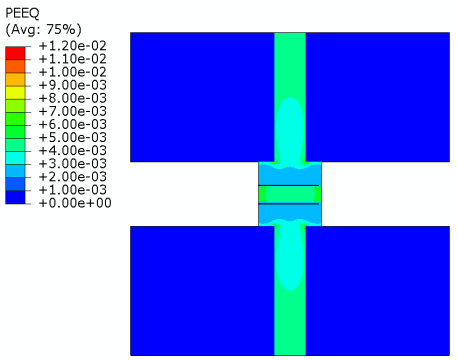
Figure 17: Contour plots of equivalent plastic strain at the maximum applied shear displacement of 1 μm, if the 5 μm-thick solder is converted entirely into intermetallic, for the cases (a) without and (b) with underfill.

3.3.3 Comparison with Thermal Mismatch Induced Deformation

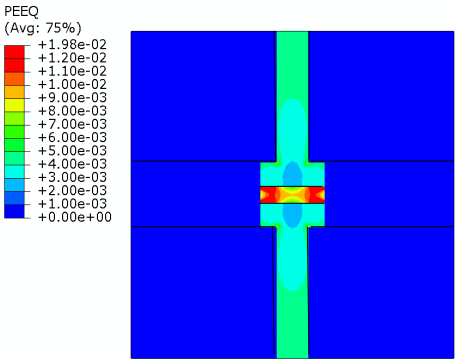
In this section we present select results on stress and deformation fields induced by thermal expansion mismatches after a simple cooling process from 250 to 20°C. When

making comparisons with the shear loading results, we use the maximum shear displacement of 1 μm as a basis (with the understanding that, if the prescribed shear displacement is smaller, the extent of internal deformation will also be smaller). The same model configuration as in Figure 6 is used, with the purpose of examining the different nature and extent of deformation caused by temperature excursion as compared to mechanical shear. To conserve space, we limit the presentation to the cases of solder and intermetallic thickness of 5 μm.

Figure 18(a) and (b) show the equivalent plastic strain contours after cooling in the cases without and with underfill, respectively, when the center region of the micro-bump is the solder alloy. Due to the fact that the Cu TSV is surrounded along its side wall by Si with a much lower CTE, significant tensile stresses exist and plastic deformation has occurred. As for the solder, its CTE mismatch with surroundings, combined with its low yield strength, have resulted in a higher degree of plasticity, especially in the case with underfill, Figure 18(b). Compared with deformation caused by the 1 μm shear displacement, Figure 12(c), thermally induced plastic strains in solder are significantly smaller. Deformation in the Cu TSV, however, is more influenced by the thermal loading.



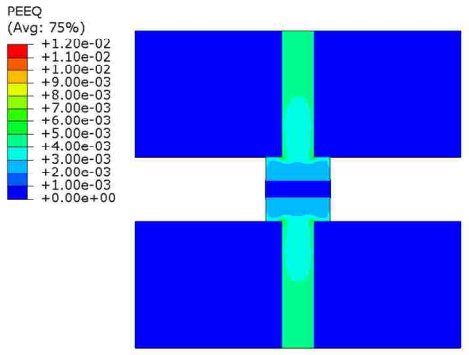
(a)



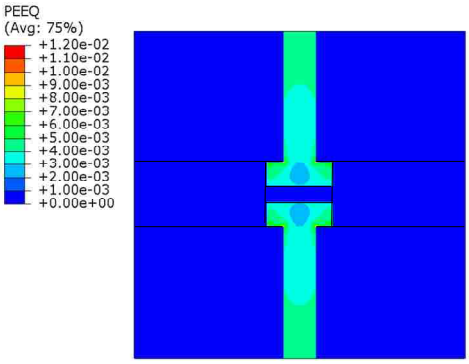
(b)

Figure 18: Contour plots of equivalent plastic strain after cooling for the cases (a) without and (b) with underfill, when the center region of the micro-bump is solder.

With the solder region entirely replaced by intermetallic, plastic deformation occurs only in Cu as shown in the equivalent plastic strain contours in Figure 19. Plastic strains in the Cu region inside the micro-bump are smaller compared to those due to shear, Figure 12, but again yielding in the entire TSV has occurred under thermal loading. A comparison between Figure 18 and Figure 19 shows that the plastic strain levels in the Cu TSV are generally insensitive to the actual joint material (solder or intermetallic).



(a)

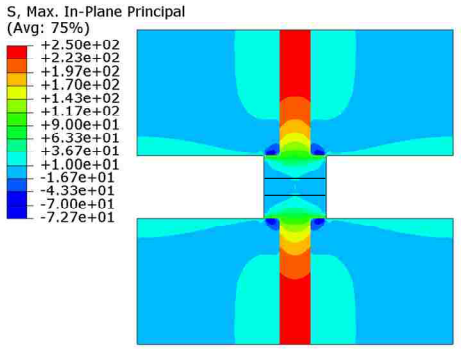


(b)

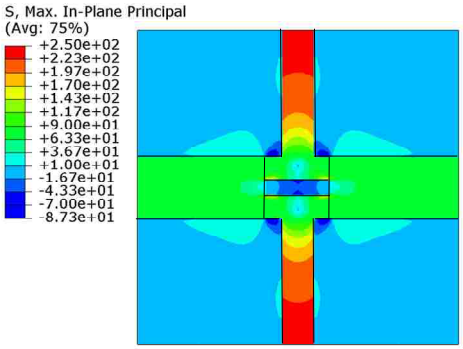
Figure 19: Contour plots of equivalent plastic strain after cooling for the cases (a) without and (b) with underfill, when the center region of the micro-bump is intermetallic.

Attention is now turned to the maximum in-plane principal stress, with Figure 20(a) and (b) showing contours without and with underfill, respectively, after cooling when the center layer of the joint is solder. The corresponding figures for the intermetallic joint are shown in Figure 21(a) and (b). The maximum tensile stresses inside the Cu TSV are comparable in all cases, as the stress state therein is dominated by its mismatch with the Si chip. Stresses inside the intermetallic, Figure 21, are much lower than those due to overall mechanical shear Figure 17. Because of the relatively high CTE value of underfill compared to all other materials, the underfill is under a tensile state after cooling

(maximum values around 90 MPa, Figure 20(b) and Figure 21(b)). As for the Si chips, the maximum tensile stresses are much lower than those caused by shear when the joint material is entirely intermetallic, Figure 16. However, the CTE mismatch generally leads to compressive stresses in Si after cooling (not shown here).



(a)



(b)

Figure 20: Contour plots of maximum in-plane principal stress (MPa) after cooling for the cases (a) without and (b) with underfill, when the center region of the micro-bump is solder.

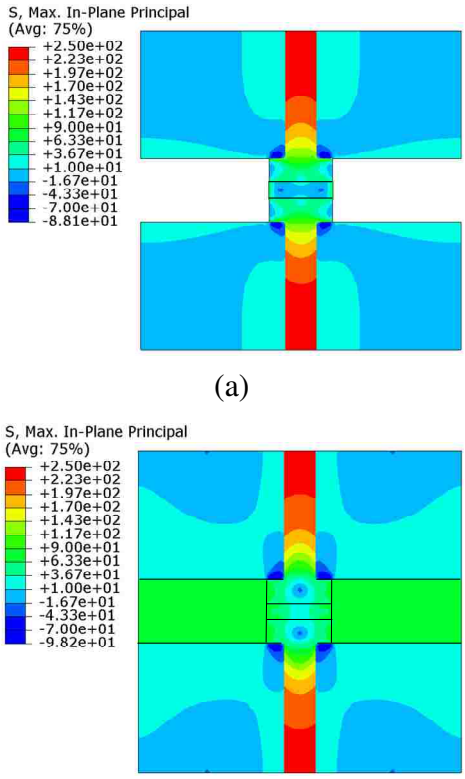


Figure 21: Contour plots of maximum in-plane principal stress (MPa) after cooling for the cases (a) without and (b) with underfill, when the center region of the micro-bump is intermetallic.

3.4 Conclusions

Parametric 2D finite element analyses were conducted to study the misalignment effects on 3D IC packages. The misalignment was implemented through a prescribed shear deformation on a model chip stack. Salient findings on the stress and deformation fields in the micro-bump, TSV, underfill and Si chip are summarized below.

- With a constant micro-bump size, a thinner solder layer sandwiched between copper pads displays a better mechanical resistance to overall shear. But thinner

solder is more susceptible to damage initiation due to faster buildup of local plastic strain.

- The existence of underfill significantly raises the shear force required to attain a given overall shear displacement. The underfill material surrounding the micro-bump can experience high shear stresses, which, in conjunction with the localization of plastic strain along the solder boundary, imply the risk of interface damage around the joint.

- If the solder alloy is entirely transformed into intermetallic, high shear stresses develop inside the intermetallic and nearby regions of copper and silicon. The intermetallic is also under high tensile stresses implying that brittle failure may become a concern under shear deformation.

- Mechanical shearing generally gives rise to a much higher stress level in and around the micro-bump area in the case of an "intermetallic joint," and a much greater degree of plasticity in the case of a "solder joint," in comparison with the inner regions of the TSV (away from the micro-bump). The inner TSV regions, on the other hand, also experience significant deformation due to thermal loading.

Chapter 4 Three-Dimensinal Analyses[2]

4.1 Introduction

In Chapter 3, a systematic 2D study on the misalignment induced shear deformation and thermal loading effect was presented. As a follow up, the present chapter is devoted to expanding the previous 2D analyses to include 3D effects. The 3D finite element model uses a representative layout to capture the basic physical features of the Si chip, TSV, solder material and underfill layer (when existent). Again, we seek to parametrically explore the trend of stress and deformation fields due to misalignment-induced shear deformation and thermal expansion mismatch.

[2] Compiled from a conference paper submitted to IMECE2012, Proceedings of the ASME 2012 International Mechanical Engineering Congress & Exposition, May 2012 [37].

4.2 Numerical Model

Figure 22 shows the model geometry. The simulation domain may be viewed conceptually as a representative area segment highlighted by the dashed rectangle in Figure 5. The model is symmetric about the front x-y plane (exposed in Figure 22), with overall dimensions of 100 µm wide (w) by 100 µm high (h) by 50 µm deep (d). The copper TSVs in the upper and lower Si chips are connected through a micro-bump (also referred to as "joint" as in Chapter 3) of thickness (t_{joint}) 20 µm and diameter (D_{joint}) 20 µm. The micro-bump is assumed to have straight cylindrical walls and a Cu-solder-Cu structure. The solder thickness (t_{solder}) is fixed in this chapter at 5 µm. In one particular case of the present modeling, we replace the entire 5 µm-thick solder layer by an intermetallic material. Outside of the micro-bump and between the chips, there is a possible underfill layer as depicted in Figure 22. The influence of underfill in the bonded chip structure subject to loading is specifically studied. The TSV diameter (D_{TSV}) is 10 µm. Cases of misalignment-induced shear and thermal loading are simulated, with and without an underfill layer in the joint region, to understand the effect of underfill on the stress fields and damage propensity of the 3D chip stack.

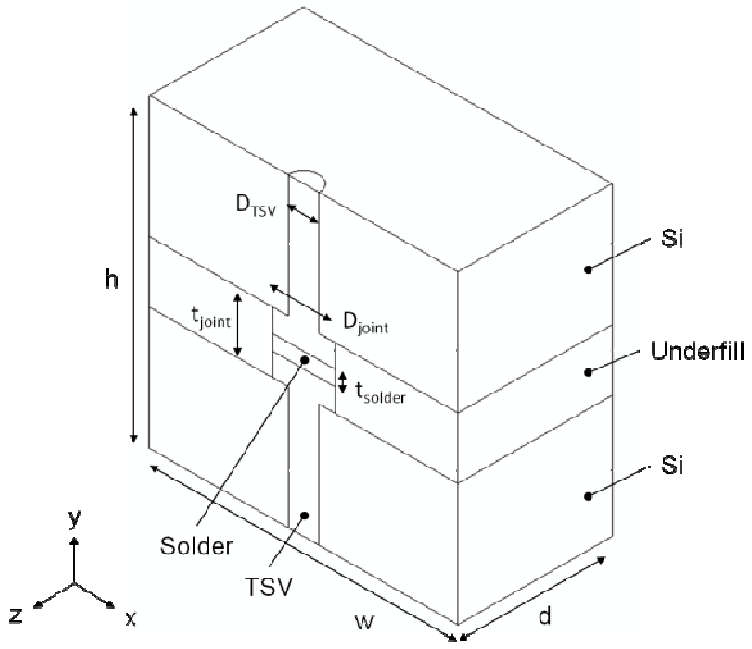


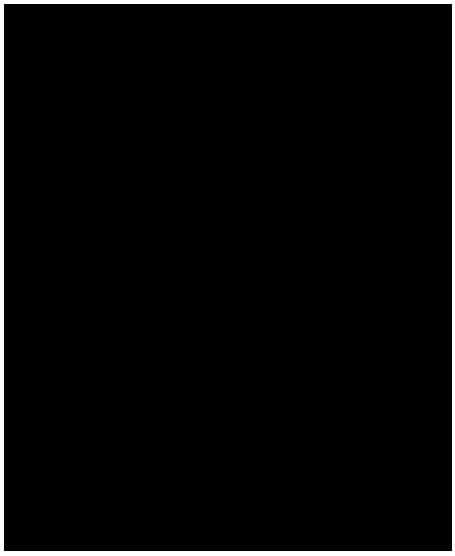
Figure 22: Model layout used in the 3D finite element modeling of a representative TSV/micro-bump bonding structure connecting two adjacent silicon chips, with an underfill layer around the joint region.

As in Chapter 3, misalignment-induced shear deformation is modeled through a prescribed shear action. The bottom boundary of the model is fixed, while the top boundary is displaced in the x-direction for up to a maximum of 1 μm (presumably the misalignment distance). The left, right and back boundaries are not constrained. Note that the current loading mode and boundary conditions do not give rise to a strict periodic deformation field representative of a true composite structure with repeated unit cells. However, since the main deformation action is centered around the micro-bump region, which is reasonably away from the boundaries of the model, key deformation features can still be obtained from the current approach. Moreover, by comparing results from the various scenarios within the present modeling framework, useful trends about overall

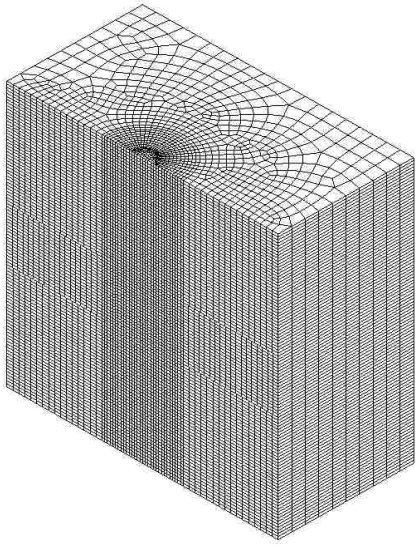
mechanical response, local deformation and damage propensity can be obtained. We also note that the present modeling focuses only on a representative micro-bump and its vicinity inside a chip stack, Figure 5, so the misalignment effect on the packaging substrate is excluded from the investigation. For gaining insight on how deformation caused by overall shear differs from that caused by thermal expansion mismatch due to processing, we also consider pure thermal loading, from 250 to 20ºC, using the same model depicted in Figure 22. During thermal loading, the left boundary (the left y-z plane) is prohibited to displace in the x-direction but tangential movement of its nodal points is allowed. The bottom boundary is prohibited to displace in the y-direction but tangential movement of its nodal points is allowed. The top and right boundaries are constrained to remain horizontal and vertical, respectively, but otherwise can adjust their positions. The boundary conditions thus ensure that the domain is a true unit cell of the periodic composite structure. [28].

The finite element program Abaqus (Version 6.10, Dassault Systemes Simulia Corp., Providence, RI, USA) is employed for the 3D computation. The model without an underfill layer, Figure 23(a), contains a total of 89,308 eight-noded linear brick elements, with mesh refinement in the TSV and joint regions. The model with an underfill layer, Figure 23(b), contains a total of 104,408 eight-noded linear brick elements, also with a finer mesh size around the TSV and joint regions. An assessment of numerical convergence led to mesh refinement around the joint. The mesh density in the regions of high strain gradient was successively increased. A more rigorous assessment of the convergence should be performed in order to accurately predict stresses and damage

propensity in an actual 3D IC. The material properties used as input parameters in the modeling are identical to those in Chapter 3 (Table 1).



(a)



(b)

Figure 23: (a) Mesh with an underfill layer removed containing 89,308 eight-noded linear brick elements, (b) Mesh with an underfill layer around the joint region containing 104,408 eight-noded linear brick elements.

4.3 Results and Discussion

Numerical results in the form of contour plots and overall mechanical response curves are now presented. Special attention is devoted to the comparison of results with the different model features. Misalignment-induced shear deformation in the micro-bump is considered first.

4.3.1 Overall Shear Response

Figure 24 shows the contour plots of shear stress σ_{xy} generated in the chip/joint structure when the applied shear displacement reaches 1 μm. A backside view of the TSV/micro-bump is also shown, with the silicon and possible underfill hidden. The results presented for the 3D modeling case show similar stress and deformation trends to those of the 2D case presented earlier. Without an underfill layer, Figure 24(a), the shear stress is largely carried by the joint, and its distorted shape is apparent. The magnitude of σ_{xy} inside the solder region is limited to about 20 MPa, due to its low yield strength and highly plastic nature. Only small regions in the Si chips, near the four corners of the joint, are under relatively high shear stress. Another contour plot, Figure 24(b), shows the shear stress σ_{xy} in the case with an underfill layer around the joint. When the same displacement is applied, much higher values of shear stress are seen in the Si and Cu regions of the chip/joint with also high stresses on the backside of the TSV/micro-bump. The shear stress carried by the solder remains limited to its plastic flow stress with an underfill layer present around the joint. However, the shear stress in the surrounding underfill can attain

150 MPa, which brings about the possibility of local debonding between the underfill and micro-bump.

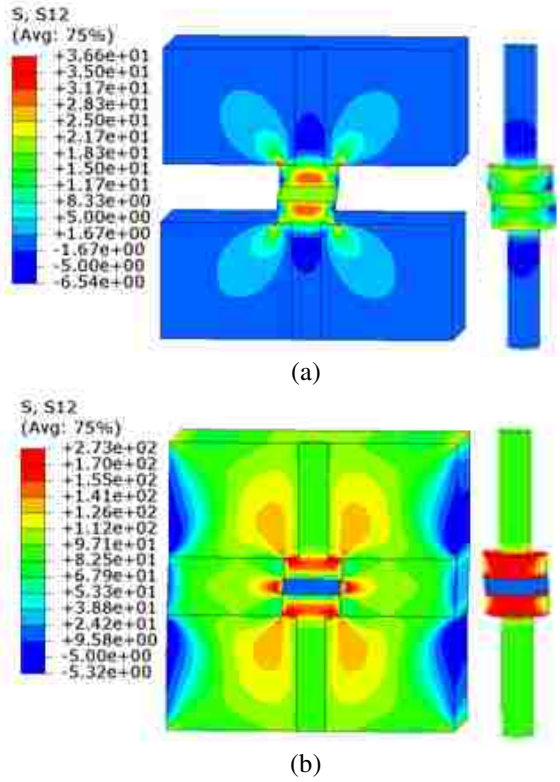
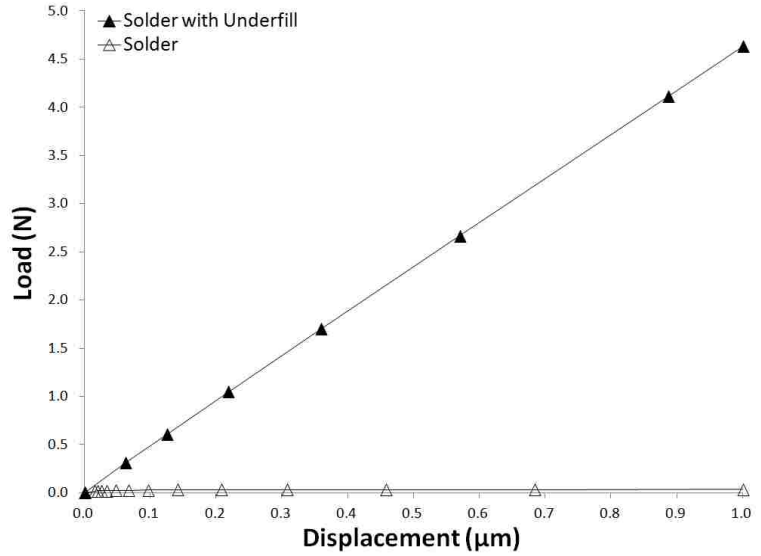


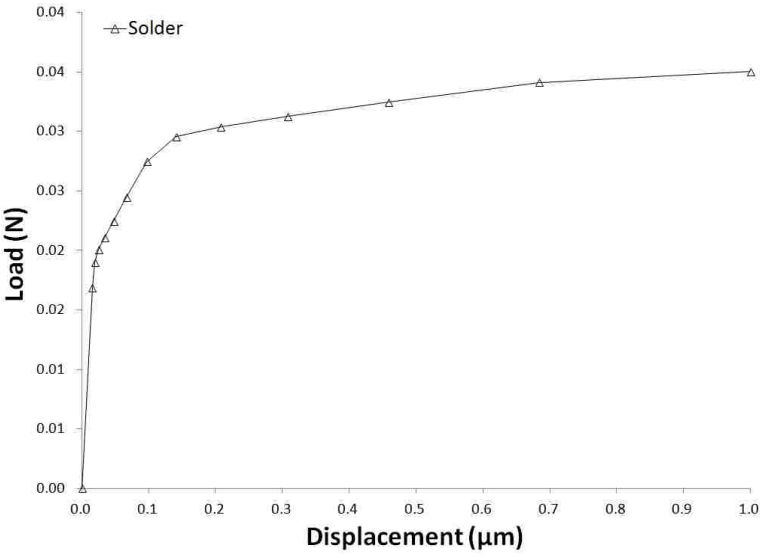
Figure 24: Contour plots of the shear stress σ_{xy} (MPa) at the maximum applied shear displacement of 1 µm. The backside of the TSV/micro-bump is also shown on the right. (a) The case without an underfill layer; (b) the case with an underfill layer around the joint.

Figure 25(a) shows the overall shear load-displacement curves for the cases with and without an underfill layer around the joint. When underfill is present, a much higher strength is obtained. This high strength suggests that the chip stack can better resist misalignment-induced shear deformation from a global standpoint. However, the risk of local damage around the joint may become higher owing to the high local stresses as illustrated by the stress distribution in Figure 24. Figure 25(b) shows the overall shear

load-displacement curve for the case without underfill around the joint at an enlarged scale. The shape of the curve shows the elastic-plastic behavior of the solder joint under shear loading.



(a)



(b)

Figure 25: Load-displacement curves up to the applied shear displacement of 1 µm for the cases (a) with and without an underfill layer, (b) without an underfill layer around the joint.

4.3.2 Plastic Deformation in Micro-bump

Figure 26 shows the contour plots of equivalent plastic strain generated in the structure when the applied shear displacement reaches 1 µm. Without an underfill layer, Figure 26(a), the shear load is carried by the solder leading to stronger plastic deformation generally in the center of the solder. When the underfill layer is present, Figure 26(b), the load is now carried in part by the underfill and the pattern of plastic deformation in the solder changes. With underfill, high plastic strains appear in the interface regions. Note also that neither the Cu TSV nor the Cu region inside the micro-bump show any notable plasticity during the deformation. The presence of an underfill layer around the solder joint is able to affect the plastic deformation pattern to a significant extent.

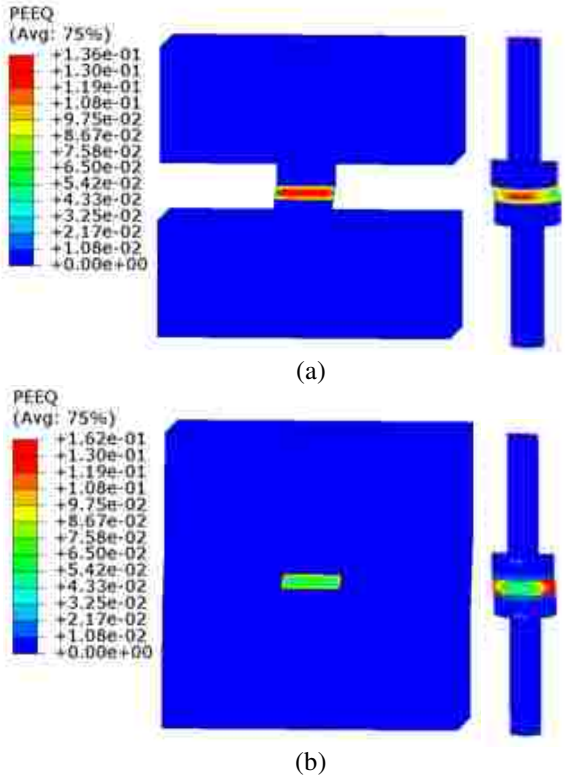


Figure 26: Contour plots of the equivalent plastic strain at the maximum applied shear displacement of 1 µm. (a) The case without an underfill layer; (b) the case with an underfill layer around the joint.

For gaining quantitative insight into solder plasticity during shear loading of the chip stack, the equivalent plastic strains were averaged over the solder volume during the deformation history, as in the 2D study. Figure 27 shows the average equivalent plastic strain curves for the cases with and without an underfill layer around the joint. It can be seen that the solder is in its elastic state, zero plastic strain, when the applied shear displacement is very small. When plasticity builds up, the average equivalent plastic strain is approximately 50% higher in the case without underfill than that with underfill. Therefore solder without an underfill layer around the joint poses a higher concern for shear induced micro-bump failure since the joint has generally undergone more significant plastic yielding.

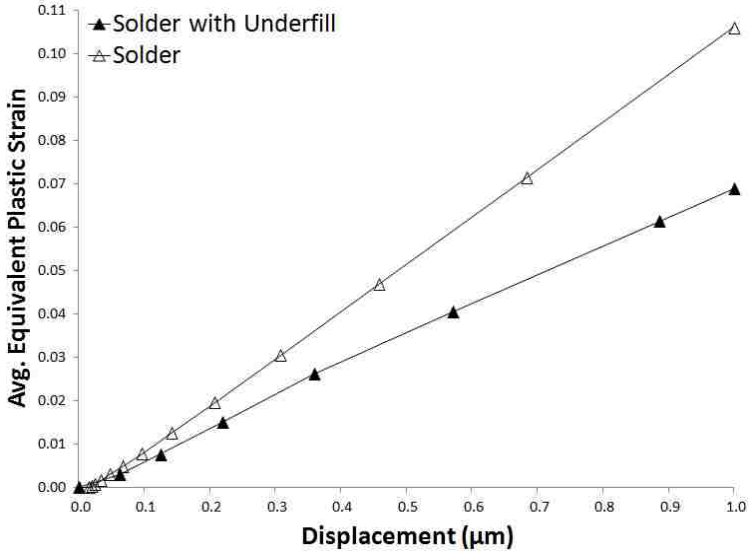


Figure 27: Equivalent plastic strains, averaged over the solder joint region, as a function of the applied shear displacement up to 1 μm, for the cases with and without an underfill layer around the joint.

4.3.3 Replacement of Solder by Intermetallic

When the solder layer in an actual micro-bump is thin, the reaction between the solder alloy and copper may transform the entire joint into an intermetallic compound layer during the post-soldering annealing process [3]. We therefore consider this special case by replacing the solder region with a Cu_6Sn_5 intermetallic layer. Figure 28 shows the contour plots of shear stress σ_{xy} generated in the chip/joint structure with an intermetallic joint when the applied shear displacement reaches 1 μm. Without an underfill layer, Figure 28(a), the maximum shear stress in the structure is about 450 MPa, with high stresses extending into the corners of Cu and Si. With underfill, Figure 28(b), the maximum shear stress is slightly higher, but the extent of high stresses in the Cu and Si corners has been reduced. The presence of the underfill layer aids in the resistance to shear and changes the subsequent location of maximum stress values in the chip/joint as also seen by examination of the stress contours on the backside of the TSV/micro-bump.

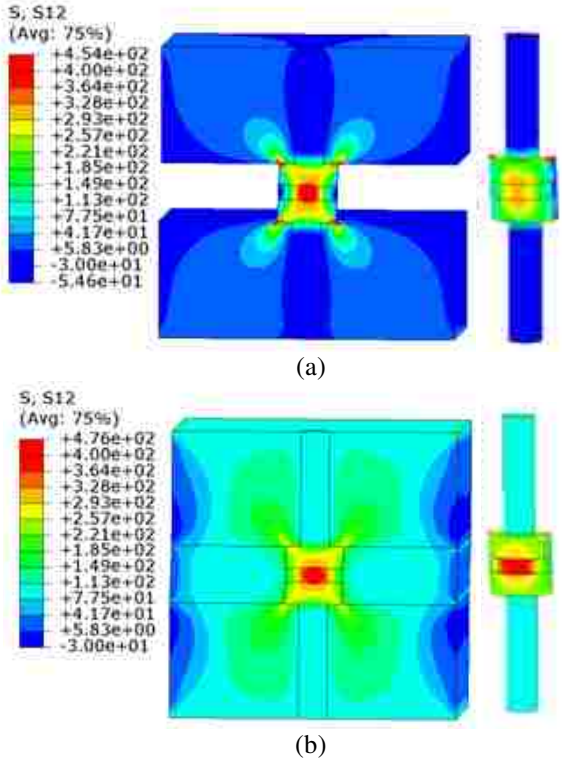


Figure 28: Contour plots of the shear stress σ_{xy} (MPa) at the maximum applied shear displacement of 1 μm when the solder joint is converted entirely into intermetallic. (a) The case without an underfill layer; (b) the case with an underfill layer around the joint.

Figure 29 shows the overall load-displacement response. By comparing the shear force magnitudes in Figure 29 and Figure 25, it is clear that, for the case without underfill, the "intermetallic joint" offers a higher resistance to shear deformation than the "solder joint." For the cases with underfill, the shear resistance is nearly identical between the two joint types since the shear load is primarily transferred between the Si layers by the underfill. Consideration of the local stress features in each case is also important. By comparing Figure 28 and Figure 24, the local shear stress increases considerably in the

chip/joint area when intermetallic replaces the solder for both cases with and without underfill. The shear stress σ_{xy} in the underfill adjacent to the micro-bump is found to be lower if the solder is completely replaced by intermetallic, approximately 100 vs. 150 MPa. The risk of debonding failure caused by the underfill is thus reduced, but the high stress in the intermetallic is concerning, reaching nearly 400 MPa in Figure 28(b).

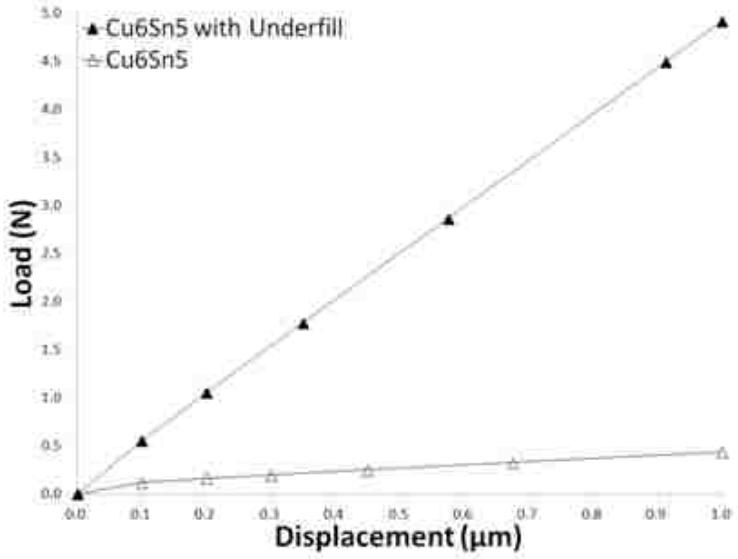


Figure 29: Load-displacement curves up to the applied shear displacement of 1 μm for the cases with and without underfill when the solder is converted entirely into intermetallic.

The maximum principal stress field also deserves attention. Figure 30 shows the contour plots of the maximum principal stress with an intermetallic joint when the applied shear displacement reaches 1 μm. For both cases, with and without an underfill layer, it can be seen that the tensile stress can reach beyond 400 MPa in the intermetallic joint. As a consequence, failure initiated at the intermetallic Cu joint is of concern. In addition, high tensile stresses are also observed in the corners of the Cu-Si interface,

which may have implications for the mechanical integrity of the Si (and the on-chip interconnects and dielectrics, which are not explicitly included in the model). In the case with underfill, Figure 30(b), the magnitude of the shear stress in the corners of the Cu-Si interface is reduced by approximately 50% as compared to the case without an underfill layer, Figure 30(a).

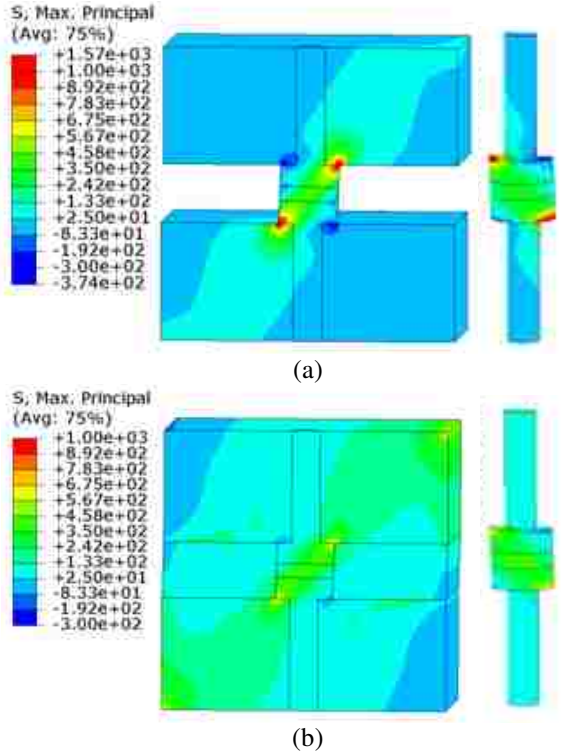


Figure 30: Contour plots of the maximum principal stress (MPa) at the maximum applied shear displacement of 1 μm when the solder joint is converted entirely into intermetallic. (a) The case without an underfill layer; (b) the case with an underfill layer around the joint.

Figure 31 shows the contour plots of equivalent plastic strain when the applied shear displacement reaches 1 μm. With the solder replaced by the stiff intermetallic, the Cu regions directly above and below the intermetallic now undergo plastic yielding which was not observed with a solder joint, Figure 26. The concern of permanent deformation

caused by misalignment thus still exists for intermetallic joints. Greater plastic strains are observed when there is no underfill.

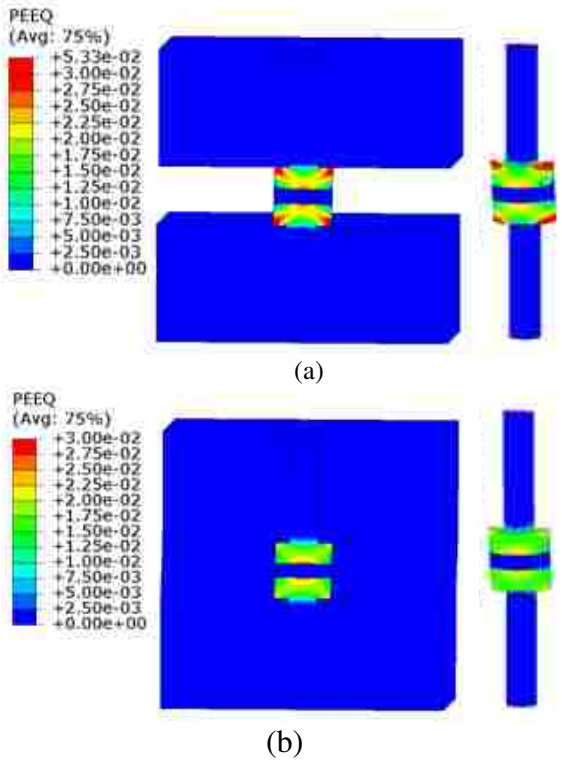
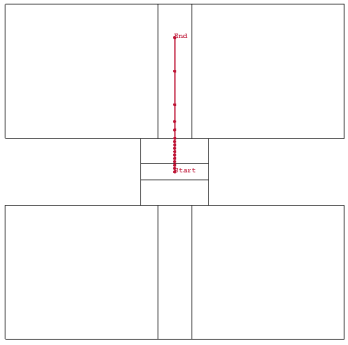


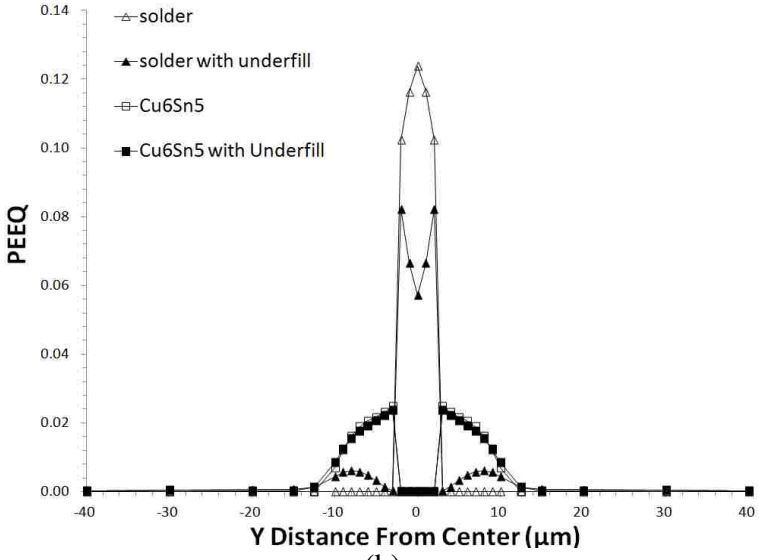
Figure 31: Contour plots of the equivalent plastic strain at the maximum applied shear displacement of 1 μm when the solder is converted entirely into intermetallic. (a) The case without an underfill layer; (b) the case with an underfill layer around the joint.

In order to provide additional insight into the propensity for damage in the TSV/micro-bump, the equivalent plastic strain was measured along a vertical path. The path starts at the center of the chip stack and extends to a vertical of 40 μm in the y-direction shown in Figure 32(a). Figure 32(b) shows the reported values of equivalent plastic strain throughout the TSV, copper portion of the micro-bump and solder or intermetallic regions. The case of solder without an underfill layer around the joint exhibits the highest value of equivalent plastic strain at the joint center which

corresponds to the contour plot in Figure 26(a). When underfill is introduced in the joint, the peek value of the equivalent plastic strain is reduced in the center of the solder region, Figure 32(b). The lack of plastic strain in the intermetallic corresponds to the contour plot in Figure 31, for the case when an intermetallic replaces the solder, the buildup of plastic strain shifts from the soft solder region into the copper portion of the micro-bump. It is interesting to note that far from the joint, greater than 15 μm, the value of equivalent plastic strain is near zero.



(a)



(b)

Figure 32: (a) Vertical path on 3D model used to report PEEQ values (zero is at the center of the model). (b) Line plot of PEEQ due to 1 μm shear displacement for the cases where the joint is solder, or intermetallic, with and without underfill respectively.

4.3.4 Comparison with Thermal Mismatch Induced Deformation

In this section we present select results on stress and deformation fields induced by thermal expansion mismatches after a simple cooling process from 250 to 20ºC. When making comparisons with the shear loading results, we use the maximum shear displacement of 1 μm as a basis. It is understood that, if the prescribed shear displacement is smaller, the extent of internal deformation will also be smaller. The same model configuration as in Figure 22 is used, with the purpose of examining the different nature and extent of deformation caused by temperature excursion as compared to mechanical shear.

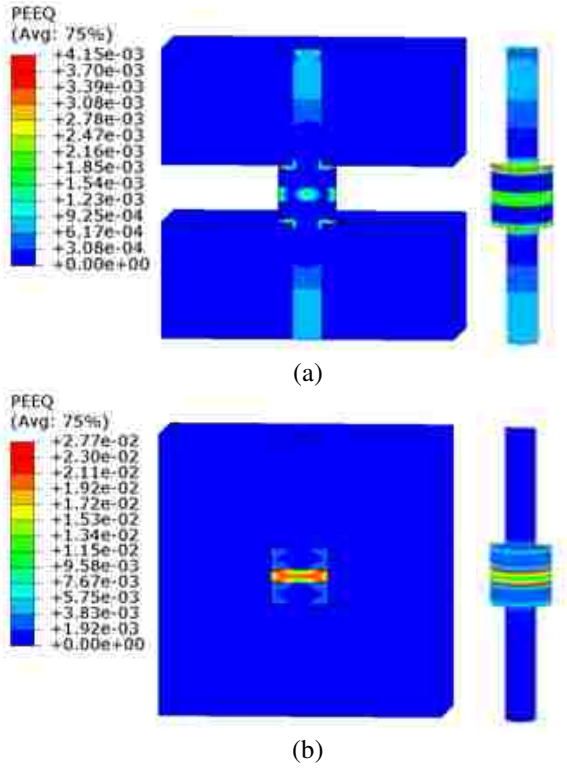


Figure 33: Contour plots of the equivalent plastic strain after thermal processing (a) for the case without an underfill layer, and (b) for the case with an underfill layer around the joint.

Figure 33 shows the contour plots of equivalent plastic strain due to thermal mismatches, when the center layer of micro-bump is the soft solder alloy. Without the underfill, Figure 33(a), the maximum equivalent plastic strain is located around an annular region at the interface of the Cu bump and the Si. If underfill exists, Figure 33(b), the maximum equivalent plastic strain becomes highly amplified in the solder joint due to its CTE mismatch with the surrounding underfill. Unlike the case of misalignment-induced shear, Figure 26, plastic deformation due to thermal strains now occurs in the Cu TSV far from the joint. Since the Cu TSV is surrounded by Si with a much lower CTE, significant tensile stresses exist. Plastic strain cannot be seen in the contour plot for the underfill case, Figure 33(b), due to the chosen strain scale. However, far from the joint the magnitude is the same as in Figure 33(a). Compared with deformation caused by the 1 μm shear displacement, Figure 26, thermally induced plastic strains in the solder are significantly smaller.

With the solder region entirely replaced by the intermetallic, plastic deformation occurs only in the Cu bump and TSV as shown in the equivalent plastic strain contours in Figure 34. Plastic strains in the Cu region inside the micro-bump are much smaller compared to those due to shear, Figure 31. Without an underfill layer, Figure 34(a), the maximum equivalent plastic strain is located around an annular region at the interface of the Cu bump and the Si which is very similar to the pattern seen for a solder joint, Figure 33(a). With an underfill layer, Figure 34(b), plastic deformation in the Cu regions directly above and below the intermetallic is enhanced in comparison with the case of no underfill, Figure 34(a).

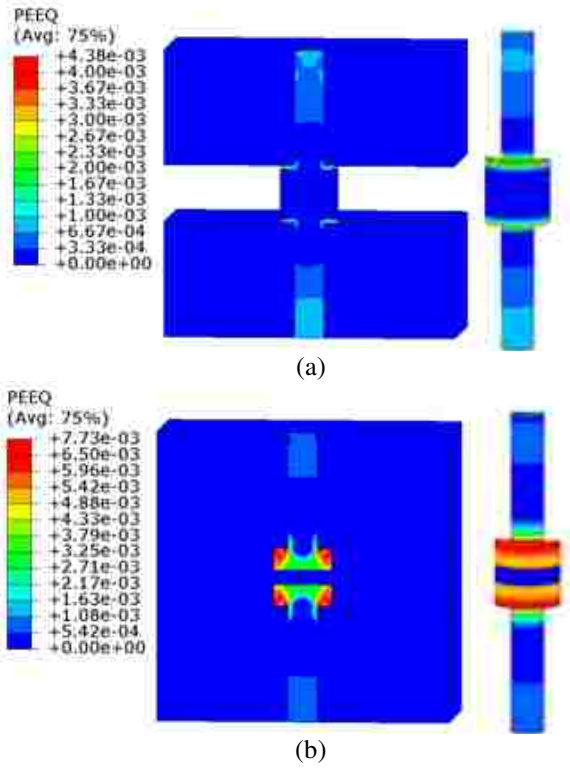


Figure 34: Contour plots of the equivalent plastic strain after thermal processing when the solder joint is converted entirely into intermetallic. (a) The case without an underfill layer; (b) the case with an underfill layer around the joint.

Attention is now turned to the maximum principal stress generated due to thermal strains. Figure 35 shows the contour plots of the maximum principal stress in the chip/joint structure after cooling. The corresponding figures for the intermetallic joint are shown in Figure 36. The maximum tensile stresses inside the Cu TSV, away from the joint, are comparable in Figure 35 and Figure 36 regardless of the existence of an underfill layer. The stress in the Cu TSV is dominated by its CTE mismatch with the Si chip. The stress distribution in the joint, however, is affected by the existence of an underfill layer. Stresses inside the intermetallic, Figure 36, are much lower than those due to overall mechanical shear, Figure 30. Because of the relatively high CTE, compared to

the other materials in this study, the underfill is under tension after cooling, Figure 35(b) and Figure 36(b). As for the Si chips, the maximum tensile stresses due to thermal processing are much lower than those caused by shear, Figure 30, when the joint material is entirely intermetallic.

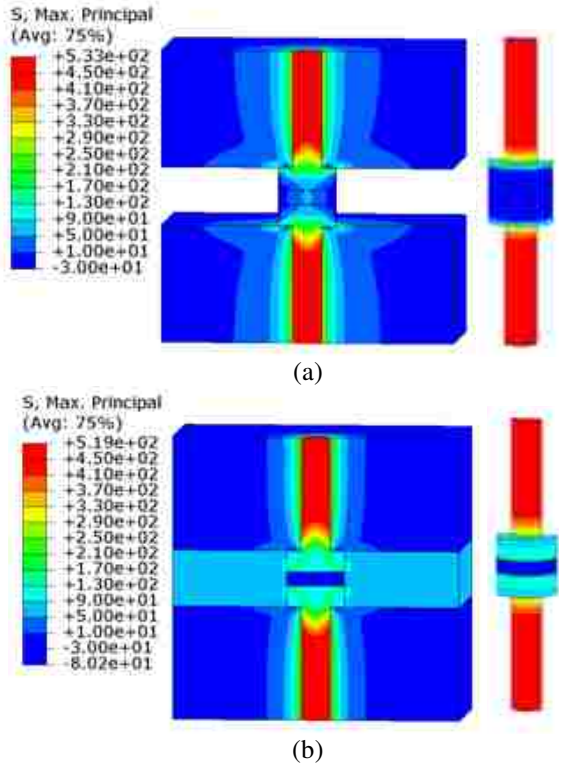
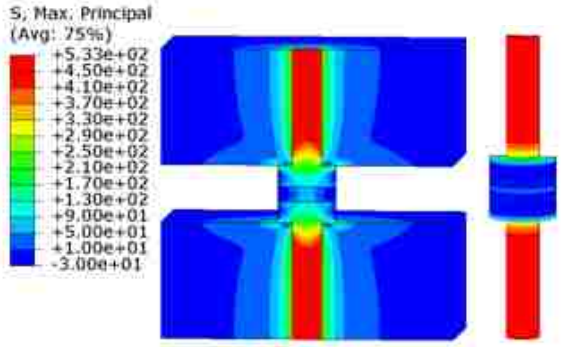


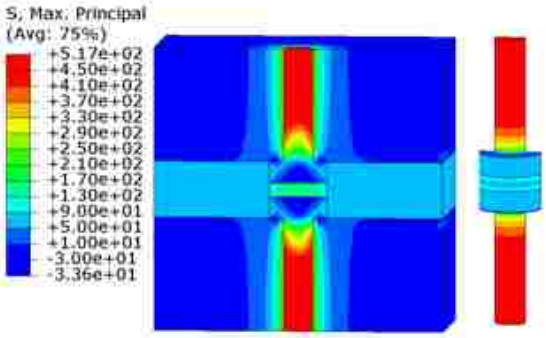
Figure 35: Contour plots of the maximum principal stress (MPa) after thermal processing (a) for the case without an underfill layer, and (b) for the case with an underfill layer around the joint. The center layer of the joint is solder.

Results presented in this section differ from those presented earlier in Chapter 3 for thermal mismatch of the 2D modeling case. A discrepancy appears between the 2D and 3D models when comparing results from the simulated thermal loading. This is mainly because that, in the 2D plane strain formulation, high tensile stresses in the out-of-plane

direction are artificially induced, which contributes to excess deviatoric quantities and thus greater plastic deformation than in an actual 3D setting. A 3D model is therefore needed to correctly predict thermal stresses as well as buildup of plastic strain in the TSV and around the micro-bump. On the other hand, for pure shear loading, the 2D and 3D results, presented in Chapters 3 and 4, respectively, are quantitatively very similar.



(a)



(b)

Figure 36: Contour plots of the maximum principal stress (MPa) after thermal processing when the solder is converted entirely into intermetallic. (a) The case without an underfill layer; (b) the case with an underfill layer around the joint.

Line plots reporting the buildup of plastic strain along a vertical path in the 3D IC are presented for the thermal processing case, Figure 37. The same vertical path used to report values of equivalent plastic strain for the shear case is used, Figure 32(a). Figure 37 shows the reported values of equivalent plastic strain throughout the TSV, copper

portion of the micro-bump and solder or intermetallic regions after thermal processing. The case of solder with an underfill layer around the joint exhibits the highest value of equivalent plastic strain. When underfill is removed from the joint, the peek value of the equivalent plastic strain is reduced in the center of the solder region, Figure 37, a result that is opposite to that found in the shear loading case. The lack of plastic strain in the intermetallic corresponds to the contour plot in Figure 34, for the case when an intermetallic replaces the solder. It is interesting to note that the buildup of plastic strain occurs in the TSV for all four cases and is relatively independent of joint material or the possibility of an underfill layer around the joint. The buildup of plastic strain in and around the joint is highly dependent upon the possibility of an underfill layer.

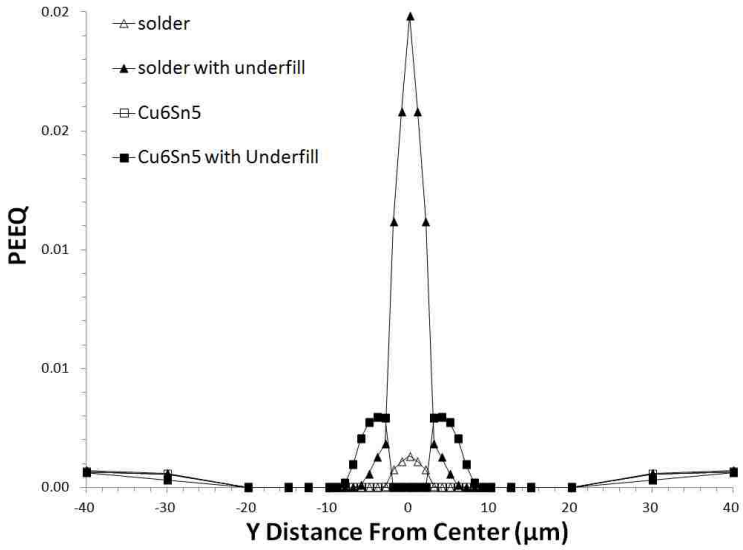


Figure 37: Line plot of PEEQ along the center of the 3D IC after thermal processing for the cases where the joint is solder, or intermetallic, with and without underfill respectively.

4.4 Conclusions

Important findings, from the three-dimensional analyses, on the stress and deformation fields, overall mechanical response, and damage propensity of the chip stack are summarized below.

- Misalignment-induced shear deformation poses strong influences on the stresses and deformation in the vicinity of micro-bump, while thermal mismatches have also the ability to influence the TSV regions away from the joint.

- The existence of an underfill layer around the joint significantly raises the shear force required to attain a given overall shear displacement. Underfill also leads to a reduction in solder plasticity and thus the propensity for ductile failure. The underfill material, however, can experience high shear stresses, which, in conjunction with the localization of plastic strain along the solder boundary, imply the risk of interface damage around the joint.

- If the solder alloy is entirely transformed into an intermetallic material, high shear and tensile stresses develop in the intermetallic and in nearby regions of copper and silicon. High tensile stresses in the intermetallic imply that brittle failure may become a concern under shear deformation.

- Accumulation of plastic strain occurs in the softest material in the micro-bump; namely in the solder region, or in the Cu bump region when intermetallic replaces the solder.

- When underfill is present during thermal cooling, relatively large plastic deformations accumulate in the solder joint due simply to CTE mismatch.

Chapter 5 Conclusions and Future Work

5.1 General Conclusions

Misalignment-induced shearing and thermal mismatch effects on 3D IC packages with TSV interconnects were studied through a series of finite element analyses. First, a 2D model of a representative chip stack was analyzed. Shearing results and mechanical response curves were presented for different solder thicknesses with and without an underfill layer around the joint. For the 2D model, a special case of an intermetallic replacing the solder entirely was also reported. Thermal loading results with both solder and an intermetallic joint were also presented for only the thinnest joint case. Secondly, a 3D model of the representative chip stack was analyzed. Similar studies were preformed on the 3D chip stack to those for the 2D model. However, the possibility of variation in the solder joint thickness was not included for the 3D model. In both modeling cases, the reliability of the IC stack was assessed by examining the local stresses in the Si, underfill, Cu and solder or intermetallic regions. Potential for damage initiation in the TSV and micro-bump was measured by the buildup of plastic strain in the solder or Cu regions. In the shear loading cases, the 2D and 3D models provide similar stress and deformation trends. A discrepancy appears between the 2D and 3D models when comparing results from the simulated thermal loading. A 3D model is needed to correctly predict thermal stresses as well as buildup of plastic strain in the TSV and around the micro-bump. The

2D model suffers from the plane strain assumption providing misleading results predicting the thermal behavior of the chip stack and TSV. Some specific findings on the stress and deformation fields, overall mechanical response and damage propensity of the chip stack are summarized below.

- With a constant micro-bump size, a thinner solder layer sandwiched between copper pads displays a better mechanical resistance to overall shear. However, thinner solder is more susceptible to damage initiation due to faster buildup of local plastic strain.

- Misalignment-induced shear deformation strongly influences the stresses and deformation in the vicinity of micro-bump, while thermal mismatches have the ability to influence the TSV in regions away from the joint.

- The existence of an underfill layer around the joint significantly raises the shear force required to attain a given overall shear displacement. Underfill also leads to a reduction in solder plasticity and thus the propensity for ductile failure. The underfill material, however, can experience high shear stresses, which, in conjunction with the localization of plastic strain along the solder boundary, imply the risk of interface damage around the joint.

- If the solder alloy is entirely transformed into an intermetallic material, high shear and tensile stresses develop in the intermetallic and in nearby regions of copper and silicon. High tensile stresses in the intermetallic imply that brittle failure may become a concern under shear deformation.

- The accumulation of plastic strain occurs in the softest material in the micro-bump; namely in the solder region, or in the Cu bump region when an intermetallic replaces the solder.

It is believed that the present study can serve as useful guidance for the design and reliability assessment in 3D ICs.

5.2 Suggested Future Work

In order to accurately predict stresses and damage propensity in a representative 3D IC, convergence of the numerical model should be confirmed. As one seeks to predict stresses and damage propensity in a realistic 3D IC, not just provide general trends, certainty of the numerical models becomes more important to those making design decisions bases upon simulation results.

In the simulations presented, misalignment-induced shear deformation of the TSV and solder micro-bumps was studied through an applied shearing action. In order to better understand the mechanical behavior of the 3D chip stack during processing, a combined loading scenario including both shearing and tensile or compressive forces should also be studied.

The current study focuses on the trends of stresses and deformations in and around the TSV micro-bump region. A detailed analysis of stresses in the Si chip layers was not specifically studied. Since mechanical stresses in the Si chip inhibit the electron mobility and thus the device electrical performance, studying the stresses in Si as a function of distance from a single TSV would be valuable. Predicting a minimum “keep away zone”

for the location of devices located near a single TSV would allow designers to maximize the number of devices and TSVs on any chip layer.

In real 3D chip stacks, many vertical paths are needed for signal and power interconnects between the multiple chip layers. Studying the pattern and spacing of TSV interconnects through the Si chip layers would prove useful in predicting trends and possible upper bound on TSV density without impaired electrical performance.

A simplified cylindrical geometry of the 3D chip stack was employed to study the trends of stress and deformations in and around the TSV and micro-bump region. Modeling a realistic tapered geometry for TSV and micro-bump would prove useful in predicting more accurate stresses and deformations. Due to manufacturing processes, the actual TSV geometry can be tapered along the length and not perfectly cylindrical as modeled in this study. The actual geometry of the solder joint in the micro-bump is spherical in shape and not purely cylindrical. The assessment of 3D IC reliability would improve by examining the buildup of plastic strains in the TSV and micro-bump regions with realistic geometry.

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