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GROWTH, PROCESSING AND CHARACTERIZATION OF GALLIUM NITRIDE BASED COAXIAL LEDS GROWN BY MOVPE

by

ASHWIN KRISHNAN RISHINARAMANGALAM

B.Tech., Electrical Engineering, The Indian Institute of Technology, Madras, July 2006

DISSERTATION

Submitted in Partial Fulfillment of the Requirements for the Degree of

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July, 2012

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DEDICATION

This work is dedicated to my mother, Mrs. R. Kala Krishnan and my father, Mr. R.V. Krishnan, whose continued support and push for tenacity throughout my life has been unparalleled.

This work is also dedicated to my teachers and near and dear friends, who have taught me the meaning of life through both, forgettable and unforgettable incidents.

Finally, I dedicate this work to the almighty lord.

विद्या ददाति विनयं

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In the end, I would like to thank the almighty god for everything my life has to offer.

- Ashwin Rishinaramangalam

Albuquerque, NM

July 2012

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[1]Robert Hall

[2] Michael J. Fox

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ABSTRACT

Gallium nitride (GaN) based coaxial (core-shell type) light emitting diodes (LEDs) offer a wide range of advantages. The active region of these LEDs is located on non-polar, $\{1\bar{1}00\}$ m-plane GaN sidewalls, which helps eliminate the quantum confined Stark effect (QCSE) and improve the radiative recombination efficiency of LEDs. The recent evolution of a catalyst free, scalable, repeatable and industrially viable device quality GaN nanowire and nanowall metal organic vapor phase epitaxy (MOVPE) growth process has enhanced the possibility of these LEDs going into production from laboratory.

Previous work has shown that these nanowires exhibited an intense photoluminescence (PL), in spite of their large surface-area to volume ratio, and lasing was observed when these nanowires were optically pumped at high intensity. In this dissertation, it is shown that as long as the GaN three dimensional (3D) structures have their critical dimension below a micron, the threading defect (TD) density along the c-direction approaches zero. A TD that enters into this structure bends towards the surface

($\{1\bar{1}00\}$ m-plane side wall) in its vicinity, thereby reducing its dislocation line energy. The possibility of growing zero defect GaN templates is extremely important in the breakdown voltage improvement, the reverse bias leakage current reduction and efficiency droop reduction.

This growth method has also been extended to device quality micron sized features, thereby presenting us with opportunity to study and explore LEDs of different sizes and shapes. In addition to the microstructure growth, two different repeatable approaches have been identified and demonstrated for the microelectronic processing of these micron-sized LEDs. Despite being far from perfect, the characterization results obtained from these LEDs have been encouraging. The technological challenges associated with the fabrication of the coaxial LEDs are also discussed in this dissertation.

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Chapter 1

Introduction

Energy saved is energy generated. In addition to improved financial capital and environmental quality, the conservation of energy sources is extremely important for increased personal security and human comfort. Light Emitting Diodes (LEDs) are poised to play a very important role in this effort. As per the Energy Efficiency and Renewable Energy (EERE) program of the Department of Energy (DOE), USA, LED lighting technology is bound to reduce the U.S. light energy expenditure by about one-quarter and contribute significantly to the nation's climate change solutions. In terms of capital, it is estimated to save about $120 billion in energy costs over the next two decades and avoid 246 million metric tons of carbon emission over the same period [1].

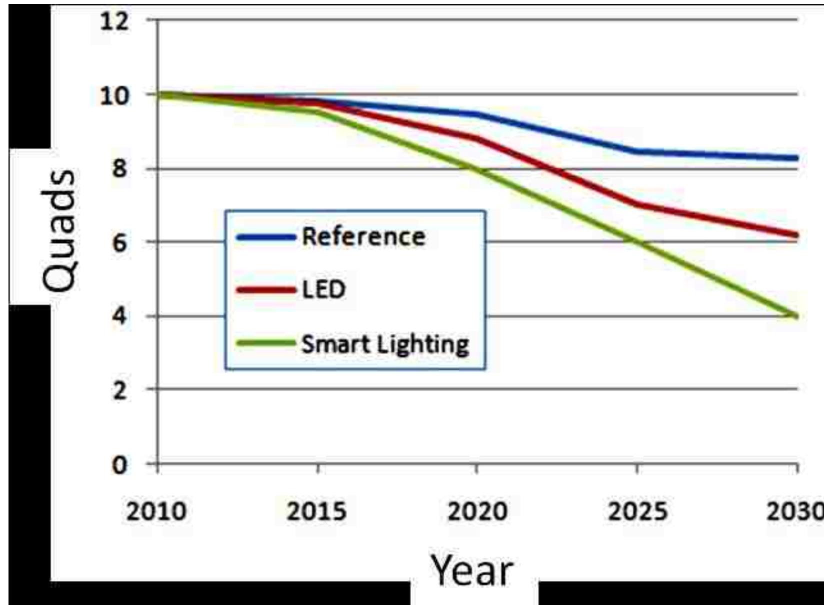

Fig. 1.1 The comparison of the energy savings proposed by DOE upon using of LEDs and the savings that is possible using smart lighting sources, graph reproduced from [2]. 1 Quad is defined as equal to 172million barrels of oil

However, simple LED bulbs replacing the incandescent lamps and compact fluorescent lamps are not the only solution to the world's energy problems. An LED light source with a control system is what the future world would be looking at, to meet the DOE's roadmap. This is one of the visions of the NSF funded Smart Lighting Engineering Research Center (SLERC). A smart lighting system should be designed in such a way that it can be more efficient, healthier and more interactive than the simple electric bulbs of today. Smart Lighting Systems would include the ability to measure and control the intensity, color, polarization, and modulation of light to enable new lighting functionality. The control system would also decide when the light would be on or off. Once successful, this lighting system that is fully controllable would deliver at least two times the energy savings of the conventional first wave LED lighting technology, as shown in Fig. 1.1. This would be roughly equivalent to the elimination of over 300 coal powered plants with the reduction in greenhouse gas emissions and air pollution and decrease in America's dependence on foreign energy sources [2]. Gallium Nitride (GaN) material system has been used in manufacturing of visible blue LEDs and laser diodes for over two decades, ever since technologists have dreamt of a full spectrum solid-state lighting future. In the following sections, LEDs based on the GaN material system, the various factors affecting their performance and the requirements for a highly efficient, high power LED are discussed.

1.1 LEDs based on GaN material system

The binary compound semiconductor GaN is a direct band gap material with a band gap of 3.39eV at 300K. This band gap corresponds to the 364nm wavelength, which falls in the ultraviolet range. The process of alloying GaN with aluminum (Al) would

result in increasing the band gap from 3.39eV until 6.1eV, which is the band gap of aluminum nitride (AlN). Hence, most of the UV LEDs have now been manufactured by alloying a little percentage (x) of aluminum to GaN to form $Al_xGa_{1-x}N$ [24, 25, 26]. This alloyed material when used in the LED active region would generate UV light of wavelengths below 364nm. However, upon alloying GaN with indium (In), the band gap can be reduced; thereby the emission wavelength of the LEDs can be increased, so as to emit in the visible region. The alloying of GaN with indium would result in decreasing the band gap from 3.39eV till about 0.7eV, which corresponds to the band gap of InN. Blue LEDs have now been highly developed and considerably efficient with indium percentage (x) in $In_xGa_{1-x}N$ of about 15-20%. However, there aren't any LED chips that provide highly efficient LED operation from the green (>500nm emission wavelength) through to the red with semiconductor alloys made from the AlGaInN materials system. This is typically referred to as the "Green Gap" problem. In addition to this, another issue plaguing today's GaN based LEDs is "efficiency droop". The drop in the external quantum efficiency of the LEDs when they are operated at high power is called efficiency droop. To understand these problems, it is first worth looking into some of the important aspects of substrates, growth and processing of GaN based LEDs discussed in the following sub-sections.

1.1.1 Crystallographic orientations in wurtzite GaN

There are three common crystalline structures shared by GaN and its family; wurtzite, zincblende and rocksalt structures. The wurtzite structure is the most thermodynamically stable structure for group-III nitrides and wurtzite GaN and its ternary alloys are the most commonly used material for making visible and deep UV

LEDs and laser diodes. The wurtzite GaN structure is a combination of two hexagonally close packed (HCP) sub-lattices, each with either Ga (Al or In) or N [20]. Some of the different crystallographic orientations in the wurtzite crystal structure have been shown in Fig. 1.2(a). Because of the asymmetry, the wurtzite crystals have two lattice constants, ‘a’ in the c-plane and ‘c’ perpendicular to the c-plane of the wurtzite crystal shown in Fig 2.

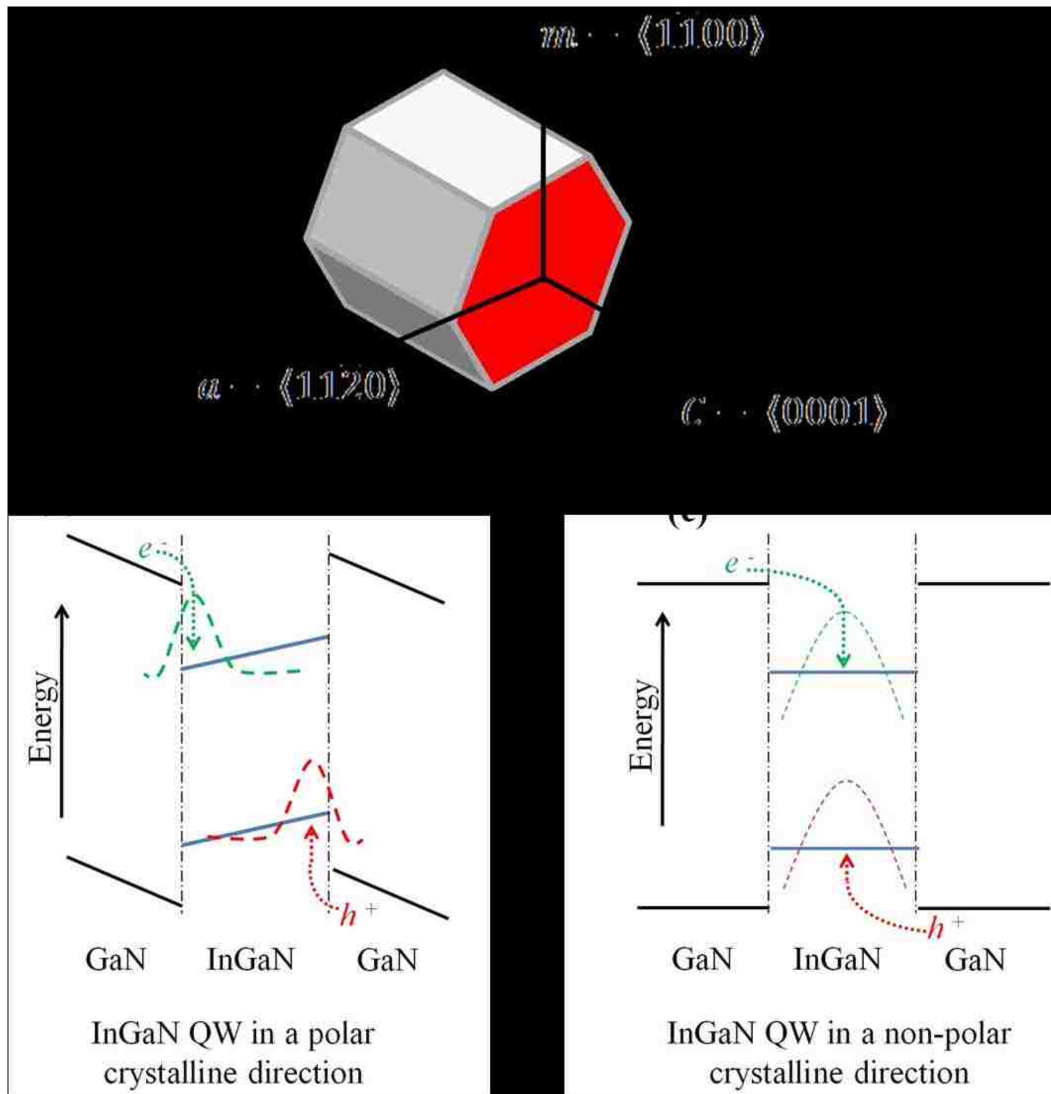

Fig. 1.2 (a)Some of the important crystallographic orientations in wurtzite GaN and energy band diagram of InGaN QW sandwiched by GaN barrier layers, showing QCSE (b) in c-plane structures and absence of QCSE (c) in m-plane structures

In GaN, the covalent bond between a 'Ga' atom and an 'N' atom is in reality, partially ionic [4, 5]. This leads to a significant spontaneous polarization electric field in the c-oriented GaN crystals. The strong electro negativity of 'N' leads to the localization of the electron cloud near the 'N' atom, hence creating a partial negative charge on the atom. This leads to a partial positive charge on the Ga atom and thus a dipole is created, which leads to a spontaneous polarization electric field in the material by itself. In case of heterostructures (for e.g. GaN/$In_xGa_{1-x}N$/GaN as shown in Fig. 1.2) grown in the c-direction, the wurtzite semiconductor nitrides lack inversion symmetry and hence exhibit these piezoelectric fields when strained along the <0001>. The strain is the resultant of the lattice mismatch between GaN and $In_xGa_{1-x}N$. The lattice mismatch, together with the spontaneous polarization, is manifested as polarization charges at the heterojunction interfaces. The resultant electric field due to these polarization charges at the interface causes band bending even during flat band conditions and forces the carriers to opposite ends of the quantum well as shown in Fig. 1.2(b). The disruption of flat band condition in the quantum well leads to a lesser electron-hole spatial overlap and a lower band gap as compared to the quantum well. This phenomenon is known as the quantum confined stark effect (QCSE). The lesser electron-hole spatial overlap leads to lower electron-hole recombination (lower internal quantum efficiency) than that is anticipated under forward bias diode turn on conditions. As the forward bias voltage is increased, the bent bands shown in Fig. 1.2(b) start to flatten out, thereby increasing the effective band gap of the quantum well, leading to a blue-shift in the electroluminescence emission. This polarization electric field is increased as the percentage of indium in $In_xGa_{1-x}N$ is increased, thereby leading to a poor green emission, in comparison to blue LEDs. This is

one of the reasons for the “Green Gap” problem. One way to tackle this is to make the quantum well thin (~2.5nm), so as to make sure there is a significant spatial overlap of the carrier distributions. The order of thickness required is far less than the conventional zinc blend quantum well sizes. Thus, there is a clear trade off required between carrier separation in the wells that favors thin wells and good confinement and photogeneration that favors thicker wells.

The $\langle 1\bar{1}00 \rangle$ direction (vector corresponding to the m-plane GaN), however, lacks the piezoelectric field that is always present in the [0001] direction. Thus, the band bending is now eliminated in the flat band condition, which promotes better spatial overlap of the electron and hole distributions, as shown in Fig. 1.2(c). These crystallographic orientations that lack the spontaneous polarization electric field are often described as non-polar orientations. Kim *et al.* [11] fabricated and demonstrated a thick InGaN MQW LED on $\{1\bar{1}00\}$ m-plane non-polar GaN substrate. It was shown that the LED had external quantum efficiency (EQE) of 45% at pulse driven conditions. The EQE remained within 10 % of the 20mA value, even at higher currents. Kim *et al.* also demonstrated m-plane LEDs that showed absence of polarization electric fields. The peak emission wavelength was plotted versus the drive current. As the drive current increased, there was no blue shift observed, which is the typical signature of the QCSE in c-plane GaN based LEDs, as described earlier.

1.1.2 Growth of wurtzite group-III nitrides and origin of threading defects

GaN is not natively available in nature. This is due to the low solubility of nitrogen in gallium and the higher vapor pressure of nitrogen on GaN [20]. As a result of this, the bulk GaN growth must resort to high temperature and high pressure growth

procedures. There is no process known till date of producing bulk GaN substrates by Czochralski and Bridgman-Stockbarger techniques that is available for most other III-V semiconductors. Hence, there is a need to grow GaN and its family of semiconductors heteroepitaxially on other natively available substrates that also have a wurtzite structure.

Table 1.1 Comparison of three common substrates used to grow c-plane wurtzite GaN

	Sapphire	**SiC**	**Silicon**
$\Delta a/a_o$ (%)	-13.8	-3.5	17
Electrical Conductivity	insulating	n-type SiC is a semiconductor	semiconductor
Cost	cheap, up to 6”	expensive	cheap

Most of the GaN commercial LEDs and Laser Diodes (LDs) are grown on c-plane sapphire, which also has a hexagonal lattice like that of GaN. In addition to sapphire, silicon carbide and silicon (111) are some of the substrates on which the growth of c-plane GaN is being carried out, both in industry and research. Table 1.1 compares the different substrates that are used to grow c-plane GaN. The lattice mismatch of c-plane GaN with respect to c-plane sapphire is about 30% at 300K with respect to the ‘a’ lattice parameter. However, when c-plane GaN is grown on c-plane sapphire, the observed lattice mismatch is about 16% at 300K. This is because the smaller cells of aluminum atoms on the c-plane sapphire are oriented 30° away from the larger sapphire unit cell as shown in Fig. 1.3.

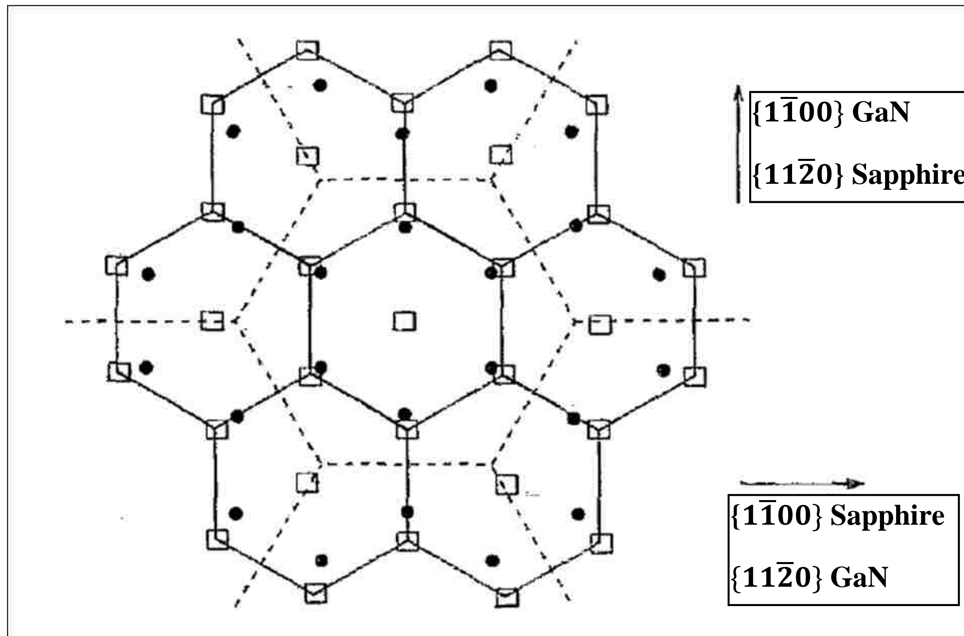

Fig. 1.3 The projection of bulk c-plane sapphire and GaN showing the Ga atoms in GaN and Al atoms in sapphire for the observed epitaxial growth orientation, figure reproduced from [3]. The black circles are Al-atom positions and the dashed lines represent sapphire c-plane unit cell. The squares are Ga-atom positions and the solid lines represent the GaN c-plane unit cell.

GaN thin films were first epitaxially grown by Maruska and Tietjen in 1969 using the reaction of gallium monochloride (GaCl) with ammonia (NH_3) [27]. Ever since, a lot of methods like hydride vapor phase epitaxy (HVPE), metal organic vapor phase epitaxy (MOVPE, also known as metal organic chemical vapor deposition, MOCVD) and molecular beam epitaxy (MBE), have been used to grow GaN thin films on sapphire. Nakamura *et al.* [10] designed an atmospheric pressure MOCVD reactor for nitride growth, which has formed the basis of a lot of the MOCVD reactors used for group-III nitride growth. The ability to perform repeatable device quality single crystalline epitaxial growth has made MOCVD the widely used technique in industry to grow GaN. Trimethyl gallium (TMG), trimethyl aluminum and trimethyl indium are the respective group-III precursors used for gallium, aluminum and indium respectively, while ammonia

NH_3 is typically used precursor for nitrogen. GaN and AlxGa1-xN ternary alloys are normally grown at temperatures in excess of 900°C to about 1100°C. However, the growth of $In_xGa_{1-x}N$ ternary alloys is normally carried out at lower temperatures in the range of 650°C-800°C. However, GaN ({0001} c-plane) has also been grown on c-plane sapphire by reactive atom source MBE [38, 39, 40, 41 and 42]. The most important aspect of the MBE growth of GaN is the ability to grow device quality single crystalline material at lower temperatures, in comparison to HVPE or MOVPE. Yoshida *et al.* [38] were one of the first to grow GaN on sapphire by reactive MBE using a two-step process. Firstly, an aluminum nitride (AlN) wetting layer (buffer layer) was deposited on the c-plane sapphire wafer at 1100°C. Following this, the temperature of the substrate was reduced to 700°C and GaN was epitaxially grown. Lei *et al.* [39] were one of the first to grow epitaxial films of wurtzite GaN on (001) silicon using MBE (electron cyclotron resonance (ECR) assisted plasma). The epitaxial GaN film was grown in two steps in a Varian GenII MBE system with an ECR source attached to one of its effusion cell ports. Firstly, a GaN-buffer was grown at low temperature (175-400°C) following which, the temperature was raised to about 600°C and the rest of the GaN film was grown at the higher temperature. In case of HVPE or MOVPE, ammonia has been used as the chemical source of nitrogen. However, predissociation of nitrogen has been employed as the basic technique of providing the nitrogen flux in MBE reactors. In the above growths mentioned, the cracking of gas source (NH_3 or N_2) was determined to be the growth rate-limiting step, mainly due to the large binding energy of molecular nitrogen (9.5 eV) that makes it extremely challenging to be used as a gas source for nitride based MBE growth systems.

Heteroepitaxy of GaN on lattice mismatched substrates results in the GaN being strained on the substrate. For thickness beyond the critical thickness of GaN on sapphire, GaN relaxes and the strain energy is released by the formation of threading defects in the order of $10^8 – 10^{10}$ cm^{-2} as shown in Fig. 1.4. In addition to this, the thermal expansion coefficient of sapphire is far higher than that of GaN, thereby leading to cracking of thick films [16].

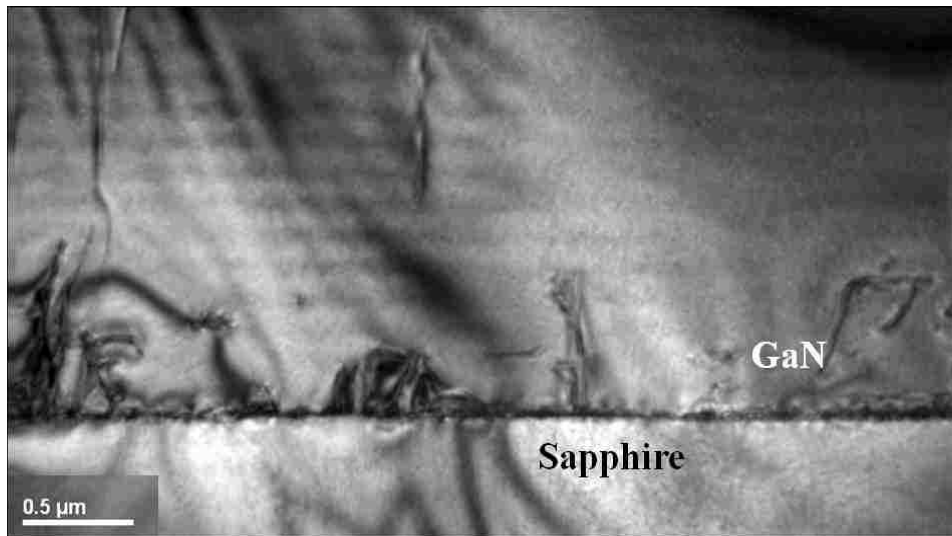

Fig. 1.4 TEM micrograph of the c-plane sapphire-GaN interface showing the threading defects originating at the interface due to the lattice mismatch between sapphire and GaN

The threading defects propagate along the material until they reach the surface where the defect energy is released. Hence, it is highly likely to find threading defects in the active region of the LED. The high density of threading defects are thought to be the reason for the failure of GaN lasers [10] and the electrical breakdown of GaN p-n junctions [17]. They also play an important role in the increase of the reverse leakage current in LEDs [9]. Although, papers have been published indicating the internal quantum efficiency being immune to the threading defect density [7, 8], Dai *et al.* [28]

have demonstrated that the IQE is significantly dependent on the threading defect density. They performed room temperature photoluminescence measurements on InGaN/GaN multi quantum well (MQW) heterostructures to verify this.

The threading defects entering the $In_xGa_{1-x}N$ quantum well also result in the generation of V-shaped defects that cause higher index facet growth at a reduced growth rate and thus result in pit formation [6]. This is more pronounced as the percentage of indium (y) in $In_yGa_{1-y}N$ is increased. Hence, the elimination of threading defects is one more potential solution to the "Green Gap" problem. Nguyen *et al.* [35] have recently evaluated the IQE of their defect-free nanowire LEDs, wherein they have been successful in demonstrating nearly zero efficiency droop at current densities of 640A/cm^2. Therefore, threading defect elimination could also present us with a potential solution to reduce, if not eliminate, the efficiency droop. New growth techniques are being devised to try reducing the threading defects. Nanoheteroepitaxy [18] has been proposed for a long time as one of the potential solutions for defect density reduction. This technique exploits selective epitaxial growth methodology using modern lithography methods for the patterning. This type of selective area growth (SAG) followed by lateral epitaxial overgrowth (also known as ELOG) has shown tendencies to be successful in limiting the defects by localizing them to selected regions of the wafer [19]. Two sets of devices, one grown on sapphire and the other grown on epitaxial laterally overgrown GaN substrates, were compared by Nakamura *et al.* [10]. The devices on the lower defect ELOG substrate had an operation time in the excess of 10,000 hours and 9nA reverse current at -20V, while that on sapphire had only around 300hrs of operable time and 1μA reverse current at -20V, respectively. Ferdous *et al.* [14] demonstrated an exponential increase in the

reverse leakage current density with increase in the defect density. It was also demonstrated that most of this leakage current was flowing through the device and not its surface. Hence, it can be concluded from the above observations that reducing the threading defect density would result in improving the device performance in a lot of ways.

1.1.3 Requirements for a highly efficient, high power droop free LED

In summary, the requirement of an LED based on GaN is that it should be highly efficient and it should be able to emit at high drive currents with constant internal quantum efficiency. In principle, the efficiency of GaN based LEDs can be improved by improving the recombination rate of the electrons and holes in the active region of the LED. This could be achieved by providing a better spatial over lap of the electrons and holes in the quantum wells by eliminating the QCSE. In other words, growing quantum wells on the non-polar GaN crystallographic orientations would lead to a better spatial overlap of electrons and holes in the active region. However, the methods of growing non-polar GaN and their ternary alloys are not very straight forward as growing c-plane GaN on c-plane sapphire. $\{1\bar{1}00\}$ m-plane GaN has been grown on other substrates like γ-$LiAlO_2$ (100) [30] by Sun *et al.* However, these γ-$LiAlO_2$ substrates are thermally and chemically unstable, which makes their preparation prior to the growth and the actual growth very difficult [29]. γ-$LiAlO_2$ has been restricted to use only in MBE because of its instability at the MOCVD growth conditions. γ-$LiAlO_2$ is actually a mixed oxide (mixture of lithium Oxide (Li_2O) and aluminum oxide(Al_2O_3)) that decomposes at temperatures around 1040^oC into its constituents. The lithium oxide is volatile and escapes as a gas under the MOCVD growth conditions. Thus, it is difficult to use γ-

$LiAlO_2$ as a viable growth substrate for MOCVD growth of GaN. Moreover, γ-$LiAlO_2$ is at least three times more expensive as compared to c-plane sapphire. Hang *et al.* [34] have recently demonstrated the growth of m-plane GaN on γ-$LiAlO_2$ by MOCVD too, but have reported similar instability issues. Thus, there is a need for different strategies to grow m-plane GaN in a cheaper and a much more reliable manner. The efficiency can be further improved by eliminating the threading defects in the active region of the LED. The elimination of threading defects would not only lead to higher internal quantum efficiency, but also would lead to a lower reverse leakage current, a higher reverse breakdown voltage and also a longer device lifetime. In addition to all these, improved carrier confinement in defect free active regions would also enhance the possibility of eliminating the efficiency droop at higher operating current levels, corresponding to high power operation.

The growth of GaN nanowires by MOCVD [21, 31, 32 and 33] without the use of a catalyst is an alternative procedure of producing m-plane GaN to grow the LED active regions on the non-polar m-plane. The methods used by Koester *et al.* [31], and Bergbauer *et al.*[32] to grow InGaN/GaN MQW structures on the m-plane of the GaN nanowires will be discussed in chapter 2 of this thesis. It has also been demonstrated in chapter 3 of this thesis that GaN nanostructures grown by the non-catalytic selective area MOCVD growth are threading defect free.

In summary, a coaxial LED based on GaN is one that we anticipate will incorporate all of the above requirements and some others to present us with the near perfect, state of the art and industrially viable visible LED. This thesis presents the

underlying intricacies involved in the fabrication of this device. The following sections deal with the motivation and background to this thesis.

1.2 Coaxial LED expected attributes

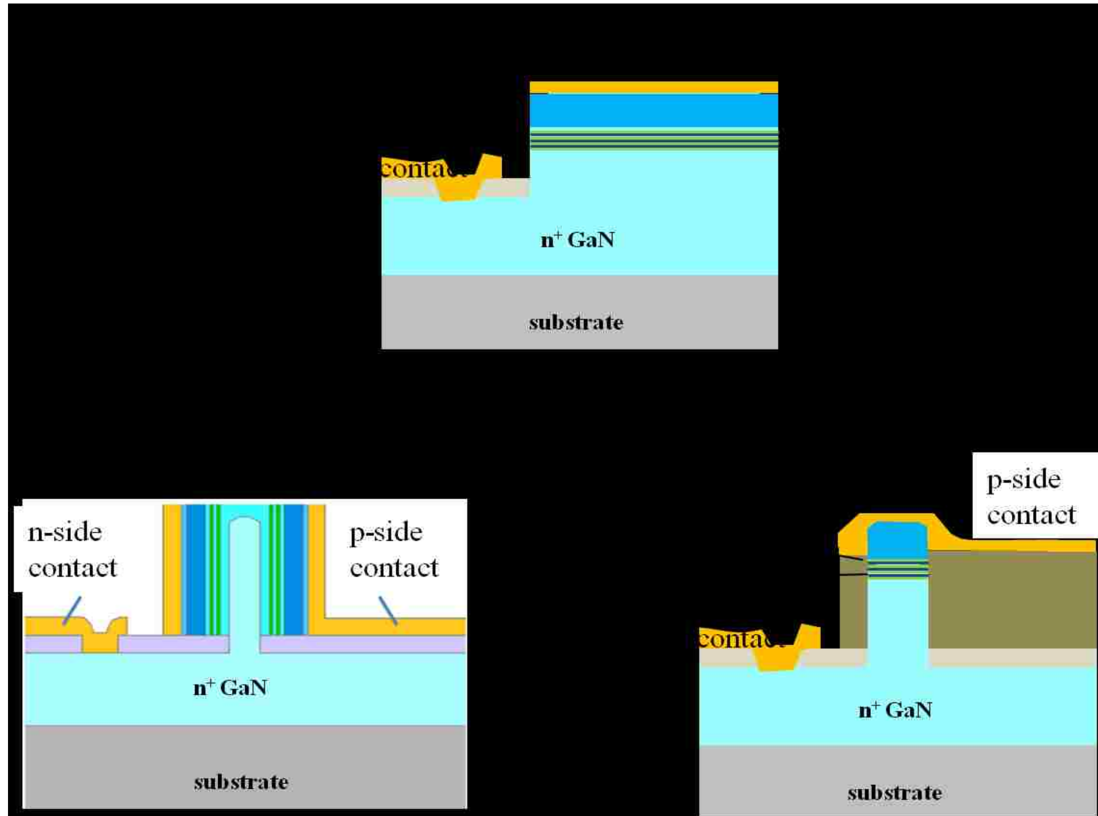

Fig. 1.5 the cross-section illustrations of (a) a conventional planar heterostructure, (b) a coaxial heterostructure and (c) a non-coaxial 3D grown heterostructure, GaN based LED, respectively. In all cases, the vertical direction is the c <0001> direction.

A coaxial LED consists of a core and a shell, just like in optical fiber geometry. The cross section of a coaxial LED is shown in Fig 1.5(b), in comparison with a conventional planar GaN based LED shown in Fig. 1.5(a) and also the cross section of a non-coaxial 3D grown LED on a similar scale is shown in Fig. 1.5(c). The core material is made up of a slightly higher refractive index material, as compared to the immediate shell to allow for natural guiding of light, thereby improving the external quantum efficiency (EQE). The coaxial LED discussed in this thesis is fabricated on a single crystal GaN nano/micro structure (wire form or a wall form) based on a scalable, non-catalytic, GaN MOCVD growth process. The salient features of the GaN based coaxial LED and comparison with the planar and the non-coaxial nanowire LED will be addressed in the following sub-sections.

1.2.1 Absence of QCSE in the GaN based coaxial LED

The side wall of this type of GaN based coaxial LED is the $\{1\bar{1}00\}$ m-plane. This side wall is extremely important because the active region is on this plane, as opposed to being on the {0001} plane in conventional (c-plane) planar and the non-coaxial nanowire based LEDs. The partial ionic nature of the gallium-nitrogen covalent bond in GaN leads to a significant spontaneous polarization field in the crystal structure along the c [0001] direction. This is true, even in the ternary $Al_xGa_{1-x}N$ and $In_yGa_{1-y}N$ ('*x*' and '*y*' being the % of Al and In, respectively) alloys. Due to lattice mismatch between ternary alloys (InGaN) on GaN, an additional strain induced piezoelectric field causes the energy bands in the quantum well to spatially bend, even during flat band conditions. This leads to disruption of the spatial overlap of electrons and holes at a given bias voltage. However, the m-plane in GaN crystallographic structure (Fig. 1.2) lacks the piezoelectric field

present in the [0001] direction. Thus, the band bending is eliminated in the flat band condition, which promotes better spatial overlap of the electron and hole distributions.

1.2.2 Absence of threading defects in GaN based coaxial LEDs

The absence of a native substrate for GaN growth has resulted in planar GaN based LEDs having a threading defect (TD) density in the range 10^8 to 10^{10} cm^{-2}. Nakamura [10] demonstrated that the TDs were centers for leakage currents and played an important role in reducing the reverse breakdown voltage. It was also demonstrated that devices that had a lot of TDs also had a very low operation time. In this respect, the coaxial LED is different from its planar counterparts. It was observed using bright-field cross-sectional transmission electron microscopy (XTEM) analysis that when a TD entered the nanostructure, the defect found a surface in the vicinity and bent towards it [15]. This procedure of defect elimination was found to be more prominent and energetically favored, than the conversion into another defect type. It is proposed that the driving force for this elimination process is the reduction of the dislocation line energy. This line energy is reduced for a TD that bends and terminates at a sidewall compared to a TD that continues to propagate along the nanostructure. This TD elimination mechanism is expected to occur in any GaN nanostructure that has a surface in close proximity to the TD.

1.2.3 High power emission for small coaxial LED foot print area

The coaxial LED is a wrap around LED as shown in Fig. 1.6(a). In comparison to a given foot print of area of a planar LED, or a non-coaxial LED (Fig. 1.6(b)), the coaxial LED has a larger active region area. From a simplified mathematical relationship, it is

possible to relate the optical power output by the LED, $P_{optical}$ as being proportional to the current (product of current density and area) as follows: -

$$P_{optical} = EQE \times J_{LED} \times Area \times \frac{hc}{e\lambda_{peak}}$$

EQE is the external quantum efficiency, J_{LED} is the current flowing through the LED per unit area, e is the magnitude of charge of an electron and λ_{peak} is the peak of the electroluminescence spectrum of a given LED. Let us assume that we have a coaxial wall LED array of length 250μm and thickness 0.5μm as shown in Fig. 1.6(d). The effective area of emission from this device, even if it is 1μm tall, is four times that of a planar LED in the same foot print area.

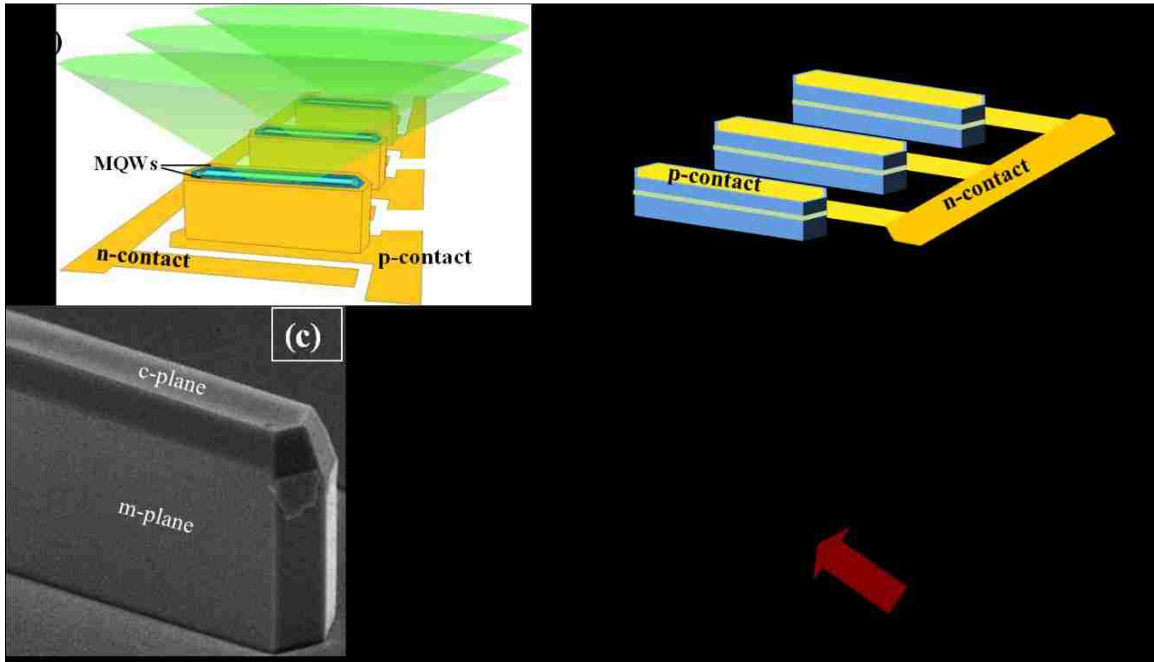

Fig. 1.6 (a) and (b) The comparison of a coaxial LED with respect to 3D grown non-coaxial LED of a similar area foot print. (c) a scanning electron microscope image of a wall structure and (d) illustration of a nanowall structure, in which only one of these dimensions needs to be nanoscale (<1μm) to get a threading defect free device.

Hence, if we assume that if a given diode current density, the external quantum efficiency of the c-plane LED and the m-plane LED are similar in magnitude, we could then anticipate four times the optical power would be generated in the coaxial LED, in comparison to either a planar LED, or a non-coaxial LED, in the same foot print area. The height of these wall devices can be increased with respect to the amount of optical output power required, by increasing the growth time.

1.2.4 Polarized light emission in GaN based coaxial LED

In addition to the absence of the QCSE, the m-plane LEDs have one more important property. A quantum well fabricated on the m-plane of GaN is bound to favor one polarization of emitted light to the other. This can be explained from the valence band structure analysis of m-plane $In_yGa_{1-y}N$ (y corresponds to % mole fraction of indium in the ternary alloy).

Under unstrained conditions, the crystal-field split-off band (SF) consists of the p_z orbitals (|Z>). This is located below the heavy-hole (HH) and light-hole (LH) bands, which are degenerate and are both an equal mixture of p_x - and p_y orbitals (|X> and |Y>)[12]. When $In_xGa_{1-x}N$ is fabricated on the c-plane of GaN, InGaN undergoes biaxial compressive strain. This strain is isotropic in both the x and y directions (a and m axes directions). This implies that the crystal symmetry is unchanged and hence the energy band diagrams do not change much, except for the loss of degeneracy of the HH and LH bands, as shown in Fig 1.7(a).

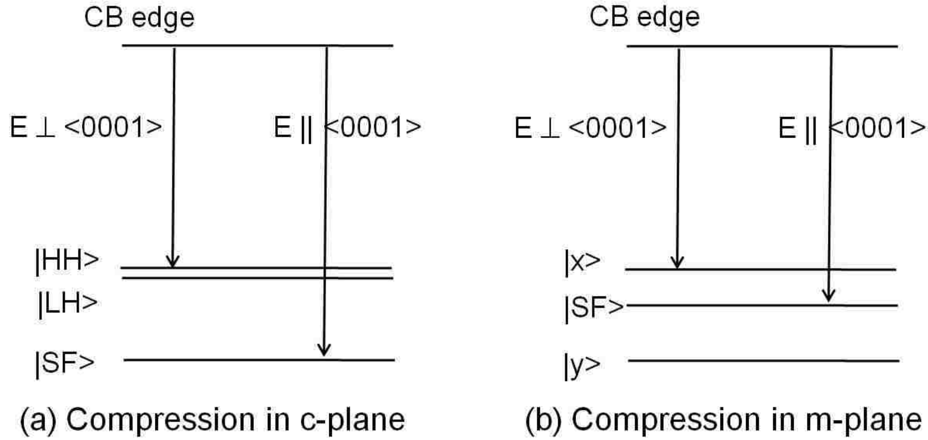

Fig. 1.7 Conduction and Valence band line ups at k=0 for InGaN on GaN in (a) c-plane and (b) m-plane. The electronic transitions are shown with the optical polarization of the emitted photon corresponding to the transition. 'E' represents the direction of electric field of the emitted photon corresponding to the transition

However, the quantum well fabricated on the m-plane is different from this. The |X> and |Y> are no longer equivalent and hence, these orbitals must be treated separately [12]. Fig 1.7(b) shows the energy band diagram of $In_yGa_{1-y}N$ strained on the m-plane GaN. The optical polarization associated with the transition is also shown in the Fig 7(b). In general, the electronic transitions are favored for the bottom of the conduction band to the top of the valence band, which in this case is |X>. This enables the surface emission to be polarized strongly with respect to x direction. The separation between the HH and the SF bands determines the degree of polarization, which increases with the increase in strain, or equivalently with increase in indium mole fraction in $In_yGa_{1-y}N$.

Masui *et al.* [12] demonstrated a polarization ratio, $\rho=\frac{I_m-I_c}{I_m+I_c}$ of about 86% for about y=0.28 indium in $In_yGa_{1-y}N$. It was also demonstrated that with the increase in the In incorporation, the polarization ratio increased, in accordance with the fact that the SF band is further away from the HH band. Recently, You *et al.* [13] demonstrated nearly

90% polarization ratio at 515nm photoluminescence emission and a 77% polarization ratio at 505nm electroluminescence emission measurement respectively. This device is anticipated to allow for around 44% energy savings in comparison to normal c-plane LEDs combined with a normal polarizer set up involved in the LED backlighting of an LCD.

1.2.5 Other attributes of UNM's coaxial LED based on GaN

The recent invention of a scalable, repeatable and an industrially viable GaN growth process has enhanced the chances of the coaxial LEDs making it to the market. Hersee *et al.* [21] demonstrated the successful controlled selective area growth of GaN nanowires over a wide range of sizes. This growth mechanism forms the basis of this thesis. It was shown that single GaN nanowires could be grown on pre-patterned GaN on sapphire by using regular MOCVD precursors, without the use of any catalyst. The ability to grow the nanostructures at pre-defined regions provides an opportunity to fabricate individually addressable LEDs that can be monolithically integrated on the same chip. Also, the unique geometry of coaxial LEDs would also facilitate their monolithic integration with driver circuitry, sensors and even control systems.

The coaxial LED based on GaN has the potential to offer a lot of benefits, in comparison to the planar or the non-coaxial 3D grown LED. The coaxial LED has a larger active region area in comparison to both, vertical p-n junction LED and the planar LED on the same foot print area, thereby anticipating more optical power output for a given current density. In addition to this, the planar and the non-coaxial 3D grown LED have been fabricated on the c-plane of GaN that has the internal polarization electric fields and a strong QCSE. The coaxial LED however would have its active region on the

m-plane, which is devoid of QCSE and would further lead to enhancement in the photogeneration.

1.3 Outline of the dissertation

This dissertation deals with the underlying intricacies involved in the fabrication of the coaxial LED based on a scalable GaN growth process. Owing to its benefits, in comparison to the current state of the art LEDs described in the earlier section, it is anticipated that the coaxial LED will exhibit revolutionary performance. The second chapter of this thesis presents a review of previous and current ongoing research in the field of GaN based coaxial LEDs that are being pursued by other research groups. The third chapter of this thesis describes how the threading defects can be eliminated in GaN nanostructures, which is extremely beneficial to the device operation lifetime. The defects in three-dimensional (3D) structures comprising an AlGaN shell on a GaN core and an InGaN shell on a GaN core are also discussed in this chapter. These results have also been published in a journal publication [37] and were presented at the electronics materials conference (EMC, 2010) [15]. Chapter 4 in this thesis deals with patterning of the growth mask and the subsequent growth of the 3D GaN structures, both at the nanoscale and the micron scale. The next chapter, (chapter 5) deals with the growth of GaN based coaxial structures, where the growth of p-GaN, AlGaN and InGaN shells around the GaN core is discussed. Some of the results of chapter 4 and 5 were presented at a plenary talk [36]. The publications containing some of the other results of chapter 4 and 5 are under preparation and are indicated in the publication section. The sixth chapter of this thesis shows the processing steps involved in the different versions of the coaxial LED processes and the important results and their analyses arising from these fabricated

LEDs. This chapter also reveals some insights on the elimination of stray GaN growth on the dielectric mask. The thesis is concluded in chapter 7 where suggestions for future work on the coaxial LED are also discussed. The publications associated with the research presented in this dissertation are listed at the end of chapter 7.

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Chapter 2

Coaxial Nanowire LEDs grown by MOVPE

Coaxial LEDs consist of a core and a series of epitaxial shells containing the active region and a lower index barrier region for light confinement, as described in the first chapter. In most cases, GaN is the core, and the active region could consist of InGaN/GaN multi quantum wells (MQWs). In some cases, a lower refractive index and higher band gap material, AlGaN is also grown epitaxially after the active region to provide both carrier confinement and a natural wave guiding of emitted light along the device axis. This additional wave guiding will improve the output coupling of light and will enhance the LED external quantum efficiency.

Several research and industrial groups around the world are also pursuing research on this emerging field of LED technology. Metal organic vapor phase epitaxy (MOVPE) growth of GaN core-shell nanowire LEDs has been developed using a catalytic VLS type approach [1,5, 11] and also a non catalytic approach using the selective area epitaxial growth method [15, 22, 28]. In this chapter, we look into some important contributions, growth details and results in the emerging field of coaxial nanowire LEDs fabricated using both of the above growth techniques. In addition to this, some theoretical analyses of the coaxial LEDs [7, 8, 25, 30 and 31] using 2D finite element analysis are also reviewed in this chapter. Following this, a short analysis is provided showing how our work complements the work of others in this field and shows how this thesis makes an important contribution to the field of coaxial LEDs

2.1 Coaxial LEDs based on catalytic growth

The vapor-liquid-solid (VLS) method of growing semiconductor nanowires was first demonstrated by Wagner and Ellis in 1964 [9]. A small particle of a heavy metal is used at desired locations to preferentially initiate semiconductor nanowire growth at these catalyst sites. The nanowire growth can be continued either until the entire metal catalyst is consumed or until the growth conditions are changed.

Dr. Charles Lieber and his group at Harvard University pioneered the core-shell GaN based nanowire LEDs and have been successful in demonstrating the VLS growth mechanism for the GaN nanowire core [1, 2]. A 0.01 molar nickel nitrate solution was deposited on a c-plane sapphire substrate and placed in the MOVPE reactor. The metal cation in the solution serves as the catalyst for the nanowire growth. Dr. George Wang and Dr. Qiming Li at the Sandia National Labs, Albuquerque, have also employed the same catalytic nanowire growth mechanism to grow core-shell GaN based nanowires. Wang *et al.* have also explored [5] the improvement in the alignment and the density control of the nanowires. A 2nm Ni metal is evaporated on (1-102) r-plane sapphire substrate by e-beam metal evaporation. This substrate is then loaded into a MOVPE reactor to initiate the semiconductor nanowire growth [12]. As the temperature of the substrate is increased in the MOVPE reactor, the continuous layer of metal transforms into a grid of minute spherical metal particles by virtue of the Gibbs-Thomson effect. The illustration of the VLS method of growing nanowires is shown in Fig. 2.1.

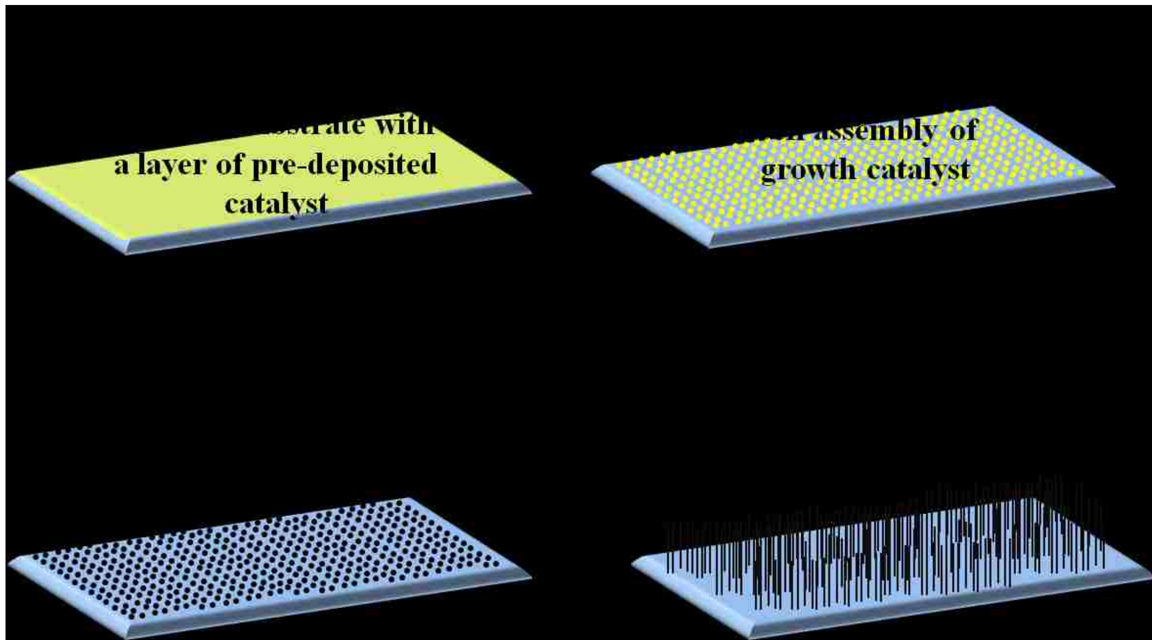

Fig. 2.1 The 'VLS' growth mechanism initiated with a self assembled growth catalyst is described

Wang's n-type GaN core nanowires [3, 4] were grown at temperatures between 900°C and 950 °C in H_2 atmosphere using trimethyl gallium (TMG) and ammonia (NH_3) as the growth precursors and silane (SiH_4) as the n-type dopant.

Nanowire LEDs grown by Qian *et al.* [1] (Leiber's group) consisted of an n type GaN core and sequentially deposited i-InGaN, i-GaN, p-AlGaN and p-GaN to terminate the LED structure [1, 2]. The n-GaN and the p- GaN are the respective electron and hole injection layers. The intrinsic InGaN layer, GaN barrier layers, and p-AlGaN layer were sequentially deposited in N_2 at significantly lower temperatures (600-800, 860, and 940 °C, respectively) to allow for InGaN growth, rather than indium segregation and evaporation. The growth was carried out using TMG, trimethyl aluminum (TMA), trimethyl indium (TMI) and NH_3 as the precursors. Lastly, the p-GaN outer shell was grown in H_2 atmosphere also at 960 °C using biscyclo pentadienyl magnesium (CPM2) as p-type dopant. The composition of *In* in $In_yGa_{1-y}N$ is varied by varying the InGaN

growth temperature, there by tuning the band gap and hence, the emission wavelength. To control indium segregation in these nanowires, thin (~8nm) InGaN layers were employed. The growth conditions of the InGaN shell structures grown by Wang *et al.* are similar [5, 12] to that of Qian *et al.* (Dr. Leiber's group).

SEM images, TEM, EDS mapping, and line scan studies of the nanostructures grown by Qian *et al.* [1, 2] have demonstrated epitaxial growth of well-defined single-crystal nanowire radial heterostructures. The SEM images of the core-shell structures grown by Qian *et al.* [1] show single crystalline GaN nanowires with a triangular cross-section similar to that shown in Fig. 2.2(a). The Cross-sectional TEM studies have revealed that the core/multishell nanowires are dislocation-free single crystals with a triangular morphology. The three sidewall planes identified (two $\{1\bar{1}01\}$ and one (0001) planes) are consistent with what was observed by Kuykendall *et al.* in [11]. The two $\{1\bar{1}01\}$ planes are semipolar crystallographic planes; thereby the magnitude of the spontaneous polarization is reduced, in comparison with that in the c direction. Wang *et al.* have observed [3] that there was virtually no $In_xGa_{1-x}N$ shell growth observed on the c-plane facet. Northrup *et al.* [13] had studied the stability of (0001) and (000-1) c-plane facets, where it was concluded that the N-terminated c-plane had a lower surface energy and hence a lower growth rate of GaN (or InGaN) was observed on this plane. Qian *et al.* [2] also support this observation by analyzing the overall InGaN/GaN shell structure on the two $\{1\bar{1}01\}$ facets as being thicker (65 nm) as compared to that on the {0001} facet (10 nm). It is also observed that the 26-period InGaN quantum-well structure was more prominent on the $\{1\bar{1}01\}$ facets, where as no quantum-well contrast variation was observed on the {0001} facet.

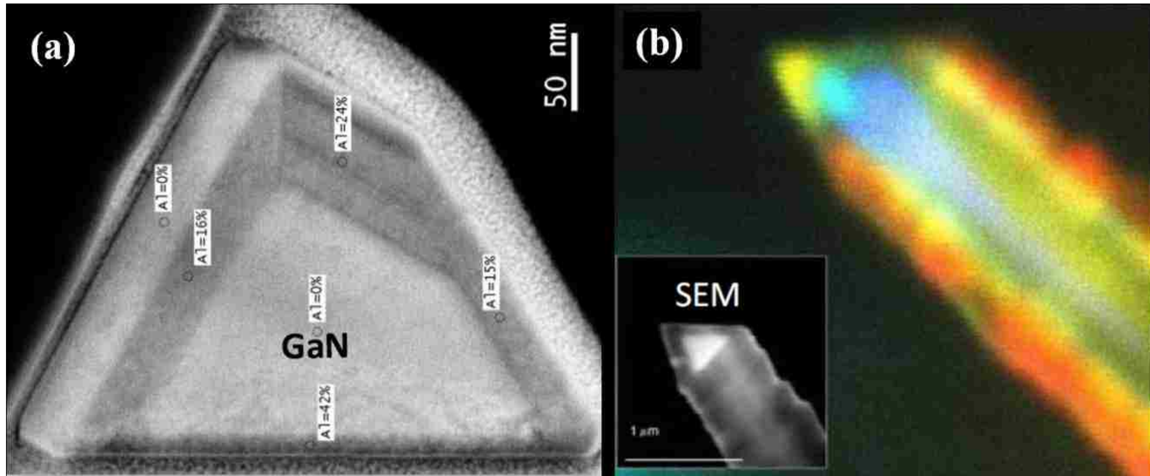

Fig. 2.2 (a) The cross-section STEM image of a Coaxial nanowire structure and (b) the corresponding composite CL image showing multicolor emission from an InGaN shell due to an In composition distribution, both images reproduced from [3]

Electron dispersive spectroscopy measurements [2] also confirm the difference in shell thickness. Convergent beam electron diffraction (CBED) was also carried out to identify these N-terminated c-planes. Wang *et al.* [3] carried out deep level optical spectroscopy (DLOS) measurements that suggest the reduction of defect-related recombination in the core of the core-shell structures, in comparison to a free standing GaN core, or even a non-coaxial p-n junction nanowire LED [3]. This indicates that a coaxial LED would have a higher radiative recombination, in comparison to a non-coaxial nanowire LED. Spatially resolved, monochromatic cathodoluminescence (CL) measurements (Fig. 2.2(b)) were performed to identify the optical properties of the core-shell nanowire structures. The CL images were taken at different wavelengths of the GaN/InGaN nanowire to identify the indium composition. The core region was found to emit at 366nm corresponding to the band edge GaN emission. The shell region immediately near the core was found to emit at 480nm. The images of the center of the

InGaN shell and the outer InGaN shell regions showed emission wavelength of up to 700 nm. These observations revealed the increase in the InGaN emission wavelength as a function of the shell thickness, thereby revealing an increase in indium incorporation in InGaN as the shell thickness is increased. Despite this increase of indium incorporation, the InGaN material quality compared better to planar InGaN grown on GaN with the similar indium incorporation in [20]. This was attributed to the fact that the nanoscale dimensions of GaN core allowed for better strain relaxation. To further verify this, Li *et al.*, [19] used 2D finite element analysis to calculate the strain energy distribution in a GaN-InGaN core-shell nanowire. This theoretical study indicated that strain relaxation is observed as the thickness of the InGaN layer was increased, thereby leading to a higher indium incorporation in the shell of the nanowire.

The electrical characterization of these nanowires involved detailed and methodical procedures of isolating the nanowires from the growth substrate. Qian *et al.* [1, 2] and Wang *et al.* [3, 4] employed a nanowire dispersion strategy to isolate single nanowires from the growth substrate. A portion of the growth substrate was immersed in alcohol and agitated to create a suspension of nanowires. A couple of drops of this suspension are added to a silicon substrate to isolate single nanowires as the alcohol dries up. After isolation, e-beam lithography was used to define the source and drain regions for the nanowire LEDs. Ti (20nm)/Al (100nm)/Ti (30nm)/Au (50nm) was sequentially evaporated on the core of the nanowire, which was exposed using a focus ion beam assisted etching as described in [1, 2]. The p-metal (Ni (150nm)/Au (50nm)) was deposited directly on the nanowire sidewall planes, which was then followed by anneal in N_2 atmosphere at 550°C for 2min.

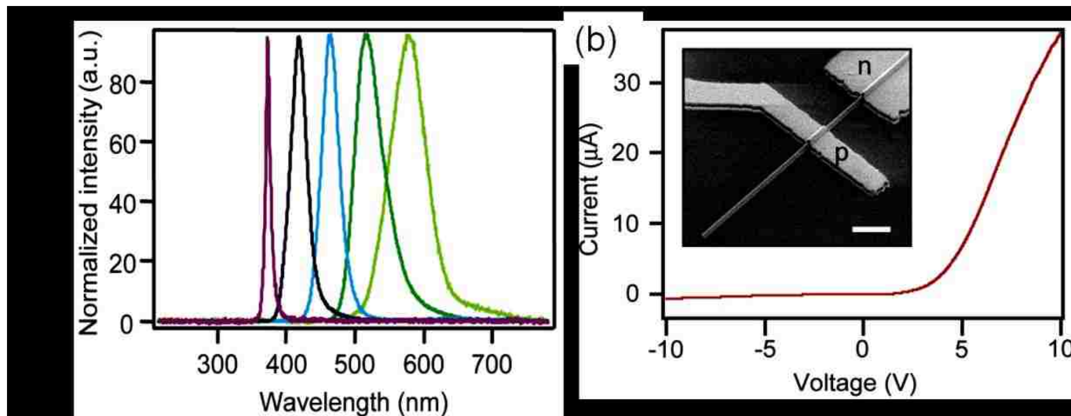

Fig. 2.3 (a) EL spectra from five representative multicolor coaxial nanowire LEDs. and (b) the corresponding I vs. V curve of a coaxial LED shown in the inset SEM image, both images reproduced from [2]

I-V characteristics measured by Wang *et al.* were indicative of the core-shell structures being more conductive in comparison to a freestanding GaN nanowire with a similar mean cross-section diameter [3, 4]. It is also observed that the nanowires grown at higher temperatures have seemingly optimal electrical and optical properties for better LED operation, in comparison to those grown at lower temperatures. I-V characteristics and electroluminescence measurements (Fig. 2.3(a) and (b)) done by Qian *et al.* are reminiscent of a GaN based diode with a typical turn on voltage of around 3V. The electroluminescence measurements have demonstrated tunable emissions from 365nm to 600nm under forward bias. The studies of the light emission from the nanowire LEDs show an enhanced light emission from the nanowire ends, as compared to the nanowire faces, suggesting a strong optical guiding phenomenon, largely due to the low index AlGaN shells and the non-absorbing GaN core acting as a natural optical fiber [2].

2.2 Coaxial LEDs based on non-catalytic growth

The growth of GaN nanowires without the use of a catalyst using selective area growth mechanism was first pioneered by our group and the work was published in [28]. Hersee *et al.* [28] and Wang *et al.* [35] have demonstrated the growth of GaN nanowires using two different MOVPE growth mechanisms, without the use of metal catalysts. Following the lead, GaN nanowires have also been grown using MOVPE [15, 22] and also molecular beam epitaxy (MBE) [32, 33] without the use of a growth catalyst. One of the issues with catalytic nanowire growth processes is potential for the incorporation of the metal catalyst into the nanowire [34]. Such incorporation is anticipated to be prohibitive for many semiconductor applications; hence the interest in catalyst-free growth approaches. Chèze *et al.* [34] have shown the presence of a higher density of basal plane stacking faults in the GaN nanowires grown using nickel as a catalyst, in comparison to the nanowires grown without catalyst. The photoluminescence obtained from these nanowires were also less intense and wider, in comparison to those grown in the absence of nickel catalyst.

GaN nanowires have been fabricated without the use of metal catalysts using an *in situ* SiN_x growth technique at CEA-LETI by Koester *et al.* [15]. The nanowires grown by this technique are grown along the c [0001] direction and are epitaxially connected to the underlying substrate. The active region (InGaN/GaN MQWs) is grown epitaxially on the non polar m-planes of the GaN nanowire. The importance of growing MQWs on non-polar orientations has already been discussed in chapter 1. Bavencove *et al.* [27] have reported the growth and fabrication of core-shell nanowire GaN based LEDs on silicon substrate. Bergbauer *et al.* [22, 23] from Osram Opto Semiconductors, Germany and glo

USA have also demonstrated the growth of GaN nanowires without the use of a catalyst using selective area growth on c-plane sapphire substrates with a patterned dielectric mask to define the locations where the nanowires are to be grown. Hersee *et al.* [28, 35] have also grown GaN nanowires using a similar selective area growth process, which forms the basis of this thesis. Nanocrystal Asia, Taiwan has also released their first GaN nanowire array on a sapphire wafer product in 2011 [36].

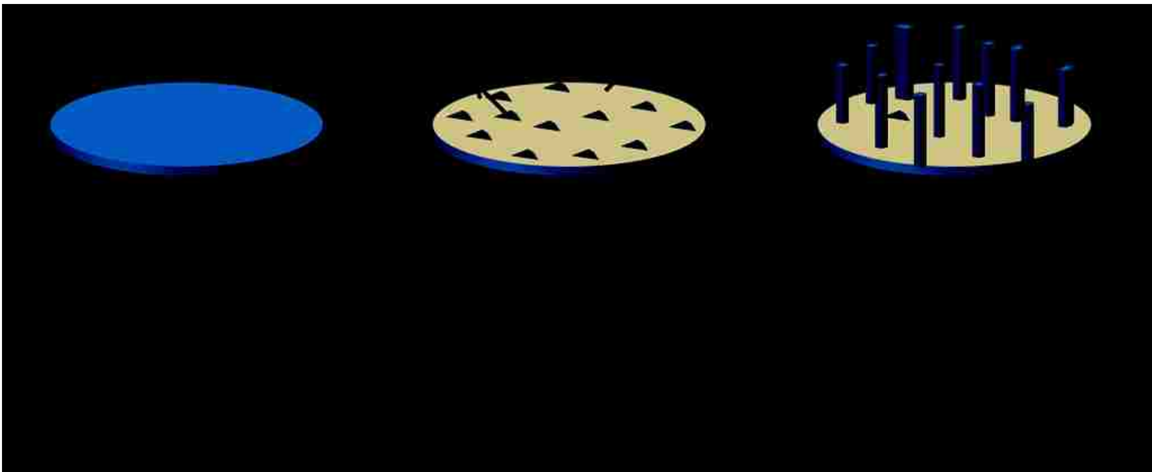

Fig. 2.4 the stepwise illustration of the non-catalytic, template free GaN nanowire growth pursued by Koester *et al.* [15]

Selectively grown GaN nanowires could form the substrate for the core-shell InGaN/GaN nanowire LEDs. Glo USA, a new start up company have also been focusing on the development and commercialization of the low cost nanowire LED based on their selective area heterostructured semiconductor nanowire epitaxial growth and process technologies.

Koester *et al.* [15] have reported the growth of GaN nanowires on c-plane sapphire substrate respectively using a thin film of *in situ* deposited SiN_x in a MOVPE chamber. The details of the *in situ* SiN_x deposition process have been discussed in [15] and the process is illustrated in Fig. 2.4. The same growth recipe has also been employed

by Bavencove *et al.* [27] on silicon substrates, instead of sapphire. On silicon, a thin AlN buffer was initially deposited to allow the growth of n-type GaN nanowires. The initial part of the core nanowire was grown n-type at around 1000°C with a low V-III ratio using TMG and NH_3 as the precursors. The later (top) part of the nanowire was grown unintentionally doped at the same temperature. After this, the temperature was reduced to around 720°C-760°C for growing the InGaN shell on the top of the GaN nanowire core. The InGaN shell was grown using triethyl gallium (TEG) and trimethyl indium (TMI) as the group III precursors at a pressure of 400mbar. The barrier GaN layers and the p-GaN outermost shell layer were grown at 830-870°C using TEG as the group III precursor. Bergbauer *et al.* [22] achieved their nanorod growth on c-plane sapphire substrates with selectively opened SiO_2 holes, patterned by nanoimprint lithography. These substrates were then loaded into a large volume industry production MOVPE reactor for the nanowire LED growth. The shape and morphology of the GaN nanowires grown by Bergbauer *et al.* was dependent on the ratio of the H_2/N_2 within the carrier gas. A minimum H_2/N_2 ratio was required for the nanowires to have vertical sidewall facets, instead of pyramidal sidewall facets. As the H_2/N_2 ratio was increased, the nanowire diameter reduced, until about a ratio of 1.25, after which the nanowire diameter remained fairly constant. However, as the nanowire pitch was increased, for a given size of the hole, the nanowire diameter increased once again from 250nm for a 540nm pitch to about 700nm for a 1600nm pitch [23]. Once the GaN nanowire core was grown, 5 InGaN/GaN MQW shells were grown with TEG and TMI as the group III precursors. The growth conditions employed resulted in an InGaN quantum well thickness of 6nm and a GaN quantum barrier layer thickness of 14nm. The LED structure was terminated with two

layers of GaN shells, one undoped layer 20nm thick and the other doped with magnesium (p-type doping) 95nm thick. Information gathered during a technical visit and discussion with glo USA personnel (March 2012) also indicates that the GaN nanowires were grown also grown using non catalytic selective area GaN growth technique. Planar GaN on sapphire wafers were used as the starting point for the GaN nanowire growth. A layer of SiNx was grown by low pressure CVD on these substrates, following which growth mask patterning is carried out either using nanoimprint lithography for smaller sized holes or regular photolithography using a stepper for larger sized holes. This substrate is then reintroduced into their MOVPE growth chamber for the nanowire LED growth. The LED growth is then carried out very similar to Bergbauer *et al.*

The SEM images of the coaxial nanowire structures grown by Koester *et al.* [16] show a smooth m-plane growth on the top portions of the nanowires (Fig. 2.5(a)). The lower part of the wire is thinner than the upper part, indicative of just the core GaN in the lower portion of the nanowires, as shown in Fig. 2.5(a) and (b) respectively. Cross-section TEM was used to characterize the core-shell heterostructures. The cross-sections were analyzed both along and perpendicular to the growth direction. The TEM images taken along the $[11\bar{2}0]$ zone axis show the presence of stacking faults. These stacking fault defects had been previously observed even in planar InGaN grown on m-plane GaN substrates [37].

The crystalline quality and defect formation of the nanowires grown by Bergbauer *et al.* were analyzed using bright field cross-section TEM (XTEM). The nanowires exhibit a smooth top and side wall planes, with a significant lateral growth, in comparison to the original size of the selective area growth openings. A significant number of

threading defects were observed near the interface of the nucleation GaN layer of the nanowires and the sapphire substrate. The defect density is however reduced as the distance from the interface along the nanowire is increased. Defect bending (which is reported in section 3.2 of chapter 3) was reported as the main mechanism for the defect reduction in these nanowires. However, some nanowires (Fig 2.5(c)) were also observed that contained threading defects proceeding through until the end of the nanowire.

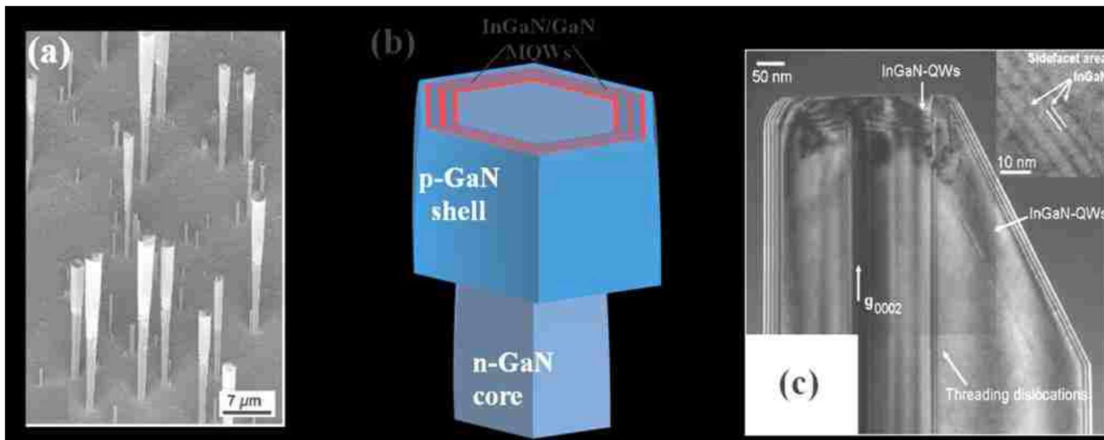

Fig. 2.5 (a) SEM images of core-shell LEDs grown by Koester *et al.*, image reproduced from [ref] and (b) illustrates the structure of the coaxial LED shown in SEM. (c) XTEM micrograph of core-shell GaN LED grown by Bergbauer *et al.* showing the propagation of a threading defect along the length of the nanowire, image reproduced from [22]

The low temperature µ-photoluminescence measurements of the nanowires fabricated by Koester *et al.* [16] indicate InGaN wavelengths from the range of around 380nm to about 410nm for different quantum well thickness and different indium incorporation achieved by varying the growth time and temperature respectively. One of the effects of the quantum confined stark effect (QCSE) in polar InGaN/GaN active regions is the increase in the emission wavelength due to the band bending, as shown in Fig 1.2(b) of chapter 1. As the forward bias voltage is increased, the band bending is

reduced, thereby effectively increasing the band gap corresponding to the photon emission (corresponding to the reduction in peak wavelength of emission). This effect is more pronounced when the active regions are thicker. However, the power dependent cathodoluminescence emission wavelength remained almost constant, even when the excitation power was varied (0.019 to 60 kW/cm^2), for two different active region thicknesses, one corresponding to a 20 second active region growth time (~10Å quantum well thickness) and the other, a 80 second growth time (~80Å quantum well thickness) respectively. The absence of blue-shift in the emission wavelength due to the quantum confined stark effect leads Koester *et al.* to believe that the active region emission is coming from the non-polar m-plane of the core-shell nanowire. Bergbauer *et al.* have used cathodoluminescence (CL) measurements to determine the spatial dependence of the indium incorporation in the nanowire LEDs grown. They determined three different indium incorporation percentages corresponding to three different localized CL emission wavelengths (384nm, 414nm and 455nm). The 414nm emission was shown to be coming from the (0001) top facet, while the 384nm and the 414nm emission were attributed to the InGaN layers on the semipolar $(10\bar{1}\bar{1})$ and $(10\bar{1}\bar{2})$ planes. Bergbauer *et al.* [22] have not reported any CL emission from the $(1\bar{1}00)$ m-plane in their work.

Koester et.al and Bavencove *et al.* have reported the fabrication of single core-shell LED. The core-shell nanowires fabricated by Koester *et al.* were laid horizontal on SiO_2 on silicon after agitation of the growth substrate in ethanol. These nanowires were then encapsulated in a spin-on dielectric, following which the sample was then dry etched to expose the nanowire. E-beam lithography was used to define the p and n contact regions of the horizontal nanowire, following which the respective metals were deposited

to complete the contacts of the LED. The current-voltage characteristics of the LEDs fabricated indicated a very high turn on voltage (~9V). The electroluminescence of the LEDs was observed for a positive bias of around 9.75V with the EL peaking at 392nm. The core-shell nanowire LEDs fabricated by Bavencove *et al.* involved a full wafer scale direct integration process. A dielectric was first deposited everywhere on the substrate to isolate the p-GaN from the n-GaN. Following this, 300nm of indium tin oxide (ITO) is deposited everywhere to form the p-contact to the nanowire LED. The n-type silicon substrate, on which these nanowire LEDs were grown, was used for the n-side contact. A CCD camera with RGB color filters was used to directly visualize the electroluminescence spectrum in real time. The LED arrays fabricated by Bavencove *et al.* were emitting at a peak wavelength of 449nm (corresponding to blue) when subjected to a CW-current of 20mA. However, the spectrum recorded on a representative single nanowire LED revealed an emission wavelength of around 417nm (violet). These observations indicated a difference in the incorporation of indium in InGaN across the different nanowires due to the varying nanowire sizes and local density dispersions.

2.3 Electrical and optical simulation studies of coaxial LEDs

The theoretical studies of Dr. Winston Schoenfeld and his group [7, 8] investigated design improvements that could lead to the fabrication of better coaxial LEDs. They used Apsys, a 2D finite element modeling software to solve the current continuity equations, carrier energy transport equation and the Schrödinger and Poisson equations. In addition to this, they have also solved the scalar wave equation for waveguiding coaxial LEDs. While the simulations do not take account of the presence of dislocations and stacking faults in the GaN based devices, their model is very useful in predicting a viable design for the electrical contacts, internal structure, and physical geometry of the coaxial LEDs. Deppner *et al.* have also published [26] a computational study of optical and carrier injection in GaN core-shell nanowire LEDs. They simulated coaxial LED with a polar, a semi-polar and a non-polar active region, similar to the LEDs fabricated and described by Bergbauer *et al.* A semi-classical simulation approach was adopted for the simulation. The bulk semiconductor regions were treated classically, where as the carriers in the active region were treated quantum mechanically in the direction of narrow confinement. Connors *et al.* [25] have also investigated the current crowding in core-shell LEDs and have determined a correlation between the doping profile and the current crowding within the device. They have used TiberCAD multiphysics simulator to simulate core-shell LEDs with a wide range of material parameter flexibility.

Useful insights into this emerging LED field of LEDs were also gained from simple optical simulations. Lévy *et al.* [30] investigated the optical guiding properties of single hexagonal/circular nanowires. They assumed a common refractive index of 2.4 for

all their nanowires in the simulation and the wavelength of interest as 380nm. A finite-difference mode solver was used to solve for the effective index of the guided modes and their electromagnetic field distributions. Kölper *et al.* [31] have proposed in their work, a simplified model for a single GaN core-shell nanowire LED, neglecting any crosstalk with neighboring nanowire LEDs or photonic crystal effects that come up because of the periodic arrangements of the nanowires. This theoretical work also included vectorial 3D solutions to Maxwell's equations.

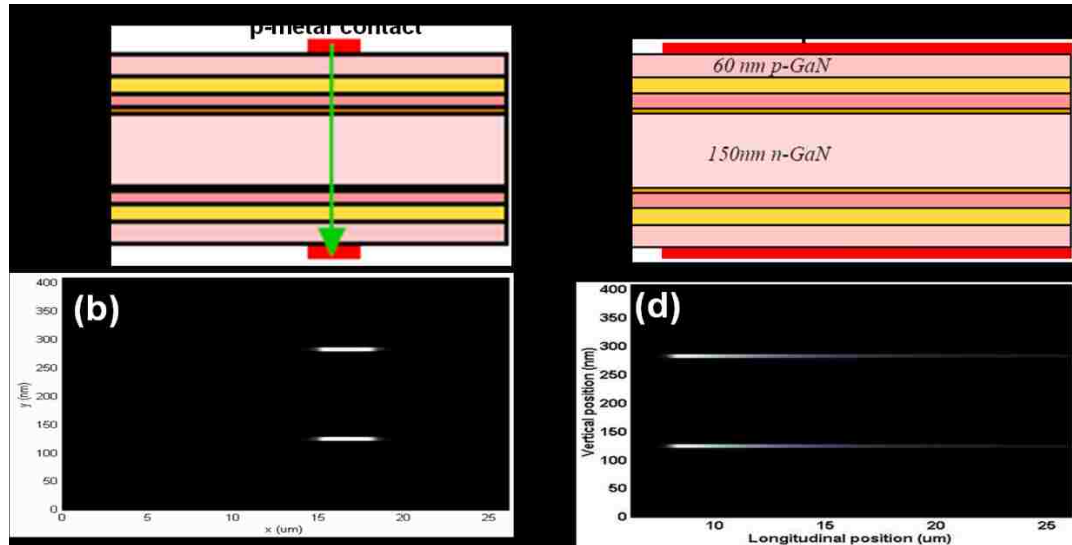

Fig. 2.6 The simulated cross-section image of a Coaxial nanowire structure with a smaller area coaxial metal p-contact (a) in comparison with a larger area coaxial transparent ITO contact (c) and the corresponding map of the light generated in the respective coaxial LEDs (b) and (d), images reproduced from [7] and [8], respectively

The model proposed by Mazuir *et al.* [7] predicts that the carriers in the simulated coaxial LEDs were choosing the path of least total resistance. The electron and hole current were separately simulated, thereby giving us an idea of the most likely location of finding electrons and holes simultaneously. The simulation shows that the electron density of states was highest in the low resistance InGaN quantum well region.

The density of states of the holes in the InGaN quantum well was however, maximum only underneath the p-contacts due to the poor conductivity of p-GaN, in comparison to n-GaN and other shell materials. This leads to a current crowding behavior under the p-contacts and the light generation is prominent only under the p-contacts (Fig. 2.6(a) and (b)). Hence, the first take away from these set of simulations is the requirement of a huge p-contact area. At the same time, a transparent p-contact would be extremely important in the light extraction.

A simulation of a coaxial LED with a bigger area transparent p-contact (Fig. 2.6(c)) in [8] showed interesting results. The electron-hole overlap was over a larger area in the quantum well. However, the result of p-GaN being less conductive in comparison to n-GaN leads to a tendency for higher current injection near the n-contact of the nanowire, which is also synonymous with the light generation (Fig. 2.6(c) and (d)). In spite of this phenomenon, the larger area p-contact is successful in reducing the current crowding under the p-contact regions, thereby enhancing the possibility of a high power operation. The current crowding behavior was also observed in the simulations executed by Connors *et al.* [25] upon using a constant doping profile in the coaxial LEDs all over the n-GaN and the respective constant doping profile in the p-GaN shell region. The observed current crowding was attributed to the effects of geometry and the difference in the conductivity between the n and p contact layers. It was clear from the conduction band diagram that the electron-hole overlap density was concentrated nearer to the p-GaN shell contact. Hence Connors *et al.* [25] considered a revision of the p-GaN doping profile, in order to reduce the current crowding effect. A doping profile was simulated that could be successful in maintaining a constant junction voltage distribution across the

cross-section of the core-shell LED (simulated structure shown in Fig. 2.7(a)) along the nanowire length. These observations lead to simulations of a set of different doping profiles for the n-GaN core of the nanowire coaxial LED. A simplified model was also used in [25] to show that an introduction of a non-constant doping profile in a core-shell nanowire LED could lead to the spreading of the current along the junction, in comparison to a device with a constant doping profile.

The LEDs simulated by Deppner *et al.* [26] consisted of an InGaN/GaN MQW active region (15% indium) in between the n-GaN core and the p-GaN shell as shown in Fig. 2.7(b). The coaxial LED consisted of three MQW growth orientations, the polar c-plane, the non-polar m-plane and the semi-polar tilted active regions respectively. The p-contact was placed only on the polar and semi-polar surfaces, while the n-contact was placed at the opposite end of the coaxial nanowire LED. The k.p calculations were performed to calculate the electron and hole distributions by simulating the energy band diagrams across the nanowire LED active regions on all the three crystalline orientations.

Deppner *et al.* also observed inhomogeneous hole current injection due to the low conductivity of the p-GaN layer. This current crowding was attributed to the fact that only 75% of the total luminescence was observed in the non-polar m-plane MQWs, despite the fact that the m-plane active region area accounted for nearly 93% of the total active region area. Most of the luminescence was observed nearer to the p-contact regions in the simulations. Thus it was demonstrated by Deppner *et al.* that the presence of the polar and semi-polar MQWs limit the carrier injection efficiency in non-polar MQWs.

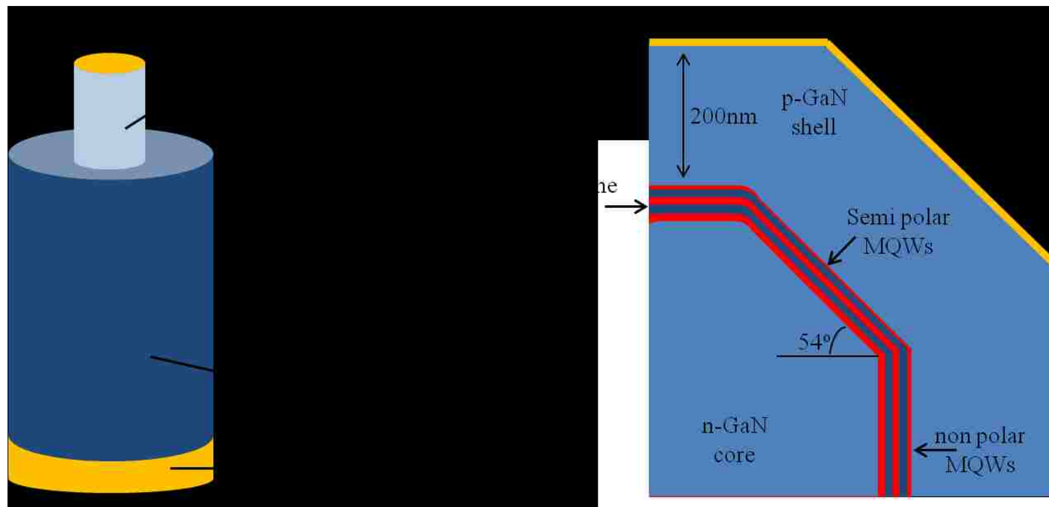

Fig. 2.7 (a) The coaxial nanowire structure simulated by Connors *et al.* [25] and (b) the cross-section of the coaxial LED structure simulated by Deppner *et al.* [26] showing the three MQW's on the polar, semipolar and nonpolar GaN orientations.

Basic ray tracing mechanisms and scalar wave equation solutions were used by Mazuir *et al.* to determine the photon propagation in a coaxial LED. It was observed that the generated photons in the LED undergo absorptions, both in the active region and the bulk material. However, one of the important observations was that most of the photons that exited the material were from the edges of the nanowire, thereby confirming the effectiveness of a natural, optical guided design of the coaxial LEDs. The other important observation from this optical simulation was that the total output power decreased exponentially with the increase in the nanowire length, thereby suggesting an advantage of using shorter coaxial LEDs with a large area p-contact.

Kölper *et al.* and Lévy *et al.* have simulated and characterized the optically guided modes in the nanowire LEDs. One of the most important advantages of the coaxial LEDs is the fact that the device structure is designed in such a way that there is a natural optical guiding phenomenon. This could potentially be beneficial for the light generated within the active region to be directionally coupled out of the LED's surface at

either ends of the nanowire LED, in comparison to a planar LED, wherein the photons generated in the active region are emitted in all directions. Kölper *et al.* [31] approximated the core-shell nanowire LEDs as having a circular cross-section, where as Lévy *et al.* [32] simulated the nanowire LEDs by using a more realistic hexagonal cross-section. Kölper *et al.* plotted the mode dispersion curves for a wavelength of λ_o = 440nm for different r_{core}/λ_o values. They considered two cases, one in which the core refractive index, n_{core} = 2.4 (equal to the refractive index of GaN at 440nm) and the cladding layer was just air (n_{clad}=1) and the second case, in which the core remains the same, while the cladding layer was silica (n_{clad}=1.5). It was concluded that embedding the nanowire in a cladding material of n_{clad}=1.5 reduces the fraction of power that is emitted into vertically guided modes. Lévy *et al.* plotted the mode dispersion curves for a wavelength of λ_o=380nm for different hexagonal radii values. They used a finite-difference mode solver to calculate the effective index of the lower order guided modes and their field distributions. The order of magnitude of nanowire sizes and density in nanowire arrays were assessed for improved optical guiding, just like in optical fibers. A low optical coupling was expected in a single mode nanowire array when the typical nanowire fill factor was around 25%, meaning a few hundred of nanometers separation between wires of mean diameter of 150nm. It was concluded that to draw a maximum benefit from the waveguide effect in nanowires for efficient extraction, the nanowire diameters had to be less than 150nm, for the criteria considered by Lévy *et al.*

2.4 Analysis of previous work

This section analyzes the previous and current research on coaxial LEDs that has been reviewed in the previous sections. The aim of this section is to show where the research on coaxial LEDs at UNM fits into this body of work. Qian *et al.*[1,2] and Wang *et al.* [3,4] have been successful in growing and characterizing GaN nanowires and GaN/InGaN/GaN MQW heterostructured core-shell nanowires using the VLS growth technique. This growth technique employs a metal based catalyst to initiate the GaN axial nanowire growth. Depending on the optoelectronic applications, the metal catalyst may be prohibitive to the performance of some devices as it has been observed in [17] that the catalyst might be incorporated into the nanowires during nanowire growth. If incorporation occurs, then unintentional defect levels would undoubtedly result. For example, gold is a well known trap center [18] in silicon, although it has been widely used as a typical catalyst in VLS growth of silicon nanowires. Metal catalyst incorporation in GaN nanowires grown by MBE has also been observed by Chèze *et al.* [34]. GaN nanowires grown using Ni as a catalyst were shown to contain many more basal-plane stacking faults and their photoluminescence was weaker, by comparison to the GaN nanowires grown under similar growth conditions but without the use of a catalyst. These differences were attributed to the effects of the catalyst Ni seeds. The self assembled catalysts that define the nanowire growth sites in the VLS growth mechanism lead to the growth of nanowires that are randomly positioned with a significant range of diameters. Wang *et al.* [3, 4] have reported the growth of vertical and exceptionally well aligned GaN nanowires oriented along the $[11\bar{2}0]$ direction on $(1\bar{1}02)$ r -plane sapphire wafers. However, the degree of alignment and size uniformity is highly dependent on the concentration of the metal catalyst solution that is being used. For all of these reasons, it

could be argued that the VLS method of growing single crystal nanowires does not provide a viable growth technique that would be acceptable to industry.

Thus, the GaN nanowires grown by non-VLS (no metal catalyst) selective area MOVPE growth methods appear to have an edge over their VLS grown counterparts. This thesis discusses LEDs that are grown using non-VLS nanowire growth technique that is scalable, repeatable and industrially viable.

One of the advantages of growing nanowires using selective area growth technique is the ability to define the nanowire growth regions with precision. The nanowire diameters grown by Hersee *et al.*, Nanocrystal Asia Bergbauer *et al.*, and Glo USA are defined by the size of the hole patterned in the growth mask (also known as a growth template) that is deposited and patterned ex-situ. While this thesis (based on Hersee *et al.* [28]) reports the use of interferometric lithography [38] to pattern the growth dielectric for nanowire growth, Bergbauer *et al.*, Nanocrystal Asia and Glo USA have also demonstrated that nanoimprint lithography can also be used to define the nanoscale patterns in the growth mask.

In all cases these nanowires are epitaxially connected to the underlying substrate, so the crystallographic orientation of the single crystal GaN nanowires will depend on the orientation of the substrate that they are connected to. Koester *et al.* [15, 16] have used a non-catalytic GaN nanowire MOVPE growth technique, but the growth dielectric, SiN_x, is grown *in situ* inside the growth chamber prior to the nanowire growth. The nanowires grown by Koester *et al.* were also single crystal and epitaxially connected to the substrate underneath. The GaN nanowires grown by Hersee *et al.*, Koester *et al.*, and Bergbauer *et*

al. have a hexagonal cross-section and have 6 smooth non-polar m-plane sidewall facets, thereby giving us the opportunity to grow InGaN/GaN MQW's on these non-polar orientations devoid of the quantum confined stark effect. Koester *et al.* have demonstrated power dependent CL measurements from these MQW's on single GaN nanowires, which show no blue shift of the peak emission upon the increase in excitation power. The nanowire LEDs fabricated by Bergbauer *et al.* and Glo USA have the MQW's along the polar c-plane and semi-polar $\{10\bar{1}\bar{1}\}$ plane, in addition to the non-polar m-plane. The PL and CL measurements indicate different emissions corresponding to different indium incorporation in $In_xGa_{1-x}N$.

Cross-section TEM micrographs of the coaxial nanowires show the existence of threading defects, some in the $<1\bar{1}00>$ direction as a result of the defects bending and other threading defects that do not bend along the [0001] direction [41]. It has already been discussed in chapter 1 that threading defects play a detrimental role in the reverse breakdown voltage, the internal quantum efficiency and the device lifetime. Thus, it is important for the threading defects to be eliminated in the GaN based nanowire LEDs.

Koester *et al.* have fabricated single GaN core-shell LEDs to examine the electroluminescence (EL) from them. Bavencove *et al.* from the same group have reported the fabrication of single nanowire GaN based core-shell LEDs and an array of core-shell GaN based LEDs. I vs. V curves from Koester *et al.* and Bavencove *et al.* indicate a very high turn on voltage, which has been attributed to the low-conductivity of p-GaN grown on the m-plane GaN. C-plane GaN is normally doped with magnesium (Mg) to achieve p-type doping [39]. However, there haven't been many studies done on Mg-doped m-plane GaN grown by MOVPE. Mclaurin *et al.* [40] have published results

on Mg-doped m-plane GaN grown by plasma assisted molecular beam epitaxy (MBE) and have demonstrated hole concentrations of up to 7×10^{18} cm^{-3}. They have also analyzed the temperature dependent Hall Effect measurements and conclude that the Mg-related acceptor state in m-plane GaN is the same as that exhibited in c-plane GaN. Due to size limitations, it is extremely difficult to perform Hall measurements on p-GaN grown on the m-plane of the GaN nanowires of interest, both in this thesis and also the research pursued by the other groups reviewed in this chapter<consider revision of the statement, suggestion appreciated>.

Although, Bergbauer *et al.* haven't published any I vs. V characteristics from the coaxial LEDs, Deppner *et al.* from the same group have demonstrated theoretical simulations on GaN coaxial structures that are similar to those grown by Bergbauer *et al.* The simulations by Deppner *et al.* [26] have demonstrated differences in the opto-electronic characteristics of the three crystallographic orientations (polar (0001) plane, semi-polar (10-1-1) and non-polar (1-100) plane, respectively) and also that the presence of polar and semi-polar wells have been shown to limit the carrier injection efficiency in nonpolar wells. Mazuir *et al.* [7, 8] and Connors *et al.* [25] have investigated the current crowding in GaN coaxial LEDs by means of theoretical 2D simulations. Connors *et al.* [25] have also studied the simulations of different doping profiles in the core and the shell of the nanowire LEDs to reduce current crowding effects. A large area p-contact has been shown to be beneficial to the performance of the coaxial LEDs to promote better hole injection into the MQW's for light generation. Glo USA (based on discussion with glo USA personnel) have been investigating the use of indium tin oxide (ITO) as transparent contact to p-type GaN with around 96% transmission for 450nm wavelength

emission. Table 2.1 shows a comparison of the different strategies of growing GaN based coaxial LEDs. This table, together with the analyses above illustrates that the non-catalytic, *ex-situ* SiN_x based selective area growth technique is a more convenient technique to grow GaN based nanowires and coaxial LEDs, as compared to the VLS type growth.

Table 2.1 Comparison of the growth techniques employed to grow GaN nanowires

	VLS grown nanowires	***In situ* SiN_x assisted nanowire growth**	***Ex situ* SiN_x assisted nanowire growth**
Use of growth catalyst	metal ions	no catalyst	no catalyst
Use of Growth template	no template	no template	dielectric based growth template
Nanowire location	randomized	randomized	controlled
Nanowire diameter control	randomized	randomized	controlled
Growth substrate	any substrate	common substrates used for GaN heteroepitaxy	common substrates used for GaN heteroepitaxy
Nanowire cross-section	triangular	hexagonal	hexagonal
Nanowire sidewalls	2 semipolar 1 polar crystallographic orientations	6 non-polar m-plane crystallographic orientations	6 non-polar m-plane crystallographic orientations
LED processing	complicated, involves isolation of single nanowires	complicated, involves isolation of single nanowires	simple self aligned process, no nanowire isolation required
Large scale manufacturing capability	industrially non viable	industrially non-viable	industrially viable

Therefore, GaN based coaxial LEDs could potentially be beneficial for solving a number of issues affecting the planar GaN based LEDs of today. The coaxial LEDs should be based on a scalable GaN growth process that could also be investigated for mass production. The coaxial LEDs when grown in a regular array could potentially be

useful, either for individual addressability, or for parallel high power operation. Since the GaN would be grown only in specified area on the substrate, there is a potential to save a lot of precursor material for similar growth rates of LED structures. In addition to this, the process involved in fabricating these nanowire LEDs in a regular array should also be inexpensive, so as to cut down on the cost of these high efficiency (anticipated) LEDs. The high efficiency operation of these LEDs can be achieved by eliminating the threading defects in the active region, eliminating the quantum confined stark effect by growing MQW's on non-polar planes of the GaN nanowires and better light extraction to prevent re-absorption in the MQW's. All these benefits can be anticipated for the coaxial LEDs fabricated using UNM's nanowire growth and process steps. The study of the approach to achieving this will be discussed in the following four chapters to come.

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Chapter 3

Threading Defect Elimination in GaN Nanostructures

This chapter describes the elimination of threading defects (TDs) in GaN nanostructures (nanowires and nanowalls). The heteroepitaxy of GaN on a lattice-mismatched substrate (e. g. sapphire) results in the GaN film being strained on the substrate. For thickness beyond the critical thickness of GaN on sapphire, GaN relaxes and the strain energy is released by the formation of threading defects in the order of $10^8 – 10^{10}$ cm^{-2}. The threading defects propagate along the c-direction until they reach the surface where the defect energy is released. Hence, it is highly likely to find threading defects in the active region of a conventional, planar-structure LED. The high density of threading defects is thought to be the reason for the failure of GaN lasers [1] and the electrical breakdown of GaN p-n junctions [2]. They also play an important role in the increase of the reverse leakage current in LEDs [3]. Although, papers have been published indicating the internal quantum efficiency is immune to the threading defect density [4, 5], Dai *et al.* [6] have demonstrated that the IQE is significantly dependent on the threading defect density. Hence, the reduction in the threading defect density is proposed to be a possible mechanism for improving the quantum efficiency [7] and reducing the efficiency droop in GaN based LEDs [8].

However, the density of threading defects in [0001] GaN nanostructures grown at UNM was reduced considerably, even though these nanostructures are epitaxially connected to an underlying planar GaN film that has a defect density in the range 10^8 to 10^9 cm^{-2}[9]. Images obtained by cross-section transmission electron microscopy (XTEM)

reveal that the nominal [0001] line direction of a TD changes when that TD enters a GaN nanostructure. The line direction of the TDs bends towards the (0001) plane, and the dislocation rapidly terminates at a $\{1\bar{1}00\}$ sidewall facet of the nanostructure [9]. It is proposed that the reduction of the threading defect line energy is the driving force for this elimination mechanism. Furthermore, it is also anticipated that this TD elimination mechanism will be active whenever a threading defect is in close proximity to a surface. A model for this TD bending mechanism is proposed in case of a simplified nanowire crystal lattice, where it is shown as to how a pure edge defect can bend and terminate at a nanowire sidewall by a simple dislocation climb mechanism.

This chapter also describes the XTEM based defect analysis of GaN-AlGaN and GaN-InGaN core-shell nanostructures.

3.1 Cross-section transmission electron microscopy sample preparation

The samples for the XTEM were prepared and imaged at Evans Analytical Group, California. The sample preparation for the XTEM imaging involved three important steps. The first step involved defining the region of interest on the sample using a layer of high density metal like platinum (Pt). In our case, the nanostructures (nanowires and nanowalls) of interest were completely covered with platinum, as shown in Fig. 3.1. The second step was the introduction of a finely focused beam of metal ions using the focused ion beam (FIB) instrument to thin the sample by ion milling to a thickness $\leq$ 100nm, for the bright field XTEM analyses. Essentially, a lamella was created by the formation of trenches adjacent to the platinum coated regions on the three sides due to the sputtering away of sample material by the high energy ions.

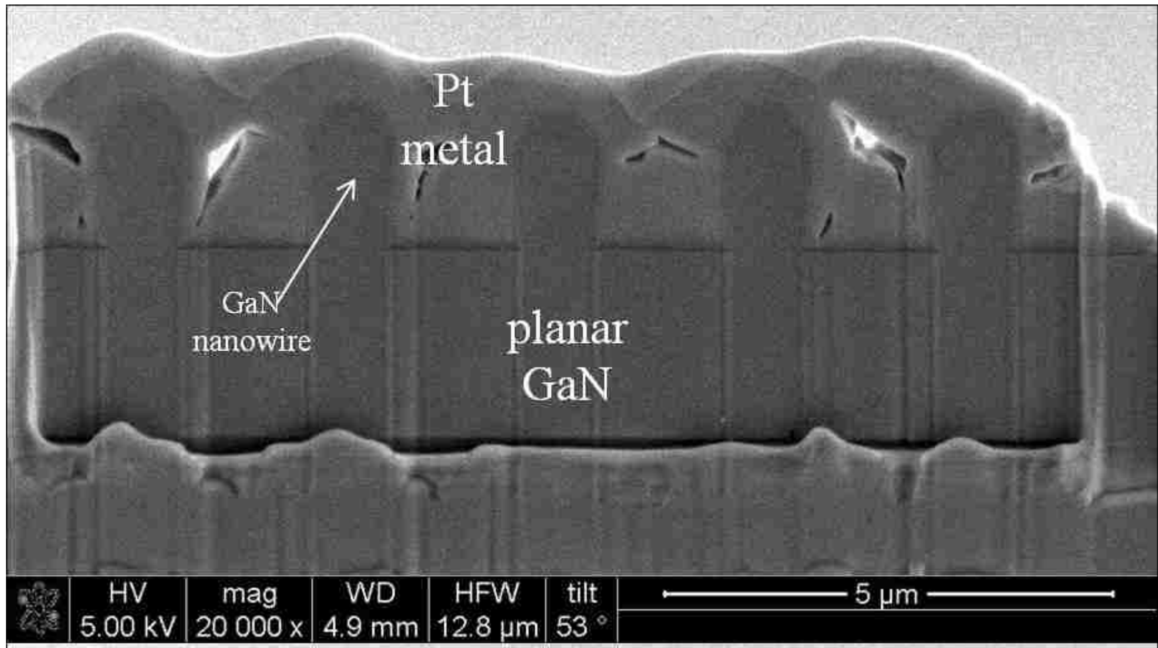

Fig. 3.1 Cross-section SEM image of GaN based nanowire array structures thinned by a FIB at Evans Analytical, California, showing Pt deposited on the nanowire structures

The thinning rate recorded for our samples (GaN on sapphire) was of the order of a few μm/hour, and hence, this process took at least 3-4 hours in order to obtain an electron transparent region. The FIB was integrated with a scanning electron microscope (SEM) making it extremely easy to image the sample in real time during the ion milling process. The third step after thinning of the sample was to transfer it using an in situ lift out technique using an internal nanomanipulator (also known as an omniprobe) to a TEM half-grid, which is then transferred to an XTEM instrument for imaging. The following subsections give us some details on the FIB process and how it could be damaging to some of the imaging applications in this thesis.

3.1.1 Functions of the FIB - SEM setup

The basic functions of the FIB-SEM setup are ion-milling of the nanostructures and the real time imaging of the sample during the ion-milling. Both these functions require a highly focused beam, one of ions (ion-milling) and the other, of electrons (SEM imaging). The liquid metal ion source (LMIS) is the typical ion source type used in all commercial and in the majority of research FIB systems [10, 11, 12]. In a LMIS, a metal with a low melting point, low vapor pressure and relatively low chemical reactivity is used. In addition to all these properties, the ion source should be heavy enough for ion milling applications. The low melting temperature of gallium makes it easy to be used and operated as the LMIS. Furthermore, gallium does not react with the material defining the needle (typically tungsten) and the evaporation is negligible. The presence of a strong electric field on the tip of the tungsten needle due to the applied extraction voltage results in the ionization of the gallium atoms.

In addition to the ion beam, there is also an electron gun to generate a beam of electrons that also impinge on the sample during the FIB based ion-milling. These electrons are used to generate secondary electrons on the surface of the sample that are then detected for the SEM imaging.

3.1.2 Theory of ion-milling

After the definition of the region of XTEM imaging interest using the deposition of a highly dense metal (e.g. Pt), ion milling is carried out to thin the sample from three different directions, as previously discussed in Fig. 3.1.

The Ga^+ ions generated by the high electric field at the tungsten needle tip were emitted in all possible directions, due to which, there was a need to focus the ion beam such that it could be directed towards the sample. The focusing of the beam of ions was achieved by a combination of electrostatic lenses using a procedure analogous to focusing of light. The simplest focusing systems consist of a collimating lens (also known as the condenser) followed by a focusing lens (also known as the objective) [12]. The micromachining precision was determined by the size and shape of the beam intensity profile on the sample and in general a smaller beam diameter leads to a better achievable milling precision.

The focused beam of Ga^+ ions was impinged on the desired region of the sample to initiate the ion-milling. The kinetic energy and momentum of the impinging ions were transferred to the solid through both inelastic and elastic interactions. The inelastic interactions between ions and the atoms (also called electronic energy loss) resulted in the ionization and emission of electrons and electromagnetic radiation from the sample. The elastic interactions between the ions and the atoms (also called nuclear energy loss) were transferred as translational energy to screened target atoms and resulted in the displacement of sample atoms from their specific locations and sputtering away from the sample surface.

3.1.3 Damages caused during FIB micromachining of GaN based nanostructures

In most cases of ion milling, there is sample damage due to the ion bombardment on the crystalline semiconductor surface. In some cases, the ions can thin a sample

beyond requirement, causing sample breakage. Hence, the precise control of the ion energy and angle is extremely important. A sample containing more than one type of material also has to deal with the issue of preferential milling, where one material is preferred over the other while the milling is occurring, leading to non-uniform sample thickness. Also, indium containing alloys (InGaN) are temperature sensitive. Since, the ion milling is an energetic process; it leads to localized heating of the sample. This can lead to either of two things; one is indium preferential sputtering and re-deposition and the other is formation of localized indium droplets, both of which have been reported by Cullis *et al.* [13] and Chew *et al*. [14]. Hence, a FIB type sample preparation is to be avoided while examining the $In_yGa_{1-y}N$ ('*y*' indicates percentage of indium). A mechanical polishing technique is more commonly employed for these, which seems to be better suited to give good XTEM and energy dispersive spectrometry (EDS) data.

3.2 Experimental XTEM evidence for bending of threading defects

The nanostructures (nanowires and nanowalls) were grown by UNM's pulsed Metal Organic Chemical Vapor deposition (MOCVD) growth process [ref] using standard high-purity metal organic and ammonia precursors as in regular MOCVD growth without the use of metal catalysts. In this selective area growth process, the nanostructures were grown onto underlying planar (0001) GaN films using selective growth in growth templates that were nano-patterned to have either holes or line apertures. Further details of the growth are discussed in chapter 4 of this thesis. After the growth, the sample was loaded in the FIB-SEM setup to prepare a sample thin enough for it to be transparent for electrons during the TEM examination. The TDs were imaged

inside these nanostructures using bright-field XTEM analysis of thinned nanowire and nanowall samples. In total, at least 100 nanostructures have been analyzed by XTEM.

3.2.1 Bending of threading defects in GaN nanowires

The TD density was previously measured to be in the range of 10^8 to 10^9 cm^{-2} in the underlying GaN planar film [3]. Given that the nanowires are epitaxially connected to this underlying GaN planar film, it was initially assumed that the TD density would be the same in the GaN nanowires as it was in the GaN planar film. Thus, in the ~100 nanowires that we have analyzed by XTEM, which represents a total cross-sectional area of >10^{-5} cm^2, it was expected to observe at least 10^{-5} cm^2 x 10^8 to 10^9 cm^{-2} = 1000 to 10,000 threading defects. In fact, **none** of the nanowires had a TD that continued to the top (c-face) surface.

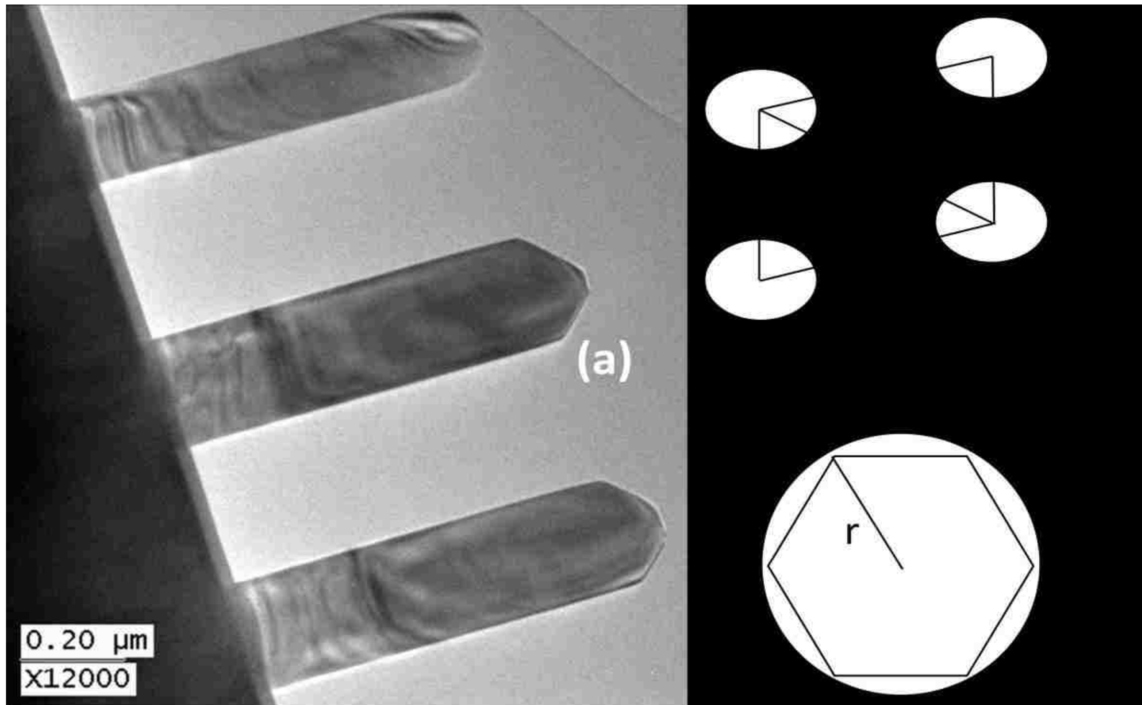

Fig. 3.2(a) XTEM of a 200nm diameter GaN nanowire on a 500nm pitch (b) a pictorial representation of a section of the array of holes and the hexagonal GaN filling in the hole, as explained in [22]

Hence, an additional defect elimination mechanism was found to be prevailing in these nanowires by the careful examination of the XTEM images. Fig. 3.2(a) shows a bright-field, XTEM micrograph of part of a GaN nanowire array. TDs are clearly observed in the planar GaN layer beneath the GaN nanowire (Fig. 3.3(a)), yet these defects are absent in the nanowire. The explanation for this behavior is revealed in Fig. 3.3. In Fig. 3.3(a), a TD is observed to enter the base of the nanowire, then to bend and terminate at the nanowire $\{1\bar{1}00\}$ sidewall. The subsequently grown GaN nanowire material is then defect-free. Fig. 3.3(b) shows another example of this bending and termination behavior. In this case bending occurs at the very start of the nanowire.

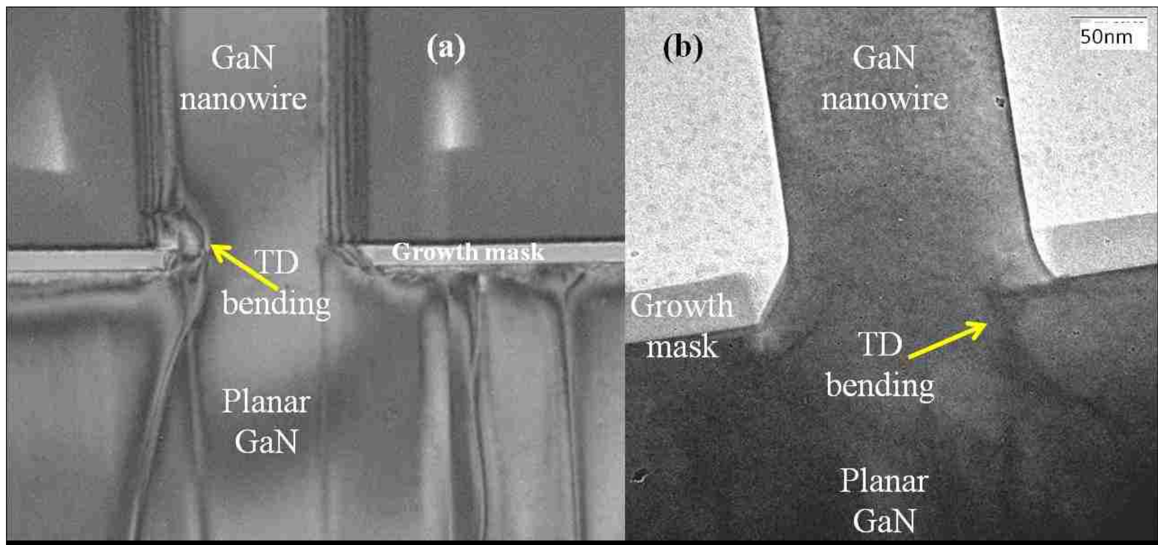

Fig. 3.3 (a) XTEM image of a GaN nanowire showing a TD bending towards the $\{1\bar{1}00\}$ sidewall after having entered the nanowire and (b) a XTEM image of GaN nanowire showing the bending by 90° and termination of a TD near the growth pattern mask

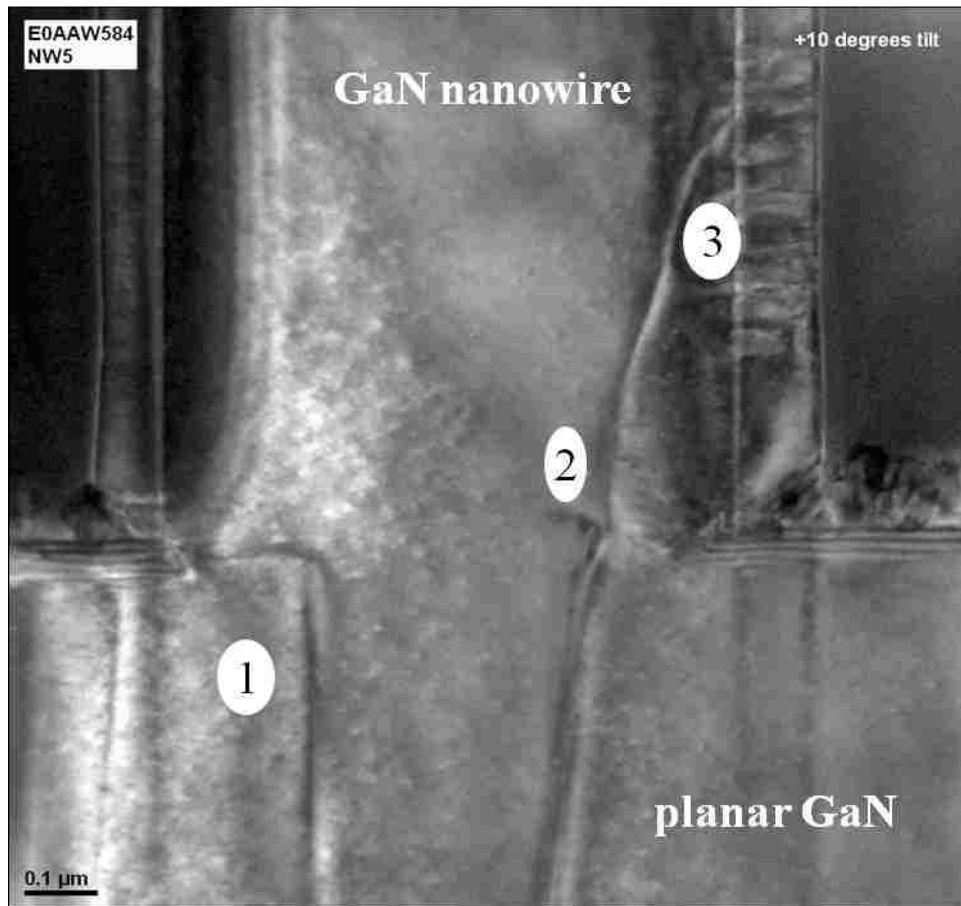

Fig. 3.4 XTEM image of a GaN nanowire taken at a 10° tilt showing three TDs labeled, (1) is observed to bend 90o to terminate near the growth mask, (2) is observed to bend and disappear in middle of the nanowire and (3) is observed to enter the nanowire, but bends in multiple steps, finally reaching the $\{1\bar{1}00\}$sidewall

Fig. 3.4 is a perfect indication of the three types of defect bending observations. The TEM image was taken at a 10° tilt with respect to the normal incidence to observe two different threading defects (2 and 3 as pointed in Fig. 3.4) at almost a similar location in the cross-section view. The TD labeled 1, bends at the very start of the nanowire growth and bends 90° towards the sidewall. The TD labeled 2 bends a little later, but seems to disappear, indication of it bending perpendicular to one of the in-plane

directions. The TD labeled 3 eventually bends in about 200nm of vertical c-direction ([0001]) travel from the GaN planar-nanowire boundary. TD bending similar to that of 3 has been observed numerous times, indicating multiple bending until they bend and terminate horizontally along the <$1\bar{1}00$> direction. This implies that bending of threading defects can occur in several steps instead of terminating at the top c-plane surface. These observations also indicate that the TD is able to reduce its length and therefore its line energy by bending and terminating at one of the six $\{1\bar{1}00\}$ sidewall planes that bind the nanowire. The observed absence of TDs in these nanowires indicates that this bending and termination process is highly efficient.

3.2.2 Bending of threading defects in GaN nanowalls

The bending of TDs was also observed in the nanowall structures. A section of the nanowall is shown Fig. 3.5(a). This shows the position of a sample thinned by the FIB in the XTEM sample preparation along the length of the nanowall and the direction of XTEM viewing of this sample, which is perpendicular to a $\{1\bar{1}00\}$ m-plane. Fig. 3.5(b) shows the bright-field XTEM image of a nanowall sample. In this sample, a TD is observed to terminate, just above the interface between the nanowall and the planar GaN layer. A TD cannot terminate inside a single crystal semiconductor. Hence, it can be interpreted that this apparent termination occurs because the TD bends towards the m-plane sidewall facet that was either in front, or behind the thinned nanowall sample. Fig. 3.5(c) shows a closer view of the disappearance of the TD. We can observe another TD appearing out of nowhere in the sample, which disappears once again after a few nanometers upwards, as shown in Fig. 3.5(c) along the c-direction, into the nanowall,

indicative of bending towards an m plane sidewall. The rest of the nanowall above this region is defect free.

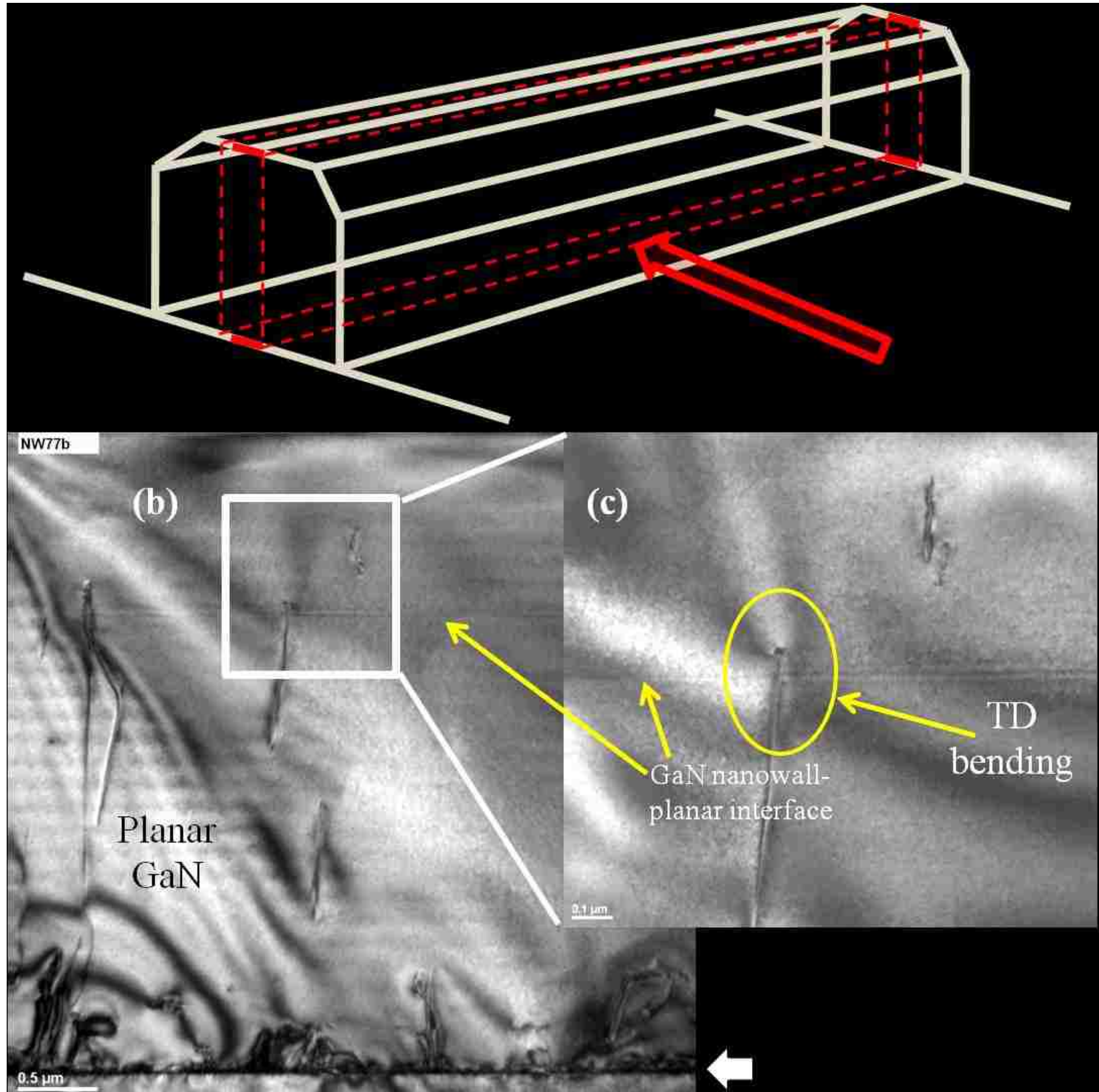

Fig. 3.5 (a) Pictorial representation of a GaN nanowall sample showing the cross-section at which the XTEM image (b) was obtained. (b) shows bending of the TDs after the GaN nanowall-planar interface. (c) shows a closer view of the TD bending and disappearance in the nanowall, indication of bending towards a surface

3.3 Analysis of bending of threading defects

According to the corollary to the third law of thermodynamics, any physical system tries to achieve a state of minimum free energy, at a given temperature. Threading defects are non-equilibrium defects that raise the free energy of epitaxially grown film and hence, there is a thermodynamic driving force that tries to reduce the TD density. Hence, a TD in a crystalline semiconductor would also want to minimize its free energy. The TD bending and termination process is likely to occur in any structure where the TD is located in the vicinity of a sidewall. This process is highly efficient because most of the GaN nanowire XTEM images that were observed were devoid of TDs, even though the epitaxial GaN under layer contained a defect density in the order of 10^9 to 10^{10} cm^{-2}. The dislocation energy (edge or screw) is proportional to the length of the dislocation itself. Hence, it is proposed that the driving force for this TD elimination mechanism is the reduction of the dislocation line energy that occurs because the dislocation shortens its length by bending and terminating at a nanowire sidewall. This energy reduction can be significant. Given the normal nanostructure geometry, where the height is greater than the diameter, this line energy is therefore reduced for a TD that bends and terminates at a sidewall as compared to a TD that is aligned along the c-direction of the nanostructure. In the following subsections, theoretical insights leading into the explanation of bending of TDs has been presented.

3.3.1 Elastic energy reduction in TDs

The distortion in the crystal structure due to the TD leads to the implication that a crystal containing a TD is not in its lowest energy state. The energy per unit length

corresponding to the TD is stored as the strain energy, E_{strain} [16]. The bending of TDs could be explained in terms of reduction of this strain energy, which could be resolved into a core component, E_{core} and an elastic component, $E_{elastic}$. Thus, the energy per unit length of a TD can be represented as below,

$$E_{strain} = E_{core} + E_{elastic} \qquad - \qquad (1)$$

The theoretical estimates of E_{core} reveal that the core energy would be a very small fraction of the total strain energy. It has been estimated that the core energy would be of the order of 1eV for each atom plane threaded by the TD [17], which is approximately equal to about 0.36eV/Å. However, the elastic energy ($E_{elastic}$) of a pure edge TD was calculated to be around 6eV for each atom plane threaded by the defect, which is approximately equal to around 2.2eV/Å. Thus, it is convenient to approximate the entire defect line energy as arising from the elastic component of the strain energy.

For a pure edge TD in GaN with a shear modulus G, Poisson's ratio ϑ and Burgers vector b, the $E_{elastic}$ can be written as below: -

$$E_{elastic}(edge) = \frac{Gb^2}{4\pi(1-\vartheta)} ln\left(\frac{R}{r_o}\right) \qquad - \qquad (2)$$

where, r_o is the core radius and R is the outer radius of the dislocation respectively as described in [18]. Similarly, the $E_{elastic}$ for a screw and a mixed TD can be written using the same definitions above as below: -

$$E_{elastic}(screw) = \frac{Gb^2}{4\pi} ln\left(\frac{R}{r_o}\right) \qquad - \qquad (3)$$

$$E_{elastic}(mixed) = \frac{Gb^2(1-\vartheta cos^2\theta)}{4\pi(1-\vartheta)} ln\left(\frac{R}{r_o}\right) \quad - \quad (4)$$

where, θ is the angle between the Burgers vector of the mixed TD and the line direction of the TD. Noting that the Poisson's ratio, ϑ is always less than '1', for a given Burgers vector, the energy per unit length of an edge TD is maximum, while that of a screw TD is minimum and the energy per unit length of a mixed TD is in between that of a screw and an edge TD with the same Burgers vector. It is thus energetically favorable for an edge TD aligned along the [0001] direction to bend 90° and convert either into a pure screw or a mixed TD. However, for a screw dislocation, bending by 90° indicates the conversion into an edge TD, which has a higher energy per unit length for a given Burgers vector, which is not energetically favorable. Thus, this explanation cannot explain the bending of [0001] screw dislocations. Hence, the reduction in the elastic energy per unit length is not necessarily the driving force in all cases to cause the bending of TDs.

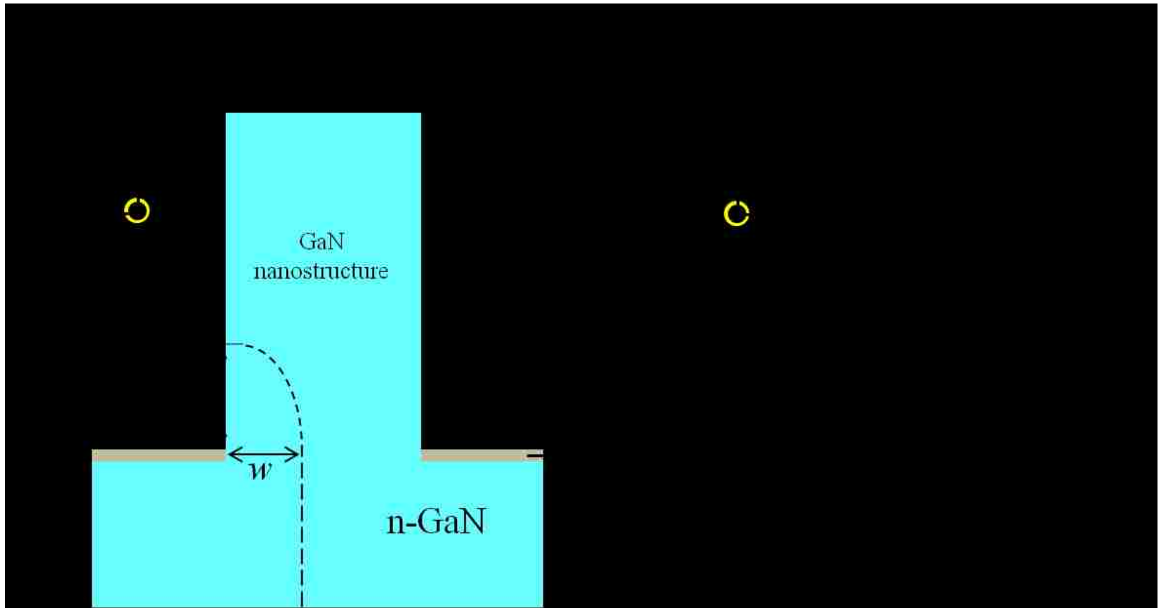

Fig. 3.6 (a) The pictographic illustration of a TD bending towards the sidewall of GaN nanostructure due to the image force acting on the edge TD located at a distance '*w*', as shown in (b)

3.3.2 Bending of TD caused due to image forces near surfaces

The changes in the free energy of a crystalline semiconductor with respect to the displacement of a TD from its propagation line direction is related to the virtual image elastic force that acts on a TD due to the influence of a free substrate [19]. Let us consider a pure edge TD aligned along the [0001] c-direction with a Burgers vector *b* in the c-plane of the GaN nanostructure at a distance *w* from the free surface, as shown in the Fig. 3.6(a). The force per unit length on the TD in the c-plane of the nanostructure due to the presence of the surface in close proximity can be obtained by simply constructing an imaginary TD at the same distance *w* from the surface, but on the opposite side of the plane as shown in Fig. 3.6(b). The image force on a TD (edge and screw) can be written in analytical equation form (using similar definitions as in equations (1)-(4)) as below: -

$$F_{c-plane}(edge) = \frac{-Gb^2}{4\pi(1-\vartheta)w} \qquad - \qquad (5)$$

$$F_{c-plane}(screw) = \frac{-Gb^2}{4\pi w} \qquad - \qquad (6)$$

The negative sign in the force equation is indicative of an attractive force towards the surface in close proximity. From the above equations, it is possible to conclude that image forces on TDs are slowly varying $\frac{1}{w}$ type forces. Thus, it is extremely likely that a TD in close proximity to a surface is attracted towards a surface due to the image force acting on it, thereby causing elimination of TDs from near-surface regions. It is also worth noting that the force on a pure edge TD is greater, in comparison to a pure screw TD with a similar Burgers vector magnitude. However, upon the onset of bending in the TDs, a pure edge TD would be converted into a mixed TD. Thus the force per unit length acting on the TD at this point is complicated and cannot be addressed just using one of the above two analytical equations in order to identify the change in free energy due to the bending.

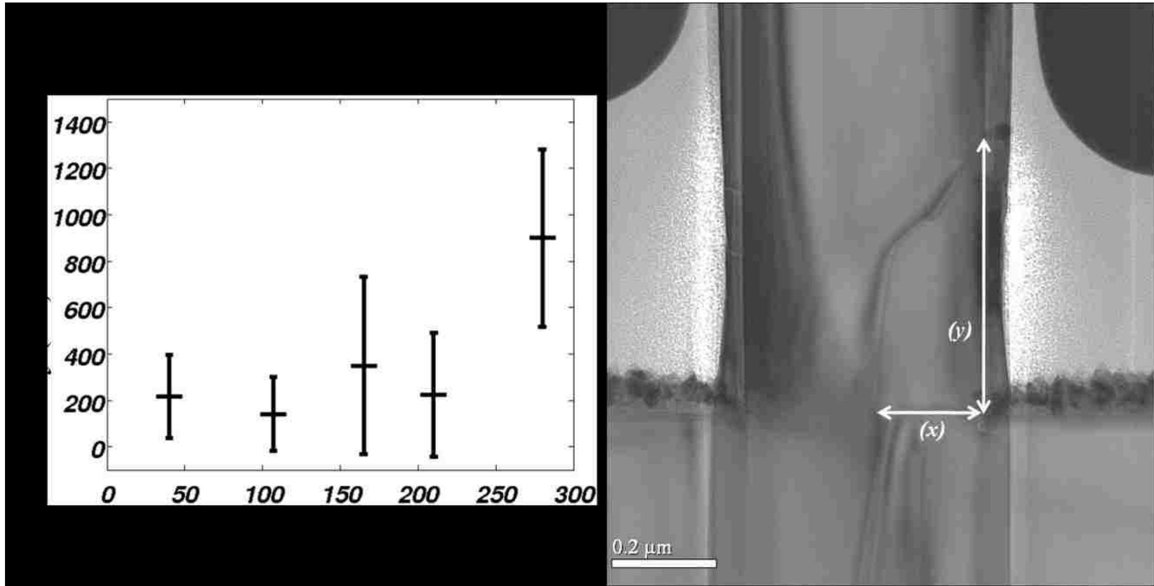

Fig. 3.7 The correlation of the [0001] length of the TD with the lateral distance from the nanostructure sidewall surface is shown. The TD [0001] length and the lateral distance from the sidewall facet is defined in (b)

3.3.3 Analysis of TDs in GaN nanostructures grown at UNM

A study was then conducted, as shown in Fig. 3.7 to investigate the exact mechanism of this bending. For the defects that showed the bending behavior, the distance of the TD from the nanostructure sidewall was noted along with the vertical [0001] distance that it took each threading defect to bend towards a sidewall, as shown in Fig. 3.7(b). It is to be noted that there is a significant scatter in this data due to the low number of these observations. The vertical [0001] length of the TD as a function of the lateral distance of the TD from the nearest sidewall facet is plotted in Fig 3.7(a). We observe a correlation between these two vector points. When the TD is further from the sidewall facet, the vertical [0001] extent of the TD is greater, when this TD is further from the sidewall facet.

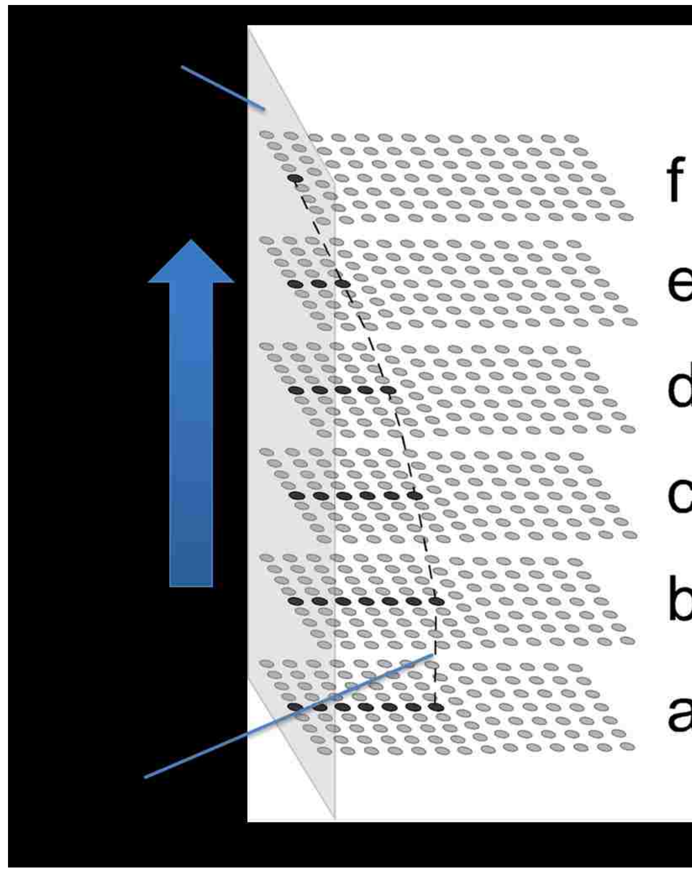

Fig. 3.8 A simple model illustrating the TD elimination by climb. The model is shown here for a simple cubic crystal, for understanding, but is proposed to be valid even for hexagonal dielemental semiconductor like GaN

A simple model of the bending mechanism is shown in Fig. 3.8. For simplicity, it is assumed that the TD is a pure edge dislocation in a cubic lattice. We consider a vertical length (a to b) of a TD that has entered the nanowire from an underlying planar layer and is 7 atomic spacings from the sidewall facet. The growth direction and the initial TD line direction are both in the vertical [0001] direction. As the growth proceeds vertically (atomic layers are added sequentially from *a* through *f*), the tip of the TD moves towards the nanowire sidewall, simply by climb. It is proposed that this bending by climb is bound to occur under the influence of the image force from the sidewall facet, as discussed in the earlier section. As this continues, eventually the TD reaches the sidewall

surface and terminates, there by leaving the growth portion above it, defect free. The termination of the TDs via conversion to another defect type is expected to be energetically unfavorable. It has been reported in literature that a pure edge TD could terminate on a stacking fault in the (0001) plane and thus be eliminated [20]. However, it is anticipated that for a stacking fault to be formed, displacement of a large number of atoms is required, which is unfavorable, as far as free energy is concerned.

The device structures grown in annulus growth patterns, as illustrated in Fig. 3.9 presents us with the advantage of a large area defect free templates to grow coaxial LEDs. The line width shown in Fig. 3.9(a) can be of sub-micron dimension, which would promote TD bending and elimination by the different mechanisms illustrated in the previous sections. Fig. 3.9(b) shows an SEM image of GaN grown in the hexagonal annulus growth apertures.

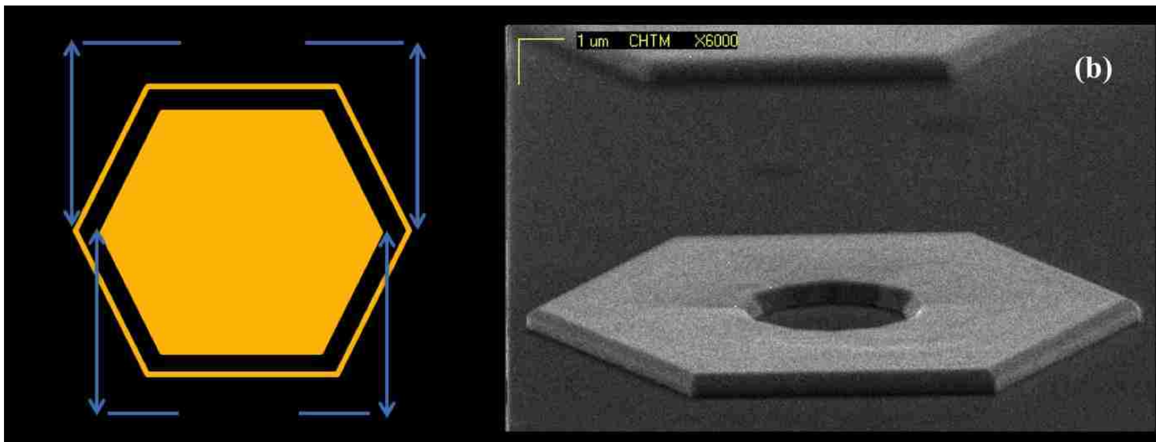

Fig. 3.9 (a) shows an illustration of annulus hexagonal growth patterns and (b) shows a SEM image of GaN grown selectively in hexagonal annulus patterns illustrated in (a). These structures would also promote TD elimination by mechanisms discussed in this section.

3.4 Coaxial Nanostructures: Study of defects

The nanostructures being studied in this thesis were fabricated using regular metal organics and ammonia in a MOCVD reactor. The details of the growth process are discussed in section 5.1 of chapter 5. As discussed in section 1.2.1 of chapter 1, owing to their non polar nature, these m-plane sidewalls are of significance in terms of fabricating quantum wells on them. For this reason, XTEM analyses were also performed on ternary alloys AlGaN and InGaN grown coaxially onto these m-plane sidewalls. Fig. 10 shows SEM images of coaxial AlGaN on GaN nanowire cores. The inner GaN core was doped n-type, and the outer AlGaN shell was doped p-type. The AlGaN layer consists of a shell approximately 50 nm thick, of $Al_{0.1}Ga_{0.9}N$ grown coaxially around a 300 nm diameter GaN nanowire core. The details of the coaxial pulsed growth of GaN based nanowires and AlGaN coaxial growth on GaN nanowire cores have been discussed in [28]. The details of coaxial pulsed growth of 3D GaN nanowalls and microstructures is discussed in chapter 4, while the growth of AlGaN and InGaN shells around 3D GaN core structures is discussed further in chapter 5.

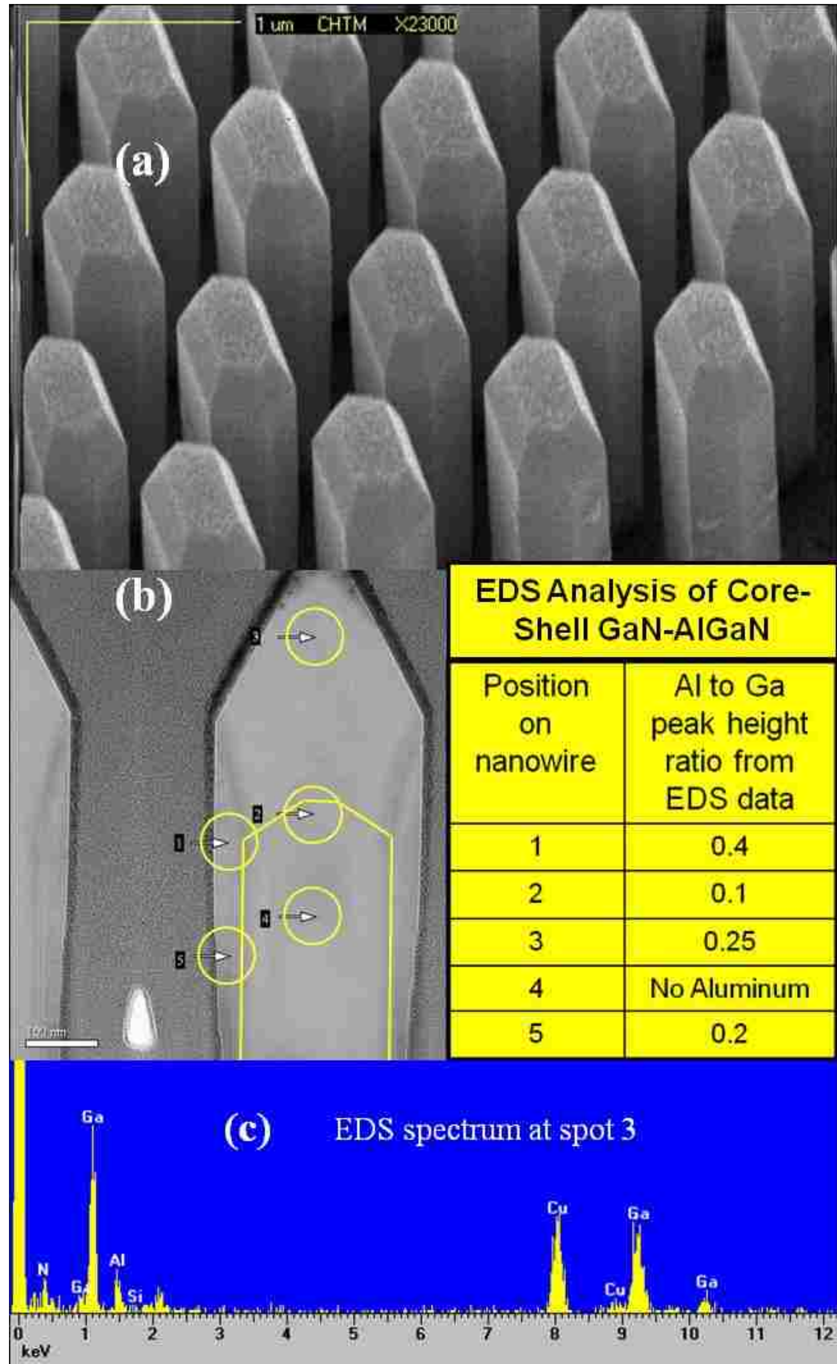

Fig. 3.10 (a) a 45° tilt SEM image of GaN-AlGaN core-shell nanowire is shown, whose XTEM image has been shown in (b) with the EDS measurements at different locations on the nanowire. The EDS spectra ((c) shows an example of an EDS spectrum at location 3 in (b)) show the presence of Al in all locations except 4, indication of a GaN core surrounded by AlGaN shell

An example of energy dispersive x-ray spectroscopy (EDS) spectra obtained on the GaN-AlGaN core-shell samples is shown in Fig. 3.10(c). The SEM, TEM and EDS characterization of AlGaN shell structures on GaN core structures are also discussed further in section 4.3 of chapter 4. EDS performed at different regions of the AlGaN on GaN XTEM sample shown in Fig 3.10(b) shows an AlGaN shell on the GaN nanowire core. The EDS is not able to give accurate quantitative information on the AlGaN composition and the spatial resolution of the EDS measurement was approximately 50nm as represented by the diameter of the yellow circles in Fig. 3.10. The EDS was however able to confirm that aluminum was present only in the outer shell and not in the inner nanowire core (position 4). The rest of the outer positions, marked by the arrow do show the presence of Al, indicative of the inner GaN nanowire being coated coaxially by an outer, coaxial $Al_xGa_{1-x}N$ layer, as required for the coaxial LED. The GaN-AlGaN structure is shown to remain defect free and the sidewall facets are smooth, after the heterojunction formation has occurred. Even at 65nm thickness, m-plane AlGaN doesn't show any sign of strain relaxation on GaN, thereby the formation of threading defects at the GaN-AlGaN interface was not observed.

The GaN-InGaN heterojunction (Fig. 3.11) consists of a shell of approximately 50 nm of $In_{0.07}Ga_{0.93}N$ grown coaxially around a 300 nm diameter GaN nanowire core. SEM analysis (Fig. 3.11(a)) shows a non-smooth surface with petal like non-planar deposits on the $\{1\bar{1}00\}$ sidewall. Here, it was assumed that indium had segregated to the surface of the nanowire $\{1\bar{1}00\}$ sidewall creating indium-rich "deposits" on the sidewall surface.

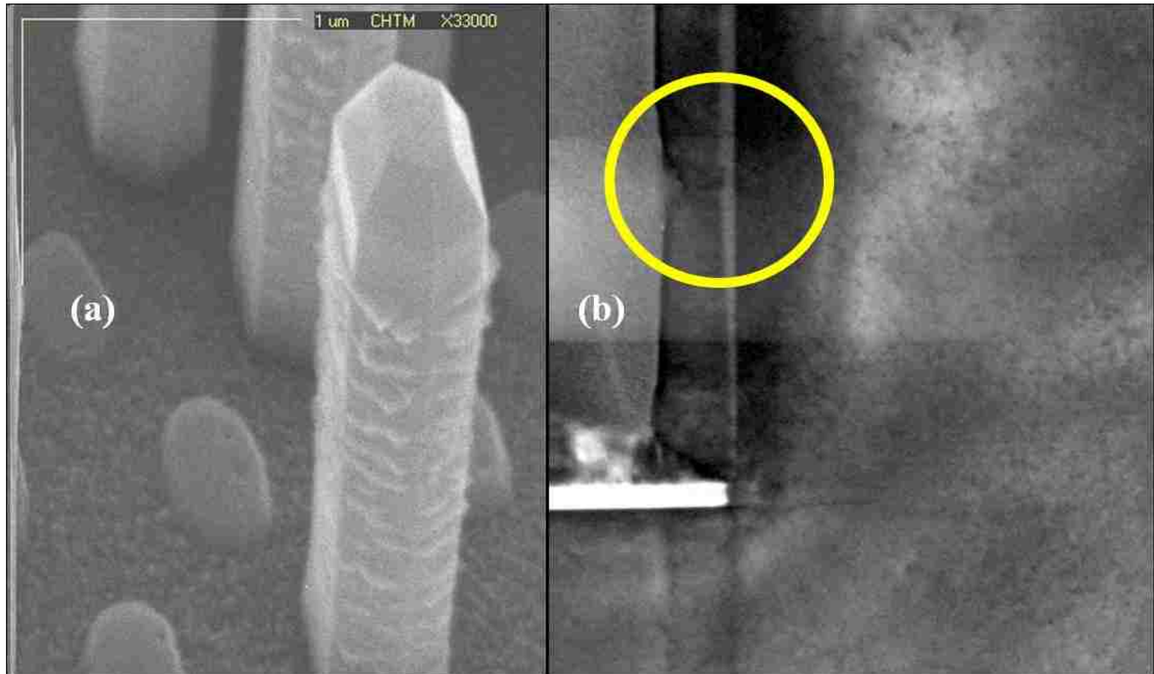

Fig. 3.11 (a) a 45° tilt SEM image of GaN-InGaN core-shell nanowire showing indium segregation in the form of petals. (b) XTEM of GaN-InGaN core-shell nanowire showing a crater in the InGaN layer

However, these indium rich deposits are not observed after the XTEM sample preparation using FIB. This was because indium would be preferentially sputtered away during the sample preparation using FIB [23]. XTEM analysis of these samples (Fig. 11(b)) revealed that these petal like non-planar deposit regions were associated with craters in the InGaN layer. These craters are related to the InGaN layer and were not observed while AlGaN shell was grown on the GaN nanowires. Also, it is observed that these defects do not propagate from the InGaN layer back into the GaN core, so even though the InGaN shell layer had defects, the inner GaN core remained free of defects. These defects have some geometrical similarity to the "vee" defects induced by threading dislocations in GaN [21], which are also as a result of phase separation or segregation of Indium. However, those previously observed "vee" defects are induced by TDs and are generally found to occur in the [0001] direction. The defects that we observe here are

oriented perpendicular to the [0001] direction. Further work like high resolution TEM might be able to explain this observed defect type. Hang *et al.* [24] have observed similar surface roughness on InGaN grown on m-plane GaN. The surface roughness was associated with basal plane stacking faults underneath that were oriented parallel to the $\{1\bar{1}00\}$ direction. Fisher *et al.* [24] have observed Frank type stacking faults, where the c-plane was abruptly stopped at the first InGaN quantum well. Wu *et al.* [25] have also observed that TDs and stacking faults were generated in high indium content m-plane InGaN multi-quantum wells on m-plane GaN.

3.5 Study of threading defects in 3D grown GaN microstructures

In the previous sections, the elimination of TDs in GaN based core and core-shell nanostructures has been discussed. It was concluded that whenever a TD was in close proximity to a surface, it would bend towards the surface. Numerous cross-section TEM images of the GaN nanostructure were analyzed in order to confirm the above observation. However, it was necessary to analyze the limit of defect free nanostructure fabrication. In other words, it was important to find out the maximum lateral distance of the TD from the sidewall surface, until which the bending of the TD to the sidewall surface could occur. Cross-section TEM images of GaN microstructures were analyzed to study the above limit. Fig. 3.12 shows the cross-section SEM image of 3D GaN microstructure grown by pulsed MOVPE. The details of the growth are discussed in chapter 4.

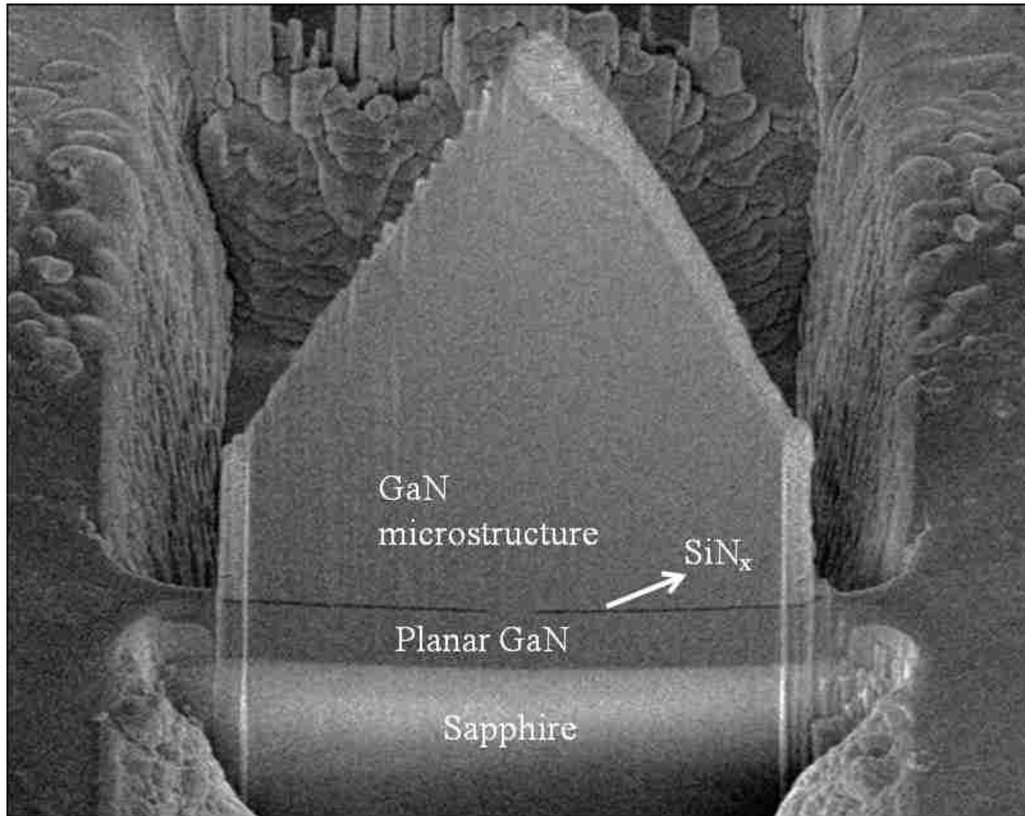

Fig. 3.12 The cross-section SEM of a 3D GaN microstructure grown by pulsed MOVPE. The cross-section was prepared using FIB

Fig. 3.13 shows the cross-section TEM image of the 3D GaN microstructure. Three TDs are labeled 1, 2 and 3 as shown in Fig. 3.13(a). The TD labeled 1 terminates at the interface between the planar GaN and the growth dielectric (SiN_x) layer. The defect labeled 2 is observed to be in close proximity to the GaN-dielectric surface. Upon close examination of the image, it is possible to conclude that the TD labeled 2 bends around the dielectric layer and terminates at the surface near the interface of GaN and SiN_x. However, the TD labeled 3 does not bend, instead is aligned along the <0001> direction, terminating at the top of the microstructure. Interestingly, the TD labeled 3 is located almost midway of the growth aperture, as shown in Fig. 3.13(b). Hence, it is quite possible that the image forces acting on the TD from the surrounding 6 $\{1\bar{1}00\}$ sidewall

facets were nearly equal in magnitude, but opposite in direction, there by leading to the TD continuing to be aligned along the c-direction, instead of bending.

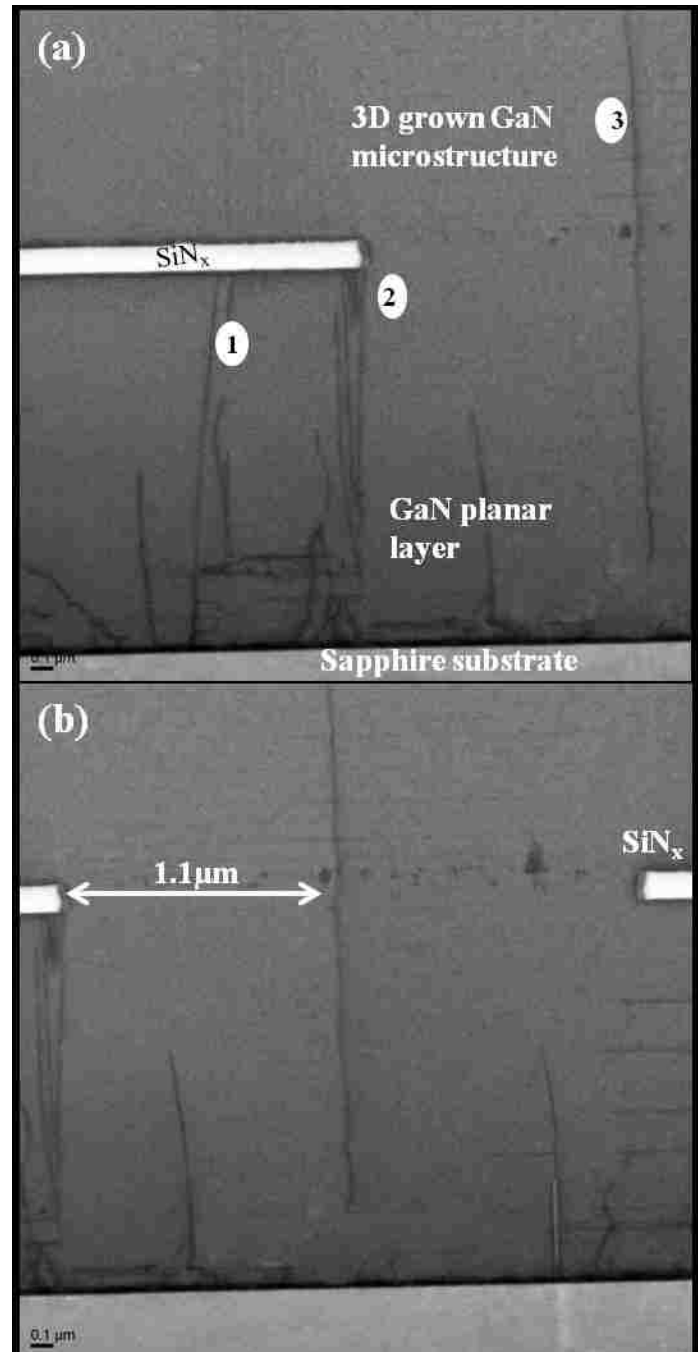

Fig. 3.13 (a) The cross-section TEM image of 3D GaN microstructure showing the three TDs labeled 1, 2 and 3. The bottom image represents the low magnification version of the top image, illustrating the lateral distance of the TD from the sidewall

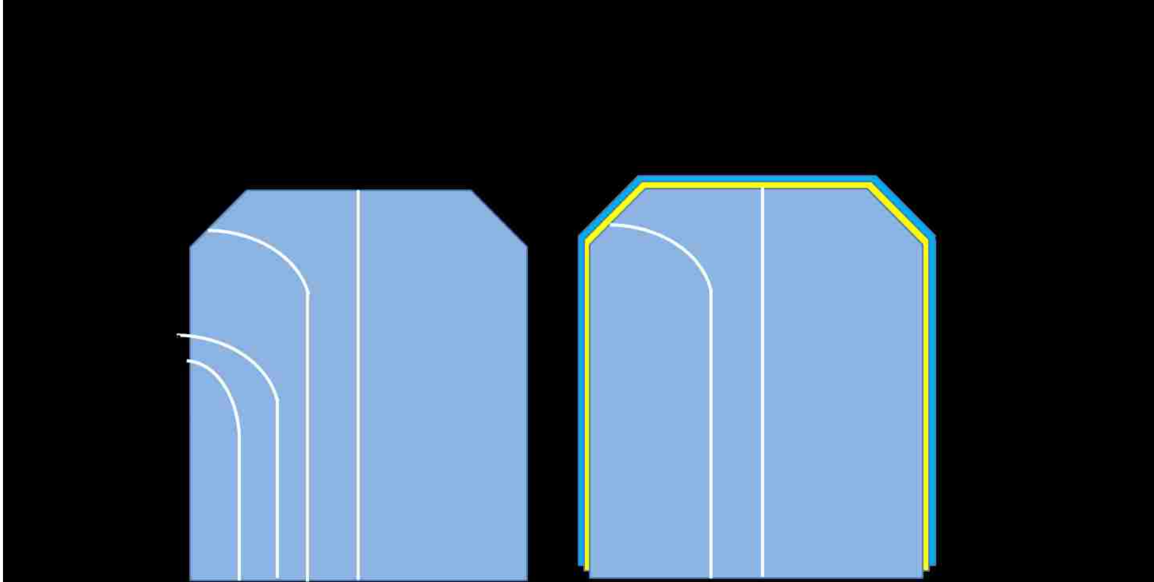

Fig. 3.14 A pictographic illustration of the TDs in a 3D GaN microstructure showing the bending of TDs in close proximity to sidewall and also the TDs further interior of the structure just propagate without bending. This could be beneficial for TD free m-plane active regions, as shown in (b)

Fig. 3.14 presents a pictographic illustration of the observations so far. It can be concluded that the TDs at the close proximity to a $\{1\bar{1}00\}$ sidewall could bend and terminate at the sidewall, simply by glide or climb. Li *et al.* [27] have also observed similar behavior of TDs in their GaN microstructures grown on pre-patterned silicon pillar arrays. It was observed by Li *et al.* that due to the large surface area to volume ratio of the 3D GaN microstructures, TDs could glide or climb and bend, causing termination of the TD at the nearby sidewall facet, thereby reducing the defect density in the top part of the GaN nanostructure. This effect was believed to be more prominent in structures that had high aspect ratios. However, we can conclude that, as the lateral distance of the TD location from a sidewall facet increased, it was less probable for a TD to bend and terminate on a sidewall. It was more energetically favorable for a TD to propagate along the <0001> direction and release the energy to the top surface, rather than bending to a

sidewall in close proximity. This leads to the $\{1\bar{1}00\}$ m-planes being defect free, thereby leading to a defect free active region in the coaxial LEDs.

Thus, there exists a critical lateral distance from a 3D GaN structure's sidewall beyond which, if a TD was located in the interior of the microstructure, it would continue to be aligned along the c-direction. This observation further strengthens the need for GaN based nanostructured LEDs, as opposed to microstructured LEDs, in terms of zero defect devices.

3.6 Conclusion

In this chapter, we have analyzed and demonstrated the elimination of TDs in GaN based nanostructures. The process of TD elimination is expected to occur extremely efficiently when the TD is within a certain capture distance of the sidewall facet of the nanostructures. It is anticipated from these analyses that sub micron (< 1μm diameter) nanostructures are likely to be defect free. As the lateral size of the nanostructure increases, this TD elimination process becomes less efficient and non-zero TD densities can be expected inside the structure. In the nanowall structures, if one of their lateral dimensions is in the submicron range, then at least 2 out of 6 nanowall sidewall facets are within close proximity to any TD and hence TD elimination by defect bending is anticipated. However, with the increase in the lateral dimensions of the structures, the TDs interior to the structure did not bend towards the sidewalls, instead were observed to aligned along the <0001> direction.

The addition of ternary alloys (AlGaN and InGaN) coaxially to n-GaN core does not appear to be modifying the TD behavior that was observed for the simple GaN

nanostructures. However, for the coaxial InGaN-GaN heterostructures, a new defect type was observed and clearly further work is necessary to improve the material quality.

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[22] For the nanowires in Fig. 2(a), which have a diameter of 200 nm and a pitch of 500 nm, the nanowire cross-section area is approximately 12% of the underlying planar film area. Considering the nanowires in the rhombic lattice array we have here, the diameter is 200nm; the pitch is 500nm and we seem to have a full hole in a given lattice as shown in Fig. 2 (b) above. The single crystal nanowires are hexagonal in cross section and so fill the circle as shown. Hence, the exact % filtering that we would observe is about 12%. In this, it would be expected that the TD density of 10^9 to 10^{10} cm^{-2} in the planar film would fall to approximately 10^8 to 10^9 cm^{-2} in the nanowires. In other words, it would mean that, in about a hundred nanowire XTEM images that we have now examined we would expect to see TDs in about 12 of them. Fig 2(a) shows the XTEM of 200nm GaN nanowires on a 500nm pitch. This image shows the absence of threading defects in the GaN nanowire.

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Chapter 4

MOVPE Growth of 3D GaN Structures

The growth of GaN based nanowire structures, using selective area growth (SAG), has already been introduced in chapter 2 of this thesis. Hersee *et al.* [1] were the first group to develop the growth process for GaN nanowires using this technique. This chapter presents an extension to the work previously pursued in our group [2], to larger circular aperture, wall structures (as introduced in chapter 1 section 1.2.3 and chapter 3 section 3.2.2) and annulus apertures (as introduced in chapter 3 section 3.3.2). Other groups like Bergbauer *et al.* [3] and companies like glo USA and nanocrystal Asia are also employing a similar SAG technique to grow GaN nanowires and GaN based coaxial LEDs, which was already discussed in section 2.2 of chapter 2. The 3D GaN structures grown for this work have been imaged using a JEOL SEM for measuring growth rates and the capture radius discussed in section 4.2. In addition to SEM, photoluminescence and TEM have also been used to characterize the GaN nanowires and the coaxial LEDs grown.

4.1 Growth of 3D GaN structures

The SAG technique of 3D GaN structures grown in this thesis involves 4 steps as described in Fig. 4.1. The first step involves the growth of a planar GaN substrate. The next step is to deposit a layer of dielectric growth mask on the planar GaN. The third step involves the patterning of the growth mask dielectric into circular or line apertures to expose the planar GaN in those regions. The last, but the most important step, is to grow GaN 3D structures from the openings specified in the third step. These four steps are discussed in detail in the following sub-sections.

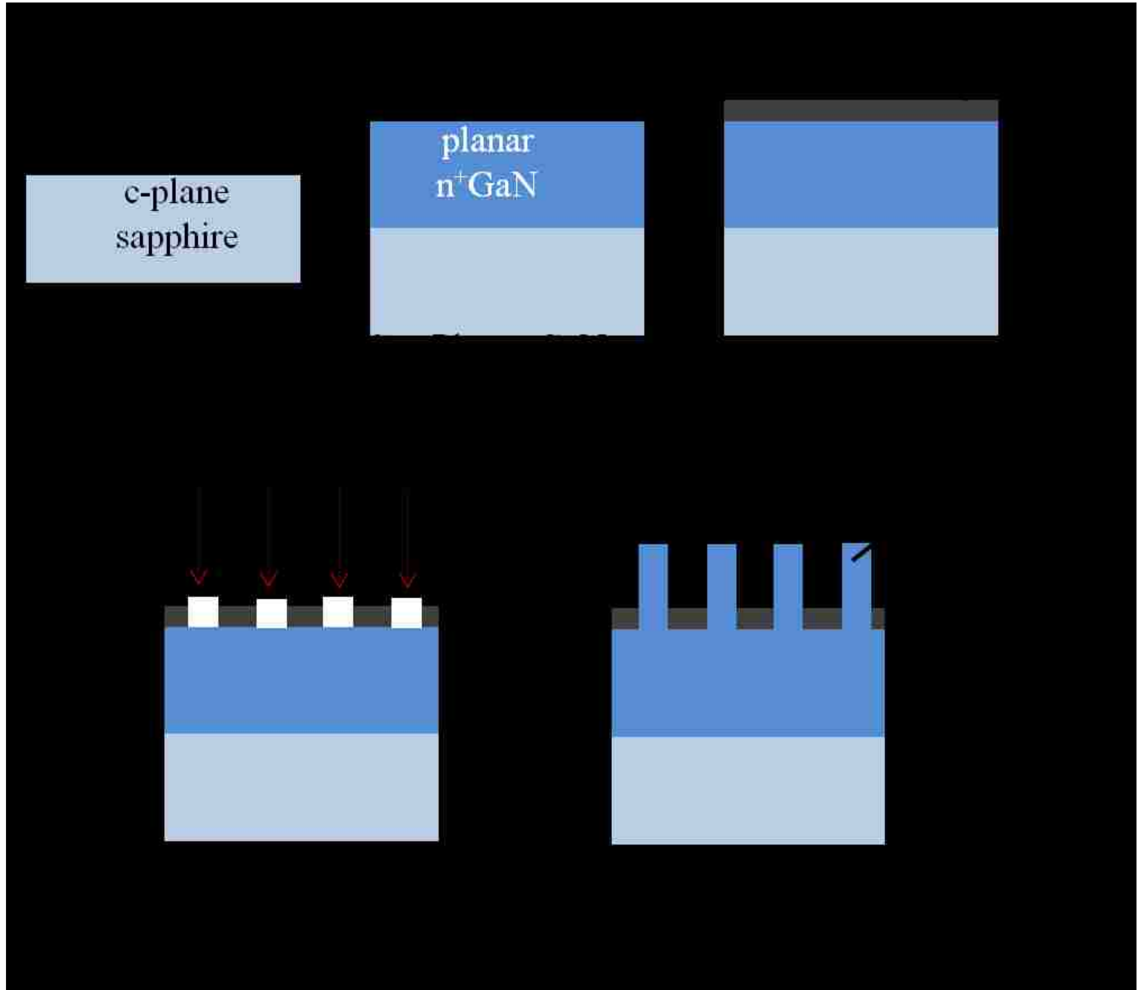

Fig. 4.1 An overview of the various steps involved in the growth of GaN 3D structures using SAG technique without the use of a catalyst.

4.1.1 Growth of planar GaN substrate

The first step is to grow a layer of planar si-doped n^+GaN on sapphire substrate. The reactor that was used to grow all samples is a Veeco TurboDisk, model P75 MOVPE growth system. This reactor is equipped with a in-situ monitoring tool called the RealTemp 200 [4]. The loadlock configuration allows the transfer of the wafer from ambient conditions into the chamber without contamination. The TurboDisk design concept minimizes the parasitic reactions in a couple of ways. One of the reasons is the separation of the gas injection system of group III and V precursors. The other reason is

due to the high-speed rotation of the wafer carrier, which has been shown to draw all the precursors to the wafer before allowing proper mixing. The RealTemp 200 system is equipped with a pyrometer that measures the temperature of the wafer and the absolute reflectivity of the wafer during growth.

The n^+GaN grown on sapphire forms the substrate for the subsequent GaN 3D structures and also the n-contact for the coaxial LEDs discussed in chapter 5. For most of the samples, at least 2μm of planar n^+GaN was grown as the substrate. The planar n^+GaN was grown using metal organic vapor phase epitaxial (MOVPE) growth technique using trimethylgallium and ammonia (NH_3) at a temperature of 1090°C and a pressure of 500torr. The V-III ratio was maintained at around 1300.

The recombination of the bound state between an electron and a hole (excitons) in a direct bandgap semiconductor after excitation leads to the emission of a photon. The measurement of this radiative recombination when done using optical excitation is called photoluminescence (PL). The emitted secondary photons from the material are detected and could be measured using a spectrometer. The spectral dependence of the intensity is then plotted against wavelength to achieve the PL spectrum. In case of direct band gap semiconductors, the most probable transition after the excitation of the electrons corresponds to the energy band gap (E_g). The PL of n^+GaN grown in our reactor is shown in Fig. 4.2. A 325nm He-Cd laser was used as the excitation source for the PL. The sharp PL peak at 3655Å is indicative of good quality GaN (E_g = 3.4eV).

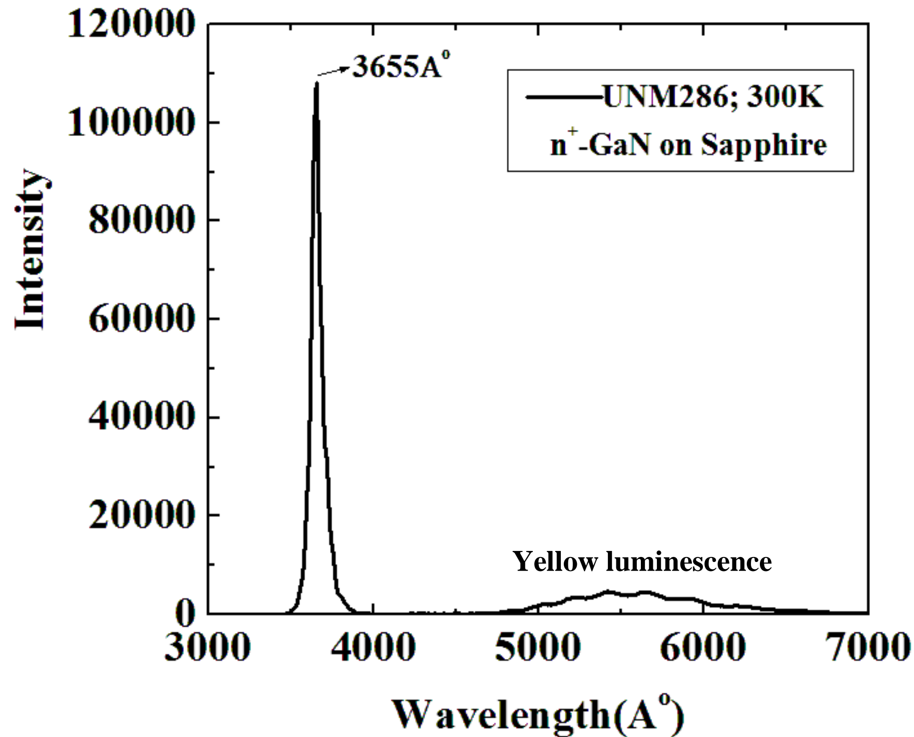

Fig. 4.2 Photoluminescence (PL) spectrum of 2.25µm thick n+GaN (Sample#UNM286) grown on c-plane sapphire is shown. The sharp PL peak is indicative of a good crystalline material. The yellow luminescence indicated is discussed in section 5.2 of chapter 5.

4.1.2 Deposition of dielectric for SAG

After the substrate is grown, a layer of dielectric is deposited ex-situ on the GaN. The dielectric used in this thesis is silicon nitride (SiNx), which was deposited by using plasma enhanced chemical vapor deposition (PECVD) technique. The gases used in the PECVD chamber were silane (SiH_4), ammonia (NH_3) and nitrogen (N_2). The measured flow rates of SiH_4, NH_3 and N_2 were 30, 50 and 15sccm, respectively. The temperature was maintained at 300°C and the pressure was maintained at 600torr. The deposition rate under these conditions was estimated at 12nm/min. The thickness of the SiN_x was measured using an ellipsometer. This measured thickness of dielectric was also consistent with that observed under the SEM after the dry etching of SiN_x that is discussed in section 4.1.4. A SiN_x dielectric thickness of 30nm was used in [2] for the growth of GaN

nanowires. However, section 6.4 of chapter 6 reveals that at least 120nm thick SiN_x was required for the successful functioning of the GaN coaxial LED discussed in this thesis.

PECVD was also used to deposit silicon dioxide (SiO_2) for one of the samples used in section 6.4 of chapter 6 for the composite dielectric. The gases used for the deposition of SiO_2 were 100sccm of nitrous oxide (N_2O) and 20sccm of SiH_4. This deposition was carried out under absence of external heating of the substrate and the pressure was maintained at 600torr. The deposition rate under these conditions was estimated around 15nm/min.

4.1.3 Patterning of dielectric for growth mask

The SiNx was patterned to expose regions on the substrate where GaN can be grown selectively. Interferometric lithography was used to pattern sub-micron diameter hole and sub-micron width line apertures in the SiN_x mask. The process of patterning of circular sub-micron apertures has been illustrated in Fig. 4.3 and the details of the interferometric patterning of SiN_x have been discussed in previous work in our group [5].

To pattern circular apertures using interferometric lithography, two interference UV exposures were required, as discussed in [5]. However, for the patterning of one-dimensional wall patterns, only one exposure was required. Fig. 4.4 shows the SEM image of a positive photoresist pattern developed using a single UV interference exposure. Following this, steps 4-7 illustrated in Fig. 4.3 are followed to achieve sub-micron line apertures. In case of the positive photoresist patterns developed by interferometric lithography, pattern reversal, illustrated in steps 4 and 5 of Fig. 4.3 was required to create circular and line aperture templates

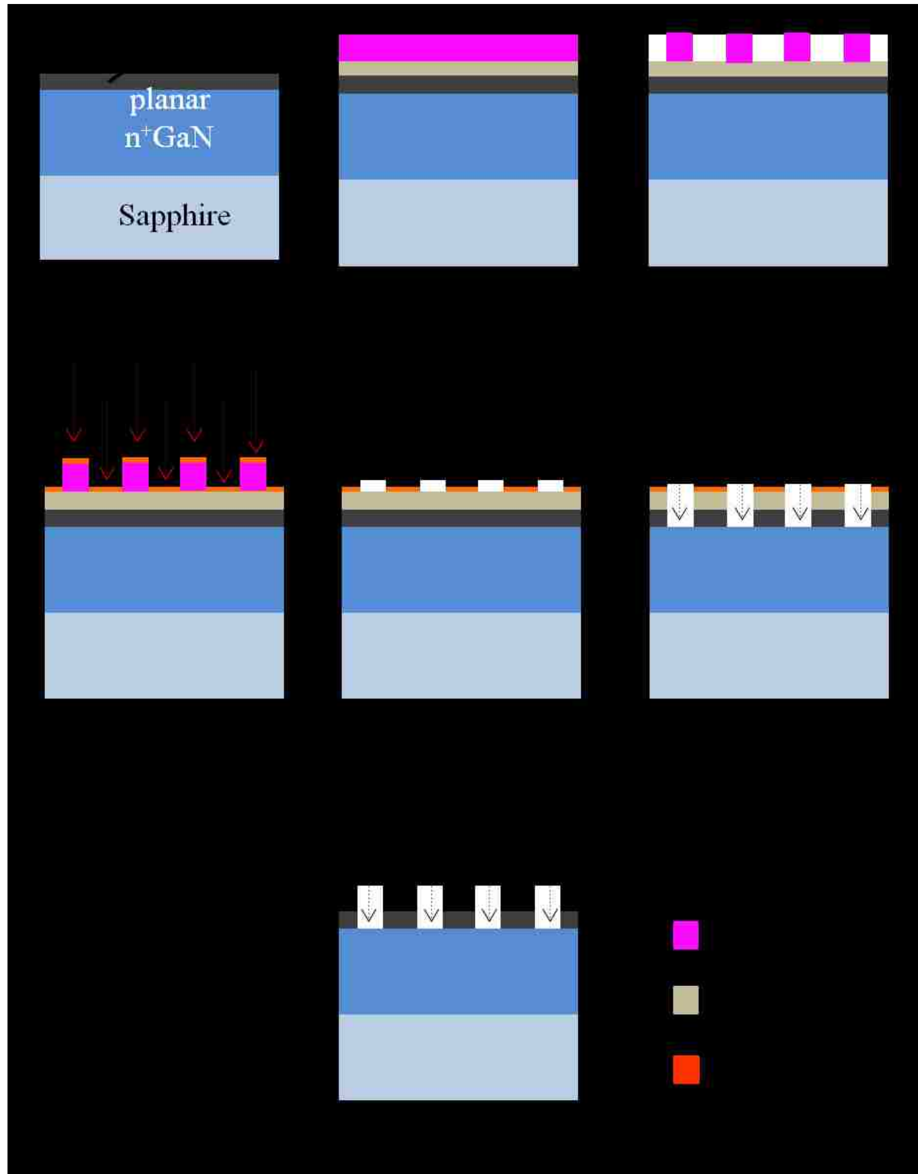

Fig. 4.3 The pictographic illustration of the nanoscale processing involved in patterning of dielectric (SiNx) to define regions to grow GaN nanowires is shown

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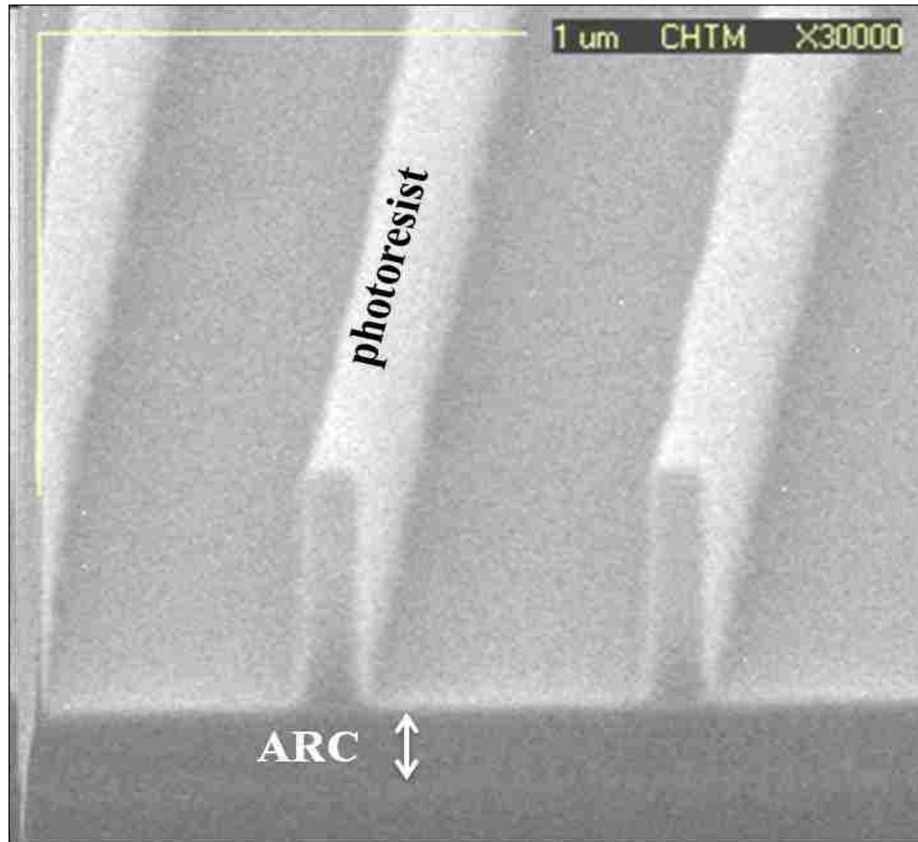


Fig. 4.4 The SEM micrograph of photoresist patterned by a single exposure interferometric lithography is shown.

The circular growth apertures of diameter larger than 1µm and the line growth apertures of line width 1µm or higher were patterned using regular mask photolithography technique. The growth mask was designed along with two other masks for the coaxial LED processing, forming a set of masks called COLED. The COLED growth mask (mask1) is figuratively illustrated in Fig. 4.5. The growth mask is a dark field mask, which has clear regions at the locations marked either as white circles or rounded rectangles. The hole and line growth patterns are varied alternatively along a given row. Each hole in the 10 by 10 array of hole aperture patterns on mask 1 are separated from their nearest neighbor by a pitch of 25µm. The diameter of each of the circular apertures in a given 10 by 10 array of circular patterns is the same. The diameter

is varied as 1.5μm, 2μm, 5μm and 10μm across different patterns along the mask. Similarly, the array of 10 line apertures in a given growth pattern have the same line width. The line width is varied as 1μm, 2μm, 5μm and 10μm across different growth line patterns across the mask.

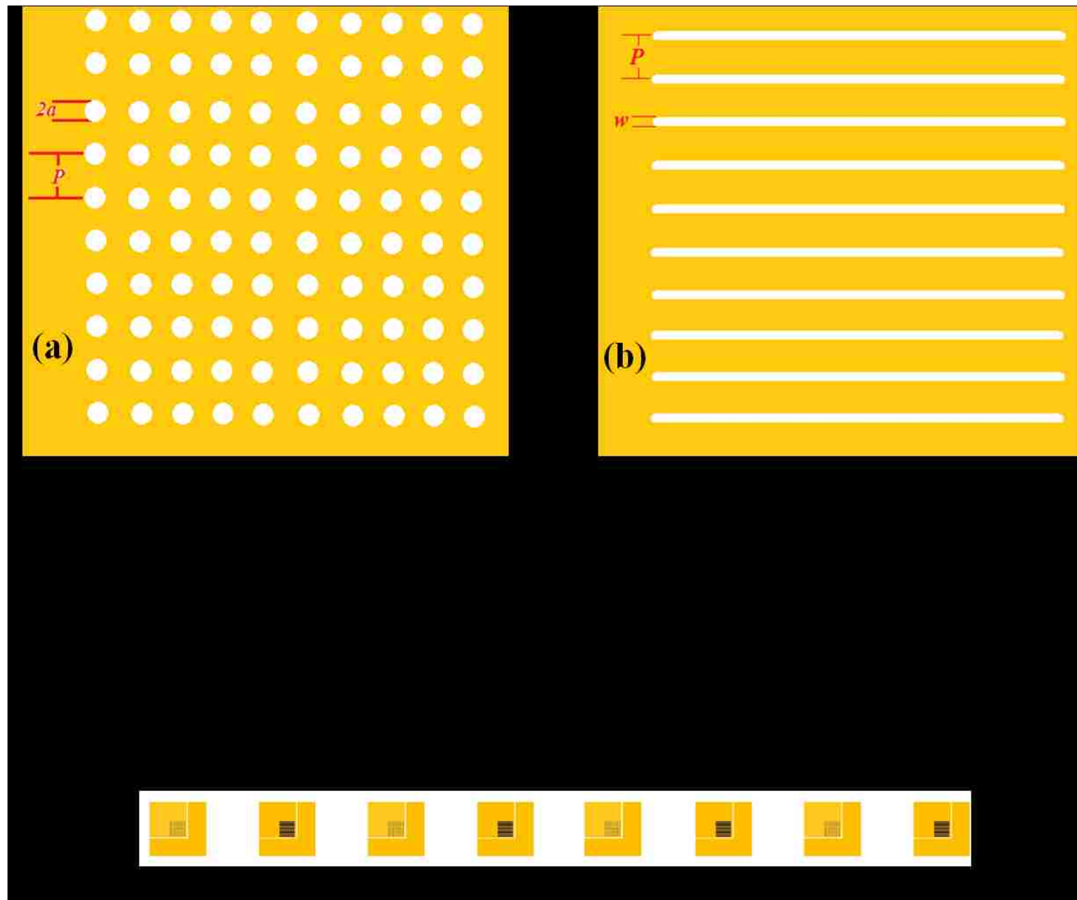


Fig. 4.5 COLED growth mask is pictographically illustrated with the circular and line aperture patterns. The vertical row of different sized LEDs is shown in (c).

It is illustrated in section 6.5 of chapter 6 as to why a hexagonal growth aperture is better than a circular growth aperture. Thus, a variation to the mask 1 was developed, in which the bigger circular growth aperture patterns were replaced by hexagonal patterns. The wider line patterns were also replaced with line apertures that had a hexagonal end. Along with these changes, some hexagonal annulus patterns were

introduced in place of some of the circular and line aperture groups, as shown in Fig. 4.6. The importance of annulus patterns was already illustrated in section 3.3.2 of chapter 3. The mask 2 and mask 3 of COLED are discussed in chapter 6.

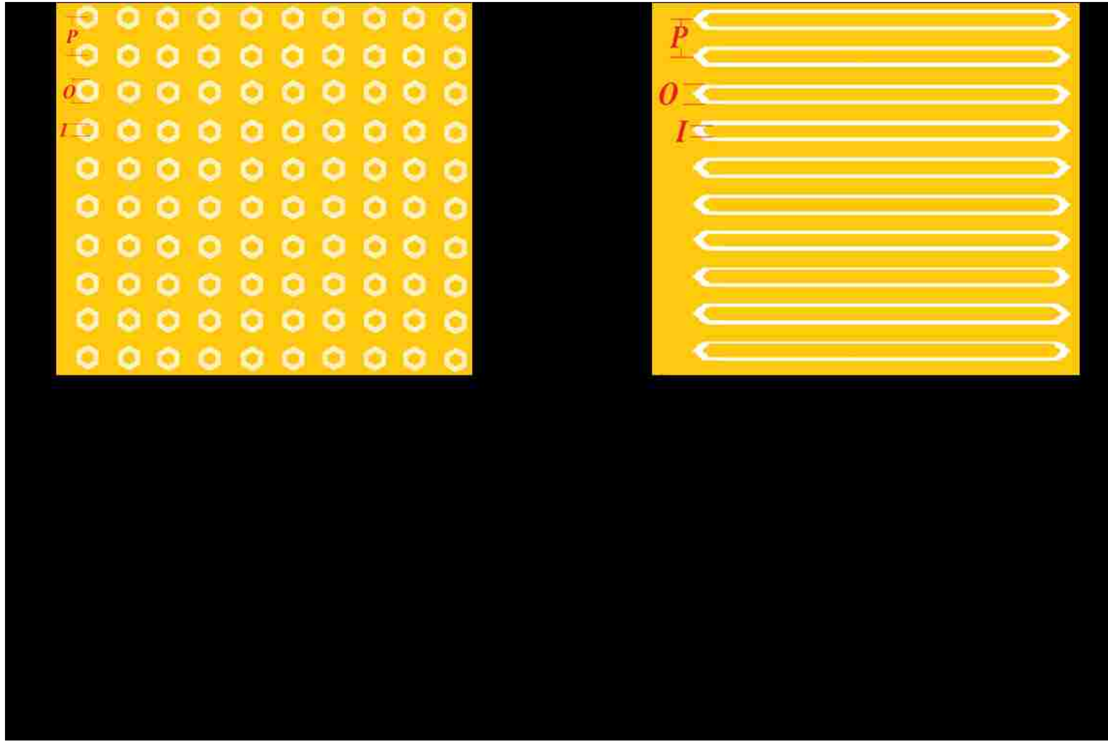


Fig. 4.6 The hexagonal and line annulus patterns in the COLED growth mask is pictographically illustrated

The growth mask patterning was carried out on the whole 2-inch sapphire wafers that had a 2μm thick layer of planar n^+GaN and a thin SiN_x dielectric layer on them. These wafers were cleaned using acetone, following which the wafers were immersed in iso-propyl alcohol (IPA) and the contents were placed in an ultrasonic bath for 5 min for rinsing. After this, each of the wafers was blown dry to prepare for photolithography. The photolithography process is illustrated in Fig. 4.7.

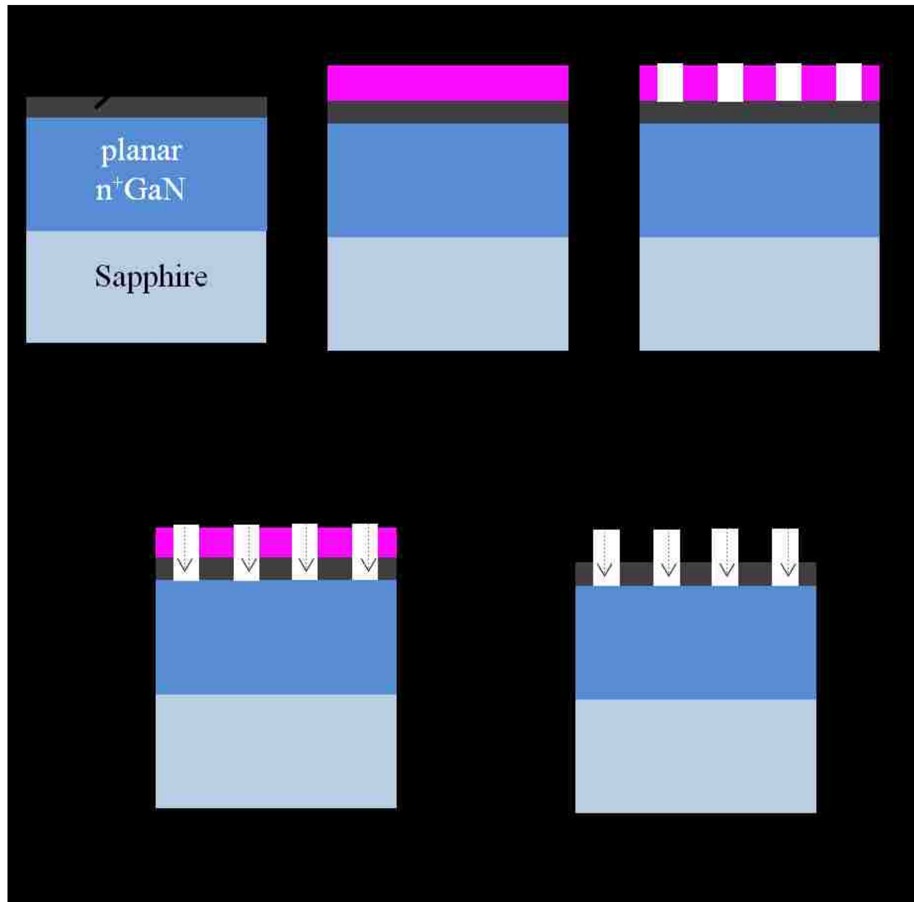


Fig. 4.7 The pictographic illustration of the regular photolithography patterning of the growth dielectric (SiN_x) using COLED growth mask

The photoresist used for the growth mask patterning is a low viscos AZ5206-E. Owing to the growth mask having 1μm features, a thin positive photoresist like 5206 was preferred. A layer of hexamethyldisilazane (HMDS) was first spun on the wafer to promote better adhesion of the photoresist. The wafer was placed on the spinner and a few drops of HMDS were poured on the wafer. The vacuum was engaged to keep the wafer in contact with the chuck and the wafer was spun at an angular speed of 4000 rotations per minute (rpm) for 30sec. Following this, the wafer was removed from the chuck and placed on a hot plate, preheated to 112°C for a minute.

After this, the wafer was placed back on the chuck of the spinner and some amount of photoresist was poured on it. The photoresist was then spin coated on the wafer after engaging the vacuum on the chuck. The wafer was spun at an angular speed of 4000rpm again for 30sec. Under these conditions, the optimal thickness of the photoresist was estimated around 520nm. Following this, a soft bake of the wafer was carried out in a furnace set at 95°C for about 2min, prior to the exposure.

After the spin-coat process, the wafer was ready for the photolithography exposure. The mask aligner used for the photolithography was a Karl Suss MJB-3. The COLED growth mask (mask 1) was first cleaned with IPA and blown dry, prior to usage. The mask holder in the aligner was placed face up with the vacuum grove visible and the mask1 was loaded with the mask side facing upwards. The mask was kept in contact with the holder by establishing a vacuum between the holder and the mask. After this, the holder was loaded in the aligner to get ready for the UV exposure.

The alignment of the growth mask with the wafer underneath is critical to the growth of the 3D GaN structures. The 2-inch circular sapphire wafer usually comes with a flat on one of the sides indicating the $<11\bar{2}0>$ a-direction of sapphire. The epitaxial relationship between GaN and sapphire has already been discussed in chapter 1. Thus, the $\{1\bar{1}00\}$ m-plane of GaN would be aligned with the $\{11\bar{2}0\}$ a-plane of sapphire. Hence, the line patterns on the mask were aligned parallel to the flat of the sapphire to grow microstructured walls with m-plane GaN sidewalls.

Once the alignment is achieved, the sample was exposed to ultraviolet light under constant power conditions. A 5sec exposure at a constant power of 350mW was determined to be optimal exposure condition for the lithography under most ambient

conditions. After the exposure, the wafer was immersed in a developer to let the photoresist develop. AZ400K was the developer used, which was diluted with water to control the developing time. AZ400K diluted with 4 parts of water (1:4) was used but not preferred because the developing time was around 15sec, which was difficult to control in comparison to the 80-90 sec developing time with the 1:6 developer solution. There was no pattern reversal required in the regular photolithography of circular and line aperture templates.

4.1.4 Reactive ion etching of growth dielectric

After the patterning of the photoresist, the SiN_x is etched in the open apertures in the photoresist. Reactive ion etching (RIE) is a dry, anisotropic etching process, capable of producing vertical etch-profiles. RIE is less sensitive to temperature and produces more repeatable etch profiles, thereby it is able to maintain the size and shape of features during pattern transfer.

RIE involves ion-assisted chemical etching of dielectric films. Carbon tetrafluoride (CF_4) has been used to etch SiN_x using our RIE system. This high-energy fluoride (F^-) ion based plasma assisted etching of SiN_x in the chamber is commonly done in the presence of oxygen gas to improve the etch rate of SiN_x. The introduction of a little bit of oxygen gas to the chamber during the etching of SiN_x has been shown [6] to improve the concentration of F^- ions in the chamber atmosphere. The gas pressure was maintained at 25mtorr during the etching of the SiN_x. The CF_4 and oxygen flows were 30sccm and 3sccm respectively. The plasma power used was 80W, which led to a DC bias voltage of around 250V. Under these conditions, the etch rate of SiNx achieved was around 50nm/min. In cases where an anti-reflection coating (ARC) was used, a simple

oxygen plasma was used to etch the ARC. Fig. 4.8 shows SEM images of portions of SiNx etched in the RIE. After the etching process, the wafers were cleaned in piranha (1 part hydrogen peroxide: 4 parts sulfuric acid) to remove the photoresist and metal mask layers as illustrated in step 7 of Fig. 4.3.

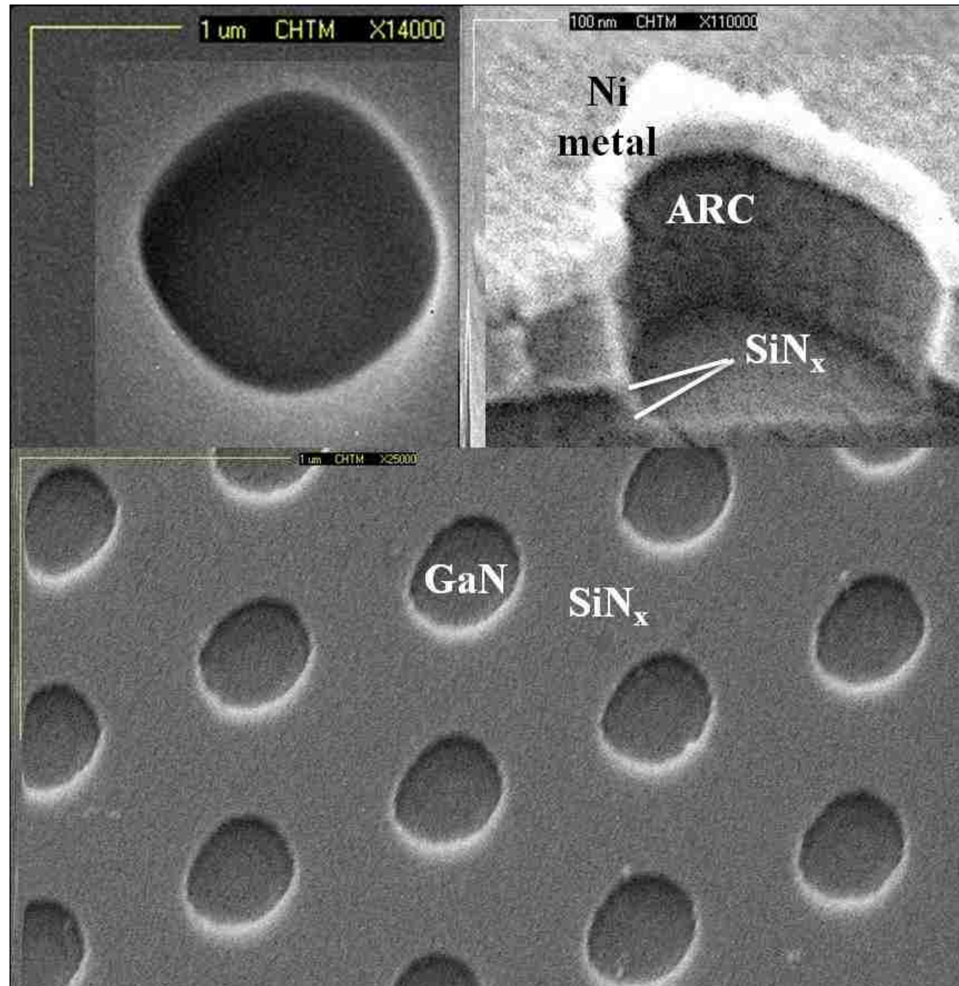


Fig. 4.8 The SEM images of growth dielectric (SiNx) etched using the RIE

4.1.5 Pulsed MOVPE selective area growth of GaN

After the patterning of the dielectric for the selective area growth, GaN is grown in the apertures using pulsed metal organic vapor phase epitaxial (MOVPE) growth technique. The process was first demonstrated for growing GaN nanowires previously in our group [2], but has been extended to grow nanowall structures (as shown in section 1.2.3 of chapter 1 and Fig. 4.12 of chapter 4) and microstructures in this thesis.

Firstly, the wafers were subjected to a high temperature *in-situ* cleaning in hydrogen ambient prior to the MOVPE growth of GaN. This *in-situ* cleaning of the sample was done at 680°C and under a chamber pressure of 100torr. After this, a thin layer of GaN was grown in the apertures to initiate the 3D growth of GaN. This is termed as the nucleation layer. It was shown in [2] that a nucleation GaN layer was necessary to achieve good fill factor in the circular nanowire growth apertures. Trimethyl gallium (TMG) was used as the group III growth precursor, while ammonia (NH_3) was used as the group V precursor. The V-III ratio used in the gas phase was similar to the conditions used for the planar n^+GaN substrate that was discussed in section 4.1.1. The nucleation growth was found to be critical for the initiation of the nanowire growth [7]. Fig. 4.9 shows four different nucleation growths that were done to determine the ideal nucleation conditions. The V-III ratio in the gas phase was maintained the same in the four samples analyzed. Pyramidal shaped nucleation structures were observed for the samples grown at 1090°C and under a chamber pressure of 500torr (Fig. 4.9(b) and (c)). It was shown in [7] that nanowire growth could not be initiated if the nucleation structures were completely bound by the pyramidal stable $\{1\bar{1}01\}$ facets. Hence, it was also concluded that the transition from the nucleation growth to nanowire growth mode would be ideal if the

nucleation was confined within the growth template. It was also shown in [2] that the nanowires had the same diameter as the growth mask apertures under this confined growth conditions. Hence, the nucleation layer grown at a temperature of 970°C and under a chamber pressure of 100torr was considered as the optimum to initiate the pulsed MOVPE growth.

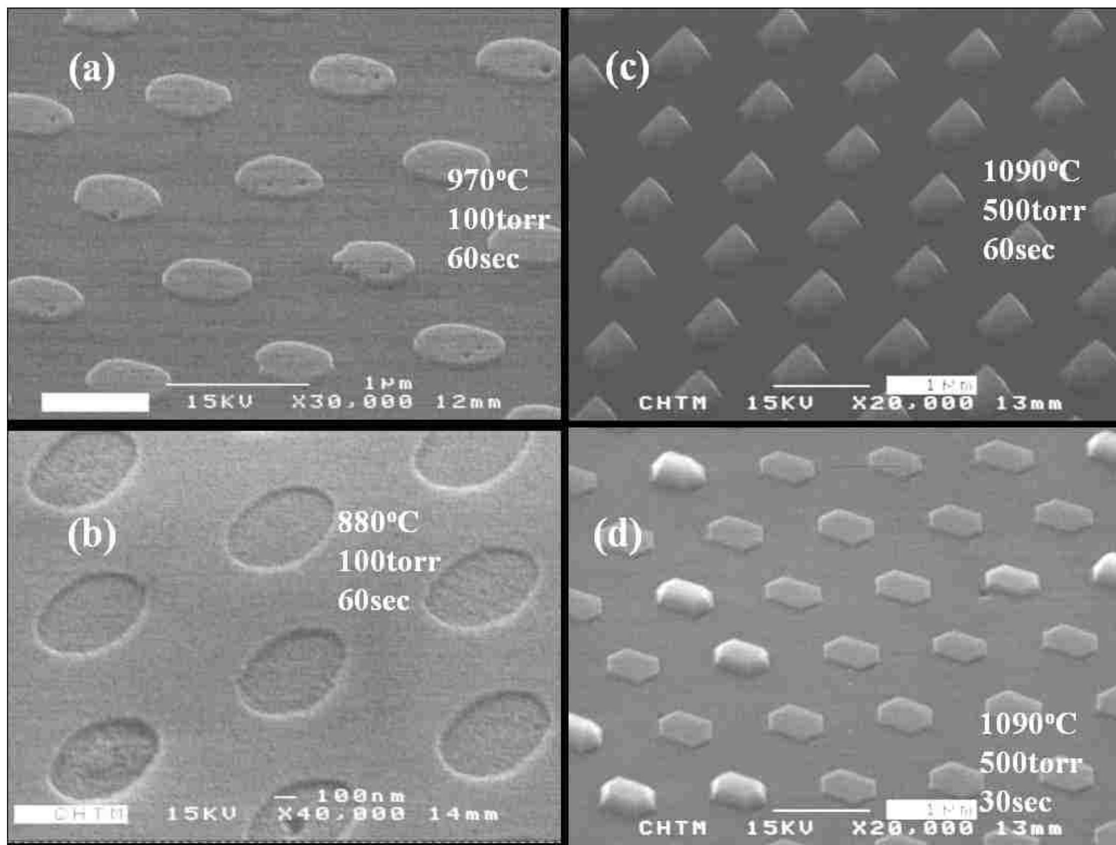


Fig. 4.9 The SEM images of nucleation growths performed at varied temperature, pressure and time are shown. (a) seems to be the most optimal condition to start the nanowire growth.

After the nucleation growth, the growth mode was switched to pulsed MOVPE growth. The growth precursors were not introduced continuously throughout the growth, instead were introduced alternatively for short durations of time, as illustrated graphically in Fig. 4.10.

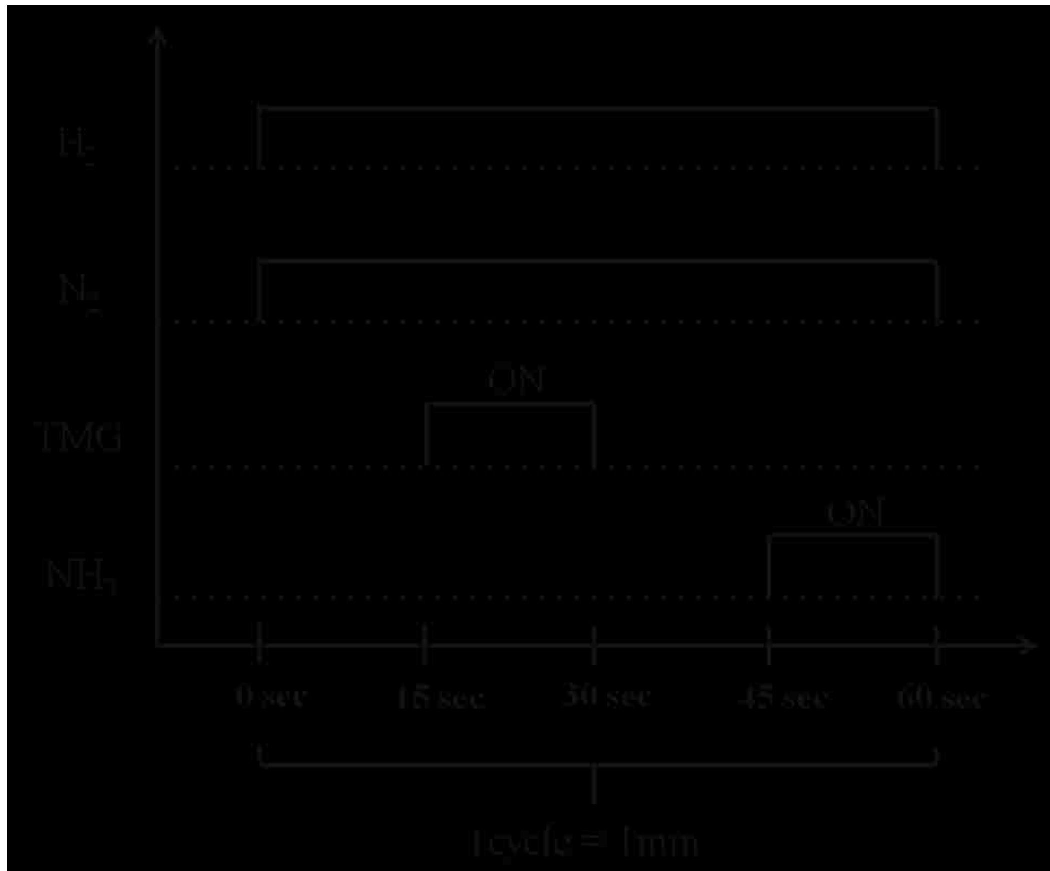


Fig. 4.10 A pictographic illustration of a cycle of the pulsed MOVPE growth of GaN

It was concluded in [2] that a low V-III ratio was needed to grow GaN nanowires on the patterned substrates. Thus, a V-III ratio of 550 was used during the pulsed growth, which was at least 2 to 3 times lower than the ratio that was used for regular planar GaN growth. A cycle is defined as the one-minute period illustrated in this Fig. 4.10. In the first and third 15sec period of the cycle, the carrier gases were flowing to maintain the chamber pressure, while the growth precursors were turned off. In the remaining 15second periods of the cycle, the growth precursors were allowed to flow alternatively. The growth temperature across the 3D GaN growth was kept constant at 970°C and the chamber pressure was maintained at 100torr. The 3D GaN structures were grown n-doped by flowing silane (SiH_4) along with TMG. Fig. 4.11 shows the SEM images of

GaN nanowires grown by pulsed growth. The <0001> direction growth rate of the nanowires was observed to be much greater than the lateral <1$\bar{1}$00> direction growth rate. Hence, the original SiNx aperture diameter was almost perfectly replicated by the nanowires grown for 150 cycles shown in Fig. 4.11.

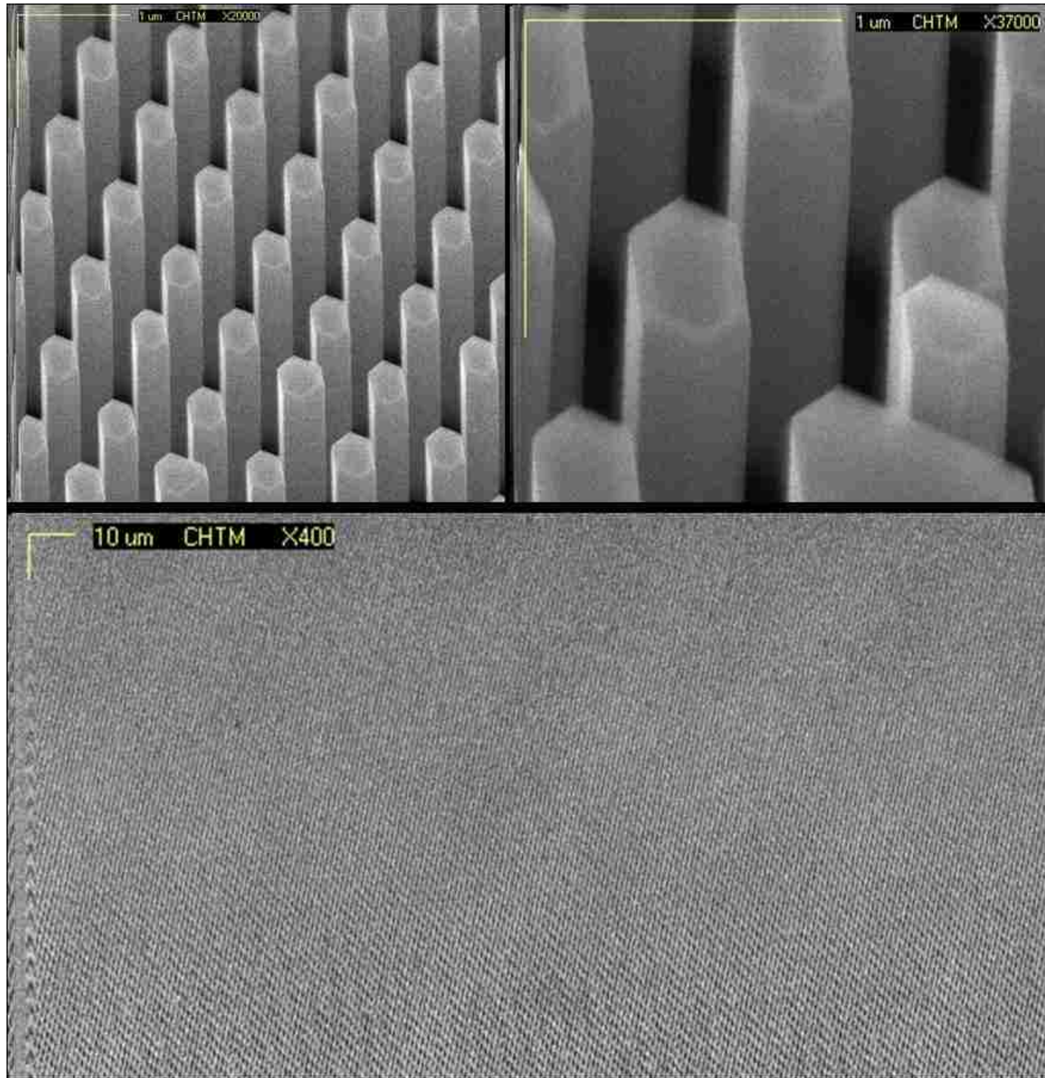


Fig. 4.11 SEM images of GaN nanowires grown for 150 cycles is shown

Fig. 4.12 shows the SEM images of GaN nanowalls grown by pulsed growth. The line apertures have been aligned along the flat of the sapphire wafer that corresponds to

the $<11\bar{2}0>$ direction for sapphire. Thus, the smooth sidewalls of the nanowalls grown corresponded to the $\{1\bar{1}00\}$ m-planes of GaN.

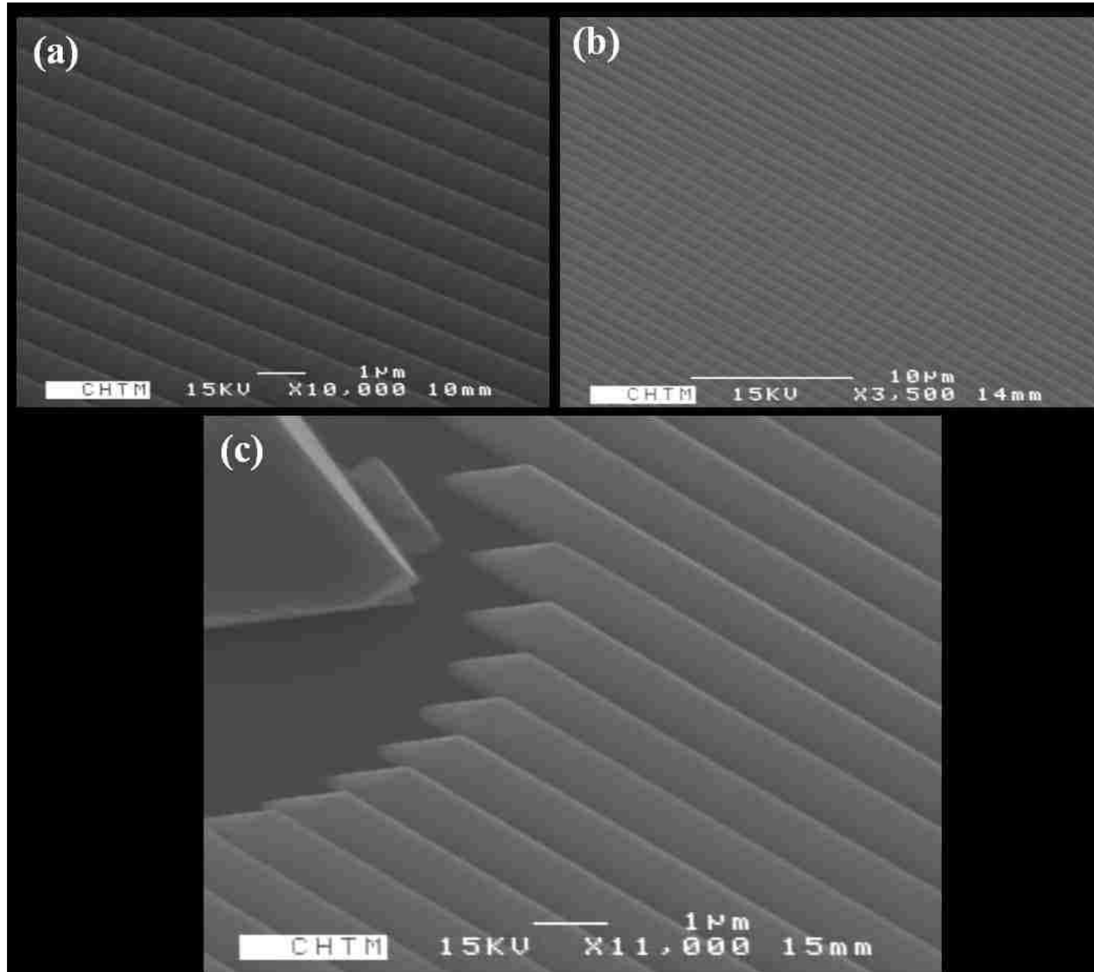


Fig. 4.12 SEM images of GaN nanowalls grown using pulsed MOVPE growth is shown. The line apertures are aligned parallel to the $\{11\bar{2}0\}$ plane of sapphire to produce smooth$\{1\bar{1}00\}$ GaN planes

Fig. 4.13 shows the SEM images of the GaN microstructures (wires and walls) grown under the same conditions. Previous work in our group demonstrated GaN microstructures grown in patterned dielectric [8] that were bound by 6 $\{1\bar{1}01\}$ pyramidal facets. However, the microstructures discussed in this thesis are the first demonstration of

micro-pillars bounded by 6 smooth $\{1\bar{1}00\}$ sidewalls. The wall structures have been aligned to the flat of the sapphire wafer to achieve $\{1\bar{1}00\}$ sidewalls.

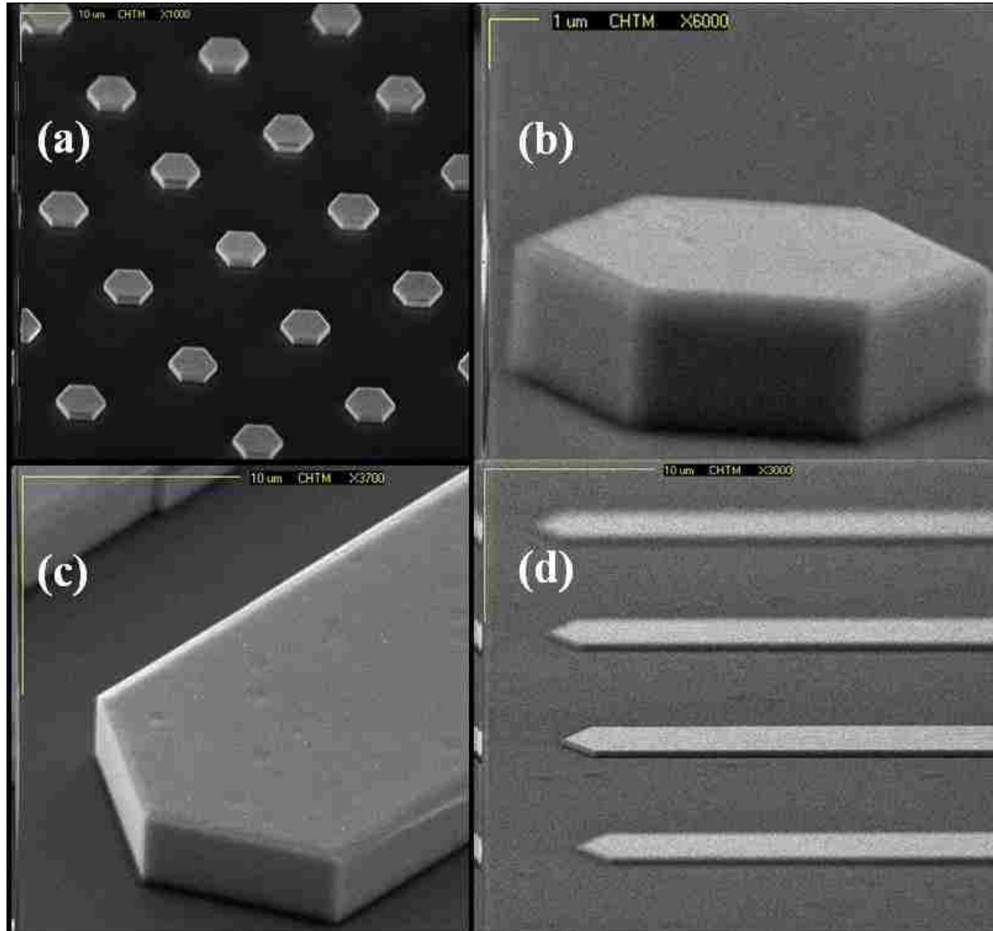


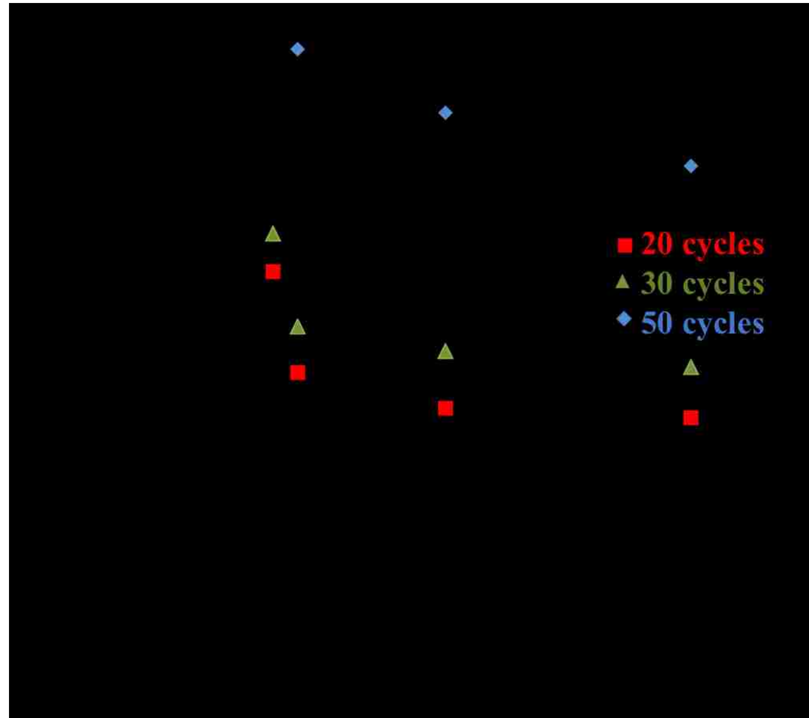
Fig. 4.13 SEM images of GaN microstructures grown by pulsed MOVPE

The micro-wires grown using the COLED growth mask showed a correlation between the height and the diameter of the different sized structures. The microstructures with a smaller diameter were taller than the ones with a larger diameter. Also, there was sufficient increase of lateral diameter of the microstructures in comparison to the diameter of the circular/hexagonal aperture in which they were grown. The analysis of these observations is presented in the following section.

4.2 Understanding the growth of 3D GaN structures: Capture radius calculation

The capture radius ρ is defined as the annulus distance around a given device structure within which the growth nutrients (TMG and NH_3) could be captured to participate in MOVPE of GaN on the already grown structure. The capture radius is anticipated to be a function of growth conditions, but not a function of the microstructure hole diameter.

To calculate the capture radius, three growth samples (NW160, NW161 and NW162) were considered. They were all grown at 970°C using the pulsed growth conditions. The TMG flow (raw/push/dd) for each of the growths was also kept constant all through the microstructure growth at (25/40/30). The ammonia flow rate was maintained at 500sccm. Under these conditions, the V-III ratio was calculated around 550. The pressure was also kept constant at around 100 torr. The number of growth cycles were reduced from 50 for NW160 to 30 for NW161 and subsequently reduced to 20 for NW162. This was done to estimate the growth rate along the vertical <0001> direction and along the lateral <1$\bar{1}$00> direction. The lateral growth parameter (*%Δ*) has been defined as the percentage increase in the diameter of the microstructure with respect to the original circular aperture diameter (*2a*). Fig. 4.14(a) shows the variation of the height of the microstructures as a function of the aperture diameter, while Fig. 4.14(b) shows the variation of the lateral growth parameter as a function of the aperture diameter. Fig. 4.15(a) presents a pictographic illustration of the capture radius defined in this thesis.



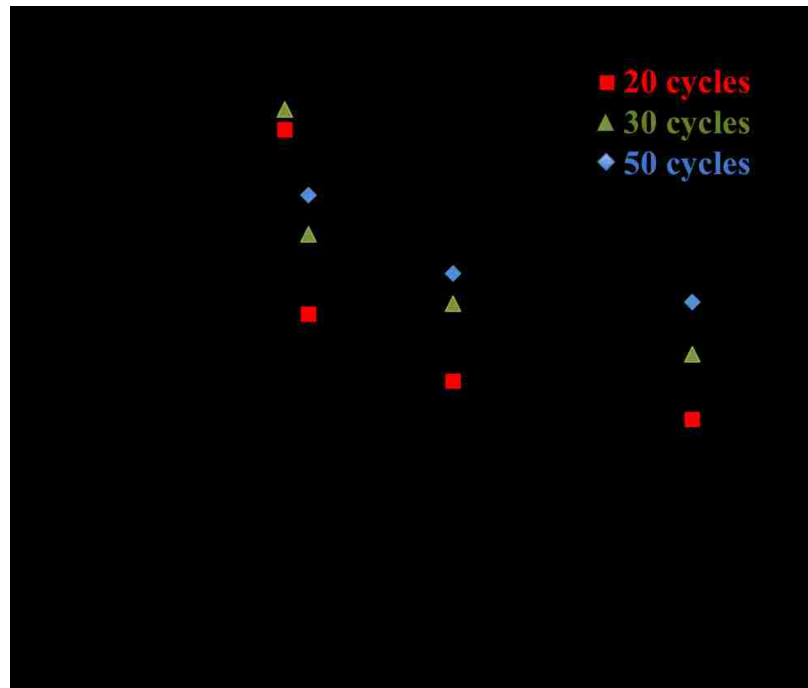


Fig. 4.14 (a) shows plot of the variation of the height *h* of the microstructures and (b) shows the plot of the lateral growth parameter (*%Δ*) vs. the aperture diameter (*2a*).

Reduction in the height and the diameter of the corresponding microstructures were observed in Fig. 4.14 as the growth duration was reduced from the NW160 (50 cycles) to NW162 (20 cycles). The height of the microstructures in the same sample is also observed to reduce with the increase in the aperture diameter. The vertical growth rate dominates over the lateral growth rate indicative of the pulsed growth mechanism proposed earlier in [7]. The observations corresponding to the lateral growth parameter in Fig. 4.14(b) suggest that the smaller aperture growth structures (1.5µm and 2µm) show a bigger increase in diameter as compared to the larger microstructures (5µm and 10µm).

The capture radius ρ shown in Fig. 4.15 is indicative of the boundary layer across a given growth structure. Once the growth nutrients (TMG and NH_3) fall within the capture annulus described by Fig. 4.15(a), they can be assimilated by the structure and contribute to the growth. The volume grown would be proportional to this capture area. The SEM micrographs of the three samples grown are shown in Fig. 4.16, 4.17 and 4.18.

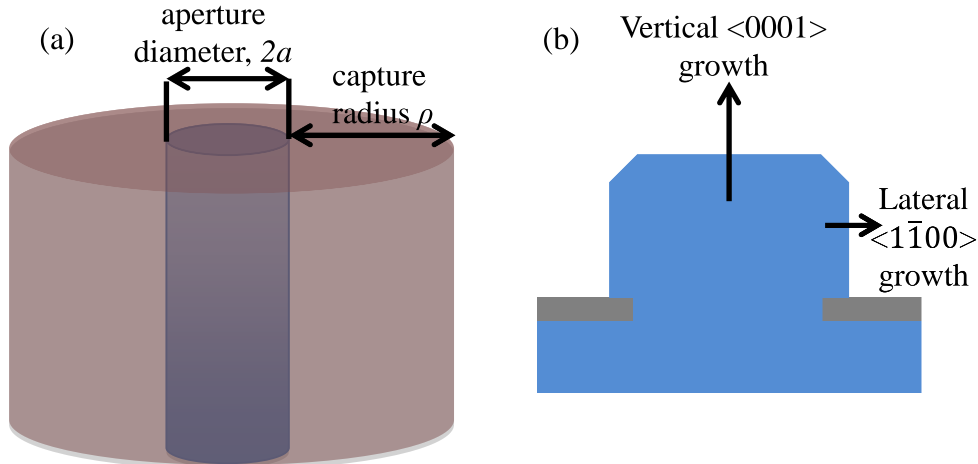


Fig. 4.15 (a) shows the capture radius, ρ as defined in this section; growth nutrients falling in the cylindrical area would contribute to the vertical <0001> growth and lateral $< 1\bar{1}00 >$growth

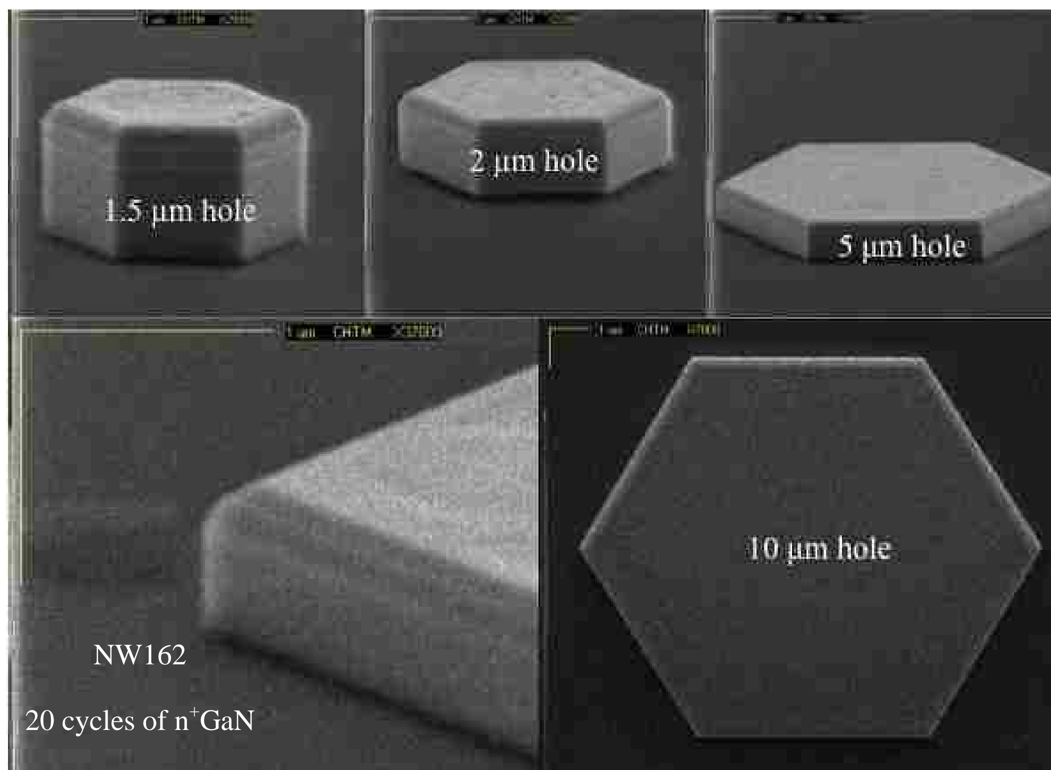


Fig. 4.16 SEM images of different size microstructure in NW162

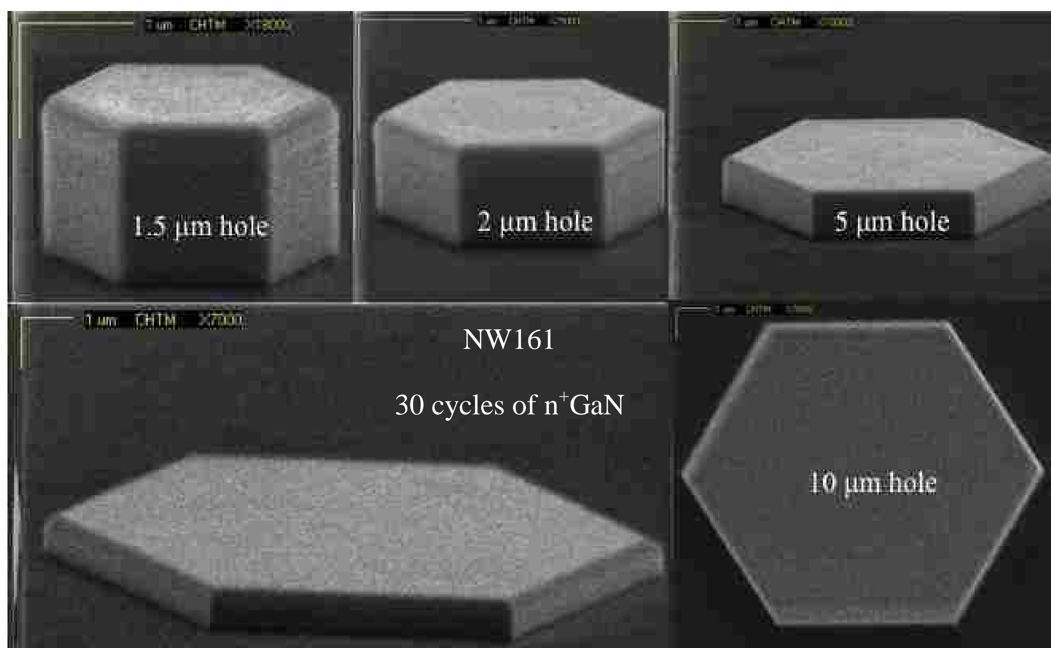


Fig. 4.17 SEM images of different size microstructures in NW161

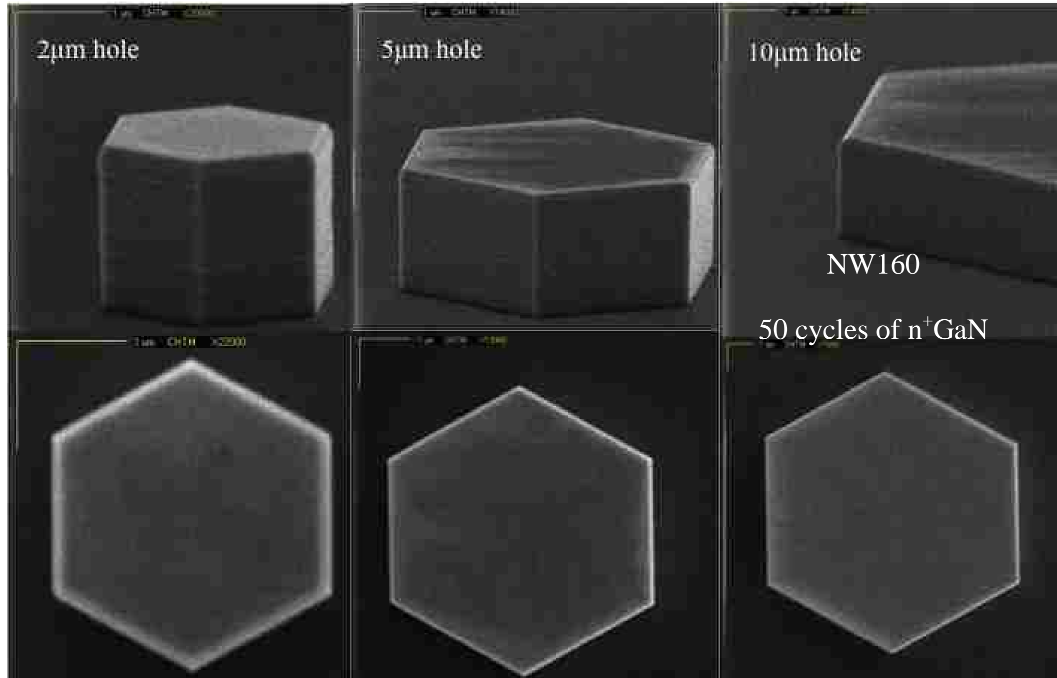


Fig. 4.18 SEM images of different size microstructures in NW160

The SEM micrographs show GaN wires with hexagonal cross-section emerging from the respective openings mentioned in Fig. 4.16, 4.17 and 4.18. The volume of the microstructures were calculated using the relationship mentioned below

$$V = Area\ of\ base\ \times\ Height$$

As discussed earlier, it is possible to relate the total volume of the structure to the surface area within the capture radius as below: -

$$V_{structure} \propto\ A_{capture}$$

$$V = Constant\ \times\ \pi(a+\rho)^2$$

The largest structures (corresponding to the 10μm holes) were considered as reference points to calculate the constant in the above equation for each of the samples. Curves are plotted for different values of capture radii, along with the actual volume of the structures to estimate the capture radius. Fig. 4.19 shows the plot of volume of the structures, *V* as a function of the aperture diameter (*2a*) for the three samples. The capture

radius value of around 0.25μm fits almost perfectly for all the device structures in the three growths as shown in Fig. 4.19. This proves that for given growth conditions, the capture radius is independent of the size of the initial aperture diameter.

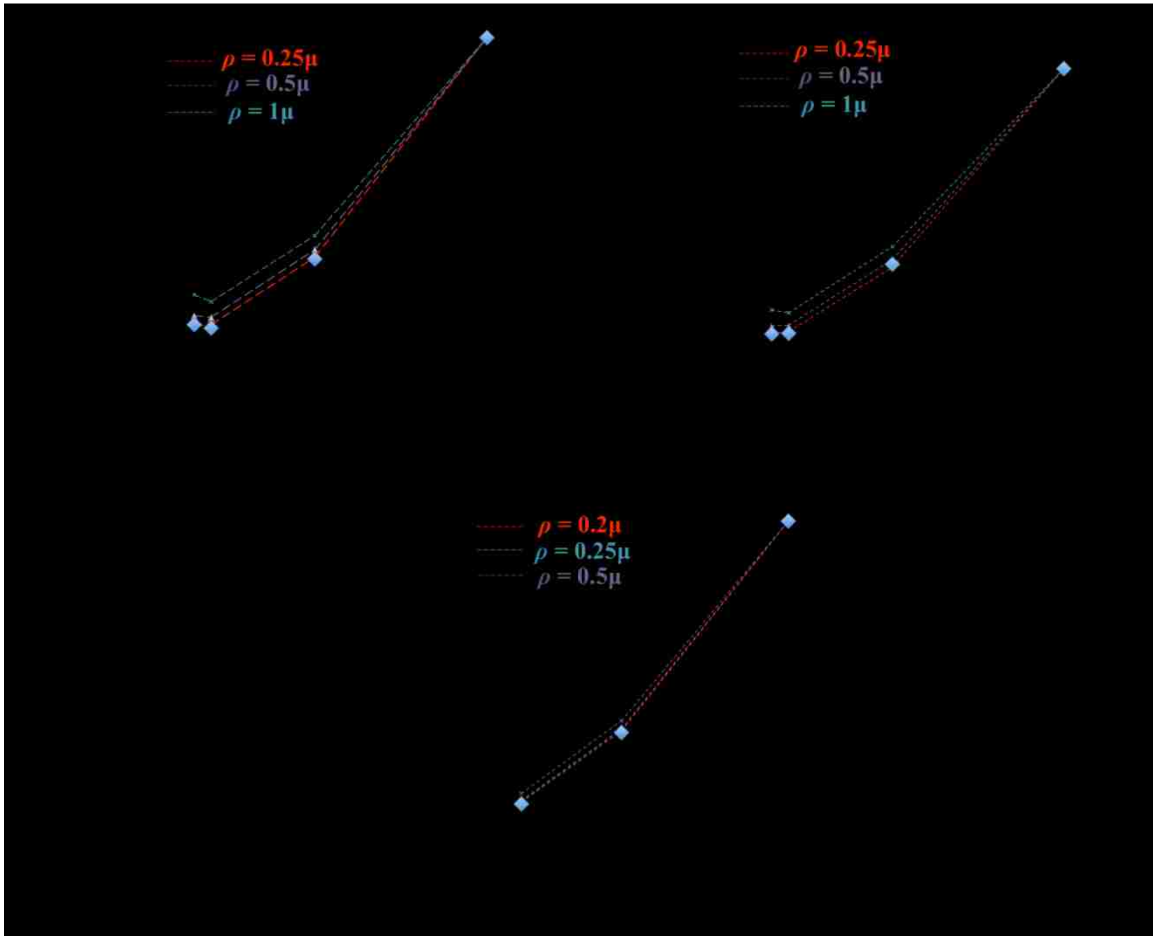


Fig. 4.19 The growth volume (*V*) of each of the structure is plotted as a function of the original aperture diameter (*2a*) for different values of capture radii and the actual volume data is represented by ♦

4.3 Understanding growth of GaN in annulus patterns

In the previous sections, 3D GaN grown in continuous circular and line apertures were presented and analyzed. In this section, 3D GaN grown in growth apertures shaped as annuli is discussed. The annulus growth apertures present us with a unique opportunity to grow large threading defect (TD) free GaN structures. It was discussed in chapter 3 that a TD in GaN bends and terminates at a $\{1\bar{1}00\}$ sidewall in close proximity to it. Thus, GaN grown in large annulus apertures, as the one shown in Fig. 4.20 could still be defect free, at the same time, present a large active region area to grow high power, TD free, LEDs.

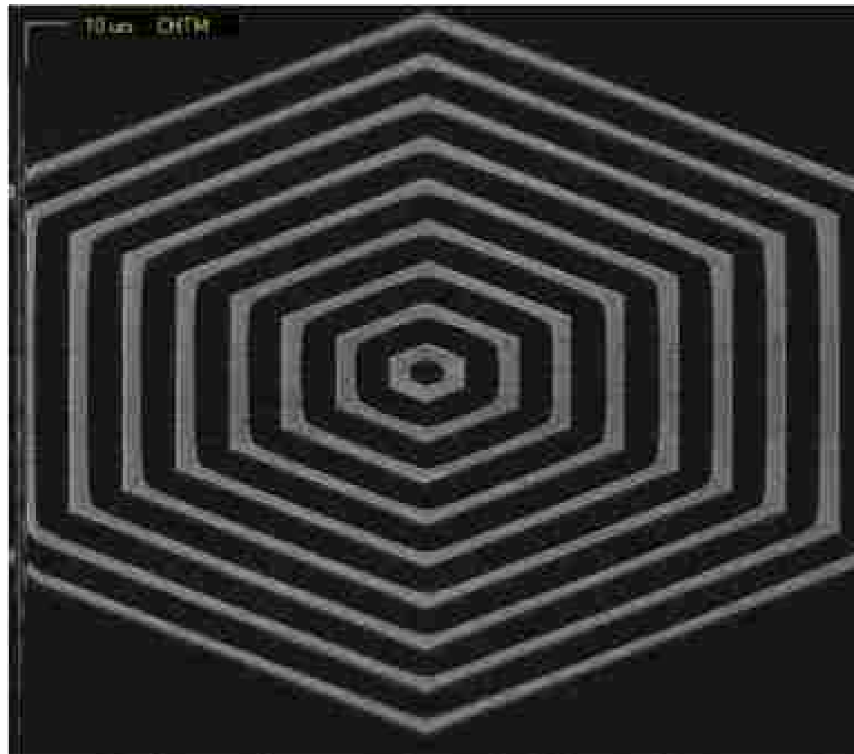


Fig. 4.20 SEM image of a multi-hexagonal annulus pattern is shown. These structures could potentially be threading defect free, but also present us with a large active area, thus leading to a high power threading defect free LED.

The patterning of the annulus type growth apertures was similar to that of the 3D GaN microstructures using regular mask photolithography. Pattern collapse was problematic and hence the developing time was critical to the annulus structures. Fig. 4.21 shows the optical microscope images of annulus patterns etched in the growth dielectric, SiN_x.

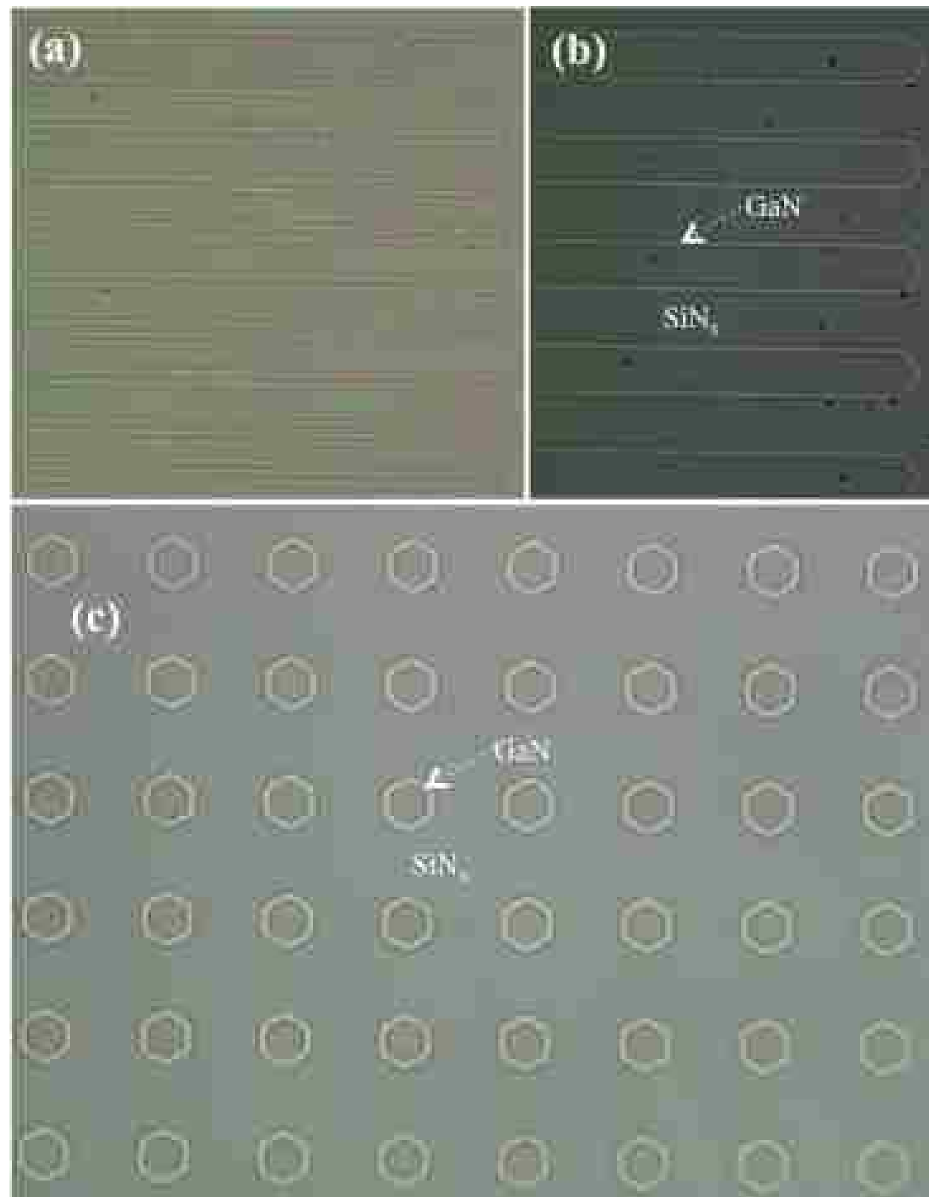


Fig. 4.21 Optical microscope images of annulus patterns etched in growth dielectric (SiNx)

3D GaN structures were grown in these annulus apertures using the same growth conditions used for growing the microstructured GaN wires and walls. Fig. 4.22 shows the SEM images of the GaN grown in hexagonal annulus patterns. The vertical <0001> growth rate of the annulus structures was observed to be greater than the outer <$1\bar{1}00$> lateral growth rate. However, the growth rate of the inner sidewalls (marked in the Fig. 4.22(a)) was higher than the outer sidewalls, once again indicative of the growth nutrients within the capture radius being captured by the growing structure. In addition to this, the inner walls growth seemed to be less controlled in comparison to the growth of the outer walls. In some cases, additional crystallographic orientations were observed to be emerging, in between the two $\{1\bar{1}00\}$ planes, as shown in Fig. 4.22(c). Leung *et al.* [9] have also observed the additional planes arising between the $\{10\bar{1}1\}$ pyramidal sidewall facets during coalescence and have concluded it to be the slow growing $\{11\bar{2}2\}$ facets. Coltrin *et al.* [10] have demonstrated that for concave growth inside the annulus features, the fast growing $(11\bar{2}2)$ faces are dominantly observed, opposite to the situation outside the annulus feature where the faster growing faces grow to disappear leaving behind the slow growing facets. They utilized the Wulff construction, a polar plot of the facet-orientation dependent growth rate, to study the different crystallographic orientations and their growth rate under similar growth conditions. In the case of the 3D structures grown in this thesis, it was not very clear as to what orientation was favored. The higher growth rate of the concave sidewalls, led to the formation of multiple crystallographic orientations, as shown in Fig. 4.22(c).

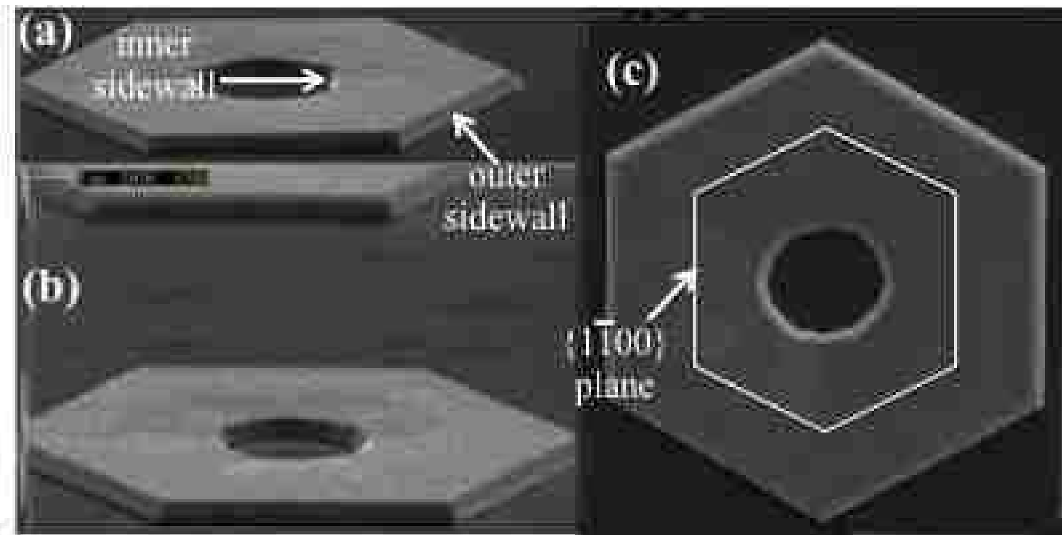


Fig. 4.22 SEM images of GaN grown in hexagonal annulus apertures are shown. (c) shows the origin of new crystallographic planes in the inner concave side of the annulus structures.

The selective area 3D GaN microstructures grown in the annulus patterns also revealed a very important observation. Fig. 4.23(a) shows the SEM image of a group of annulus wall 3D GaN microstructures grown under the same growth conditions as specified earlier in the section for 20cycles (NW162). The 3D GaN annuli are uniform on the outside (convex side), but is tapered from the starting of a given line pattern towards its center in the inside (concave side). Fig. 4.23(b) shows the SEM image of a group of hexagonal annulus 3D GaN microstructures grown under the same growth conditions for 30cycles (NW161). It is noticeable that the annulus structures inside the group still have a void inside, while the structures on the boundary of the group have coalesced internally. This indicates that the growth rate of the structures on the edge of a given group pattern is much greater than the growth rate of the structures that are not on the edge. Hence, the capture radius is anticipated to be greater for those structures that are on the edge of a given group pattern.

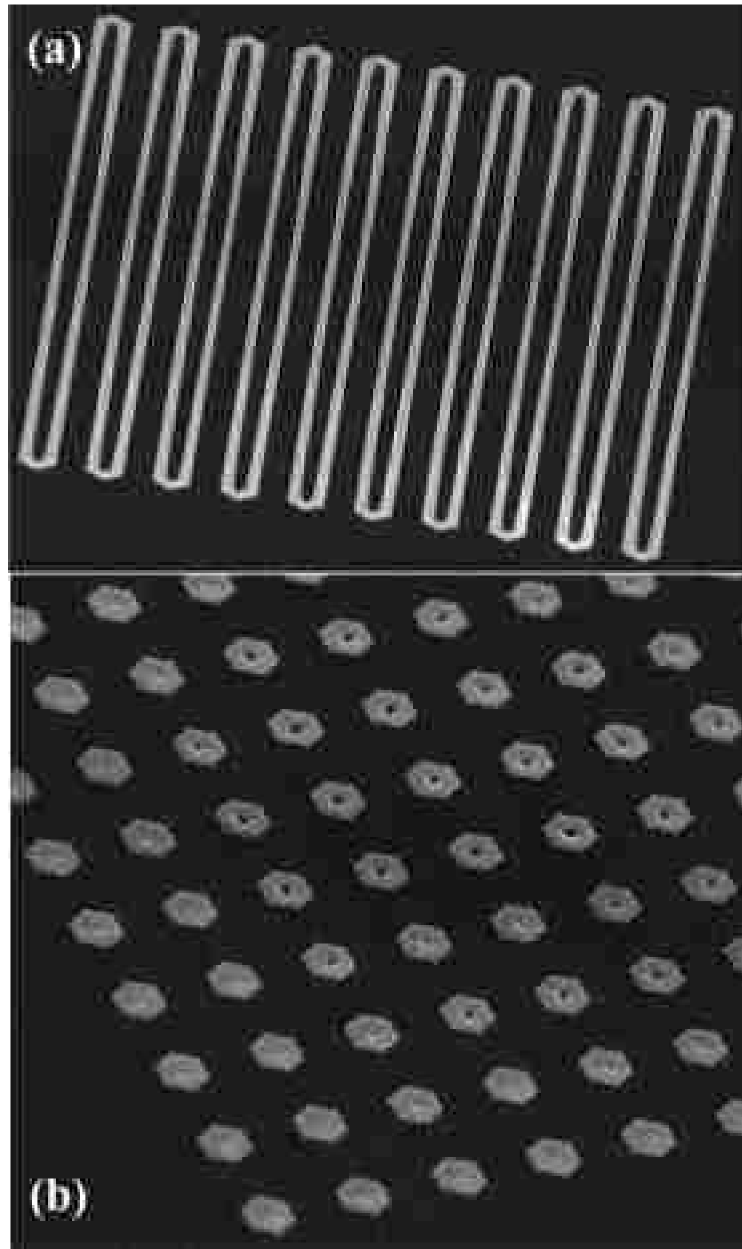


Fig. 4.23 SEM images of GaN grown in (a) annulus line apertures and (b) hexagonal annulus apertures is shown, indication of the difference in growth rate in the structures on the edge of a given group and those near the center.

4.4 Growth of GaN nanowires in selective area nanowire growth (SANG) patterns

In section 4.1.4, the growth of GaN nanowires using pulsed MOVPE growth technique was discussed. The nanowires were grown in circular apertures patterned using interferometric lithography based patterning technique introduced in [5] and also highlighted in Fig. 4.3. The growth dielectric was patterned all over the wafer and hence, the nanowires were grown out of the apertures across the whole wafer. In section 4.1.4, the nanowires were grown on the entire wafer and hence the n-contact fabrication step involved plasma assisted dry etching of GaN nanowires, which is more difficult to control rather than that of planar GaN. This issue has been further highlighted in the section 5.1 of chapter 5. However in this section, the growth of GaN nanowires in selected regions of the wafer was discussed. This method is referred to as selective area nanowire growth (SANG) technique in this thesis. The nanowire growth regions are self-aligned with the p-side and n-side contacts to fabricate the nanowire LED, thereby making it very convenient to fabricate the coaxial nanowire.

The growth mask for the SANG technique was patterned exactly in a similar technique as described in Fig. 4.3 for the continuous nanowire growth pattern. An additional photolithography step was introduced in between step 5 and step 6 illustrated in Fig. 4.3, to grow GaN nanowires and self-aligned coaxial LEDs. This step has been further illustrated in Fig. 4.24.

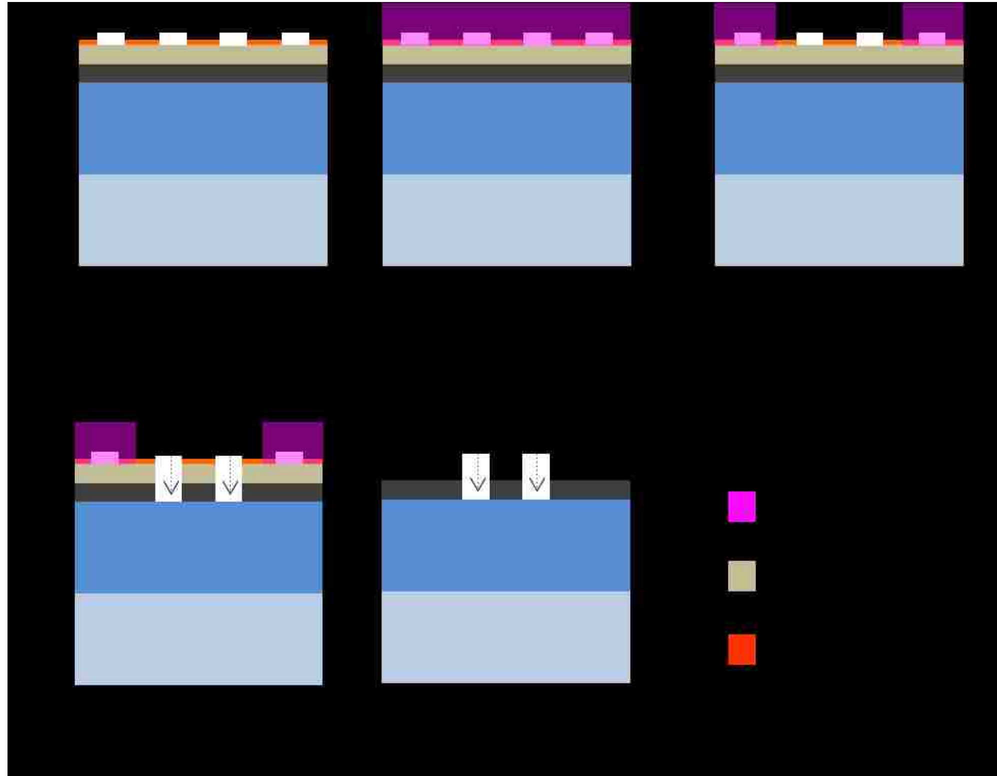


Fig. 4.24 The pictographic illustration of the nanoscale processing involved in patterning of dielectric (SiNx) patterns to define regions to grow GaN nanowires in the selective area nanowire growth (SANG) is shown

The GaN nanowires were grown in these patterned substrates at the same temperature (980°C) and pressure (100torr) as all the 3D GaN structures were grown at in this thesis. However, the V-III ratio had to be changed to achieve well-directed uniform GaN nanowires. The study was conducted to achieve this is described in the following sub-section.

The V-III ratio of 550 that was used for the growth of 3D nanowires was initially used to grow these nanowires as well. However, it was observed, as shown in Fig. 4.25 that under these conditions, the nanowires coalesced with each other, in some cases, leading to a planar GaN film, similar to epitaxially lateral over grown (ELOG) GaN films.

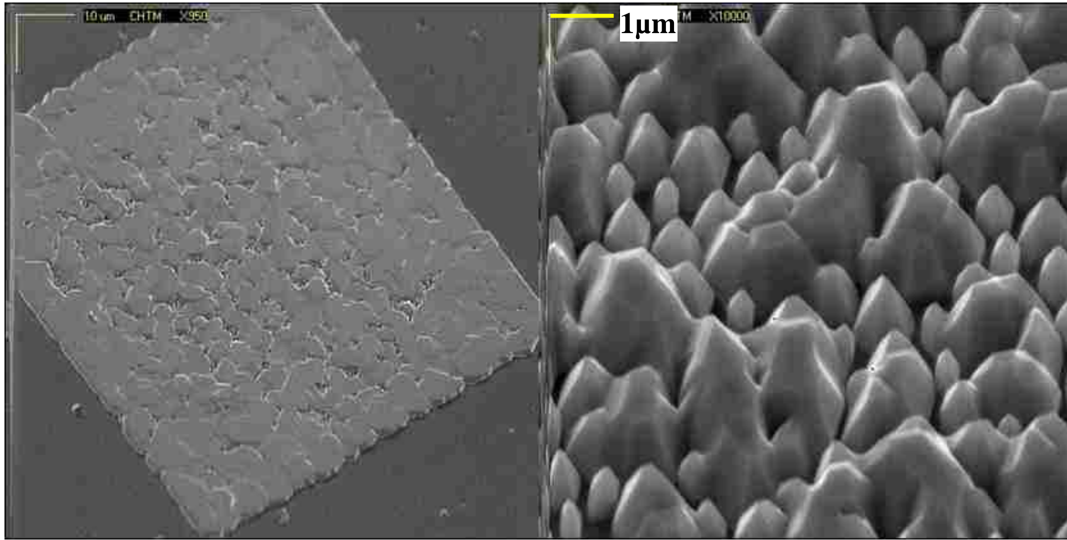


Fig. 4.25 The GaN nanowires grown in the SANG patterns with a V-III ratio of 550, which was used in the other nanowire and microstructure growths described in the earlier sections.

Thus, the V-III ratio was increased in the subsequent growths to achieve distinguishable GaN nanowires, instead of a coalesced GaN film. Fig. 4.26(a) shows a group of GaN nanowires grown at a higher V-III ratio of 2460 (sample#NW155), while Fig. 4.26(b) shows a group of nanowires grown at a V-III ratio of 1080 (sample#NW158). NW155 was grown for 20cycles, while NW158 was grown for 40 cycles. In both these cases, the nanowire growths were far from perfect. Another important difference between the two growths shown in Fig. 4.26 was the initial hydrogen ambient bake time. NW155 had a bake time of about 1min, while it was reduced to 30sec for NW158. This was attributed to why NW158 had complete pyramidal nanostructures, while NW155 had incomplete, irregular structures.

Fig. 4.27 shows a group of GaN nanowires grown at a V-III ratio of 878 (sample#NW156). The initial hydrogen ambient bake time was maintained at 30sec and the growth time was 20cycles. The nanowires grown under these conditions had a

hexagonal cross-section with a height of 1.5μm. The nanowires had a pyramidal top, as shown in Fig. 4.27(a), indication of a faster growth rate. Thus, the V-III ratio was reduced for the next growth in order to get flat top nanowires.

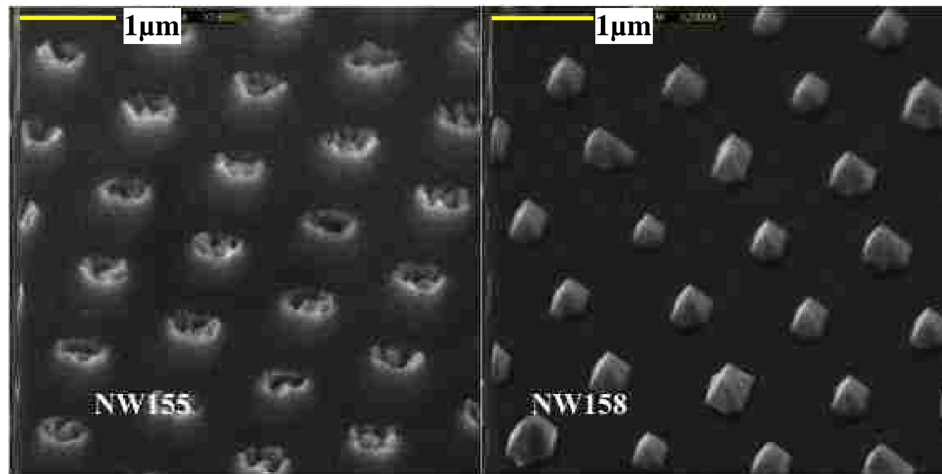


Fig. 4.26 SEM images of NW155 (V-III ratio = 2460) and NW158 (V-III ratio = 1080) are shown. These images are illustrating the fact that a lower V-III was needed to achieve GaN nanowires.

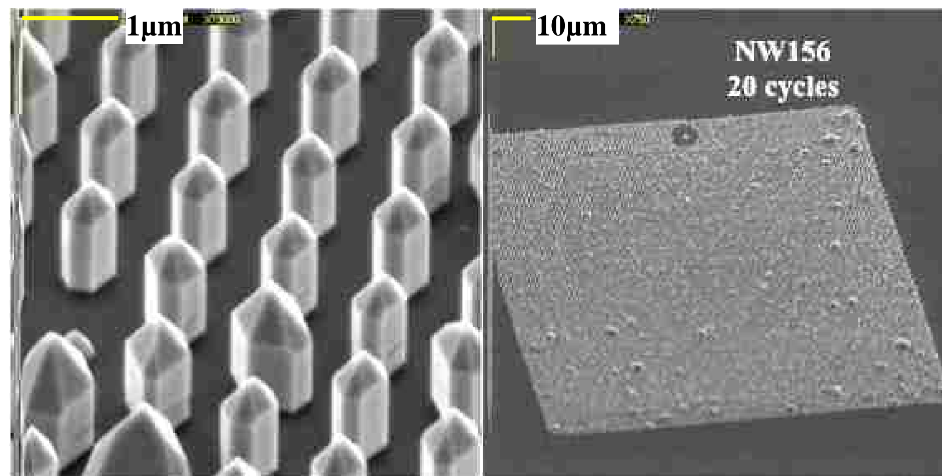


Fig. 4.27 SEM images of NW156 (V-III ratio = 878) are shown. The GaN nanowire growth has been achieved, but the nanowires have pyramidal tops, indicating a necessity of a higher V-III ratio to get flat top nanowires by reducing the growth rate.

Fig. 4.28 shows a group of GaN nanowires grown at a V-III ratio of 965 (sample#NW157). Once again, the initial bake time was maintained at 30sec, while the growth time was increased to 40cycles. The nanowires grown under these conditions had flat tops with a hexagonal cross-section and a height of about 2μm. The V-III ratio of around 965 was thus anticipated to be perfect to grow GaN nanowires in the SANG patterns.

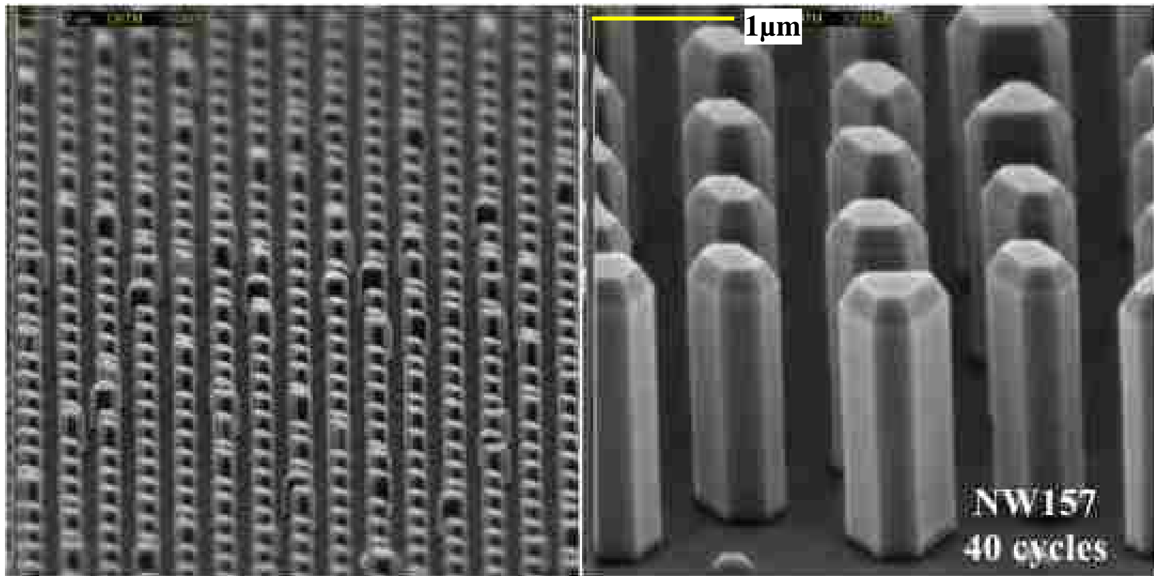


Fig. 4.28 SEM images of NW157 (V-III ratio=965) are shown. The GaN nanowires have flatter tops, in comparison to NW156. A slight increase in V-III could improve the flatness of the top facet of the nanowires.

4.5 Conclusion

The GaN 3D structures were grown using selective area growth method without the use of a catalyst using pulsed MOVPE growth. The growth of 3D GaN structures on various templates was discussed and analyzed. Although it was concluded that a low V-III ratio was necessary for the growth of GaN nanowires in [5], the V-III ratio needed was shown to be a little higher while growing 3D GaN structures in SANG growth patterns. The 3D GaN microstructures grown had 6 $\{1\bar{1}00\}$ sidewalls, which was different from what was demonstrated in earlier work [8]. The capture radius was defined and calculated as about 250nm for the GaN microstructures grown under the growth conditions specific for the 3D GaN growth. 3D GaN patterns were grown on hexagonal annulus patterns using the same growth conditions used for 3D GaN microstructure growth. The annulus wall patterns showed a considerably higher lateral growth rate on the edges, in comparison to the center. Thus, for the microstructure growth, the capture radius was anticipated to be higher for the structures on the edge of a given group pattern as compared to the growth structures within a group. The hexagonal annulus pattern also revealed differences in the growth rates of the inner concave sidewalls and outer convex sidewalls. It was shown in [10] that the faster growing crystallographic planes cease to exist on the outer convex side, while the faster growing planes on the inner concave side of the annulus structures were shown to exist. Thus, the inside of the hexagonal annulus structure had a different shape in comparison to the outside of the same structure. GaN nanowire growths on SANG patterns was also demonstrated and a higher V-III ratio was shown to be required to grow nanowires in these patterns. These structures were then

used as the core for the core-shell structures and coaxial LEDs discussed in the next chapter.

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Chapter 5

Growth of Coaxial 3D structures based on GaN

In the previous chapter, the selective area growth (SAG) of GaN in different shaped apertures was discussed. The GaN (doped with silicon to give n-GaN) was grown in circular apertures of diameters in the range of 300nm to about 10μm. The n-GaN grown 3D in these apertures was then used as the core for the subsequent coaxial structures. Shell materials, other than binary GaN, were also grown coaxially around the n-GaN, thereby exploring the possibility of making homo-junction LEDs, as well as hetero-junction LEDs. The growth of coaxial structures is discussed in section 5.1. GaN was grown p-type coaxially around the n-GaN core to create p-n homo-junction core-shell structures. On the other hand, $Al_xGa_{1-x}N$ ('*x*' indicates the % of aluminum in the alloy) and $In_yGa_{1-y}N$ ('*y*' indicates % of indium in the alloy) were grown coaxially around the n-GaN to fabricate hetero-junction coaxial structures. These structures are then processed using the coaxial LED process, discussed in chapter 6 to fabricate p-n junction LEDs.

Core-shell GaN based LEDs have a number of benefits, which were already highlighted in section 1.2 of chapter 1. Qian *et al.* [1] were one of the first to fabricate GaN based coaxial LEDs and demonstrate their electrical and optical characteristics. Their core-shell structures were grown using the catalytic VLS growth mechanism, which was discussed in section 2.1 of chapter 2. Subsequently, Koester *et al.*, [2] and Bavencove *et al.* [3] also demonstrated GaN based coaxial LEDs grown without the use of catalyst using *in-situ* grown SiN_x based SAG technique. Bergbauer *et al.* [4] have also

demonstrated core-shell structures based on GaN grown by ex-situ grown SiN_x based SAG technique, which is very similar to the SAG technique employed in this thesis to grow core-shell structures. However, the pulsed MOVPE growth of core-shell GaN based structures pursued in this thesis is unique. In this section, the growth of coaxial GaN based structures is discussed.

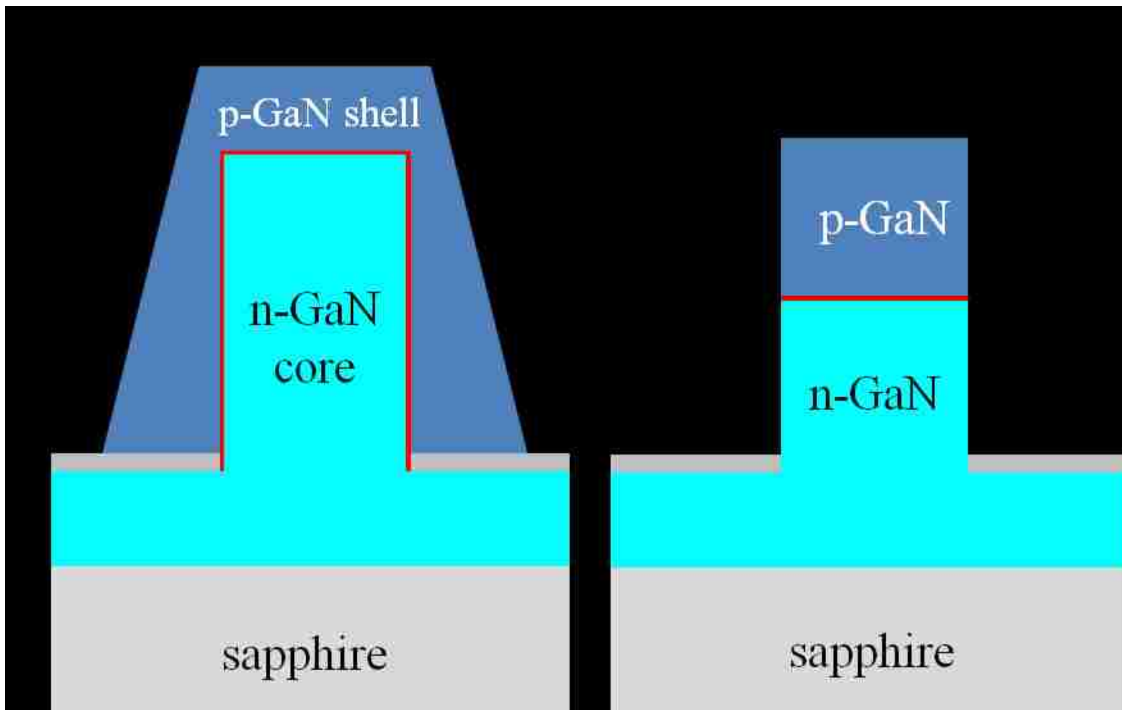

Fig. 5.1 (a) The structure of a coaxial p-n homo junction GaN based LED compared with (b) the structure of a non-coaxial p-n homo junction GaN based LED analyzed and reported in [6]

5.1 Growth of p type GaN shell on n-type GaN core

The structure of the p-n homo-junction coaxial GaN diode is shown in Fig. 5.1(a). The GaN core is doped with silicon (Si) to achieve n-type GaN, while the outer GaN shell is doped with magnesium (Mg) to achieve p-GaN. GaN based p-n homo-junction nanowire LEDs have been fabricated in previous work [5]. The *I-V* and the *L-I* curves

obtained from the diodes fabricated in [5] were reported in [6]. These p-n junction diodes were non-coaxial, as shown in Fig. 5.1(b) and thus had a smaller active region area, in comparison to the coaxial p-n junction LED (Fig. 5.1(a)).

The n-type GaN was grown using pulsed MOVPE growth technique, which has been discussed in section 4.1 of chapter 4. The use of pulsed MOVPE growth was shown to generate non-coaxial vertical growth of p-GaN. Thus after the growth of the core, the p-GaN shell was grown using regular MOVPE growth technique with trimethyl gallium (TMG) and ammonia (NH_3) as the source precursors. 40sccm of Biscyclopentadienyl Magnesium (CPM2) was flown along with the source precursors to incorporate Mg, the p-type dopant. The p-GaN was grown under a chamber pressure of 200torr and at a temperature of 1000°C. After the growth of p-GaN, the sample was thermally annealed at 700°C in nitrogen atmosphere, *in-situ*, to activate the p-type dopants. Fig. 5.2 shows the scanning electron microscope (SEM) images of the coaxial p-n homo junction microstructures (wires and walls).

The SEM images of the coaxial homo-junction LED show rough top c-plane facets. Further investigation is required to find out the exact reason for the surface roughness. However, the top side being rough is a blessing in disguise for better light extraction for LEDs. The SEM images shown in Fig. 5.2 also indicate structures with a pyramidal cross-section.

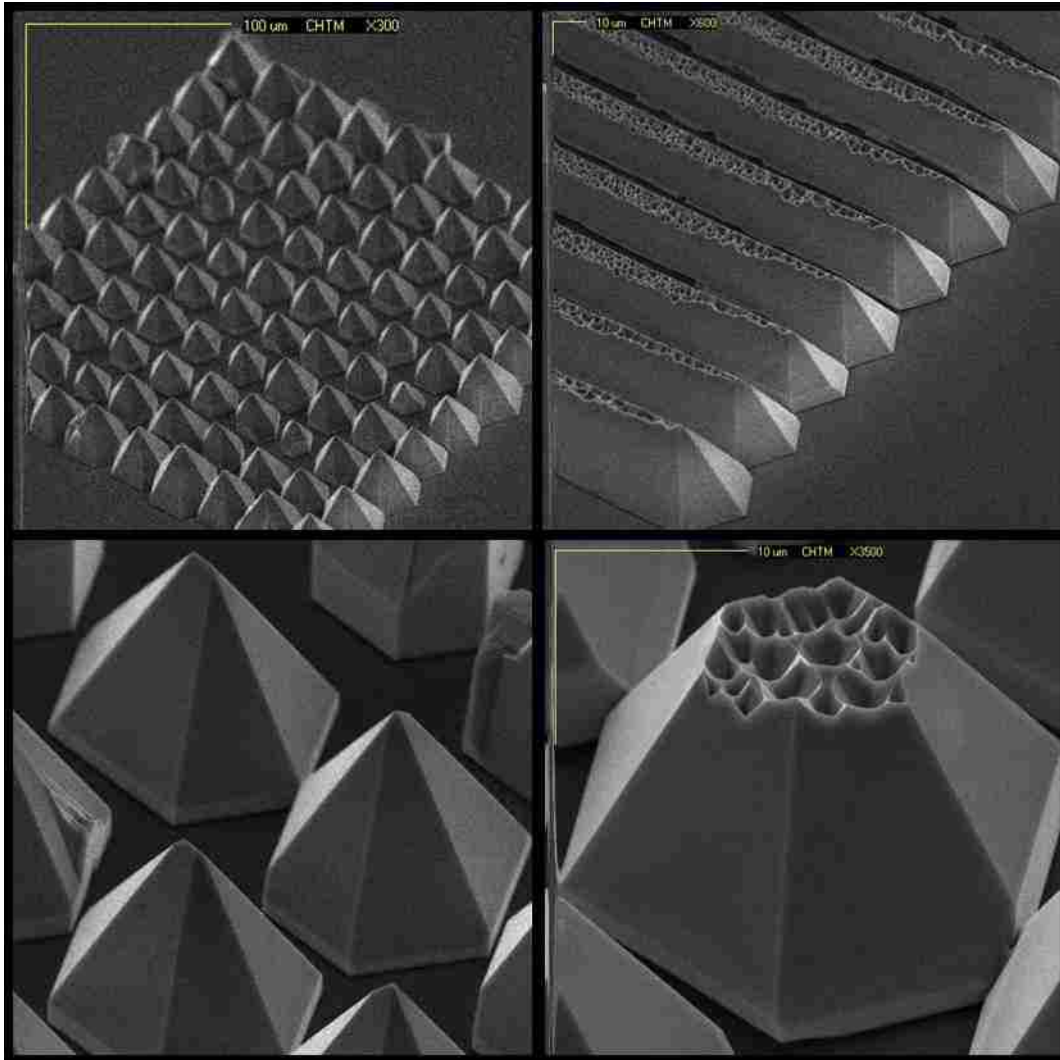

Fig. 5.2 SEM micrographs of p-n homo junction coaxial GaN based LEDs

Previous work [7] has shown the growth of pyramidal GaN based structures using regular MOVPE growth technique with $\{1\bar{1}01\}$ sidewalls. In [7], GaN was grown selectively in growth apertures patterned on planar GaN on substrate. The pyramidal GaN nanostructures were shown to grow laterally, thereby leading to the coalescence of individual 3D GaN nanostructures to produce a planar low TD GaN film. Using these growth conditions, GaN could be grown laterally around the 3D GaN structures with vertical $\{1\bar{1}00\}$ m-plane sidewalls. Fig. 5.3 shows the SEM image of the cross-section of the coaxial p-n homo-junction GaN based LED grown using the growth technique

described previously. It can be observed from the cross-section SEM image that the p-n junction could be still maintained on the non-polar vertical $\{1\bar{1}00\}$ sidewalls. The clear contrast between the pulsed grown n-GaN core and the p-GaN shell grown by regular MOVPE is also observable in the image.

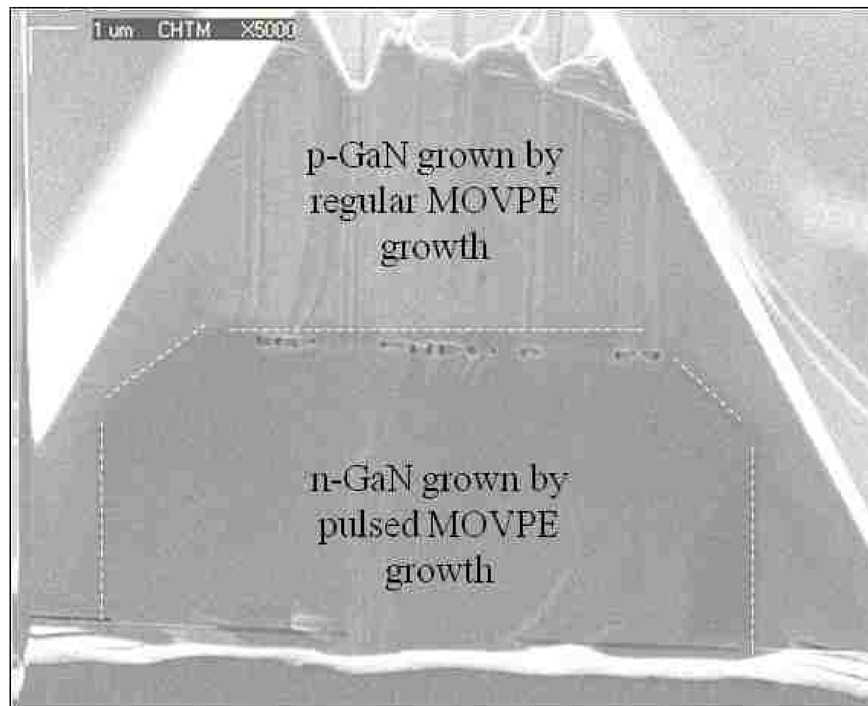

Fig. 5.3 The cross-section SEM image of a p-n homo junction GaN based LED

The SEM image shown in Fig. 5.3 also shows a number of voids on the top c-plane between the pulsed grown n-GaN and the p-GaN grown using the regular growth conditions. The n-GaN cores grown by pulsed MOVPE growth have a flat c-plane top and have a nitrogen-terminated surface. However, the pyramidal 3D GaN structures have been shown to have a gallium-terminated surface. It was also concluded in [15] by Chen *et al.* that N-polar crystals favored the growth of GaN wires with vertical sidewalls, while Ga-polar crystals favored the growth of inclined facets, limiting the vertical extension and lead to the formation of pyramids. The change in the growth mode in between the

core n-GaN and the shell p-GaN section leads to the two oppositely oriented GaN crystals bonding with each other. This could lead to the formation of inversion domains (ID's) along the <0001> c-direction. Romano *et al.* [12] and Xin *et al.* [14] have observed the formation of micro-voids, nanopipes and inversion domains in GaN grown by molecular beam epitaxy (MBE) and MOVPE. It was observed in [12] that under Ga rich growth conditions, the flat GaN surfaces were favored, while nitrogen rich conditions produced more pyramidal hillocks. Rouviere *et al.* [13] have studied the different crystallographic defects in Ga-polar materials, where the irregular, wide shaped voids/holes were observed to appear in poor quality materials at the interface of columnar grains. Further investigation of the voids observed in these p-n homojunction GaN microstructures is required.

5.2 Growth of p-AlGaN shell on n-GaN core

The growth of $Al_xGa_{1-x}N$ (x = fraction of aluminum) shell surrounding the GaN core was carried out entirely using pulsed MOVPE growth conditions, similar to that used for 3D GaN micro/nanostructures. It was shown in chapter 4 that during the pulsed growth involving TMG and NH3 as the growth precursors, the growth rate of GaN was much higher in the <0001> c-direction, as compared to the lateral <$1\bar{1}00$> direction. However, the addition of TMA during the pulse cycle of TMG to grow AlxGa1-xN altered this growth mechanism. This suggested that aluminum had a higher diffusion rate as compared to gallium. One of the reasons attributed to this was that the growth precursor to incorporate aluminum (Al), trimethyl aluminum (TMA), was more reactive as compared to TMG at the given growth conditions. This reason could also explain the deposit of polycrystalline material on the dielectric mask during the growth of AlGaN-

GaN coaxial structures, which was absent during the growth of GaN core 3D structures (as shown in Fig. 5.4(c)).

The GaN core was grown under a chamber pressure of 100torr and a temperature of 970°C using TMG and NH3 as the growth precursors. The GaN core was doped n-type by flowing SiH_4 along with TMG. The AlGaN shell was grown under the same chamber pressure (100torr), but at a different temperature (960°C). Biscyclopentadienyl magnesium (CPM2) was flown along with TMG and TMA, so that the shell may be doped with magnesium (p-type). NH_3 was used as the group V precursor. The V-III ratio for this growth was maintained at 550 for the core-shell growth.

Fig. 5.4(a) shows the SEM images of GaN-AlGaN coaxial nanowires grown by pulsed MOVPE growth technique, along with a comparison with just core GaN nanowires (Fig. 5.4(b)) grown for the same length of time. It can be observed that while the GaN core nanowires had flat tops, the $Al_xGa_{1-x}N$ nanowires had predominantly pyramidal tops. Hence, the evolution of the new semi-polar planes could also be correlated to the growth of $Al_xGa_{1-x}N$ around the GaN core structures. Fig. 5.4(c) shows the cross-section transmission electron microscope (TEM) image of an array of AlGaN-GaN coaxial nanowires showing the GaN core and AlGaN shell having different contrast. The polycrystalline deposits on the mask are also observed in this image. A detailed TEM image of AlGaN-GaN core-shell nanowires was already shown in Fig. 3.10 of chapter 3. The electron dispersive spectroscopy (EDS) analyses presented in chapter 3 showed the presence of aluminum in the outer section of the nanowires, indicative of $Al_xGa_{1-x}N$ shell around the GaN core.

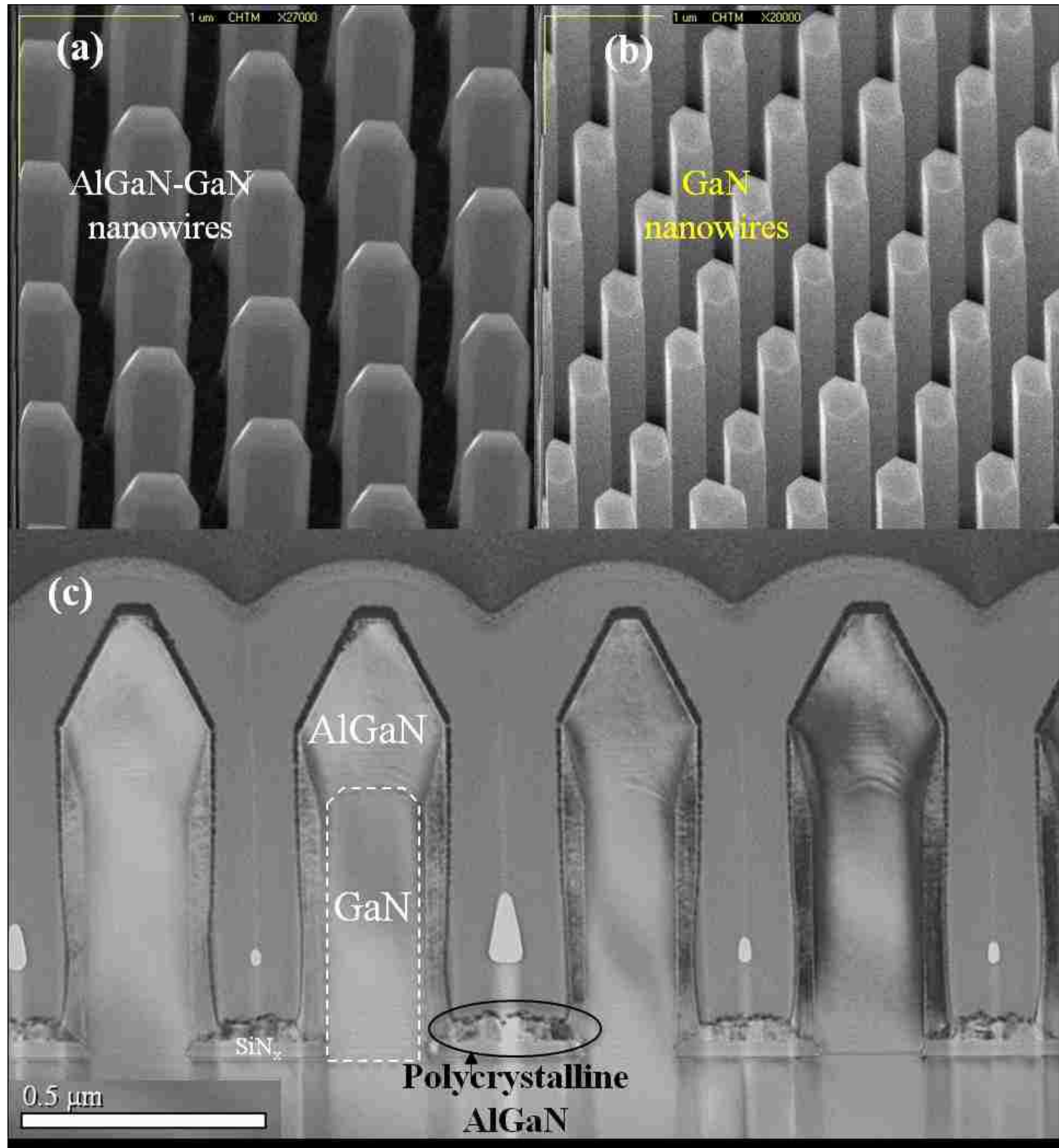

Fig. 5.4 (a) SEM micrographs of AlGaN-GaN coaxial structures in comparison with (b) core GaN nanowires, (c) shows the cross-section TEM image of an array of AlGaN-GaN coaxial nanowires.

AlGaN shells were also grown around 3D GaN microstructures, which were grown using the pulsed MOVPE growth technique on substrates patterned using the COLED mask set. The growth conditions for the core-shell structures were the same as for the core-shell nanowires. Fig. 5.5 shows the SEM images of AlGaN-GaN coaxial

microstructured holes and walls along with a comparison of the coaxial microstructures with core GaN microstructures. It can be observed that the AlGaN-GaN coaxial micro-structures also had a pyramidal top with a reduced c-plane.

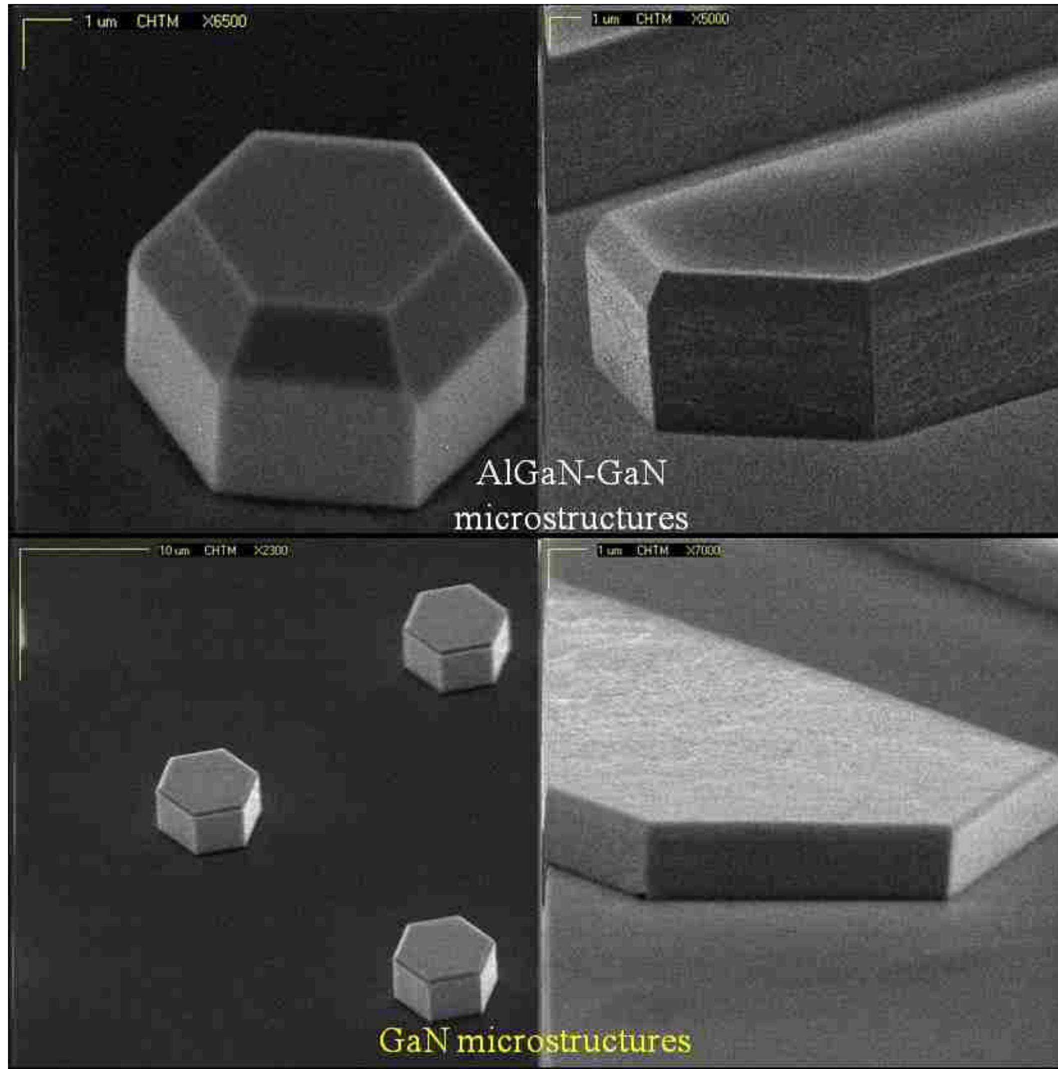

Fig. 5.5 The SEM micrographs of AlGaN-GaN coaxial microstructures and their comparison with core GaN microstructures. The GaN microstructures have flat tops, while the AlGaN-GaN coaxial structures have pyramidal tops.

The photoluminescence (PL) spectrum from an AlGaN-GaN coaxial nanowire LED sample is shown in Fig. 5.6. In the PL of some of the coaxial LED samples, at least two compositions of Al in $Al_xGa_{1-x}N$ could be deduced from the PL spectra. This was an

indication that the incorporation of aluminum was different on different crystallographic orientations.

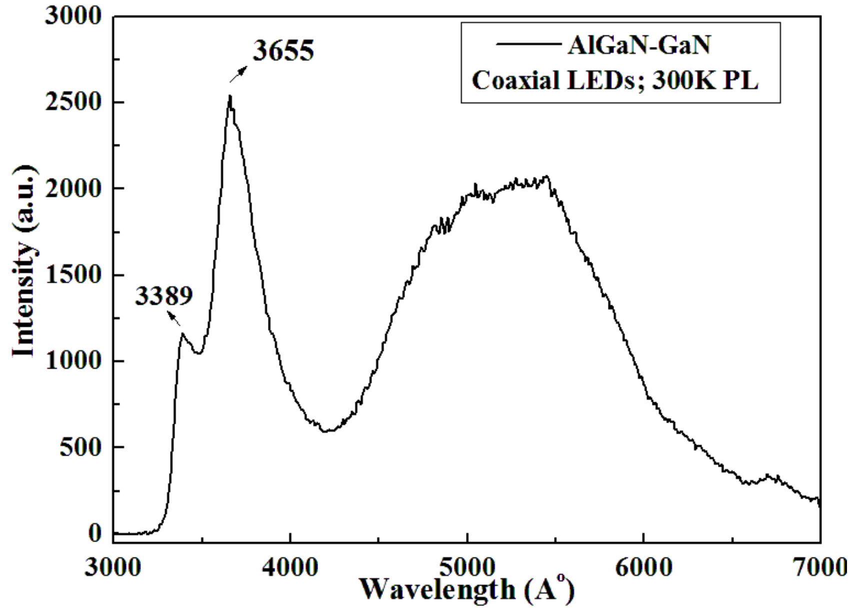

Fig. 5.6 PL spectrum of NW#73B (an AlGaN - GaN coaxial LED sample) at 300K

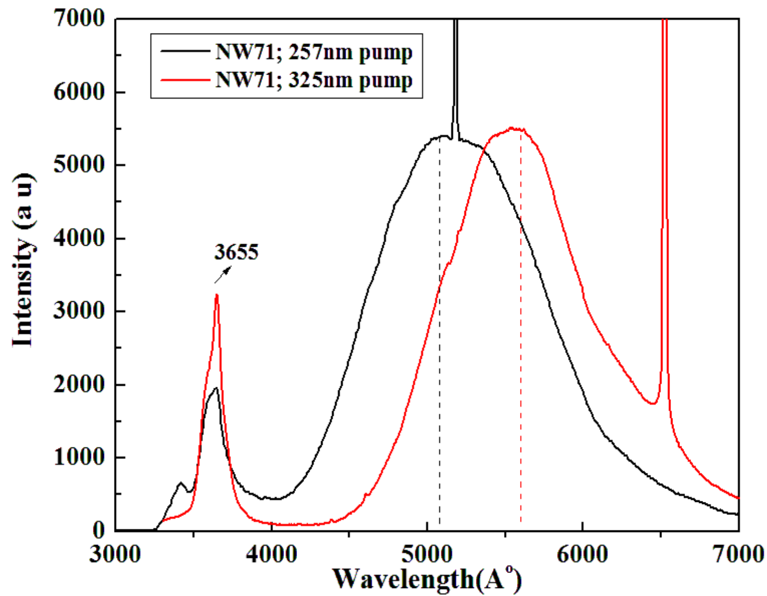

Fig. 5.7 PL spectra of nw71 (AlGaN-GaN coaxial LEDs) using two lasers (Ar:ion-257nm and He-Cd-325nm wavelength)

Fig. 5.7 shows the PL of AlGaN-GaN coaxial nanowire LED excited with different laser sources. The absorption coefficient, α (units of cm^{-1}), of a semiconductor is defined as the inverse of the thickness over which the semiconductor material can absorb 64% of the incident photons on the given material.

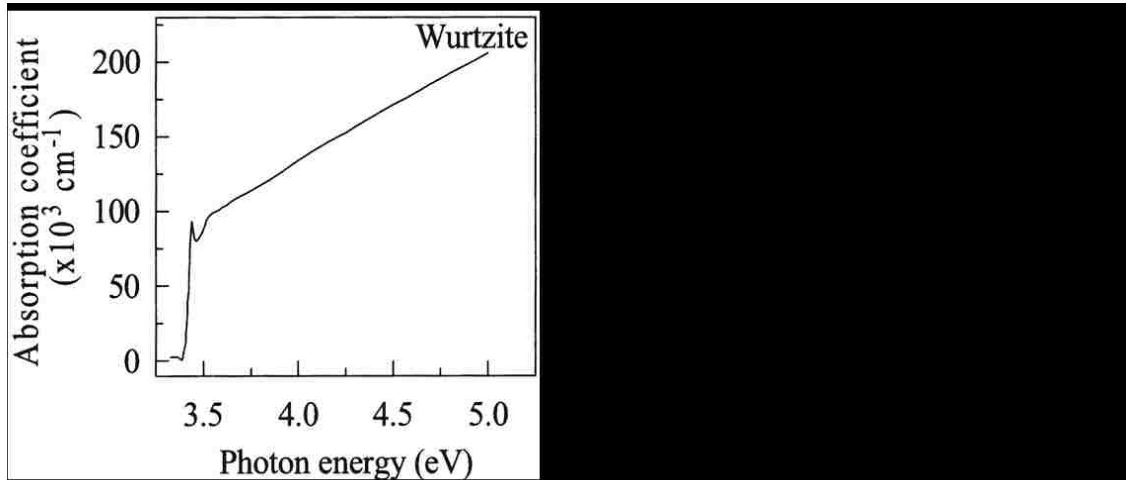

Fig. 5.8 (a) shows the absorption coefficient of wurtzite GaN as a function of incident photon energy in eV, image reproduced from [9] and (b) shows a simple illustration of the energy band diagram of GaN with transition between the energy level of the donor and the defect (group III vacancies) energy level corresponding to the yellow luminescence.

The absorption coefficient parameter is dependent upon the energy of the incident photons and increases with the increase in energy of the incident photons, as shown in Fig. 5.8(a). In other words, the thickness over which most of the incident photons would be absorbed would be much lesser if the energy of the incident photons was higher. The light excitation from the He-Cd laser (325nm excitation) seems to be absorbed over a much higher thickness, in comparison to the shorter wavelength (higher energy), 257nm Ar: ion laser. Hence, the PL spectra obtained by shorter wavelength laser excitation seems to show a peak corresponding to the AlGaN (340nm), while the PL obtained by the longer wavelength laser does not show the peak, even though the wavelength of the

excitation laser is shorter than the wavelength corresponding to the AlGaN under consideration. Hence, the shorter wavelength, 257nm Ar: ion laser was often preferred to estimate the % of Al in the coaxial structures, as opposed to the longer wavelength, 325nm He-Cd laser.

It is also possible to note a blue shift in the yellow defect luminescence of the nanowire sample upon excitation with a shorter wavelength laser. The yellow luminescence has been attributed to the group III vacancies in GaN by Hofmann *et al.* [9]. Positron annihilation experiments performed by Saarinen *et al.* [10] suggest a direct correlation of the yellow luminescence and group III vacancies. The trapping of the positron by the presence of negative and neutral vacancies due to the missing positive ion core provides a direct probe of the vacancies in the sample. The intensity of the yellow luminescence was found to correlate with the concentration of vacancies, represented by an energy level of a group III vacancy (E_{vIII}) , between the valence band energy level (E_v) and conduction band energy level (E_c), as shown in Fig. 5.8(b). For $Al_xGa_{1-x}N$, this difference between the vacancy energy level and the conduction band energy level (E_c) is larger than for GaN. Hence, a blue shift was observed in the yellow luminescence, as shown in Fig. 5.7. The laser excitation using the 325nm laser was absorbed more in the GaN core, as opposed to the AlGaN shell and thus the yellow luminescence was centered on 550nm.

5.3 Growth of InGaN shell on n-GaN core

In the previous two subsections, the growth of p-GaN and p-AlGaN shells around the GaN core was discussed. In this subsection, the growth of undoped InGaN shells

around GaN cores was discussed. The growth conditions are still being refined to achieve the ideal InGaN shell layer over the GaN core. The importance of being able to grow InGaN multi-quantum well shells over n-GaN core structures was already discussed in chapter 1. The information obtained and presented in this subsection is just a study of some samples, where it is believed that InGaN shell growth was observed, but in general, the growth of InGaN shell structures has been problematic.

The MOVPE growth of InGaN shells was different from the growth conditions used for the growth of AlGaN and p-GaN shells over GaN cores. It has been demonstrated in [11] that the growth of InGaN required a temperature of 700-800°C in the absence of hydrogen (H_2) carrier gas. However, the flow of H_2 gas during the pulsed growth of GaN cores and AlGaN shells was found to be necessary [5]. Hence, the InGaN shells were grown using regular MOVPE growth mode, instead of the pulsed MOVPE growth technique, in the absence of hydrogen gas. After the pulsed MOVPE growth of GaN core nanowire structures at 970-980°C using TMG and NH_3, the temperature of the substrate was gradually reduced to around 700-800°C depending upon the required composition of indium in $In_yGa_{1-y}N$. It has been shown in [11] that the indium incorporation in $In_yGa_{1-y}N$ was temperature dependent and hence, in all the experiments, the flow of trimethyl indium (TMI), the growth precursor used for growing $In_yGa_{1-y}N$, was kept constant at 40sccm and the chamber pressure was maintained at 100torr. TMG, TMI and NH_3 were the gases that were flown to grow the InGaN layer. Nitrogen (N_2) gas was flown as the carrier gas, thereby completely eliminating the H_2 from the chamber. The V-III ratio in the gas phase was calculated as around 15500. Fig. 5.9 shows the SEM

images of GaN nanowires with a layer of InGaN grown (InGaN growth time = 24min) on them.

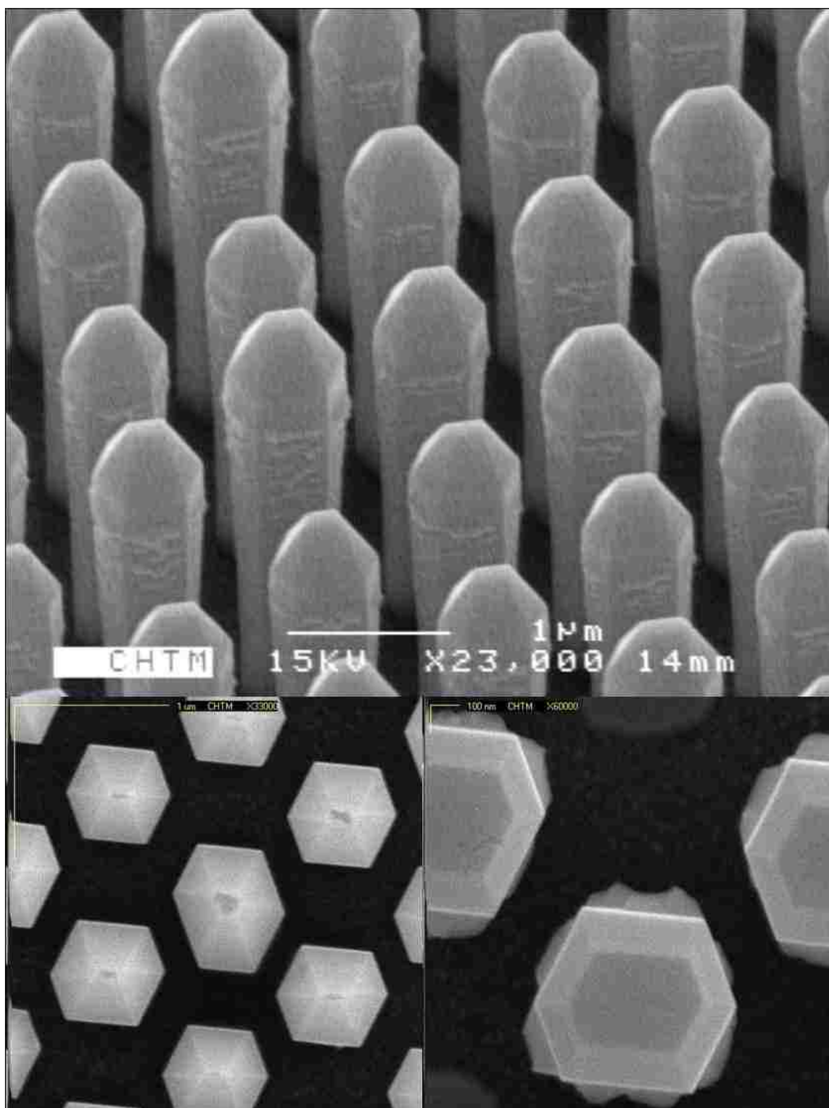

Fig. 5.9 SEM images of InGaN-AlGaN-GaN coaxial structures grown by MOVPE

A simple study using low temperature photoluminescence (77K PL) was conducted to analyze the incorporation of indium (y) in $In_yGa_{1-y}N$ with respect to the growth temperature. Table 5.1 shows the different samples that showed luminescence corresponding to InGaN. In the samples (NW#8, 10, 11 and 15), an additional shell layer of AlGaN was grown between the GaN core and the InGaN shell. This was done because it was reported in previous work [5] that GaN nanowires with InGaN shells had poor fill factor. The addition of AlGaN shell between the GaN core and the InGaN shell was believed to stabilize the growth of InGaN and avoid the GaN nanowires from melting during the InGaN growth.

NW#8	700	390-460	443	130	24 min InGaN
NW#10	650	374-480	454	1	24 min InGaN
NW#11	750	395-425	401	11	24 min InGaN
NW#15	700	399-434	416	31	12 min InGaN

Table 5.1 The 77K PL details of various nanowire samples with a layer of InGaN grown around the nanowires

The 77K PL spectra of the three samples analyzed are shown in Fig. 5.10. It was clear from NW#8 and NW#11 that upon lowering the growth temperature, the indium incorporation also increased, thereby increasing the peak wavelength of 77K PL

emission. It was also observed that the peak emission wavelength was also dependent on the growth time.

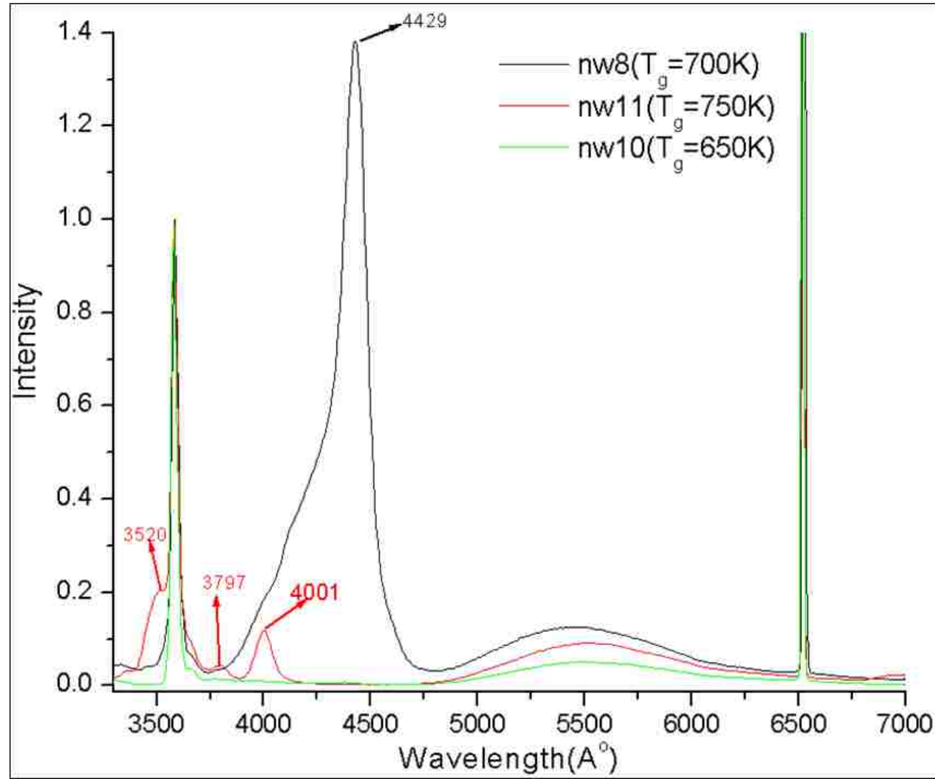

Fig. 5.10 PL spectra of three samples with InGaN shell wrapped around an AlGaN-GaN coaxial structure grown at three different temperatures are shown.

Fig. 5.11(a) shows a graphical illustration of the linewidth of the 77K PL obtained from the three samples mentioned in table 1, while Fig 5.11(b) shows a plot of the percent relative intensity of the InGaN PL peak with respect to the growth temperature. The incorporation of indium into the 3D GaN structures is still being pursued.

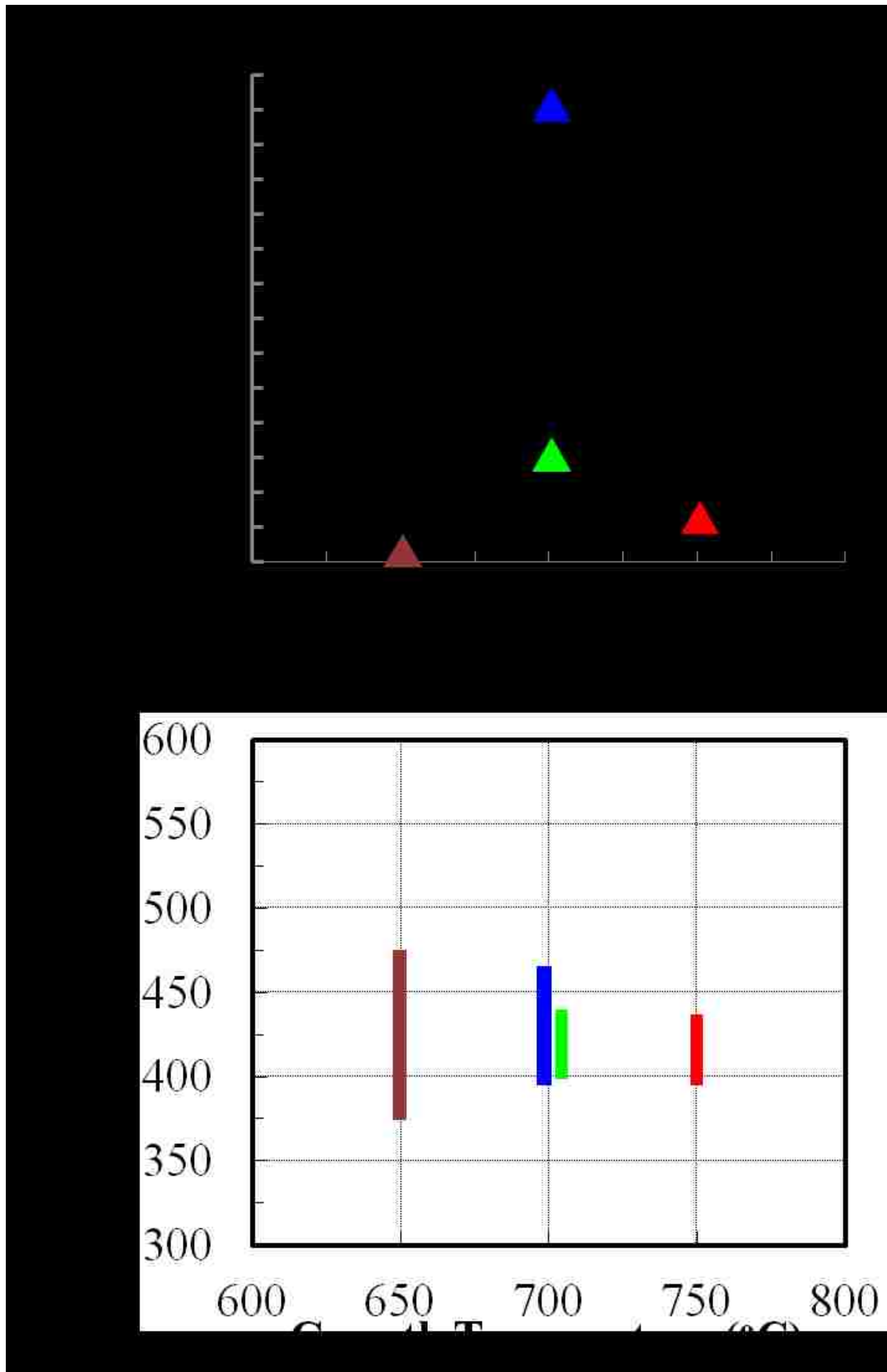

Fig. 5.11 The plot of the intensity of 77K InGaN PL was shown in (a), (with reference to the intensity of the GaN PL) and the line width of the InGaN PL was shown in (b), for samples, whose InGaN layer was grown at different temperatures.

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Chapter 6

Processing and Characterization of Coaxial LEDs based on GaN

In the previous chapter, the growth of coaxial GaN based structures was discussed. In this chapter, the basic steps involved in the fabrication of the coaxial LED are discussed along with the characterization results from the fabricated LEDs. Two different processing approaches were adopted to process the coaxial LEDs. The first approach was called a liftoff based p-metal process (process 1.1), while the second approach was a non-liftoff based p-metal process (process 1.2).

6.1 Process 1.1: Liftoff based p-metal process

The steps of process 1.1 are illustrated pictographically in Fig. 6.1

Step 1: Photolithography: p-metal mask

After the growth of the coaxial structures, the first step was to define the region where the coaxial structures are electrically pumped. This is also the section where the p-GaN/p-AlGaN is exposed to the ambient. This region was defined using regular mask photolithography. The sample was prepared for the photoresist spinning, which was already discussed in section 4.1 of chapter 4, using acetone, following which the wafers were immersed in iso-propyl alcohol (IPA) and the contents were placed in an ultrasonic bath for 5 min for rinsing, After which, each of the wafers was blown dry using nitrogen gas.

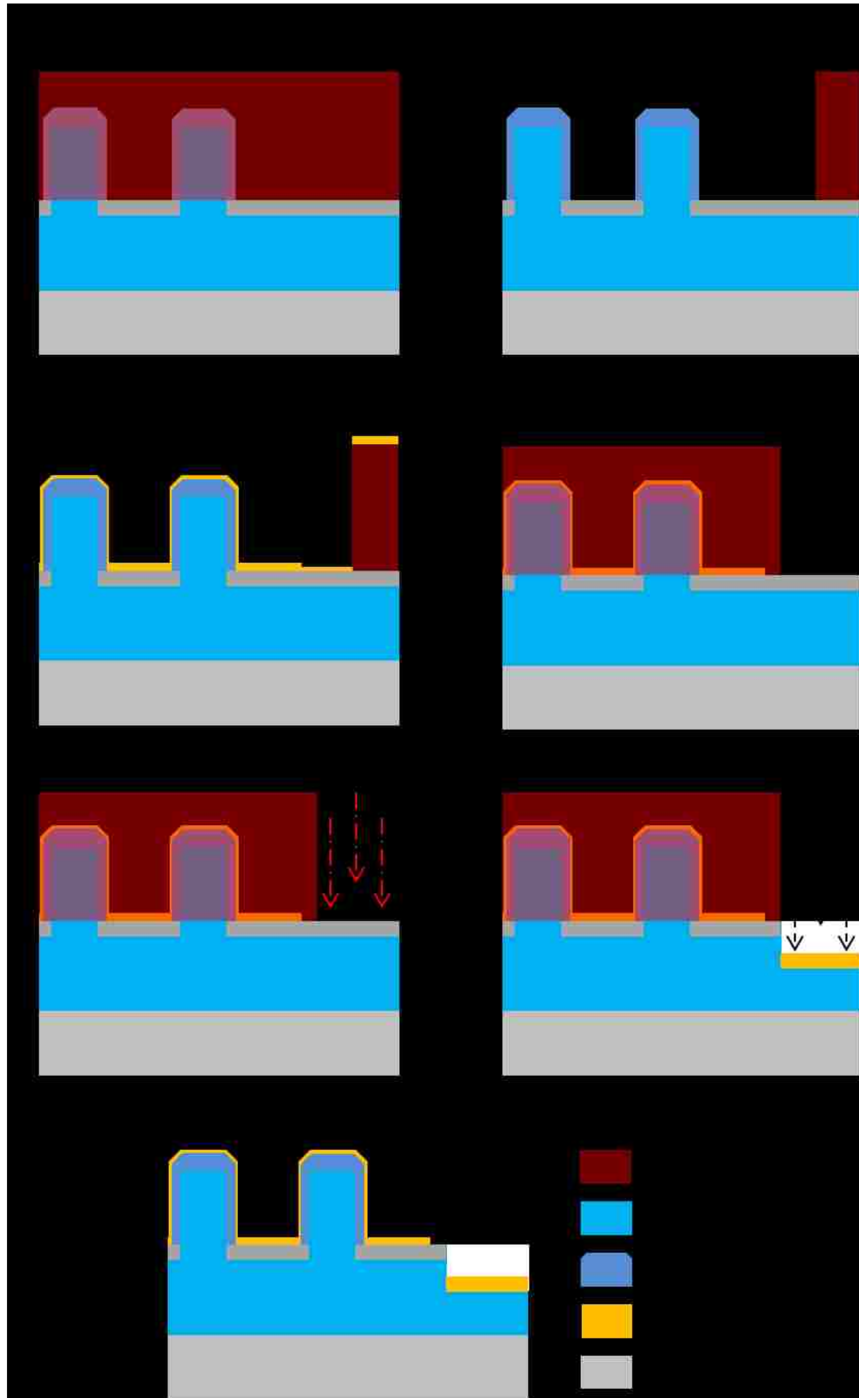


Fig. 6.1 The schematic illustration of the steps involve in process 1.1 (p-metal liftoff based coaxial LED process)

The photoresist used for the growth mask patterning is AZ4330. For this, the wafer was placed on the chuck of the spinner and some amount of photoresist was poured

on it. The photoresist was then spin coated on the wafer after engaging the vacuum on the chuck. The wafer was spun at an angular speed of 4000rpm for 30sec. Under these conditions, the optimal thickness of the photoresist was estimated around 3.5μm. Following this, a soft bake of the wafer was carried out on a hotplate set at 90°C for about 2min, prior to the exposure.

After the spin-coat process, the wafer was ready for the photolithography exposure. The mask aligner used for the photolithography was the Karl Suss MJB-3, which was also used for defining the features in the growth dielectric. The p-metal mask was first cleaned with IPA and blown dry, prior to usage. The mask holder in the aligner was placed face up with the vacuum grove visible and the p-metal mask was loaded with the mask side facing upwards. The mask was kept in contact with the holder by establishing a vacuum between the holder and the mask. After this, the holder was loaded in the aligner for UV exposure.

At this juncture, there was a slight difference between the p-metal side patterning for the coaxial nanowire LEDs and the coaxial microstructured LEDs. In case of the former, the p-metal mask used was from the nichia's GaN LED process masks, which were discussed in previous work [9]. There was no alignment required because this was the first lithography step used for the coaxial nanowire LEDs. In case of the coaxial microstructured LEDs, the COLED mask set was used. The COLED mask1 (also known as the growth mask) was used to pattern the growth dielectric to grow the 3D GaN microstructures, which was already discussed in section 4.1 of chapter 4. In case of the coaxial microstructured LEDs, the COLED mask2, also known as the p-metal mask, was used to define the LED region. The COLED masks are self-aligned set of masks and

hence, the p-metal definition required alignment of mask2 with the grown microstructures (mask1 growth mask pattern). Fig. 6.2 shows the pictographic illustration of the self-aligned COLED set of masks used. Both mask2 (p-metal mask) and mask3 (n-metal mask) are dark field masks that are transparent at the respective defined region, as shown in Fig. 6.2(b) and (c) respectively.

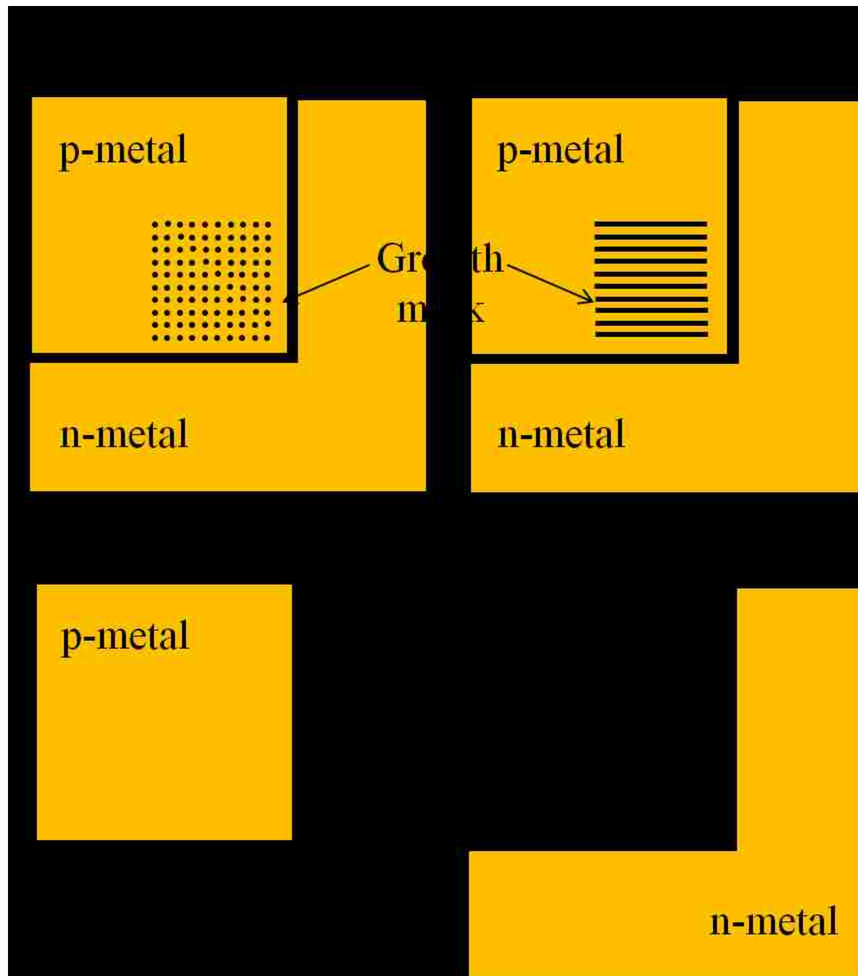


Fig. 6.2 The pictographic illustration of the three COLED masks aligned to each other is shown in (a); (b) shows mask2 (p-metal mask) and (c) shows mask3 (n-metal mask). Each of these masks is a dark field mask open in the golden sections shown.

After the alignment (in case of the COLED patterns), the sample was exposed to ultraviolet light under constant power conditions. A 5sec exposure at a constant power of 280mW was determined to be optimal exposure condition for the lithography under most

ambient conditions. After the exposure, the wafer was immersed in a developer to let the photoresist pattern develop. AZ400K was the developer used, which was diluted with water to control the developing time. AZ400K diluted with 4 parts of water (1:4) was preferred and the developing time was calculated to be around 70-80 seconds.

Step 2: Angled deposition of p-metal by e-beam evaporation

After the photolithography, the sample is prepared for the deposition of p-metal layers. Before loading the sample into the e-beam evaporator, the sample was loaded in the reactive ion etcher (which was discussed in section 4.1.4 of chapter 4). After loading, the sample was subjected to oxygen (O_2) plasma cleaning to remove leftover photoresist from the patterned regions. This process is also referred to as ashing. The flow rate of O_2 used was around 10 sccm under a chamber pressure maintained at 15mtorr. The etch time recorded was around 1min. After the ashing process, the sample was soaked in dilute hydrochloric acid solution (1HCl: $10H_2O$) to remove any native oxides that might have been formed during the ashing process.

After this, the sample was loaded into the e-beam evaporator and the chamber was pumped to a base pressure of 2×10^{-6}torr. The sample was loaded in a non-conventional angled manner, so as to allow for metal layer deposition on the sidewalls of the 3D coaxial structures, as highlighted earlier in Fig. 6.1. The conventional and the non-conventional angled wafer loading procedures into the e-beam metal evaporator are pictographically illustrated in Fig. 6.3(a) and (b) respectively.

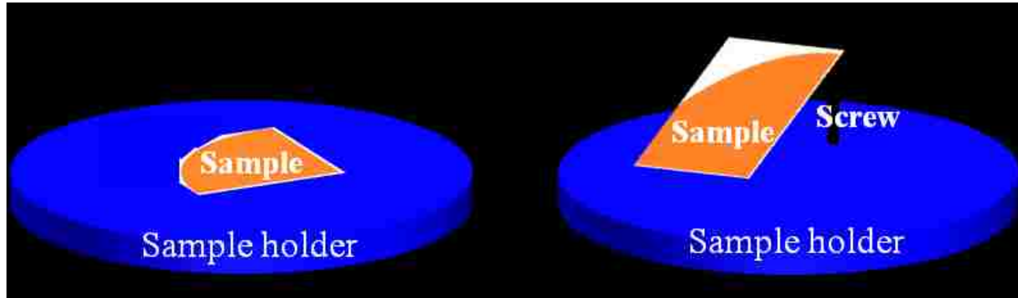


Fig. 6.3 (a) shows the conventional wafer loading mechanism into the metal evaporator and (b) shows the non-conventional angled loading mechanism.

Upon reaching the base pressure, e-beam evaporation of the metal layers was initiated. Some LED samples used thick p-metal layers, while some of the samples used thin p-metal layers depending on the direction in which the light was extracted. The details of the light extraction are discussed in subsequent sections. The layers of metals used for the thick p-metals were 50nm nickel (Ni) followed by 50nm of gold (Au). In case of the thin p-metal layers, 10nm Ni was first evaporated followed by 6nm of Au. After the evaporation of the metal layers, the sample is unloaded and the direction of wafer alignment is changed to deposit the p-metal layers over the regions that were shadowed during the first evaporation step. A minimum of two evaporations was required to achieve complete coverage of the p-metal layers. In most cases, four evaporations were performed to ensure all the regions of the coaxial LED had the contact metals on it.

After the evaporation of the metal layers, the sample is unloaded and then immersed in acetone for about an hour to initiate the liftoff. After that, an acetone spray gun was used to remove the metal and the photoresist, following which the sample was cleaned in IPA and then blown dry using nitrogen gas. Fig. 6.4 shows SEM images of coaxial microstructures LED sample with one layer of p-metal angled evaporation.

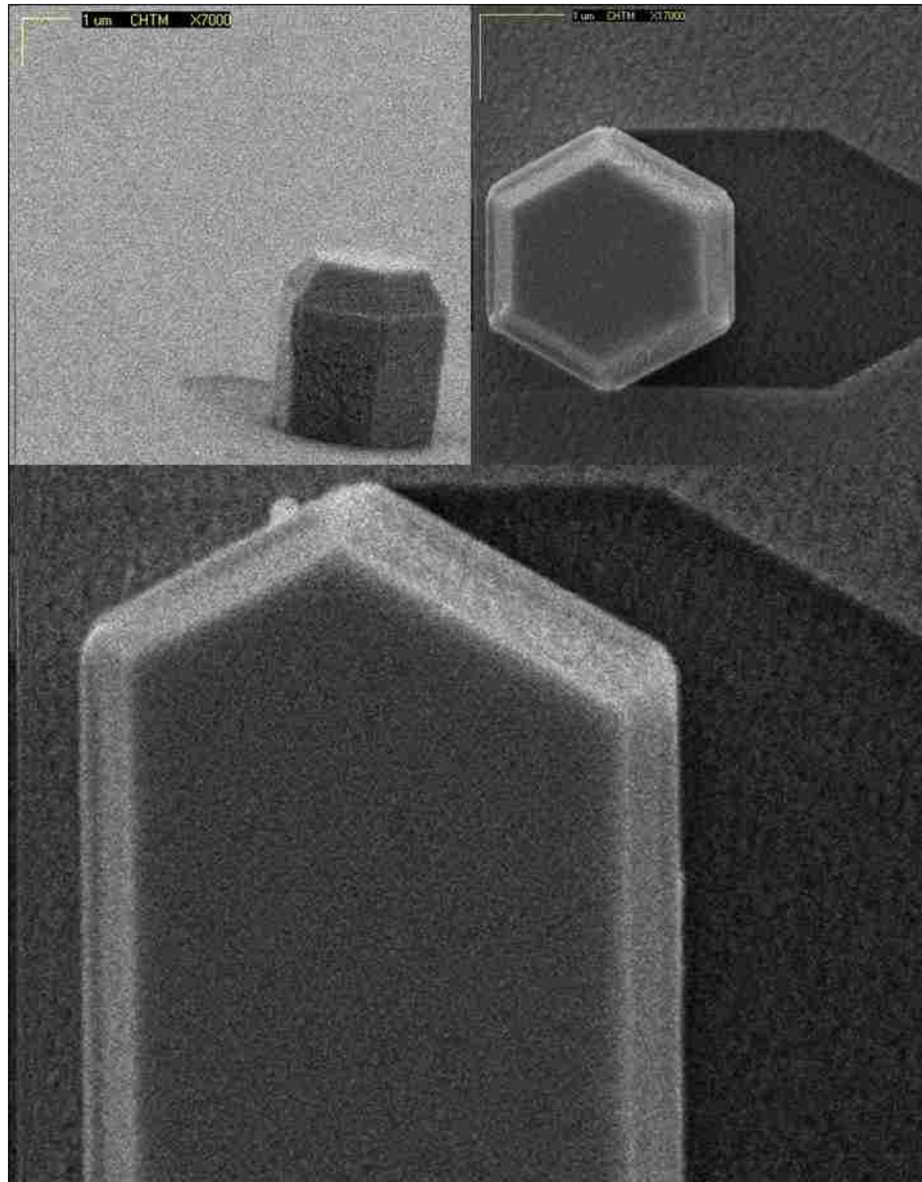


Fig. 6.4 SEM micrographs of coaxial microstructures after a single angled p-metal evaporation run. The shadow is reminiscent of the existing coaxial LED structure.

Step 3: Photolithography: n-metal mask

After the p-metal deposition, the next step was defining the n-contact pad region. The photolithography was carried out in a similar method to that discussed in step 1. A layer of photoresist (AZ4330) was spun coated on the wafer, in a similar method to that discussed in step 1 and the sample was soft baked on the hotplate set at 90°C for about

2min. Following this, the sample was then exposed to ultraviolet light in the Karl Suss MJB-3 mask aligner. Once again the nanowire coaxial LEDs used the Nichia's GaN LED process n-metal mask, while the microstructured LEDs used the COLED mask3 (n-metal mask) that was illustrated pictographically in Fig. 6.2(c). In both the cases, the masks were aligned to the previously used pattern that defined the p-metal regions. After the exposure, the sample was immersed in the 1:4 diluted AZ400K developer solution for about 70-80 sec to develop the n-side contact pattern.

Step 4: Inductively coupled plasma (ICP) etching

After defining the n-contact pattern, the sample was loaded in the PlasmaTherm ICP etcher to etch the dielectric layer and to expose the n-GaN layer underneath it, as illustrated in Fig. 6.1. ICP etching was chosen over other etching techniques because of two important reasons. One of the reasons is because dry etching is capable of producing anisotropic vertical etch profiles with good repeatability that was required for reliable pattern transfer. The other reason is due to the fact that during the growth of AlGaN shell around the GaN core, it was pointed out in section 5.1.2 that there was a layer of polycrystalline AlGaN that was deposited on the growth dielectric. Thus, the only dry etching technique that was found to be suitable was the ICP etch technique.

The sample was attached to a 4-inch double side polished sapphire wafer using mung, silver based chemical glue material designed for high vacuum applications. After that, the sapphire wafer was loaded into the ICP loading chamber and the chamber was pumped to a sub-atmospheric pressure range to facilitate the wafer transfer from the loading chamber to the etching chamber through a load lock mechanism. After the

sample attached to the 4-inch sapphire was loaded into the etching chamber, the chamber was pumped to a base pressure. The PlasmaTherm ICP consists of two independent power supplies, one capable of controlling the power for the plasma, while the other to set up the DC bias between the wafer substrate and the ionized gas molecules during the etching process. The ICP power was a radiofrequency power source operating at 2 Mhz, while the second radiofrequency power source to setup the DC bias operates at 13.56 Mhz. A chloride based etch chemistry was used to etch features in the coaxial LED samples. The ICP power was fixed at 500W and the DC bias power was fixed around 50W. The chlorine (Cl_2) gas flow was fixed at 20sccm and a little bit of inert gas (5sccm of argon (Ar)) was also added to the etch chemistry. The temperature was maintained at 25°C and the chamber pressure during the etching was maintained at 5mtorr. Under 50W of DC bias power, the DC bias voltage obtained was around 140-160V. Fig. 6.5 shows the SEM images of etch profiles obtained by 2min and 5min of etching of the coaxial LED samples under the above conditions in the ICP etcher.

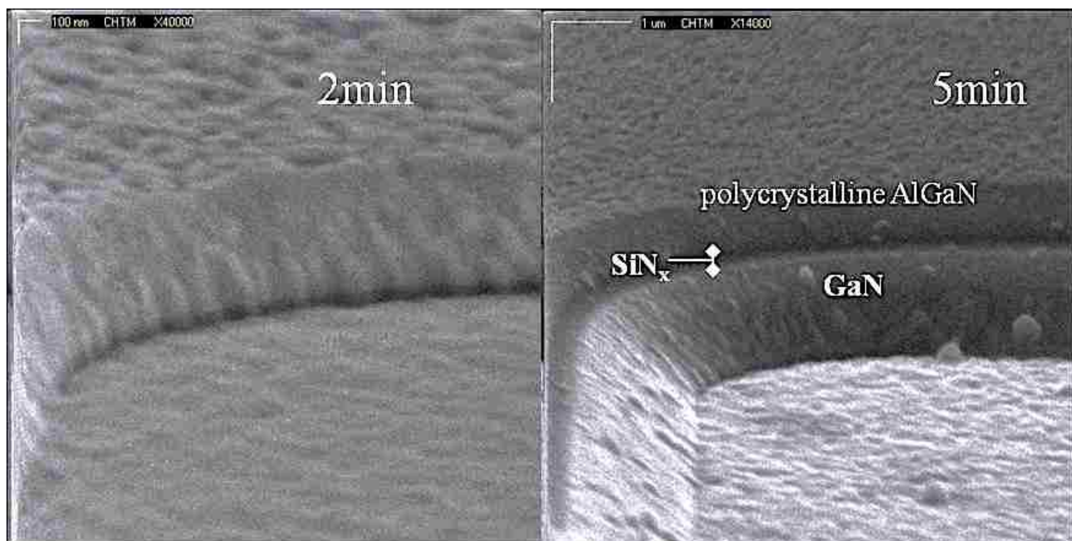


Fig. 6.5 SEM images of a coaxial LED sample etched using the ICP for 2min and 5min respectively

Step 5: Deposition of n-metal by e-beam evaporation

After the ICP etching of the coaxial LED sample, the next step in the fabrication of the LED was the deposition of the n-metal layers. The sample was loaded into the e-beam evaporator in the conventional manner, pictographically illustrated in Fig. 6.3(a), and the chamber was pumped down until a base pressure of 2×10^{-6}torr was reached. The e-beam metal evaporation was initiated and the n-metal layers (25nm titanium/ 100nm aluminum/ 50nm nickel/ 100nm gold) were evaporated on the samples. After the metal evaporation, the sample was removed from the chamber and was immersed in acetone for 1 hour. Following this, the acetone spray gun was used to liftoff the photoresist and the metal. The sample was then cleaned with IPA and blown dry with nitrogen (N_2) gas.

Step 6: Thermal annealing of metal layers

After this, the sample was loaded into the rapid thermal annealer (blue RTA) in order to anneal the deposited metal layers with the semiconductor. The sample was annealed in N_2 atmosphere at 550°C for 15 min. The sample was then taken out of the RTA and was ready for characterization.

6.2 Process 1.2: Non-liftoff based p-metal process

The non-liftoff based p-metal process is pictographically illustrated in Fig. 6.6. This process is similar to the liftoff based p-metal process, except for the patterning of the p-metal layers. This process was employed for the microstructured coaxial LED samples using the COLED mask set. The process steps are illustrated in the following sub-sections.

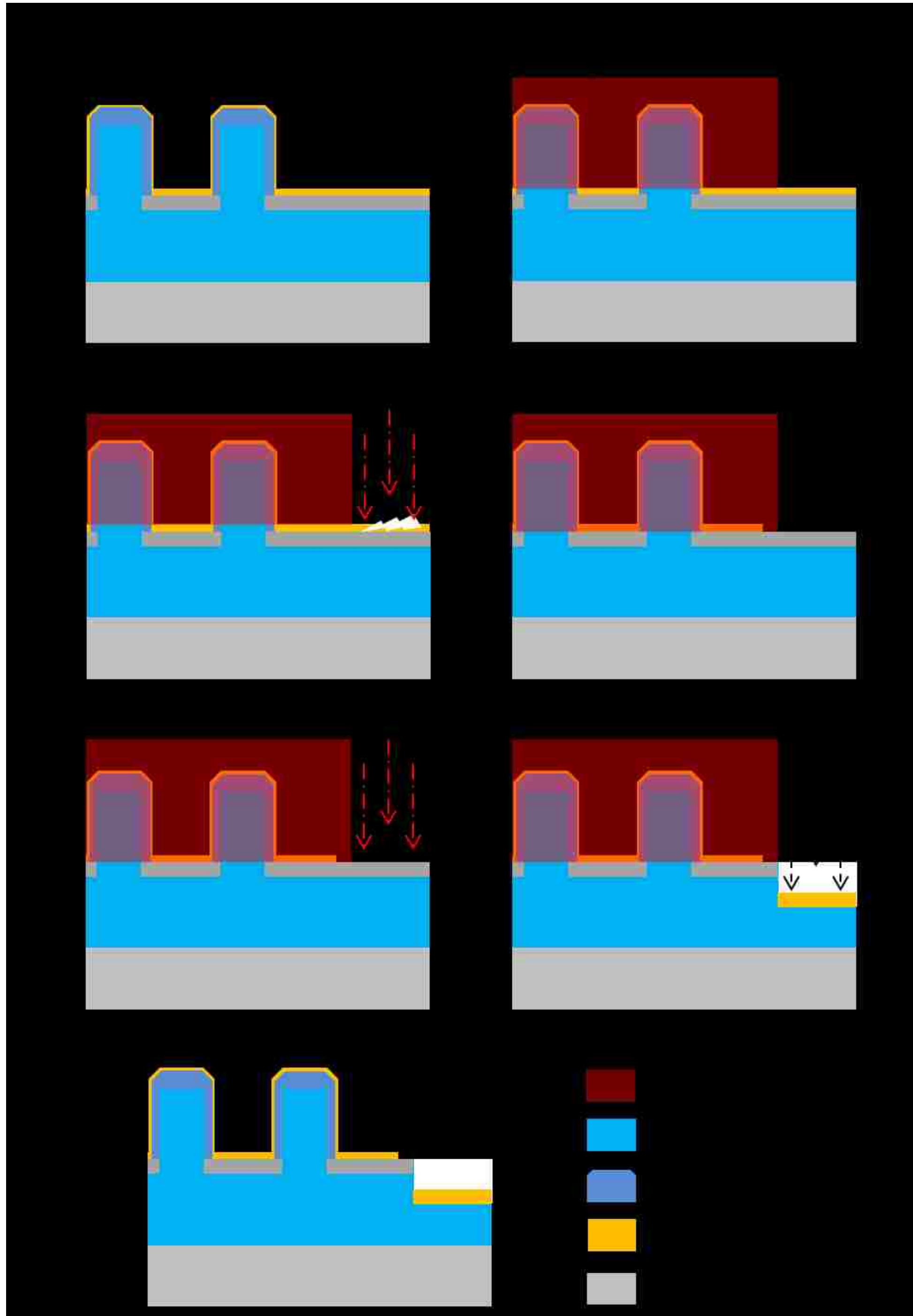


Fig. 6.6 The schematic illustration of the steps involved in coaxial LED process 1.2 (non-liftoff based p-metal process)

Step 1: Angled e-beam evaporation of p-metal layers

The sample, after the growth of coaxial GaN based structures, was first cleaned in acetone, and followed by a cleaning in IPA and blown dry using N_2 gas. After cleaning, the sample was loaded into the metal evaporator in the non-conventional manner highlighted in Fig. 6.3(b) and the chamber was allowed to reach a pressure of 2×10^{-6}torr. The p-metal layers were then evaporated on the sample and then the sample was removed from the chamber in order to change the position of the sample on the carrier for the second angled evaporation. After the four angled evaporation runs, the sample was unloaded from the metal evaporator chamber.

Step 2: Patterning of p-metal side: Acid based wet etch

After the p-metal layers were evaporated on the sample, the LED region was defined on the sample using the bright field version of the COLED mask2 (p-metal mask). The bright field COLED mask2 is transparent all over, except the regions highlighted by the golden 500μm by 500μm square structure in Fig. 6.2(b). Prior to the photoresist spin coating, the sample was cleaned with acetone and IPA, followed by blowing dry using N_2 gas. This was followed by spin-coating of the sample with AZ4330 and then placed on the hot plate set at 90°C for 2min for soft baking. This was followed by photolithography using the bright field COLED mask2 similar to the method described in section 5.2.1. After the exposure, the sample was immersed in a diluted AZ400K (1:4) developer solution.

After the photolithography, the sample was then treated with an acid based wet etch solution to pattern the LED p-side contact metal layer. The metal layers exposed to

the etch solution are etched, while the metal layer under the photoresist remains unetched. The etch chemical used was aqua regia solution, which was a combination of 1 part of nitric acid (HNO_3), 3 parts of hydrochloric acid (HCl) and 10 parts of water (H_2O). This etch was first performed at room temperature with little success. However, upon raising the temperature of the solution to about 50^oC, the etch rate of the metal improved considerably. For the metal layers (two angled metal evaporation runs) with 10nm of Ni and 5nm of Au per run, under the etch conditions mentioned above, an etch time of 45-50 sec was recorded. In most cases, a little bit of over etch along the edges of the p-metal pattern was observed because of the isotropic nature of the chemical etch. Fig. 6.7 shows the optical microscope images of two samples etched for 35 sec (a) and 45 sec (b), respectively under the above mentioned etch conditions. It is possible to notice left over metal particles in the sample etched for 35sec, while the sample etched for 45 sec was clean, with a little bit of undercut along the edges of the growth pattern. This was thus considered the optimal condition to etch the metal layers.

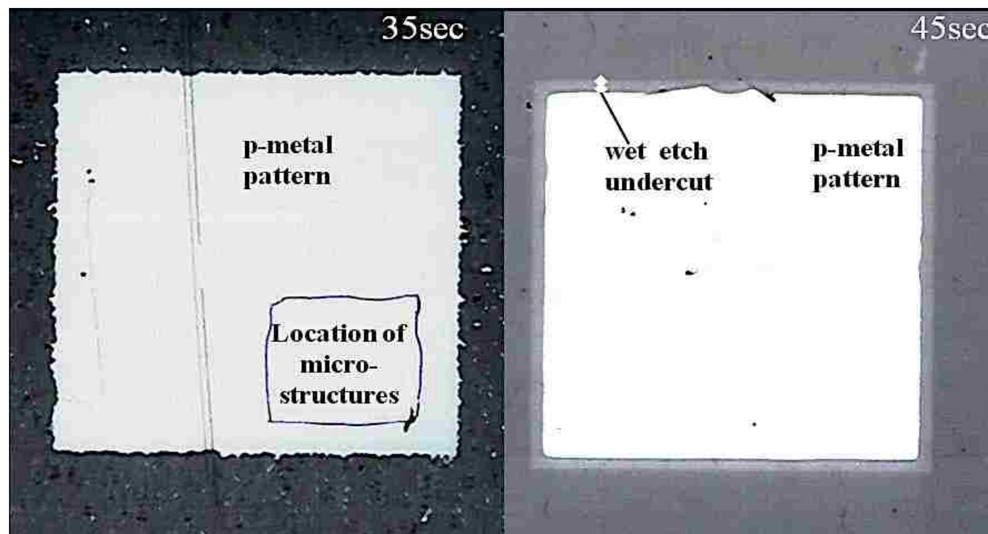


Fig. 6.7 The optical microscope images of test structures etched with aqua regia for 35sec and 45sec, respectively

The remaining steps (step#3, 4, 5 and 6) of the process1.2 are exactly similar to what was discussed in the liftoff process (process 1.1).

6.3 Estimation of dielectric thickness for coaxial LED based on GaN

The coaxial LED architecture was introduced in section 1.2 of chapter 1. Fig. 6.8 shows the cross-section of the coaxial LED. It is clear that the dielectric layer, in addition to serving for the growth aperture needs to be thick enough to isolate the p-contact and the n-contact metal regions shown in Fig. 6.8 to prevent the flow of leakage current through the dielectric. A study was then conducted to estimate the minimum thickness of dielectric required to reduce the leakage current through the dielectric SiN_x isolation layer.

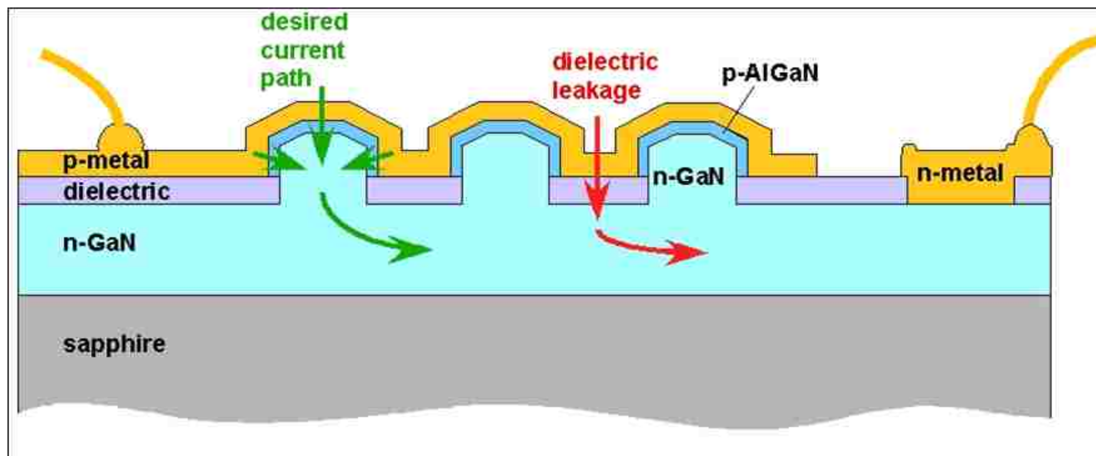


Fig. 6.8 The cross-section of the coaxial LED showing the desired current path and a possible leakage path through the growth dielectric layer.

The test structure to estimate the minimum thickness of growth dielectric was processed in a method similar to the coaxial LED liftoff based p-metal fabrication process illustrated in Fig. 6.1. The growth dielectric (SiN_x) of varying thicknesses was deposited using plasma enhanced chemical vapor deposition (PECVD) technique on n^+GaN, which was grown on sapphire using MOVPE growth discussed in section 4.1.1 of

chapter 4. After that, photolithography was performed using mask 2 of the COLED to expose a 500μm by 500μm square region on the SiNx dielectric. Following this, the metals for the p-contact (50nm Ni /50nm Au) were deposited in the e-beam metal evaporator on each of the samples at the same time using the conventional loading procedure illustrated in Fig. 6.3(a). After the metal evaporation, the samples were soaked in acetone and liftoff was performed, thereby defining the p-contact region. Following this, photolithography was performed using mask 3 of the COLED to expose the L-shaped n-contact region on the dielectric. This was then followed by a reactive ion etch (RIE) in order to etch the SiN_x to expose the underlying n^+-GaN layer. After this, the n-metal stack (25nm Ti/ 100nm Al/ 50nm Ni/ 100nm Au) was evaporated on the exposed n^+GaN region in the e-beam metal evaporator, following which the samples were once again soaked in acetone and liftoff was carried out to define the n-contact region. The metal deposition was then followed by a thermal anneal in N_2 atmosphere at 550°C for 15 min.

After the processing, the dielectric test structures were then subjected to an electrical current leakage test in the characterization lab. A voltage was applied across the p and n contact metals and the electric current flowing through the dielectric was measured using the Keithley 2400 source meter interfaced via labview to the computer. The breakdown voltage of the growth dielectric (SiN_x) under consideration in this thesis was defined as the voltage at which the measured current was 10nA. The breakdown voltage was then plotted, as a function of the thickness of the growth dielectric to estimate the minimum thickness of dielectric layer required for a leakage current of 10nA through the dielectric layer, as shown in Fig. 6.9.

It was anticipated that the maximum operating voltage of the LED would be around 10V. Thus, the 60nm thick SiN_x was considered optimum growth dielectric thickness.

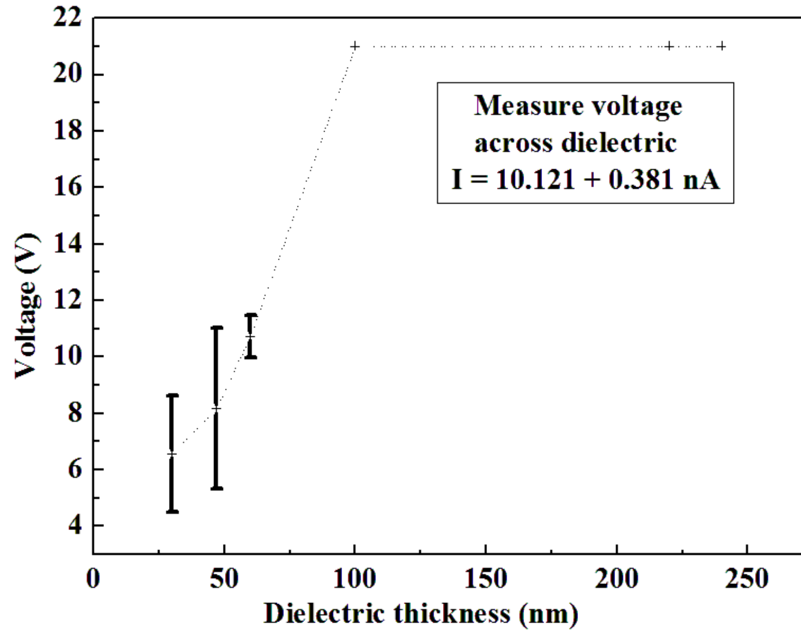


Fig. 6.9 The breakdown voltage plotted as a function of dielectric thickness. The breakdown voltage is defined for a current = 10nA. For dielectric thicknesses above 100nm, the voltage source meter limit (21V) was reached.

6.4 Elimination of stray growth on growth dielectric

In the previous section, the study of the estimation of growth dielectric thickness was discussed. Another important aspect of selective area growth is the elimination of stray growth from the surface of the growth dielectric. In previous work, the growth substrate with growth dielectric (SiNx) was patterned all over the wafer using interferometric lithography. Under these conditions, the growth of GaN was preferentially initiated only in the patterned apertures in the growth dielectric (SiNx). However, when 3D GaN structures were grown in the COLED or the SANG patterns, the growth of GaN was not only observed inside the patterned apertures, but also on the

dielectric layer, in between the grouped growth patterns, as shown in Fig. 6.10(a). A cross-section SEM image across the stray growth on the mask is shown in Fig. 6.10(b). It was observed that the GaN on the growth dielectric was growing through self-created apertures in the growth dielectric. It is still unclear to us as to what the mechanism of the aperture creation was, but it was anticipated that any 3D GaN growth on the dielectric layer would be deteriorating to the performance of the coaxial LED.

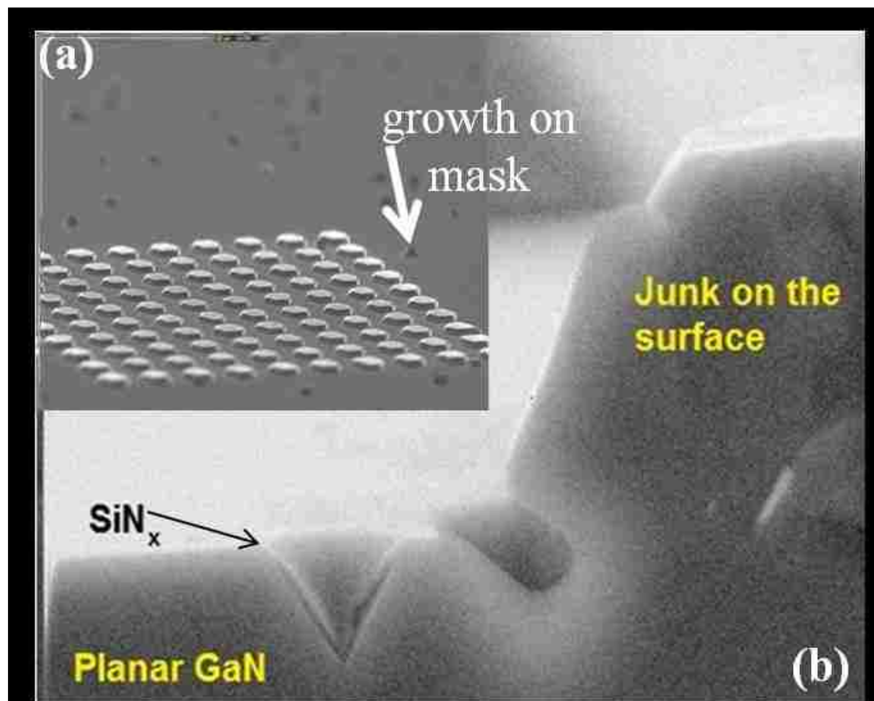


Fig. 6.10 The SEM images of coaxial LEDs with (a) showing the growth of stray 3D GaN islands on the dielectric and (b) showing the cross-section of the 3D GaN islands.

A study was conducted to investigate the effects of the stray growth of GaN on the growth dielectric (SiNx). Planar GaN doped with silicon (n^+GaN) was grown on 2" sapphire wafers using regular MOVPE growth as described in section 4.1.1 of chapter 4. Following this, SiN_x of varying thicknesses were grown on the wafers using PECVD technique described in section 4.1.2 of chapter 4. These wafers were then introduced into

the MOVPE growth reactor and the 3D GaN growth recipe described in Fig. 4.10 of section 4.1.4 of chapter 4 was initiated for about 100 cycles. Upon examination of the samples under the SEM after the growth, GaN islands were observed on the growth dielectric. After this, these wafers were processed in a similar fabrication process as the coaxial LEDs described in the previous sections and illustrated in Fig. 6.1 to produce dielectric test structures.

These dielectric test structures were then subjected to an electrical leakage test, similar to the test structures described in the earlier section. The current (I) versus voltage (V) characteristic of one of the representative dielectric test structures is shown in Fig. 6.11(a). The current-voltage characteristic is observed to be nearly symmetric and ohmic, which confirmed that the 3D GaN islands were indeed growing through the growth dielectric. A representative I-V characteristic of the same test structure fabricated on another piece of the same wafer, not subjected to the growth recipe in the reactor, is also analyzed separately. The difference in the magnitude of electric current (I) between the two samples can be clearly observed in the log-linear plot comparison of the sample before growth and of the sample after growth, shown in Fig. 6.11(b), which is indicative of an alternate leakage path apart from the current through the dielectric.

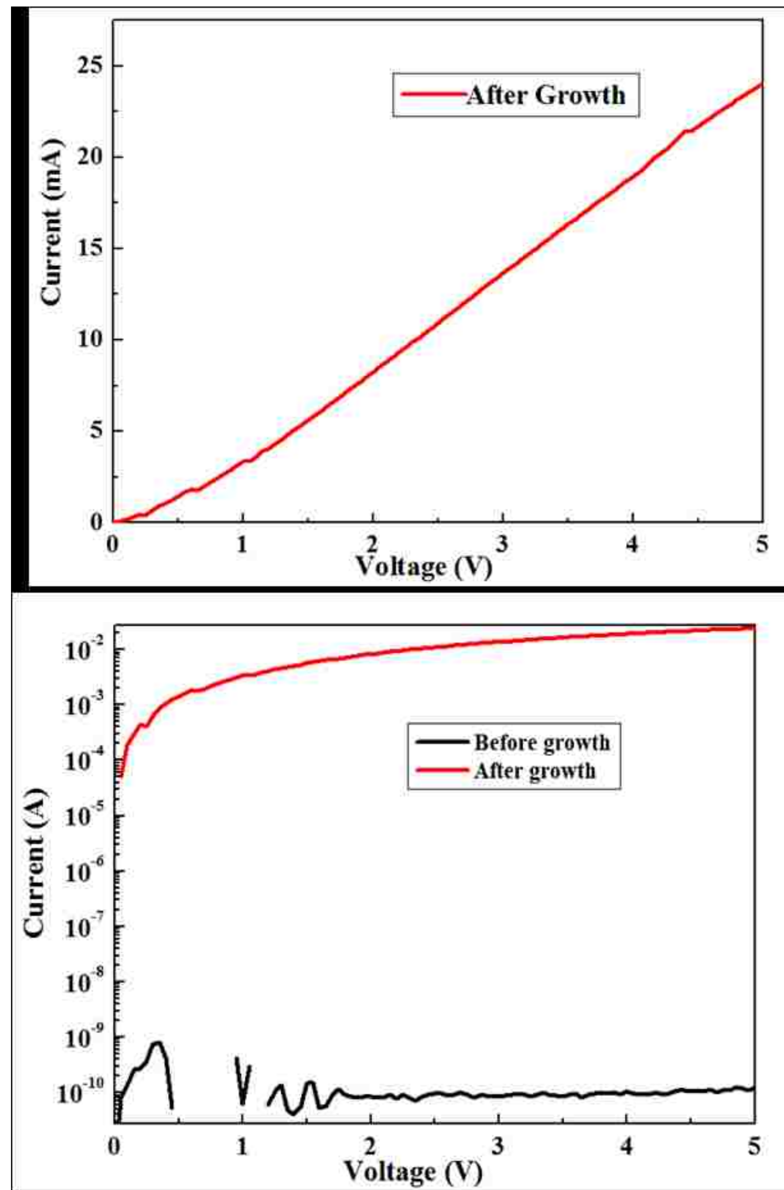


Fig. 6.11 The current-voltage characteristics of dielectric test structures (a) fabricated on test samples that were subjected to growth conditions and (b) shows the I-V characteristics comparison of representative samples, one subjected and one not subjected to pulsed MOVPE growth conditions

Fig. 6.12(a) (similar to Fig. 6.9) shows the log plot of the measured voltage (V) as a linear function of different thicknesses of growth dielectric at a given electric current magnitude of 100nA. These measurements were performed on the samples that had 3D GaN islands on the dielectric, grown as a result of them being subjected to the 3D GaN growth conditions. The log-linear plot shown in Fig. 6.12(b) shows the combination of

plots shown in Fig. 6.9 and Fig. 6.12(a), respectively. It can be observed that even at 100nA (10 times the current under consideration in Fig. 6.9), the measured voltage across the dielectric, in case of the samples subjected to the growth conditions, were much lower than for the samples that were not subjected to the growth conditions.

The dielectric layer was also modified, in order to check if this effect was a material related effect. A composite dielectric was deposited on two bare n^+GaN on sapphire wafers. This composite dielectric consisted of a 100nm thick SiN_x on top of a 140nm SiO_2, the total dielectric thickness measuring about 240nm. The dielectric layer was deposited using PECVD with the respective source gases, which was discussed in section 4.1.2 of chapter 4. Once again, one of these wafers was introduced into the growth reactor and subjected to the 3D GaN growth conditions, while another sample of the same was not. After this, both these samples were processed for dielectric test structure testing using the COLED masks 2 and 3, respectively. The dielectric test structures were then subjected to the electrical leakage test. It was observed once again that for the sample subjected through the growth conditions that the voltage across the dielectric layer was very low, when a 100nA current was passed through the test structure, in comparison with that measured at 10nA on the sample that was not subjected to the growth conditions. This comparison has also been highlighted in Fig. 6.12(b). This proved that the observed stray GaN 3D island growth on the dielectric would be anticipated even on other dielectric materials.

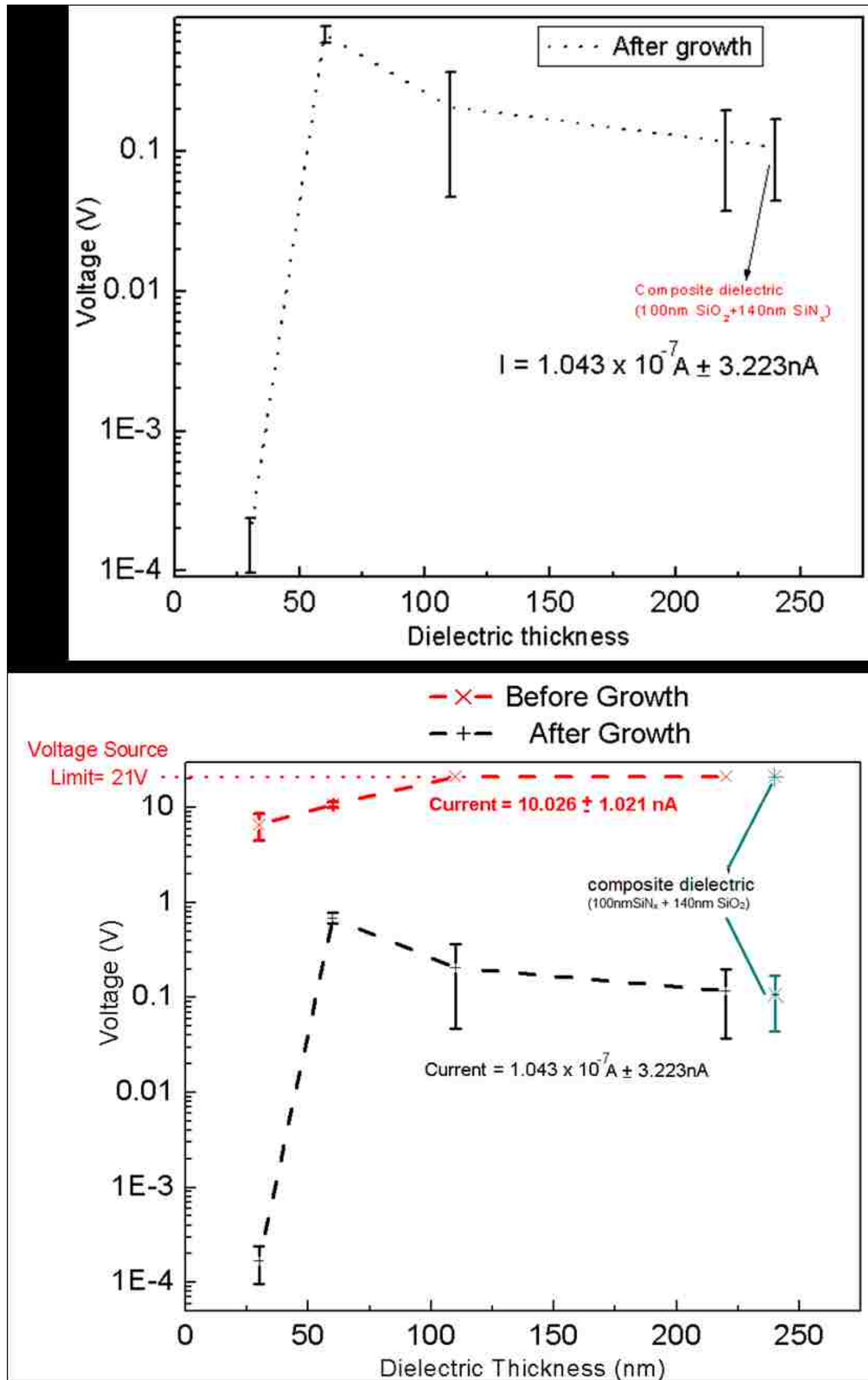


Fig. 6.12 (a) The voltage across the dielectric test structures at a current of 0.1µA plotted on a log scale and (b) the combination of Fig. 9 and Fig. 12(a) on the same log-linear plot showing the difference in breakdown voltage, as defined in section 6.3.

Hence, it was concluded that elimination of the stray GaN island growth on the mask was important to the successful functioning of the coaxial LED. This was achieved by a simple, yet innovative technique of capturing excess growth nutrients in a region near the coaxial LED group patterns. This region was referred to as the growth sink region. The growth sink region was an aperture region created near the coaxial LED group aperture patterns. In comparison to the original hole and line aperture sizes of the LED group patterns, the sink aperture patterns had to be much larger in size, in order to be in a position to capture the excess growth nutrients and prevent nucleation on the growth dielectric.

The preliminary demonstration of the growth sink was performed using the already available COLED mask set. The patterning of the growth dielectric for the coaxial LED features was already discussed in section 4.1 of chapter 4. After etching through the growth dielectric (SiN_x) to define the group circular and line aperture patterns, a second lithography step was added. The lithography steps are exactly the same as described in section 4.1.3 of chapter 4, with the exception of using the COLED mask3 (n-metal mask), instead of mask1 (growth mask). After the wafer was coated with the HMDS and the photoresist, the mask3 was used during the exposure using the MJB-3 aligner. This mask3 was aligned with the mask1 lithography patterning that was already carried out on the wafer using the alignment markers on the masks. After this, the wafers were developed and the reactive ion etching of the dielectric was carried out, in a similar method illustrated in section 4.1.4 of chapter 4. Following this, the substrates were cleaned in piranha and then loaded into the growth reactor for the 3D GaN growth. The optical microscope picture of coaxial LED grown and fabricated in the aperture patterns,

with the sink region is shown in Fig. 6.13(a) and without the sink region is shown in Fig. 6.13(b). Fig. 6.13(c) shows the GaN microstructures grown on the growth template with a growth sink. The mask region on the samples with the sink looks clean, while the mask region on the samples without the sink is covered with GaN islands nucleated during 3D GaN growth during MOVPE.

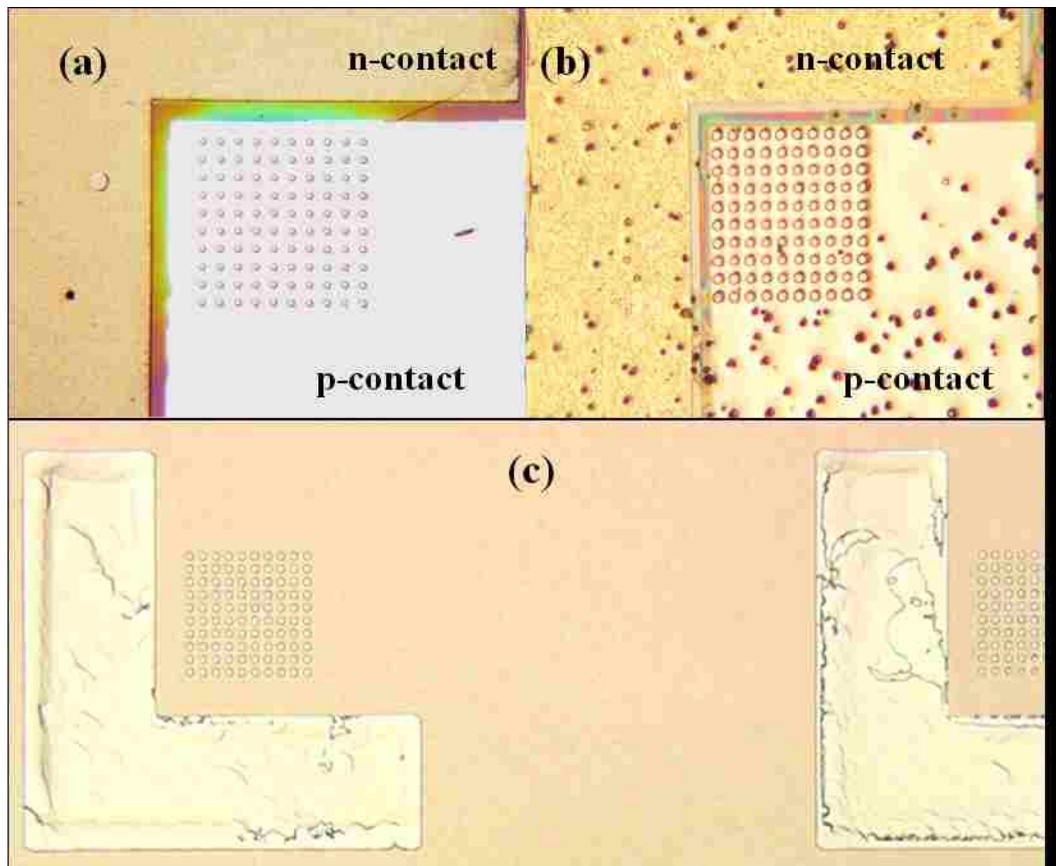


Fig. 6.13 (a) Coaxial LED fabricated on growth patterns with sink shown in (c), in comparison to (b) that shows coaxial LED fabricated on growth patterns without sink. The growth mask is clean in (c), devoid of GaN islands, in comparison to the samples grown on patterns without sink.

The current leakage test was then performed on the dielectric layer of the 3D grown GaN with the sink, in a similar method to that performed on the earlier dielectric test structures. Fig. 6.14 shows the log-linear plot of the dielectric test structures

fabricated, which is the same graph as shown in Fig. 6.12(b) with the additional breakdown voltage data point of the sample with the growth sink shown in Fig. 6.13 (a). This sample (dielectric thickness = 45nm) showed a breakdown voltage (as defined in section 6.3) of around 3.2V for 10nA current. Hence, the sink region was successful in improving the breakdown voltage of the growth dielectric by the elimination of the stray 3D GaN growth on the dielectric layer. However, the quality of the dielectric layer did show some deterioration after going through the growth process in the reactor chamber. This deterioration was observed in terms of the breakdown voltage reduction of the GaN sample with a 45nm thick SiNx layer on it.

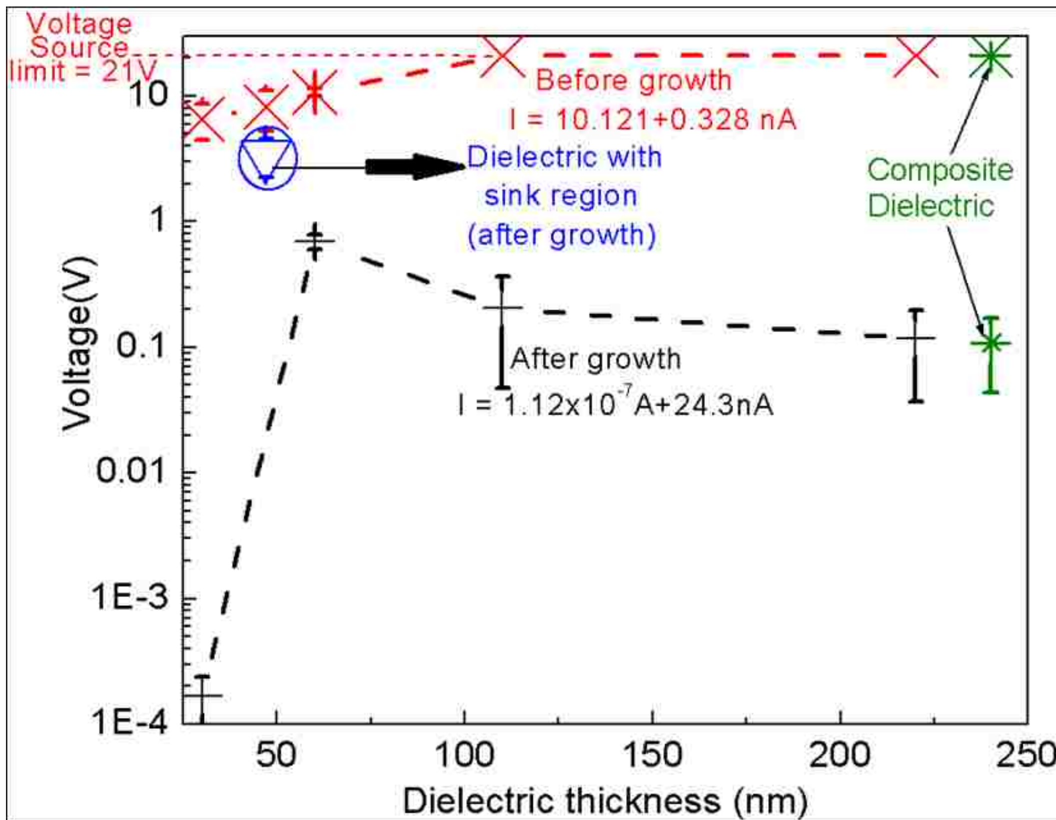


Fig. 6.14 The breakdown voltage plotted for dielectric test structures fabricated on four different samples, 1) SiNx on GaN, 2) SiNx on GaN subjected to pulsed MOVPE growth conditions, 3) composite dielectric (140nm SiNx on 110nm SiO2) subjected to both the cases mentioned in 1) and 2) and 4) SiNx on GaN patterned with growth sink, subjected to MOVPE growth conditions.

6.5 Elimination of current leakage through gaps between microstructures

In the previous sections, the microelectronic fabrication of coaxial LEDs was discussed. After the fabrication, the LEDs were tested to analyze the current (*I*) versus voltage (*V*) characteristics. In the initial stages of testing, *I* vs. *V* characteristics of the fabricated diodes resembled that of either a resistor or a leaky schottky diode. One of the elements of current leakage, which was discussed in section 6.4, was occurring through the 3D GaN islands that were grown unintentionally on the growth mask. This leakage current was observed in *I* vs. *V* characteristics as a resistor. It was discussed in section 6.4 as to how this leakage current could be eliminated. The other current leakage path that was investigated was found to occur through the incomplete filling of the growth apertures by the nano/microstructures. This leakage mechanism is pictographically illustrated in Fig. 6.15.

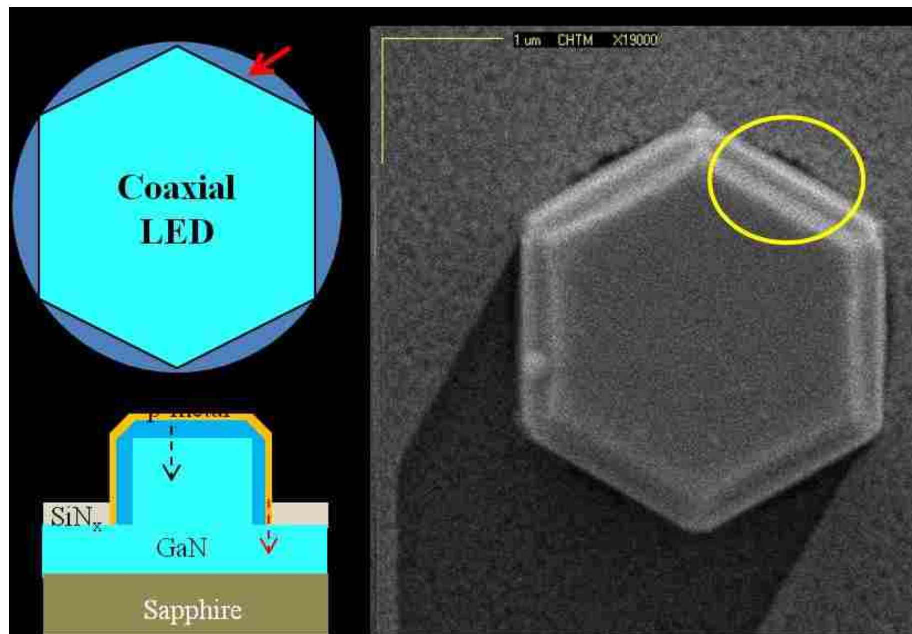


Fig. 6.15 The current leakage mechanism observed in coaxial LEDs with insufficient lateral growth to fill the gaps between the circular apertures and the coaxial structures with regular hexagonal cross-section. The black arrow in the LED schematic represents the desired current direction and red arrow indicates the direction of leakage current observed.

The leakage mechanism shown above was bound to occur in the coaxial structures that had insufficient lateral growth to cover the gaps between the coaxial microstructure and the growth apertures. After the growth, the LEDs were fabricated using the process steps highlighted in process 1.1. During the p-metal layer deposition, there is a possibility of the metal layers filling into these gaps and creating an alternate electrical path. The current-voltage characteristics obtained from these LEDs had a substantial amount of leakage current flowing, both in the forward and the reverse bias voltage conditions, as shown in the representative I–V curve of Fig. 6.16(a).

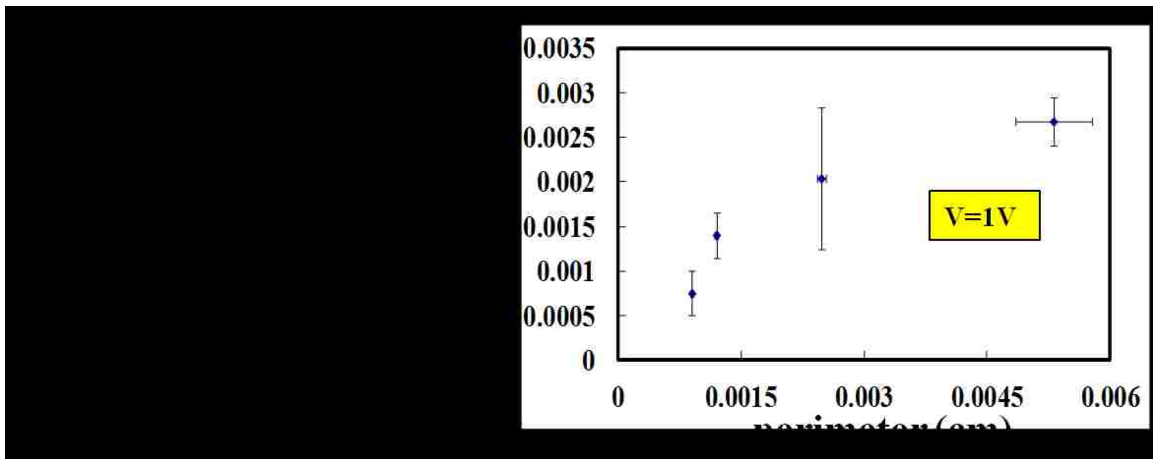


Fig. 6.16 (a) shows a representative I vs. V characteristic of a coaxial LED fabricated, showing the current leakage through the gaps mentioned in Fig. 6.15 and (b) shows the plot of the current measured at V=1V, as a function of the perimeter of different sized coaxial wire microstructured devices

It is possible to conclude that the area of the gap in between the 3D structures would proportionally increase with the size of the growth apertures, in case of the wire structures. Thus, at a given bias voltage applied to the LED, the leakage current measured would also proportionally increase with the increase in growth aperture size. Fig. 6.16(b) shows the plot of the current flowing through the devices as a function of the microstructure (wire) perimeter (in cm), for a given applied bias voltage (1V).

Hence, it was important to eliminate this alternate path for electrical conduction. Fig. 6.17 shows four possible methods, by which these gaps can be isolated from the p-metal layers.

The method involving the use of spin on dielectric was implemented and the LED fabricated using this method was tested and the characterization results are presented in the succeeding section. The use of hexagonal growth apertures, instead of circular apertures was demonstrated to grow 3D GaN structures, discussed in section 4.3 of chapter 4. The details of the other mentioned methods are discussed in chapter 7, as part of future work.

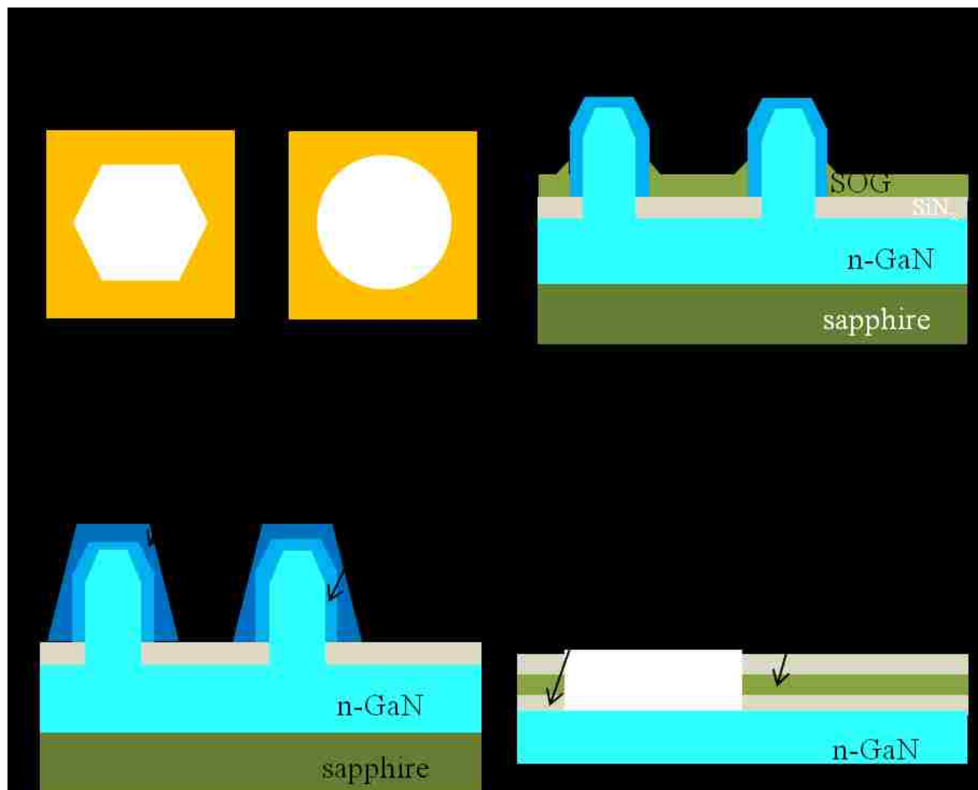


Fig. 6.17 The four possible methods of eliminating the current leakage highlighted in Fig. 15 is described. (1) The use of hexagonal growth apertures instead of circular, (2) use of spin-on glass, (3) additional p-GaN pyramidal outer shell to cover the gaps and (4) LOCOS.

6.6 Characterization of pAlGaN-nGaN coaxial LEDs

The growth of the coaxial nanowire and microstructured pAlGaN-nGaN LEDs was discussed in section 5.2 of chapter 5. The LEDs were processed using the liftoff technique discussed in section 6.1 of this chapter. Prior to the processing, a layer of spin-on dielectric was spun on the sample to fill in the gaps between the coaxial structures and growth apertures (discussed in the earlier section).

6.6.1 Processing of coaxial LED using spin on dielectric

The spin-on dielectric (also known as spin-on glass (SOG)) used for the LEDs was Honeywell ACCUGLASS T-512B [ref], which is chemically designed to fill narrow, high aspect area gaps with precision. Prior to the spinning of SOG, the sample wafer was cleaned with acetone and IPA and blown dry. After that, the sample was placed on the spinner and a layer of SOG was spun on it at 3000rpm for 30 sec. This was followed by anneal in a furnace set at 450°C for 30-45min in nitrogen (N_2) atmosphere.

After the spin coating of SOG, an etch back was performed, so that the coaxial structures could be exposed for the p-metal evaporation. In order to achieve this, the sample was loaded in the reactive ion etcher (RIE) to initiate etching of SOG. The etch chemistry used was similar to etching of silicon nitride (SiN_x), which was discussed in section 4.1.4 of chapter 4. A chamber pressure of 25mtorr was used and oxygen gas (3sccm) and carbon tetra fluoride (30sccm) were introduced into the chamber. After this, the plasma was initiated and the sample was etched for 10min. Fig. 6.18 shows the cross-section of a GaN microstructure surrounded SOG after a 5min etch. Ideally, the sample was etched until the top and some portion of the sidewalls of the device structures were

exposed. After these two steps, the LEDs were fabricated by the methods discussed in process 1.1.

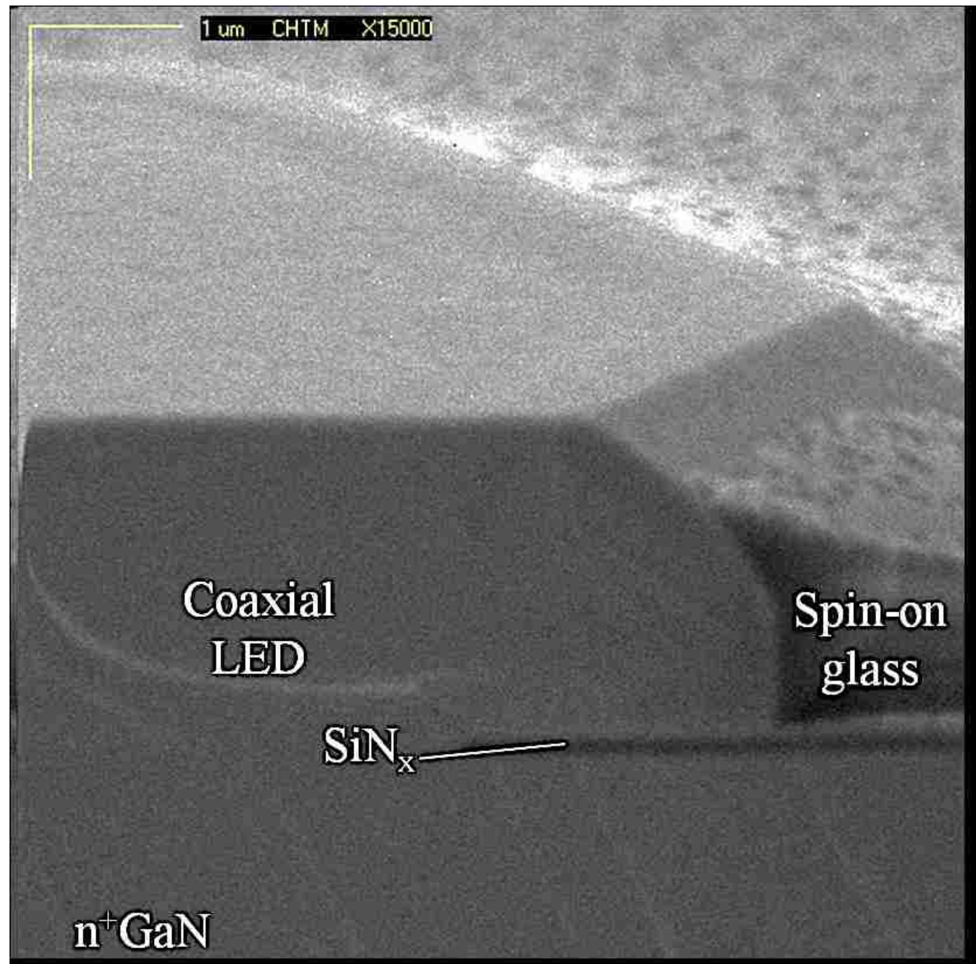
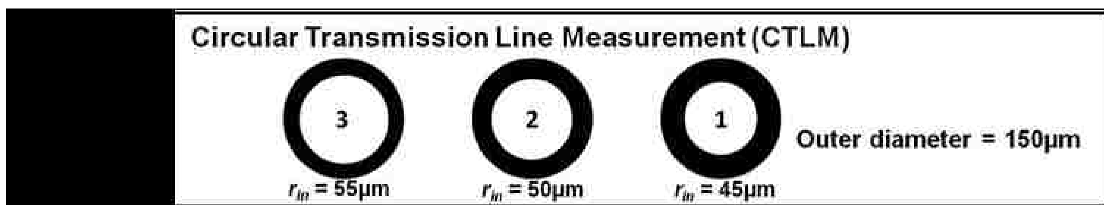


Fig. 6.18 The cross-section SEM image of a coaxial LED sample fabricated with spin-on glass, followed by a 5min etch back to expose the top and a portion of sidewalls of the LED structure

6.6.2 Thin metal layer contacts to p-GaN

To enable light extraction from the top of the coaxial microstructures, thin p-metal contacts were explored. The important properties to be considered for the thin contacts to p-GaN were the ohmic nature and transparency to emitted light from the coaxial LEDs. However, it was difficult to measure the contact resistance on the coaxial microstructures due to the small size of the features to probe and test. Thus, the thin p-

contacts were developed for planar p-GaN films. Circular transmission line models (CTLM), as shown in Fig. 6.19(a) were used to analyze the contact resistivity of the p-type GaN films. A 10nm nickel metal followed by 6nm gold was deposited on the p-GaN. Following this, a non liftoff procedure was used to fabricate the p-metal circular transmission line measurement (CTLM) patterns using wet etch technique of Ni/Au using an aqua regia solution. This was followed by anneal in N_2 atmosphere at 550°C for around 15min. The contacts were nearly ohmic, and further investigation of annealing conditions could improve the ohmic behavior. The current vs. voltage curves of the p-metal CTLM's are shown in Fig. 6.19(b). A 56% transmission was achieved at 327nm wavelength, the spectrum of which is shown in Fig. 6.19(c). The discussions with glo USA personal revealed that they have also used a similar transparent contact approach for their nanowire LEDs. Indium tin oxide (ITO) is deposited by glo as their transparent (~95% transparent at 450nm) p-contact, followed by a non liftoff dry etch process to retain the ITO only on the nanowire LEDs. The use of ITO as a p-contact area is also listed in chapter 7 as part of future work, in regards to the coaxial LEDs process development.



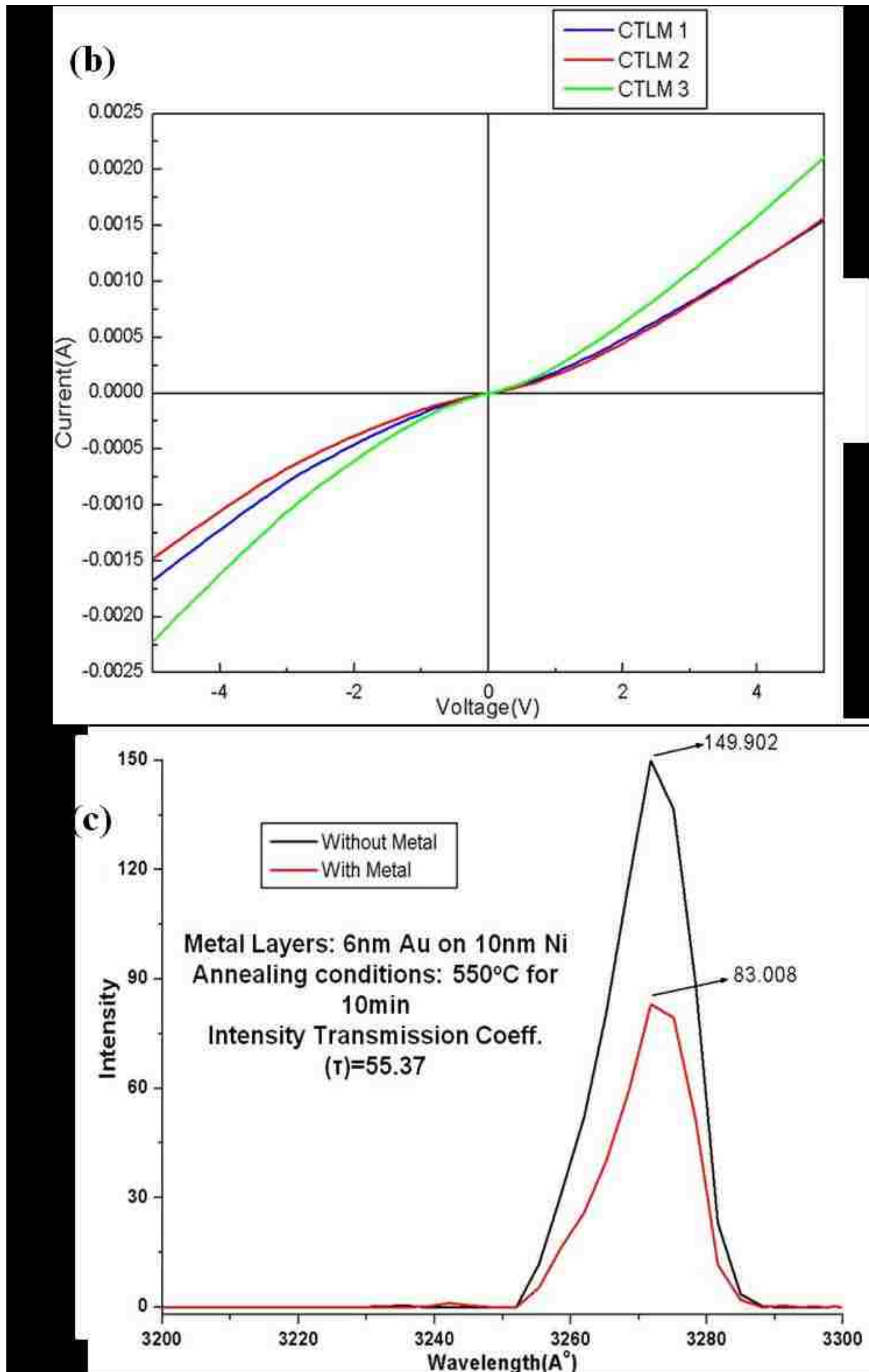


Fig. 6.19 I vs. V characteristics of different circular transmission line model (CTLM) patterns shown in (a), fabricated on p-GaN using thin p-metal layers, is shown in (b). The transmission coefficient calculated at 327nm, of the thin metal layers fabricated on p-GaN on sapphire is shown in (c)

6.6.3 Electrical and optical characterization of coaxial LEDs

The current-voltage characteristics of representative microstructured p-AlGaN/n-GaN wire and wall devices fabricated using SOG are shown in Fig. 6.20.

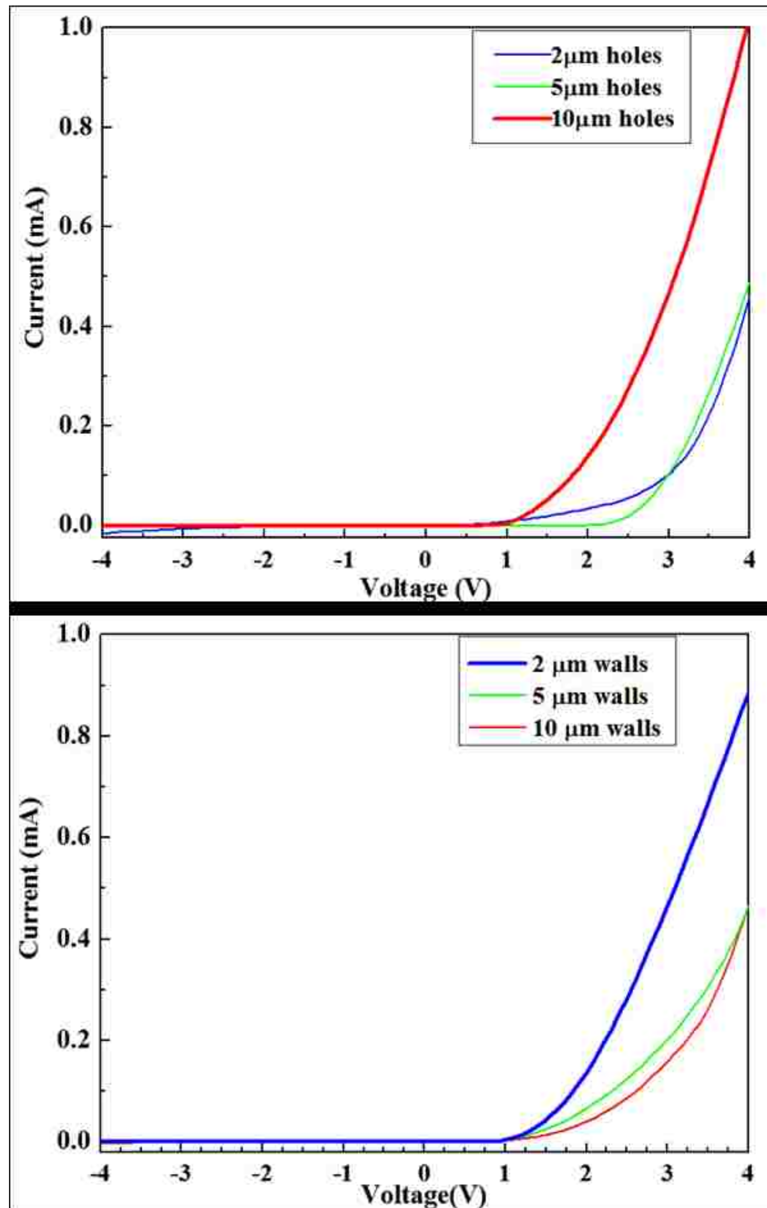


Fig. 6.20 Current vs. voltage characteristic of representative microstructured coaxial LED devices, wires (a) and walls (b) are shown.

The results reported here are far from ideal and we are continuingly trying to improve the performance of the LEDs. Most of the diodes analyzed showed diode like

characteristics with a turn-on voltage between 1.5-4V. Since the band gap of GaN is 3.4eV at room temperature, a turn on voltage around 3V is a reasonable estimate. However, some of the samples were turning on at a lower voltage. Fig. 6.21 shows the equivalent circuit diagram of a real diode, which is a combination of a series resistor and an ideal diode.

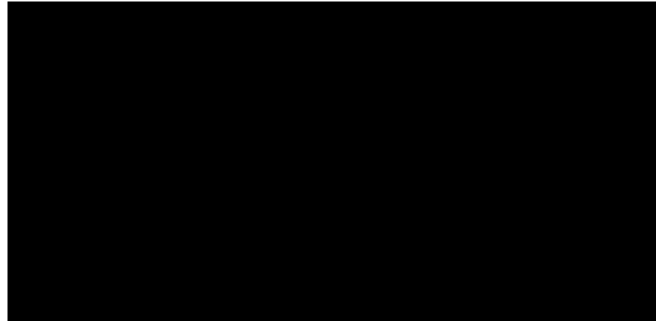


Fig. 6.21 The equivalent circuit of a real diode under consideration in coaxial LEDs

The series resistance in a real diode is a combination of the contact resistances (p and n contact resistance) and the semiconductor resistance (p-GaN, n-GaN and the space charge layer or the active region). The actual bias voltage across the diode (V) as a function of the current (I) can be written as follows:

$$V = IR_s + V_d \qquad \text{-- (1)}$$

where, V_d is the voltage drop across the ideal diode and R_s is the series resistance. The current through an ideal diode can be written in terms of the voltage across it as below,

$$I = I_s(e^{\frac{qV_d}{\eta KT}} - 1) \qquad \text{-- (2)}$$

Hence, from (2), V_d can be written in terms of the current, I as below,

$$V_d = \frac{\eta KT}{q} \log\left(\frac{I+I_s}{I_s}\right) \qquad \text{-- (3)}$$

Hence, from equations (1) and (3), we get,

$$V = IR_s + \frac{\eta KT}{q} \log\left(\frac{I+I_s}{I_s}\right) \quad \text{-- (4)}$$

where, I_s is the reverse saturation current, T is the absolute temperature, k is the Boltzmann constant , q is the electronic charge and η is the ideality factor. Simplified curve fitting using MATLAB was used to determine the unknown parameters in equation (4). The current, I vs. voltage, V data points was available and the temperature was assumed to be 300K. The reverse saturation current for each of the diode curves analyzed was assumed to be the value of current, I at V= -5V. Hence, the unknown parameters to be determined were the series resistance, R_s and the ideality factor, η. Fig. 6.22 shows the non-linear fit (solid line) of one of the representative I vs. V data points (circles), and the fitting parameters (R_s and η) were obtained.

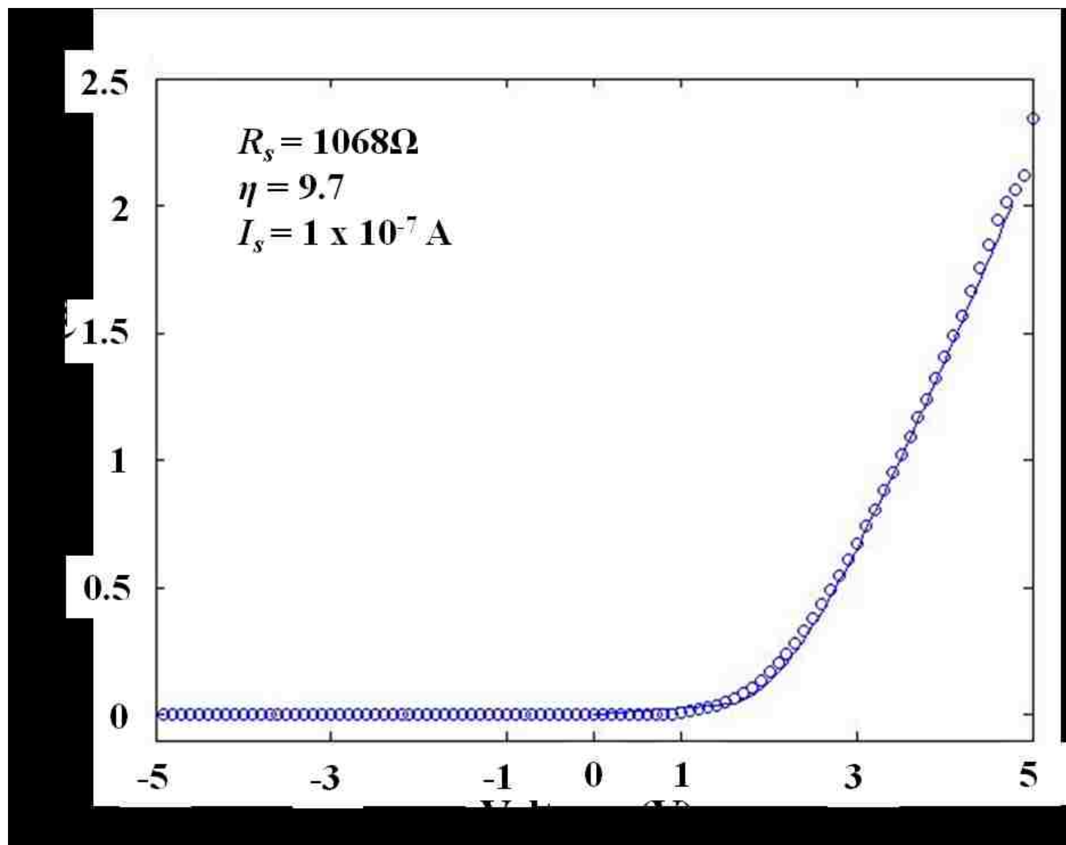


Fig. 6.22 The plot of current vs. voltage data points (o) together with the best fit I vs. V characteristic simulated (solid line) using MATLAB is shown. The parameters calculated are also shown in the plot.

Fig. 6.23 shows the photocurrent measured from some of the representative wall coaxial LEDs as a function of the current (*L* vs. *I* curves) through them. The light emitted from the wire LEDs was weak and it was increasingly difficult to get an *L* vs. *I* curve for the wire devices using a simple silicon detector. The photocurrent magnitude increased with the increase in device current, which is typical of LEDs. The light emitted by the coaxial devices was faint, to even be detected by the USB2000 spectral analyzer for the spectral resolution of the emitted light. One particular LED was successful in emitting enough photons to be successfully resolved by the spectrometer. The spectrum and *I* vs. *V* curve of the particular device is shown in Fig. 6.24.

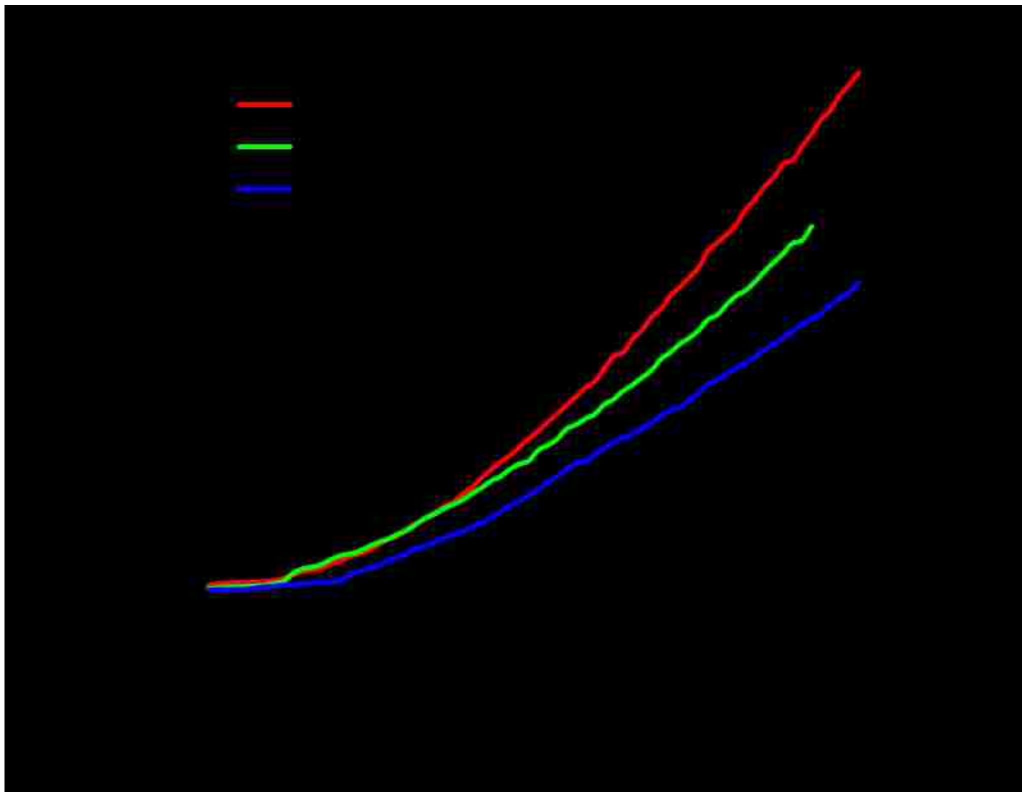


Fig. 6.23 The plot of the photocurrent obtained from the silicon detector used, as a function of the device current, for representative coaxial wall LEDs of different sizes

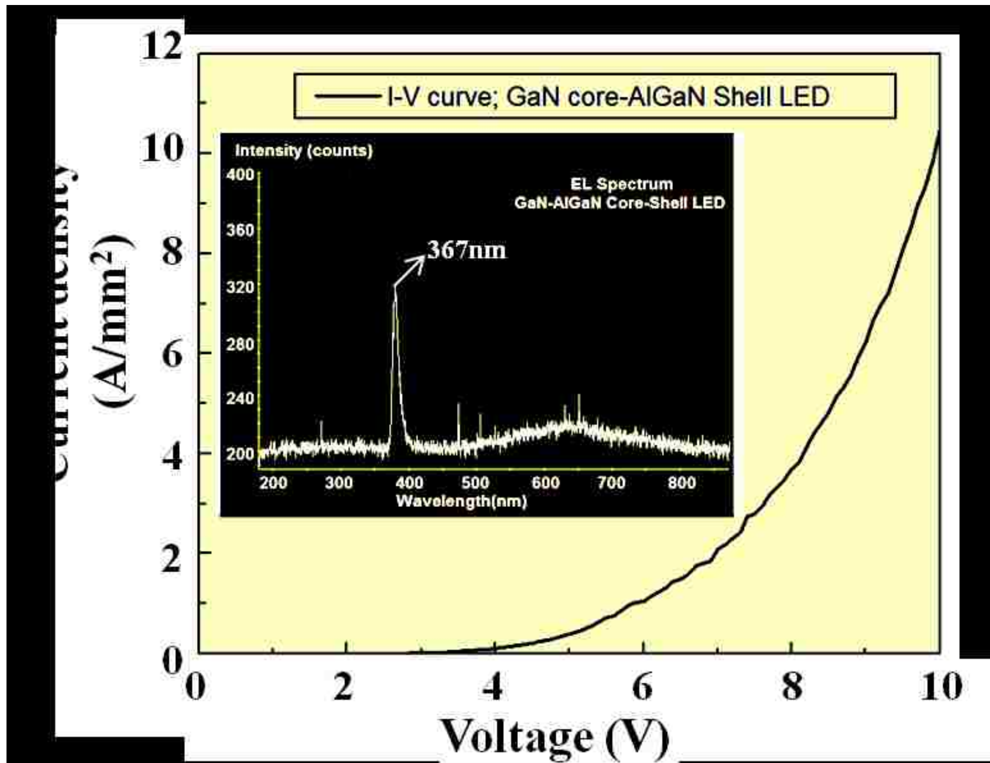


Fig. 6.24 Current vs. voltage characteristic of a 10μmwall device (device#NW104_06_04) and the electroluminescence spectrum (inset image) obtained from the same device.

6.6.4 Results and discussion

The series resistance and ideality factor obtained were pretty high in comparison to LEDs that were reported in [1, 2]. However, an ideality factor, $\eta >> 2$, has been observed frequently for GaN based LEDs [1, 2, 3, 4]. It was shown in [1] that the reason for the high ideality factors were the presence of unipolar heterojunctions and metal-semiconductor junctions, which were behaving as additional rectifying (diode like) centers. In case of the coaxial LEDs, the unipolar junction was absent, but the metal-semiconductor junction was present (metal – p-GaN Schottky junction). Magnesium (Mg) is commonly used as the acceptor dopant in p-type GaN layers. It has been calculated in [7] that the activation energy of the Mg dopant in GaN is larger (E_a = 150meV to 250meV) than most p-type dopants in other III-V semiconductors. It was also

shown in [7] that p-type doping was difficult to achieve in $Al_{0.2}Ga_{0.8}N$. The activation energy, E_a of the acceptor impurities in $Al_xGa_{1-x}N$ was also shown in [8] to increase with the increase in composition of aluminum (x). In addition to the above activation energy related issue, it was also shown in [5, 6] that electrically inactive magnesium-hydrogen complexes were formed during MOVPE growth, which leads to the low p-type doping in GaN based devices. Thus, the low doping efficiency combined with the large activation energy of Mg acceptors together results in large series resistances, high operating voltages and higher ideality factors in GaN based LEDs. Thermal annealing of p-GaN in N_2 at 700°C was suggested by Nakamura *et al.* [10] as one of the possible solutions to activate the acceptors. This was implemented in the coaxial LEDs as well, but further investigation of the p-GaN and p-AlGaN doping in them is required. In spite of these issues, the results obtained from the coaxial LEDs are encouraging and further research and development in the field could potentially lead to the realization of a revolutionary LED design with a compact, surface emitting geometry.

6.7 Conclusions

In this chapter, the various steps involved in the processing of the coaxial LEDs were discussed. The p-metal liftoff based technique was the widely used technique in most of the devices processed in this dissertation. A simple, yet innovative angled e-beam evaporation of p-metal was pursued to achieve deposition of the metal layers even on the sidewalls of the coaxial nano/microstructure. Following this, the LED mesa was defined and dry etching was performed to expose the n-side of the LED, on which the n-metal layers were deposited. A non-liftoff based p-metal process was also designed and implemented, where in the p-metal was deposited previous to the lithography step of

defining the p-contact region. This technique is particularly useful while using either thin p-metal layers, or indium tin oxide (ITO) transparent p-contact layers to enable light extraction from the top of the coaxial LED defined in Fig. 1.5 of chapter 1. Discussion with glo USA personnel revealed that it was important to get the light out from the top of the coaxial nanowire LEDs in order to avoid re-absorption of the emitted photons in the n-GaN substrate. Thus, their approach was to use a 95% transparent ITO p-contact layer, which was patterned using a non-liftoff, dry etch based p-metal process.

Some technological challenges with regards to the coaxial LED fabrication process were also addressed in this chapter. The importance of a growth sink to capture the excess growth nutrients and thereby preventing their deposition on the growth dielectric was highlighted. It was shown that the 3D GaN islands deposited unintentionally on the growth dielectric could be degrading to the functioning of the coaxial LED. Apart from this, the minute gaps existing in between the coaxial structures and the aperture patterns in the growth dielectric was also shown to be menacing to the successful functioning of the coaxial LED. Both these challenges proved to be alternate leakage path for the electrical current through the LED structures. The use of a high aspect ratio spin-on dielectric to fill these gaps was listed as one of the solutions to elimination of the leakage current.

The characterization results of the LEDs fabricated using the liftoff based p-metal process (using spin-on dielectric to fill the gaps mentioned above) was presented in the later sections of this chapter. The LEDs exhibited rectifying (diode-like) current-voltage characteristics with turn on voltages in the range of 1.5-3V. Some of the current vs. voltage characteristics were theoretically analyzed using curve fitting technique. The

diode ideality factor and the series resistance values were estimated using this curve fitting technique. A high series resistance and a large ideality factor were estimated for the current-voltage characteristics obtained for the coaxial LEDs. This was mainly attributed to the low p-doping levels in the shell layers. The activation of the p-type doping (Mg atoms) is considered an important step in the successful fabrication of a GaN based LED and further work is needed to analyze the doping levels in the coaxial structures fabricated in this dissertation.

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Chapter 7

Conclusions and Future Work

The growth, processing and characterization of GaN based coaxial LEDs have been discussed in this dissertation. The motivation for the fabrication of the coaxial LEDs was highlighted in chapter 1 of this thesis. GaN based coaxial LEDs have the potential to be efficient light emitters, in addition to being cost effective. The coaxial LED design presented in this thesis offers a non-polar active region template with a compact, surface emitting geometry and a natural guiding phenomenon. Some results on coaxial LEDs fabricated by other research groups were also presented in chapter 2. However, UNM's coaxial LED design is unique in the sense that it is based on a scalable, repeatable and industrially viable GaN growth process. This further motivated the study of these coaxial LEDs.

It was demonstrated in chapter 3 that the GaN nanostructures (wires and walls) were defect free. The threading defects (TDs) present in the underlying planar GaN layer often were filtered by the growth dielectric. However, the TDs entering the nanowires often bend towards the nearest $\{1\bar{1}00\}$ sidewall in close proximity to it. It was concluded that this phenomenon could be observed in any GaN structure that had a surface close to the TD. A simple TD elimination model based on climb was also presented and conversion into another defect type was considered energetically unfavorable.

Previous work reported the growth of GaN nanowires using a catalyst free selective area MOVPE growth process. In this dissertation, the evolution of this growth process as being scalable, repeatable and industrially viable has been demonstrated. The

pulsed MOVPE growth of GaN nanowires was extended to nanowalls, microstructure wires, walls and annulus patterns. The vertical and the lateral growth rates of the microstructures were analyzed and a capture radius was calculated, which was shown to be independent of the dimensions of the growth structures. The GaN microstructures grown on annulus patterns also demonstrated that the fast growing crystallographic planes grow to extinction and the stable slow growing orientations are more prominently visible during growth. This was in contrary to the inner concave side of the microstructures grown in annulus patterns, where the fast growing crystallographic orientations were prominently observed.

Following this, p-GaN, AlGaN and InGaN shell structures were grown around the GaN core structures, to create the coaxial structures necessary for the LEDs. The growth of p-GaN shell on n-GaN core involved a change of growth mode and lead to the formation of voids and inversion domain boundaries at the core-shell interface on the {0001} c-plane. The growth of AlGaN shells on GaN core nanowires was demonstrated in previous work and this was extended to other structures (nanowalls and microstructures). InGaN shells were also grown around AlGaN-GaN coaxial structures and the results were listed in chapter 5. However, the growth of InGaN based core-shell structures still needs refinement and we are continuing to explore this.

The growth of coaxial structures was followed by the fabrication of the coaxial LEDs. Two different approaches were employed to fabricate the coaxial LEDs. One approach was based on a liftoff-based technique of p-metal definition, while the other approach involved a non-liftoff-based technique to define the p-metal area. The technological challenges associated with the fabrication of the coaxial LED were also

addressed with special emphasis to the stray 3D island growth on the growth mask regions that could potentially serve as alternate electrical leakage path. The results obtained from the coaxial LEDs processed were presented and analyzed. The coaxial LEDs had high series resistance value and a high ideality factor. This could be attributed to the low p doping of the shell layers and the poor electrical ohmic contact between the p-metal and the p-AlGaN/p-GaN layers.

The coaxial LEDs need further refinement in terms of growth and processing, but the initial results have been encouraging. The growth, processing and characterization of GaN based coaxial LEDs with InGaN remains one of the most important priorities for future work. The addition of InGaN to the nanowires has been challenging, but several techniques like high pressure MOVPE and molecular beam epitaxy technique of growing InGaN/GaN quantum wells could be explored. Also, further research of the growth of 3D GaN structures in the annulus patterns is necessary.

The pyramidal growth of p-GaN shell on GaN core was demonstrated in this dissertation. The pyramidal growth around the coaxial LEDs was listed in section 6.5 (Fig. 17) of chapter 6 as one of the techniques to eliminate the electrical leakage occurring through the gaps between the coaxial structures and growth apertures. However, further research is required to develop defect (voids/ inversion domains) free GaN. Another technique highlighted in Fig. 17 of chapter 6 was the use of a localized oxide layer (localized oxidation of silicon - LOCOS method). In this method, a thin layer of polysilicon is sandwiched between two layers of growth dielectric and patterned in a similar method to the silicon nitride (SiN_x) growth dielectric. After the growth of coaxial structures, the sample is annealed at high temperature in the presence of air to oxidize the

polysilicon layer to form SiO_2. This oxide is anticipated to successfully fill the gaps between the growth dielectric and the coaxial microstructures to resist the electrical leakage.

Appendix A

Conference and Journal Publications

1. **Rishinaramangalam A. K.**, Hersee S. D., Fairchild M. N., Zhang L., Varangis P., “Threading Defect Elimination in GaN Nanostructures”, , presented at Electronics Materials Conference, June 23-25, Notre Dame, Indiana

2. Hersee S.D., **Rishinaramangalam A.K.**, Fairchild M., Talin A.A., “MOVPE Grown GaN Nanowires and Nanowire Devices”, (plenary) International Workshop on Nitrides (IWN 2008), Montreux, Switzerland, October 2008

3. **Rishinaramangalam A. K.**, Fairchild M. N., Balakrishnan G. Hersee S. D., “MOVPE growth of high index templates for MBE growth of InGaN LEDs”, - NAMBE 2012, submitted.

4. Hersee S. D., **Rishinaramangalam A. K.**, Fairchild M. N., Zhang L., Varangis P., “Threading Defect Elimination in GaN Nanowires”, *J. Mat. Res.* **26** 2293-2298 (2011)

5. Hersee S. D., Fairchild M., **Rishinaramangalam A. K.**, Ferdous M, Zhang L, Varangis P., Swartzentruber B., Talin A. A., "GaN nanowire light emitting diodes based on templated and scalable nanowire growth process”, *Electronics Letters*, **45** 75, (2009)

6. "Electronic transport in nanowires: from injection-limited to space-charge-limited behavior", F. Léonard, A. A. Talin, A. Katzenmeyer, B. S. Swartzentruber, S. T. Picraux, E. Toimil-Molares, J. G. Cederberg, X. Wang, S. D. Hersee and **A. Rishinaramangalum**, Proc. SPIE 7406, 74060G (2009); doi:10.1117/12.827495

Publications under preparation: -

7. **Rishinaramangalam A. K.**, Fairchild M. N., Hersee S. D., Balakrishnan G., “Selective area 3D growth of GaN in annulus type patterns”, *Appl. Phys. Lett.*, (in preparation).

8. **Rishinaramangalam A. K.**, Fairchild M. N., Shima D., Balakrishnan G., Hersee S. D., “Inversion domain boundaries and micro-void formation in GaN based coaxial microstructures grown by MOVPE”, *J. Crys. Growth.*,(in preparation)

9. **Rishinaramangalam A. K.**, Fairchild M. N., Hersee S. D., Balakrishnan G., “Theoretical estimation of growth nutrient capture radius in GaN based microwires grown by MOVPE”, Appl. Phys. Lett.,(in preparation)