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Design of a Readout Integrated Circuit (ROIC) for Infrared Imaging Applications

Anahita Khoshakhlagh

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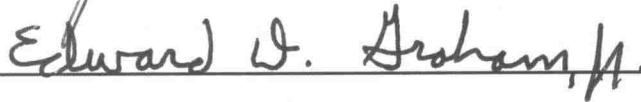
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Approved by the Thesis Committee:



Chairperson





Design of a Readout Integrated Circuit (ROIC) for Infrared Imaging Applications

by

Anahita Khoshakhlagh

B.S., University of New Mexico, 2008

THESIS

Submitted in Partial Fulfillment of the
Requirements for the Degree of

Master of Science
Electrical Engineering

The University of New Mexico

Albuquerque, New Mexico

December, 2010

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Dedication

To my parents, Shahnaz and Rahman, for their support and encouragement they have given me for graduation.

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ABSTRACT OF THESIS

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Abstract

There has been a growing interest in using Infrared (IR) imaging systems in various applications ranging from medical diagnosis to military surveillance. The quality of the IR imaging systems depends on 1) the sensitivity of the Focal Plane Arrays (FPA) as the transducer of the electromagnetic wave and 2) the Readout Integrated Circuit (ROIC) that provides the pixel data to the processing unit. In this thesis, we describe specific ROIC designed for a dual-band IR imaging system. In particular, we focus on the ROIC part and propose an efficient circuit that meets several design objectives, including minimum power, minimum cost, and maximum dynamic range. We start with analog design of different parts of the circuit based upon a bottom-up design discipline. We then validate our design using TSpice simulation and analyzing the time/frequency response of the circuit at each step. Next, we proceed with layout design, where we present our final ROIC layout

designed using Tanner EDA tools. Finally, we explain the ROIC test bed developed at the Center for High Technology Materials (CHTM), University of New Mexico, which can be used to test Indigo-based IR imaging systems as well as our designed ROIC.

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Chapter 1

Introduction

1.1 Infrared Spectrum

Infrared (IR) is a form of light (or radiation) that is invisible to the human eye. It is the portion of the electromagnetic spectrum found between visible light and radio waves, at wavelengths extending from 0.7 to 300 micrometers, which equates to a frequency range between approximately 1 and 430 THz. Figure 1.1 shows the infrared spectrum. Here, it can be seen that the portion of the infrared electromagnetic spectrum can be divided into near-IR, mid-IR and far-IR. Each of these bands has its own characteristics. Near infrared is closer to the visible light while far infrared is farther from that.

Today, there is a growing interest in using IR imaging systems due to their fruitful applications ranging from medical diagnosis to military surveillance. For example, these systems can help in several forms such as disaster rescue, night vision, homing and tracking, ecology and weather forecasting, target acquisition, predictive inspection and maintenance, surveillance, short range communication, remote temperature sensing, spectroscopy and medical diagnostic and treatment. Figure 1.2 illustrates a few applications of IR imaging. Thermal imaging cameras detect radiation in the infrared range of the

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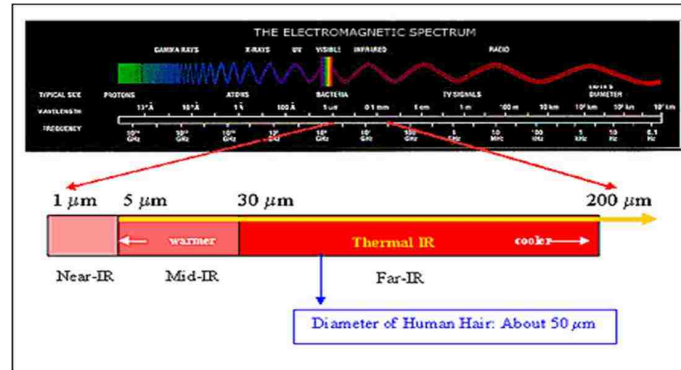


Figure 1.1: Infrared Spectrum [3].

electromagnetic spectrum. In particular, images produced with that radiation is called thermograms. According to the black body radiation law, IR radiation is emitted by all objects near room temperature [19]. Therefore, it is possible to see an environment without visible light with thermography. The amount of radiation emitted by an object is directly dependent upon the temperature; therefore, thermography allows one to see variations in temperature. Mostly, far infrared is associated with thermal emission or heat.

Quality of IR cameras has been improved significantly in recent years. Mono-color IR cameras are now replaced with multi-color imaging systems to enhance the quality of IR images based on information from different IR bands. The output stream of the IR camera is then converted to the video stream after some processing. Figure 1.3 depicts a general block diagram for converting IR radiation to a video sequence. Two main components of an infrared camera system is Focal Plane Array (FPA) and Readout Integrated Circuit (ROIC). These two components are explained in the next section.

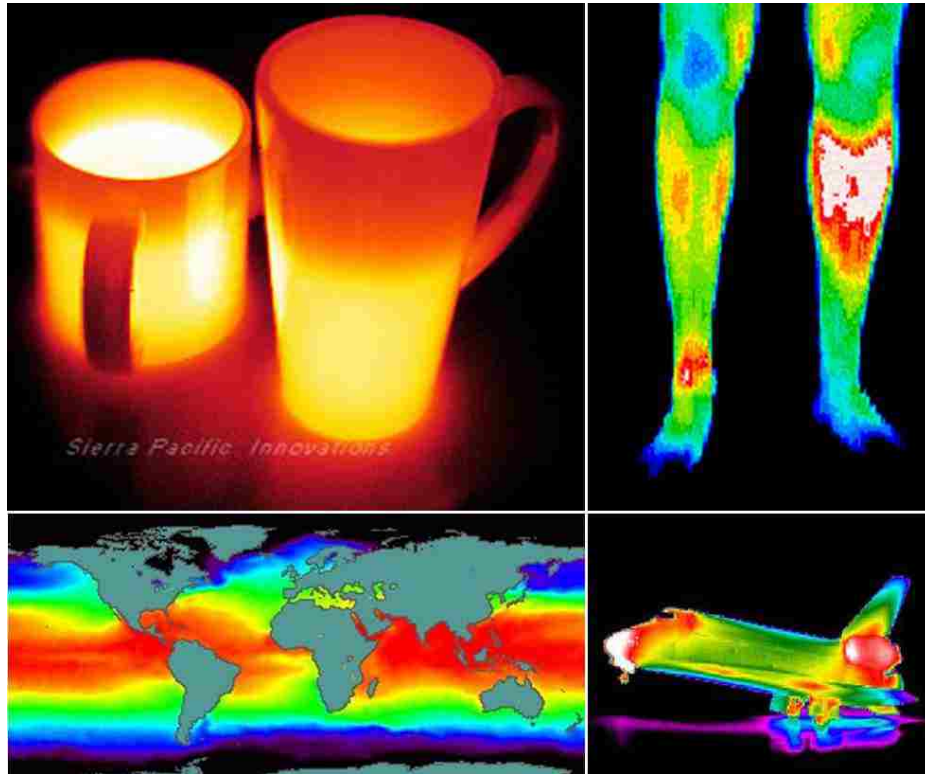


Figure 1.2: Infrared applications: Infrared image of two cups containing very hot drink (upper left), medical infrared scan show an injured leg (upper right), infrared map of global sea surface temperatures (lower left) and infrared image of a landing space shuttle (lower right) [3].

1.2 Focal Plane Array

An FPA is an image sensing device consisting of an array of light-sensing pixels at the focal plane of a lens. FPAs are used mostly for imaging purposes, but can also be used for non-imaging purposes such as spectrometry, Light Detection And Ranging (LIDAR), and



Figure 1.3: Converting IR radiation to IR video sequence.

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wave-front sensing. In infrared imaging, FPA refers to the part that converts IR radiations to electrical charges. FPA consists of grid of IR detectors. An IR detector is a photodetector that is sensitive to IR radiation. There are two main types of IR detectors: thermal and photonic [1].

The thermal effects of the incident IR radiation can be detected by applying temperature dependent phenomena. For example bolometers and microbolometers are based on changes in resistance. The thermoelectric effect is used in thermocouples and thermopiles. Thermal expansion can be followed by Golay cells. Also pyroelectric detectors are mostly used in IR spectrometers.

On the other hand, photonic IR detectors are based on thermal effects in semiconductor. The photo sensitivity of this type of detectors is dependent on wavelength. The materials in these IR detectors are semiconductors with narrow band gaps such as Ge, InGaAs, InGaSb, InSb, HgCdTe, etc. Photonic detectors are divided into two main groups: intrinsic and extrinsic. Intrinsic type is also divided into photoconductive type and photovoltaic type. Photoconductive detectors are made from materials such as: PbS, PbSe, InSb and HgCdTe [19]. In photovoltaic type detectors materials such as Ge, InGaAs, InAs, InSb and HgCdTe can be utilized. Extrinsic type detectors are mostly made from Ge/Au, Ge/Hg, Ge/Cu, Ge/Zn, Si/Ga and Si/As [19].

The response time and sensitivity of photonic (quantum) detectors are much higher than thermal detectors, but usually these have to be cooled to reduce the thermal noise. IR detectors are cooled to improve the signal to noise ratio (S/N) and to keep the temperature of the detector at a constant point. There are several cooling mechanisms such as: cryogenic dewar cooling using liquid nitrogen, thermoelectric cooling, Joule-Thomson cooling and gas-circulation cooling.

One of the most important characteristics of the IR detectors is the detectivity symbolized by D^* . D^* is the photo sensitivity per unit active area of a detector which make

it possible to compare different detectors with one another. The noise may come from the background fluctuation, operating circuits or the IR detector itself. Usually, background fluctuation noise dominates the other two noise types and also puts a theoretical limit on D^* . This background noise is called Background Limited Infrared Photodetection (BLIP) [19].

1.3 Readout Integrated Circuit (ROIC)

The ROIC is a silicon chip with circuits that are responsible to integrate, amplify, and multiplex the weak detector charges. The readout circuit acts as an interface between the FPA and the signal processing unit. Figure 1.4 shows how FPA and ROIC are connected to each other in a hybrid structure.

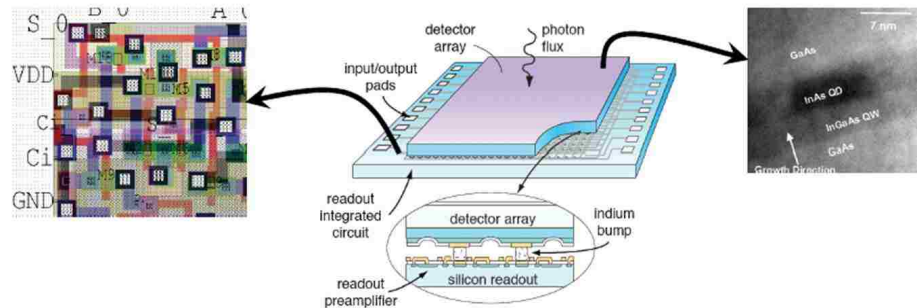


Figure 1.4: Hybrid structure of FPA and ROIC [23].

Figure 1.5 shows a block diagram for ROIC. The ROIC and FPA are connected by an array of indium bumps, which provide the electrical interface of the individual detector elements (pixels) to the corresponding ROIC input unit cells. The induced small current by the IR radiation is integrated and sampled in the corresponding unit cell. The outputs of the unit cells are then swept row by row and converted to a serial stream of bits by means of a control circuit as we explain later. This serial stream is then passed to the

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processing unit for post processing and anti-aliasing. Figure 1.6 shows how a single detector in the FPA connects to its corresponding unit cell in the ROIC through an Indium bump.

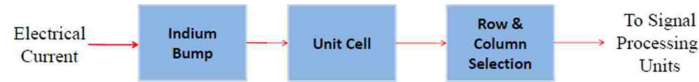


Figure 1.5: General block diagram of a ROIC.

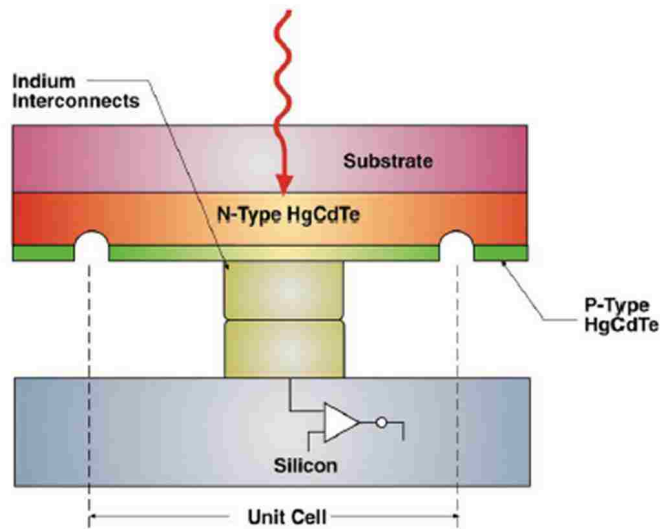


Figure 1.6: Connection of a single detector to the unit cell by Indium bump [11].

1.3.1 Connecting Bump

The main type of conductive interconnect solder bump for direct connection of active devices to substrates is the indium bump. Indium bump technology is a process used mainly for flip-chip hybridization of semiconductor components. This technology has been part of the electronic interconnect process for about 40 years as part of a low cost assembly process. Indium is chosen as the main material of the bump due to the desirable properties such as cryogenic stability, thermal and electrical conductivity, self-adhesive

(ductile) nature and relative ease of application. In the indium bump process, indium is deposited as the last step in the metallization processing of a device wafer. In commercial ROICs, indium bumps are already in place [18].

1.3.2 Unit Cell

The unit cell converts the electrical current at each detector to a voltage for each pixel. The unit cell consists of an integrator, a preamplifier, and a sample & hold circuit. The preamplifier amplifies the weak current coming from the detector. Transforming the small diode incremental current, generated by infrared radiation, into a relatively large measurable output voltage is commonly done by integrating the photocurrent in a capacitor during a fixed period of time. There are two main modes for ROIC circuits: current-mode and voltage mode. The majority of the reported readout circuits are implemented in voltage mode. The ROIC designed in this project is a voltage mode device. Current-mode ROIC is less prevalent but shows good properties such as less silicon area. There are generally many different methods for building the ROIC unit cell. Source-Follower per Detector (SFD), Direct Injection (DI) and Gate-Modulation Input (GMI) are common methods that are frequently used in FPAs. More complex techniques such as Buffered Direct Injection (BDI) and Capacitive Transimpedance Amplifier (CTIA) which provide excellent performance, also exist. More explanation on these techniques can be found in Chapter 2. At the end of the integration time, the integrated voltage is sampled and held on a hold capacitor (sample and hold capacitor). Each row is sequentially connected to an array of column amplifiers via the column buses that are shared by all of the pixels in a column. There are two commonly used modes for integration: Integrate-While-Read and Integrate-Then-Read. In the Integrate-While-Read mode, while frame n is being read, frame $n + 1$ is being integrated. In Integrate-Then-Read mode, integration for frame $n + 1$ begins only after all of the pixels in frame n have been read. More explanation regarding the ROIC unit cells can be found in Chapter 2.

1.3.3 Row and Column Selection

The provided voltages (or currents) by the unit cells are converted to a stream of bits by the means of a control circuit that sweeps the rows of columns of the FPA. Two main signals that are used for time synchronization of the circuit are line synchronization (LSYNC) and frame synchronization (FSYNC), which along with the clock (CLK), multiplex the provided array of the unit cell voltages to a serial stream sequentially. More explanation on control circuit is provided in Chapter 2.

1.4 Our Proposed Approach

1.4.1 Motivation

Most of the commercial ROICs available in the market are suitable only for single-color FPAs, where the bias voltage of the ROIC for mono-color FPAs is fixed. As a result, they are not suitable for multicolor FPAs. There are some important design considerations for multicolor ROICs, including: 1) the ROIC should apply the proper bias voltage and read the data from the FPA, 2) the ROIC circuit should be designed at the exact size of the FPA for hybrid assembly. The goal of this thesis is to develop a 128x128 pixel dual-band ROIC with the following properties:

1. Provide considerably larger bias voltage in both polarities
2. Amplify and integrate the weak signals generated by the infrared detectors
3. Multiplex all amplified signals into a video signal
4. Be packed into a small Silicon area of 30um x 30um (matched with the FPA pixel size)

1.4.2 Technical Approach

For the FPA we employed an array of high efficiency quantum dot (QD) infrared detector arranged such that they can detect both near and far infrared spectrums. We used CTIA unit cell topology which has good bias control, good noise immunity and high sensitivity. Unlike DI and BDI, the input impedance of the CTIA is independent of the detector current. Moreover, CTIA can provide bipolar integration for both positive and negative biases, which makes it a perfect choice for our ROIC to work with a dual-band FPA. The schematic and layout are designed using Tanner EDA tools [5], based on 0.35um high-voltage CMOS technology process offered by MOSIS.

1.5 Outline of the Thesis

This thesis is structured as follows. In Chapter 2 we provide a more detailed explanation on ROIC. In Chapter 3 we explain our designed read out integrated circuits part by part. The testing and measurement results are given in Chapter 4. We conclude in Chapter 5.

Chapter 2

General Structure of a Readout Integrated Circuit (ROIC)

A typical FPA is composed of n columns by m rows of individual cells or pixels, which define the infrared image frame. The interface circuit (or driving circuit) of each cell, which converts the current from each photodiode to a voltage at each pixel, is referred to as *ROIC Unit Cell*. A control circuit is also needed to synchronize the operation of the unit cells and convert the output of the IR pixels to a stream of bits [13]. A general architecture of a ROIC circuit is shown in Figure 2.1. In this mode, digitization of the integrated current occurs at the column amplifiers. Note that there are two main modes for ROIC circuits in general: current mode and voltage mode. Voltage mode ROICs are more common and the high-level circuit shown in Figure 2.1 is actually a voltage mode ROIC. In the next section we explain the differences between current mode and voltage mode ROICs.

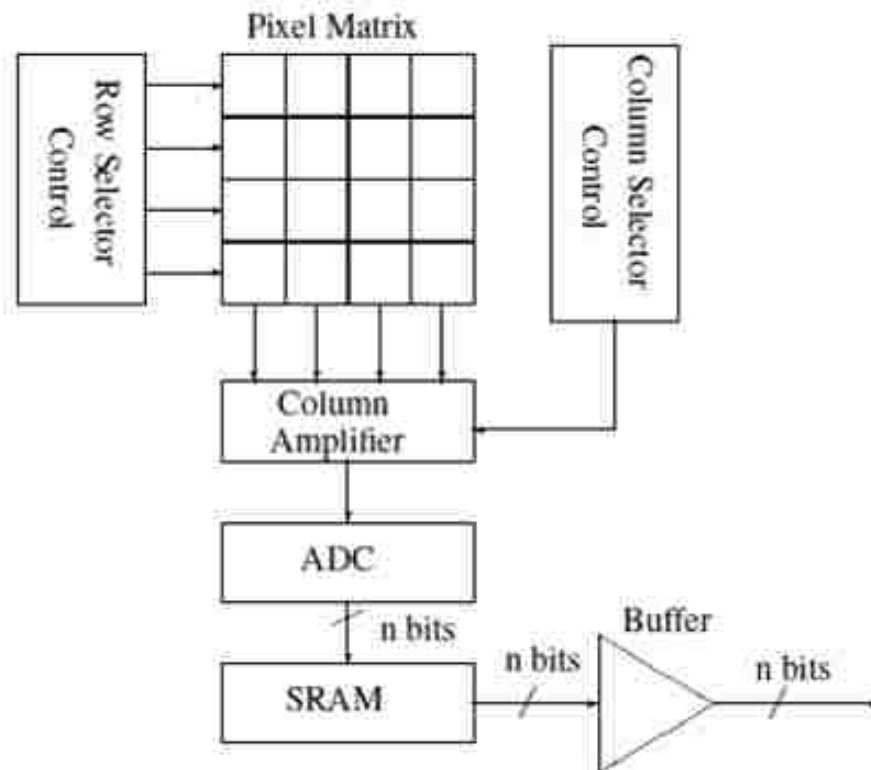


Figure 2.1: Architecture for voltage mode readout circuits [9, 10].

2.1 ROIC Unit Cell

In this section, we explain the ROIC unit cells in more details. Transforming the small diode incremental current, generated by infrared radiation, into a relatively large measurable output voltage is commonly done by integrating the photocurrent via a small capacitor during a fixed period of time. The capacitor's voltage at the end of the integration period should be proportional to the current and, as such, represents the incident infrared radiation of the pixel corresponding to the location of the infrared diode photo sensor. A simplified schematic of a unit cell is shown in Figure 2.2. Note that each pixel requires an individual unit cell and, as a result, the overall ROIC circuit consists of a very large number (thousands) of these cells.

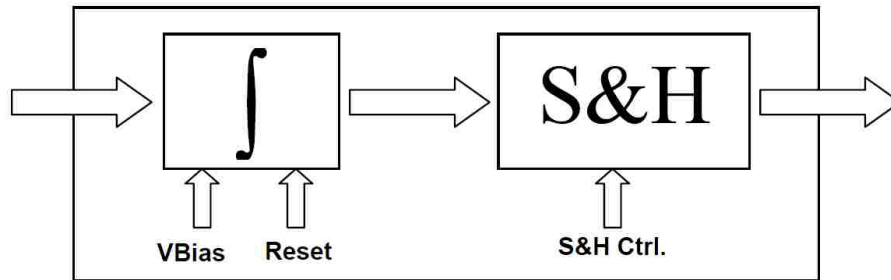


Figure 2.2: Simplified Schematic of a unit cell.

Voltage vs. Current Mode for ROIC Operation

A high performance, efficient ROIC circuit has three important characteristics:

1. For dark current and detector noise reduction, it should provide a controlled detector bias.
2. The circuit should have low input impedance. This will result in obtaining high injection efficiency for integrating the maximum amount of current generated by the detector on the integration capacitance. Also, it will increase its bandwidth and decrease its input referred noise.
3. The circuit should have a large dynamic range. This will increase the maximum charge storage capacity, which requires a large integration capacitance and a high voltage swing.

In order to meet these requirements, two different modes for operation of ROIC can be considered: current mode and voltage mode. The majority of the reported readout circuits are implemented in voltage mode. The general framework of a voltage mode ROIC circuit is illustrated in Figure 2.1. In this mode, digitization of the integrated current occurs at the column amplifiers. The architecture of a current mode ROIC is also shown in Figure 2.3. As shown in this figure, the integration capacitor is placed outside the pixel. As a result,

as windowing, signal skimming, Integrate-While-Read, and Integrate-Then-Read operations. In the sequel, we provide a brief introduction to different topologies of integrators and sample-and-hold circuits and then we explain why we chose CTIA in our design.

1. Source-Follower per Detector (SFD) [12, 16]: A schematic of SFD circuit is shown in Figure 2.4. As shown in this figure a source follower composed of two NMOS transistors: MNI and MNL, along with a PMOS M-Rst, which acts as a reset gate. The total integration capacitance is the summation of C_{detector} and the input capacitance of the SFD. The integration capacitance is reset using M-Rst and then charged using I_{detector} . The cell voltage is samples using M-Sel, which is controlled by the output control circuits.

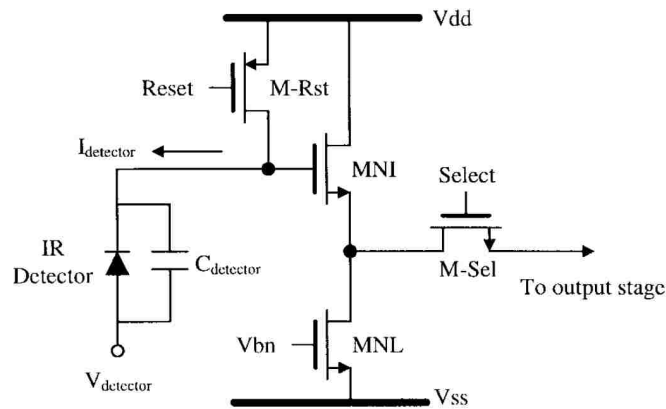


Figure 2.4: Schematic of the SFD readout circuit [12].

Some main pros and cons of SFD are listed below:

- Pros: simple structure, suitable for high-density and low power applications.
- Cons: nonlinear behavior and change of circuit characteristics during integration. This is the direct result of the detector bias voltage changes through integration. Furthermore, SFD is not immune to noises induced by switching.

2. Direct Injection (DI) [12, 16]: Figure 2.5 shows a simple schematic of a DI readout circuit. In this topology a PMOS transistor (M_{DI}) is used to direct the $I_{detector}$ to the integration capacitor C_{int} . This capacitor is reset using an NMOS M-Rst transistor, which is clock-controlled. Finally, the sampled voltage is multiplexed to the output circuit using M-Sel.

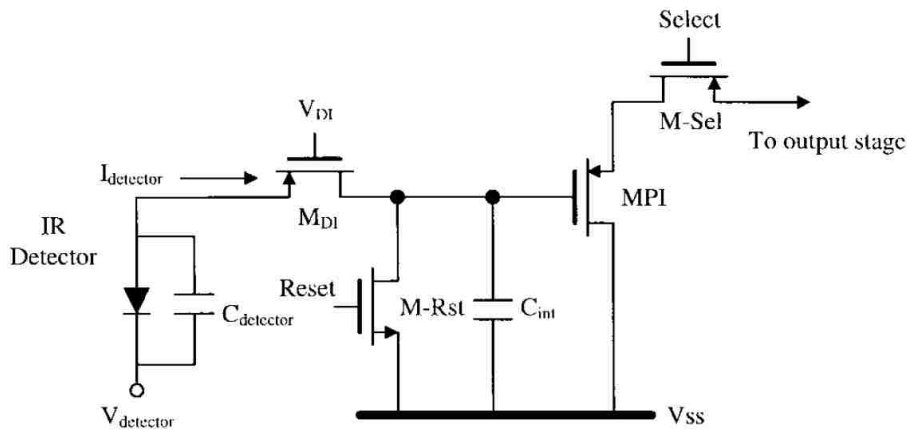


Figure 2.5: Schematic of the DI readout circuit [12].

- Pros: better bias control than the SFD during integration using the common gate PMOS. Low power, simple and suitable for high-density applications.
 - Cons: DI is not suitable for the applications of low-background IR image readout. A stable and low noise DC bias is needed in the DI circuit, which is usually hard to provide. The nonlinearity and noise sensitivity are still problematic.
3. Gate-Modulation Input (GMI) [12, 16]: A simple schematic of the GMI readout circuit is shown in Figure 2.6. The readout circuit has a current-mirror configuration with the tunable bias to control the current gain. This current is then mirrored using M_{input} and directed to charge the integration capacitor C_{int} . This capacitor is then reset to high using M-Rst, which is clock-controlled. The sampled voltage is multiplexed to the next stage using NMOS M-Sel. The current gain of the current mirror

circuitry is tunable by the adjustable bias V_{source} .

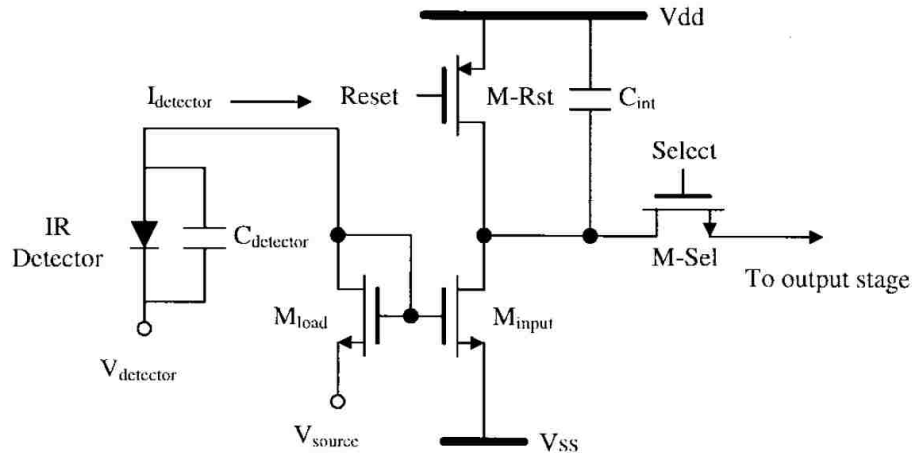


Figure 2.6: Schematic of the GMI readout circuit [12].

- Pros: the inherent current gain of the GMI leads to higher detection sensitivity compared to that of DI. Also, the noise immunity is improved in this topology. Moreover, the adaptive current gain in the GMI can be controlled by the background level and thus the realizable background suppression leads to a higher dynamic range.
 - Cons: the injection efficiency of the GMI is dependent on the ratio of detector shunt resistance to input resistance, which leads to nonlinearity of the circuit. Also, both injection efficiency and current gain of the GMI are sensitive to the variations of the threshold voltages.
4. Buffered Direct Injection (BDI) [12, 16]: BDI which is shown in Figure 2.7 and can be considered as the improved version of the DI topology. As shown, the circuit is similar to that of DI except that an Op-Amp is connected between gate node of the common-gate input device and the detector node. The negative feedback connection of the Op-Amp can decrease the input impedance. The bias control of BDI is more

stable than DI and SFD, since the detector bias is controlled by the input voltage of the differential pair instead of gate-to-source voltage of the DI circuit.

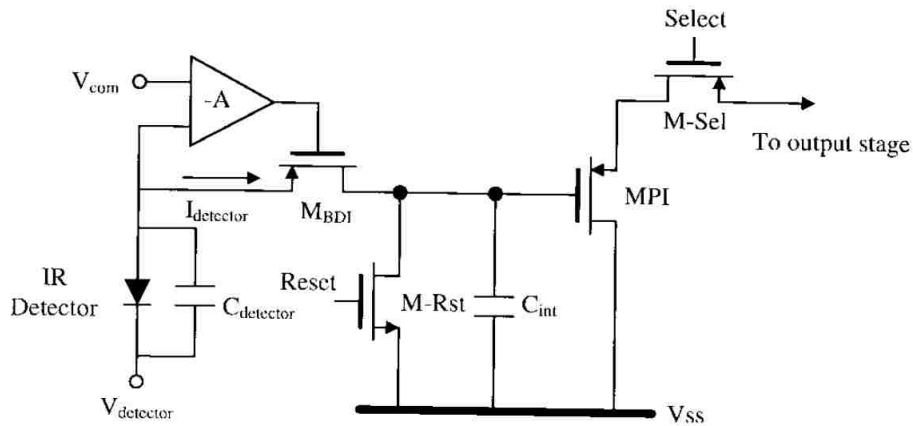


Figure 2.7: Schematic of the BDI readout circuit [12].

- Pros: The nonlinearity and noise problem of DI circuit are improved considerably in BDI.
- Cons: the additional Op-Amp consumes active power during integration as well as silicon real estate. This makes the BDI design inappropriate for large-scale low-power applications.

5. Capacitive Transimpedance Amplifier (CTIA) [12, 16]: The schematic of CTIA is shown in Figure 2.8. In this design, the integration circuit is placed in the feedback loop of the Op-Amp. Similar to previous designs, M-Rst is used to discharge C_{int} . Good bias control can be obtained in the CTIA similar to the BDI.

- Pros: good bias control, good noise immunity and high sensitivity due to the Miller effect on C_{int} . Unlike DI and BDI, the input impedance of the CTIA is independent of the detector current. Moreover, CTIA can provide bipolar integration for both positive and negative biases.

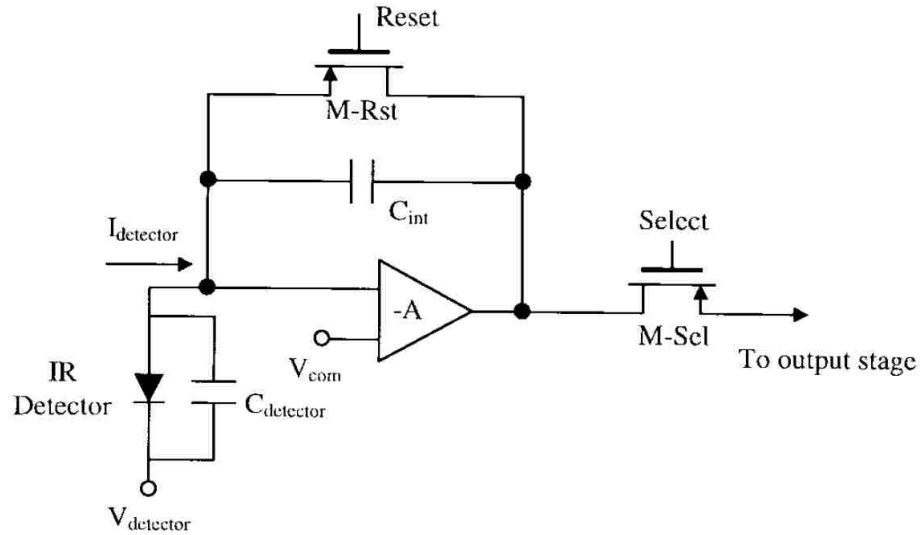


Figure 2.8: Schematic of the CTIA readout circuit [12].

- Cons: the feedthrough effect of the reset clock can be coupled to the detector node and affect the stability of both detector bias and amplifier operational point. Moreover, similar to BDI, high power consumption can be a problem. In addition due to Op-Amp, CTIA requires a large area and therefore is not suitable for high density FPAs.

In our design, we selected CTIA due to its capability of bidirectional integration. More details regarding our design is given in Chapter 3.

2.2 Row and Column Decoding Circuit

A general architecture for a typical ROIC circuit is shown in Figure 2.9. As seen in the figure, the outputs of the ROIC unit cells are multiplexed into one or several outputs using a row/column decoding circuit.

Chapter 2. General Structure of a Readout Integrated Circuit (ROIC)

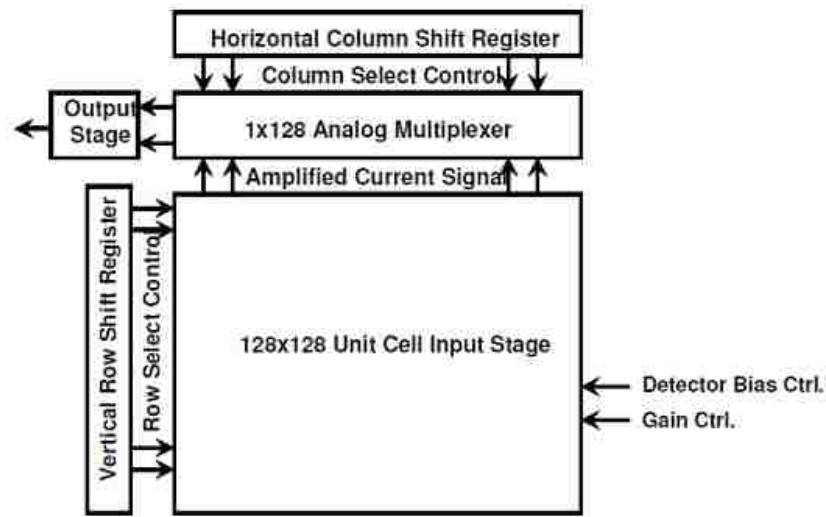


Figure 2.9: A typical ROIC architecture.

A more detailed schematic of a standard 320x256 readout circuit is then shown in Figure 2.10. As shown in this figure, FPA consists of a network of unit cells. Depending on the mode of operation, the output of the FPA is multiplexed into a single or several outputs. In this section, we introduce the multiplexing circuit that is used to decode the row and column outputs.

As explained in Section 2.1.1, the detector current in each unit cell flows through the gate of the integration transistor and the charge is collected into the integration capacitance. The resulting voltage is then sampled and held using the S&H circuit. Note that, typically the detector bias voltage in modern ROICs is digitally controlled by the means of a command register and then the analog bias voltage is generated by a Digital to Analog Converter (DAC).

The output of the S&H circuit (after a skimming stage) is held and, at a certain time, is multiplexed to the output(s). The resulting sequence of the bits at the output pins are then transferred to the processing units. The output data rate depends on the design of the ROIC circuit. A typical data rate for a standard 320x256 ROIC circuit is around 6 MHz.

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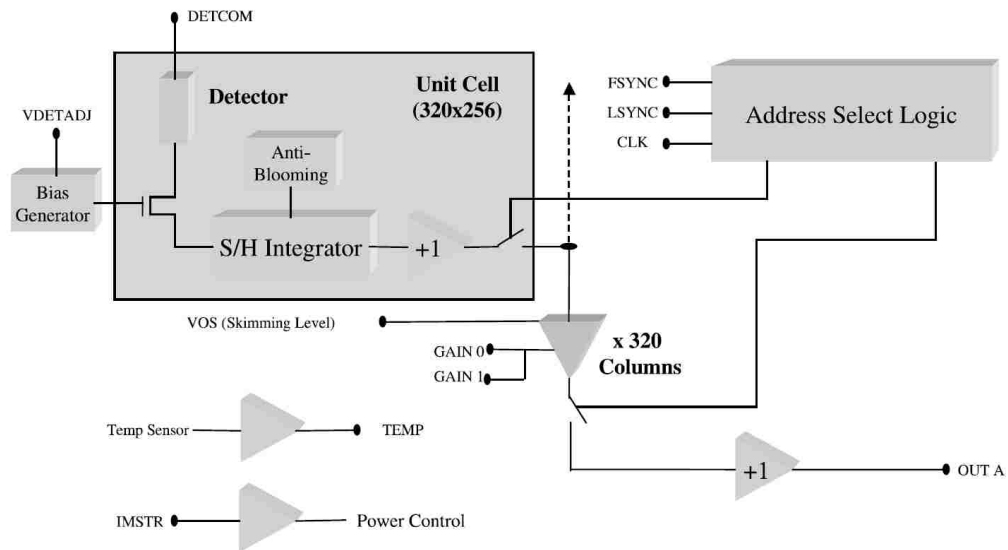


Figure 2.10: Schematic of a standard 320 readout circuit [7, 8, 14].

Depending on the mode of operation of the ROIC, the first pixel is defined differently. Figure 2.11 depicts four possible ways (default, inverted, reverted and inverted & reverted), to define the first pixel in the FPA and, as a consequence, the readout order. Note that we assumed single output readout for the ROIC but it is straight forward to extend the concepts to multiple output readout.

In the default mode, the lowest left-hand pixel is defined as pixel [0,0]. This pixel is the first pixel to be readout in the single output mode. This mode of operation would be chosen for a "normal" inverting optical system. By placing the bottom row at the "bottom" of a camera system, and using this type of lens a normal raster scan image will be presented which is shown in Figure 2.11.

When the first cell is selected in the matrix, other cells should be selected sequentially and in a timely manner. There are three pulses that control the readout cell position in the column, row, and frame. Those are clock pulse (CLK), line synchronization pulse (LSYNC) and frame synchronization pulse (FSYNC). These pulses control two shift reg-

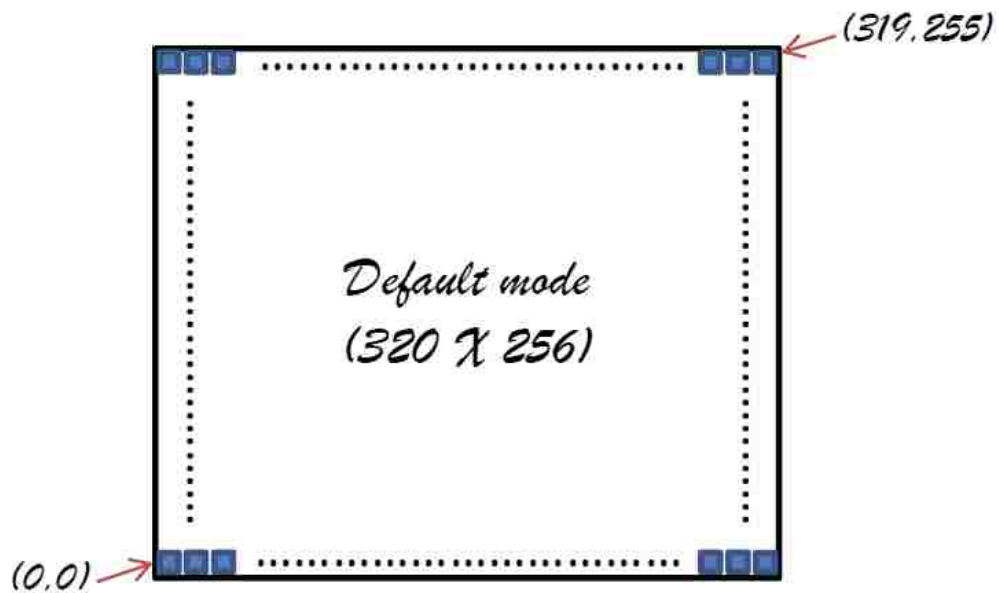


Figure 2.11: ROIC readout order in default mode.

isters; one for the row select control and one for the column select control. Here is a short description of the control signals:

- CLK: The master clock is the highest frequency clock. This signal provides a reference for pixel readout, and in addition, all the other clocks (FSYNC, and LSYNC) are integral number of CLK periods.
- LSYNC: Controls the readout synchronization of each individual line on the array.
- FSYNC: The rising edge of FSYNC marks the beginning of the frame time. The rising edge of FSYNC is also used to apply a control word, after it has been loaded. FSYNC also controls the integration time.

Starting from the first cell in the first row, the outputs of all cells in the row go to the column multiplexer. With each clock pulse, the multiplexer connects the output of one of the cells in the first row to the output stage. After multiplexing the last cell in

the row, the LSYNC pulse triggers the row shift register. As a result, the second line will be selected and the column shift register is also reset. Similar to the first row, each column will again be selected sequentially by the clock pulse. At the end of the frame, the FSYNC pulse resets both row and column shift registers and the pointer returns to its initial position to start a new frame. The LSYNC and FSYNC pulses are generated based on the ROIC operation mode (Integrate-While-Read or Integrate-Then-Read). Those modes are explained in the next section.

2.2.1 Integrate-While-Read and Integrate-Then-Read Modes of Operation

A commonly used macro structure for ROIC features snapshot mode integration, where all the pixels are integrated simultaneously. In such a case, the integration time is controlled by FSYNC signal. FSYNC signal triggers the beginning of each frame. During each frame period, the integration time varies depending on the mode of integration. Two commonly used modes are Integrate-While-Read and Integrate-Then-Read. Next, we explain briefly these two modes of integration.

In Integrate-While-Read mode, the rising edge of the FSYNC triggers the beginning of the frame. It is then followed by a sequence of LSYNC signals for every line change. Note that the pattern that the ROIC sweeps through the frame is determined by the sweep mode. Frame integration is triggered by the falling edge of the FSYNC. Note that the frame time, in this case, is approximately equal to the read time. In Integrate-Then-Read mode, similar to the Integrate-While-Read, the rising edge of the FSYNC begins the frame cycle, followed by the LSYNC readout pulses. The FSYNC falling edge triggers the integration cycle. However, in this mode, FSYNC signal remains high until the end of readout sequence and the integration starts just after the readout. Figure 2.12 illustrates the timing diagram of these two modes.

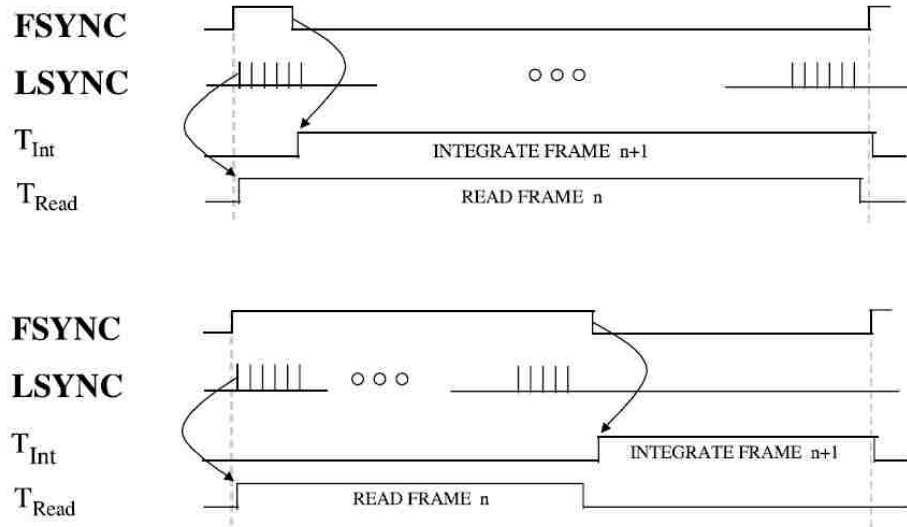


Figure 2.12: The timing diagram of the Integration-While-Read (up) and Integrate-Then-Read (down) integration modes [7, 8, 14]

2.2.2 Timing of the integration process

Figure 2.13 shows the detailed timing of the integration process. The rising edge of the FSYNC clock is considered as the starting point of a frame. The FSYNC pulse occurs at a regular frequency for a given frame rate. The location of the falling edge of the FSYNC pulse is varied to control integration time.

In Figure 2.13 the rising edge of FSYNC triggers the global sample and hold (C_{INTSH}) followed by the reset of the integration capacitor (C_{INTRST}). The falling edge of FSYNC releases C_{INTRST} . When the Integrate signal is high, integration of photocurrent is occurring for all pixels. When the C_{INTRST} signal is high, all unit cell integration capacitors are held in reset.

The pulse widths of the global unit cell sample and hold (C_{INTSH}) and global unit cell reset (C_{INTRST}) are shown in Figure 2.13. Note that the global clocks have a fixed rise

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and fall time. The rise and fall time of these signals is controlled on-chip and does not depend on the master clock frequency. The minimum FSYNC pulse width and minimum global unit cell reset clock pulse width times are also detailed in Figure 2.13.

Note that the waveforms labeled "INTEGRATE" and "C_{INT}RST" on Figure 2.13 are not actual on-chip signals, but they illustrate the integration and reset times.

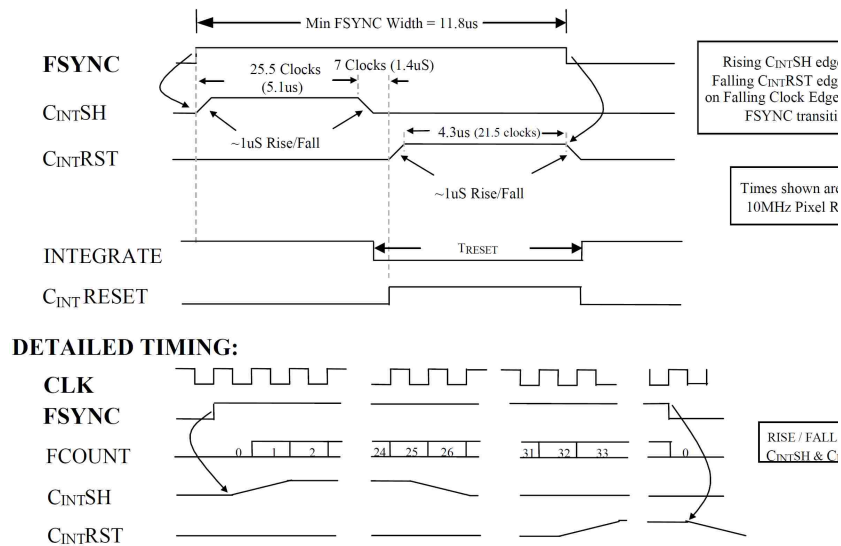


Figure 2.13: Integration time [8].

Column Amplifier

As shown in Figure 2.1, there is a unit called column amplifier. The functions of the column amplifier are: amplification and skimming. First the signal from the unit cell is sampled and held into the column amplifier. Then the sampled signal is amplified. The gain of the amplifier is controllable and is usually in the range of 1-4. Also a global skimming or offset function is implemented within the column amplifier and can be enabled or disabled. The column amplifier is also used to drive the output multiplexer bus.

Chapter 3

Design of a Read Out Integrated Circuit (ROIC) for Infrared Imaging

In this section, we explain our designed ROIC circuit by characterizing its building blocks and then explaining how these blocks are designed to meet the required specifications.

As explained in Chapter 2, two different parts of the ROIC circuit are the unit cell and the control circuit. The ROIC unit cell is the interface between the FPA and the processing unit, which is controlled by the sequential signals generated by the control unit. We used Capacitive Transimpedance Amplifier (CTIA) topology for the unit cell design. CTIA benefits from good bias control, good noise immunity and high sensitivity [15]. Furthermore, unlike DI and BDI topologies, the input impedance of the CTIA is independent of the detector current. Moreover, CTIA can provide bipolar integration for both positive and negative biases. However, in CTIA topology the feedthrough effect of the reset clock can be coupled to the detector node and affect the stability of both detector bias and amplifier operational point. Moreover, similar to BDI, high power consumption can be a problem [12, 16]. The power consumption can be decreased by using low V_{DD} for the parts that do not need high dynamic range. In our design, for the Op-Amp of the

integration circuit we use $V_{DD} = 15$ V to obtain a high dynamic range of 15 V. For the other parts, $V_{DD} = 3.3$ V have been used to decrease the total power consumption of the circuit.

Next, we start with the design of the ROIC unit cell and then proceed with characterization of the control circuit.

3.1 Design of ROIC Unit Cell

In this part, we explain the design of our ROIC unit cell. We start with characterization of different elements of the ROIC unit cell and then proceed by providing the overall unit cell circuit.

3.1.1 Integration Circuit

As mentioned in previous section, we have selected the CTIA topology for our design. Based on the CTIA circuit shown in Figure 2.8, the voltage at the output node voltage of the Op-Amp is given by:

$$V_{\text{out}}(t) = \frac{1}{C} \int_0^t I_{\text{out}}(\tau) d\tau + V_{\text{out}}(0), \quad (3.1)$$

where I_{out} is the output current of the infrared detector and C is the integrator capacitance. In order to reset the integration, we added a switch parallel to the capacitor. Each time the switch is closed, the capacitor discharges and when the switch is open the integration starts again. The integration process is controlled by the FSYNC pulse, which was explained in detail in Section 2.2.

3.1.2 Analog Switch and the Sample & Hold Circuit

The purpose of the sample and hold circuit is to hold the analog voltage steady for a short time, while the following system performs some operation that takes a small amount of time [2]. In a sample and hold circuit a capacitor is used to store the analog voltage, and an electronic switch or gate is used to alternately connect and disconnect the capacitor to the analog input. The rate at which this switch is operated is called the *sampling rate*. Figure 3.1 illustrates the output of our designed S&H circuit with a sinusoidal input. The test-bed

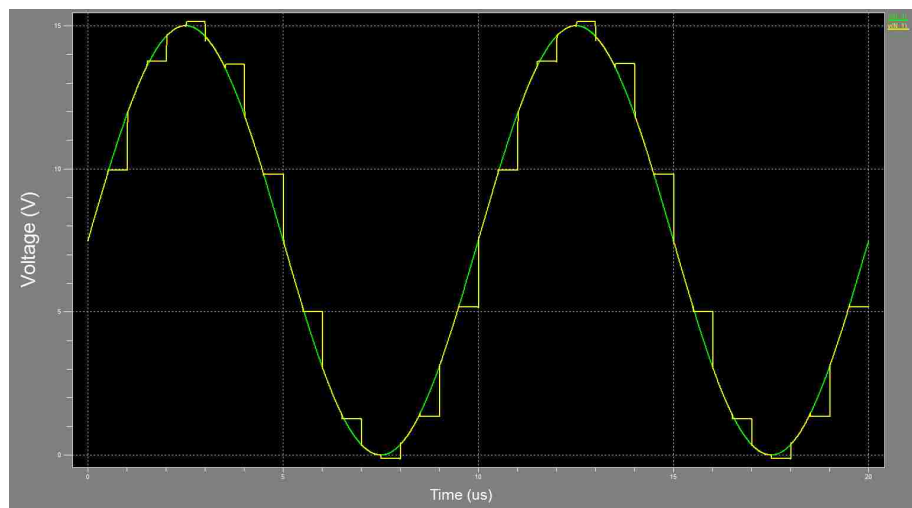


Figure 3.1: Output of our designed S&H circuit with a sinusoidal input.

used to generate the waveform is also shown in Figure 3.2. The main part of the sample and hold circuit is the analog switch, whose schematic is shown in Figure 3.3.

3.1.3 Op-Amp Circuit

The schematic of the differential amplifier is shown in Figure 3.4. The performance of the Op-Amp circuits are characterized by parameters such as differential gain, Common-Mode Rejection Ratio (CMRR), Band Width, Power dissipation and Dynamic Range. We

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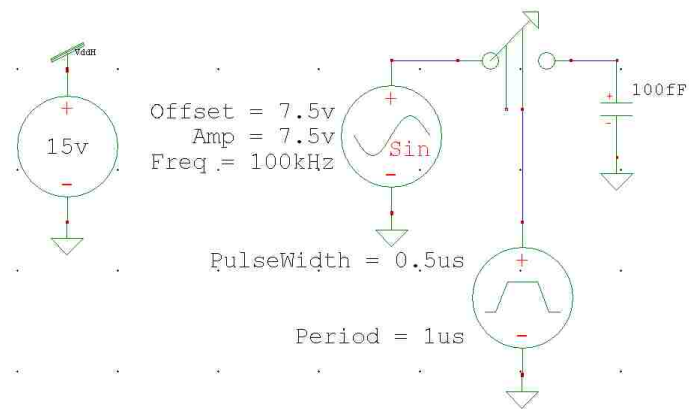


Figure 3.2: The test-bed used to generate the wave form of Fig. 3.1.

used active-load topology to increase the output differential gain. Assuming the same $\frac{W}{L}$ ratio for all the MOS transistors, the differential gain of this active-loaded MOS pair is given by [6, 21]:

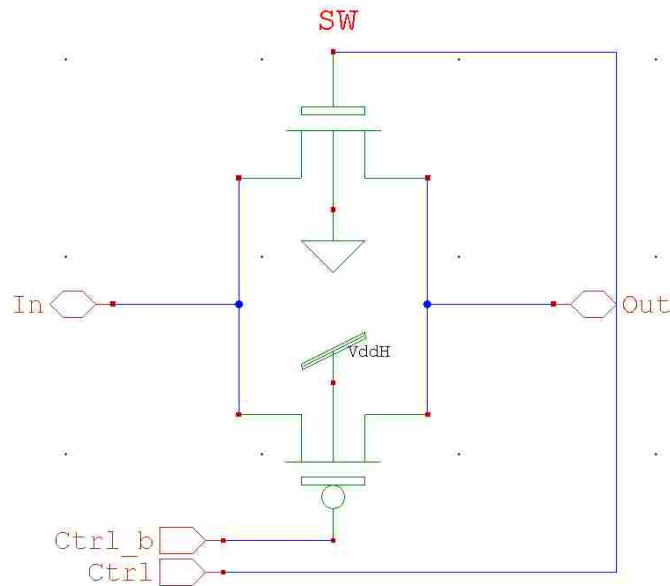


Figure 3.3: The schematic of the analog switch used.

where μ_n is the charge-carrier effective mobility and C_{ox} is the gate oxide capacitance per unit area of the transistor. Equation 3.5 shows that the $\frac{W}{L}$ ratio directly affects the DC bias current and, as a result, the differential gain. Table. 3.1 presents the numerical values of the Op-Amp design parameters. In this design, $\frac{W}{L} = 1.57$ has been selected. Another parameter that plays a key role in the operation of the active-loaded amplifiers is the MOS output resistance, which is controlled by parameter λ .

Now assume that the source-degeneration resistance of the current source is R_{SS} . Then the common-mode gain and CMRR of the differential level is calculated as follows [6,21]:

$$A_{cm} = -\frac{1}{2R_{SS}} \frac{r_o}{1 + g_m r_o} \approx -\frac{1}{2g_m R_{SS}}$$

$$\text{CMRR} = \frac{|A_d|}{|A_{cm}|} \approx g_m^2 r_o R_{SS}. \quad (3.6)$$

To obtain a higher CMRR, the biasing circuit should provide higher output resistance r_o . Furthermore, the current source should provide higher source-degeneration resistance R_{SS} .

The working bandwidth of the Op-Amp circuit is dictated by the overall input capacitance and input resistance. The low-pass behavior of the circuit is shown in Figure 3.5, where the 3dB gain of $BW_{3dB} = 52.47$ MHz has been calculated from the frequency response. The schematic of the testing circuit is also shown in Figure 3.6. Figure 3.7 and Figure 3.8 show the test circuit used to characterize the propagation delay and its output waveform. The same configuration was then used to calculate the dynamic range of the circuit as shown in Figure 3.9 and 3.10.

3.1.4 Analog Buffer Circuit

Analog buffer is mainly used to provide a noiseless regulated voltage for the next digital stages. As shown in Figure 3.10 , an Op-Amp with a direct negative feedback is used as a

buffer. The dynamic range of the buffer circuit is 0.746 V-15 V, within which the output voltage has no distortion.

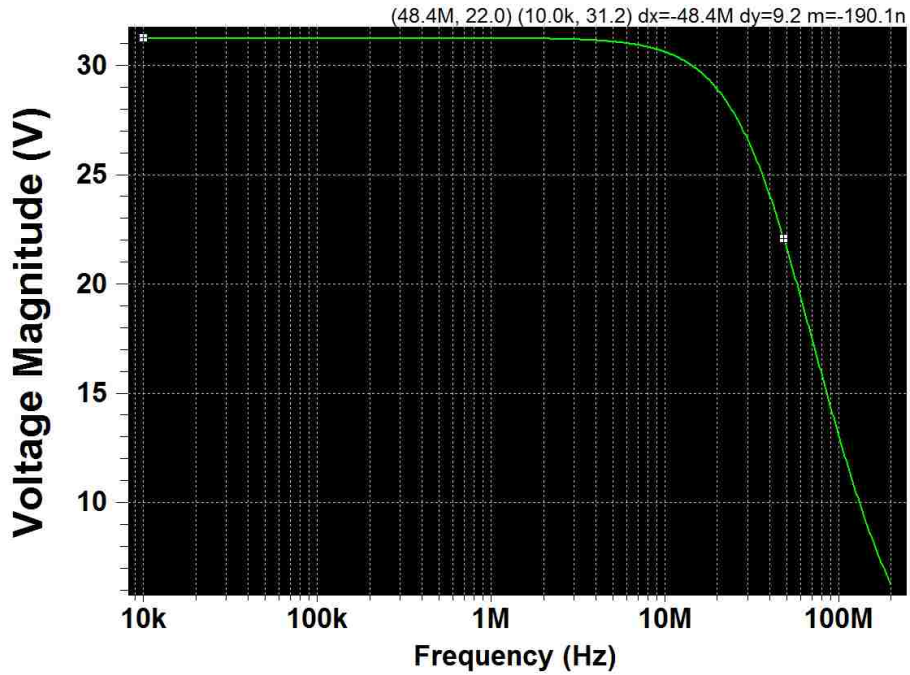


Figure 3.5: The frequency response of the Op-Amp circuit.

Table 3.1: The parameters of the Op-Amp circuit

Temperature	300 K	80 K
Gain	68.8 dB	82.8 dB
3dB Bandwidth	48.29 MHz	69.98 MHz
Static Power	1.63 mW	1.71 mW
Dynamic Range	0.61 V- 15 V	1.19 V- 15 V
Propagation Delay	$t_{LH} = 0.296$ ns, $t_{HL} = 1.27$ ns	$t_{LH} = 0.127$ ns, $t_{HL} = 0.847$ ns
$\frac{W}{L}$	1.57	1.57

The schematic of the overall designed unit cell is presented in Figure 3.11, where the previously described components have been used.

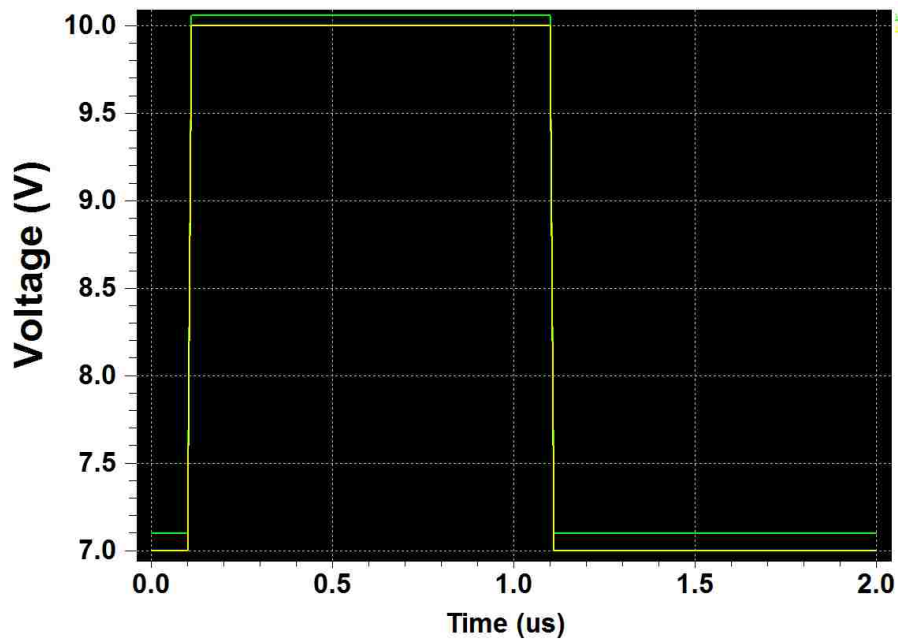


Figure 3.7: The transient characteristic of the Op-Amp buffer circuit (for temperature = 300K).

- CP0 and CP1 : clock inputs.
- MR : overriding asynchronous master reset input.

The counter is advanced by either a LOW-to-HIGH transition on CP0 while CP1 is LOW or a HIGH-to-LOW transition on CP1 while CP0 is HIGH¹. A HIGH on MR resets the counter to zero (Y0 = Y059b = HIGH; Y1 to Y9 = LOW) independent of the clock inputs (CP0 and CP1b).

Figure 3.12 shows the relationship of D flip-flop outputs (Q1-Q5) and the circuit outputs (Y0-Y9). DeMorgan's theorem can be formulated as shown in equation 3.7:

¹in our simulations the counter is advanced by a LOW-to-HIGH transition on CP0 while CP1 is LOW

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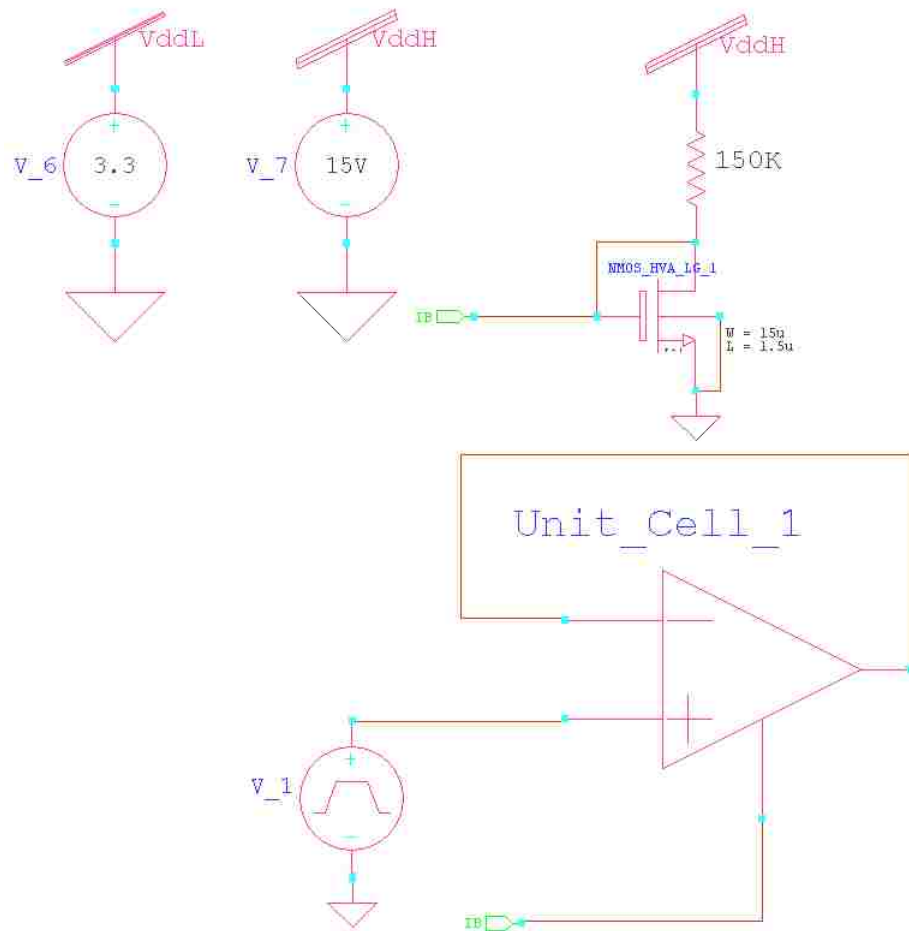


Figure 3.8: Schematic of the test circuit used to characterize the transient behavior.

$$Y_0 = \overline{Q_1} \cdot \overline{Q_5}$$

$$Y_1 = \overline{Q_2} \cdot Q_1$$

$$Y_2 = Q_2 \cdot \overline{Q_4}$$

$$Y_3 = \overline{Q_3} \cdot Q_4$$

$$Y_4 = \overline{Q_5} \cdot Q_3$$

$$Y_5 = Q_1 \cdot Q_5$$

$$Y_6 = \overline{Q_1} \cdot Q_2$$

$$Y_7 = \overline{Q_2} \cdot Q_4$$

$$Y_8 = Q_3 \cdot \overline{Q_4}$$

$$Y_9 = \overline{Q_3} \cdot Q_5$$

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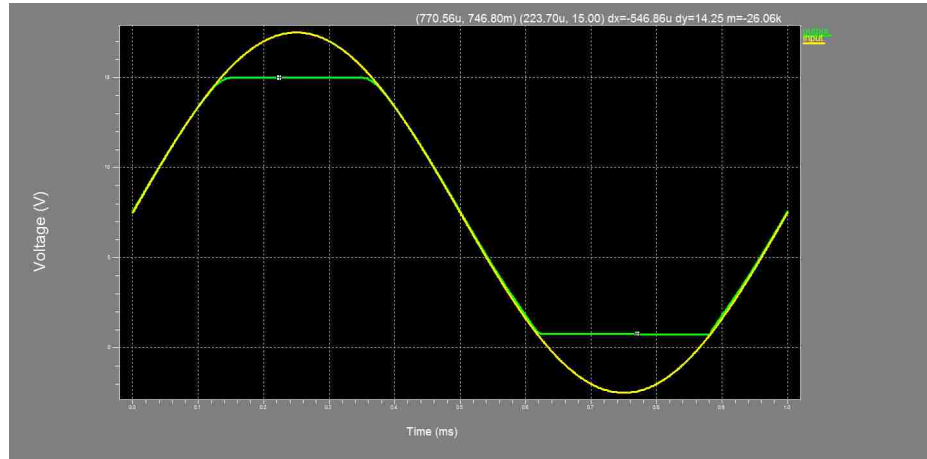


Figure 3.9: The dynamic range of the Op-Amp buffer circuit.

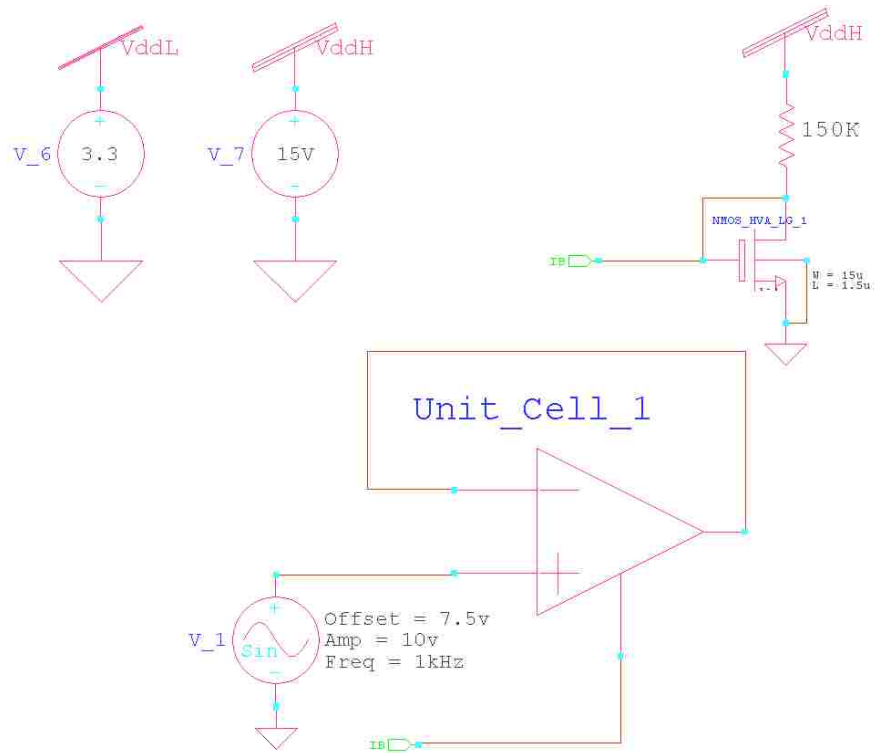


Figure 3.10: Schematic of the test circuit used to calculate the dynamic range.

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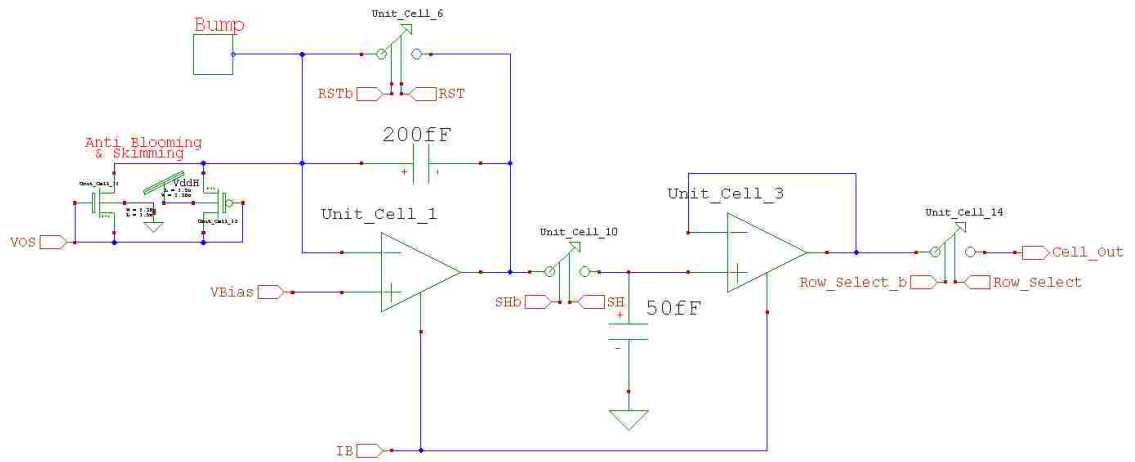


Figure 3.11: The overall design of the unit cell circuit.

To show how the circuit in Figure 3.12 works, we first assume that the clock is 0 and as a result the outputs of the D flip-flops (Q1-Q5) are to be 0, which sets the Q5b and Y0 to 1 and the rest of the output values (Y1-Y9) to be remain at 0. In the next stage with the

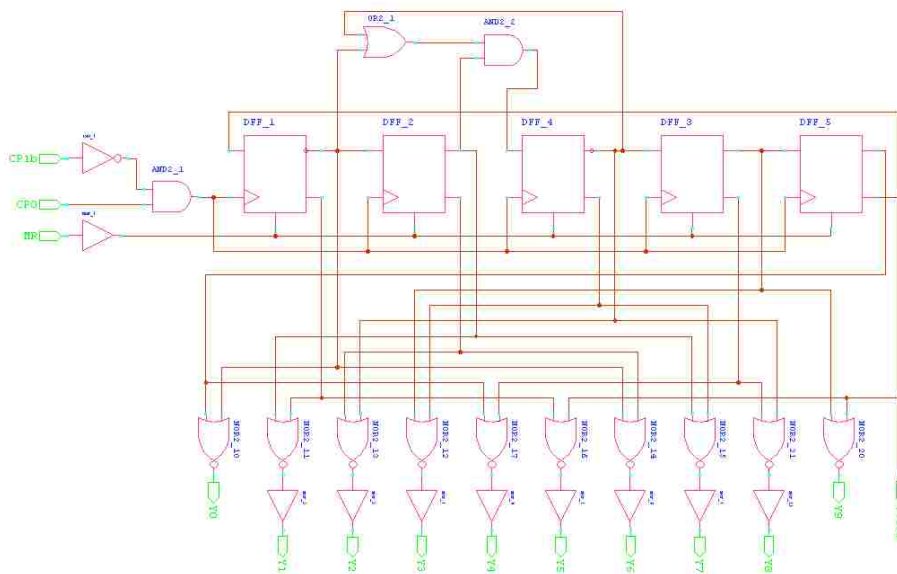


Figure 3.12: 10-bit-counter schematic.

Table 3.2: Circuit input/ output definitions [22]

CP1b	The CP1b input should be low (0V) for normal operation. When high it disables counting so that clock pulses are ignored and the count is kept constant.
CP0	The count advances as the CP0 input becomes high (on the rising-edge), which CP0 input acts just like a normal clock.
MR	The Master Reset input should be low (0V) for normal operation (counting 0-9). When high it resets the count to zero (Y0 high). Counting to less than 9 is achieved by connecting the relevant output (Y0-Y9) to reset, for example to count 0,1,2,3 connect Y4 to reset.
Q1-Q5	D flip-flop outputs.
Y0-Y9	Each output Y0-Y9 goes high in turn as counting advances.
YO59b	Active LOW output from the most significant flip-flop (Q5b) which will be used for cascading the decade counters.

clock pulse (CP0) rising from low to high Q1 gets the previous value of Q5b, which is 1 and Q2, Q3, and Q5 in the same order get the previous values of Q1, Q4, and Q3, which used to be 0. The current value of Q4 depends on the previous value of Q1, Q2, and Q4, which in this case is 0. Using the formulas in (. 3.7), Y1 will be 1 and the rest of the output values will be 0. The output values in the next stages can be derived in the same manner, which are summarized in table Table 3.3.

The schematic in Figure 3.13 is used to generate the output waveforms of the counter circuit. As we will discuss later, the 10-bit counter will be used as a building block for column-select and row-select circuits. The output waveform is shown in Figure 3.15.

In order to have a larger counter (more than 10 bits), we need to cascade the 10-bit counters together. The schematic of cascading the 10-bit counter is shown in Figure 3.14. Once the value of the last bit from any block is set to 1, the current block will be disabled and, at the same time, the clock starts to affect the next block. Also, by connecting the MR input of each stage to the first output of its previous neighbor, the block will not be functional, while the clock pulse starts to affect the outputs. This procedure is repeated till the last block, when the last output is fed back to the first stage to reset the whole circuit.

Table 3.3: Circuit output values

CLK	0	1	2	3	4	5	6	7	8	9	10
Q1	0	1	1	1	1	1	0	0	0	0	0
Q2	0	0	1	1	1	1	0	0	0	0	0
Q3	0	0	0	0	1	1	1	1	1	0	0
Q4	0	0	0	1	1	1	1	1	0	0	0
Q5	0	0	0	0	0	1	1	1	1	1	0
Y0	1	0	0	0	0	0	0	0	0	0	1
Y1	0	1	0	0	0	0	0	0	0	0	0
Y2	0	0	1	0	0	0	0	0	0	0	0
Y3	0	0	0	1	0	0	0	0	0	0	0
Y4	0	0	0	0	1	0	0	0	0	0	0
Y5	0	0	0	0	0	1	0	0	0	0	0
Y6	0	0	0	0	0	0	1	0	0	0	0
Y7	0	0	0	0	0	0	0	1	0	0	0
Y8	0	0	0	0	0	0	0	0	1	0	0
Y9	0	0	0	0	0	0	0	0	0	1	0

Table 3.4 presents the rise-time, fall-time and propagation delay of the cascaded circuit for two different temperatures. It can be seen that the time constants experience smaller values for lower temperatures, which can be explained by the fact that the semiconductor circuit is faster at lower temperatures.

Table 3.4: Circuit input/ output definitions

Quantity	Temp	300 K	80 K
Rise Time (ps)		85.1	59.5
Fall Time (ps)		82	54.2
Propagation Delay (ns)		3.02	2.89

3.3 Layout Design

In this section we represent the layout design for final ROIC circuit of the previous section. Layout design is the final step in the digital circuit design cycle. The output of the layout

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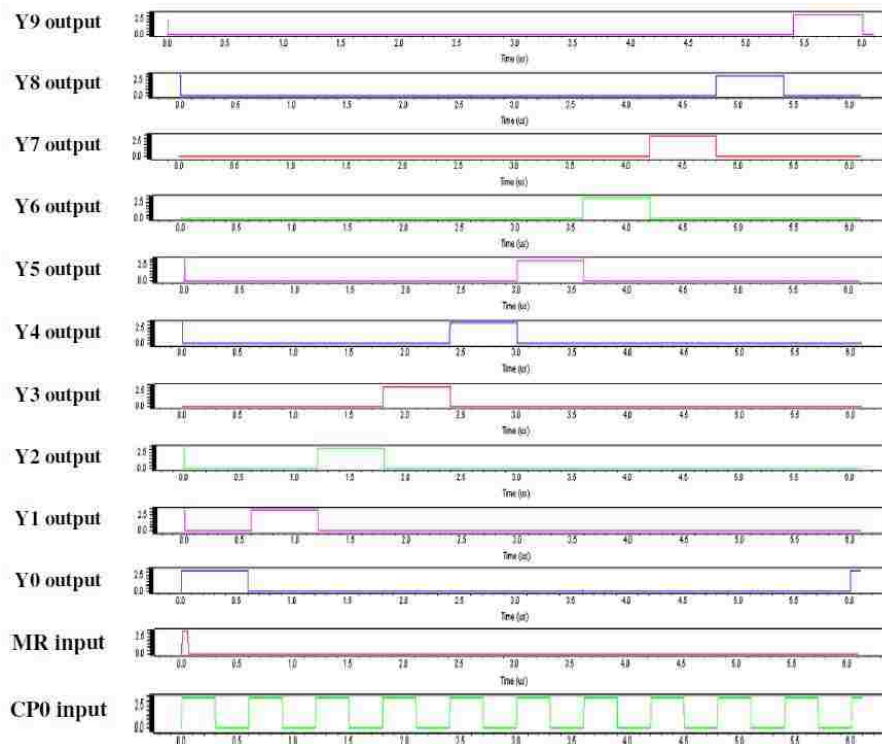


Figure 3.15: Circuit input/output waveforms.

designing the layout.

Figure 3.16 shows the layout of the CMOS analog switch. As explained earlier an analog switch is used in both the integration and the S&H circuits. The layout of the differential active-loaded amplifier is shown in Figure 3.17 where 6 transistors are used.

Figure 3.19 represents the overall layout design of a unit cell. As shown below the size of the unit cell is 30 microns by 30 microns for a 128x128 FPA. As shown on the figure, there exist two large capacitors in the layout: one in the S&H circuit and one in the integration circuit. Five percent and twenty three percent of the total area have been used for these two capacitors respectively. It is worth mentioning that two different methods have been used to design the integration and S&H capacitors.

The integration capacitor is implemented using a POLY2 layer and POLY layer. The

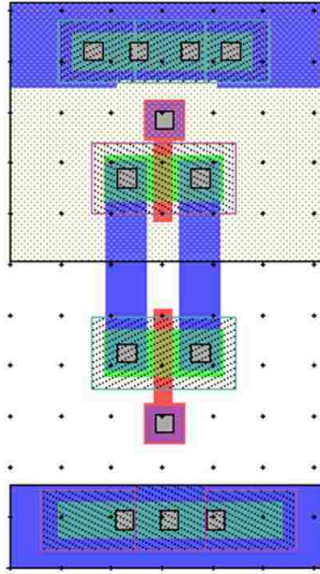


Figure 3.16: Layout of the analog switch (a part of the unit cell circuit).

two layer act as the parallel plate. The linear (and fixed) value of the capacitor is calculated using $C = C_{P2P}WL$, where W and L are the width and the length of the polysilicon layer and C_{P2P} is the capacitance of POLY2 to POLY per unit area. The value of C_{P2P} for AMI $0.5 \mu m$ process is $2.4 \text{ fF}/\mu m^2$ [4], which results in a 500 fF integrator capacitance. Note that the value of the capacitance in this case is constant and not a function of the applied voltage. This is necessary for the integrator capacitor to provide a linear behavior. However, the S&H capacitor is built via an NMOS transistor as shown in Figure 3.18.

In this case, based on the applied voltage, the operating region of the transistor changes which results in a nonlinear effect. Table 3.5 shows the value of the capacitor in different regions [20].

Table 3.5: The channel capacitance based on the operating region

Operating Region	C_{GB}	C_{GS}	C_{GD}
Cut-off	$C_{ox}WL_{eff}$	0	0
Linear	0	$\frac{1}{2}C_{ox}WL_{eff}$	$\frac{1}{2}C_{ox}WL_{eff}$
Saturation	0	$\frac{2}{3}C_{ox}WL_{eff}$	0

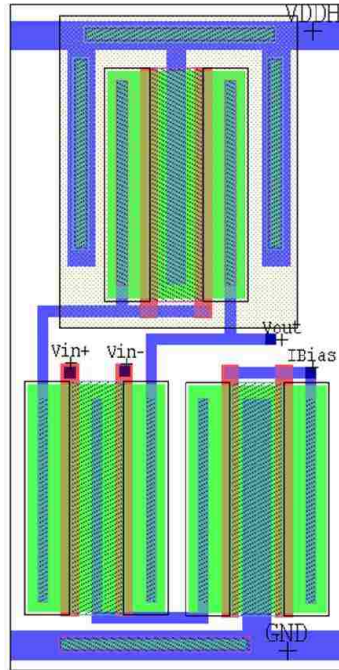


Figure 3.17: Layout of the active-loaded amplifier (a part of the unit cell circuit).

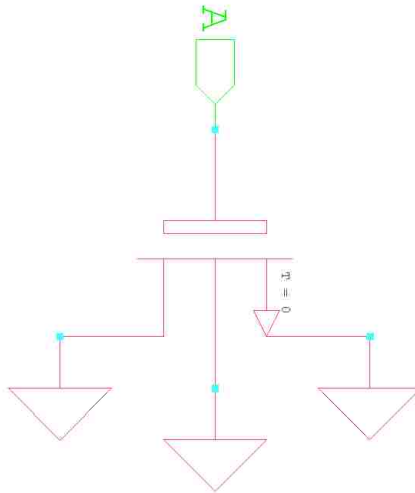


Figure 3.18: Schematic of a NMOS transistor used as a nonlinear capacitor.

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In Table 3.5, L_{eff} is the effective length of the depletion region which varies as a function of the applied voltage. As shown in Table 3.5, the channel capacitance is a non-linear function of the applied voltage and varies rapidly as the gate voltage (and as a result the operating region) changes. However, this is fine for the S&H circuit. The resulting capacitance is then calculated as

$$C = C_{GS} + C_{GD}. \quad (3.8)$$

The provided design formulas are then used to calculate the required W and L based on the capacitance needed. The calculated values, however, are not precise. That is due to the fact that the values provided in Table 3.5 are only an approximation. To get a value close enough to desired value, one should follow an iterative trial and error procedure. Fortunately, the CAD tools can provide a precise estimate of the designed capacitor after the layout is designed.

The layout of the Row/Column select circuit is shown in Figure 3.20. The final layout of the ROIC which uses the layouts of the unit cell and the Row/Column circuit is shown in Figure 3.21.

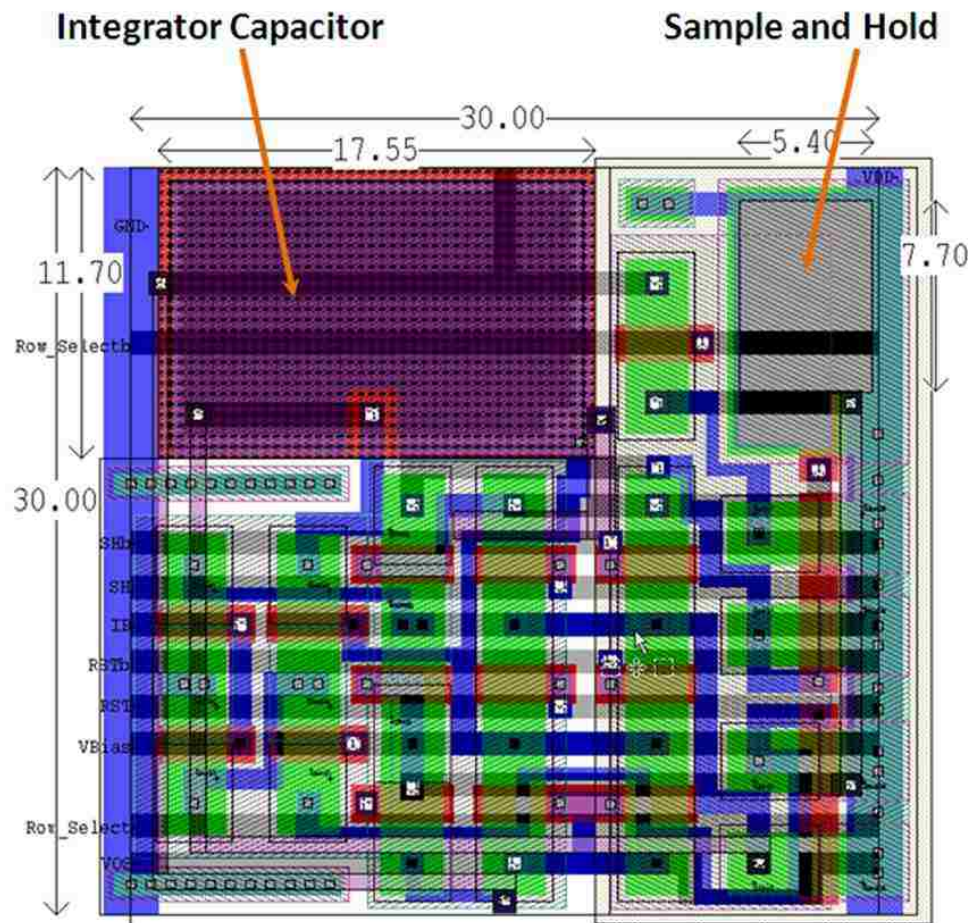


Figure 3.19: Overall layout of a unit cell.

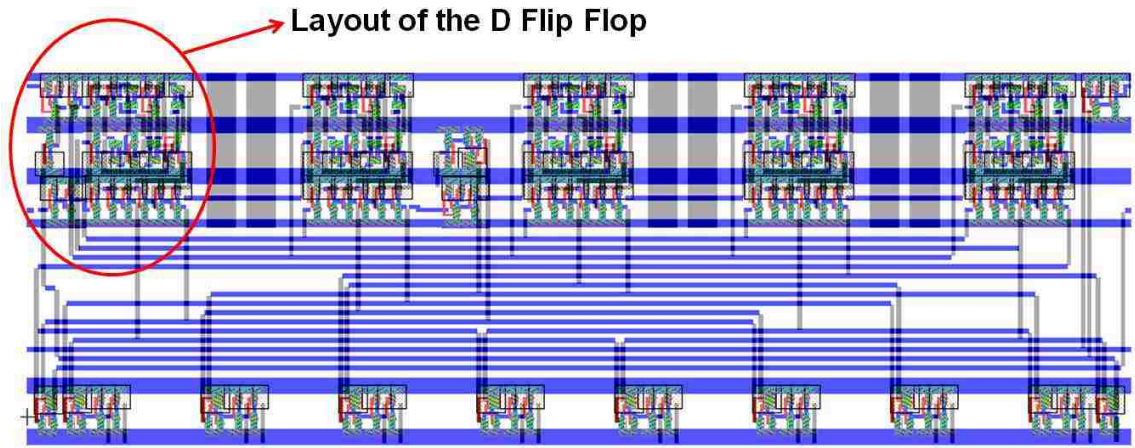


Figure 3.20: Layout of the row/column select circuit.

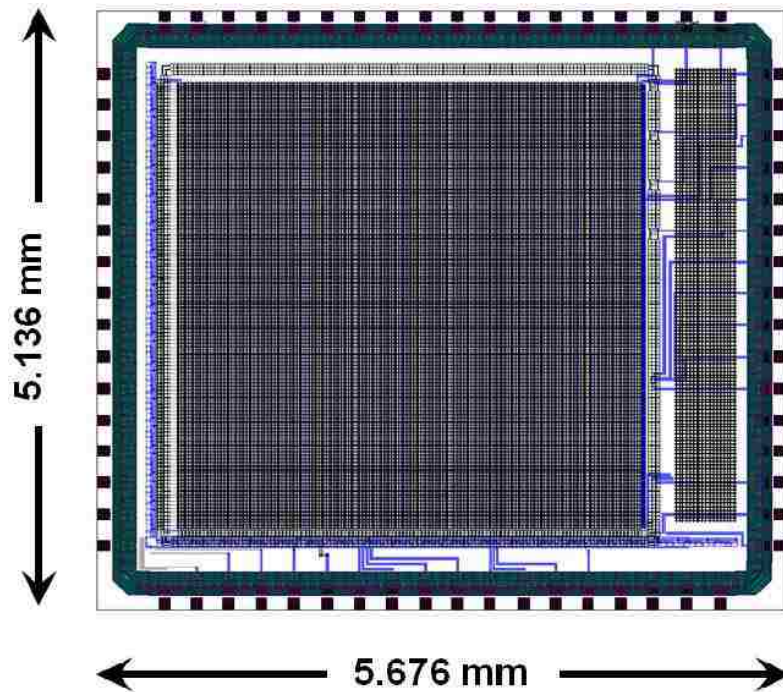


Figure 3.21: Complete layout of the ROIC.

Chapter 4

Testing and Measurements

In the Center for High Technology Material (CHTM) at the University of the New Mexico, test bed has been developed to test the designed ROIC circuit. This test bed is a replacement for the complex digital processing unit that is usually shipped with the third party IR imaging solutions. For example Figure 4.1 shows a complete IR imaging system using Indigo ROIC [8] which includes an onboard DSP card, a temperature controller and several interface circuits. A typical system like the one shown in Figure 4.1 costs around \$50,000. Therefore, it is frugal and wise to design a low cost test/processing unit that can be used as an alternative for existing expensive systems. Such a system should also provide full control over the ROIC interface circuit and must be designed to be compatible for a large class of ROIC circuits including our proposed one. In the following, we explain the ROIC test circuit designed and built at the CHTM and provide some preliminary results obtained using two Indigo ROICs. Note that our designed ROIC has not been tested completely yet. However, we provide some guidance regarding how to test the designed ROIC using this test bed. Further testing/debugging of the ROIC circuit is left as a future work.

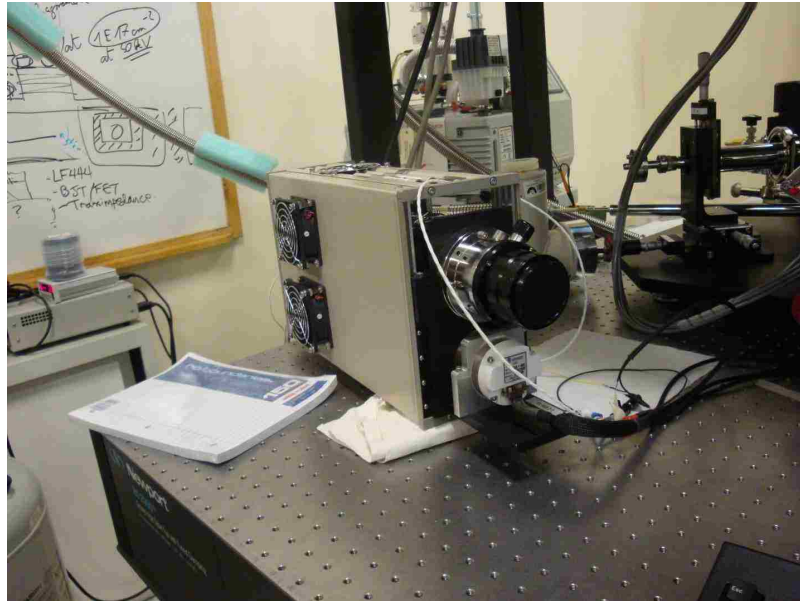


Figure 4.1: A typical commercial IR imaging system with integrated temperature controller and DSP board.

4.1 The UNM ROIC Test Procedure

The UNM 128x128 ROIC is designed based on CTIA using TSMC 0.35um double poly, 4 metal layers, and high voltage process. The unit cells are on a 30um x 30um pitch with the well capacity of at least $2e6$ electrons. The current version of this ROIC supports only single output, full window operation. One of the unique characteristic of this ROIC is its large bidirectional bias voltage range. The block diagram and layout of the ROIC designed at UNM is shown in Figure 4.2. It consists of 128x128 unit cell at 30um x 30um pitch. The readout timing is similar to Indigo chip, where by setting LSYNC and FSYNC the cell can be read as Integrate-While-Read timing or Integrate-Then-Read timing.

The unit cell architecture of the ROIC is shown in Figure 4.3. The integration is performed using CTIA techniques as explained before. Currently, the gain control is disabled in this version of the ROIC and the overall path gain is set to 1.0.

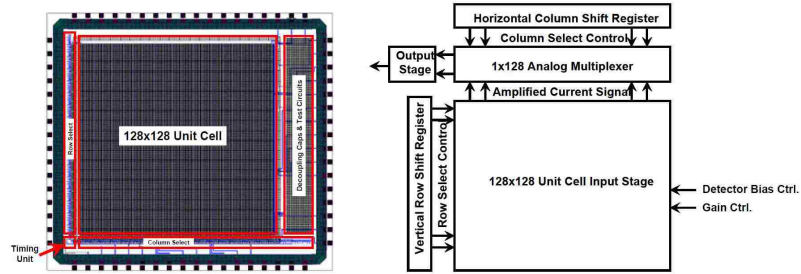


Figure 4.2: UNM ROIC layout and block diagram.

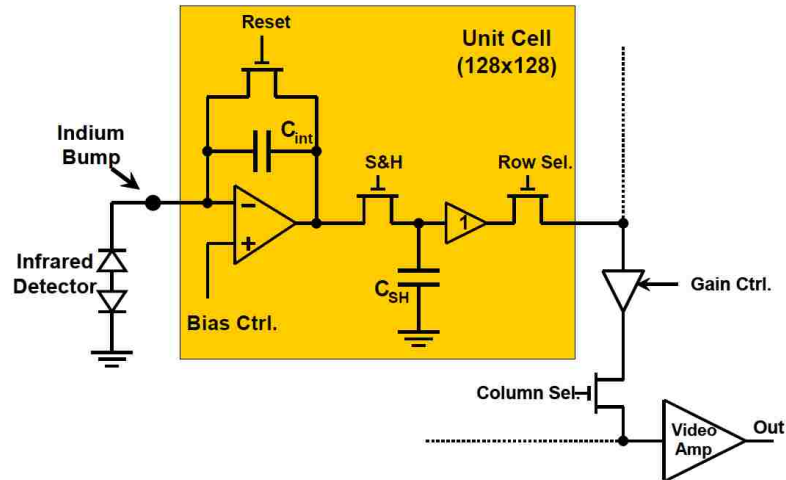


Figure 4.3: The overall architecture of the unit cell.

4.1.1 UNM ROIC Pin Diagram

The pin diagram of the ROIC is shown in Figure 4.4. The ROIC is die attached and bonded into a 68 pin LCC package. The test procedures in this document will be applied only on the red pins shown in Figure 4.4. For now, we have only bare silicon ROIC available for the test. The list of the pins used for the preliminary test is listed in Table 4.1.

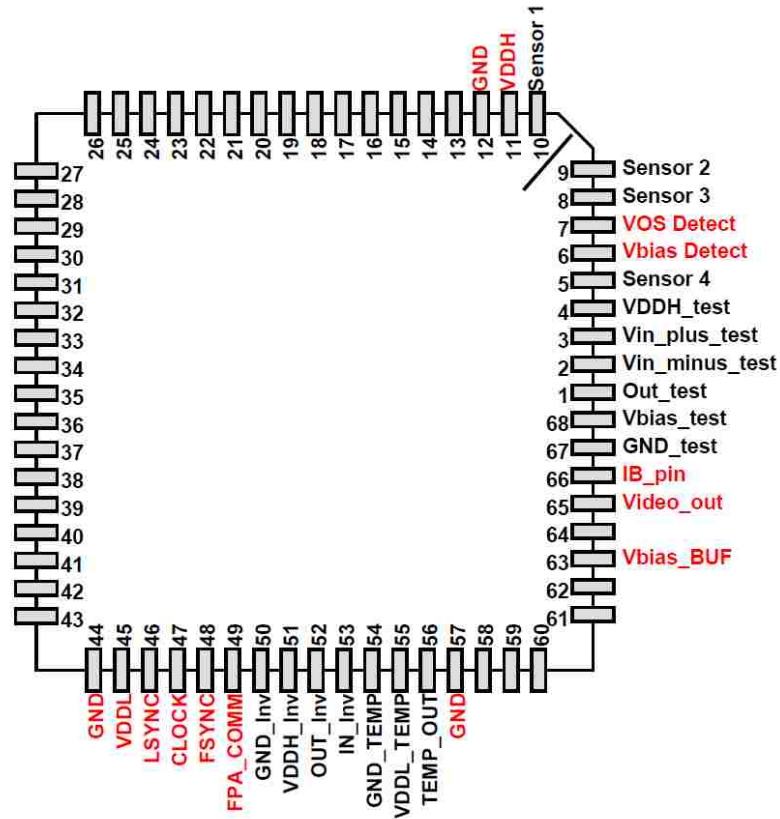


Figure 4.4: The pin diagram of UNM ROIC.

4.1.2 More On Pin Descriptions

Here we provide more information on UNM ROIC pins:

- VDDH, VDDL, and GND are the power supply pins.
- Clock, LSYNC, and FSYNC are timing signals. Similar to Indigo, the following timing pattern can be applied to read the ROIC as Integrate-While-Read timing or Integrate-Then-Read timing. The timing diagram is shown in Figure 4.5. However, unlike Indigo, in this ROIC the pixel rate is equal to the clock rate (not double that rate). The first two rows and the first six columns of the readout data are used for

timing setups and are not valid data. Similar to Indigo, the readout starts from the lower left pixel of the array and scans horizontally.

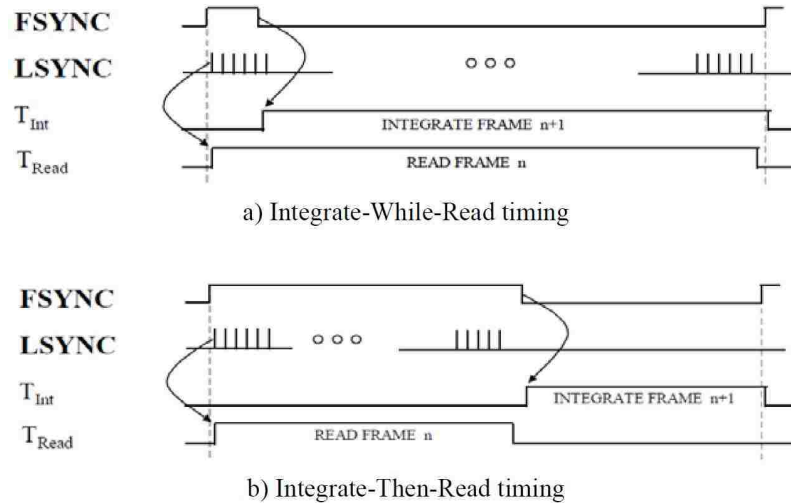


Figure 4.5: FSYNC and LSYNC timings for integration mode setting.

- VOS_Detect is used for anti-blooming and/or dark current compensation. It must be shorted to Vbias_Detect for the initial testing. However, if, during the initial testing, the output of CTIA saturates, VOS_Detect can be used to compensate the input offset of CTIA.
- IB_pin is the unit cell bias current adjustment. To limit the total chip power dissipation to about 4 W, a current of 15 μ A must be fed to this pin. This can be done by connecting the pin to VDDH through a 470 kohm resistor to the supplied voltage source.
- Video_BUF is the driver current control of the video amplifier. The bias current can be delivered by connecting the pin to VDDH through a 22 kohm resistor.
- Video_Out is the output video signal. The total path gain of the system is 1.0, therefore the output signal may need some gain for bare silicon test. In this version of

ROIC, the reference for the output video signal is V_{bias_Detect} and the total swing is from GND to VDDH. For example, if we set V_{bias_Detect} to 4.0 V, the output video signal can range from 4.0 to 8.0 V or 4.0 to 0 V, depending on the direction and magnitude of the detector current.

4.2 The Structure of The ROIC Test bed

The ROIC test bed was originally implemented to serve as a interface/test board for Indigo-based IR imaging systems. However, it has been designed as general as possible to ensure versatile future use for UNM ROIC too. As a starting point, the original implementation of a sample indigo-based IR imaging systems was explored. The commercial IR imaging system used along with its Liquid Nitrogen (LN_2) dewar is shown in Figure 4.6. The overall hardware architecture of the system is shown in Figure 4.7.

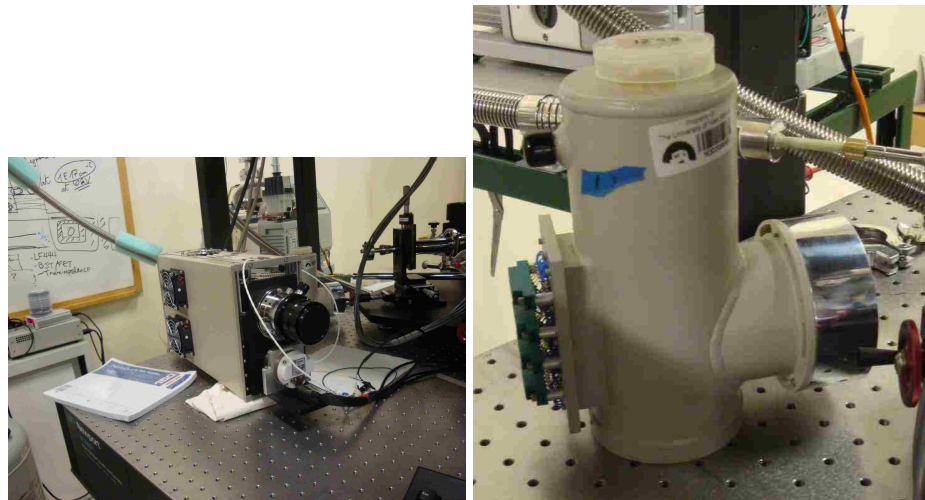


Figure 4.6: The reference commercial IR imaging system used at CHTM. The DSP board is shown in the left where the Liquid Nitrogen (LN_2) dewar is shown in the right.

As shown in Figure 4.7, the system is software controlled and is interfaced to a PC with an analog video card installed. The video card is used to transfer the IR video frames to the

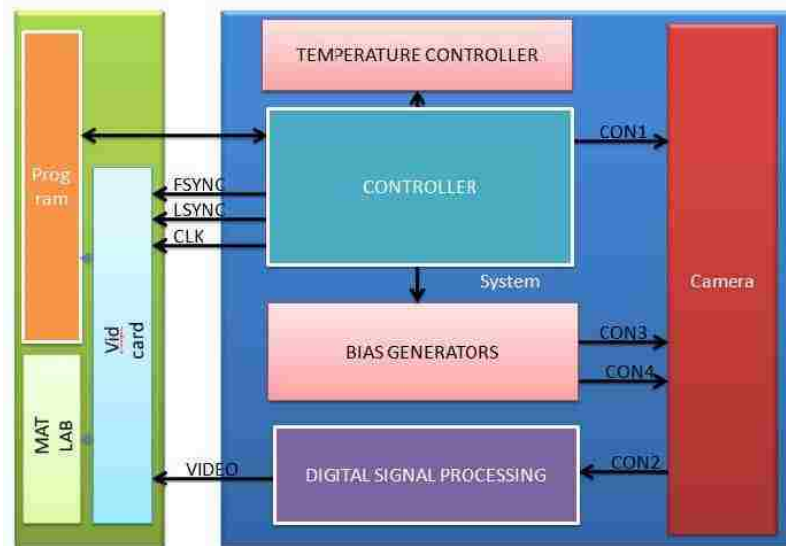


Figure 4.7: The hardware architecture of the commercial IR imaging system used at CHTM.

PC to be displayed on the screen. The same structure is followed in the implementation of the ROIC test bed: we use a video grabber card to transfer the analog video frames to the PC. However, unlike the commercial system, we use an FPGA board along with some signal conditioning circuits to generate the control signals (LSYNC, FSYNC, CLK, etc.). The NI PCI 1410 video grabber card has been chosen to convert the analog video signal to digital frames to be shown on the screen. These digital frames can then be used for further processing. In order to generate the control signals we use a Xilinx Spartan 3E FPGA board. Note that, in the future, more compact prototypes can be designed. The overall hardware architecture of the designed systems is shown in Figure 4.8. The designed circuit and the block diagrams presented in this thesis are courtesy of Philippe Nguyen [17].

In order to connect the FPGA board to the dewar, some signal conditioning is required. For instance, to generate the bias voltage of the ROIC ($0 \sim 5 \text{ V}$), a simple circuit using an LM317 linear regulator has been designed. Also, since the VCC of the FPGA board is

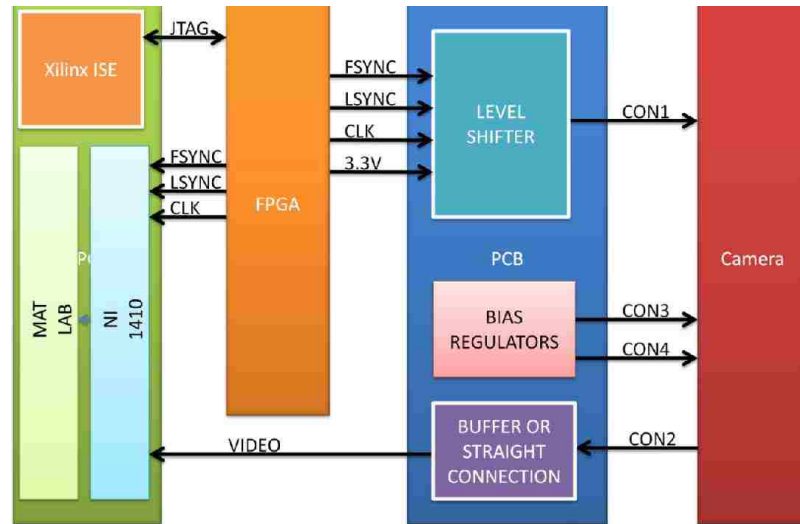


Figure 4.8: The hardware architecture of the designed PC-based IR imaging system.

3.3 V, a level shifter is required to shift the control signals generated by the FPGA board to 5.0 V. Note that the level shifter must be fast enough to work with the frequency of the video grabber. We used an MAX3379E level shifter that is guaranteed to work up to 8.0 Mhz. Finally, the output analog video signal should be buffered and in order to do that, a TLO82 Op-Amp is used in buffer configuration. The overall signal conditioning circuit is packaged into a single PCB. Figure 4.9 shows the schematic of the signal conditioning circuit.

4.2.1 Result For Indigo Third Party ROICs and Guidelines For Testing UNM ROIC in Future

After several preliminary tests, the designed test bed was successfully interfaced to the Indigo ROIC 9705. The Figure 4.10 shows some IR images taken using the designed test bed. The designed test bed is ready to test the UNM ROIC with minimal modifications.

Chapter 4. Testing and Measurements

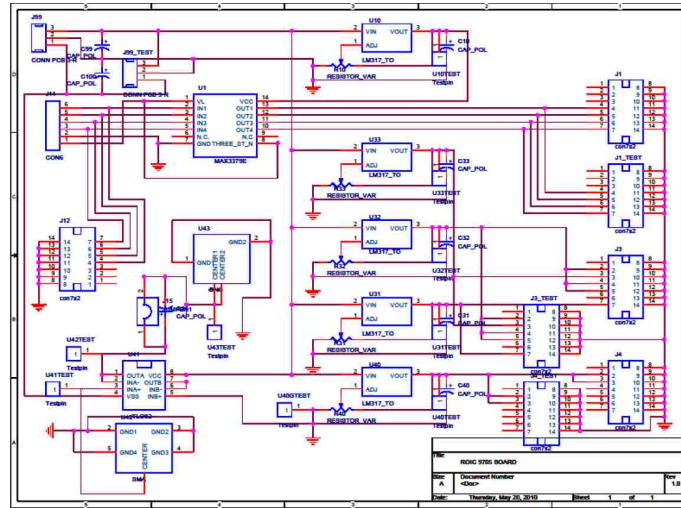


Figure 4.9: The schematic of the signal conditioning circuit [17].

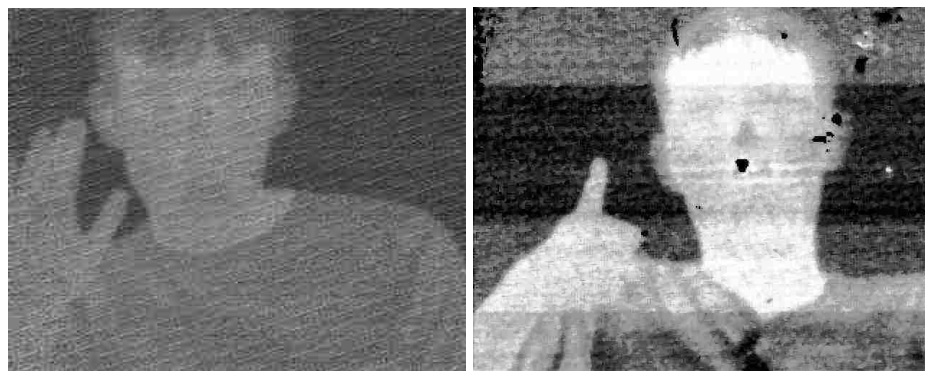


Figure 4.10: Some results using the designed test bed and Indigo ROIC [17].

Table 4.1: Summary of the pin descriptions

Pin Number	Pin Name	Pin Description
11	VDDH	This is a 8.0V DC power supply for analog parts
46	VDDL	This is a 3.3V DC power supply for digital parts
44, 67, and 12	GND	Ground pins
47	CLOCK	This is a 5MHz clock with 3.3V swing to get about 60 F/S rate
46	LSYNC	Line Sync pulses with 3.3V swing similar to Indigo chip
48	FSYNC	Frame Sync pulses with 3.3V swing similar to Indigo chip
6	Vbias_Detect	Detector Bias, to be set at 4.0V for initial test but can be adjusted from 1.5V 6.5V
49	FPA_COMM	Detector common potential or analog reference voltage= 4V, can be left open in bare silicon test
7	VOS_Detect	A DC voltage for Idark compensation, to be shorted to Vbias_Detect (pin 6) for initial test
66	IB_pin	Unit cell bias current adjustment, connect to VDDH via a 470KOhm resistor
63	Video_BUF	Output video drive control, connect to VDDH via a 22KOhm resistor
65	Video_Out	Output video, may need some external signal condition

Chapter 5

Conclusion and Future Work

In this thesis, we explained the design of a high speed, low noise Readout Integrated Circuit (ROIC) for Infra Red (IR) imaging applications. The quality of the IR imaging systems depends on 1) the sensitivity of the Focal Plane Arrays (FPA) as the transducer of the electromagnetic wave and 2) the readout integrated circuit (ROIC) that provides the pixel data to the processing unit. We started with ROIC unit cell, where we provided the schematics of different parts of our designed unit cell circuit and analyzed the behavior of each part through Spice simulations. We then proceeded with the design of row/column select circuit, where we explained how FSYNC and LSYNC signals (used to generate a serial stream of the pixel values) are generated. The layout of the ROIC circuit was performed using Tanner EDA tools. Finally, we explained a general purpose ROIC test bed developed at the Center for High Technology Materials (CHTM), University of New Mexico, for use in testing the Indigo-Based IR imaging systems as well as our designed ROIC.

As for the future extension, we will test our designed ROIC on a practical IR camera system. The CHTM ROIC test bed has not been used to test our ROIC yet. So far, only an Indigo-based IR camera system has been tested using this test bed. However, the test

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bed was designed to support both Indigo and UNM ROICs with minor modifications. Therefore, the next step will be to prepare the CHTM test bed to test our designed ROIC. Once we are able to test our ROIC circuit, we can debug any possible design errors and modify the circuit accordingly.

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