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ANALOG MULTIPLY AND ACCUMULATE FPA READOUT CIRCUIT WITH DIGITAL MULTIPLY AND SIGN MAINTENANCE

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THESIS

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ANALOG MULTIPLY AND ACCUMULATE FPA READOUT CIRCUIT WITH DIGITAL MULTIPLY AND SIGN MAINTENANCE

By

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B.S Electrical Engineering, University of New Mexico, 2008
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ABSTRACT

The high bandwidth and power needed to process the data coming from modern high resolution focal plane arrays leads to the necessity for fast and efficient read out and data processing. A system that performs block recognition and image classification with efficiency and low latency is presented.

The system is comprised of an analog signal processor that will be integrated into the read out integrated circuit. This enables the capability to read out the focal plane array information and process it completely in the analog domain in a comparably very small amount of operational steps.

The steps and techniques of the design flow, including definition of problem, concepts and design of system architecture, simulation of system, and analog lay out practices are covered.

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Chapter 1

Introduction

1.1 Background Information

Image classification and region recognition are commonly used image processing algorithms. The ability to break down an image's features into separate blocks has many potential uses, ranging from surveillance to manufacturing feature recognition.

Image classification is generally carried out by running an image through a number of filters. Each filter targets a specific light wave frequency, and when applied to a two-dimensional image signal, it will output only the elements of the signal that are within the filter's pass-band. If a set of filters that cover the entire image frequency are applied, then each image pixel can be categorized into a certain frequency pass-band.

Figure 1.1 is a diagram of the algorithm that will be used to create the different frequency target filters. It shows that the algorithm used to create these spectrum filters are based on the form $I_{out} = W_1 * I_1 + W_2 * I_2 + W_3 * I_3 + W_k * I_k$. Figure 1.2 shows the typical architecture of a system that would implement this filter architecture. The "FPA" block is a focal plane array, which is used to capture the light and generate the photocurrents. The "ROIC" is a read out integrated circuit; used to convert/buffer/amplify the photocurrents into voltages. The "ADC" is an analog to digital converter. The storage unit could be any kind of digital data storage. Finally, the central processing unit is some kind of digital signal processing block.

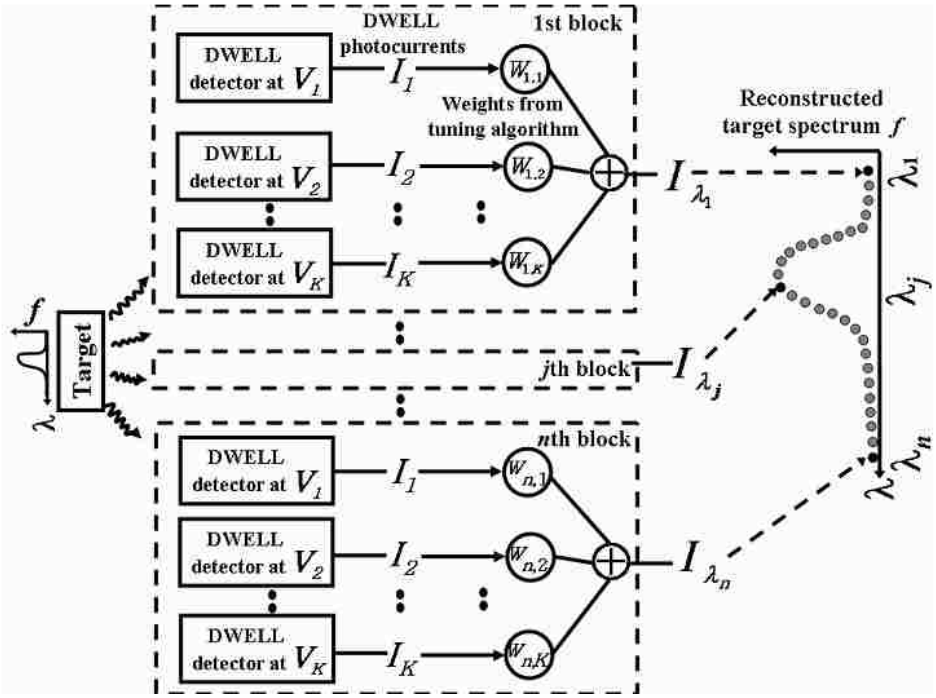

Figure 1.1: Graphical representation of the filtering technique used for spectrum recognition [6]

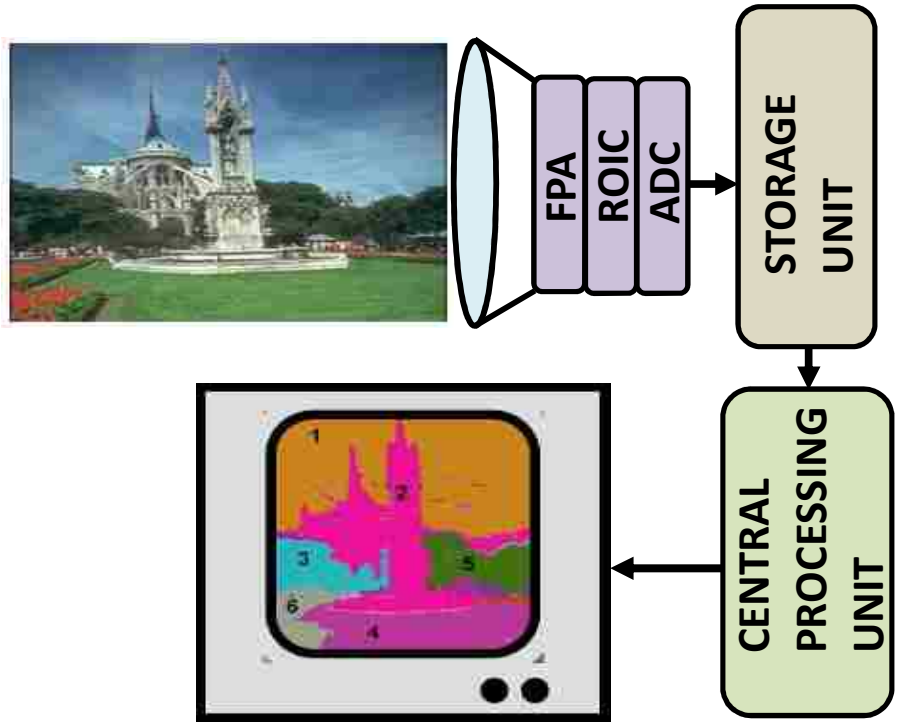

Figure 1.2: Typical architecture for implementing the algorithm shown in figure 1.1 [6]

1.2 Statement of Problem

The system shown in Figure 1.2 has some limitations and drawbacks due to the digital signal processing architecture scheme. First, in order to process an analog signal digitally, it must be converted to a digital signal with an ADC. Second, the connection from the ROIC/ADC to the storage unit needs to have a large bandwidth capability in order to process high resolution images at video frame rates. Finally digital data must be processed in a separate system which will add another stage of complexity and latency.

1.3 Thesis Introduction and Proposal

This thesis covers a circuit that will handle the multiply and accumulate spectral filters within the ROIC itself. The circuit will process the photocurrent signals in the analog domain without the use of a storage element or digital processing system. The ADC will also be replaced by a simple analog comparator network. The comparator network will enable the ability to apply numerous filters in parallel, and then sense which filter best matched with the image data. This comparator network is not within the scope of this thesis, and is mentioned for the sake of discussing the overall system. The proposed system is shown in Figure 1.3. Note that the processed image will come directly from the signal processing ROIC.

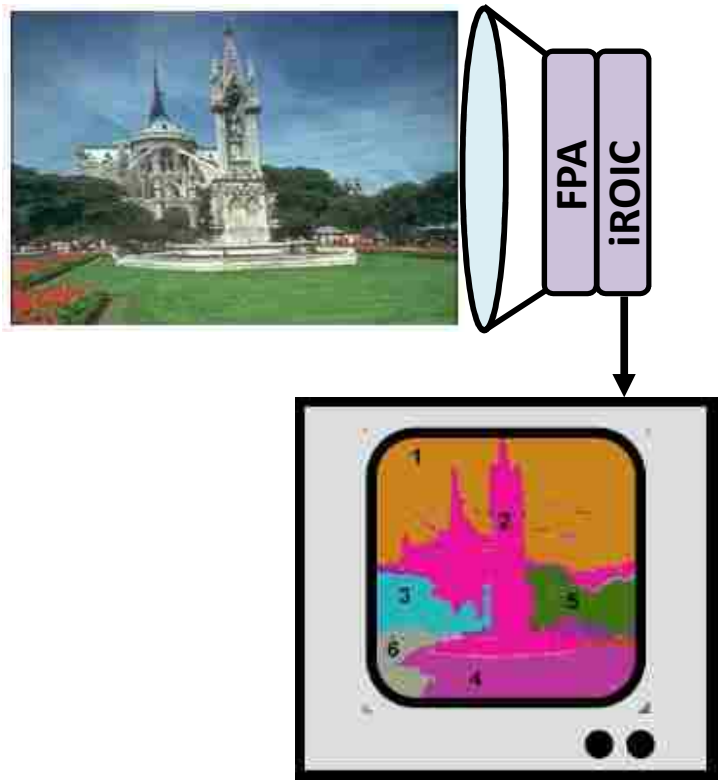

Figure 1.3: Proposed architecture for implementing the algorithm shown in Figure 1.1. iROIC represents the analog signal processing ROIC.

1.4 Outline of Thesis

This thesis will first go over each sub-component of the overall system. Each chapter will sequentially cover the flow from the input of a signal to the final processed output signal. After each sub-component is covered, the entire system will be presented. The following chapters will start with the design of a basic two stage operational amplifier, including design based on simulations in the transient and frequency domains. It will then discuss a system to provide the capability to optionally invert an analog signal. A system that will take the optionally inverted signal and convert it into a signal current is then covered. Next, a section discussing channel length modulation will be provided. The discussion of channel length modulation will carry into a section that discusses a

system that multiplies current. Finally a circuit that is used to convert the signal current back into a signal voltage is discussed.

Chapter 2

Operational Amplifier Design

2.1 Introduction

This chapter covers the general design of an NMOS differential pair two stage operational amplifier (opamp). The design techniques used in this section are intended to be practiced on opamp's that are used in a negative feedback, power regulation style architecture. This means that things such as gain bandwidth and open loop operating characteristics are not the most critical design elements. This section will concentrate primarily on DC operating point, offset, stability compensation, and transient current drive capabilities. These items will be covered in the context of the SPICE circuit simulator.

Figure 2.1 shows the diagram of a simple two stage, NMOS differential pair operational amplifier. There are six main components within the structure: The current bias circuit, consisting of M9 and M8; the differential amplifier current sink NMOS, M1; the differential pair devices, M2 and M3; the active load devices, M4 and M5; the output stage devices, M6 and M7; and finally the stability compensation devices, R_{Null} and C_{Comp} .

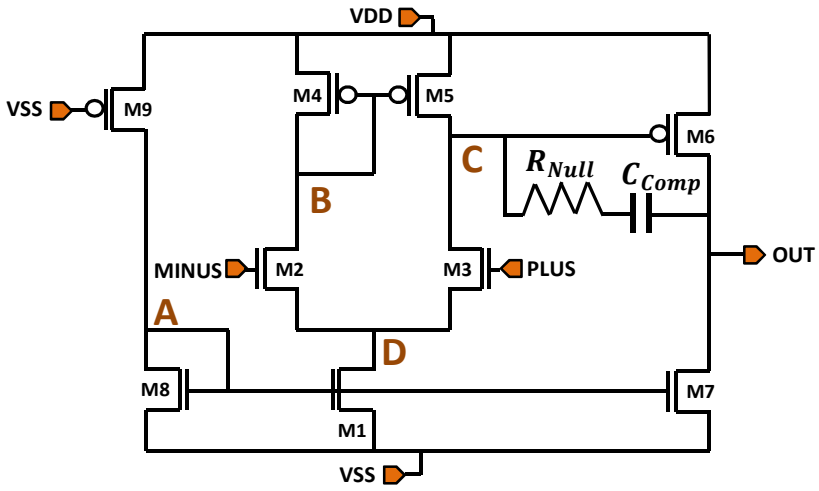

Figure 2.1: Circuit diagram of an NMOS differential pair two stage operational amplifier

2.2 Description of Opamp Devices

This subsection will cover each of the component groups listed above except for the stability compensation devices, which will be covered in section 2.3.

The current bias circuit is generally a decent starting place as it doesn't have any circuits to depend on. In the configuration shown there is a simple PMOS (M9) device acting as a resistor with its source tied to VDD, its gate tied to VSS, and its drain to the drain of the NMOS (M8) device. The NMOS device has its gate and drain tied to the drain of the PMOS device and its source to VSS. The current going through the bias is determined by the width to length (W/L) ratios of M9 and M8. M9 has a very low (much less than one) W/L ratio and M8 is sized after the size of M9 is established to provide the desired amount of current. The current going through M8 and M9 is determined and set to the desired current to be pulled by M5.

A PMOS device is used in order to provide the ability to easily turn off the opamp if needed. With the addition of an inverter and pull-up/pull-down devices on the output

stage gates the opamp can easily be turned off and the output node pulled to a high Z state. A resistor or other current bias technique could easily be used in place of M9, but this solution is simple and reliable. The current value will depend on numerous factors; a good starting point is to make sure that M8 and M9 are saturated with good margin.

The differential amplifier current sink (M1) determines a few major DC operation characteristics of the opamp. For our purposes the main concern for this circuit is that is sinks enough current to keep all of the differential amplifier's transistors in saturation under all operating conditions. This need to keep all transistors in saturation also translates into this device determining the minimum input common mode range (ICMR). The ICMR is important when the opamp will be used as a buffer as shown in Figure 2.2, as it will be one of the things that determine how low of a signal the opamp can buffer. The current through M1 is also related to the slew rate of the amplifier, which determines its response speed, and the gain of the differential amplifier [1].

The active load devices (M4 and M5), are used as an active load for the differential pair legs. Being that they are directly in line with the matched pair, the two devices must be matched and carefully laid out (circuit layouts are covered in Chapter 8). Their sizing will directly affect the maximum ICMR. If they are not sized properly, the differential pair may not be able to pull its output low enough to fully turn on the output stage. The active load device lengths additionally play a strong role in the DC gain of the opamp. These two devices also play a role in the transient offset. If in a buffer setup the output of an opamp is consistently under its target, the lengths of M4 and M5 can be extended to bring the transient solution higher. Figure 2.3 shows the analog buffer simulation results from modifying the lengths of M4 and M5 from 1.52u (orange trace) to

4.00u (green trace). The input is the yellow trace. As shown the analog buffer went from ~8mV of offset to <1mV of offset.

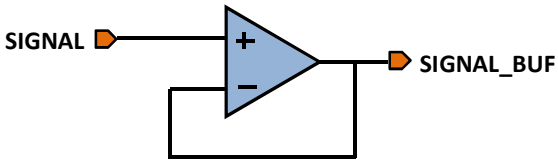

Figure 2.2: Analog operational amplifier buffer

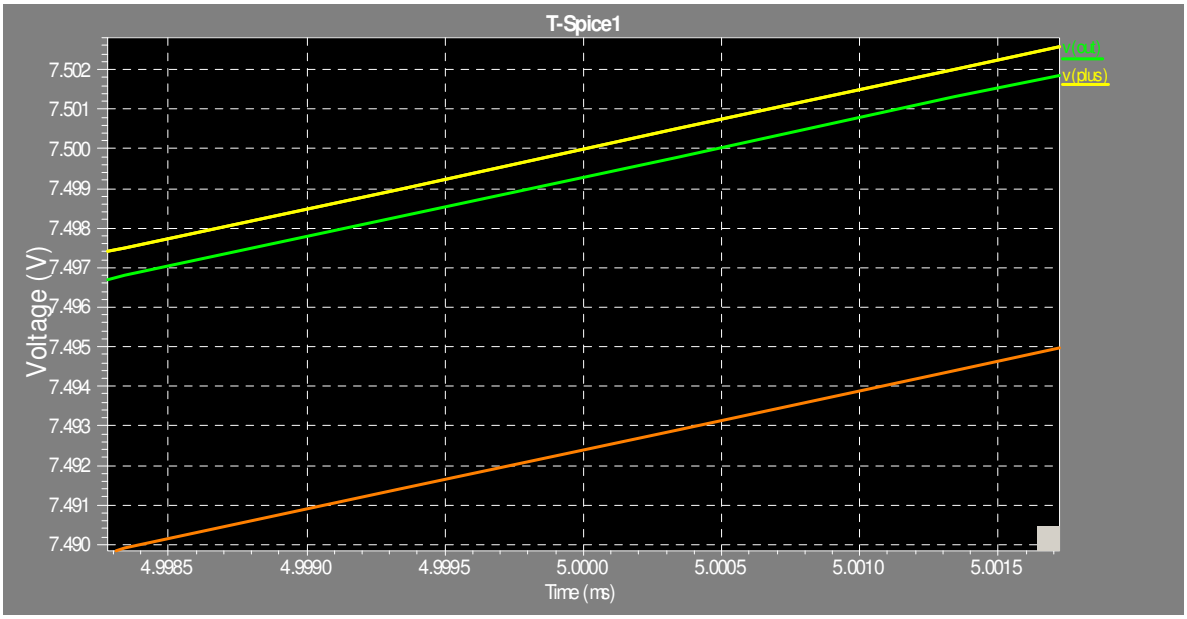

Figure 2.3: Circuit diagram of an NMOS differential pair two stage operational amplifier

The differential pair (M2, M3) is the main decision making feature of the two stage opamp. Its function is to place two matching amplifiers in competition with each other over a set amount of current. Since this pair of amplifiers shares only a single current then if one of the amplifiers receives a slightly higher VGS voltage it will receive

a larger portion of the available current and its output, the drain net of M2 or M3, will reduce. The sizing of M2 and M3 will alter the DC gain of the opamp [1].

The output stage (M6, M7), serves as an inverting amplifier that adds significant gain and drive capabilities to the opamp. The inverting PMOS, M6, influences the maximum voltage output and the gain characteristics of the opamp. The current load, M7, influences the minimum voltage output and how much current can be provided at that minimum voltage. M7's length parameter has a relatively large effect on the opamp gain [1]. The relative strength between M6 and M7 can also influence the DC offset of the opamp.

Most SPICE simulators provide the ability to use a .OP statement [2]. This will provide DC bias information for each device within your simulation. The .OP is extremely useful when checking the levels of margin for maintaining saturation. Table 2.1 displays an excerpt of a typical .OP output.

	M1	M8	M2	M3
MODEL	nch_hva.6	nch_hva.6	nch_hvs.5	nch_hvs.5
TYPE	nmos	nmos	nmos	nmos
REGION	Saturation	Saturation	Saturation	Saturation
vbs	-56.86344u	-53.38241u	-1.9242	-1.9242
vds	1.92407	1.31196	11.53822	11.55304
vdsat	265.04648m	264.59874m	227.56478m	227.44992m
vgs	1.31201	1.31202	2.07598	2.0758
vth	986.41543m	987.11472m	1.8655	1.86546
ib	-1.92419p	-1.31207p	-32.61612n	-33.39205n
id	18.29783u	17.17769u	9.18656u	9.17727u
ids	18.29783u	17.17768u	9.15394u	9.14387u

Table 2.1 Typical .OP output

In conclusion of this subsection, an overall large signal example of the opamp in operation when configured as an analog buffer is provided. This example will start by

assuming that the buffer is in a steady state, meaning that the two inputs to M2 and M3 are in equilibrium. Now let us say that something loads the output node and pulls it below the gate voltage on M3. Since the output net is connected to the gate of M2 its gate voltage will drop. This causes M2 to take less share of the total available current and also cause net "B" to increase in voltage. M3 will take on the extra available current which will cause the voltage on net "C" to drop. The gate voltage on M4 and M5 will increase which will further ease the voltage reduction of net "C". As the voltage on net "C" reduces, the gate voltage on M6 drops, which causes an increase in the VSD on M6. This action will cause the "OUT" terminal to rise. The mirror of this behavior will take place if the "OUT" terminal gets pulled higher than the gate voltage on M3. If the system is well compensated, this process will not oscillate.

2.3 Opamp Compensation

This subsection will cover the stability compensation of a two stage opamp. The analog buffer will be the main focus of this section. The circuit shown in Figure 2.4 shows the test setup used for this circuit. A large inductor is placed in the feedback loop to disconnect the system from small signal feedback while still allowing the simulator to find a solution to the DC operating point. A large capacitor is placed at net "A" to separate the small signal AC voltage from the DC operating point solution. This setup puts the system into an open loop configuration, injects a small signal voltage input at net "A", and allows the measurement of operations between net "A" and net "B". The "LOAD" block within Figure 2.4 represents the circuitry that this circuit will be driving.

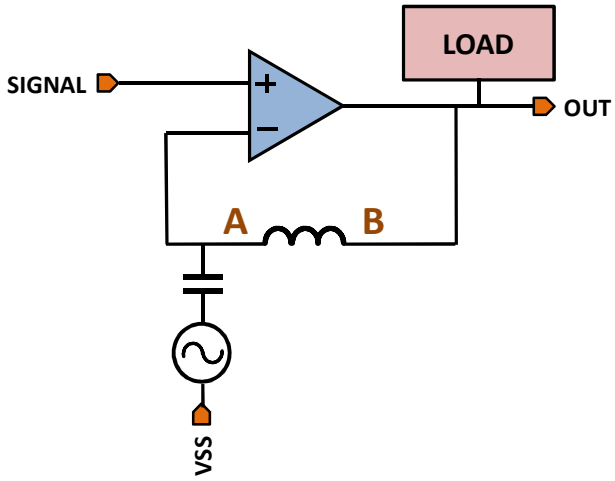

Figure 2.4: Stability analysis setup for the analog buffer

Now that the test setup for frequency analysis has been identified, we will take a closer look at what is going on within the opamp. The effects of R_{Null} and C_{Comp}, shown within Figure 2.1, on the frequency response of the system will be covered in theory and in simulation. From this point forward R_{Null} and C_{Comp} will be referred to as the nulling resistor and the compensation capacitor.

Phase margin is a term that will be used numerous times throughout this manuscript. In a negative feedback amplifier system the term "negative" is not exactly a solid concept. The circuit in Figure 2.4 is setup to inject a sinusoidal signal on net "A". Since this sinusoidal source feeds the negative opamp input, the inverse of the sinusoidal is expected at the output net "B". In a sinusoidal signal the inverse to a given signal is simply that signal phase shifted by 180 degrees. If our system is not stable there will be some frequency where instead of our feedback being 180 degrees out of phase, it will be in fact in phase with the input sinusoidal. If this occurs, the system will oscillate. Phase margin is defined as how close the phase of the source signal and the phase of the

feedback signal get while the amplifier is making positive, non-zero gain. Figure 2.5 shows how the "A" (Input) and "B" signals would look under different phase margin results. Note that there is no gain between the source signal and the feedback signal. This indicates the amplifier has reached its unity gain frequency or the frequency which the amplifier has a gain of 0dB. The phase margin at frequencies higher than the unity gain frequency do not affect the stability of the system, as the system is by definition attenuating at frequencies higher than the unity gain frequency.

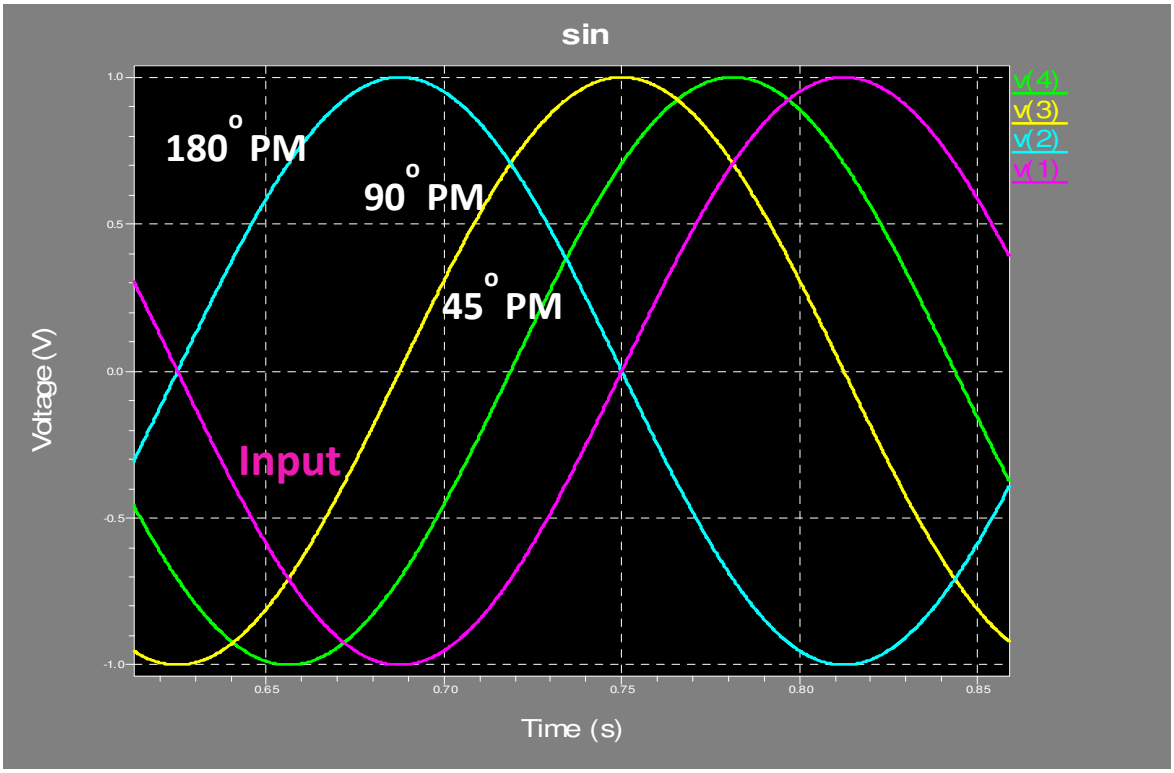

Figure 2.5: Phase shifts for different phase margins (PM)

The use of C_{Comp} , a compensation capacitor, is often referred to as Miller compensation [1]. The Miller effect describes the fact that the capacitance between the

input and output of a class A amplifier increases with the gain of the amplifier [3]. In a feedback amplifier setup, such as our analog buffer, this gain dependent, input to output capacitor is helpful. It introduces a dominant pole into the feedback loop. Adding a pole to the feedback loop alters the system's frequency response characteristics in a couple of ways. The first is that it causes a -20dB per decade reduction in gain starting at the location of the pole. This causes the opamp to become a low pass filter and attenuate high frequencies. The second effect of adding a pole is that the phase response of the feedback signal will drop 45^{o} (from 180^{o}) from the decade prior to the pole to the decade after the pole [4]. If the Miller capacitance is large enough and the system goes into attenuation before the negative feedback gets pushed to the point of having poor phase margin, then the system can be stabilized with just the Miller capacitance

Unfortunately the Miller capacitance is generally not large enough to fully compensate the opamp for real world loading situations. Additionally in a normal opamp there is usually more than one pole, which causes the phase to reduce to the point of having poor, or no, phase margin. Because of this a compensation capacitor is added to the circuit in addition to the Miller capacitance. This additional capacitance decreases the frequency of the dominant pole and increases the frequency of the secondary pole. These changes cause the unity gain frequency to reduce and the 45^{o} phase changes to take place at much more ideal locations.

Figure 2.6 shows the frequency analysis simulation results from three different circuits. The top graph displays the gain vs. frequency plot and the bottom graph displays the phase vs. frequency plot. The pink traces are the results from an uncompensated opamp buffer, the yellow traces are the results from an opamp buffer

with only an added compensation capacitor, and the orange traces are the results from an opamp buffer with an added nulling resistor and an added compensation capacitor.

The uncompensated gain result (pink trace) shows two poles prior to the unity gain frequency. This causes the system to be unstable due location of the two poles and the double decrease in phase margin. The results with the added compensation capacitor (yellow trace) look much better. The dominant pole has been pulled to a lower frequency, which causes the unity gain frequency to reduce, and the secondary pole has been pushed to a frequency past the unity gain frequency. This means that not only the unity gain frequency reduced, but also that the phase margin shift due to the second pole doesn't occur until after the system is in attenuation. This double positive brings our system well within an acceptable phase margin.

Some issues can arise in certain loading situations due to the addition of a large compensation capacitor. The capacitor also introduces a right hand plane zero into the frequency response [1]. This zero causes an increase in high frequency gain. It can be especially detrimental if its location and accompanying increase in gain falls somewhere near the unity gain frequency. The frequency characteristics of the zero are the opposite of the pole. The zero will cause a 20dB per decade increase in gain and a positive 45^{o} phase margin shift.

The term "zero" is an abstraction of the fact that the compensation capacitor practically becomes a short at high frequencies. This causes the differential amplifier to overdrive the output stage and push a little extra gain at high frequencies. A simple solution to this issue is to place a resistor, a nulling resistor as it's called, in series before the compensation capacitor as shown in Figure 2.1. This added resistor will limit the

overdrive capabilities of the differential amplifier which pushes the right hand plane zero into the stable left hand plane. Since the zero causes the inverse of the behavior of a pole, a common practice is to size the resistor in order to place the zero on top of the secondary pole. This causes no increase in gain and gives the added benefit of stopping the reduction of phase margin.

It is often the case that the zero resulting from the compensation capacitor is already at a frequency that is higher than the unity gain frequency. The nulling resistor can still be of great benefit even in these situations. The orange traces within Figure 2.6 show the results from adding a series nulling resistor. Note that the gain response prior to the unity gain frequency has little change, but the phase margin of the system is pushed out and increased.

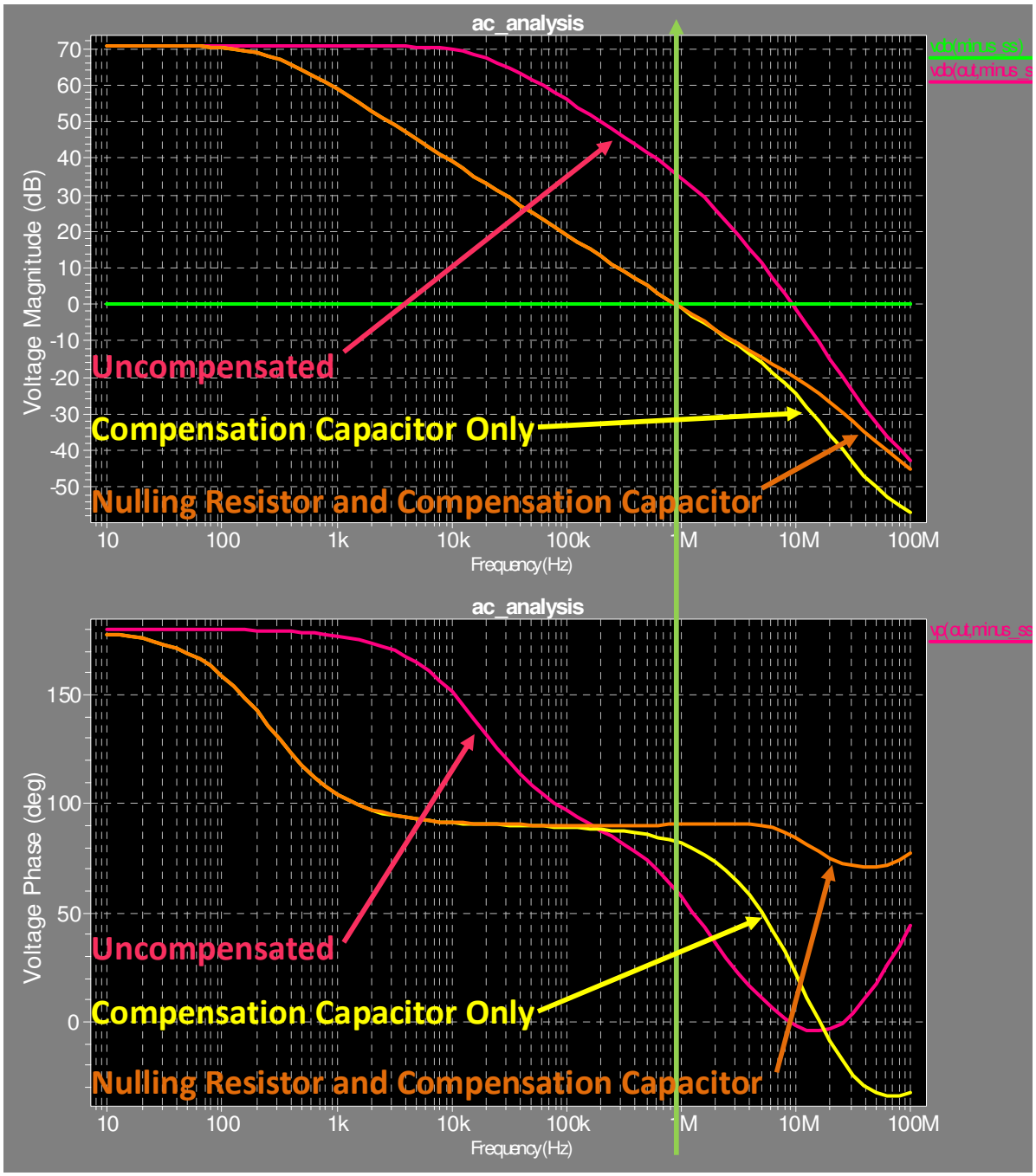

Figure 2.6: Frequency analysis results from an analog buffer with no compensation (pink), compensation capacitor only (yellow), and nulling resistor and compensation capacitor (orange)

2.4 Tailoring Opamps for Certain Loads

The top level circuit discussed within this thesis uses four different variations of the two stage NMOS differential pair opamp. The system has very different load and drive characteristics which require different circuit characteristics. The differential amplifier is kept the same on each opamp. The output stage and stability compensation components are different for each design.

Table 2.2 shows the sizing for an opamp used for the inverter and buffer discussed in Chapter 3. As discussed within Chapter 3, these opamps need to drive a moderate current load and a small capacitive load. This means the output stage is made reasonably large and the compensation components smaller.

Table 2.3 shows the sizing of the opamp used in the current bias generation circuits covered in Chapter 4. This system has relatively large gain when compared to the other circuitry. This means the system needs a larger compensation capacitor to keep the system stable. The opamp also drives very little current to its load, so there is no need for a large output stage.

Table 2.4 shows the sizing of the opamp used for VDS correction circuitry, which is covered in Chapter 5. This system does not have the high gain of the current bias generation setup or the high current demands of the buffer setup. This opamp is sized with a smaller output stage and a smaller compensation capacitor and nulling resistor.

Table 2.5 shows the sizing of the opamp that provides the solution for the current to voltage conversion circuitry covered in Chapter 6. This system needs an opamp that can provide a large amount of current and drive a relatively smaller capacitive load.

	Width (um)	Length (um)	Multiple (um)
m1	3.22	2.5	3
m2	3.22	4.5	8
m3	3.22	4.5	8
m4	3.22	3	6
m5	3.22	3	6
m6	3.22	1.52	75
m7	3.22	1.52	25
m8	3.22	2.5	3
m9	3.22	140	1
Rnull	4	14	1
Ccomp	120	30	1

Table 2.2: Opamp device sizing for the buffer/inverter circuitry

	Width (um)	Length (um)	Multiple (um)
m1	3.22	2.5	3
m2	3.22	4.5	8
m3	3.22	4.5	8
m4	3.22	3	6
m5	3.22	3	6
m6	3.22	1.52	12
m7	3.22	1.52	4
m8	3.22	2.5	3
m9	3.22	140	1
Rnull	4	62	1
Ccomp	120	90	1

Table 2.3: Opamp device sizing for the current bias generation circuitry

	Width (um)	Length (um)	Multiple (um)
m1	3.22	2.5	3
m2	3.22	4.5	8
m3	3.22	4.5	8
m4	3.22	3	6
m5	3.22	3	6
m6	3.22	1.52	12
m7	3.22	1.52	4
m8	3.22	2.5	3
m9	3.22	140	1
Rnull	4	14	1
Ccomp	120	30	1

Table 2.4: Opamp device sizing for the VDS control circuitry

	Width (um)	Length (um)	Multiple (um)
m1	3.22	2.5	3
m2	3.22	4.5	8
m3	3.22	4.5	8
m4	3.22	3	6
m5	3.22	3	6
m6	3.22	1.52	150
m7	3.22	1.52	50
m8	3.22	2.5	3
m9	3.22	140	1
Rnull	4	14	1
Ccomp	120	30	1

Table 2.5: Opamp device sizing for the current to voltage conversion circuitry

Chapter 3

Optionally Selectable Analog Inverter

3.1 Introduction

This chapter covers the operation and design of the selectable regulated analog signal inversion circuitry. This circuitry is provided in the overall design to provide the ability to account for signage when performing a multiply and accumulate. This circuit will also be referred to as the input section of the top level design. Section 3.2 covers the transient operation design concerns and section 3.3 covers the frequency domain design concerns for the inverter setup. The frequency domain design concerns for the analog buffer are covered within Chapter 1.

3.2 Transient design Concerns

Figure 3.1 shows the classic opamp analog inverter. This structure incorporates two resistors with an identical resistance and an opamp setup as shown below. The leftmost resistor in Figure 3.1 essentially serves as voltage to current conversion. Ideally the opamp will pull net "A" to the level of the "MID_BIAS" input under any value of the "SIGNAL" input. This means that a voltage input of "SIGNAL" will create a current flow $I_{Inv} = (SIGNAL - MID_{BIAS})/R$. As covered in Chapter 1, the inputs to the opamp route directly to the gates of MOSFET devices and draw a negligible amount of current. This means that the current developed in the leftmost resistor also flows in the rightmost resistor. Since the opamp is working to keep net "A" at the same value as the "MID_BIAS" input, it will reduce its output voltage until its inputs are aligned. The

current through the rightmost resistor is then $I_{Inv} = (MID_{BIAS} - SIGNAL_{INV})/R$. If we equate the current through each resistor the solution $SIGNAL\_INV = -SIGNAL$ is developed.

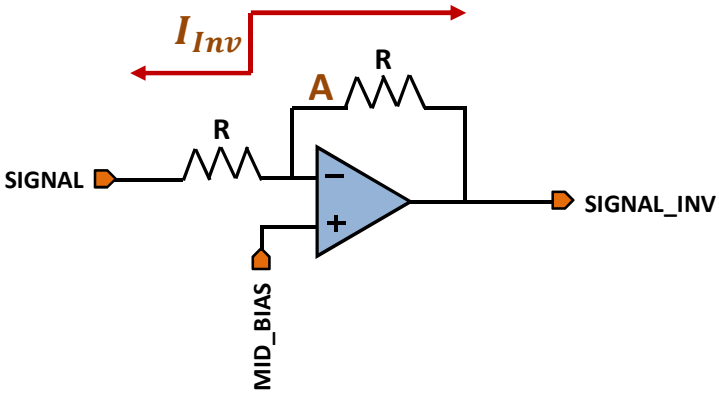

Figure 3.1: Analog operational amplifier inverter

Figure 3.2 shows the full buffered, optionally inverted input stage. Since the inversion stage needs to actively draw current, a buffer is added. A full transmission gate mux is provided to allow the selection of either the buffered signal or its inverted version. The "MID_BIAS" input serves as the value that defines the point of "zero" in the system. This "zero" point can be described by anything being under its value will be considered negative and anything above its value will be considered positive.

Outside of the internal biases of the opamp, the main transient design concerns for this circuit lie in the current driving capabilities of the opamp and the sizing of the two resistors. For example let's say the maximum value for the input "SIGNAL" is 14V and the "MID_BIAS" input is set to 7.5V. This means there's a 6.5V drop across the rightmost resistor. The resistor is then sized with the maximum voltage value in context.

Figure 3.3 shows the transient operation of the opamp when setup as a buffer driving a +/-200uA load. The opamp handles this load well and it will be used as the

maximum load criteria. The minimum current specification relates to how low can the current signal be before its signal to noise ratio falls to the point of being unacceptable. If the resistors are sized to 50kOhm the opamps have to supply a maximum of +/-130uA. This value meets both upper and lower current limits and keeps the overall resistor size down.

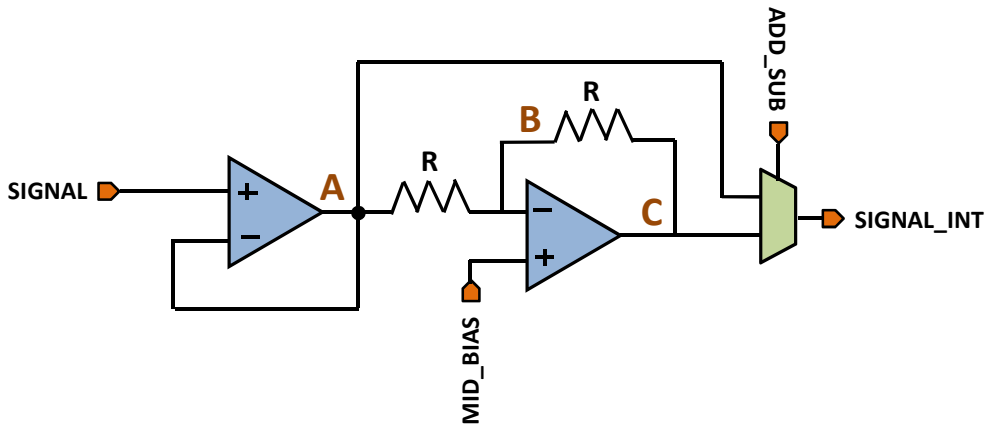

Figure 3.2: Analog optional inverter with buffer stage

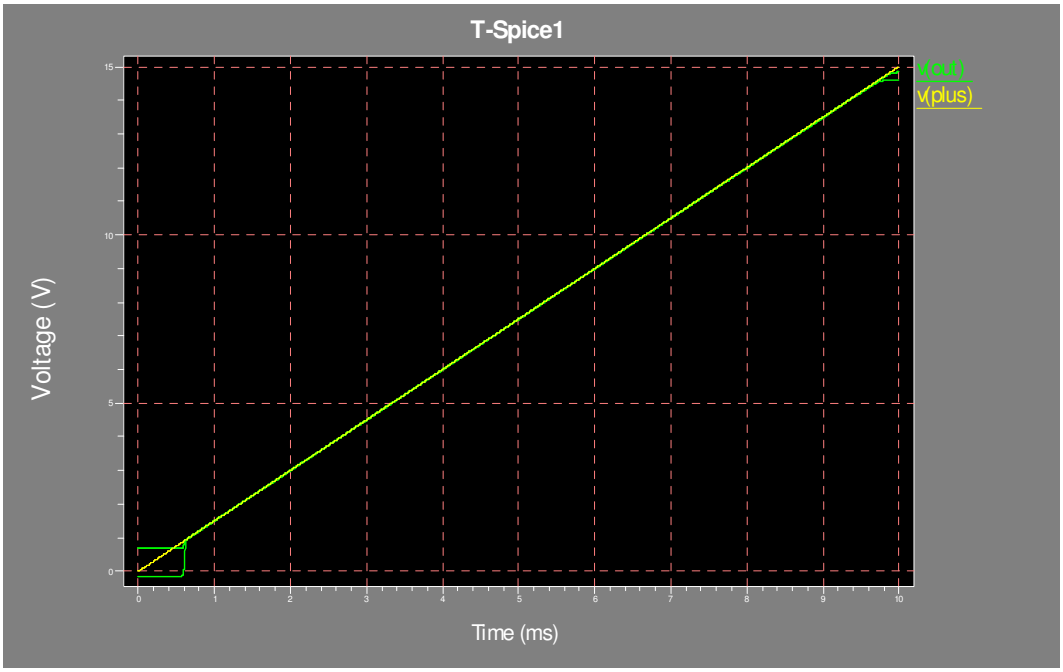

Figure 3.3: Transient current driving capabilities of the signal inversion operational amplifier under a +/- 200uA load

3.3 Frequency Design Concerns

This sub-section covers the frequency domain design theory and results of the input stage. As noted earlier the frequency domain design of the opamp buffer is covered in depth within Chapter 1. The circuit shown in Figure 3.4 shows the test setup used for this circuit. A large inductor is placed in the feedback loop to disconnect the system from small signal feedback while still allowing the simulator to find a solution to the DC operating point. A large capacitor is placed at net "A" to separate the small signal AC voltage from the DC operating point solution. This setup puts the system into an open loop configuration, injects a small signal voltage input at net "A", and allows the measurement of operations between net "A" and net "B". The "LOAD" block within Figure 3.4 represents the circuitry that this circuit will be driving.

The simulation results of this circuit are shown in Table 3.1. Wave form results are shown in Figure 3.5.

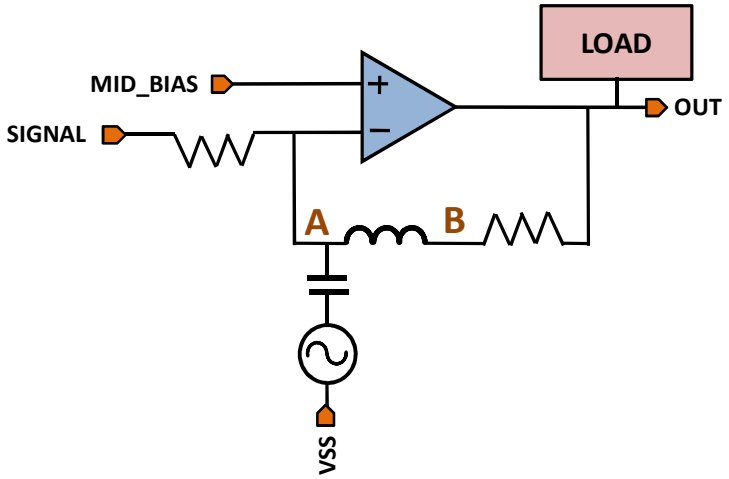

Figure 3.4: Stability analysis setup for the analog inverter

corner	temp	my_initial_gain_db	my_three_db_freq	my_unit_freq	my_phase_margin
TT	-55	5.34E+01	1.61E+04	7.57E+06	8.52E+01
TT	0	5.29E+01	1.27E+04	5.64E+06	8.40E+01
TT	55	5.26E+01	1.02E+04	4.39E+06	8.33E+01
FF	-55	5.25E+01	2.12E+04	9.04E+06	8.66E+01
FF	0	5.18E+01	1.71E+04	6.73E+06	8.52E+01
FF	55	5.14E+01	1.40E+04	5.26E+06	8.43E+01
SS	-55	5.42E+01	1.20E+04	6.21E+06	8.40E+01
SS	0	5.38E+01	9.30E+03	4.62E+06	8.31E+01
SS	55	5.37E+01	7.35E+03	3.59E+06	8.27E+01

Table 3.1: Stability analysis results for the analog inverter

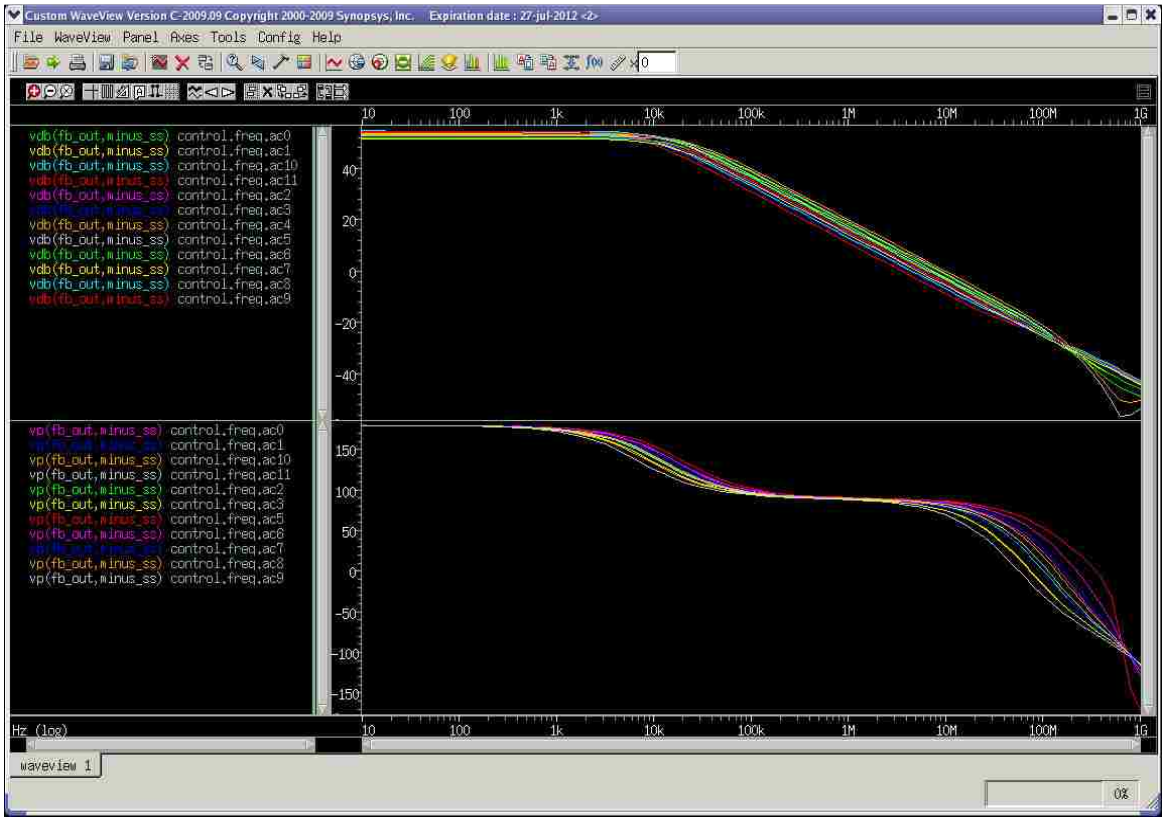

Figure 3.5: Stability analysis wave forms for the analog

Chapter 4

Signal Current Bias Generation

4.1 Introduction

Within this Chapter a circuit that converts signal voltage to signal current bias is covered. This is the second stage of our overall circuit; the first stage was covered in Chapter 3. This circuit is necessary because signal currents lend themselves to being amplified through current mirror techniques, which is how our signal multiplication is carried out. The details of the signal multiplication are covered within Chapter 5

This subsection also contains information about transient design considerations and frequency domain design considerations for the signal voltage to signal current converter.

4.2 Description of Architecture

The regulated current bias incorporates five main components. The first is some kind of differential sensing amplifier; the second is either a PMOS device or NMOS device; the third is a resistor(s); the forth is a high voltage supply; finally the fifth is a low voltage supply.

The differential sensing amplifier could be either a full two stage operation amplifier (opamp), or a simple single stage differential amplifier (diffamp), or some other differential sensing amplifier. The current bias circuit has been simulated with both a diffamp and an opamp and can be made to operate with either architecture. There are tradeoffs between the two designs. The opamp can create much more gain and a more

precise overall solution, but at the expense of system stability and lower phase margin. The system can be compensated with enough given area for compensation capacitance and nulling resistance. The diffamp removes a gain stage out of the feedback loop and gives a much lower direct current (DC) gain. This causes the system to be more stable, but also makes the current bias less accurate. This thesis covers the use of an opamp for this stage of the circuit.

The NMOS or PMOS device serves as the element that provides the current to the resistor. These devices are used to force the opamp to develop a gate to source voltage (VGS/VSG) to provide the correct amount of current.

The resistors are used to provide a reliable and measureable voltage drop.

4.3 PMOS Current Bias Generation

Figure 4.1 shows the diagram of the current bias that uses a PMOS driver. As shown, the system is configured to have negative feedback. This causes the opamp to seek a solution that will cause both of its inputs to be the same value. If we assume that the *SIGNAL_P* is equal to the input *SIGNAL* and the resistor has resistance *R* then we cause the system to develop current $ID = (SIGNALP - MID\_BIAS)/R$. The system will push current through resistor R until the *SIGNAL* input equals the *MID*_BIAS supply. If the *SIGNAL* input drops below the *MID_BIAS* supply, the system will put the PMOS device into cut-off. Conveniently the *ID* that the system develops runs directly through the PMOS device. If a linear signal is sent to the opamp, the VSG being produced by the opamp is a non-linear signal that produces a linear current. This powerful relationship allows the

ability to generate a current bias that produces a linear current from a linear voltage input and then mirror that bias and its accompanying current to other devices.

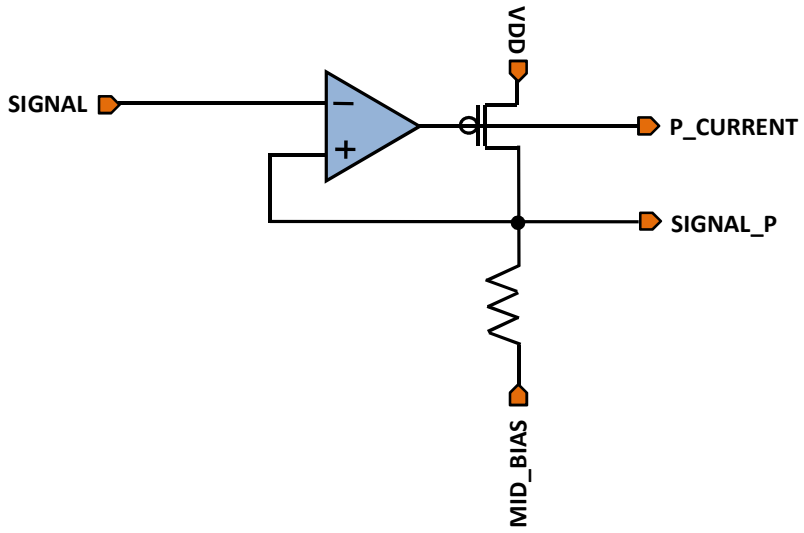

Figure 4.1: PMOS signal voltage to signal current converter

4.4 NMOS Current Bias Generation

Figure 4.2 shows the diagram of the current bias that uses an NMOS driver. The operation of this circuit is alike the circuit in Figure 4.1 with a few exceptions. The basic setup uses an opamp, an NMOS, and a resistor. As with the circuit in Figure 4.1, the system is setup with negative feedback to the opamp. Again this means that the opamp will make adjustments and try to make its two inputs equal. The main difference is that now the transistor will develop the current $ID = (MID\_BIAS - SIGNAL\_N)/R$. In this configuration, instead of pushing current through the resistor, as was the case with the circuit in Figure 4.1, the circuit now pulls current through the resistor.

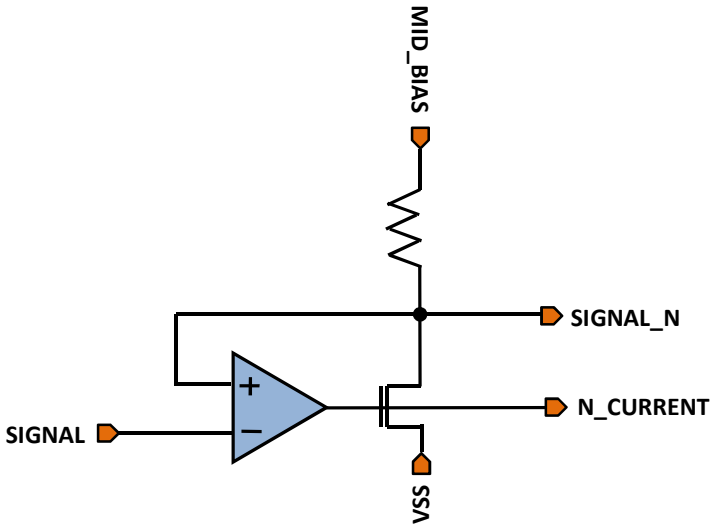

Figure 4.2: NMOS signal voltage to signal current converter

4.5 Full Swing Current Bias

Figure 4.3 shows the diagram of both the NMOS and PMOS based current bias circuits placed together as they will be shown later in this document. The two circuits form a full swing push-pull signal current bias generator. When the input SIGNAL is higher than the MID_BIAS supply the P_CURRENT signal will be active and the N_CURRENT signal will be pulled low. When the input SIGNAL is lower than the MID_BIAS supply, the N_CURRENT signal will be active and the P_CURRENT signal will be pulled high.

Figure 4.4 shows the overall operation of the full circuit. Within Figure 4.4, signal ampoutP corresponds to P_CURRENT, ampoutN corresponds to N_CURRENT, the current through R0 corresponds to the resistor within the NMOS current bias, and the current through R1 corresponds to the resistor within the PMOS current bias. As shown, the full circuit produces a full swing linear current when a linear signal is input.

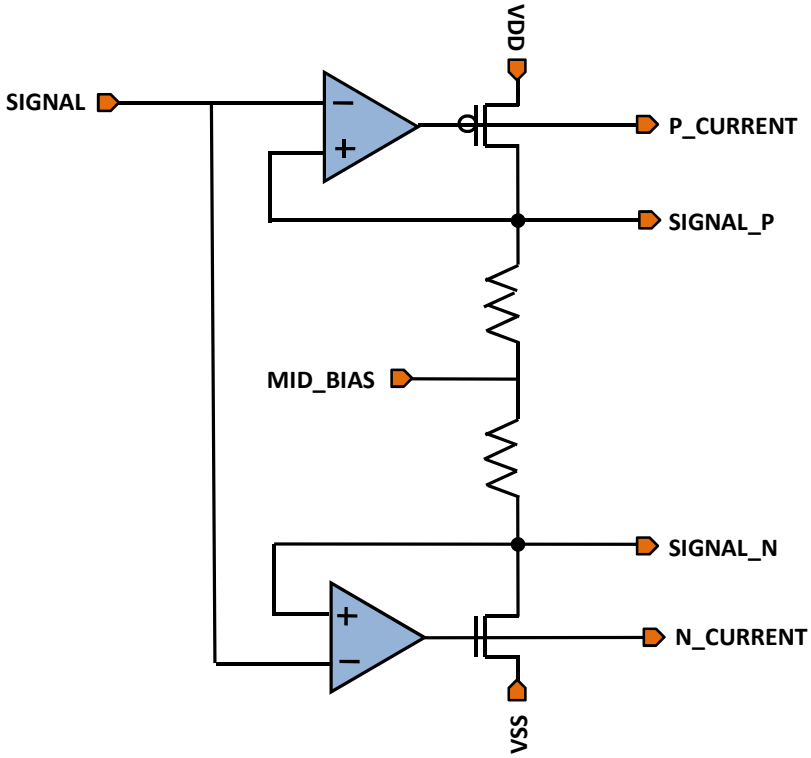

Figure 4.3: Full push/pull signal voltage to signal current converter

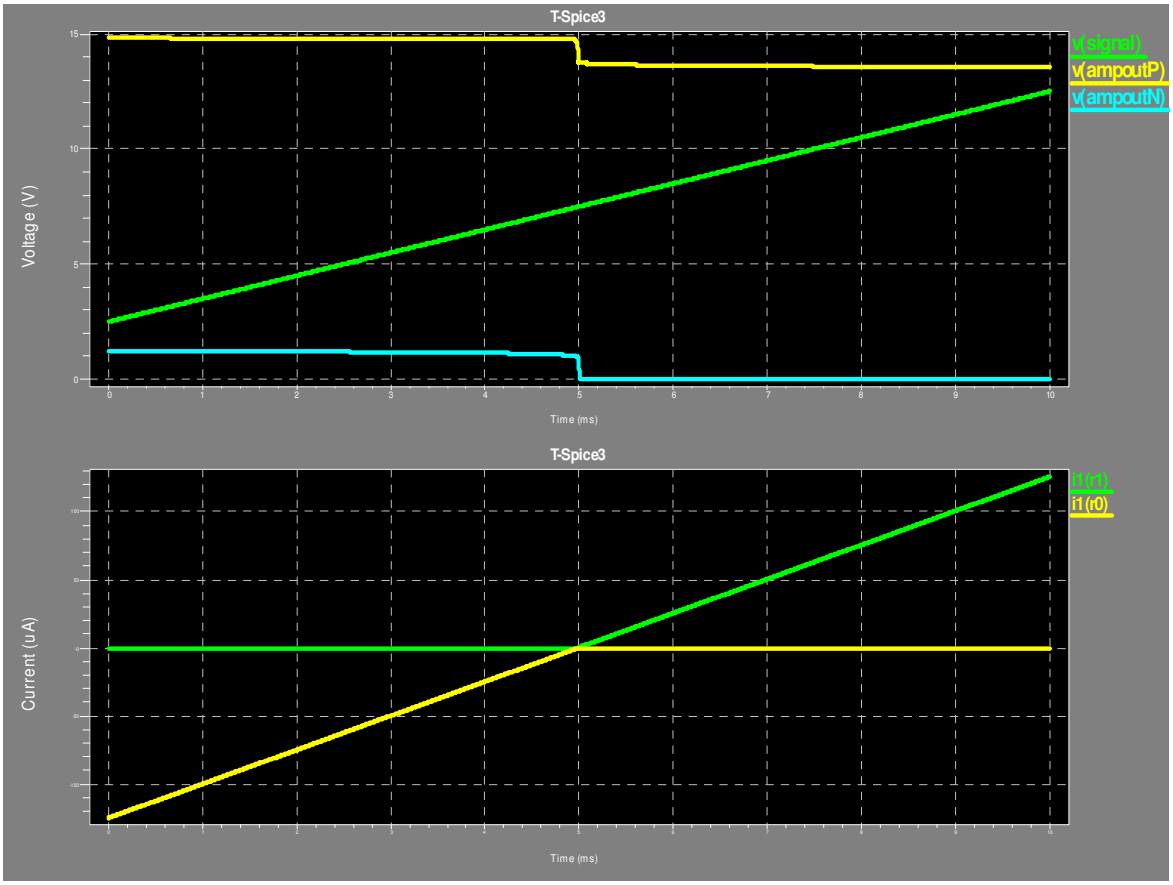

Figure 4.4: Wave forms of the full current bias circuit in a full signal

4.6 Frequency Analysis

This section covers the stability analysis performed on the current bias circuits. Table 4.1, Figure 4.5, and Figure 4.7 are provided to detail the frequency response of the PMOS current bias. Table 4.2, Figure 4.2, and Figure 4.8 are provided to detail the frequency response of the NMOS current bias. A more detailed explanation for stability analysis in integrated circuitry can be found in Chapter 1.

A large inductor is placed in the feedback loop to disconnect the system from small signal feedback while still allowing the simulator to find a solution to the DC operating point. A large capacitor is placed at net "A" to separate the small signal AC

voltage from the DC operating point solution. This setup puts the system into an open loop configuration, injects a small signal voltage input at net “A”, and allows the measurement of operations between net “A” and net “B”.

Compensation of the current bias is made a little more difficult due to the high gain that is produced by the circuit. If a two stage opamp is used then there are three gain stages in the design. These gain stages create nearly 80dB of DC gain. Since this system is intended for a power regulation style circuit and not a pure small signal purpose, the gain bandwidth is not the critical area of design to focus on. If the gain bandwidth is not a primary concern then we can compensate for stability with simple compensation capacitance and nulling resistors.

The compensation technique covered in Chapter 1 will be used for the opamp section of the circuit. We will introduce a strong dominant pole and a strong nulling resistor within the feedback loop. The dominant pole will help attenuate the frequency response and the nulling resistor will be mainly used to push out the phase response. The phase difference, gain, gain bandwidth, and unity gain frequency is measured between the signal generated at point A within Figure 4.5/Figure 4.6 and the signal at point B across a frequency sweep.

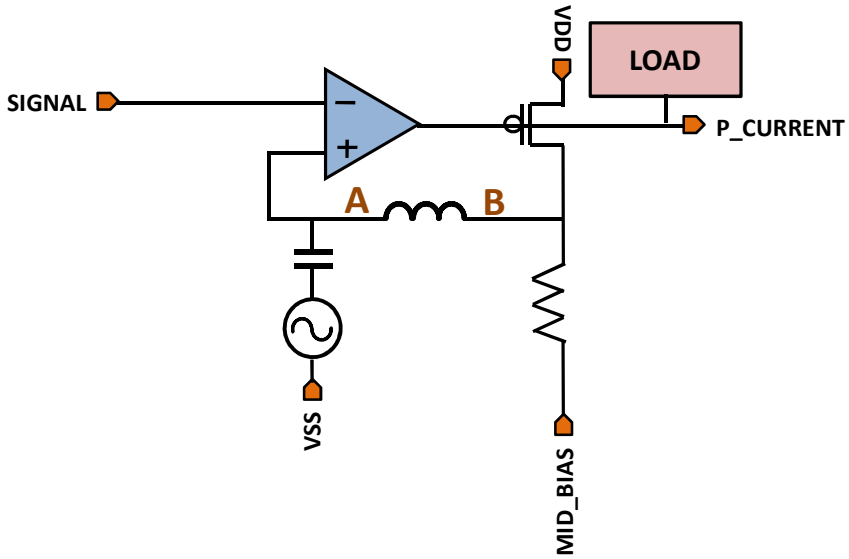

Figure 4.5: PMOS current bias stability analysis setup

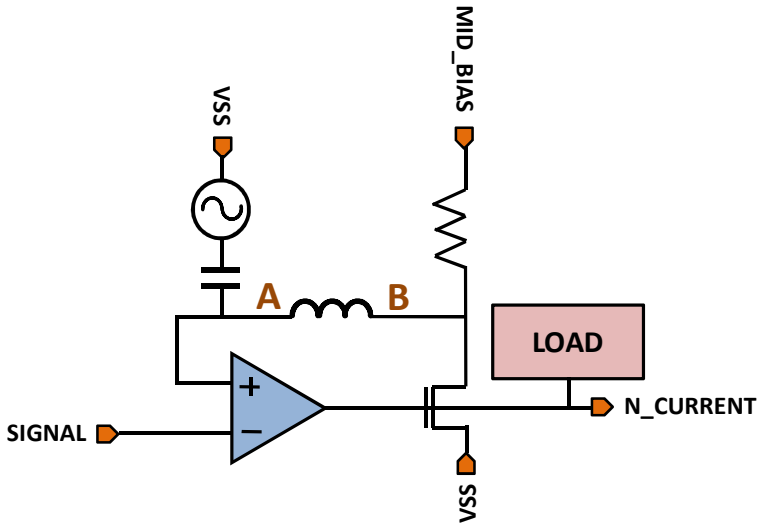

Figure 4.6: NMOS current bias stability analysis

corner	temp	my_initial_gain_db	my_three_db_freq	my_unit_freq	my_phase_margin
TT	-55	7.99E+01	8.68E+03	3.54E+07	4.90E+01
TT	0	7.89E+01	6.66E+03	2.08E+07	5.38E+01
TT	55	7.79E+01	5.36E+03	1.29E+07	5.04E+01
FF	-55	7.79E+01	1.31E+04	4.62E+07	4.48E+01
FF	0	7.56E+01	1.13E+04	2.71E+07	5.32E+01
FF	55	6.90E+01	1.38E+04	1.31E+07	5.29E+01
SS	-55	8.15E+01	5.77E+03	2.52E+07	5.28E+01
SS	0	8.05E+01	4.39E+03	1.45E+07	5.20E+01
SS	55	7.98E+01	3.42E+03	9.25E+06	4.22E+01

Table 4.1: PMOS current bias stability results

corner	temp	my_initial_gain_db	my_three_db_freq	my_unit_freq	my_phase_margin
TT	-55	8.56E+01	3.38E+03	3.81E+07	5.80E+01
TT	0	8.23E+01	3.27E+03	2.18E+07	6.26E+01
TT	55	7.93E+01	3.23E+03	1.32E+07	6.14E+01
FF	-55	8.21E+01	5.90E+03	5.16E+07	5.41E+01
FF	0	7.85E+01	5.94E+03	3.00E+07	6.17E+01
FF	55	7.51E+01	6.05E+03	1.84E+07	6.45E+01
SS	-55	8.85E+01	1.97E+03	2.67E+07	6.10E+01
SS	0	8.55E+01	1.84E+03	1.50E+07	6.11E+01
SS	55	8.29E+01	1.76E+03	9.30E+06	5.30E+01

Table 4.2: NMOS current bias stability results

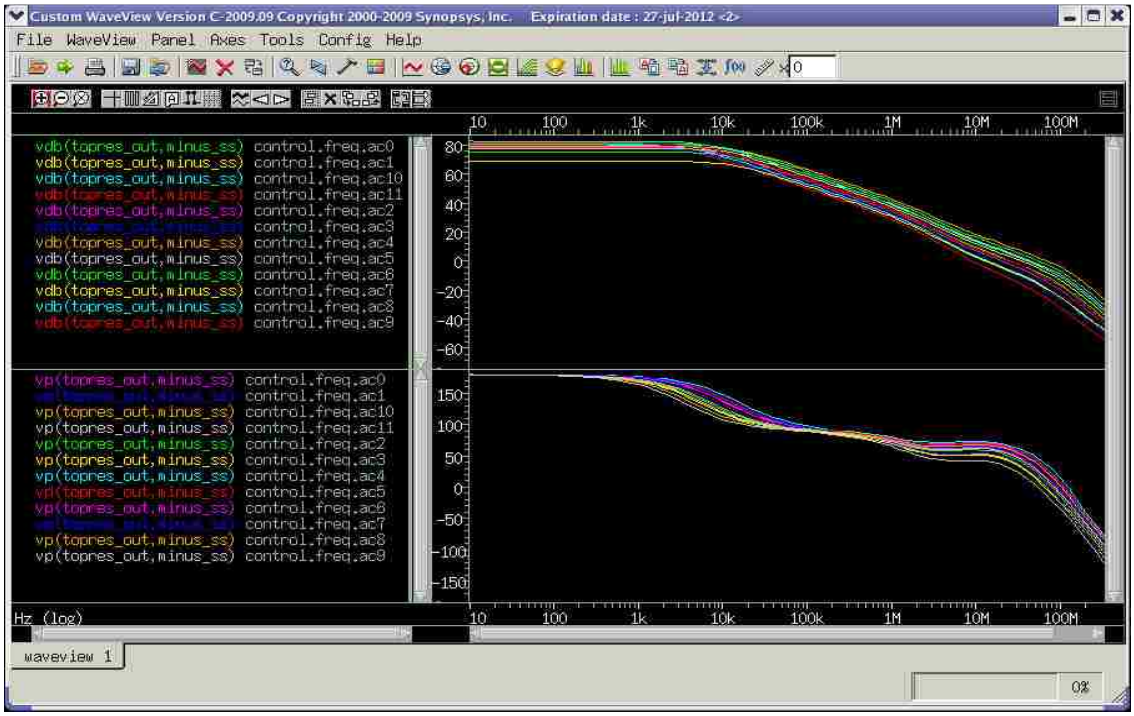

Figure 4.7: Wave forms of the PMOS current bias frequency analysis

Figure 4.8: Wave forms of the NMOS current bias frequency analysis

Chapter 5

Current Multiplication

5.1 Channel Length Modulation

In order to fully discuss the circuit covered in this section we must first go over a non-ideal effect that is purposefully accounted for within the current multiplication circuit structure.

Channel length modulation (CLM) is a short channel non-ideal effect that causes a relationship to arise between the drain to source voltage (VDS) and the saturation current (IDsat) of a transistor. In the ideal transistor model, once the VDS exceeds the gate to source (VGS) voltage minus the threshold voltage (VT) the transistor is assumed to be in saturation (VDSsat). In Equation 5.1.1 $IDsat$= the drain to source current, K'_n= the technology parameter (transconductance coefficient), W/L= transistor width to length ratio, V_{gs}= the gate to source voltage, and V_{th}= the threshold voltage. In the simple transistor model presented in the Equation 5.1.1, a change in VGS makes a change in IDsat independent of what the VDS value is. So for every value of VGS we get a flat IDsat result over all VDS > VDSsat values.

$$IDsat = K'_n \frac{W}{L} (V_{gs} - V_{th})^2 \quad (5.1.1)$$

In reality and with the transistors we have used for this circuit, there is a dependency between the IDsat and the VDS > VDSsat value. This effect is well explained by CLM which is best described through the pinch-off effect. The pinch-off effect is directly related to the depletion region width of the reversed biased P/N junction that exists between the drain implant and the bulk of the transistor. In an NMOS device,

as the drain voltage is increased with respect to the body voltage (VDB), the drain to bulk P/N junction becomes more reversed biased. This increase in reverse bias physically causes the P/N junction depletion region to grow. If enough VDB is present and the VGS voltage has put the transistor into deep inversion, the depletion region will collide with the inversion layer and cause it to reduce in physical length across the transistor gate length. As carriers hit the depletion region they are quickly transported across the drain to bulk P/N junction due to the electric field within the depletion region [3]. Figure 5.1 shows a diagram of an NMOS device experiencing CLM.

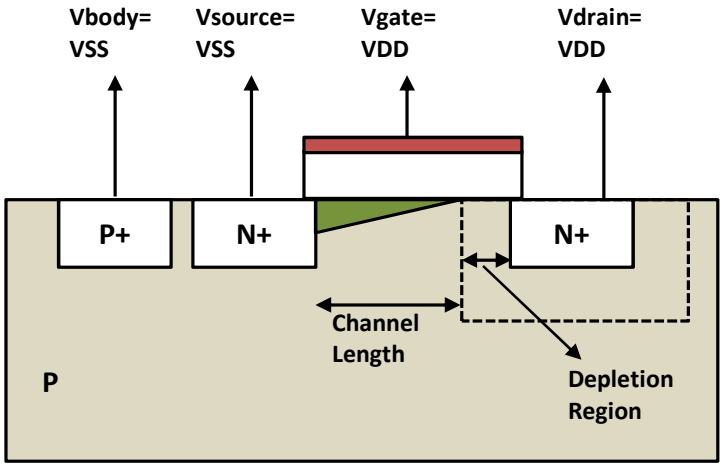

Figure 5.1: NMOS cross section diagram

As shown in Figure 5.1, as the depletion region grows, the effective channel length reduces. This means that as the VDB increases, the effective channel length reduces. A shorter channel length results in more drain to source current flow.

Equation 5.1.1 can be modified to include some basic parameters to perform a first order approximation of CLM. Equation 5.1.2 shows these additions. In Equation 5.1.2 λ= channel length modulation parameter and V_{ds}= drain to source voltage.

$$IDsat = K'_n \, {}^{W}/_{L} \, (V_{gs} - V_{th})^2 (1 + \lambda V_{ds}) \quad (5.1.2)$$

Since we are using a high voltage process that involves a double diffusion implant, our transistors are even more susceptible to CLM. A double diffusion implant involves an n- implant into a p- substrate and then an n+ implant within the n- implant. This technique is used in efforts to make the MOSFET immune to the hot carriers that can become present in high voltage applications [5]. In Figure 5.2, an NMOS device is shown which uses an n-type double diffusion (NDD) implant, with the first implant being n- and the second n+. This lower doped implant increases the depletion region width, which increases the transistor's susceptibility to CLM.

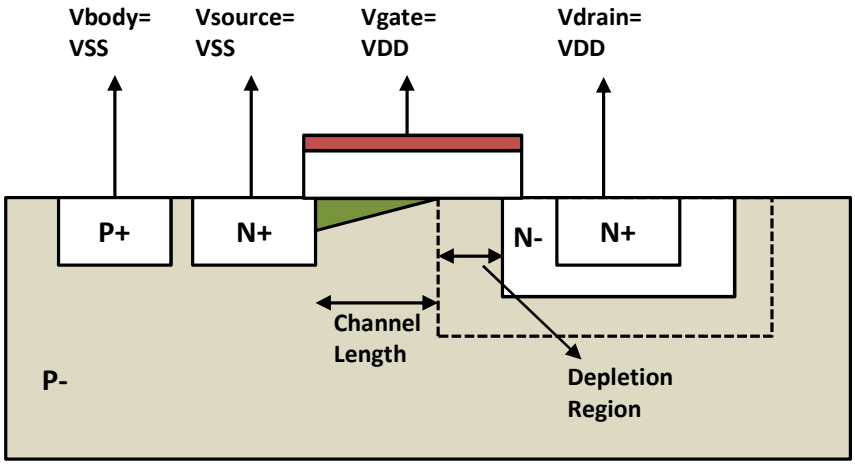

Figure 5.2: NMOS cross section diagram with double drain implant

Figure 5.3 shows the simulation results for an NMOS device that does not have the NDD implant. The wave forms show the drain current (ID) resulting from a sweep of VDS over different gate voltages. Figure 5.4 shows the simulation results for an NMOS device with the NDD implant. As shown the ID of the NMOS with the NDD implant has a

strong dependence on the VDS even while VDS > VDSsat. Also note that the slopes of the NMOS with the NDD implant are greater than the slopes of the NMOS without the NDD implant. This dependency causes the need for a targeted circuit solution.

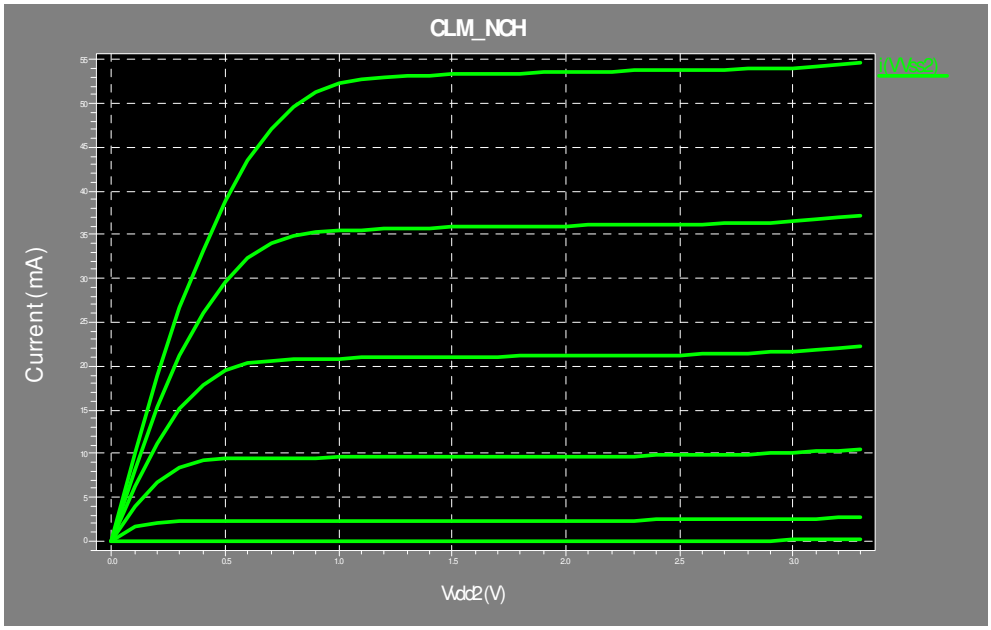

Figure 5.3: NMOS without NDD ID vs. VDS sweep, over different VGS voltages

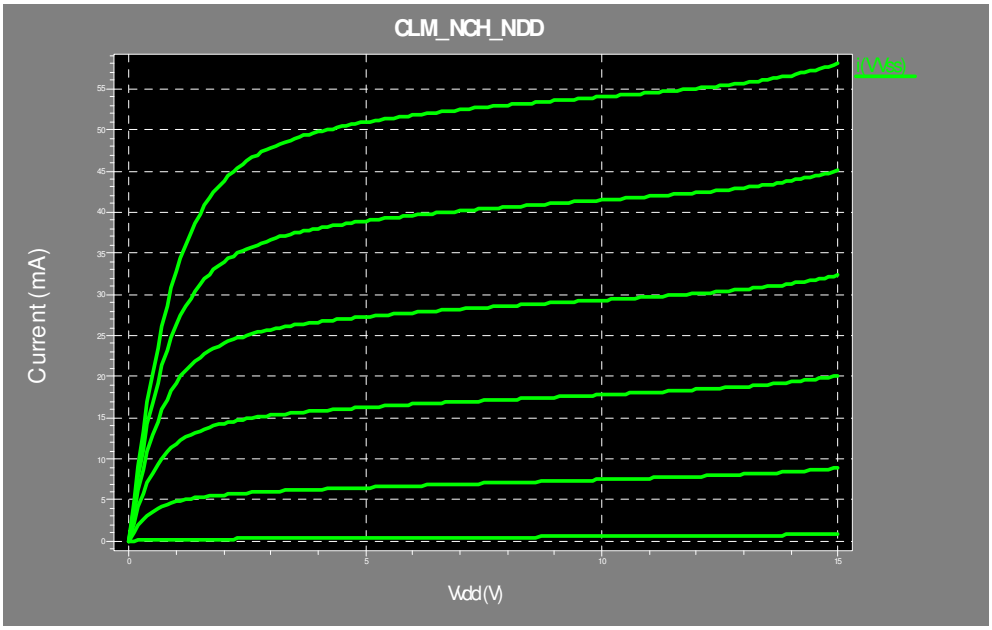

Figure 5.4: NMOS with NDD ID vs. VDS sweep, over different VGS voltages

5.2 Current Mirror Multiplication

This section covers the operation of the current multiplier stage of our overall circuit. In Chapter 4 a circuit that created NMOS and PMOS current biases was covered. The circuit covered in this section will use these current biases to mirror and multiply the current generated within the regulated current biases.

An in depth analysis of how the CLM discussed in Section 5.1 affects this circuit and the technique used to alleviate the side effects of CLM will be presented. Additionally results from stability analysis and transient design considerations will also be supplied.

The simplest way to perform current multiplication while dealing with modern MOSFET devices is to employ current mirrors. Figure 5.5 displays a diagram of a simple current mirror that can be used to multiply current. If we assume the bias PMOS device

is in saturation then the first order transistor equation provides good insight into why the current mirror works so well. In the equation below it can be seen that if the VGS stays at the same value, any change in width to length (W/L) ratio will cause a linear change in the IDSAT. This is exactly how the current mirror is used. A VGS is developed on M1 as a result of the I_{BIAS} being drawn through it, and that VGS is sent to M2. If the W/L ratio of M2 is X times larger than the W/L ratio of M1 then X times more current will flow through M2 then M1.

$$IDsat = K'_n {}^{W}/_{L} (V_{gs} - V_{th})^2$$

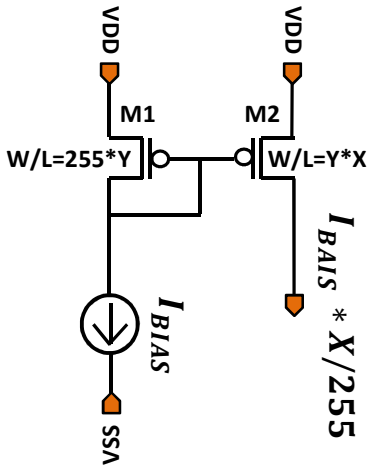

Figure 5.5: Basic current mirror

Figure 5.6 shows a diagram of the push side of the current multiplier. The PMOS devices labeled 1,2,X are intended to indicate the relative W/L ratio. 1 being a W/L=1, 2 being a W/L=2, etc. The sizing of each multiplier leg is binary. In the full version of this circuit there are eight current multiply options, as in W/L=1, 2, 4, 8, 16, 32, 64, 128. This gives the option to have any multiplication factor between 0 and 255. Note that M1 is sized so that the maximum multiplication value will cause the current mirror to output I_{BIAS}.

This technique will scale the multiplication maximum and minimum to fit within our power headroom. The opamp and gating PMOS device will be covered in Section 5.3.

The activation of each current mirror is controlled by a transmission gate coupled to a pull-up or pull-down transistor. In Figure 5.6 these circuits are represented by the blocks labeled "TGATE PULL-UP". Figure 5.7 shows a diagram of the transmission gate with a pull-down device and Figure 5.8 shows a diagram of the transmission gate with a pull-up device. These circuits are used as the gating/activation feature of the current multiplier. D1, D2, and DX from Figure 5.6 connect to the "SELECT" input of the circuit in Figure 5.8. The "P_CURRENT" and gate connections from Figure 5.6 connect to the "IN" and "OUT" terminals within Figure 5.8 respectively.

In the case of the push side of the current multiplier, PMOS devices are used to multiply the bias current. These transmission gate/pull-up circuits act to gate the signal into the current multiplier legs. When selected, the transmission gate will be turned on and the pull-up PMOS will be deactivated. When not selected, the transmission gate will be turned off, the pull-up PMOS will be turned on, and the gate of the non-selected current mirror legs will be pulled up to VDD. This allows the control of a current mirror leg without adding any circuitry into the current path. The gate leakage is relatively low so the resistance of the pass gate does not come into play, which allows it to pass the full signal voltage without any negative side effects. When the circuit is deactivated, the gate of the current mirror is disconnected from the signal and also pulled up to VDD. This shuts off the current mirror completely.

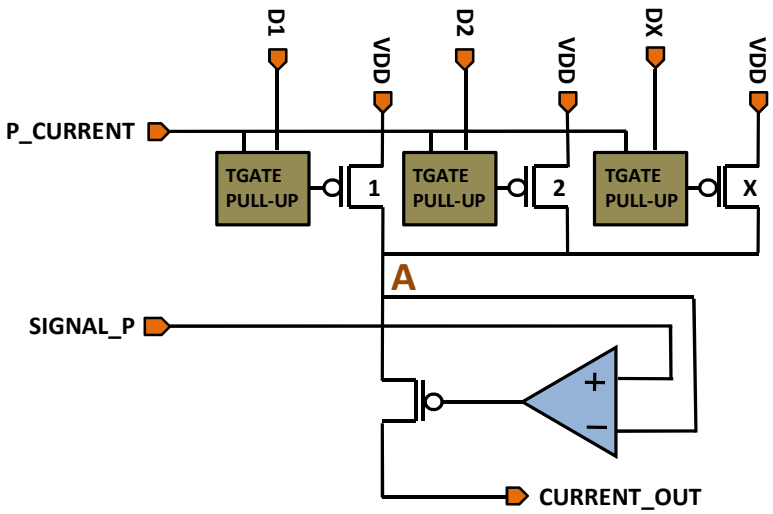

Figure 5.6: Push section of the current multiplier

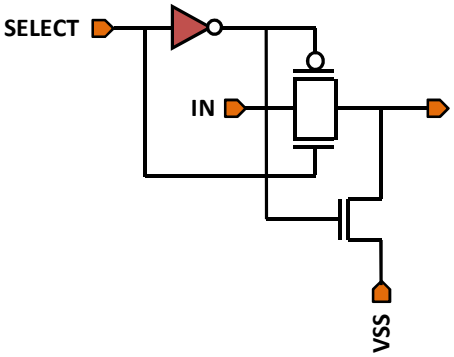

Figure 5.7: Pass gate with integrated pull-down

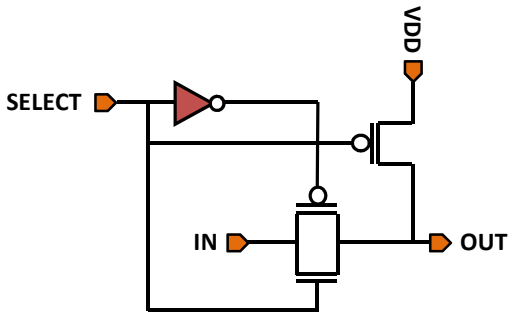

Figure 5.8: Pass gate with integrated pull-up

5.3 Operation of a PMOS Current Multiplier

This subsection will cover the opamp and gating PMOS shown in Figure 5.6. First, the system operation of a full swing current multiplier without the opamp or PMOS is covered. Second, two options to fix the issues that arrive with the removal of the opamp and gating PMOS are covered. Third the full circuit will be covered and the results presented.

The results in Figure 5.10 come from simulations performed on the structure shown in Figure 5.9. As shown, the input bias generation circuit has been put into context within the current multiplication circuit, and the gating PMOS and opamp on the output of the current mirror have been removed. The results in Figure 5.10 show the operation for the entire push and pull current bias and multiplication circuits together. For the sake of keeping the clutter down, only the PMOS side of the circuit is shown within the figures of this section. The entire circuit can be seen in Figure 5.14.

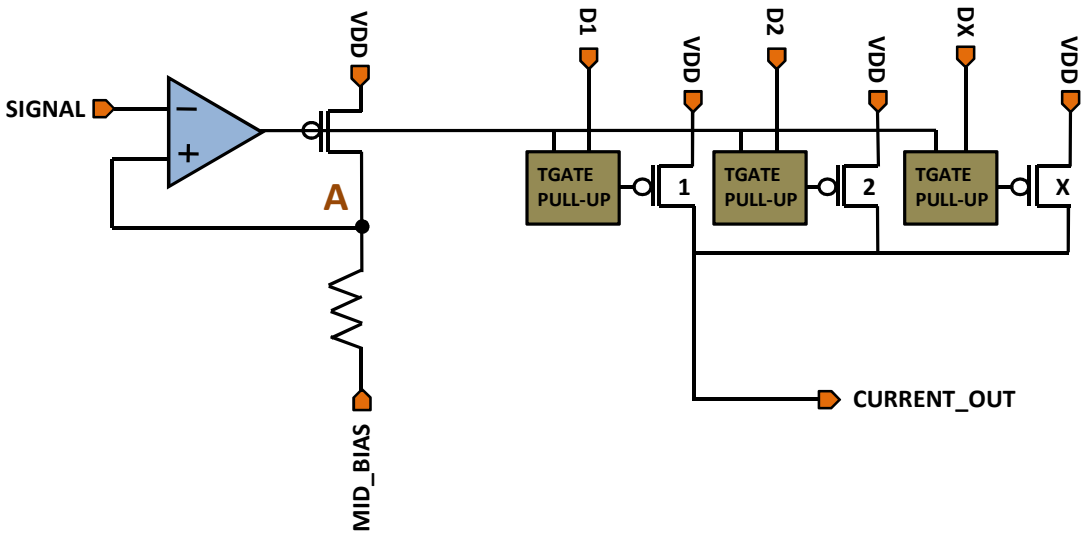

Figure 5.9: Push section of the current bias and current multiplier without gating PMOS or opamp

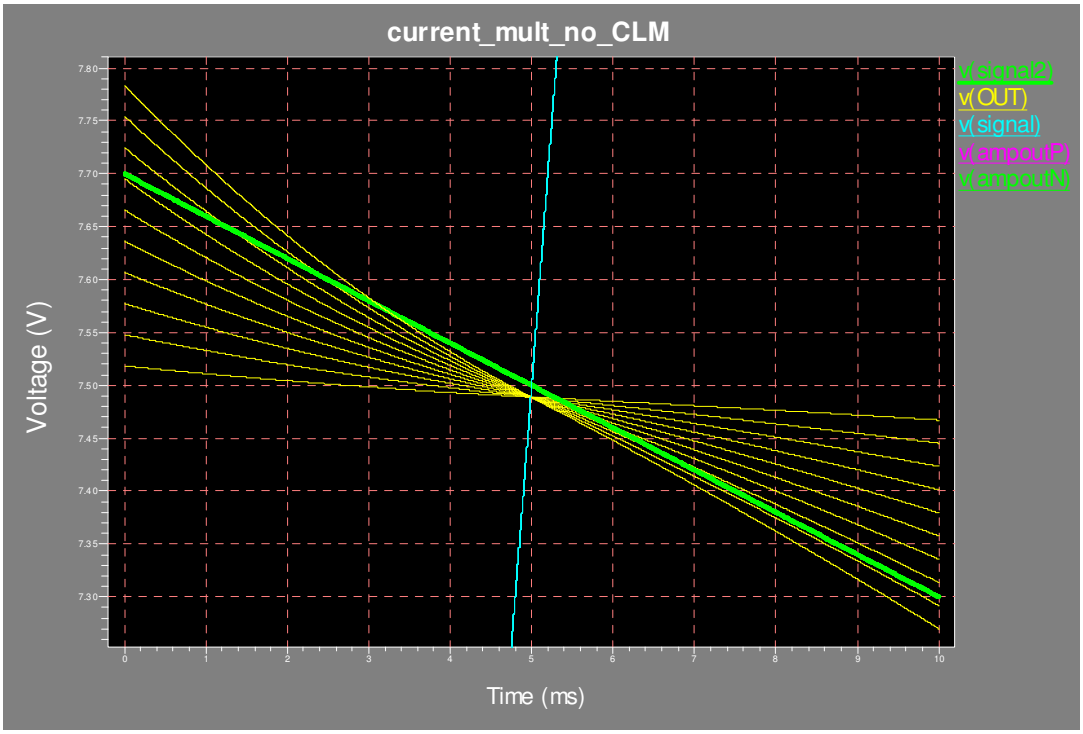

Figure 5.10: Current multiply without voltage gating PMOS and opamp

Figure 5.10 displays some non-ideal effects within the simulation over a selection of multiply settings. The green line represents the input signal and the yellow lines the offending multiply results. The poor operation can be explained through channel length modulation (CLM). As covered in Section 5.1, CLM is the modification of a transistor's IDSAT due to changes in the transistor's VDS. There are a couple of reasons why the results of these simulations are non-linear.

The first thing to point out is that the "CURRENT_OUT" signal within Figure 5.9 actually connects to a transimpedance amplifier that keeps the signal at the "MID_BIAS" level. The transimpedance amplifier is covered in Chapter 6. This means that the VDS across the current multiplication devices is pegged at the "MID_BIAS" voltage. The

second thing to cover is that the current bias circuit by definition makes net "A" within Figure 5.9 equal to the input signal. This means that the VDS across the current bias PMOS varies with the input signal. These two circuit behaviors mean that the CLM is solved for within the regulated current bias and contained within the bias signal sent to the current multiplier. The current multiplier then uses that bias signal to mirror and multiply the bias current. Unfortunately the transistors within the current multiplier maintain a steady, single VDS due to the transimpedance amp. The non-linearity in the simulations is due to this offset.

There are a couple of ways to solve this issue. The simplest method would be to use a resistor on each multiply leg as shown in Figure 5.11. These resistors are sized in order to make the VDS drop across the current multiplication transistors the same as the VDS drop across the current bias transistor. The main issue with this technique is that the current multiplier is really a current divider in the overall circuit. Since the system really divides the current, a multiply of 1 will result in current $I_{Sig} = I_{Bias}/(2^x - 1)$. In order to produce the correct VDS for this situation we would need a resistance of $R_{Sig} = R_{Bias} * (2^x - 1)$. In the case of the full level circuit where X=8, the resistors required to use this technique would be too large for actual implementation.

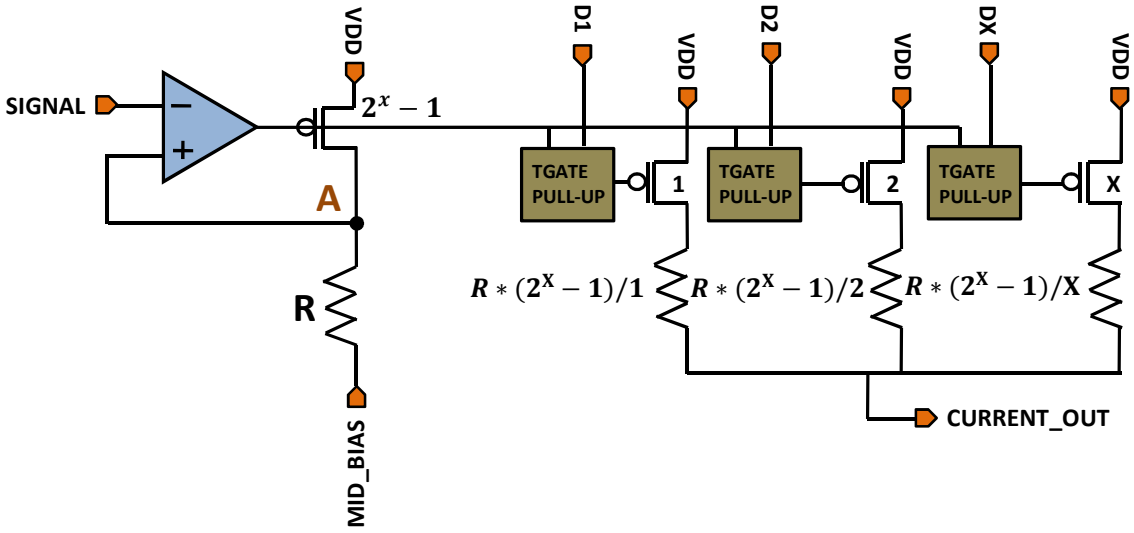

Figure 5.11: Push section of the current bias and current multiplier with resistor based VDS correction

Another option to solve this issue is to use an active regulation system to force the VDS drop across the current multiply transistors to equal the VDS drop across the regulated current bias transistor. This is the technique that was selected for the final circuit that this thesis is based on. Figure 5.12 shows a diagram of this system. The opamp and gating PMOS effectively create an active, dynamically adjustable resistor. The system will make signal "A" within the diagram equal to the drain output of the current bias PMOS device. This will actively control and align the VDS drop on the current multiplication devices with the VDS drop on the current bias PMOS device.

The operation of the circuit in Figure 5.12 is shown in Figure 5.13. The simulation results from a selection of multiply options are shown. Note the increase in linearity over the operation of the circuit shown in Figure 5.9. The VDS correction simulates very well and gives the level of accurate linearity needed for the overall circuit.

Figure 5.14 shows a diagram of the entire circuit with both NMOS and PMOS current biases and current multipliers.

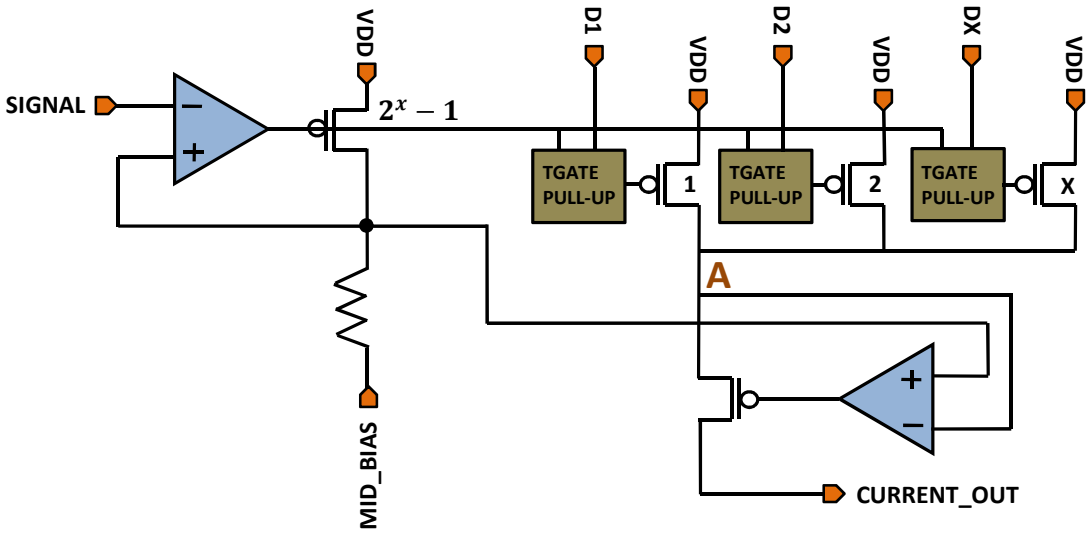

Figure 5.12: Push section of the current bias and current multiplier

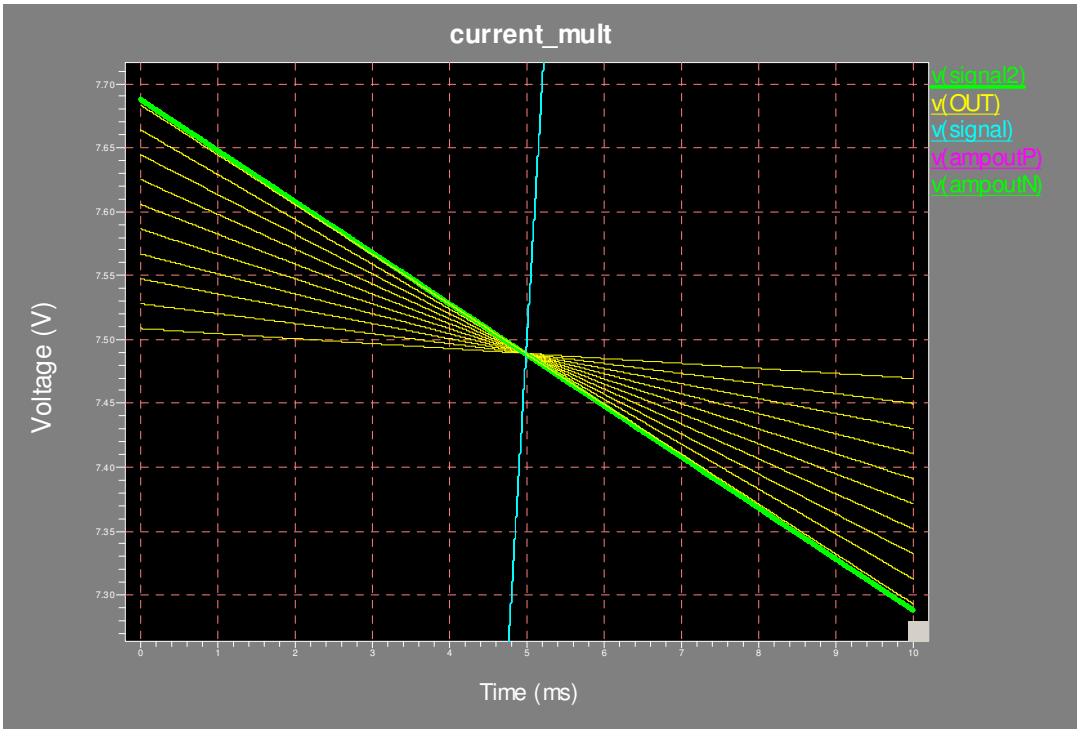

Figure 5.13: Current multiply with voltage gating PMOS and opamp

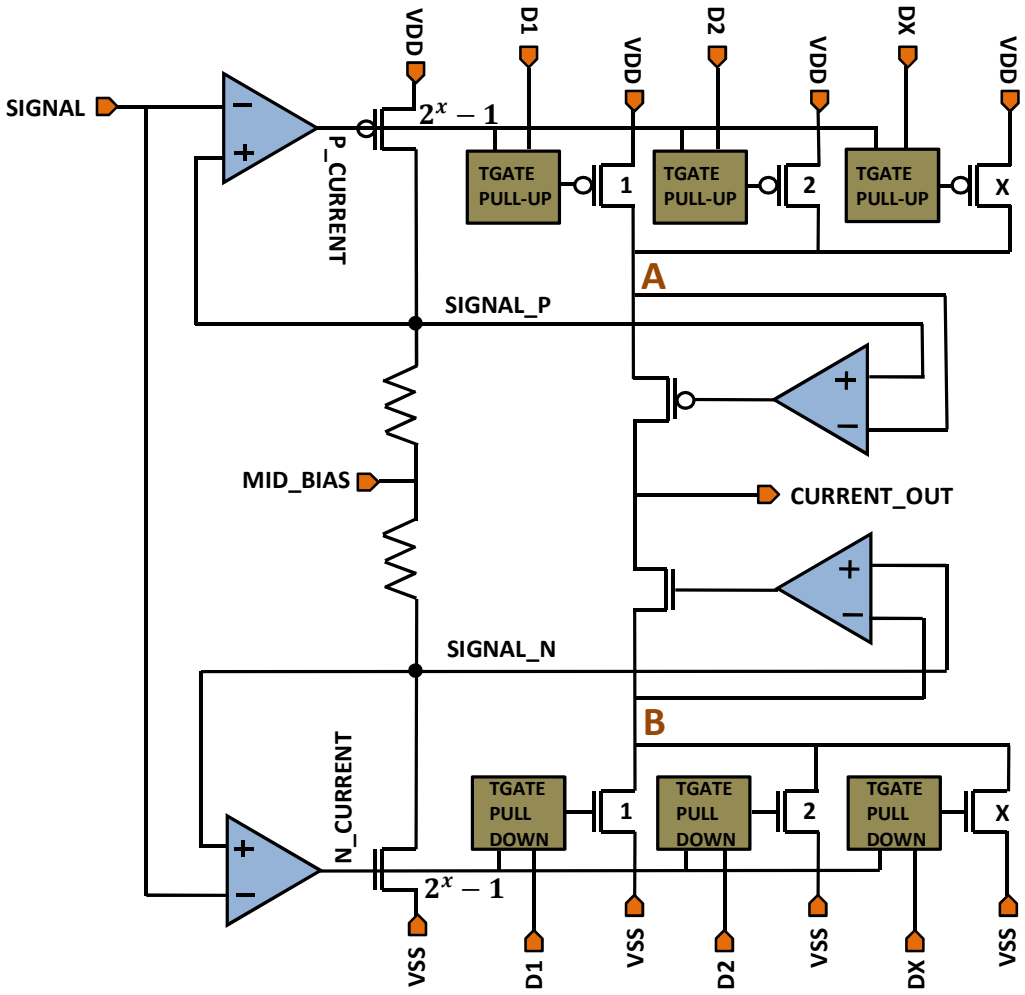

Figure 5.14: Full swing current bias and current multiplier

5.4 Current Multiplier Stability Analysis

This sub-section covers the stability analysis performed on the VDS regulation portion of the current multiplier circuitry. Table 5.1 and Figure 5.17 are provided to detail the frequency response of the PMOS VDS control circuitry. Table 5.2 is provided to detail the frequency response of the NMOS VDS control circuitry. A more detailed explanation for stability analysis in integrated circuitry can be found in Chapter 1.

A large inductor is placed in the feedback loop to disconnect the system from small signal feedback while still allowing the simulator to find a solution to the DC operating point. A large capacitor is placed at net "A" to separate the small signal AC voltage from the DC operating point solution. This setup puts the system into an open loop configuration, injects a small signal voltage input at net "A", and allows the measurement of operations between net "A" and net "B".

Compensation of the VDS control circuitry is not a large task when compared to the compensation of the current bias circuitry covered in Chapter 4. This is largely due to a much lower operating DC gain within the system as compared to the current bias system. The lower DC gain is due to the low gain of the output stage of the VDS control circuitry. The output stage in a small-signal sense is really a source follower. This architecture doesn't allow the output stage to add any voltage gain to the feedback loop. All of the gain in the system is provided by the opamp itself.

The compensation technique covered in Chapter 1 will be used for the opamp section of the circuit. We will introduce a strong dominant pole and a strong nulling resistor within the feedback loop. The dominant pole will help attenuate the frequency response and the nulling resistor will be mainly used to push out the phase response. The phase difference, gain, gain bandwidth, and unity gain frequency is measured between the signal generated at point A within Figure 5.15/Figure 5.16 and the signal at point B across a frequency sweep.

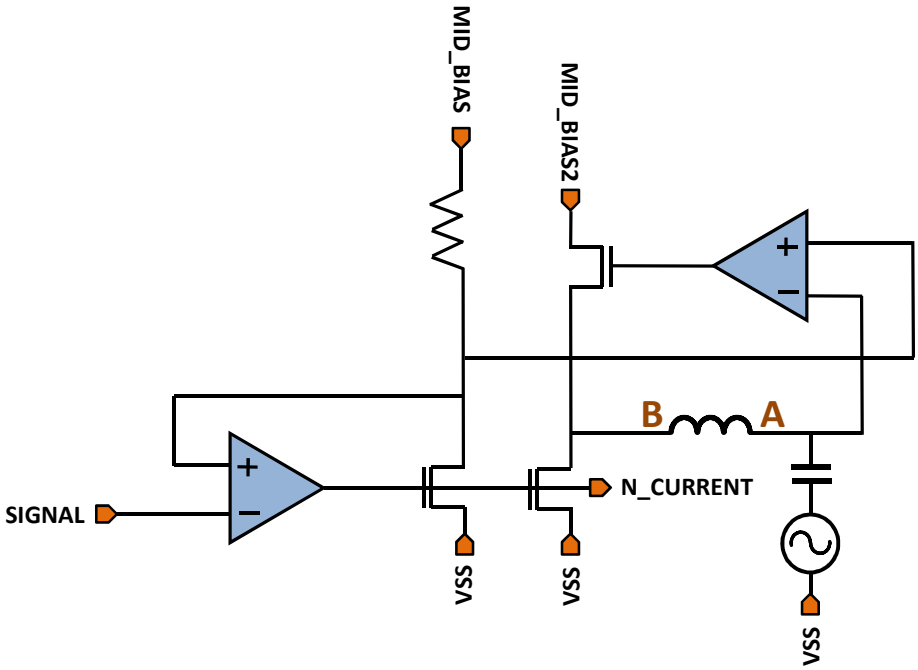

Figure 5.15: NMOS VDS current multiplication control circuitry's stability analysis setup

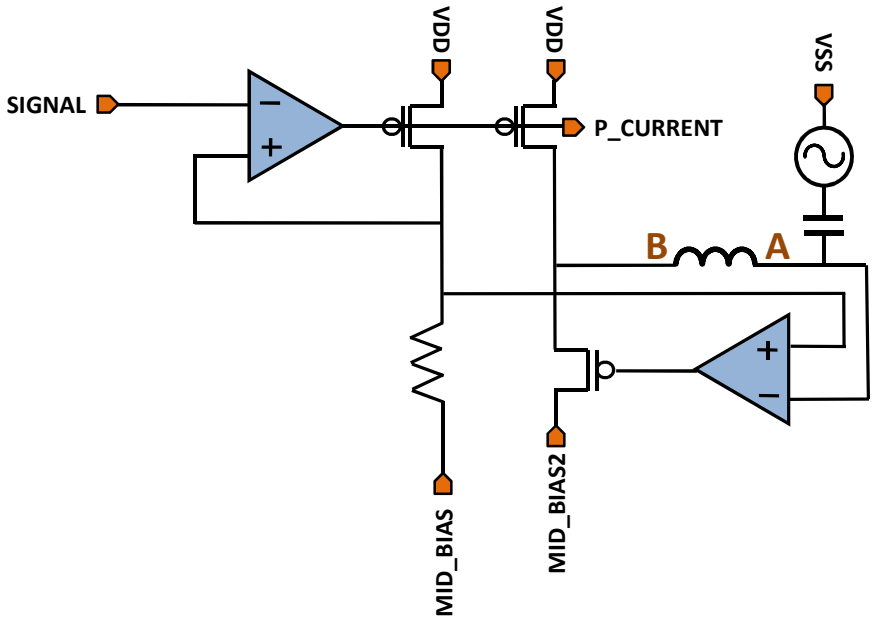

Figure 5.16: PMOS VDS current multiplication control circuitry's stability analysis setup

corner	temp	my_initial_gain_db	my_three_db_freq	my_unit_freq	my_phase_margin
TT	-55	6.32E+01	4.13E+03	5.94E+06	8.53E+01
TT	0	6.19E+01	3.51E+03	4.35E+06	8.44E+01
TT	55	6.09E+01	3.03E+03	3.35E+06	8.38E+01
FF	-55	6.25E+01	5.39E+03	7.20E+06	8.64E+01
FF	0	6.12E+01	4.65E+03	5.28E+06	8.53E+01
FF	55	6.00E+01	4.08E+03	4.06E+06	8.46E+01
SS	-55	6.39E+01	3.09E+03	4.81E+06	8.44E+01
SS	0	6.27E+01	2.59E+03	3.52E+06	8.37E+01
SS	55	6.17E+01	2.21E+03	2.71E+06	8.33E+01

Table 5.1: NMOS VDS current multiplication control stability analysis results

corner	temp	my_initial_gain_db	my_three_db_freq	my_unit_freq	my_phase_margin
TT	-55	5.55E+01	1.13E+04	6.63E+06	8.46E+01
TT	0	5.44E+01	9.44E+03	4.88E+06	8.34E+01
TT	55	5.36E+01	8.00E+03	3.78E+06	8.26E+01
FF	-55	5.46E+01	1.48E+04	7.85E+06	8.58E+01
FF	0	5.34E+01	1.27E+04	5.83E+06	8.44E+01
FF	55	5.24E+01	1.10E+04	4.51E+06	8.32E+01
SS	-55	5.63E+01	8.43E+03	5.48E+06	8.35E+01
SS	0	5.54E+01	6.90E+03	4.02E+06	8.25E+01
SS	55	5.47E+01	5.76E+03	3.11E+06	8.19E+01

Table 5.2: PMOS VDS current multiplication control stability analysis results

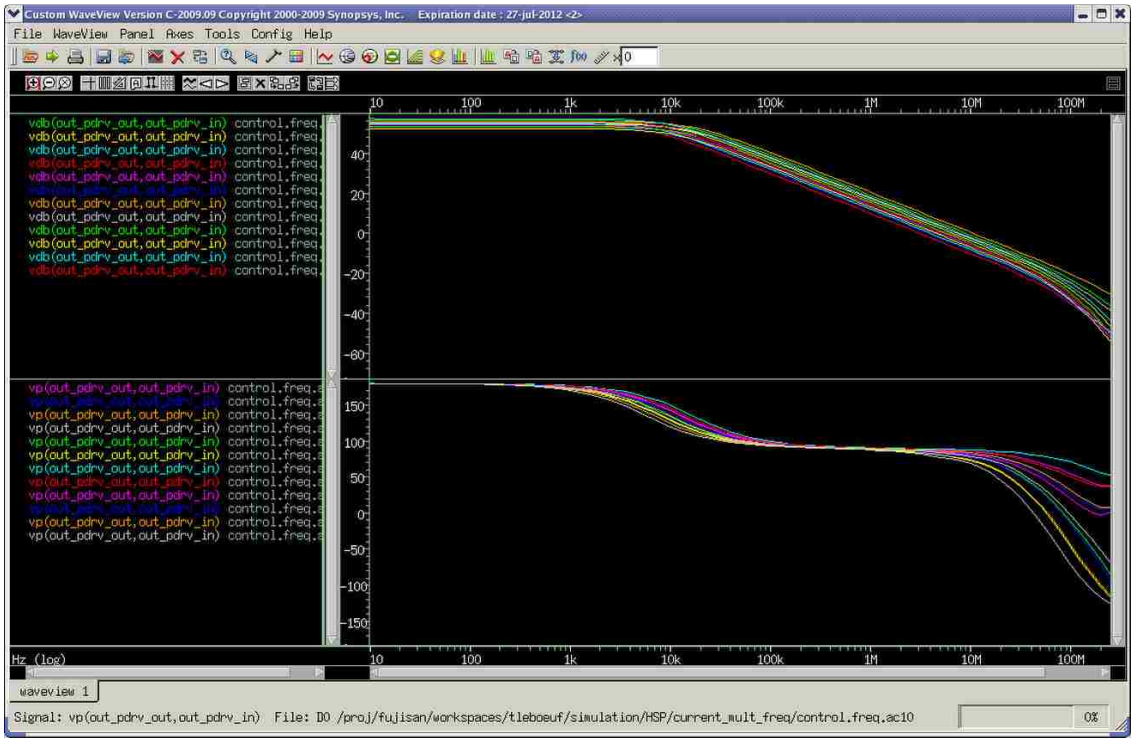

Figure 5.17: Wave forms of the PMOS VDS current multiplication control stability analysis

Chapter 6

Signal Current to Signal Voltage Conversion

6.1 Introduction

This section covers the operation and design of the final stage current to voltage converter. It is used to add the currents from all of the multiply stages and output a corresponding signal voltage. Section 6.2 covers the transient design concerns for this circuit and Section 6.3 covers the frequency analysis of the circuit.

6.2 Operation and Design

This circuit is essentially the same architecture as the regulated analog inverter covered in Chapter 3 with one main difference. The regulated analog inverter has a voltage input and this circuit has a current input. The regulated analog inverter features a resistor in line with the voltage input, which effectively coverts the input voltage into a current, which then feeds into the circuit covered within this section.

Figure 6.1 shows the diagram of the regulated current to voltage converter. The architecture is setup to take advantage of negative feedback. Under this configuration, the opamp will alter its output in effort to align its input voltages. If a current is sent to the "SIGNAL_CURRENT" input, the opamp will reduce its output voltage in order to keep the negative input at the same value as the "MID_BIAS" input. The simple equation describing this operation is $-VOLTAGE\_OUT = I_{SIGNAL}/R$.

Resistor "R" is sized in accordance to the maximum I_{SIGNAL} that the circuit will deal with and the maximum current the opamp can supply. In the overall circuit, each

current multiply stage can generate a maximum of 100uA of signal current. There are four current multiply circuits connected in parallel to the regulated current to voltage converter so a maximum of 400uA must be dealt with. Chapter 4 discussed a circuit that will create a current bias based on a resistor value. That setup has the same basic Ohm's law relationship that this circuit has with its resistor. It is setup so that at a maximum current multiply, the output current will equal the current being generated in the current bias circuit. We can use the current bias circuit's resistor size to determine the current to voltage converter's resistor size. Since there are four current bias and current multiply circuits we can simply use ¼ the resistor size those circuits use. This means that if all four current multiply circuits are on their maximum settings, the system will not exceed the power supply headroom.

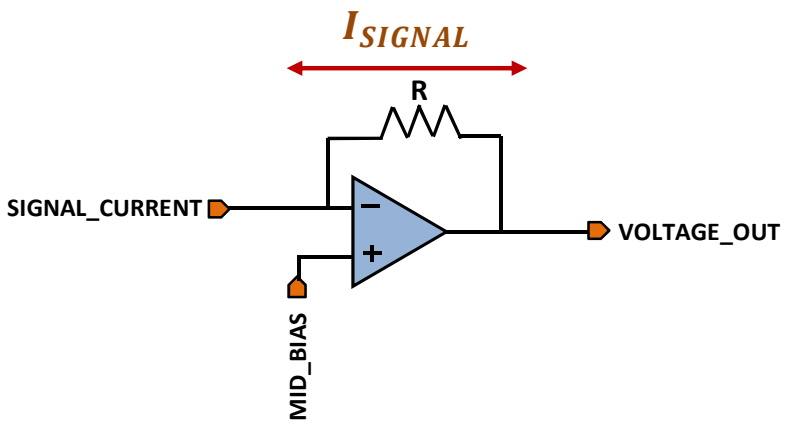

Figure 6.1: Regulated current to voltage converter

6.3 Current to Voltage Converter Frequency Analysis

This sub-section covers the frequency domain design results and theory of the regulated current to voltage converter. The circuit shown in Figure 6.2 shows the test setup used for this circuit. A large inductor is placed in the feedback loop to disconnect the system from small signal feedback while still allowing the simulator to find a solution to the DC operating point. A large capacitor is placed at net "A" to separate the small signal AC voltage from the DC operating point solution. This setup puts the system into an open loop configuration, injects a small signal voltage input at net "A", and allows the measurement of operations between net "A" and net "B". The "LOAD" block within Figure 6.3.1 represents the circuitry that this circuit will be driving.

The simulation results of this circuit are shown in Table 6.1. Wave form results are shown in Figure 6.3.

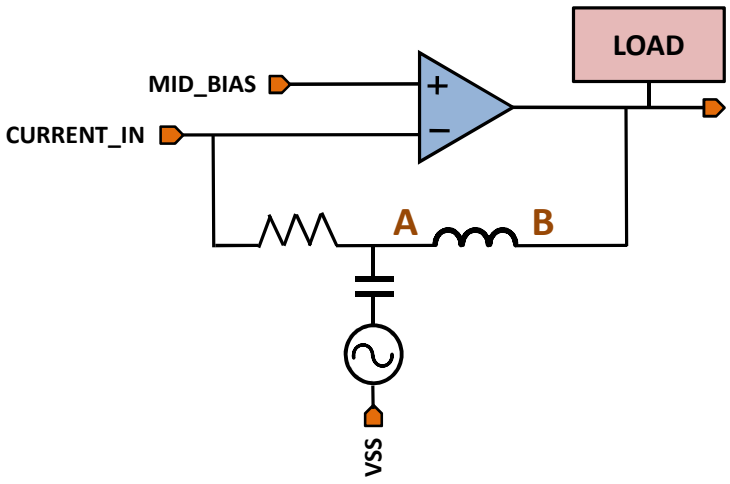

Figure 6.2: Stability analysis setup for the regulated current to voltage converter

corner	temp	my_initial_gain_db	my_three_db_freq	my_unit_freq	my_phase_margin
TT	-55	6.28E+01	4.03E+03	5.50E+06	8.67E+01
TT	0	6.20E+01	3.20E+03	3.96E+06	8.56E+01
TT	55	6.13E+01	2.66E+03	3.03E+06	8.50E+01
FF	-55	6.21E+01	5.29E+03	6.65E+06	8.78E+01
FF	0	6.12E+01	4.25E+03	4.82E+06	8.65E+01
FF	55	6.05E+01	3.56E+03	3.71E+06	8.57E+01
SS	-55	6.35E+01	3.03E+03	4.47E+06	8.57E+01
SS	0	6.26E+01	2.41E+03	3.20E+06	8.48E+01
SS	55	6.19E+01	1.99E+03	2.44E+06	8.43E+01

Table 6.1: Results of the active current to voltage converter frequency analysis

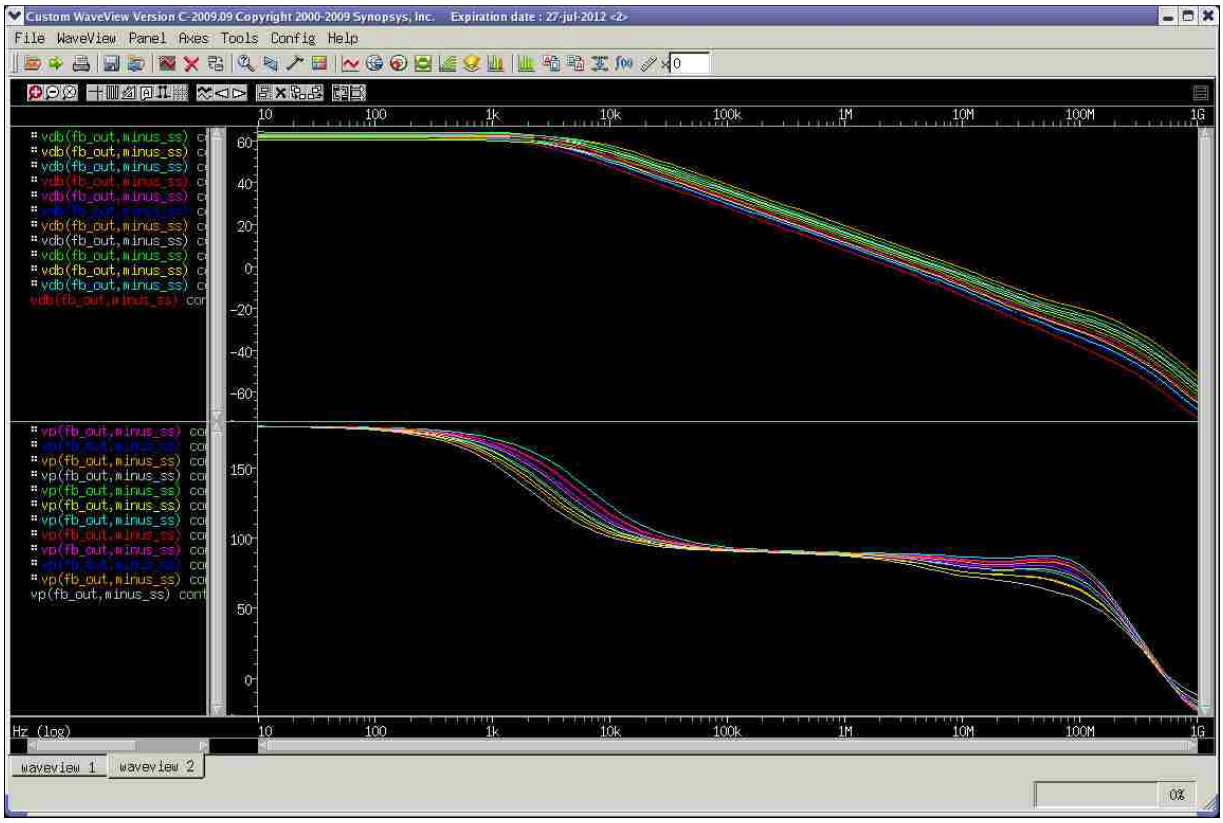

Figure 6.3: Wave forms of the active current to voltage converter frequency analysis

Chapter 7

Top Level Analog Multiply and Accumulate System

7.1 Introduction

This section will cover the analog signal multiply and accumulate circuit in its entirety. The simulation results for the circuit in the context of processing an image will also be covered.

7.2 Top Level Operation

Figure 7.1 shows the combination of Figure 3.2, the input stage, and Figure 5.14, the current bias generator and current multiplier circuits. This figure shows the overall multiply section. The signal first arrives at a buffer. The buffer drives to one input of a two input multiplexor (mux) and an analog signal inverter that drives to the other input of the mux. The mux is used to provide the ability to create a negative multiply. If the multiplier value is negative, the signal is simply inverted. The signal coming out of the mux then feeds into both the push and pull current bias generation circuits. As covered in Chapter 4, these circuits create current biases that then feed to multiplying current mirrors. The VDS is then corrected across the current multipliers and a multiplied current is generated.

Figure 7.2 displays the total multiply and accumulate system. The green blocks represent the current multiplier shown in Figure 7.1. As covered in Chapter 5 there are eight multiply bits in the full circuit; the multiply bits between D2_X and D8_X are represented by the "…" characters. Each current multiplier output simply connects to the

same line in parallel. Since currents add and subtract in parallel, our accumulation stage is easily accomplished with just a wire. The last circuit in the system is the regulated current to voltage converter. It will take the accumulated currents and produce and output voltage.

Figure 7.3 shows the results from every possible positive and negative multiply with a single signal driving each multiply section's signal input. Figure 7.4 is a close-up shot of the different multiply options. These figures show a small percentage of the possible multiply combinations, as the input of each multiply block is tied together.

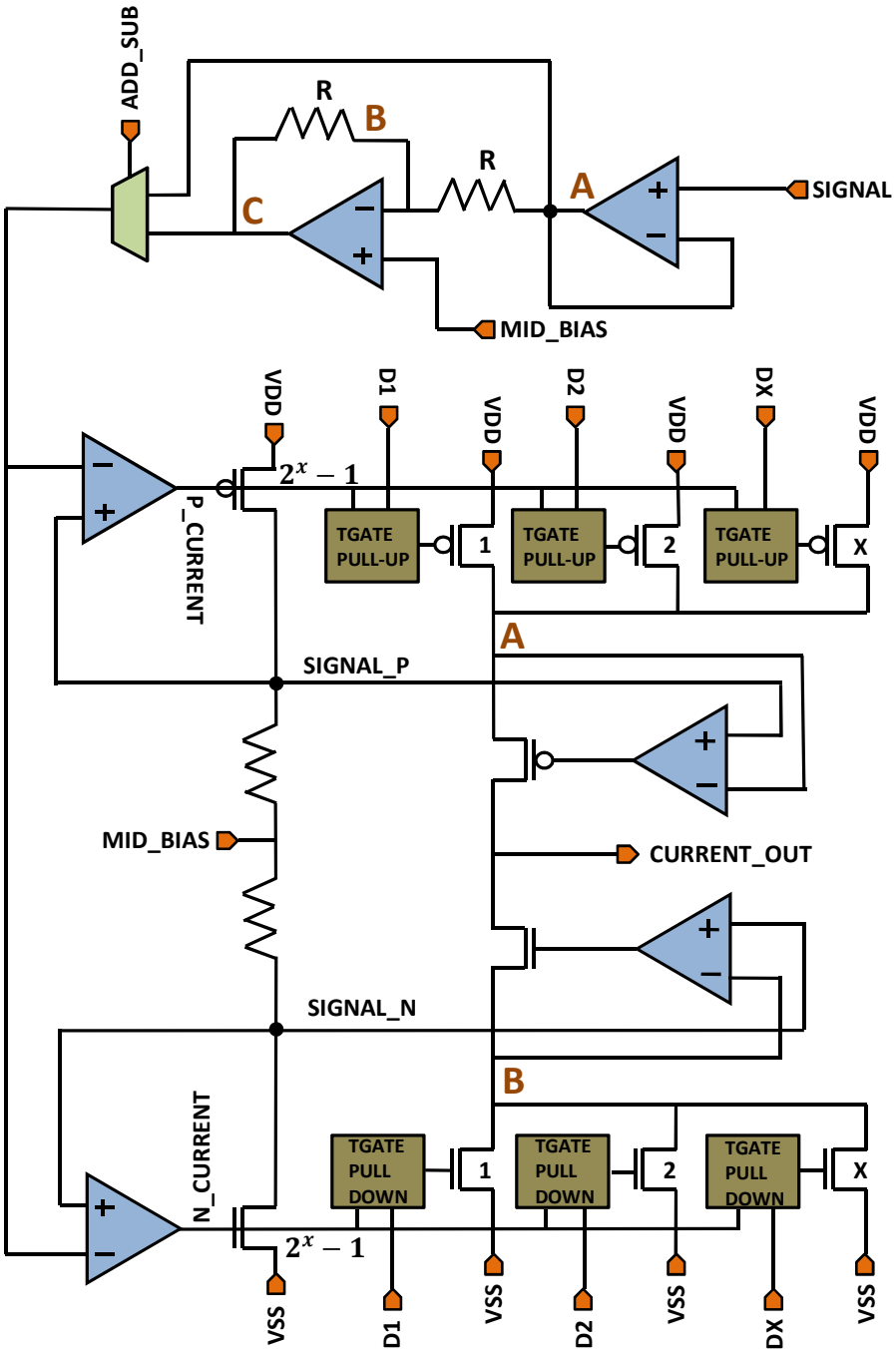

Figure 7.1: Full swing current bias and current multiplier with optional inversion input stage

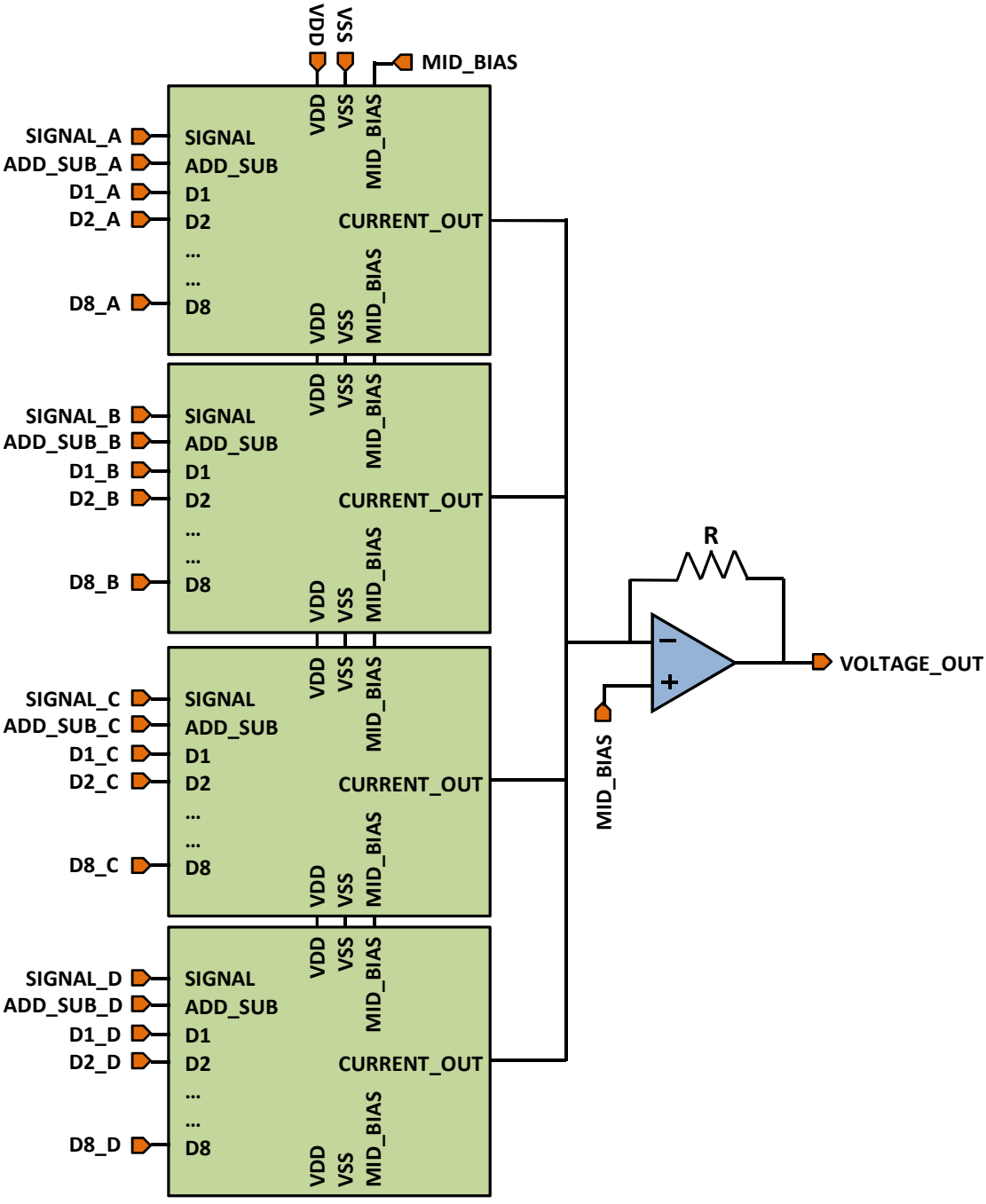

Figure 7.2: Full analog signal multiply and accumulate circuit.

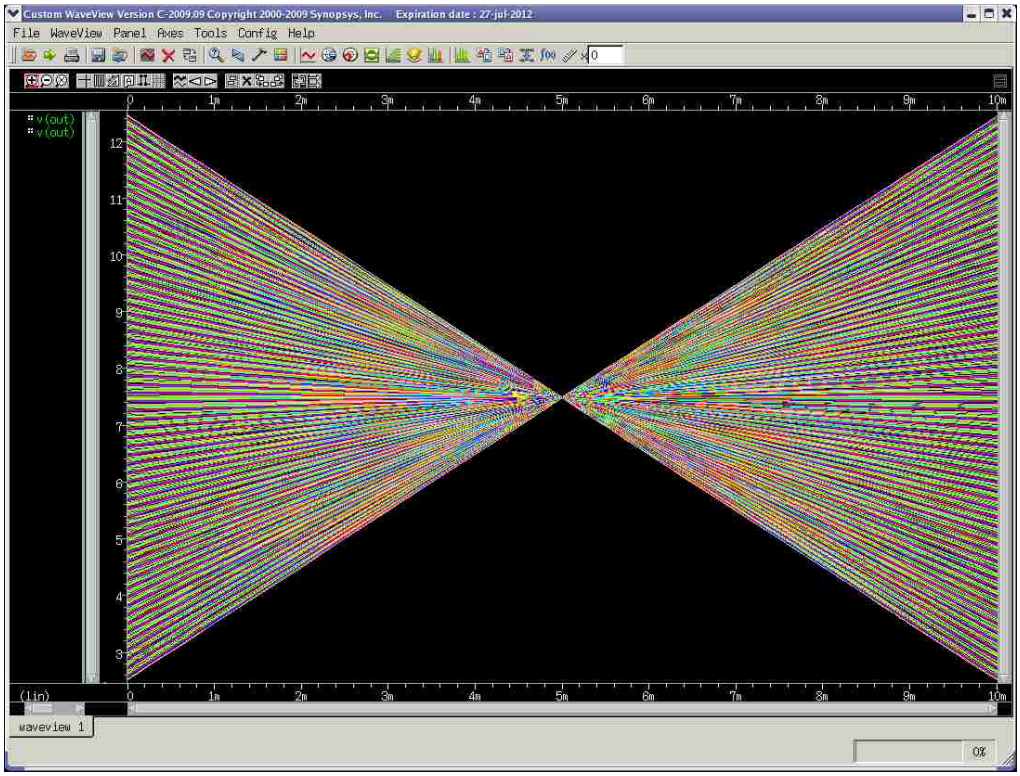

Figure 7.3: Full view of multiply options

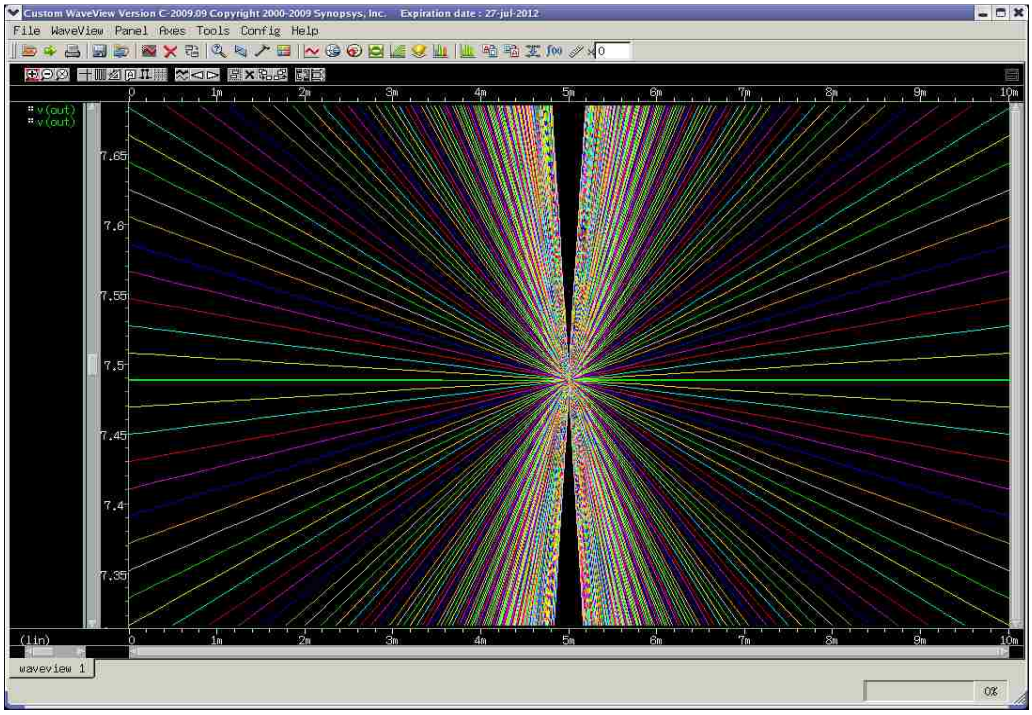

Figure 7.4: Close-up view of the multiply

7.4 Full System Simulation of With Real World Inputs

The system shown in Figure 7.2 is actually one of the multiply and accumulate sections shown within Figure 1.1, which is discussed in Chapter 1. The system shown in Figure 1.1 can be emulated with the circuitry presented in this chapter by simply running different photodiode based voltages and multiplication factors through the circuit and finding the set of voltages and multiplications that yield the greatest result.

The signals group at UNM provided a series of multiplication weights and input voltages with which to test the circuit out.

The weights and input voltages are as follows:

$\mathbf{W}_1$ = [15 -109 32 10], $\mathbf{W}_2$ = [24 -63 -5 -8], $\mathbf{W}_3$ = [11 3 -128 24]

$\mathbf{V}_1$ = [5.00 0.09 0.29 3.11], $\mathbf{V}_2$ = [4.45 0.05 0.10 1.19], $\mathbf{V}_3$ = [4.20 0.04 0.11 2.99]

As shown within Figure 1.1 the algorithm to apply the filter weights to the input voltages is:

$a_i = \mathbf{w}_i^T \mathbf{V}_1$, $b_i = \mathbf{w}_i^T \mathbf{V}_2$, $c_i = \mathbf{w}_i^T \mathbf{V}_3$

Where i = 1, 2, 3

$\mathbf{F}_1 = [a_1, a_2, a_3]$, $\mathbf{F}_2 = [b_1, b_2, b_3]$, $\mathbf{F}_3 = [c_1, c_2, c_3]$.

When these weight/voltage combinations are calculated, the results are as follows:

$\mathbf{F}_1$ = [**105.57**, 88.0, 92.79], $\mathbf{F}_2$ = [76.4, **93.63**, 64.86], $\mathbf{F}_3$ = [92.06, 73.81, **104.0**]

The results from the simulation using the same inputs are as follows (in Volts):

$\mathbf{F}_1$ = [**7.6030**, 7.5858, 7.5898], $\mathbf{F}_2$ = [7.5745, **7.5913**, 7.5631], $\mathbf{F}_3$ = [7.5898, 7.5719, **7.6014**]

The results are near to 7.5 because 7.5 is the determined mid-point between the power rails and serves as the "zero" point in the simulation. The numbers are all close in value due to the overall resolution of the system. If all the inputs are maxed out at 5v and the multiply is set to 255 (2^8-1) then the maximum result is 5100V. The system will scale this voltage down to 12.5V by design. If the ratio of the unscaled hand created result is compared to the ratio of the simulation results we see:

5V/(7.603V-7.5V)=48.5

5100V/105.57V=48.3

The ratios are fairly close, which tells us that the system is working as expected.

Chapter 8

Description of Test Chip Layout

8.1 Introduction

This chapter will discuss the layout of the test chip that was taped out. The test circuit contains a small version of the overall system and is intended to verify the basic current bias and multiplication scheme. The device names used in this chapter relate to the devices shown in Figure 2.1.

8.2 Layout Descriptions

Figure 8.1 displays the layout of the NMOS differential pair used within the opamp designs. The red highlighted parts are the wires and actual poly gates of transistor M3. The orange highlighted parts are the wires and poly gates of transistor M2.

There are a few key elements in this layout. Being that M2 and M3 are a matched pair, their overall matching is extremely important. This layout shows the checkerboard configuration. M2 and M3 are interwoven to reduce the potential of any non-ideal processing event effecting one device and not the other. Also note that the matched pair is guard ringed with an active diffusion that is grounded. This will effectively create somewhat of a power island for the matched pair and help with any oddities that may crop up within the bulk silicon.

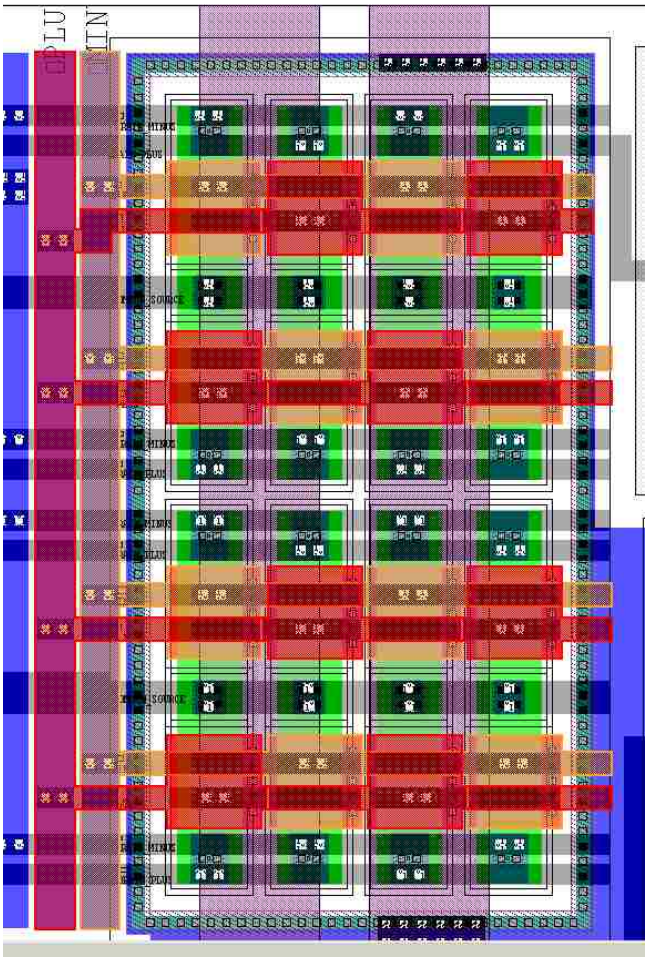

Figure 8.1: NMOS differential pair

Figure 8.2 displays the layout of the complete opamp. The leftmost device is the current bias PMOS, M9. The pink and green connected matched pair is the PMOS active load for the differential pair, M4 and M5. The yellow and light blue connected devices are the NMOS side of the current bias and the diffamp current sink, M8 and M1 respectively. The red and orange connected devices are the differential amplifier matched pair, M2 and M3. The large device on the bottom (cut off) is the compensation capacitor. Finally the two rightmost devices are the output stage PMOS, M6, and the output stage NMOS, M7.

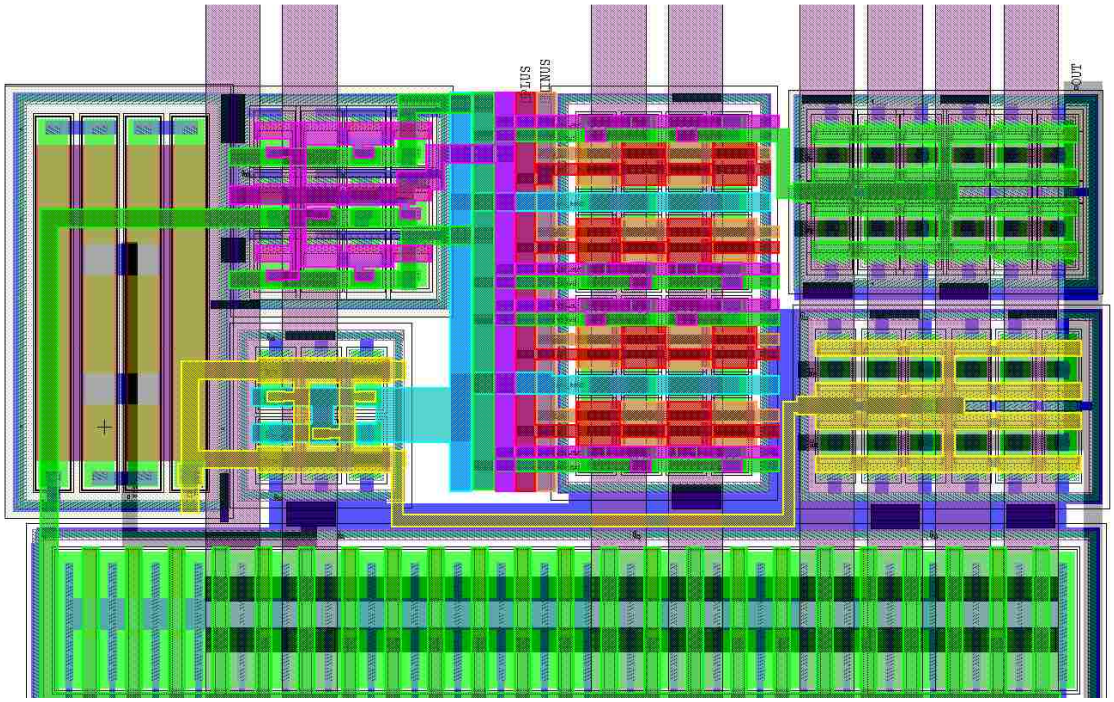

Figure 8.2: Two stage NMOS differential pair operational amplifier with highlights of key nets

Figure 8.3 displays the top level layout of the test structure. As mentioned earlier the system is a bare-bones version of the total circuit. There are two current multipliers; each with only a 2 bit multiply and a bit for signage, and a current to voltage converter.

The top two thirds of the layout are the two current multipliers. The leftmost section of the current multiplier is the optionally selectable signal inverter and buffer. The middle section is the current bias generation circuitry. The rightmost section shows the pass gate/pull-up and current mirror devices. The bottom third of the circuit shows the current to voltage converter and the output buffer.

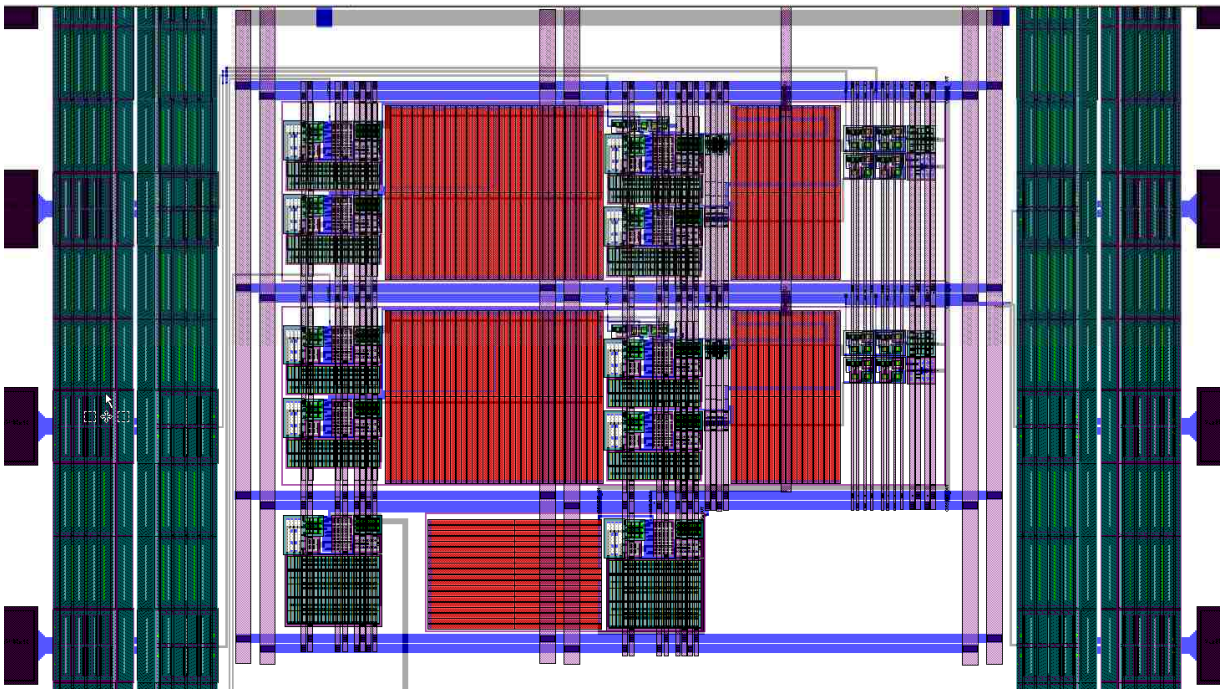

Figure 8.3: Full test chip layout with positive and negative 2 bit multiply

Chapter 9

Conclusion and Future Work

9.1 Conclusion

This thesis presented an analog circuit that can implement filters that use a multiply and accumulate algorithm. The circuit is intended to be used in conjunction with a read out integrated circuit and a focal plane array. Since the entire signal processing regime happens within the analog domain, all of the necessary circuitry to perform operations such as block recognition and image classification can take place within the same micro-chip that houses the read out integrated circuit. This opens up a level of speed and parallel processing that is not easily obtainable with a normal multi-system digital signal processing architecture.

My overall idea for this thesis was to provide and describe my personal design flow: The introduction and definition of the problem, the architecting of the system, figuring out and designing each sub-component, simulating and validating the top level circuit, and finally the actual circuit layout.

9.2 Future Work

There is still work to do on this circuit. There is a test chip currently in the process of fabrication that will need to be verified. The full version of the circuit, as presented in this thesis, still needs to be laid out and verified as well.

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