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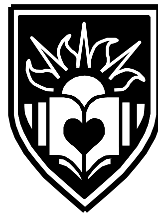
Amorphous Metal-Oxide Based Thin Film Transistors on Metal Foils: Materials, Devices and Circuits Integration

by

Shahrukh Akbar Khan



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Abstract

Amorphous oxide semiconductors are a new class of materials with electrical and optical characteristics uniquely suited to large area flexible electronics. In particular, amorphous indium-gallium-zinc oxide (a-IGZO) thin films have garnered considerable interest due to room temperature processing, large area uniformity and visible transparency. These are ideal traits for using them as active layers in thin film transistors (TFTs) which form the backbone of active matrix display and other large area electronic applications; however, for these devices to be commercially viable, an in-depth analysis of device operation and reliability is warranted.

In this dissertation we present fabrication and characterization of RF sputtered a-IGZO TFTs on flexible metal foils. Dimensionally stable flexible steel foils allows greater freedom to integrate small feature TFTs for high performance analog and digital circuitry and active matrix based display system. Compared to a-Si:H TFTs, a-IGZO TFTs have a much higher field-effect mobility (μ_{FE}=7~15 cm^2/Vs), a low threshold voltage (V_T~0V) exhibiting enhancement mode operation, excellent switching properties (subthreshold swing ~370mV/dec), low Off-current level (around 10 pA) and a small parasitic series resistance employing Mo as source/drain electrode without the need of additional contact doping. Nonlinearity of the TFT transfer characteristics (I_{DS}-V_{GS}) in a-IGZO TFTs manifests in a gate bias (V_{GS}) dependent field-effect mobility due to the finite conduction band-tail slope in a-IGZO. The field-effect mobility is weakly thermally activated with an activation energy around 15 meV, while the threshold voltage linearly

decreases with temperature with a coefficient of -17.5 mV/°C. In these TFTs, minimal hole accumulation occurs which bodes well for greater control of threshold voltage. The interface of SiO_2/a-IGZO is probed with a subthreshold slope technique with extracted interface trap density, D_{it} values near the conduction band edge to be around $5x10^{13}$ $cm^{-2}eV^{-1}$. The origin of the low frequency noise of a-IGZO TFTs with SiO_2 gate dielectric is identified as a generation-recombination (g-r) noise component at drain currents below 5 nA and a pure 1/f noise at higher drain currents.

To address the reliability issues in a-IGZO TFTs, electrical instability due to DC bias-temperature stress is studied. A novel low temperature N_2O plasma treatment is developed and shown to have remarkable effects in suppressing threshold voltage shift (ΔV_T) which improves device stability. A stretched exponential model originally developed for a-Si:H TFTs has been successfully applied to describe the bias stress instability mechanisms for plasma treated a-IGZO TFTs. It is suggested that post N_2O treatment passivates the interface states and homogenizes the poor quality a-IGZO film with reduced sub-gap defect density.

The effect of mechanical strain on the performance of a-IGZO TFTs and circuits is systematically investigated which can provide a better understanding of IGZO TFT performance when flexed. A whole range of circuits and systems based on a-IGZO TFTs are demonstrated which validates the technological importance of this material. The relative high performance of the discussed circuits bodes well for on-panel monolithic integration of more involved circuits to drive active matrix displays or other large area electronic systems.

Chapter 1

Amorphous Oxide Based Semiconductor Materials for TFTs and Large Area Electronic Applications

1.1 Introduction

In recent years great strides have been taken in the development of thin film transistors (TFTs) using nonconventional materials such as transition metal oxide conductors and semiconductors. These transition metal oxides are a special class of materials with high transparency in the visible spectrum and controllable carrier concentration. This is unique since transparency and conductivity are thought to be somewhat mutually exclusive as the high band gap (>3 eV) makes carrier doping

challenging. The use of these metal oxide materials has thus ushered in the era of "Transparent Electronics". Two competing approaches to oxide electronics appear to be emerging, involving the use of either a binary metal-oxide or an amorphous oxide semiconductor (AOS) as the thin-film transistor (TFT) channel layer. The binary metal-oxide path virtually always relies on the use of zinc oxide (ZnO), although other binary metal-oxide candidates such as tin oxide (SnO_2), indium oxide (In_2O_3), or titanium dioxide (TiO_2) have been employed. ZnO, in particular has been extensively studied [1.1] for its application as active layers in semiconductor devices. A series of advances have been reported for ZnO, particularly in terms of film growth technology [1.2], its application in devices such as LEDs [1.3,1.4] and the elucidation of its intrinsic properties [1.5], which led to demonstrations of mesoscopic effects in ZnO heterojunction systems [1.6] and proved that oxides can compete with conventional semiconductors. Although material simplicity is indeed a compelling benefit of this approach to oxide electronics, binary metal-oxides are difficult to manufacture with an amorphous microstructure and, concomitantly, acceptable electronic properties for applications in active electronic applications. Especially, the mobility in ZnO based devices suffers from grain boundary effects. Another serious problem of ZnO, particularly for use in TFTs, is their high concentration of residual free electrons due to native defects such as zinc interstitials and oxygen vacancies. Consequently, it has been difficult to control the threshold voltage and to fabricate normally-off TFTs using polycrystalline ZnO channels.

The second approach based on amorphous oxide materials include materials that are composed of post-transition cations with $(n-1)d^{10}ns^{0}$ ($n \geq 4$) electronic configurations. When multicomponent combinations of these cations are employed, resulting oxides tend to remain amorphous, because of crystal frustration, and yet possess relatively good electron transport properties as a consequence of having conduction bands which are derived from spherically-symmetric s-orbitals with relatively large atomic orbital radii [1.7]. This discovery by *Hosono et al.* in 2004 led to demonstration of room-temperature deposited amorphous indium gallium zinc oxide (IGZO) TFTs using pulsed laser technique on flexible polyethylene terephthalate (PET) substrates. Their work sparked worldwide interest for use of these materials in display and other large area applications since the high mobility of oxide-based TFTs are suited to high resolution displays. At the same time this would enable integration of switching TFTs in the active-matrix and driver-integrated circuits (driver ICs) on the same plastic substrate, which can reduce cost and provide a more compact display. When employed as a semiconductor layer in TFT

Figure 1.1 Unique electrical properties of amorphous oxide semiconductors including wide bandgap, high mobility, low-temperature processing and optical transparency can enable novel electronic applications. [Adapted from Cover Story, Nikkei Electronics Asia, 2007[1.13]].

applications, such materials, namely zinc tin oxide (ZTO), zinc indium oxide (ZIO or IZO), and indium gallium zinc oxide (IGZO), have yielded high-performance thin-film transistors (TFTs) [1.8-1.12].In addition to display control elements, several other applications have been suggested. Depending on deposition conditions, these oxide semiconductors can show sensitivity to humidity or specific gases which make them applicable as sensors [1.14-1.17]. Additionally due to their high performance and ability to be built upon each other in a vertical arrangement, oxide-based TFTs are possible sense and control elements for high density memory applications [1.18]. Figure 1.1 gives the host of applications that are possible by utilizing the advantages afforded by amorphous oxide materials.

1.2 Overview of Transparent Oxide Semiconductors (TOSs)

TOSs are a series of metal oxides, composed of heavy metal cations (HMCs) with an outside shell electronic configuration of $(n-1)d^{10}ns^{0}$ ($n \geq 4$) and oxygen anions [1.7]. In terms of this definition, the candidates of HMCs to form TOSs can be sorted out from the chemical periodic table and their electronic configurations are in Table 1.1.

TOSs (Transparent Oxide Semiconductors) have wide bandgaps in which the ns orbitals of the HMCs (Heavy Metal Cations) primarily constitute the bottom part of the conduction band and the oxygen 2p orbitals form the top of the valence band [1.7]. Uniquely, the spatial spreading of the outside ns orbitals with a spherical symmetry in the

Table 1.1 Candidate TOS and Their Electronic Configuration

Cu $[Ar]3d^{10}4s^1$	**Zn** $[Ar]3d^{10}4s^2$	**Ga** $[Ar]3d^{10}4s^24p^1$	**Ge** $[Ar]3d^{10}4s^24p^2$	**As** $[Ar]3d^{10}4s^24p^3$
Ag $[Kr]4d^{10}5s^1$	**Cd** $[Kr]4d^{10}5s^2$	**In** $[Kr]4d^{10}5s^25p^1$	**Sn** $[Kr]4d^{10}5s^25p^2$	**Sb** $[Kr]4d^{10}5s^25p^3$
Au $[Xe]4f^{14}5d^{10}6s^1$	**Hg** $[Xe]4f^{14}5d^{10}6s^2$	**Tl** $[Xe]4f^{14}5d^{10}6s^25p^1$	**Pb** $[Xe]4f^{14}5d^{10}6s^25p^2$	**Bi** $[Xe]4f^{14}5d^{10}6s^26p^3$

[Ar]: $1s^22s^22p^63s^23p^6$

[Kr]: $1s^22s^22p^63s^23p^63d^{10}4s^24p^6$

[Xe]: $1s^22s^22p^63s^23p^63d^{10}4s^24p^64d^{10}5s^25p^6$

HMCs is much larger than that in light metal cations such as aluminium, leading to a wider conduction band. Since the carrier mobility is inversely proportional to the curvature of the energy versus k-relationship of the conduction band, TOSs are electrically active and differ from light metal oxides such as MgO and Al_2O_3 which are typical insulators [1.19]. The metal ion radius, metal and oxygen bond length and angle

Table 1.2 Electrical Parameters of Common TOS

HMC	TOS	ion radius (pm)	M-O length (Å)	M-O-M angle	Overlap
Zn 4s	**ZnO**	**1.16**	**1.976**	**108.2°**	**0.6045**
Ga 4s	β-Ga_2O_3	0.88	1.978	100.4°	0.4632
Ge 4s	GeO_2	0.71	1.738	130.0°	0.2848
Cd 5s	CdO	1.25	2.348	90.0°	0.6905
In 5s	**In_2O_3**	**0.95**	**2.180**	**98.2°**	**0.5613**
Sn 5s	SnO_2	0.77	2.052	101.9°	0.4523

are among the critical parameters that determine the carrier mobility of these oxide semiconductors. Table 1.2 lists these critical parameters of the common HMCs and TOSs, and their ns orbital overlap integrals [1.19]. As seen from this table, the Zn-Zn 4s and the In-In 5s orbitals have large overlap integrals compared with the other HMCs. As a result, ZnO and In_2O_3 should have high carrier mobility. This has already been proven by Hall-effect measurements: single crystalline n-type ZnO has a Hall mobility of around 200 cm^2/Vs, and single crystalline n-type In_2O_3 has a Hall mobility as high as ~ 160 cm^2/Vs [1.19]. Moreover, the large ns-ns orbital overlap makes the mobility less sensitive to any angular variation or bond stretching in the M-O-M bonds; as such, the mobility of TOSs is immune to the structural disorder because of such ionic bonding. Thus, amorphous TOSs still display considerable carrier mobility comparable to their crystalline counterparts. This characteristic cannot be found in other types of semiconductor materials. For instance, the mobility of polycrystalline silicon (covalent bonding) is 2~3 orders of magnitude higher than that of amorphous silicon (a-Si:H). Despite their large bandgaps, these oxide materials can be processed with native or extrinsic defects that contribute to the creation of free carriers and a positioning of the Fermi level near or within the conduction band. The placement of the Fermi level inside the conduction band might be expected to lead to optical absorption with transitions from the Fermi into empty conduction band states, rendering the materials opaque. Even at high carrier concentration, however, visible transparency is not severely limited.

1.2.1 Amorphous Transparent Conducting Oxides (ATCOs)

ATCOs are composed of post-transition metal oxides exhibiting n-type carriers [1.20, 1.21]. Oxygen vacancies or interstitial low-valence cation (Zn^{+}) dominate the carrier concentration in these ATCO films. For these ATCOs, the mobility is still close to that of the polycrystalline even in the amorphous material. It is very different from a-Si:H, which has a extremely low mobility (<1 cm^2/Vs) compared to the several orders higher mobility in polycrystalline (30~300 cm^2/Vs) or crystalline silicon (>1000 cm^2/Vs). Although there is more than one mechanism explaining the conduction behavior for these ATCOs, the most widely accepted theory of carrier transport is the overlapping of s orbitals in these transition metal atoms [1.19-1.21]. Among various conductive oxides, the InZnO (IZO) system exhibits many advantages for the flexible transparent TFTs such as high field effect mobility, high transparency, room temperature compatible processing, large area deposition by sputtering, plastic substrates available, and is a cheaper process [1.20, 1.22-1.23]. Other conductive oxides may not fit all the requirements for the flexible transparent TFTs. The first requirement is that the film has to be transparent in the visible region, which means the bandgap has to be greater than 3 eV. CdO-PbO and $AgSbO_3$ systems have a bandgap smaller than this requirement [1.24, 1.25]. The second requirement is the film must be amorphous and conductive as deposited in room temperature. CdO-CeO_2 is very resistive (resistivity ~1×10^4 ohm-cm) [1.26] as deposited if no dopants are added in. In addition, Cd^{2+} is toxic against the environment [1.27]. Amorphous In_2O_3 looks like a good candidate, however, when the oxygen ratio increases

a little bit, it becomes polycrystalline [1.24]. ZnO is always polycrystalline as deposited [1.25]. In_2O_3-ZnO systems have a wide range of amorphous materials in In/Zn ratio and various oxygen partial pressure [1.24, 1.25]. In this material system, the carrier concentration can be adjusted by controlling the oxygen partial pressure or the O_2/Ar ratio. a-IZO has high mobility (10~50 cm^2/Vs) [1.23] as deposited at room temperature which is at least one order higher than amorphous Si. Ga_2O_3-ZnO (GZO) system has a little bit lower mobility than IZO. InGaZnO (IGZO) also has a lower mobility compared to IZO [1.25]. The last candidate is ITO, which is widely used for electrodes in LEDs, solar cells and LCDs [1.28-1.30]. Compared to ITO, IZO has a higher work function [1.31-1.33], higher transmittance in the infrared region [1.32], and lower In concentration than ITO [1.34].

1.2.2 TFTs with Multicomponent Oxide Layers: InZnO (IZO)

Several researchers have explored various stoichiometries of indium zinc oxide (IZO) by RF sputtering for TFTs [1.34-1.38]. IZO TFTs typically exhibit high channel mobilities (up to 40 cm^2/Vs), but suppressing carrier concentration is difficult as is the case in binary In_2O_3 and SnO_2 oxides. As a result, many of the reported IZO TFTs are "normally on" devices ($I_{DS} > 0$ at $V_{GS} = 0$ V), i.e., depletion-mode devices. The initial report of IZO-based ($Zn_2In_2O_5$) TFTs employed a staggered bottom gate structure with an atomic layer deposited (ALD) Al_2O_3-TiO_2 superlattice as the gate insulator. Barquinha et al. and Yaglioglu et al. utilize room temperature In_2O_3-10 wt %ZnO as the semiconductor layer in staggered bottom-gate TFTs. Barquinha et al. [1.37] obtain channel mobilities

approaching 40 cm^2/Vs while exploring the effect of semiconductor thickness (15 to 65 nm) on device performance. Yaglioglu et al. [1.38] observed a channel mobility and V_T of 20 cm^2/Vs and -3.2 V, respectively, for their TFTs which employ thermally grown SiO_2 as the gate gate insulator. A route towards solution deposition of IZO has been explored by Lee et al [1.39]. Lee et al demonstrated that IZO via inkjet printing is a viable option to realize the semiconductor layer for TFTs. These IZO-based TFTs exhibit turn-on voltages of -25 V and mobility of 7.4 cm^2/Vs after processing at 600°C.

1.2.3 TFTs with multicomponent oxide layers: InGaZnO (IGZO)

Indium gallium zinc oxide (IGZO)-based TFTs have been fabricated by pulse laser deposition (PLD) and RF sputtering [1.40]. The initial IGZO-based ($InGaO_3(ZnO)_5$) TFTs employed single crystalline IGZO layers, with indium oxide layers alternating with gallium zinc oxide layer, which were obtained through the use of a high temperature anneal and yttria-stabilized zirconia substrates [1.40]. These TFTs employ a coplanar top-gate structure with a 80 nm thick HfO_2 gate insulator. The channel mobility, V_T, and Ion/Ioff are 80 cm^2/Vs, 3 V, and 10^6, respectively. Yabuta et al. explored amorphous IGZO-based ($InGaZnO_4$) TFTs with a staggered top-gate structure [1.41]. RF sputtering is used for deposition of the semiconductor and insulator (Y_2O_3) layers. While no intentional substrate heating is used, the maximum processing temperature is 140ºC due to heating from the sputtering process during insulator deposition. The channel mobility, V_T, and Ion/Ioff ratio are 12 $cm^2/V.s$, 1 V, and 10^8, respectively. Park et al. have formed TFTs via a self-aligned process [1.41]. In this process a top gate device is realized with

100 nm of CVD grown silicon dioxide as the gate insulator. After patterning of the gate electrode and gate dielectric, the device is exposed to argon plasma, whereby creating oxygen vacancies in the exposed semiconductor region, rendering this area more conductive. These conductive semiconductor regions constitute the source and drain regions. Kim et al. [1.42] have demonstrated a passivated IGZO TFT, utilizing a CVD silicon dioxide as the passivation layer. The TFT stack prior to source and drain deposition was annealed at 350ºC. Devices with the passivation layer exhibited a mobility of 36 cm^2/Vs and a V_{on} of 0 V; however devices without the passivation layer showed reduced performance due to damage during the source and drain patterning.

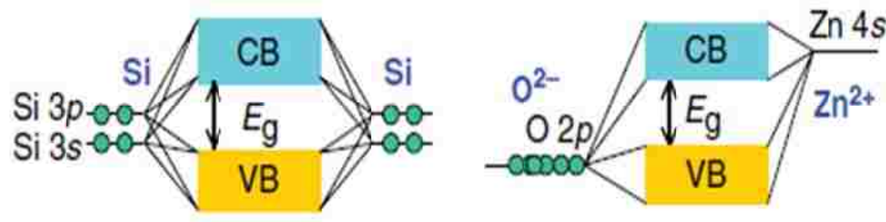

Figure 1.2 Schematic band structures of (a) Si and (b) ZnO. The makeup of CBM and VBM in ZnO by metal s orbitals, and O^{2-} 2p orbitals respectively. [Adapted from Ref. 1.44].

1.3 Carrier Transport in Amorphous Metal Oxides

The electronic structures of most oxides are quite different from those of covalent semiconductors. In the classic covalent semiconductor Si, conduction band minimum (CBM) and valence band maximum (VBM) are made of anti-bonding (sp^3 σ^*) and bonding states (sp^3 σ) of Si sp^3 hybridized orbitals and its bandgap is formed by the

energy splitting of the σ*– σ levels [1.43]. In ionic oxides on the other hand, CBM and VBM are usually formed by different ionic species. CBMs are mainly made up of orbitals from the metal cations, such as Zn^{2+} 4*s* orbitals, and VBMs are mainly made up of O^{2-} 2*p* orbitals. This is schematically shown in Fig 1.2. In representative wide-bandgap oxide

semiconductors like ZnO, SnO, In_2O_3, the unoccupied *s* orbitals of these cations have large spatial sizes and form hybridization even with second neighboring metal [1.44]. This can explain the small electron effective masses typical of these types of oxides. The above electronic structure can also explain the large mobility found in amorphous oxides like a-IGZO. Because of the unique electronic structure, a-IGZO is insensitive to bond angle variance of metal-oxide-metal chemical bonds induced by structural randomness.

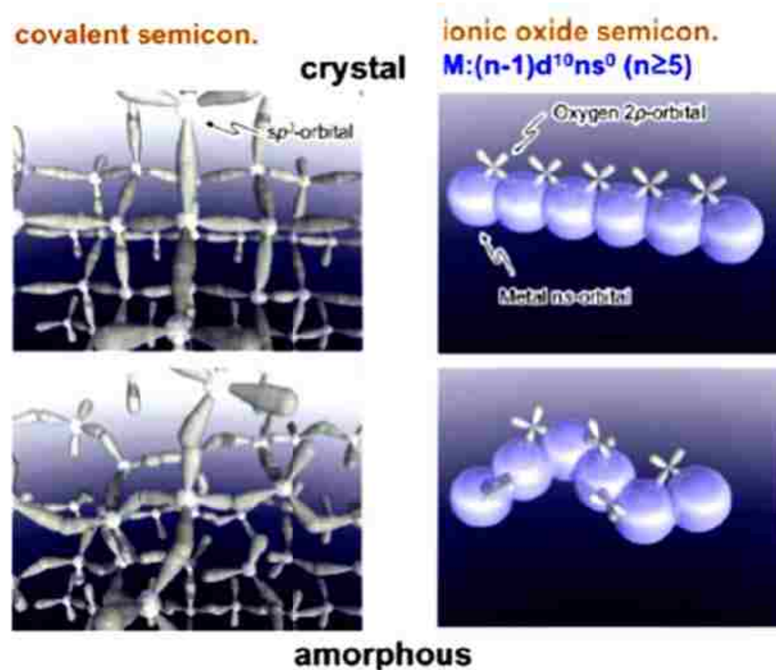

Figure 1.3 Orbital drawing of electron transport in conventional compound semiconductor and ionic oxide semiconductor [Adapted from Ref 1. 44]

Unlike ZnO, a-IGZO can have a uniform amorphous phase because multiple oxides (In_2O_3 & Ga_2O_3) are introduced to promote the glass phase formation [1.45] and the amorphous phase is thermally stable up to ~500°C [1.46]. Usually, amorphous semiconductors exhibit much deteriorated carrier transport properties than associated crystalline materials. This is because the chemical bonds in the covalent semiconductors are made of sp^3 orbitals with strong spatial directivity. As illustrated in Figure 1.3, in anamorphous oxide semiconductors (such as a-IGZO), electrons are conducting through metal ion's *ns* orbital. Since *ns* orbital is symmetrical, the conducting path and carrier mobility can still be preserved even in amorphous phase. To ensure a high mobility in amorphous phase, a sufficient *ns* orbital overlap between metal ions is necessary. To satisfy this requirement, Hosono *et al.* proposed a working hypothesis which predicts the metal ion should be heavy post transition metal cations with electronic configuration of $(n\text{-}l)d^{10}ns^0$, where $n \geq 4$ [1.7]. To have good TFT electrical properties, control of carrier concentration is premium and unlike in ZnO the incorporation of Ga^{3+} actually helps in suppressing the oxygen vacancies in a-IGZO thin-film since it has a stronger bonding to oxygen than Zn or In ions [1.46].

1.4 Amorphous Oxide Based TFTs for Active Matrix Displays

In displays, thin film transistors (TFTs) are used as switching components in the active-matrix over a large area. Currently, liquid crystal displays (LCDs) mostly use amorphous Si as the channel layer in TFTs; however, this material offers low mobility (<1 cm^2/Vs) and requires high process temperature (350ºC) [47], and as such a-Si:H

TFTs are not available for high resolution displays on cheap substrates. Organic TFTs have very low mobility (< 1 cm^2/Vs) and may have reliability concerns. Oxide-based TFTs have at least one order higher mobility (10~50 cm^2/Vs) [48] than a-Si:H TFTs and organic TFTs and can be deposited at room temperature. The high mobility of oxide-based TFTs, make them available for high resolution displays; this allows integrating switching TFTs in the active-matrix and driver-integrated circuits (driver ICs) on the same substrate, which can reduce cost and provide a more compact display. Furthermore, oxide-based TFTs have other advantages such as room temperature deposition, higher

Table 1.3 Comparison of Different TFT Technology for Displays

Technology	Mobility (cm^2/Vs)	Visible Light Transparency	Large Area Uniformity	Comments
a-Si:H	<1	Poor	Good (Gen-8)	Low mobility, limited current driving capability
Poly-Si	~100	Poor	Poor (Gen-4)	Additional crystallization process required
ZnO	20~50	Good	Poor	Strong tendency to form poly phase
a-IGZO	3~12	Good	Good (Gen-8)	Balance between mobility and uniformity

transparency, and minimum surface roughness. Table 1.3 gives a comparison of different TFT technologies for active matrix display based applications. The oxide-based TFTs have great potential to realize a roll-to-roll display. If this technology can be realized, it may not only replace the current a-S:H TFTs for LCDs, but will also create new applications such as transparent active electronics on glass, electronic books, light weight flexible displays that could eventually change the whole display industry.

1.5 Organization of the Dissertation

This dissertation focuses on design, fabrication and characterization of a-IGZO TFTs on mostly flexible thin metal substrates. A brief and succinct review of present status of amorphous oxide based materials is presented first. In chapter 2, the process tuning of RF-Sputtered a-IZO and a-IGZO thin films for TFTs and circuits is discussed with emphasis on device optimization. Low temperature processing of a-IGZO is compatible with plastic substrates but metal foils provide greater dimensional stability to fabricated small feature TFTs. Device (a-IGZO TFT based) fabrication and circuit integration on flexible metal foils is presented next with comprehensive electrical analyses to characterize a-IGZO TFTs on flexible substrate. Reliability of a–IGZO TFTs under DC electrical voltage and current bias stress at elevated temperatures are discussed in chapters 3 and 4. The electromechanical stability of a-IGZO TFTs on flexible metal foils is introduced in chapter 5. Various a-IGZO TFT based circuits are described with demonstration of an electrophoretic display in collaboration with the Flexible Display Center of Arizona State University in chapter 6. In an effort to dope ZnO with nitrogen, various techniques are employed and the results from TFT structures are detailed. Ab initio calculations based on rigid band theory confirms persistent n-type transport in these devices and are presented in chapter 7. Finally in the concluding chapter, a summary of the present work along with suggestions for future research is delineated.

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Chapter 2

Process Optimization Of Amorphous Oxide Thin Films and Electrical Characterization of a-IZO and a-IGZO TFTs On Metal Foils

2.1 Introduction

As we have noted in the introductory chapter, thin film transistors (TFTs) have significant technological importance in displays and other large-area electronic applications. Nevertheless, the range of applications possible from these TFTs have been somewhat limited by their overall poor performance on low cost substrates compared to conventional silicon MOSFETs. This poor performance can be characterized using several measures, including field-effect mobility, subthreshold slope, device hysteresis, and bias stress stability. More importantly, these parameters have implications towards the implementation of TFTs in real applications. Additionally, at a more fundamental

level, all of these parameters reveal important electrical characteristics of the semiconductor thin films, the interface between semiconductor and the dielectric layers and robustness of the device processing; therefore, by fabricating TFTs one provide useful measure of the electrical properties of new materials, which in turn can aid the development of real application demonstrations. Untill now, large area flexible systems are enabled by a-Si:H or organics which suffer from low mobilities that limit their use in driver electronics that require higher current drive. Amorphous oxide TFTs are an attractive alternative to traditional thin film silicon (Si) based devices since they offer several key advantages such as high mobilities, transparency in the visible spectrum and low processing temperature. As flexible substrate materials, metal foils like stainless steel and flexible plastics have been used with demonstration of high performance devices and systems [2.1,2.2]; however, in the case of plastic substrates shrinkage and elongation due to medium-to-high temperature processes as well as susceptibility to gas permeation are bottlenecks. Although the low process temperature of metal oxides is quite compatible with plastic substrates, we chose to fabricate such TFTs on thin metal foils instead, since they offer high mechanical strength, flexibility, light weight as well as greater dimensional stability which afford small geometry features of the devices and circuits.

In this chapter we will discuss the process optimization of amorphous metal oxide thin films for TFT fabrication on stainless steel metal foils first. Given that the main focus of this study is on the optimization of oxide semiconductor for application in TFTs and other large area electronic circuits, electrical characterization of standalone devices are discussed in details in the second half of this chapter.

2.2 Effect of Deposition Parameters in Amorphous Oxide Thin Films

2.2.1 Process Parameters Effect on Growth Rate of Oxide Thin Films

In order to optimize the electrical, structural and optical properties of the oxide thin films by RF sputtering, we varied oxygen partial pressure and RF power density. A comparative study is done on a-IZO films as well to elucidate the common aspects of optimizing these unique thin films. The targets were commercially available 6 inch diameter, dense IZO ceramic target (In_2O_3:ZnO %weight 90:10) and IGZO target (In_2O_3:Ga_2O_3:ZnO 1:1:1 molar ratio).The growth rate of sputtered films is highly dependent not only on the material composition but also on the deposition parameters. Furthermore, the growth rate can affect the properties of the sputtered thin films. It is known that for a given material certain deposition conditions leading to too high or too low growth rates can negatively affect the film's properties; under these extreme conditions the sputtered species can damage the growing film due to severe bombardment or reach the substrate without enough energy to create a compact film. Thus before going into electrical properties of amorphous oxide thin films, it is important to see how their growth rates are affected by deposition parameters and composition. The deposition of oxides by sputtering in a pure argon ambience (even if starting from a ceramic target) generally results in films with high oxygen deficiency. This is essentially related to the threshold energy required to sputter a particle, which is higher for a metal-oxide than that for a metal [2.3]. Additionally sputtered species from a target heading towards the substrate can be dissociated inside the plasma, increasing the chance of non-

stoichiometric film formation. For these reasons, a small percentage of oxygen, typically less than 10% is usually added in the argon atmosphere in order to have better control of the stoichiometry of the growing film. Fig 2.1 shows the effect of the increasing %O_2 on

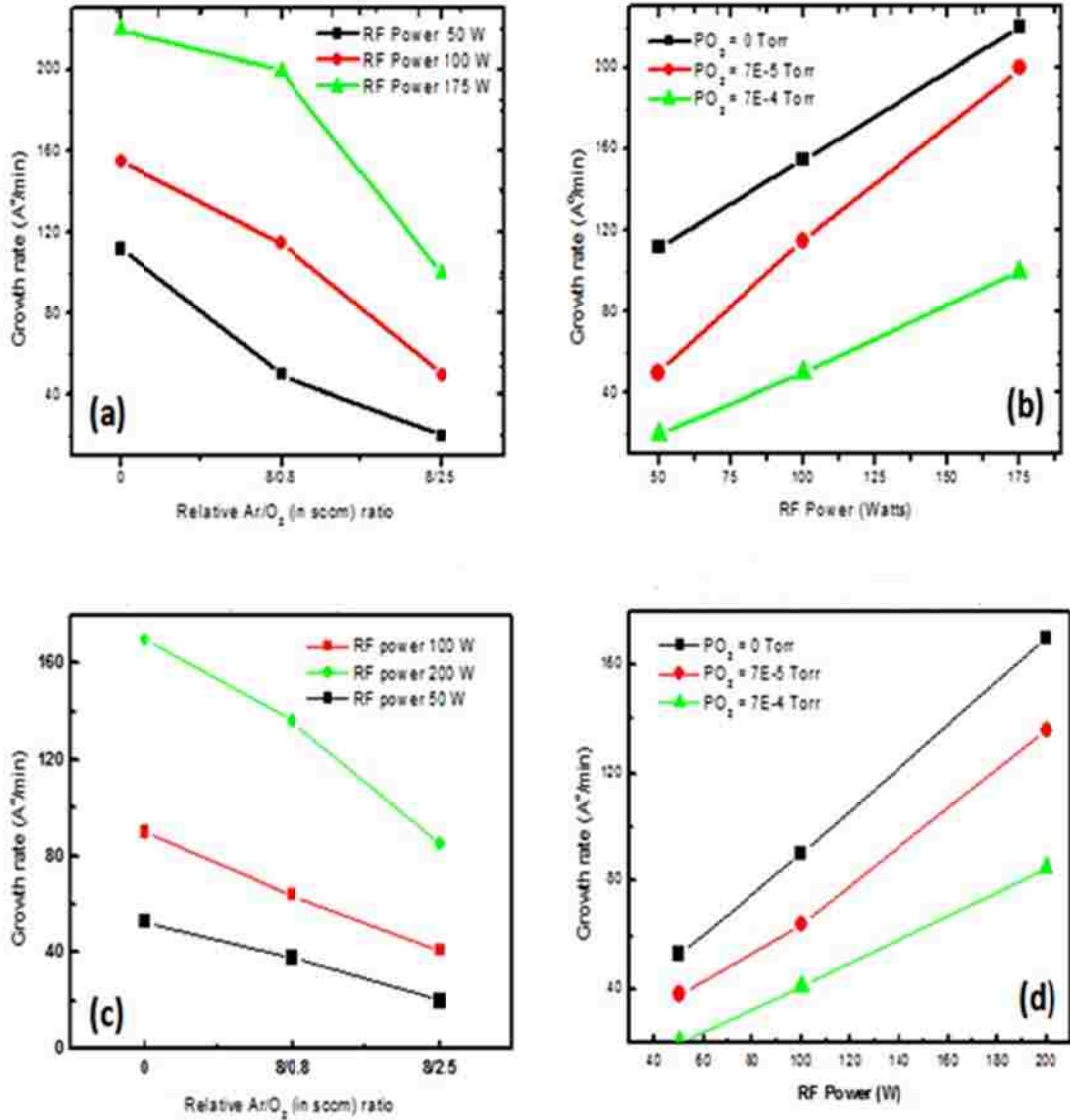

Figure 2.1 Dependence of growth rate of (a) & (b) IZO and (c) & (d) IGZO on %O2, $P_{deposition}$ and $P_{RF\text{-}Power}$. Flow rates in sccm (standard cubic centimeters per minute)

the growth rate, for film produced from targets with different compositions (IZO %wt 90/10 In_2O_3/ZnO) and IGZO (In_2O_3:Ga_2O_3:ZnO 1:1:1 molar ratio). Regardless of the composition, growth rate decreases as %O_2 increases which can be attributed to the following:

- Repsuttering of the growing film due to bombardment of highly energetic oxygen ions 2.[3]. This is especially relevant for depositions performed at higher %O_2.
- Change of surface conditions of the target [2.4]. For instance if a pure argon ambient is used, target surface will be less oxidized, favoring the sputtering of the cations rather than the ZnO aggregates. Additionally, the energy transfer from an Ar^+ incident ion to the sputtered target material is greatest when the mass of the ejected particle is closer to that of the ion, resulting in a greater sputtering rate in the absence of oxygen [2.5].
- For low %O_2, the oxidation reaction takes place essentially on the substrate, which is reflected in a small or even negligible decrease on the growth rate when compared to pure argon atmosphere. However, for higher %O_2, target oxidation starts to play an important role decreasing the growth rate.

The total deposition pressure of the sputter ambient, $P_{deposition}$, also affects the growth rate of the analyzed oxide thin films. In general, the growth rate decreases as the $P_{deposition}$ increase. This is related to the lower mean free path of sputtered species for higher $P_{deposition}$ due to their more intense scattering by gas atoms and molecules during their path from the target to the substrate. Also the sputtering power, $P_{RF\text{-}Power}$, directly affects

the discharge voltage, and it is expected that growth rate will increase for higher $P_{RF\text{-}Power}$, which can be verified by Fig 2.1 (b) and (d). For IGZO, sputtering with different $\%O_2$, an almost a linear relationship is found between growth rate and different $P_{RF\text{-}Power}$. For low $P_{RF\text{-}Power}$, the energy of the incident ions is not enough to have a large number of sputtered species arriving at the substrate surface. In this condition, the sputtered species are also prone to collisions on their path to the substrate surface leading to non-ideal film conditions and low $P_{RF\text{-}Power}$ processing condition was avoided for thin films used in TFTs.

Also noticeable from the graphs are the effects of target composition on the growth rate. With the same deposition conditions, IZO has a larger growth rate than that of IGZO. This can be related to the different mass (atomic number) and binding energy of the elements composing the ceramic targets [2.6]. The thin film growth rate decreases when compared to binary oxides like In_2O_3 and is typical of multicomponent oxides with higher concentrations of zinc and gallium [2.7]. Surface imaging with AFM reveal that the as-deposited IZO and IGZO films possess very smooth surface with minimal roughness (less than 5 nm). Even after annealing at 300ºC the films remain amorphous which is consistent with what is reported in other studies [2.6-2.8]. It has been shown that multicomponent oxides with higher number of elements (IGZO for example) are harder to crystallize, due to increased disorder in the structure. IZO has been known to crystallize at much higher temperatures (>500º C) and for higher In content in the films. The higher temperatures are irrelevant to this particular study since the goal was to investigate low-temperature oxide based electronics. The fact that these oxides present an amorphous structure which is stable for a broad range of compositions and anneal

temperatures is of major importance to the application of these films in TFT devices. The amorphous films present a smoother interface and can be deposited with better uniformity and reproducibility than their crystalline thin film counterparts.

2.2.2 Process Parameters Effects on Electrical Properties of IZO and IGZO Films

Apart from impurity doping, oxygen vacancies derived from stoichiometry deviations in the deposited films are the main contributors for electrical conduction in amorphous metal oxides. The conduction band in oxides is mainly made up of the unoccupied orbitals of the metal cation; therefore, the energy levels of oxygen vacancies (V_o), that is the non-bonding state of the metal cation, is formed in or near the conduction band minimum allowing the vacancies to act as a shallow donor but not as an effective electron trap. These oxygen vacancies are readily ionized near room temperature, with each doubly charged oxygen vacancy contributing two free electrons, preserving charge neutrality [2.9]. The variation of $\%O_2$ during sputtering is therefore one of the most effective ways to control the electrical properties of oxide semiconductors. Fig 2.2 and Fig 2.3 show the dependence of resistivity on P_{O2} and $\%O_2$ for a-IZO and a-IGZO films. The main trend is for resistivity, ρ (Ω-cm) to increase with P_{O2} ($\%O_2$). This is consistent with the idea of reduction of oxygen vacancies; the additional oxygen atoms supplied using a higher $\%O_2$ can be incorporated in the film, filling the high number of oxygen vacancies that are created when sputtered in a pure argon ambient. This is clearly visible for IZO films in Fig 2.2, where ρ variation is more than 6 orders of magnitude for $\%O_2$ variation from pure argon to 12.5%. The highest ρ variation occurs for $\%O_2$ varied

between 0-2% for IZO and %O_2>10% for IGZO. Although some oxygen vacancies may still be compensated above these values for a-IGZO, the increase in ρ between 2-12.5% can also be attributed to a different mechanism for high %O_2; the intense substrate bombardment by highly energetic oxygen ions can cause considerable resputtering of the

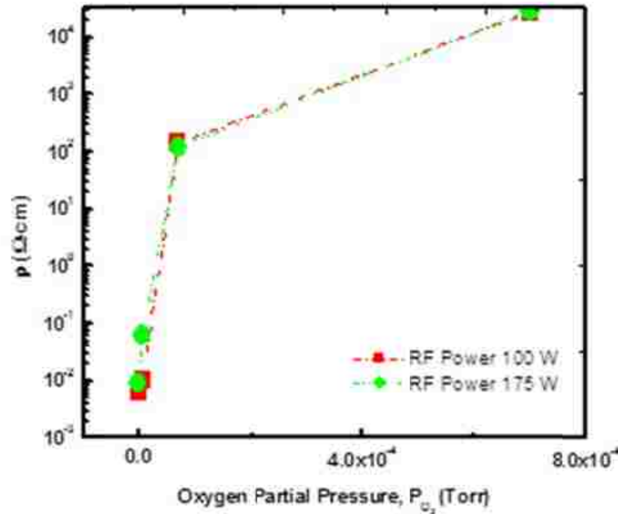

Figure 2.2 Dependence of ρ of a-IZO films with P_{O2} and $P_{RF\text{-}Power}$.

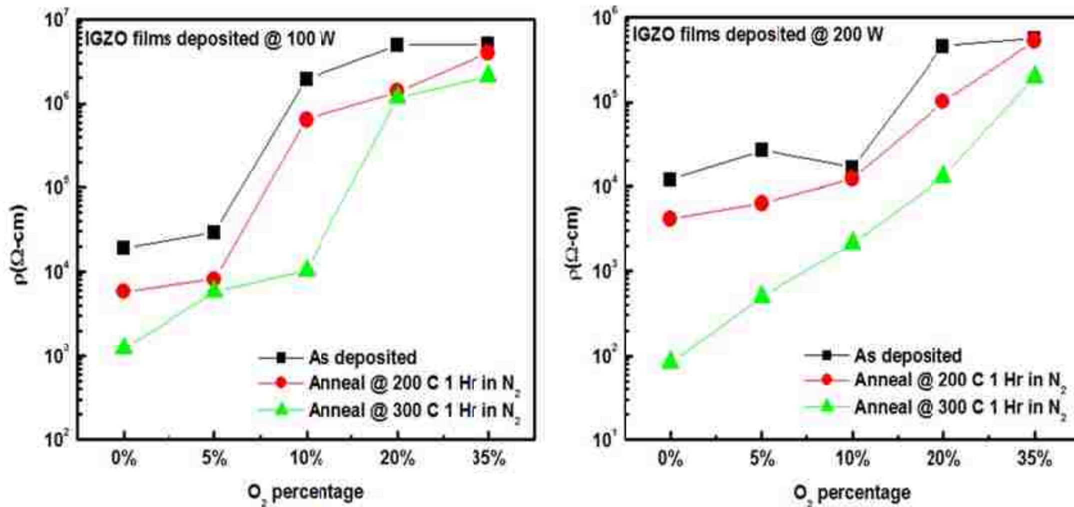

Figure 2.3 Dependence of ρ of a-IGZO films with %O_2, $P_{RF\text{-}Power}$ and annealing

deposited films, including structural defects on its growing surface, raising the film ρ. As we have noticed in the previous sub-section, since the growth rate decreases substantially for $\%O_2 > 10\%$, what is suspected is that the compactness of the film is also affected which might account for the increased ρ. For IGZO films, a lower RF power leads to a more resistive film. This can be tentatively attributed to less sputtering induced damage on IGZO films. The higher energy of the sputtered species arriving at the substrate surface allows them to increase the mobility of other particles present on the substrate by momentum transfer; this allows them to reach equilibrium sites within the film structure, forming a denser and defect free film with low ρ. In IGZO films, it is expected that the higher RF power leads to films with increased indium content, which may also contribute to a reduced ρ. An additional mechanism can be also at play here. With higher RF power, as more species are sputtered from the target and move in the plasma subjected to less scattering, more oxygen is needed to oxidize them when reaching the substrate and also to reoxidize the target surface, which easily gets reduced during the sputtering process. Chaing et al [2.10] reported higher carrier concentration for IGZO films deposited with higher RF power. Even though higher RF power generally leads to a highly conducting films, very high ρ can still be achieved under these conditions by using a high $\%O_2$. For the a-IGZO films deposited at a moderate 100 W of RF power, it is seen the ρ doesn't vary much for $\%O_2$ ~5% or less. This could be due to the fact that a better equilibrium between oxygen concentration in the film and the atmosphere exists from room temperature and higher and the film should also be structurally more stable [2.11]. Regarding the effect of annealing temperature on the ρ of the a-IGZO films, it is expected

that increased adsorption or desorption of oxygen is expected to happen as the annealing temperature goes up; however, we did all our annealing in an N_2 ambient and as such surface interaction with oxygen either via physisorption, chemisorptions or desorption can be ruled out for the observed decrease with anneal temperature. A more plausible explanation is that annealing in N_2 environment promotes structural rearrangement and reduces the internal stress effects of the films [2.12]. Annealing can also promote some degree of recrystallization of the as deposited oxide thin films, but the anneal temperature range used in this study is probably lower than the typical temperature ranges this process is reported to happen in these oxides.

A characteristic feature of amorphous oxide semiconductors is observed in the relationship between Hall mobility (μ_e) and carrier concentration (N_e) as seen in Fig 2.4. μ_e increases with increasing N_e for a-IGZO films and has been shown to follow the same.

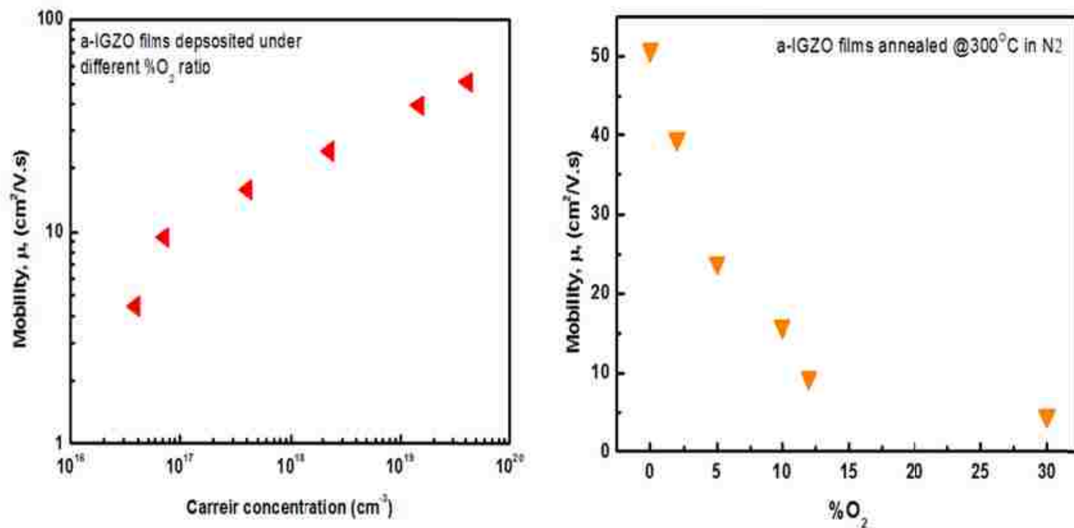

Figure 2.4 Dependence of Hall mobility of a-IGZO films with %O_2; all films were annealed at 300ºC in N_2 ambience.

trend in crystalline IGZO films [2.13]. This trend is opposite to those of simple crystalline semiconductors because μ_e of crystalline semiconductors usually decrease with increasing N_e due to enhanced impurity scattering effects.

For a-IGZO films annealed at 300ºC, a continuous increase of μ_e is verified with increasing N_e from $N_e \sim 10^{16}$ cm^{-3} onwards which means that most of the defects affecting the films with low N_e are eliminated. At $N_e > 10^{18}$ cm^{-3}, carrier mobility sharply increases with N_e, which is consistent with the existence of potential barriers associated with the random distribution of gallium and zinc atoms [2.13]. These barriers should have a relatively small height, as the conduction is essentially dominated by the large indium 5s spherical orbitals, which easily overlap even in a disordered structure, while the zinc and gallium cations assure that this structure does not crystallize and prevent excessive free carrier generation [2.13]. Although not shown here, at $N_e > 10^{20}$ cm^{-3}, ionized impurity scattering dominates charge transport, which gives rise to lower mobility. The optimum condition for IGZO deposition is at $P_{RF\text{-}Power}$ of 100 W, with 2-10% O_2 at a total chamber pressure of around 5mTorr.

2.3 Process Flow of Amorphous Oxide TFT Fabrication

The flexible metal foil substrates used in this research were stainless steel type 304 having a diameter of 150 mm and were 100-µm thick. The surface roughness of the stainless steel foil substrates has been a major issue for the fabrication of microelectronics. We have demonstrated that a surface roughness of 1 nm is achievable (Fig. 2.5). This can be achieved by sequentially polishing the foils with mechanical

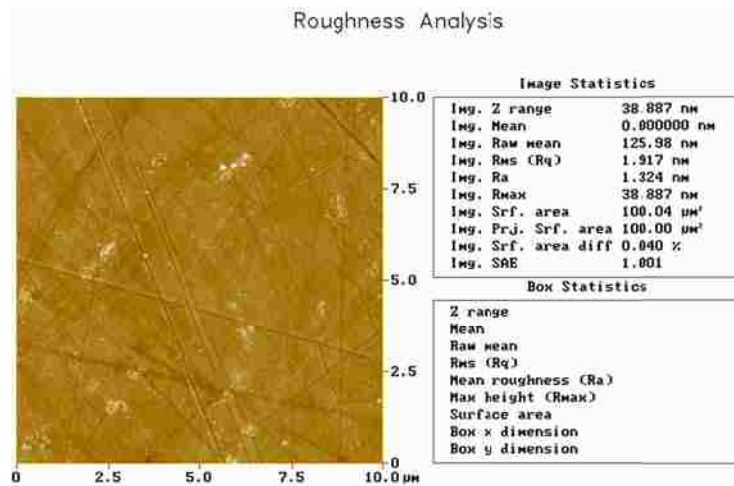

Figure 2.5 AFM image of polished stainless steel substrate

means followed by chemical-mechanical polishing. With that smooth surface, there is no requirement for an additional planarization layer. Chemical resistance of steel substrates allows standard RCA and Piranha based CMOS cleaning before the insulating layers are coated on top to electrically isolate the substrates from active device components. The thickness of this insulation is critical not only from the viewpoint of yield (i.e. avoid shorts through pinholes/particles to the conductive substrate), but also because it detrimentally affects circuit performance through parasitic capacitive coupling [2.14]. In our case, the metal foils were coated with a 3 µm thick silicon dioxide film deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300°C; the SiO_2 film was deposited in multiple steps with a cleaning step used after each deposition cycle. Each layer was 1µm thick and this approach was followed in order to reduce particles and eliminate pinholes that could compromise the integrity of the insulating layer. The SiO_2 film was deposited on both sides of the metal foil substrate for stress balance which

inevitably minimizes the warping of the metal foil caused by the thermal mismatch between the substrate and the insulator.

An important difference for many TFTs, including amorphous silicon and a-IGZO, compared to conventional silicon MOSFETS, is that a staggered structure is typically used. In staggered structures, the contacts are not on the same plane as the accumulation channel, but rather, on the opposite interface of the active layer. This is very different than conventional coplanar MOSFETs where buried wells form the contacts directly in contact with the inversion channel. The staggered structure has the potential for significant contact effects (since the current must travel through the entire active layer to reach the metallic contacts), particularly as a function of the active layer thickness. Typical structures designed for this dissertation is the bottom-gate inverted staggered structure TFT architecture (shown in Fig 2.6) with either exposed back channel or with a passivated back channel. Compared to widely used TFT technologies such as polysilicon and amorphous silicon, the main difference in the amorphous oxide TFTs is the lack of a heavily doped region between the contacts and the active layer. This heavily doped region is the most common way to form ohmic contacts to semiconductors by sufficiently thinning the contact barrier so that carriers can freely tunnel. In amorphous oxide TFTs, metal contacts rather than doped contacts are commonly used primarily due to process simplification. Most importantly, metals such as Mo and Al form relatively good contacts as deposited with a relatively low specific contact resistivity. This can be further reduced by using plasma treatments before contact metallization to create a high carrier

concentration interface [2.15]. As a result, for a variety of applications, such as AMOLED, these contacts appear sufficient and are very simple to form.

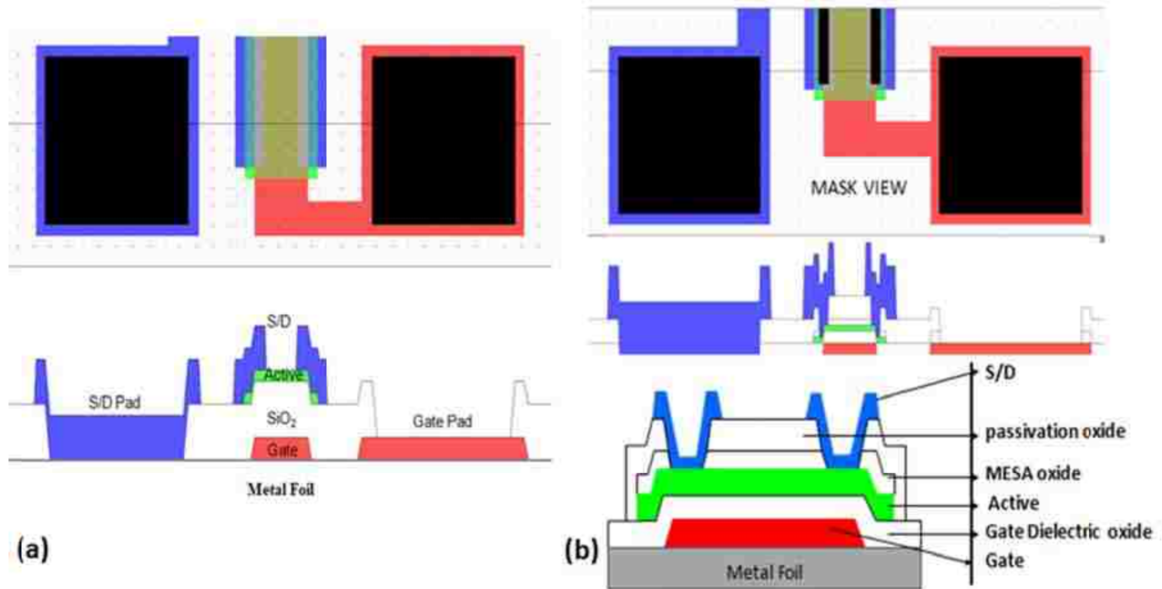

Figure 2.6 Device Schematic of unpassivated and back-channel passivated amorphous Oxide TFTs.

For the unpassivated staggered bottom gate TFT structure, the TFTs are fabricated by first depositing 150 nm of Mo by RF sputtering onto SiO_2 passivated 6 inch Steel wafers and lithographically patterning and wet etching to form the gate layer. A 100 nm thick SiO_2 was then deposited by PECVD at 300°C with breakdown field exceeding 8MV/cm. Then a 50 nm of a-IGZO thin film is deposited by RF sputtering from a 6-inch diameter commercially available IGZO target (1:1:1 molar ratio of In_2O_3:Ga_2O_3:ZnO). Sputtering is carried out at a RF power density of 1 W/cm^2 at a chamber pressure of 5 mTorr. The optimized a-IGZO active layer is patterned by wet etching in dilute HCl (40:1 in DI water). Contact openings to the gate pads are accomplished by lithography and selective

etching of the oxide layer. Mo source and drain metallization is done by RF sputtering and subsequent lift-off. An N_2O plasma treatment is done on the back channel post fabrication in a PECVD chamber at room temperature.

For the back channel passivated structure, a blanket 50 nm of IGZO was deposited followed by a 50 nm of low temperature SiO_2 film (mesa oxide) by RF sputtering right after the dielectric layer deposition. The optimized IGZO/SiO_2 stack was patterned by combination of dry (CF_4) and wet etching (dilute HCl). A thicker (70 nm) sputter deposited passivation oxide capped off the patterned layers to protect the active channel region. Contact openings to access the pads were accomplished by lithography and selective etching of the oxide layer. Subsequently, opening of source/drain electrodes were done by dry etch. In order to reduce etch damage and improve contact resistance, the patterned S/D areas were treated in Ar plasma. Finally, Mo source and drain metallization was done by RF sputtering and subsequent lift-off. Completed devices underwent 1 hr anneal at 300°C in N_2 ambient before testing could proceed.

2.3.1 Low Temperature N_2O Plasma Passivation Scheme: Clues from a-IZO TFT

The low temperature N_2O plasma treatment to improve a-IGZO TFT characteristics and device stability (discussed in chapter 3 and 4) originated from our earlier work on a-IZO TFTs [2.52]. The a-IZO TFTs had bottom gate staggered structure with the back channel non-passivated. The active layer (40 nm of a-IZO) and source drain layers (150 nm IZO) were sputter deposited at RF power densities of 1 and 2 W/cm^2 and with relative Ar/O_2 flow ratios of 10 and 50 respectively. ITO gate was also

sputter deposited at 1 W/cm^2 with no oxygen flow. The a-IZO TFTs were subjected to post-fabrication anneal in N_2 at 350°C for 30 minutes followed by a low temperature (125°C) N_2O plasma treatment in a PECVD chamber for 5 minutes.

Figure 2.7 shows the transfer characteristics of a-IZO TFTs with and without the post-fabrication N_2O treatment with device dimensions of W/L = 64 μm/16 μm at a drain bias of 1 V. The a-IZO TFTs have on/off current ratio around 10^5 for N_2O passivated case and around 10^6 for non-N_2O treated case. In the saturation mode, the field effect

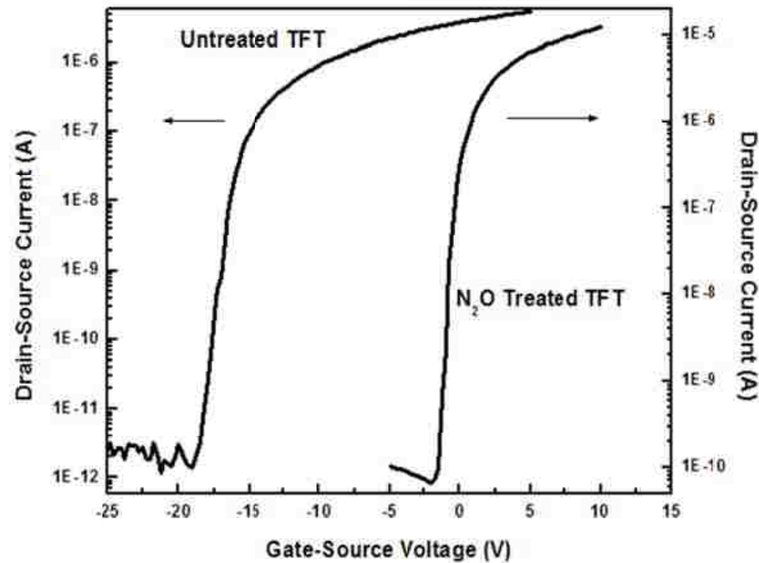

Figure 2.7: Effect of N_2O plasma treatment on IZO TFTs; Transfer characteristics of a-IZO TFTs (W=64μm, L=16 μm) with and without N_2O plasma treatment at V_{DS}=1V.

mobility calculated was 12cm^2/V.s and 25cm^2/V.s for N_2O treated and non-treated case respectively. The non-N_2O treated TFTs are depletion-mode devices (threshold voltage, V_T~-12V) which means even at zero gate bias there is significant source-drain current. For applications in display devices it is highly desirable to obtain enhancement-mode

devices. The post-fabrication N_2O plasma treatment results in enhancement-mode a-IZO TFTs (V_T~1.3V). The idea is that nitrogen species in the plasma can reduce the sensitivity of relative O_2/Ar ratio to carrier concentration. Nitrogen is also known to act as an acceptor in ZnO system and can annihilate shallow donor (mostly oxygen vacancies) levels. In Figure 2.7, it is easily seen that we can get enhancement mode TFTs by this

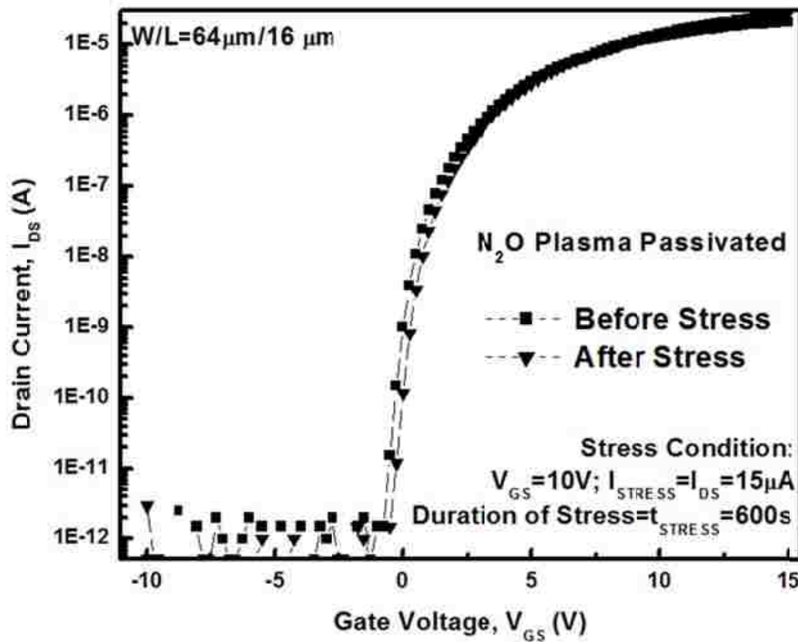

Figure 2.8 Constant current stress effects on N_2O plasma treated IZO TFTs; Transfer characteristics of a-IZO TFTs (W=64µm, L=16 µm) at V_{DS}=1V before and after 15µA current stress for 600 s with V_{GS}=10V for the duration of stress.

simple plasma treatment. The resulting TFTs had steeper gate voltage swing of about 0.3 V/decade (compared to 0.46V/decade for non-N_2O treated TFT) with On/Off current ratio going down slightly. Although this may be due to some plasma induced damage but the same treatment also improves device reliability and thus outweighs the drawbacks. The low values obtained for the gate voltage swing indicates the existence of a low

density of surface states at the semiconductor-insulator interface after the N_2O plasma passivation. The beneficial effects of N_2O plasma passivation become evident when a-IZO TFTs are bias stressed to assess stability of the devices. In Fig 2.8, the transfer characteristics of a-IZO TFTs (W=64μm, L=16 μm) are shown before and after a constant current stress of 15μA for 600s. The gate voltage during the constant current stress period was held at V_{GS}=10V. The shift in threshold voltage, ΔV_T is small (less than 1 V). For all the a-IGZO TFT device fabrication discussed in greater detail throughout this chapter and in the subsequent chapters, this post deposition N_2O treatment was adopted and shown to have significant effects in terms of device operation and reliability.

2.4 Electrical Characterization of a-IGZO TFTs on Steel Foil

Electrical characterization of n-channel a-IGZO TFTs on flexible substrates can help us understand the device performance and can provide valuable information to improve the device fabrication process. In this section we present the electrical characterization of a-IGZO TFT on steel foil fabricated from optimized thin films. The TFTs had the staggered bottom gate architecture as in Fig 2.6 with back channel passivation unless otherwise stated.

2.4.1 Basic I-V Characteristics of a-IGZO TFTs On Steel Foil

a-IGZO transfer (I_{DS}-V_{GS}) and output (I_{DS}-V_{DS}) characteristics were measured in ambient conditions in a light tight probe station. The electrical properties were measured

by a HP4145 parameter analyzer automated by LabView software. The transfer characteristics of a-IGZO TFT extracted at V_{DS}=0.1V is shown in Fig 2.9. We extracted the threshold voltage (V_T) and field effect mobility (μ_{FE}) based on the standard MOSFET equation in the linear region (with $V_{DS} \ll V_{GS}-V_T$,):

$$I_{DS} = \mu_{FE} C_{ox} \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right] \cong \mu_{FE} C_{ox} \frac{W}{L}[(V_{GS} - V_T)V_{DS}] \qquad (2\text{-}1)$$

where C_{ox} is the gate insulator capacitance per unit area (F/cm^2), μ_{FE} is the field effect mobility (cm^2/V.s), W and L are TFT channel width and length, respectively. The extraction method of V_T and μ_{FE} will be discussed in the subsequent sections in details. From linear extrapolation method used, V_T is 1.25V and μ_{FE} ($\mu_{FE} = \frac{g_m}{C_{ox}\frac{W}{L}V_{DS}}$) derived from the maximum transconductance ($g_m = \partial I_{DS}/\partial V_{GS}$) is 14.22cm^2/V.s. Compared to a-Si:H TFTs, the μ_{FE} is an order of magnitude higher and is consistent with the unique metal ion's *ns* orbital conduction in a-IGZO. The subthreshold slope is given by:

$$SS = \left(\frac{\partial log(I_{DS})}{\partial V_{GS}}\right)^{-1} \qquad (2\text{-}2)$$

The calculated subthreshold slope is 390 mV/decade and is comparable to the state of the art a-Si:H TFTs. This ensures a fast TT response and also reduces voltage of the gate driving signal. The TFT off-state current (I_{OFF}) is seen to be in the 10^{-10} A range and does not increase with increasing negative gate voltage.

The output characteristics of the a-IGZO TFT under various gate to source voltages (V_{GS}) ranging from 4-20V are shown in Figure 2.10(a). During each measurement, the drain to source voltage (V_{DS}) was varied from 0-20V. A very clear distinction between linear and saturation region is obtained. This suggests that less than

20V of drain voltage (V_{DS}) is adequate for operating a-IGZO TFTs in an active-matrix configuration. A good ohmic

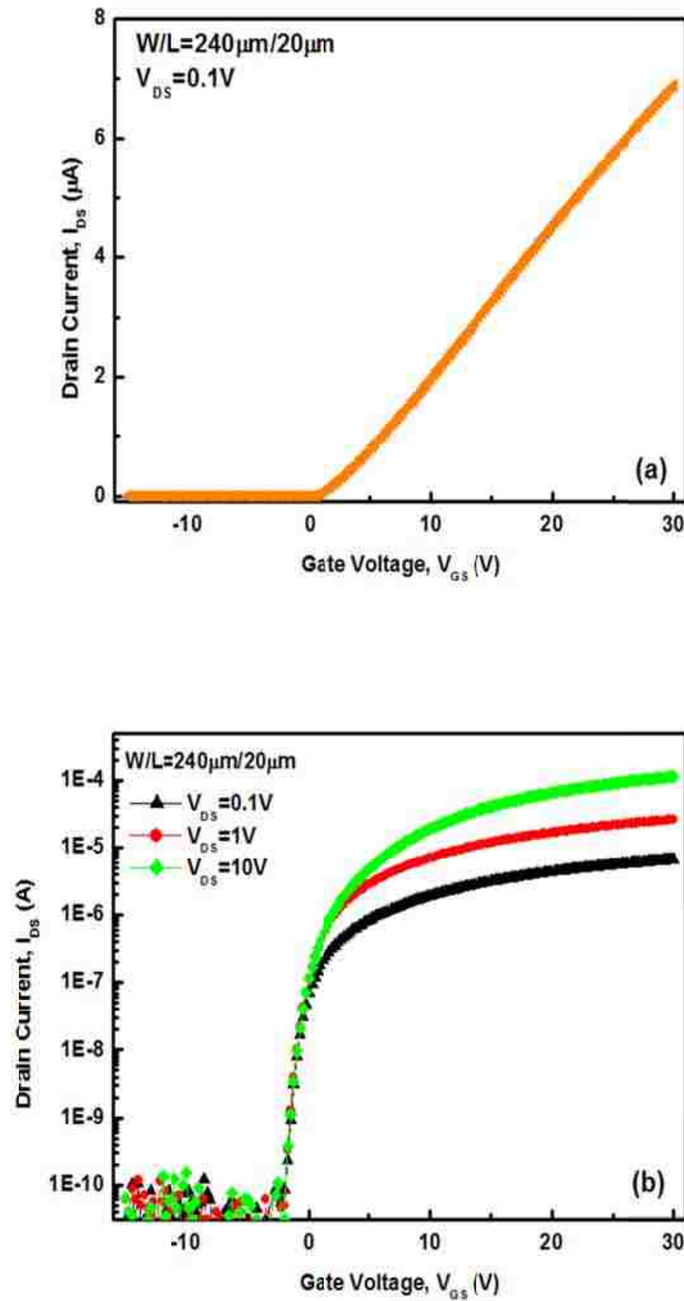

Figure 2.9 Transfer characteristics of a-IGZO TFTs (W=240μm, L=20 μm) on stainless steel at V_{DS}=0.1V (a) linear plot (b) semi-log plot.

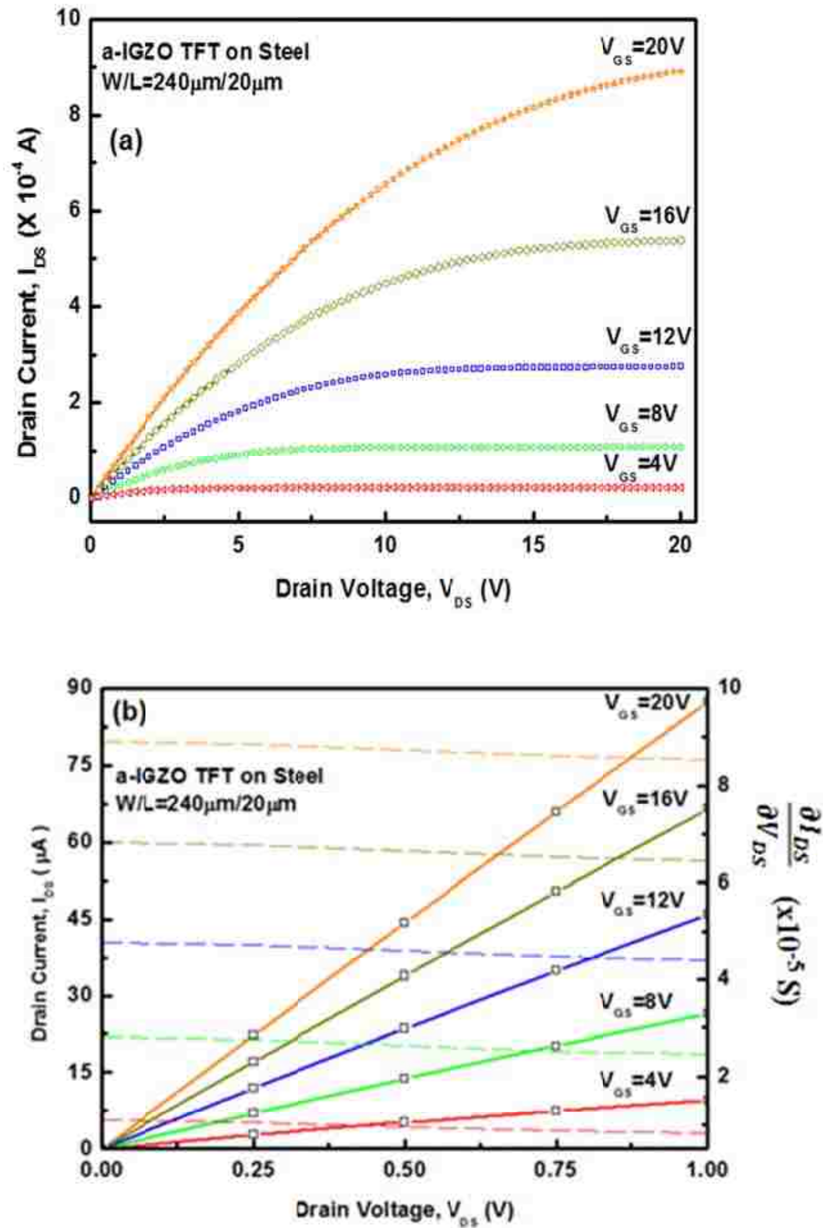

Figure 2.10 Output characteristics of a-IGZO TFTs (W=240μm, L=20 μm) on stainless steel at (a) different V_{GS} values. (b) A zoom-in plot of output characteristics near V_{DS}~0V.

source/drain contact is another important aspect for TFT evaluation. A non-ohmic contact, bulk-limited contact and high bulk density-of-states (DOS) can all manifest in TFTs to exhibit a non-linear drain current behavior called "current crowding", at low V_{DS} [2.16].

Figure 2.8(b) shows the output characteristics near the origin (V_D ~0V) and there is no current crowding observed in the fabricated a-IGZO TFTs. The absence of current crowding can be better appreciated by plotting the derivative of the output curves ($\delta I_{DS}/\delta V_{DS}$) which is also shown in Figure 2.10(b). These properties are highly desirable for a-IGZO TFT to be used in active-matrix arrays.

2.4.2 Threshold Voltage Extraction

2.4.2.1 Linear Extrapolation Method

In this method V_T is determined by extrapolating a line tangential to the I_{DS}-V_{GS} characteristics of n-channel a-IGZO TFTs at the point of maximum transconductance. The intercept of this line with the V_{GS} axis yields V_T. This method is commonly used for bulk Si and SOI based MOSFETs because of its simplicity. An example of applying this method to determine V_T is shown in Fig 2.11. The V_T extracted is 1.8V.

2.4.2.2 Transconductance Change Method

For device modeling and simulation, it is essential to know the band-bending (surface potential) of at least one gate bias from which the band-bending at all gate biases can be calculated. In this method, the gate voltage at which the derivative of the low drain voltage transconductance ($\delta I_{DS}/\delta V_{GS}$) is a maximum, relates to the threshold band-bending. The extrapolated V_T using this method is relatively insensitive to series resistance and their interface trap density near the band edge [2.17]. Fig 2.12 shows

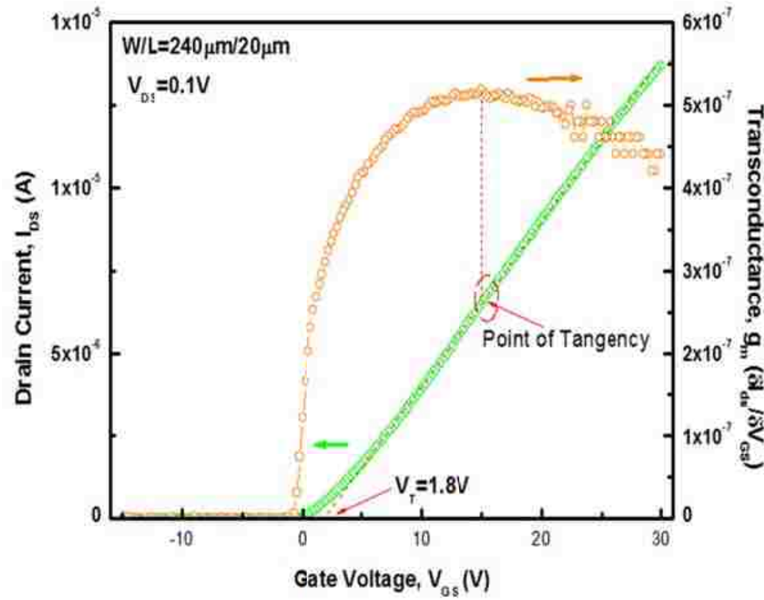

Figure 2.11 Linear extrapolation method of extracting V_T of a-IGZO TFTs (W=240μm, L=20 μm) on stainless steel.

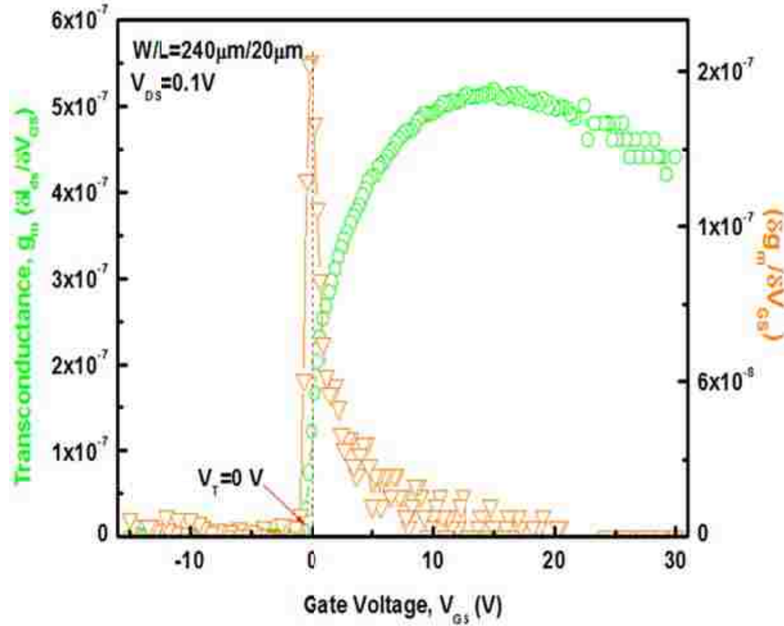

Figure 2.12 Transconductance change ($\delta g_m/\delta V_{GS}$) method of extracting V_T of a-IGZO TFTs (W=240μm, L=20 μm) on stainless steel

implementation of this method to determine V_T. The extracted V_T is 0V. Clearly the linear extrapolation method overestimates V_T. In the linear method the μ_{FE} is assumed to be constant whereas in actual a-IGZO TFTs μ_{FE} has V_{GS} dependence which is discussed later. For this study, the transconductance change method was used prevalently to determine V_T.

2.4.2.3 Turn On Voltage

For devices deviating from the ideal square law model [2.18], some researchers have proposed using an analogous figure-of-merit, denoted the turn-on voltage, V_{on}. The gate voltage at the onset of conduction (distinguished by a sharp increase from a threshold current level) establishes V_{on} [2.18]. V_{on} is attractive for several reasons: ambiguous model fitting (i.e. extrapolation) is not required, V_{on} identifies the lower range of device operation, and as shown in Fig. 2.13, V_{on} is independent of drain voltage (as long as V_{DS} > a few kT/q). In practice, anomalous subthreshold current characteristics, possibly due to a displacement or gate leakage current, are sometimes seen for low V_{DS}; therefore $V_{DS} > 5$ V is typically used when determining V_{on}. The disadvantage of this method is that changes in subthreshold slope directly interact with this voltage. Particularly for device where non-ideal humps in the drain current and large subthreshold swing are observed, V_{on} varies by a lot.

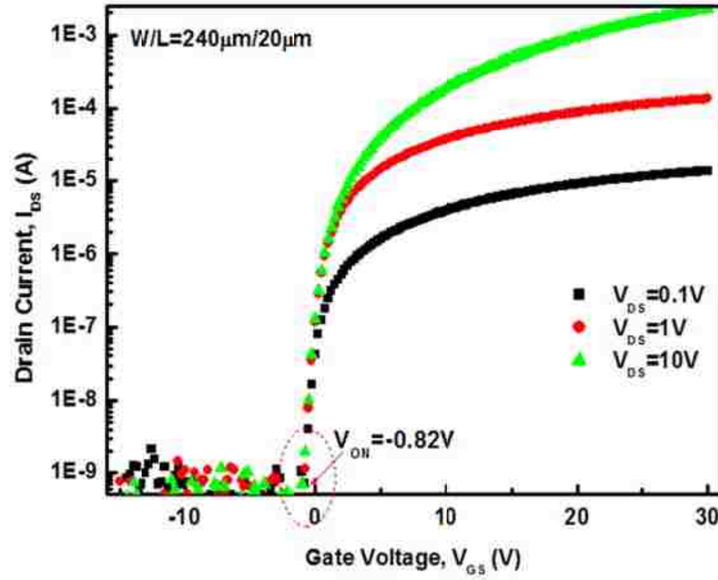

Figure 2.13 Turn on voltage, V_{on} extraction of a-IGZO TFTs (W=240µm, L=20 µm).

2.4.3 Mobility in a-IGZO TFTs

The mobility of the field-effect device is the average mobility of the channel carriers that results from taking into account all applicable scattering mechanisms including phonon, ionized impurity and interface roughness. From the well known Matthiessen's rule, the following expression for mobility is found:

$$\frac{1}{\mu_e} = \frac{1}{\mu_O} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \tag{2-3}$$

where μ_e is the electron mobility, μ_O is the semiconductor bulk mobility, μ_{SR} is the surface roughness mobility and μ_C is the coulomb scattering mobility. As the channel mobility quantifies the current drive capability and maximum switching frequency of a TFT, accurate extraction is vital. Similar to V_T estimation, there are multiple ways to

extract the channel mobility, all resulting in slightly different values. Additionally, the gate leakage current is typically not accounted for, and can affect the extracted values.

2.4.3.1 Mobility Extraction: μ_{eff}, μ_{FE}, and μ_{sat}

The effective mobility, μ_{eff}, and the field-effect mobility, μ_{FE}, are both determined from classic MOSFET based drain current expressions with assessment of the linear regime of operation (the so-called below pinch-off region); while the saturation mobility, μ_{sat}, is established from the saturation region (above pinch-off). The below pinch-off drain current relationship can be described and approximated as, [2.19]

$$I_{DS} = \mu \frac{W}{L} Q_n V_{DS} - \mu W \frac{kT}{q} \frac{dQ_n}{dx} \tag{2-4}$$

$$I_{DS} \approx \mu \frac{W}{L} Q_n V_{DS} \tag{2-5}$$

where Q_n is the mobile channel charge density, W is the gate width, and L is the gate length of the TFT and the direction x is into the cahnnel. To directly determine Q_n, a measurement of the gate-to-channel capacitance as a function of gate voltage is required. Alternatively, it is often useful to obtain a first order approximation of Q_n from electrostatics,

$$Q_n = C_{ox}(V_{GS} - V_T). \tag{2-6}$$

The approximation shown in (2-6) is obtained by assuming a uniform channel charge density. When biasing at low V_{DS} (~50-100 mV), this assumption is reasonable and allows the second term of (2-4), which is related to carrier diffusion, to be neglected; however, neglecting this diffusion-related term does introduce some error in mobility determination.

For a MOSFET operating in the subthreshold regime ($V_{GS} < V_T$) and near the threshold voltage, a significant diffusion current flows and the approximation in (2-5) deteriorates. Thus, mobility assessment in these regions results in significant error; however, at gate voltages appreciably larger than V_T this error is minimized [2.19]. Differentiating (2-5) with respect to V_{DS} or V_{GS} determines the channel conductance (g_d), or transconductance, (g_m), respectively. The channel conductance and transconductance are related as follows,

$$g_d = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_{V_{GS=Constant}} \quad (2\text{-}7)$$

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS=Constant}} \quad (2\text{-}8)$$

The effective mobility or field-effect mobility is then determined by

$$\mu_{eff} = \frac{g_d}{\frac{W}{L}C_{ox}(V_{GS}-V_T)} \quad (2\text{-}9)$$

$$\mu_{FE} = \frac{g_m}{\frac{W}{L}C_{ox}V_{DS}} \quad (2\text{-}10)$$

It is worth noting that determination of μ_{eff} requires a value for V_T, in contrast to μ_{FE}, which is not explicitly dependent on V_T. The channel mobility is sometimes estimated from the above pinch-off drain current; mobility estimates from this region of device operation are denoted as, μ_{sat} . One method of extracting μ_{SAT} is to have the TFT biased in a diode connected fashion where the drain is tied to the gate and measure I_{DSAT} . This biasing configuration is only applicable if the device under test is an enhancement-mode ($V_T > 0$). Square law theory asserts that the above pinch-off drain current is given by,

$$I_{DSAT} = \mu_{SAT} C_{ox} \frac{W}{2L}(V_{GS} - V_T)^2 \quad (2\text{-}11)$$

μ_{SAT} is extracted using

$$\mu_{SAT} = \left(\frac{d\sqrt{I_{DSAT}}}{dV_{GS}} \sqrt{\frac{1}{C_{ox}\frac{W}{2L}}} \right)^2 \tag{2-12}$$

The above methodology alleviates the need to evaluate V_T and reveals that μ_{sat} is determined from the slope of the $\sqrt{I_{DSAT}}$ vs. V_{GS} characteristic. M_{SAT} is an inaccurate assessment of the "channel" mobility, as it is an average of the mobility in the channel and the mobility in the pinched-off region of the channel. It becomes useful to determine μ_{sat} when the gate leakage current significantly affects the below pinch-off current characteristics. The μ_{eff} , μ_{FE}, can be thought of as average and incremental mobility values. A non-linear I_{DS}-V_{GS} typical of TFTs translates to V_{GS} dependent apparent mobility values. Throughout this work, μ_{FE} is used since there is less ambiguity in its determination due to the fact that a value of V_T is not required. Figure 2.14 shows exemplary $\mu - V_{GS}$ characteristics of a-IGZO TFTs for the three mobility estimation techniques (μ_{eff}, μ_{FE}, and μ_{SAT}) discussed in this section. μ_{eff} and μ_{FE} is determined using V_{DS} = 100 mV. μ_{SAT} is calculated using (2-12) with $V_{DS} > V_{GS} - V_T$. It should be noted that the μ_{eff} characteristic shows an anomalously large value near V_T, which is due to the singularity present in (2-9) when $V_{GS} = V_T$. Considering the μ_{FE} characteristic in Fig. 2.14, the mobility initially increases with increasing gate voltage, peaks at a certain V_{GS} and then decreases. The initial increase may be due to an increasing ratio of free to trapped charge with increasing gate voltage. At lower gate voltages, the mobility is possibly trap-limited. [2.19]. The decrease at higher V_{GS} may be caused by several effects. At higher V_{GS}, carriers are drawn closer to the oxide-semiconductor interface and the mobility

degrades due to enhanced Coulombic scattering, which arises from interface states, and interface roughness scattering [2.19] The mobility decrease may also be due in part to increasing contact resistance effects with increasing gate voltage.

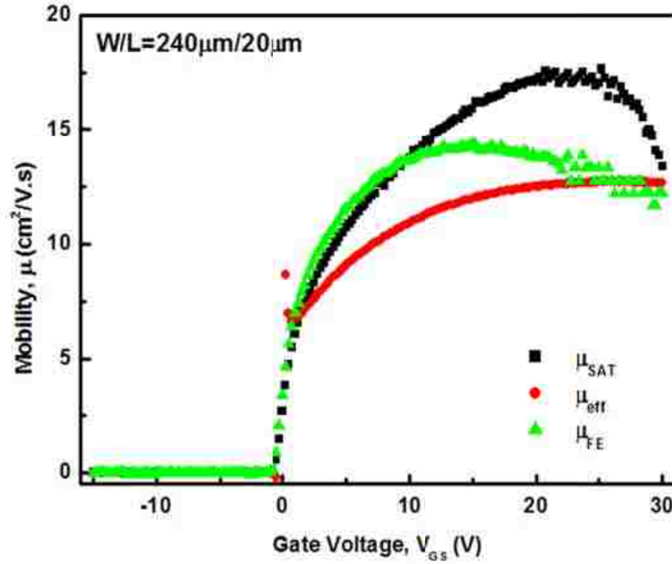

Figure 2.14 μ-V_{GS} characteristics of a-IGZO TFTs (W=240μm, L=20 μm); μ_{eff} and μ_{FE} are determined with V_{DS}=100mV while V_{DS}=30V for determining μ_{sat}.

2.4.3.2 V_{GS} Dependence of Mobility

The V_{GS} dependent mobility, $\mu_{FE}(V_{GS})$ as shown in Fig 2.14 stems from a non-linear I_{DS}-V_{GS} behavior observed at the higher V_{GS}. This necessitates defining I_{DS} (2-1) with the V_{GS} dependent field-effect mobility ($V_{DS} \ll V_{GS}-V_T$):

$$I_{DS} \cong \mu_{FE}(V_{GS}) C_{ox} \frac{W}{L} [(V_{GS} - V_T) V_{DS}] \tag{2-13}$$

The extracted μ_{FE} is proportional to the V_{GS} and reaches a peak value of 14.75 $cm^2/V.s$ and decreases at higher V_{GS}. Such behavior has also been seen in other oxide semiconductor TFTs [2.20]. It is believed that a portion of the induced channel charges

are trapped in band tail states (or deep states) and cannot contribute to the I_{DS}. To explain $\mu_{FE}(V_{GS})$ in disordered material devices like a-Si:H TFTs, Shur et al. [2.21] showed that μ_{FE} the can be expressed as the free carrier mobility, μ_n scaled by the ratio of the free charge density to the induced carrier density:

$$\mu_{FE}(V_{GS}) = \mu_n \frac{Q_{Free}}{Q_{Induced}} = \mu_n \frac{Q_{Free}}{(Q_{Free}+Q_{Trapped})} \quad (2\text{-}14)$$

where μ_n is the electron band mobility. In MOSFETs, Q_{Free}~$Q_{Induced}$. However, in typical a-Si:H and disordered materials like a-IGZO, μ_{FE} is expected to be much lower than μ_n due to the high density of traps. Since charge components $Q_{Trapped}$ represent the charge over the thickness, μ_{FE} is representative of the modulation of device conductance including the geometry, the semiconductor and the dielectric layers and the channel charge profile. Shur et al also show a power law dependence of μ_{FE} on V_{GS}:

$$\mu_{FE}(V_{GS}) = \mu_n \left(\frac{V_{GS}-V_T}{V_{AA}}\right)^{\alpha} \quad (2\text{-}15)$$

where V_{AA} is a material dependent parameter and α is the power coefficient which describes the dependence of $\mu_{FE}(V_{GS})$ on effective gate voltage (V_{GS}-V_T). For the ease of parameter extraction, (2-15) is further simplified as:

$$\mu_{FE}(V_{GS}) = K(V_{GS} - V_T)^{\alpha} \quad (2\text{-}16)$$

where K becomes a material dependent parameter. It should be noticed that the K has the unit of $cm^2/V^{\alpha+1}.s$. The I_{DS} by accounting for $\mu_{FE}(V_{GS})$ can be written as:

$$I_{DS} \cong KC_{ox}\frac{W}{L}(V_{GS} - V_T)^{\gamma}V_{DS} \quad (2\text{-}17)$$

Where γ=α+1. Using this approach, V_T and K values can be obtained (Fig 2.15 (a) and(b)). A similar method has also been used to extract the threshold voltage of a-Si:H

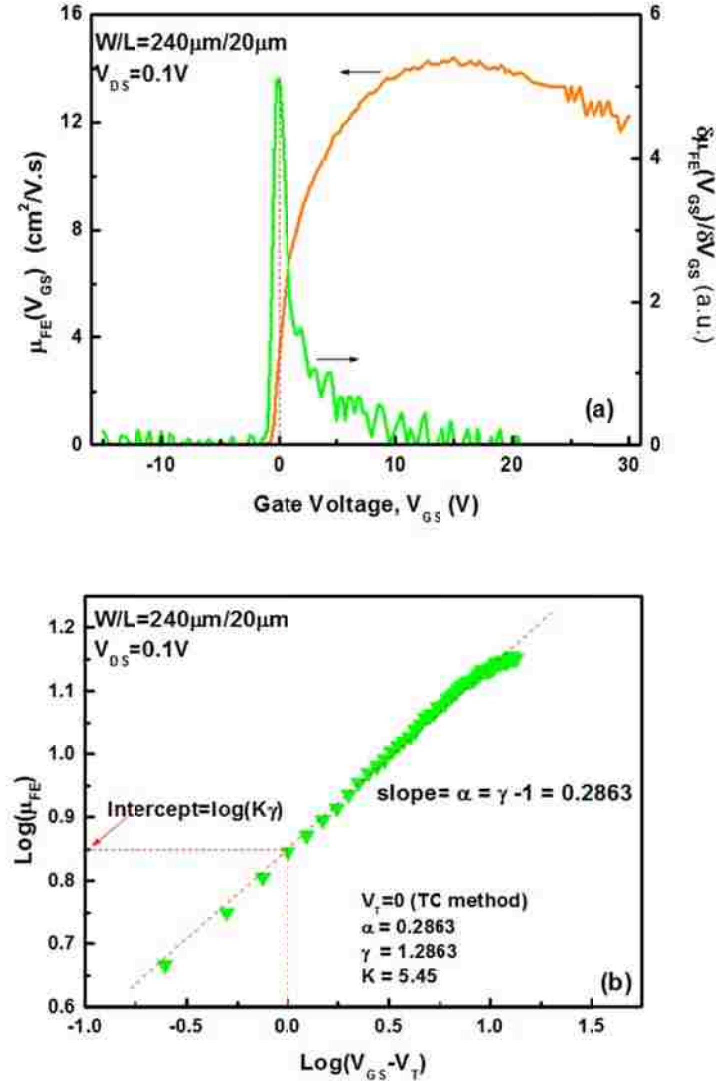

Figure 2.15 (a)μ_{FE}-V_{GS} characteristics of a-IGZO TFTs (W=240μm, L=20 μm); (b) log-log plot of μ_{FE} vs. (V_{GS}-V_T)

TFTs [2.22]. The V_T is first defined as the V_{GS} value at which maximum $\partial\mu_{FE}/\partial V_{GS}$ occurs (V_T =0V: same as determined from the transconductance change, TC method) . Such phenomenon is fundamentally due to the difference in a-IGZO deep gap and band tail density of- states (DOS) properties. The γ-1 and K are extracted from the linear fit of the log(μ_{FE})-log(V_{GS} - V_T) :

$$\log(\mu_{FE}) = \log(K\gamma) + (\gamma - 1)\log(V_{GS} - V_T) \quad (2\text{-}18)$$

The extracted $\gamma = \alpha+1$ for our RF sputter a-IGZO TFT is similar to values reported for RF-puttered IGZO TFTs [2.23]. Kishida et al. [2.24] showed that the movement of TFT surface band bending with gate voltage changes when the electrons are trapped in the band-tail states and the γ can be expressed as [24]:

$$\gamma = 2\left(\frac{T_G}{T}\right) - 1 \quad (2\text{-}19)$$

where T is the measurement temperature and T_G is the characteristic temperature of the amorphous semiconductor density-of-states (DOS) distribution around the position of the Fermi level. The equation is valid for $T < T_G$. For a-Si:H, T_G commonly represents the characteristic temperature of the conduction-band-tail-states and a high density of such states causes the non-ideal condition of $\gamma > 1$. If we assume that the same idea holds true for a-IGZO TFTs, we can extract the T_G for our a-IGZO TFT to be around 343ºK (or kT_G ~29 meV). One possible origin of the conduction-band-tail-state in a-IGZO is the variation of In-O-metal bond angles [2.25].

2.5 Interface Trap Characterization of a-IGZO TFTs

The subthreshold slope technique was first proposed by R.J. Van Overstraeten [2.26] to determine the interface trap density of MOS devices. This method is readily applicable to long channel devices and at low drain bias. The current in the subthreshold region can be written as

$$I_{DS} = I_O exp\left(\frac{qV_{GS}}{nkT}\right)\left[1 - exp\left(-\frac{qmV_{DS}}{nkT}\right)\right] = I_{DS(Max)}\left[1 - exp\left(-\frac{qmV_{DS}}{nkT}\right)\right] \quad (2\text{-}20)$$

where

$$n = 1 + \frac{C_d + C_{it}}{C_{ox}} \tag{2-21}$$

$$m = 1 + \frac{C_d}{C_{ox}} \tag{2-22}$$

where C_{ox} is the oxide capacitance, C_d is the depletion capacitance, C_{it} is the interface trap capacitance and I_{DSMax} is the maximum drain current in the subthreshold region for a given V_{GS}. The transfer characteristic of a-IGZO TFT (W=240μm, L=20 μm) at low V_{DS} is plotted in Fig 2.16.

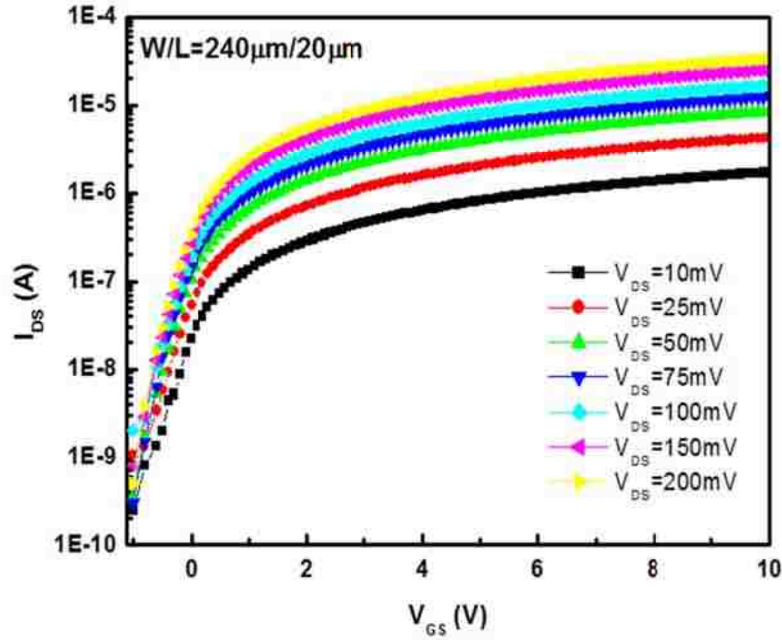

Figure 2.16 Transfer characteristics of a-IGZO TFTs (W=240μm, L=20 μm) at various low V_{DS}.

The extraction procedure for interface trap density, D_{it}, requires the determination of parameters 'm' and 'n'. We can proceed by determining 'm/n'. This can be done by plotting $\log(1-I_{DS}/I_{DSMax})^{-1}$ vs. V_{DS} for various V_{GS} (Fig 2.17), where I_{DSMax} is the drain

current corresponding to V_{DS}=200mV for each applied gate bias. The slope of this curve yields the ratio m/n:

$$\frac{m}{n} = 2.3\frac{kT}{q}\left(\frac{\partial \log\left(1-\frac{I_{DS}}{I_{DSMax}}\right)^{-1}}{\partial V_{DS}}\right) \tag{2-23}$$

The parameter 'n' can be obtained from the measured I_{DS}-V_{GS} curve at V_{DS}=200mV. The slopes of the curves vary with V_{GS} and the corresponding values of 'n' can be obtained by

$$n = \frac{q}{2.3kT}\left(\frac{\partial \log I_{DS}}{\partial V_{GS}}\right)^{-1} \tag{2-24}$$

The n value is related to the experimentally determined subthreshold values as:

$$SS = \left(\frac{\partial \log I_{DS}}{\partial V_{GS}}\right)^{-1} = 2.3n\frac{kT}{q} \tag{2-25}$$

Combining (2-24) and (2-25) we can determine the parameter 'm' by:

$$m = 2.3\frac{kT}{q}n\left(\frac{\partial \log\left(1-\frac{I_{DS}}{I_{DSMax}}\right)^{-1}}{\partial V_{DS}}\right) \tag{2-26}$$

With values of 'm' and 'n' know, the interface trap density, D_{it} is given by

$$D_{it} = \frac{C_{it}}{q} = \frac{C_{ox}}{q}(n-m) \tag{2-27}$$

The extracted D_{it} as a function of V_{GS} is shown in Fig 2.18. It can be shown that D_{it} follows an exponential band-tail distribution by correlating V_{GS} to different trap energies.

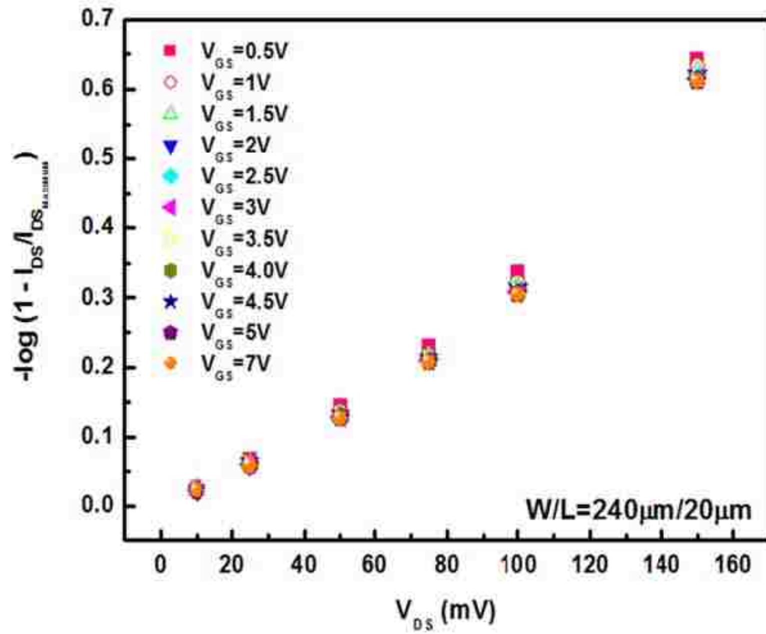

Figure 2.17 Extraction of m/n ratio of a-IGZO TFTs (W=240μm, L=20 μm) at various low V_{GS}.

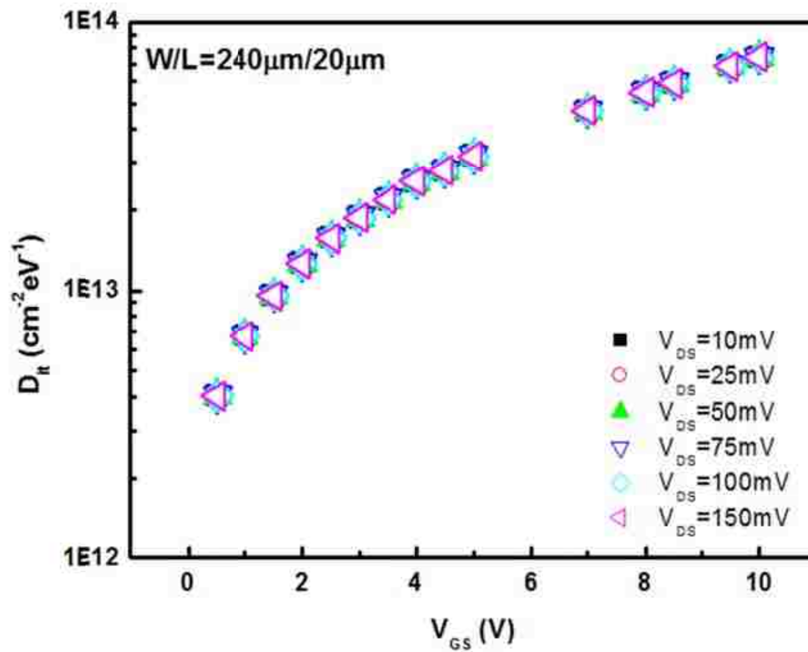

Figure 2.18 Extracted D_{it} of a-IGZO TFTs (W=240μm, L=20 μm) as a function of V_{GS}.

2.6 Contact Resistance of a-IGZO TFTs

The complete analysis of a-IGZO TFT electrical performance has to include the extraction of TFT source and drain series resistance and the intrinsic field effect mobility that can be degraded due to parasitic source/drain resistances. The intrinsic a-IGZO TFT parameters are representative of the electrical characteristics of the conduction channel itself without the effect of parasitic series resistance. The origin of the series resistance may be just non-negligible contact resistance at the metal/semiconductor interface; however, in the inverted staggered geometry pursued in this work, since the carriers need to traverse the length of the bulk semiconductor from the accumulation channel, this resistance includes the parasitic source resistance, R_S, the channel resistance, r_{ch}, and also the parasitic drain resistance, R_D. The parasitic resistances are often referred to as the contact resistance. The voltage applied across the source and drain of a transistor, terminals S and D in Fig. 2.19, may differ from the voltage dropped across S' and D' if parasitic resistances are large. When R_S and R_D are large, a higher applied bias is needed across the source and drain to inject carriers into the device, resulting in apparent lower reported mobilities.

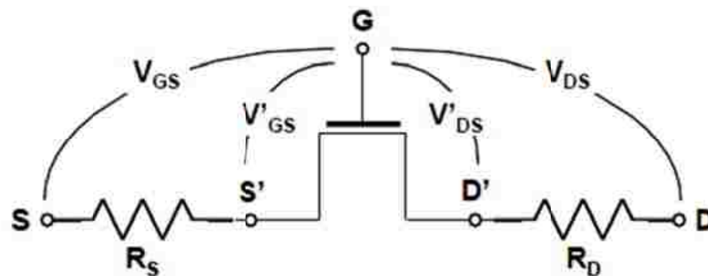

Figure 2.19 Schematic of an intrinsic transistor with lumped parameter representation of source and drain resistance.

2.6.1 Contact Resistance Estimation from TFT Structures

There are many experimental techniques for determining contact resistance. Contact resistance can be determined by using a variety of structures such as a two-terminal structure, a multiple-terminal structure including the transfer line method (TLM) test structure, Kelvin test structures, pn-junctions, Schottky barrier diodes, solar cells, bipolar junction transistors, and MOSFETs [2.27]. For a MOSFET test structure, physical device parameters such as channel width, channel length, and source/gate and drain/gate overlap distance can be varied to observe how these parameters affect contact resistance. Various analytical techniques have been proposed for extracting contact resistance from a MOSFET test structure. At low drain bias, the drain current of semi-insulating MOSFET can be written as [2.19]:

$$I_{DS} = \frac{\beta_{eff}[V_{GS}-V_T-V_{DS}/2]V_{DS}}{1+[\theta_S+\beta_{eff}R_{SD}].\left[V_{GS}-V_T+2\lambda_n\sqrt{2\phi_F}-\frac{V_{DS}}{2}\right]-2\beta_{eff}R_{SD}\lambda_n\sqrt{2\phi_F}} \tag{2-28}$$

For the inverted staggered a-IGZO TFT geometry, (2-28) reduces to

$$I_{DS} = \frac{\beta_{eff}[V_{GS}-V_T-V_{DS}/2]V_{DS}}{1+[\theta_S+\beta_{eff}R_{SD}].\left[V_{GS}-V_T-\frac{V_{DS}}{2}\right]} \tag{2-29}$$

where we can define

$$\beta_{eff} = \mu_i\left(\frac{W}{L_M-\Delta L}\right)C_{ox} \tag{2-30}$$

here, μ_i is the intrinsic electron mobility, L_M is the drawn mask channel length, ΔL is the reduced mask length due to processing, θ_S is the surface roughness parameter and R_{SD} is

the combined series resistance of source and drain terminals. By arranging the drain current expression we get:

$$R_M = \frac{V_{DS}}{I_{DS}} = \frac{1+\theta_S\left[V_{GS}-V_T-\frac{V_{DS}}{2}\right]}{\mu_i C_{ox}\cdot\left[V_{GS}-V_T-\frac{V_{DS}}{2}\right]}\left(\frac{L_M-\Delta L}{W}\right) + R_{SD} \tag{2-31}$$

We can plot R_M vs. L_M/W (shown in Fig 2.18) based on the transfer characteristics of TFTs with different LM. The slope of curve gives

$$a = \frac{1+\theta_S\left[V_{GS}-V_T-\frac{V_{DS}}{2}\right]}{\mu_i C_{ox}\cdot\left[V_{GS}-V_T-\frac{V_{DS}}{2}\right]} \tag{2-32}$$

From Fig 2.20, the crossing point of different V_{GS} curves gives the value of ΔL=0.17μm and R_{SD}=1.62kΩ. The relatively low R_{SD} value indicates that Mo can form good ohmic contact to a-IGZO. In a-Si:H TFTs, for example can be as high as 10^6 Ω [2.28]. If we plot the slopes from Fig 2.20, denoted "a" vs. $1/(V_{GS} - V_T - \frac{V_{DS}}{2})$, we can extract θ_S and μ_i. The extracted values are 0.019V^{-1} (θ_S is quite low for the mobility degradation) and 9.14 $cm^2/V.s$ (with R_{SD}=1.62k Ω it is around 5.13 $cm^2/V.s$ for this set of measurements) respectively (shown in Fig 2.21).

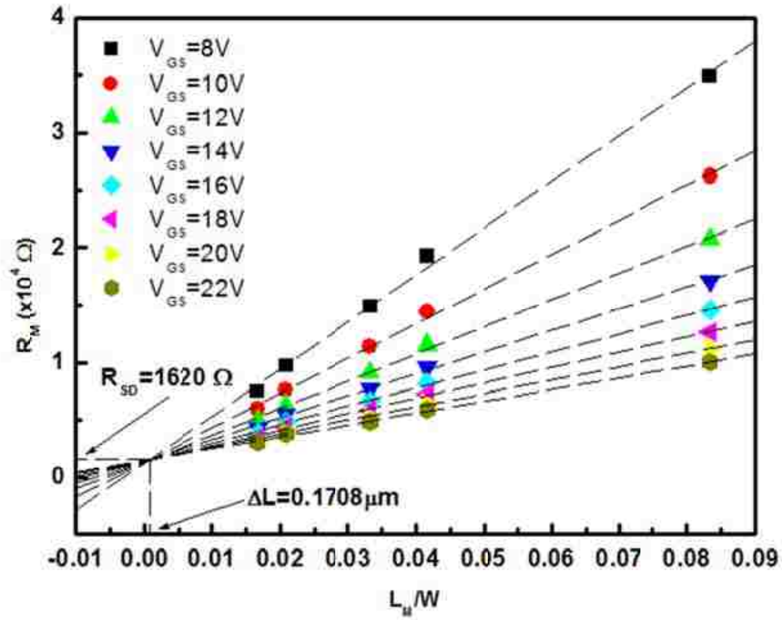

Figure 2.20 Plot of R_M vs. L_M/W at different V_{GS} of a-IGZO TFT

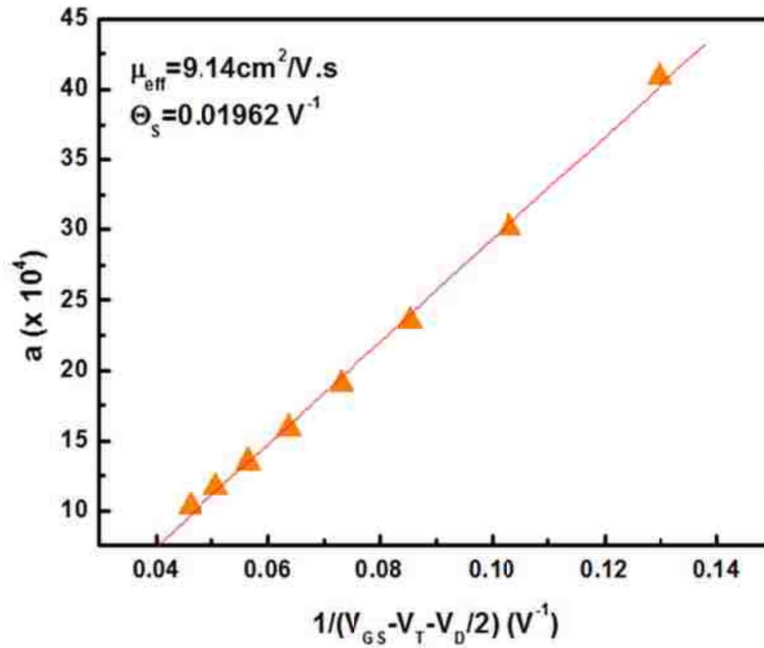

Figure 2.21 Plot of ‘a” vs. $1/(V_{GS} - V_T - \frac{V_{DS}}{2})$ to determine θ_S and $\mu_i$of a-IGZO TFT

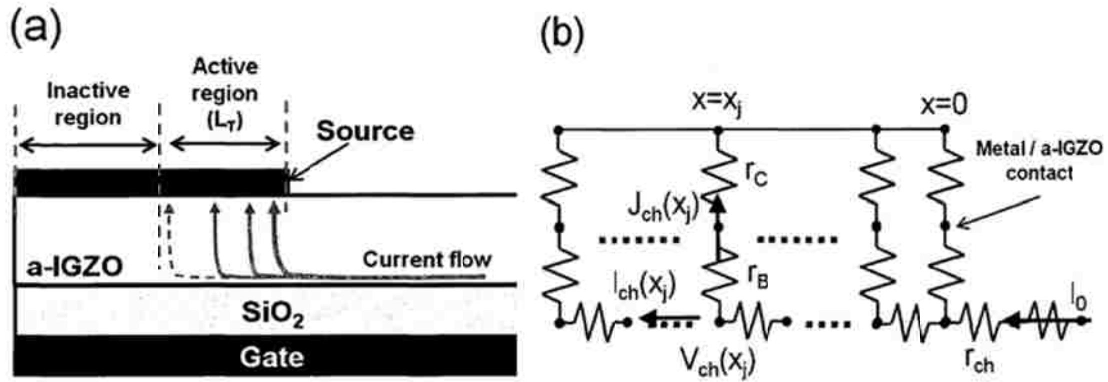

Figure 2.22 (a) Representation of transfer length, L_T and (b) equivalent circuit near the source electrode as a distributed resistive network to model current distribution (Adapted from Reference 2.28).

2.6.2 V_{GS} Dependent Contact Resistance

Implicit in the discussion in the previous section was the assumption that R_{SD} is V_{GS} independent. However, this assumption is in fact not accurate because the bulk a-IGZO resistivity is controlled by the V_{GS}. Therefore we need to carefully ascertain the effect of V_{GS} on channel resistance (r_{ch}) and R_{SD}. TFT series resistances are closely related to the overlap between source (drain) contact and gate contact. The TFT drain current does not usually flow through the whole source or drain contact but is more likely limited to a specific area of the contact [2.28]. Figure 2.22 illustrates the cross section and simplified schematic circuit diagram [2.28] at the source contact of a- IGZO. This process is closely related to the bulk a-IGZO resistivity. The length (transfer length, L_T) required for current to transfer from channel to S/D electrodes should decrease with

increasing V_{GS}. The total TFT on-resistance (R_T) should be re-written as the sum of R_{SD} and r_{ch} with length L ($\neq L_M - \Delta L$; L_M is drawn mask length):

$$R_T = \frac{V_{DS}}{I_{DS}} = r_{ch}L + 2R_{SD} \qquad (2\text{-}33)$$

where r_{ch} can be expressed as simply as $r_{ch} = \frac{1}{\mu_i C_{ox} W(V_{GS}-V_T)}$. Figure 2.22(b) shows the distributed circuit model used to derive the mathematical formula for analysis. This methodology was developed by Kanicki et al [2.28] for a-Si:H TFTs. The change of the horizontal channel current (I_{ch}) at position x under source electrode can be expressed as

$$\frac{\partial I_{ch}}{\partial x} = -WJ_{ch}(x) \qquad (2\text{-}34)$$

with

$$J_{ch}(x) = -\frac{V_{ch}(x)}{r_{Ceff}} \qquad (2\text{-}35)$$

and

$$r_{Ceff} = r_B + r_C \qquad (2\text{-}36)$$

In the above equations, W is the channel width; $J_{ch}(x)$ is the vertical current density at position x; $V_{ch}(x)$ is the voltage in the channel at position x; r_{ceff} is the effective contact resistance and r_B and r_C are the vertical bulk and contact resistivity respectively. From the mathematical formulations of the above equations Kanicki et al showed that r_{Ceff} can be expressed as:

$$r_{Ceff} = \frac{WR_{SD}{}^2}{r_{ch}} \qquad (2\text{-}37)$$

$$L_T = \frac{R_{SD}}{r_{ch}} \qquad (2\text{-}38)$$

The extracted r_{ch} vs. V_{GS} is plotted in Fig 2.23. The L_T is between 0.3μm-1.35μm and r_{Ceff} is calculated to be between 2^{-3}-8^{-3} Ω-cm^2.

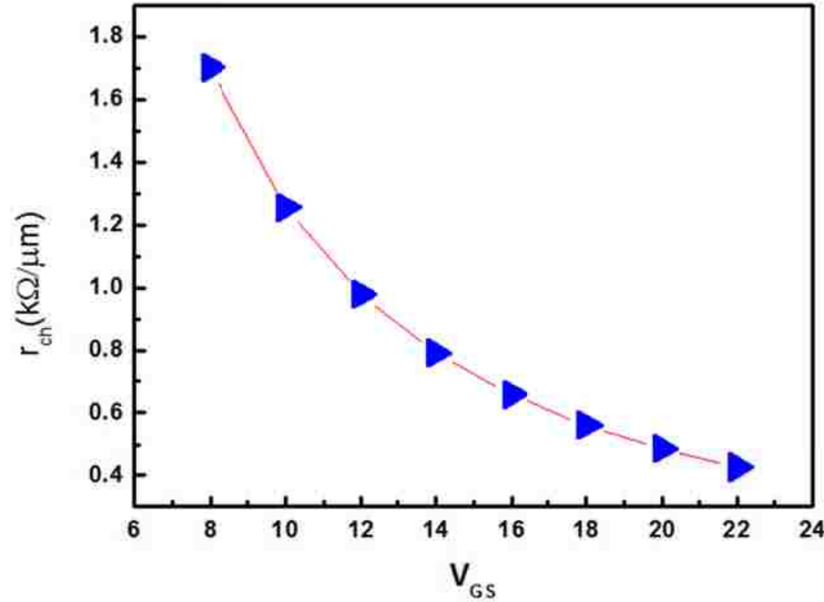

Figure 2.23 Plot of r_{ch} vs. V_{GS} of a-IGZO TFT

2.7 High Frequency C-V Characteristic of a-IGZO TFTs

The understanding of capacitance-voltage (C-V) characteristics is indispensable for the design of circuits and systems and can provide valuable information about the operation of the device. Also layout dependence of the C-V curve is important. In a series of C–V measurements, the ac impedance between the source and gate was measured for various frequencies and gate biases for a-IGZO TFT on steel. For negative biases applied to the gate, a-IGZO is depleted, and the capacitance is the series combination of just that

of the source pad with the insulator and semiconductor. As a positive gate bias is applied to the gate, an accumulation layer in the channel forms electrically connecting the source to the drain and surrounding channel regions. In addition, the charge can move from the source contact through the thickness of the a-IGZO to the dielectric/semiconductor interface. Both of these factors increase the capacitance, provided that the measurement frequency is slow compared to the R–C time constant for charge to pass through the contact resistance to the channel and along the channel. The series capacitance as a function of gate bias and frequency is shown in Fig. 2.24. The transition from depletion with no ac current-spreading from the source to full spreading occurs within a few volts; thus, the transition from depletion to accumulation also occurs within a few volts. This rapid transition indicates that the interface is of very good quality and that further improvement of TFT switching is possible with improvement of the contact resistance.

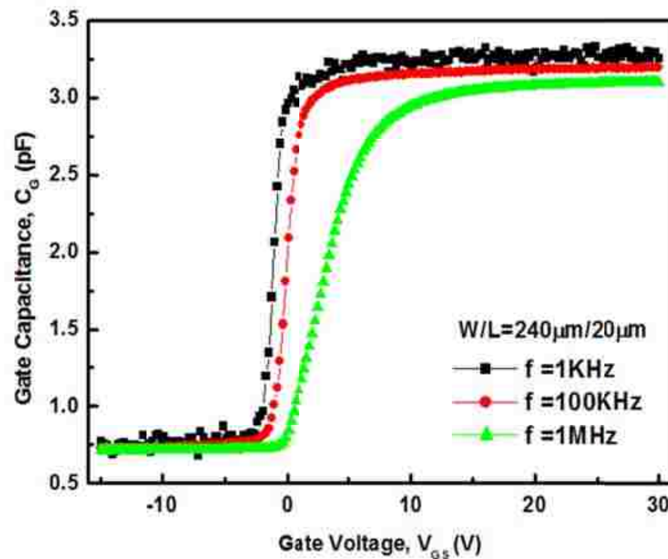

Figure 2.24 Frequency dependent C-V of a-IGZO TFT (W=240 µm, L=20µm).

2.7.1 Layout Dependent C-V Characteristic of a-IGZO TFTs

Layout dependent C-V analysis was done following a methodology described in [2.29].The different parameters are defined as follows: the overlap width of the region between gate and a-IGZO active layer (W_{IGZO}), the length of the region between S/D and a-IGZO active layer (L_{IGZO}), and the length of overlap region between gate and S/D (L_{OV}). W_{IGZO} =6 μm, L_{IGZO} =12 μm, and L_{OV} =6 μm in the devices that are measured. The width of the TFT, W (W= 240, 160, 80 and 40 μm, for L = 20 μm) and length of the TFT L (L= 20,10,8 and 5 μm, for W = 240 μm) dependence of the C-V characteristic of a-IGZO TFT is shown in Fig 2.25 measured at a frequency of 1MHz. It is obvious that C_{MAX} is dependent both on W and L while C_{MIN} is dependent on the width W. Based on experimental C-V results, Lee et al. specifies layout dependent C-V model in the following manner:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}};\quad C_{IGZO} = \frac{\varepsilon_{IGZO}}{t_{IGZO}};\ C_{OV} = \frac{C_{ox}C_{IGZO}}{C_{ox}+C_{IGZO}} \tag{2-39}$$

$$C_{MAX} = C_{ox}W_{eff-GC}L_{eff-GC}; \tag{2-40}$$

$$W_{eff-GC} = W + 2(W_{IGZO} + W_O);\ \ l_{eff-GC} = L + 2(L_{OV} + L_o) \tag{2-41}$$

$$C_{MIN} = C_{OV}2W_{eff-OV}L_{eff-OV}; \tag{2-42}$$

$$W_{eff-OV} = W + 2(W_1);\ \ l_{eff-OV} = (L_{OV} + L_1) \tag{2-43}$$

Where W_{eff-GC} and $L_{eff-GC}$are the effective channel width and length whileW_{eff-OV} and l_{eff-OV} are defined as the effective overlap width; $W_O$and $L_o$are characteristics width and length related the fringing capacitances between gate and active channel, $W_1$and L_1

and are related to the fringing overlap capacitance between gate and S/D. Model parameters from the experimental characterization are extracted to be W_O = 7.14μm, L_O = 3.06 μm, W_1 = 8 μm, and L_1 = 2.4 μm. Equivalent capacitance model for the a-IGZO TFT (shown in Fig 2.24) can be described

$$C_G(V_G) = C_T(V_G) W_{eff-GC} L_{eff-GC} \quad (2\text{-}44)$$

$$C_T(V_G) = \frac{C_{ox}C_B}{C_{ox+}C_B};\ C_B = \frac{\partial Q_{loc}}{\partial V_G} + \frac{\partial Q_{Free}}{\partial V_G}(V_G) \quad (2\text{-}45)$$

where $C_T(V_G)$ is V_G-dependent total gate capacitance per unit area, C_B is the capacitance per unit area due to V_G-responsive total charge in the active film, Q_{loc} is the localized

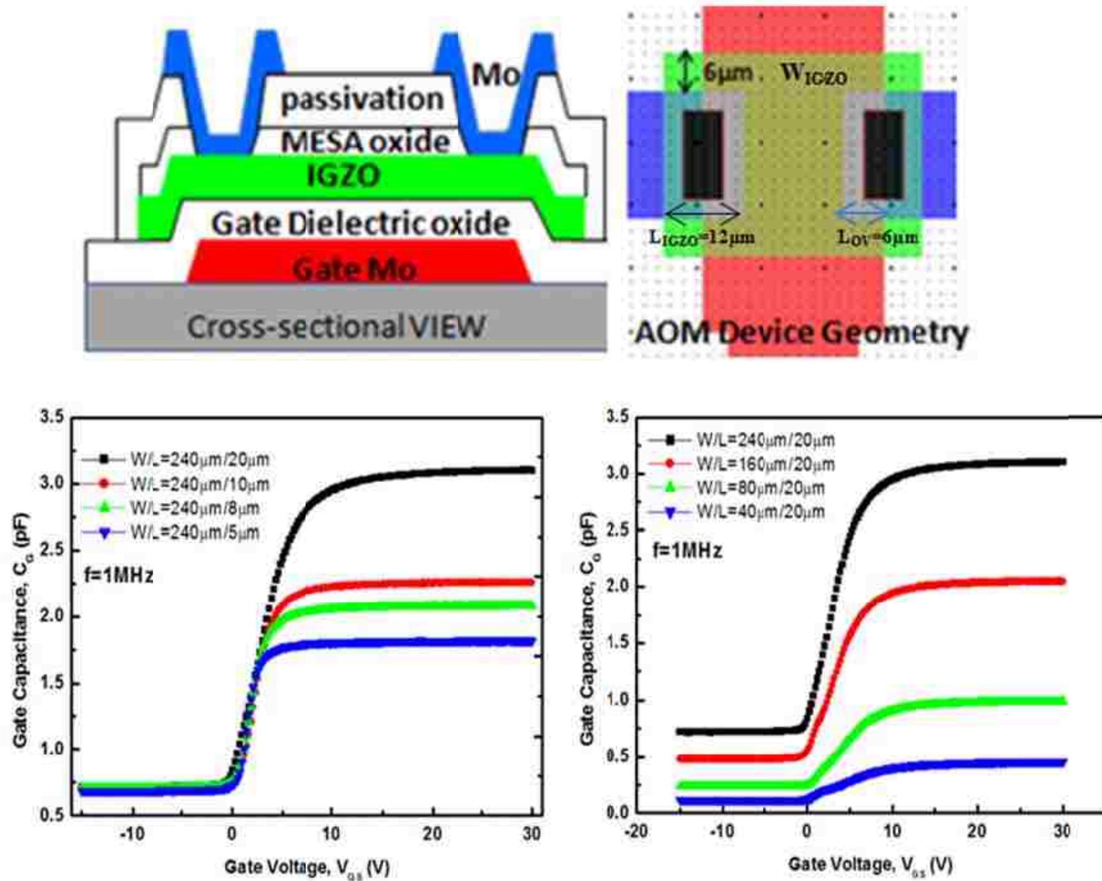

Figure 2.25 Layout dependent C-V characteristics of a-IGZO TFTs; The geometric parameters and cross-sectional view of TFT is shown above also.

trapped charges per unit area, Q_{free} is the free charge per unit area. Fig. 2.26 shows the cartoon band diagram with equivalent capacitance model illustrating the mechanism of V_{GS} dependent C-V characteristics. Electrons are injected from the S/D contacts into a-IGZO active layer at positive gate voltage ($V_G > 0$). The barrier height denoted in the Fig 2.26 is for Mo (0.2-0.4eV) [2.30-2.31]. Some of the injected electrons are trapped in the subgap DOS of a-IGZO while others are free charges in the CBM close to the SiO_2/a-IGZO interface. These electrons respond to the small signal (f =1MHz) superimposed onto V_{GS}, resulting in V_{GS} dependent C_{GS} response as indicated in Fig. 2.24. For negative gate voltage ($V_G < 0$), a-IGZO layer is depleted and the active bulk charges (Q_{loc} and Q_{free}) cannot respond to the variation of the small signal and C_G saturates at C_{MIN}.

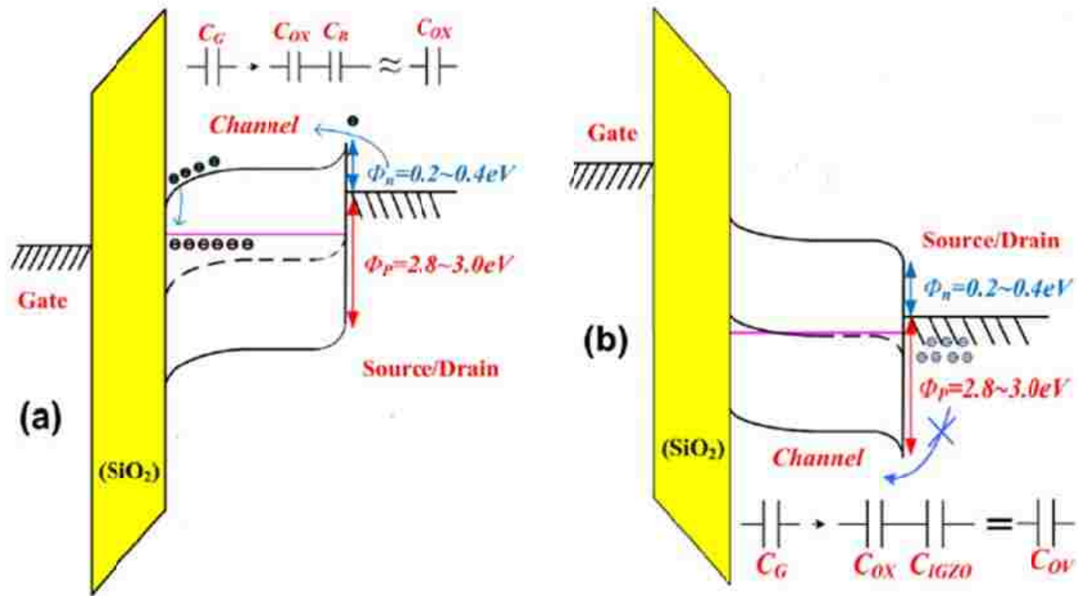

Figure 2.26 Cartoon representation of band diagram of a-IGZO with Mo S/D under (a) $V_G > 0$ and (b) for $V_G < 0$. Φ_n and Φ_p are electron and hole barrier (Adapted From Reference[2.29]).

2.8 Dual Gate Characteristic of a-IGZO TFTs

It is well known that a-Si:H TFT performance is strongly affected by the charge density at the interface between the a-Si:H and passivation layers (mostly SiN_x) [2.32]. As such, measuring the characteristics of TFTs with a dual-gate configuration is of considerable interest because the top gate on the back side of the semiconductor layer introduces another parameter that is equivalent to the charge density at the interface [2.33]. The interaction between the top- and bottom-gate electric fields, and in turn, the charge coupling shows appreciable variation from material to material. Thus, the use of a dual-gate structure is convenient for addressing issues of materials and correlating them with device performance. In order to utilize a-IGZO, which is a new material, in commercial applications, it is important to understand the main a-IGZO TFT features that are different from those of conventional Si:H TFTs [2.34].

One of the main features that distinguishes a-IGZO from a-Si:H is the difficulty of obtaining p-channel TFTs with oxide based materials. This difficulty is thought to originate from the intrinsic nature of the energy band structure in oxide semiconductors [2.35]. A conventional silicon-on-insulator (SOI) can be used to analyze the interface in terms of hole accumulation at the top interface of a-IGZO TFTs. Fig. 2-27(a) and (b) show I_{DS}-V_{GB}(V_{GB} is bottom gate bias) and $\partial g_m/\partial V_{GB}$ characteristics at various V_{GT} (V_{GT} is top gate bias) values, ranging from −20V to 20 V, for a-IGZO TFTs (W=240 μm, L=20μm) having a 70-nm a-IGZO layer; the thicknesses of the bottom and top SiO_2 were 100 nm. However, the top SiO_2 is deposited by RF sputtering as opposed to PECVD for

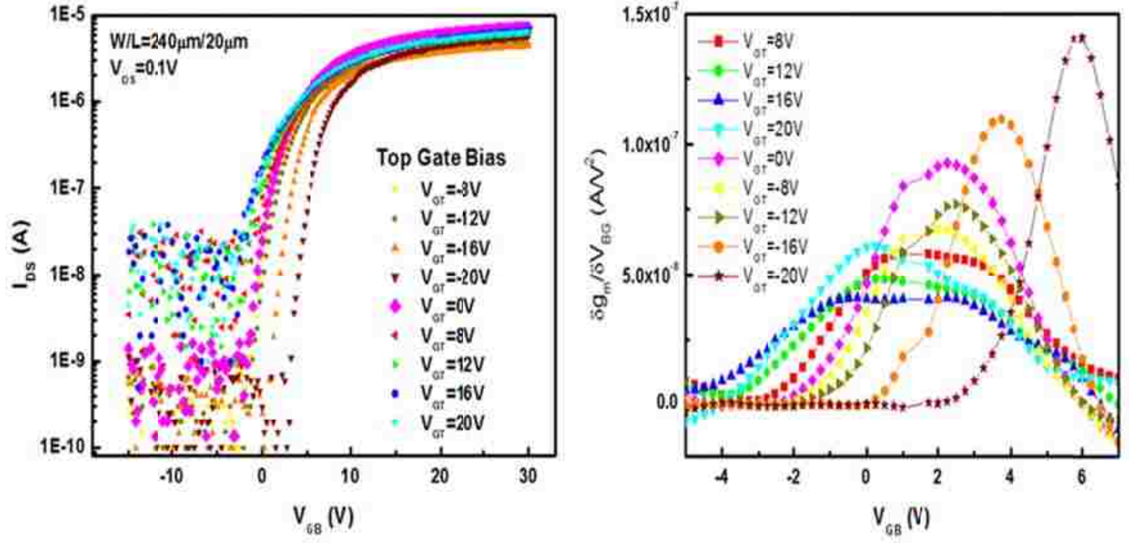

Figure 2.27 I_{DS}-V_{GB} and $\partial g_m/\partial V_{GB}$ characteristics of a-IGZO TFT (W=240 μm, L=20μm) with various V_{GT}.

the bottom dielectric layer. The I_{DS}-V_{GB} and $\partial g_m/\partial V_{GB}$ curves show parallel shifts in response to variations in V_{GT}. We should note that the curve shifts are not symmetrical with respect to the curve at V_{GT} = 0 V. In addition, the shifts on the negative side are more significant. Fig. 2.28 summarizes, on the basis of the results shown in Fig. 2.27(a) and (b), the dependence of threshold voltage (V_T) on V_{GT} for the given a-IGZO thickness. As seen in the figure, the relationship between V_T and V_{GT} is linear. This is similar to that which has been observed for n-channel SOI devices. It is well known that for fully depleted n-channel SOI devices, the V_T shift due to the substrate-bias effect can be related to capacitances of the depleted Si layer, the buried oxide layer, and the gate insulator [2.36]. By analogy with n-channel SOI devices, we obtain the following expression:

$$\frac{\partial V_T}{\partial V_{GT}} = -\frac{C_{IGZO} C_{GT}}{C_{GB}(C_{IGZO}+C_{GT})} \tag{2-46}$$

where C_{IGZO} is the a-IGZO depletion capacitance, C_{GT} is the top SiO_2 capacitance, and C_{GB} is the bottom SiO_2 capacitance. This equation can be derived from the relationships that describe the charge coupling between the bottom and top gates in a fully depleted SOI operation. We have made the same assumptions as those commonly used in a classical SOI theory with details described in [2.36]. One should note that the differential in (2-46) represents the ratio of two capacitances. One is the C_{GB} value that denotes the bottom-gate insulator capacitance, and the other is the $[(C_{IGZO}C_{GT})/(C_{IGZO} + C_{GT})]$ value that denotes the capacitance given by the series association of C_{IGZO} and C_{GT} in a fully depleted operation. Thus, this expression is valid only when the a-IGZO layer is fully depleted. In other words, this expression can only be applied to the situation in which V_{GT} is negative. By replacing the capacitance values in (2-46) with the thicknesses of the layers, we obtain

$$\frac{\partial V_T}{\partial V_{GT}} = -\frac{t_{GB}}{\frac{\epsilon_{GB}}{\epsilon_{IGZO}}(t_{IGZO})+t_{GT}} \tag{2-47}$$

where t_{GB} is the bottom SiO_2 thickness, t_{IGZO} is the a-IGZO thickness, t_{GT} is the top SiO_2 thickness, ε_{GB} is the bottom SiO_2 dielectric constant, and ε_{IGZO} is the a-IGZO dielectric constant (with $\varepsilon_{IGZO} = 11$ [2.37] and $\varepsilon_{GB} = 4$). It can be seen from (2-47) that dV_T/dV_{GT} should decrease with increasing t_{IGZO}. This is the trend we observe as well (not shown here).

The experimental results agree well with the SOI model. In n-channel SOI devices, the threshold voltage levels off once holes accumulate at the top interface as a result of negative gate bias. This is due to hole accumulation at the top surface that suppresses the penetration of top gate electric field into the active layer. However, as can

be seen in Fig. 2.27, the threshold voltage of the a-IGZO TFTs does not level off with decreasing V_{GT}, which is indicative of minimal hole accumulation. This behavior is in sharp contrast with conventional n-channel SOI devices. In a-Si:H based TFT for example, hole accumulation occurs at the top SiN_x/a-Si:H interface with limited penetration of the top-gate field. This limited penetration leads to a somewhat weaker interaction between the top and bottom fields for a-Si:H . For a-IGZO, band bending due to negative V_{GT} values appears to extend throughout the a-IGZO thickness. Holes in such oxide semiconductors as a-IGZO have been known to be strongly localized because of their unique energy band structure with strong localization of holes at the upper edge in the valence band (localized O 2p orbitals) [2.37]. As noted earlier, a-IGZO TFTs respond in a more pronounced manner with variation of the top- and bottom-gate fields than a- Si:H TFTs. This may be attributed to the low density of localized states in the energy

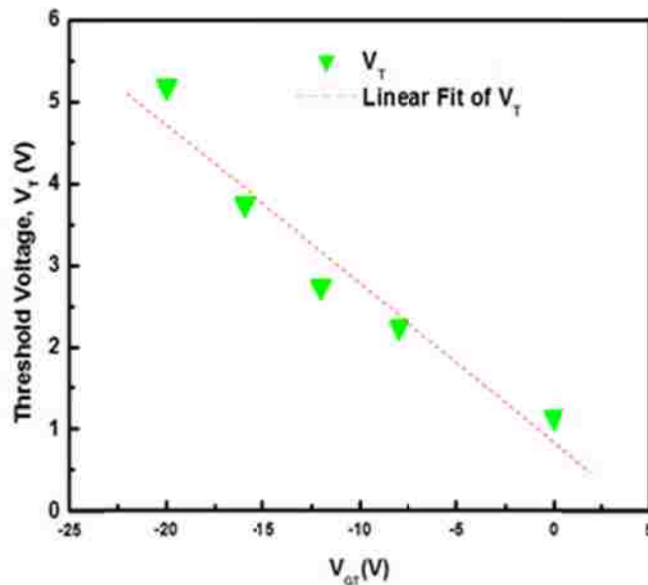

Figure 2.28 Dependence of V_T with various V_{GT} for dual-gate a-IGZO operation.

gap of a-IGZO [2.38]. Kimura et al. [2.38] have numerically estimated the density of localized states in a-IGZO on the basis of C–V measurements on a-IGZO TFTs and have shown that a-IGZO does not have the Gaussian-type state distribution commonly observed in a-Si:H and that it has a lower density of localized tail states than a-Si:H.

A comparison of experimentally derived dual-gate characteristics with SOI-model-based results gives considerable insight into the role of the top interface in electronic devices incorporating a-IGZO TFTs. In an active matrix LCD (Liquid Crystal Display) display, the performance may be adversely affected due to ions that are induced in the LC layer. The generation of ions can be attributed to the degradation of the LC (Liquid Crystal) layer after long-term LCD operations. The results of such generation are equivalent to what would occur if positive or negative V_{GT} values were applied to the top gate. For an LCD display driven by a-IGZO backplane array such estimation would be particularly important to an attempt to achieve stable LCD operations. a-IGZO TFTs could also be applied to other electronic devices, including inverter and logic circuits based on NMOS a-IGZO TFT arrays. In such devices, an appropriate control of charge density at the top interface, that is, a proper V_T control would be essential for achieving stable circuit operations.

2.9 Low Frequency Noise Characteristics of a-IGZO TFTs

Low frequency noise is an important figure of merit in device analysis. It represents not only the smallest signal the device is capable of handling, but it is also a powerful technique for defect characterization and investigation of hot carrier phenomena

in TFTs. Although there have been a number of reports on the electrical characterization of a-IGZO TFTs, very little is known about their low-frequency noise (LFN) properties. In recent reports, in the high drain current range, the results reveal $\frac{1}{f}$ noise (flicker noise) as the dominant LFN (Low Frequency Noise) source attributed to the mobility fluctuation mechanism [2.39-2.42]. In this work, we collaborated with Dr. C.A. Dimitriadis's group at Aristotle University of Thessaloniki, Greece to examine the noise properties of bottom-gate a-IGZO TFTs in the low drain current range, where the effect of the series resistance is negligible. The transfer characteristics of the devices were measured using a computer-controlled system including a Keithley 6514 electrometer and two Keithley 230 voltage sources. Noise measurements were performed at room temperature using a SR760 fast Fourier transform spectrum analyzer preceded by a SR570 low-noise current preamplifier. The gate and drain biases were supplied by CdNi batteries to reduce any external low-frequency noise. Fig. 2.29(a) shows typical plots of power spectral density S_I versus frequency f, measured at different drain currents with $V_{DS} = V_d = 0.1$ V. At very low drain currents, the spectra show a generation-recombination (g-r) type noise with a plateau at very low frequencies followed by a $\frac{1}{f^2}$ decrease, related to trapping and detrapping processes of carriers at discrete traps with a dominant time constant τ. The g-r noise is described by the relation $S_{gr} = S_{gr}(0)/ [1+(f/f_c)^2]$, where $S_{gr}(0)=S_I(0)$ is the plateau of the g-r noise spectrum and f_c is the corner frequency directly related to the trap time constant ($\tau = 1/(2\pi f_c)$). Fig. 2.29(b) presents the extracted parameters of $S_{gr}(0)$ and f_c at drain currents $I_d = 0.3$ and 2 nA.

The dependences of the g-r noise parameters $S_I(0)$ and τ on the drain current are presented in Fig. 2.30, where a maximum is observed in both curves. It is seen that the maximum value of $S_{g\text{-}r}(0)$ is at a higher value of I_d than the maximum value of τ and the increase of τ with increasing I_d is non-linear. The non-linear dependence of τ on I_d suggests that the discrete trap centers responsible for the g-r noise are located in the IGZO material at some distance from the gate oxide/semiconductor interface, i.e. these are bulk traps and not interface states for which τ has been shown to be linearly dependent on I_d [2.43]. The finding that τ is not constant but has a non-linear dependence on I_d indicates that the g-r bulk trap centers are not homogeneously distributed over the thickness of the depletion region, but they are located in a thin layer of the depletion region which influences the nearby carriers in the conducting channel [2.43]. For complete characterization of the g-r trapping parameters, noise measurements as a function of temperature are required, which was not pursued in this particular study [2.44].

For drain currents $I_d > 5$ nA, the g-r noise is overshadowed by a higher 1/f noise component as shown in Fig. 2.29(a). The deviation from the g-r noise is related to the emerging influence of oxide traps located close to the IGZO/SiO_2 interface. Fig. 2.31 shows the variation of the normalized drain current spectral density S_I / I_d^2 with the drain current and the corresponding transconductance-to-drain current ratio squared $(g_m/I_d)^2$, measured at frequency f = 2 Hz. It is clearly seen that S_I / I_d^2 varies as $(g_m/I_d)^2$ in the drain current region above 1 nA. This finding indicates that the 1/f noise originates from carrier

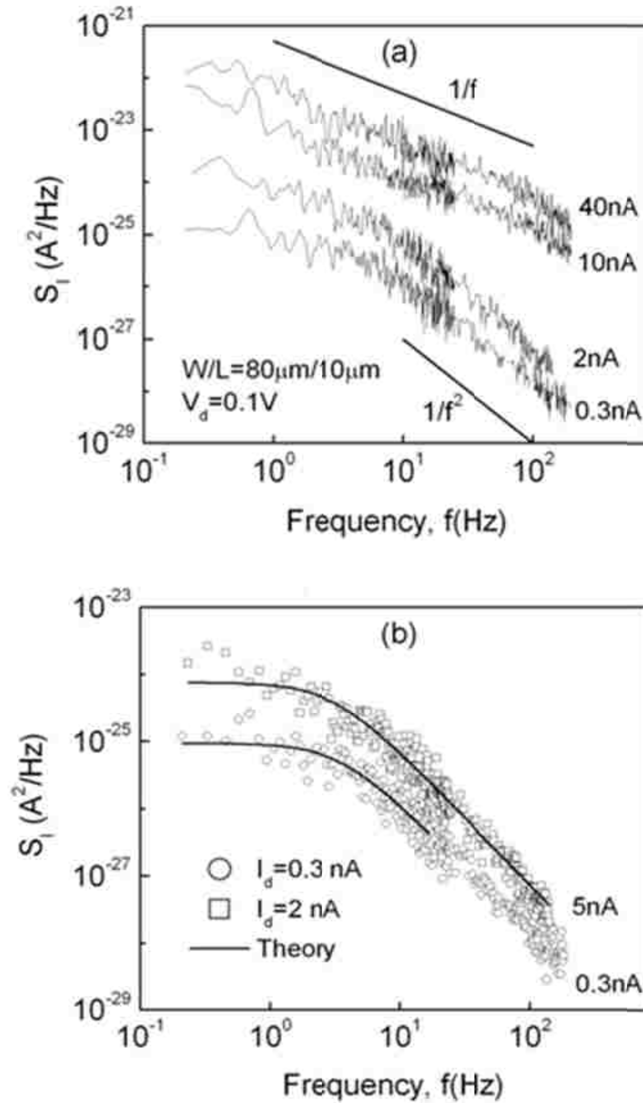

Figure 2.29 (a) Drain current noise spectra of IGZO TFT, measured at drain voltage V_d = 0.1 V and different drain currents. (b) The generation-recombination components were reproduced using the g-r parameters: $S_I(0) = S_{gr}(0) = 9.3 \times 10^{-26}$ A^2/Hz, f_c = 3.63 Hz for I_d = 0.3 nA and $S_{gr}(0) = 7.4 \times 10^{-25}$ A^2/Hz, f_c = 3.1 Hz for I_d = 5 nA.

number fluctuations due to electron exchange between the channel and the traps located in the gate insulator close to the interface [2.43]. The Hooge mobility fluctuations model predicts [2.45] that S_I / I_d^2 should vary as $1/I_d$, which is not valid as shown by the broken

line in Fig. 2.31. According to the carrier number fluctuation model, the drain current noise is given by [2.45]

$$\frac{S_I}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 \times \frac{q^2 kTN_{t,ox}}{WLC_{ox}^2 f \alpha_t} \tag{2-48}$$

where q is the electron charge, kT is the thermal energy, C_{ox} is the gate capacitance per unit area, $N_{t,ox}$ is the density of the gate insulator traps ($cm^{-3}eV^{-1}$) and α_t is the tunneling attenuation coefficient of the electron wave function in the gate oxide, which for SiO_2 is taken 10^8 cm^{-1} [2.45]. From the data of Fig. 2.31 and using (2-48) we found $N_{t,ox} = 2.3 \times 10^{20}$ $cm^{-3}eV^{-1}$. The generation of pure 1/f noise indicates uniform spatial distribution of

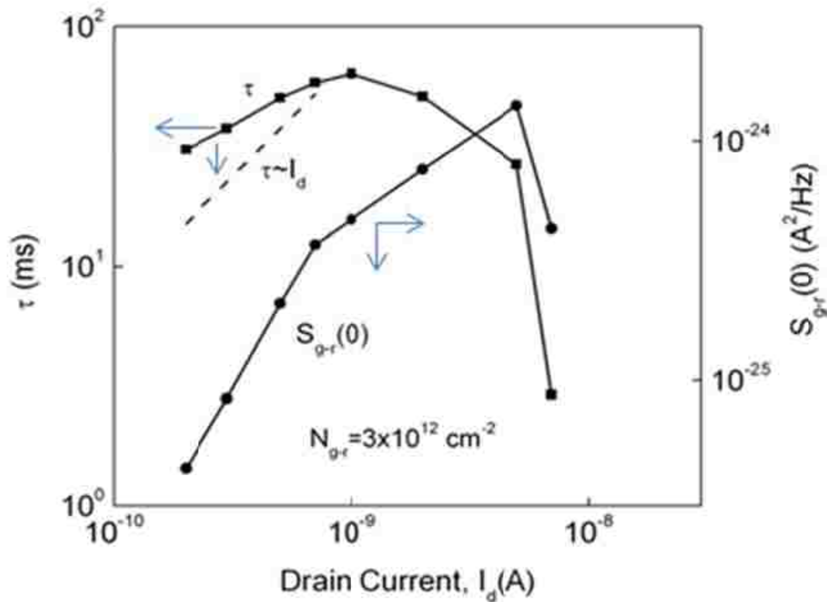

Figure 2.30 Variation of $S_{gr}(0)$ and τ with drain current for the g-r noise in IGZO TFT with W/L = 80 μm/10 μm.

the traps in the gate oxide [2.45]. The trap spatial distribution can be determined by converting the frequency to tunneling depth through the relation $1/2\pi f = \tau_o \exp(\alpha_t x)$, where τ_o is the time constant at the interface and x is the distance into the oxide from the interface. The typical value of τ_o is 10^{-10} s for traps distributed up to 5 nm [2.46]. The constant trap distribution profile is presented in the inset of Fig. 2.31.

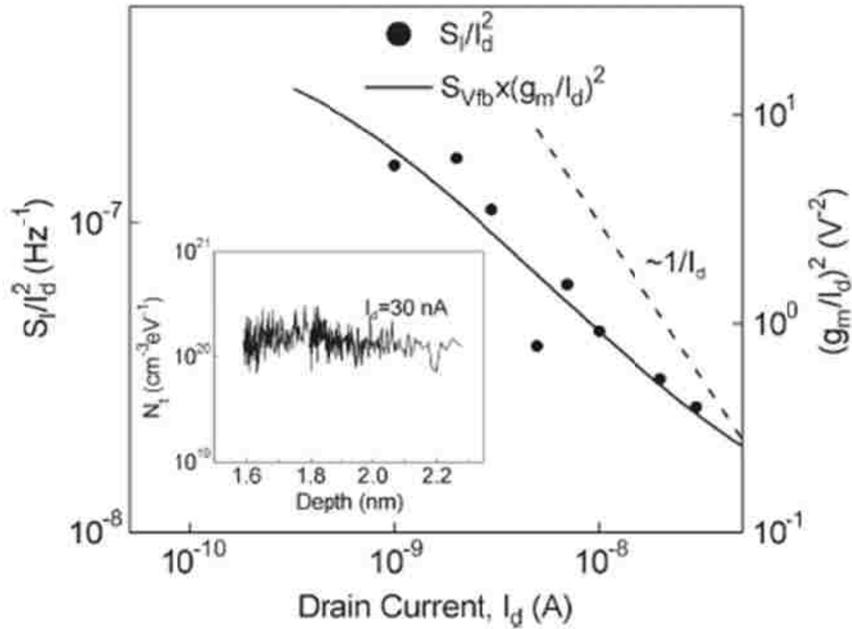

Figure 2.31 S_I / I_d^2 versus I_d plot of the IGZO TFT, measured at the frequency of f = 2 Hz. The solid line is the best fit to (2-48) with $N_{t,ox} = 2.3 \times 10^{20}$ cm^{-3}eV^{-1} The dashed line is the S_I / I_d^2 vs. $1/I_d$ relation from the mobility fluctuation model. The inset presents the gate oxide trap density profile derived from the noise spectrum at drain current I_d = 30 nA.

The origin of the low frequency noise of a-IGZO TFTs with SiO_2 gate dielectric was investigated in the low drain current range. Two different sources of noise were identified: a g-r noise component at drain currents below 5 nA and a pure 1/f noise at

higher drain currents. The g-r parameters indicate that the g-r noise originates from bulk traps located in a thin layer of the depletion region. The drain current dependence of the normalized power spectral density S_I / I_d^2 shows that the 1/f noise is due to the carrier number fluctuations mechanism. As a result of the pure 1/f noise, the gate oxide traps have a uniform spatial distribution.

2.10 Temperature Dependent Analysis of a-IGZO TFTs

Temperature dependent field effect measurements can provide valuable information of device function. For example, at temperatures below room temperature, the dominant mechanism for carrier transport in a-Si:H is ascribed to variable-range hopping, while band conduction occurs easily in a-IGZO [2.47]. At higher temperatures, free carriers in a-Si:H are thermally activated, and thus, band transport, which is sporadically interrupted by trapping at the localized tail states below the conduction band mobility edge E_c, contributes to the conductivity. On the other hand, free carriers in a-IGZO mainly originate from point defects in the system.

2.10.1 Meyer-Neldel (MN) Conduction in a-IGZO TFTs

Transfer characteristics and representative field effect parameters of a-IGZO TFTs (W=240µm, L =20 µm) at different temperatures ranging from 20°C to 80°C, is shown in Fig. 2.32. From the figure, we observe that μ_{FE} is weakly thermally activated, with very low activation energy ($E_{a\mu}$) 15meV, V_T decreases with a temperature coefficient of 17.5mV/°C and the subthreshold slope (SS) slightly increases from 0.5 to

0.7V /dec. There is no anomalous Off current increase at elevated temperatures either which points to stable operation of these devices. There is evidence of thermally activated

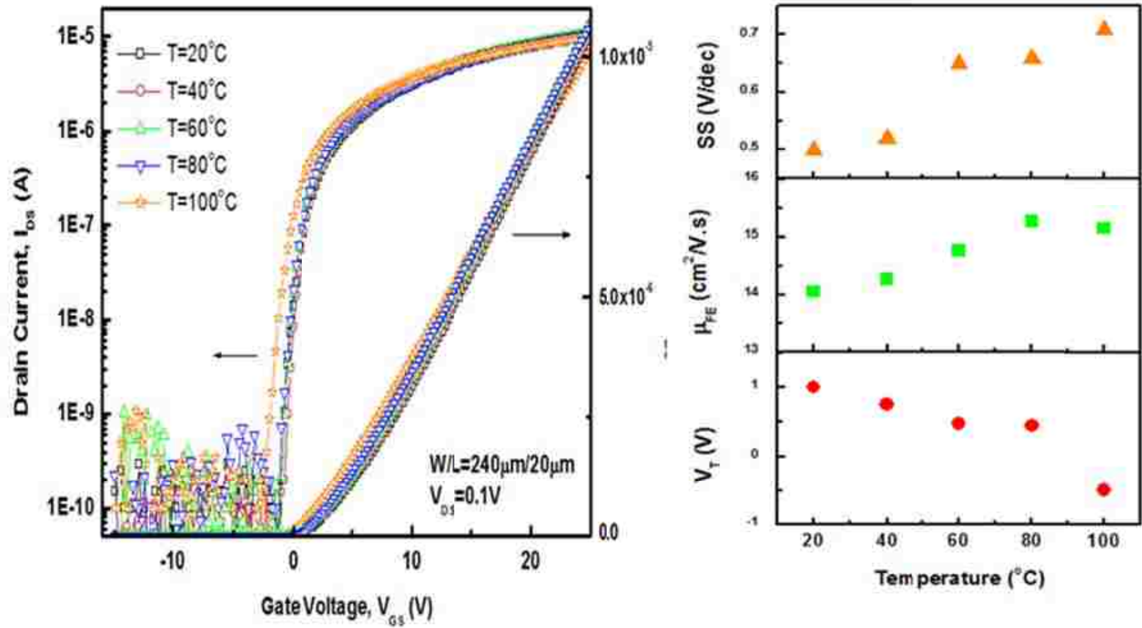

Figure 2.32 Temperature dependence of a-IGZO TFT and the representative field effect parameter variation.

channel conductance. Figure 2-33 shows from the Arrhenius plots that the channel conductance, G (Ω^{-1}) and the channel conductance prefactor (G_0) significantly changes with V_{GS} in the subthreshold region ($-1 < V_{GS} < 0.5$). In the above-threshold region ($0.5 < V_{GS}$), however, G_0 is almost constant irrespective of V_{GS}. On the other hand, for the a-Si:H TFT, G_0 appears to vary with V_{GS} over the entire V_{GS} region studied. The channel-conductance prefactor, G_0 increases exponentially with E_a, which suggests that the channel conductance follows the MN rule, which can be expressed as [2.48]

$$G = G_0 exp\left(-\frac{E_a}{kT}\right) = G_{00} exp(AE_a) exp\left(-\frac{E_a}{kT}\right) \quad (2\text{-}49)$$

where k denotes the Boltzmann constant and A the MN parameter. From the slope of the straight lines in Fig. 2.33, we estimate the A^{-1} values to be 14.3 meV. The Meyer-Neldel rule in generally considered to be an intrinsic property of a material applicable whenever the Fermi level position is varied, regardless of whether this shift is caused by introducing extra defect states to the sample or as in this case, by applying an electric field [2.48]. For our a-IGZO TFTs, the MN parameter is constant over a broad range of E_a values in the subthreshold region (Fig 2.34).

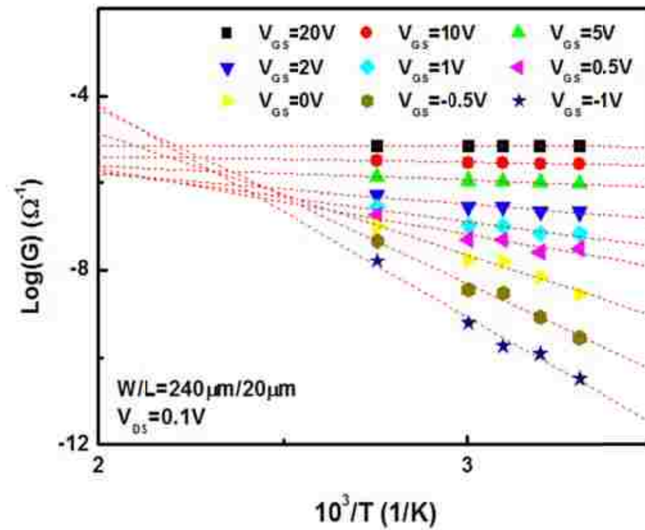

Figure 2.33 Temperature dependence of drain current; the linear fit determines the slope to measure activation energy, E_a for the different V_{GS}.

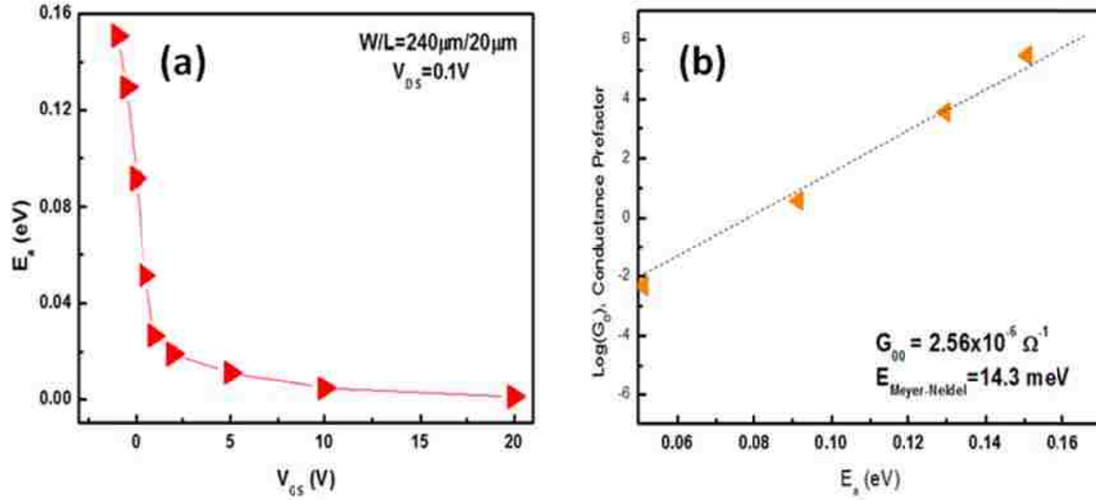

Figure 2.34 (a) dependence of Experimental E_a on V_{GS} and (b) channel conductance prefactor, G_0 dependence on E_a validating Meyer-Neldel Conduction.

2.10.2 Point Defect Generation with Thermal Excitation

The lower V_T observed for the increased temperatures in Fig. 2.30 may be associated with the generation of point defects, peculiar to oxide semiconductor. Thermally excited oxygen atoms that can leave their original sites induce vacancies (point defects) with remaining free electrons at the sites. The lower V_T observed at the higher temperatures can be attributed to these free electrons generated along with the oxygen vacancies. We assume that an oxygen vacancy induces two free electrons. According to the statistical thermodynamics, in order to minimize the free energy of the system, it is inevitable that point defects are generated depending on the ambient temperature [2.49]. The generation of point defects increases the internal energy of the system and at the same time increases the entropy of the system, resulting in the minimization of the free energy. In addition, since the defect formation involves the carrier generation, the charge neutrality needs to be taken into account. On the basis of

the assumption that the density of point defects n is much lower than the densities of lattice and interstitial sites, n is given as [2.50]

$$n = C_1 exp\left(-\frac{W}{3kT}\right) \quad (2\text{-}50)$$

where C_1 denotes the constant related to the entropy for the formation of one vacancy and two free electrons, k the Boltzmann constant, and W the defect formation energy. The V_T decrease (ΔV_T) seen in Fig. 2.32 can be thus related to W by

$$2et_{IGZO}C_1\left[exp\left(-\frac{W}{3kT}\right) - exp\left(-\frac{W}{3kT_{room}}\right)\right] = \Delta V_T C_{ox} \quad (2\text{-}51)$$

where T_{room} stands for the room temperature, C_{ox} the capacitance of the gate insulator, e the electronic charge, and t_{IGZO} the thickness of the a-IGZO semiconductor layer. If W is

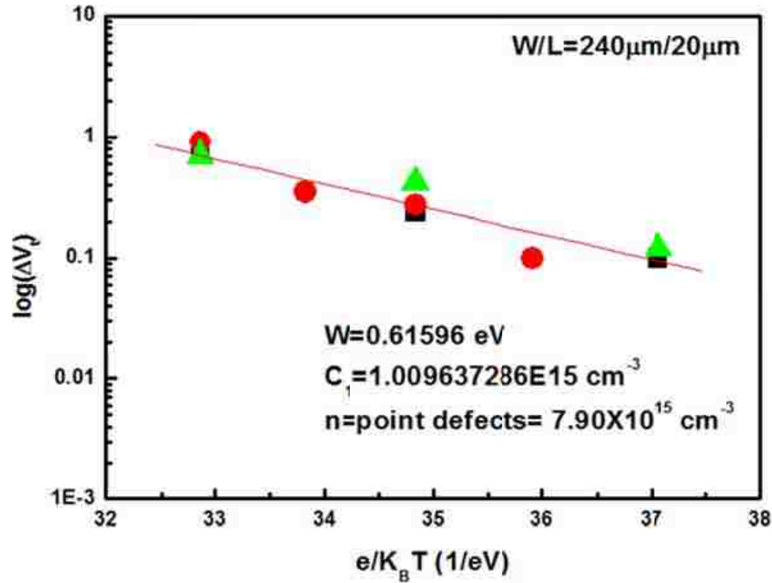

Figure 2.35 Point defect density determination from dependence of Experimental $\ln(\Delta V_T)$ vs. e/k_BT plot of 3 different IGZO TFTs

much higher than the energy at room temperature (0.026 eV), then the second term on the left-hand side can be neglected. Taking the logarithm of both sides we obtain

$$\ln(\Delta V_T) = -\frac{W}{3kT} - \left[ln\left(\frac{C_{ox}}{2et_{IGZO}C_1}\right)\right] \tag{2-52}$$

W and C_1 can be derived from the slope and intercept of the straight line shown in Fig 2.35. We obtain a W of 0.62 eV and a C_1 of 1.009^{15} cm^{-3}. Using these values, the defect density is estimated to be 7.9×10^{15} cm^{-3} at room temperature. This estimated defect formation energy is of the same order as those for typical oxide semiconductor crystals ranging from approximately 0.5 to 2.0 eV [2.51].

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Chapter 3

Suppression of Voltage Bias Temperature Stress Induced Instability (NBTI/PBTI) in N_2O Treated Amorphous IGZO Thin Film Transistors on Flexible Metal Substrates

3.1 Introduction

In flat panel displays of today, active matrix thin-film transistors (TFTs) form the backbone of the switching elements in the pixel design and are integral part of the gate driving circuitry. Although amorphous silicon (a-Si:H) has been the mainstay in display devices to date, there is immense interest these days to engineer new approaches to integrated electronics that utilize non-Si based materials deposited at low temperatures on cheap and flexible substrates. Amorphous oxide semiconductors as mentioned before are a class of materials with unique electronic, structural and transport properties that allow such integration [3.1]. They have gained considerable attention and have been used as

active channel layer of thin film transistors (TFTs) that find broad range of applications in active-matrix electronic papers[3.2], organic light-emitting diode (OLED) devices[3.3] and high resolution liquid-crystal displays (LCD)[3.4]. In particular, amorphous indium gallium zinc oxide (a-IGZO) TFTs are attractive alternative to traditional silicon (Si) based devices since they offer several key advantages such as high mobilities (>10cm^2/V.s), an amorphous crystal structure which, due to a lack of grain boundaries, can aid in achieving good uniformity and ease of manufacturing, transparency in the visible spectrum and very low processing temperature [3.5].

Replacing a-Si:H in the mature AMLCD industry will be difficult but a-IGZO can enable future TFT backplanes for higher-performance AMLCDs, 3-D displays, active matrix organic light-emitting diode (AMOLED) displays, large area flexible electronics, and transparent electronics [3.6-3.9]. Ultrahigh-resolution displays of tomorrow with faster frame rates will require TFTs that are not currently possible with a-Si:H technology. Also in such an emissive display, the demand for TFT stability is paramount since any shift in threshold voltage, ΔV_T, would cause pixel-to-pixel nonuniformity [3.10]. Although it is possible to use a-Si:H for this application, its inherent instabilities must be compensated with additional TFTs, which require additional area and complicated circuit designs. To ensure reliable pixel switching and circuit operation based on a-IGZO TFTs, it is imperative to evaluate their electrical stability. It becomes even more critical in the case of current driven OLED displays because it can lead to variations in the respective pixel brightness [3.11]. There is a plethora of studies that report on gate bias induced instability of various multi-component oxide based TFTs [3.12-3.18]. To summarize,

electrons trapping at the gate dielectric/channel interface without the creation of new defect states or gate-field induced oxygen adsorption were mainly attributed for ΔV_T under prolonged positive gate bias stressing conditions. These assignments of the charge trapping, injection, or channel defect creation models as the origin of the ΔV_T instability can be understood in the framework of a-Si:H TFTs. The long term stability and reliability is therefore absolutely critical for a-IGZO based technology to gain foothold over their a-Si:H based counterparts and for mass production. Bias temperature stress induced ΔV_T in these devices needs to be minimized for this purpose. This stringent requirement also applies to the switching transistors for other active matrix electronics, including display modes such as e-paper and LCDs, which is helpful to achieve a low power consumption and simple circuit design. For this reason, the device instability of oxide TFTs has been mainly examined under positive gate bias. In active matrix display devices however, the switching TFT undergoes continuous negative pulsed gate bias stress and in fact, duration of the negative bias is larger than that of positive bias [3.19]. Thus device degradation by NBTI (Negative Bias Temperature Stress Instability) is a critical issue that needs to be addressed in greater detail.

In this chapter we discuss suppression of bias temperature stress related instability in a-IGZO by post-fabrication N_2O treated plasma passivation. As mentioned before, since the ΔV_T instability can be understood within the framework of a-Si:H TFTs, a succinct review of instability in a-Si:H TFT is provided first, followed by stability concerns in metal oxide TFTs. Evolution of threshold voltage shift with time and temperature dependent bias stress measurements are done to elucidate the effects of N_2O

plasma treatment on the NBTI and PBTI (Positive Bias Temperature Stress Instability) of a-IGZO TFTs.

3.2 Bias Temperature Stress Instability: Framework of a-Si:H TFTs

a-Si:H is an inherently metastable material which must be hydrogenated to be electrically useful. The role of hydrogen in the amorphous network is to satisfy dangling bonds, so that related trapping states distributed across the band gap are, at least to a large extent, passivated. From reliability point of view, this is problematic since the distribution of states within the band gap is not stable but as it turns out, depends on the Fermi level position, as established by an electrical bias in a TFT [3.20]. The instability

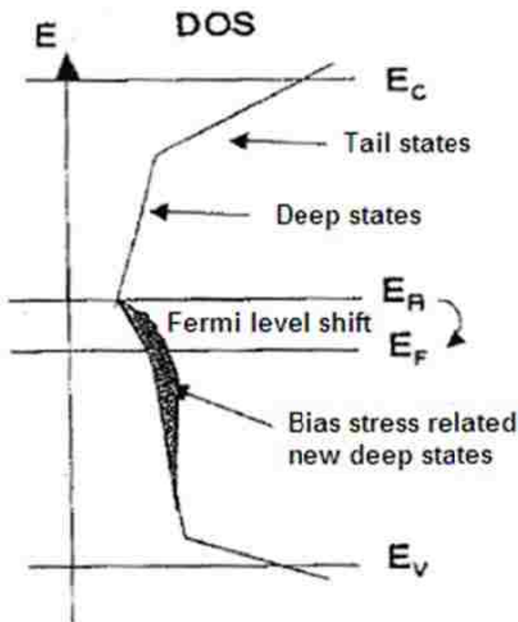


Figure 3.1 Bias induced metastable defect states in a-Si:H TFTs. E_A is the flat-band Fermi level. Adapted from Ref. [3.20].

in a-Si:H TFTs has generally been attributed to one of two mechanisms: charge injection and subsequent trapping in the a-Si:N_x:H gate insulator, or a bias-induced increase of silicon dangling bonds [3.21-3.22]. The mechanism related to metastability is point defect creation in the a-Si:H layer or at the a-Si:H/a-Si:N_x:H interface that increases the density of deep gap states [3.23]. When a positive gate bias causes electrons to accumulate at the channel/dielectric interface, most of these electrons reside in the conduction band tail states. These tail states have been identified as weak silicon-silicon bonds which, when occupied by electrons, can break to form silicon dangling bonds or deep state defects [3.23]. The accumulation of electrons in the conduction band tail states causes a metastable increase in the density of deep defect states as shown in Fig 3.1. Since the subthreshold slope in the transfer characteristics of n-channel TFTs does not change after positive bias stress, the newly created states must be located below the flat band Fermi level. The increase in the number of defect states causes the ΔV_T [3.23].

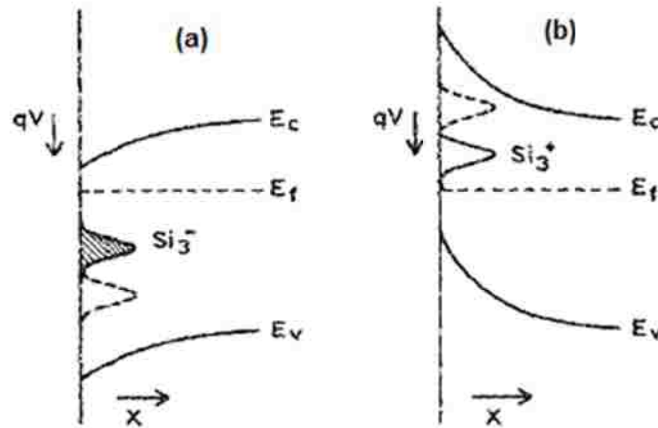


Figure 3.2 Band bending in a-Si:H under (a) accumulation and (b) inversion.The created dangling bonds are negatively charged under positive bias and positively charged under negative bias. qV is bias on the gate. Adapted from ref. 3.24.

Using ambipolar a-Si:H TFTs it was shown that if the density of deep gap states is modified in the a-Si:H and the Fermi level moves through these states in establishing the conduction channel accumulation layer, the electron and hole current-voltage curves would shift in opposite directions [3.24]. The band bending diagrams showing deep gap states filling under accumulation and inversion are illustrated in Fig 3.2.

Several mechanisms of electron injection and trapping have been proposed to explain ΔV_T and the hysteresis in I-V characteristics of TFTs [3.25]. Fig 3.3 shows the band diagram of a Metal-Insulator-Semiconductor (MIS) structure, with the nitride (a-

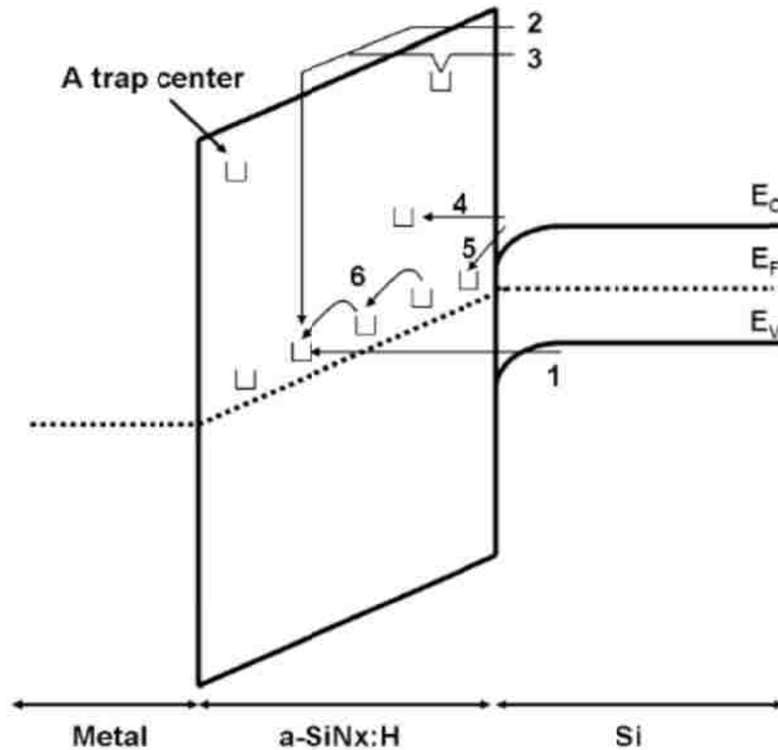


Figure 3.3 Charge trapping mechanisms: 1- direct tunneling from valence band, 2- Fowler-Nordheim injection, 3- trap-assisted injection, 4- constant-energy tunneling from silicon conduction band, 5- tunneling from conduction band into traps close to E_F , and 6- hopping at the Fermi level. Adapted from Ref. [3.25].

Si:N_x:H) as the insulator biased with a positive voltage. The gate/nitride/channel trilayer in TFTs is essentially an MIS capacitor. Once the electron accumulation channel forms near the a-SiN_x:H interface, several electron injection and trapping mechanisms may occur. A simplified view of the different mechanisms is depicted in Fig 3.3 and are numbered, they are direct tunneling from valence band, Fowler-Nordheim injection, trap-assisted injection, constant-energy tunneling from silicon conduction band, tunneling from conduction band into traps close to E_F , and hopping at the Fermi level, respectively [3.25]. Determining which one is dominant is not easy and, in general, they are dependent on the nitride trap density and the applied electric field. Mechanisms 1-3 are believed to occur at relatively large electric fields, while others may happen even at low fields [3.25].

In contrast to the defect state creation which is irreversible and stable at room temperature, charge trapping is reversible even at room temperature [3.26], and initial drain current can be recovered [3.27]. Indeed, charge release (detrapping) from the nitride dielectric, back into the TFT channel layer, is energetically favorable when the gate bias is removed. In Fig. 3.3, assume that we apply a gate bias to the TFT or MIS structure and, thus, some amount of charge is trapped in the nitride dielectric. The trapped charges occupy energy levels close to the nitride Fermi level which is below the Fermi level of channel layer. Once the gate bias is removed, the energy of trapped charges lies above the Fermi level in the channel layer. This energy difference favors detrapping and back-tunneling of charges into the channel layer.

Building on results showing charge injection to be the primarily responsible mechanism for ΔV_T, Libsch and Kanicki [3.26] found they could adequately model all

their bias-temperature stress data regardless of the magnitude of the stress bias, its polarity, or the temperature at which the stress was applied, using the well-known stretched exponential equation. They reasoned that for shorter stress times, smaller gate voltages, or lower temperatures, carriers are injected from the a-Si:H channel layer into energy states located at the a-Si:H/nitride interface and in a transitional layer close to the interface. At higher stress times, larger gate voltages, or higher stress temperatures, a larger fraction of the states near the interface are filled, which increases the probability of re-emission from these filled states, towards those deep in the nitride. They stated that the motion between traps is diffusive superimposed with a drift velocity caused by the electric field [3.26].

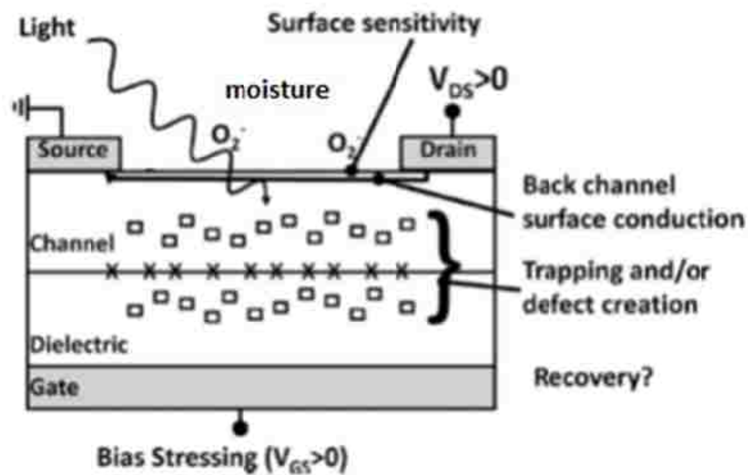


Figure 3.4 Schematic representations of potential instabilities in the a-IGZO TFTs. Adapted from Ref. [3.29]

3.3 Instability Concerns in a-IGZO TFT

Based on the understanding that has been developed for a-Si:H/a-SiN_x:H TFTs [3.26-3.27], we can expect that bias stressing and or illumination may lead to instabilities

such as charge trapping and, possibly, defect formation in the a-IGZO layer, in the gate dielectric, or at the a-IGZO/dielectric interface. It might also be expected that an increased temperature or a simultaneous exposure of a device to both bias stress and illumination could lead to enhanced or additional instabilities. In most of the reported a-IGZO TFTs, the back surface is exposed to atmosphere. Metal oxides are well known as gas sensors [3.28], and thus, one might also expect instabilities due to back surface/ambient interaction.

While not an issue for our back channel passivated a-IGZO devices, the interaction with ambient molecules on the back surface could lead to "back-channel" surface conduction in the bottom gate devices. The encapsulation or passivation or surface treatment of the back surface, so as to reduce or eliminate the interaction with the ambient, would be expected to have an impact on the operation and stability of bottom gate devices. Finally, the generation and recovery of all of these instabilities over time may lead to a time-dependent operation. The stability concerns are shown in Fig. 3.4. Although the ΔV_T in a-IGZO TFTs can be understood within the a-Si:H TFT instability mechanisms, the fundamental material difference between a-Si:H and a-IGZO-based oxide semiconductors should be considered carefully. The relative low sensitivity of the electron mobility of these oxide semiconductors to their corresponding crystal structure was explained by Nomura *et al.* [3.30]. In typical covalently bonded materials such as Si, carrier transport is primarily through the directional sp^3 orbitals and is affected by structural randomness that greatly reduces bond overlap and carrier mobility. In metal oxides, nondirectional ns orbitals make up the conduction band attributed to the higher

bonding. Since the overlap of these s orbitals is not significantly altered by the introduction of randomness, carrier transport and, thus, mobility is relatively insensitive to randomness. This fundamental difference in bonding may also play a role in TFT stability and reliability [3.31-3.32].

3.4 Bias Temperature Stress Experiments in a-IGZO TFTs

3.4.1 N_2O Treated a-IGZO TFT Fabrication

The TFTs were fabricated on stainless steel substrates, coated with 1 μm thick PECVD SiO_2 layer to electrically isolate the substrate. The IGZO TFT device has a staggered, bottom-gate architecture as shown in Fig. 3.5. The devices were fabricated by first depositing 150 nm of Mo by RF sputtering and photographically patterning and wet etching to form the gate layer. A 100 nm thick SiO_2 was then deposited by PECVD at 300°C with breakdown field exceeding 8MV/cm. Then, a blanket 50 nm of IGZO was deposited followed by N_2O plasma treatment in PECVD chamber at 100 W for 5 minutes before a 50 nm of low temperature SiO_2 film (mesa oxide layer) could be deposited by

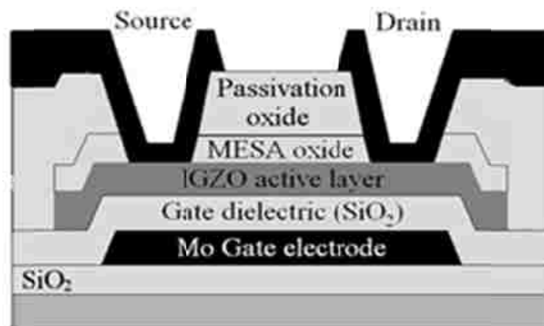


Figure 3.5 Cross-sectional schematic of a fabricated N_2O plasma treated a-IGZO TFT, with SiO_2 back-channel passivation.

RF sputtering. The IGZO sputtering was from a 6-inch diameter commercially available target (1:1:1 molar ratio of In_2O_3:Ga_2O_3:ZnO). The optimized IGZO/SiO_2 stack was patterned by combination of dry (CF_4) and wet etching (dilute HCl~40:1 in DI water). A thicker (70 nm) sputter deposited passivation oxide capped off the patterned layers to protect the active channel region. Contact openings to access the pads were accomplished by lithography and selective etching of the oxide layer. Subsequently, opening of source/drain electrodes were done by dry etch. In order to reduce etch damage and improve contact resistance, the patterned S/D areas were treated in Ar plasma. Finally, Mo source and drain metallization was done by RF sputtering and subsequent lift-off. Completed devices underwent 1 hr anneal at 300°C in N_2 ambient before testing could proceed.

3.4.2 N_2O Treated a-IGZO TFT Electrical Measurements Under Bias Stress

The transfer characteristics of the devices were measured with Lab-View interface-controlled semiconductor parameter analyzer (HP4145B) and in a probe station with the devices mounted on an automated heating chuck. A series of NBTS (Negative Bias Temperature Stress) and PBTS (Positive Bias Temperature Stress) measurements were conducted (at temperatures between 20°C-80°C) for the steady-state conditions at predetermined stress voltage (V_{GS_STRESS} = ± 20V) applied to the gate electrode with the drain terminal shorted to the source terminal (V_{DS}=0 V) to maintain a uniform electrical field distribution along a-IGZO/SiO_2 interface. Each series of BTS experiments was done

on the same TFT and to ensure consistent initial TFT properties, the thermal annealing at 100°C was carried out for 10 min in N_2 ambient to revert to pristine device operation.

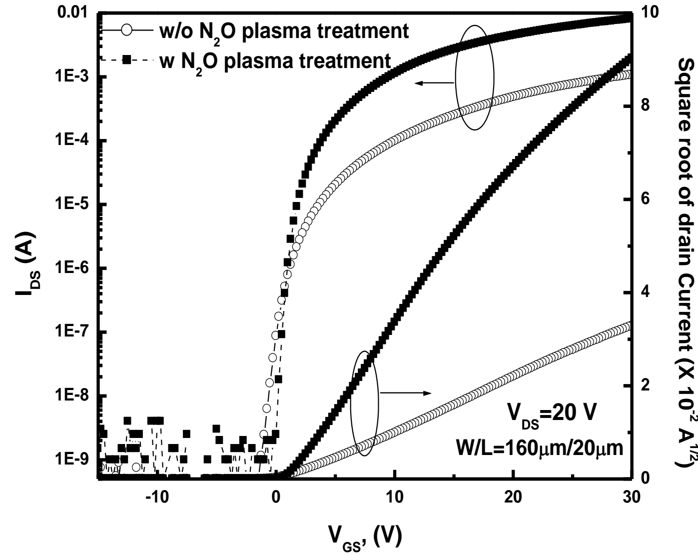


Figure 3.6 I_{DS}-V_{GS} characteristics of a fabricated a-IGZO TFT, W=160μm, L=20μm measured at V_{DS} = 20 V.

3.5 BTS induced ΔV_T instability in N_2O Treated a-IGZO TFTs

3.5.1 Electrical Properties of a-IGZO TFT without stress

Typical TFT parameters are extracted from transfer (I_{DS}-V_{GS}) and output (I_{DS}-V_{DS}) curves. Transfer characteristics of plasma treated and as-deposited a-IGZO TFTs with channel length of 20μm and channel width of 160μm measured at V_{DS} =20V is shown in Fig 3.6. The IGZO TFTs operate in n-type enhancement mode and exhibit hard saturation. The PECVD SiO_2 dielectric (Breakdown voltage > 8MV/cm) is effective in suppressing gate-leakage current below 10 pA which results in high I_{ON}/I_{OFF} ratio. Field effect mobility of 13.5cm^2/V.s and 15.07cm^2/V.s is calculated using standard MOSFET

equations in the linear and saturation regime respectively. The other parameters are listed in Table 3.1. The slight increase in threshold voltage calculated from linear extrapolation of $\sqrt{I_{DS}}$-V_{GS} plot can be explained by the following equation [3.33]:

$$V_T = \frac{q}{C_{GS}}\left[\left(N_t - n_{to}\right) - \left(n_1 - n_{co}\right)\right] + V_{FB} \tag{3-1}$$

where C_{GS} and V_{FB} are defined as the gate capacitance density and flat band voltage. N_t, n_{to}, n_1 and n_{co} are mean trap density, equilibrium density of occupied traps, conduction band density when $E_F = E_t$ (E_t=trap energy) and equilibrium conduction band density. The V_T denoted by (3-1) specifies a threshold voltage for a discrete trap model. The equation is applicable to either an acceptor-like or a donor-like trap. In the context of the discrete trap model, the $[q/C_{GS}(N_t-n_{to})]$ term corresponds to the gate voltage required for complete trap filling, while $[q/C_{GS}(n_1-n_{co})]$ is equal to the corresponding conduction band stte filling voltage, when the Fermi-level is equal to the trap energy, so that all of the traps are essentially filled. Since the N_2O treatment improves the subthreshold swing with little hysteresis, no additional trap creation is indicated; rather a reduction of sub-gap density can be attributed for the threshold voltage movement.

Table 3.1: Device Parameters of N_2O Plasma Treated vs. As-Deposited a-IGZO TFT

	Mobility μ (cm^2/V.s)	Threshold Voltage (V)	Substhreshold slope (mV/decade)
No Plasma treated	13.1	-0.2	690
N_2o Plasma treated	15.7	0.7	360

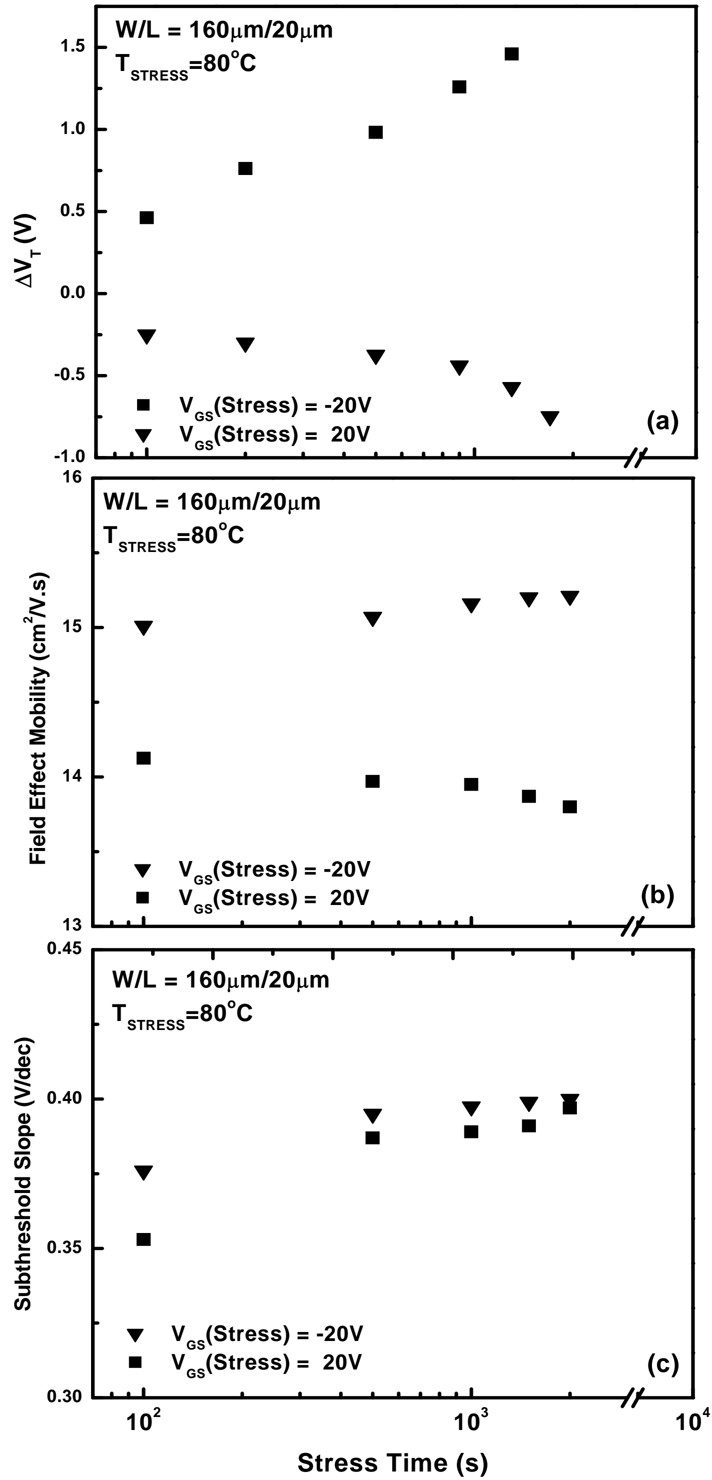


Fig.3.7 (a) ΔV_T, (b) μ_{FE}, (c) SS of NBT and PBT stressed N_2O treated a-IGZO TFTs (W=160μm, L=20 μm) as a function of stress time (t_{STRESS}).

3.5.2 Electrical Properties of a-IGZO TFT with BTS

The time evolution of device degradation was monitored by interrupting the BTS at fixed time periods. The duration of the total bias stressing was 2000 s for this particular study. Fig. 3.7(a)-(c) show the key TFT parameters, ΔV_T, μ_{FE}, SS observed as a function of stress time (t_{STRESS}) during the NBTS and PBTS experiments at 80°C with the gate bias V_{GS}=-20V/20V for N_2O plasma treated case. We held V_{DS}=20V to precisely probe the subthreshold properties of the a-IGZO TFTs. The ΔV_T is calculated as the difference between threshold voltages at each stressing time step and the initial values of the same before each BTS experiment ($V_{T_initial}$). The results indicate that during circuit operation involving a-IGZO TFTs, both positive and negative clock cycles can cause change in electrical properties of the TFTs and warrant careful circuit design paradigm to account for these shifts. When compared to as-deposited devices, the degradation due to NBTI was worse than that compared to PBTI. Severe ΔV_T has been reported for a-IGZO TFTs under NBTS both in ambient light and UV illumination conditions and the degradation mechanisms have been attributed to subgap density of state generation and subsequent field-assisted trapping in as deposited and unannealed TFTs [3.34]. As such we decided to further investigate the ΔV_T with time and temperature under NBTI.

3.5.3 Suppression of NBTI of N_2O Treated a-IGZO TFT

Fig. 3.8(a)-(b) shows the typical results observed during the NBTS experiments at 80°C with V_{GS}=-20V for both as deposited and N_2O plasma treated case. TFTs which were not subjected to post- processing N_2O plasma treatment exhibited uniform negative ΔV_T shift for both ON and subthreshold regions in a-IGZO TFTs. For the N_2O treated devices, the

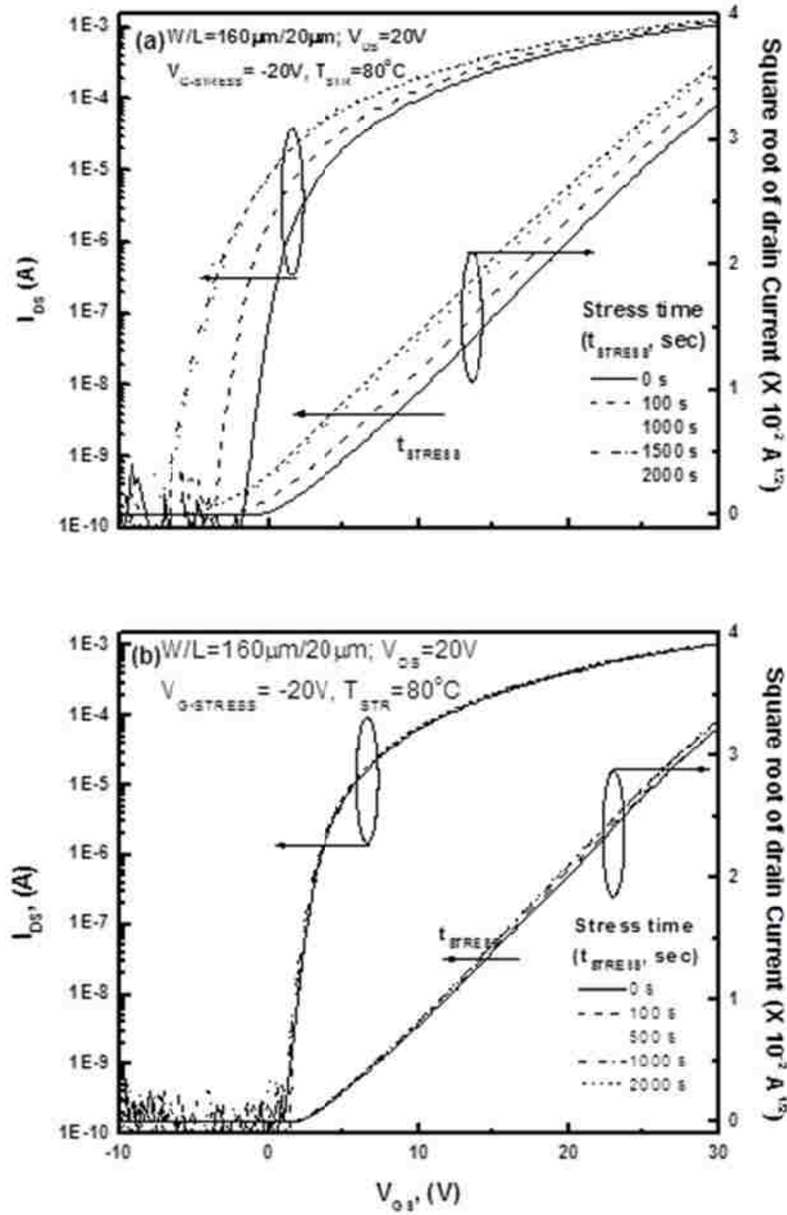


Figure 3.8. Time evolution of a-IGZO TFTs with -20 V V_{G_stress} @ 80ºC; (a) as-deposited a- IGZO TFT and (b) N_2O plasma treated IGZO TFTS.

ΔV_T is still discernible albeit very small. The above results indicate that the creation of additional trapping states at the interface of channel/dielectric layers due to bias stressing is negligible and that the ΔV_T is primarily due to the traps located at the interface or in the bulk semiconductor region.

In a-Si:H TFT, deep-gap states originate from rather weak Si-dangling bonds. The subthreshold swing in such devices can be associated with the density of deep bulk sates (N_{BS}) and interface states (N_{SS}) density at the semiconductor/channel region by the following equation [3.35]:

$$SS = \frac{kT}{q\log(e)}\left[1 + \frac{qd_{ins}}{\varepsilon_{ins}}\left(\sqrt{\varepsilon_{semi}N_{BS}} + qN_{SS}\right)\right] \tag{3-2}$$

where k (Boltzman constant), T (temperature), and q (electric charge) are the usual physical parameters; ε_{ins} and ε_{semi} are permittivity in the insulator and semiconductor, respectively; d_{ins} is the effective thickness of the insulator. If this conjecture holds true for a-IGZO TFT, the bulk states of the a-IGZO active layer can be estimated by considering a sole contribution from bulk states in (3-2) (by setting N_{SS}=0). Biasing the TFT can cause the amorphous Si network to be unstable and the network can rearrange to break the Si-Si bonds [3.23]. However, in a-IGZO, instead of the hybridized sp^3 orbitals, carriers are conducting through metal cation's ns-orbitals with large inter M-O (metal-oxide) overlap [3.30]. Such mechanism presumably allows a-IGZO to have a high immunity to dangling bond creation and maintain a low density of deep-gap states. Fig. 3.9 (a) illustrates the time evolution of bulk state density and characteristic temperature of the conduction-band-tail-states (T_G). A high T_G in a-Si:H network commonly correlates to a high density of band-tail states and non-ideal film quality [3.35].

As shown in Fig 4.9 (a) and (b), both the bulk-state and interface trap state density are higher in the as- deposited a-IGZO films whereas they are substantially reduced for the N_2O plasma treated case. The variation of kT_G is very small and is fairly close to 25 meV in the latter case. This indicates that once the a-IGZO TFTs are subjected to the

N_2O plasma treatment, the conduction band-tail remains largely unaffected even with longer bias stressing.

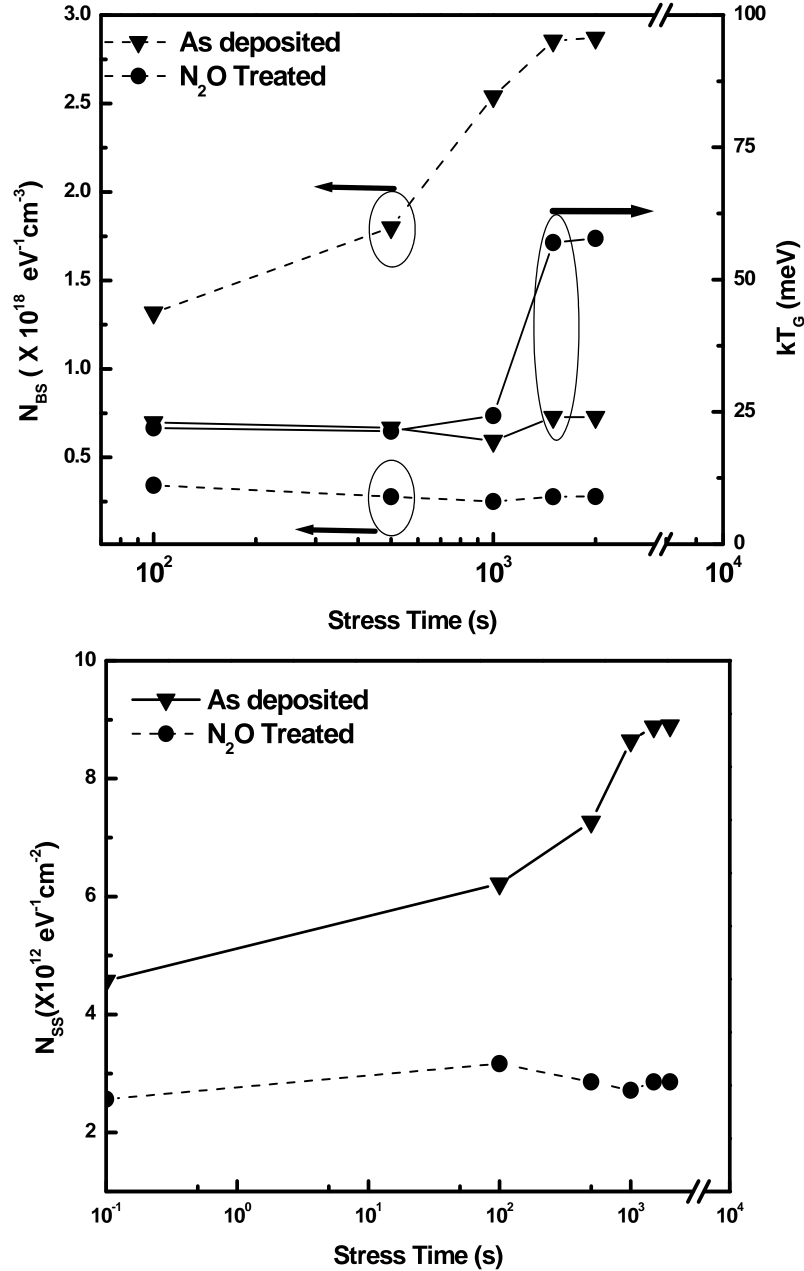


Figure 3.9. (a) Density of bulk-states (N_{BS}) and characteristic temperature (kTG) of conduction-band-tail states and (b) interface density (N_{SS}) states in as-deposited and N_2O plasma treated a-IGZO TFTs.

3.6 Stretch-Exponential Model for N_2O treated a-IGZO TFT

To better understand the physics of NBTS induced degradation in a-IGZO TFT, we performed a numerical analysis based on the stretched-exponential model commonly used for a-Si:H TFTs. The model, which was originally developed for a-Si:H TFTs based on charge injection/ trapping concept [28], is expressed by the following equation:

$$|\Delta V_T| = |\Delta V_O|^{\alpha}\left\{1-\exp\left[-\left(\frac{t_{stress}}{\tau}\right)^{\beta}\right]\right\} \tag{3-3}$$

where, $$\Delta V_O = V_{G_STRESS} - V_{T_initial} \tag{3-4}$$

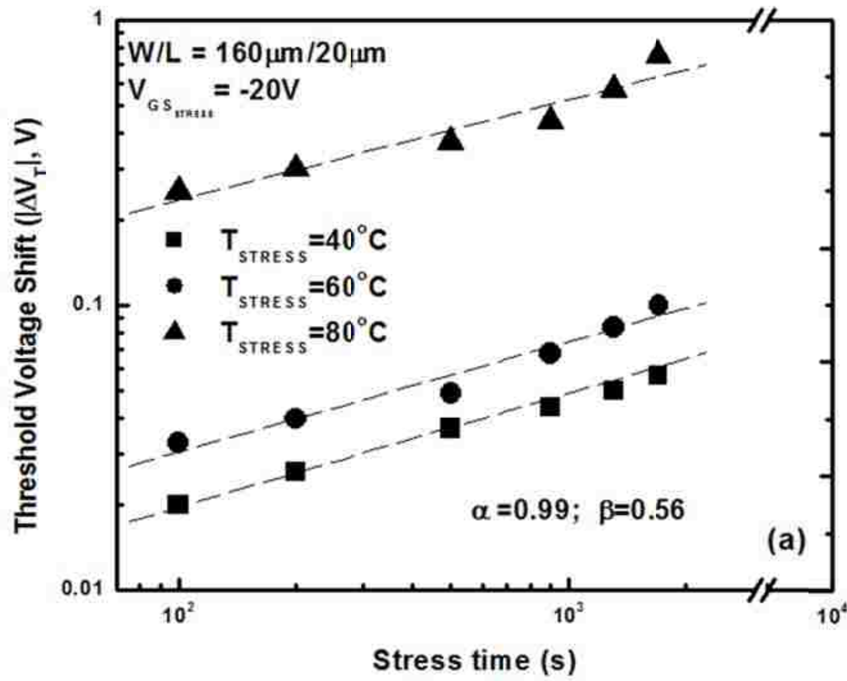
and $$\tau = \tau_o \exp\left(\frac{E_\tau}{kT_{STRESS}}\right) \tag{3-5}$$

In the above equations, ΔV_o is the effective voltage drop across the gate insulator, $\Delta V_{T_initial}$ is the initial threshold voltage; α is the fitting parameter for ΔV_o dependence and β is the stretched exponential factor. The τ represents the characteristics trapping time and E_τ in (3-3) is the average effective energy barrier that carriers in conducting channel needs to overcome before they can enter the insulator or near interface region, with τ_o being the thermal pre-factor for emission over barrier. For a very short stress time ($t_{STRESS} << \tau$), (3-3) can be further shortened as -

$$|\Delta V_T| \cong \Delta V_O^{\alpha}\left(\frac{t_{STRESS}}{\tau}\right)^{\beta} \tag{3-6}$$

This is a straightforward power law dependence of β of t_{STRESS} and has been applied to model BTS data [17-18]. On the other hand, for infinite stress time, (3-3) will give a saturated behavior with $\Delta V_T \rightarrow (\Delta V_o)^{\alpha}$. Both logarithmic and stretched-exponential time dependence models were derived to qualitatively describe ΔV_T in a-Si:H TFTs based on the charge trapping mechanisms. However, the logarithmic time dependence assumed no further redistribution of the charges trapped at the interface deeper into the the bulk-dielectric, whereas the stretched-exponential time dependence hypothesized the emission of trapped charges toward deep states in the bulk dielelectric [3.26]. It is also plausible that the amorphous structure of the gate dielectric will lend itself to an appreciable number of band-tail states which can act as transport states for the emitted lower energy trapped state charge [3.26]. The extent this can happen depends on the type of dielectric and active layer used and also on deposition and processing conditions.

Fig 3.10 (a) and (b) show the time dependence of ΔV_T with different temperature ranges (40°C-80°C) to demonstrate the applicability of stretched-exponential model for describing N_2O treated a-IGZO TFTs. For even lower temperatures, the ΔV_T is too small (few mV) to make reliable analysis within the BTS time range (2000s) chosen in this study. The model fits well with the experimental data (dashed lines are numerical fits to model) with α and β determined to be 0.99 and 0.56 respectively. The α is determined from the $\log(|\Delta V_T|)$ vs $\log(|\Delta V_o|)$. For comparison purposes we also repeated the BTS values from PBTS measurements with positive V_{GS_STRESS} =20V and obtained α and β values of 1.02 and 0.71 respectively. The extracted α for PBTS (1.02) is larger than the one extracted for NBTS (0.99) which is indicative of a-IGZO TFT's sensitivity to the



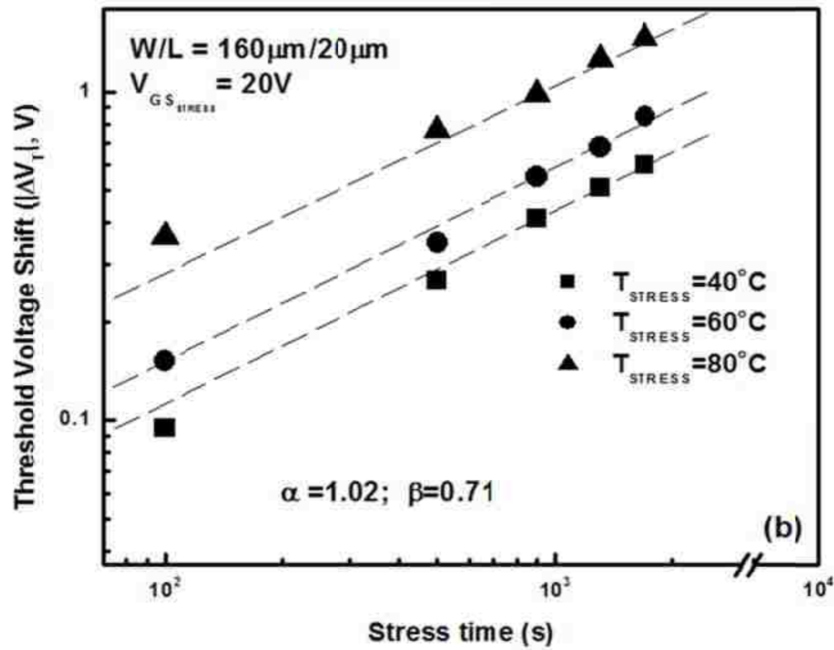


Figure 3.10 ΔV_T evolution with time at different T_{STRESS} ranging from 40ºC-80 ºC (a) NBTS (b) PBTS; Symbols represent experimental data while dashed lines are numerical fit to stretched-exponential model.

polarity of bias stress. The characteristic trapping time, τ, is treated as fitting parameter and plotted as a function of $1/kT_{STRESS}$ in Fig. 3.11. for both PBTS and NBTS on N_2O treated a-IGZO TFTs. Table 4.2 summarizes all the parameters used in the stretched-

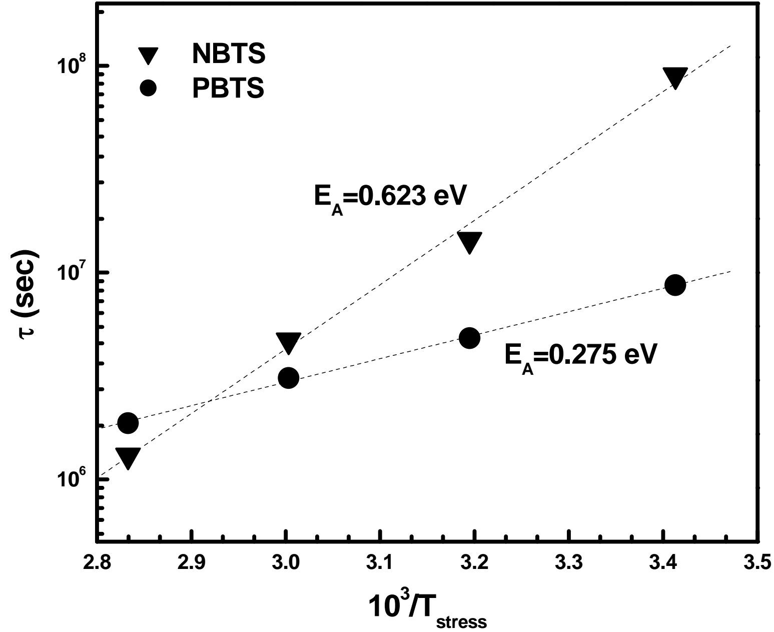


Figure 3.11. Characteristic trapping time, τ, for both NBTS and PBTS plotted against $1/T_{STRESS}$ (from 20ºC-80 ºC).

exponential model. The extracted $E_A=E_\tau$ for positive bias temperature stress, BTS (0.275 eV) is smaller than the value of negative BTS (0.623 eV). This suggests that the electrons experience a lower energy barrier than holes do during the charge injection process near the a-IGZO/SiO_2 interface. Electron injection is very efficient and can quickly fill out the available states which in-turn increases the chance for re-emitting these filled states [3.36]. As a result, the characteristic trapping time for positive BTS to reach the saturation point is lower than that of negative BTS. Although the fitting is prone to errors

due to short stress times and small ΔV_T variation in N_2O plasma treated a-IGZO devices, the stretched-exponential model is able to give us a trend seen from the experimental data. The model seems to work even with different magnitude of the stress voltage, BTS polarity and varied stress temperatures. This implies that the carrier injection from conducting channel and the subsequent charge trapping plays an important role in the a-IGZO TFT BTS instability.

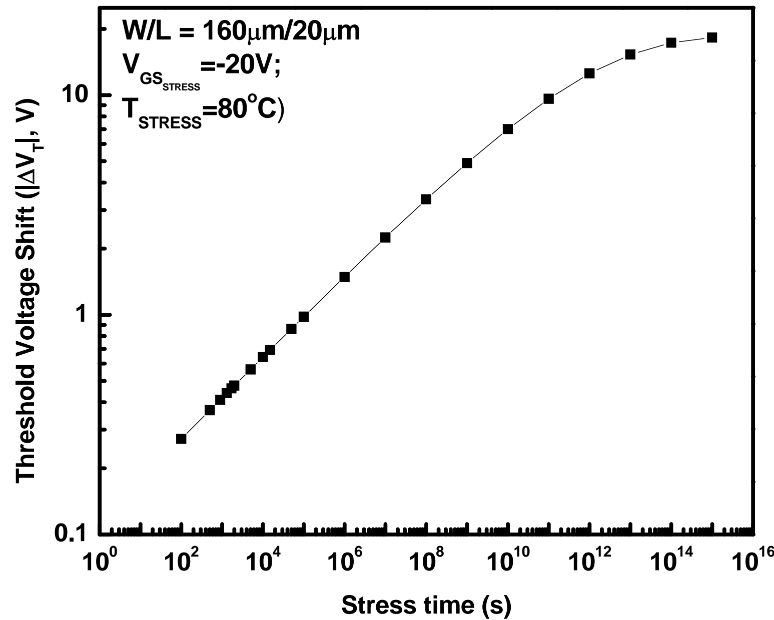


Figure 3.12. Simulated ΔV_T vs. t_{STRESS} for NBTS (-20 V, 80ºC) of N_2O treated a-IGZO TFT; refer to Table 3.2 for the simulation parameters.

The stretched-exponential model predicted ΔV_T for relatively short stress time; however, we did not observe a strong saturated behavior expected for longer stress times. To see if we get saturated behavior of $\Delta V_T \rightarrow (\Delta V_o)^{\alpha}$ for infinite t_{STRESS} we simulated the ΔV_T over a long stress time (10^{15} sec). Fig 3.12 shows that for negative bias stress of -20 V, the

simulation predicts a saturation knee at $t_{STRESS} > 10^{14}$ sec with $\Delta V_T \approx 10$ V and $\Delta V_T < 5$ V at a stress time around 10^9 sec. indicating long term device stability with N_2O plasma treatment of a-IGZO TFTs.

Table 3.2: Stretched Exponential Model Fitting Parameters for NBTS and PBTS of N_2O Treated a-IGZO TFTs

Stretched Exponential Model Parameters	NBTS (V_{GS_STRESS} = -20V)	PBTS (V_{GS_STRESS} = 20V)
α	0.99	1.02
β	0.56	0.71
E_A(eV)	0.623	0.275

3.7 Conclusion

In summary, we have investigated the negative-bias-temperature stress induced instability in a-IGZO TFTs. Through the post IGZO N_2O plasma treatment, the stress instability improves remarkably which indicates the importance of post IGZO process for robust pixel and driver circuitry operation. The function of the N_2O treatment is believed to not only passivate the interface states but also homogenize the relatively poor quality sputter deposited IGZO films to a more high quality film by reducing the sub-gap defect state density. The stretched–exponential equation models well the instability in treated a-IGZO TFTs and further simulation dictates long term stability in N_2O treated a-IGZO devices.

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Chapter 4

Threshold Voltage Stability of N_2O Treated Amorphous IGZO Thin Film Transistors on Flexible Metal Substrates Under Constant Current Temperature Stress

4.1 Introduction

From a reliability standpoint, a critical issue for future large area active matrix organic light emitting diode (AMOLED) display applications is the threshold voltage stability in thin film transistors (TFTs) under constant current stress operating conditions because of the current driven nature of the OLED devices [4.1-4.3]. The driving scheme in a typical AMOLED device comprising of two TFTs (namely the switching TFT, i.e. Sw-TFT, and the driving TFT, i.e. Dr-TFT), one storage capacitor (C_{st}) and an OLED is depicted in Fig. 4.1. The switching TFT (Sw-TFT) needs to adequately charge the storage capacitor to a desired voltage level during a short scanning time (T_{scan}); therefore, the gate voltage (V_{GS}) has to be held at a relatively high voltage but the drain voltage (V_{DS})

does not. The driving TFT (Dr-TFT) on the other hand has to precisely supply a desired current to the OLED during a long light-emitting time period (T_{emit}). Since a constant I_{OLED} current has to be maintained, the drive TFT must be operated in the saturation mode where the V_{GS} is tied to V_{DS} in a diode-connected fashion. This is the preferred method of operation particularly in current-programming schemes [4.4]. During constant gate bias stress, the channel charge and hence the on current continuously decreases to eventually saturate the threshold voltage shift [4.5]. In the constant current stressing mode (Dr-TFT in diode connected mode) the V_{GS} continuously adjusts to compensate for the shift in threshold voltage (ΔV_T) to maintain a constant drain current (I_{DS}). Due to this time varying nature of the gate voltage, prediction of ΔV_T is complicated and warrants further investigation.

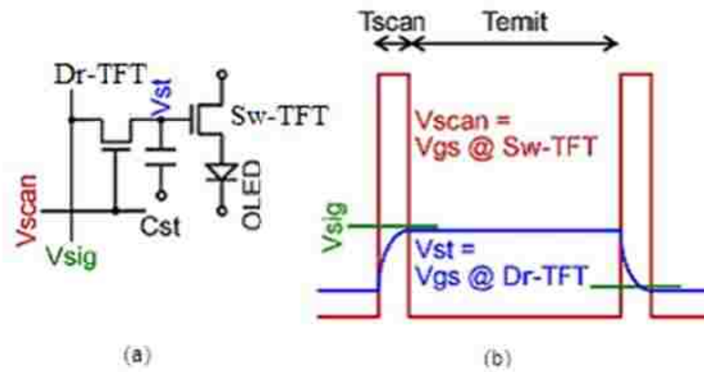


Figure 4.1 Circuitry and driving method of a typical AMOLED display; (a) Pixel circuit, (b) Programming Voltages.

Hydrogenated amorphous silicon (a-Si:H) and low temperature poly-crystalline silicon (LTPS) based TFTs are mainstay in typical current driven active-matrix display applications. Poly-Si TFTs have high mobility and exhibit relatively better ΔV_T stability

but non-uniformity of other electrical characteristics due to presence of grain boundaries is an outstanding issue [4.6]. On the other hand, a-Si:H TFTs show highly uniform electrical properties over large area but suffers from inherent meta-stable effects due to the long range disorder in the a-Si:H matrix[4.7]. Based on the understanding that has been developed for a-Si:H/Si_3N_4 TFTs [4.8-4.10], bias stressing may lead to instabilities such as charge trapping and possibly defect formation in the semiconductor channel, in the gate dielectric, or at the dielectric/semiconductor interface. Also an increased temperature and stringent stressing environment could lead to enhanced or additional instabilities. In the inverted-staggered bottom gate a-IGZO devices under investigation, the back-channel surface conduction can be an additional pathway to degradation due to interaction with the ambient. The encapsulation or passivation of the a-IGZO surface to reduce the interaction with the ambient would be expected to have an impact on the operation and stability of the bottom gate devices. All these instability mechanisms over a period of time are bound to manifest themselves in a time-dependent operation. Studies investigating the electrical stability of a-IGZO TFTs have been reported [4.11-4.16], and a parallel shift in TFT transfer characteristics when subject to either constant bias or current stress is commonly observed, and several possible degradation mechanisms have been put forth. Nomura et al. [4.16] suggested that shallow traps are the origin of subthreshold slope deterioration and ΔV_T in unannealed and non passivated a-IGZO TFTs devices, while deep charged traps which cannot be removed by annealing are responsible for small ΔV_T [16]. On the other hand, Lee et al. [4.11] and Suresh et al. [4.12] attributed the instability to charge trapping in the channel/dielectric interface or in

the bulk dielectric layer. This chapter addresses experimental results of the stability of N_2O treated a-IGZO TFTs that are electrically stressed with different constant currents in a wide temperature range. The goal is to investigate factors affecting the degradation including stress time, stress current, stress temperature, and TFT biasing conditions.

4.2 Experiments for Current Temperature Stress Study

Constant current temperature stress (CCTS) measurements were performed on N_2O treated a-IGZO TFTs. The a-IGZO TFT device has a staggered, bottom-gate architecture with the back channel passivation. The TFTs are fabricated by first depositing 150 nm of Mo by RF sputtering onto SiO_2 passivated 6 inch steel wafers and lithographically patterning and wet etching to form the gate layer. A 100 nm thick SiO_2 is then deposited by PECVD at 300°C. This is the maximum process temperature in the entire fabrication sequence. Then a 70 nm of a-IGZO thin film is deposited by RF sputtering from a 6-inch diameter commercially available IGZO target (1:1:1 molar ratio In_2O_3:Ga_2O_3:ZnO). The optimized a-IGZO active layer is patterned by wet etching in dilute HCl. After patterning, the IGZO active area is subject to N_2O plasma treatment in PECVD chamber at 100 W for 5 minutes. Contact openings to the gate pads are accomplished by lithography and selective etching of the oxide layer. Finally, Mo source and drain metallization is done by RF sputtering and subsequent lift-off.

For the devices undergoing CCTS studies, the measurements were done in the lab ambient and in light-tight conditions using a Hewlett-Packard 4145B semiconductor parameter analyzer with probes for low-noise, high-current sensitivity measurements.

The current-voltage measurement was automated by a Lab-View software controlled program. The device temperature was regulated by a heated chuck and a digital temperature controller and monitor. Before each measurement, the TFTs were placed on the heated chuck which was stabilized at the desired measurement temperature to allow for thermal equilibrium. Two different biasing conditions, namely linear and saturation mode were employed during the CCTS measurements which corresponded to operating the TFT in the linear and saturation regime, respectively. In the linear stress mode, the V_{GS} was held at 20 V while a constant stress current (I_{STRESS}) was applied to the drain of the TFT, as shown in Fig. 4.2(a). The stress condition was interrupted at predetermined time steps (t_{STRESS} = 100s, 200s, 500s, 900s, 1300s, 2000s), to obtain the transfer characteristic of the a-IGZO TFTs in the saturation regime (V_{DS} = 20V) by sweeping V_{GS} from -5 V to -20 V in 0.25 V increments. In the saturation stress mode, the TFT was biased in the diode-connected configuration with V_{GS} tied to V_{DS} as is shown in Fig 4.2 (b) which allows on-line monitoring of the V_{GS} with stress time evolution. In this case,

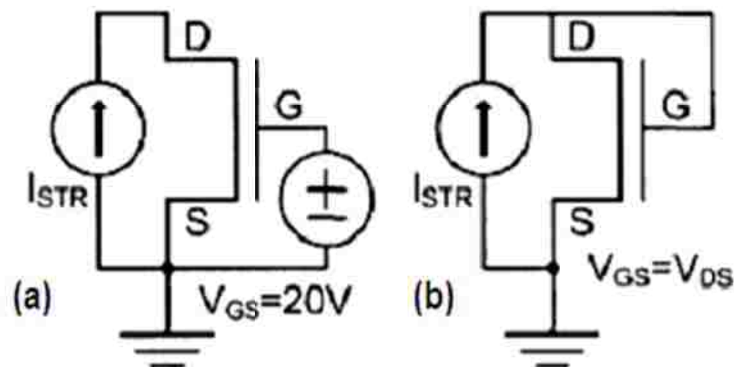


Figure 4.2 a-IGZO TFT biasing condition during constant current stress measurement: (a) Linear current stress Mode (V_{GS}=20 V); (b) Saturation stress mode (V_{GS}=V_{DS}).

Table 4.1: Constant current stress conditions

	Stress Biasing Condition	I_{STRESS} (μA)	T_{STRESS} (°C)
Linear Stress Mode	$I_{DS}=I_{STRESS}$	20	40, 60, 80
	V_{GS} = 20V	20, 50, 100	60
Saturation Stress Mode	$I_{DS}=I_{STRESS}$	100	40, 60, 80
	$V_{GS} = V_{DS}$	50, 100	60

the change in V_{GS} is solely due to and equal to the ΔV_T [4.17]. As mentioned before, the V_{GS} adjusts to maintain the $I_{DS}=I_{STRESS}$ unchanged. The total stress time and number of points when the stress mode was interrupted are the same as in the linear mode. The transfer characteristics was obtained by sweeping V_{GS} from -5 V to-20 V withthe TFT

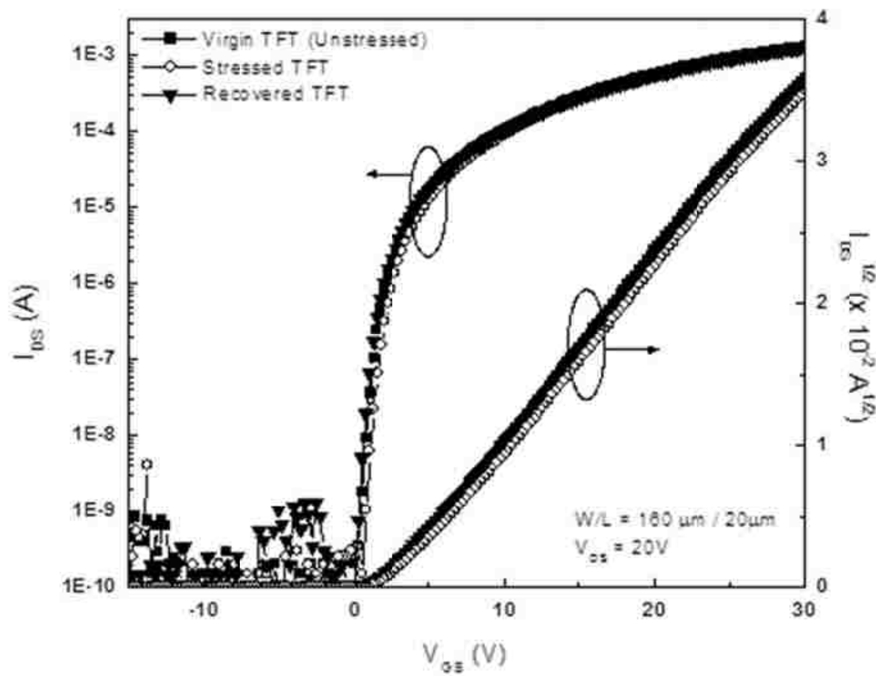
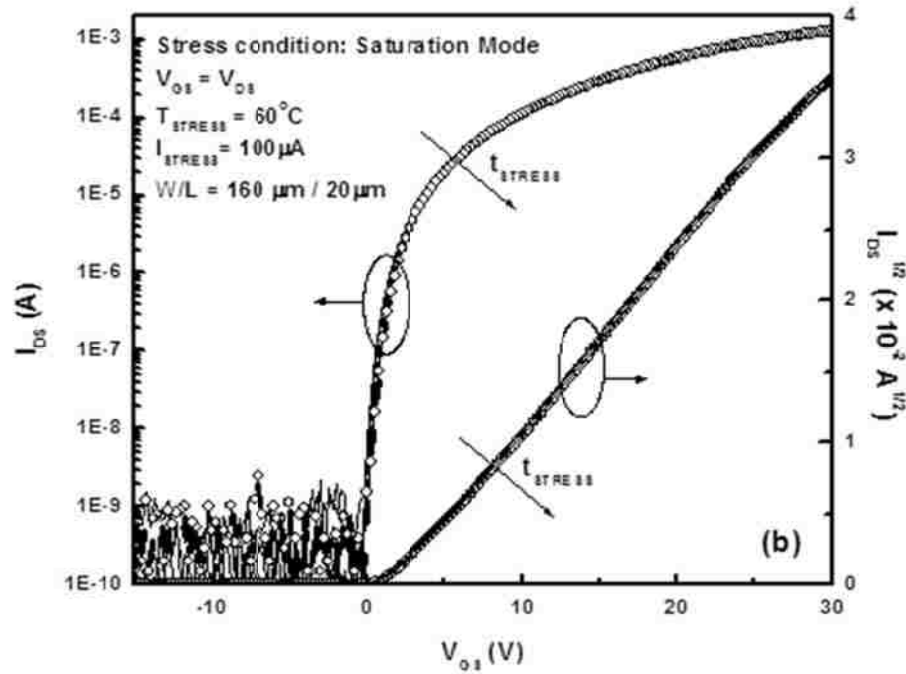


Figure 4.3 a-IGZO TFT (W=160μm, L=20μm) transfer characteristics before and after CCTS, after 2000s of CCTS stress and recovered state after 10 min thermal annealing post-stressing.

still in the diode connected mode ($V_{GS} = V_{DS}$) so as to mimic the driving scheme in a typical AMOLED application. The measurement sequence described above was repeated for several levels of stress current (I_{STRESS}) and stress temperature (T_{STRESS}) for both CCTS setups. Table 4.1 summarizes the CCTS conditions used. For both CCTS setups, after the 2000s CCTS stressing, the TFT was subjected to N_2 furnace anneal at 100°C for 10 minutes to almost recover to virgin state (unstressed), as shown in Fig. 4.3.

4.3 Electrical Properties of N_2O Treated a-IGZO TFTs after CCTS

Electrically stressing the a-IGZO TFTs at elevated temperatures and different stress current levels and evaluating the behavior of the ΔV_T should provide significant insight into the instability mechanisms of these devices. In this section, we will discuss the time evolution of ΔV_T of our N_2O treated a-IGZO TFTs with varying temperature and stress current levels. Fig. 4.4(a) and (b) show the transfer characteristics of N_2O treated a-IGZO TFTs in linear and saturation current stress modes respectively. A rigid positive ΔV_T is evident in both stress modes. The CCTS linear was performed at T_{STRESS} = 60°C with V_{GS} held at 20V, at a stress current level of I_{STRESS} = 20μA. At this specific level of stress current, V_{DS} was measured to be around 0.7V, which corresponds to the linear regime of TFT operation. The CCTS saturation was performed at T_{STRESS} = 80°C with the gate and drain tied together, and at a stress current level of I_{STRESS} = 100 μA, which sets $V_{GS} = V_{DS}$ to be 9.6V. The threshold voltage (V_T), field effect mobility (μ_{FE}) and the subthreshold slope (SS) of the unstressed N_2O treated a-IGZO TFTs are 1.52 V, 15.41 $cm^2/V.s$ and 400 mV/dec respectively; after 2000s of CCTS, these values are 3.14 V, 15



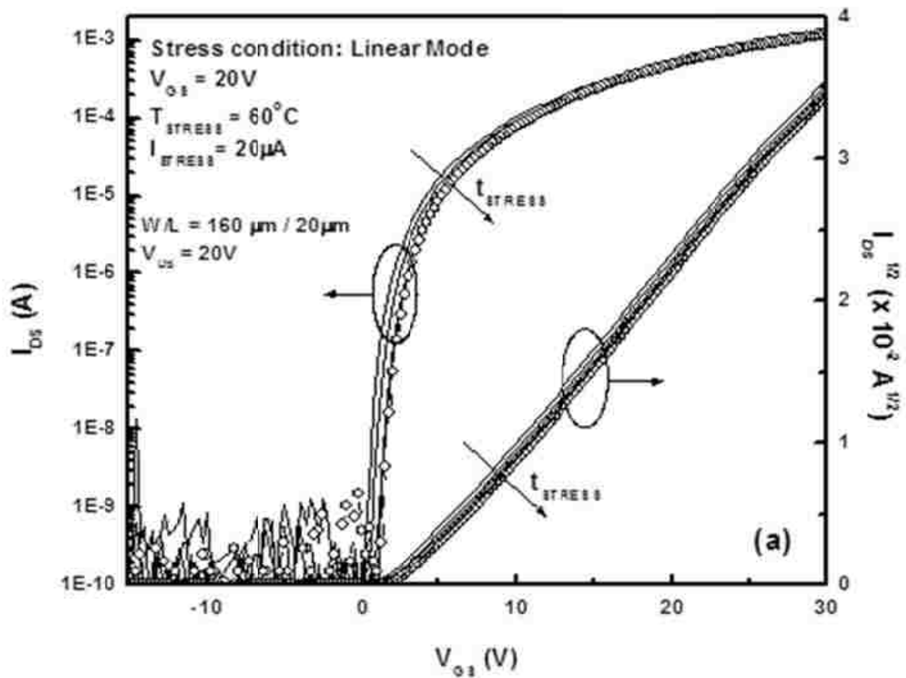


Figure 4.4 Effect of constant current stress on transfer characteristics of N_2O treated a-IGZO TFT (W=160µm, L=20µm); (a) Stress in linear mode and (b) Stress in saturation mode.

$cm^2/V.s$ and 460 mV/dec in the linear mode and 2.1 V, 15.25 $cm^2/V.s$ and 432 mV/dec in the saturation mode respectively. As we can see from Fig. 4.4, even after suffering these strict CCTS conditions, the TFT off-current remained almost the same while there was only a slight degradation in subthreshold slopes and negligible decrease in the field effect mobility slightly (1-2%). The ΔV_T is < 2V (~0.5 V in saturation mode) which is remarkable when compared to a-Si:H TFTs subject of similar stress conditions (for example, is $\Delta V_T > 5V$ for 15µA of constant current stress at 75°C) [4.18].

4.4 Effect of Stress Temperature on ΔV_T of N_2O Treated a-IGZO TFTs

To understand the origin of instability in a-IGZO TFTs under constant current stress, it is imperative to investigate the temperature dependence of ΔV_T since some of the degradation mechanisms may be temperature mediated. In order to ascertain the exact kinetics of instability, we performed measurements for both CCTS setups at stress temperatures (T_{STRESS}) ranging from 40°C to 80°C in 20°C steps. The time duration for stress is defined as t_{STRESS}. The stress currents are 20µA and 100µA for linear and saturation mode of stressing respectively. A stress current level of 20µA is deemed adequate since it is comparable to the maximum drive current of a 15" XGA full color AMOLED display [4.19]. As is evident from Fig 4.4, a much higher current stress level is required to have measurable ΔV_T in the saturation (diode connected) mode since we observed that the TFTs are electrically more stable when stressed under CCTS saturation mode as opposed to CCTS linear mode for the same I_{STRESS} level.

The device degradation is defined as the change in threshold voltage

$$\Delta V_T = V_T\,(t = t_{STRESS}) - V_T\,(t = 0) \qquad (4\text{-}1)$$

V_T, which was extracted by drawing a line to V_{GS} axis from the intersection point of transconductance (g_m) and $\frac{\partial g_m}{\partial V_{GS}}$ plots for unambiguous determination of V_T. The change of density of interface trap states (ΔD_{it}) with stress was negligible as seen from Fig 4.5 for both linear and saturation mode of current stress. The ΔD_{it} can be found by the change in subthreshold slopes before and after stress by the following relation

$$\Delta D_{it} = \frac{C_{ox}}{\ln(10) q^2 k_B T}\left(SS_{t_{STRESS}} - SS_{t0}\right) \qquad (4\text{-}2)$$

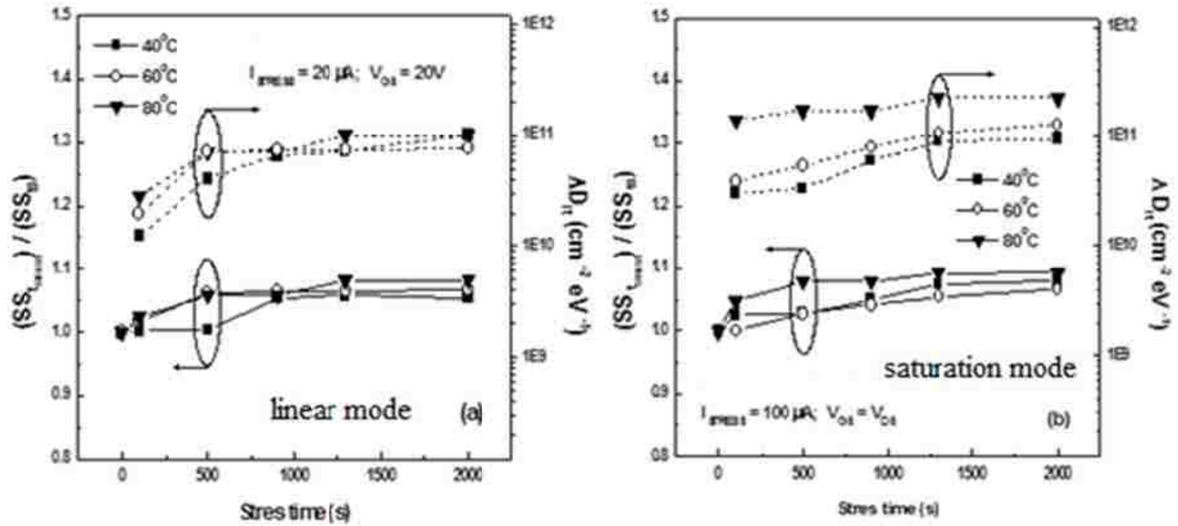


Figure 4.5 ΔD_{it} and Normalized Subthreshold values of a-IGZO TFTs (W=160μm, L=20μm) under constant current stress at 40°C, 60°C and 80°C; (a) linear stress mode and (b) saturation stress mode.

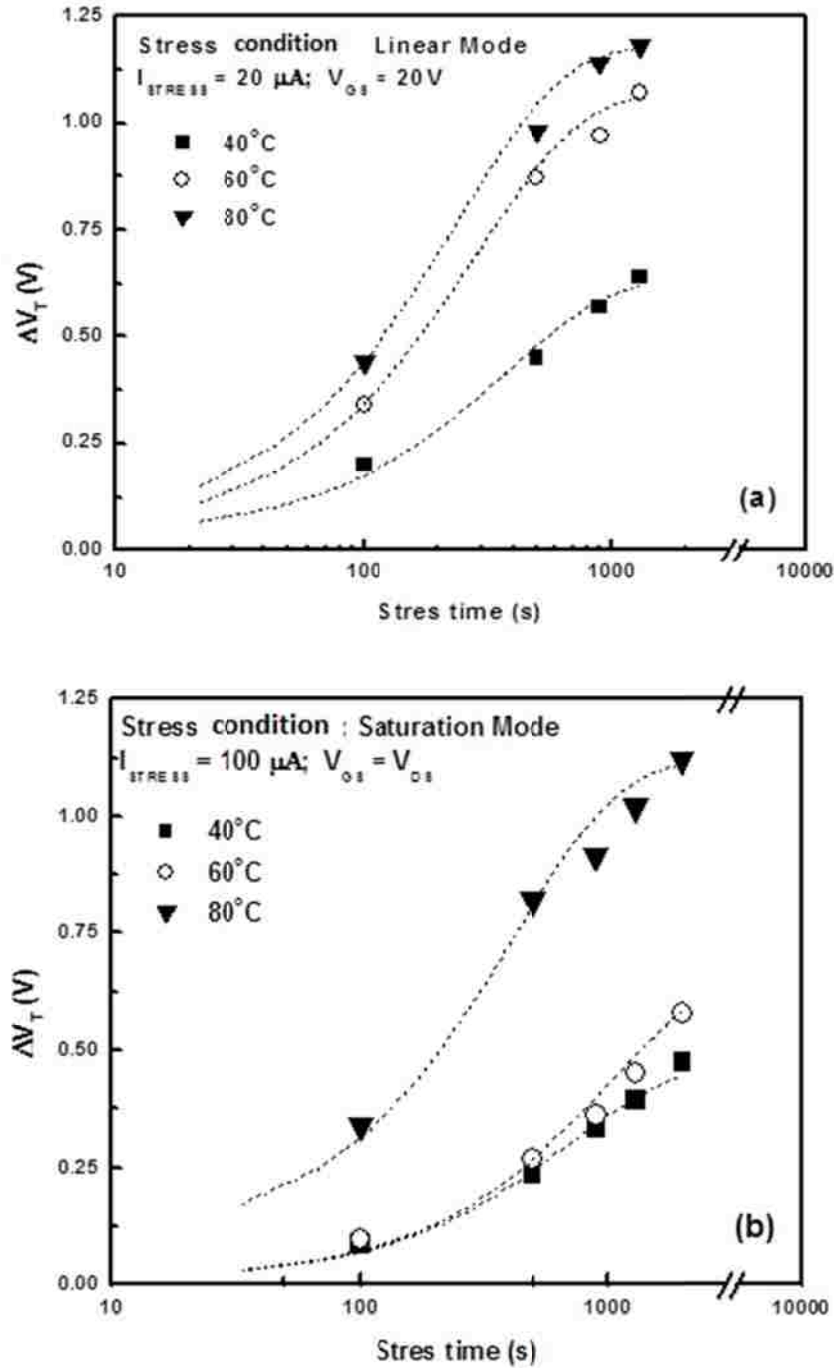


Figure 4.6 ΔV_T evolution with time of a-IGZO TFTs (W=160µm, L=20µm) under constant current stress at 40°C, 60°C and 80°C; (a) linear stress mode and (b) saturation stress mode. Symbols are experimental data; dashed lines are stretched exponential model described by equation (4-4).

Fig. 4.6(a) and Fig. 4.6(b) show typical temperature dependences of the a-IGZO TFT ΔV_T as a function of stress time for various T_{STRESS} under CCTS linear and saturation mode. There is a very small but discernible temperature dependence of ΔV_T for both CCTS setups, with a stronger dependence in the linear mode of stress. The ΔV_T increased by raising the stress temperature. Slight degradation of subthreshold slope is noticeable at larger temperature stress possibly attributed to secondary instability such as field induced interface state creation.

4.4.1 Thermalization Energy Concept of ΔV_T: Absence of Defect State Creation in N_2O Treated a-IGZO TFT

A common practice to compare the stability of different TFTs has been to evaluate their ΔV_T over time at varying temperature range to mimic more stringent bias stress conditions. A model that correlates the effect of stress temperature and stress time is based on thermalization energy developed for a-Si:H TFTs by Deane et al. [4.20]. They combined time and temperature variables with a new parameter, thermalization energy as defined as $E_{th} = k_B.T_{STRESS}.\ln(\nu.t_{STRESS})$ which signifies that after a time of t_{STRESS} at a stress temperature of T_{STRESS}, all defect creation sites with energy less that E_{th} would have converted to defects [20]. It has been shown that ΔV_T plotted as a function of E_{th} for different temperatures overlay perfectly with a single fitting parameter, the attempt-to-escape frequency, ν. In a-Si:H TFTs, ν has been shown to be 10^{10} Hz as reported by several research groups [4.21]. It seems that ν is unique to defect state creation, and it

has been attributed to the probability of an electron attempting to break weak Si-Si bonds [4.22]. If ν is smaller it means that electrons attempt to break weak Si-Si bonds less frequently and thus the rate of defect creation and ΔV_T are smaller. Therefore, the parameter v was considered as a figure of merit for device stability.

Using the kinetics of defect creation, it was shown that ΔV_T and E_{th} have the following relationship [4.20] with the parameters defined in reference 20:

$$\Delta V_T = C\left[1 - \frac{1}{(1 + \exp[(E_{th} - E_A)/k_B T_0])^{\frac{1}{\varepsilon}}}\right] \tag{4-3}$$

By fitting the experimental data of ΔV_T to (4-3), one can extract various parameters, including E_A, the energy barrier for defect state creation. By fitting the experimentally determined ΔV_T to (4-3) with fitting parameters $k_B T_0$ = 0.0309 eV and ε = 11.5, (experimentally determined from accumulation and depletion capacitance of high frequency IZO/IGZO/SiN_x/MoW structures) [4.23] along with the parameter C set at (V_{GS}-V_T) in the linear mode and 2/3($V_{GS}-V_T$) in the saturation mode, the energy barrier for defect state creation E_A can be extracted and has been found to be 0.6485 eV. The value of attempt-to-escape velocity, υ to ensure best overlap of ΔV_T-E_{th} was determined to be 1 MHz (10^6 Hz) which is the same as used in a previous study [4.24]. The resulting ΔV_T curve according to (4-3) and our experimentally determined curve is depicted in Fig. 4.7. Our measurement data shown in Fig. 4.7 for both linear stress mode and saturation stress mode, the measured ΔV_T is smaller than that predicted by (4-3). The above analysis

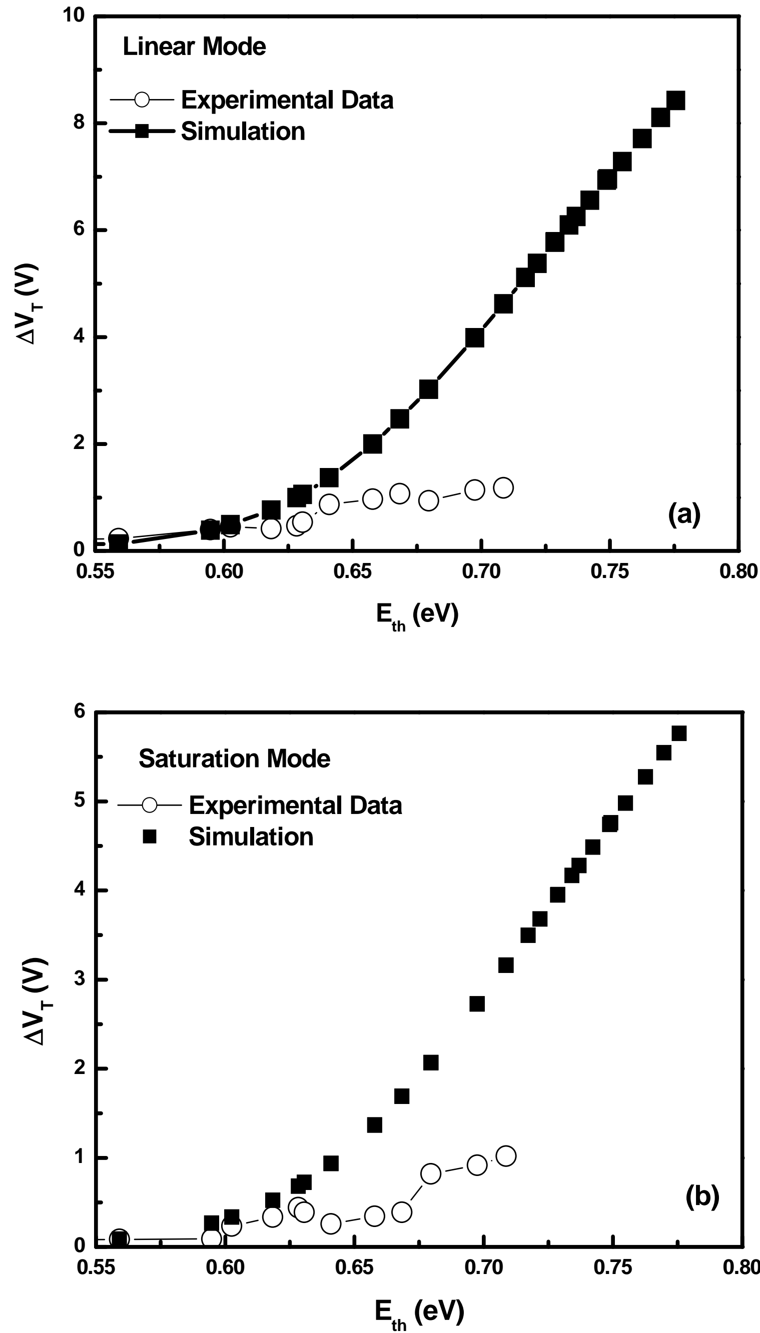


Figure 4.7 ΔV_T of N_2O treated a-IGZO TFTs (W=160μm, L=20μm) at different temperatures as a function of the thermalization energy. (a) linear stress mode and (b) saturation stress mode. Hollow symbols are experimental data filled ones simulation.

argues that there is only weak evidence of defect state creation and although ΔV_T shows relative temperature dependence. In nc-Si:H TFTs, such absence of defect state creation in the constant current stress mode has been reported [4.18] although it has been suggested that defect creation is possible at a higher value of E_A. These observations imply that defect state activation in our devices in the constant current stressing can only take place at much higher thermalization energies such as at higher temperatures and/or higher stress times.

In general, it is difficult to envisage a single degradation mechanism that explains the variation of both subthreshold slope degradation (SS) and ΔV_T since one or several mechanisms can be at play concurrently, depending on the material characteristics, quality of semiconductor-dialectic interface and bias stressing conditions. In our case, CCTS does not deteriorate the important TFT performance parameters such as field effect mobility and SS, but causes only the parallel shift of the transfer characteristics. These results suggest that extra defect states that affect the SS value are not generated in the N_2O treated a-IGZO TFTs by constant current stress. The SS value is very sensitive to subgap trap states around the Fermi level of a semiconductor channel and deteriorates by increase in the subgap trap density [4.25]. This cannot be explained only by the effect of temperature alone, rather increases of trap states by the heating must be considered. This suggests that the degradation process in the untreated a-IGZO TFTs is controlled by thermally activated mechanism. In the N_20 treated a-IGZO TFTs we argue that these subgap states are drastically reduced. In RF sputtered a-IGZO TFTs, it has been suggested that if acceptor like deep trap states are added as interface traps below the

Fermi level, these states are charged negative at V_{GS} above the turn-on voltage and can explain the positive ΔV_T [4.26]. A similar model is employed for a-Si:H TFTs with concurrent degradation of a SS value [4.27]. If the charged states are far deeper than E_F, the SS value should not be affected much by the increase in the trap density. In our study of our N_2O treated a-IGZO TFTs such deep state creation is retarded as N_2O treatment homogenizes the IGZO films.

4.5 Effect of Stress Current on ΔV_T of N_2O Treated a-IGZO TFTs

Increased current stress levels are also expected to manifest in larger ΔV_T of a-IGZO TFTs; therefore we performed CCTS measurements at various I_{STRESS} levels. In the linear mode, I_{STRESS} levels of 20μA, 50 μA, and 100μA and in the saturation mode 50μA and 100μA were applied. The stress temperature (T_{STRESS}) was fixed at 60°C. Current stress levels lower than 50 μA had a negligible shift in ΔV_T and as such we did not explore lower I_{STRESS} values in the saturation mode. Fig. 4.8 shows the time evolution of ΔV_T with a different stress current level in the linear and saturation modes. We can see that ΔV_T with time, becomes less dependent on stress current level when $I_{STRESS} > 20$ μA in the linear mode. This is not surprising since the V_{GS} was fixed at 20V for all levels of I_{STRESS} in the linear mode, therefore ideally the channel induced charge will remain almost the same as long as the TFT operates in the linear regime. On the other hand, in the saturation mode, ΔV_T-t_{STRESS} increases with I_{STRESS} levels and becomes independent of I_{STRESS} once normalized to the injected charge Q_{inj} (= I_{STRESS} x t_{STRESS}), as shown in Fig. 4.9. Q_{inj} is a commonly used parameter to evaluate the ΔV_T caused by trapped charge

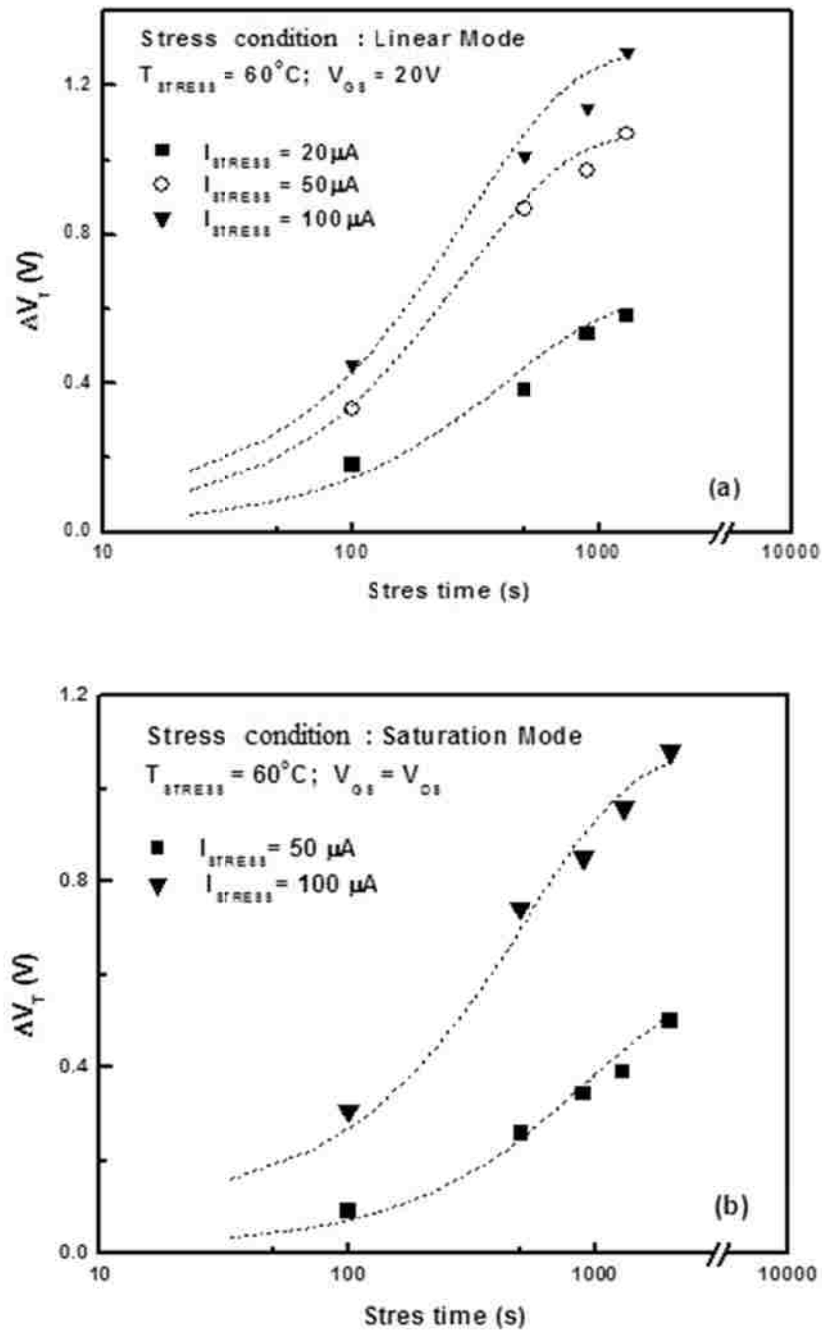


Figure 4.8 ΔV_T of N_2O treated a-IGZO TFTs (W=160μm, L=20μm) at different I_{STRESS} levels with time. (a) Linear stress mode and (b) Saturation stress mode. Symbols are experimental data; dashed lines are stretched exponential model given by (4-4).

in the gate dielectric for c-Si MOSFETs [4.28]. In the diode connected confirmation, the V_{GS} adjusts with I_{STRESS} levels, and therefore, at higher I_{STRESS} we have more channel induced charge at a higher V_{GS}. Due to a counteracting source-drain electric field, the carrier concentration closer to the drain is significantly lesser than that in the linear regime. Since the number of carriers getting trapped per time and unit area varies in

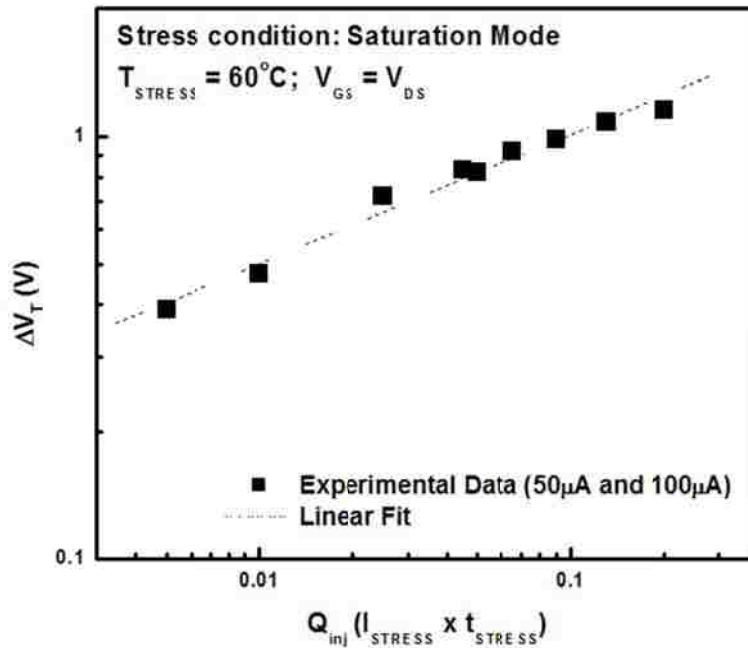


Figure 4.9 ΔV_T of N_2O treated a-IGZO TFTs (W=160μm, L=20μm) as a function of injected charge for 50μA and 100μA I_{STRESS} levels in saturation stress mode. Symbols are experimental data, dashed line is linear fit.

proportion to the induced charge, the decrease in channel charge closer to the drain may help explain the smaller ΔV_T shift under constant current stress. We conclude from our experimental results that for the same I_{STRESS}, the a-IGZO TFTs are electrically more stable when V_{GS} is smaller.

4.6 Physical Mechanisms of Instabilities in N_2O Treated a-IGZO TFTs Due to Current Temperature Stress

Under constant current stressing in the saturation mode, V_{GS} progressively increases to compensate for ΔV_T and thus $[V_{GS}(t)-V_T(t)]$ term remains constant over time. This is evident from Fig 4.10. Such compensation by V_{GS} implies that the position of the Fermi level at the a-IGZO/a-SiO_2 interface remains fixed and the band tail states are unchanged. In the case of a-Si:H TFTs under constant current stress, ΔV_T may increase indefinitely until the V_{GS} reaches the supply voltage or the density of weak bonds

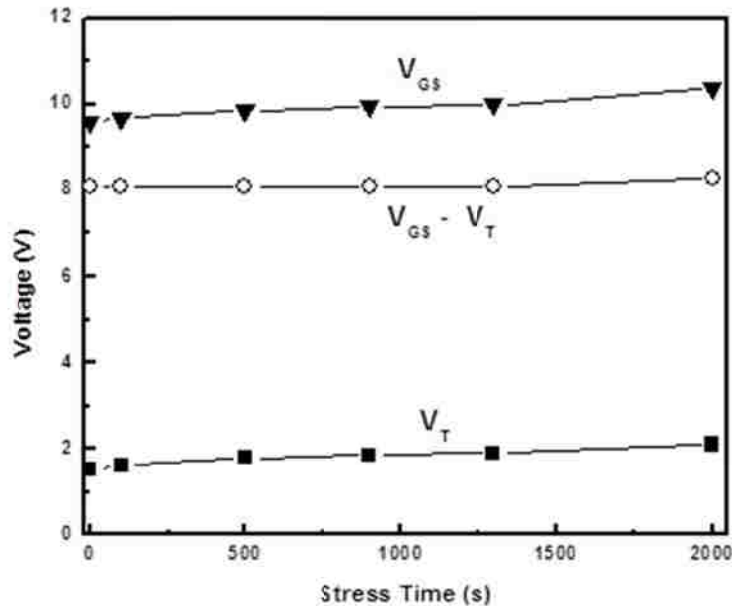


Figure 4.10 V_{GS}, V_T and Gate-overdrive voltage, V_{GS}-V_T, as a function of time in the saturation (diode-connected) current stress mode.

becomes a rate limiting factor. At higher stress voltages, defect state creation in a-Si:H was observed to be no longer dominant. In this case, Powell et al. [4.29] argued that ΔV_T is governed by charge injection from the channel into the gate dielectric interface without

subsequent redistribution of trap states in the bulk of silicon nitride (a-SiN_x) dielectric, and was to be a temperature independent process. Libsch and Kanicki [4.27] also argued that trapped carriers first thermalize in a broad distribution of band tail states at their channel/a-SiN_x interface and then move to deeper energy levels inside the a-SiN_x at longer stress times, higher temperatures and larger electric fields. In the latter case, the measured ΔV_T was highly temperature dependent. Based on our experimental data, we interpret our threshold voltage shift to be the result of charge injection from the a-IGZO channel into traps located at the a-IGZO/a-SiO_2 interface and in the gate insulator near the interface. The stretched exponential model based on charge injection/trapping was developed for a-Si:H TFTs [4.27]. The stretched exponential time dependence is generally used to explain the relaxation phenomena in disordered systems [4.30], but its origin in many materials is still under debate. In recent years, the stretched exponential model has been demonstrated to be applicable to metal oxides [4.31] and organic semiconductors [4.32] to give a phenomenological description of the stress behavior, irrespective of the underlying trapping mechanisms. The stretched exponential equation during the stress and recovery phases is defined as

$$\left|\Delta V_T\right| = \left|\Delta V_O\right| \left\{1 - \exp\left[-\left(\frac{t_{STRESS}}{\tau}\right)^{\beta}\right]\right\} \tag{4-4}$$

where, $\Delta V_o = [V_T\,(t = \infty) - V_T\,(t = 0)]$ is the maximum threshold variation; β ($0 < \beta \leq 1$) is the dispersion parameter reflecting the width of the involved trap distribution. In other

words, β represents the distribution of time constants that characterize the trapping process. The value of β closer to 1 depicts a narrow distribution, whereas $\beta < 1$ indicates a broader distribution of time constants. In terms of ΔV_T response, $\beta = 1$ depicts an exponential function, whereas $\beta < 1$ leads to a response slower than the exponential function (or becomes stretched) for times beyond the characteristic trapping time (τ) of carriers. The characteristics trapping time, τ in (4-4) is thermally activated and is given by

$$\tau = \tau_o \exp \left(E_\tau / k_B T \right) \qquad (4\text{-}5)$$

where, E_τ is the average effective energy barrier that the carriers in a-IGZO need to traverse before they can enter the insulator and τ_o is the thermal prefactor for emission over the barrier. In order to gain quantitative insight into device degradation, we consider the well-accepted stretched exponential model for explaining the instability mechanism developed originally for amorphous silicon TFTs. This model has been used successfully used by different groups to explain the time dependence of ΔV_T for a-IGZO TFTs [4.33-4.34]. For our a-IGZO devices, the time evolution of ΔV_T for all stress times fitted well to the stretched exponential model which is used to describe both defect creation and interface charge-trapping mechanisms. The fitting parameters τ and β at different temperatures during both setup of constant current stress at various temperatures are listed in Table 4.2. From Table 4.2, the value of τ varies between 8.2×10^5 s to 4.3×10^8 s in the linear stress mode for temperatures ranging from 40°C-80°C whereas it is between 2.7×10^8 s to 1.6×10^7 s for the same temperature range in the saturation mode. The

decrease in τ value as the temperature and or current stress increases is indicative of more charge trapping at higher stress values. The increase in β with increasing value of gate bias and current stress indicates that the trap distribution becomes more uniform, and hence, the response is less stretched. When the temperature increases from 40 °C to 80 °C, the parameter τ changes in the range of 10^8-10^7s for the saturation mode whereas it varies between 10^8-10^5 s in the linear mode of current stressing. A smaller τ leads to a larger ΔV_T for a given stress time.

Table 4.2: Extracted stretched exponential model parameters

	Stress Biasing Condition	T_{STRESS} (°C)	β	τ (sec)
Linear Stress Mode	$I_{DS}=I_{STRESS}$	40°C	0.28 ± 0.001	4.31×10^8
	V_{GS} = 20V	60°C	0.34 ± 0.001	1.26×10^6
		80°C	0.39 ± 0.004	8.20×10^5
Saturation Stress Mode	$I_{DS}=I_{STRESS}$	40°C	0.588 ± 0.003	9.67×10^8
	$V_{GS} = V_{DS}$	60°C	0.6052 ± 0.001	2.93×10^7
		80°C	0.59126 ± 0.006	1.03×10^7

For example, increasing the temperature reduces the *τ* in the saturation mode by one order of magnitude while in the case of linear mode stressing, its reduction is by three orders. This implies a higher stability and longer term reliability of a-IGZO TFTs in AMOLED current driven mode even at higher temperatures. From Fig 4.11, we see that there is an

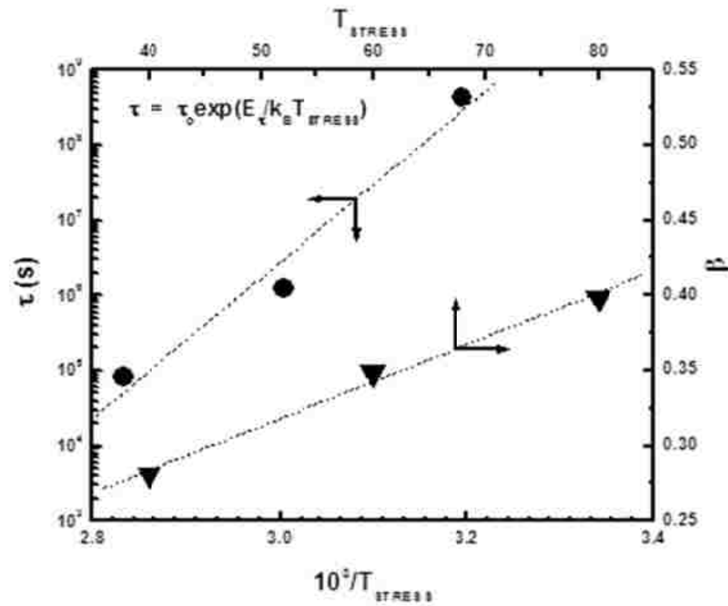


Figure 4.11 The variation of extracted fitting parameters τ and β as a function of stress temperature in the linear mode. Circles and triangles are extracted data and dashed lines are linear fit of data.

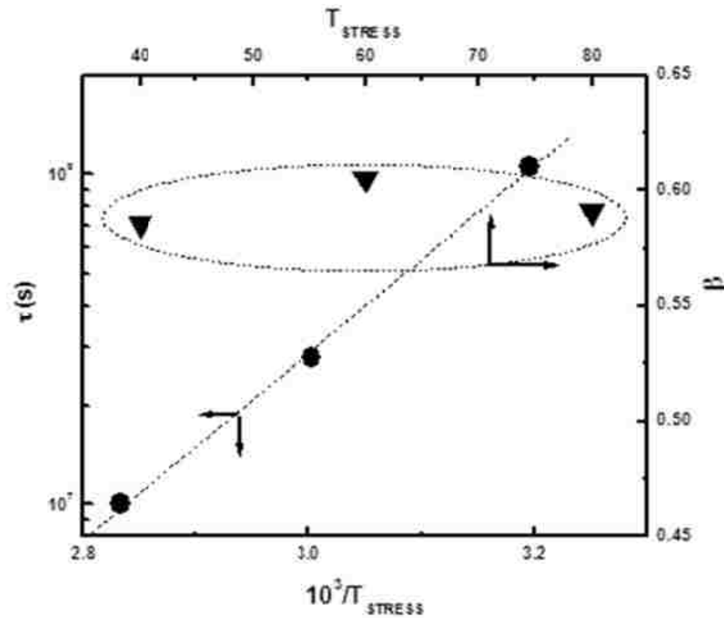


Figure 4.12 The variation of extracted fitting parameters τ and β as a function of stress temperature in the saturation mode. Circles and triangles are extracted data and dashed lines are linear fit of data.

increase in β value with increasing temperature indicating that trap distribution becomes more uniform and the response is less stretched (a larger fraction of states in the insulator near the interface will become filled, giving rise to an increasing probability of emission from these states). The temperature dependence of β is also suggestive of multiple trapping mechanisms. From Fig 4.12, one may also find that the parameter β is fairly temperature independent for the saturation stress mode (carriers hop or inject directly into lower energy states located at the a-IGZO/SiO_2 interface and in the SiO_2 transitional layer close to the interface). Temperature dependence of τ provide the average effective barrier height for electron transport (E_τ) which are obtained to be 0.56 eV for the case of saturation mode and 1.7 eV for linear mode of stress. The fitting parameter τ as a function of $1/k_BT_{STRESS}$ is plotted in Fig 4.11 and τ_o is extracted to be $9.1x10^{-2}$ s for the saturation mode and $2.6x10^{-25}$ s for the linear stressing mode.

According to the Si-Si weak bond breaking model proposed by Jackson, Marshall, and Moyer [4.35], the hypothesis to explain the TFT bias instability is that hydrogen diffusion causes the stretched-exponential behavior of ΔV_T with stress time. Deep state creation in a-IGZO/SiO_2 would require atomic migration (most likely involving cations). Atomic migration involving atoms such as Zn, Ga, or In usually require rather large migration energies (~3-4 eV) [4.36] and in that context seems incompatible with a-IGZO/ SiO_2 TFT instabilities. A more likely scenario is local atomic rearrangement, such as bond length or bond angle distortion and is thought to be thermodynamically and kinetically possible; however, local atomic rearrangement is expected to simply modify

the band tail state distribution, which would not lead to new state creation. As noted earlier, a-IGZO material systems are thermodynamically more stable material in which the band tail and deep state density is determined by processing details and particularly by the post-deposition processes. The band tail and deep state density in a-IGZO has been reported to be orders of magnitude smaller than that of a-Si:H [4.37]. All IGZO constituents are atoms much larger, less mobile and thus less reconfigurable than Hydrogen.

4.7 Conclusion:

Constant current temperature stress (CCTS) studies were performed on N_2O treated a-IGZO TFTs in linear mode where V_{GS} was held constant during the stress period and in saturation mode where the TFT was diode-connected to maintain a constant I_{DS}. In both modes of stressing, ΔV_T-t_{STRESS} shift with temperature and stress current was observed. In general, maintaining a lower temperature and smaller V_{GS} is beneficial to a-IGZO TFTs electrical stability. For the same level of I_{DS}, the TFTs are more stable when operating in the saturation regime than in the linear regime. From the observed behavior of ΔV_T- t_{STRESS}, we can conclude that there is only weak evidence of defect state creation in a-IGZO TFTs under constant current stress; the TFTs exhibit a ΔV_T of around 1 V under 2000 s stress with I_{STRESS}=100 μA at T_{STRESS}=60ºC. The substhreshold slope, off-current and field effect mobility remain unaffected in this stressing mode. The kinetics of ΔV_T- t_{STRESS} follow the stretched-exponential dependence predicted for charge trapping

in the interface/dielectric. In contrast to a-Si:H TFTs where ΔV_T does not saturate over time, that of a-IGZO TFTs saturates under constant current stress.

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Chapter 5

Electromechanical Stability of Amorphous IGZO Based TFTs and Circuits on Conformable and Thin Flexible Metal Foils

5. 1 Introduction

Mechanically flexible electronics have gained a lot of attention as novel applications like electronic books, roll-up displays and mobile communications gadgets which catch the fancy of consumers. Inexpensive and light-weight flexible electronics would be more rugged and portable than the more conventional rigid substrate-based electronics. Novel large area electronics, such as electronic paper, sensor skin, and electrotextiles, require building electron devices on flexible and deformable substrates [5.1-5.4]. Substrates such as organic polymers and stainless steel foils can be deformed into arbitrary shapes, but inorganic semiconductor device materials, such as amorphous silicon (a-Si:H) and silicon nitride (Si_3N_4), are brittle and crack easily when substrates are

deformed; therefore, it is desirable to reduce the strain in device structures on deformable substrates. A better understanding of the relationship between the electrical performance of the devices and the applied mechanical strain is also important. Although low temperature process ability of IGZO TFTs is compatible with plastic substrates, a greater dimensional stability (reduced shrinkage or elongation of the substrate during TFT fabrication) of thin metal foils allows implementation of circuit designs with smaller feature sizes. As these devices and circuits find increasing applications on flexible substrates, they will be subject to repeated flexing or bending; therefore, understanding the electrical performance of IGZO TFTs under mechanical strain becomes essential. There have been a number of studies on electro-mechanical characteristics of a-Si:H TFTs but no systematic investigation of IGZO TFTs on metal foils are reported. This study systematically investigates the influence of both tensile and compressive strain on IGZO TFTs. Correlation of electrical performance and mechanical strain will allow greater freedom when designing circuits based on IGZO TFTs.

5. 2 Manifestation of Strain on TFT based backplanes

TFTs on flexible substrates could be deformed due to internal forces that are at play during the fabrication process. This can happen due to built in stress in the films, a differential thermal expansion mismatch between films and substrates or even by interaction with the ambient conditions like uptake/release of humidity. A TFT backplane can also be deformed by an application of external forces that bends it, shapes it conformally or elastically stretches it. Fig 5.1 illustrates the active electronics fabricated

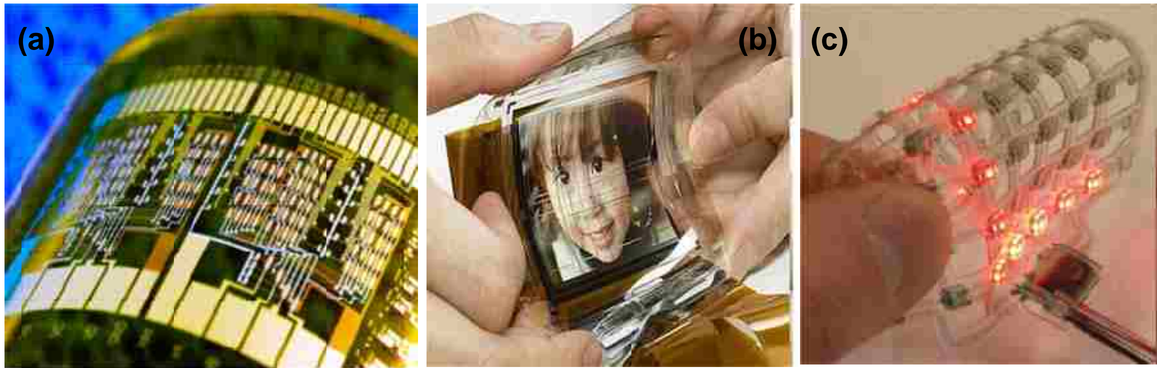

Figure 5.1 Examples of electronics on deformed substrates, (a) Carbon nanotube TFTs on a curved plastic surface, (b) Flexible Full Color OLED display on plastic; (c) Elastic stretching of passive LED matrix with enhanced deformability.

on different types of deformed substrates. In Fig 5.1(a), electronic circuitry fabricated with carbon nanotube is formed on curved plastic substrates (devices pioneered at University of Illinois at Urbana Champaign). The deformation on the curved surface may be large and not necessarily uniform over the entire area. For TFT backplanes, a more realistic scenario is the one depicted in Fig 5.1(b) where an OLED display (from LG display) is fabricated on flexible plastic substrate and may be subjected to repeated bending or flexing. The strain experienced by the active devices in this case may be small especially if they lie on a neutral plane on the compliant substrate. Finally 6.1 (c) shows shaping of passive LED array (from IMEC in Belgium) on elastically deformed and stretchable plastic substrate.

TFTs are built on flexible substrates one layer at a time. Typical layer sequencing involves substrate planarization and passivation followed by the active thin film depositions. Standard thicknesses of flexible substrates are between 50-200μm with passivation layer around 0.5-5μm and the active TFT layers around 0.5-1μm. In our lab,

poly-Si based TFT backplanes are fabricated on steel substrates and a corresponding schematic cross-section is shown in Fig 5.2 with planarization layers, active TFT layers, pasivation layers as well as a OLED front plane integrated on top of the TFT backplane. To assess the electromechanical stability of TFTs, we have to consider the mechanical integrity of semiconductors, insulators and metal lines on flexible substrates.

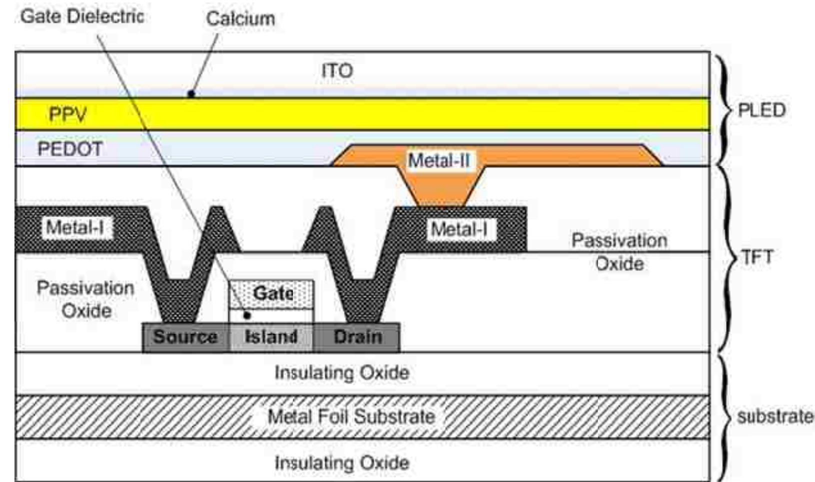

Figure 5.2 Schematic cross-section of poly-Si TFT on flexible steel substrates fabricated in Lehigh Display Research Lab.

The mechanics of TFT devices on flexible substrates can be approximated by considering a single homogeneous film that completely covers the substrate. This approximation simplifies analysis and modeling. The stress σ, a force applied to an area, is the response to the strain ε [5.5]:

$$\sigma = Y \cdot \varepsilon \tag{5-1}$$

and

$$\varepsilon = \frac{\Delta l}{l} \tag{5-2}$$

where Y is the elastic modulus. σ and Y have units of pressure (GPa). Strain, ε, is dimensionless and is frequently stated in percent. The behavior of the film-on-substrate structure under stress depends strongly on the elastic moduli and thicknesses of the substrate Y_s, d_s and the film Y_f, d_f. When $Y_f \cdot d_f << Y_s \cdot d_s$, the substrate dominates and the film complies with it. This is the case for TFTs on steel or metal foils. The film/substrate stack curves only slightly and the stress in the substrate is small even if the built in stress in the film is large. When $Y_f \cdot d_f >> Y_s \cdot d_s$, the film dominates, a scenario rarely encountered in TFT based backplanes but may arise in electronic textiles or skins. When $Y_f \cdot d_f \approx Y_s \cdot d_s$, as may be the case in TFTs (i.e. a-Si:H on polyimide substrate) on very compliant substrates like plastic, it gives rise to complicated mechanical situations. For a quantitative understanding of the mechanics of TFT film stack on a flexible substrate, a brief and succinct description of strain induced by fabrication or by external bending forces is summarized.

5.2.1 Built in Strain in a TFT films/Flexible Substrate Stack

Built in stress originates in films that are grown out of equilibrium atoms seeking to move to low-energy, equilibrium positions. During the deposition process, stress is induced due to surface stress effects, crystallite coalescence, grain growth, vacancy annihilation, effect of impurities and phase transformations. After the film is grown, temperature of the films-substrate system may change to a different level and the mismatch strain will be induced due to the difference of thermal expansion coefficient between film and substrate. It can be described by [5.6]

$$\varepsilon = \varepsilon_0 + (\alpha_f - \alpha_s)\Delta T \quad (5\text{-}3)$$

where α_f and α_s are the thermal expansion coefficients of the film and the substrate and ΔT is the temperature difference. Consequently, the mismatch strain, in (5-3) needs to be accommodated by elastic and inelastic deformation in the film. If the film remains elastic within the temperature change, this mismatch strain induces a biaxial stress in the plane of the film, σ_T , given by [5.7]

$$\sigma_T = \frac{Y_f \varepsilon_T}{1 - \nu_f} \quad (5\text{-}4)$$

where, Y_f is Young's modulus and ν_f is Poisson's ratio of the film ($\nu \approx -\Delta L\perp/\Delta L\|$; where, $\Delta L\|$ is the variation in change of length in the parallel direction of applied strain and $\Delta L\perp$ is the variation length in the longitudinal direction).

5.2.2 Bending Strain in a TFT films/Flexible Substrate Stack

The flexible film/substrate system could be subjected to additional stresses by externally applying bending moment. Any such bending or stretching induces strain in the thin films as well as the substrate. Fig 5.3 illustrates a TFT/substrate bent to a cylinder of radius R. The film and the substrate have thicknesses d_f and d_s and Young's moduli Y_f and Y_s. When bent, the top surface is in tension and the bottom surface is in compression. One surface sandwiched between this stack, known as the neutral surface, has no strain. If the film and the substrate have different elastic moduli ($Y_f > Y_s$), so that the neutral

surface is away from the mid-surface and toward the film, the strain in the top surface, ε_{top} is given by [5.8]:

$$\varepsilon_{top} = \left(\frac{d_f + d_s}{2R}\right)\frac{\left(1 + 2\eta + \chi\eta^2\right)}{\left(1+\eta\right)\left(1+\chi\eta\right)} \tag{5-5}$$

where $\eta = d_f / d_s$ and $\chi = Y_f / Y_s$. In this study, the top thin film stack is composed of SiO_2 and metal lines with Y_f ranging from 50-200 GPa and a-IGZO (Y_f~30-250 GPa [5.9]); the substrates is stainless steel (Y_s =195 GPa) [5.10]. With these conditions, Y_f/Y_s =1 and the neutral surface is approximately the mid-surface of the stack and (5-5) reduces to

$$\varepsilon_{top} = \frac{\left(d_f + d_s\right)}{2R} \tag{5-6}$$

It is clear that the minimum allowable radius of bending scales linearly with the total thickness assuming the TFTs fail upon reaching a critical strain value.

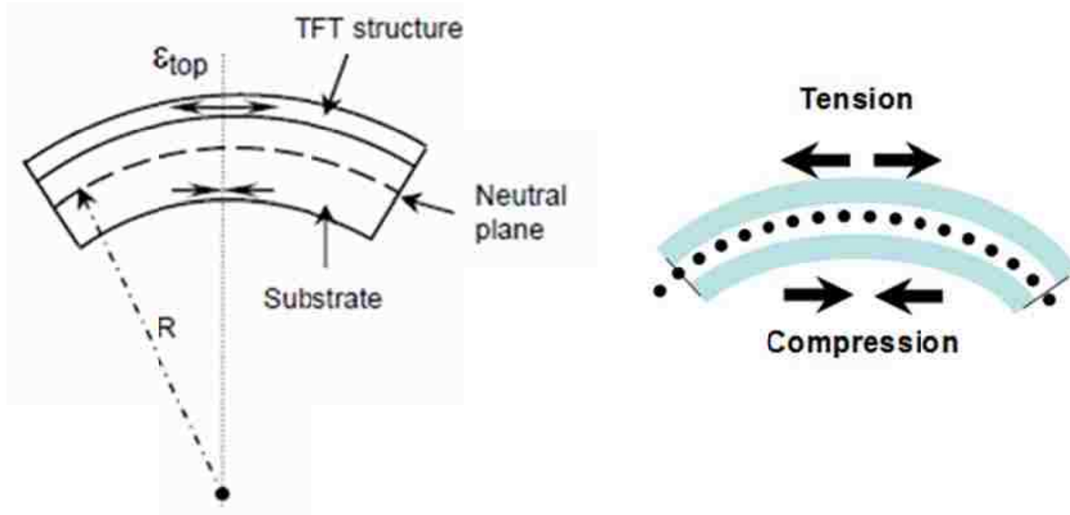

Figure 5.3 Thin film/foil structure bent to a cylindrical roll. The TFT is put into a well defined strain, which is tensile when the film is on the outside and compressive when on the inside.

5.3 Mechanical Integrity of film Stack on Flexible Steel Substrate

A two-point bending approach previously employed for poly-Si TFTs on steel foil [5.11] was adopted for ascertaining electromechanical stability of TFT film stack on metal foils. When bent, the steel substrate can be plastically deformed and the bending radius can be calculated by fitting an ellipse to the digital image of the bent curve. For electrical isolation as well as stress balance, the steel substrate was coated with PECVD deposited 2 μm SiO_2 layer on both sides. With one side coated with 2 μm SiO_2, warping of the samples was observed after the film deposition. The residual stress in CVD SiO_2 on SUS304 steel substrate can be calculated from the well-known Stony relation [5.12] :

$$\sigma = \frac{Y_s d_s^{\,2}}{6d_f}\left(\frac{1}{R_1} - \frac{1}{R_2}\right) \tag{5-7}$$

where R_1 and R_2 are radii of samples before and after film deposition and the other parameters are as defined earlier. The built in stress was calculated to be around 0.79GPa which includes both intrinsic strain and thermal mismatch strain. Fig 5.4 shows the crack

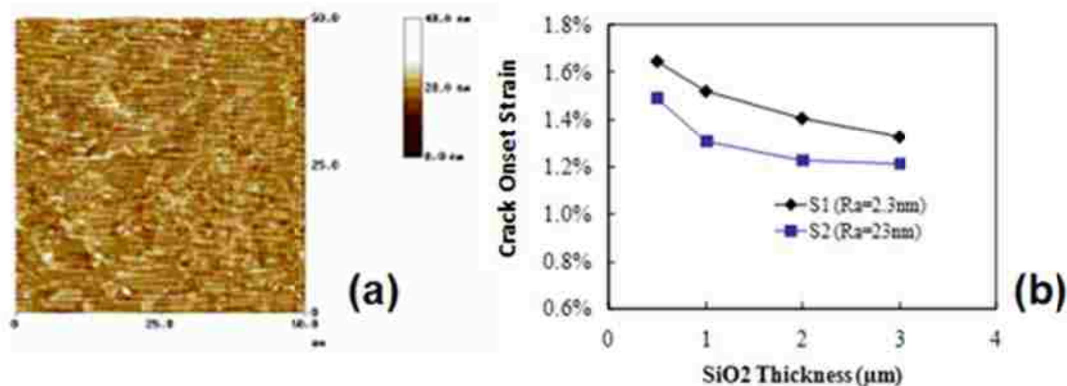

Figure 5.4 Surface roughness of SUS 304 stainless steel substrates and crack onset strain on PECVD SiO2 on SUS 304 substrates with different surface roughness.

onset strain of PECVD SiO_2 with different thicknesses. A rougher and thicker substrate has a lower crack onset strain and this agrees well with prediction from fracture mechanics [5.13] which states that strain to failure of brittle layers scales inversely with the thickness. For a-IGZO TFT fabrication, SUS304 substrates with surface finish of lessthan 2 nm were used to increase the crack onset strain in the SiO_2 films. A 2μm coating was deemed suitable for both resistance against cracks as well as reducing shorts between the conductive substrate and the active TFT components on SiO_2 layer. Crack onset strain for metal interconnects on SUS304 with 2μm SiO_2 on both sides was shown to have even higher strain resistance (>3.5%) [5.10]. As we noted earlier, the steel substrate is plastically deformed after the bending test. When compared to the failure strain of SiO_2, metal lines and the active TFT a-IGZO layers, the critical strain of steel is substantially lower (0.13%). For steel foil substrates (100μm thick) which are used in this study, the minimum elastic bending radius was calculated to be 38.5 mm. It is worth noting the flexibility of the a-IGZO TFT stack on substrate can be efficiently improved by decreasing the thickness of the steel substrates.

5.4 Characterization of a-IGZO TFT and Circuits Under Strain

Inverted staggered IGZO TFTs and circuits on 100μm thick, type SUS304, stainless steel substrates were fabricated for this study. The steel wafers had surface roughness (Ra) of around 2 nm and was coated with 2 μm thick PECVD SiO_2 layer on both sides to electrically isolate the substrate as well as to prevent thermal expansion mismatch. The IGZO TFTs were strained by bending dies with dimensions of 20 mm by

30 mm to fit cylinders of different radii. The die was well constrained (Fig 5.5) to conform to the curvature of the cylinder for accurate strain calculations. The corresponding strain, ε, was then calculated from the relationship $\varepsilon = z / R$, where R is the bending radius and z is the distance from the neutral plane to the active layer of the TFTs. For our sample, the neutral plane is located approximately in the middle of the stainless steel foil substrate and since the length and width of the steel foil are orders of magnitude higher than its thickness, applied strain is uniaxial. The bending direction was parallel to the source-drain current path and the bending radius determined the corresponding applied strain.

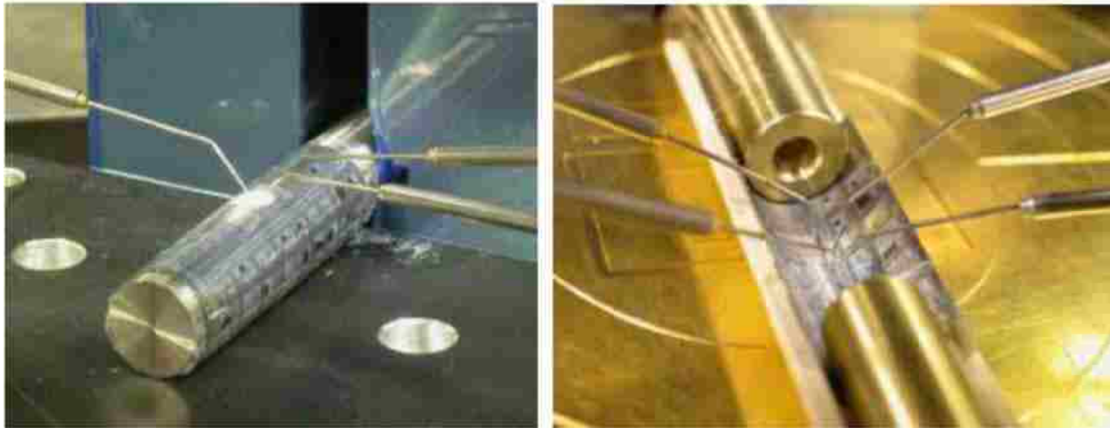

Figure 5.5 Steel foils dies with a-IGZO TFT under (a) Tensile and (b) compressive strain

Transfer characteristics were measured at drain to source voltage of V_{DS}=0.1 V for standalone IGZO TFTs at each bending radius. From each set of transfer characteristics we extracted the off-current, on-current, gate leakage current, field effect mobility and threshold voltage of the TFTs under tensile strain. To ensure that the applied electrical strain during measurement did not mask the mechanical strain measurements,

we waited for 5 min after measuring the characteristics before changing the radius and remeasuring the TFT characteristics. In a similar fashion, 7-stage IGZO ring oscillator circuits were also investigated with the applied tensile strain parallel to the oscillator's TFT channel direction. A Tektronix P6243 1GHz active probe with < 1pF input capacitance was used to monitor the oscillation frequency. Only tensile strain was applied since compressive strain did not substantially affect the a-IGZO TFT mobility and On current values. Oscillation frequency of the ring oscillator was measured at different supply voltages of 6, 18, 22 and 26 V. Propagation delay was then calculated by dividing the oscillation period with the number of stages at each supply voltage level and bending radius.

5.4.1 Electrical Properties of Discrete IGZO TFTs Under Strain

Non-flexed TFTs for this particular study exhibited linear field effect mobility of 11.2 $cm^2/V.s$, threshold voltage around 2.5 V and sub-threshold swing of 0.5 V/decade and On/Off current ratio exceeding 10^7. The uniaxial tensile/compressive strain applied with different bending radius varied from 0.1-1% and 0.1-0.5% respectively. The figure of merit when measuring TFTs under mechanical deformation is critical (failure) strain level which corresponds to the onset of physical damage in most brittle layers of the device. In a-Si:H TFTs for example, the failure strains are in the range of 0.3%-0.5% [5.14]. In Fig 5.6, representative transfer characteristics of stand-alone IGZO TFTs with dimensions of W/L=240μm/10μm in the virgin state (no strain applied) and at various tensile/compressive strains are shown. All measurements are taken in dark to decouple

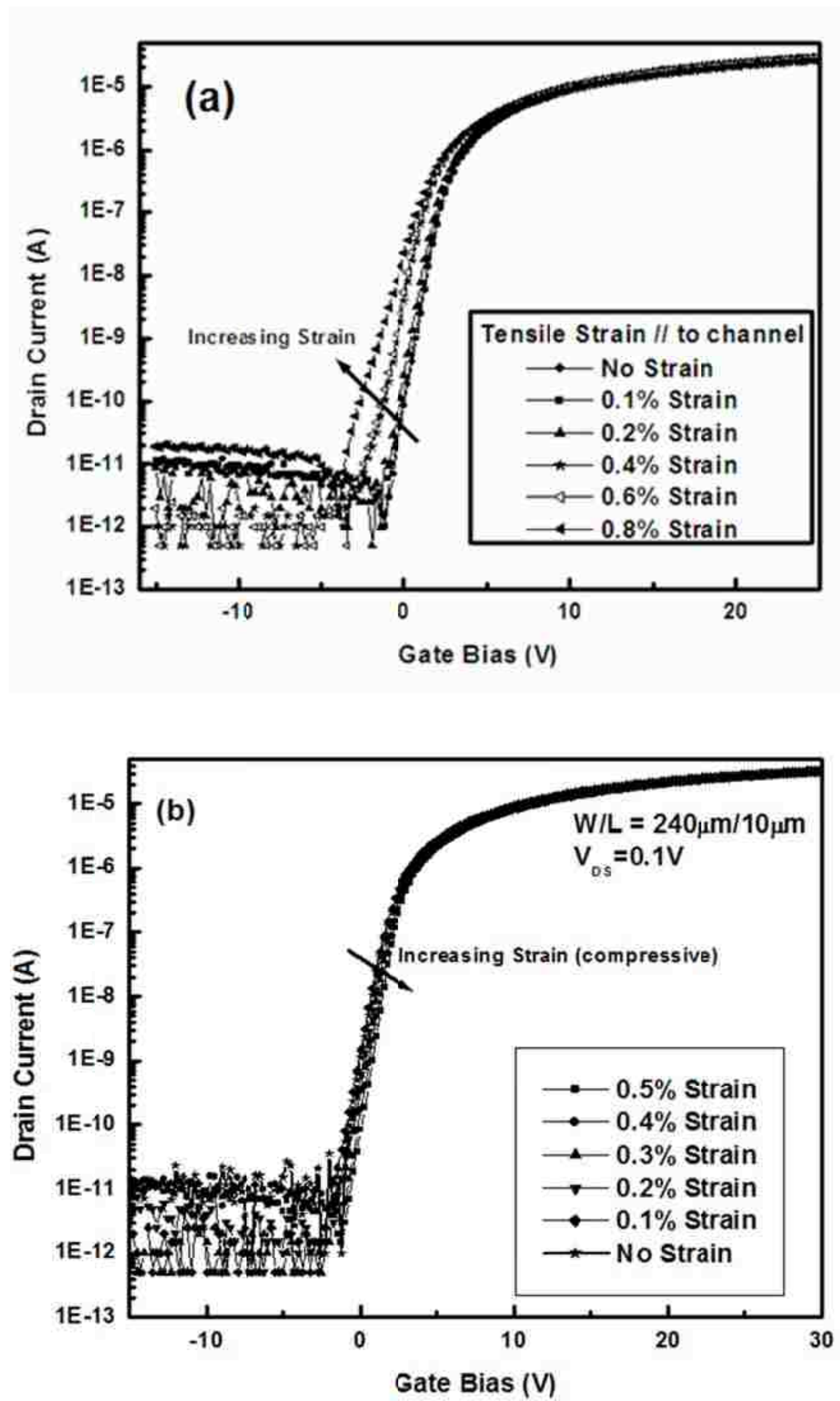

Fig 5.6. Transfer characteristics of IGZO TFT at V_{DS}=100 mV (W/L=240μm/10μm) with (a) Tensile strain and (b) Compressive strain

effects of illumination during bending. It is obvious, from Fig 5.6 that the transfer characteristic moves in opposite directions for tensile and compressive strain. It is worth mentioning that since the measurement of the characteristics under compressive strain follows a tensile bending, the observed shift caused by compressive strain is smaller than the shift that would've been observed if the tensile strain hadn't been applied. The threshold voltage shift, ΔV_T is around 1V for 0.8% tensile strain whereas this shift is less than 200 mV for 0.52% compressive strain. In a-Si:H TFTs, a similar trend was observed [5.14] with no effect on electrical properties resulting from a compressive strain substantially less than 1.8%. This study was limited by lack of additional cylindrical geometry to apply a greater compressive strain. The subthreshold swing degrades with increasing tensile strain and remained virtually unchanged for compressive strain. Because the elastic deformation of the steel substrate has a small and reversible effect on the electrical properties of a-IGZO TFTs, the critical strain level where the TFT fracture occurs may be all the information that is needed from a practical point of view. In Fig 5.7, we see that the TFTs remained functional up to a maximum tensile $\varepsilon_{critical}$ of 0.8%. This is slightly higher than that reported for a-Si:H TFT on metal foils. An increase in I_{off} (off current) and gate leakage current, I_L is observed for applied tensile strain levels larger than 0.8%, followed by device failure at $\varepsilon_{critical}$. Optical microscope inspection reveals that cracks localized near Mo patterns appear and develop preferentially at the edge of the source/drain layers at this tensile strain level.

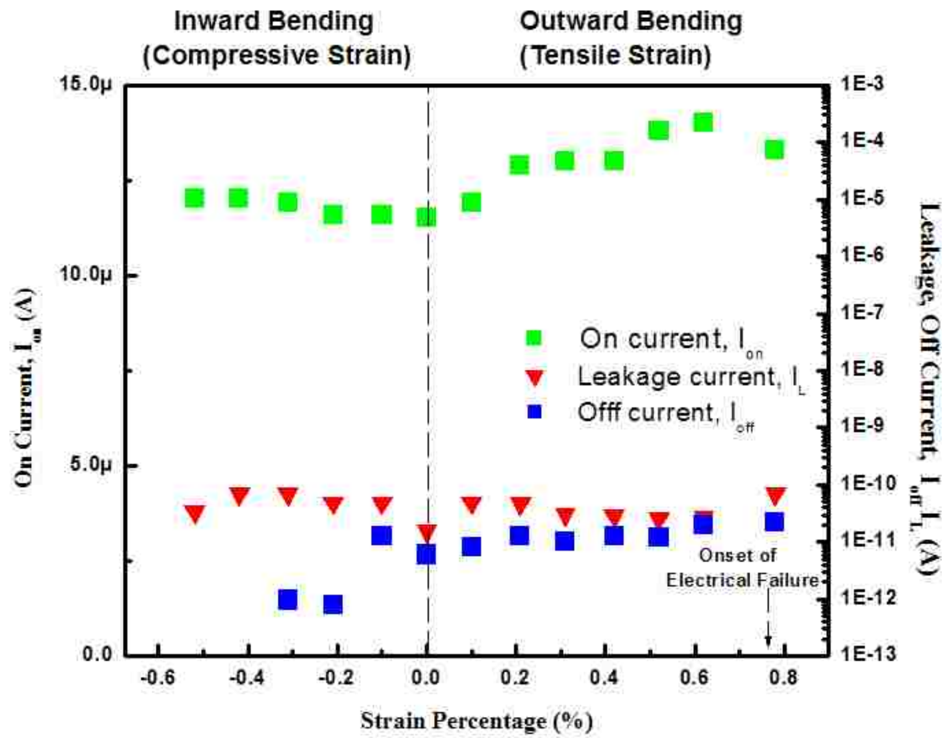

Fig 5.7 Evolution of On-current, Off-current and Gate-leakage current of a-IGZO TFT (W/L=240µm/10µm) with tensile and compressive strain.

The typical drain current (I_{DS}) versus drain voltage (V_{DS}) characteristics of the same TFT with (at 0.6% of tensile strain) and without uniaxial mechanical strain at V_{GS}-V_T = 1, 3 and 5V is depicted in Fig 5.8. There is drain current enhancement for different V_{GS}-V_T (20%, 17% and 11% respectively) with increasing tensile strain up to 0.6%.

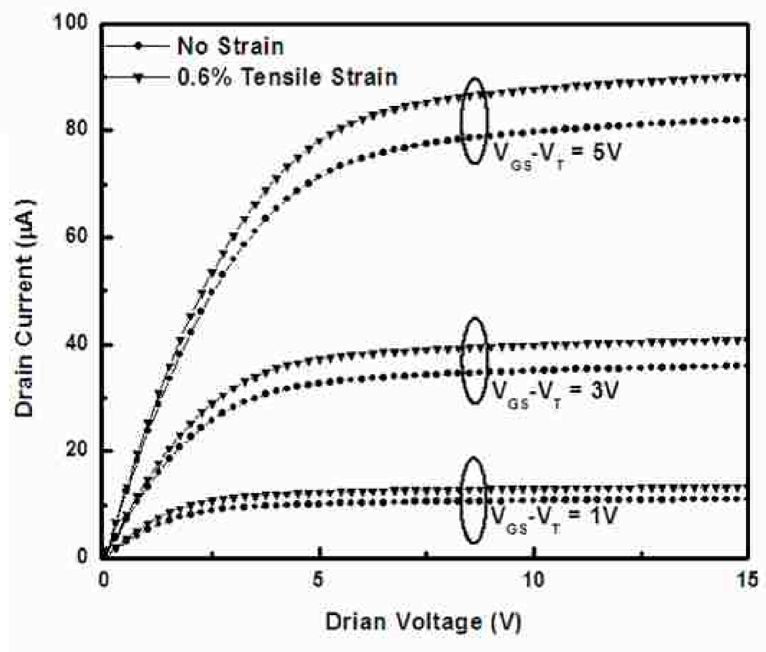

Fig 5.8 Output characteristics of a-IGZO TFT (W/L=240μm/10μm) with different gate-overdrive voltages for 0.6% tensile strain applied.

The increase in on-current correlates well with the higher field effect mobility observed with increasing tensile strain. For tensile strains larger than 0.8%, the mobility starts to decrease. This result is consistent with the behavior of a-Si:H TFTs under tensile strain [5.14]. In Fig 5.9(a), we see that the relative change of mobility with tensile strain scales with TFT channel length. The changing rate of mobility is dependent on channel length for devices with the same width. A strong dependence of mobility on TFT channel length is indicative of the presence of parasitic series resistance [15], whereas no dependence on width is observed. The parasitic series resistance in the source and drain regions of a TFT can be described by

$$\frac{1}{\mu_0} = \frac{1}{\mu_i} + R_P\left(\frac{W}{L}\right)C_{ox}\left(V_{GS} - V_T\right) \qquad \text{(6-8)}$$

where μ_0 is the low field mobility, μ_i is the intrinsic mobility without the effect of parasitic source/drain resistance and R_p is the parasitic series resistance. Fig 5.9 (b) shows the normalized carrier mobility μ_i / μ_{i0} as a function of tensile strain for a-IGZO TFTs. The μ_i was extracted to be 11.45cm^2/V.s for the non-strained case. A linear fit gives the following relation between the μ_i and the applied tensile strain: $\mu_i = (0.108\varepsilon + 1.005)\mu_{i0}$.

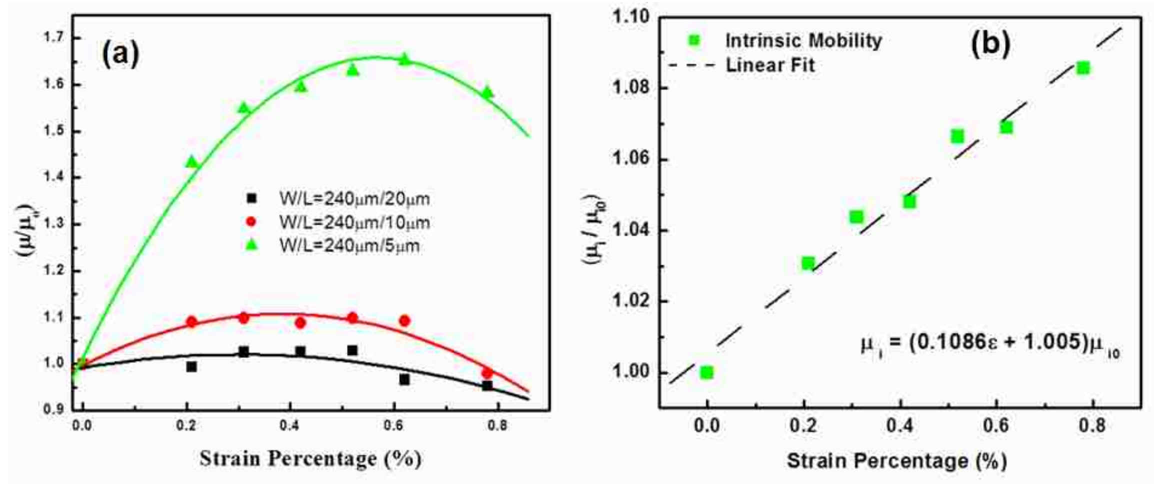

Fig 5.9 (a) Normalized linear field effect mobility voltage (μ/μ_O) of IGZO TFT with various dimensions with tensile strain. (b) Normalized intrinsic mobility, (μ_i / μ_{i0}) (W/L=240μm/10μm) with strain.

The threshold voltage, V_T, decreases with increasing tensile strain (Fig 5.10(a)) which is quite contrary to that observed in a-Si:H TFTs. This decrease of V_T can be verified from capacitance-voltage (C-V) measurements of MIS (Metal/SiO_2/IGZO) structures under tensile strain (Fig 5.10(b)).

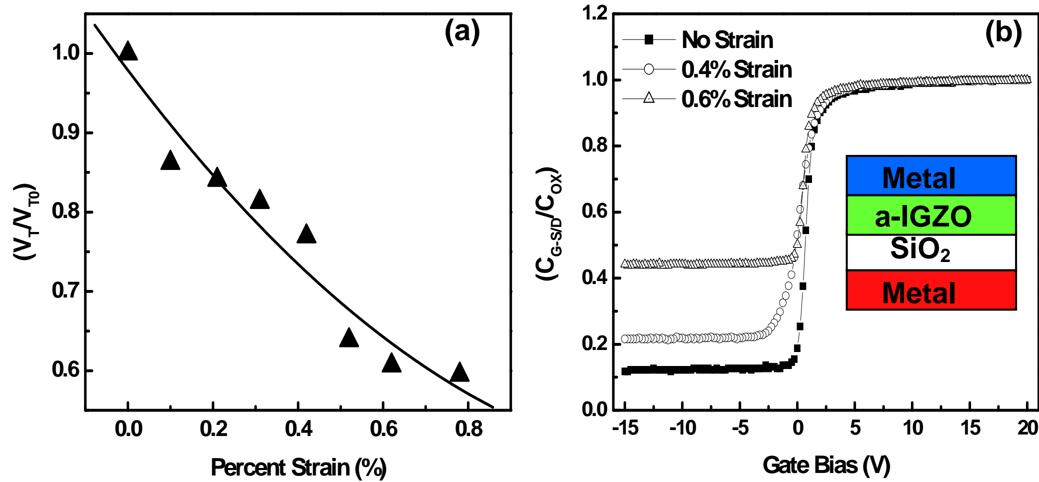

Fig 5.10 (a) Normalized threshold voltage (V_T/V_{TO}) of IGZO TFT with dimensions of W/L =240µm/10µm) with tensile strain. (d)The shift in threshold voltage is verified by capacitance voltage measurements of MIS structures with increasing strain.

5.4.2 Electrical Properties of IGZO TFT Based Circuits Under Tensile Strain

Flexible circuits based on IGZO TFTs will be subjected to global strain due to either bending of the substrates or by package strain. In any case, it is imperative to know the circuit performance with various levels of strain in order to have greater design freedom. The effect of tensile strain on dynamic characteristics of the IGZO TFTs are evaluated from 7 stage ring oscillator circuits (L_{load}=L_{drive}=16 µm, W_{load}=64 µm, W_{drive}=256 µm), exhibiting oscillation frequency of 85.7 KHz when non-flexed at a supply voltage of 15 V. Increasing longitudinal tensile strain reduces (Fig 5.11(a)) the propagation delay per stage (oscillation at 88.6 KHz at 15 V and tensile strain level of 0.4%) which can be directly correlated to relative mobility increase with applied strain. The relative change of propagation delay with strain is reduced as the power supply

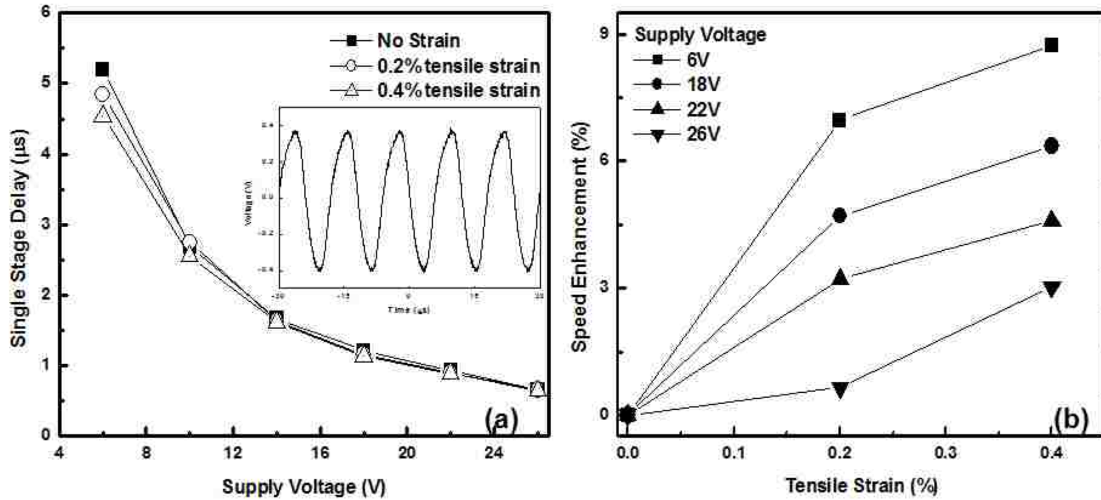

Figure 5.11 Characteristics of 7 stage IGZO ring oscillator (L_{load}=L_{drive}=16 µm, W_{load}=64 µm, W_{drive}=256 µm) under tensile strain: (a) Single stage propagation delay decrease with supply voltage (oscillator output for VDD =15 V shown as inset) and applied strain, (b) Measured speed enhancement of the same ring oscillator from 6V-26V of supply voltage under various strain levels.

voltage increases. This may be due to the drain bias dependence [5.16] of piezo-resistive coefficient in the a-IGZO channel. The speed enhancement of IGZO TFT based ring oscillator circuit (Fig 6.11(b) is also supply voltage dependent and due to a large current enhancement under uniaxial tensile strain.

5.4.3 Physical mechanisms of strain effects on a-IGZO TFT with strain

The effect of mechanical strain for devices on flexible substrate has been explored for a-Si:H TFTs [14,15] and organic TFTs [5.17]. For a-Si:H TFTs, the failure strain is from 0.5~1.0% in tension and 1.0~2.0% in compression; the mobility was reported to scale linearly with applied strain. These mobility changes under strain is correlated with a broadening or steepening of the conduction band tail in a-Si:H. The mobility of a-Si:H is

dominated by frequent trapping in the conduction band tail states. Compared to a-Si:H TFT the failure strain of organic pentacene TFT is much higher due to the excellent plasticity of organic material. Because the carrier transport mechanism for pentacene is hopping and the strain changes the spacing between pentacene molecules, the mobility of pentacene TFT decreases under compressive strain and increases under tensile strain [5.17].

In a-IGZO TFTs, we observed an increase in linear field effect mobility with tensile strain (same as in a-Si:H TFTs) and a corresponding negative shit in V_T (contrary to a-Si:H TFTs); however, the subthreshold swing worsened with increased tensile strain. Therefore, the correlation of reduction of Urbach energy (valence band tail slope) with decrease of conduction band tail states to explain the mobility increase in a-Si:H TFTs is not applicable to a-IGZO TFTs. Mechanical strain causes either an increase (for tensile strain) or a decrease (for compressive strain) of the inter-atomic distance of the semiconductor layers in a TFT. The direction of this change is parallel to the applied strain. It has been shown in the case of a-Si:H TFTs that the conductance change with strain is maximum when the applied strain is parallel to the current path in a TFT. In our case, the variation in change of length ($\Delta L_{\parallel}$) is also parallel to the current path. The variation length in the longitudinal direction ($\Delta L_{\perp}$) corresponding to the width and thickness variations of the a-IGZO layer is induced by the Poisson effect and quantified by the Poisson ratio v, where $v_f \approx -\Delta L_{\perp}/\Delta L_{\parallel}$. With a theoretical boundary of $-1 < v_f < 0.5$, this relation shows that the direction of applied strain remains dominant when it comes to changing the inter-atomic distances and consequently the current in a TFT. The

Poisson ratio of IGZO is not known, but its closest material, ZnO, has a Poisson ratio of $v_{ZnO} \approx 0.35$ [5.18]. With increasing tensile strain, the inter-atomic distance is increased which causes an effective decrease in the energy level splitting (ΔE) of the bonding and antibonding orbitals between the atoms in the semiconducting layer [5.19]. This changes the value of the Fermi function toward the conduction band edge in the case of tensile strain and away from it in the case of compressive strain. This conductance increase (additional availability of electrons for transport) results in a negative shift of V_T for tensile strain and the increase in energy spacing leads to a positive shift $V_{T.}$ The mobility increase for tensile strain can be correlated with a decrease in the electron–lattice

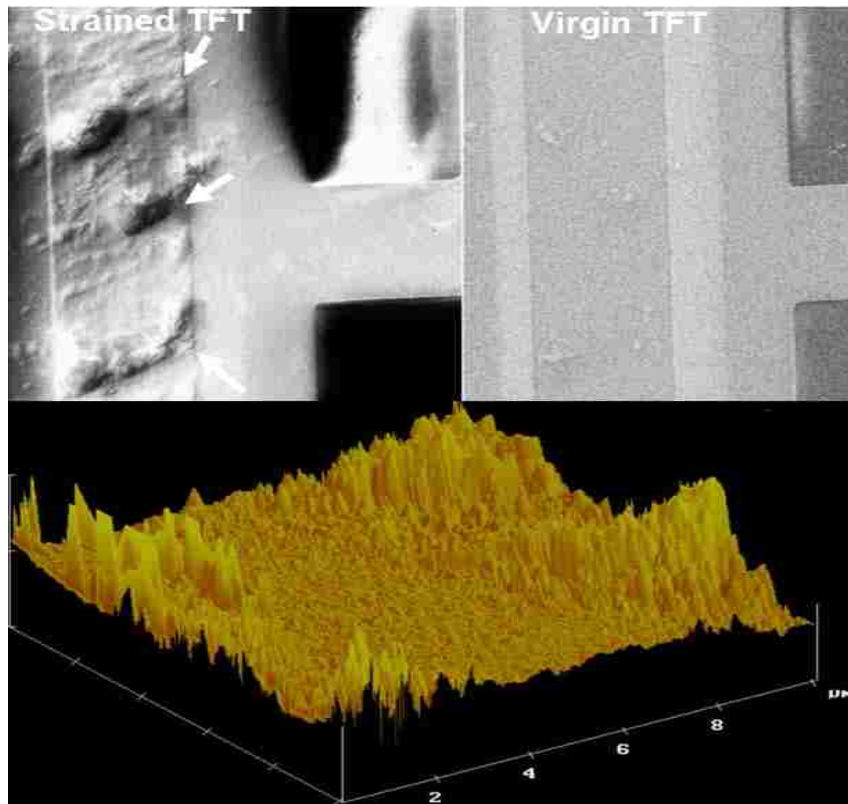

Figure 5.11 SEM image of a-IGZO TFT ((L=10 µm, W=240 µm) after undergoing 0.8% tensile strain and 0.5% compressive strain. Crack propagate along the edge of gate/source-drain edge first and then there's hint of buckling (AFM).

interaction due to the decreased energy spacing in the direction parallel to the current flow. This decreases the effective mass m* of the charge carriers (m* ~ ΔE) [5.20] and affects their mobility (μ ~ 1/m*). The increase in free carrier density under tensile strain can also explain the increase in capacitance observed in the Metal/SiO_2/IGZO structures. Finally, SEM imaging (Fig 5.11) after both tensile strain and compressive strain reveals that cracks first propagate around the edge of gate and source/drain overlap region from underneath SiO_2 layer and a subsequent buckling (revealed by AFM) of the whole TFT stack.

5.5 Conclusion

We have applied uniaxial tensile and compressive strain ranging from 0.1% - 1% to amorphous IGZO TFTs and circuits fabricated on stainless steel foils by outwardly bending them to cylindrical surfaces with different bending radii. Tensile strain increases field effect mobility and reduces threshold voltage of stand alone devices. IGZO TFTs remained functional up to an applied strain level of 0.8% with critical strain (failure mode) level at 0.9%. a-IGZO TFT showed greater immunity against compressive mechanical bending the important TFT parameters did not change much up to 0.5% of applied strain. IGZO TFT based ring oscillator had lower propagation delay per stage and speed enhancement with applied tensile strain. In summary, this study provides us with some understanding of IGZO TFTs under mechanical strain and allows for predicting IGZO TFT based circuit performance when flexed.

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Chapter 6

Amorphous IGZO Based Circuits and Systems on Conformable and Thin Flexible Metal Foils

6. 1 Introduction

Electronics on flexible substrates have attracted a great deal of attention these days since mechanically flexible, large area electronics can usher in the era of ubiquitous computing as well as enable novel applications such as roll-up displays, wearable sensors, imaging devices etc. Many factors contribute to the allure of flexible electronics as they are more rugged, lighter and portable compared to their rigid substrate based counterparts. Hydrogenated amorphous silicon (a-Si:H) [6.1], low-temperature polycrystalline silicon (LTPS) [6.2] and organic materials [6.3] have been examined as active layer materials in such flexible devices. As we have noted before, a-Si:H is the material that is most widely investigated for flexible electronics and has been demonstrated to be useful in developing

flexible solar cells and TFTs [6.4]; however, device performances and applications are limited by the properties inherent to this material. The field-effect mobilities of a-Si:H TFTs are only < $2cm^2/V.s$ because the drift mobility of a-Si:H is controlled by hopping between localized tail states [6.5]. These values are not satisfactory for high-resolution carrier injection devices such as organic electroluminescence displays. We also know that polycrystalline Si TFTs exhibit large variations in device characteristics due to grain boundaries; Therefore, extra circuits have to be included to compensate for the deviations of the device characteristics which limit the resolution and aperture ratio of the displays. We have shown until now that oxide TFTs, specifically based on amorphous IGZO can have superior performance that significantly exceeds that of amorphous and nanocrystalline Si and approaches that of larger grain poly-Si without the complexities and uncontrolled variability of polycrystalline materials. The simplicity of processing is also another attractive feature when circuit integration is the topic at hand. Since source/drain contacts can be directly placed onto the a-IGZO channel layer, additional steps associated with source/drain doping (as is the case for a-Si:H and LTPS) are obviated. An added feature is the possibility of creating transparent electronics by fabricating all electrodes and channel materials with > 80% transmittance in the visible spectrum which would enable all transparent displays with larger aperture ratio eliminating the need for opaque light shields. This will afford larger real estate for pixel TFTs and therefore larger current drive which is due to high mobility of a-IGZO TFTs. Thus, AMOLED integration with transparent electronics would be compatible with a conventional metal cathode-on-top OLED structure [6.6].

The application of a-IGZO TFTs, however, is not limited to simple switching elements in active-matrix displays; rather, the relatively high performance allows integration of thin-film analog and digital circuits and possibly, microwave devices [6.7]. There has also been considerable interest in integrating the row and column drivers for AMOLED displays onto the same [6.8] backplane as the pixel switches. This requires a relatively high performance circuit technology. Recently, IGZO ring oscillator circuits on silicon substrates with 0.5 μm channel length and 0.5 μm source-gate and source-drain overlap were reported to operate at ~7 ns/stage with a saturated-load inverter design, and <1 ns/stage with a novel bootstrapped inverter design [6.9]. In addition, high temperature ZnO TFTs (400-600°C) deposited by pulsed laser deposition have exhibited high field-effect mobility >100 $cm^2/V{\cdot}s$, maximum channel current density >400mA/mm and interesting microwave performance with f_T = 2.45 MHz and f_{max} = 7.45 MHz on high resistivity Si wafers [6.7]. In most of the recent demonstrations, rigid substrates such as Si wafers and glass substrates with high performance lithography and small alignment tolerances have been used.

The relative low process temperature fabrication of a-IGZO TFT is very suitable for demonstrating circuits and systems integration on pliable, conformable substrates such as polymeric substrates; however, as a vehicle of demonstration, metal foils offer great dimensional stability that allows for implementation of circuits with small feature sizes. Furthermore, they offer superior chemical resistance in a number of harsh environments and better thermal spreading behavior that plague typical plastic substrates. Throughout this chapter, the development of thin film a-IGZO based NMOS-only

architecture circuits on flexible metal foils will be described. Both static and dynamic (clocked circuits) that comprise the essential elements of display devices and other large area electronics will be demonstrated. The effects of design geometry and different circuit topology on the performance of circuits will be discussed. These circuit demonstrations served to both identify functionality for real application as well as confirm the lack of a large number of slow interface states in these a-IGZO devices. Finally, a short discussion on creating p-type TFTs with oxide materials which would enable fabrication of complementary CMOS circuits will be presented as a prelude to our efforts towards achieving such functionality in oxide semiconductors.

6. 2 a-IGZO Based Circuit Integration and Design Considerations

6.2.1 Circuit Design and Integration

Multiple device configuration is possible when employing IGZO TFTs for circuit integration and both top-gate and bottom gate configurations have been used by various groups [8-9]. A top gate design could potentially have the added benefit of yielding higher channel mobility, if the surface of the channel layer is smoother than that of a bottom gate dielectric. A smoother interface between the channel layer and gate insulator reduces interface roughness scattering, which improves the channel mobility [6.10]; however, high-k dielectric by either RF sputtering or by more exotic ALD techniques has been used in such device configurations. In our case, since we wanted to avoid the potentially damaging plasma bearing radicals (H_2 species mostly) on top the IGZO films, a bottom gate design is deemed suitable. The a-IGZO TFT circuits have a staggered,

bottom-gate device architecture. The circuits are fabricated by first depositing 150 nm of Al by RF sputtering onto oxide coated stainless steel wafers and lithographically patterning and wet etching to form the gate layer. We have also fabricated a-IGZO TFTs on other flexible metal foils such as dimensionally stable Ni-Fe alloys and ultra low cost Al to demonstrate the transferability and repeatability of IGZO deposition processes to different compliant substrates. A 100 nm thick SiO_2 is then deposited by PECVD at 300 °C; then 50 nm of optimized a-IGZO thin film is deposited by RF sputtering from a 6-inch diameter commercially available IGZO target (1:1:1 molar ratio of In_2O_3:Ga_2O_3:ZnO) followed by a low temperature mesa oxide as a protection layer. The N_2O plasma passivation treatment of the IGZO films is carried out prior to the mesa oxide deposition in PECVD ambience. Sputtering is carried out at a RF power density of 1 W/cm^2 at a chamber pressure of 10 mTorr (10 vol% O_2 diluted with Ar). A low RF power density is used to mitigate potentially damaging bombardment of the growing films by energetic negative oxygen ions, which can cause substantial stress in the film [6.11]. The a-IGZO/SiO_2 stack is patterned by combination of wet and dry etching in dilute HCl and PECVD CF4 chemistry respectively. A thicker passivation oxide (70 nm) is then deposited and contact openings to the gate pads are accomplished by lithography and selective etching of the oxide layer. Source and drain contact opening are also open through the mesa/passivation oxide stack. Finally, Mo source and drain metallization is done by RF sputtering and subsequent lift-off. The complete devices are then subjected to post-fabrication anneal in N_2 ambience at 300 °C for 1 Hr.

LEdit Software was used to layout a 6 inch mask set with a variety of circuits on a particular die which was repeated across the mask set. Figure 6.1 delineates mask layout of a 5-stage ring oscillator with a-IGZO TFT and the corresponding cross-sectional view

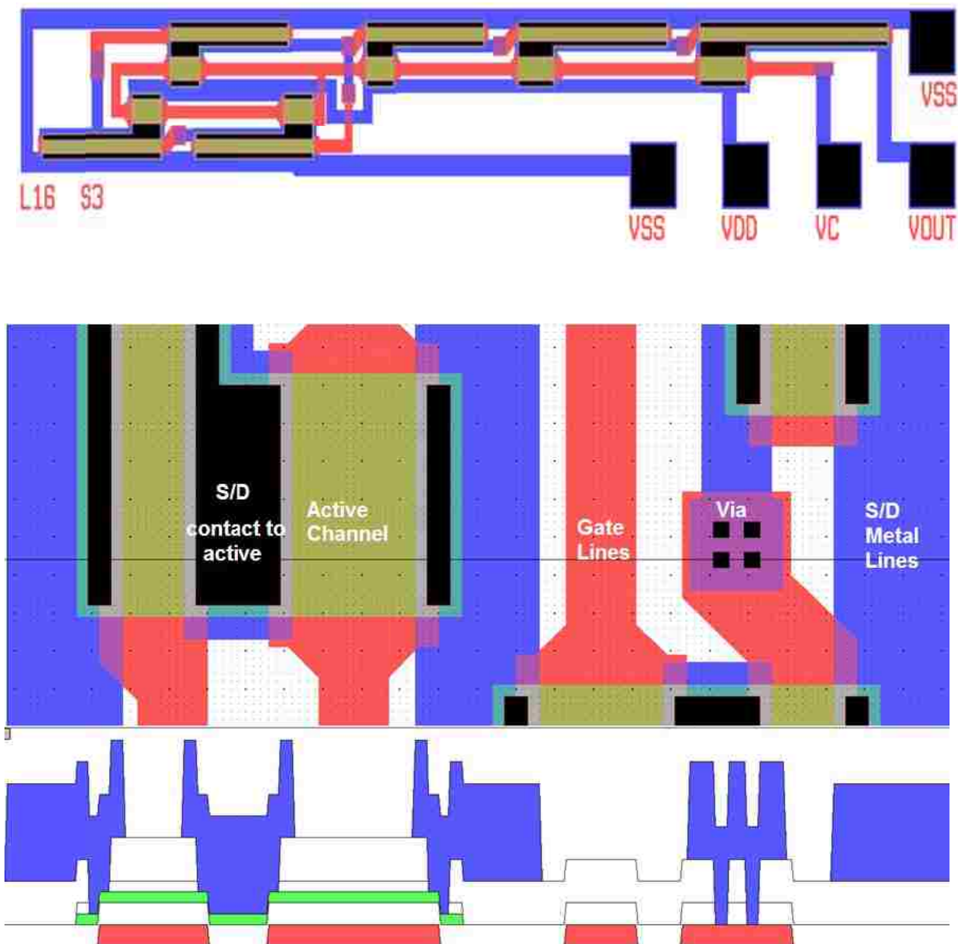


Figure 6.1 Mask layout of a 5-stage ring oscillator design based on a-IGZO TFTs and cross-sectional view of the corresponding TFT devices. The probing pads are labeled in the completed design (top)

of the devices. To gain more understanding of static and dynamic performance of the a-IGZO technology, both analog and digital logic circuits were designed and will be

discussed herein. A high performing technology, such as thin film electronics based on a-IGZO has the added advantage of high level integration of electronic functions. In this fashion, reductions in cost, space and complexity become an asset of fully integrated display and other large area systems.

6.2.2 a-IGZO TFT Scaling and Uniformity

The greater dimensional stability of flexible metal foils allows for design rules much tighter than those used with other compliant substrates. As such, feature lengths, layer spacings, device density and ultimately circuit performance can be noticeably improved. In order to design electronic circuits, dependency of these parameters on

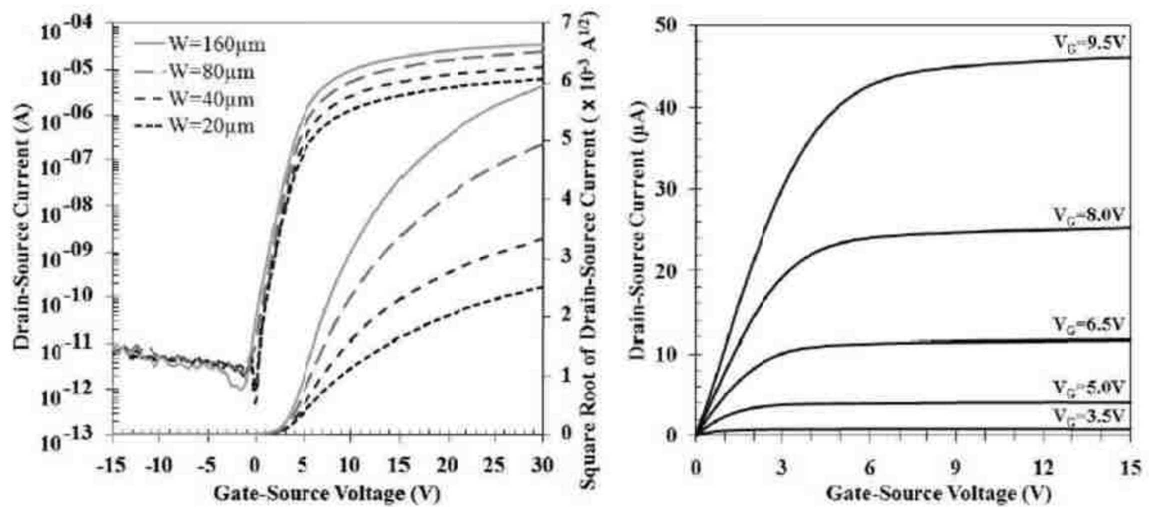


Figure 6.2. (a) Transfer characteristics (I_{DS}-V_{GS}) of discrete IGZO TFTs with channel length of 10μm and various channel widths (shown in the graph) at V_{DS}=1V; (b) Output characteristics (I_{DS}-V_{DS}) of the TFT with W/L=160μm/10μm and V_{GS} varied from 3.5V-9.5V in 1.5V steps.

material properties and fabrication conditions, as well as dependency on structural conditions (such as length and width) need to be determined. When incorporating digital

and analog control circuits, it is crucial that scalability of device performance such as current drive can be controlled by design parameters. To this end, a variety of devices of different dimensions are incorporated in the mask set that can be used as a basis for system design as well as for monitoring of technology performance. Fig 6.2 demonstrates that a-IGZO TFTs scale well with varying dimensions and V_{DS} biasing. It is noticeable that drain currents in the μA range can easily be obtained with gate voltages of only 5 V. IGZO TFTs also exhibit good short range uniformity in their characteristics because of the amorphous nature of the active material. The short range uniformity is important inalmost all of the circuit applications involving TFTs. For example, active-matrix displays require good uniformity of the backplane TFTs for smooth rendering of the

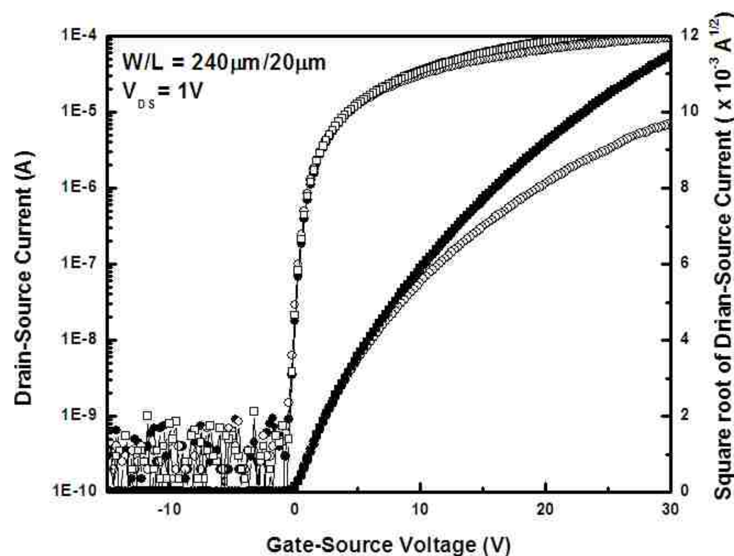


Figure 6.3 Transfer characteristics (I_{DS}-V_{GS}) of 5 different discrete IGZO TFTs in close proximity of each other with channel length of 20μm and channel width of 240μm at V_{DS}=1V

displayed images. The difference in performance among the neighboring TFTs in a pixel circuit is a critical issue. Figure 6.3 shows transfer characteristics of 5 different TFTs

selected from adjacent dies superimposed onto each other to demonstrate short range uniformity of RF sputtered a-IGZO TFTs on 100 μm thick flexible steel foils. The average threshold voltages (V_T) of the measured TFTs were 0.7±0.02V, average filed effect mobilities (μ_{FE}) were 15.01±0.2 $cm^2/V.s$ and average substhreshold slopes (SS) were 0.35±0.07 V/dec.

6.3 a-IGZO Based Inverters

6.3.1 CMOS Inverter vs. NMOS only Inverters

An inverter is the essential element of digital circuit design. A properly designed inverter block can be the basis of more complex and involved digital circuits. The most common inverter structure is the static complementary MOSFET inverter shown in Fig. 6.4. The CMOS inverter uses PMOS as pull-up system and NMOS as pull-down system to obtain inversion of the input voltage level. The voltage transfer characteristic shown below explains the response of an inverter output voltage (V_{OUT}) to specific input voltages (V_{IN}). The voltage transfer curve is a figure of merit for the static behavior of the inverter. V_{IL}, V_{IH}, V_{OL} and V_{OH} are parameters which determine the limits of inverter stability. From Fig 6.4(b), V_{IL} is the smallest input voltage recognized as logic "LOW", and V_{IH} is the smallest input voltage recognized as logic "HIGH". Noise margin is a parameter critical for good design of digital circuits. It determines the allowable noise voltage limit on the input of a gate electrode, so that the output will be unaffected. They are defined as NM_H (V_{OH}-V_{OL}) and NM_L (V_{IL}-V_{OL}).

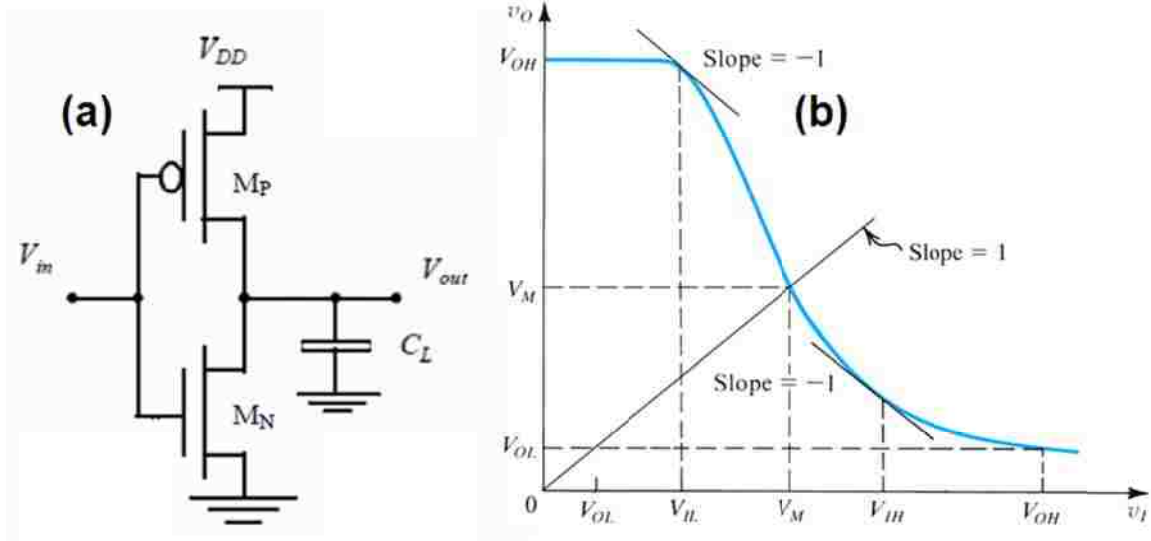


Figure 6.4. (a)An ideal CMOS inverter with NMOS and PMOS TFTs; (b)Voltage Transfer characteristics CMOS inverter with the logic levels and noise margins defined. [Adapted from Ref. 6.11]

6.3.2 a-IGZO NMOS only Inverters with Saturated Load

a-IGZO based TFTs fabricated are unipolar devices and operate in enhancement mode regime; therefore, an inverter with two enhancement-mode TFTs (load and drive TFT) can be designed in the configuration shown below (Fig. 6.5) with the load tied in a diode-connected fashion so as to mimic a resistor. When the input level is pulled to a logic level "high", both the load and drive TFTs are conducting and pulls the output close to logic level "low" (GND in this case). The geometric sizing ratio of the load and drive TFTs, known as β (beta) ($\beta = (W_{Drive}/L_{Drive})/ (W_{Load}/L_{Load})$ determines how strongly the output is pulled low and the nominal gain margin. When the input level is "low", the load TFT pulls the output level close to supply voltage, V_{DD}. The gain of an all-enhancement

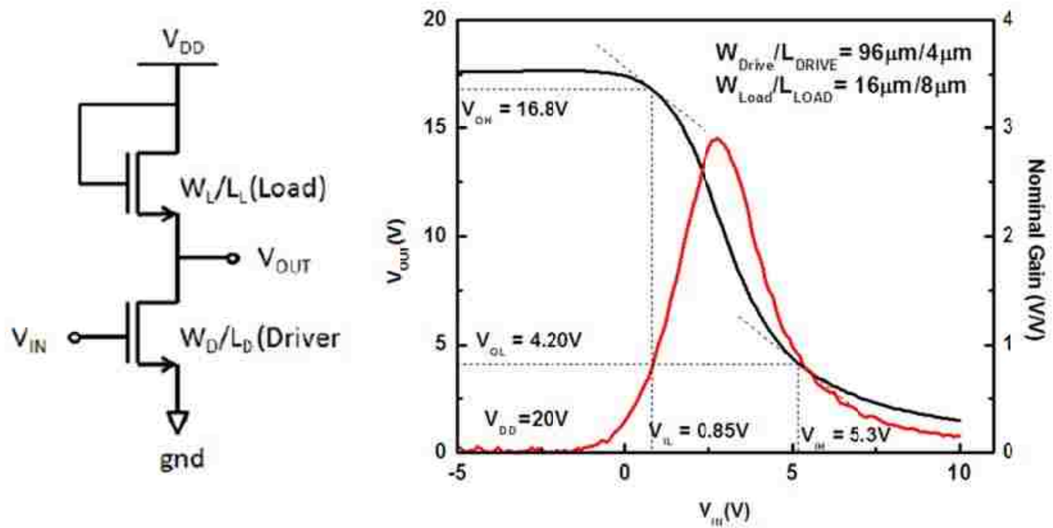


Figure 6.5. NMOS only saturated-load inverter circuit schematic; Voltage transfer characteristic of a-IGZO inverter with ($\beta = (W_{Drive}/L_{Drive})/(W_{Load}/L_{Load}) = (96\mu m/4\mu m)/(16\mu m/8\mu m)$).

mode inverter is ideally equal to the square root of the β. In the enhancement-enhancement type of inverter topology, it is difficult to pull the output to V_{DD}-$V_{T(Load)}$ and therefore logic level conversion is an issue. Fig 6.5 shows the voltage transfer characteristics of an all-enhancement mode inverter with $\beta = (W_{Drive}/L_{Drive})/(W_{Load}/L_{Load}) = (96\mu m/4\mu m)/(16\mu m/8\mu m)$. The supply voltage is set at 20V. The noise margins (NM_H =11.5 V and NM_L=3.35V) are highly asymmetric and is non-ideal. The experimental gain ($|\partial V_{out}/\partial V_{In}|$) of the inverter is also depicted in Fig 6.5 and found out to be around 3. This is somewhat lower than the theoretical value of $\sqrt{\beta} = \sqrt{12} = 3.46$. This may be related to several possible reasons. First the patterned a-IGZO active channel layer is larger than the source/drain pads in both the load and drive TFT and therefore the effective load width may be larger leading to a reduced β. Second, there is no one-on-one relationship of the β ratio to the actual ratio of conductance because the two TFTs are

biased at different points and the mobility of a-IGZO TFTs have voltage dependence [6.12]. The effective mobility of the drive TFT is lower than the load TFT at the logic

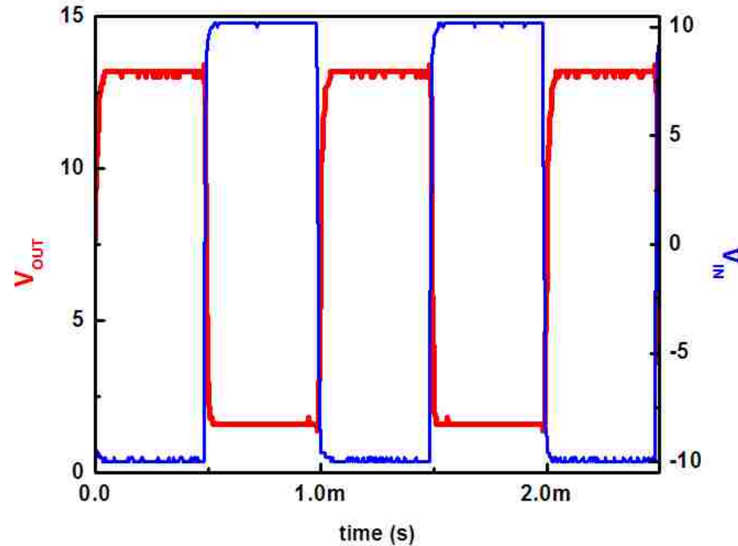


Figure 6.6. Dynamic response of the NMOS only saturated-load inverter circuit ($\beta = (W_{Drive}/L_{Drive})/(W_{Load}/L_{Load}) = (96\mu m/4\mu m)/(16\mu m/8\mu m)$).

level inversion point, reducing the difference in conductance and therefore affecting the effective gain. From the discussion above we can allude to the fact that high gain saturated load inverters using oxide-based TFTs with V_{GS} dependent mobility may represent a significant challenge especially when large dive TFTs will introduce large parasitic capacitances amplified by the Miller effect [6.13]. Despite the drawbacks, we see that inverter does exhibit requisite characteristics needed for a variety of digital circuits and this all-enhancement mode inverter with saturated load is used in the subsequent circuit designs. Finally, the dynamic response of the inverter is shown in Fig 6.6. The rise time and fall time are measured to be 25.2μs and 12 μs respectively.

6.3.3 Effect of varying β and V_{DD} on Inverter characteristics

The geometric sizing of the drive and load TFTs is expected to affect the output swing and the propagation delay of the inverter. A larger β ratio will result in greater pull-down strength toward the low rail voltage and as a consequence the output swing suffers. Fig 6.7 (a) shows the effect of β ratio on the voltage transfer characteristics of an all-enhancement mode TFT with saturated load. As seen in the figure, the output voltage can be regulated and shifted up by decreasing the β ratio. A larger β ratio results in a steeper voltage transfer characteristics and improved noise margins; however, it is

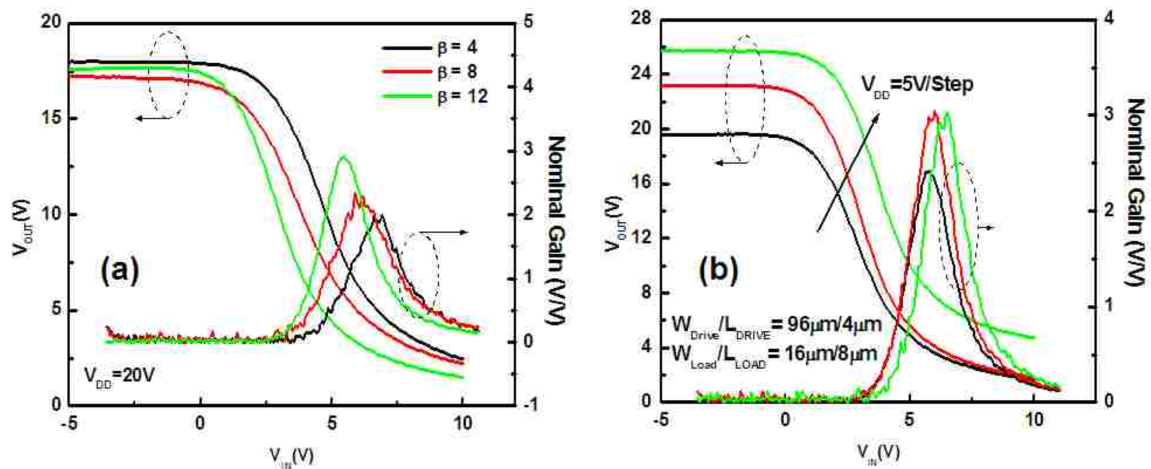


Figure 6.7 Voltage transfer characteristics of all-enhancement mode inverter for (a) varying β ration and (b) varying the supply voltage, V_{DD}.

expected that a smaller β ratio will lead to greater operating frequency for a given V_{DD}. Fig 6.7 (b) on the other hand depicts the effect of varying V_{DD} for a given β ratio. The V_{OH} (output high voltage) is shifted up by 7 V for a 10 V increase in V_{DD} (33V up from

23V); the low output stabilizes at different voltage levels as well (4.7V for V_{DD} =33V and 1.7V for V_{DD} = 23V). The gain is expected to increase with V_{DD} scaled up.

6.3.4 a-IGZO NMOS only Inverters with different types of Loads

As we can imagine, NMOS only inverters with a-IGZO TFTs can be implemented in multiple configurations depending on the type of load used. The diode-connected saturated load configuration is the most common one. However, as we have noted in the preceding section, the drawback of this structure is that the output can reach a maximum voltage of V_{DD} - $V_{T(Load)}$ due to the V_T drop across the load TFT. If we can have a control voltage (gate voltage of load TFT) that effectively determines the resistance of the load TFT as shown in Fig 6.8 (b), we can circumvent this problem. This can be achieved by operating the load TFT in linear regime, with at least $V_{GLoad} > V_{DD} + V_{TLoad}$. A pure resistive load (Fig 6.8 (c)) will also work at the expense of higher power consumption. In Fig 6.9, the effect of the gate voltage of the load as a control voltage is shown. As expected, the output high level is pulled closer to supply rail (V_{DD}) by a control voltage that is at least one V_T higher than the diode-connected fashion. All the three cases mentioned above are examples of “Ratioed Logic”, since the output level depends on the ratio of the impedances (i.e. on W/L ratios) of the pull-up and the pull-down devices.

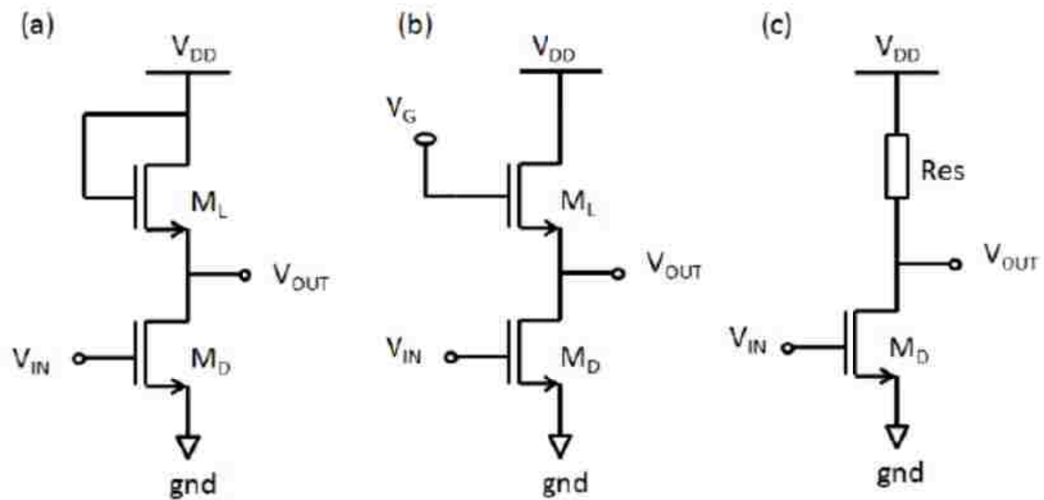


Figure 6.8 Different load configuration of NMOS only inverter; (a) diode-connected load, (b) Linear mode TFT as load, (c) A purely resistive load.

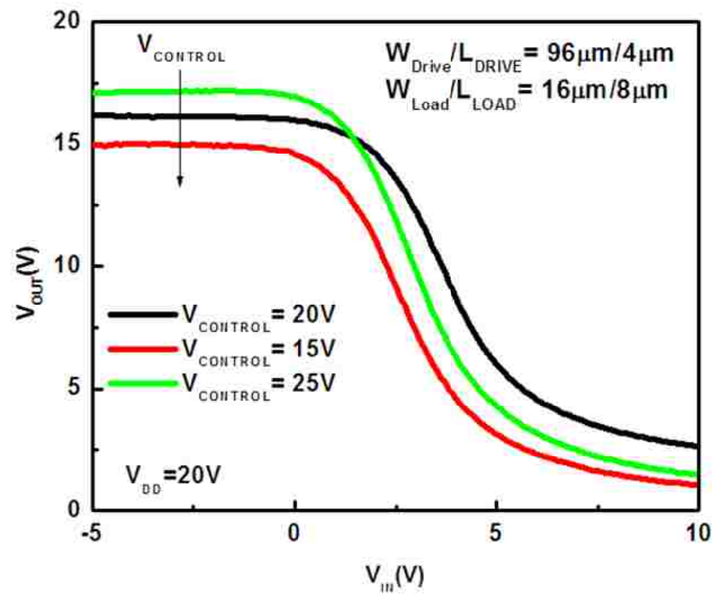


Figure 6.9 Effect of Control voltage signal on inverter voltage transfer characteristics

6.3.5 Enhancement-Depletion type a-IZO/a-IGZO NMOS only Inverters

Due to the difficulties in accomplishing the p-type operation in oxide based TFTs, most of the AOS (amorphous oxide semiconductor) logic circuits have been implemented with n-channel TFTs. In a-IGZO TFTs, it is difficult to invert the channel for p-type operation because of a very high density of states above the valence band edge. This has been the main drawback in making high-performance logic circuits. For more involved circuitry employing a-IGZO TFTs like in an analog amplifier, a higher gain than that achievable with all-enhancement mode inverters is required. An enhancement-depletion (E-D) type inverter topology can achieve this. In this circuit configuration (refer to Fig 6.11), the gate and source of the load TFT (depletion mode) are tied together to provide effectively a constant current source. This design allows the output high, V_{OH}, to reach

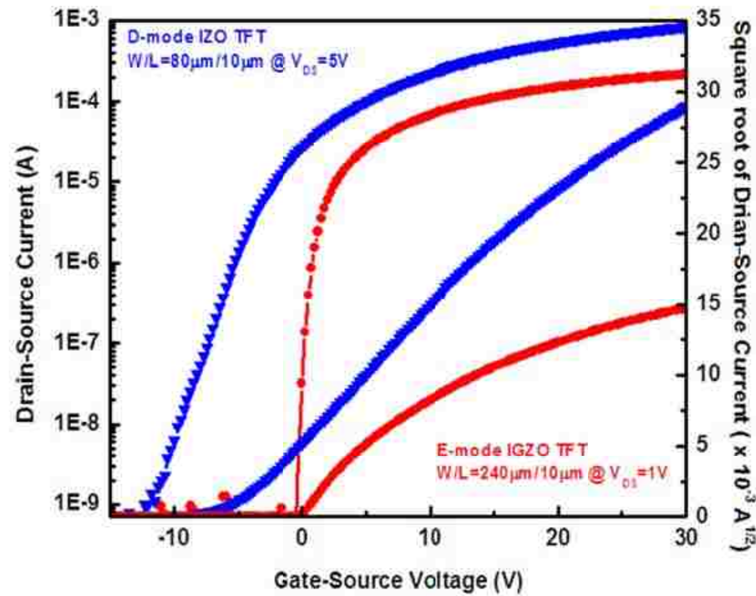


Figure 6.10 Transfer characteristics of depletion mode IZO TFT (W/L=80μm/10 μm) and Enhancement mode a-IGZO TFT (W/L=240μm/10 μm).

V_{DD} and the output low, V_{OL}, to approach the lower rail voltage. The output low, $V_{OL,}$ is ultimately limited by the ability of the E-mode TFT to sink the current source at a low V_{DS}. There are reports of high gain oxide based E-D inverters implemented in various ways. Mourey et al [6.14] showed hydrogen plasma treated V_T shift in ZnO TFTs to implement E-D inverter while others have resorted to a-IGZO channel thickness variation to control the V_T to obtain depletion type TFT [6.15]. We have implemented E-D inverter by combining a-IZO as a depletion load and a-IGZO as an enhancement drive TFT. The V_T movement with N_2O treatment of a-IZO TFTs can also be used as E-D inverter. Fig 6.10 shows the transfer characteristics of a-IZO and a-IGZO TFTs as depletion and enhancement mode TFTs used in our E-D inverter. As is clearly evident, there is a more than 5V V_T separation between the two mode TFTs which is useful in proper E-D

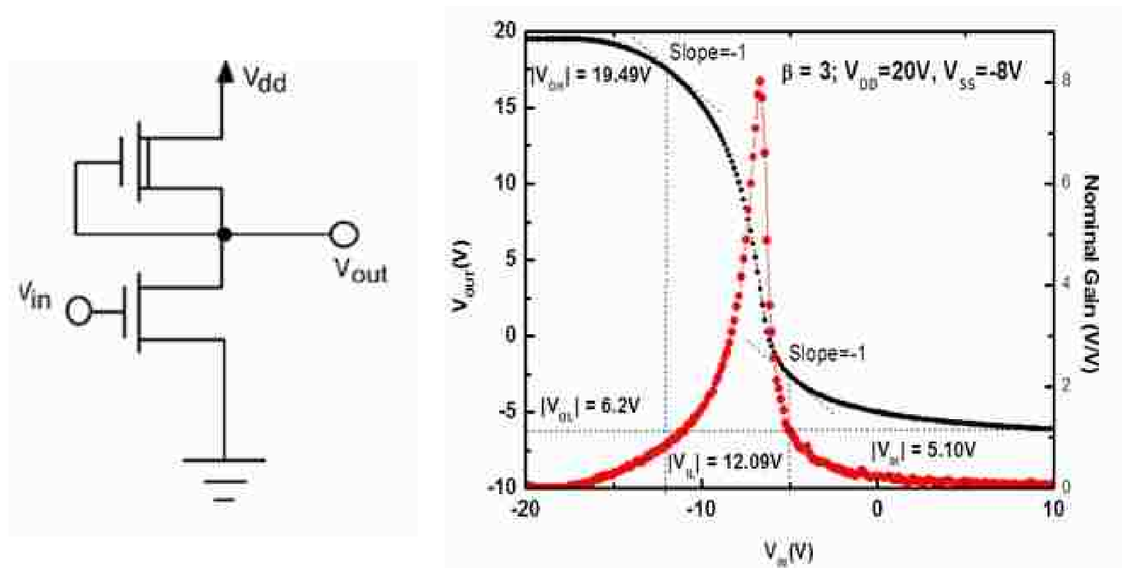


Figure 6.11 Effect of Control voltage signal on inverter voltage transfer characteristics

inverter operation. Fig 6.11 shows the voltage transfer characteristics of an a-IGZO/a-IZO based Enhancement-Depletion inverter with a geometric scaling ratio of $\beta = (W_{Drive}/L_{Drive})/(W_{Load}/L_{Load})= (240\mu m/10\mu m)/(80\mu m/10\mu m)$. The depletion mode TFT is always on since the gate and source are tied together and it enters saturation when the drain voltage exceeds the source voltage by V_{TD} (V_T of depletion mode IZO TFT). On the contrary, the enhancement mode TFT turns on after the gate voltage exceeds the source voltage by V_{TE} (V_T of enhancement mode IGZO TFT). At V_{DD}= 20V, excellent gain of 8.01V/V is obtained with V_{OH}=19.5V at V_{IN}=-20V and V_{OL}=-6.2V (VSS=-8V) at V_{IN}=10V. Compared to all-enhancement mode inverter employing saturated load, the E-D type inverter has a larger gain and wider swing range. The noise margins are improved but remained asymmetric ($|NM_H|$=14.3V and $|NM_L|$=5.9V) with the transition width ($|V_{IH}-V_{IL}|$=7.8V) substantially increased.

6.4 a-IGZO based static Logic Circuits (NAND and NOR logic circuits)

Once the basic building block of inverter design is perfected, other digital logic circuits like pseudo NAND and NOR circuits can be easily designed and implemented. The NAND and NOR level circuit implementation typifies the series and parallel type of TFT connection needed to represent Boolean logic functions. The all-enhancement mode saturated load inverters discussed in the earlier sections comprise the active load element of these circuits. To achieve functionality in digital form, the output is required to have a rail-to-tail swing that represents binary logic. Due to the unavailability of p-type TFT in oxide based devices, this is difficult to attain. In our design, the relative sizing of the

individual TFTs are optimized to get close to rail-to-rail swing of 15V. In NAND operation, the output is "high" when either of the inputs (A or B) is "high", or if none of them is "high". The output goes to low only if both the inputs are "high". Fig 6.12 shows the NAND logic circuit operation with a 15V output swing. The fidelity of the logic conversion is excellent with very low rise and fall times. In NOR type operation, a logic "high" output will result if both of the inputs are "low". If one or both of the inputs are

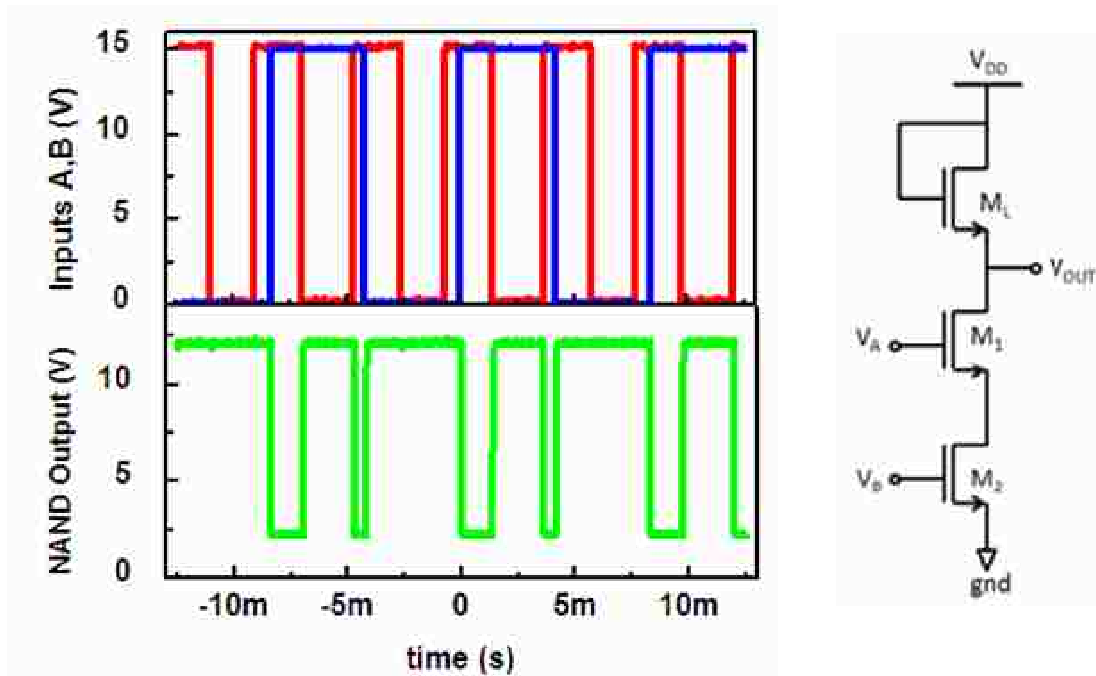


Figure 6.12 a-IGZO based Pseudo NAND circuit and logic level conversion

"high", a low output will transpire. NOR operation is verified in circuit implemented with a-IGZO TFTs in Fig 6.13. For both NAND and NOR circuits, the input A is a square wave with 0-15V swing and 50% duty cycle and input B has a double delay of 4ms with the width of the square wave pulse being 2ms. V_{DD} is 20V and the load TFT is diode connected as a saturated load.

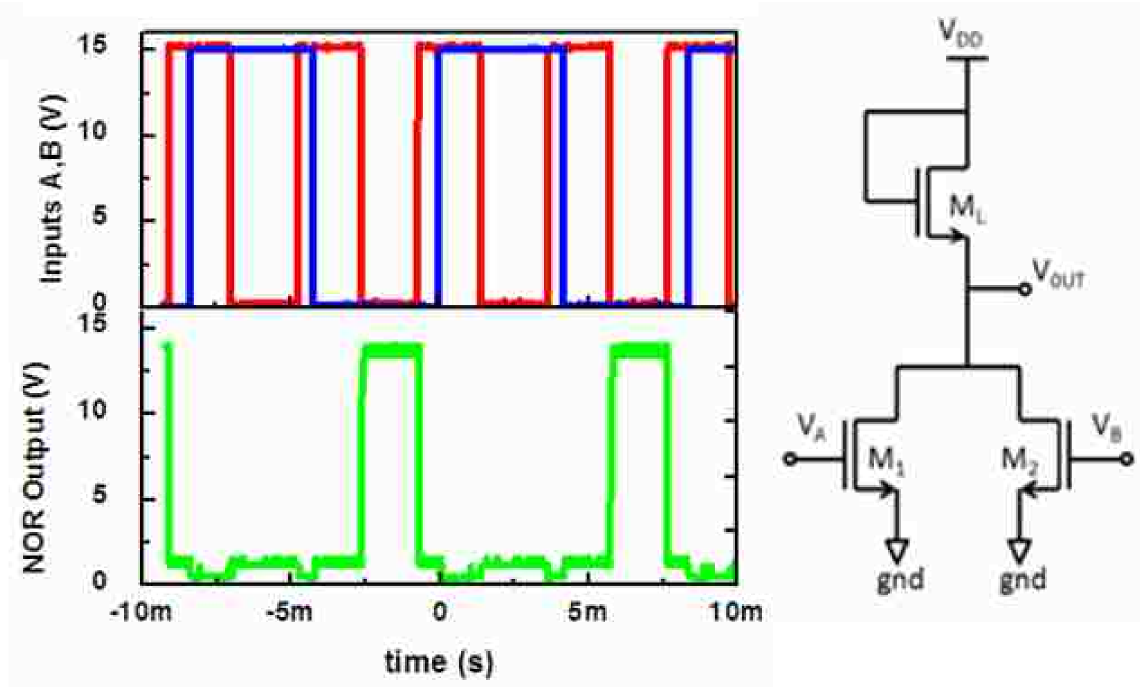


Figure 6.13 a-IGZO based Pseudo NOR circuit and logic level conversion

6.5 a-IGZO based Ring Oscillators

Ring oscillators are typically used as the voltage-controlled oscillator of most phase locked loops [6.16]. They are also a basic circuit to benchmark the performance of a technology. The oscillators are composed of odd number of inverter stages connected back-to-back, with the output of the last stage connected back to the input of the first one (Fig 6.14). When a supply voltage is applied to this type of configuration, the gates of the transistors in a particular stage drift towards a low or high potential. This in turn causes a voltage swing in the output of that particular inverter, forcing the following inverter to swing as well. This sequence is continued until the original stage is reached and its input

gate forced to the opposite state. This process repeats indefinitely, causing the circuit to oscillate at a characteristic free running frequency. The propagation delay of per stage is related to the oscillation frequency and given by:

$$t_{PD} = \frac{1}{2N.f_{oscillation}} \tag{6-1}$$

Ring oscillator characteristics such as number of functional stages (device yield), oscillation frequency (device speed), and operating voltages (functionality) can help benchmark the technology capability.

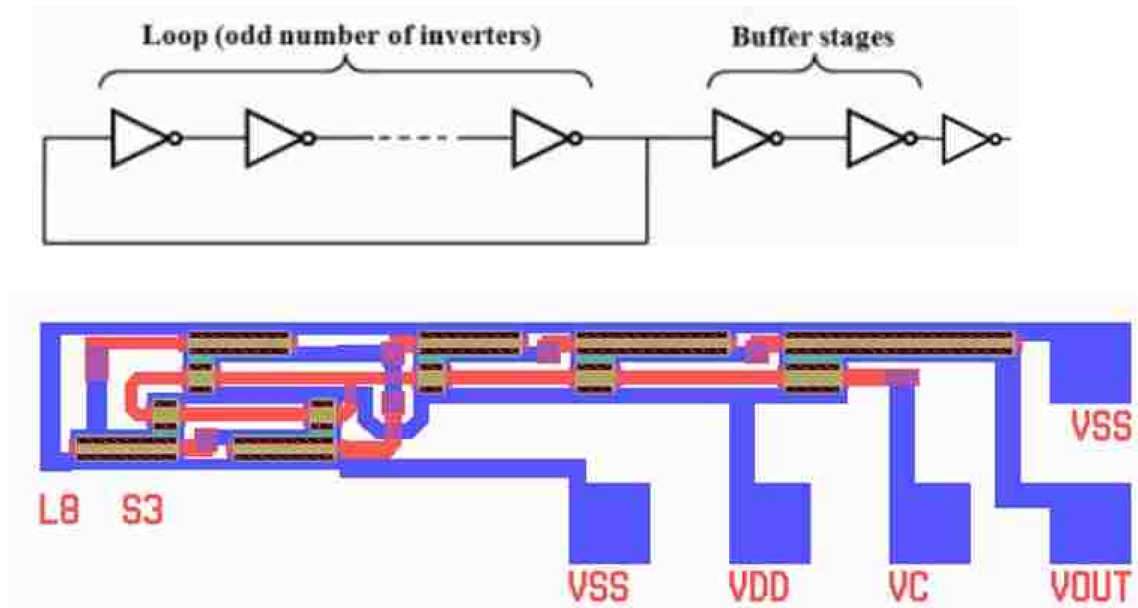


Figure 6.14 Circuit schematic and LEdit layout of a 3-stage Ring Oscillator with 8μm channel length and 3 additional output buffers to prevent loading.

Dynamic properties of a-IGZO TFTs are as important as static properties for applications of TFTs to active-matrix displays. Ring oscillator circuits can also be used to estimate the operation frequency of circuits under the influence of parasitic capacitances and

resistances, but more importantly to ascertain whether TFTs can charge/discharge capacitive loads. We designed and fabricated various ring oscillator circuits with different beta ratios for dynamic characterization of these devices. Oscillation frequencies of the ring oscillator were measured at different supply voltages. Propagation delay was then calculated by dividing the oscillation period with the number of stages at each supply voltage level. The a-IGZO based ring oscillators were fabricated on highly flexible and dimensionally stable 100 μm thick Ni-Fe alloy metal foil for this study. The low and nominally constant coefficient of thermal expansion over a wide range of temperature and excellent mechanical and chemical robustness of Ni-Fe alloys affords implementation of circuits with smaller design features. The dynamic characteristics of the IGZO TFTs are evaluated from 3 stage ring oscillator circuits (L_{load}=L_{drive}=8 μm,

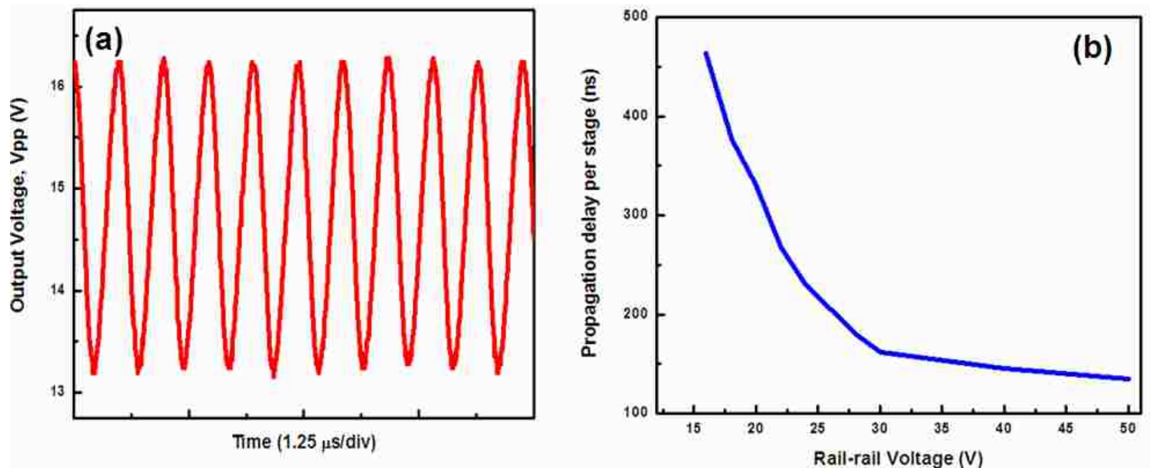


Figure 6.15 Characteristics of 3 stage IGZO ring oscillator on Ni-Fe foils (L_{load}=L_{drive}=8 μm, W_{load}=32 μm, W_{drive}=256 μm); (a) output swing, (b) propagation delay with increasing supply voltage

W_{load}=32 μm, W_{drive}=256 μm), exhibiting oscillation frequency of 360 KHz when non-flexed at a supply voltage of 15 V in Figure 6.15. At a larger supply voltage of 50 V, the

oscillation frequency is 1.065 MHz corresponding to single stage propagation delay of 156 ns which is faster than reported values of RF sputtered IGZO TFT based circuits on a flexible platform [6.12]. Circuit operation is also confirmed with minimal change when devices are flexed.

6.6 Clocked a-IGZO Based Digital Circuits

A majority of the work however, has focused on optimization of discrete devices as opposed to complete device integration. From the viewpoint of application of TFTs to realizable circuits, the dynamic characteristics of the TFTs are of paramount importance. In this regard, shift registers can be used as a good benchmark as they are the most commonly employed scanning circuits for sequential addressing of matrix based systems such as displays and sensors. In this section, we demonstrate a half-bit and full-bit shift register with maximum operating frequency of about 40 kHz from bottom gate staggered-structure a-IGZO TFT. The present results suggest that a-IGZO TFT technology doesn't suffer from slow states and has the potential to realize practical integrated circuits for demanding applications such as flat panel displays with operating speed much faster than a-Si:H TFT technology.

6.6.1 Design of Half Bit Shift Register Circuit based on a-IGZO TFTs

This half-bit shift register design employs a pseudo n-type, serial input, parallel output circuit which uses non-overlapping two-phase clock signals (*ClkA* & *ClkB*) for timing and shifting of a synchronized input (sync) signal [17]. In turn, this sync signal is

buffered to each addressed line controlling a display [6.6], sensor or memory array. Single stage schematic of the half bit shift register is depicted in Figure 6.16(a). Besides power supply (V_{dd}) and ground (V_{ss}), there is an extra fixed supply terminal, V_c, which is a control voltage for all the load transistors. The control voltage makes it possible to adjust the effective resistance of the load transistors so that optimum performance can be achieved. In a more compact design it may be desirable to eliminate the control voltage (possibly by connecting it to the supply voltage) to reduce the number of external connections (i.e. for highly integrated display modules) [6.18]. In this case, great care has to be taken to size the load transistors. The sync signal is received from the previous stage (its S_o port) via the stage S_i terminal and is outputted to the next stage (its S_i port) via the stage S_o terminal. The clock terminal of every odd stage receives the *ClkA* as opposed to every even stage that receives the *ClkB*.

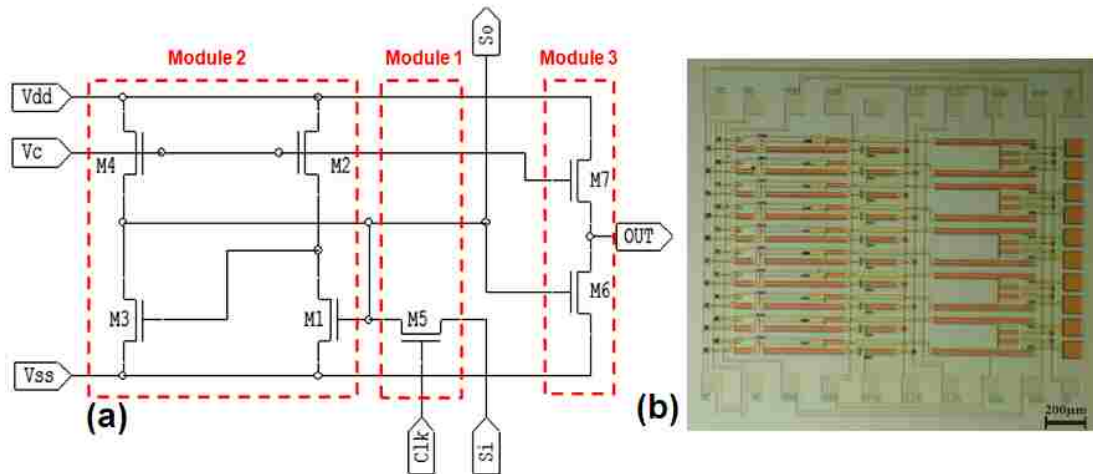


Figure 6.16 (a) Schematic of a single stage, pseudo n-type half-bit shift register. L_{M1-M7} =10um and W_{M1}=400um, W_{M2}=80um, W_{M3}=100um, W_{M4}=20um, W_{M5}=150, W_{M6}=500, W_{M7}=100um. (b) Optical micrograph of a-IGZO half-bit shift register with 10 stages. Scale shown is 200µm.

Each stage of the half-bit shift register consists of only seven transistors with constant channel length of 10µm but with different channel widths which are selected based on the operational use of associated TFT devices to obtain optimum performance. Three independent modules can be distinguished from each stage. The first module is a switching unit which consists of only a single transistor (M5) that transmits the sync signal from the previous stage to the second module of the current stage every time its gate terminal is selected (pulled to the high voltage) by the clock pulse. The second module is a latching element which effectively withholds the charge during the time that stage is not addressed (i.e. frame time of a display). This module consists of two independent inverters in a loop. The first inverter, comprising of M1 and M2 TFTs, is in forward direction with respect to the propagation direction of the signal in the stage as opposed to the second inverter (M3, M4) that is in reverse direction. Drive transistor M1 is designed to be as large as 400µm wide to ensure sufficient driving power to charge up the next module. The third module is a buffer or an inverter which comprises of TFTs M6 and M7. The transistor M6 is a relatively large TFT in order to drive the output loads. All the load transistors (M2, M4, and M7) are designed with a W/L ratio to achieve a reasonable rise time and supply voltage level (power consumption) and to permit sufficient output pull down at a reasonable fall time. The Aim-Spice software package is used to simulate the performance of a-IGZO inverters and a load over drive TFT W/L ratio of about 1/5 is deemed satisfactory. This ratio has been consistently employed for all the inverters in the design. The layout of the half bit shift register includes ten stages

with 125μm pitch size which occupies an effective (without pads) area of about 2.2mm^2. The optical micrograph of the fabricated half bit shift register is shown in Figure 6.16(b).

6.6.2 Performance of Half Bit Shift Register Circuit based on a-IGZO TFTs

The output characteristics of the half bit shift register at a clock frequency of 20kHz is depicted in Figure 6.17. While sync signal is at Hi voltage level, the 1st stage receives the *ClkA* pulse (P_{A1}) which programs the stage latch. The output signal of the latch is then inverted and outputted by the buffer stage. The output of 1st stage (Out1) stays Hi until it receives the second *ClkA* pulse, P_{A2} (at this instant the sync signal is at Lo level). In the mean time, while the Out1 is still at Hi, the latch of 2nd stage is enabled by the *ClkB* pulse (P_{B1}) and is programmed by the S_o signal of the first stage. This sets the second stage output (Out2) to Hi. Thus, from rising edge of P_{B1} to P_{A2}, both Out1 and Out2 are at Hi level. Out2 returns to Lo level as soon as the stage receives the second *ClkB* pulse, P_{B2} (at which instant the 1st stage has been reset). This sequence continues all the way to the last stage and resumes back from the 1st stage with another sync pulse.

To complete a 12 V output swing, maximum fall and rise time of about 12μs and 9μs is measured respectively. This suggests that a maximum operating frequency of about 47kHz is attainable; however, the present design and process technology gives a maximum operating frequency of 40kHz since optimum performance for all stages is not obtained at higher frequencies. The supply voltages, to obtain 12 V output swing, are about 12 V, -11 V, and 5 V for V_{dd}, V_{ss}, and V_c respectively. This is while the clocks and sync signals have amplitude of about 14V and 10V respectively. We have also confirmed

operation of the circuit at minimum rail to rail supply voltage of 15V but it substantially increases the fall and rise time and limits the maximum operating frequency to only 10kHz.The minimum transition time is obtained with a rail to rail supply voltage of 20 V.

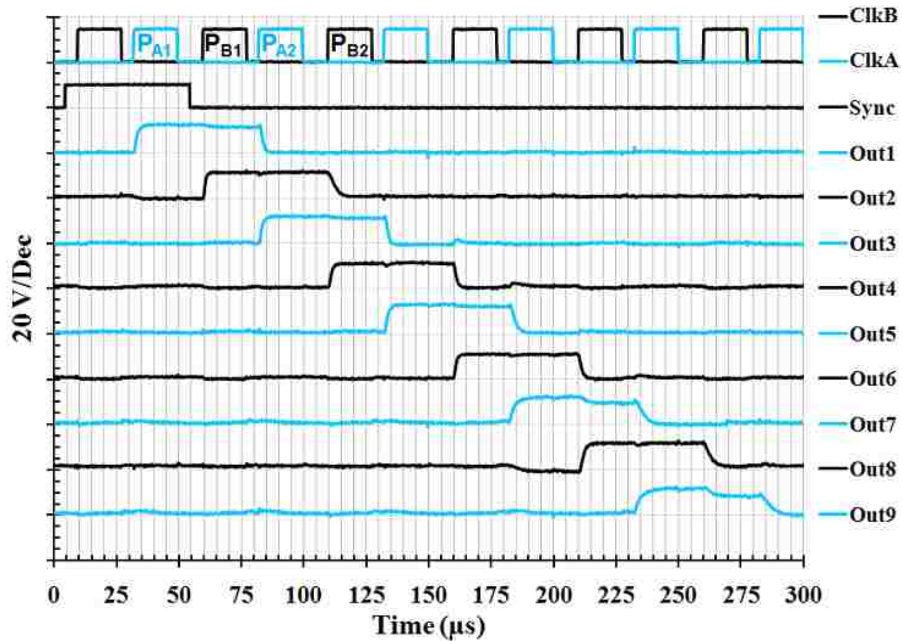


Figure 6.17 Output characteristics of nine consecutive stages of IGZO half bit shift register at 20kHz clocking frequency.

6.6.3 Full Bit Shift Register Circuit Implementation based on a-IGZO TFTs

In contrast with half bit shift register architecture, the full bit shift register is designed to scan an array of pixels in a way by which not more than a single line is addressed at a time. This is particularly beneficial for large size displays where sub-pixels are placed in a single row (not square) or for large area and low resolution sensing systems. As depicted in Fig. 6.18(a) the full bit shift register is constructed of five distinguishable modules. The second and fourth modules are latching elements that are formed by two inverters in a loop with one inverter in forward direction (Module 2: M1

& M2; Module 4: M7 & M8) and the other in reverse (Module 2: M3 & M4; Module 4: M9 & M10) with respect to the propagation direction of the signal in the stage. The sync

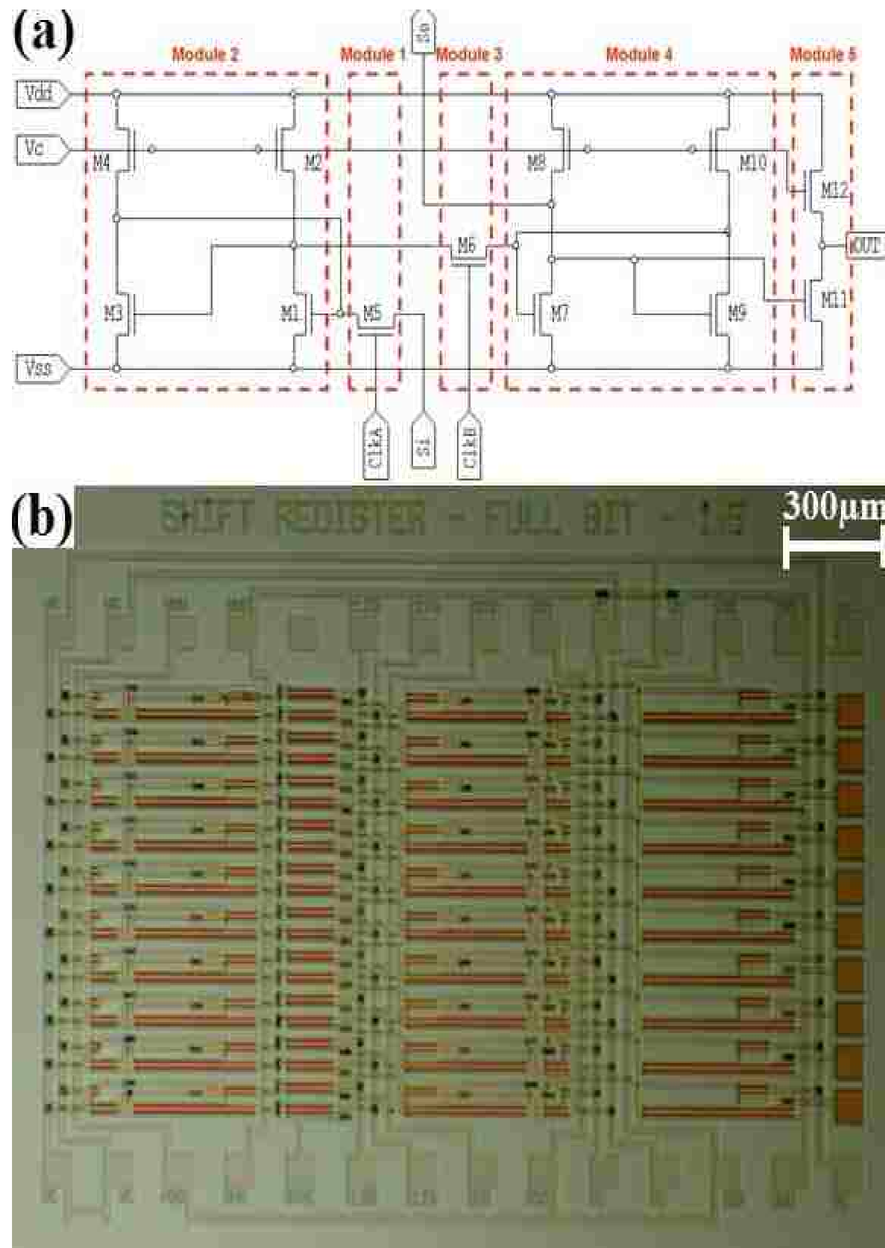


Figure 6.18 (a) Circuit schematic and (b) Optical micrograph of the a-IGZO full bit shift register.

signal is imported into the stage and stored in the first latch (module 2) via S_i terminal and transistor M5 (module 1) with its gate controlled by *ClkA*. The stored data of the first latch is introduced to the second latch (module 4) via transistor M6 (module 3) with its gate controlled by *ClkB*. The sync signal stored in second latch is then sent to the next stage, through S_o terminal, as well as the output buffer (module 5) which inverts the signal one last time. All the inverter structures consist of two transistors where one drives the output node while the other acts as a load. To ensure sufficient driving power and also to obtain reasonable transition speed, the channel width over length ratio (W/L) of the load TFTs is designed to be five times smaller than the drive TFTs. Furthermore, the gate terminals of the drive TFTs are independently addressed by a controlling signal (V_c) to obtain an optimum operating point for the circuit. A multiple stage shift register is formed by placing the stages side by side and serially connecting their sync input (S_i) and output (S_o) terminals. Optical micrograph of a ten stage full bit shift register is depicted in Fig. 6.18(b). The circuit layout with stage pitch size of 125μm and length of 2600μm occupies an effective area of about 3.25mm^2 (excluding the pads).

The full bit shift register output waveform for eight consecutive stages at clocking frequency of 10kHz is depicted in Fig. 6.19. In order to complete output swing of about 10V (for all stages), rail to rail supply voltage of 20V (Vss = -4V and Vdd = 16V) and control voltage of 5V is applied. The sync and clock pulses also have a peak to peak voltage value of 10V (0V to 10V) and 15V (-5V to 10V) respectively. First latch of the 1st stage is programmed with the sync signal as soon as it receives the A1 pulse. The B1 pulse then sets the second latch of the 1st stage and pulls down its output. Output of the 1st

stage is set upon receiving the B2 pulse since its first latch is reset by the sync signal during the A2 pulse. The 2nd stage is similarly programmed by the A2 and B2 pulses and

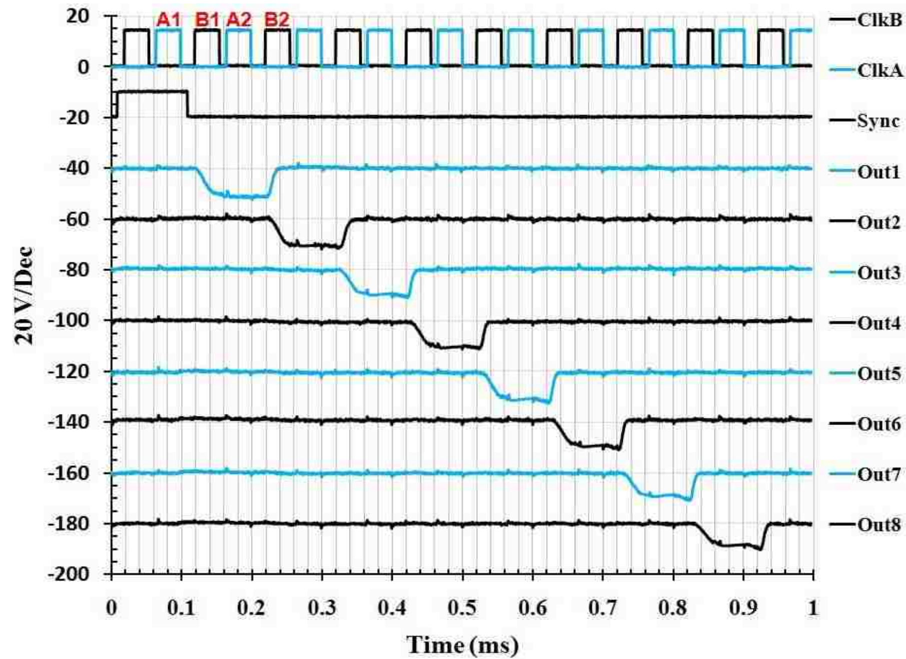


Figure 6.19 Output characteristics of 8 consecutive stages of IGZO full bit shift register

output of the 1st stage (its second latch) as the sync. Due to double programming of the sync signal in each stage, output pulses of adjacent stages do not overlap and therefore multiple-line addressing of the system-under-scan is avoided. Relatively long layout of the circuit causes a latency of about 5μs which is the time that takes for the stored data in the first latch to reach and charge up the second latch followed by the output buffer from the moment that stage receives a rising edge of the *ClkB* pulse. Single output buffer architecture of the circuit do not offer fall time and rise time faster than 30μs and 10μs respectively. This suggests maximum operating speed of about 25 kHz. The circuit is also fully functional at minimum rail to rail supply voltage of about 18V.

6.7 Display System based on a-IGZO TFTs

The development of a display system entails the incorporation of several components of different nature and function that are brought together by a controlled sequence of electronic signals. Material science of thin films and innovative processing techniques are tailored to device active components, such as transistors, with suitable performance levels. From the basic device structures, pixel units can then be built to regulate light emission. Once the active transistors have been characterized, implementation of the basic display elements can follow.

6.7.1 a-IGZO Based Pixel Circuit for Active Matrix OLED Display

The active pixel element can be designed using only two transistors. The first transistor would act as a sampling switch that can read a voltage signal from a data line and pass it through to the second transistor. This voltage is used to control current flow of the drive transistor and is stored on the pixel capacitor. In order to determine the optimal sizing of all these components, parameters such current drive, leakage current and capacitance are essential. In a VGA size display with a typical refresh rate of 60 Hz, pixel times as low as tens of microseconds are all that is needed in order to program the right light level. Furthermore, the current level which is to remain constant through the entire frame cycle is controlled by the parameters discussed above; this makes it crucial to have a good understanding of the dynamic properties of the active pixel. The circuit schematic of a 2TFT-1Capacitor pixel and corresponding layout of the same is shown in Fig 6.20

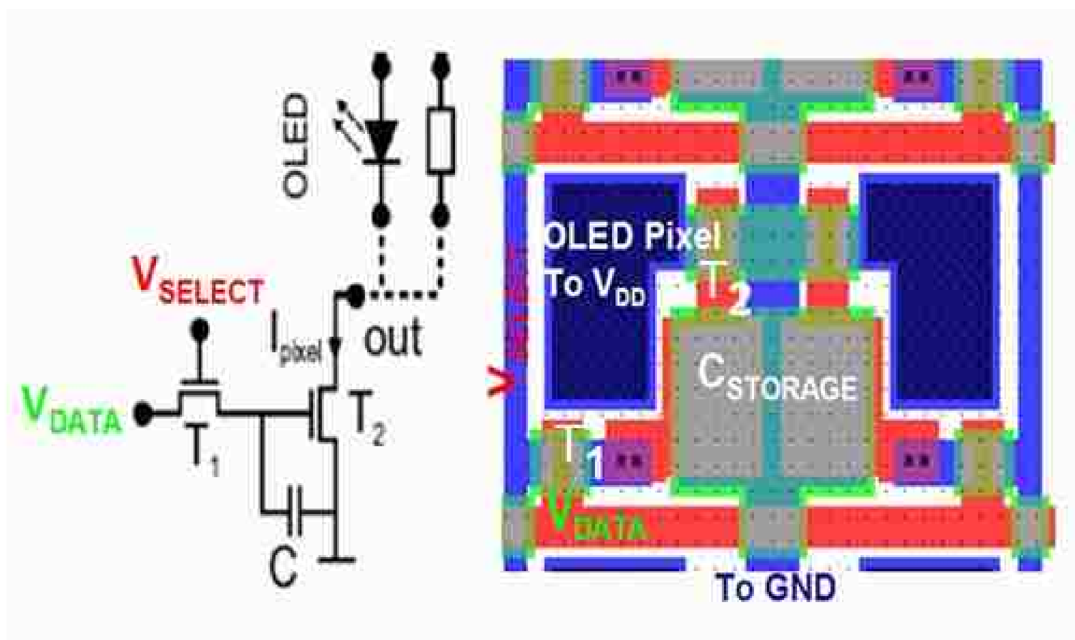


Figure 6.20 Circuit schematic and mask layout of active matrix OLED pixel.

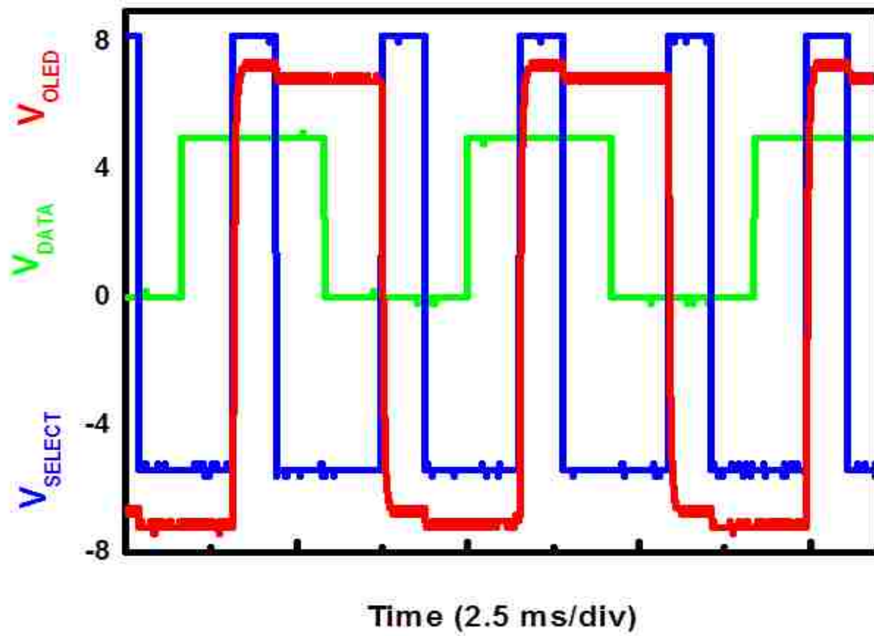
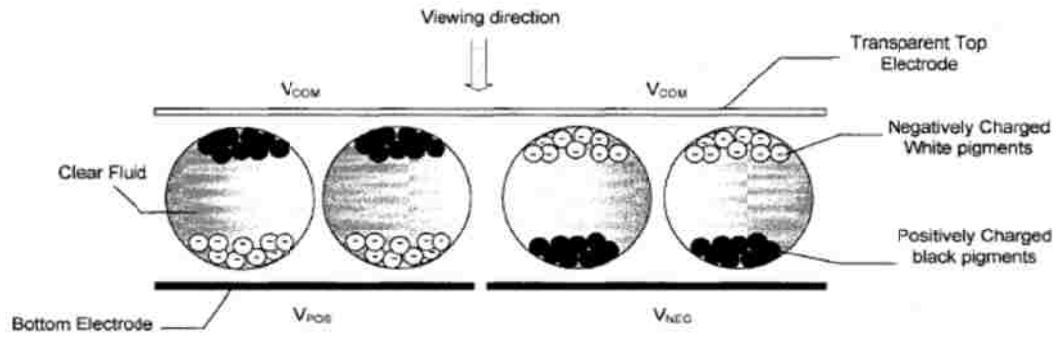


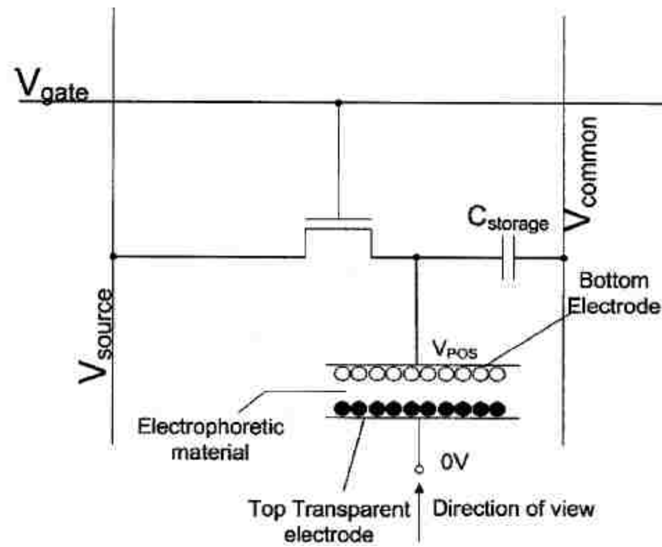
Figure 6.21 Driving of an OLED with a-IGZO based pixel circuit

Both the switching and drive TFTs (T_1 and T_2) have identical dimensions (W/L=80μm/10 μm). To mimic the load, a 520 kΩ resistor was used instead of the actual OLED device. The driving scheme of the pixel circuit was with a V_{SELECT} (-5V, 8V, 120Hz, 20% duty cycle) signal to selectively address the pixel and with a V_{DATA} (0V, 5V, 120Hz, 50% duty cycle) signal to pass on the data to be retained during the frame time. V_{OLED} can be correlated to current flowing through the pixel. As we can see from Fig 6.21, the charging of the capacitor according to V_{DATA} coincides with the onset of V_{SELECT} signal and the state is retained until the end of the scanning period. The V_{OLED} is modulated at 120 Hz as expected and can be related to modulation of luminescence from an actual OLED device.

6.7.2 a-IGZO Based Electrophoretic Display

We partnered with the Flexible Display Center at Arizona State University to demonstrate an electrophoretic display with a-IGZO TFT backplane developed in our lab. Electronic display can be dynamically rewritable and compatible with digital components. Information can be stored in the external device and this obviates the need to print out loads of documents. Electronic paper or E-paper consumes ultra low power with high brightness and contrast ratio with full viewing angle. Microencapsulated electrophoretic The microcapsule consists of negatively charged white and positively charged black pigments chips suspended in a clear fluid as depicted in Fig 6.22. Application of a negative voltage on the top electrode will accumulate the positively charged black pigments near the top electrode and when viewed from the top will appear as a black





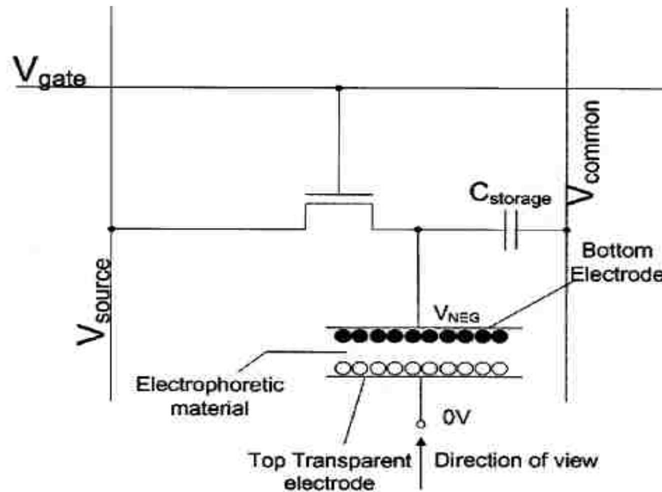


Figure 6.22 Cross section of microcapsules and voltage addressing of black/white image material pioneered by E-Ink Corporation can enable E-paper displays with such desirable attributes. [Adapted from Ref 6.19].

image. The opposite phenomenon happens for the white pigments and gray scale images can be displayed in this manner. The inherent bistable nature of the microcapsules ensures that they can hold their current state without the need for any voltage application. This unique feature enables ultra-low power consumption and makes many applications such as E-paper displays feasible.

Fig 6.22 also shows the driving scheme of the electrophoretic material with a single pixel circuit of an active matrix backplane. It consists of a-IGZO TFTs deposited and fabricated at Lehigh, a source or column line, a gate or row line and a storage capacitor. The top electrode of the storage capacitor is tied to the electrophoretic material. The gate line is enabled when the data is ready on the corresponding source line. This data is transferred to the storage capacitor which is used to hold the data for a row time. The electrophoretic material will experience a change in voltage and switch the pigments to black or white depending on the voltage. A V_{POS} on the anode (bottom electrode) will turn the black pigments and a V_{NEG} will turn the white pigments toward the viewing side. A 0V on the storage capacitor make the electrophoretic material to hold its previous state. A QVGA (240x320 pixels) display was integrated at the Flexible Display Center with a-IGZO TFT backplane fabricated at Lehigh. The display has a 3.8" diagonal area with a pixel size of 240μm x 240μm. The display was driven using an AM100 Active Matrix EPD prototype Kit. Fig 6.23 shows a 16 level gray scale image being updated on a QVGA electrophoretic display on Si substrate at a frame rate of 50Hz. The average drive current is 65μA with the drive current map of the pixel array shown in the figure.

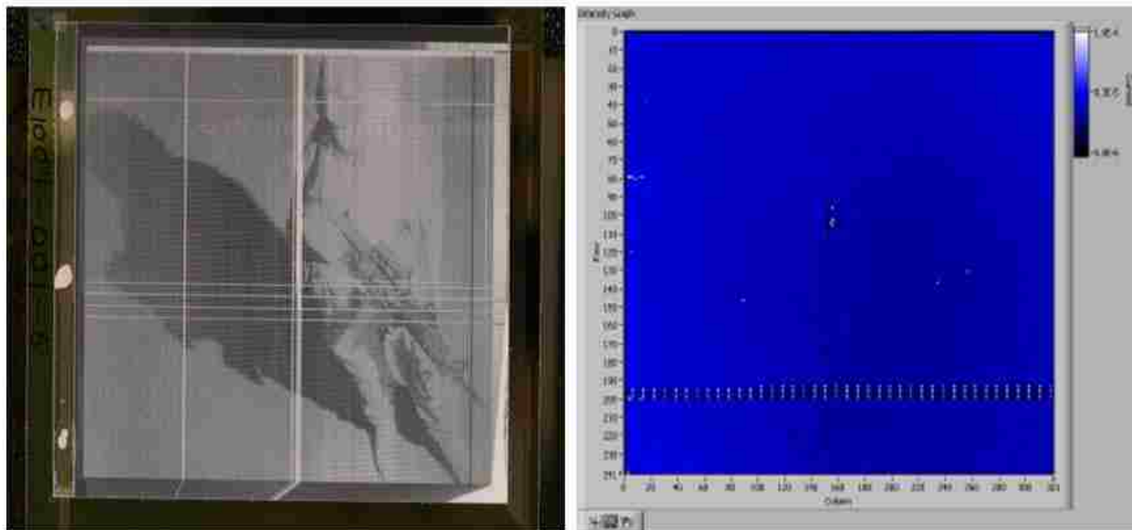


Figure 6.23: a-IGZO TFT base active matrix backplane QVGA (320 x 240 pixels) display image and corresponding drive current map of the array

6.8 Conclusion

In this chapter we have demonstrated a whole range of circuits on thin flexible metal foils using a-IGZO TFTs. The circuits can be used as building blocks for integrated electronics that employ a-IGZO TFT technology. The relative high performance of the fabricated circuits bodes well for integration of more involved circuits to drive active matrix displays or other large area electronic systems. NMOS only circuit configurations are possible with current a-IGZO TFT technology and limitation of a suitable p-type oxide material is a bottleneck for CMOS operation. A complementary technology analogous to CMOS is highly desirable for low power conversion, low heat dissipation, high packing density, large output swing and better noise margin. The development of p-type AOS (amorphous oxide semiconductor) have proven elusive so far, but we believe

that ongoing research and development efforts devoted to realization for a p-type oxide TFTs are not only timely but quite justified since the payoff is so much larger.

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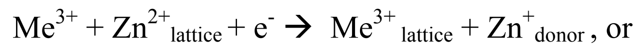
Chapter 7

Observation of Persistent n-type behavior in N_2 Doped RF Sputtered ZnO From TFT measurements: Clues From Rigorous Ab Initio Calculations

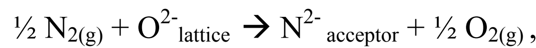
7.1 Introduction

Current n-channel TFT technology (like a-IGZO) is quite analogous to NMOS silicon based technology. The development of robust p-type oxide semiconductor for use as channel materials in TFTs remains a considerable challenge. While significant advances have been made in identifying and depositing new wide-bandgap materials for applications in optoelectronics, a high performance p-type TFT has remained elusive. The availability of p-channel and n-channel oxide based semiconductors can have huge technological and commercial implications since realization of CMOS-like technology with low power consumption, simple circuit architecture and analog and digital circuitry

will be possible. ZnO is intrinsically n-type semiconductor and realization of p-type ZnO has proven similarly challenging, albeit very desirable. Experimental and theoretical quest for p-conductivity in ZnO is also motivated by the design needs for p-type ZnO-based solid-state lighting sources in the form of LEDs and laser diodes. Among the concepts for engineering design of ZnO-based TFTs, LEDs and laser diodes is substitutional doping of oxygen or zinc in their lattice positions by elements of different formal charge which generate donor or acceptor centers by 'valence induction', e.g.

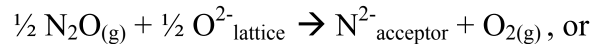


$$Me^{3+} + Zn^{2+}_{lattice} + e^{-} \rightarrow Me^{3+}_{lattice} + Zn^{+}_{donor}\text{, or}$$

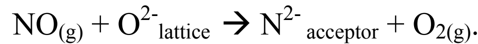


$$\tfrac{1}{2} N_{2(g)} + O^{2-}_{lattice} \rightarrow N^{2-}_{acceptor} + \tfrac{1}{2} O_{2(g)}\text{,}$$

and from nitrogen oxides:



$$\tfrac{1}{2} N_2O_{(g)} + \tfrac{1}{2} O^{2-}_{lattice} \rightarrow N^{2-}_{acceptor} + O_{2(g)}\text{, or}$$



$$NO_{(g)} + O^{2-}_{lattice} \rightarrow N^{2-}_{acceptor} + O_{2(g)}.$$

Upon excitation, the donor centers pass the electron to the conduction band and the acceptor centers create holes by removing an electron from the valence band. The conditions for successful doping for n- or p-conductivity require that energy of the donor centers be close to the bottom of the conduction band (BCB), and the acceptor centers be close to the top of the valence band (TVB), i.e. that the valence induction doping generate shallow donors for n-conductivity and shallow acceptors for p-conductivity. Focusing on p-ZnO, extensive experimental effort has so far yielded less than convincing evidence that p-conductivity can be achieved by anion doping, such as by nitrogen substitution of the lattice oxygen of ZnO [7.1-7.10] A simple cause of the failure was found in the

theoretical result pioneered by Van de Valle et al. [7.1] that N- substitution of lattice oxygen generates *deep* acceptor centers, not the desired shallow acceptors.

In this chapter, we address whether the theoretical result for nitrogen-doped ZnO is reproducible by performing calculations using different platforms and in addition examining the effects of structural distortions, spin polarization and spin-orbit coupling which have so far not been considered; we also show that different types of N-doping in a ZnO TFT circuitry results only in a decrease of the native n-conductivity of ZnO but not giving rise to p-conductivity, a result expected from deep acceptor centers.

7.2 N-doping of ZnO

7.2.1 N as a Substitution Dopant in ZnO

N-doping in sputtered ZnO thin films-There has been a large amount of effort expended so far by various groups to realize p-type ZnO using nitrogen (N) as a possible shallow acceptor dopant. For substitution on the O site, N is expected to be an acceptor that is closest to O in terms of atomic size and electron configuration, $1s^2 2s^2 2p^6$ for the closed-shell O^{2-} and positively charged N^{2-}. In addition, N has been conclusively shown to act as a shallow acceptor in another II-VI semiconductor, namely ZnSe, enabling the design of LEDs and lasers [7.8-7.10]. The N acceptors may also be compensated if there are donor centers in a greater abundance than that of the acceptors. This acceptor compensation can happen via the formation of defects such as O vacancies, complexes with Zn interstitials or N_2 molecules [7.11-7.13]. The key challenge is thus to introduce acceptors without being overwhelmed by compensating donors. As a nitrogen source,

some researchers used N_2O gas, which is a mild oxidizing gas stronger than O_2 and weaker oxidant than NO_2 [7.14-7.15]. The idea of using oxidizing environment may be traced to the desire to keep the acceptor centers in positively charged state, and when ionized, to prevent neutralization of electronic holes in the valence band by reducing agents that supply electrons for this process. A number of experimental efforts resulted in reports of *p*-type ZnO using NH_3 in CVD [7.16], an atomic N source in MBE [7.17], NO [7.18], N_2O [7.19], diallylamine [7.20] and NH_3 [7.21] as N doping sources in MOCVD; metalorganic MBE [7.22] and plasma-assisted MBE using a NO source [7.23] or a mixture of N_2 and O_2 [7.24] have also been tried. The oxidation of sputtered Zn_3N_2 thin films was reported to yield *p*-type ZnO [7.25] as was N implantation of sputtered ZnO thin films [7.26]. Guo et al. [7.14] used N_2O plasma for nitrogen doping of ZnO film by PLD. They found that nitrogen doping was enhanced using the active N formed by N_2O gas flowing through an electron-cyclotron-resonance (ECR) source.

7.2.2 Doping of RF Sputtered ZnO by N_2, N_2/O_2, N_2O and PECVD N_2O Treatment

We investigated N-doping of ZnO thin films deposited by RF sputtering using N_2, N_2/O_2 and N_2O in-situ during sputtering as well as treating the undoped films with N_2O plasma in a PECVD chamber. Carrier conduction and transport was verified from current-voltage characteristics of fabricated bottom-gate staggered structure TFTs (Thin Film Transistors). The sputtering was carried out in a Kurt J. Lesker 4-target capable, cryo-pumped backed sputtering machine. The undoped ZnO thin films were sputtered from 99.999% purity ZnO target in an argon and oxygen (10:1) ambient onto SiO_2 (2KA^o)

coated Si wafers. The base pressure in the sputtering chamber was about 10 mTorr and the RF power was 400 watts. The conductivity and carrier concentration as determined from four-point and hall measurements for the undoped ZnO thin film was 4×10^{-2} (Ω-cm)$^{-1}$ and 3×10^{18} cm^{-3} respectively. In an $Ar/N_2/O_2$ (10:1:1) ambient, the conductivity and carrier concentration was reduced to 8×10^{-4} (Ω-cm)$^{-1}$ and 8×10^{16} cm^{-3} respectively. In an N_2O assisted deposition (N_2O/Ar), the conductivity was further reduced to 9×10^{-6} (Ω-cm)$^{-1}$. One set of undoped ZnO thin films were subjected to N_2O plasma treatment in a PECVD chamber at 500 mTorr of total chamber pressure and a N_2O flow rate of 720 sccm at different plasma power (500-800 Watts) in an effort to enhance N-doping similar to work of Guo et el. [7.14]. The resulting films had conductivity around 1×10^{-6} (Ω-cm)$^{-1}$. In all of the above cases of N-doping, no carrier conversion was indicated from the Hall data. Table 7.1 provides a summary of the conductivity of the different N doped sputtered ZnO films with thickness of around 70 nm; the carrier concentration of the N_2O treated samples could not be determined due to limit of the measurement apparatus.

Table 7.1: Comparison of conductivity and carrier concentration of various N-doped sputtered ZnO thin film samples

Sample	RF (Watt)	N_2O plasma	Conductivity (ohm-cm)$^{-1}$	Hall mobility (cm^2/V.s)	Carrier concentration (cm^{-3})
[a]Undoped ZnO	400	No Post-Treatment	$4X10^{-2}$	9	$3X10^{18}$
[b]N_2 assisted ZnO	400	No Post-Treatment	$8X10^{-4}$	20	$8X10^{16}$
[c]N_2O plasma ZnO	400	Treated at 500 W	$9X10^{-6}$	NA	$< 10X10^{14}$
[d]N_2O plasma ZnO	400	Treated at 800 W	$5X10^{-6}$	NA	$< 10X10^{14}$

[a]Sputtered ZnO sample in Ar/O_2 ambient; [b]Sputtered ZnO sample in $Ar/O_2/N_2$ ambient; [c,d] Samples are sputtered ZnO thin films doped by plasma N_2O in PECVD

The structural, electronic and optical properties of sputtered ZnO films are strongly influenced by the various processing conditions, such as gas phase compositions, plasma conditions and deposition temperature. In the undoped ZnO, excess, interstitial Zn ions or oxygen vacancies can contribute free electrons for electrical transport. For growth above a critical partial pressure (~10^{-5} Torr in our case), we believe the undoped films became close to stoichiometric with fewer structural defects and had high resistivity. From AFM imaging, the films exhibited granular morphology with average grain size around 20 nm. As is obvious from Table 7.1, the conductivity decreases for ZnO doped with N_2 in an N_2 sputtering ambient. However, higher hall mobility is obtained with reduced carrier concentration (Fig 7.1). This type of carrier transport contrasts greatly with that observed

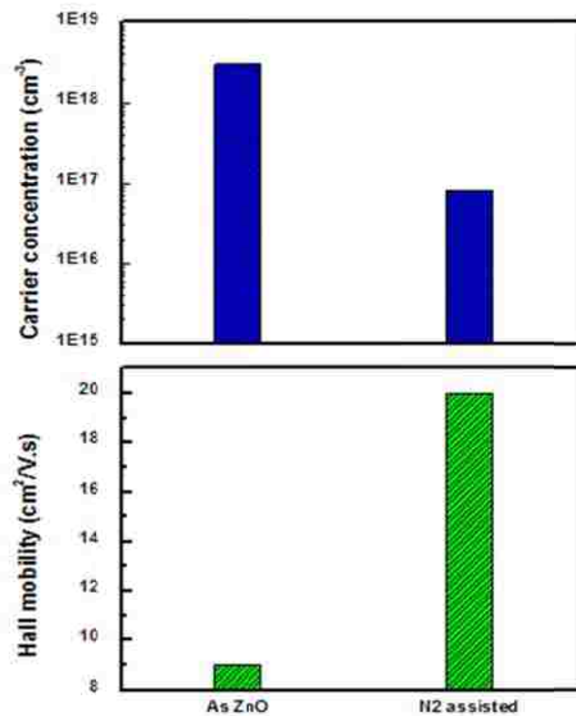


Figure 7.1 Hall mobility and carrier concentration of RF Sputtered undoped and N-doped ZnO thin films.

for multicomponent amorphous IGZO, where the hall mobility decreases as the carrier concentration goes down. Both are composed of post-transition metals and have possibly direct overlap of spatially spread ns orbitals of neighbouring metal cations. As a result, a highly ordered crystalline structure is not needed to achieve high mobility. The relationship of mobility and carrier concentration in such a case can be characterized by the dominance of an impurity scattering in carrier transport [7.27]. The deviation of the films from the degenerate conducting ZnO film may have resulted from lowering the Fermi level further away from the conduction band bottom associated with the decrease in electron carrier concentration. In an N_2/O_2 environment, the ratio required to reveal the effect of N_2 has to be adjusted so as to promote reactivity of N_2 more than that of O_2.

7.2.3 Results of TFTs from N-doped ZnO Films:

We then fabricated bottom-gate TFTs with the various N-doped ZnO films described above as active channel (70 nm) with PECVD SiO_2 (100 nm) as dielectric and Au/Ti (100nm/20nm) as source/drain contacts. TFTs showed persistent n-type current-voltage characteristics from both undoped and N-doped ZnO TFTs (Fig. 7.2 (a)). The reduced carrier concentration of N-doped ZnO films (from $10^{18}cm^{-3}$ to $10^{16}cm^{-3}$) results in enhancement mode TFTs as shown in Fig. 7.2(b). For the undoped ZnO case, the TFT device could be turned off only after applying a large negative bias due to large carrier concentration in the films. The On/Off ratio, threshold voltage and mobility in the N_2 assisted TFTs were 10^6, 5V and 5.6 $cm^2/V.s$ as extracted from the transfer characteristics.

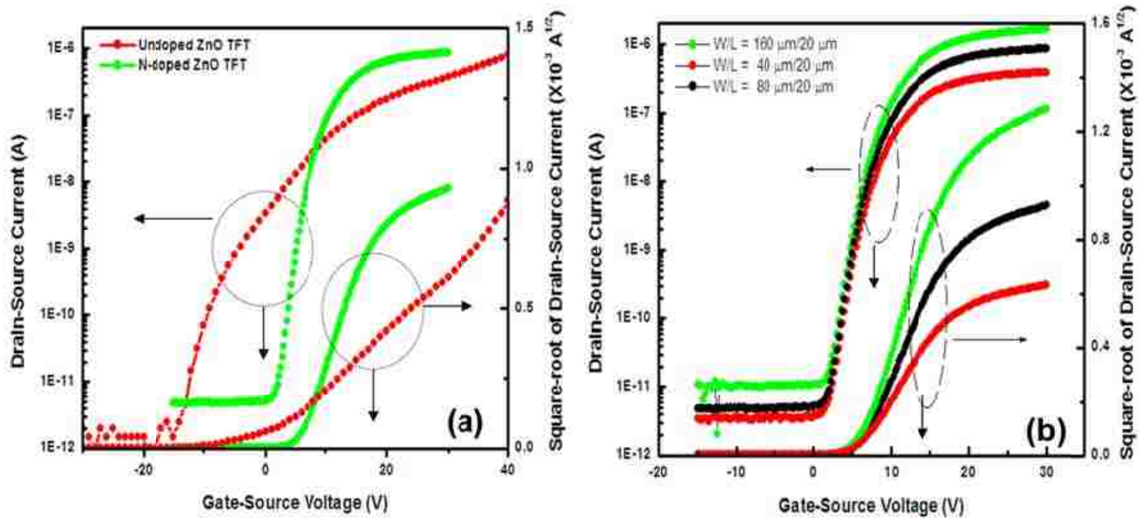


Figure 7.2 n-type conduction from both undoped (a) and N-doped ZnO (b) thin film as active channel in TFT. The figure shows the transfer characteristics (I_D-V_{GS}) of a discrete undoped and N-doped ZnO TFT with width and length ratio W/L=40μm/20μm at drain-source voltage V_{DS}=5V; (b) shows the transfer characteristics of N-doped ZnO TFT at W/L = 160μm/20μm, 80μm/20μm, 40μm/20μm at drain-source voltage V_{DS}=5V;

The TFTs scaled well with bias and geometry. The subthreshold slope improved by more than a factor of two (from 4V/dec to 1.5V/dec), wchich is indicative of lower trap state density in N_2 deposited TFT. Finally, in Fig 7.3, the transfer characteristics of TFTs from N_2O doping of as deposited ZnO films is shown and compared with the N_2 assisted deposition. Although all the TFT parameters deteriorated in the N_2O treated case (μ_{FE}~0.5cm^2/V.s, V_T~12V), what is significant is the relative reduction of Off-current which decreases with increasing RF power of the N_2O treatment. The reduction in off current can be directly attributed to the reduction of oxygen vacancy in the non depleted region at the top surface of the channel. The On current is also shown to decrease which is directly correlated to the reduction of effective carrier concentration in the films. It is

also seen from Fig 7.3(b) that N_2O doping during the depositions of the ZnO films had a greater effect in reducing carrier concentration resulting in further decrease in On-current.

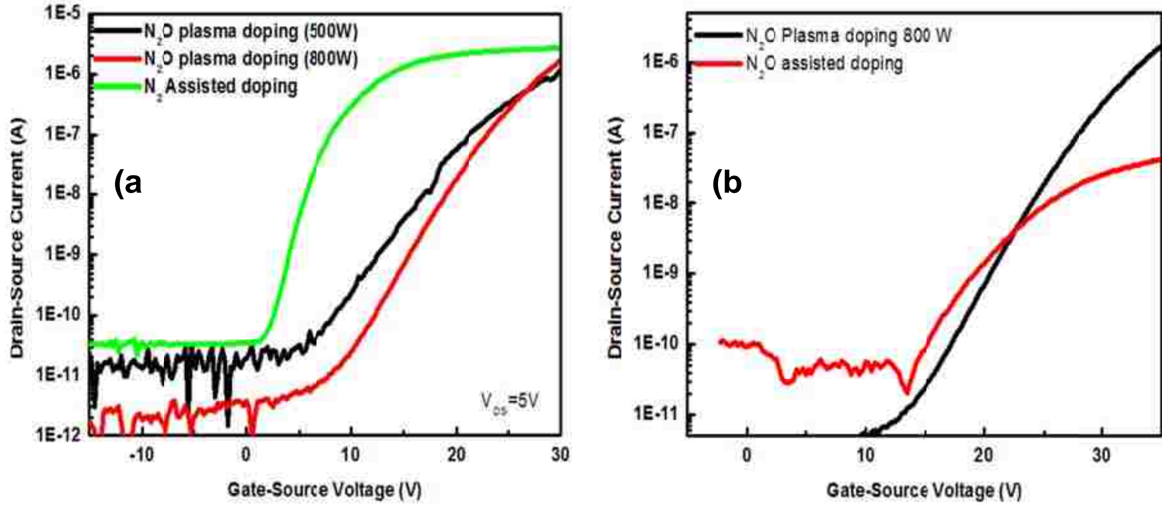


Figure 7.3 (a)The figure shows the transfer characteristics (I_D-V_{GS}) of a N_2-doped ZnO TFT and N_2O-doped TFT with width and length ratio W/L=160μm/20μm at drain-source voltage V_{DS}=5V; (b) Comparison of N_2O doping in plasma and sputter ambience.

7.3 Ab Initio Calculations of N-doping of ZnO

7.3.1 Theory

The computational work presented herein was largely due to the efforts of Dr. Kamil Klier. The computational platform used for all-electron calculations of the doped ZnO materials was the all-electron periodic DFT-FP-LAPW theory imbedded in the Wien2k-10.1 package [7.28]. In this set of codes, the crystal space is divided into atomic spheres in which the eigenfunctions are described by spherical harmonics, and interstitial space with plane waves that match amplitudes and derivatives at the interface with the atomic spheres. Reciprocal space is characterized by user-defined set of **k**-vectors,

presently 32 **k**-points for scf and dos calculations and 61 **k**-points for the band structure calculations. The currently used options included: optimization of atomic positions within the unit cells using the PORT routine, spin polarization (SP), and spin-orbit (SO) coupling using the second-variational method [7.29], and the modified Becke-Johnson potential (mBJ) that accounts well for bandgaps in wide-gap semiconductors [7.30]. Calculations with inclusion of the SP and SO options in Wien are carried out step-wise: First, the exchange-correlation potential is generated by a lapw0 routine; then in the lapw1c routine, the SP eigenvalues and eigenvectors are generated by solving the Kohn-Sham equations by diagonalizing the matrix of the system Hamiltonian in the basis of eigenvectors based on the density functionals for the spin-up and spin-down manifolds; this is followed by calculation of Fermi level and expansion of electronic charge densities in lapw2 routine; computation is done of core states and mixing of electron densities in the core and valence states in each scf cycle till convergence is attained. Presently we used the LDA functional [7.31] to scf convergence followed by recalculation using the mBJ potential, again to convergence. In both steps, SO coupling is added in the lapwso code which computes new eigenvalues and eigenvectors for the following steps which entail the generation of valence charge densities, core states, and re-entering the result into the next scf cycle till convergence is reached. The Hamiltonian for the SO step has the form

$$\hat{H}_{SO} = \frac{\hbar}{2Mc^2}\frac{1}{r}\frac{dV}{dr}\begin{pmatrix} \vec{\sigma}\vec{l} & 0 \\ 0 & 0 \end{pmatrix}, \tag{7-1}$$

where $\sigma_x, \sigma_y, \sigma_z$ are the Pauli-spin matrices, $\bar{l}$ is the angular momentum vector, *M* the relativistically enhanced mass of electron, and *V* is the potential within the atomic sphere. Application of $\hat{H}_{SO}$ couples the spin-up and spin-down eigenvectors calculated in the lapw1 step. The limitations are in that the SO procedure applies only to the space inside atomic spheres, not the interstitial space, and that only "small" spin-orbit interactions are calculated. However, none of these limitations have been encountered in the present study, as confirmed by comparison with SO-free calculations.

7.3.2 Models for ZnO-N

The models for the present calculations were derived from the crystal structure of wurzite ZnO in which the following substitutions were made: one nitrogen atom for lattice oxygen in ZnO-N. The unit cells contained 32 and 128 non-equivalent atoms in ZnO, and the internal coordinates were fully optimized within the fixed wurtzite crystal structure with parameters a = b = 0.325 nm and c = 0.520 nm such that the 32-atom cell was bounded by a = b = 0.650 nm and c = 1.040 nm and the 128-atom cell by a = b = 1.300 nm and c = 1.040 nm. The reason for carrying out calculations for the 128-atom supercell was to examine the effects of the defect concentration; in the model with repeating 32-atom cells, the nearest N-N distances are 0.325 nm, still of concern with interactions to form non-local acceptor bands, while in the repeating 128-atom supercells, the defects are separated by twice as large distance of 0.650 nm where such interactions are expected to be smaller. A comparison of the two calculations allows us to assess effects associated with changes in defect concentrations. Figure 7.4 shows a graphic

representation of the ZnO structures along with local structural motifs for the nitrogen dopant sites.

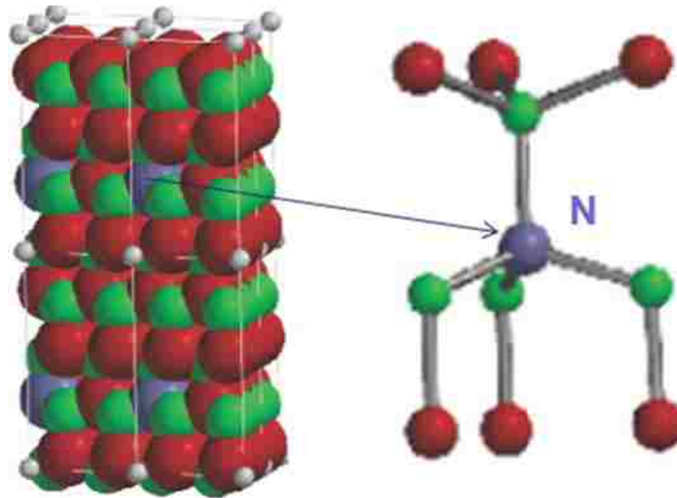


Figure 7.4 ZnO structure of repeating 32-atom cells with N substituted for lattice O. Two sets of calculations involved either one substituent atom in the 32 atom unit cell, or one substituent atom in a 128 atom supercell generated from four 32-atom unit cells. The ball models depict two such cell arrangements stacked along the principal hexagonal axis in vertical direction. Local motifs around the dopant sites are also shown in expanded form. Color coding: Zn … green, O … red, N … blue. The small grey spheres mark the corners of the unit cell and do not represent real atoms.

7.3.3 Theoretical Results

7.3.3.1 Structural Distortions

Structural changes caused by the dopants were determined by full optimization of internal coordinates with the following goals: (i) Do the substitutions cause significant distortions so as to yield incompatibility with the ZnO matrix, and (ii) Is electronic structure of the doped ZnO affected by the substitutions, and (iii) Do the structural distortions depend on the dopant concentration. The results show that introduction of the N defect does give rise to structural distortions of the original $P6_3mc$ ZnO lattice, up to

4-5%. Briefly, substitution of one lattice O atom by N results in a contraction around the nitrogen center, mainly in the crystal c-direction. The substitutions create close to perfect tetrahedral environment from the original ZnO structure which is compressed along the c-direction by ca. 2% from ideal hexagonal diamond structure. Furthermore, the distortions are very similar for the larger and the smaller unit cell, each containing a single dopant atom, and therefore they do not depend on the defect concentration within the range studied. It will be seen below, however, that changes in electronic structure do occur with changes in concentration.

Density of N^- states in N-doped ZnO showing spin-up and spin-down polarization. Empty acceptor states are at E > 0.

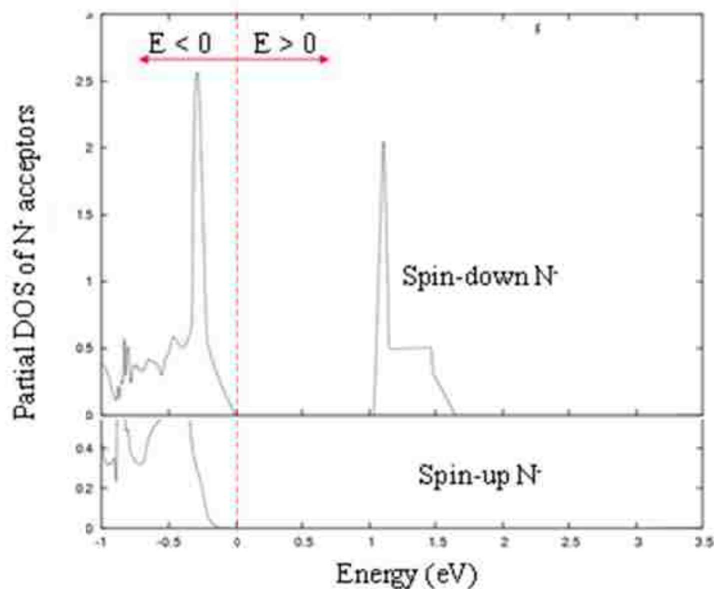


Figure 7.5 Partial DOS in the $Zn_{16}O_{15}N$ unit cell showing empty acceptor centers associated with spin-down nitrogen levels at 1.0 – 1.6 eV above the top of the O2p valence band. The notation N^- signifies the formal charge of nitrogen in the substitutional site for lattice oxygen, formally O^{2-}.

7.3.3.2 Electronic Structure of ZnO-N

The densities of states in the 32 and 128 atom unit cells of N-doped ZnO are represented in Figures 7.5 and 7.6. The corresponding energy band structure in the momentum space is represented in Figure 7.7.

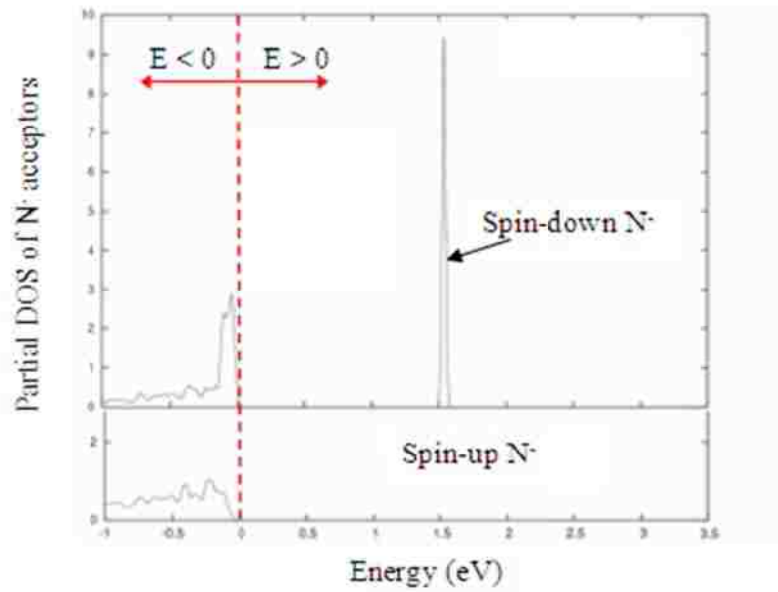


Figure 7.6 Partial DOS in the $Zn_{64}O_{63}N$ unit cell showing empty acceptor centers associated with spin-down nitrogen levels at 1.6 eV above the top of the O2p valence band.

The energy dispersion for the $Zn_{64}O_{63}N$ unit cell is similar, except for more flat nature of the intra-gap N acceptor level at 1.6 eV above the top of the valence band, as is also evident from the DOS plot in Figure 7.6. The N-acceptor bandwidth in the $Zn_{16}O_{15}N$ indicates interaction between the relatively highly concentrated nitrogens, which lowers the interaction-free energy in the diluted $Zn_{64}O_{63}N$ by some 0.6 eV, still however at undesirably high energy above the TVB.

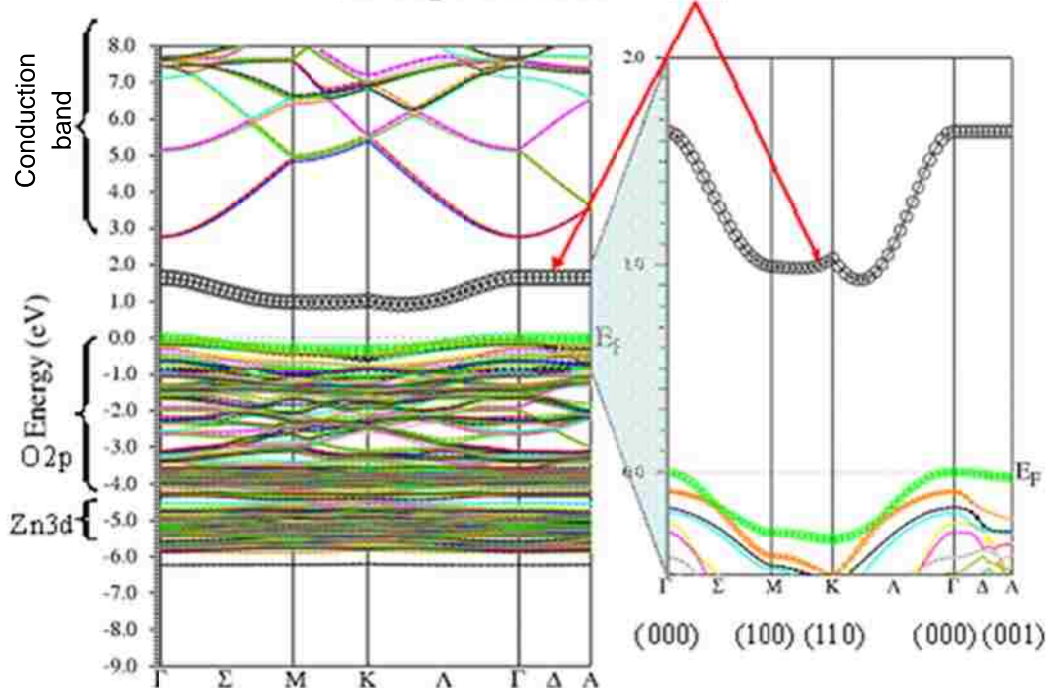


Figure 7.7 Energy dispersion curves for the $Zn_{16}O_{15}N$ unit cell. Nitrogen levels are highlighted with larger circles. The Fermi level E_F is set at zero at the top of the valence band (TVB). Left – overall band structure showing the O2p valence band at 0.0 to -4.0 eV, the narrow Zn3d sub-valence band at -4.0 to -6.0 eV, direct energy bandgap of 2.8 eV at the Γ point, and the intra-band nitrogen acceptor levels at 1.0 – 2.0 eV with a minimum near the K-point of the Brillouin zone. Right – expanded view in energy range from -0.5 eV to 2.0 eV shows detail of the acceptor level and near-TVB dispersion.

To assess the degree of localization of the nitrogen acceptors, which is indicated by the narrow empty band within the bandgap, we have examined polarization near the N dopant center in terms of differences between spin-up and spin-down charges within the atomic spheres. Figure 8.8 shows that the spin polarization is indeed localized at the nitrogen atom, with rapidly decreasing spurious polarization at the Zn and O neighbors.

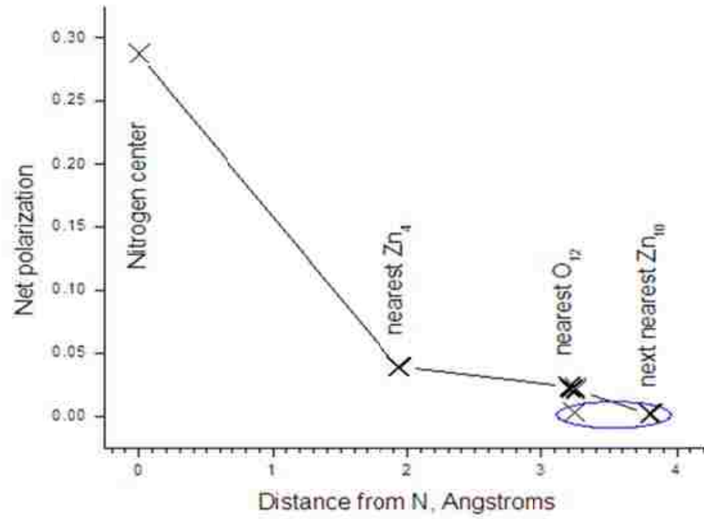


Figure 7.8 Difference of spin-up and spin-down charge densities at the nitrogen dopant center substituting for lattice oxygen, the nearest coordinating zinc atoms, the oxygen atoms further out, and the next-nearest Zn shell. Model: optimized $Zn_{64}O_{63}N$.

7.3.3.3 Effective mass of holes near the top of the valence band

Mobility of current carriers is related to effective mass, assuming a rigid band model for the system with ionized acceptor centers and a parabolic shape of the $E_i(\mathbf{k})$ curve near band edges. Upon excitation of an electron from the valence band to the acceptor center, the effective mass of the hole is estimated from the curvature of energy bands in momentum space using the relationship $\mu_{eff,i} = \hbar^2 / (\partial^2 E_i / \partial k^2)_{TVB}$ for each particular band i near the top of the valence band (TVB). The values of $(\partial^2 E_i / \partial k^2)_{TVB}$ were obtained by fitting the $E_i(\mathbf{k})$ curves by a parabola at the Γ point where the TVB is found in all ZnO-based materials investigated. Table 7.2 summarizes the effective masses determined by this method.

Table 7.2 Effective mass of holes in the valence band of ZnO in units of mass of free electron μ_0

Model	Relative effective mass of hole at the Γ–point of the TVB [a] $m_h = \mu_{eff,i}/\mu_0$	Direction of E_i(**k**) [b]
ZnO - so spin-down or spin-up	1.75, 1.83, **0.31**	Γ —> Δ —> A or Γ —> Σ —> M
$Zn_{16}O_{15}N$ -so	0.41, **0.35**	Γ —> Δ —> A
$Zn_{16}O_{15}N$ -so	0.90, 0.76	Γ —> Σ —> M

[a] Hole masses in the top three bands of the valence band. "Light holes" are highlighted. Effective masses in the N-doped ZnO are slightly higher than those in pure ZnO, as expected from the disruption of the perfect crystal symmetry by the dopants. For the N-doped, the corresponding E_i(**k**) curves are shown in the expanded insets of Figures 8.7. Note the anisotropy of $\boldsymbol{E_i}$(**k**) curves in the Γ —> A and the Γ —> Λ —> K directions. For pure ZnO, the values based on the same level of calculation are given but the well-known band structure is not shown here. The effective mass μ_e of an electron at the bottom of the conduction band of pure ZnO was calculated at $\mu_e = 0.24\ \mu_0$, in excellent agreement with experimental $\mu_e = 0.24 – 0.29\ \mu_0$.[6.32]
[b] Direction indicated by the high symmetry critical points of the Brillouin zone pertinent to effective masses given in column 2.

7.3.3.4 Magnetic moments

The nitrogen dopant introduces an odd-electron configuration in the stoichiometric zinc oxide associated with compositions $Zn_xO_{x-1}N$. The ensuing magnetic moments are not necessarily integer multiples of the Bohr Magneton owing to the combined effects of

dispersion, spin polarization and spin-orbit coupling. The results based on the present level of theory are summarized in Table 7.3. The N-doped ZnO displays magnetic moment close to 1 Bohr Magneton.

Table 7.3 Magnetic moments in Li- and N-doped ZnO

Model	**Magnetic moment, Bohr Magnetons with magnetization in the <00.1> direction**
ZnO[a]	0
$Zn_{16}O_{15}N$	0.99970
$Zn_{64}O_{63}N$	0.99967

7.3.4 Implementations and Limitations

Every substitutional valence-induction doping for n- or p-conductivity requires that the stoichiometry of the matrix be preserved. In the case of nitrogen, substitution NO(g) + O(lattice) --> O_2(g) + N(lattice) would satisfy such a requirement – however, the nature of the deep acceptors generated in this way makes the nitrogen doping unsuitable for p-conductivity in ZnO.

7.4 Conclusions

The present investigation confirms the theoretical calculations of Van de Walle et al. which conclude that N-doping of ZnO generates deep acceptors and hence is not leading to p-conductivity. This is consistent with our experimental result that N-doping will decrease the native n-conductivity of ZnO but not yield a p-conducting ZnO. The valence-inducing dopant N gives rise to ZnO lattice distortions which amount to a contraction around the N site. The structural distortions do not depend on the dopant concentration, within the range at. 0.8 – 3.1% in total ZnO. N anion doping generates deep acceptor centers, which form a broader band at higher concentrations and a sharp non-dispersed level at lower concentrations, both located at the nitrogen center.

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Chapter 8

Conclusions and Future Work

8.1 Summary of Results

The crux of the research presented here has been to explore the novel metal oxide based TFTs on a flexible platform. Amorphous Indium Gallium Zinc Oxide (a-IGZO) was chosen since among the different flavors of metal oxide thin films actively pursued in recent years, a-IGZO has garnered considerable interest based on device performance and reproducibility using commercially feasible, large area processing techniques like RF sputtering. Thin metal foils was the substrate of choice since it offered dimensionally stable flexible platform for device fabrication and allowed greater freedom to design small features for demonstration of high performance circuitry and eventually an active matrix based display system.

By fine tuning process parameters, mostly RF power and relative oxygen partial pressure, optimum a-IGZO thin films are obtained from a ceramic IGZO target (In_2O_3:Ga_2O_3:ZnO 1:1:1) . The resulting films presented a very smooth surface and amorphous structure with moderate carrier concentration in the $10^{17}cm^{-3}$ range deemed quite suitable for use as active layers in TFTs. A comprehensive electrical analysis was performed for the inverted staggered a-IGZO TFTs. Compared to a-Si:H TFTs, a-IGZO TFTs have a much higher field-effect mobility (μ_{FE}=7~15 cm^2/Vs), excellent switching properties (subthreshold swing ~370mV/dec), and a low off-current level (around 10 pA). The fact that tail state density is much lower than in a-IGZO than that of a-Si:H, an order of magnitude higher mobility is quite expected.

Mo and Al form good ohmic contact to a-IGZO with no evidence of current crowding around V_{DS}~0V. Through transmission line analysis (TLM), the source/drain (S/D) series resistance in a-IGZO TFT is found to be much smaller than values typical of a-Si:H TFTs. Nonlinearity of the TFT transfer characteristics (I_{DS}-V_{GS}) in a-IGZO TFTs manifests in a gate bias (V_{GS}) dependent field-effect mobility due to the finite conduction band-tail slope in a-IGZO. The field-effect mobility is weakly thermally activated with an activation energy around 15 meV, while the threshold voltage linearly decreases with temperature with a coefficient of -17.5 mV/°C. The current On-Off ratio and subthreshold slope almost remained the same within the investigated temperature range. The Meyer-Neldel (MN) parameter was observed to be constant (14.3 meV) over a broad range of activation energies.

From dual-gate analysis, where a top gate at the back of the a-IGZO channel is used to examine charge coupling between the front and back interface, we showed that minimal hole accumulation occurs in these oxide TFTs which is in contrast with n-channel SOI devices. Having control over the threshold voltage has implications when designing circuits with NMOS only devices. The origin of the low frequency noise of a-IGZO TFTs with SiO_2 gate dielectric is investigated in the low drain current range. Two different sources of noise were identified: a generation-recombination (g-r) noise component at drain currents below 5 nA and a pure 1/f noise at higher drain currents. The g-r parameters indicate that the g-r noise originates from bulk traps located in a thin layer of the depletion region. The drain current dependence of the normalized power spectral density S_I / I_d^2 shows that the 1/f noise is due to the carrier number fluctuations mechanism. As a result of the pure 1/f noise, the gate oxide traps have a uniform spatial distribution.

To address the reliability issues in a-IGZO TFTs, Electrical instability due to negative-bias-temperature stress (NBTI) in bottom gate staggered amorphous Indium Gallium Zinc Oxide (a-IGZO) thin film transistors (TFTs) on flexible steel foil was investigated. An N_2O plasma treatment is shown to have remarkable effects in suppressing rigid negative threshold voltage shift (ΔV_{th}) in transfer (I_D-V_{GS}) characteristics of a-IGZO TFTs due to prolonged negative bias stressing. The time evolutions of bulk, interface and conduction band tail states reveal that N_2O treatment efficiently reduces them for grater bias stress stability. The widely used stretched exponential model for a-Si:H TFTs has been applied to describe the bias stress instability

for plasma treated a-IGZO devices. It is suggested that post N_2O treatment passivates the interface states and homogenizes the poor quality a-IGZO film to a more high quality film with reduced sub-gap defect density.

Further evidence of the improved stability of a-IGZO TFTs was found from constant current temperature stress (CCTS) studies which are important if these devices are to be integrated in current driven pixel architecture applications. The stressing on N_2O treated a-IGZO TFTs was done both in linear mode where V_{GS} was held constant during the stress period and in saturation mode where the TFT was diode-connected to maintain a constant I_{DS}. In both modes of stressing, ΔV_T-t_{STRESS} shift with temperature and stress current was observed. In general, maintaining a lower temperature and smaller V_{GS} is beneficial to a-IGZO TFTs electrical stability. For the same level of I_{DS}, the TFTs are more stable when operating in the saturation regime than in the linear regime. From the observed behavior of ΔV_T- t_{STRESS}, we can conclude that there is only weak evidence of defect state creation in a-IGZO TFTs under constant current stress; the TFTs exhibit a ΔV_T of around 1 V under 2000 s stress with I_{STRESS}=100 μA at T_{STRESS}=60C. The substhreshold slope, off-current and field effect mobility remain unaffected in this stressing mode. The kinetics of ΔV_T- t_{STRESS} follow the stretched-exponential dependence predicted for charge trapping in the interface/dielectric. In contrast to a-Si:H TFTs where ΔV_T does not saturate over time, that of a-IGZO TFTs saturates under constant current stress.

To address electromechanical stability, we have applied uniaxial tensile and compressive strain ranging from 0.1% - 1% to amorphous IGZO TFTs and circuits

fabricated on stainless steel foils by outwardly bending them to cylindrical surfaces with different bending radii. Tensile strain increases field effect mobility and reduces threshold voltage of standalone devices. IGZO TFTs remained functional up to an applied strain level of 0.8% with critical strain (failure mode) level at 0.9%. a-IGZO TFT showed greater immunity against compressive mechanical bending; the important TFT parameters did not change much up to 0.5% of applied strain. IGZO TFT based ring oscillator had lower propagation delay per stage and speed enhancement with applied tensile strain. This systematic study can provide us with better understanding of IGZO TFTs under mechanical strain and allows for predicting IGZO TFT based circuit performance when flexed.

A whole range of circuits and systems based on a-IGZO TFT were demonstrated on thin flexible metal foils using a-IGZO TFTs. This validates the technological importance of this material system and can provide important guideline for more involved circuit designs. The circuits can be used as building blocks for integrated electronics that employ a-IGZO TFT technology. The relative high performance of the discussed circuits bodes well for on-panel monolithic integration of more involved circuits to drive active matrix displays or other large area electronic systems. We do note however, the limitation of NMOS only circuit configurations possible with current a-IGZO TFT technology. A complementary technology analogous to CMOS is highly desirable for low power conversion, low heat dissipation, high packing density, large output swing and better noise margin. The development of p-type AOS (amorphous oxide semiconductor) have proven elusive so far, but we believe that ongoing research and

development efforts devoted to realization for a p-type oxide TFTs are not only timely but quite justified since the payoff is so much larger.

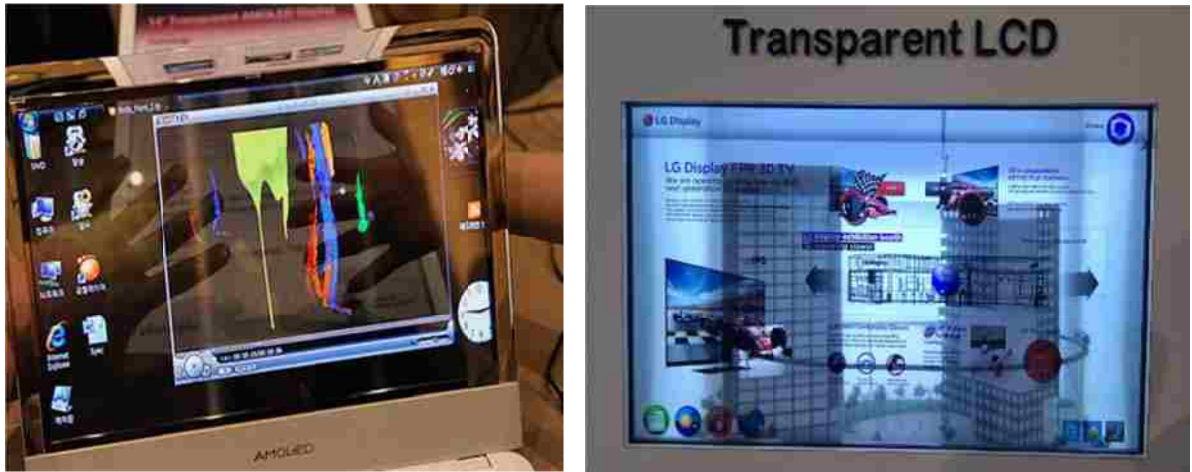
The present investigation also confirms persistent N-type behavior in nitrogen doped ZnO system. N-doping of ZnO generates deep acceptors and hence is not leading to p-conductivity. This is consistent with our experimental result that N-doping will decrease the native n-conductivity of ZnO but not yield a p-conducting ZnO. The valence-inducing dopant N gives rise to ZnO lattice distortions which amount to a contraction around the N site. The structural distortions do not depend on the dopant concentration, within the range at. 0.8 – 3.1% in total ZnO. N anion doping generates deep acceptor centers, which form a broader band at higher concentrations and a sharp non-dispersed level at lower concentrations, both located at the nitrogen center.

8.2 Looking Forward

As with any kind of research work, a large number of issues still remain unexplored and need future work. Metal oxide based thin films are a new class of materials with unique properties but the extensive research thrust in this area has already borne fruit. Due to their superior device properties and low fabrication cost comparable to those of their a-Si counterpart, metal oxide TFTs have the potential to be incorporated into commercial flat panel displays, such as AMLCD and AMOLED displays. In flexible AM displays, metal oxide TFTs will still be a strong competitor, due to their large-area scalability and low temperature capability. However, the following technical challenge

should be overcome in order to exploit the advantage of oxide TFTs. The low-temperature process compatible with plastic substrates essentially involves the creation of a large defect density in the gate insulator, semiconductor and passivation layer. The large trap density resulting from the low-temperature process would negatively impact the stability of the devices, including their temperature, bias and light stability, as well as their device performance, such as their mobility and contact resistance. Therefore, besides searching for a killer application for flexible displays and improving the manufacturing techniques, a significant amount of fundamental research still remains to be done, which includes the exploration of novel materials with high mobility and stability and understanding the deterioration mechanism of oxide TFTs against electrical and light stress. There are currently prototype devices and active matrix displays that have used amorphous metal oxide as the channel layer in the TFT backplane electronics; transparent displays from leading companies shown below are exemplary applications.

Transparent Displays: This is probably the most fascinating and immediate demonstration of the concept of transparent electronics. Although it sounds quite futuristic, there have already been demonstrations of fully transparent prototype displays by giants in the display industry, Samsung and LG display (Fig 8.1).



Transparent Oxide TFT based Prototype AMOLED displays unveiled at CES 2011 (a) Samsung; (b) LG Display

Figure 8.1 Transparent Display prototypes incorporating a-IGZO oxide as TFTs

Ultra low cost substrates for flexible and disposable electronics:

IGZO TFTs on Paper: The low process temperature of oxide TFT is readily amenable for use with low cost substrates like plastic and paper. There are some reports of using oxide based TFTs on plastic substrates already. The use of oxide TFTs can even enable stable device performance on paper substrates to usher in the ear of ubiquitous computing. There are efforts underway in our lab to integrate a-IGZO TFTs with printable paper substrates. Initial results are promising. For a maximum process temperature of around 100ºC and use of polymeric dielectrics, we were able to realize fine feature length (1–2µm) TFT with low leakage and decent TFT characteristics. Fig 8.2 shows fabricated array of a-IGZO TFTs on paper substrate and a cross sectional schematic of the devices.

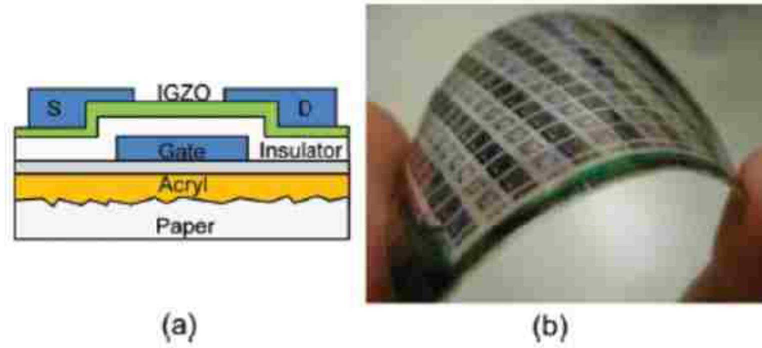


Figure 8.2. (a) Schematic cross section of fabricated a-IGZO TFT and (b) photograph of a-IGZO TFT array with methyl siloxane based gate dielectric on planarized paper.

IGZO TFTs on Low Cost Al Foils: We have also efforts underway to demonstrate AMOLED type of displays on very low cost Al metal foils. Aluminum is a suitable alternate choice as a substrate for flexible electronics over both plastics and other metals because of its low density, high strength, low cost, ease of recycling and high corrosion resistance. The robust process developed on steel can be adopted for Al foils as long as good dielectric can be deposited at low enough temperatures since Al foils need substrate stabilization. Heat treatment along with a pre-anneal process before device fabrication was crucial for thermal stabilization of Al alloy substrates as determined from thermal run-out experiments and detailed macrostructure analysis. IGZO TFTs with maximum process temperature of 300°C with threshold voltage of 3-5V, field effect mobility of around 10 $cm^2/V.s$ and subthreshold swing of 1.0 V/decade were obtained. The results suggest that low-temperature IGZO TFTs with uniform characteristics on large-area, very low-cost Al substrates is possible and opens up new route to high throughput roll-to-roll manufacturing of flexible electronics. Fig 8.3 and 8.4 show results of substrate

stabilization and first demonstration of high performance logic circuits on Al foils.

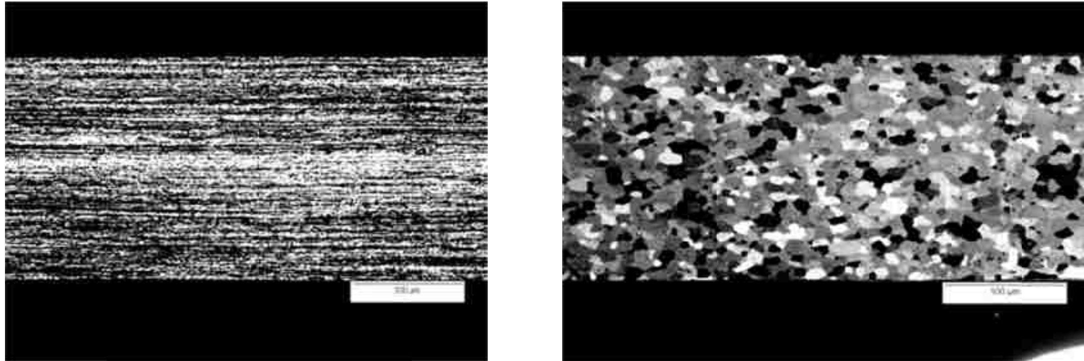


Fig.8.3 (a) Elongated grains of 50XX Al alloy after cold working with high dislocation density; (b) Equi-axed grains after pre-annealing

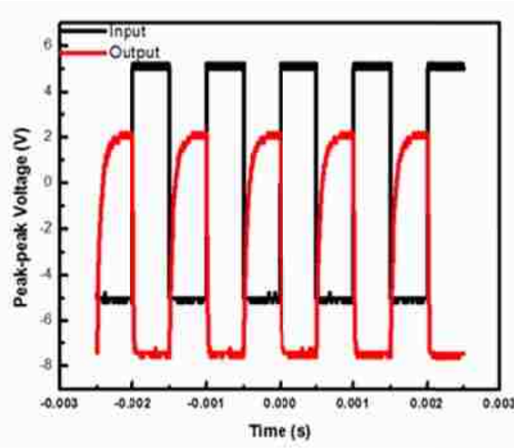


Fig. 8.4 Fabricated n-type IGZO inverter ($(W/L)_{Drive}$ = 384μm/16μm and $(W/L)_{Load}$ = 64μm/32μm) and corresponding logic-circuit operation at 1 KHz.

Sub-micron Scaling of IGZO TFTs:

Recently our collaboration with Dr. C.A. Dimitriadis's, group at Aristotle University of Thessaloniki has resulted in showing evidence that layout and device architecture can have implications when theses TFTs are eventually scaled down. With different width of the region between gate and *a*-IGZO active layer (W_{IGZO}), the length of

the region between S/D and *a*-IGZO active layer (L_{IGZO}), and the length of overlap region between gate and S/D (L_{OV}), it was shown from low frequency noise measurements that in devices with certain layout N_{st} decreases with decreasing channel length and increases with increased length. This discovery bodes well for devices with a specific architecture to be better candidates for sub-1 μm scaling of TFTs.

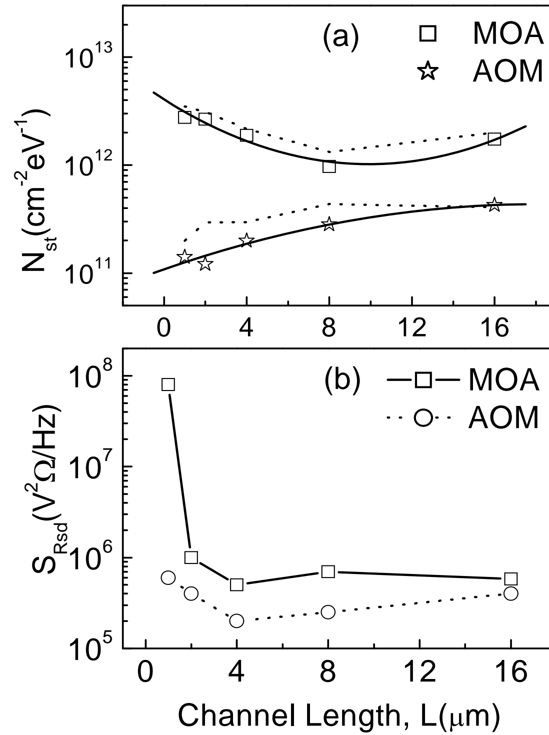


Figure 8.5. (a) Density of gate insulator traps N_{st} and (b) spectral density of source-drain series resistance S_{Rsd} versus channel length, L of 2 different architecture (MOA and AOM) a-IGZO TFTs.

Exploration of p-channel TFTs:

Exploration of p-channel TFTs is highly desirable as a means of realizing a complementary circuit technology with oxide-based TFTs. As we noted before, having good p-type oxide material has so far been elusive. Potential channel materials include

NiO and Cu_2O. Hole injection will likely pose a difficult challenge in forming these TFTs. One drawback is that most p-type oxides either have poor mobility or require a high temperature annealing treatment to achieve reasonable performance. It is expected that developmental efforts devoted to the realization of a p-type oxide TFT will continue since the implications for fully CMOS oxide electronics will be huge.

Overall, there are a variety of directions this work could continue towards, including both fundamental and applied research. Although a-IGZO TFTs is a relatively new and unexplored category of thin-film devices, the potential lies in their transparency, uniformity, low processing temperature, and good electrical performance. As this work continues to grow, integration of these oxide films into different types of applications will be essential. For now it is reasonable to suggest that these novel metal oxide TFT based applications will be available in the very near future.

Appendices

Appendix A:

a-IGZO TFT Fabrication

The flexible metal foil substrates used in this research were stainless steel type 304 having a diameter of 150 mm and were 100-um thick. The back channel passivated structure is a 5-mask process quite typical of TFT fabrication employed in active matrix backplane fabrication. The step by step process is detailed in the following fabrication sequence:

- **Mask 1:** Gate Deposition: Gate Mo (150nm) deposited and patterned. Mo is deposited by DC sputtering in a Kurt J. Lesker system. Patterning is by standard lithography using positive resist AZ703 and lift-off resist, LOR10B. Patterned steel wafers are rinsed with DI water and dried before dielectric deposition.
- Gate Dielectric (SiO_2) deposition by PECVD @ 300ºC (100nm). The process details (Diluted SiH_4 in He/N_20/ chemistry; Breakdown field~8MV/cm^2) are elaborated in tabular format later.
- Blanket IGZO (50-70nm) deposition with RF sputtering from a ceramic IGZO target (1:1:1 molar ratio of In_2O_3:Ga_2O_3:ZnO) was carried out (5-10% volume O_2 in Ar) at a RF power of 100 Watts. The ceramic target was purchased from SCM Inc, NY. Some IGZO thin films underwent an N_2O treatment in PECVD after this.
- Blanket Oxide (50nm) deposition with RF sputter to cover IGZO. Sputtering of the SiO_2 was done in ambient chamber temperature at 200 W (10% O_2 in Ar).

- **Mask 2:** Patterning of the IGZO/Oxide stack with dry/wet etch (AZ 2020 Negative patterning) (dry etch of sputter oxide in CF_4 plasma in RIE (300W, Etch rate- 25nm/min) followed by dilute HCL (CMOS grade HCL with 40/1 dilution in DI Water) etch of IGZO; PR stripped in AZ400T Stripper)
- Deposit thicker (100nm) passivation oxide (Sputter oxide again).
- **Mask 3:** Open access to gate pads and contact holes for circuit integration. This is first of two contact pad openings. To have access to the gate pad, the PECVD oxide and the sputtered SiO_2 is etched by wet etch with commercially available SILOX etchant.
- **Mask 4:** Source and drain contact holes opening is done next. The Passivation , the mesa oxide are dry etched first (Dry etch in a RIE system with CF_4 gas at 300Watts on top of IGZO). For some devices, S/D area is Ar plasma treated in RIE (100 W, Ar 10 sccm, 1 min) to reduce contact resistance.
- **Mask 5:** S/D metallization (120 nm of Mo) is done in DC sputtering in pure Ar .
- Completed TFT anneal (300ºC, N_2 Ambient, in tubular furnace for 1hr).

1. PECVD system

Process	Gas (sccm)	Power (W)	Temp (ºC)	Pressure (Torr)	Dep rate (Å/Min)
Isolation SiO_2 Passivation SiO_2	SiH_4 (480), N_2O (720), HE (2000)	400	300	1	190
Gate SiO_2	SiH_4 (120), N_2O (720), HE (2000)	400	300	1	50
N_2O Treatment	N_2O(720)	100	RT	0.5	N/A

2. PVD system

Process	Gas (sccm)	Power (W)	Temp (ºC)	Pressure (mTorr)	Dep rate (Å/Min)	Time (min)
IGZO	Ar/O_2(8/0.8)	100 RF	RT	5	50	N/A
Mo S/D/G	Ar(15)	250 DC	RT	8~9	140	N/A

3. Dry etching system - TECHNICS PEII-A plasma system

Process	Gas (sccm)	Power (W)	Pressure (Torr)	Etch rate (Å/Min)
Sputtered SiO_2 etching	CF_4 (15), O_2 (5)	300	0.2	80
O_2 plasma for surface treatment / descum	O_2 (20)	100	0.15	N/A

4. Wet chemical process

Process	Chemical	Remark
Piranha clean	H_2O_2:H_2SO4=3:1	
Oxide etch Buffer HF	NH_4F:HF=6:1	
Oxide etch SILOX	Silox 100%	E/R=10Å/sec
RCA clean (acid)	H20:H2O2:HCl=5:1:1	@70 C
RCA clean (base)	H20:H2O2:NH4OH=5:1:1	@70 C
Mo lift off	MICROCHEM EBR	
IGZO etch	DI:HCl (40:1)	RT

5. Furnace process

Process	Ambient gas	Temp (ºC)	Time (hr)
Post metallization anneal	N_2	300	0.5~1

Chip Layout and Device Photo Gallery:

There were 47 dies that were laid out across the 6 inch wafer. The Fig A.1 shows the location of the dies on the wafer and the family of test structures, stand alone TFTs and circuits within each die.

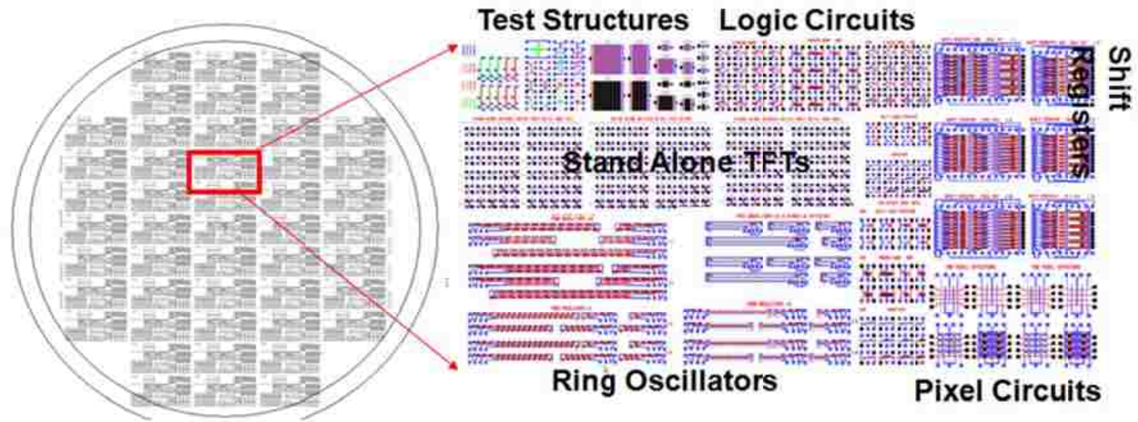
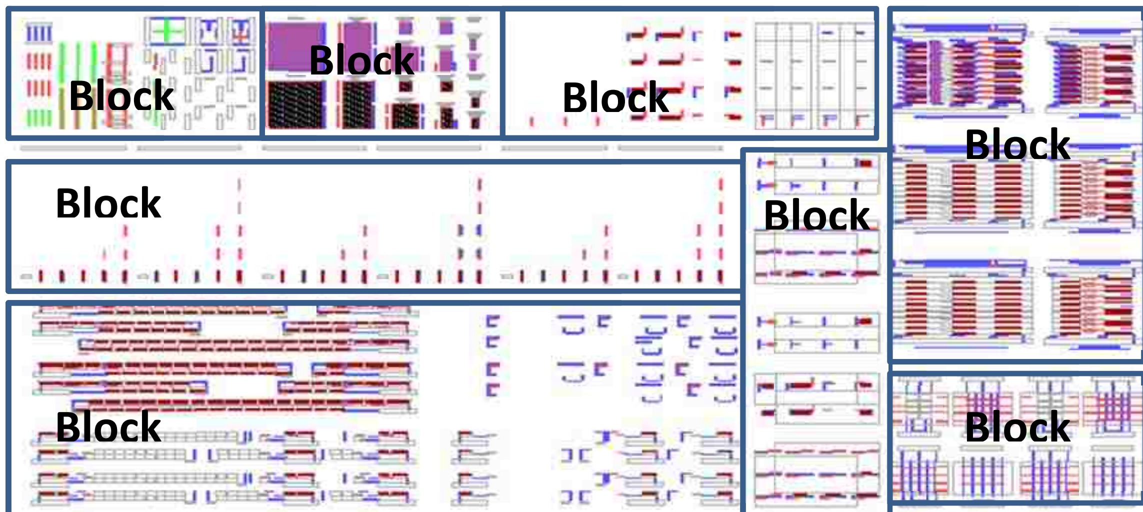
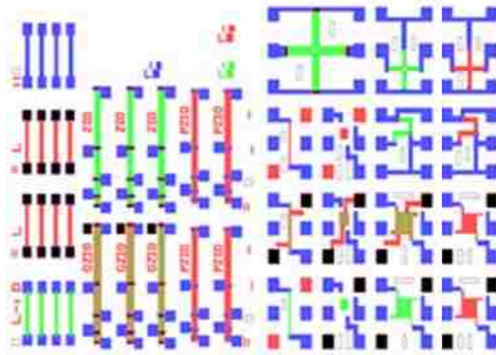


Figure A.1: 6 inch wafer with the individual dies laid out all-across. The family of test structures , stand alone TFTs and circuits within each die.

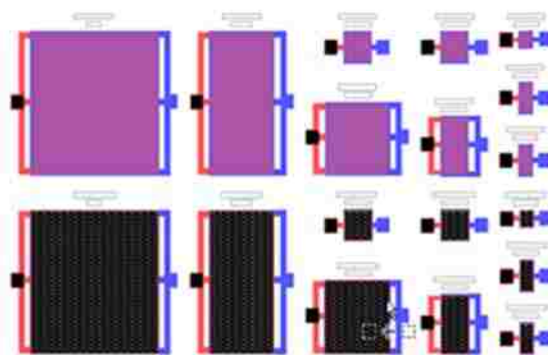
Layout of One Die on the Mask



Block1



Block2

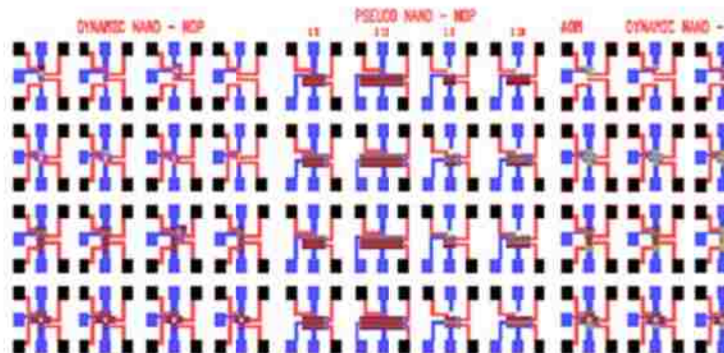


Sheet resistance measurements geometries
Contact resistance measurement geometries
Kelvin bridge structures
Van der Pauw Structures
Gated van der Pauw structures

Capacitor measurements geometries
Active-metal overlap
Metal-Poly overlap
Active-Poly overlap

Block3

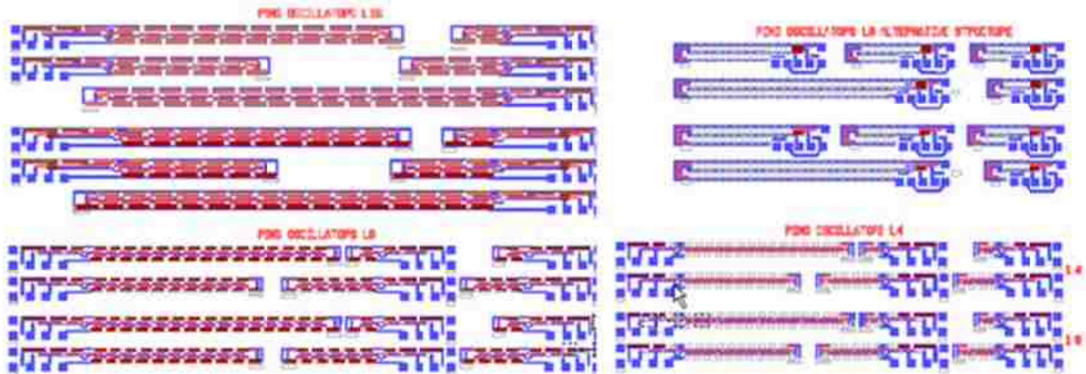
Pseudo logic circuits
Dynamic NAND
Dynamic NOR



Stand alone TFT geometries
With different active-S/D overlaps
Different width geometries
Different length geometries

Block4

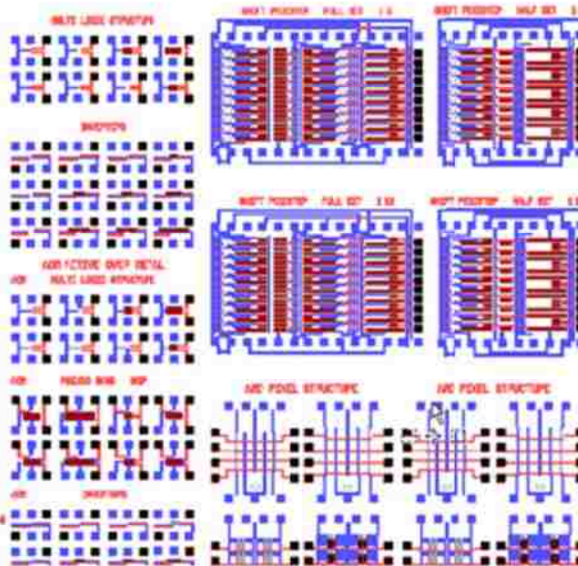
Block5



Different Ring Oscillator Circuit geometries
With different drive-Load ratios
Different width geometries
Different length geometries

Block6 **Block7**

Multi Logic circuits
NOR
NAND
Inverters
With different load-drive TFT ratios



Memory Circuits
Shift register
Full bit and
Half bit designs

Block8

Pixel Circuits

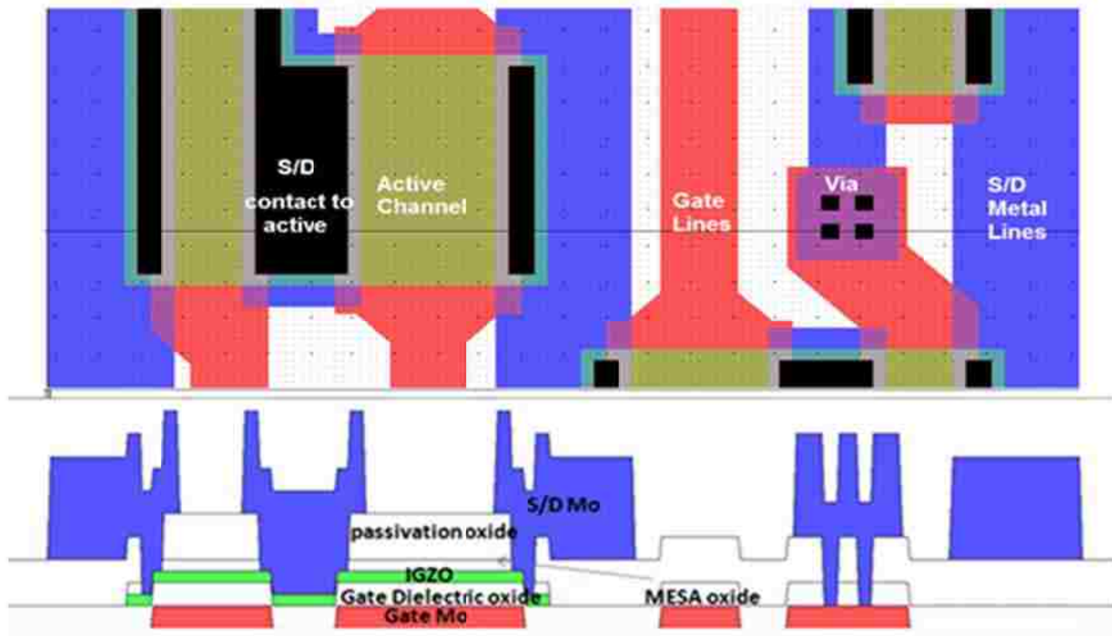


Figure A.2: Typical Circuit Integration Scheme of a-IGZO TFTs Fabricated at Lehigh

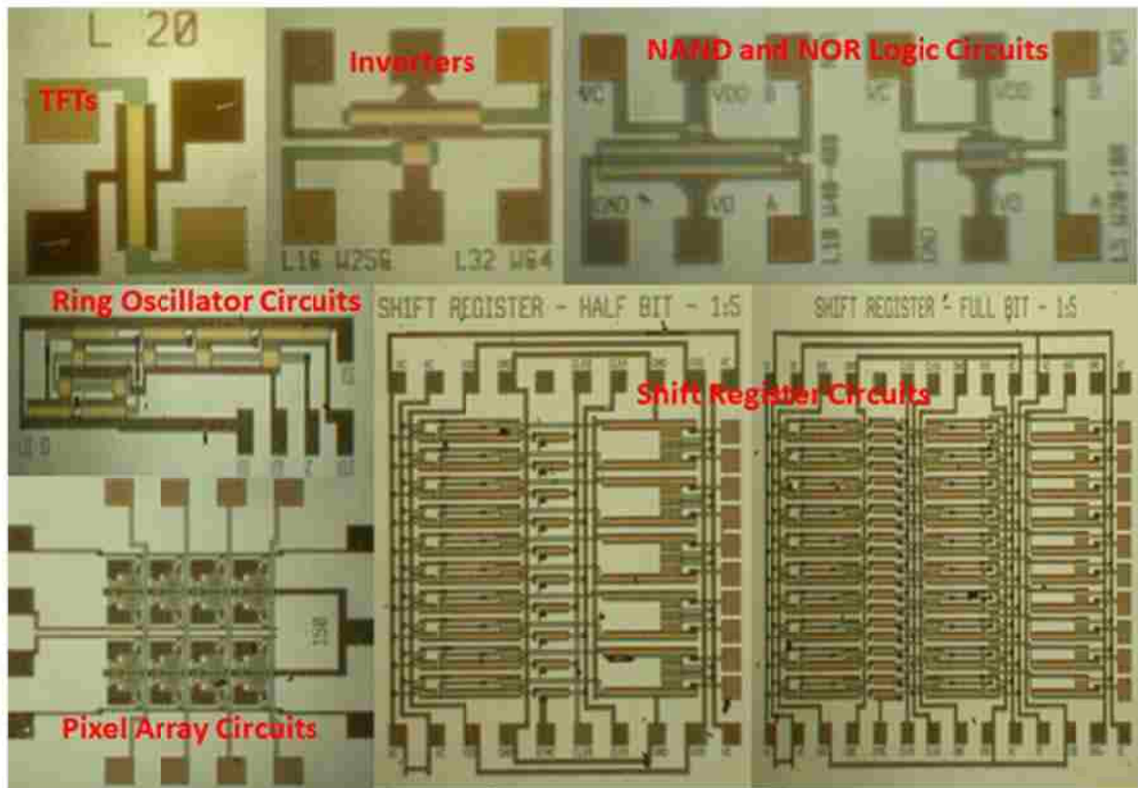


Figure A.3: Images of a-IGZO TFT based Devices and Circuits

Appendix B:

Demonstration of an EPD Display with a-IGZO Backplane (Lehigh, Versatilis and FDC Collaboration):

We partnered with Versatilis, a Vermont based Start-up Company and the Flexible Display Center at Arizona State University (FDC) to demonstrate an electrophoretic display (EPD-Display) typically found in e-paper type applications. The scope of the collaboration was to help evaluate our IGZO process as well as to give a guideline to FDC in developing their own metal oxide based backplane technology. A mask-layout view and actual image of an individual pixel is shown in Fig B.1. The individual array maps for Lot E1009-001 is shown next. The EPD display consisted of an array of 240x320 pixels.

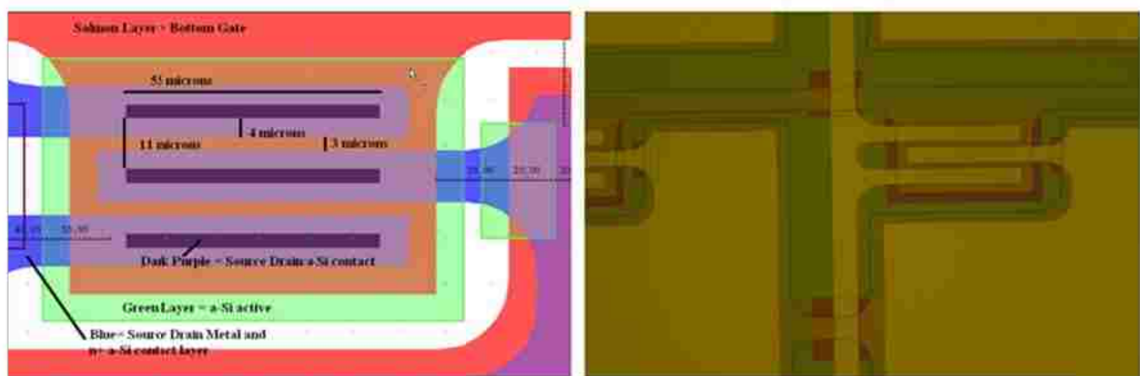


Figure B.1: FDC Mask layout an individual pixel and the corresponding fabricated image. The EPD-display consisted of 240x320 such pixel to form the backplane.

The back channel passivation mesa oxide and the passivation oxide by the low temperature process were also evaluated. The FTIR spectra for the PECVD deposited SiO indicates good dielectric quality is akin to thermal oxide. The low temperature sputter deposited SiO has a pronounced bump between 3400 and 3600 wavenumbers.

This bump is usually attributed to Si-OH. In addition, there is a large shoulder on the main peak near 1250 wavenumbers. This shoulder is attributed to the “caged” structure of SiO and is associated with asymmetric stretching of the Si-O caused by the disorder of the “caged” structure. The large peak at 1040 wavenumbers is associated with symmetric stretching of the Si-O bond due to the more orderly “ladder” structure.

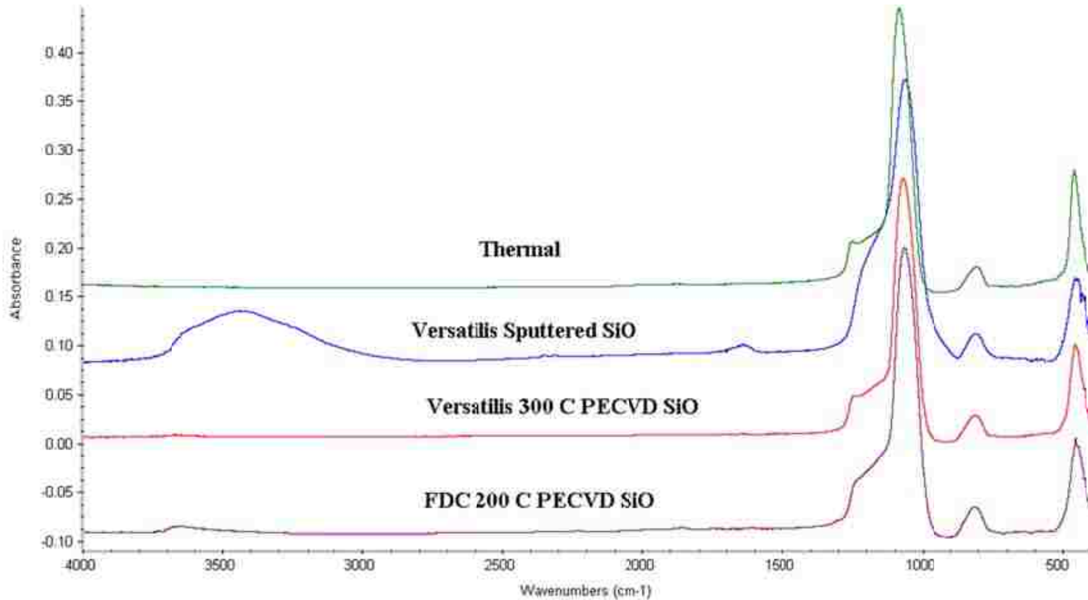


Figure B.2: FTIR spectra of SiO deposited at Lehigh University for Versatilis. The FDC PECVD SiO and thermal SiO are shown as a comparison.

The individual array maps for Lot E1009-001 can be found below. Recall that the fabricated FDC EPD displays consist of an array of 240x320 pixels. It should be noted that there is a center-to-edge variation in the drive current. The results seem to correlate with the center-to-edge variation in the IGZO thickness. It was deemed that more control over IGZO thickness in our sputtering process is needed. A present system that can accommodate 8" type targets is presently under investigation in our lab. After an array

repair process which checks row-to-ground, column-to-ground, and row-to-column leakage (Rows or columns with a total leakage above 100 microamps were singulated by

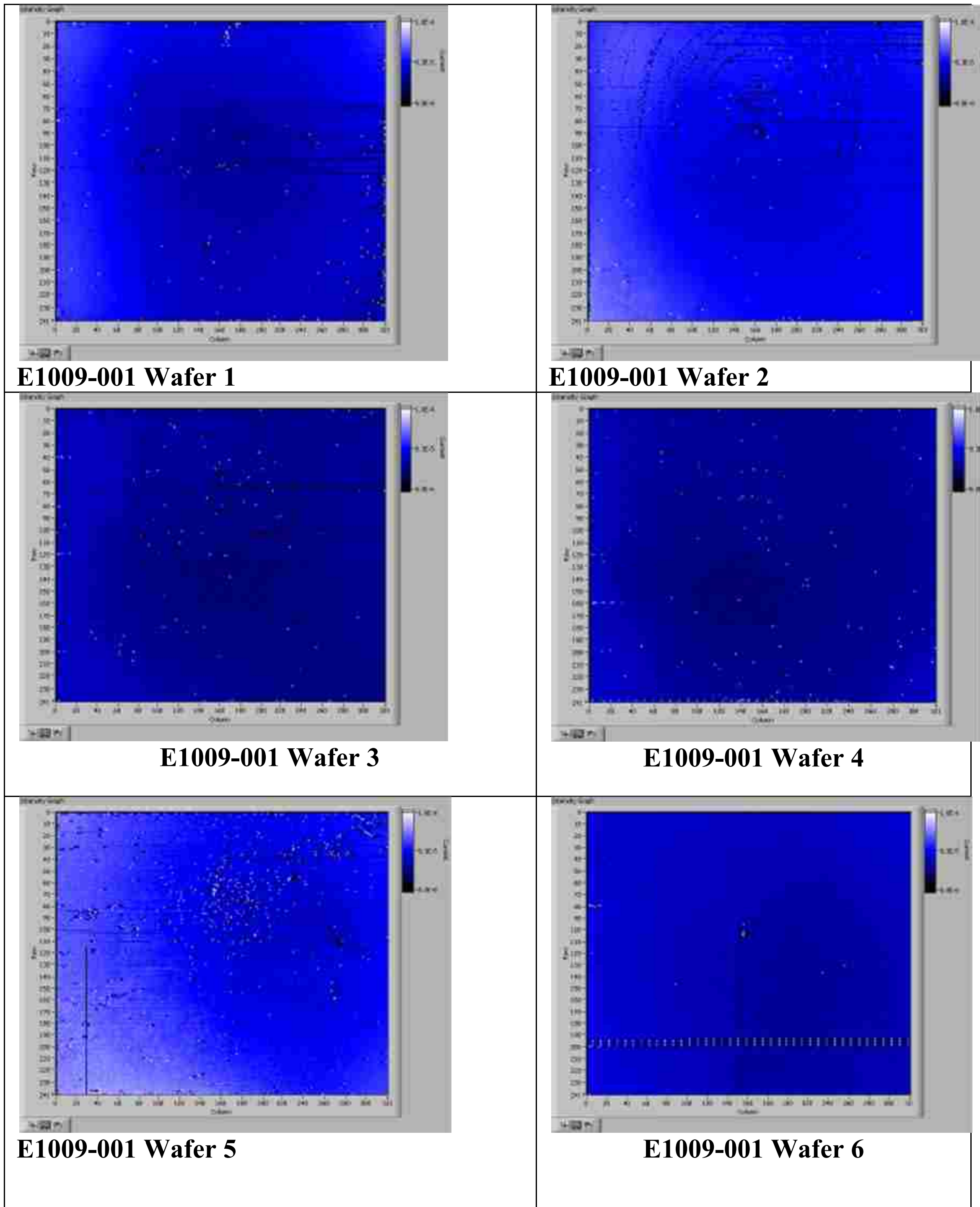


Figure B.3: Array Current Map for Lot E1009-001.

blowing the individual row or column fuse) wafer 6 was selected to be fabricated for a complete EPD-display (Wafer 6 required 9 lines to be cut). The driven image by the a-IGZO based backplane is shown below:

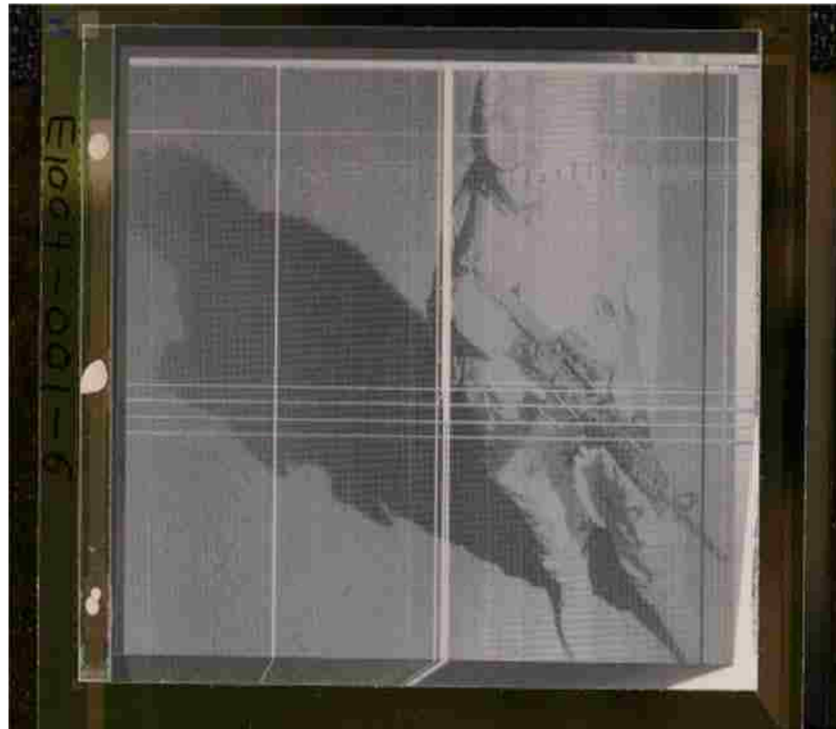


Figure B.4: Lot E1009-001 Build Photo

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Andreas Tsormpatzoglou, Nikolaos A. Hastas, Charalabos A. Dimitriadis, **Shahrukh A. Khan** and Miltiadis K. Hatalis , "Layout Dependent Low Frequency Noise Measurements of Amorphous IGZO Thin-Film Transistors for Sub-µm Scaling", Accepted for publication in *IEEE Electron Device Letters, 2011.*

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Nackbong Choi, **Sharhukh A. Khan**, Xiaoxiao Ma, and Miltiadis Hatalis, "Amorphous Oxide Thin Film Transistors with Methyl Siloxane Based Gate Dielectric on Paper Substrate", *Electrochem. Solid-State Lett.,* Volume.14, Issue 6, pp. H247-H249, 2011.

Abbas Jamshidi−Roudbari, **Shahrukh A. Khan**, and Miltiadis K. Hatalis, "Integrated Full−Bit Shift Register by Low−Temperature Amorphous Indium Gallium Zinc Oxide Thin−Film Transistors", *Electrochem. Solid-State Lett.,* Volume. 14, Issue 5, pp. J19-J21, 2011.

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Shahrukh A. Khan, Xiaoxiao Ma, Nackbong Choi and Miltiadis Hatalis , "Absence of Defect State Creation and Threshold Voltage Stability of N_2O Treated Amorphous IGZO Thin Film Transistors on Flexible Metal Substrates Under Constant Current Temperature Stress", manuscript under preparation, to be submitted to *IEEE Transactions on Materials and Device Reliability, 2011.*

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Shahrukh A. Khan, Xiaoxiao Ma, Nack-Bong Choi and Miltiadis Hatalis , "Electromechanical Stability of Amorphous IGZO (a-IGZO) TFTs on Metal Foils", manuscript under preparation to be submitted to *Journal of Vacuum Science and Technology B, 2011.*

Vita

Mr. Shahrukh Akbar Khan was born on November 4th, 1977 in Dhaka, Bangladesh to Mr. Akbar Hussain Khan and Mrs. Sayeeda Bilquis Jahan. He attended Mirzapur Cadet College, one of the most prestigious boarding schools in Bangladesh for his high school studies and graduated in 1995 with top honors. He was ranked 15th in the nationwide standardized exams held in 1993 and was recognized by the honorable Prime Minister of Bangladesh for academic excellence. He then headed to upstate New York, USA to attend University of Buffalo, NY and graduated with a Bachelor's degree in Electrical Engineering in February, 2002 with high honors. He was awarded a graduate fellowship and subsequently obtained a Master's degree in Electrical Engineering in June, 2004. His Master's thesis was on transport limiting behavior of a-Si:H/crystalline-Si heterojunction devices for photovoltaic applications under the supervision of Dr. Wayne Anderson.

Mr. Khan transferred to Lehigh as a doctoral student with a Doctoral Fellowship from the department of Electrical Engineering in September of 2006. He has received the Sherman Fairchild Fellowship during 2007-2009 periods to continue his work on low temperature amorphous oxide based thin film transistors for future display applications. His academic and research interests are in physics of semiconductor devices, fabrication and characterization TFTs, TFT based circuit design, thin film and organic photovoltaic devices. He is a student member of IEEE, a member of MRS, an associate member of the Scientific Research Society of Sigma Xi, an inducted member of Engineering Honor Societies of Tau Beta Pi and Etta Kappa Nu.