2014

Wide Bandwidth - High Accuracy Control Loops in the presence of Slow Varying Signals and Applications in Active Matrix Organic Light Emitting Displays and Sensor Arrays

Thomas Charisoulis
Lehigh University

Wide Bandwidth - High Accuracy Control Loops in the presence of Slow Varying Signals and Applications in Active Matrix Organic Light Emitting Displays and Sensor Arrays

by

Thomas Charisoulis

Presented to the Graduate and Research Committee

of Lehigh University

in Candidacy for the Degree of

Doctor of Philosophy

in

Electrical Engineering

Lehigh University

January, 2015

Approval of the Doctoral Committee

" Wide Bandwidth - High Accuracy Control Loops in the presence of Slow Varying Signals and Applications in Active Matrix Organic Light Emitting Displays and Sensor Arrays"

Received and approved by the Doctoral Committee Directing the proposed program of study for Thomas Charisoulis, a Ph.D. Canditate in the Department of Electrical and Computer Engineering, on this date of _____.

_____
Dissertation Advisor

Committee Members:

_____
Dr. Miltiadis Hatalis, Committee Chair

_____
Dr. Douglas Frey, Dissertation Advisor

_____
Dr. James Hwang, Dissertation Advisor

_____
Dr. Kapil Sakariya, External Member

τόδε ἔργον ἀέξεται, ᾧ ἐπιμίμνω.
Rendition: Your work will be completed, only if you take it seriously.
Homer, Odyssey
Book 14, lines 66-67

Acknowledgements

FIRST and foremost, I would like to thank Ruobing Chen for being next to me through the most exciting years of my life, holding me true to my goal and enabling me to question some of my deepest scientific thoughts. This work would have not be a part of this world if she was not there to provide her love and understanding, guiding me through the dark times of our life. My dear Moumi, for that you have my deepest gratitude!

My mother, Maria Tsiruki, is also one of the few people sacrificing their life so that I can go to school and get a good education gaining a fighting chance in this world. Was it not for her and her efforts to provide for me during the early years of my life this dissertation would have never taken place. Dear mother, Thank you!

My father, even though he is not an academic, he strongly supported academic thought teaching me in my early years to be inquisitive and never take anything for granted. He supported all my decisions when I chose the Doctorate path and he is also the reason for Homer's quote. Dear father, thank you!

Of course, I would be remiss if I did not mention my uncle Thanos Tsirukis and my aunt Vicky Papageorgaki, for providing me with a roof over my head as well as a warm plate of food during the cold winters here in Bethlehem, PA. Thank you for your support.

I would also like to thank my brother George Charisoulis, for being there when I

needed him, providing me emotional support and often visiting me during my studies to reassure me and help me push forward to my graduation. I would also not be here if it was not for his huge emotional support and the endless hours we spent on the phone talking to each other. Thank you little borther! (Also Pileas and Laertis should be added here - my youngest brothers. Although they are too young to know, receiving daily updates with their pictures always helped me, enlightening my mood!)

I would also like to thank Prof. Hatalis and Prof. Frey, my advisors, for believing in me and recognizing my talent. They gave me the motive to continue to perform admirably and provided me with precious guidance when I needed it the most. They have made me question the trust in myself multiple times during my academic career, making me a better student and a better engineer. Dear professors, from the bottom of my heart, Thank you!

My gratitude also goes to the other two members of my committee, Prof. James Hwang who has been one of my trusted committee members since the very beginning and Dr. Kapil Sakariya, who saw my potential and decided that I was worth the time he put traveling from California to attend my dissertation's defense. Thank you!

My work in the lab would have been extremely monotonous if it wasn't for Mr. Grant Reed to lighten up my mood on a day to day basis, thank you Grant for making me smile even during the toughest days of my Ph.D.. I would also like to extend my gratitude to Dr. Andreas Tsormpatzoglou for guiding me through my first paper submission process and teaching me how a good researcher keeps his notes. My gratitude also goes to all of my undergraduate students that also participated in small parts of my research, namely Jordan Thimot, Collin Reiman, Charlie Bremer and Michael Wilson.

Finally I would like to thank Mr. David Morrisette and Mr. Ted Bowen, our

Engineering department's IT staff, for their support and patience. All the simulations and data gathering done for this dissertation is mainly due to their help! My thank you also goes out to The Technology Collaborative, Sherman Fairchild Center for Solid State Studies and the National Aeronautics and Space Administration who where the sponsoring organizations that made all this work possible through their financial support.

Contents

List of Tables

List of Figures

Abstract

THIS dissertation deals with the problems of modern active matrix organic light-emitting diode AMOLED display back-plane drivers and sensor arrays. The research described here, aims to classify recently utilized compensation techniques into distinct groups and further pinpoint their advantages and shortcomings. Additionally, a way of describing the loops as mathematical constructs is utilized to derive new circuits from the analog design perspective. A novel principle on display driving is derived by observing those mathematical control loop models and it is analyzed and evaluated as a novel way of pixel driving. Specifically, a new feedback current programming architecture and method is described and validated through experiments, which is compatible with AMOLED displays having the two transistor one capacitor (2T1C) pixel structure. The new pixel programming approach is compatible with all TFT technologies and can compensate for non-uniformities in both threshold voltage and carrier mobility of the pixel OLED drive TFT. Data gathered show that a pixel drive current of 20 nA can be programmed in less than 10μsec. This new approach can be implemented within an AMOLED external or integrated display data driver. The method to achieve robustness in the operation of the loop is also presented here, observed through a series of measurements. All the peripheral blocks implementing the design are presented and analyzed through simulations and verified experimentally. Sources of noise are identified and eliminated, while new

techniques for better isolation from digital noise are described and tested on a newly fabricated driver. Multiple versions of the new proposed circuit are outlined, simulated, fabricated and measured to evaluate their performance.

A novel active matrix array approach suitable for a compact multi-channel gas sensor platform is also described. The proposed active matrix sensor array utilizes an array of P-i-N diodes each connected in series with an Inter-Digitated Electrode (IDE). The functionality of 8x8 and 16x16 sensor arrays measured through external current feedback loops is also presented for the 8x8 arrays and the detection of ammonia (NH3) and chlorine (Cl2) vapor sources is demonstrated.

Chapter 1

Introduction

VISION; the most refined and detailed of the human senses; Humans have always relied on it for their survival as well as their entertainment. Furthermore it was the first sense ever used to interface humans with machines. To this day one rarely, if ever, finds a complex machine having an output human interface that does not require the user's vision as a means to relay information back to the user. Recognizing this basic human need, many endeavors in recent years have spawned a multi-billion dollar industry, the flat panel display industry.

Since the early years, computers have evolved a great deal, therefore, the growing necessity of relaying a plethora of information by the better machines, require faster, sharper and brighter displays to satisfy the user. This has been the driving force to producing cheaper higher definition displays in the past decade and it has recently received widespread attention from many vendors providing high resolution, low power and low cost monitors and displays in all of the portable devices in the market today.

As technology progresses, new techniques are invented for implementing sharper

High-Definition displays, such as more efficient Solid State Light Emitting Diodes (LEDs) and Organic Light Emitting Diodes (OLEDs), that require high speed, robust back-plane drivers to supply the required signals for operation to satisfy the users' ever growing demand in Higher Quality products. Specifically, the display quality is directly dependent on the materials responsible for illumination which relates to the brightness of the display; the density of the illuminating devices which is associated with the sharpness and the frequency of updating the displayed data which translates to the smoothness of the displayed image.

Most of all the materials and devices utilized today have physical limitations that affect their uniformity and their stability during their operational lifetime. In all the existing AMOLED backplanes there are means of correcting these limitation in order to improve the quality of the image. and respectively adjusts the driver to drive the illuminating elements harder or faster in order to produce the desired end product. Collectively these means are known as compensation circuits or methods. Different ways of implementing those compensation circuits aimed to fine-tune the quality of the projected image have been reported in recent years.

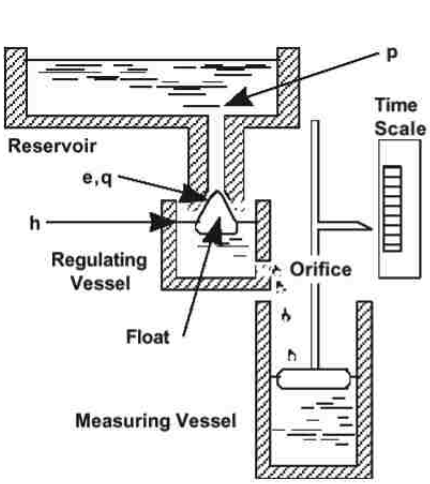
As it is explained in this dissertation, most of the compensation circuits employed nowadays are internal to the pixel circuit and very little work has been done to expand the knowledge on external compensation approaches due to their large overhead when deployed with digital circuitry. External compensation suffers from a common misconception of sluggish response times, which is wrongly associated with the large parasitics present in a modern back-plane. However, there are many simple abstract mathematical constructs that can be applied in circuit design, which can be beneficial in a multitude of ways, to the modern approaches in driving displays.

1.1 Control Loop history

Since ancient times, man has been trying to innovate to find ways to control the environment around him. Some examples of ancient craftsmanship and innovation can be found as early as ancient Greece, where a "mechanical engineer" of the era with the name of Ctesibius was the first to come up with a mechanical way of regulating the water in a tank that creates a constant water flow for taking accurate time measurements [2].

As seen in figure 1.1(a), his invention was based on a regulating vessel (h), holding the water dripping from a reservoir (p). The regulating vessel slowly drips water to a Measuring tank holding a float with an orifice that pointed to a time scale. Another float (e,q in figure 1.1(a)), plays the role of the mechanical feedback shutting the valve when the regulating vessel is full of water. This was history's first documented closed feedback loop that gave birth to the invention known as Alexandria's clock, which is shown in figure 1.1(b) and was inspired by the time measurement setup Ctesibius invented.

Almost two millenia later, Sir James Watt was the brilliant engineer that produced another closed feedback loop regulator, known as the governor, responsible for regulating the revolutions per minute of steam engines while idling. It was comprised of a central shaft, attached through a belt to the rotating parts of the engine, while two metal balls were mounted onto it on either side. Those balls were connected to a ring at the top of the shaft, which moved up and down along the axis of the shaft. This ring was, in turn, connected to the valve of the steam engine supplying steam to the engine's pistons, providing motion as shown in figure 1.2. Moreover, one could control actively the rotations per minute of the idling engine by actively moving the ring either direction along the shaft's axis.



(a) The water thief, an Invention to track time by Ctesibius.

(b) Clock of Alexandria.

Figure 1.1: Ancient Feedback systems

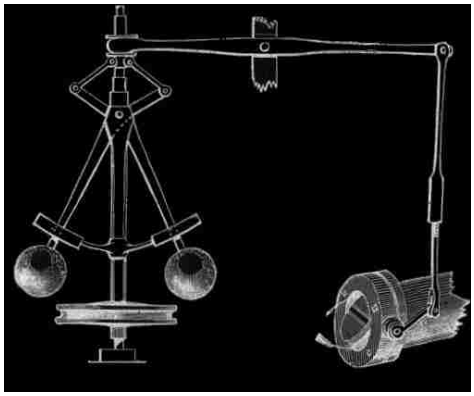


Figure 1.2: The steam engine rpm regulator known as the governor

In 1868, shortly after the discovery of linear algebra, while Sir J. C. Maxwell trying to explain the motion of a governor. In a paper he wrote to the royal society in London named "on governors" [3], he started formulating mathematics for producing analytical solutions to Ordinary Differential Equations describing the motion of the governors and how it can be controlled systematically. Today, these differential equations are known as the system's characteristic equations and they describe feedback loops analytically. About a hundred years later, in 1954, Kalman started writing his

thoughts on loops controlled electronically by a computer [4] and started formulating a general theory describing a mathematical space in which any type of control loops are easily described, something that later was described as the state space, a mathematical way of formulation allowing for easy implementation of complex loops and filters used to this day.

Control loops have been used throughout the millenia and have many immediate applications in the field of electrical engineering today, spanning from active filter implementations for signal processing, to controlling electric motors providing motion in many industrial and household applications. All those techniques for implementing the loops have been analyzed over the years and aspects, such as large dynamic range and wide bandwidth, have been extensively studied. In the ever-shifting display industry, as modern applications become increasingly complex while at the same time the demand for more high quality products increases, new techniques must be invented to keep up with the demand. Of particular interest to this dissertation os a technique combining wide bandwidth properties with large dynamic range properties of a single control loop trying to control one signal in the presence of larger, slower varying signals; Such a technique can find immediate applications in the field of AMOLED displays.

This dissertation focuses on expanding the existing control loop theory and define and advance techniques to successfully measure tiny quantities especially in the presence of large slow varying signals within very fast time slots. Specifically, in chapter 2 a general systematic approach is presented that helps the analysis of control loops that will be applicable for the aforementioned case. Chapter 3 outlines the practical applications of those loops and previously used techniques are discussed and analyzed. Part of the previous work is presented here as well. Chapter 4 presents my proposed solution to those applications along with some preliminary data. Chap-

ter 5 includes the measurement techniques utilized to extract the data and their significance towards evaluating the operation of the complex loops. Chapter 6 describes the peripheral devices utilized within the integrated chip (IC) to produce and measure fine currents. Chapter 7 outlines the application of control loops to sensor arrays and complex systems along with detailed information on modeling procedures utilized to simulating the complex systems presented in this thesis. Finally, Chapter 8 includes a summary of the work along with suggestions for future research on expanding the suggested switching control loop theory and thoughts on future practical applications.

Chapter 2

Time Varying control loop theory

2.0.1 Investigation of a single first order Loop

THE transfer function for a simple Linear Time Invariant (LTI) feedback loop shown in figure 2.1, is well defined and can be represented in state space by equations 2.1.

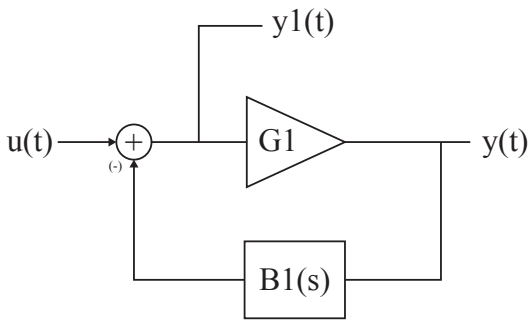


Figure 2.1: A simple loop

$$H(s) = \frac{G_1}{1 + G_1 B_1(s)} = \frac{Y(s)}{U(s)} \tag{2.1a}$$

$$H_1(s) = \frac{1}{1 + G_1 B_1(s)} = \frac{Y_1(s)}{U(s)}. \tag{2.1b}$$

Equation 2.1b is the transfer function relating the input to the "error" output of the feedback loop $y_1(t) \longleftrightarrow Y_1(s)$ revealing how quickly and how accurately the loop can respond to match the input function $u(t)$. Since any arbitrary feedback loop might have multiple poles in its feed-back path, without loss of generality the gain function from the system's output $y(t)$, to the summing input node following the feedback path, could generally be approximated as a polynomial function of s such that $B_1(s) = a_n s^n + a_{n-1} s^{n-1} + ... + a_1 s + a_0$. For simplicity, the special case where there is only one pole in the loop is investigated and the feedback becomes of the form $B_1(s) = a_1 s + a_0$. Then equation 2.1b becomes of the form shown in 2.2a and its time domain equivalent differential equation in 2.2b.

$$H_1(s) = \frac{\dfrac{1}{a_1 G_1}}{s + \dfrac{a_0 G_1 + 1}{a_1 G_1}} \tag{2.2a}$$

$$y_1'(t) = -\frac{a_0 G_1 + 1}{a_1 G_1} y_1(t) + \frac{1}{a_1 G_1} u(t). \tag{2.2b}$$

and if these constants are substituted by some figures of merit used to describe analog circuits such as forward gain and frequency where $A = a_0 G_1$ and $\omega = a_1 G_1$

then:

$$H_1(s) = \frac{\frac{1}{\omega}}{s + \frac{A+1}{\omega}} \tag{2.3a}$$

$$y_1'(t) = -\frac{A+1}{\omega} y_1(t) + \frac{1}{\omega} u(t). \tag{2.3b}$$

The change in these constants is inserted to show equivalence of the loops with physical loops one can practically build and test in the lab. The first order differential equation described by 2.3b can be solved and acquire the output of the system for a step response input, by obtaining the state transition matrix, a scalar exponential for this case (eq. 2.4a), then inserting it to the input-output equation 2.4b. Solving equation 2.4c yields the resulting equation 2.4d

$$\phi(t, t_0) = e^{-\int_{t_0}^{t} \frac{A+1}{\omega} d\tau} \tag{2.4a}$$

$$y_1(t) = \phi(t, 0) y(0) + \int_0^t \phi(t, \tau) \frac{1}{\omega} u(\tau) d\tau \tag{2.4b}$$

$$y_1(t) = e^{-\int_0^t \frac{A+1}{\omega} d\tau} y(0) + \int_0^t e^{-\int_\tau^t \frac{A+1}{\omega} d\tau} \frac{1}{\omega} u(\tau) d\tau \tag{2.4c}$$

$$y_1(t) = e^{-\frac{A+1}{\omega} t} + \frac{1}{A+1} \left(1 - e^{-\frac{A+1}{\omega} t} \right). \tag{2.4d}$$

The solution of the output $y_1(t)$ in equation 2.4d is the error accumulation. Due to the exponentials in the equation the solution converges to $\frac{1}{A+1}$ while choosing a larger Gain A enables $y_1(t)$ to converge faster to a value closer to zero with less

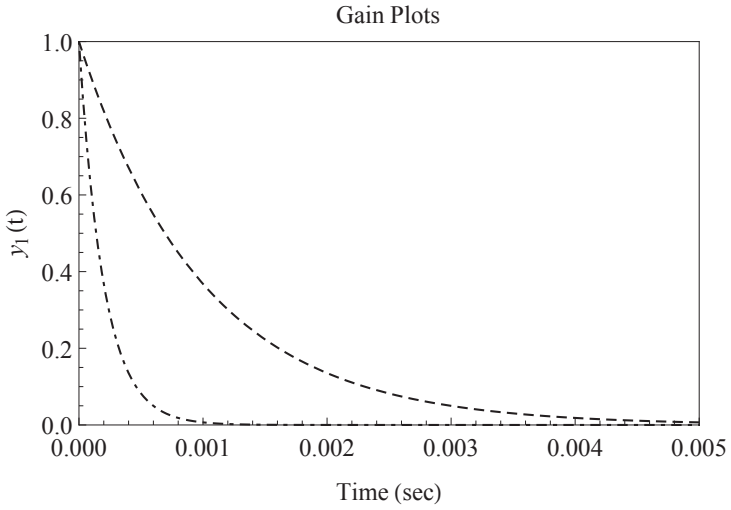


Figure 2.2: Error output with different gains where: Dashed $A = 10^6$, Dot-dashed $A = 5 \cdot 10^6$

residual error at its final point.

2.0.2 Single first order loop with time varying gain A(t)

One family of gain functions $A(t)$ worthy of investigation are of the form

$$\frac{a_0 + a_1 t + \cdots + a_n t^n}{b_0 + b_1 t + \cdots + b_n t^n}$$

where the exact order of the numerator versus the denominator are important in the way the gain evolves as a function of time. Specifically, if the power of the numerator is greater than the denominator then the gain is divergent, tending possibly non-linearly to infinity; if both the powers of the numerator and denominator are the same, these functions become bounded and the gain converges to a constant value or if the power of the denominator is larger than that of the numerator then the gain converges to zero.

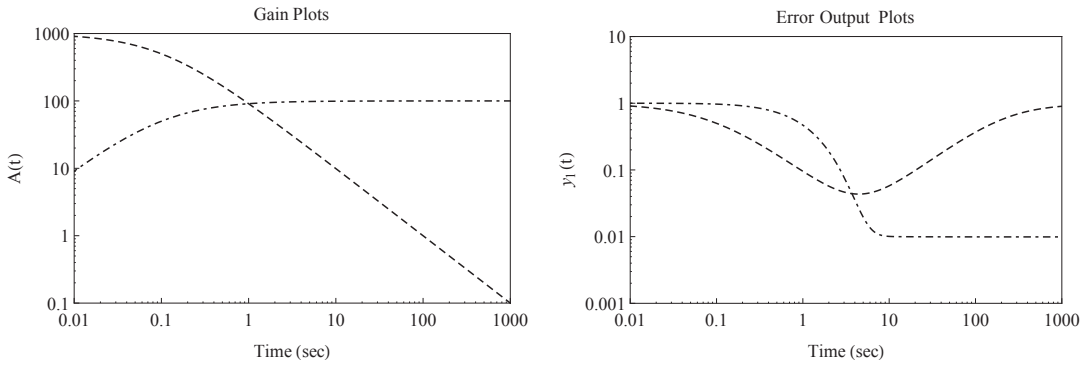
This specific mathematical form is chosen as the most general case of non-periodic, bounded functions, accurately representing a gain that varies with time, first rising to a high value and then becoming a constant. Here, for visualization purposes, the simplest gain function $\frac{a}{1+bt}$ is initially selected and substituted in equation 2.4c to produce the analytical solution represented by equation 2.5. Then a function with one power higher than before in the numerator, namely $\frac{at}{1+bt}$ is selected and substituted in equation 2.4c as before, producing the analytical solution presented in equation 2.6, where $\Gamma(a,z)$ is Euler's extension of the incomplete factorial function $\Gamma(s,x) = \int_x^\infty t^{s-1}e^{-t}dt$.

$$y_1(t) = e^{-\frac{t}{\omega}}\left\{(bt+1)^{-\frac{a}{b\omega}} + \right.$$
$$\left. + e^{-\frac{1}{b\omega}}\left(-\frac{bt+1}{b\omega}\right)^{-\frac{a}{b\omega}}\left[\Gamma\left(\frac{a}{b\omega}+1,-\frac{bt+1}{b\omega}\right)-\Gamma\left(\frac{a}{b\omega}+1,-\frac{1}{b\omega}\right)\right]\right\} \quad (2.5)$$

$$y_1(t) = e^{\frac{a\log(bt+1)-bt(a+b)}{b^2\omega}} +$$
$$+\frac{b^{1-\frac{2a}{b^2\omega}}e^{-\frac{(a+b)(bt+1)}{b^2\omega}}\left(-\frac{(a+b)(bt+1)}{\omega}\right)^{\frac{a}{b^2\omega}}}{a+b}\cdot$$
$$\cdot\frac{\left[\Gamma\left(1-\frac{a}{b^2\omega},-\frac{(a+b)(bt+1)}{b^2\omega}\right)-\Gamma\left(1-\frac{a}{b^2\omega},-\frac{a+b}{b^2\omega}\right)\right]}{a+b} \quad (2.6)$$

Choosing $a = 1000, b = 10$ and $\omega = 100$ for both cases the output gains and error curves are represented in figures 2.3(a) and 2.3(b)

As seen, in the first case the error is minimized and then it slowly returns very close to its initial value of one (Blue line in fig 2.3(b)), as the gain converges asymp-

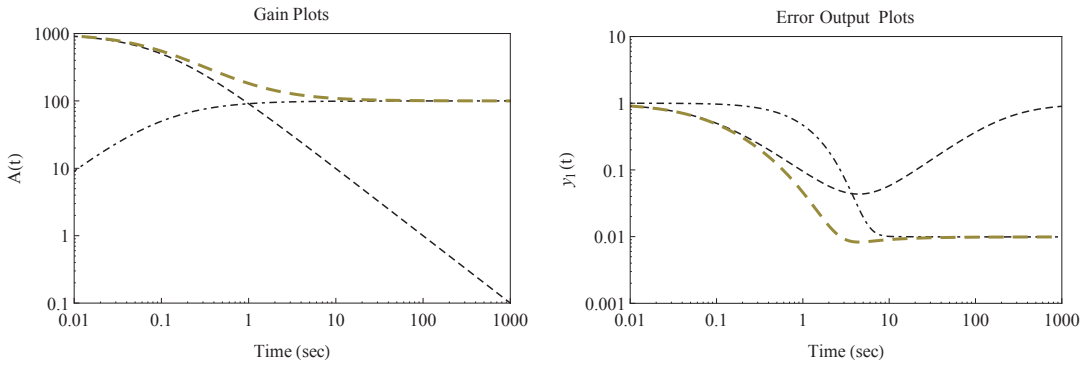


(a) (b)

Figure 2.3: (a) Fractional Gain Function Examples and (b) Error Outputs from Fractional Gains.

totically to zero (Blue line in fig 2.3(a)). The reason is the gain, starting initially from a high value and the "error output" of the loop matches the input, until it droops to values lower than one, increasing the error output of the loop. In the second case, where the gain rises from a relatively small value, converging to a large one (Pink line in fig 2.3(a)), the error converges to a very small value (Pink line in fig 2.3(b)), but that convergence requires longer time due to the smaller absolute gain value in contrast with the first case where the gain initially is really large. In the ideal case the gain should be chosen to be initially high as in case one and then kept steady as in case two in order to minimize the time needed for the $y_1(t)$ "error" output node to settle in a value as small as possible.

It is mandatory for the gain function matching the description above, to have the same order in the numerator and denominator, as well as $A(t) > 1$ at any given time t to ensure convergence. Therefore the gain function would be of the form $A(t) = \dfrac{a+bt}{c+dt}$, where $a, b, c, d \in \Re^+$. For illustration pirposes a function such as $A(t) = \dfrac{1000+1000t}{1+10t}$ is chosen and presented in figure 2.4(a). The analytical solution is found to be of the form presented in equation 2.7.



(a) Fractional Gain Functions

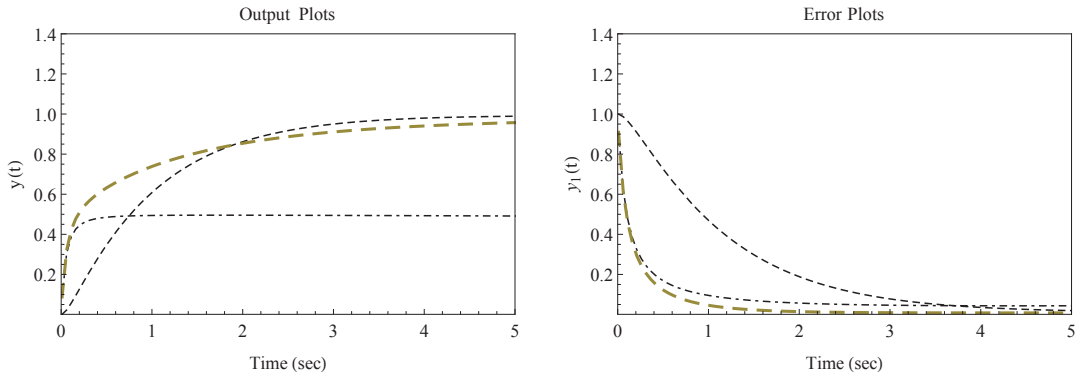
(b) Error Outputs from Fractional Gain Functions

Figure 2.4: Fractional Gain Examples including the combination (Dashed) of the two functions

$$y_1(t) = \exp\left(-\frac{(bc-ad)\log\left(\frac{c}{c+d\ t}\right) + d\ t(b+d)}{d^2\omega}\right) + \frac{d^{\frac{2(ad-bc)}{d^2\omega}+1} e^{-\frac{(b+d)(c+dt)}{d^2\omega}} \left(-\frac{(b+d)(c+dt)}{\omega}\right)^{\frac{bc-ad}{d^2\omega}}}{b+d} \cdot \cdot \frac{\left(\Gamma\left(\frac{ad-bc}{d^2\omega}+1, -\frac{(b+d)(c+dt)}{d^2\omega}\right) - \Gamma\left(\frac{ad-bc}{d^2\omega}+1, -\frac{c(b+d)}{d^2\omega}\right)\right)}{b+d} \tag{2.7}$$

There are many reasons why this gain should be chosen instead of a constant maximum gain that guarantees the output goes to the smallest value possible in the shortest amount of time. One of those is to avoid saturating the output of the comparator node producing non-linearity problems. To further clarify, the functions $y(t)$ and $y_1(t)$ from figure 2.1 are presented as linear functions of time shown on figures 2.5(a) and 2.5(b).

Note that the output converging faster to the steady state value, as expected, comes from the loop implemented with a gain having equal order polynomials to the numerator and denominator respectively (green dashed line) in figure 2.5(a).



(a) Plots for node $y(t)$ (b) Plots for node $y_1(t)$

Figure 2.5: $y(t)$ and $y_1(t)$ linear plots with time. Dashed: $G1(t) = \dfrac{1000t}{10t+1}$, Dot-dashed: $G2(t) = \dfrac{1000}{10t+1}$ and Large-dashed: $G3(t) = \dfrac{1000t+1000}{10t+1}$

The same loop's error node value in figure 2.5(b) (green dashed line) is the one converging to zero in a shorter amount of time as well. These useful observations provide insight into how a loop is forced to converge to a value with more accuracy just by implementing a time-varying gain control function.

In reality such functions do not always have an analytical solution and if they do it has an extremely complicated form. This is clear to all of the cases described and solved previously as well as for instance in equation 2.8 where the output of the loop with $A(t) = \dfrac{1000+1000t}{1+10t}$ is calculated for $\omega = 100\ [rad/sec]$.

$$y(t) = \frac{100000\ \sqrt[10]{-1}10^{7/10}e^{-\frac{101t}{100}-\frac{101}{1000}}(t+1)\left(\Gamma\left(\frac{19}{10},-\frac{101}{1000}\right)-\Gamma\left(\frac{19}{10},-\frac{101(10t+1)}{1000}\right)\right)}{101\ 101^{9/10}(10t+1)^{19/10}} \tag{2.8}$$

Finding a solution becomes harder when the loop is of a higher order and has extra poles in its feedback path. However, analytical solutions and methods of solving

such higher order loops can be found utilizing the approach presented in this chapter; More over they can be translated to a circuit with direct practical application in the uniform brightness display driver described in chapter 4.

2.0.3 Control Loop Basics

Similar multiple loops for systems that provide their internal variable for control through negative feedback have been analyzed in the past [5, 6], with stability as a main focus for analysis. This is because most applications use feedback as a form of system control, forcing the system operation within the bounds of its control loops to achieve a desired behavior. That leads to forward gain limiting satisfying the Nyquist criterion for stability, placing poles correctly on the Left Half Plane (LHP).

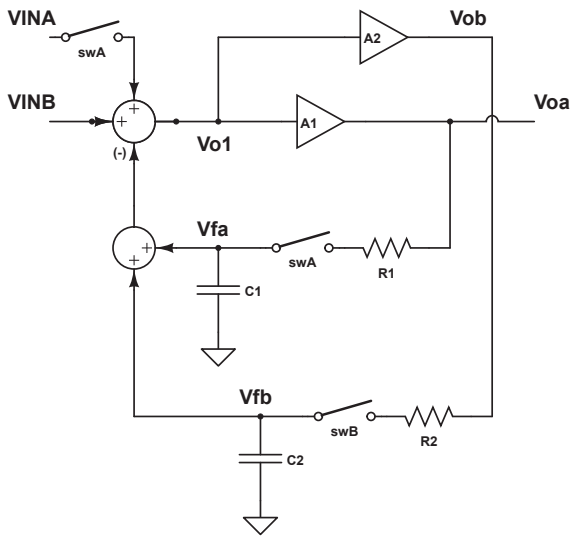


Figure 2.6: Switched Muliple Feedback Control Loops

The addition of switching between multiple feedback loops, renders stability as

not the sole plant variable describing the system. Dynamic range is another variable worthy of investigation where for example, a system with multiple feedback loops operating in different time slots (figure 2.6), accumulates error, making sensitivity as a plant variable that is available for control via feedback. Figure 2.6 is the direct mathematical representation of multiple feedback loop. Node Vo1 in figure 2.6 is responsible for accumulating error due to the finite time in each of the loops operation.

Many techniques exist for minimizing error accumulation at the output of the summing node. Some of them include variation of switching time between loops of different gains therefore different accuracies, or the ability to vary the forward gain of these loops with time. The second technique is the continuous subcategory equivalent of the first in which the two loops are forced to track two different values that differ by orders of magnitude added to the same node while minimizing the error in both cases.

The complexity is increased dramatically even for the case of a simple single pole loop if the system is not Time Invariant as in the example of the second technique mentioned above, where the forward gains of A1 and A2 in the case of figure 2.6 are introduced as functions of time. Specifically, when the goal is the minimization of the accumulated error, choosing the right function for implementation in the forward gains becomes more important than simply ensuring the stability of each loop. The main reason for this is the time limitation that exists due to switching in the amount of time each gain is operational.

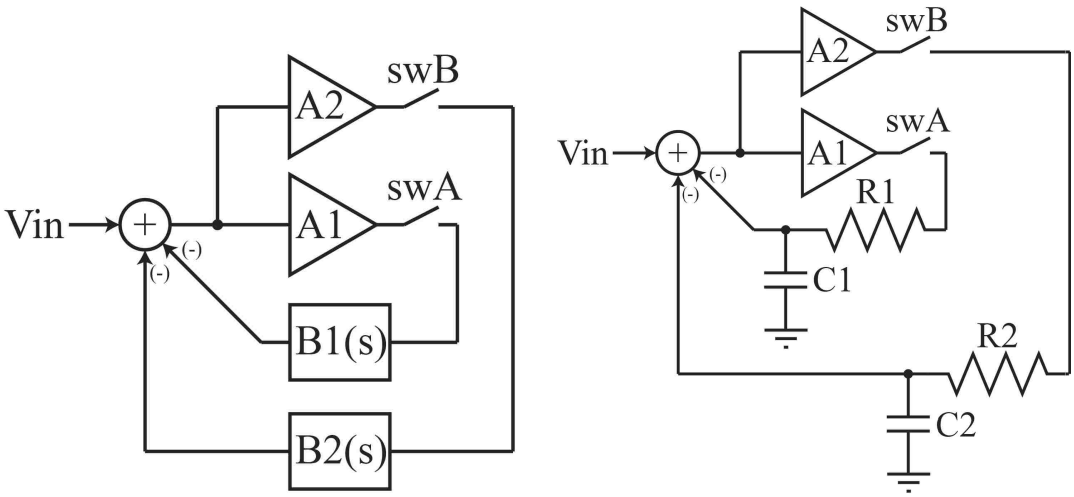
Therefore in order to maximize accuracy in shorter times, the poles of each loop are allowed to exist in the Right Half Plane (RHP) rendering the system unstable for a short period, as long as their projected trajectories move them back to the LHP at the end of the loop's operation.

As a consequence, there exists only one family of functions allowed to implement the loops' forward gains. Another research goal of this dissertation is to investigate methods in discovering such functions that lead to loops with wider dynamic ranges, operating in shorter times and for smaller signals as well as their translation into practical applications for implementation in a display driver.

It is critical to mention at this point that although mathematically it is sound to choose gain A as large as possible, but when the order of the loop is greater than one, the maximum gain becomes limited to lower values. Things become even more complicated with some of the applications mentioned here that operate in discrete time. Moreover, there is also an accumlation of error in many cases where the loop has to operate at a predetermined short time due to wide bandwidth signals, found for example is numerous sample and hold applications.

To better illustrate the problem let's assume an example of a modern sample and hold application where the signal $u(t)$ has a small and a large component with $u_L(t) = 1$ and $u_S(t) = 10^{-6}$, while the chosen gain is $A = 100k$ and assuming that the loop does not operate within a predetermined fixed time, then $y_1(\infty) = 9.999 \cdot 10^{-6}$. That shows that the smallest signal this loop can detect in the presence of the large unit step has to be greater than 10^{-5}. One way of solving this problem is by utilizing a multiple loop technique that utilizes two loops with different gains: A fine, higher gain loop locked to the small signal and a coarse, lower gain loop locked to the larger signal present at the input.

Those two loops must operate within two separate time slots in order to minimize the error. First the coarse loop locks on to the large signal leaving a residual error to be absorbed and almost eliminated by the fine loop due to its higher gain. This multiple loop setup's block diagram is shown figure 2.7 and the proposed operation



(a) Fine and coarse loop block diagram. (b) Error Outputs from Fractional Gains

Figure 2.7: A coarse and fine setting multiple loop representation.

happens as follows:

First swA closes and then assuming that both gains $A1$ and $A2$ are $100k$, loop 1 comprised of $A1$ and $B1$ produces an output $V_{O1} \sim 10^{-5}$. After swA becomes an open circuit and swB is closed, loop 2 comprised of $A2$ and $B2$ is programmed with $V_{O1} \sim 10^{-5}$ and produces as its output $V_{O1} \sim 10^{-10}$. It is now immediately clear that the total error is 4 orders of magnitude smaller than the smallest input, therefore $u_S(t)$ error is 0.1%, and $u_L(t)$ is 1ppm, enabling input signals with components down to 1ppm to be sensed accurately in this way.

2.1 Adding more to the complexity

All the loops described previously in this chapter have been first order. In reality, complex active control loops around real amplifiers rarely are of the first order, generally having more than one poles in their feedback path. Their output response

for a step input some times includes ringing due to various reasons as for example when the designer of such loops has no option but to place the poles of that loop close to the imaginary axis on the left half plane, creating ringing in the transient output response of the system.

On the other hand, looking at the output solution of the same LTI system as shown in figure 2.8, if the poles are close to the $r = \pm jm$ lines (black line in figure 2.8), there is little ringing at the system's response, but having them closer to the imaginary Axis (red line in figure 2.8) that ringing dominates the output of the circuit. The most important point by empirically observing the system is clear: the output in the case of the red line in fig. 2.8, will intersect the steady state value for the first time faster than the black line in the same figure since the red line crosses the steady state line at 0.12 but the black makes it at 0.28 (normalized unit-less time). Unfortunately ringing remains a problem. It can only be completely eliminated if the poles initially are placed exactly near the imaginary axis but moved closer to the $r = \pm jm$ lines as the transient progresses.

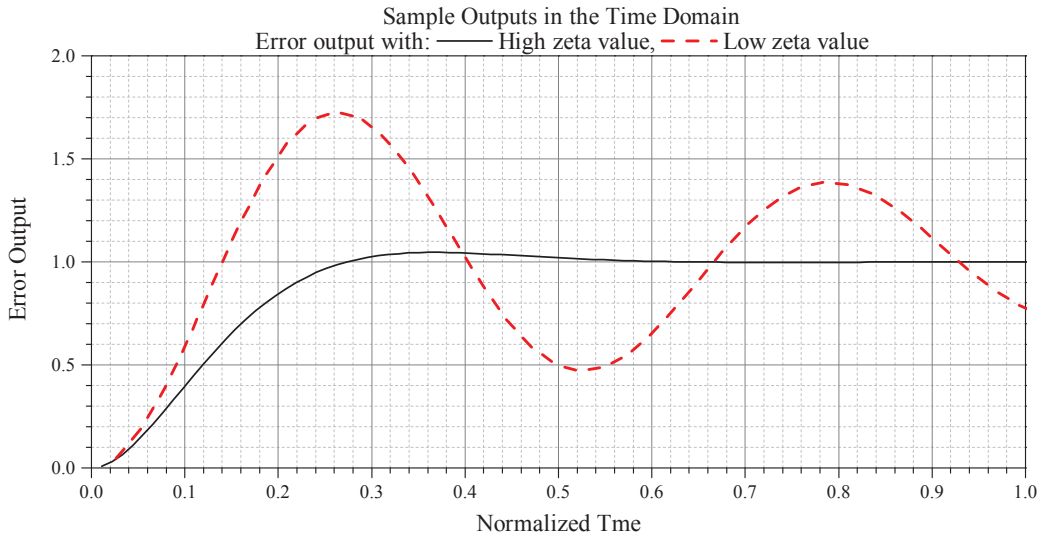


Figure 2.8: Transfer function Solutions for a system with poles close to (red) the $r = \pm jm$ line and (black) the real Axis.

Later in this dissertation an approach utilizing the coarse and fine setting technique described in this section is presented and a practical circuit is designed based on that approach to program displays. Moreover, that circuit could become a Linear Time Variane (LTV) circuit, minimizing the transient time.

Chapter 3

Applications of novel Feedback Techniques in Modern Organic Light Emitting Diode Displays

3.1 Introduction

FROM the different appropriate flat panel technologies for displays, the ones based on Light Emitting Diodes are the strongest candidates, for they achieve the highest quality with the lowest power consumption. Those LEDs are fabricated "en masse" on a large area substrate, forming arrays of active illuminating cells that can be controlled electronically through a driver to produce pictures and images, resulting in a machine-human interface known today as the Active Matrix LED Display. Since some of the materials used to form the active illuminating cells are organic, those displays were named Active Matrix Organic Light Emitting (AMOLED) Displays.

3.2 The Problems of Conventional Display Drivers

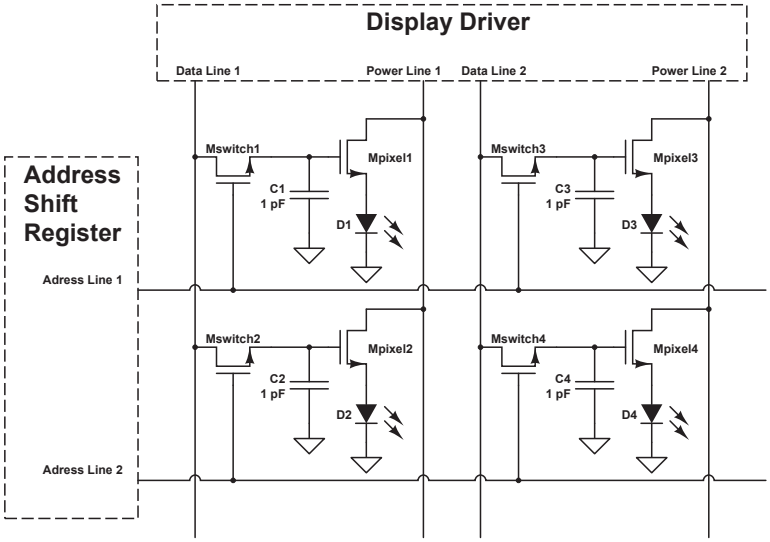
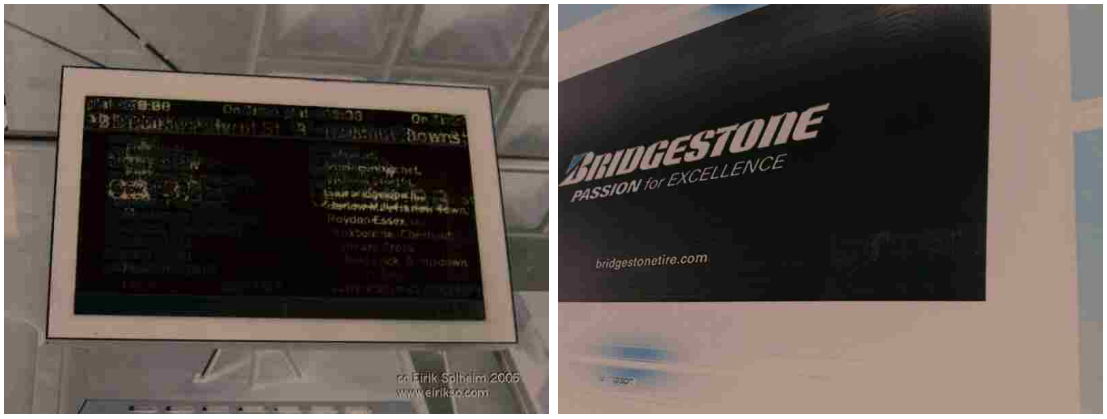


Figure 3.1: A conventional 2-TFT pixel circuit array

The driving scheme of AMOLED displays has been the topic of research and innovation for over ten to twenty years. The basic pixel circuitry used in such displays consists of two Transistors and one Capacitor where one transistor is used as a switch and the other one as a current source driving the Light Emitting Material (figure 3.1). This approach was initially proposed for active matrix electroluminescent displays in 1975 by Brody et. al. [7] and it is a variation of this scheme that is still used today by modern LCD display manufacturers.

In the case of AMOLED displays the drive transistor controls the amount of current sourced in the OLED device through the square law formula making its current dependent on parameters, such as threshold voltage and mobility, rendering this pixel circuitry sensitive to variations of such device parameters.

$$I_{DS} = \frac{K'_n}{2}(V_{GS} - V_{TH})^2 \tag{3.1}$$



(a) (b)

Figure 3.2: Image Burn in examples.

According to equation 3.1 if a constant voltage that corresponds to the same brightness level of an image, is stored at the capacitors of two different pixels that differ in their K'_n and V_{TH} values, then they will produce different currents through their channels making their respective LEDs illuminate with different brightness intensity. Some examples of such a failure in displays is seen in figure 3.2.

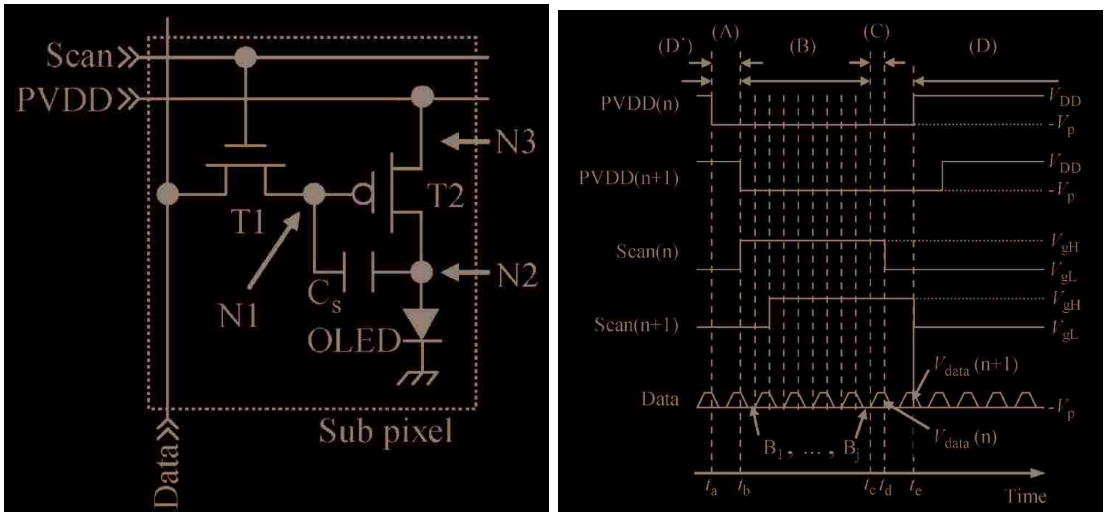
These problems caused by variations in mobility and threshold voltage can be overcome by compensating the data programmed to the pixel through Data Pulse Amplitude Modulation (DPAM). The DPAM technique can be classified into three distinct groups such as (I) Multiple TFT pixel circuit compensation, (II) Digital External Feedback and (III) Analog External Feedback.

The first group (I) includes circuits that deploy from 3 to 6-TFTs per pixel [8–17] for sensing the TFT characteristics in order to adjust the Pulse of the Data being programmed to the pixel. These topologies are utilized either for the electronic compensation of the threshold voltage shift [10,18], [16], the mobility degradation or both [8,9], [11,12]. However, as it is obvious to the reader, these approaches may be difficult to implement in high resolution mobile displays (cellphones, tablets) as the

large area required by the complex pixel circuitry may not be available. Furthermore, the multitude of additional components (TFTs and control lines) may result in a lower manufacturing yield, especially for large display sizes.

In the second group (II), the brightness non-uniformity issues are solved with the help of a digital feedback loop which is external to the pixel circuit on a separate platform [8], [9]. A constant current is forced through the pixel and the drain voltages of all the driving TFTs are measured and stored to an external memory during the display off time. These values are compared to the new values gathered after the display on time and the Vth shift corresponding to the degradation during the off time of the display is extracted. This method requires extra sense lines in the array and at least one more transistor per pixel. Furthermore this approach does not correct for the degradation during the display on time and the external memory that stores the drain voltages of all the display transistors adds extra system complexity.

In the third group (III) category the driving TFTs characteristics such as threshold voltage and mobility are sensed and the Data Pulse's Amplitude is modulated at the same time during the pixel's addressing time. The TFT sensing and Pulse adjusting happens external to the display, such as in a separate silicon chip or in the integrated display driver [11], [13], [16]. Still, a 3-TFT 1-Capacitor circuit is the best method utilized thus far for sensing the characteristics of the driving transistor, which in turn implies the use of two extra lines one for addressing the third TFT and one for the current sense line. The extra transistor and lines contribute to more components per unit area which may affect the yield or the display resolution.



(a) New 2-TFT 1-Capacitor Compensation circuit

(b) Timing Diagram

Figure 3.3: 2T1C Circuit proposed by S. Ono et. al. along with the timing diagram.

3.3 Group I: Examples of pixel-internal compensation circuits

3.3.1 Internal Compensation: A 2T1C Approach

In 2007 S. Ono et. al. [16] proposed a technique that utilized only 2-Transistor 1-Capacitor without the aid of external feedback. The pixel circuit described in their paper, was comprised of a slightly different architecture than the traditional 2T1C proposed by Brody at. al. as shown in figure 3.1, where the capacitor was connected from the Drain of the pixel drive transistor to the Gate instead of the Gate to the Source.

The operation of the circuit utilized four steps: Prepare, Program V_T, Write Data and Emit. In the prepare step f the circuit, beginning at $t = t_a$, as presented in the timing diagram of figure 3.3, The PVDD line becomes $-V_P$ and the node voltages are

$V_{N1} = V_{data}^{0} + \delta V$, $V_{N2} = V_{OLED,th}$ and $V_{N3} = -V_P$, where $\delta V = V_{OLED} - V_{OLED,th}$.

Next during the program V_T step, at $t = t_b$ the scan line is changed to V_{gH} and the detection is repeated j times due to the large capacitances $C_S + C_{OLED}$ retaining the charge while the pixel drive transistor is forced to conduct in reverse to discharge them and discover the V_{th} of the transistor. The time constant is described as $\tau_S = \frac{2\,(C_S + C_{OLED})}{\beta}$ and it is obviously dependent on those capacitances as well as the beta ratio of the transistors discharging them. When V_{N2} becomes less than the threshold voltage of the OLED, T2 will turn off when V_{th} is stored in C_S. Then at time $t = t_C$ the node voltages become: $V_{N1} = -V_P$, $V_{N2} = -V_P - V_{th2}$ and $V_{N3} = -V_P$.

At the Write Data step, the scan line becomes V_{gL} at $t = t_d$ and the node voltages are: $V_{N1} = V_{data}$, $V_{N2} = \frac{C_S}{C_S + C_{OLED}}\,(V_{data} + V_P) - V_P - V_{th2}$ and $V_{N3} = -V_P$. The voltage stored in the capacitor C_S is:

$$C_S = \frac{C_{OLED}}{C_S + C_{OLED}}\,(V_{data} + V_P) + V_{th2}. \tag{3.2}$$

Finally during the emit step, the node voltages are: $V_{N1} = \frac{C_{OLED}}{C_S + C_{OLED}}\,(V_{data} + V_P) +$ $V_{th2} + V_{OLED}$, $V_{N2} = V_{OLED}$ and $V_{N3} = -V_{DD}$. The transistor becomes forward biased once again, the total current carried by the transistor is described by equation 3.3, which is not dependent on the threshold voltage of the transistor.

$$I_{SD} = \frac{\beta}{2}\left[V_{DD} - \frac{C_{OLED}}{C_S + C_{OLED}}(V_{data} + V_P) - V_{OLED}\right]^2 \tag{3.3}$$

It should be noted at this point that an approach utilizing the aforementioned 2-TFT, 1-Capacitor pixel circuit reported by S. Ono et. al. [16], would require a high speed switching scheme. This is necessary in order to sense the TFT characteristics and avoid the large detection time constant that is imposed by the storage capacitor tied to the gate of the pixel in conjunction with the capacitance of the OLED material. However, in certain cases such as displays when is needed to operate at fast frame times the Ono technique may be impractical. Moreover this approach is valid only for technology nodes that retain the same doping in the Source and Drain, therefore the same forward V_{gs} and reverse V_{dg} threshold voltages for the T2 PMOS driving the OLED.

3.3.2 Internal Compensation: A 4T1C Approach

In 2003 Joon-Chul Goh et.al. [19], presented a pixel compensation circuit with 4T2C and five lines. Before the description of the circuit's operation, it is noted that transistor T1 as seen in figure 3.4 has to be designed and sized to be in the subthreshold region during the entire operation of the pixel circuit. The three steps are Reset, Compensate and Input Data.

In the first (step (1) in figure 3.4), the pixel is reset. During the compensate step, the source of T1 has $V_{comp} - \delta V$ and C1 stores V_{th1} while at the Input Data step the gate of T1 has $V_{INPUT} + V_{th1}$. The difference of the gate voltage between the compensation and the Data Input steps is presented in equation 3.4.

$$\Delta V_{gs} = V_{INPUT} + V_{th1} - V_{INPUT} + \Delta V_{INPUT} - V_{th1}. \tag{3.4}$$

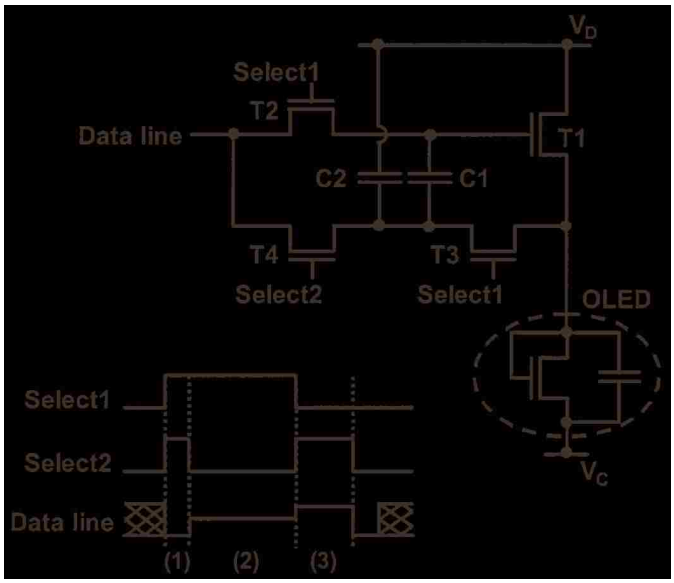


Figure 3.4: J.C. Goh's 4T2C Pixel circuit and timing diagram.

Note that the subthreshold slope equation in Volts/Dec. is of the form

$$S_t = \frac{\Delta V_{gs}}{\Delta Log(I_{ds})} = \frac{V_{INPUT} + V_{th1} - V_{INPUT} + \Delta V_{INPUT} - V_{th1}}{Log(I_{out}) - Log(I_{comp})}. \tag{3.5}$$

And for a low temperature polysilicon technology with a very large subthreshold slope, ΔV_{INPUT} has no effect in the output current, therefore that current is directly controlled by V_{INPUT} and it is independent of V_{th} and μ variations. One of the downsides of this technique, that is often overlooked, is that the transistor is biased to be in the sub-threshold region where the current being carried by the drive transistor is directly proportional to the voltage across the Drain to Source terminals, therefore the slightest change in series contact resistance from pixel to pixel would create variations independent of the uniformity of threshold voltages and mobilities of the pixel transistors. Another downside is associated with the technologies utilized in displays, where sometimes the sub-threshold slope S_t would not always be very large,

as a result this compensation technique is still highly process-dependent.

3.3.3 Internal Compensation: A 5T1C Approach

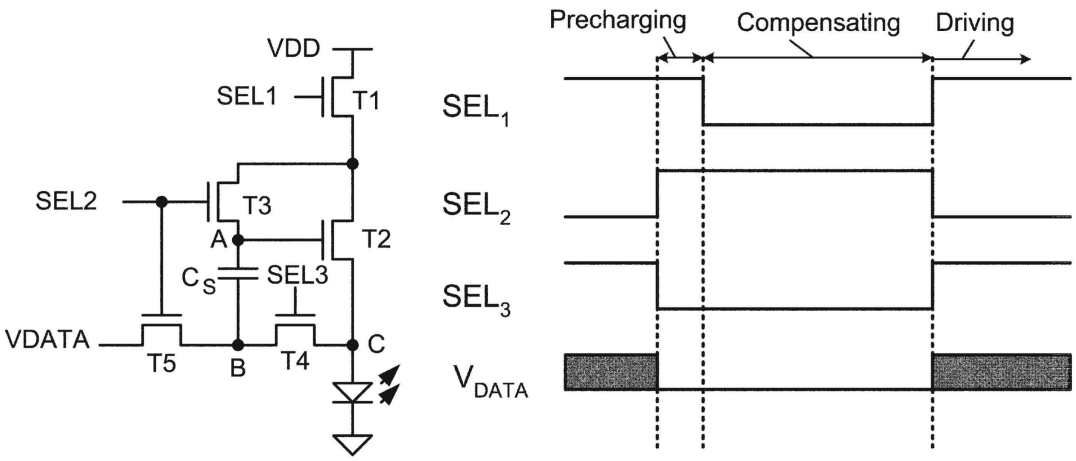
This family of pixel circuits has had a couple of permutations when it was proposed by two separate groups, first During 2007 by S. J. Ashtiani [10] and later in 2008 by C. L. Lin. [12]. This circuit has three phases of operation, the precharging, the compensating and the driving phase.

During the precharge phase node A as shown in figure 3.5 is at VDD and V_{data} is set to $-V_P + V_{OLED1}$. Then at the compensating phase, SEL1 becomes low and the capacitor is being discharged through the transistors. Node A is $V_{T2} + V_{OLED}$ and the voltage across C_S then becomes $V_{CS} = V_{T2} + V_{OLED} - V_{OLED1} + V_P$. Finally during the driving phase the C_S voltage of the capacitor becomes the Gate to Source voltage of the driving TFT. Figure 3.5(c) presents the three phases of operation to better illustrate the steps of operation of that pixel circuit.

Note that the current carried by T2, presented in equation 3.6, is not dependent on T2's threshold voltage and it is quasi dependent on the difference quantity ΔV_{OLED}.

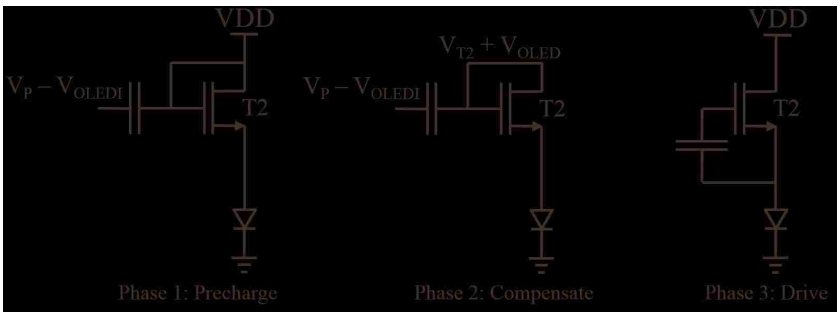
$$I_{DS} = \frac{k^{'}}{2}(V_{th} + \Delta V_{OLED} + V_P - V_{T2})^2 = \frac{k^{'}}{2}(\Delta V_{OLED} + V_P)^2 \tag{3.6}$$

This circuit provides an excellent alternative for designs where the threshold voltage variation is large but unfortunately it does not provide any mobility compensation, therefore when the material ages with time and the mobility drifts from



(a) The 5-TFT 1-Capacitor Compensation circuit

(b) Timing Diagram



(c) The three step process of operation of the circuit proposed by S. J. Ashtiani.

Figure 3.5: 5T1C Circuit proposed by S.J. Ashtiani along with the timing diagram. Note that the same ciruit schematic can be used for C. L. Lin's permutation having both SEL3 and SEL1 lines connected together. Figure 3.5(c) shows the three phases of operation.

its original value, still some of the pixels might have visible brightness degradations. More importantly the circuit within the pixel utilizes a lot of line and a lot of transistors making it harder to deploy for larger resolutions as the overhead for designing a display with that circuit increases quadratically.

3.3.4 Internal Compensation: A 6T1C Approach

A yet a more complex compensation technique with 6T1C and seven lines was presented from C. L. Lin in 2011 where the circuit again operated in three stages, Reset, Compensation and Emission.

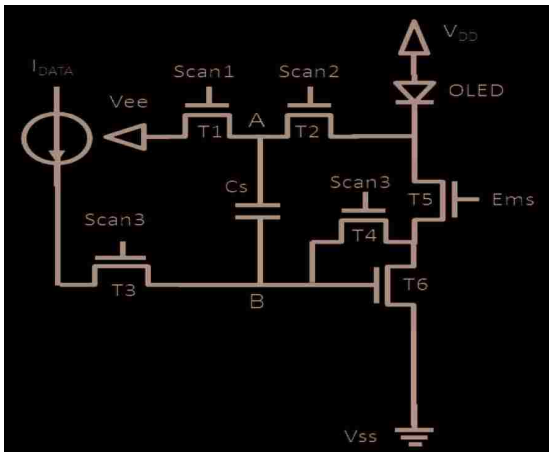
First, as shown in the timing diagram of figure 3.6(b), the pixel is reset. Then, during the compensation phase as node A approaches $VDD - V_{TH,OLED}$, I_{data} is forced through T3, T4 and T6. The voltage at node B is described by equation 3.7.

$$V_B = \sqrt{\frac{2I_{data}}{k}} + V_{th6} \tag{3.7}$$

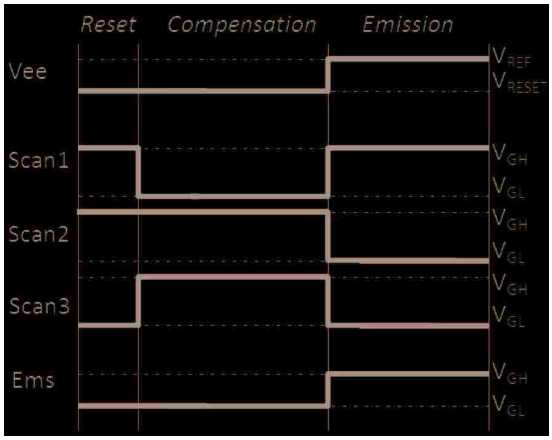
During the emission stage the voltage at the node A is set to Vref again as a result the voltage at node B becomes $V_B = \sqrt{\frac{2I_{data}}{k}} + V_{th6} + V_{ref} - VDD + V_{TH,OLED}$ as a result the total OLED becoming as shown in equation 3.8

$$I_{OLED} = \frac{1}{2} \cdot k \cdot \left(\sqrt{\frac{2I_{data}}{k}} + V_{ref} - VDD + V_{TH,OLED} \right)^2 \tag{3.8}$$

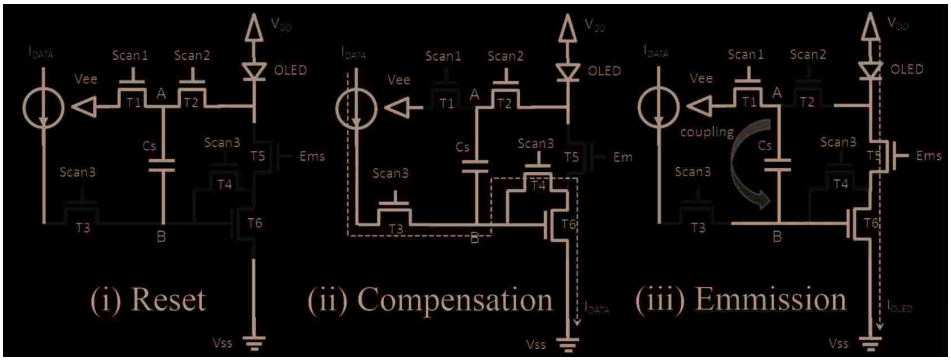
At this point it should be noted that the upsides of this technique is that there is no dependency on V_{TH6} and the current I_{data} has a linear relationship with I_{OLED}, as a result capacitor C_S is being charged with a larger current permitting it to operate at higher speeds. To add another benefit to the list of benefits, the aging effect of the driving TFT (T6) is also compensated with this method. The downside of the described circuit is the tremendous overhead resulting form the plethora of



(a) The 6-TFT 1-Capacitor Compensation circuit



(b) Timing Diagram



(c) The three step process of operation of the circuit proposed by C. L. Lin.

Figure 3.6: 6T1C Circuit proposed by C. L. Lin along with the timing diagram. Figure3.6(c) presents the three steps of operation.

required signal lines as well as the number of TFTs per pixel implementing such a setup, making it less useful for higher ppi displays implemented with the current technology.

3.4 Group II: Examples of Compensation Circuits External to the Displays

In this Group, the compensation circuits include feedback loops implemented externally on in the periphery of the display backplane. There are three subcategories associated with this group, namely Digital External Compensation, Analog External Compensation and Hybrid External Compensation circuits. To better illustrate the general technique, a block diagram of an external Analog feedback loop is presented in figure 3.7.

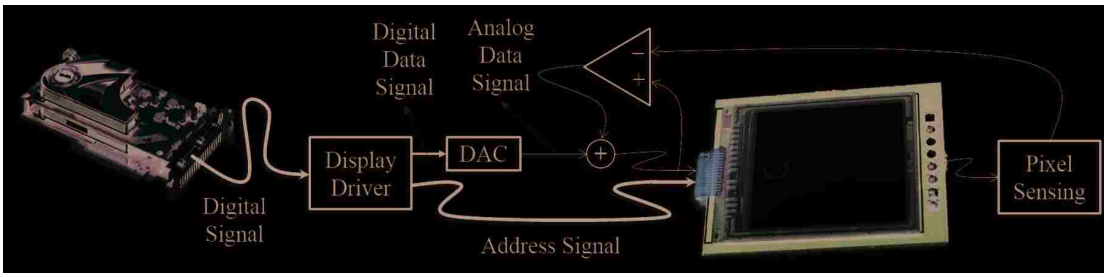


Figure 3.7: External Compensation scheme.

Note that the signal provided by the graphics card is always in a digital form. The difference between the first two categories is whether the sensing that takes place, is implemented through digital or analog circuitry. In the case of figure 3.7, the sensing is analog and the Data Pulse Amplitude Modulation (DPA-Modulation or DPAM) taking external to the display does not involve any extra digital circuits storing and recalling digital values, therefore the technique presented in this block diagram is a form of analog DPA-Modulation.

3.4.1 Digital External Compensation: A 3TFT Approach

During 2010, H.J. In et. al. [8] came up with a simple pixel structure using a video data correction method for pixel circuit compensation. Specifically, they utilized an external digital driver IC to extract and store the Vth characteristics of the TFTs and the OLEDs. They external digital circuit they utilized is shown in figure 3.8

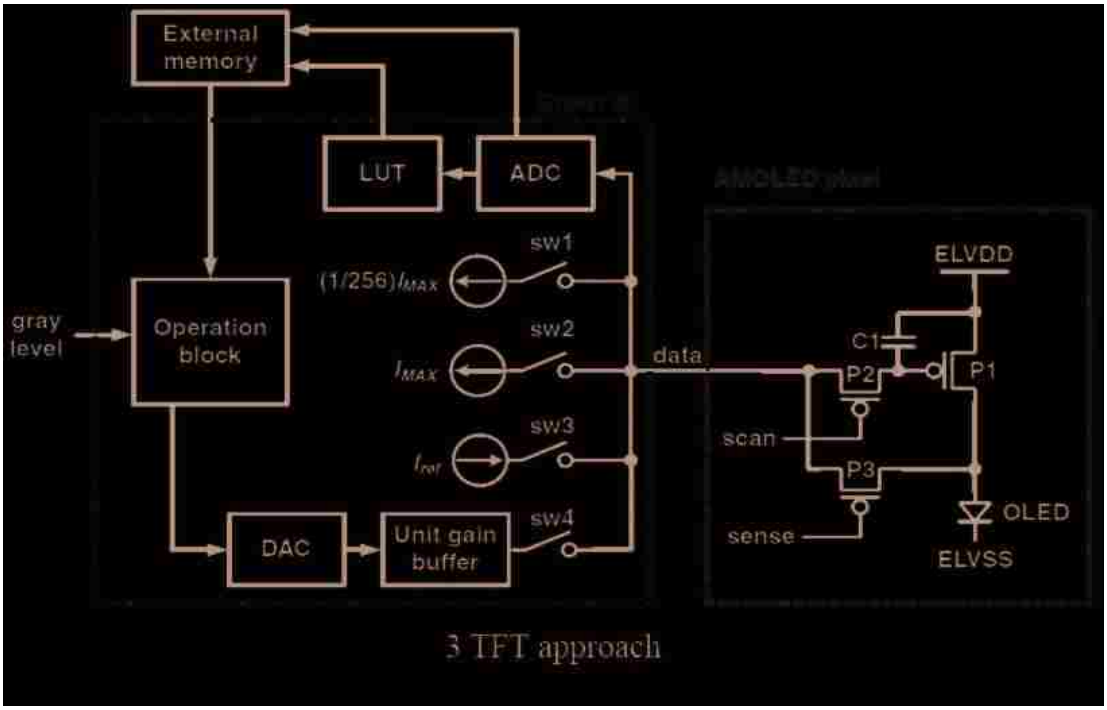


Figure 3.8: Digital External Compensation.

The circuit's operation happens in three steps. During the first step, ELVSS becomes a high potential and the lowest gray level (Imax/256 for this case) flows through transistors P1 and P3. The data line voltage is memorized and this procedure repeats itself for the highest gray level Imax. The two measured potential levels are stored and utilized to extrapolate the degradation of P1.

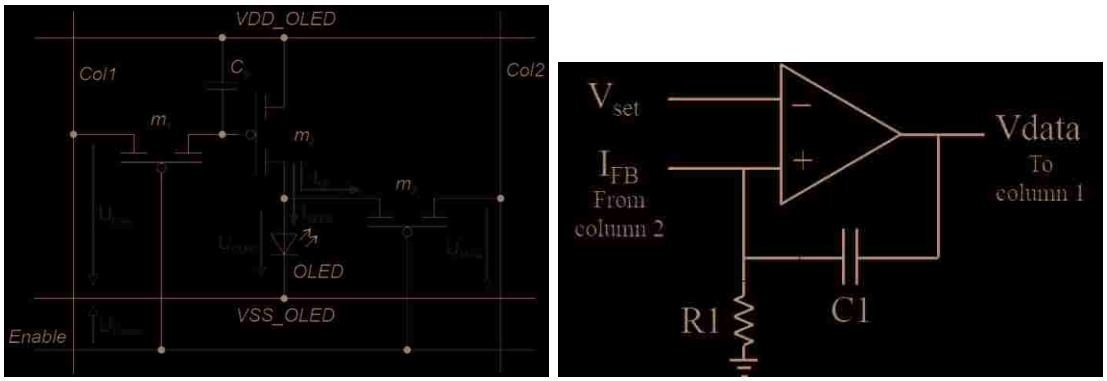
During the second step of operation, ELVDD and ELVSS become low, Iref is forced through the OLED and the data line voltage is stored. A dummy OLED

integrated on the periphery of the display driver is utilized to compare it against the pixel's OLED and calculate the degradation. During the third step of operation, sw1, sw2 and sw3 are open and sw4 is closed. ELVDD is high and ELVSS is low. The scan line turns P2 on to receive the gray level modulated according to each individual pixel's drive transistor and OLED.

Although this is a very powerful technique, able to compensate even the most extreme of cases, it gets quite involved with designing the digital code and architecture of such a system. Moreover, the required memory that stores and extrapolates the LED's degradation can be quite large in specific cases, something of a problem, especially for portable displays.

3.4.2 Analog External Compensation: Alternate 3TFT Approach

In 2011 P. Schalberger et. al. [11], presented an analog feedback technique. In his implementation, one capacitor and five lines where included. The operation of the circuit utilized 4 distinct steps:



(a) Analog feedback Architecture with an Alternate 3-TFT pixel circuit approach.

(b) Timing Diagram

Figure 3.9: Analog feedback Architecture P. Schalberger et. al..

First the enable line became low, adressing the row of pixels. Then, in the second step, the VSS_OLED line is set to a potential greater than half of that of Vcol2, forcing the current through the pixel to flow through Col2 and into the driver. The driver was comprised of a current comparator with its plus and minus imputs connected to a reference and Col2 and its output attached to Col1. This driver is responsible for comparing the two currents, modulating the voltage at Col1, which would be stored in pixel's capacitor Cs as shown in figure 3.9. Once the loop finds equilibrium, the current carried by m_2 is forced to the OLED.

Note that the external driver is an analog driver and it is mandatory for the operation of the circuit. During the second step of the loop's operation the driver's Vset is set to the desired value and I_{FB} is initially zero. Therefore Vdata becomes Large. When I_{FB} starts to flow through Col2 in the second step of operation, it raises the potential to the plus input terminal of the amplifier, thus lowering Vdata. The loop finds equilibrium only once $I_{FB} \cdot R1 = V_{set}$.

Having described the previous example, it is clear that this category seems to be the most promising of all of the above. It utilizes external drivers and few additional components per pixel to achieve its functionality. However, this circuit still suffers from significant disadvantages such as 3TFTs/pixel, an extra sensing line per column and an integrating filter in its feedback path making its response time extremely slow.

There is very little research done in this specific compensation group due to misguided popular belief that all external analog current feedback drivers are slow because they drive capacitive loads with tiny current sources.

In this dissertation we are going to shatter this misguided belief by delving deeper into the operation of active circuits, utilizing some of the most fascinating techniques of linear time varying circuits, to produce amazing results, adding to the knowledge

on this field and expanding the ever growing horizons of the analog circuit principles in design!

3.5 Group III: Examples of Digital/Analog Hybrid Compensation Circuits

There are very few circuits associated with this approach. However R. P. Le et. al. has come up with a Analog/Digital Feedback hybrid external circuit [20], which has two modes of operation.

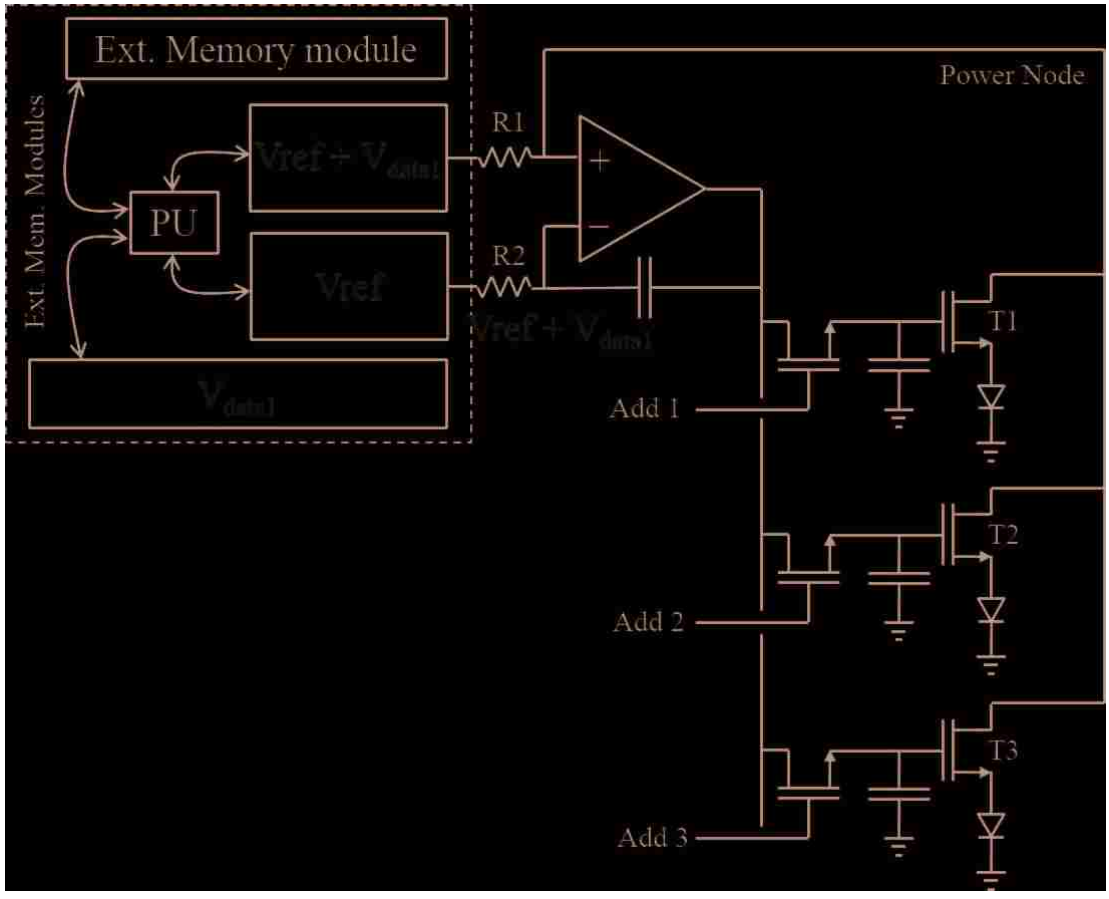


Figure 3.10: Hybrid Digital/Analog Circuit described by R. P. Le.

The first mode of operation has five steps. In the first step, the column memory module is loaded with Vref. In the second step, the Reference memory is modulated with Vref for the addressed pixel. During the third step the external memory module is queried by the processing unit (PU) for Vdata to store it to the temporary memory module. In the fourth step, the column memory is modulated by the PU to generate a current though resistor R1. Finally, when the minus and plus input terminals of the opamp are at the same potential the loop finds equilibrium and the process repeats it self with the only variation that for each addressed pixel, Vref becomes $Vref = Vref + Vdata_{(n-1)}$

The second mode of operation is a lot more straighforward, because each pixel is programmed individually and loaded to a separate power node during its non-addressing time through circuitry not display in the schematic shown in figure 3.10.

This technique has a lot of upsides such as accurate programming and it could also work adequately fast for modern displays, it combines however all of the shortcomings of the digital external architectures as well as the integrating capacitor also found in the previously proposed external analog technique. This not only renders the system complex, but also its performance is slow due to the presence of an integrating external capacitor.

Chapter 4

A new compensation method and Initial Implementation from Display Research Lab

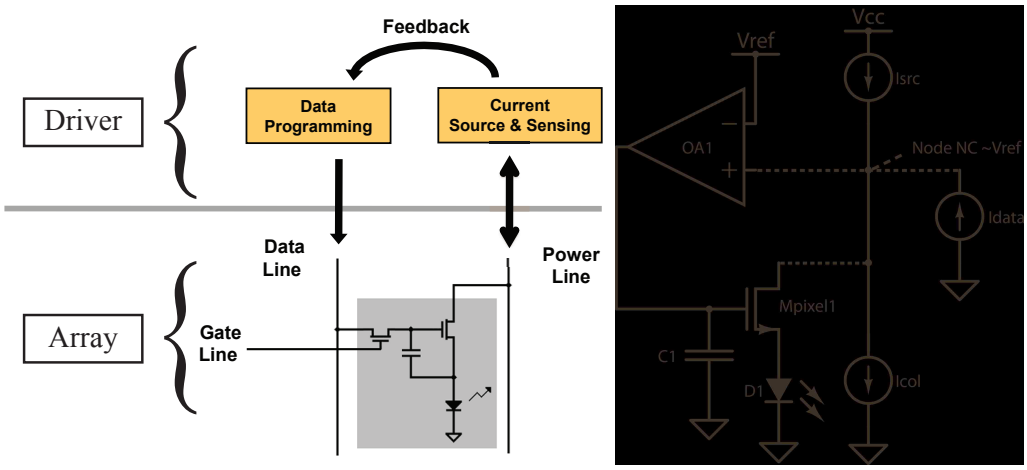
4.1 Introduction

4.1.1 Basic principles

The first and most important goal of the proposed research work is to present solutions to overcome the above issues via a new principle based on the current feedback method and driver architecture compatible with the 2-TFT 1-Capacitor pixel circuit. The current feedback technique incorporated in an external loop is not to be rejected, but better implemented with a different sensing and programming scheme. As presented in [21], a high speed, high resolution circuit based on external feedback principle could be devised, interfacing externally with the display that would satisfy

the most demanding of applications that exist today.

In order to elaborate further, the basic principle behind the feedback loop is presented and briefly analyzed. A 2T-1C pixel circuitry within an AMOLED TFT backplane requires an address (or scan) line, a data line and a power line. The power line however, could be utilized to both supply the current carried by the pixels of that line as well as sense the current that is programmed at the addressed pixel. In the driver external to the active matrix array shown in figure 4.1, a feedback circuit between a data line and a power line is used to adjust precisely the current at the addressed pixel during the addressing time.



(a) Block Diagram (b) Circuit Schematic

Figure 4.1: Basic Principle

Specifically, figure 4.1(a) shows that the drain of each transistor Mpixel is connected to a high impedance node. Starting with the Mpixel transistor turned off, if this high impedance is driven with a current source, the potential will rise at the node where the current source is applied. Consequently that voltage is be sensed and applied to the gate of the transistor Mpixel, which in turn lowers the potential at the Drain, while forcing the transistor's I_{DS} current to be equal with that of the current source.

Our approach eliminates the need for an extra sensing line since the power line can also be used for sensing, thus eliminating the need for an extra transistor per pixel as well. To achieve that, the fact that NC node is a high impedance node is exploited and the voltage change that comes from the addition of a small current applied at NC is sampled as shown in figure 4.1(a).

Since there is a large number of pixels connected to the same column, the voltage at the Drains of all the Mpixel transistors in this column must be relatively constant in order to avoid any I_{DS} current perturbations in each transistor of this column while a pixel is being programmed. These current perturbations originate from the short channel effects and the finite output impedance of the TFTs. Since a 2-TFT pixel circuit is mandatory, the design must include a voltage regulator that will be connected to all the Drains of the transistors, keeping all the drains in constant potential in order to avoid the perturbations.

4.1.2 The Circuit from the Analog Design Perspective And Early Design Endeavor

In order to fix a constant potential at the Drain of all the pixels a PMOS transistor in a diode connected configuration (M1) is used to hold a constant potential at about V_{TH} below the positive rail, as shown in figure 4.2. Switch SW1 isolates sampling capacitor Csample1 form the voltage at drain of the regulator transistor M1 during the programming stage.

This circuit operates in two stages. First SW1 is closed, and the voltage at both the inputs of GM1 is copied. Then SW1 is opened and a pixel is addressed and Idata flows pulling again node NC to a lower potential. The positive terminal of GM1

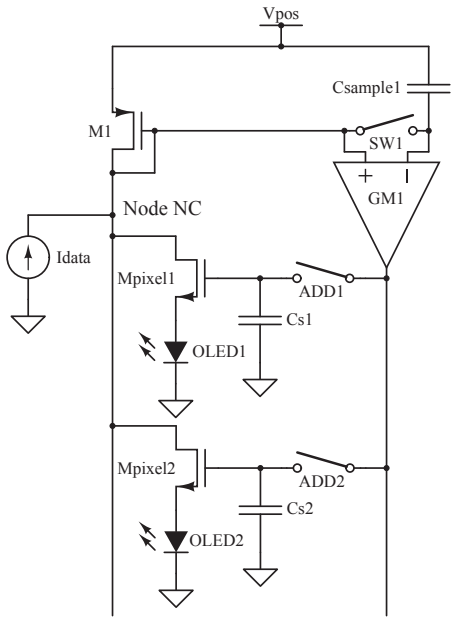


Figure 4.2: Schematic of the proposed feedback loop circuit.

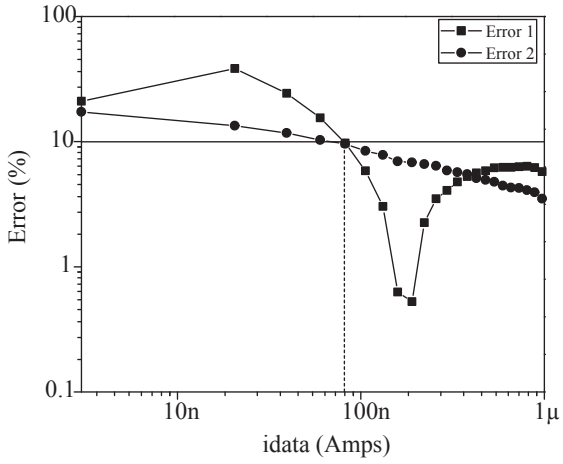


Figure 4.3: A graph containing the programming errors of currents ranging from 3nA to 1μA for 2 pixels with a x10 mobility variation.

is held at a constant voltage applied across Csample1. The negative input of GM1 therefore is drawn to a lower potential, consequently the output of the GM1 amplifier will move to a higher potential, setting the voltage at the gate of the addressed Mpixel transistor to the desired level.

The results presented in figure 4.3 are from the simulation of the circuit shown in figure 4.2. Pixel 2 has a mobility degradation of 90% from Pixel 1 and both can be programmed with a current of 80nA or above, while the error in their respective programming currents can be kept below 10%. The column current is assumed to be 5μA during the pixel programming stage. The driver was implemented with single crystal silicon transistors and simulated with the help of Cadence, using ONC5's technology with a minimum gate length of .6μm. The only downside of this implementation is that the more pixels are connected to the same column, the more the operating point of transistor M1 changes, therefore the voltage at the drains of all the pixel transistors does not remain constant for large Column Current (Icol) values.

Based on that observation, a prototype circuit was devised [22] that partially solves this problem. As shown in figure 4.4, a voltage regulator with two outputs is comprised of OA1 in conjunction with Msense and Msource. Msense and Msource's operation is separated by a switch MSW1. The output of the voltage regulator maintains a constant potential at node NC, keeping the operating point constant with variations of Icol. The sensing element is comprised of error amplifier OA2, that senses any changes in node NC and applies them to the gate of the addressed pixel.

4.2 Proposed Circuit Operation

The total column current carried by the power line is sensed. This takes place before the initialization of the pixel addressing period and the transistors Msw1 and Msw2 used as switches are turned on. Amplifier OA1 charges the gates of Msense and Msource forcing them into saturation and gate voltage of Msource is stored in

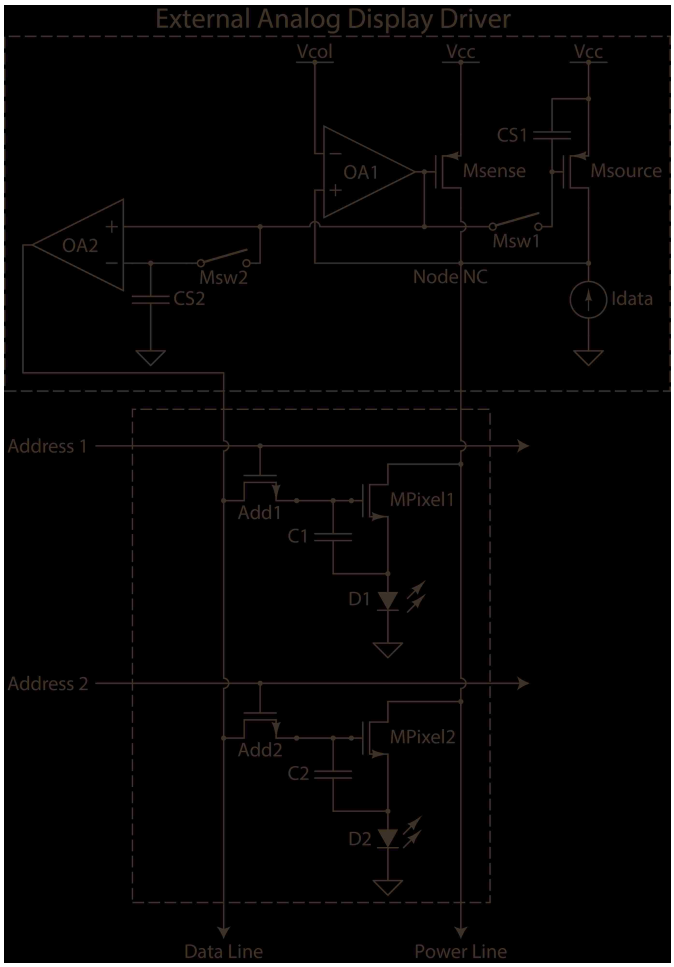


Figure 4.4: Circuit schematic of a specific driver implementation

capacitor CS1. Note that there is no data current input at this time. This procedure regulates the voltage at node NC, keeping it constant at the same potential as the negative terminal of OA1, which is connected to a reference voltage source named Vcol as shown in figure 4.4. At the same time this reference voltage is set across CS2 at the negative terminal of OA2. Then after the pixel is addressed the transistors Msw1 and Msw2 are turned off.

Transistor Msource is many times larger than transistor Msense, thus most of the column current is provided by Msource.

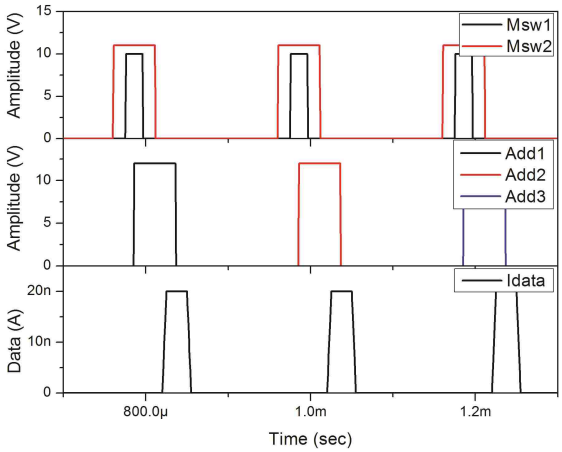


Figure 4.5: Switching scheme diagram

4.2.1 First Stage of operation Column Current Sensing

The pixel is addressed by turning on its address TFT (Add) during the period the Msw1 and Msw2 are on, so that C1 connected to the gate of MPixel1 is discharged (reset) through the output of OA2 as it will be explained in section 4.2.2. After Msw1 and Msw2 are turned off a data current Idata is introduced to the high impedance node NC which changes the potential of node NC and the output of OA1. This small change is sensed through OA2 which forces the pixel drive transistor (MPixel) to source the exact current supplied by Idata. When this occurs Node NC returns to its reference value (Vcol) and the output of OA2 stabilizes to a voltage that is required for the addressed pixel drive TFT to source the pixel current (Idata). The pixel addressed TFT is then turned-off and the required gate voltage for the drive TFT is stored in the pixels storage capacitor. For better visualization of the above switching scheme a switching diagram is presented in Figure 4.5.

Node NC, as seen in the circuit of figure 4.4, is a high impedance node. The current signal is multiplied by that impedance, and then sensed through OA1 that has a gain A_{OA_1}. That signal is applied to the inverting input of OA2 that has a

gain of A_{OA_2} to be applied in turn to the gate of the pixel transistor. Therefore the total gain of the loop would be

$$G_{LOOP1} = -Z_{NC} \cdot A_{OA_1} \cdot A_{OA_2} \tag{4.1}$$

$$V_{Mpixel_G} = G_{LOOP1} \cdot I_{DATA} \tag{4.2}$$

4.2.2 Loop implementation and Amplifier Design

The above description of the circuits operation signifies the importance of utilizing a stable amplifier design in the loops implementation to avoid unnecessary instability issues. Moreover, parasitics associated with the power and data lines, add extra poles in the feedback path. These parasitics are either a result from the physical size of those lines, or the amount of drive transistors attached to them. The extra poles prohibit the use of arbitrary large signal gains in the loops feedback amplifiers, thus limiting the sensitivity of the input to small signals. One simple solution to the above problem is to utilize as simple an amplifier design as possible. Such an amplifier must have a single ended output as well as the ability to drive significant loads. Moreover, due to the topology of the circuit since the output of OA1 is connected to the input of OA2 as shown in Figure 4.4, it is required that the differential pairs are NMOS and PMOS respectively.

Amplifier OA1 in conjunction with the Msense and Msource PMOS and any of the NMOS pixel driver transistors (Mpixeli in Figure 4.4) result in a low drop-out regulator topology as shown in Figure 4. This circuit sets Msource and Msense to track the total column current generated by the turned on pixels during the operation

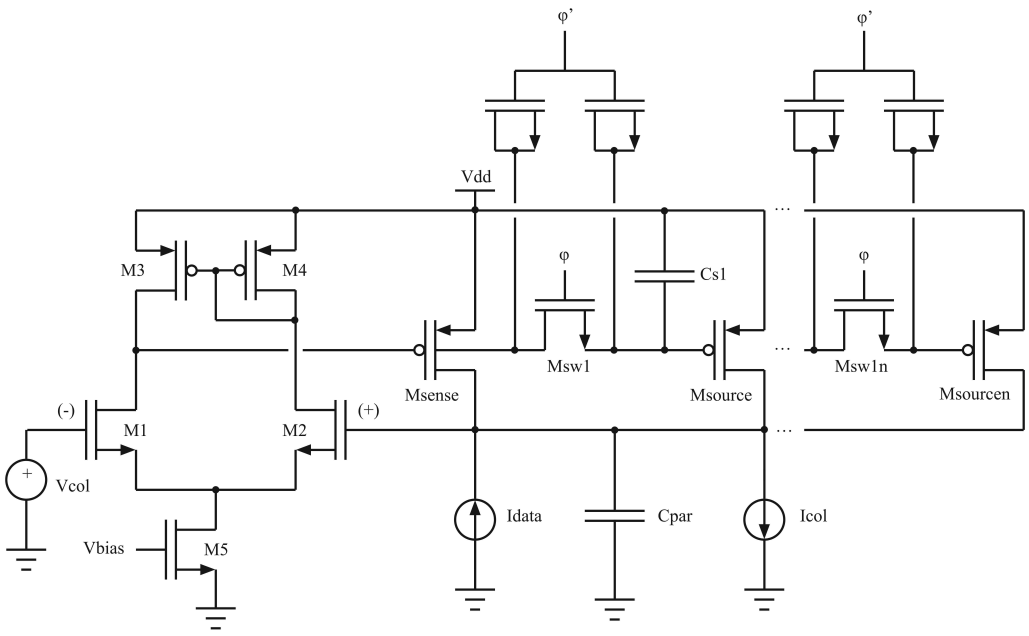


Figure 4.6: Low Drop-out Topology of OA1

cycle of OA1. In section 4.1.1 and figure 4.1(b), Isrc represents transistor Msource and Icol represents the total amount of pixels that are on during the addressing of the programmed pixel.

If the addition of extra output stages in the design of OA1 is avoided, the output of above low drop-out regulator is a high impedance node, and can be compensated and stabilized by the addition of a capacitor to ground. Since this node (NC in figure 4.4) is physically a line supplying power to all the pixels, a big parasitic capacitance is associated with it, the exact number of which is discussed in chapter 5. This capacitance is represented by Cpar in Figure 4.6.

The reader should note that the operating point of this amplifier will change the larger the total column current becomes tipping the differential pair and forcing the output of OA1 to a lower potential. If the output drops below the voltage provided by Vcol, transistor M1 will be in triode dramatically dropping the gain of OA1. This

can be avoided by changing the total width of the Msource transistor by adding multiple instances of Msource in parallel that can be independently controlled by different Msw1n switches that have the same phase as Msw1. The effective width of the Msource transistor modulated in this way, bringing the operating point of the topology back to the desired levels. It is with the help of this setup that a single pixel can be addressed and programmed while the total column current is supplied by a combination of Msource transistors that are on during the addressing step.

It should be also noted that at the end of the total column current sensing cycle and before the addressing step, switch Msw1 has to completely vacate its charge when switched off to avoid pumping it back to the gates of the Msourcen transistors. This extra charge into the gates in an ideal case where CS1 is a large capacitor has a minimal effect, but in the modern IC world where the capacitances used are as small as possible, it will create a small step in the gate voltage which multiplied by the transconductance of the effective Msource transistor will result in a current step. In turn, depending on how big the current step is the circuit could become unstable or inaccurate during the data-programming step. To help evacuate the charge and reduce the voltage step at the gate of Msource, two switching transistors with half the size of Msw1 short their Sources and Drains to the output of OA1 and the gate of Msource respectively, while both their gates if selected are supplied with a 180 degree offset clock of Msw1.

Amplifier OA2 for simplicity can also be a variation of the transconductance amplifier OA1 where the input differential pair is comprised of PMOS transistors and with the addition of a switch transistor connected at OA2's output that operates with the same phase as the Msw2 switch. This transistor facilitates the operation of the circuit during the pixel discharge phase, grounding the gate of the addressed pixel thus resetting it as is shown in Figure 4.7.

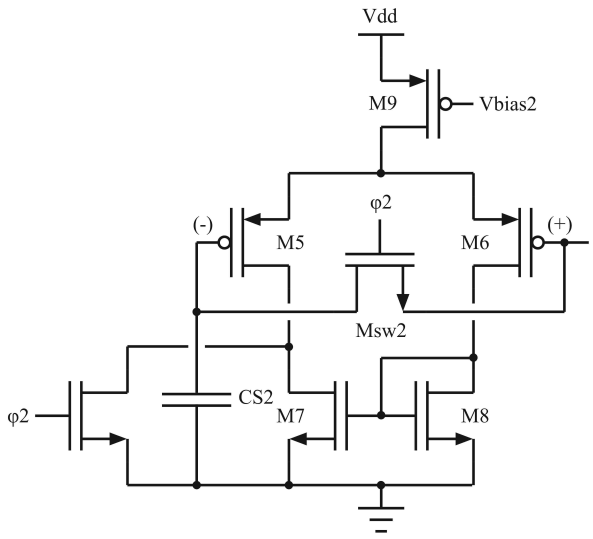


Figure 4.7: Topology of amplifier OA2

During the addressing step, when the data current is forced into node NC, there are two loops in operation, the loop between OA1 and Msense transistor and OA2 and Mpixel. Those loops are designed such that the transconductance of OA1 and Msource is many times smaller than OA2 therefore the second loop destabilizes by the small Idata current and finds equilibrium when Idata is carried by the addressed pixel. Finally the output of that system it is connected to an RC network of parasitics that will be calculated and explained in the next section.

4.3 Panel Line Parasitics

To calculate the parasitics in this paper, a process with three metal layers is referenced, where the dielectric thicknesses between metal 1 and metal 2 as well as metal 1 and substrate are 900nm and metal 3 and metal 2 is 1100nm. The insulating material between the poly-silicon gate layer, metal 1, metal 2 and metal 3 is Silicon Oxide as presented in Figure 6. The associated area normalized capacitances and

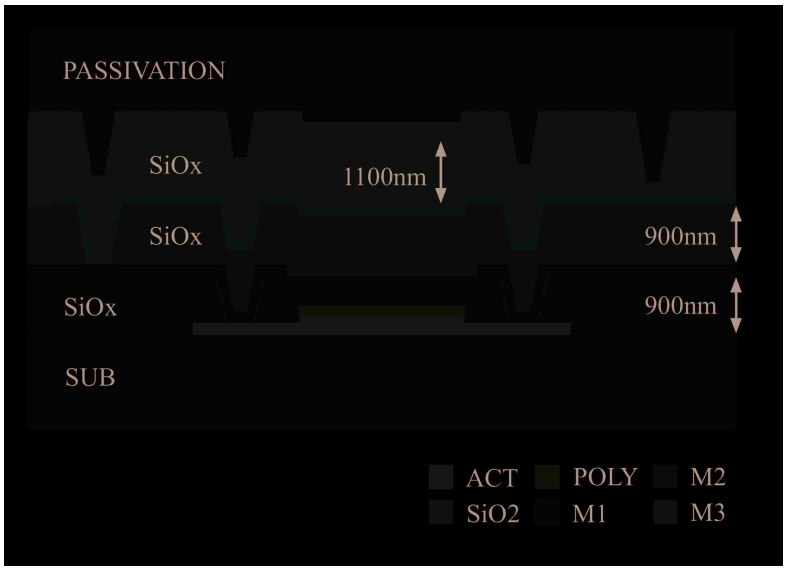


Figure 4.8: Cross-sectional view of referenced technology.

sheet resistances are presented in Tables 4.1 and 4.2.

Table 4.1: Metal Capacitances

Capacitor Electrodes	Capacitance [fF/μm^2]
M1 to Substrate / M1 to M2	0.04
M2 to Substrate	0.02
M3 to Substrate	0.012
M3 to M2	0.032
M3 to M1	0.018

Table 4.2: Sheet Resistances

Layer	Sheet Resistance [Ω/sq.]
M1	0.085
M2	0.085
M3	0.04
Poly	25

The physical dimensions of a modern 300ppi display backplane vary from 90mm to 100mm height and 50mm to 60mm width for portable devices, but in order to accurately calculate the parasitics allowing adequate room for design error in each feedback circuit, we are assuming a display that has 100mm height and 60mm width,

which has the largest 300ppi handheld-device backplane found today in the market. With these size assumptions it is immediately clear that the Power Line and the Data Line in the proposed circuit will be roughly 100mm each, since they vertically connect to each pixel in a column. Therefore for a 3m wide line, the total area of those wires over the substrate is 3x$10^5 \mu m^2$ which translates to a total base line capacitance of 3.6pF between the Power and Data Lines to ground.

The Power and the Data lines are placed on the third metal layer that has the smallest sheet resistance and the smallest capacitance to the substrate. Due to the topology of the pixel circuit these lines will only intersect the address lines placed horizontally using metal 2. Assuming there are 1000 pixels connected to a column, there are 3000 horizontal address lines (1000 RGB pixels) intersecting the Power and Data lines. For simplicity, if the entire wiring layout utilizes 3μm wide lines for the interconnections, then the total parasitic capacitance area is 27x103μm^2 per vertical line between M3 and M2. That amounts to 0.864pF of capacitance added to the base line parasitics between M3 and the substrate.

The fringe capacitance is calculated by using a 20% of the total capacitance connected to that node, which is about 0.892pF. That capacitance is modeled in parallel with the baseline capacitance, producing a total number for the parasitic capacitance of 5.357pF connected between the Power and Data lines respectively.

Figure 4.9 represents the schematic of the proposed circuit including the parasitics where the RC network on the right side of the figure represents the backplane parasitics evaluated prior to the design of the circuit. This RC network was instantiated twice in the final design layout, one time attached between node NC and the drain of the last pixel Mpixn and one time between the output of OA2 and the drain of the last address transistor Addn.

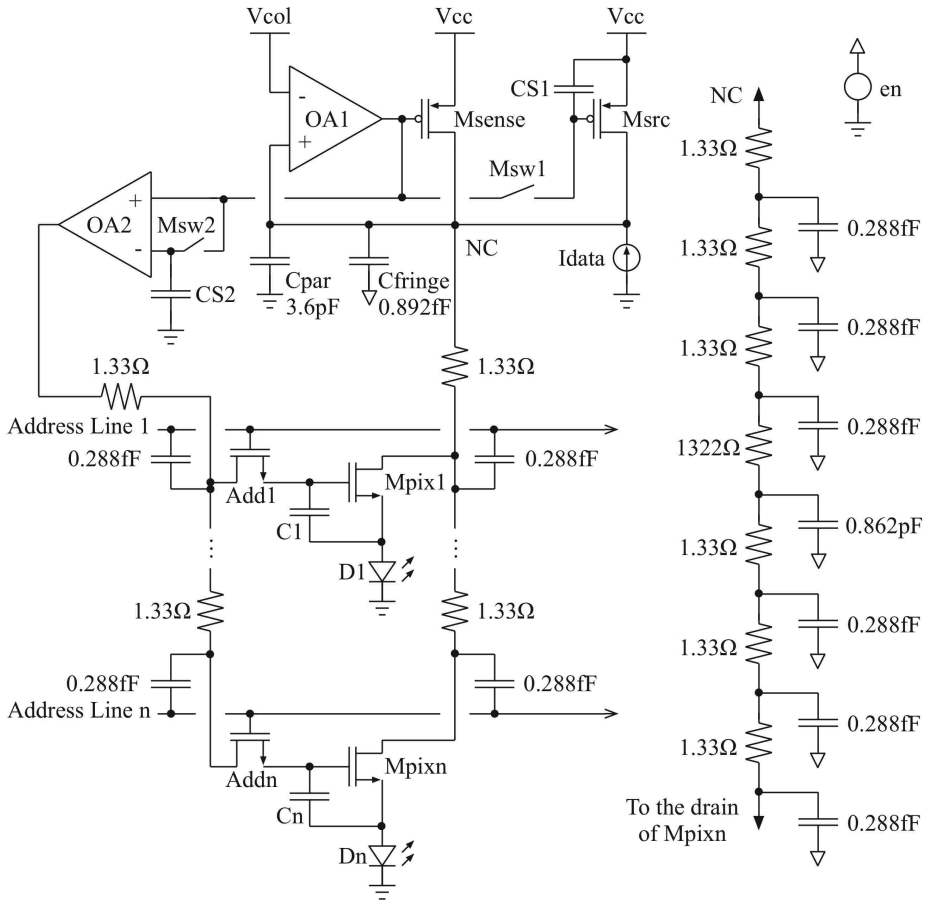


Figure 4.9: Left: Line parasitics of the back plane, Right: line parasitics simulation used in the fabricated IC.

It should be noted that these capacitances are not hard limits, but worst-case scenario estimations that are taken into account during the design procedure. Also important is the fact that not all of these capacitances are connected to ground, but rather to other lines, such as for example the address capacitance between the Power Line and the address lines. For simplicity we consider here that these capacitors are collectively connected not to the same ground, but to a separate one carrying switching noise as shown at the top right of Figure 4.9.

The total resistance of a 3m by 100mm wire on the third metal layer is 1.33k

based on the numbers presented in Table 4.2. The parasitics of the address lines can be easily calculated and included in the design using a similar procedure as described above. A generic shift register circuit is utilized to provide the necessary switching signals to the display and all the horizontal lines are loading the separate output buffers of each of the shift registers stages. Although there might be significant loading in these lines, their interference with the proposed circuit is coupled through the noisy ground as shown at the top right side of figure Figure 4.9 and further analysis of those parasitics falls outside of the scope of this work.

As seen by the total enumeration of the parasitics so far, the most important part in designing the proposed circuit is amplifier OA2. In order to evaluate the transient of this circuit three constraints are imposed in the design of amplifier OA, namely: (a) OA2 when paired with any of the addressed Mpixels has to have larger transconductance than OA1 paired with Msense as mentioned in **section 4**, (b) OA2 has to be able to adequately drive the RC network depicted in the right side of Figure 4.9, (c) must be able to detect small changes in its input voltage. Assuming that constraints (a) and (b) can be easily addressed by design, the only thing required is to evaluate how small of a voltage change there is at node NC and how fast that change happens during the pixel addressing time when Idata is applied to it.

The sensitivity of the output of the amplifier OA2 versus the Idata current change in node NC is given by:

$$V_{OA2} = I_{data} \cdot R_O \cdot \frac{g_{OA2}}{g_{sense} \cdot ro_{sense}} \cdot \left(\frac{g_{ds5} + g_{ds7}}{g_{ds5} \cdot g_{ds7}} \right) //Z_O \tag{4.3}$$

By adjusting the ratio $\frac{g_{OA2}}{g_{sense} \cdot ro_{sense}}$, the sensitivity of the loop to small currents

can be adjusted. Moreover, the series resistance of the power line is connected in series with the combination of the output impedances of Mpixel and Msense, and the total capacitance of the power line to the substrate is an order of magnitude larger than the overlap capacitance between the power line and the address lines. Therefore, as a first order approach, the overlap capacitance and the series resistance of the power line can be considered secondary effects to this calculation and taken into account later in the design process as margin of error. Just before Idata is applied, the impedance of NC is the parallel combination of Cpar and the combination of the output Mpixel and Msense impedances. In the TFT technology mentioned earlier, if all 1000 pixels are fully on at that time (which is rarely the case), the total worst-case output impedance Ro can be as low as 18kΩ. These parasitics give a maximum Idata pulsing frequency limit at 2.5 MHz, well outside 60 kHz, which is the frequency of operation for this circuit driving a column of 1000 pixels with a 60Hz refresh rate.

4.4 Simulation Results

Cadence was used to simulate the feedback architecture principle using CMOS devices provided by MOSIS using 1.5μm technology. The pixel was simulated using the following device parameters, threshold voltage 0.5 and 2.5V and mobility from 0.1 and 10cm2/Vs between Pixel 1 and Pixel 2, respectively.

Simulation results for a programming current of 20 nA, presented in the left graph of Fig. 4.10, show that the circuit charges the storage capacitor adequately fast because the output of OA2 is a low impedance node, thus any transient phenomena associated with the slow rise time of the voltage across the storage capacitor for low gray levels are eliminated [12].

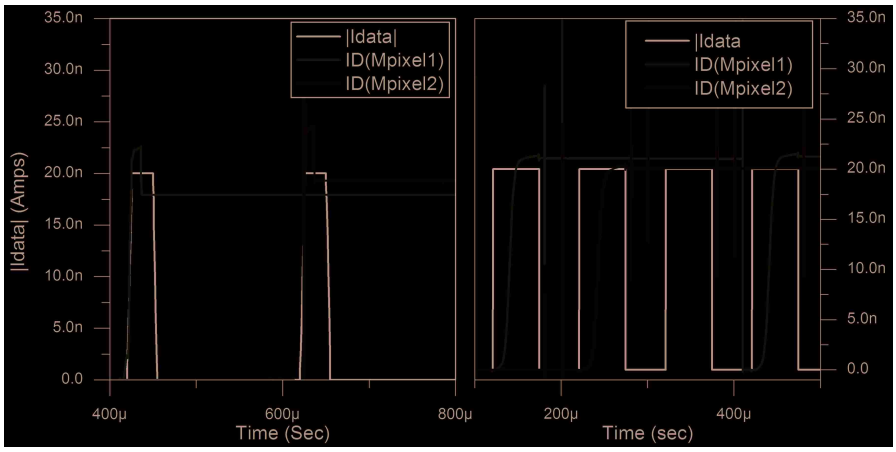


Figure 4.10: Transient simulation results for (a) 1.5μm, and (b) 0.18μm technologies.

Furthermore, the addressing time can be as small as 50μs for currents down to 20 nA as seen in the right graph of Fig. 4.10, in contrast with the study of Fruehauf et al. [11]. Using smaller geometry device technologies such as 0.18μm devices, for example, yields even better transient and programming accuracy results as shown in the simulation presented in the right graph of Fig. 4.10.

The reason that the results yield better performances in this case is that although our proposed approach with careful design can be applied independent of technology for the driver ICs, there are always hard limits inherent to the technologies used to implement those drivers. For older technologies, such as in the case of the AMIS 1.6, the minimum width in the layout of PMOS and NMOS devices is in the order of 45μm. This has significant importance to the charge pumped out of the switching transistors and into the holding capacitors, which in turn creates small bumps in the voltages of the gates those capacitors are connected to and that can translate directly to an error in the programmed pixel current as shown in the left graph of Fig. 4.10. Another hard limit is in the total gain of the amplifiers OA1 and OA2 utilized in the implementation of the loop, where the older the technology is the lower are the maximum transconductance and output impedances of the transistors

comprising those amplifiers resulting in compromise between accuracy and transient time versus gain and stability of the feedback loop implementation.

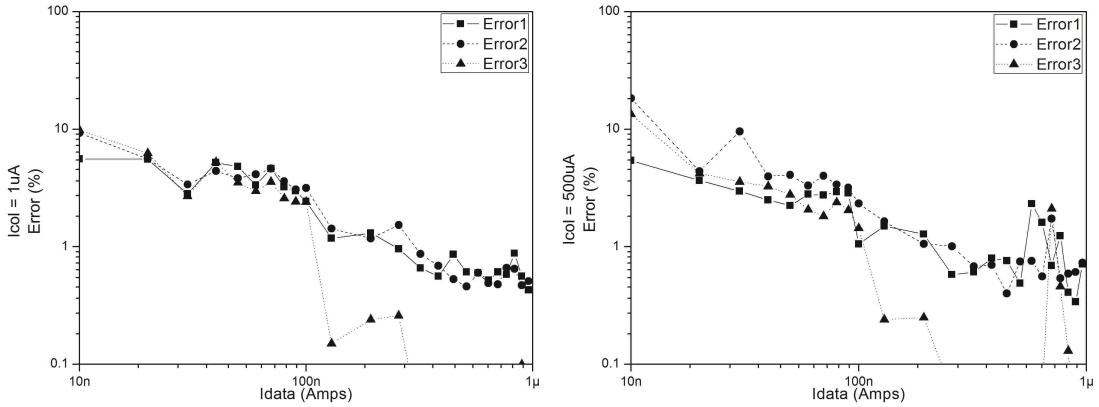
In addition to the driver circuit shown in Fig. 4.4, we have designed an alternate circuit and simulated it using device characteristics of a 0.5μm technology. Figure 4.11 presents the error of the current flowing through each pixel versus the actual input data current, for this other design. These three different pixels were implemented using the same technology, but have extreme variations in mobility emulated by a length variation in the driving transistor of 30μm while having the same width giving an emulated mobility variation of 96.77%.

The simulations where run with additional pixels connected to the power node NC, programmed with different voltages at the gates of their drive TFTs, so that the total column current would vary from 1μA up to 0.5 mA. Furthermore, realistic parasitic capacitors and resistors simulating the power lines and gate lines parasitics are included in our simulations. Errors 1, 2, and 3 were calculated with the $\frac{I_{data} - I_{pixel}}{I_{data}}$ formula, and they represent the error of the current programmed to those pixels. The error was around 10% for currents as low as 10 nA and was reduced at higher programming currents.

4.5 Experimental Results

4.5.1 High current measurements

In order to achieve controlled variations between pixels, an early experiment was performed in single crystal silicon, fabricated initially using the MOSIS 1.5μm technology. Early experimental data suggest that a current ranging from 4μA to 16μA,



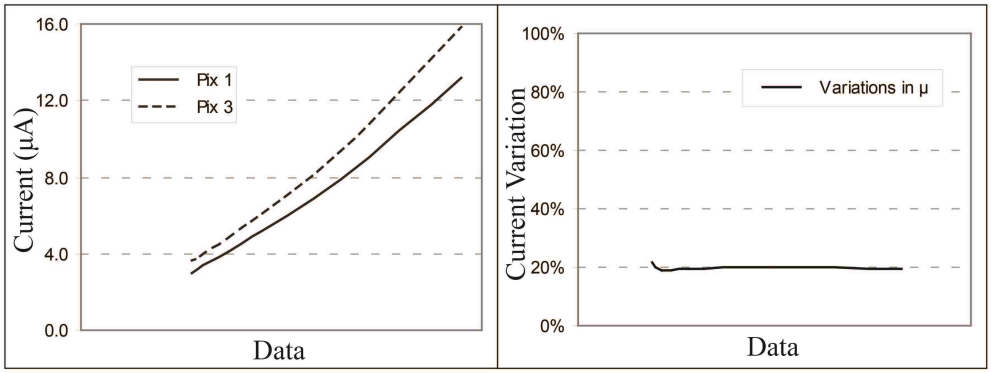
(a) 1μA Error (b) 0.5mA Error

Figure 4.11: Programming error, for another driver circuit implemented with 0.5μm technology, as a function of programming current for two different column current values, 1μA and 0.5mA.

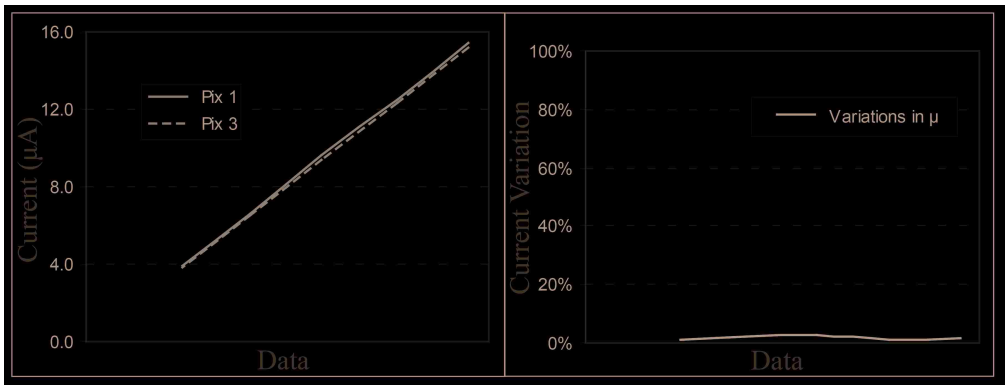
when programmed to a pixel has a variation below 10% even for great variations in mobility and threshold voltage. Pixels are implemented with predetermined characteristics that emulate mobility and threshold voltage variations.

For the mobility variations, the pixel drive transistors are single crystal silicon mosfets designed with two different channel lengths of 25 and 30μm while having the same width giving an emulated mobility variation of around 20%. For the threshold voltage variations, the pixel drive transistor connects to an external voltage at the source. Its initial threshold voltage is about 0.57V, and the external voltage source is set to around 0.15V thus having a threshold voltage variation of around 25%. Therefore, the 3 pixel iterations in the fabricated circuit are as follows:

- Pixel 1: original pixel (Vth= 0.57V, L=30μm)
- Pixel 2: 25% Increase in Vth (Vth = 0.72V, L=30μm)
- Pixel 3: 20% Increase in μ (Vth = 0.57V, L=25μm).



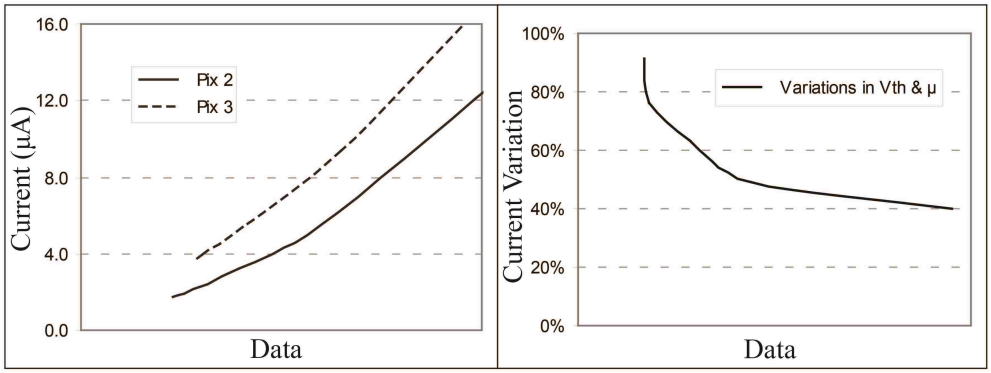
(a)



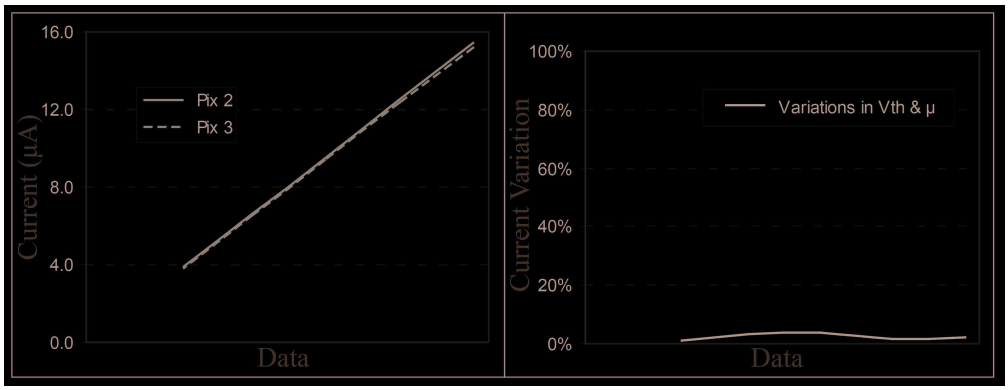
(b)

Figure 4.12: Experimental comparison for high currents of Pixel 1 and Pixel 3 when programmed with the conventional 2T1C approach: (a) Left: drive TFT current and Right: drive TFT current uniformity; and when programmed with the new drive architecture: (b) Left: drive TFT current and Right: drive TFT current uniformity. Total column current is 0.5 mA.

Figure 4.12 shows a comparison between the experimentally measured programming currents of Pixel 1 and Pixel 3 when programmed with the conventional 2T1C approach: (a) Left: drive TFT current and (a) Right: drive TFT current uniformity; and when programmed with the new drive architecture, (b) Left: drive TFT current and (b) Right: drive TFT current uniformity. Figure 4.12 focuses solely on variations in mobility but not threshold voltage. Figure 4.13 shows a comparison between the experimentally measured programming currents of Pixel 2 and Pixel 3 when programmed with the conventional 2T1C approach: (a) Left: drive TFT current and



(a)



(b)

Figure 4.13: Experimental comparison for high currents of Pixel 2 and Pixel 3 when programmed with the conventional 2T1C approach: (a) Left: drive TFT current and Right: drive TFT current uniformity; and when programmed with the new drive architecture: (b) Left: drive TFT current and Right: drive TFT current uniformity. Total column current is 0.5 mA.

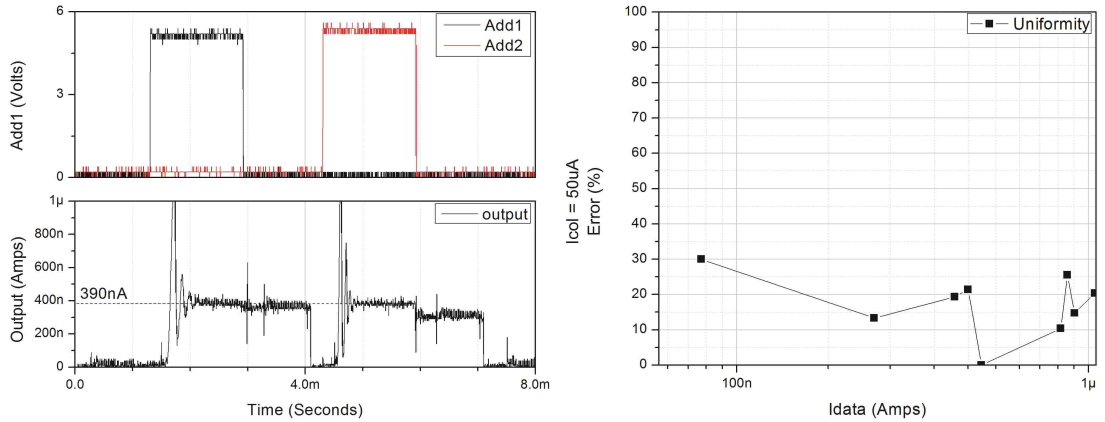
Right: drive TFT current uniformity; and when programmed with the new drive architecture, (b) Left: drive TFT current and Right: drive TFTcurrent uniformity. Figure 4.13 focuses on both mobility and threshold voltage. The experimental setup for both Figs. 4.12 and 4.13 used a total column current of 0.5 mA. The experimental setup limited the accuracy of these early measurements to high programming current values. In our latest design, we have implemented an integrated testing circuitry that enabled us to extend the range of measurements by about two orders of magnitude as it is shown in the next section.

Even though these tests were conducted using currents that vary from 4 to 16μA for this version of the proposed circuit, the choice of operating currents is somewhat irrelevant because the proposed circuit can operate equally well at lower current levels as it is shown in the next section. Moreover, these currents could be potentially found in modern OLED display applications, which utilize pulsing of the LEDs at higher currents such as TV monitors [23], where the active LED area is many times larger than that of portable applications. This current pulsing is utilized for various reasons among which is to achieve peak efficiency of the LED current-to-light conversion and minimize the stress exerted in the circuitry around the display that is forced to carry constant currents.

4.5.2 Low Current Measurements

The results presented in Figs. 4.12 and 4.13 are for high programming currents for the prototype preliminary design. The inherent capacitances in this type of circuits might be prohibitive to the extraction of measurements in the lower current range without perturbing the system; we were able, however, to extract measurements of pixel-to-pixel current uniformity for currents lower by about two orders of magnitude using the exmperimental setup procedure as it is explained in chapter 6, figure 6.4. Similarly to our early design, our new driver design implements pixel-to-pixel mobility variations using variations in the channel length of the driver transistor. Specifically, we fabricated pixels with lengths of L=1μm for Pixel 1 and L=10μm for Pixel 2 in order to achieve an effective mobility variation of 90% between them.

Programming data currents down to 80 nA have experimentally been verified in those pixels. An example of the operation of this circuit is presented in Fig. 4.14(a) where in the top graph, the addressing pulses for Pixel 1 and Pixel 2 are shown,



(a) (b)

Figure 4.14: (a) A sample output measurement of the pixel current using the current mirror setup implemented for this circuit and (b) pixel current uniformity between pixels with mobility variation of 90%. The total column current is 50μA.

and the data current through the pixel is monitored at the same time in the bottom graph. These data were extracted during a programming cycle of a data current of 390 nA. More detailed measured data information is found in Fig. 4.14(b) where the Pixel 1 to Pixel 2 uniformity is presented for various data currents down to 80 nA. The experimentally determined error shown in Fig. 4.14(b) is higher than the simulated error shown in Fig. 4.11. We have attributed this difference to switching noise associated with our IC design as well as experimental setup. Such noise might not be present in an actual AMOLED display if it is driven by a back plane made of TFTs, and thus, we expect that the uniformity of the programming will be similar to the simulated one in an AMOLED display driven with the new architecture. This will presented in more detail in chapter 5.

In Fig. 4.14(a), the small step in the output current measurement of Pixel 2 is the switching error associated with all the 2-TFT 1-capacitor circuits due to charge pumped to the storage capacitor from the gate of the address transistor switch (e.g., Add1 and C1, Add2 and C2, etc. in Fig. 2) during Add2 pulses negative edge. There

are several switching techniques able to compensate the stepping error in this type of circuits that could also be implemented as a part of the external circuitry in the border of the display backplane.

Although so far, these results look promising, the current range for mobile devices is down to the single or double digit nano-Ampere levels spanning three orders of magnitude (for example 1 - 1000 nA). Even more cumbersome are the display monitors used as TVs or computer screens with a range that spans four orders of magnitude, up to the micro-Ampere levels (for example 1 - 10000 nA) due to the larger devices implemented in the display requiring more current to elevate brightness compensating for the increased distance the observer's eyes are placed from the monitor's surface.

Initially the calculation of the feedback loop surmised that the capacitance parasitics of this circuit is large enough to stabilize the loop for large currents. As described in [24], This circuit is using a series of transistors Msrc connected in parallel to depending on the magnitude of the total column current in order to provide the necessary current signal to accommodate Icol.

One of the main reasons the programming range is restricted by the output, is due to overdriving the column. If the column carries a lot or current due to the multitude of pixels connected to it, this forces the input Amplifier OA2 to saturate as a result the gain is dropped dramatically since the input does not have enough headroom to sense the Idata applied at the critical node NC. Moreover, another look on the basic principle reveals that node NC has to constantly have as high an impedance as possible in order to sense minute changes in current and the total. The addition of the extra Msrc transistors however drops the total impedance amount of the output lower the more pixels get programmed and the larger the total column

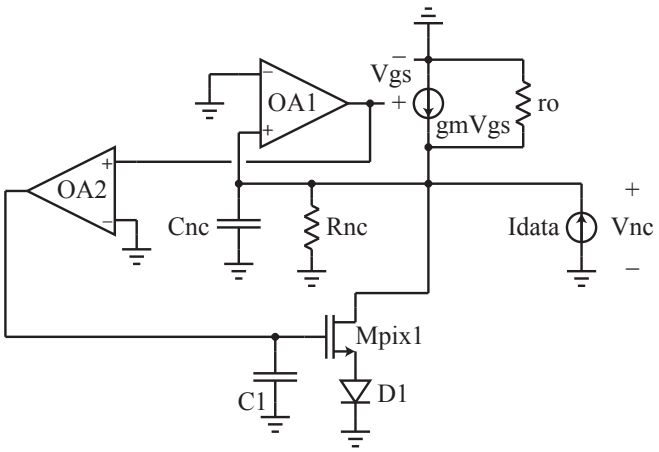


Figure 4.15: The AC equivalent of the circuit presented in 4.4.

current becomes. That restricts the designer of this circuit to utilize only the gain of OA2 as a sole means of setting the lower and the higher boundaries, thus limiting the total current operating range of this circuit, limiting the total number of pixels it can program.

Equations 4.4 and 4.5 are the node equations describing the total system's response and they are derived utilizing the simplest AC equivalent presented in figure 4.15, where opamps OA1 and OA2 are considered to be ideal without a roll-off at high frequencies with a gain of A1 and A2 respectively, while assuming $C_{nc}$is the total capacitance of the power line and R_{nc} is the total impedance of the pixels in parallel with the total impedance of the Msrc transistors.

$$\left(sC_{nc} + \frac{1}{R_{nc}} + \frac{1}{ro} + A1\right) V_{nc} + I_{pix} = -I_{data} \tag{4.4}$$

$$-\frac{gm_{pix}\ A2\ A1}{sC1} + I_{pix} = 0 \tag{4.5}$$

It is assumed that the voltage V_{gs} at the gate of the M_{sense} transistor is described

by $V_{gs} = A1 \cdot V_{nc}$. The resulting system's matrix is presented in equation 4.6.

$$A = \begin{pmatrix} sC_{nc} + \dfrac{1}{R_{nc}} + \dfrac{1}{ro} + A1 & 1 \\ -\dfrac{gm_{pix}\ A2\ A1}{sC1} & 1 \end{pmatrix} \tag{4.6}$$

And by using the input output equation 4.7

$$y = (\,0\ \ 1\,) \cdot A^{-1} \cdot \begin{pmatrix} V_{nc} \\ I_{pix} \end{pmatrix} \tag{4.7}$$

the system's transfer function is derived and expressed by equation 4.8

$$I_{pixel} = \frac{\omega_0^2}{s^2 + \dfrac{\omega_0}{Q}s + \omega_0^2} \cdot I_{data} \tag{4.8}$$

where

$$\omega_0^2 = \frac{A1\ A2\ gm_{pix}}{C1\ C_{nc}} \tag{4.9}$$

$$Q = \frac{C_{nc}\ R_{nc}\ ro\sqrt{\dfrac{A1\ A2\ gm_{pix}}{C1\ C_{nc}}}}{A1\ Rnc\ ro + Rnc + ro}. \tag{4.10}$$

$$Re\{p_1, p_2\} = \frac{\omega_0}{2\ Q} \tag{4.11}$$

Q is found from equation 4.10 and it is a function of the square root of the product of A1 and A2. This is particularly important because normally opamps have a very large gain, making the quantity $\sqrt{A1\ A2}$, therefore the Q, very large. It is known form the literature [25] that a circuit having the above transfer function the real

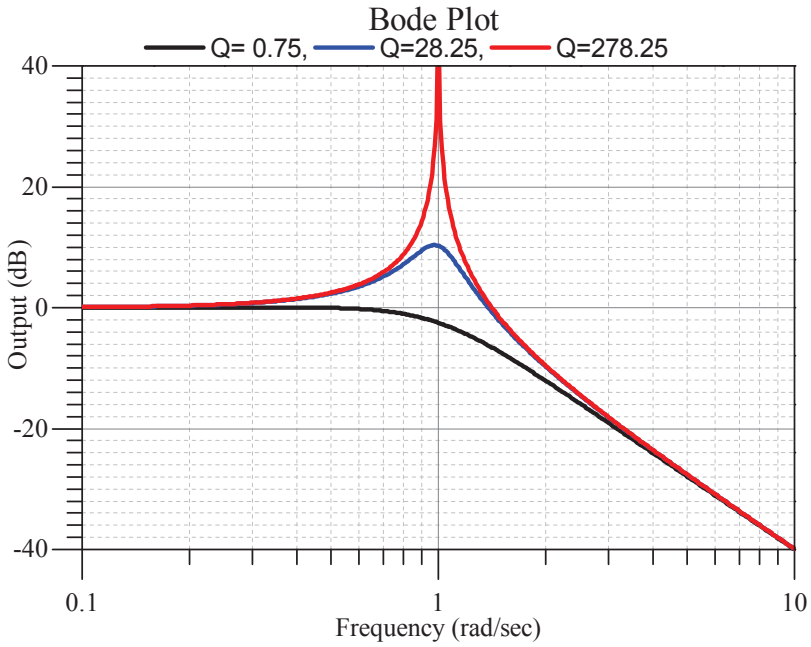


Figure 4.16: Bode Plot of equation 4.8 for different Q values.

part of its poles is described by equation 4.11. Specifically since the real part of the poles is an inverse function of the Q factor as shown in equation 4.11, the larger the Q the closer the poles are to the Imaginary axis, as a result a lot of ringing is observed at the output and as it has been explained earlier it is very important for the transient of this kind of feedback systems to have their poles placed very close to the $x = \pm j \cdot m$ lines to avoid over-damping and sluggish response times when responding to step input signals [1].

Utilizing a slightly older technology and "chocking" the gain of OA2 the results presented in figure 4.12 and 4.13 are easily achieved, however when the display data driver is integrated with newer technology transistors having higher output impedances, as a result having amplifiers with larger gains, it becomes harder to control the Q value while increasing the dynamic range of the circuit. Figure 4.17 depicts the target input data current (green line) vs the pixel Current (red line) and the oscillations seem to die out, due to limitations in the simulator's minimum time

step, whereas it has been confirmed experimentally that such circuits fail to operate altogether.

In our example [21], for the circuit in figure 4.9, the data gathered with a version of this loop where its gain was kept at a minimum value. In reality, to cover the four orders of magnitude in the dynamic range, the loop's gain has to be larger to increase the loop's sensitivity in minute changes of input current. But as shown in equation 4.1, the signal propagates through both OA1 and OA2 amplifiers making the loop unstable due to the large gain.

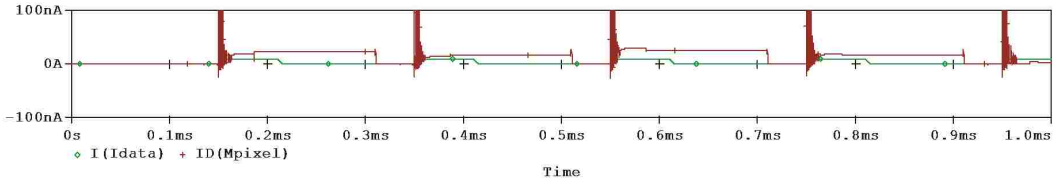


Figure 4.17: Simulation ran with Cadence.

It should be pointed out that for the range of interest, the target pixel's current (red line) oscillates wildly, settling to different values creating systematic non-uniformity in the target programming current. The effect becomes even more pronounced using an even smaller time-step in the simulations.

In Chapter 5, the part of my work that aimed to develop a new and improved current feedback circuit driver to drive displays is presented. This new driver will have the ability to program pixels with currents as low as 1nA while the total current carried by the column could be in the range of mili-Amperes, covering the entire range of devices from TVs down to cellphones and watches.

Chapter 5

Current Feedback Compensation circuit and Method for 2T1C AMOLED Displays

5.1 Introduction

IN the following pages a novel improved circuit is presented and analyzed. An expansion of the analysis on the basic principle as found in section 4.1.1 is presented in section 5.2, while in section 5.3 the new proposed circuit's control loop is explained with the help of an ideal equivalent. The parasitics in such a display backplane panel are listed and included in the analysis of the topology and the steps for designing the circuit are described in the same section. Data for a mobile 4.7 inch display application for both the simulated and fabricated chip are included in section 5.6 and concluding remarks are included in section 5.9.

5.2 Circuit Implementation

All 2T-1C pixel circuits within a LED TFT backplane require a minimum of three lines ensuring the operation of the circuit, namely the address (or scan) line, the data line and the power line, where ground is not taken into consideration as it is normally a metal layer deposited across the entire backplane called the "ground plane" layer. In an effort to compensate the threshold voltage and mobility some techniques utilize extra scan and/or sensing lines combined with an external driver to correct for the pixel driver degeneration [10, 16, 18], as mentioned in the introductory section 3.2, with a minimum of only one extra sensing line found in [11]. Although in most cases where the resolution is limited to 350ppi that technique can be effective, the extra lines add extra parasitics and restricts the maximum display resolution.

Previously, section 4.1.1 demonstrated how the power line can be utilized to both supply the total current carried by the pixels of that line and to sense the current that is programmed to the addressed pixel [26, 27]. This is achieved by utilizing an external driver topology where the power node is converted to a high impedance node attached to a sensing amplifier that modulates the data pulse amplitude during the pixel address time, shown in figure 4.1(b). The voltage at the Drains of all the Mpixel transistors in this column must be kept to a relatively constant potential however, in order to avoid any I_{DS} current perturbations in each transistor attached to the same power node while a pixel is being programmed (node NC in figure 4.1(b)).

These current perturbations, originating from the short channel effects and the finite output impedance of the TFTs, are greatly magnified due to the large number of pixels connected to the same column. Since 2-TFT pixel circuit is used, the external driver first must include a voltage regulator that operates in the time slots created between two consecutive pixel addressing cycles. This regulator fixes the

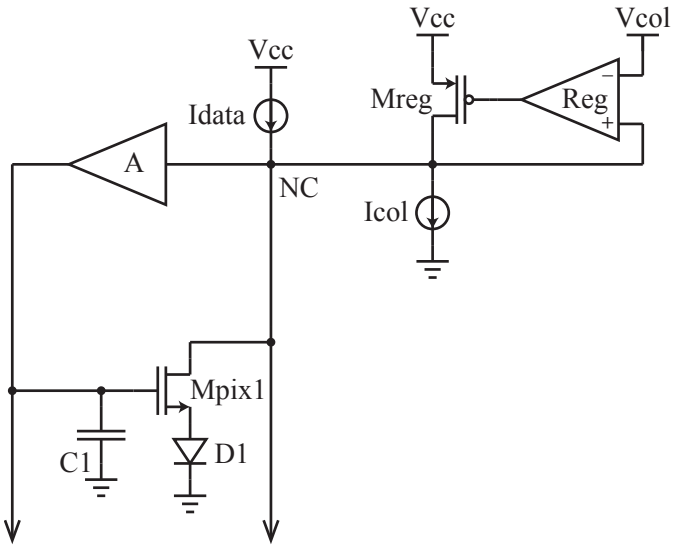


Figure 5.1: Regulated high impedance power node.

potential to a constant at the drains of the pixel driving transistors and eliminates these perturbations while retaining the high impedance configuration mandatory for sensing small data currents. The low dropout regulating configuration is attached to the power node of the column (NC), as presented in figure 5.1, where the drain of a transistor with large (W/L) ratio supplies the total column current Icol, dropping the total small signal impedance at that node by as small an amount as possible while fixing its potential to the value of Vcol.

The second programming loop in this driver must include an amplifier that is attached to the gates of the pixel driving transistors (Amplifier A in Fig. 5.1). It is this loop that must destabilize during the introduction of the I_{data} current to node NC, forcing the addressed pixel to carry the excess current in order for the circuit to find equilibrium. Normally, in all display drivers the data to be programmed to a pixel is a digital multi-bit voltage signal. A simple high-output impedance transconductance Digital to Analog Converter (DAC) can be utilized to convert the provided signal to an I_{data} current, however, describing such a circuit falls outside the scope of this paper and a simple external current source will be used providing

the appropriate signals.

Previously, at an early implementation of this basic principle two loops were utilized, a regulator fixing a constant potential at NC supplying the total column current [27] and a sensing loop attached to the gates of all the pixels depicted in figure 5.2. The previously proposed circuit operates in two steps: the programming step and the regulating step. During the regulating step between the addressing of two consecutive pixels, Msw1 and Msw2 are shorted and the previously programmed pixels are modeled by the Icol current source. During the programming step, Msw1 is open and Mreg transistor is set to supply the Icol current while Msw2 is open as well storing the previous potential value at the gate of Mreg to capacitor Cst1. I_{data} is applied to node NC destabilizing the loop which finds equilibrium only when the current through the addressed pixel is equal to I_{data}. In this circuit the input of the sensing loop was attached to the gate of the regulator transistor Mreg, in order to increase sensitivity at lower current levels. However, this limits the dynamic range of the circuit's pixel current programming ability to two orders of magnitude. The trade-off in the previously described topology is between sensitivity and stability since the larger the gain has to be in order to sense smaller signals at the critical node NC the more unstable the circuit becomes. Moreover the I_{data} signal is multiplied by the impedances of Mreg in parallel with all the output pixel transistors' impedances at NC creating a small voltage signal. That small voltage signal is then gained by both the regulating and sensing amplifiers before it is translated to a current by the addressed pixel and added to node NC completing the loop as shown in figure 5.2.

This approach utilizes the regulating amplifier Reg during both the regulating and the sensing step which increases the complexity of the circuit design, since the designer has to carefully pick the ratio of the regulating and sense amplifiers' gains to avoid oscillations. Since the circuit must have the ability to detect lower I_{data}

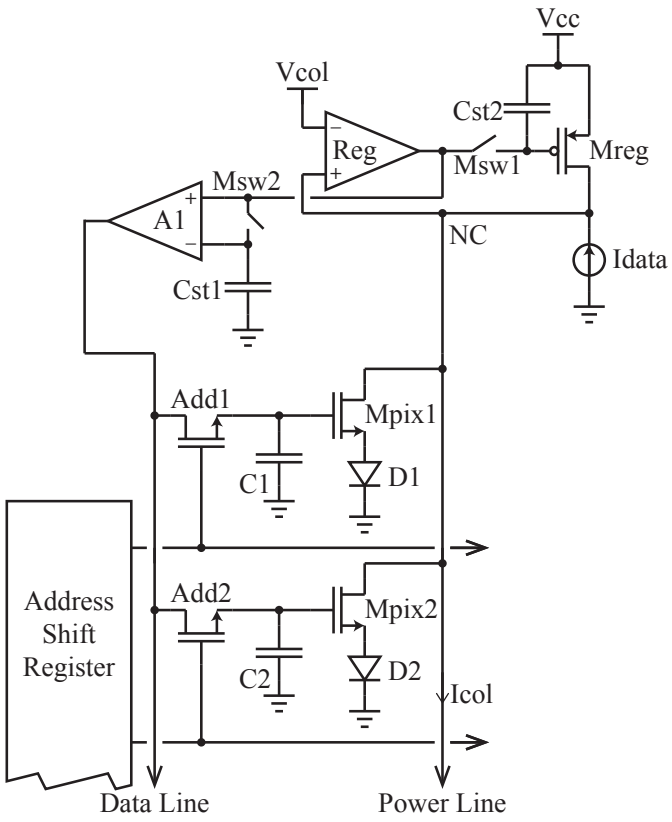


Figure 5.2: Earlier implementation of the basic principle.

currents, limiting the gain of the regulating amplifier is standard practice which restricts the dynamic range of the total column current supplied at the power node by the drain of Mreg. Moreover, the bigger the total column current gets, the more the operating point during the regulating step deviates from that during the sensing step for the Reg amplifier. Thus, when Reg amplifier is switched to operate between the two loops, it has to instantaneously change operating points which might render the circuit unstable.

In order to avoid the aforementioned problem a new circuit is proposed which

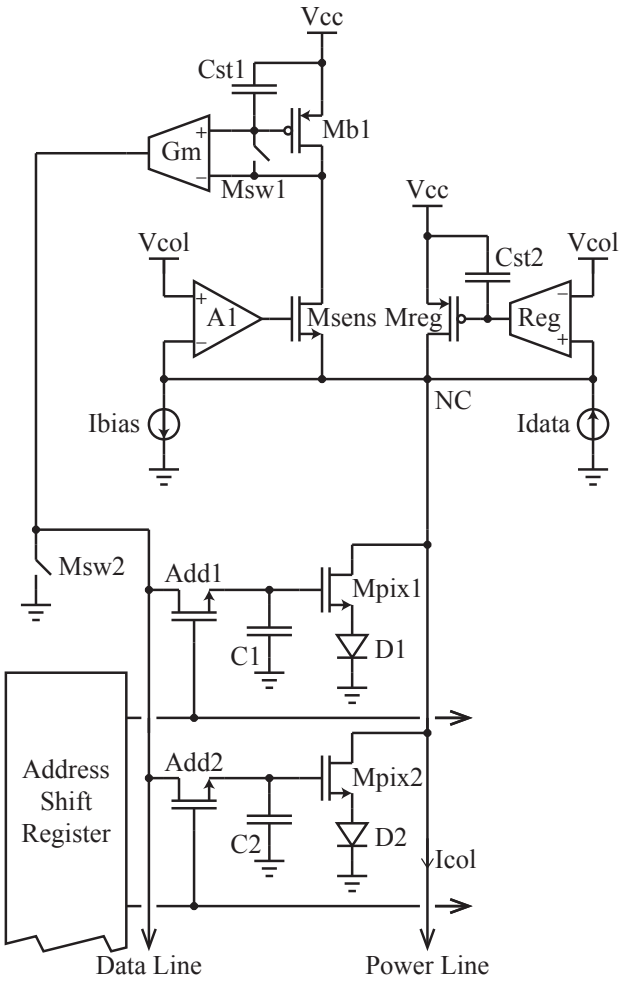


Figure 5.3: The improved circuit implementation.

disassociates the two loops by introducing another regulator loop as shown in figure 5.3.

In this new circuit topology, the Reg amplifier is deactivated during the pixel addressing time while A1 amplifier is activated and transistor Msens acts as a buffer, passing the I_{data} current while maintaining a constant potential Vcol at node NC. During the regulating step, amplifier A1 is deactivated and amplifier Reg is activated to regulate the potential at NC while at the same time, current source I_{data} is no longer active making the current through Mreg equal to the exact sum of the previous

Icol current plus the drain current of the previously addressed pixel, which in this case is the previous I_{data}. Note that A1 amplifier is not affected by the change in the operating point of Reg amplifier since those two are decoupled allowing the regulating circuit to be independently designed to accommodate the large changes in the total column current. Moreover, Cst2 storage capacitor can be designed to have a large enough value to keep the loop involving Mreg stable when the circuit transitions from the regulating step to the programming step, switching amplifier Reg off. The exact value of capacitor Cst2 and its effect on the design of the circuit, in conjunction with a more complicated technique utilized to hold Msense's operating point near its nominal value is described in section 5.2.

The A1 and Reg amplifiers are controlled by a single current source in series with a selector switch sourcing the current either from A1 or from source amplifiers accordingly and it is controlled by a an external voltage signal. When the selector signal is low, A1 amplifier is activated and when it is high, Reg amplifier is activated. Moreover, there exists a switch attached to the output of Gm amplifier, namely Msw2 as shown in figure 5.3 and it is used to reset the addressed pixel's storage capacitor in the beginning of the addressing period.

To describe the exact operation of the circuit first we assume that it has already cycled through the startup procedure and some of the pixels in the column are already programmed with a data current (modeled by Icol current source). We are also assuming that the circuit is in equilibrium and that it is about to address a random pixel (N-th pixel). Note that Msw1 is supplied with a square wave that has the same frequency and Duty Ratio as the I_{data} pulses, but 180 degrees offset in its phase as depicted in figure 5.4. Since the programming step with the regulating step are non-overlapping presented also in figure 5.4, the operation takes place as per the following. These steps (named as: Regulating, Balancing and Programming):

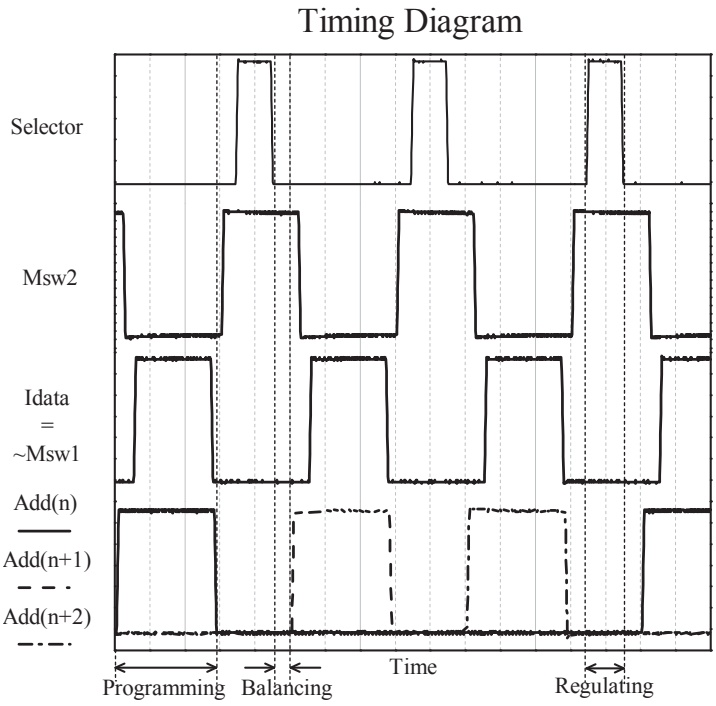


Figure 5.4: Timing Diagram.

(a) Regulating step

The selector switch, after receiving a high signal, deactivates the sensing amplifier and activates the regulating amplifier respectively, as shown on the right side of figure 5.5. The total current applied to node NC at this moment is Icol plus the previously programmed current I_{data}. Amplifier Reg changes the potential at the gate of transistor Mreg, forcing it to provide the total current $Icol + Idata_{(n-1)}$, keeping the critical node NC at the same potential as Vcol. The voltage at the gate of Mreg is kept in capacitor Cst2, which does not discharge when Reg amplifier is deactivated since it is connected to a high impedance output of a differential amplifier, which floats to any voltage value when that amplifier is turned off.

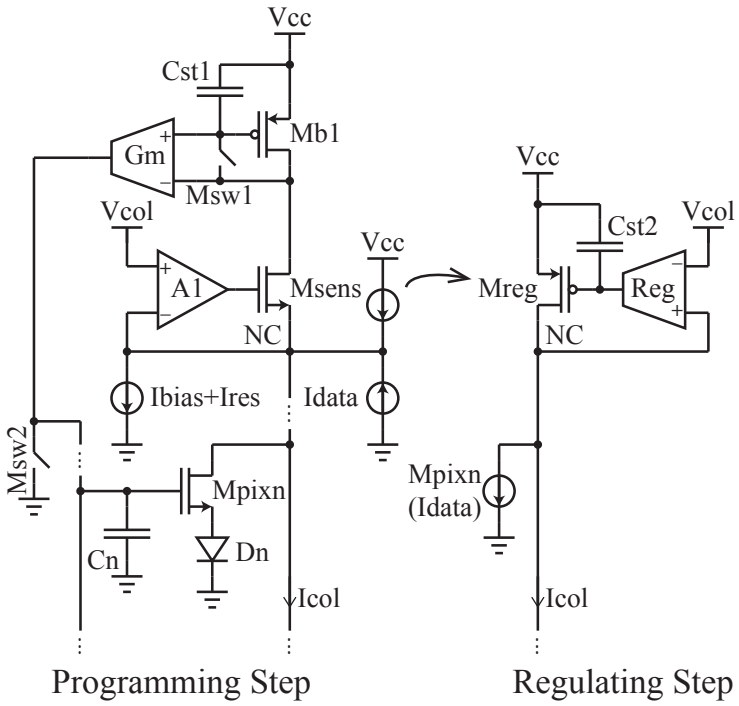


Figure 5.5: Equivalent loops isolated by switching. Left: programming loop and Right: Regulating loop.

(b) Balancing step

Setting the selector switch to low, Reg amplifier is deactivated and the equivalent circuit topology is shown on the left side of figure 5.5. The Mreg transistor remains in saturation due to the capacitor Cst2 which retains the charge when Reg amplifier switches off. Although the Mreg transistor is set to carry the entire column current, it is not perfectly matched to Icol, therefore it is safe to assume that a residue current of unknown polarity is coming out of node NC. This current is shown on the left side of figure 5.5 as being superimposed to the bias current source having a new effective value of Ibias+Ires. When switching from Reg amplifier to sens amplifier, a tiny amount of charge could be pumped into or evacuated out of capacitor Cst2, which creates a voltage step that is responsible for the residual current at node NC. The capacitor is chosen carefully so that the maximum absolute value of this residue

current is always smaller than Ibias by a fixed amount, thus when the selector switch activates the sens amplifier, the programming step's topology can absorb that current difference by finding a new stable point of operation.

(c) Programming step

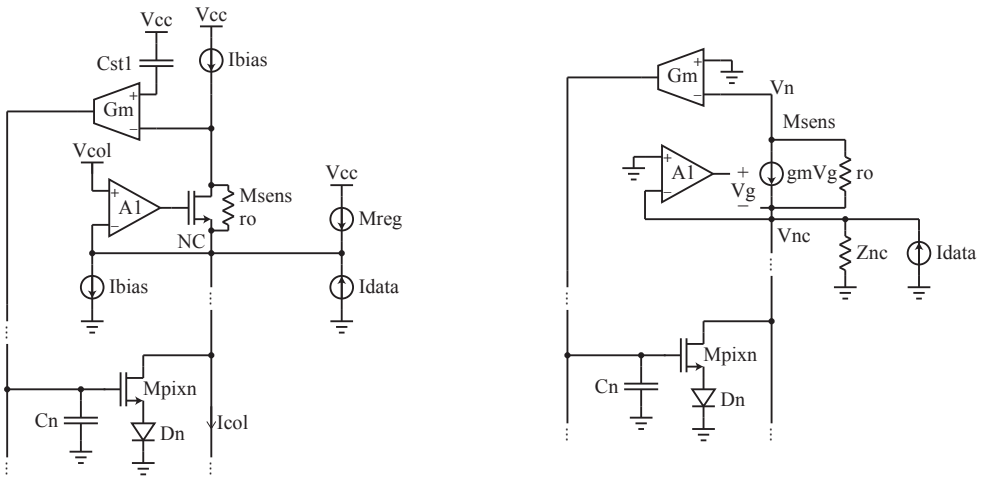
The N-th pixel's address switch is shorted providing a path to ground since Msw2 has remained on from the previous step. During this time the voltage at the drain of Msens is sampled and stored in capacitor Cst1. After an adequate and fixed amount of time, Msw2 is deactivated and the target I_{data} current is applied to NC while at the same time Msw1 is deactivated holding the previously stored voltage. Msens transistor allows the data current pass through and the loop created between Gm and the addressed pixel is destabilized, finding equilibrium only when the addressed pixel carries I_{data}. After the circuit finds equilibrium the address and the I_{data} pulses are no longer applied and Msw2 and Msw1 are activated once more. The residual I_{data} current programmed into the addressed pixel changes the voltage at the drain of Msens transistor and does not affect the potential at node NC which remains at the same value as Vcol during the entire operation of the programming step.

The above described procedure is repeated for every pixel in the column. Note that the balancing step does not require extra switching to take place but it rather happens during the time the selector switch deactivates and before the address switch is activated. In general it is a subsequence of the programming step and it is presented separately to facilitate the explanation of this circuit.

5.3 Designing The Circuit

Different information content for a given display may require different areas of the display to exhibit different illumination intensity. Therefore the displays' operating voltages may vary based on their sizes as well as their back-plane technologies and the materials used for the LEDs. For example, a portable device such as a smart phone or tablet may target low power consumption which directly translates to lower back-plane operating voltages and currents, smaller display sizes as well as organic LED materials to increase the efficiency for low to medium range illumination intensities. A TV or a desktop computer monitor on the other hand, require larger display area and greater intensity of illumination therefore a back-plane compatible with larger operating voltages may be required. Moreover, recent advances on wearable electronics push the boundary even further by requiring portable displays that consume the least amount of power to offer high brightness and require back-planes which require efficient LED materials that operate at low voltages but with the ability to provide large currents for short periods of time.

Based on the previous constrains, two versions of the proposed circuit are presented in this section: a high voltage operating at 12V and a low voltage operating at voltages as low as 5V. The high voltage circuit is aimed for applications where large voltages and currents are required due to higher intensity demands and larger LED areas, while the low voltage circuit is aimed for portable applications consuming less power and require lower voltages in their power supply lines. Despite the small difference in the topology and the operating points of the circuits, the basic idea behind the proposed designs is the same for both of them.



(a) Ideal addressing loop.

(b) AC analysis of the ideal loop.

Figure 5.6: Ideal Loop

5.3.1 Loop Description

Specifically, as it is described in section 5.2, during the programming step of the circuit's operation, just after the addressed pixel has been reset and just before the moment I_{data} is applied to NC, the total column current will be perfectly matched and supplied by the Mreg transistor as shown in figure 5.6(a), as it would ideally be represented by a current source. Also node NC would have a fixed potential level equal to Vcol while the drain of Msens would be at the same potential as the negative input terminal of Gm. The Ibias current sources cancel out each other and the circuit is in equilibrium, assuming the operating point of Gm is set in such a way that its quiescent output voltage is not large enough to turn on Mpixn transistor.

To facilitate the description of the loop, an AC equivalent is presented in figure 5.6(b), where all the DC current sources are ignored and the DC voltage sources are treated as AC ground. The AC potential at node NC is named V_{nc} and the AC potential at the negative input terminal of the Gm amplifier is named V_n. The

amplifiers A1 and Gm are considered to be ideal, having gains of A1 and Gm respectively. Note that an impdeance Z_{nc} is connected at NC, mimicking all the parasitics attached to that node resulting from the parallel combination of the finite output impedance of all the Mpix transistors, which for this ideal case it is assumed to be a simple resistor Rnc.

5.3.2 Ideal Loop Transfer Function Calculation

Assuming

$$V_g = -V_{nc}(A1 + 1)$$

the node voltage equations based on figure 5.6(b) are:

$$\begin{aligned}
\left[\frac{1}{R_{nc}} + \frac{1}{ro} - gm(A1+1)\right] V_{nc} - \frac{1}{ro} V_n - I_{pix} &= -I_{data} \\
\left[-\frac{1}{ro} + gm(A1+1)\right] V_{nc} + \frac{1}{ro} V_n &= 0 \\
Gm \cdot gm_{pix} \cdot \frac{1}{sC_n} V_n - I_{pix} &= 0.
\end{aligned}$$

The nodal system's matrix resulting from those equations is:

$$A = \begin{pmatrix}
\frac{1}{R_{nc}} + \frac{1}{ro} - gm(A1+1) & -\frac{1}{ro} & -1 \\
-\frac{1}{ro} + gm(A1+1) & \frac{1}{ro} & 0 \\
0 & \frac{Gm \cdot gm_{pix}}{sC_n} & -1
\end{pmatrix} \tag{5.1}$$

where the total system equation is

$$A \cdot \begin{pmatrix} V_{nc} \\ V_n \\ I_{pix} \end{pmatrix} = \begin{pmatrix} -I_{data} \\ 0 \\ 0 \end{pmatrix}$$

having an input-output equation of the form

$$y = (\,0\ 0\ 1\,) \cdot \begin{pmatrix} V_{nc} \\ V_n \\ I_{pix} \end{pmatrix}.$$

The solution of the circuit is then:

$$y = (\,0\ 0\ 1\,) \cdot A^{-1} \cdot \begin{pmatrix} -I_{data} \\ 0 \\ 0 \end{pmatrix} \tag{5.2}$$

Where $y = I_{pix}$.

Perturbations at the drain of Msense ensure that the gate of Mpixn rises when I_{data} is applied. The transfer function from I_{data} to I_{pix} is presented in equation 5.3:

$$I_{pix} = \quad -\frac{\frac{1}{\tau}}{s + \frac{1}{\tau}} \cdot I_{data}. \tag{5.3}$$

Where:

$$\tau = \frac{C_n}{Gm \cdot gm_{pix}[1 + gm \cdot ro \cdot (1 + A1)]R_{nc}}.$$

If the data current is a unit step with an amplitude of 1, the output in the time domain is described by:

$$I_{pix}(t) = -I_{data}\left[1 - exp\left(-\frac{t}{\tau}\right)\right]. \tag{5.4}$$

Since the system is first order, it is described by the exponential approach function and because it only has one pole, amplifiers A1 and Gm for the ideal case could be designed with arbitrarily large gains to minimize the transient time needed to charge the pixel's capacitor Cn.

5.3.3 Non-Ideal Loop Transfer Function Calculation

The order of the loop is increased due to a complex impedance present in the circuit that was deliberately ignored in the previous analysis, which adds a pole to the transfer function. Specifically, using most the assumptions made in beginning of this section unaltered, plus assuming that Mreg and all the pixel transistors have finite output impedance as well as non-zero drain-to-source capacitance, the pole is introduced to the loop due to the capacitor attached in the critical node nc. A resistance R is also connected from the drain of Msens to AC ground, which is related to the finite output impedance of transistor Mb1 shown at the top of figure 5.3. The amplifiers, for the purpose of this analysis, are still considered ideal, having gains of A1 and Gm respectively. This new AC equivalent circuit is presented in figure 5.7.

Using the first assumption of section 5.3.2 in combination with the nodal equations extracted from figure 5.6(b) where the complex impedance Z_{nc} is replaced with a resistor R_{nc} in parallel with a capacitor C_{nc} the nodal incidence matrix is:

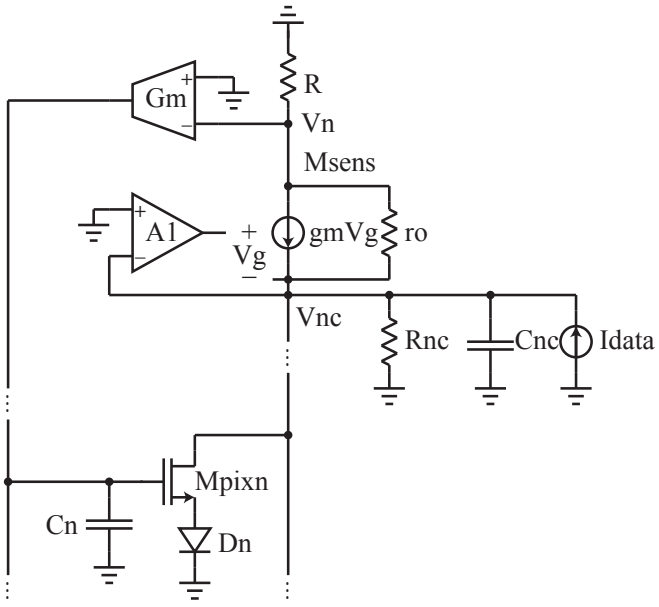


Figure 5.7: AC analysis of the non-ideal loop.

$$A = \begin{pmatrix} \frac{1}{R_{nc}} + sC_{nc} + \frac{1}{ro} - gm(A1+1) & -\frac{1}{ro} & -1 \\ -\frac{1}{ro} + gm(A1+1) & \frac{1}{ro} + \frac{1}{R} & 0 \\ 0 & \frac{Gm \cdot gm_{pix}}{sC_n} & -1 \end{pmatrix} \tag{5.5}$$

The solution of this circuit is then found by combining equations 5.2 and 5.5.

With the help of the nodal incidence matrix for this circuit, the transfer function is:

$$\frac{I_{pix}}{I_{data}} = \frac{\frac{1}{C_{nc}} \cdot \omega_\beta \cdot g_\alpha}{s^2 + s\frac{1}{C_{nc}}\left[\frac{1}{R_{nc}} - g_\alpha\right] + \frac{1}{C_{nc}} \cdot \omega_\beta \cdot g_\alpha} \tag{5.6}$$

where

$$g_\alpha = \frac{gm(A1+1) - \dfrac{1}{ro}}{\dfrac{ro+R}{ro}}$$

and

$$\omega_\beta = \frac{Gm \cdot gm_{pix} \cdot R}{C_n}.$$

Note that if $R \longrightarrow \infty$ and $C_{nc} \longrightarrow 0$ G_{pix} becomes

$$G_{pix} = \frac{Gm \cdot gm_{pix}}{C_n}$$

and the transfer function becomes the same as in the ideal case described by equation 5.3.

5.4 Technology Interface and Parasitics

Modern display back-planes utilize Thin-Film Transistors (TFTs), implemented with various technologies spanning from Silicon such as Low Temperature Poly-Silicon (LTPS), to various conductive oxides such as Indium-Gallium Zinc-oxide (IGZO). Depending on the application, those backplanes have different sizes ranging from several tens of millimeters for applications such as watches, smart phones and tablets, to over a meter for large TV displays. An estimation of the parasitics associated with these technologies is presented in this section, which will further facilitate interfacing the proposed circuit to these technologies, by carefully taking into account during the design process most of these parasitics resulting from the layout of the interfaced back-plane.

Most of the aforementioned TFT technologies have multiple metal layers for the

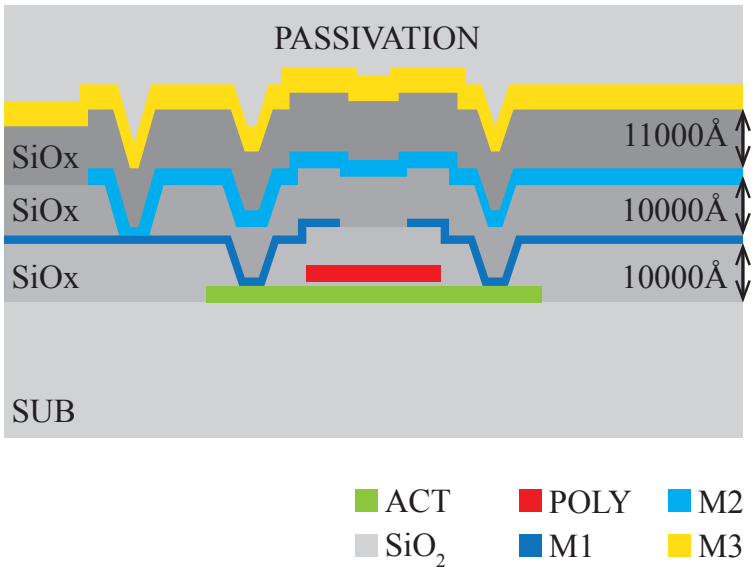


Figure 5.8: Crossection of a typical three metal technology node.

Table 5.1: Specs of a typical 3 metal technology node

	$t_{ox}[A]$	C'_{ox} [fF/um^2]
M1 to substrate	10000	0.0345
M1 to M2	10000	0.0345
M2 to substrate	21000	0.0164
M3 to substrate	31000	0.0111
M3 to M2	11000	0.0314
M3 to M1	21000	0.0164

interconnects but here a technology node with only three metal layers is utilized for simplicity to implement the backplane [24] as shown in figure 5.8. Typical Metal to Metal dielectric thicknesses range from 1μm between Metal 1 and Metal 2, up to 1.1μ between Metal 2 and Metal 3. Another assumption is that the insulating material used between the metal layers is mostly Silicon dioxide that has a dielectric constant of $\epsilon_{SiOx} = 0.0345fF/\mu m$. Table 5.1 lists the dielectric distances as well as the per unit area normalized capacitance between the metal layers.

The panel sizes for modern applications range from 4.7 inches for mobile devices

Table 5.2: Various Panel Sizes and Associated Parasitics

Diagonal [in]	4.7	5.5	9.7	45	55	65
Aspect Ratio	16:9	16:9	16:9	16:9	16:9	16:9
Height [cm]	5.85	6.85	12.08	56.04	68.49	80.94
Width [cm]	10.40	12.18	21.47	99.62	121.76	143.90
Pixel Density (ppi)	350 - 500	350 - 500	350 - 500	34 - 100	34 - 85	34 - 70
Vertical Pixel Resolution	1434 - 2048	1678 - 2397	2959 - 4227	750 - 2206	917 - 2292	1083 - 2231
Vertical RGB pixel resolution equivalent (x3)	4301 - 6145	5033 - 7190	8877 - 12681	2250 - 6619	2750 - 6876	3250 - 6692
Line Capacitance [pF]	3.48	4.07	7.18	6.24	76.29	90.16
Fringe (20%) [pF]	0.70	0.81	1.44	1.25	15.26	18.03
Power to Data Line Overlap Capacitance [pF]	1.22 - 1.74	1.42 - 2.03	2.51 - 3.58	7.06 - 20.78	8.63 - 21.58	10.20 - 21.01
Total Line Capacitance [pF]	5.39 - 5.91	6.30 - 6.91	11.12 - 12.19	14.55 - 28.27	100.18 - 113.13	118.40 - 129.20

such as smart phones and tablets, up to 65 inches for modern TVs. Table 5.2 utilizes the widely used 16:9 aspect ratio, to calculate the panel's exact dimensions. Note that the panels having smaller diagonal dimensions used in cell phones and tablets, are normally driven in parallel from the short edge of the panel designated in Table 5.2 as Height, while the larger displays such as TV monitors are driven in parallel from the long edge designated in Table 5.2 as Width. This is a general rule of thumb because border size limitations in the portable devices provide fewer options for the driver's chip placement. Moreover for large displays this is a significant advantage, since less pixels have to be addressed by the driver, making the data transmission rates smaller. Therefore the width is used for the address line density calculations in portable displays and the height for the larger TV monitors. To calculate the vertical address line densities we are assuming 350ppi to 500ppi resolutions for the portable devices which are slightly higher than the modern portable displays, as well as 34ppi to 100ppi bordering at the higher end of 4k TV displays. We are also assuming that all the power lines and the data lines are 3μm wide for all portable devices and 10μm wide for all the larger TV monitors.

Typically since a 2T1C setup is utilized, the vertical lines are the power lines attached to node NC and the data lines attached to the output of the Gm amplifier, while the horizontal lines are attached to the outputs of the shift register as shown in figure 5.3. The horizontal lines are provided with the address switching signals, but most of the time they are at low potential, therefore, we can assume that the parasitic capacitances between Power Line and the address lines as well as Data Line and address lines are all grounded from the side of the data lines [24]. Since the Power and Data lines have the same width while they are both placed on the same metal layer, they are physically similar to each other thus the parasitics will be the same for both of them. Finally in the line capacitance calculation there is an

additional 20% is conservatively added due to fringe capacitance. The bottom row in table 5.2 lists the range of the parasitic capacitances based on the Pixel densities of different panel sizes for different applications.

Table 5.3: Line Resistivity

Layer	Resistivity [mΩ/sq.]
M1	85
M2	85
M3	40

It should be mentioned that these are not hard limits, rather estimated values of the parasitic capacitance's range that will facilitate the calculation of the loop's pole placement in order to fine-tune the design of the proposed circuit to achieve the best possible performance. Another important fact which should not be omitted is that those Total Line Capacitances numbers should not be represented as a single lumped capacitor model but rather as a resistive-capacitive (RC) transmission line.

Based on the values included in table 5.2 for a display panel having a 4.7 inch diagonal with 500ppi density (modern phones and tablets) and table 5.3 for a generic TFT technology, the panel's transmission lines can be modeled as shown in the left side of figure 5.9. Ideally all 2048 pixels are to be tested interfacing with the proposed circuit, but in order to present the design and analysis of the circuit's topology the column can be modeled using single lumped capacitors as shown on the right of figure 5.9. The individual line resistors and capacitors before pixels 1 and 2048 are three orders of magnitude smaller compared to the line's total resistance and capacitance, therefore they can be omitted for simplicity from the analysis. Moreover with the help of this calculation it is found that Rnc and Cnc in figure 5.7 are 1385Ω and 5.914pF respectively.

Quantities R and ro are impedances related to the inverse of the output con-

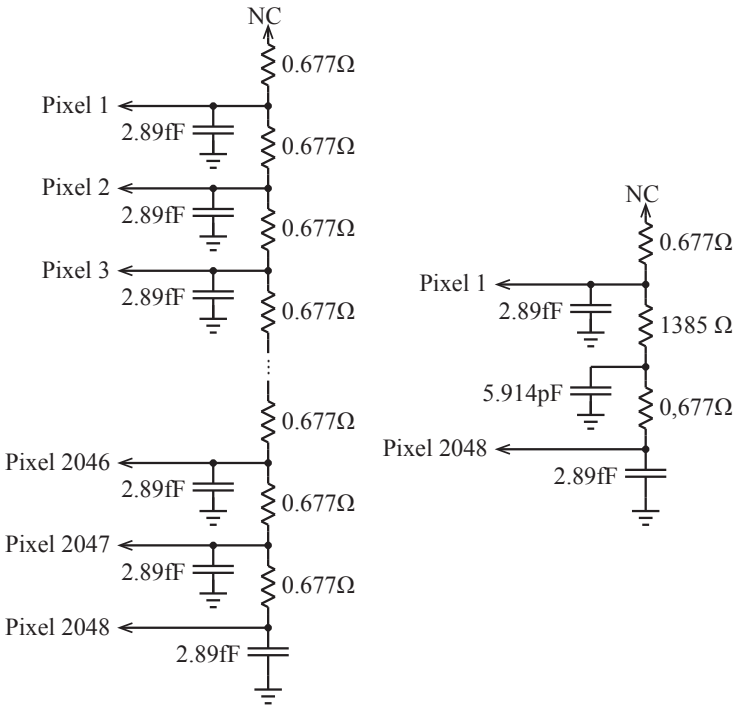


Figure 5.9: Typical transmission line representation.

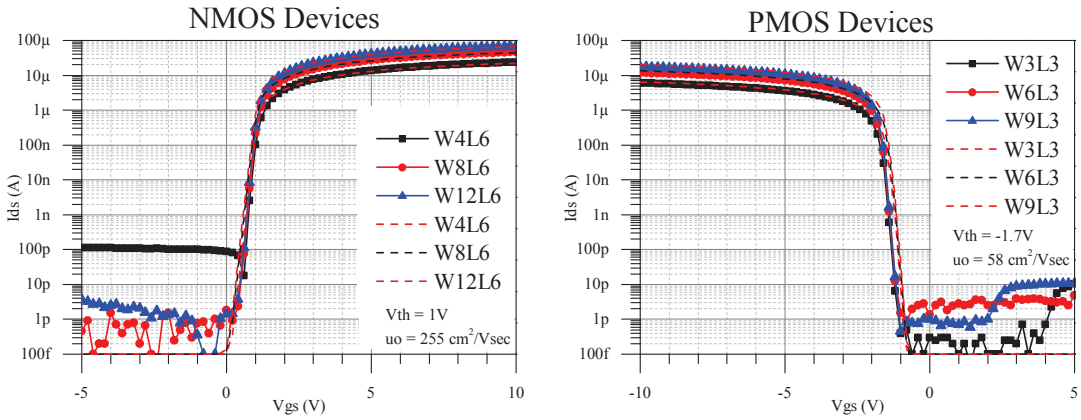
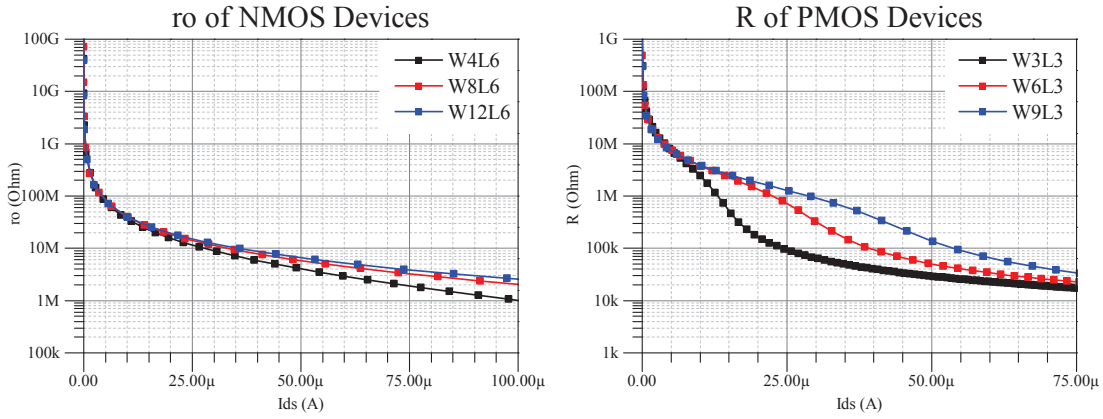


Figure 5.10: Transfer Characteristics of NMOS and PMOS devices.

ductance (gds quantity) of transistors Mb1 and Msens respectively, based on their appropriate bias conditions calculated from figure 5.3. The device characteristics of a single crystal technology node utilized in this design are presented in figure 5.10, where a minimum high voltage device length of 3μm is mandatory, the NMOS de-



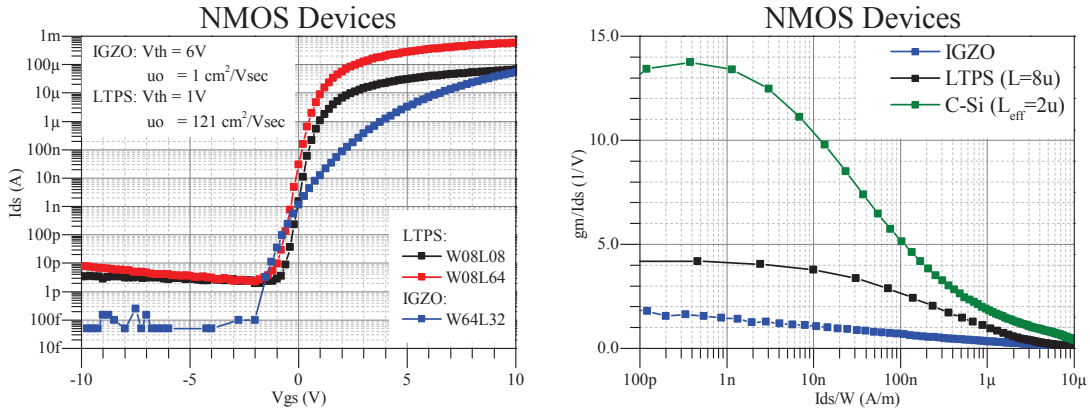
(a) (b)

Figure 5.11: R and ro quantities.

vices have a threshold voltage of $V_{th} = 1V$ and a mobility of $\mu_n = 255\ cm^2/V \cdot sec$, while the PMOS devices have a threshold voltage of $V_{th} = -1.7V$ and a mobility of $\mu_n = 58\ cm^2/V \cdot sec$.

The current used for the calculation of R and ro is Ibias+Ires, which is produced during the balancing step, as mentioned in section 5.2. Assuming that the current for the maximum brightness is 1μA then for 2048 pixels the absolute maximum current in the column Icol would be 2.048mA. Moreover, if Ibias is 10μA, while the maximum current variation of the residue current is $\pm$0.25% of the total column current which for this case ranges between $\pm$5μA, therefore the quantity Ibias+Ires varies between [5μA,15μA]. With the help of figure 5.11 we can derive that R ranges from 500kΩ to 9MΩ, while ro from 25MΩ to 80MΩ.

As a final step before the pole placement calculations, the transconductance of the pixel drive transistor is calculated. This quantity is dependent on the backplane technology and Figure 5.12(a) depicts transfer characteristics of the aforementioned LTPS [28] and IGZO [29] transistors with a Vds voltage of 8V, while figure 5.12(b) is a plot of the transconductance efficiency (also known as gm/Id) versus the current



(a) (b)

Figure 5.12: Calculation of the pixel transconductance gm_{pix}.

these transistors are biased. From 5.12(b) and for Data currents in the range of 1nA to 1μA, it is found that LTPS has a transconductance of 4.2nS to 1μS and IGZO 1.4nS to 0.4μS.

Table 5.4: Quantities used for Pole placement evaluation

Cnc	5.914pF
Rnc	1385kΩ
Ibias+Ires	[5μA, 15μA]
ro	[80MΩ, 25MΩ]
R	[500kΩ, 9MΩ]
IGZO gm_{pix}	[1.4nS, 0.4μS]
LTPS gm_{pix}	[4.2nS, 1.0μS]

Table 5.4 combines all the previously calculated values concluding the example of interfacing the driver with a 500ppi 4.7inch display panel. These values are used next to describe to the reader the pole placement calculation and the analytic evaluation of the proposed circuit's feedback loop. It is important to mention that these values will vary even more, based on the technology the driver is implemented and the technologies with which the driver is interfacing. However, as it is shown in subsection 5.5, these values are used as constraints for designing the amplifiers in the

proposed circuit's topology.

5.5 Pole Placement

The poles of the non-ideal loop equation 5.6 are of the form $p_{1,2} = r + jm$ and they are calculated analytically in equation 5.7. It is always desirable in a second order system to have poles located in the left half plane, as close to the $r = \pm jm$ lines as possible, to minimize ringing in the system's response and avoid over-damping and sluggish response times when adjusting to step input signals. Ringing can be especially harmful when the system must respond within a limited time frame, imposed in this case by the minimum addressing time.

$$p_{1,2} = -\frac{1}{2C_{nc}}\left(\frac{1}{R_{nc}} - g_\alpha\right) \pm \\ \pm\frac{1}{2C_{nc}}\sqrt{\left(\frac{1}{R_{nc}} - g_\alpha\right)^2 - 4 \cdot C_{nc}\omega_\beta g_\alpha} \tag{5.7}$$

5.5.1 Non-Ideal Loop Pole Calculation

Real Poles

The quantity inside the square root in equation 5.7 has to be positive, therefore

$$\left(\frac{1}{R_{nc}} - g_\alpha\right)^2 \geq 4 \cdot C_{nc}\omega_\beta g_\alpha \;\Rightarrow \\ g_\alpha^2 - 2\left(\frac{1}{R_{nc}} + 2C_{nc}\omega_\beta\right) g_\alpha + \frac{1}{R_{nc}^2} \geq 0 \tag{5.8}$$

where the roots produce $(g_\alpha - g_{\alpha 1})(g_\alpha - g_{\alpha 2}) \geq 0$ with

$$g_{\alpha 1,2} = \frac{1}{R_{nc}} + 2C_{nc}\omega_\beta \pm \pm 2\sqrt{\left(\omega_\beta C_{nc} + \frac{1}{R_{nc}}\right)\omega_\beta C_{nc}} \tag{5.9}$$

and since g_α is a physical quantity, $\omega_\beta \geq -(R_{nc}C_{nc})^{-1}$ and $\omega_\beta \geq 0$, thus $Gm > 0$.

Since the poles are real for this case, there are only two regions in which g_α has solutions, $g_\alpha \geq g_{\alpha 1}$ or $g_\alpha \leq g_{\alpha 2}$ producing:

$$\frac{g_{\alpha 1}(ro + R) + 1}{ro \cdot gm} - 1 \leq A1 \leq \frac{g_{\alpha 2}(ro + R) + 1}{ro \cdot gm} - 1. \tag{5.10}$$

Imaginary poles

In this case the quantity inside the root has to be negative, therefore by solving the same system it is found that:

$$\frac{g_{\alpha 2}(ro + R) + 1}{ro \cdot gm} - 1 \leq A1 \leq \frac{g_{\alpha 1}(ro + R) + 1}{ro \cdot gm} - 1. \tag{5.11}$$

The poles found by equation 5.7 can be rewritten as:

$$p_{1,2} = -\frac{1}{2C_{nc}}\left(\frac{1}{R_{nc}} - g_\alpha\right) \pm$$
$$\pm j\frac{1}{2C_{nc}}\sqrt{4 \cdot C_{nc}\omega_\beta g_\alpha - \left(\frac{1}{R_{nc}} - g_\alpha\right)^2}. \tag{5.12}$$

In order for the poles to be as close to the real axis as possible, quantity $Im[p_{1,2}]$ has to be minimized by $\frac{\partial Im[p_{1,2}]}{\partial g_\alpha} \longrightarrow 0$ since $C_{nc}, R_{nc}, \omega_\beta, g_\alpha > 0$, where:

$$\frac{\partial Im[p_{1,2}]}{\partial g_\alpha} = \frac{1}{2C_{nc}} - \tag{5.13}$$
$$- \frac{2\omega_\beta C_{nc} + g_\alpha - \frac{1}{R_{nc}}}{2C_{nc}\sqrt{\left(\frac{1}{R_{nc}} - a\right)^2 - 4g_\alpha\omega_\beta C_{nc}}}$$

This leads to:

$$g_\alpha \longrightarrow \frac{1 - \omega_\beta C_{nc} R_{nc}}{2R_{nc}} \tag{5.14}$$

and including g_α and ω_β then:

$$A1 \longrightarrow \quad \frac{1}{2gmro}\frac{2R_{nc} + R + ro}{R_{nc}} -$$
$$- \frac{1}{2gmro}\frac{C_{nc}Gmgm_{pix}R(R + ro)}{C_n} - 1. \tag{5.15}$$

All the possible accepted subcategories for the pole placement solutions are calculated as functions of the gains Gm and A1 based on equation 5.7 and they are presented in equations 5.10, 5.11 and 5.15.

Over-damping is a situation bounding the calculation of Gm and A1 gains and must be taken into account. To explain this constraint, we are again referring to the selected case of a 4.7 inch display driving 2048 pixels, assuming a refresh rate of 60Hz. The address time available for each pixel should be half the clock period assuming roughly 50% duty cycle, which amounts to a total available addressing time of $t_0 = 4\mu$sec for each pixel. To further clarify the impact of the available addressing time in circuit terms, the proposed system's equation 5.6 can be rearranged into equation 5.16 using equations 5.17 and 5.18.

$$\frac{I_{pix}}{I_{data}} = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \tag{5.16}$$

$$\omega_0 = \sqrt{\frac{1}{C_{nc}}\omega_\beta g_\alpha} \tag{5.17}$$

$$\zeta = \frac{1}{2\sqrt{C_{nc}\omega_\beta g_\alpha}}\left(\frac{1}{R_{nc}} - g_\alpha\right) \tag{5.18}$$

In order for the system to accurately respond in the given time t_0, quantity ω_0 has to be $\omega_0 \geq \frac{2\pi}{t_o}$. The larger the ω_0 is the faster the system responds. In case ζ has a very low value, there is ringing at the current output waveform, the amplitude of which can be momentarily almost two times larger than the settling value. The observer's eye might misinterpret this as an increase in brightness and that is why ζ should be chosen between 0.5 to 1. Values greater than 1 will force the system to produce an over-damped output with a possible transient larger than the available address time. Based on the analysis so far, using the results of Table 5.4, we can

calculate that Gm$\sim$16.68μ and A1=703 for ζ of 0.6 and t_0 of 4μsec. This falls exactly into the high and low limits calculated from equation 5.11:

$$689 \leq A1 \leq 764.$$

Amplifier Gm has to have a very small gain. This can be implemented with the use of a filter placed in series with a large gain Gm amplifier along the feedback path, in order to produce the desired values of ζ and ω_0 forcing the circuit to operate closer to the selected operating point.

5.6 Simulation and Chip Fabrication

Utilizing the above analysis, a single crystal silicon chip was simulated and fabricated as a proof of concept, using a generic 600nm technology node. A single column driver was part of this chip, driving a series of three test pixels, connected to the parasitic line depicted on the right side of figure 5.9. The circuit was designed using the above analysis for a portable 4.7 inch display with a 60Hz refresh rate.

In order to simulate a realistic single LTPS backplane column, Single crystal Silicone transistors (SC-Si) were utilized having the appropriate parasitics attached around their Gate, Drain and Source Terminals. These SC-Si transistors have half W/L ratios as opposed to the LTPS equivalents since the mobility of LTPS is about half that of SC-Si as graphed on the left side of figures 5.12 and 5.10. A variation in the SC-Si pixels' lengths is used, simulating the mobility variation due to degradation of the material with time. The pixels' Source terminals were wired to diode-connected transistors whose Source terminals were attached to the bonding pads of the chip

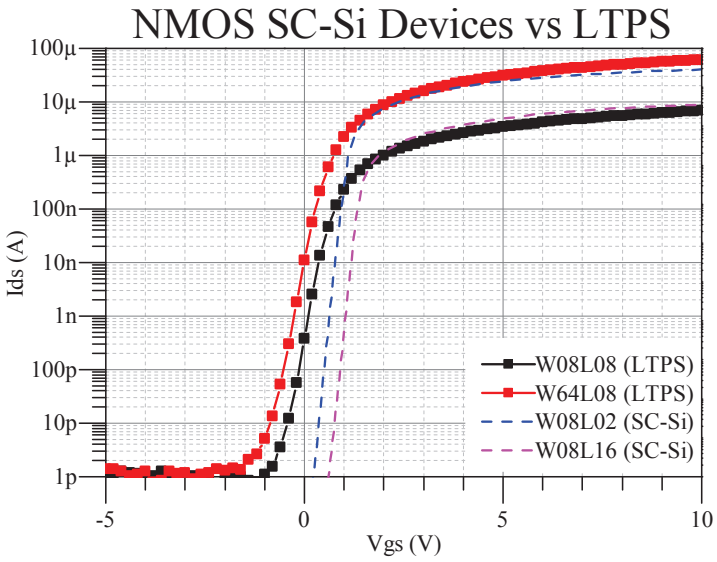


Figure 5.13: Single Crystal Silicon Devices Simulating the saturation characteristics of LTPS.

(Terminals Out 1-3 in figure 5.14). This permits the use of a Source-Measure Unit (SMU) connected directly to those pins, modulating the voltage for creating the threshold voltage variations, while measuring the current carried by the individual pixels. No actions where taken to fit the sub-threshold slope of the SC-Si transistors to that of the LTPS, since the pixel transistors are always in saturation during the proposed circuit's operation, except for the brief time the pixel is reset and turned on again.

A comparison between the resulting SC-Si and some generic LTPS transistors is presented in figure 5.13. Note that the proposed difference in Lengths from 2μm up to 16μm for the SC-Si transistors, simulates an equivalent mobility degradation of 87.5%. In this extreme case, the design of the proposed circuit has to be based on a gm_{pix} transconductance degradation of 87.5%, which translates to a lower limit of the LTPS transconductance as measured on table 5.4 of 0.525nS. A simple hand recalculation similar to the one presented in the Pole Placement section reveals the appropriate minimum limit for the gains used in this circuit. Note that table 5.5

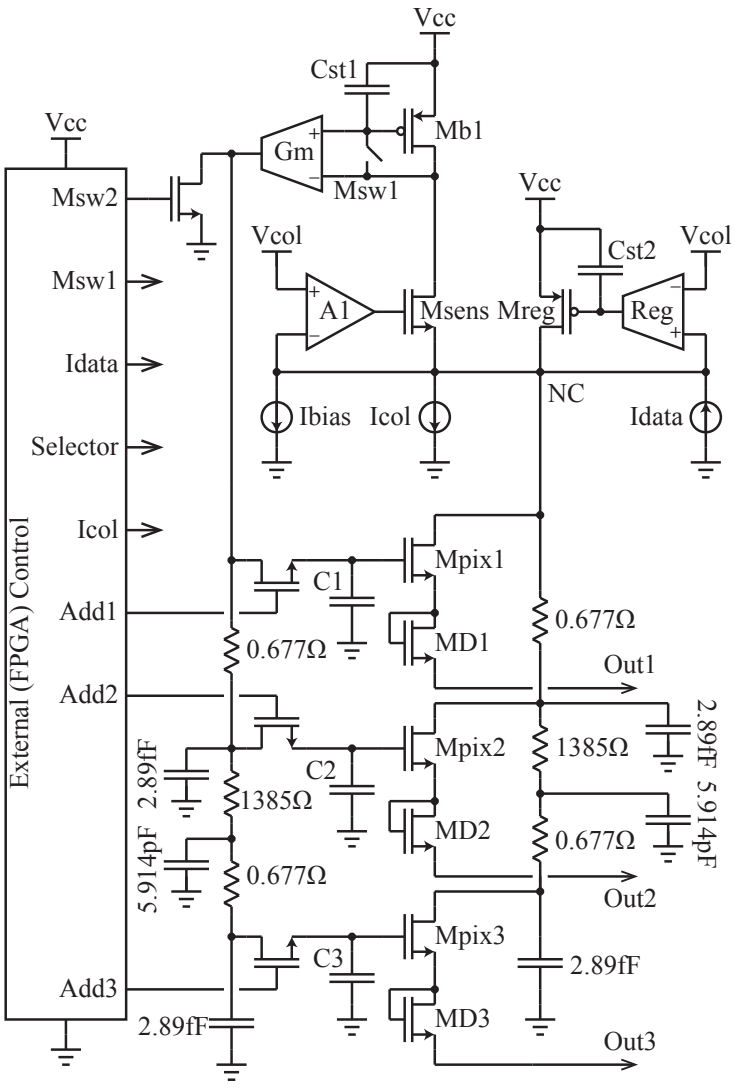


Figure 5.14: Schematic of the Simulated and Fabricated Circuit.

includes the W/L ratios of the pixels implemented with the SC-Si transistors. Those pixels simulate the LTPS transistors used in a backplane having all equal W/L ratios of 64/8 but with different mobilities due to degradation that vary from the normal 121 $cm^2/V \cdot sec$ down to 16 $cm^2/V \cdot sec$, translating to a maximum mobility degradation of 87%.

Figure 5.14 includes the exact circuit schematic of the fabricated chip used also in the simulations. Some extra capacitive parasitics are also present, resulting from

Table 5.5: Equivalent Mobilities

SC-Si	W/L [μm/μm]	LTPS μ_0 [$cm^2/V \cdot sec$]	% Degradation
Pixel 1	8/2	121	0%
Pixel 2	1/10	48	60%
Pixel 3	1/30	16	87%

the wiring of the externally controlled nodes to bonding pads of the fabricated chip. These parasitics however are not presented here, because they have minimal impact in the loop's operation since they are wired to voltage sources providing the switching signal inputs. Node NC is also wired to a pad connected to a current source providing the I_{data} current, which as mentioned in section 5.2 is controlled externally.

5.6.1 Verification of Circuit's Robustness for the entire Dynamic Range of Idata.

In section 6.2, data are presented about amplifiers Gm, A1 and Reg DC and AC operation such as Bode Plots as well as DC seeps, while the transistor level design of those amplifiers is shown in figure 5.15. For better conceptualization of the DC operation of the complete circuit, figure 5.15 illustrates the complete circuit topology excluding the pixels and the parasitics. Note that at node NC there is a resistor connected in series with the output of a Source Measure Unit (SMU). The SMU is used to measure the current through the resistor Rcol and is set to provide a constant voltage equal to GND. The current carried by R_{col} is constant and equal to:

$$I_{R_{col}} = \frac{V_{nc}}{Rcol}.$$

Another source measure unit named SMU2 is connected to the source of transistor

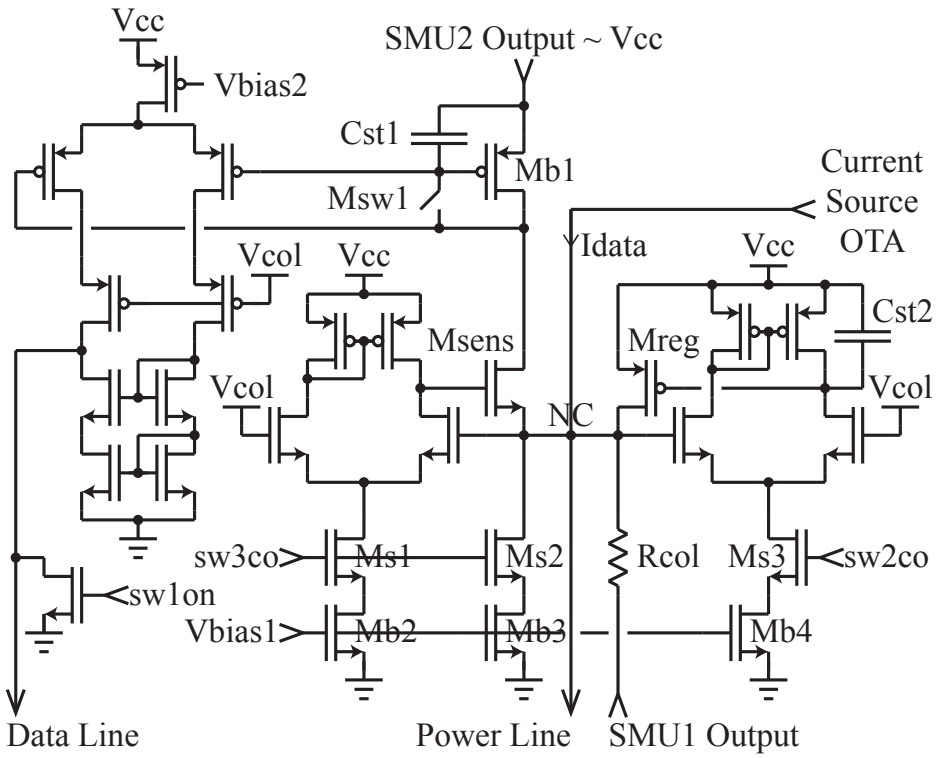


Figure 5.15: The complete circuit diagram of figure 6.1.

Mb1 (figure 5.15). SMU2 is set to provide a constant voltage equal to Vcc while it is measuring the current flowing through the Msens transistor. Since amplifier Reg is a linear regulator it is tested first to make sure that it is operating within its normal parameters. Setting sw3co as well as swOTA to ground and sw2co to Vcc (figure 5.15). Only Reg amplifier is activated. By sweeping the SMU voltage at the terminal of R_{col},the current is sweeped from 10μA to 1mA and the voltage level node NC is continuously monitored through an oscilloscope. Figure 5.16 shows that the DC voltage of node NC has a constant potential independent of the current flowing into NC due to Reg amplifier. Note that node NC is at 3V since Vcol is arbitrarily set to be at 3V for controlling the current through the resistor more accurately during this measurement. The small graph inside figure 5.16 shows that the voltage at NC varies roughly by 40mV and that variation is independently linked and controlled by changing the length of the Mreg transistor during the design process.

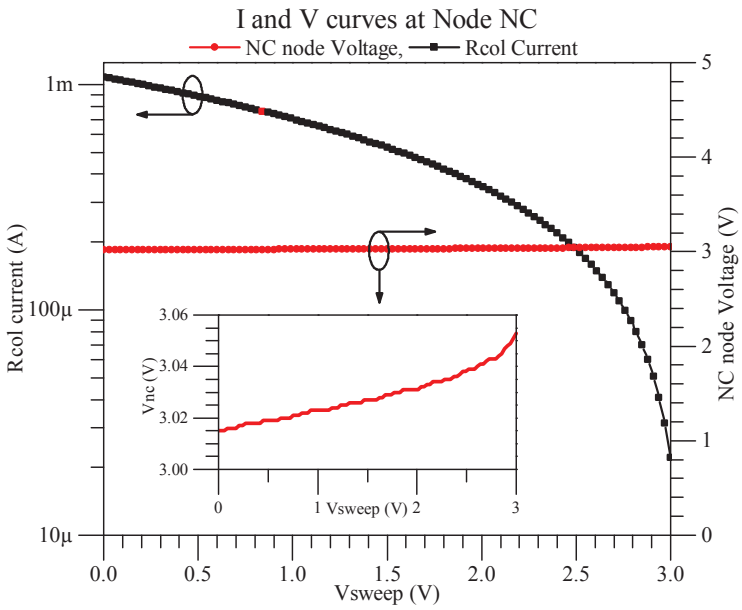


Figure 5.16: Current through the R_{col} resistor vs. NC node's voltage.

Before the A1 amplifier is observed, SMU1 is set to ground and resistor R_{col} is chosen so that the total column current is roughly 120μA. This is chosen arbitrarily within a range of currents varying from larger than the maximum pixel current and less than the maximum column current. Next, the A1 amplifier is activated by setting sw2co to ground and sw3co to Vcc. Vbias1 is chosen so that at steady state, the dc bias current of the A1 amplifier will be equal to 10μA, same as the current through transistor Mb1. In essence, Reg amplifier has been programmed to accommodate Icol's 120μA of current while the A1 amplifier is turned on and standing by. The voltage at Node NC remains constant, as previously explained and the switch signal at swOTA, as shown in figure 6.2, is set to Vcc. Vin is sweeped and the OTA's R_d resistor is chosen such that at the output a data current that ranging from 0 to 20μA is produced.

Figure 5.17 depicts the absolute measured currents though the SMUs where SMU1 is represented by the Column Current (red Line) and SMU2 is represented by the Sense Node Current (black line). Note that The sense node current is at 10μA and

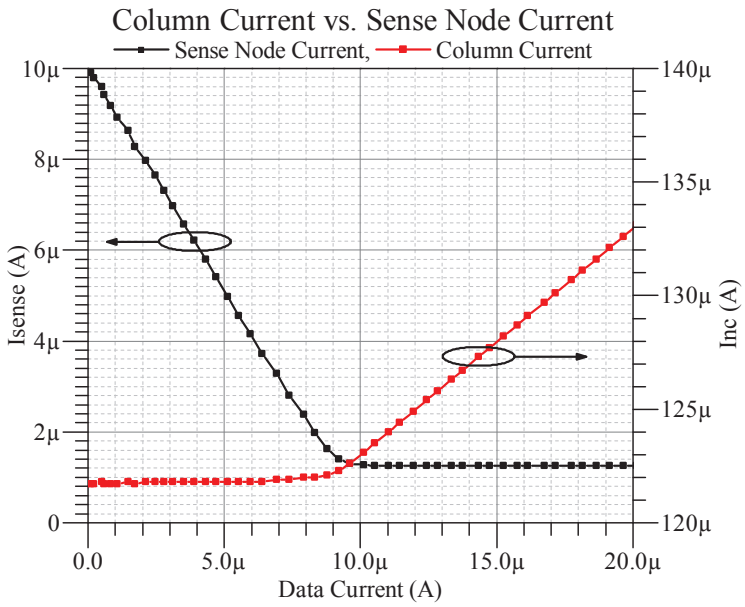


Figure 5.17: The measured currents going through the sense transistor and Rcol in figure 5.15

the Column Current is at 120μA as calculated. The Data Current is forced through node NC and the current through Mb1 gradually becomes less until the I_{data} value surpasses the current supplied by the Constant Current Source (CCS) transistors Ms2 and Mb3 (figure 5.15) which is 10μA. At that moment the only path able to carry current is through resistor R_{col}. Note that in figure 5.17 as long as I_{data} (x-axis) is below 10μA The total column current (red line) remains constant and when it surpasses the total current provided by the CCS transistors it starts to flow towards SMU1 (red line increases). It should also be noted that for Data Currents above 10μA, the A1 amplifier no longer is no longer operational and node NC is no longer regulated. The potential at node NC is increased as current is being carried by resistor R_{col}.

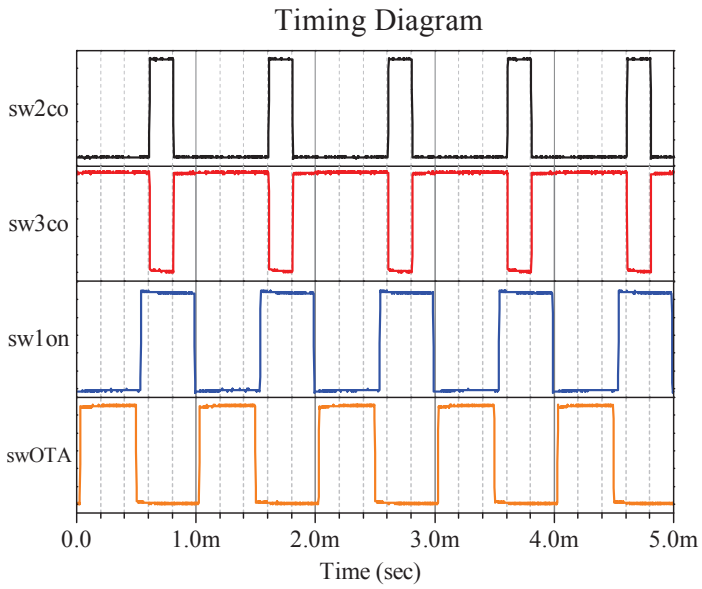


Figure 5.18: The timing Diagram.

5.6.2 Explanation of transient noise in the pixel current

Having verified the system's operation at DC, sw1co, sw2co, sw3co and swOTA are supplied with the appropriate pulses for the operation of the circuit. As shown in figure 5.15 for the circuit to operate properly sw3co has to the same as pulse sw2co negated, as shown in the top two diagrams of figure 5.18. Also clear is that the duty ratio of sw2co depends on the time Reg amplifier requires to adjust to the new total column current, which is the previously programmed total column current, plus or minus the newly programmed pixel current. This quantity is highly dependent on capacitor Cst2, since the larger that capacitor is, the more time it will take for the Reg amplifier to adjust, therefore the bigger sw2co's duty ratio will be. We calculate for the current design a normal value for that capacitor, which enables the circuit to behave normally, is 40pF.

Utilizing the experimental setup integrated into the chip and providing it with the correct switching, as explained previously and presented in figure 5.18 and 5.4,

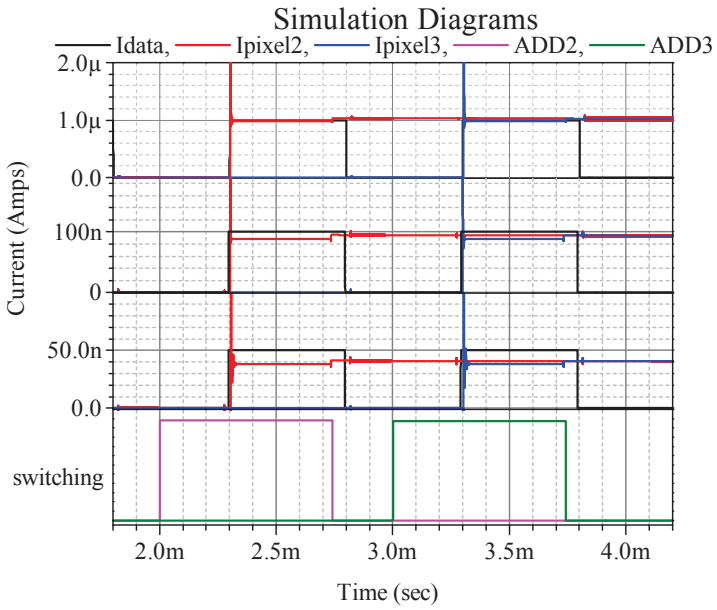


Figure 5.19: Simulations of the prototype high voltage driver. The total column current is only 10μA for this measurement.

an early attempt to compare the measured data of the current through the pixel transistors versus the simulations is presented. The goal of this early attempt was to evaluate how close was the design of the control loop based on the assumptions made for the parasitics attached to this driver design. The analysis presented here will evaluate the performance based on pixels 2 and 3 because they are situated the furthest from the driver, having most (for pixel 2) or all the line parasitics (for pixel 3) attached between their physical location and the driver.

Some of the gathered data of the fabricated chip for pixel 3 are presented in figure 5.20. Here it is immediately clear that there is a discrepancy between the operation of the loop in the simulations and the operation of the loop in the presence of real signals. As one can observe, for larger data currents the circuit operates similarly to the simulations with the only exception being noise present in its output. For lower data currents, however, this noise becomes a prohibiting factor in the circuit's operation, "drowning" the signal into noise, not allowing the loop to accurately lock

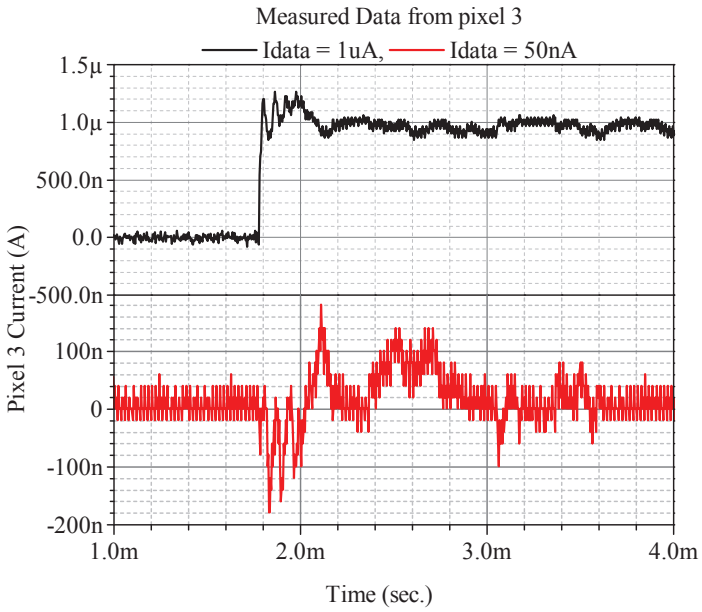


Figure 5.20: Pixel 3 data of the prototype high voltage driver. The total column current is only 10μA for this measurement, same as figure 5.19.

to it.

For Icol=23μA, the data are gathered and concatenated in the graphs included in Figure 5.21. The programming error drops to around 10% when Idata is around 200nA, only slightly off of the posed specifications described previously. When the total column current Icol is increased to 183μA however, there is an offset in the programmed pixel current as shown in figure 5.22(a) and the error becomes tremendous for the entire Idata range and especially for the low values.

The transconductance of the large Mreg transistor is presented in the top graph of figure 5.23. Careful experimentation reveals that perturbations coupled to the gate of Mreg through capacitor Cst2 are responsible for disturbing the normal operation of the programming loop. These perturbations originate from capacitively coupled digital noise as well as shot noise currents leaking into the substrate underneath Mreg's channel. When the voltage noise spectral density present at the gate of the Mreg PMOS transistor reaches 200nV/$\sqrt{Hz}$, the current noise spectral

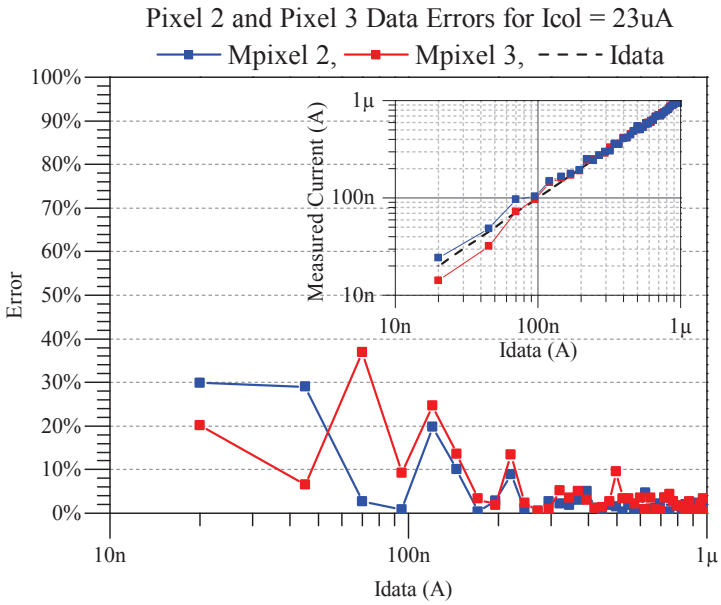
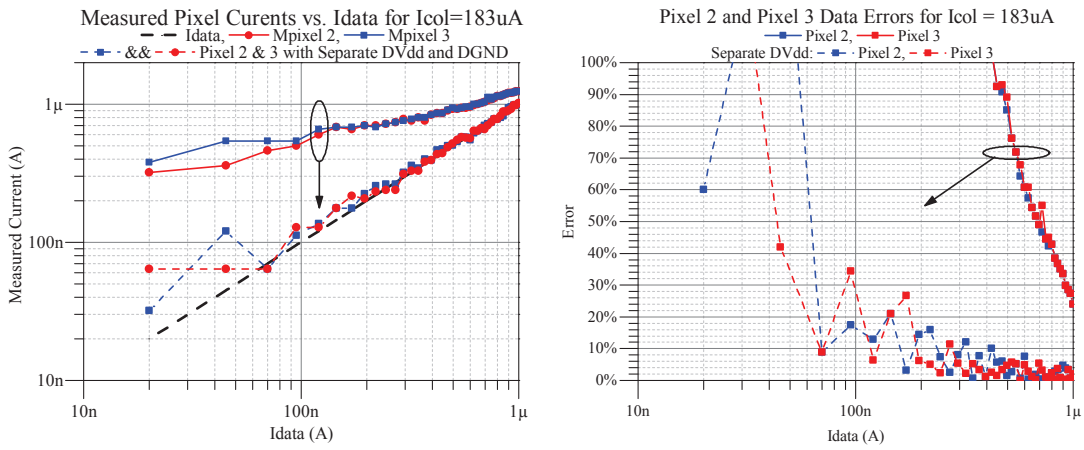


Figure 5.21: Graph of the calculated Error in the pixel currents for Pixels 2 and 3 vs. Idata. The measurements are presented in the smaller graph included here.

density present in the Mreg PMOS transistor's channel is calculated with the help of equation 5.19 where I_{Mreg}^{noise} is the noise present in its channel, e_n is the noise spectral density present at its, gm its transconductance and BW is the total Band Width available for the nominal operation of the circuit.

$$I_{Mreg}^{noise} = E_n \; gm \; \sqrt{BW}. \tag{5.19}$$

The larger the total column current is, the larger the transconductance of the Mreg transistor, therefore the larger the noise present in its channel during the programming time as shown at the bottom of figure 5.23. Specifically for a column current in the range of 200μA the total noise current is around 200nA, an order of magnitude larger than the minimum programming current of 20nA. This is very problematic since the error at very low currents becomes remarkably large, barely dropping below 20% for the largest Idata currents of 1μA as shown in figure 5.22.



(a) (b)

Figure 5.22: Measured Pixel Currents for (a) Icol=183μA with the same and with separate DVdd and DGND power supplies and (b) Calculated Errors vs. Idata.

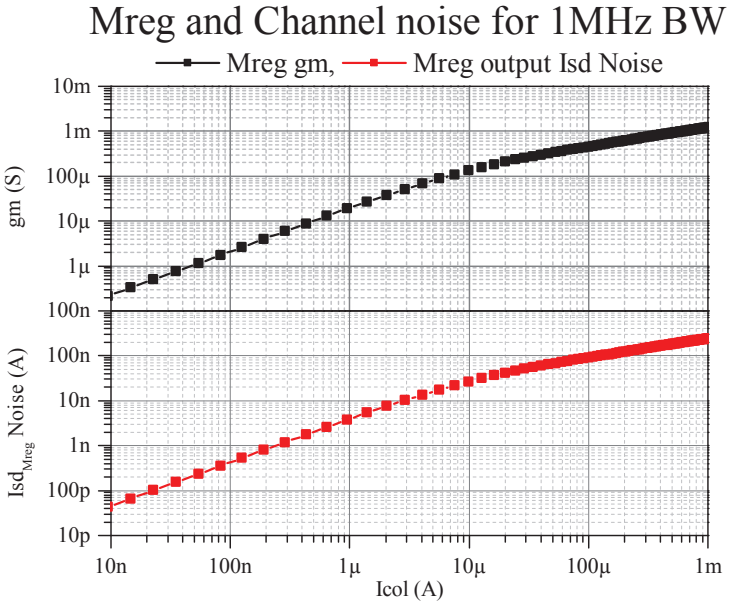


Figure 5.23: Mreg transistor's transconductance and current noise in the channel for a BandWidth of 1MHz [1], versus the Column Current Icol.

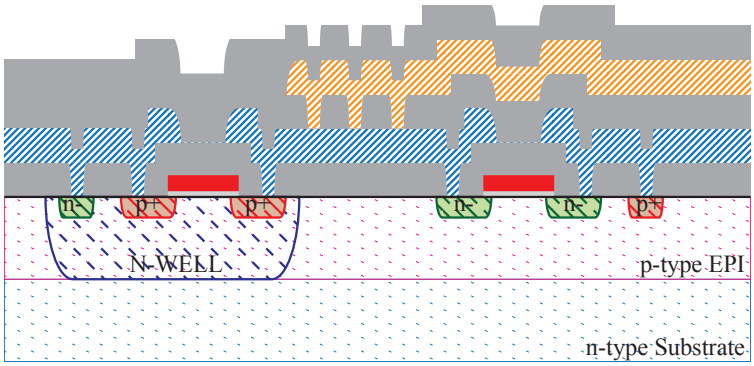
5.7 New Techniques for Better Isolation from the Digital Noise

5.7.1 Digital Noise shielding techniques

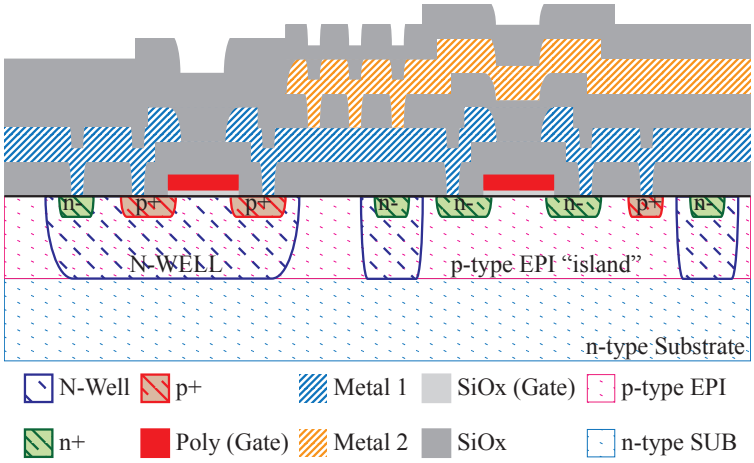
The technology node utilized in the layout of the aforementioned driver is a Single N-well, epitaxial P-type material over an n-type substrate technology, with a minimum feature size of 600nm. As opposed to all the PMOS transistors which are partly isolated in their own N-Wells, the NMOS transistors have their channel directly exposed to the p-type epitaxial material.

This is very problematic because potential variations localized around the area of the NMOS transistor channels directly modulate their drain to source currents. A good practice in design is to put p^+ contacts attached directly to the substrate as close to the NMOS transistors as possible as shown in figure 5.24(a). Those contacts create a one sided pp^+ junction the p-type epitaxial substrate, connecting it externally to the lowest possible potential (GND in our case). This ensures that the p-type EPI will always be as close to ground as possible, with the only limitation being the maximum current the pp^+ junction can sink. In some cases quickly evacuating the free charge from the substrate might create a problem if there exists only one such pp^+ junction with a relatively small maximum current density it can accommodate before collapsing.

Since this is a single well technology, the N-Well doping layer can be used to surround sensitive or noisy transistors and define separate p-type bodies around the NMOS transistors, grounded separately, isolating them from the rest of the NMOS as well as the PMOS transistors in the circuit as shown in figure 5.24(b). Even better



(a)



(b)

Figure 5.24: (a) Crossectional view of the technology implementing the design and (b) the same except on the right where a p-type island is defined by surrounding the NMOS with an N-Well guard ring.

results are achieved when the digital circuitry is separated from the analog while separate power lines are utilized for powering the digital circuit from the analog ones, isolating the digital noise from the critical nodes in the rest of the layout. This digital DVDD and DGND lines are attached to all the transistors (NMOS and PMOS) implementing switches.

It is not always feasible to put the switching transistors far away from the analog circuitry, therefore double guard rings are utilized for isolation. One such example is

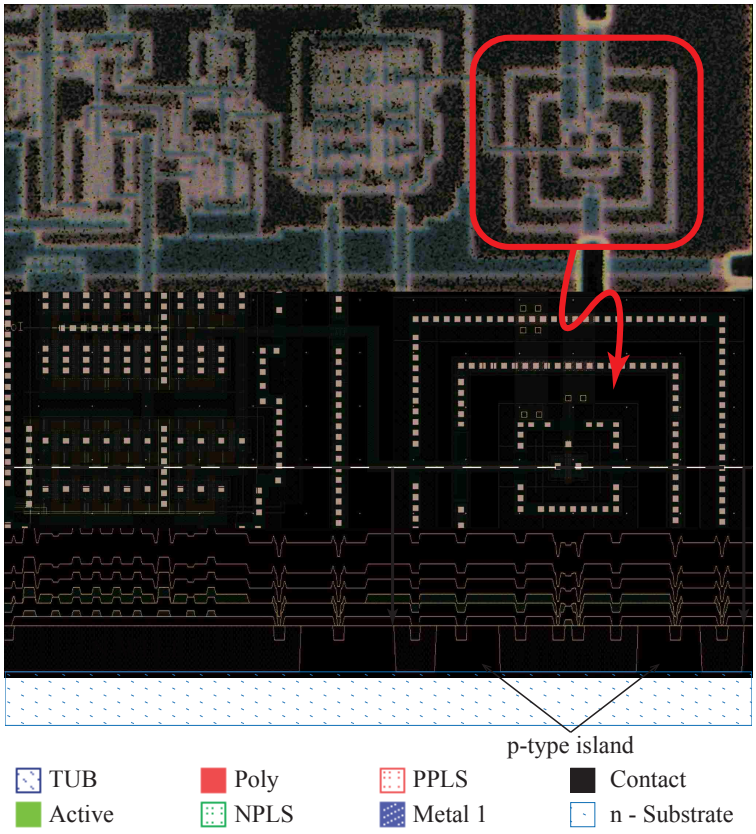


Figure 5.25: Layout of the Msw transistor from the low noise fine output Operational Transconductance amplifier of figure 6.2

found in figure 6.2, whre the Msw transistor has to be physically close to the output of the fine OTA in order to produce a zero output current when swOTA becomes low. The layout of such a circuit is presented in figure 5.25, where the PMOS resides inside an N-Well, surrounded by a n^- guard ring attached to DVCC. Both of the transistor and the n^- ring are surrounded by another N-Well n^- ring, also attached to DVCC. Between those two N-Wells there exists yet another p^+ guard ring attached to DGND, whose function is to ground the p-type island area surrounding the innermost N-Well guard ring. This entire structure represents the double shielded guard rings and it is utilized everytime a switch transistor must be surrounded by analog circuitry.

The results gathered after utilizing the guard rings and the seperate digital power

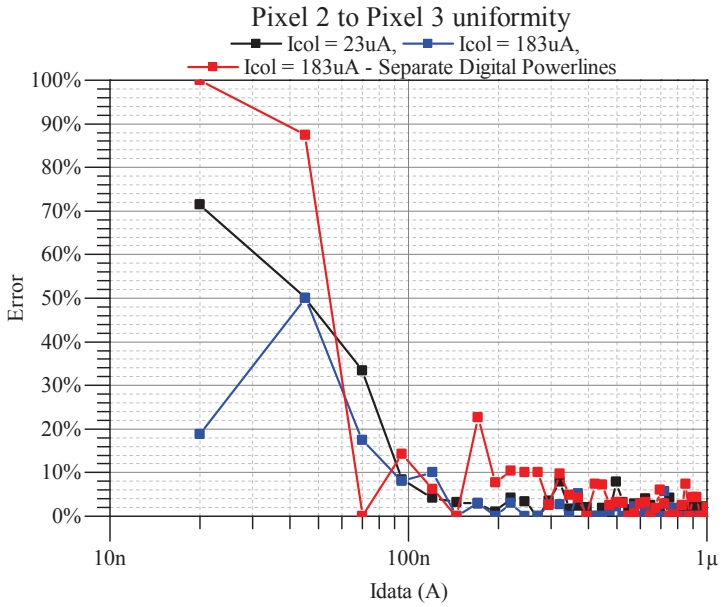


Figure 5.26: Uniformity of Pixel 2 to Pixel 3 programmed currents.

lines are presented with the dashed lines in figure 5.22. The extracted uniformities between the currents of pixels 2 and 3 are presented in figure 5.26.

5.7.2 Dominant Capacitor Isolation

The results after the digital isolation are better, but still the error remains at around 15% for programming currents of more than 200nA and does not approach the expected 50nA with 10% of programing error **as was surmized earlier in the beginning of this paper**. The reason the current falls outside from the expected specifications lies within the physical layout of the dominant capacitor Cst2.

The gate node of the Mreg PMOS transistor whith which this capacitor is connected, is one of the most sensitive nodes of this circuit as has been proven by the innaccuracies of the loop when noise is coupled through that node in section 5.6.2. It stands to reason that a great deal of care has to be put into the design of this

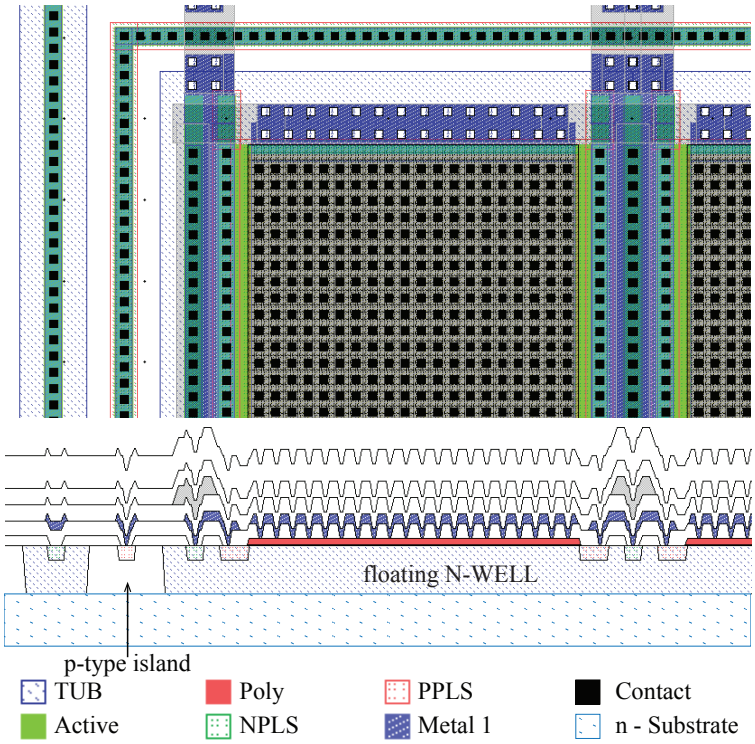


Figure 5.27: Isolated Dominant Capacitor Layout and Cross-section.

individual capacitor in order to avoid unneeded behaviour. To that extend, a large portion of this capacitor could be connected externally, though it is always a good principle to integrate some of that capacitance directly to the chip, as close to the critical node as possible.

In integrated chip design, capacitors are some of the most difficult elements in designing a chip due to their large size. In figure 5.27, the cross-section of a part of the dominant capacitor's layout is presented. This is a p-type CMOS capacitor utilizing the gate oxide as the capacitor's dielectric, which provides the designer with the highest sheet capacitance density due to its small thickness. The capacitor is isolated from the rest of the circuit by a surrounding N-well guard ring connected to both the most positive analog power supply and the positive terminal of the capacitor, also seen in the schematic of figure 5.15. The negative terminal of that

capacitor connected to the gate of the Mreg transistor is the Poly, which is insensitive to the aforementioned noise.

In our approach, the large capacitor size needed for the operation of the circuit will occupy a large amount of area over the substrate near the Mreg PMOS transistor, which has the sideffect of coupling noise into its gate. This originates from its lower terminal, implemented by the N-well for this case. This terminal is directly exposed to flicker noise leaking out of the PMOS transistor's N-Well due to large currents coursing through its channel, which is then coupled into the N-well of the capacitor through the n^- substrate making the gate of the Mreg transistor susceptible to flicker noise. A technique that ensures the isolation of the capacitors from this kind of noise is to utilize n-type CMOS capacitors in isolated floating p-type islands. However, the circuit topology has to change partially to be able to accommodate this changes and the change is shown in figure 5.28.

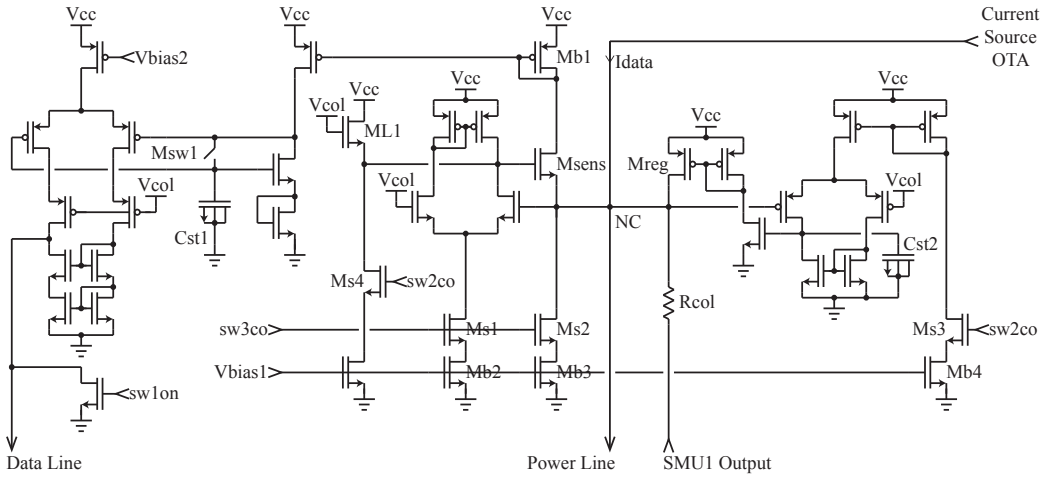


Figure 5.28: Variation of the proposed topology for better noise isolation.

Note that capacitors Cst1 and Cst2, in this figure, are NMOS transistors with floating body, having all three of ther source, drain and body terminals grounded, while their gates are connected to the sensitive nodes of the circuit. Since the p-type EPI "island" as presented in figure 5.24(b), plays the role of the negative terminal of

the capacitor attached to ground and its thickness is very large, the n^- regions are totally isolated from any noise being coupled through the n-type SUB. This is only the case assuming the positive power supply where the N-Well defining the p-type EPI "island", is also noiseless. It should also be pointed out that the Reg Amplifier is not implemented with a NMOS but with a PMOS diff pair, in order to drive the equivalent output stage comprised of a NMOS driving the Mreg transistor through a current mirror as presented in the right of figure 5.28.

Finally the extra transistor branch added, comprised of Ms4 and ML1, ensures that Msens transistor will remain in the off state during the Reg amplifier's operation. For example, when Ms1 switches off, the circuit is no longer supplied by a constant current. If this branch is omitted, The left-over charge is evacuated through the positive power supply VCC, raises the potential at the gate of Msens, turning it on. In this situation, the Mreg transistor is unable to match exactly the current flowing through Rcol, which renders the circuit inoperable at large Icol currents. When sw3co becomes low and sw2co high, since the current through Ms4 is known, transistor ML1 is sized correctly so that the gate node of Msense will be kept close to 3V, prohibiting it to turn on and induce negative offset in transistor Mreg, during the operation of the Reg amplifier.

5.8 Measurements of the Ipixel currents for the entire Dynamic Range

Modern OLEDs, based on the type of material, have a bias voltage ranging from 4 to 8 volts for achieving optimal efficiency [30–33]. In this version of the proposed circuit, Vcol controls the voltage level of node NC, therefore based on the bias voltages used

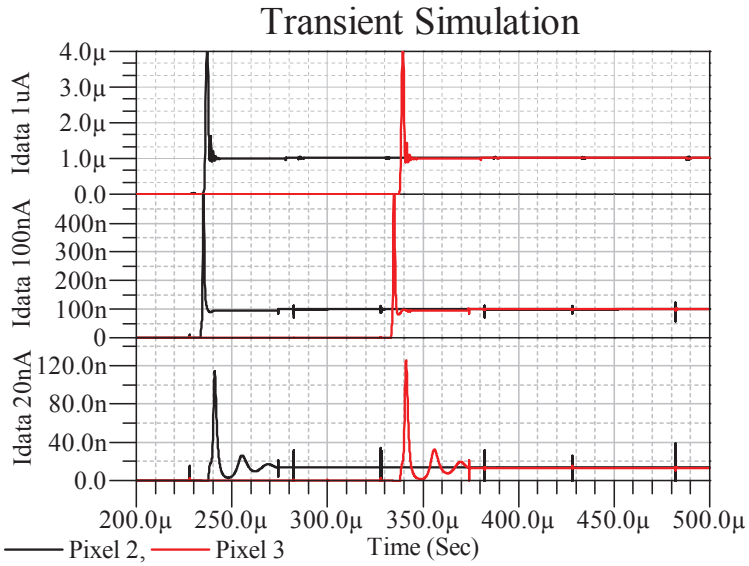


Figure 5.29: Transient simulation of the new circuit for Pixels 2 and 3.

for operating OLEDs, NC is set to 3.5V, allowing enough headroom only for some of the LED technologies interfacing with the circuit to operate normally assuming a supply voltage Vcc of 5.5 to 6V and maximum programming currents of 1μA. Other versions of this designs for higher voltages can also be fabricated and have proven to be successful driving currents as low as 20nA [26]. Figure 5.29 presents the simulated and measured data for the degraded pixels 2 and 3 for programming currents of 20nA, 100nA and 1μA.

The uniformity between pixel 2 and pixel 3 is noticeable despite the 60% and 87% degradation in mobility (table 5.5); a systematic way is mandatory to evaluate the error between the pixels and the I_{data} programming current, as well as the pixel to pixel uniformity. During the circuit simulation, the programming current is swept from 10nA to 1μA and the simulation is ran multiple times so pixels 1, 2 and 3 are programmed with the respective current each time. The errors are calculated with the help of equation 5.20.

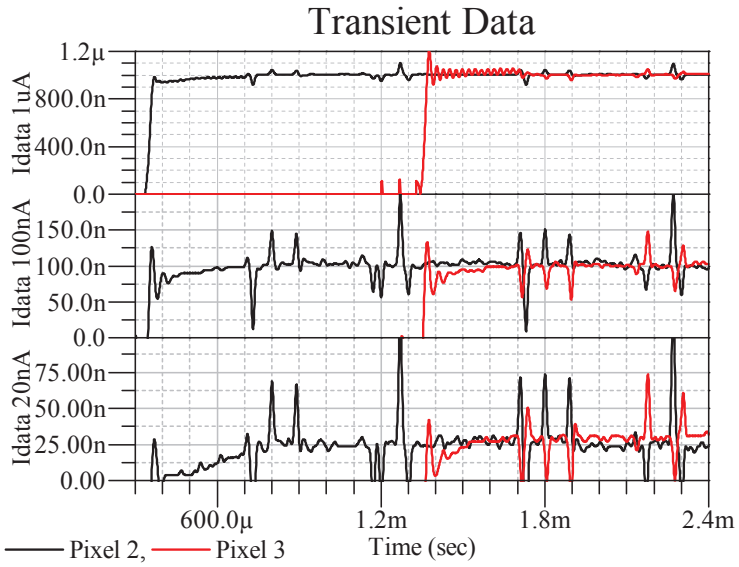


Figure 5.30: Transient Measured Data of the new circuit for Pixels 2 and 3.

$$\%e = \frac{|I_{data} - I_{pixel}|}{I_{data}} \tag{5.20}$$

This circuit was simulated while supplied with the pulses shown in figure 5.18 and the transient results are shown in figure 5.29. Note that this simulation was done in a similar setup as the one presented in figure 5.19, but here, the error appears to be almost non-existent especially for the low currents.

Naturally, the fabricated chip's gathered data are expected to be slightly different from the simulations, thus extra precautionary steps ensuring the elimination of noise were taken during the new layout of the chip. These include also the digital noise shielding and dominant capacitor isolation techniques previously described. Design rules such as separating the digital from the analog lines from intersecting and physically placing the analog circuits as far away as possible from the digital ones, were incorporated in the new design as an extra safety measure.

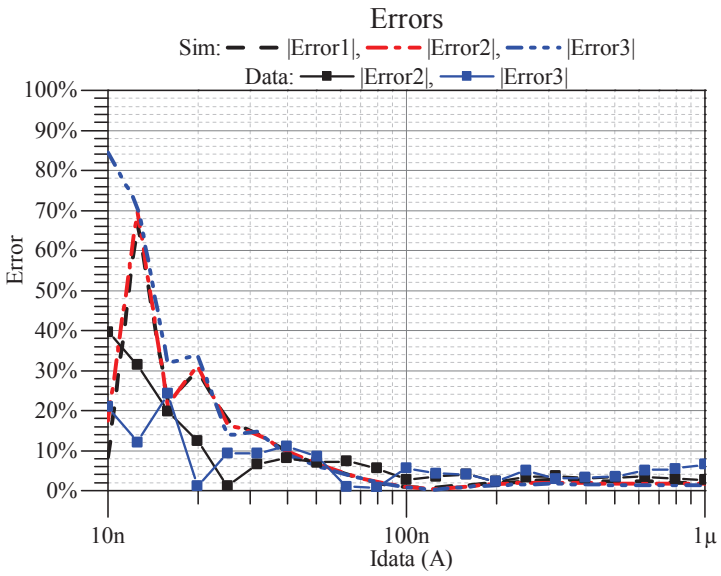
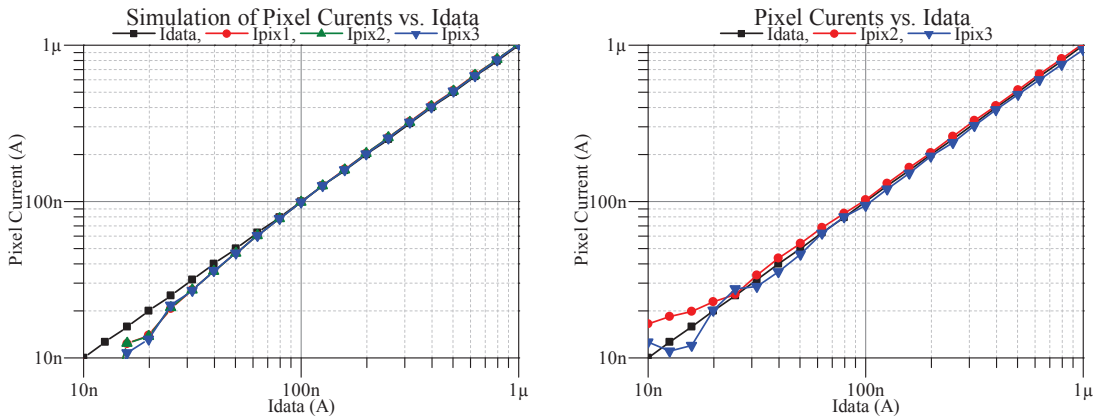


Figure 5.31: Errors of simulated and fabricated circuit.

The fabricated chip's gathered data for pixels 2 and 3 are presented in figure 5.30. As it is seen, there are still spikes in the pixels' currents associated with switching noise. The behavior of the driver concerning the current output levels, however, closely resembles the simulations as opposed to the currents previously measured and presented in figure 5.20. To further support this claim, error graphs similar to the previous figures 5.21 and 5.22 are presented in figure 5.31. The dashed lines in this graph represent the Simulated errors and the solid lines represent the gathered data.

During the specification of the circuit's operation, it was surmised that the system should be able to program a pixel current of 50nA with 10% of error. In figure 5.31 the simulated pixels' Errors drop below the specified 10% at 40nA, while the fabricated system's measured Idata programming current errors drop down to the 10% Error line as low as 20nA. Moreover, figures 5.32(a) and 5.32(b) outline the simulations and gathered data of the pixel currents versus the programming Idata current for the entire dynamic range. The measured data here show that the systems is operating



(a) (b)

Figure 5.32: I_{data} versus I_{pixel} currents for Pixels 2 and 3.

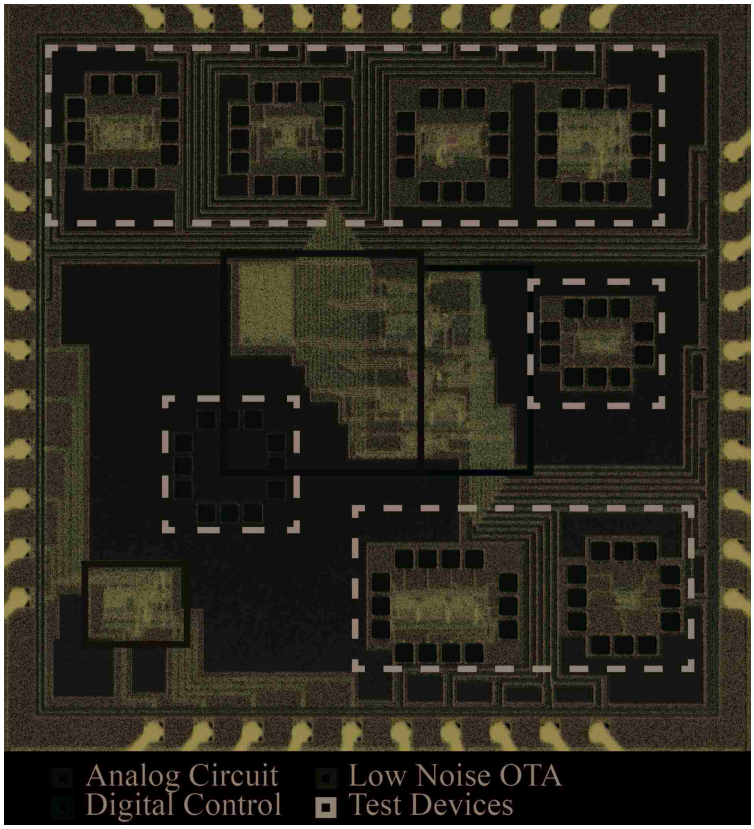


Figure 5.33: Photomicrograph of the Fabricated Pixel Driver.

normally for the entire dynamic range of data currents, closely following the Idata lines as opposed to the data gathered and presented in figure 5.21 and 5.22(a).

Figure 5.33 illustrates a photomicrograph of the fabricated driver. Around the chip, individual devices are placed for all the previously described testing purposes. At the center lies the programming column driver. On the left side of the figure, the analog wiring is directed to the pads and away from the digital wiring to avoid any unnecessary intersections. On the right the digital wiring is visible, and it is directed also away from the analog to the pads. At the bottom left, the low noise, fine output OTA is presented. I has been placed separately from the main circuitry for testing purposes and it was externally connected to it during the data gathering procedure.

5.9 Conclusion

In this chapter, the novel, evolved, AM(O)LED driver architecture is presented and analyzed, compatible with 2-transistors 1-capacitor pixel structures operating without no extra sensing lines or additional pixel components. A feedback circuit implemented between a pair of power and data lines enables accurate programming of the pixel drive TFT current independent of any variations in mobility or threshold voltage, by utilizing the power line as both power and sense line. The operation of the circuit is described step by step while parasitics of select panels are listed and utilized in an experimental prototype design implementation of the circuit. This new approach has been verified through both circuit simulations as well as through a prototype IC driver driving SC-Si test pixels. Our analysis proves while our circuit simulations and experimental results verify that a high level of accuracy for drive TFT currents as low as 20nA can be achieved, maintaining the fast programming times with our topology. The new approach is compatible with all backplane TFT technologies and can be implemented either externally on the backplane periphery or with an integrated TFT display data driver.

Chapter 6

Peripheral Devices, Measurement Techniques and Validation

6.1 Introduction

A newer, more successful design was presented in [1]. A method of decoupling and using both amplifiers OA1 and OA2 in the feedback loop is described changing the transfer function and the internal plant variables for controlling the loop, while preserving the functionality of the basic principle. The basic theory is well defined, there are, however, plenty of subjects not fully clarified, such as the impact of all the devices interfacing with the loop.

The description of such peripheral devices internal to the chip is presented in this chapter, for devices such as the data supplying current source or the output buffers for the pixel current measurements. Insight about the impact of those devices on the feedback control loop is provided through their analysis, while in the following

sections, the steps for careful layout of the control loop are revealed.

In the previous sections the main system was described omitting some of the devices that supply the signal or extract the measurements. These devices, however, can be as much sophisticated in their operation and layout as the driver itself. This chapter's purpose is to expose the reader to some of the challenges in interfacing the peripheral devices with the main circuit, while explaining their operation along with the operation of the internal ones such as Msens, Mreg and Gm.

6.1.1 Implementation of the I_{data} Current Source

In one of the implementations of the display driver [1], the I_{data} current source has its positive terminal attached to ground and its negative terminal attached to node NC. Although such a representation for calculating the AC response of the loop is acceptable, in reality the current source will be the drain of a transistor, therefore its positive terminal should be attached to the positive power supply as shown in figure 6.1.

An accurate low noise trans-conductance (OTA) amplifier is utilized in order to translate the analog voltage signals provided by the graphics card's Digital to Analog Converter (DAC) to current signals read by the column driver. Due to popular demand, most modern transconductance amplifiers are designed for high bandwidths and fast response times [34], with little attention paid to their output current level accuracy [35] since the are normally used as comparators driving specific loads. For the proposed application, the current source attached to node NC is replaced with the OTA, which has a very large output impedance, operating at frequencies as high as 1MHz. More over this OTA must have a very large degree of linearity to produce a current as low as 1nA and as large as 1uA with less than 1% of error at

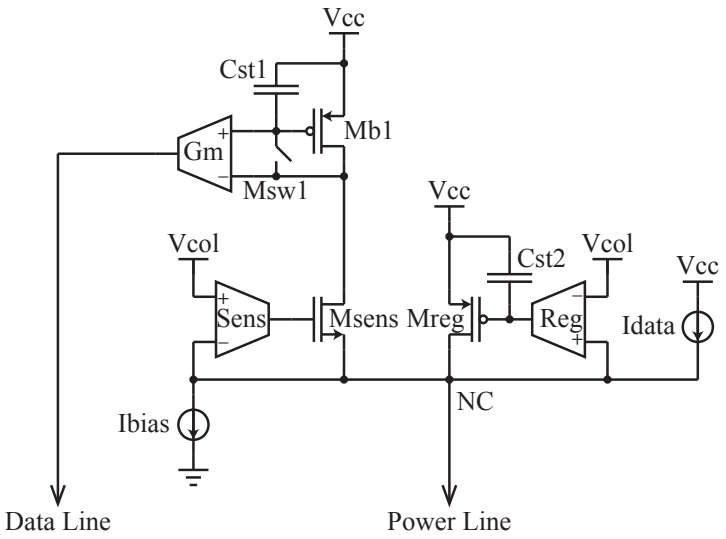


Figure 6.1: The previously described circuit [1].

those frequencies, therefore the operating point of this amplifier has to be chosen to satisfy these specifications. Figure 6.2 presents described OTA topology utilized in the experiments described in this paper.

To meet the above specifications of wide range and large output impedance, a telescopic folded-cascode differential input pair implemented with P-type Metal Oxide Semiconductor (PMOS) transistors is chosen as the first stage. Those PMOS allow for the common input voltage range to operate from very low potentials without running into the problem of saturating the input, while the folded cascode topology retains the dynamic range unchanged. The final stage is a current-mirror buffer stage, comprised of a cascoded PMOS transistors, driven by the previous folded-cascode topology to provide the necessary, positive polarity, output currents. The current reference side of the current mirror, sources its output to resistor R_d and a voltage is produced. Resistor R_d can have an arbitrarily large value, since the current also depends on the size of the PMOS transistor driving it. The trade-off is that this resistor has to have a minimum value that is set by the maximum size of transistors

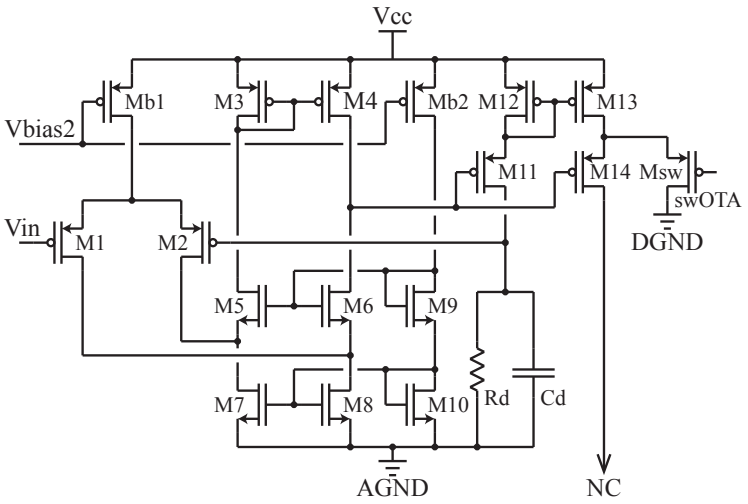


Figure 6.2: The low noise fine output Operational Transconductance Amplifier.

that allows for output C_{gd} and C_{ds} capacitances to be minimized in order for the circuit to operate at the required frequency of 1MHz. Assuming that the maximum input voltage is 2.5V, the current mirror is designed with the appropriate ratio to produce the required current at the output, which connects to NC. That voltage produced by resistor R_d, is sampled and fed back to the negative terminal of the input differential pair, thus stabilizing the overall circuit.

Note that transistor Mb2 is supplied with the same Vbias as the current source Mb1 and it is utilized simply to bias the folded-cascode differential input pair. In addition, instead of providing switching pulses with different levels at the input Vin of the OTA, a step waveform with different dc levels corresponding to the input data current is provided. At the very last stage, a PMOS switch is placed in parallel with the output, which when switched on, draws the entire current to ground, switching the output transistor off and making it behave as an open circuit. This minimizes the turn-on transient response of the OTA since current is already flowing out from the output the entire time and the channels in all the transistors, except the output PMOS, have already been formed. It is also important to observe that the switching

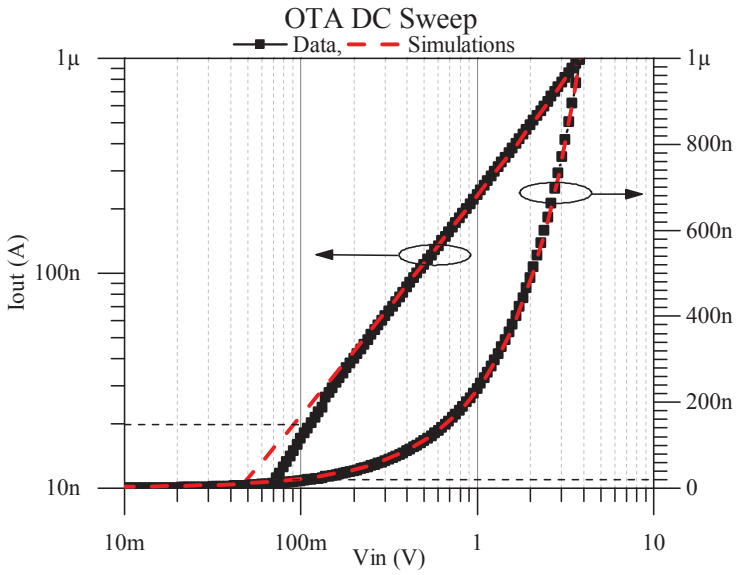


Figure 6.3: A DC sweep of the proposed OTA.

transistor Msw is provided with a negated switching signal since it is a PMOS, while its output is transferred to the Digital Ground which is separate than Analog Ground to avoid excess switching noise in the sensitive analog circuit. Analog and Digital Ground are both connected off chip in latter implementations of this circuit.

Figure 6.3 depicts a DC sweep of the input, spanning almost three orders of magnitude ranging from 50mV up to 4V. The right axis in the same plot, represents the output I_{data} current of the driver as a semi-log x function of the input voltage. The left axis on the graph illustrates the loglog x output plot I_{data} current vs the input data voltage, which better represents the function at very low values of 50mV up to the very larger ones of 4V. Note that for the log log plot the linearity is maintained in both the simulations and the gathered results through almost the entire range of operation.

6.1.2 Current Buffer for Independent and Unaltered Data Gathering

One of the most important steps for verifying this circuit is measuring the current through the programmed pixel without perturbing the system and keeping the loading down to a minimum during the measurements process. Current mirrors are implemented with the 3 pixel drivers in order to measure the current coming from the output. For the low current measurements, the column current is copied into a measured line, which is connected to a simple instrumentation amplifier circuit that converts the current to a voltage. Fig. 6.4 shows the experimental setup used for the low current measurements. A buffer circuit that decouples the current signal coming from the output measurements of the pixels is designed and fabricated on chip while the rest of the measurement setup is implemented separately on a printed circuit board, in order to have a better control of the gain of the transconductance instrumentation amplifier circuit that converts the current to a voltage. In order to minimize the error between the reference and the output currents these mirrors where cascaded and laid out utilizing the a Common Centroid layout scheme.

To further increase the accuracy while measuring the output currents, a buffer - regulator is used to set the voltage of the measure line at the same potential as node NC. That buffer topology is presented in fugure 6.4. Note that Vbias is controlled externally setting the total output bias current. That current has to be chosen appropriately so that when combined with resistor R_S it should produce 5V at the drain of transistor Mb1. Cblk has a large enough value setting the -3dB point of the high-pass to a very low frequency, while effectively blocking the DC offset at the output. Finally the output resistor is 1MΩ but the value it has may varie depending on the level of the currents under measurement. Finally the output is hooked up

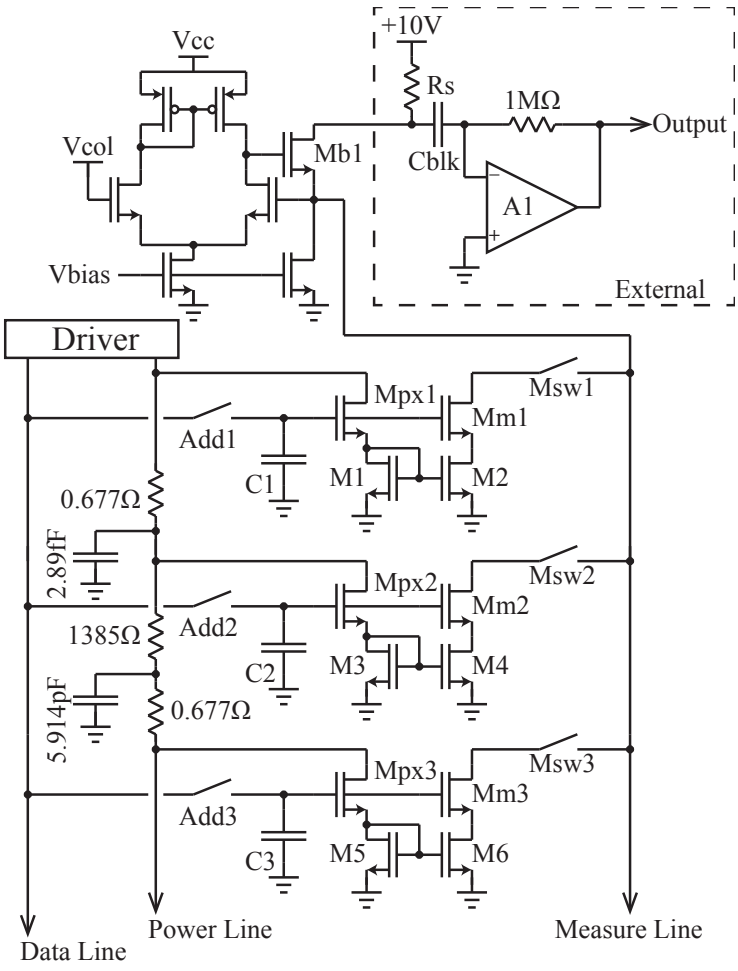
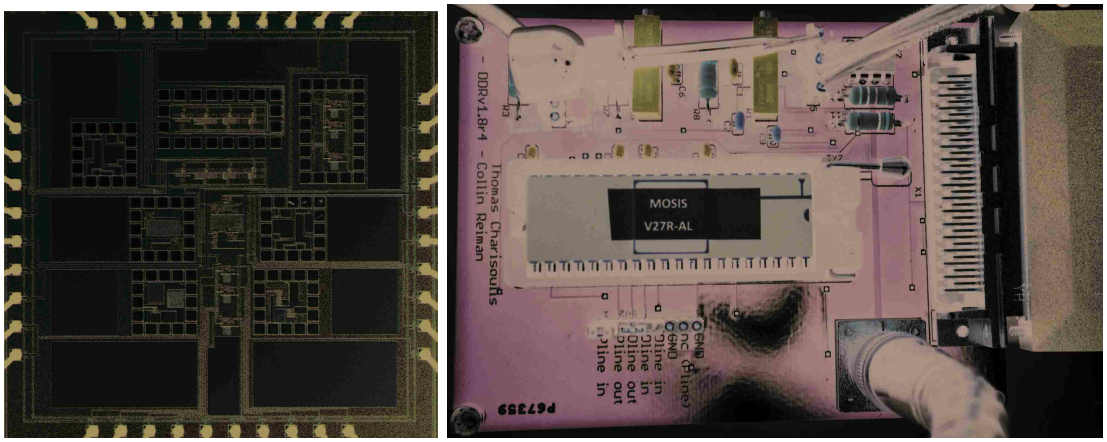


Figure 6.4: Pixel Current Mirrors for accurate pixel current measurements.

to a 10x or 100x oscilloscope probe to measure the voltage output which is directly related to the current flowing through the pixel under measurement.

The measuring scheme may vary, depending on the level of detail required. Generally the observation of the transient might be necessary, therefore if all the Msw transistors have exactly the same waveforms in phase, frequency and duty cycle as the Add transistors, the output will include the transient. However, sometimes the need for very accurate steady state pixel measurement might be desirable, therefore the pixel could be measured only when the respective Add switch has finished its programming cycle. Naturally, one pixel can be monitored continuously just by



(a) (b)

Figure 6.5: (a) Picture of the single crystal silicon fabricated driver for 1 column with 3 pixels and (b) a picture of the setup to extract the low current measurements.

having Msw on the entire programming cycle; this method enables measurements of the pixel to describe its behavior during the tho different sensing and programming cycles [1].

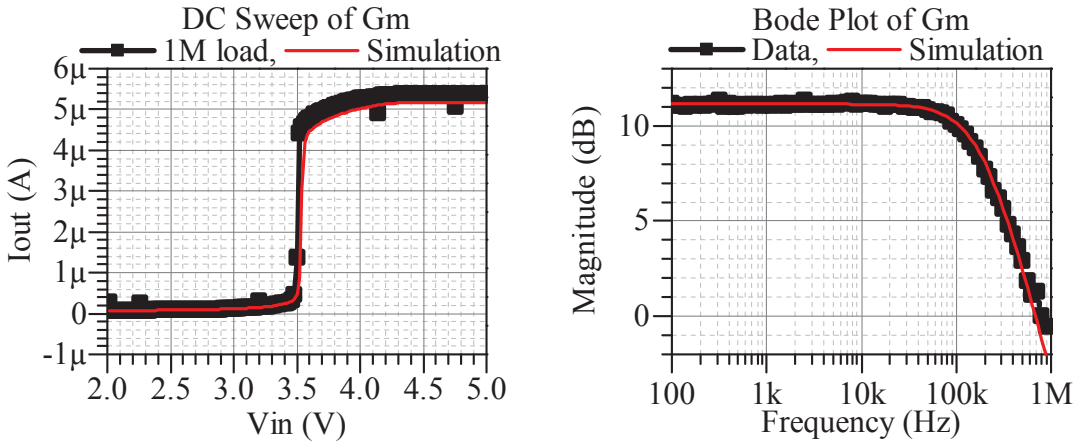
For measuring the pixel without perturbing the feedback loop, separate current mirrors copy the current flowing through the pixel to a separate output measure line connected to the buffer interfacing with the instrumentation amplifiers. Switches are connected in series with the current mirror outputs that enable selective current measurements to be conducted during any time slot of the circuits operation. This enables sampling of the pixel current during the different stages of operation such as the timeslots prior, during or after the addressing and the programming of the pixel takes place. This setup, depicted in Fig. 6.4, is used only for the extraction of accurate measurements of the pixel current, and it is not in any way connected to the overall feedback loop supplying the 2-transistor 1-capacitor pixel circuit. The only effect that it has in the overall circuits operation is that it loads down the gates of the pixel with the extra capacitance that comes from the current mirror transistors gates tied to the node connected at the gates of the Mpixel transistors and Ci capacitors

as shown in Fig. 6.4. A photo-micrograph of the MOSIS fabricated pixel column driver is presented in Fig. 6.5(a). A picture of the experimental setup is shown in Fig. 6.5(b).

6.2 OPAMP and OTA Designs with AC and DC sweeps

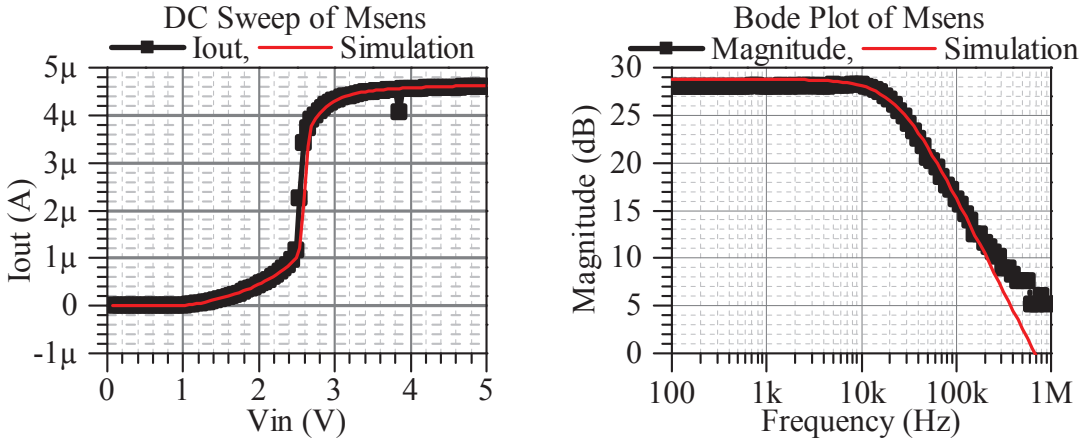
In section 5.6.1, amplifiers Msens as well as the current buffer OTA in figures 5.15 and 6.4 respectively are topologically as well as physically identical. For the purpose of this measurement for the transconductance amplifier named Gm, whose block diagram is shown in figure 6.1 and the transistor level design is shown in 5.15, the Vcol terminal is set to Vcc/2.

In figures 6.6 and 6.7 the reader can easily observe that the simulations are very close to the real fabricated circuits, especially under the isolation modifications the amplifiers underwent, in order to shield them against noise from the digital circuitry and shot noise from the substrate.



(a) (b)

Figure 6.6: (a) DC sweep and (b) Bode Plot of Gm OTA.



(a) (b)

Figure 6.7: (a) DC sweep and (b) Bode Plot of Msens OTA.

Chapter 7

Applications of Measurement Loops to Sensor Arrays

7.1 Introduction

IN this chapter, applications for sensors utilizing measurement loops is presented. Sensor arrays are similar to display arrays, comprised of pixels including a single sensing element and a switching element for readout purposes. The sensing element is implemented in multiple ways using passive components such as capacitors etc.. In a normal setup, the sensors are addressed similarly to a display and can be read-out sequentially or in parallel.

Normally, for better read-out, the sensor array outputs are applied to the inputs of buffer circuits to strengthen their signals. The output signal of these sensors is comprised of a very large DC component and a very small delta difference. The DC component is the background measurement and the small delta difference is

the measured signal of interest, since in most applications the background signal is known. Sensing the small delta difference many times is proved to be hard if not impossible and it is the reason why arrays of sensors are deployed. These arrays average the small signals, better identifying the large DC components and separate them from the small delta values of interest.

As presented in chapter 2, the fine and coarse sensing technique can be immediately applied in this case as well. Moreover, these sensors also suffer from degradation of their pixels circuits with time and this is another area where an external current measuring feedback loop is applied to provide better readout for the small delta output values of the sensors.

Many approaches have been invented recently for sensing various gases/odors and vapors. One of the most important requirements for compact sensing is small size, therefore the combined use of novel materials sensitive to various gases interacting with solid state electronics becomes mandatory for producing accurate electrical signal output for measurement readout. Moreover, materials interacting differently with multiple gases are required for higher accuracy measurements of different types of gas mixes. Carbon and Graphene are among the most popular of those materials, including Silicon that is always required for the electronics interface.

Examples of such sensing solid-state elements include graphene-silicon interface heteroxtructures [36–38], where transistor and schottky diode devices are built specifically for sensing certain gases and vapors. These proposed devices show excellent repeatability of measurements as well as moderate speed of measurement reiteration but their accuracy of 10ppm and their inability to be deployed with the same sensitivity for multiple gases limits their performance in some sensor applications.

Carbon in the form of Carbon nano-Tubes (CNTs) has also received a lot atten-

tion in recent years due to their small size, immediate application in industrial and scientific equipment as well as due to their low cost and ease of fabrication [39, 40]. The use of CNTs varies in form; for example in [39] a minaturized gas ionization sensor is described, where the CNTs are used as electrodes to measure the current discharge between them for different gases and vapors, whereas in [40] CNTs were investigated as resistive gas sensor Thin Films for sub-ppm NO_2 gas detection. Both of these approaches excellent measurement repeatability and reiteration speed, but there also exist impracticalities such as in the case of [39] where the use of voltages in the triple digits is employed and in case of [40] where the sensor is specifically fabricated for measuring one specific type of gas only. CNTs have also been used on top of a pair of inter-digitated electrodes (IDEs) as the gas sensing element and have been utilized for the detection of different gases and vapors. Based on previous research, presented in [41–43] the principle behind these gas sensors is based on the change in resistivity of the CNTs, when they are exposed to specific gases and vapors.

In all the sensors of the work mentioned above separate wiring is utilized for measuring the resistance and conductance change if each of the active (graphene-silicon interface) or passive (CNTs) sensor sites thus limiting the number of sensing pixels utilized within a compact platform. Deploying micro-scale gas sensors with a large number of sensing sites is very versatile and can benefit many diverse applications such as incorporation in portable hand-held devices or in places that is physically hard to monitor. A novel active addressing system is proposed in this paper that enables the averaging of a plethora of measurements from multiple sensor pixel sites and this new approach can be integrated with minor changes into all of the above sensing schemes.[1]

[1]This research was sponsored by the National Aeronautics and Space Administration via an interagency agreement with US Department of Homeland Security

The addressing method will be presented and a simple model for the LTPS TFTs and P-i-N diodes used in this method will be described and used to simulate the proposed design. Following, the fabrication of the proposed systems is described and the sensor measurements supporting our simulated data and method are presented.

7.2 Driving schemes of the proposed setup

7.2.1 Passive Arrays

Various sensor arrays 8x8 and 16x16 are investigated; the circuit schematic of an 8x8 array is shown in fig. 7.1. In order for the proposed system to isolate a specific sensor site and measure its resistance value, a diode has been placed in series with the CNT (resistive element as shown in fig. 7.1). One of the X inputs is chosen through a multiplexer circuit (MUX) and a constant current source is then applied at that terminal. One of the Y outputs is chosen through a de-multiplexer (DMUX) switch to be at low potential, providing a path for the current to flow through. The voltage then is measured across the active X - Y terminals, thus since the current is known and constant, a value for the resistance is obtained.

In the case of the simple 8x8 arrays, the MUX and DMUX switches are a system of relay switches external to the sensor and not included in the layout of the proposed setup, as opposed to the 16x16 array where three different driving schemes are explored and presented. This setup is mostly used as a simple sensor system in order to calibrate the equipment against the on series resistance Rs within each diode used to isolate a specific pixel under measurement. This configuration is also useful for observing the effect of the leakage current of the non-addressed diodes by setting one of the Y columns to a high potential, grounding all the X lines and

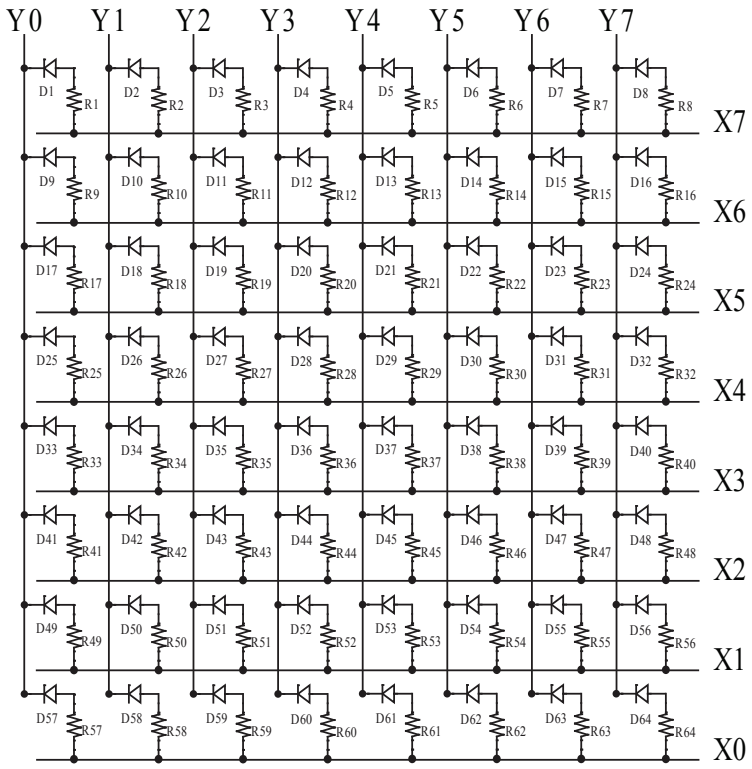


Figure 7.1: Figure 1. The 8x8 schematic diagram. A similar topology is used as well for the 12x12 arrays.

measuring the current flowing through all the diodes connected to that column. This measurement utilized to characterize the inaccuracies in the active setups presented in later sections.

7.2.2 Active Array Addressing Method I

One of the two driving techniques is to separate the 16x16 array into 8x8 arrays through the use of Low Temperature Poly-Silicon (LTPS) Thin Film Transistors. These TFTs are used as switches where their gates are all connected together in two separate groups of eight, horizontally as well as vertically producing four wires that can be used to separate the 16x16 array in four smaller 8x8 arrays as shown in fig. 7.2. In this case external MUX and DMUX switches are used externally as well, as previously described in section 7.2.1 to access the smaller 8x8 arrays and measure the resistance across their pixels. Moreover an external controller attached to all the inputs (XswA,XswB,YswA,YswB) is in sync with the MUX and DMUX switches, facilitating the addressing of the sub-arrays.

Note that the sensor impedance measured with this configuration is affected by the series on resistance of the diode and the TFT. The use of the passive setup as described in section 7.2.1 enables the calibration of the Data Acquisition instruments against variations in the on resistance of the diodes. Standalone Low Temperature Poly-Silicon TFTs are also fabricated separately on the same wafer for the ease of characterization of the transistor's on resistance. All the data are analytically presented in the modeling section of this paper.

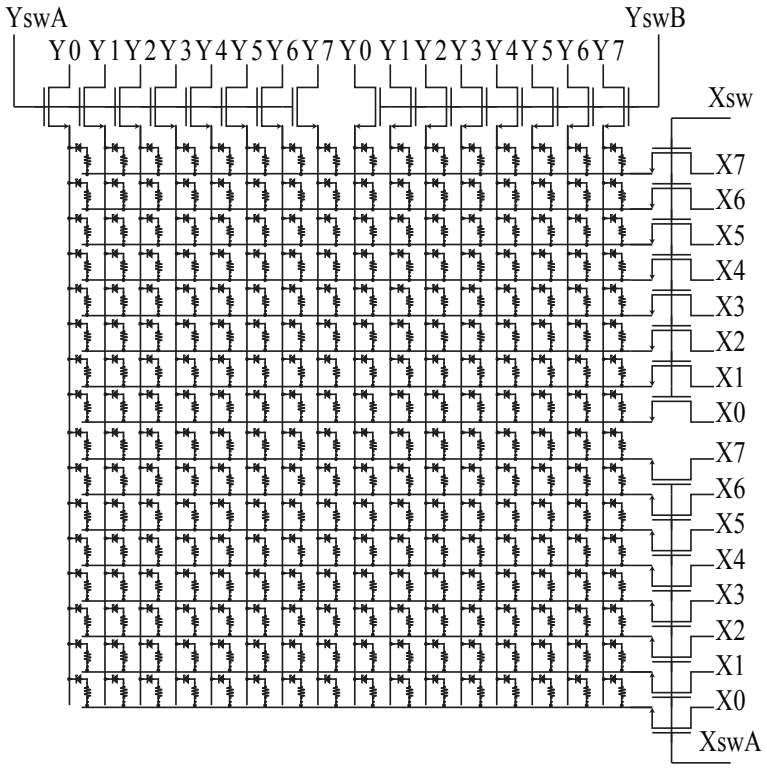


Figure 7.2: The 16x16 schematic including the two vertical groups of the switch transistors.

7.2.3 Active Array Addressing Method II

The other driving technique presented in this paper has the previously external MUX and DMUX circuits integrated on the periphery of the sensor. Moreover some simple digital circuitry is used in order to carry the current from the selected column through the addressed pixel and ground it through the selected row. In order to visualize and better explain this approach a simple schematic for one pixel is presented in fig. 7.3. The lines named Y line HIGH and X line Low are the power supplies connected to the logic gates as well as the inverters, Current line and Line Lo are the lines connected to the external current source and Y0 Y3 as well as X0 X3 are the control bits. When the bits X0 X3 are logic ones, the output of the NAND gate on the right side is at low potential thus the PMOS transistor that has its gate connected to the output of the NAND gate is ON. Inversely, if Y0 Y3 are logic zeros, the output of the NOR logic gate is at high potential, therefore the NMOS transistor that follows its gate connected to the output of the NOR logic gate is ON. A path is formed between the Current Line, the PMOS, the resistor, the diode and the NMOS towards Line Lo where the current source is applied externally. The voltage is measured across the Current Line and Line Lo terminals and the resistance is derived using Ohms Law. Therefore by using two separate four Bit Binary Counters providing the X and Y control signals the IDEs in all the pixels of the 16x16 array are scanned and measured individually as shown in fig. 7.4.

Using this method there is a large offset in the voltage measured across the two terminals where the current is applied, which translates into a large resistance that is measured in series with the resistor of interest due to the ON resistance of the NMOS and the PMOS transistors. The sensing resistor in this setup has a value of up to 4 orders of magnitude larger than the on resistance of the Poly-Silicon PMOS

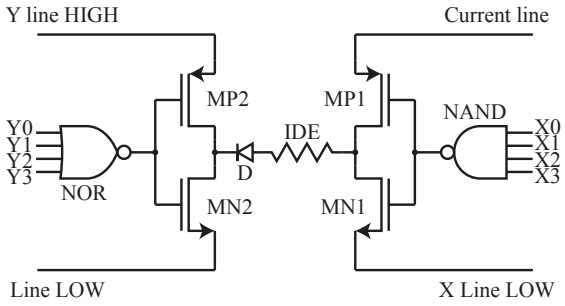


Figure 7.3: A simple schematic illustrating the addressing and measurement of an individual pixel.

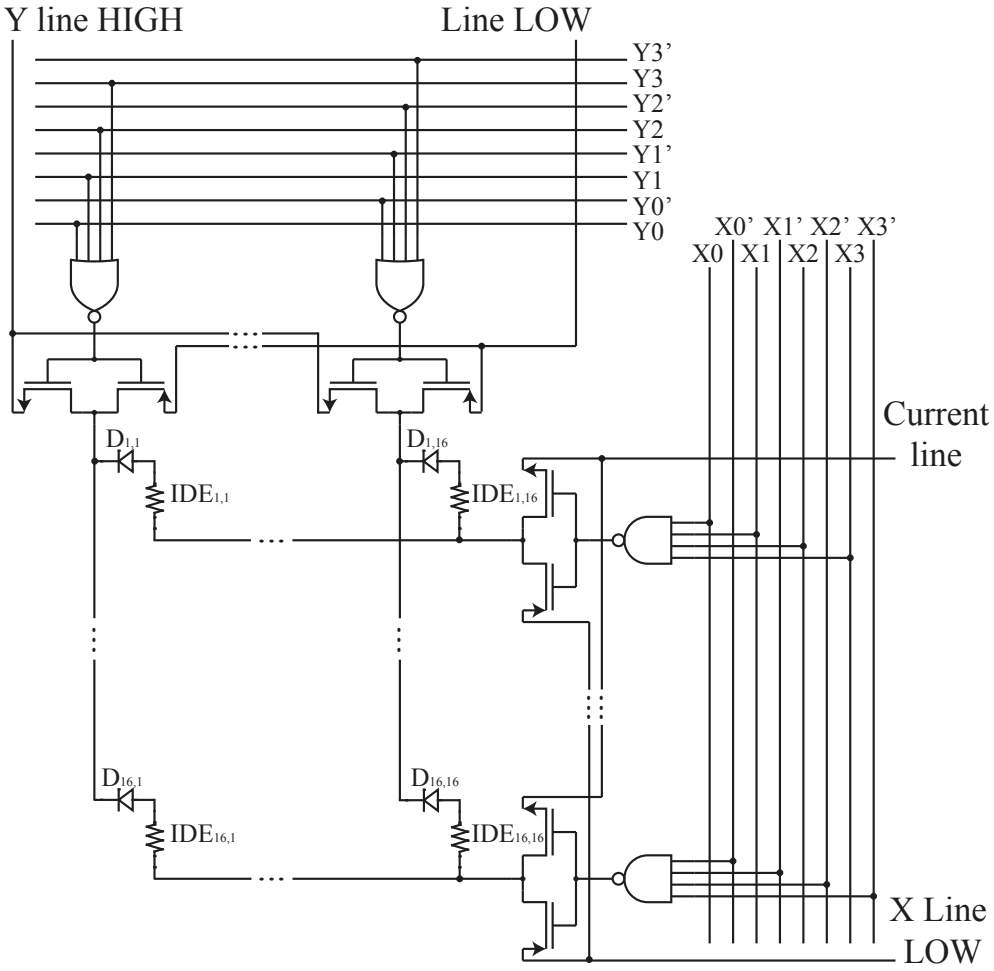


Figure 7.4: A schematic representation of the array with the fully integrated drivers. Note that Y0 Y3 and X0 X3 will be connected to two external binary counters providing the control Signals. Y line HIGH and X line LOW are connected to the power supplies of the driver. Current line and Line LOW are connected to an external current source.

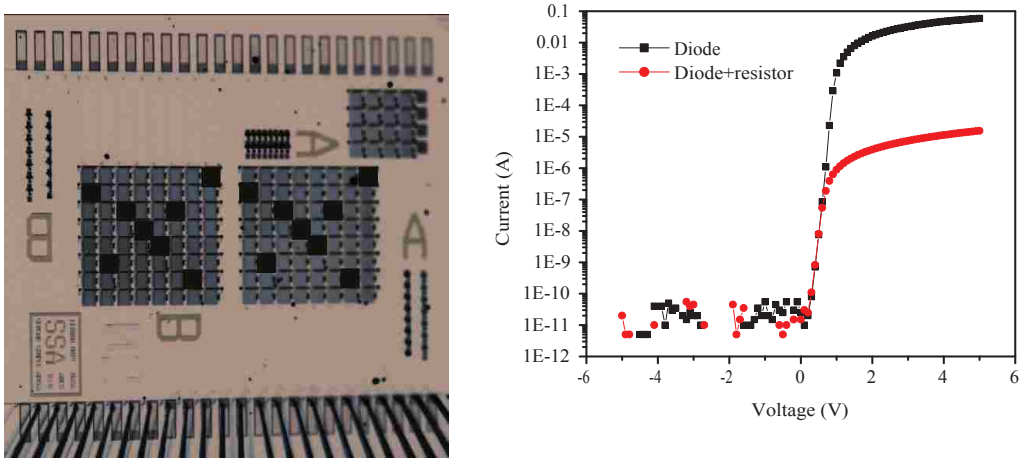
and NMOS transistors thus the decrease in sensitivity is reduced only by 0.1%. Also during the gas sensing measurement only the resistor difference R is needed in order to derive the gas concentrations, therefore this small limitation in sensitivity is not critical. A schematic of the entire active array is presented in fig. 7.4.

In similar setups where the sensing element is a heterojunction structure, the series resistance represented in this schematic by the Interdigitated Electrodes (the sensing element in this case), has to be up to 4 orders of magnitude lower in order to enable accurate sensing of the change in the transconductance due to various gases.

7.3 Device fabrication and system verification

All the active elements in the previous setups were implemented both with SOI and LTPS TFT technologies. The diodes that are part of the active sensing element in each pixel were fabricated with these technologies and have very low noise [44], which would further increase the sensitivity of the resistance change in the measured pixel. After fabrication and Before the CNT coating, the IDEs are open circuits. In order to facilitate the verification process, test resistors connected to the X lines before the diodes in parallel with the IDEs were designed during layout in the following pixels of each 8x8 array for example: (8,8), (7,1), (6,6), (5,3), (4,4), (3,5), (2,2), (1,7) shown in fig. 7.5(a). In all the 8x8, 12x12 and 16x16 arrays some random diodes are probed and measured in two separate ways. A diode is first measured, without and then with the test resistor in series by probing directly the pixels. A representation of the resulting I V characteristics is shown in fig. 7.5(b).

Following the procedure described in Sec. II-A, an entire 8x8 array is measured, and only the pixels with the test resistors attached to them (highlighted with red in

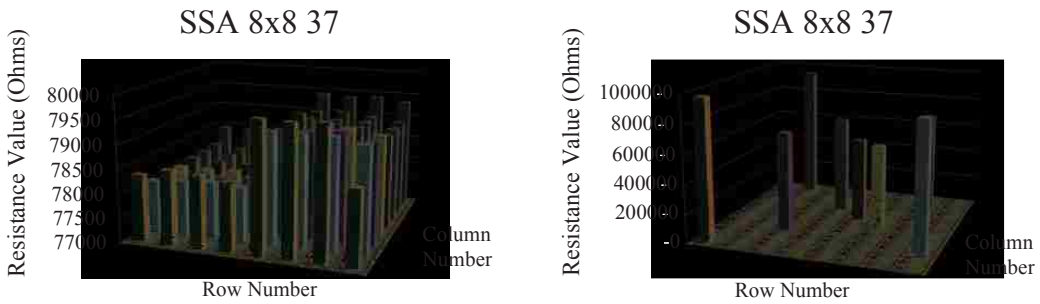


(a) Test resistor locations

(b) Diode I-V curves

Figure 7.5: (a) Location of test resistors in the array and (b) Diode measurement results: The dark curve presents the I-V characteristic curve of the diode. The light curve presents the IV characteristic curve or the diode in series with the resistor that make up the sensing element.

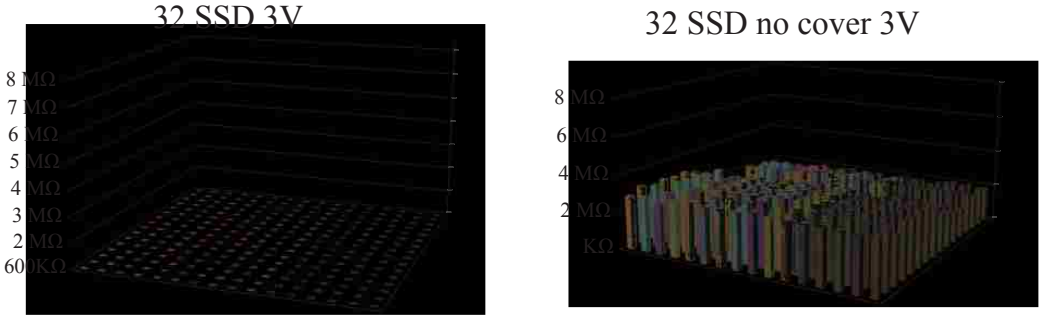
fig. 7.5(a) present a resistance within our measured range of up to 100MΩ; the rest of the pixels are out of range, and as expected are open circuits (fig. 7.6(a)). Using this measuring procedure is helpful for detecting only line defects that would render an entire column or row of an array inoperable. Since it is mandatory to verify that every active component on these sensors is operational, all of the fabricated 8x8 and 16x16 arrays were coated with a PEDOT:PSS solution before the final CNT coating. The PEDOT:PSS used is conductive [45], and it shorts the IDEs, providing a path to carry the current from X to Y terminals. All the 8x8 12x12 and 16x16 sensors are measured again after being coated with the solution. A sample of the gathered data is presented in figures 7.6 and 7.7.



(a) PDOT covered array

(b) array with PDOT removed

Figure 7.6: IDE resistance Measurements for an 8x8 array implemented on an SOI wafer (a) coated with PEDOT:PSS and (b) after the PEDOT:PSS solution was removed.



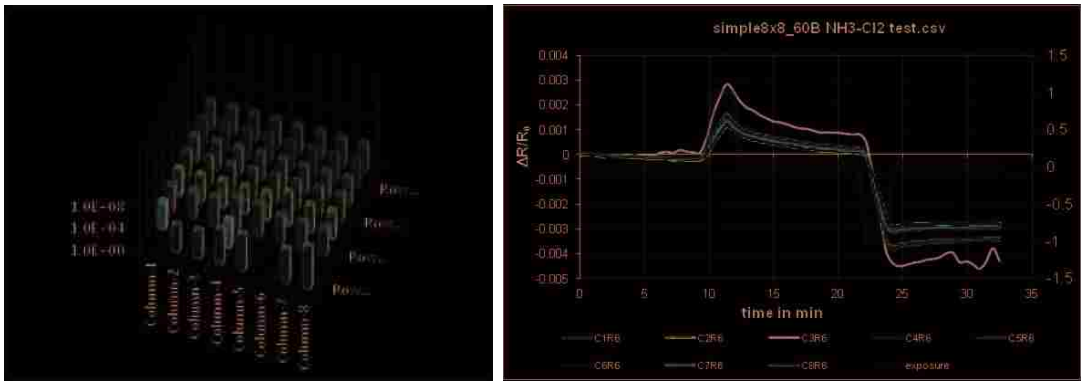
(a) PDOT covered array

(b) array with PDOT removed

Figure 7.7: IDE resistance Measurements for a 16x16 array implemented on a Quartz glass wafer (a) coated with PEDOT:PSS and (b) after the PEDOT:PSS solution was removed.

7.4 Gas Concentration measurements

An 8x8 sensor array chip was used for CNT coating as a real chemical sensor array. A carboxylic acid group modified carbon nanotube (CNT-COOH) was deposited onto all 64 sensor-channels in the array. The base resistances of these sensing channels have been measured and presented in fig. 7.8(a). Windex and Bleach were used as ammonia (NH_3) and chlorine (Cl_2) vapor sources as we used in a smartphone-sensor



(a) Base resistance (b) Time diagram

Figure 7.8: 7.8(a) Base resistances of 64 sensors with CNT-COOH coatings and 7.8(b) NH_3 and Cl_2 test. The gray line in the plot corresponding to right Y axis indicates the chemical exposures. Positive 1 stands for NH3 exposure and negative 1 stands for Cl2 exposure. Because all the response curves are in the same shape, only 8 response curves (8/64) are shown here.

demo in order to further compare the results. We recorded the base resistance of the arrays in a normal room air mixture for 10 minutes as baselines, and then followed by 2 minutes exposure to Windex that is in a 25 ml vial. The concentration of ammonia in Windex is about 30ppm. After NH3 exposure the chip is in air recorded another 10 min resistances as baseline, then followed by a 2 minutes exposure to Bleach that Cl2 concentration in it is about 2ppm. The sensor responses shown in fig. 7.8(b) are very similar to those from the traditional SWCNT IDE sensor array without diodes [42].

7.5 Conclusions

A novel CNT gas sensor array approach is presented, which increases the measurement sensitivity of various gases and vapors due to the data gathered with increased resolution on a specific site. Furthermore the size of the proposed sensor arrays is

reduced as opposed to the individually addressed ones due to the novel addressing approach descried in this paper for the 16x16 arrays. These sensors were fabricated both with SOI and LTPS TFT technologies and covered with a carboxylic acid group modified carbon nanotube (CNT-COOH). Measurements of ammonia (30ppm) and chlorine vapors (2ppm) were displayed in figure 7.8 with positive response to Amonnia exposure and negative response to chlorine exposure.

Chapter 8

Conlcusion

8.1 Introduction

8.1.1 LTV Systems

IN this dissertation, the theory behind Linear, Time Varying, first order control loops has been partially formulated. It was also proven that a direct application lies in the field of displays, where the basic principles of Analog Circuit Design can be applied in conjunction with a new and unique current driving scheme to produce a novel feedback architecture. Moreover, part of this dissertation was focused on all of the aspects concerning the invention, design, fabrication and characterization of a novel backplane architecture for 2-Transistor 1-Capacitor Active-Matrix OLED displays, as well as practical applications of the aforementioned control loops to sensor arrays.

Previously reported approaches in driving such displays have been categorized in three groups and representative examples have been illustrated and analyzed from

each particular group. In addition, all those examples have been compared against each-other to pinpoint any advantages and disadvantages, while group III (Examples of Digital/Analog Hybrid Compensation Circuits) in chapter 3 was identified as the most likely group, versatile enough to allow the implementation of the theoretical principles described in this dissertation.

Specifically, in chapter 2 the theory on how the error output can converge faster to the steady state value was formulated for the single loop case, having time varying gains A(t). Although solving the differential equations might prove impossible, there are cases where the gain functions of time can be chosen in such a way to allow for an analytical solution to exist. However, when the loops become higher than the first order, the problem becomes even more difficult. For example, combining the theory formulated in chapter 2 and equation 5.5 from chapter 5 one can see that the state matrix in the s-domain is not just a simple constant, but rather a more complicated matrix dependent on the frequencies of that domain.

Since the poles are directly dependent on the gains of amplifiers Reg and A1, they can be easily controlled by varying the gains of those amplifiers, making them functions of time. One could then theorize that a specific gain function, having a sinusoidal periodic waveform with the opposite polarity than the transient and with time constants within the range of the error output's total transient response time, could enable the system to converge to the steady state value faster. This, however, is the case only if those gain functions are multiplied by a constant factor decreasing with time within the transient response time window (equations 8.1 or 8.2).

$$A1 = Ae^{-at}cos(\omega_\alpha t) \tag{8.1}$$

$$Gm = Be^{-bt}cos(\omega_\beta t) \tag{8.2}$$

8.1.2 Noise and Loops for sensor Applications

Another area of interest is noise, as discussed in chapter 6. In that chapter the various effects of thermal and shot noise on the performance of the circuit have been presented and analyzed. It is clear that the noise phenomena here, as in every analog IC chip, play a very important role in the degradation of the circuit's behavior. Previously, in the same chapter, some of the techniques mitigating some of the substrate's noise into the critical nodes have been described as well as their implementation in a new circuit. Additionally, as it was shown, utilizing external FPGA driving cards to provide the switching as well as linear power regulators to provide noiseless power to the chip has further decreased the noise level in the measured pixel currents.

In chapter 7, some simplified measuring loops for sensor applications have been described and analyzed here. Various implementations of these measuring loops have been implemented into functional sensors utilizing a LTPS backplane and through measurements it was proven that their accuracy is increased to 2ppm for various gases and vapors.

8.2 Future Research Recommendations

Some ideas for follow-up research in this field are suggested below, based on the formulated theory as well as the data presented in this dissertation.

1. Application of Linear Time Varying theory to Current feedback circuit: A lot of effort put into this field in formulating the general theory by Tsakalis and Ioannou et. al. in [46–48], while people like Frey et. al. in [49] have been applying almost all of the basic principles in practical designs. In the data presented in the previous chapters, knowing the rough form of the gains and what the output of the circuit should look like, one could work backwards to find an analytical solution of the output of the circuit and the exact gain equations. After these functions are produced, they can be included in the circuit schematic as function generator directly attached to the Vbias1 and Vbias2 inputs of the circuit shown in figure 5.15. This can enable the proposed current feedback loop to operate at higher speeds, minimizing the total error at the output with less active components in its feedback path.

2. Noise Isolation: In our investigation of the noise impact to the critical nodes of the circuit we have discovered a direct relationship between the quality of layout and the quality of our output. Moreover, it has been discovered that the circuit is extremely sensitive to noise coupled from external noise sources, therefore work on applying better isolation techniques to the layout are beneficial to the accuracy of the control loop. Moreover an integrated driver interfacing directly with an equivalent display load would provide the best data, pushing the limits of the circuit's performance to new levels.

3. LED to LED uniformity verification: In industry, there is always a form of

visual verification of the end-product. Specifically, by using external sensors in a dark room its individual LED's brightness is measured and analyzed as a function of the driven current. In our case, since a display panel with the exact specifications is not available "off the shelf", a an array of micro-LEDs, such as the 0404 by QuasarBrite, could used interfacing with a slightly altered version of the previously proposed driver (to accommodate the currents of operation of those LEDs), to help further prove the concept. Moreover, utilizing a light sensor and a dark box, the curve of brightness versus the currents can be extracted and compared to multiple LEDs of the same color, in a similar column simulation as described in chapter 5 to include the parasitics of that driver.

4. Multiple loops for continuous and/or switching modes of operation: The sensitivity of the driver can further be improved with the dimming principle of driving an LED hard for an amount of time much smaller than the frame time (e.g. the LED is on only while being addressed). Chapter 5 presents how the programming loop, comprised of amplifiers A1, Gm and the programmed pixel, is decoupled from the Regulating loop. Using the same principle there, a third loop designed to drive larger currents (e.g. 1μA to 20μA) could be wrapped around the Node of the Column (NC). This loop will have a data programming current source that turns off slightly before the addressing of the pixel stops, resetting the pixel. Assuming that the total frame time for a 60Hz display is 16.67ms, the addressing time is 16μsec if the column has 1000 pixels. Driving the pixel with 20μA, therefore, an effective current of 20nA with the same equivalent brightness is observed, due to the eye's integrating ability. With careful design, this can further push the accuracy of the system to even sub nano-Ampere levels!

5. All new generation of all-NMOS system for IGZO backplanes: As presented

by Tsividis et. al. [50], it is possible to produce all-NMOS circuits such as differential pairs and Transconductance amplifiers. Moreover, coupled with the modern marvels of the Gm/Id method, one can accurately extract and pinpoint the operating point of any transistor in the circuit utilizing simple transfer and output curves of the transistors for different bias levels within the power lines. Both of the aforementioned two techniques can be combined to design, fabricate and characterize a new version of the proposed display driver that might have the possibility to push the display industry into a new era!

Chapter 9

Appendices

9.0.1 Appendix I: Modeling Approach for an all-NMOS driver circuitry

Finally, in a recent joint effort with the University of Thessaloniki, Greece, a novel potential based model appropriate for fast and accurate simulations has been proposed in [51]. The goal was to analytically model the current through the channel of the NMOS transistor and present the capacitances calculated in closed form. My research was also aimed to uncover potential applications in the field of displays, with all NMOS circuitry.

In the proposed model, the free charge density in the channel of an IGZO transistor is extracted by using a Gaussian distribution to calculate the density of states and approximate the surface potential, and it is described by equation 9.1

$$n_{free,fb} = \frac{I_d^2}{\epsilon_S \ kT\mu^2(W/L)^2V_d^2} \tag{9.1}$$

In [51] the surface potential is separated in two regions, for weak electrical fields and for strong electrical fields. Those fields are presented in equations 9.2 and 9.3

$$\phi_{S1} = V_g - V_{fb} - 2\frac{kT_{t1}}{q}q_{S1} \tag{9.2}$$

$$\phi_{S1} = V_g - V_{fb} - 2\frac{kT_{t2}}{q}q_{S2} \tag{9.3}$$

where:

$$q_{S1} = W_0\left[exp\left(\frac{q(V_g - V_t - V)}{2kT_{t1}}\right)\right] \tag{9.4}$$

$$q_{S2} = W_0\left[exp\left(\frac{q(V_g - V_on - V)}{2kT_{t2}}\right)\right] \tag{9.5}$$

$$V_{on} = V_{fb} + \phi_{F0} - \frac{2kTt2}{q}ln\left(\frac{q}{C_{ox}}\sqrt{\frac{\epsilon_S N_{t2}}{2kT_{t2}}}\right) \tag{9.6}$$

And instead of expressing the current analytically based on the surface potentials, it is expressed in terms of the effective charge densities as shown in equation 9.7 for below threshold and 9.8 for the second region with the strong vertical fields.

$$I_{d1} = 4\frac{W}{L}\mu C_{ox}\left(\frac{kT_{t1}}{q}\right)^2 (q_{ss1} - q_{sd1}) \tag{9.7}$$

$$I_{d2} = 2\frac{W}{L}\mu C_{ox}\left(\frac{kT_{t2}}{q}\right)^2 \left[(q_{ss2}^2 - q_{sd2}^2) + 2m(q'_{ss2} - q'_{sd2})\right] \tag{9.8}$$

where

$$q_{ss1} = W_0\left[exp\left(\frac{q(V_g - V_t)}{2kT_{t1}}\right)\right] \tag{9.9}$$

$$q_{sd1} = W_0\left[exp\left(\frac{q(V_g - V_t - V_d)}{2kT_{t1}}\right)\right] \tag{9.10}$$

$$q_{ss2} = W_0\left[exp\left(\frac{q(V_g - V_{on})}{2kT_{t2}}\right)\right] \tag{9.11}$$

$$q_{sd2} = W_0\left[exp\left(\frac{q(V_g - V_{on} - V_d)}{2kT_{t2}}\right)\right] \tag{9.12}$$

$$q'_{ss2} = W_0\left[exp\left(\frac{q(V_g - V_{on})}{2mkT_{t2}}\right)\right] \tag{9.13}$$

$$q'_{sd2} = W_0\left[exp\left(\frac{q(V_g - V_{on} - V_d)}{2mkT_{t2}}\right)\right] \tag{9.14}$$

Then, equation 9.15 is used as an interpolation function that matches the limiting behavior in the regions of weak and strong vertical fields, to find the compact drain current model.

$$I_d = \frac{I_{d1} \cdot I_{d2}}{(I_{d1}^{1/m} + I_{d2}^{1/m})^m} \tag{9.15}$$

```
1  // VerilogA for Thomas, IGZO_NMOS, veriloga
2
3  `include "constants.vams"
4  `include "disciplines.vams"
5  `define PHY_EPSOX   (3.9 * `P_EPS0)
6
7
8  module bhv_NMOS(d,g,s);
9
10 parameter real Teff1=1216.84    from (0:inf);
11 parameter real Teff2=3671.09    from (0:inf);
12 parameter real uo=7.3       from (0:inf);
13 parameter real Vt=0.3       from [-5:inf);
14 parameter real Von=2.03     from (-inf:inf);
15 parameter real m=0.5        from [0:inf);
16 parameter real b1=0.03      from [0:inf);
17 parameter real b2=0     from [0:inf);
18 parameter real tox=100n     from (1n:10u);
19 parameter real W=16u        from (0.5u:1000u];
20 parameter real L=10u        from (0.5u:1000u];
21 parameter real Ioff=1p      from [0.001p:inf);
22
```

```
23 real Q,Q1,Q2,qu1,qu2,qu,qu1Vs,qu2Vs,Q1Vs,Q2Vs,QVs,quVs, u, Coxp, ...
       QS, QD, QG, ig, id, is, i1, i2, i3, i4, i5, i6, kTt1, kTt2, ...
       Ids, CDD, CDG, CDS, CGD, CGG, CGS, CSD, CSG, CSS, gm, gds, ...
       gmovid;
24
25 inout d,g,s;
26 electrical d,g,s,a;
27
28 analog function real lambert;
29 input x;
30 real x;
31 begin
32 lambert=ln(1+x)*(1-(ln(1+ln(1+x))/(2+ln(1+x))));
33 end
34 endfunction //lambert
35
36 analog begin
37 //Parameter Dependent Variables and Physical constants
38 Coxp= `PHY_EPSOX/tox;
39 kTt1=`P_K*Teff1/`P_Q;
40 kTt2=`P_K*Teff2/`P_Q;
41
42 qu1  = exp((V(g,s)-Vt-V(d,s))/2/kTt1);
43 qu2  = lambert(exp((V(g,s)-Von-V(d,s))/2/kTt2));
44 Q1   = Coxp*kTt1*qu1;
45 Q2   = Coxp*kTt2*qu2;
46 Q    = Q1*Q2/pow((pow(Q1,m)+pow(Q2,m)),1/m);
47 qu   = qu1*qu2/pow((pow(qu1,m)+pow(qu2,m)),1/m);
48
49 qu1Vs = exp((V(g,s)-Vt)/2/kTt1);
50 qu2Vs = lambert(exp((V(g,s)-Von)/2/kTt2));
51 Q1Vs  = Coxp*kTt1*qu1Vs;
```

```
52 Q2Vs   = Coxp*kTt2*qu2Vs;
53 QVs    = Q1Vs*Q2Vs/pow((pow(Q1Vs,m)+pow(Q2Vs,m)),1/m);
54 quVs   = qu1Vs*qu2Vs/pow((pow(qu1Vs,m)+pow(qu2Vs,m)),1/m);
55
56 u=uo*(1+b2*(V(d,s) -2*((pow(QVs,2)/quVs ...
       -pow(Q,2)/qu)/kTt2/pow(Coxp,2)))) ...
       /(1-b1*(pow(QVs,2)/quVs)/(kTt2*pow(Coxp,2)));
57
58 I(d,s) <+ 1e-4*2*W/L*u* ((pow(pow(QVs,2)/quVs,2) ...
       -pow(pow(Q,2)/qu,2)) /pow(Coxp,3)/pow(kTt2,2) ...
       +2/Coxp*(pow(QVs,2)/quVs-pow(Q,2)/qu))+Ioff;
59
60 Ids      = 1e-4*2*W/L*u* ((pow(pow(QVs,2)/quVs,2) ...
       -pow(pow(Q,2)/qu,2)) /pow(Coxp,3)/pow(kTt2,2) ...
       +2/Coxp*(pow(QVs,2)/quVs-pow(Q,2)/qu))+Ioff;
61
62 //Charge calculation
63 QG = W*W*u/6/Ids/Coxp*(3*(QVs*QVs*QVs/quVs -Q*Q*Q/qu) ...
       +2*(QVs*QVs*QVs -Q*Q*Q));
64
65 QD = -2*W*W*W*u*u/L/Ids/Ids* ...
       (2*QVs*QVs*QVs*QVs*QVs/3/Coxp/Coxp/quVs/quVs ...
       +5*QVs*QVs*QVs*QVs*QVs/6/Coxp/Coxp/quVs ...
       +4*QVs*QVs*QVs*QVs*QVs/15/Coxp/Coxp ...
       -2*QVs*QVs*QVs*Q*Q/Coxp/Coxp/quVs/quVs ...
       -Coxp*Coxp*Coxp*Coxp*Coxp*QVs*QVs*QVs*Q*Q/Coxp/Coxp/quVs ...
       +4*Q*Q*Q*Q*Q/3/Coxp/Coxp/qu/qu ...
       -4*QVs*QVs*Q*Q*Q/3/Coxp/Coxp/quVs ...
       -2*QVs*QVs*Q*Q*Q/3/Coxp/Coxp +3*Q*Q*Q*Q*Q/2/Coxp/Coxp/qu ...
       +2*Q*Q*Q*Q*Q/5/Coxp/Coxp);
66
67 QS=-QG-QD;
```

```
68
69 // Transcapacitance Calculations
70 CDD = ddx(QD,V(d));
71 CDG = ddx(QD,V(g));
72 CDS = ddx(QD,V(s));
73 CGD = ddx(QG,V(d));
74 CGG = ddx(QG,V(g));
75 CGS = ddx(QG,V(s));
76 CSD = ddx(QS,V(d));
77 CSG = ddx(QS,V(g));
78 CSS = ddx(QS,V(s));
79
80 I(d,a) <+ CDD*ddt(V(d))+CDG*ddt(V(g))+CDS*ddt(V(s));
81 I(g,a) <+ CGD*ddt(V(d))+CGG*ddt(V(g))+CGS*ddt(V(s));
82 I(s,a) <+ CSD*ddt(V(d))+CSG*ddt(V(g))+CSS*ddt(V(s));
83
84 // For gmOvId
85 gm=ddx(Ids,V(g));
86 gmovid=ddx(Ids,V(g))/Ids;
87 gds=ddx(Ids,V(d));
88 end
89 endmodule
```

However the implementation of this method in a verilogA code has not been verified and no attempt has been made for implementing an analytical description of the trans-capacitances of the IGZO devices.

This part of the research intends on discovering a potential continuous model for the IGZO devices that sufficiently describes the complete operation of IGZO transistors. The goal is for this model to be compact and easily described by a computer code for simulations. This model will then be used in an attempt to

design and simulate a novel driver that can be later fabricated into a fully functional prototype.

Bibliography

[1] T. Charisoulis, D. Frey, and M. K. Hatalis, "Current feedback compensation circuit and method for 2T1C displays," *IEEE Transactions on Circuits and Systems*, vol. I, 2014.

[2] Ctesibius, "The water-thief," 265 BC.

[3] J. C. Maxwell, "On governors," *Proceedings of the Royal Society of London*, vol. 16, pp. 270–283, 1867.

[4] R. Kalman, "On the general theory of control systems," *IRE Transactions on Automatic Control*, vol. 4, no. 3, pp. 110–110, 1959.

[5] I. Horowitz, "Design of multiple-loop feedback control systems," *Automatic Control, IRE Transactions on*, vol. 7, no. 3, pp. 47–57, 1962. ID: 1.

[6] R. D. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *Power Electronics, IEEE Transactions on*, vol. PE-2, no. 2, pp. 109–124, 1987. ID: 1.

[7] T. Brody, F. C. Luo, Z. P. Szepesi, and D. H. Davies, "A 6 6-in 20-lpi electroluminescent display panel," *Electron Devices, IEEE Transactions on*, vol. 22, no. 9, pp. 739–748, 1975.

[8] H. J. In and O. K. Kwon, "Simple pixel structure using video data correction method for nonuniform electrical characteristics of polycrystalline silicon thin-film transistors and differential aging phenomenon of organic light-emitting diodes," *Japanese Journal of Applied Physics*, vol. 49, no. 3, p. 03CD04, 2010.

[9] H. J. In, K. H. Oh, I. Lee, D. H. Ryu, S. M. Choi, K. N. Kim, H. D. Kim, and O. K. Kwon, "An advanced external compensation system for active matrix organic light-emitting diode displays with poly-si thin-film transistor backplane," *Electron Devices, IEEE Transactions on*, vol. 57, no. 11, pp. 3012–3019, 2010.

[10] S. J. Ashtiani, G. R. Chaji, and A. Nathan, "Amoled pixel circuit with electronic compensation of luminance degradation," *Display Technology, Journal of*, vol. 3, no. 1, pp. 36–39, 2007.

[11] N. Fruehauf, P. Schalberger, M. Herrmann, and A. Vielwock, "Current mirror and current feedback driving of active matrix organic light emitting displays," in *Active-Matrix Flatpanel Displays and Devices (AM-FPD), 2012 19th International Workshop on*, pp. 277–280, 2012. ID: 1.

[12] C. L. Lin, C. C. Hung, S. K. Hsu, K. W. Chou, and C. D. Tu, "P-52: A new current programming pixel circuit for compensating luminance degradation of amoled," in *SID Symposium Digest of Technical Papers*, vol. 42, pp. 1292–1295, Wiley Online Library, 2012.

[13] J.-Y. Jeon, Y.-J. Jeon, Y.-S. Son, K.-C. Lee, H.-M. Lee, S.-C. Jung, K.-H. Lee, and G.-H. Cho, "A direct-type fast feedback current driver for medium- to large-size amoled displays," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pp. 174–604, 2008. ID: 1.

[14] A. Shin, B. Yoon, and M. Y. Sung, "A novel current driving method using organic tft pixel circuit for active-matrix oled," in *Microelectronics, 2007. ICM 2007. Internatonal Conference on*, pp. 413–416, IEEE, 2007.

[15] Y.-H. Tai, B.-T. Chen, Y.-J. Kuo, C.-C. Tsai, K.-Y. Chiang, Y.-J. Wei, and H.-C. Cheng, "A new pixel circuit for driving organic light-emitting diode with low temperature polycrystalline silicon thin-film transistors," *Display Technology, Journal of*, vol. 1, no. 1, pp. 100–104, 2005.

[16] S. Ono, K. Miwa, Y. Maekawa, and T. Tsujimura, "Vt compensation circuit for am oled displays composed of two tfts and one capacitor," *Electron Devices, IEEE Transactions on*, vol. 54, no. 3, pp. 462–467, 2007.

[17] D. Fish, N. Young, M. Childs, W. Steer, D. George, D. McCulloch, S. Godfrey, M. Trainer, M. Johnson, and A. Giraldo, "32.1: Invited paper: A comparison of pixel circuits for active matrix polymer/organic led displays," in *SID Symposium Digest of Technical Papers*, vol. 33, pp. 968–971, Wiley Online Library, 2002.

[18] C. L. Lin, T. T. Tsai, and Y. C. Chen, "A novel voltage-feedback pixel circuit for amoled displays," *Journal of Display Technology*, vol. 4, no. 1, pp. 54–60, 2008.

[19] J.-C. Goh, H.-J. Chung, J. Jang, and C.-H. Han, "A new pixel circuit for active matrix organic light emitting diodes," *Electron Device Letters, IEEE*, vol. 23, no. 9, pp. 544–546, 2002.

[20] D. Gagnot, H. Guermoud, and P. Le Roy, "Image display device and display device control method," July 29 2005. US Patent App. 11/658,944.

[21] M. N. Troccoli and M. K. Hatalis *Active matrix display and method*, 2013.

[22] M. N. Troccoli and M. K. Hatalis, "Active matrix display and method," Mar. 5 2013. US Patent 8,390,536.

[23] T. Tsujimura, "Amorphous/microcrystalline silicon thin film transistor characteristics for large size oled television driving," *Japanese journal of applied physics*, vol. 43, no. 8R, p. 5122, 2004.

[24] D. F. Thomas Charisoulis, Matias Troccoli and M. Hatalis, "Novel analog feedback current programming architecture compatible with 2-transistor 1-capacitor pixel for active matrix organic light-emitting diode displays," *Journal of Society for Information Display*, 2014.

[25] A. S. Sedra and K. C. Smith, *Microelectronic Circuits Revised Edition*. Oxford University Press, Inc., 2007.

[26] T. Charisoulis, D. Frey, and M. Hatalis, "Feedback architecture for uniform brightness in tft amoled displays," in *Photonics Conference (IPC), 2013 IEEE*, pp. 182–183, IEEE, 2013.

[27] T. Charisoulis, M. Troccoli, D. Frey, and M. K. Hatalis, "35.2: A new feedback current programming architecture for 2t1c amoled displays," in *SID Symposium Digest of Technical Papers*, vol. 44, pp. 465–468, Wiley Online Library, 2013.

[28] A. Jamshidi-Roudbari, S. A. Khan, and M. K. Hatalis, "Integrated full-bit shift register by low-temperature amorphous indium gallium zinc oxide thin-film transistors," *Electrochemical and Solid-State Letters*, vol. 14, no. 5, pp. J19–J21, 2011.

[29] P.-C. Kuo, A. Jamshidi-Roudbari, and M. Hatalis, "Electrical characteristics and mechanical limitation of polycrystalline silicon thin film transistor on steel foil under strain," *Journal of Applied Physics*, vol. 106, no. 11, p. 114502, 2009.

[30] H. Nakanotani, K. Masui, J. Nishide, T. Shibata, and C. Adachi, "Promising operational stability of high-efficiency organic light-emitting diodes based on thermally activated delayed fluorescence," *Scientific reports*, vol. 3, 2013.

[31] Z. Wang, M. Helander, J. Qiu, D. Puzzo, M. Greiner, Z. Hudson, S. Wang, Z. Liu, and Z. Lu, "Unlocking the full potential of organic light-emitting diodes on flexible plastic," *Nature Photonics*, vol. 5, no. 12, pp. 753–757, 2011.

[32] H. Meng, J. Luo, W. Wang, Z. Shi, Q. Niu, L. Dai, and G. Qin, "Top-emission organic light-emitting diode with a novel copper/graphene composite anode," *Advanced Functional Materials*, vol. 23, no. 26, pp. 3324–3328, 2013.

[33] M. C. Gather, A. Khnen, and K. Meerholz, "White organic light-emitting diodes," *Advanced Materials*, vol. 23, no. 2, pp. 233–248, 2011.

[34] R. Sarpeshkar, R. F. Lyon, and C. Mead, *A low-power wide-linear-range transconductance amplifier*, pp. 267–313. Neuromorphic systems engineering, Springer, 1998.

[35] G. Ferri and W. Sansen, "A rail-to-rail constant-g m low-voltage cmos operational transconductance amplifier," *Solid-State Circuits, IEEE Journal of*, vol. 32, no. 10, pp. 1563–1567, 1997.

[36] M. A. Uddin, A. K. Singh, T. S. Sudarshan, and G. Koley, "Functionalized graphene/silicon chemi-diode h2 sensor with tunable sensitivity," *Nanotechnology*, vol. 25, no. 12, p. 125501, 2014.

[37] A. Singh, M. Uddin, T. Sudarshan, and G. Koley, "Tunable reversebiased graphene/silicon heterojunction schottky diode sensor," *Small*, 2013.

[38] A. Singh, M. A. Uddin, T. Sudarshan, and G. Koley, "Gas sensing by graphene/silicon hetrostructure," in *Sensors, 2013 IEEE*, pp. 1–4, 2013. ID: 1.

[39] A. Modi, N. Koratkar, E. Lass, B. Wei, and P. M. Ajayan, "Miniaturized gas ionization sensors using carbon nanotubes," *Nature*, vol. 424, no. 6945, pp. 171–174, 2003.

[40] L. Valentini, I. Armentano, J. Kenny, C. Cantalini, L. Lozzi, and S. Santucci, "Sensors for sub-ppm no 2 gas detection based on carbon nanotube thin films," *Applied Physics Letters*, vol. 82, no. 6, pp. 961–963, 2003.

[41] J. Janata, *"Principles of Chemical Sensors"*. New York: Plenum, 1989.

[42] Y. L. AJing Li and M. Meyyappan, "Nano chemical sensors with polymer-coated carbon nanotubes," *sensors Journal, IEEE*, vol. 6, pp. 1047 – 1051, Oct. 2006.

[43] M. Cinke, J. Li, B. Chen, A. Cassell, L. Delzeit, J. Han, and M. Meyyappan, "Pore structure of raw and purified hipco single-walled carbon nanotubes," *Chemical Physics Letters*, vol. 365, no. 1, pp. 69–74, 2002.

[44] S. Ummartyotin, J. Juntaro, C. Wu, M. Sain, and H. Manuspiya, "Deposition of pedot: Pss nanoparticles as a conductive microlayer anode in oleds device by desktop inkjet printer," *Journal of Nanomaterials*, vol. 2011, p. 26, 2011.

[45] A. Jamshidi-Roudbari and M. K. Hatalis, "Voltage noise characteristics of polysilicon pin diodes," *Electron Devices, IEEE Transactions on*, vol. 58, no. 4, pp. 1054–1062, 2011.

[46] K. S. Tsakalis and P. A. Ioannou, "Adaptive control of linear time-varying plants: a new model reference controller structure," *Automatic Control, IEEE Transactions on*, vol. 34, no. 10, pp. 1038–1046, 1989.

[47] K. S. Tsakalis and P. A. Ioannou, "A new indirect adaptive control scheme for time-varying plants," *Automatic Control, IEEE Transactions on*, vol. 35, no. 6, pp. 697–705, 1990.

[48] K. S. Tsakalis and P. A. Ioannou, *Linear time-varying systems: control and adaptation*. Prentice-Hall, Inc., 1993.

[49] D. R. Frey, "Improved super-regenerative receiver theory," vol. 60, no. 12, pp. 3267–3278, 2013.

[50] Y. P. Tsividis and P. R. Gray, "An integrated nmos operational amplifier with internal compensation," *IEEE Journal of Solid-State Circuits*, vol. 11, no. 6, pp. 748–753, 1976.

[51] A. Tsormpatzoglou, N. Hastas, N. Choi, F. Mahmoudabadi, M. Hatalis, and C. Dimitriadis, "Analytical surface-potential-based drain current model for amorphous ingazno thin film transistors," *Journal of Applied Physics*, vol. 114, no. 18, p. 184502, 2013.

Biography

THOMAS Charisoulis received his B.S. in Physics from University of Athens Greece in 2010 and his M.S. in Electrical Engineering from Lehigh University in 2012. He has worked in a Bio Application Specific IC Designer position with BOSCH as well as a Display back-plane Designer at Apple Inc. in Cupertino, CA. Currently he is working towards the completion of his Ph.D. Degree in the area of Display Technologies, TFT Backplanes and Analog ASIC Design.

He has participated in numerous projects where the use of Analog circuits facilitates the operation of various VLSI applications such as sensor arrays (gas sensors, bio-sensors, touch sensors etc.) and pixel arrays (AMOLED Displays etc.). He has also participated in projects involving the characterization, modeling and developing new technologies such as of IGZO and LTPS TFT's. His areas of interest are in wide bandwidth, high accuracy circuits and systems theory for high speed, low power analog and mixed signal circuit design with IGZO and LTPS TFT technologies for display, sensor and bio-sensor applications.

In 2001 at the age of 16, Thomas Charisoulis was awarded from Hellenic Mathematical Society of Greece for qualifying to the last round of the Greek national competition award. Recently he has been awarded with the Sherman Fairchild Graduate Fellowship award for 3 years in a row. He is a student member of the IEEE society and a qualified Ph.D. Candidate at Lehigh University currently holding a research

assistants position in Lehigh Universitys Display Research Lab.

— Thomas Charisoulis