

2019

CMOS Closed-loop Control of MEMS Varactors

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CMOS Closed-loop Control of MEMS Varactors

by

Mohammad Javad Asadi

Presented to the Graduate and Research Committee
of Lehigh University
in Candidacy for the degree
of Doctor of Philosophy

in

Electrical Engineering

Lehigh University
May 2019

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Approved and recommended for acceptance as a dissertation in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

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Acknowledgments

I would like to express my sincere gratitude to my advisor Prof. James C. M. Hwang for his continuous support, encouragement, and patience. I highly appreciate his valuable guidance through my PhD study which helped me to grow up and become an independent researcher. I would also like to thank my committee members, Prof. Svetlana Tatic-Lucic, Prof. Wenxin Liu, Prof. Herman F. Nied, and Dr. Charles L. Goldsmith for reviewing the dissertation and providing me with their valuable comments and suggestions.

I am grateful to my former and current colleagues at Compound Semiconductor Technology Laboratory (CSTL), specially, Dr. Cristiano Palego, Dr. Laura Jin, Dr. Yaqing Ning, Dr. Xi Luo, Dr. Vahid Gholizadeh, Yaghoob Rahbarihagh, Xiao Ma, Zhibo Cao, Xin Jin, Kevin Xiong, Xiaotian Du, Lei Li and Xiaopeng Wang who have cooperated with me and made my research experience at CSTL enjoyable. I would also like to thank Dr. Charles Goldsmith, the president of MEMtronics Corp., who never hesitated to share his knowledge with me during our collaboration on research projects.

My sincere and deepest gratitude to my wonderful and lovely wife, Fatemeh, my great parents, sister, and brother. I really appreciate their unconditional love, patience, and

unwavering support. This thesis would not have been possible without their encouragement and endless love.

Last but not least, thank God who I always feel his presence in entire of my life and whom I trust the most. The words are not enough to express the gratitude that he deserves.

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Abstract

A closed-loop capacitance sensing and control mix-mode circuit with a dedicated sensor electrode and a proportional-integral controller was designed for MEMS varactors. The control was based on tuning the bias magnitude of the MEMS varactor according to the difference between sensed and target capacitances. Simulations were done to optimize the CMOS circuit performance and ensure the high-voltage handling capability. The sensing/control circuit has a sensitivity of 1 fF, a settling time of 200 μ s, and a voltage capacity of 90 V.

In a hybrid integration with a MEMS varactor, the circuit could switch the varactor capacitance from 270 fF to 365 fF in 15 ms which could be improved to be faster mainly by monolithic assembling of CMOS chip and MEMS varactor, as well as increasing the current capacity of the control circuit outputs. The control circuit was able to hold the varactor capacitance to 285 ± 5 fF at temperatures between 25 °C and 80 °C.

Furthermore, with the varactor as the tuning element of a substrate-integrated-waveguide (SIW) resonator, the control circuit tuned the resonance frequency from 33.2 GHz to 33.9 GHz, while keeping them constant to within $\pm 0.1\%$ over a temperature range

of 25–90 °C.

The control circuit occupies an area of 1.7 mm² and consumes 6 mW. The present closed-loop-controlled MEMS-tunable resonators could be used in a quartz SIW multipole filter to realize tunable, small-size, light-weight, low-cost, robust, and reliable millimeter-wave filters that are critical to 5G and other future-generation wireless communication systems.

Chaper 1 Introduction

Micro-electro-mechanical systems, known as MEMS, is a technology based on miniaturization of the devices that combine electrical and mechanical components which results in feature size and actuating range within and below microscale. From the actuation mechanism point of view, several methods such as magnetic [1], piezoelectric [2], thermal [3], and electrostatic [4] have been used in MEMS. Among these, electrostatically-controlled MEMS switches and varactors (variable capacitors) with high linearity, low loss, and low power consumption, are promising building blocks for reconfigurable RF front ends [5]. In particular, although development of MEMS varactors has not progressed at the pace of MEMS switches, they have potential to be used in very high-Q (100–400) operation, especially at mm-wave frequencies, and also in tunable networks [5].

This dissertation focuses on electrostatically-controlled MEMS varactors and explores the opportunity of CMOS closed-loop control for the MEMS varactors. In this chapter, first, the principles of the electrostatic MEMS switches and varactors will be briefly discussed. Then, open-loop and closed-loop control approaches for the MEMS devices will be summarized. Finally, organization of the dissertation will be presented.

1.1 Fundamentals of Electrostatic MEMS Devices

A typical configuration of the electrostatic MEMS is two parallel-plate structure in which one electrode is fixed and the other one is moveable (known as membrane). Fig. 1-1(a) shows a MEMS switch fabricated in [6]. As can be seen, it consists of a thin metal membrane suspended a few micrometers above the stationary electrode covered by a dielectric layer. Cross-section schematic of the MEMS switch is shown in Fig. 1-1(b). When a DC voltage is applied to the electrodes, an attractive electrostatic force is generated and causes the membrane to deflect downward. If the applied voltage is sufficiently high, the membrane snaps to the dielectric layer and creates a capacitive short. This voltage is called pull-in voltage. When the membrane is pulled down, the switch is in ON state, and when it is released, the switch is in OFF state.

Considering the first approximation of this structure in which the effect of dielectric layer is neglected, the relationship between the applied bias voltage V and the electrostatic force between two electrodes F_{EL} can be extracted as [7],

$$F_{EL} = \frac{\varepsilon AV^2}{2(g-x)^2} \quad 1-1$$

where ε is permittivity of air, A is the overlapping area of the electrodes, x is the deflection

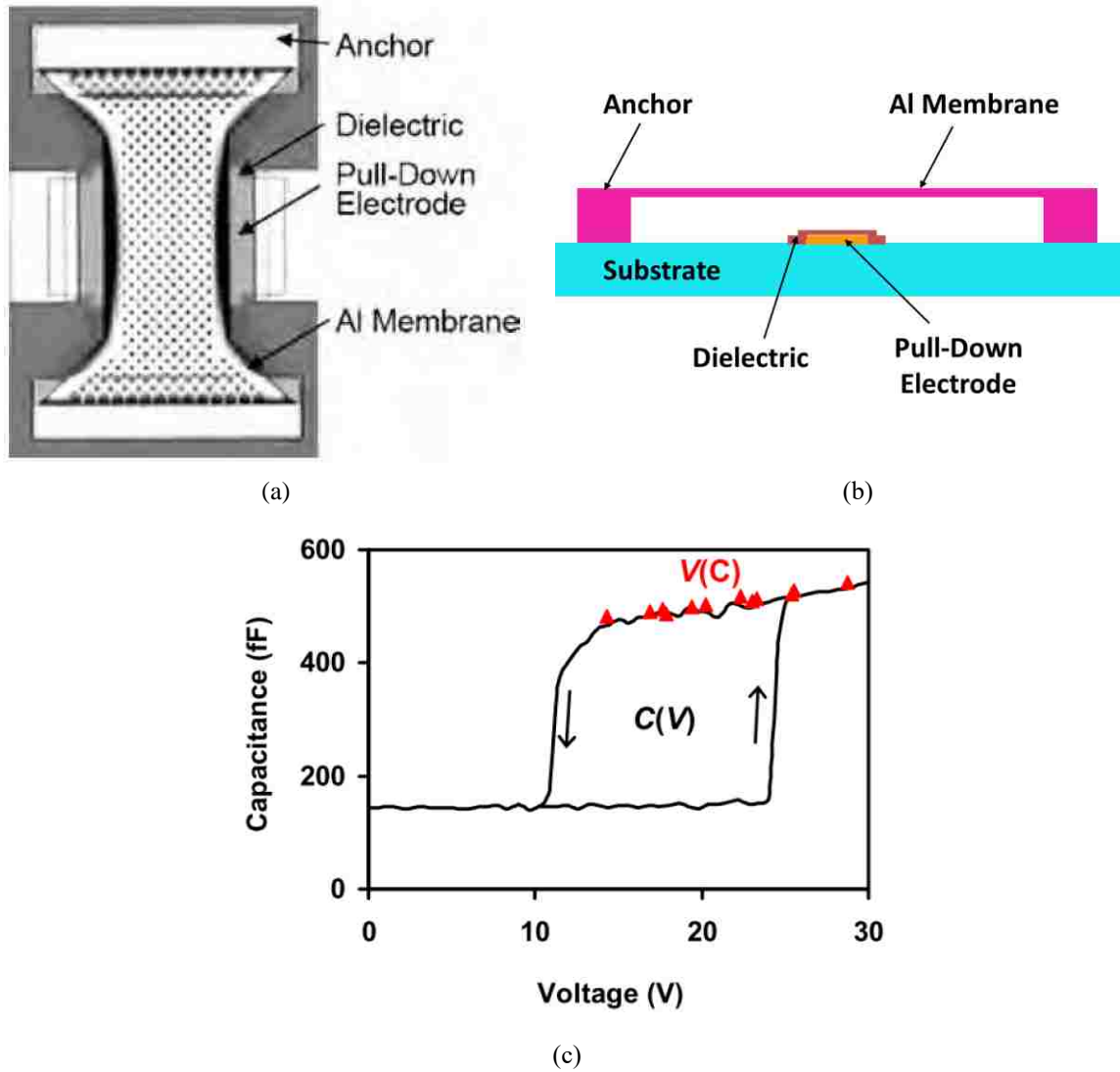
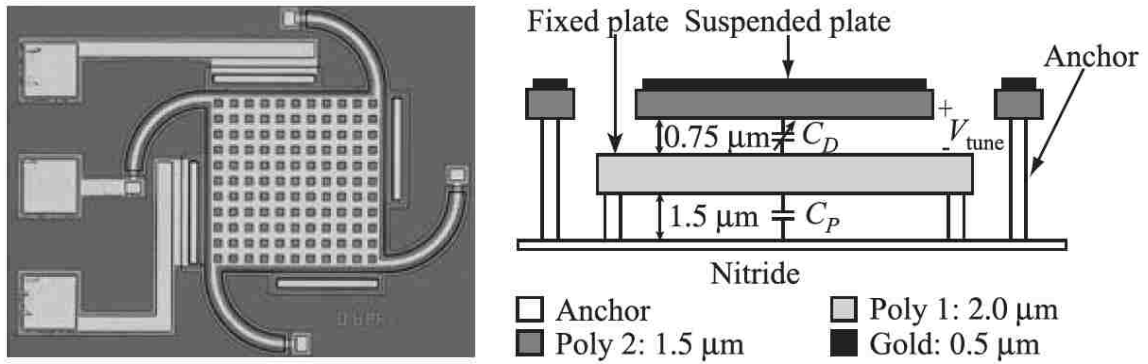


Fig. 1-1. (a) Top view [8] and (b) cross-section schematic of an electrostatic MEMS switch. (c) Typical C - V characteristic of an electrostatic MEMS switch [9].

of the membrane, and g is the airgap when the membrane is released, and no bias voltage is applied. As equation (1-1) implies, the electrostatic force increases by increasing the bias voltage and causes further deflection of the membrane toward the stationary electrode and

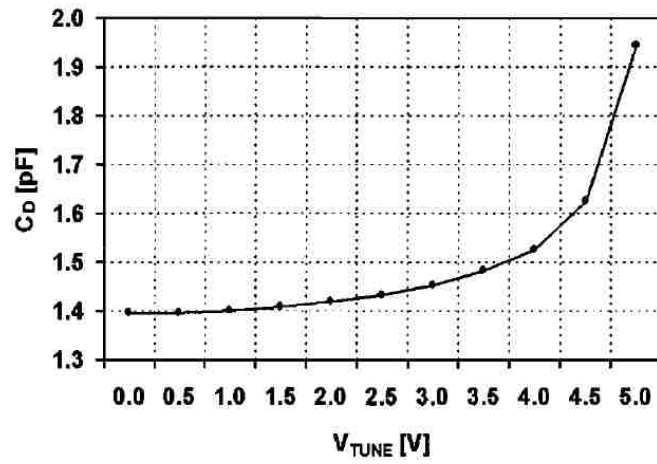
increases the equivalent capacitance of the MEMS. Fig. 1-1(c) shows a typical capacitance–voltage (C - V) characteristics of a MEMS switch. As can be seen, in order to transfer the MEMS switch from ON state to OFF state, the bias voltage should be decreased to less than a certain value which is called pull-out voltage.

The principles of the electrostatic parallel-plate varactors are similar to those for the electrostatic MEMS switch. MEMS varactors operate in the contactless region of the C - V characteristic in which the membrane can deflect with the bias voltage without being pulled down. In this case, the tuning range of the MEMS capacitance is limited by the pull-in voltage and the membrane can deflect up to approximately 1/3 of the air gap g [5]. Fig. 1-2(a) and Fig. 1-2(b) shows, respectively, top view and cross-section schematic of a MEMS varactor fabricated in Columbia University [10]. The membrane was fabricated using a polysilicon layer covered by a 0.5- μm gold with an airgap of 0.75 μm . As Fig. 1-2(c) shows, the MEMS varactor capacitance is tunable from 1.4 to 1.9 pF for a control voltage from 0 to 5.5 V. As expected, due to the nonlinear nature of the electrostatic force in MEMS varactor, most of the capacitance variation (1.5–1.9 pF) happens from 4 to 5.5 V. Increasing the bias voltage to fairly higher than 5.5 V will result in collapse of the membrane which is not desirable in MEMS varactors.



(a)

(b)



(c)

Fig. 1-2. (a) Top view and (b) cross-section schematic of an electrostatic MEMS varactor [10]. (c) Measured C - V characteristic of the MEMS varactor [10].

1.2 Applications of Electrostatic MEMS Devices

Due to their relatively small size, light-weight, no DC power consumption, and manufacturability on low-cost silicon substrate, electrostatic MEMS devices have found

many applications in recent years. Electrostatic MEMS devices have been used in micromirrors [11], force sensor [12], resonator [13], etc.

In particular, radio-frequency (RF) MEMS switches and varactors, designed to be used in RF circuits, have a lot of applications in modern communication systems. RF MEMS switches and varactors can be used as tunable components to realize reconfigurable RF front-end which can be programmed for operating in different modes, such as time-division multiple access (TDMA), code-division multiple access (CDMA), and orthogonal frequency-division multiple access (OFDMA) modes, and frequency bands, like Cell, digital cellular system (DCS), personal communications service (PCS) and international mobile telecommunications (IMT) bands [14]. In conventional transceiver of the mobile handsets, for each frequency band, the entire front-end architecture has to be duplicated to match the associated frequency band which increases the size, loss, and cost of the system.

More specifically, switching networks used in virtually every communication system, are built using coaxial switches which are heavy and costly for satellite systems, and using PIN diodes which are lossy for wireless devices where the available DC power is limited [5]. The MEMS switches are excellent candidates to replace coaxial switches and PIN diodes in switching networks for satellite and base-station system applications.

Furthermore, in today's dense electromagnetic environment with ubiquitous wireless systems, proper management of the spectrum is a concern for communication systems, and it highlights the need for high-performance frequency-agile filters in receiver front-end that can tune on-the-fly to operate in under-utilized spectrum. In order to achieve a small-size, light-weight, and low-power-consumption frequency-agile filter, MEMS varactors are effective choices to be used as the tunable components of the filter.

1.3 Open-loop Versus Closed-loop Control of MEMS Devices

Unlike the macro systems, the MEMS devices are small and typically fast which make the MEMS control system unique [15]. Both open-loop and closed-loop approaches have been used for driving the MEMS devices. The choice between open-loop or closed-loop driving depends on many facts such as sensitivity to device parameters, sensitivity and complexity of driving circuitry, availability and properties of the feedback, and application requirements [16].

One of the aspects of the MEMS devices that can be improved by both open-loop and closed-loop control, is the dynamic response. For example, pre-shaped input signals in open-loop manner have been used to drive an electrostatic MEMS in optical switching

applications to achieve a fast response and short settling time [15]. On the other hand, for the applications in which precision is required as well as speed, closed-loop control has been used for the MEMS devices [17]. In such applications, although the open-loop approach decreases the complexity of the control system, it is extremely sensitive to parameter uncertainties and degrades the required precision.

Furthermore, closed-loop control has been used for inertial sensors [18]–[20] to improve their performance. Similarly, beside improving the dynamics, closed-loop control has been used in electrostatic MEMS devices to extend the travel range of the membrane beyond its natural limitation [21], [22]. This will provide an opportunity for the MEMS varactors to significantly increase their tuning range.

Several issues associated with reliability and robustness of the MEMS devices also can be mitigated by closed-loop control. For example, the C - V characteristics of the electrostatic MEMS devices can drift due to process variation [23], material creep [24], temperature change [25], RF power loading [26], [27], dielectric charging [28]–[30], etc. Dielectric charging occurs when, under a high voltage, the charges are injected from the metallic electrodes to the dielectric layer. Fig. 1-3 shows the effect of dielectric charging on $C(V)$ characteristic of a typical electrostatic MEMS switch. As the main life limiter of

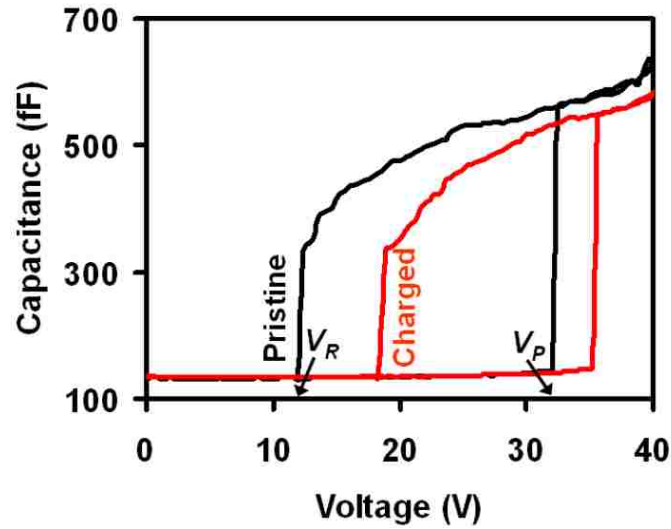


Fig. 1-3. Measured $C(V)$ characteristic of a typical electrostatic MEMS switch in pristine and charged states [31].

electrostatic MEMS, dielectric charging has been the subject of intensive studies. Although several approaches such as design improvement [32]–[34], adopting novel dielectric materials and fabrication processes [35], [36], and applying pre-shaped and bipolar actuation voltage under open-loop control [29], [37], [8], have been proposed to mitigate the effect of dielectric charging, closed-loop-control techniques [9], [38]–[40] have been the most promising ones.

Whereas most of the MEMS control techniques have been developed for on/off switches, the present dissertation focuses on MEMS varactors which capacitance needs to

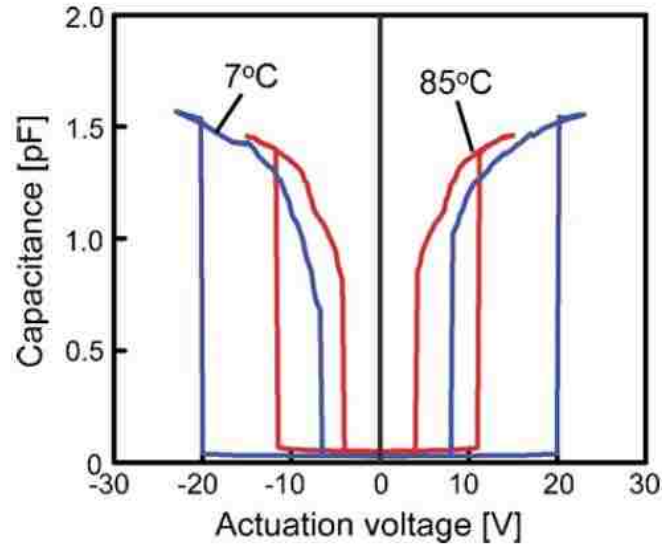


Fig. 1-4. Temperature dependence of the C - V characteristic of a typical electrostatic MEMS switch [41].

be sensed and controlled in flight at high speed while maintaining stability. Coupled with the bias requirement for electrostatic control, such a high-speed and high-voltage system presents unique challenges and necessitate analog approach rather than digital for designing high-speed control circuit.

Although MEMS varactors do not suffer from dielectric charging as severely as MEMS switches, their C - V characteristics can still drift due to other factors such as temperature changes. Basically, the residual stress σ of the membrane changes with ambient temperature according to [26]:

$$\Delta\sigma = E\Delta\alpha\Delta T \quad 1-2$$

where E is Young's modulus of the membrane, $\Delta\alpha$ is the difference in thermal expansion coefficient between the membrane and substrate, and ΔT is the change in temperature. This change in stress impacts the spring constant k of the membrane according to [42], [26]:

$$k = \frac{8\gamma(1-\nu)(\sigma_0 - \Delta\sigma)tw}{L} \quad 1-3$$

where γ is a geometric factor to account for the nonrectangular shape of the membrane, ν is the Poisson's ratio of the membrane material, σ_0 is the residual stress at the reference temperature, and t , w , and L are the thickness, width and length of the membrane, respectively. As equation (1-3) shows, the spring constant of the membrane decreases by increasing the ambient temperature and causes the membrane to be softer and, as Fig. 1-4 experimentally confirms, result in lower pull-in voltage of the electrostatic MEMS switches. In order to compensate for the effect of ambient temperature variations, and improving the temperature stability of the MEMS devices, there have been several proposals such as engineering the material [43], [44] or geometry [45] of the MEMS devices. As an effective approach, micro-ovens have been used in closed-loop manner to locally control the ambient temperature of the MEMS devices [46]–[48]. The main disadvantages of this technique are slow response and high power consumption. Additionally, this technique can solely compensate for the ambient temperature and is not

able to mitigate the effects of other aforementioned issues associated with reliability and robustness of the MEMS devices.

In this dissertation, a high-speed, high-voltage, and low-power consumption closed-loop mixed-mode circuit developed in standard 5-V CMOS technology is described, and the experimental results of the circuit for controlling a MEMS varactor are demonstrated.

1.4 Organization of the Dissertation

Chapter 1 summarized an introduction about MEMS devices, specifically electrostatically-controlled MEMS switches and varactors. The fundamentals, applications, and control techniques including both open loop and closed loop for the MEMS devices were presented.

In Chapter 2, first, the MEMS varactor and its customized compact model will be described in detail. Then, a high-level design of the CMOS sensing/control circuit and the associated challenges will be discussed. Finally, the simulation results of the integrated CMOS closed-loop control will be shown to further investigate and optimize the performance of the control circuit.

Chapter 3 demonstrates the measurement results of the fabricated CMOS chip without

the MEMS varactor. To this end, the experimental verification of each critical circuit block as well as the complete control circuit will be presented.

In Chapter 4, the measurement results of the closed-loop control of the MEMS varactor which is wire-bonded to the CMOS chip will be demonstrated. In addition, the robustness of a single-pole SIW tunable resonator realized by the MEMS varactor under closed-loop control will be evaluated.

Finally, Chapter 5 provides the conclusions of this dissertation as well as recommendations for future research.

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Chapter 2 CMOS Control Circuit Design and Implementation

There are several critical aspects in design of sensing/control CMOS circuit for MEMS varactors. First, the CMOS integrated sensor must be capable of sensing a very small capacitance variation (a few femto-farad) and converting it to an analog voltage in order to be used by control circuit. Second, since operation voltage of the electrostatic MEMS devices are very high (on the order of 100 V) [1], the control circuit which is designed by a standard low-voltage CMOS technology, must be able to handle such a high-voltage. Third, in order to integrate the whole circuit, the high-voltage and low-voltage blocks needs to be monolithically implemented on the same substrate in CMOS chip. Finally, as was mentioned in previous chapter, the CMOS circuit must be very fast to sense and control the capacitance of the varactor in flight while maintaining stability.

In this chapter, first, the MEMS varactor will be described in detail along with modeling principles. Then, a high-level design principle of the CMOS sensing/control system will be illustrated with detailed discussion on some sub-circuits and associated challenges. Finally, the simulation results of the integrated CMOS closed-loop control, which includes the compact model of the MEMS varactor, will be presented to investigate

and optimize the performance of the control circuit.

2.1 MEMS Varactor Modeling and Simulation

For proof of concept, Fig. 2-1 shows schematically a silicon-on-insulator (SOI) MEMS varactor as the tuning element of a quartz substrate-integrated-waveguide (SIW) filter, which is orders-of-magnitude smaller, lighter and lower cost than conventional filters built in metal waveguides [2]. Electrically, Terminal 1 is connected to the gold electrode on the bottom of the silicon bulk where the electrostatic bias V_{MEMS} is applied. Terminal 2 is used to ground the gold electrode on the bottom of the silicon membrane. Terminal 3 is connected to the tuning via of the quartz SIW, upon which the MEMS varactor is flip-mounted. Terminal 4 is connected to the sensor electrode of the capacitance sensing/control circuit, which is isolated from the main RF signal path of the filter. This prevents the capacitance-sensing circuit from introducing noise to the RF signal, and the RF signal from affecting the performance of the capacitance-sensing circuit. The size and location of the sensor electrode are carefully traded off between isolation and sensitivity. For example, the farther the sensor electrode is from the tuning via, the better the isolation but the lower the sensitivity.

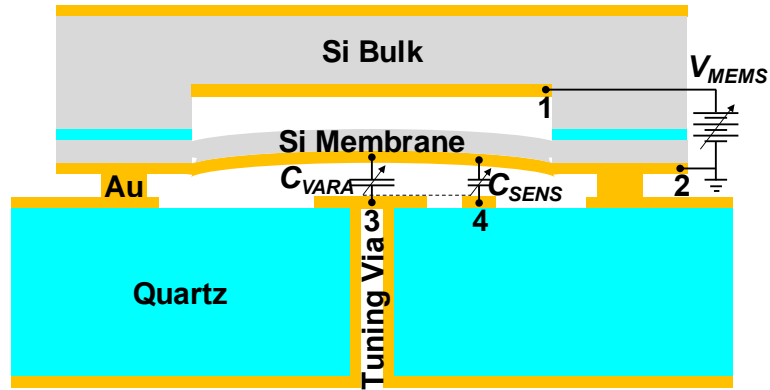


Fig. 2-1. Cross-section schematic of a silicon-on-insulator MEMS varactor as the tuning element of a quartz substrate-integrated waveguide filter.

The electrostatically controlled membrane is composed of 1- μm silicon and 0.5- μm gold. The air cavity between the silicon bulk and the membrane is 20- μm high. The silicon membrane is hexagonally shaped with a span of 3470 μm between two opposing sides, whereas the tuning via is donut-shaped with inner and outer diameters of 228 μm and 292 μm , respectively. The sensor electrode is a 560 $\mu\text{m} \times 310 \mu\text{m}$ rectangle, 620- μm away (center-to-center) from the tuning via. The SIW is 3000- μm wide and 762- μm high.

With Terminal 1 biased by V_{MEMS} , the silicon membrane bows upward and the varactor capacitance C_{VARA} between Terminal 2 and Terminal 3 decreases. Since the filter does not allow ready access to the tuning via for the direct measurement of C_{VARA} , the C - V characteristics of both the varactor and the sensor, C_{VARA} and C_{SENS} , were simulated by the

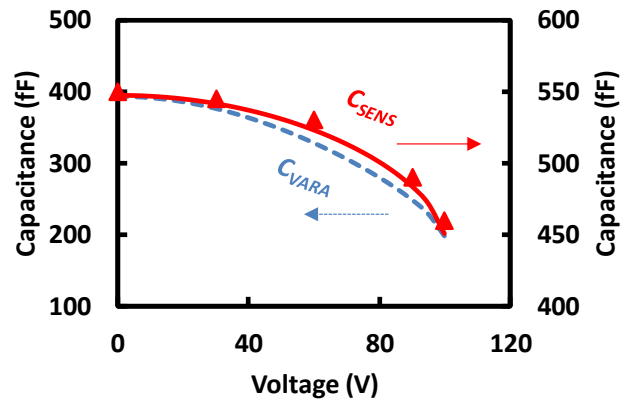


Fig. 2-2. Simulated (curves) vs. measured (symbols) bias dependence of the capacitances of the MEMS varactor (C_{VARA} , dashed curve) and the capacitance sensor (C_{SENS} , solid curve).

ANSYS finite-element Multiphysics program, accounting for the parasitics of interconnect lines and bonding pads. Fig. 2-2 shows that the simulated C_{VARA} tracks C_{SENS} closely, whether C_{SENS} is simulated or measured, with the measurement performed by using a Keysight Technologies 4294A precision impedance analyzer at 1 MHz. Thus, C_{VARA} can be inferred from C_{SENS} for the control purpose. In practice, C_{VARA} does not have to be precisely known, so long as its tuning effect on the filter is calibrated through C_{SENS} .

Based on the ANSYS simulation results, a compact MEMS varactor model was built using Verilog-A code. According to [3], [4], the maximum displacement z of the MEMS varactor membrane is described by a mass of m in series with a damper of b , a spring

constant of k ,

$$m\left(\frac{\partial^2 z}{\partial t^2}\right) + b\left(\frac{\partial z}{\partial t}\right) + kz = F \quad (2-1)$$

where F is dominated by the electrostatic force. Under the parallel-plate assumption,

$$F \approx \frac{\epsilon_0 A_{BIAS} V^2}{2(g_{CAV} - z_{AVE})^2} \quad (2-2)$$

where ϵ_0 is the permittivity of vacuum, A_{BIAS} is the bias electrode area overlapping with the membrane, g_{CAV} is the average air cavity size in the membrane resting position, and z_{AVE} is the average displacement of the membrane to the bias electrode. Assuming z_{AVE} is proportional to the z with a ratio p ,

$$z_{AVE} = pz \quad (2-3)$$

Equation (2-1) can be simulated by an equivalent circuit comprising an inductor L' , a resistor R' , and a capacitor C' , as in the following:

$$L'\left(\frac{\partial^2 V'}{\partial t^2}\right) + R'\left(\frac{\partial V'}{\partial t}\right) + \frac{V'}{C'} = \frac{V'_{IN}}{C'} \quad (2-4)$$

where $L' = m$, $R' = b$, $C' = 1/k$, $V'_{IN} = F/k$, and $V' = z$ is the voltage across the capacitor C' .

This equivalent circuit has been conveniently implemented in Cadence Design Environment by using the Verilog-A code. The simulated V' or z is used to evaluate the

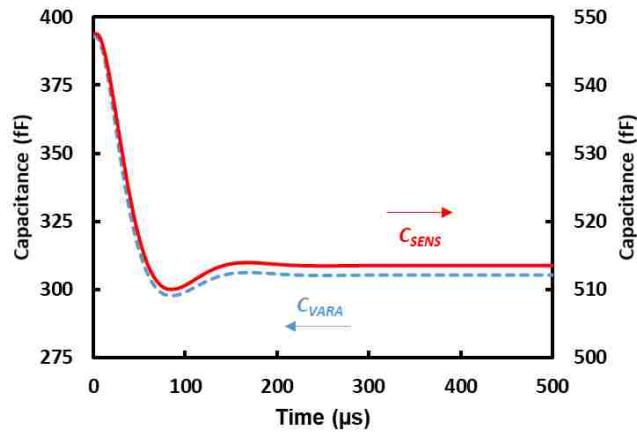


Fig. 2-3. Simulated transient capacitances of the MEMS varactor (C_{VARA} , dashed curve) and the capacitance sensor (C_{SENS} , solid curve) using customized compact model.

capacitance of both varactor and the sensor, C_{VARA} and C_{SENS} according to:

$$C = \epsilon_0 \frac{A}{g_{GAP} + z'_{AVE}} \quad (2-5)$$

where A is the tuning via/sensor electrode area overlapping with the membrane, g_{GAP} is the average air gap between the tuning via/sensor electrode and the membrane in its resting position, and z'_{AVE} is the average displacement of the membrane to the tuning via/sensor electrode. Fig. 2-3 shows the transient capacitances of the MEMS varactor and capacitance sensor simulated by Cadence Design Environment using the customized compact model.

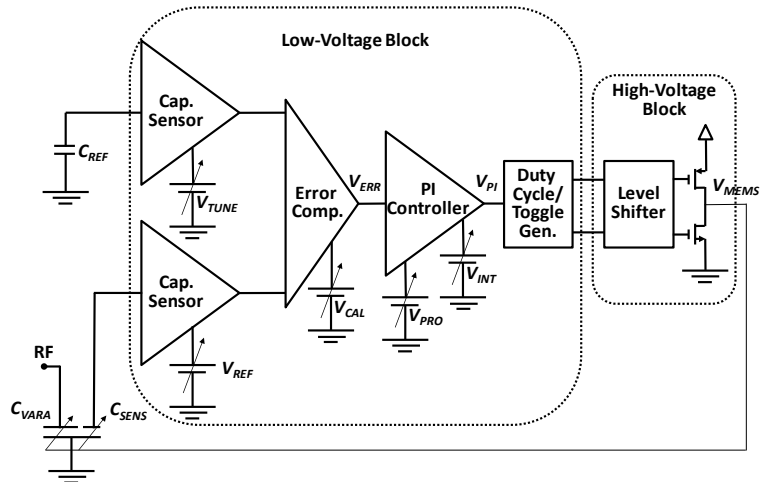


Fig. 2-4. Block diagram of the present closed-loop control circuit.

2.2 High-level CMOS Control Circuit Design

Fig. 2-4 shows the block diagram of the present control circuit, which is similar to the previous on/off control circuit [5], except a proportional-integral (PI) controller is incorporated to ensure stable and robust analog control, and a separate sensor electrode is dedicated to capacitance sensing as described in Sec. 2.1. With the well-tuned PI controller, zero steady-state error and optimized dynamic response can be achieved without adding extra complication due to D-controller. It can be seen from Fig. 2-4 that C_{SENS} is sensed periodically and converted to a pulse-width-modulated (PWM) signal, which is synchronized and compared with the PWM signal of a similar sensing circuit on an on-

chip reference capacitance C_{REF} . Although C_{REF} is fixed, its PWM signal can be scaled by V_{TUNE} to make it appear as a different target capacitance C_{TARG} . Depending on the pulse-width difference Δt , between that of C_{SENS} and C_{TARG} , an amplitude-modulated analog error signal V_{ERR} is generated by the error comparator and fed to the PI controller to generate the control signal V_{PI} . V_{PI} is then used to toggle a single-pole double-throw high-voltage switch at different duty cycles. By toggling between the high-voltage supply and the ground, the switch can increase or decrease V_{MEMS} to decrease or increase C_{VARA} , respectively. In addition to the high-voltage switch, the high-voltage block includes a level shifter to amplify V_{PI} to that required to drive the high-voltage switch. In current design, the high-voltage is provided directly from an off-chip power supply which can be generated using charge-pump techniques as demonstrated in several reports [6], [7]. Additional tuning voltages in the low-voltage block such as V_{CAL} , V_{PRO} , and V_{INT} allow nulling of the error comparator, and adjustment of the proportion and integration constants of the PI controller.

2.3 Capacitance Sensor Design

Typical problems related to implementation of MEMS control systems are sensing which is rather problematic at the small scale and relatively fast dynamics [8]. Previously,

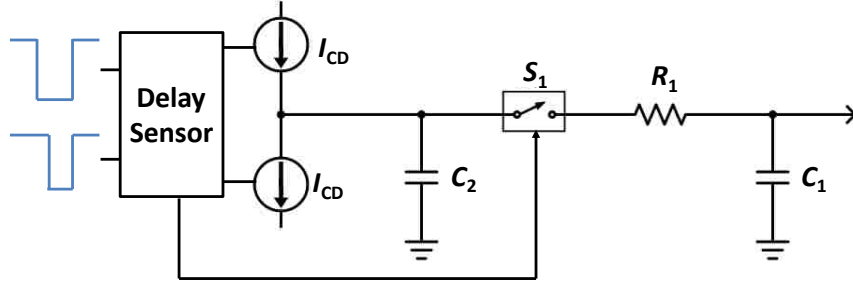


Fig. 2-5. Detailed schematic of the error comparator.

in [5], in order to avoid adding significant noise interfering with the RF signal, a novel capacitance sensing technique was developed without applying a high-frequency ac signal as used in conventional capacitance sensing schemes [9]. Presently, since the capacitance sensor electrode is isolated from the RF signal path, capacitance sensing and control can be performed independently and continuously, which results in faster and more sensitive control than that of [5]. Similar to the capacitance-sensing circuit of [5], C_{SENS} and C_{TARG} , including their associated parasitics, are sensed by discharging through two identical current sources I_{DIS} . The time it takes to decrease the discharge voltage V_{DIS} to V_{REF} and V_{TUNE} , are used to form the two PWM signals proportional to C_{SENS} and C_{TARG} , respectively.

From the two PWM signals, Fig. 2-5 shows schematically how the error comparator translates the pulse-width difference Δt into the analog error signal V_{ERR} . Note that $V_{ERR} > 0$ for $C_{SENS} > C_{TARG}$ and $V_{ERR} < 0$ for $C_{SENS} < C_{TARG}$. In a set time period, two identical

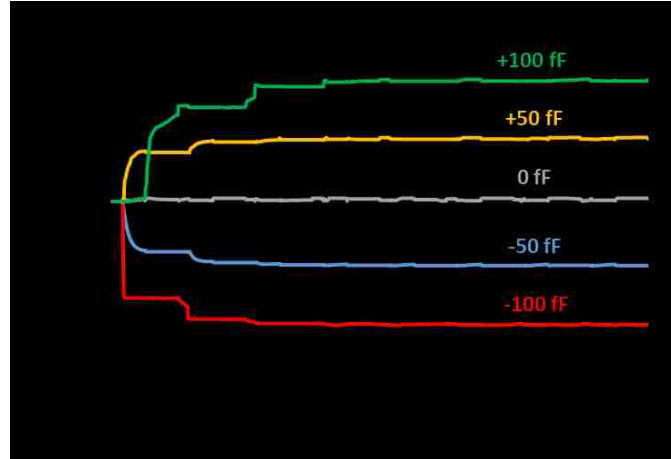


Fig. 2-6. Simulated analog error signals V_{ERR} for different deviations of the sensed capacitance C_{SENS} from the target capacitance C_{TARG} .

current sources, I_{CD} , charge or discharge the capacitor C_2 . If $\Delta t > 0$ ($C_{SENS} > C_{TARG}$), the delay sensor turns on the top I_{CD} and turns off the bottom I_{CD} to charge C_2 . If $\Delta t < 0$ ($C_{SENS} < C_{TARG}$), the delay sensor turns off the top I_{CD} and turns on the bottom I_{CD} to discharge C_2 . The switch S_1 turns on momentarily to sample the voltage on C_2 and hold it on another capacitor C_1 . In addition, C_1 together with the resistor R_1 functions as a low-pass filter (LPF) to suppress the noise from S_1 . Therefore,

$$\Delta t = (V_{DIS}/I_{DIS})(C_{SENS} - C_{TARG}) \quad (2-6)$$

On the other hand, since C_1 is designed to be much smaller than C_2 ,

$$V_{ERR} = (I_{CD}/C_2)\Delta t \quad (2-7)$$

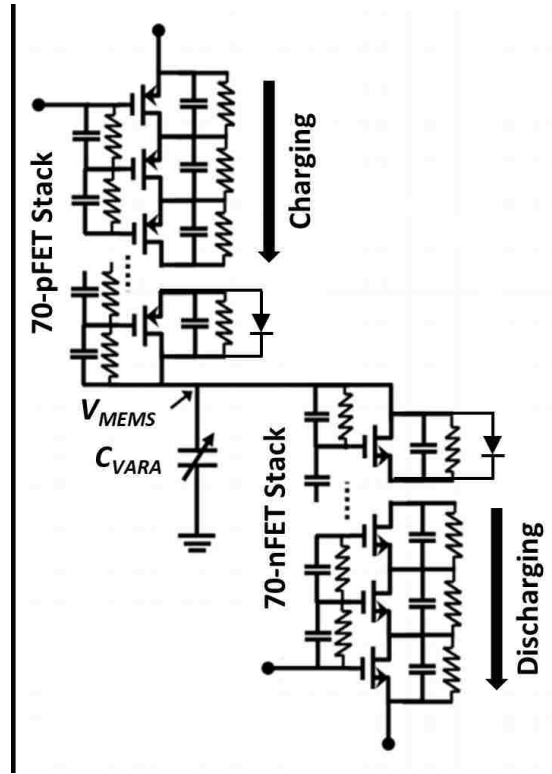
From equations (2-6) and (2-7),

$$V_{ERR} = (V_{DIS} \cdot I_{CD} / C_2 \cdot I_{DIS}) (C_{SENS} - C_{TARG}) \quad (2-8)$$

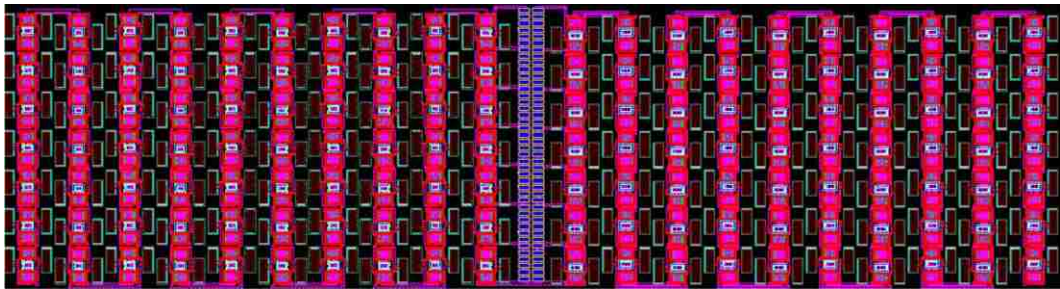
which confirms that V_{ERR} is proportional to the difference between C_{SENS} and C_{TARG} . Fig. 2-6 shows the simulated V_{ERR} for different deviations of C_{SENS} from C_{TARG} . It can be seen that in a few microseconds, V_{ERR} settles down to a value proportional to $C_{SENS} - C_{TARG}$ as predicted analytically by equation (2-8).

2.4 High-voltage Switch

The biggest challenge of the present design was for the CMOS control circuit to handle the high bias required by the MEMS varactor, which could exceed 100 V as shown in Fig. 2-2. One common technique to extend high-voltage capability of a switch is to stack multiple devices in series [10], [11]. Device stacking allows for high voltage to divide equally across more devices, so that no single device is stressed. Theoretically, the achievable drive level of such high-voltage switch is proportional to the number of stacked devices and is eventually limited by the substrate voltage tolerance. For the current design, based on the standard 5-V CMOS SOI technology, 70 pFETs and 70 nFETs were stacked in two ladders to share the high voltage as shown in Fig. 2-7(a) [12]. For the voltage drop



(a)



(b)

Fig. 2-7. (a) Schematic and (b) layout of the $900\ \mu\text{m} \times 240\ \mu\text{m}$ high-voltage switch.

across each FET to be safely below the breakdown specification of 6 V, both statically and dynamically, resistor and capacitor ladders were used to ensure even voltage distribution

across the FET ladders without large spikes. To further protect the FETs, diode clamps were added across the source and drain of the seven most vulnerable FETs closest to the MEMS varactor. The number of FETs was traded-off between spike suppression and the size of the capacitor ladders, which are much larger than that of FETs and resistors. Each FET has a gate width of 15 μm ; each set of stacked diodes across the source and drain of each FET occupies an area of 330 μm^2 ; each resistor is 3.2 M Ω ; each capacitor is 288 fF. Other critical parameters such as metal spacing and the breakdown voltage of the buried oxide were also carefully considered to ensure the reliability of the high-voltage block. After several iterations between schematics and layout, shown in Fig. 2-7(b), the simulations including interconnect parasitics show that all the stacked FETs operate within the safe voltage range without being affected by the high voltage. Fig. 2-8(a) and Fig. 2-8(b) show the source-drain voltage waveforms of four FETs sampled at the top, middle, and bottom of both the p-FET and n-FET ladders in response to turning the high-voltage switch on and off. It can be seen that all of the voltage spikes are less than the breakdown voltage of 6 V. Fig. 2-8(c) and Fig. 2-8(d) compare the voltage spikes of the bottom (worst-case) FETs with and without interconnect parasitics. They show that parasitics increase both the magnitude and duration of the voltage spikes.

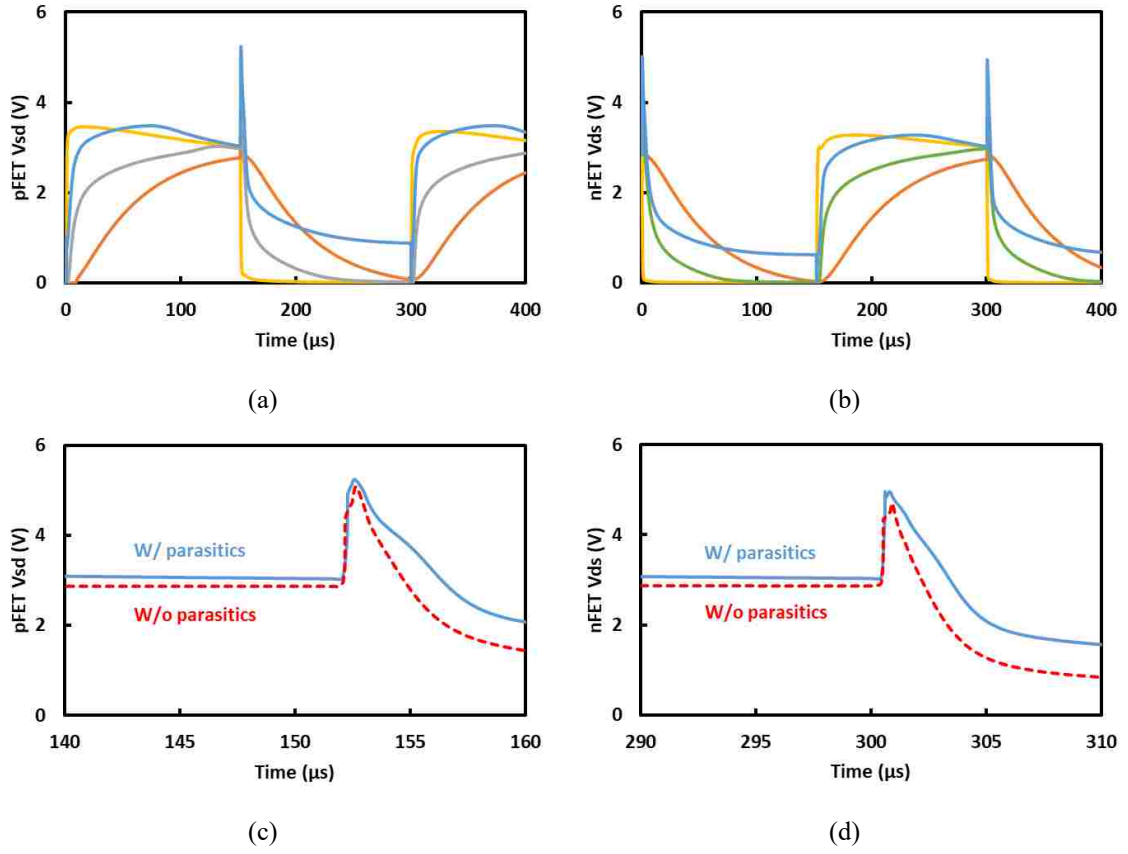


Fig. 2-8. Source-drain voltage waveforms simulated with interconnect parasitics for four FETs on the top, middle and bottom of (a) p-FET stack and (b) n-FET stack. Source-drain voltage waveforms simulated with and without interconnect parasitics for the bottom (worst-case) FET on (c) p-FET stack and (d) n-FET stack.

2.5 Simulated Closed-loop Control

The designed control circuit was simulated in Cadence Design Environment with the MEMS varactor compact model described in Sec. 2.1. As the MEMS varactor has a natural frequency on the order of 10 kHz, the clock frequency was chosen to be 1 MHz. Simulating

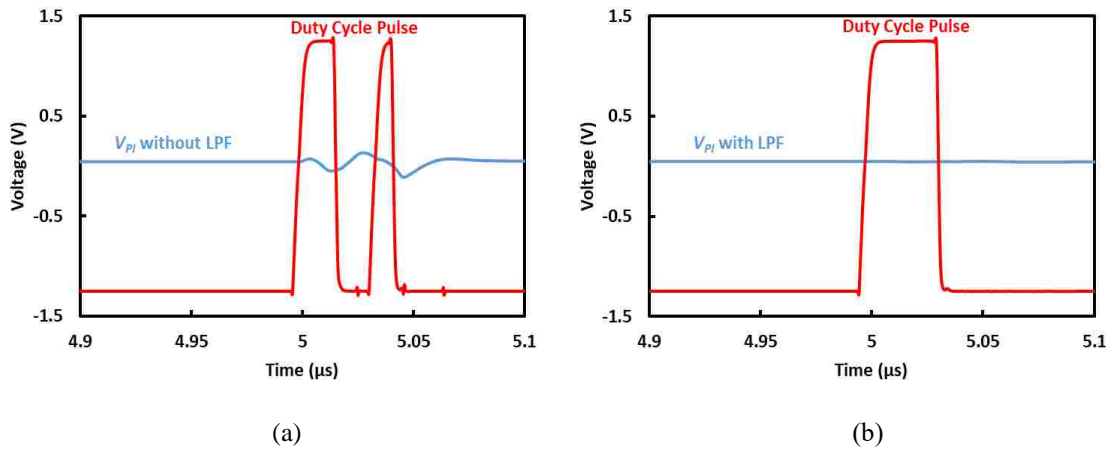
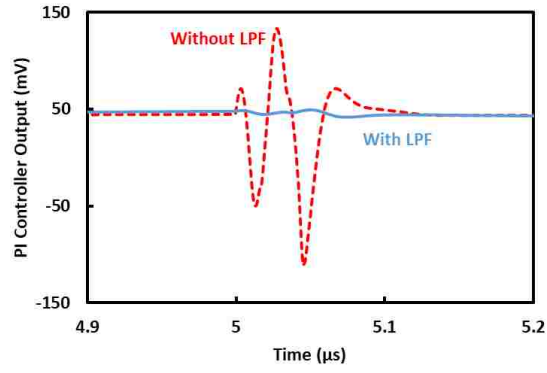


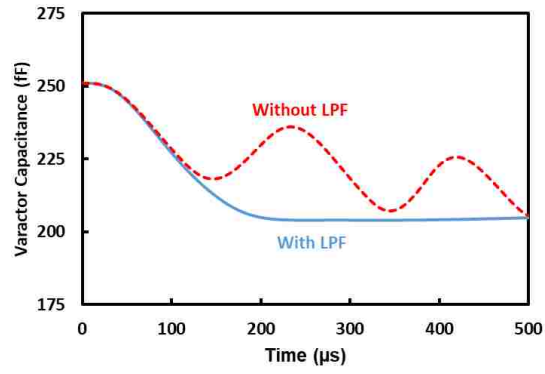
Fig. 2-9. Simulated PI controller output V_{PI} and duty cycle pulse (a) without and (b) with LPF.

the entire CMOS circuit disclosed another big challenge associated with integrating the high-voltage block (high-voltage switch and level shifter) with the low-voltage block (capacitance sensor, error comparator, PI controller, and toggle generator) on the same chip. Despite the SOI technology, capacitive coupling through the common substrate allows the high-voltage block to generate significant noise on the low-voltage analog signal and to degrade the performance of the control circuit. For example, Fig. 2-9(a) shows the simulated PI controller output V_{PI} and duty cycle pulse. It can be seen that once the high-voltage blocks are excited by the duty cycle pulse, the pulse starts to fluctuate resulting in spurious signals. To overcome this challenge, several techniques were suggested in literatures [13], [14] which usually make the design complicated. For this circuit, a 25-

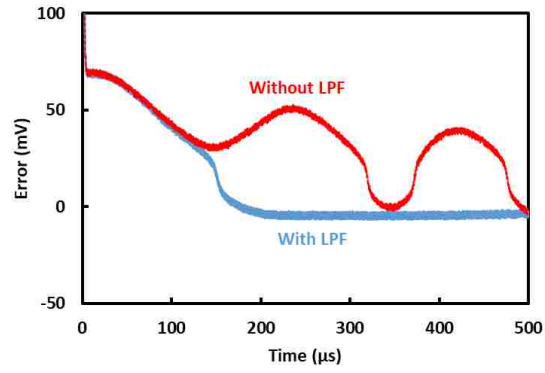
MHz LPF was added to the PI controller output. The filter has more than 30 dB loss for fluctuations at 25 MHz reducing them to just a few millivolts which is tolerable for the performance of the present circuit. As the result, Fig. 2-9(b) shows stable PI controller output V_{PI} in proportion to the duty cycle of the pulse. Furthermore, Fig. 2-10 compares the performance of the circuit for the cases with and without the LPF. As can be seen, with the LPF, the varactor capacitance C_{VARA} and the analog error signal V_{ERR} steadily settle down in 200 μ s, whereas the circuit without the LPF oscillates and is not able to catch the target steadily. On the other hand, the settling time of 200 μ s achieved in this simulation is comparable to the inverse of the natural frequency of the MEMS varactor and difficult to achieve by a purely digital control circuit.



(a)



(b)



(c)

Fig. 2-10. Simulated (a) PI controller output V_{PI} , (b) MEMS varactor capacitance C_{VARA} , and (c) analog error signal V_{ERR} , with and without the LPF.

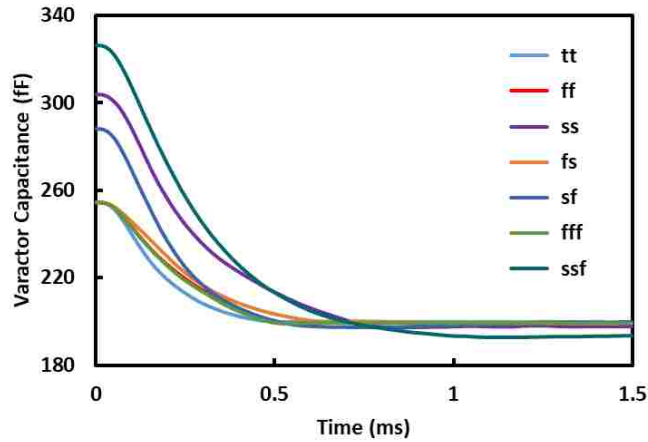


Fig. 2-11. Simulated transient capacitance of the MEMS varactor with the control circuit fabricated with three standard deviations from typical process parameters.

In order to ensure that the designed CMOS control circuit is robust against process variations, the circuit was simulated under six groups of process corners [15] provided by the foundry. Fig. 2-11 compares the transient capacitance of the MEMS varactor for typical NMOS and PMOS (tt) with that for process corners of fast-fast (ff), slow-slow (ss), fast-slow (fs), slow-fast (sf), fast-fast functional (fff), and slow-slow functional (ssf) at three standard deviations. As can be seen in the figure, in most cases, the transient capacitance can approach the target value within approximately the same time.

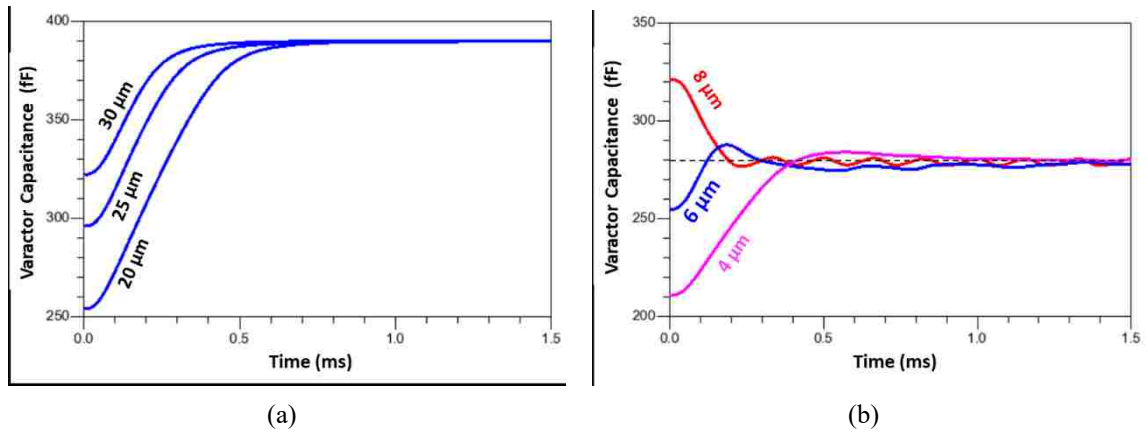


Fig. 2-12. Simulated transient capacitance of the MEMS varactor with (a) cavity sizes of 20, 25 and 30 microns and (b) air gaps of 4, 6 and 8 microns.

Beside circuit variations due to fabrication process tolerance, each MEMS varactor may also have different characteristics [16]. For example, for the present MEMS varactor, some parameters such as, air cavity size and air gap can vary for each fabricated chip, which the former affects the capacitance range and the latter change the operation voltage of the device. To evaluate the robustness of the control circuit, Fig. 2-12 shows simulated transient responses, for three different MEMS cavity sizes and air gaps, as example. It can be seen that in all cases the control circuit can achieve the target capacitance with the same set of proportional and integral parameters. If necessary, these parameters can be optimized for each MEMS varactor for the best dynamic response.

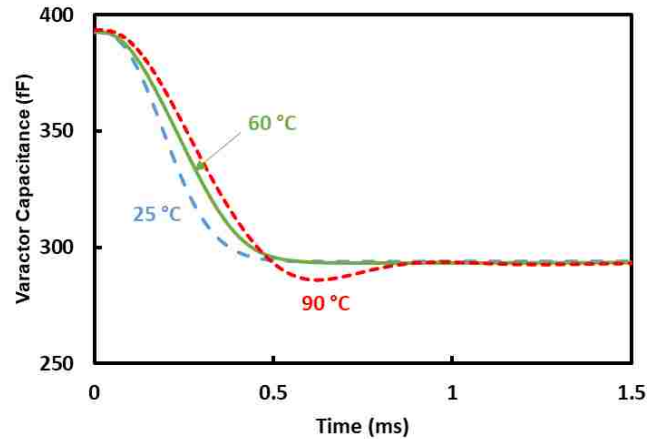
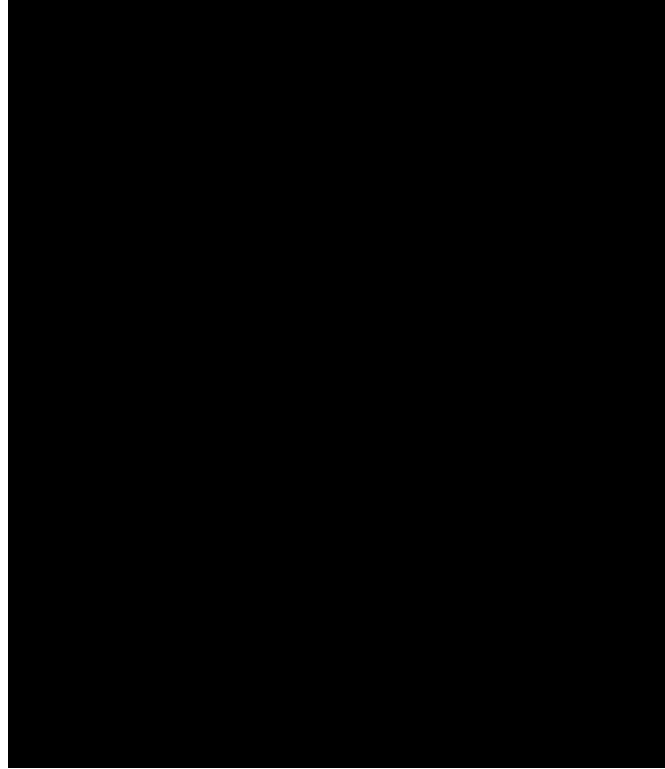


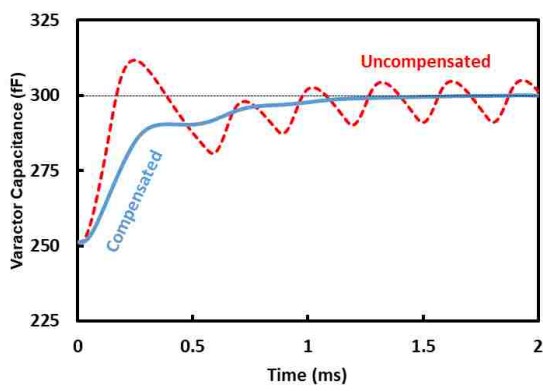
Fig. 2-13. Simulated transient capacitance of the MEMS varactor for temperatures of 25, 60 and 90 °C.

Finally, robustness against temperature variation was also verified. Fig. 2-13 shows that the same target capacitance was achieved at temperatures of 25, 60, and 90 °C, except that the settling time lengthened for higher temperatures. For this simulation, MEMS varactor model was customized for each temperature by fitting the simulated and measured $C-V$ characteristics of the MEMS varactor.

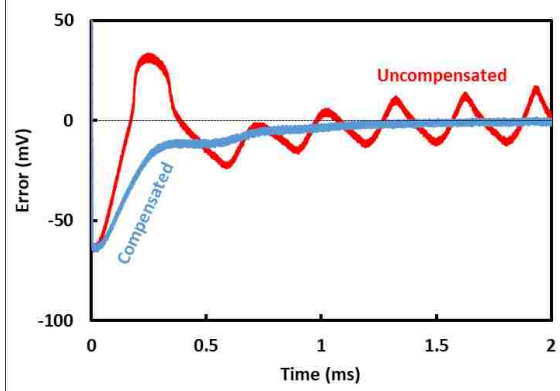
As can be seen in Fig. 2-12(b), in some cases there is insufficient discharge time for the circuits to reach the target steadily without oscillation. To overcome this problem, speed was sacrificed for stability by increasing the discharging time with a compensation resistor in series with the MEMS capacitor as shown in Fig. 2-14(a). Fig. 2-14(b) shows that with the resistor, the circuit steadily reaches the target without oscillation.



(a)



(b)



(c)

Fig. 2-14. (a) Schematic of the high-voltage switch with a compensation resistor added in series with the MEMS capacitor, and simulated transient (b) capacitance, and (c) error of the MEMS varactor for compensated and uncompensated cases.

2.6 CMOS Circuit Layout Implementation

The above-described control circuit with encouraging simulated performance was implemented in 180-nm CMOS SOI technology [17]. The reason to use SOI technology is to take advantage of the insulating substrate which decouples the body of each transistor and enables the FET stacking to handle high voltages [17]. As Fig. 2-15 shows, in order to take the best advantage of the $5 \times 5 \text{ mm}^2$ available die area, six separate chips were designed to fit in the area. Beside the complete control circuits including low- and high-voltage blocks on the same chip, separate configurations also were considered to implement the low-voltage and high-voltage blocks on separate chips for evaluation and diagnosis. Also, for more detailed diagnosis, the fundamental components, such as logic gates, summer circuit, ramp generator, comparator, current source, and analog and digital buffers were included individually in the chips.

To ensure that the performance of the designed circuits is not significantly degraded by parasitic capacitances and resistances associated with circuit interconnects, post-layout simulation was performed. As a result, for instance, it was found out that the fan-out capacity of the digital buffer needed to be increased to provide enough current for

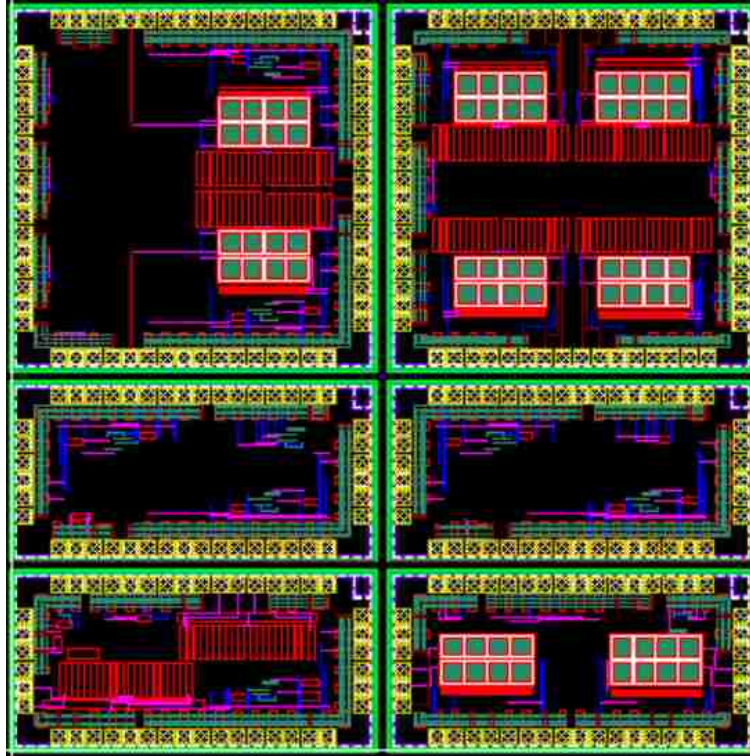


Fig. 2-15. Layout of the 5 mm \times 5 mm six separate chips designed to include complete control circuit as well as several fundamental components for evaluation and diagnosis.

extra capacitance from the interconnect parasitics. With the improved digital buffer, Fig. 2-16, as an example, shows the performance of the overall control circuit with and without interconnect parasitics. It can be seen that the system with interconnect parasitics is also able to follow the target smoothly without ripple and steady-state error. The transient capacitance with parasitics can be improved by retuning the PI controller.

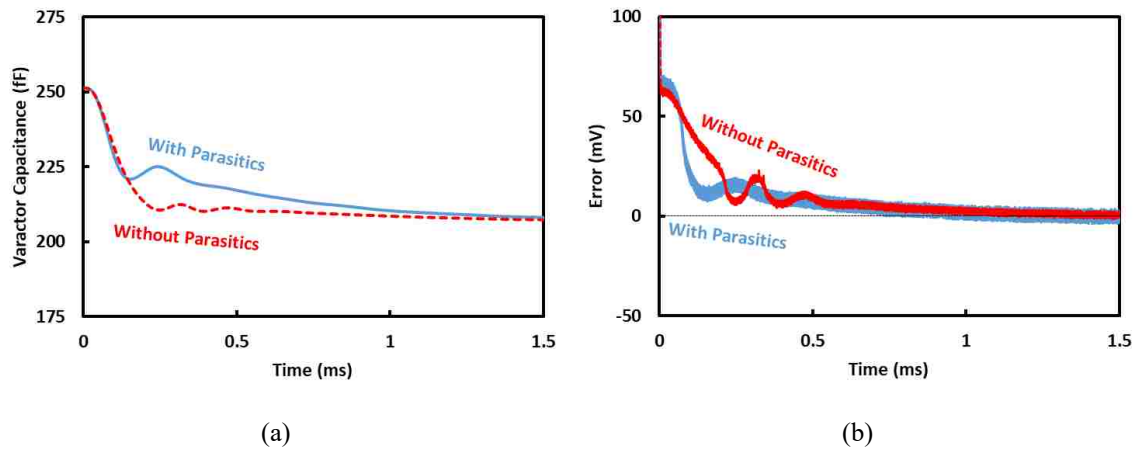


Fig. 2-16. Simulated transient (a) capacitance and (b) error of the MEMS varactor controlled by the CMOS circuit with and without interconnect parasitics.

Finally, the layout was checked by several CAD tools to ensure compliance with foundry requirements. For example, Design-Rule Checker (DRC) was used to check the local and global pattern densities, and other minimum and maximum size requirements; Floating Gate/Antenna Rule was used to increase reliability and yield during fabrication; Layout Versus Schematic (LVS) was used to ensure matching with schematics.

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Chapter 3 CMOS Control Circuit Verification

In this chapters, the measurement results of the CMOS chip without the MEMS varactor will be discussed. To this end, first, the functionality of each critical circuit block such as capacitance sensor and high-voltage switch will be verified, then the complete control circuit will be tested, and the detailed internal signals will be monitored to check the expected outputs. DC power supplies, and other necessary voltages, such as V_{TUNE} for target capacitance tuning, V_{REF} for reference voltage of the capacitance sensor, V_{PRO} and V_{INT} for tuning PI controller parameters, V_{CAL} for calibration, and CLK for clock signal will be applied. Also, a multi-channel oscilloscope will be used to monitor output signals from the CMOS chips for diagnosis, such as *Duty Cycle* for duty cycle pulses, *Toggle* for charging/discharging control signal of the MEMS varactor, V_{ERR} for analog error signal, V_{PI} for PI controller output, and V_{MEMS} for output voltage of the high-voltage switch. Also, using V_{TUNE} which was designed initially for tuning the target capacitance, it is possible to artificially generate error signal and monitor the output signals to verify the functionality of the chips.

3.1 Measurement Setup

The designed CMOS circuit was fabricated at Global Foundry through the MOSIS multi-project wafer (MPW) program. Fig. 3-1 shows that the fabricated $1.3 \text{ mm} \times 1.3 \text{ mm}$ chip was mainly occupied by the high-voltage block and input/output ports. (The chip is actually one quarter of a $2.6 \text{ mm} \times 2.6 \text{ mm}$ die.) To facilitate the evaluation of the chips, a printed circuit board (PCB) was designed and fabricated. Furthermore, a universal zero-insertion-force (ZIF) socket was used to accommodate all six chips of different input/output pad configurations, with each chip first mounted on a low-profile quad-flat-package (LQFP) to dual-in-line-package (DIP) adaptor. The PCB size is $12'' \times 14''$ to accommodate 64 bayonet Neill-Concelman (BNC) connectors for applying the inputs and monitoring the outputs, including that of different functional blocks of the control circuit as shown in Fig. 3-2. Furthermore, decoupling capacitors were added to the appropriate lines which can be connected/disconnected using dual in-line package (DIP) switches according to the supply lines of the chips under test.

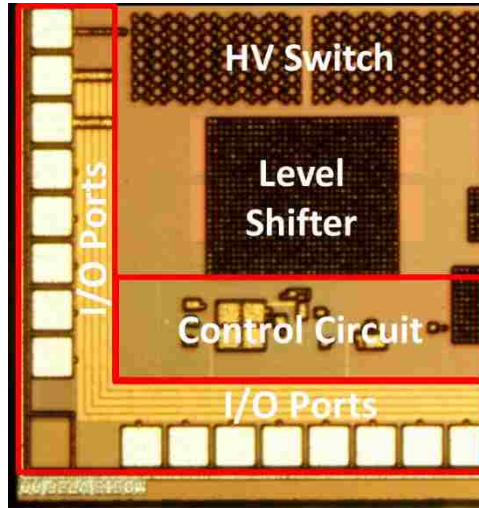


Fig. 3-1. Micrograph of the 1.3 mm × 1.3 mm control circuit chip.

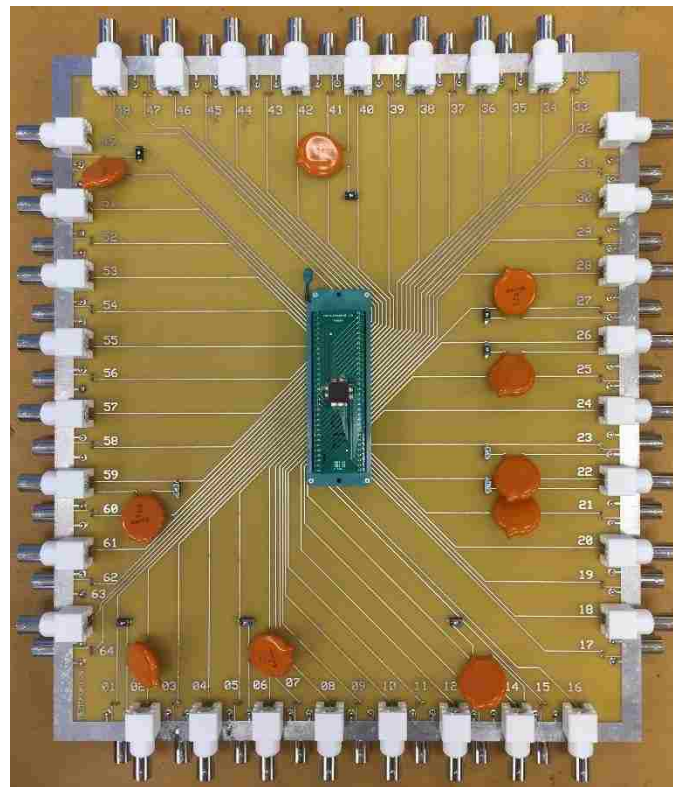


Fig. 3-2. The 36 cm × 31 cm custom printed-circuit board for evaluating the various chips.

3.2 Measured Performance of the Capacitance Sensor

Fig. 3-3(a) shows that both the pulse-width difference Δt and the analog error signal V_{ERR} are linearly dependent on the tuning voltage V_{TUNE} , in agreement with equation (2-6) and (2-8), respectively. Notice that the linear region of this capacitance sensor is much wider than the dynamic range required by the control circuit. Fig. 3-3(b) shows that V_{ERR} reaches a steady state in less than 5 μs in response to a step change in V_{TUNE} , which matches the simulated results shown in Fig. 2-6. As was mentioned before, in this design, changing V_{TUNE} causes the reference capacitance to appear as different values and consequently, the sensor circuit generates different error signals V_{ERR} while the reference is a constant capacitor. Presently, the capacitance sensing speed is mainly limited by the discharge current I_{DIS} and parasitics. In other words, the small current I_{DIS} should discharge the sensing capacitor along with large parasitics which result in a long time for capacitance to be sensed. By increasing I_{DIS} and monolithically integrating the control circuit with the MEMS varactor, the sensing speed can be improved.

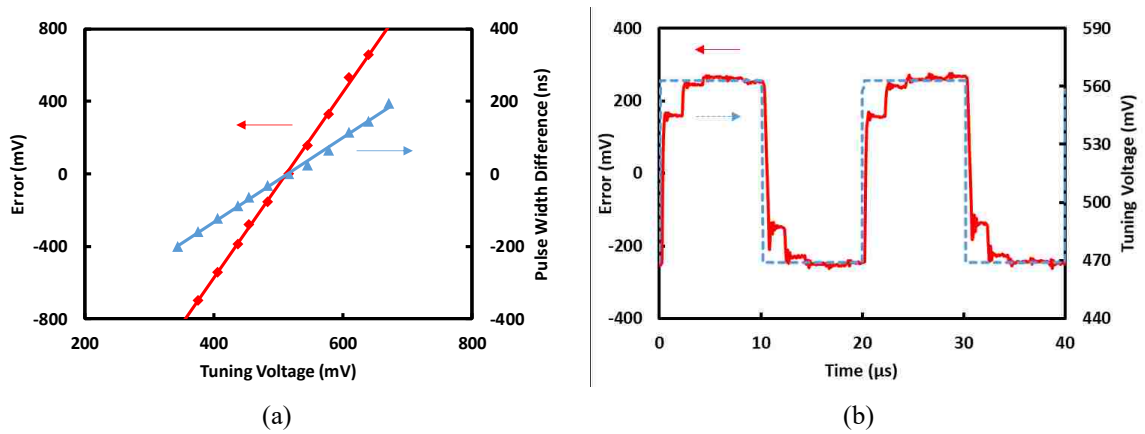
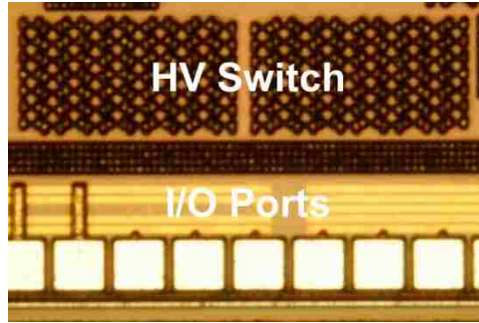


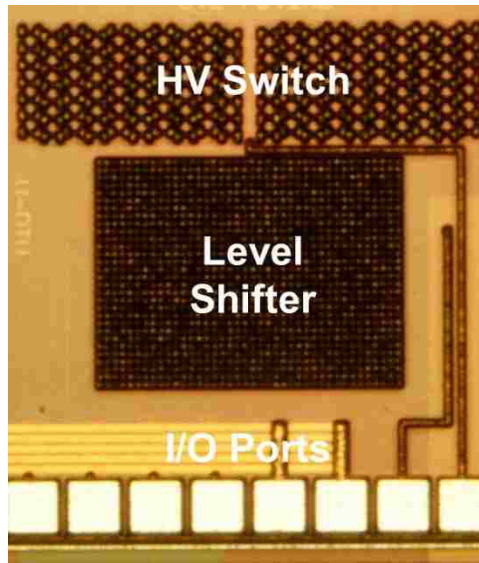
Fig. 3-3. Measured pulse width difference Δt and error signal V_{ERR} in response to (a) steady and (b) transient values of tuning voltage V_{TUNE} .

3.3 Measured Performance of the High-voltage Switch

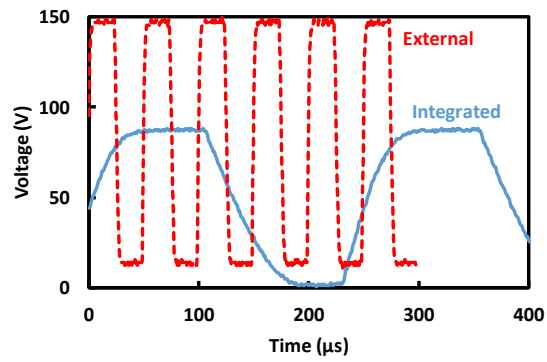
Fig. 3-4(a) shows the fabricated high-voltage switch as a stand-alone circuit block which can be tested independently and using off-chip level shifter and signal generators. As Fig. 3-4(c) shows, the high-voltage switch by itself could handle 150 V and charge/discharge the load capacitor periodically. However, the performance degraded to 90 V, as shown in Fig. 3-4(c), when the high-voltage switch was monolithically integrated with the level shifter, as shown in Fig. 3-4(b). For the voltage higher than 90 V, the switch still could charge the load capacitor to the supply voltage without any failure in the FETs,



(a)



(b)



(c)

Fig. 3-4. Micrograph of the high-voltage switch (a) stand alone and (b) with integrated level shifter. (c) Measured output waveform of the high-voltage switch with integrated and external level shifters.

Table 3-1 Comparison of the High-voltage Switches

Year	2013	2013	2016	2017	2019
Technology	0.5 μm SOS CMOS	45 nm SOI CMOS	0.6 μm SOI CMOS	0.6 μm SOI CMOS	0.18 μm SOI CMOS
Device	3.3 V	1.5 V	5 V	5 V	5 V
Voltage (V)	40	44	30*	50	90 /150*
Speed	NA	20 kHz	NA	NA	4 kHz
Reference	[1]	[2]	[3]	[4]	Present

* With external level shifter

while it fails to discharge the load capacitor completely to the ground. This performance degradation in high voltage, is mainly due to limitation of the drive capacity of the integrated level shifter, which can be enlarged in a future design. (It can be seen in Fig. 3-4(b) that the present level shifter is already as large as the high-voltage switch.) Continued operations at 90 V and 4 kHz as well as hold-on in on/off states for more than a week were completed without any failures in the high-voltage block.

Table 3-1 compares the performance of the designed high-voltage switch with that of previous published works. Despite the relatively low switching frequency, the preset design has the highest voltage capacity for both cases of external and integrated level shifter.

3.4 CMOS Control Circuit Function Verification

Since the functionality of the fundamental components was successfully verified, as demonstrated in previous sections, performance of the CMOS control circuit with all circuit blocks could be experimentally evaluated. The circuit was tested with a capacitance signal artificially applied to its input by adjusting tuning voltage V_{TUNE} . The clock signal CLK, supply, and high-voltages were provided by off-chip function generator and power supplies. The output signals were monitored using a multi-channel oscilloscope. Fig. 3-5 shows that the measured internal and output waveforms, such as the PI controller output V_{PI} , the toggle signal, the duty cycle signal, and the MEMS varactor bias V_{MEMS} agree with that simulated. For example, the toggle signal changes the logic depending on whether the sensed capacitance is below or above the target, the duty cycle is proportional to amplitude of the PI controller output, and the high-voltage switch output, which will be connected to the MEMS, increases or decreases. Since analog error signal and PI controller output overlaps, the analog error signal V_{ERR} is not shown in the figures. In this measurement setup without MEMS varactor wire bonded, the varactor capacitance was provided by the parasitic capacitance from the bonding pad and wire connecting the chip to the package.

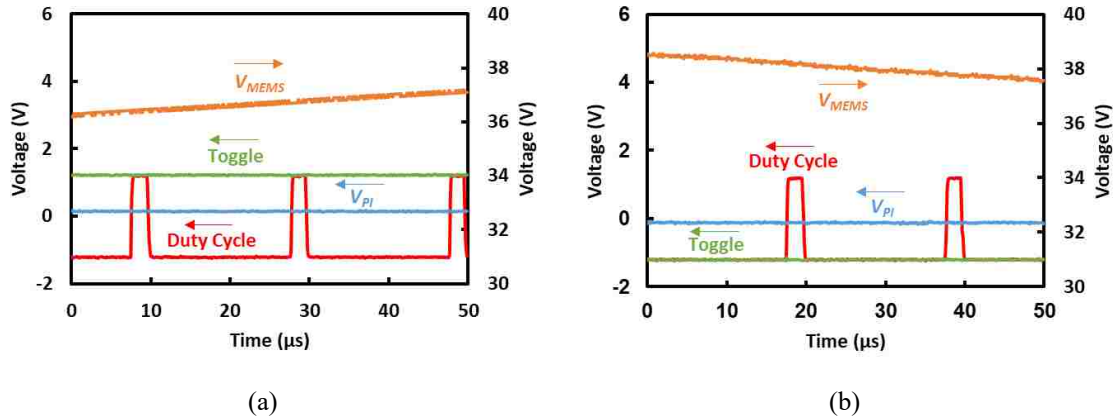


Fig. 3-5. Measured internal and output waveforms of the control circuit, including PI controller output V_{PI} , toggle signal, duty cycle pulse, and MEMS bias voltage, with the input capacitance signal (a) above and (b) below the target.

The demonstrated measurement results verified the functionality and performance of the CMOS sense/control circuit without MEMS varactor wire bonded. In next chapter, the experimental results of the CMOS closed-loop control circuit with the MEMS varactor will be discussed and the robustness of the MEMS varactor under closed-loop control will be evaluated.

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Chapter 4 Experimental Demonstration of Closed-loop Control of MEMS Varactor

After verification of functionality of the CMOS circuit blocks and performance of the control circuit, a MEMS varactor flip-mounted on a single-pole SIW resonator was wire-bonded to the packaged CMOS chip with open lid as shown in Fig. 4-1(a). Although this hybrid assembly added more parasitics than in the previously demonstrated monolithic integration [1], the measured performance was acceptable for temperature compensation as will be shown in this chapter. Fig. 4-1(b) shows in detail the tuning via and sensor electrode of the resonator before they are covered by the MEMS varactor as described in Section 2-1. Aside from the tapered input and output transitions, the resonator is similar to the cascaded resonators used in fixed-frequency SIW filters [2]. The overall size and shape of a four-pole *tunable* filter is the same as that of a four-pole *fixed-frequency* filter, shown in Fig. 4-1(c), without its resonators obscured by the MEMS varactors.

In this chapter, the measurement results of the closed-loop control of the MEMS varactor will be demonstrated. To this end, the packaged and wire-bonded CMOS control circuit will be supplied with necessary voltage sources and signal generators, and the V_{ERR} ,

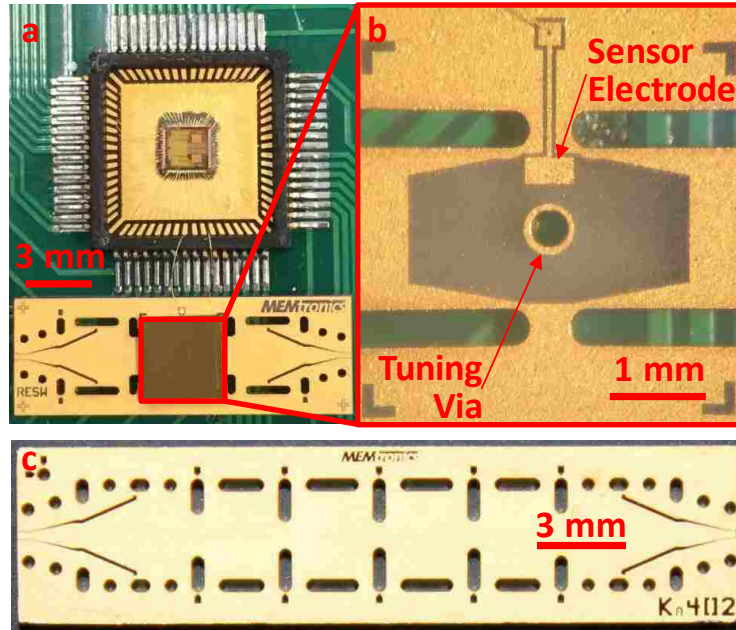


Fig. 4-1. Micrographs of (a) the packaged control circuit wire-bonded to a MEMS varactor, with the MEMS varactor flip-bonded on a tunable SIW resonator, (b) details of the resonator under the flip chip showing the tuning via and capacitance sensor, and (c) a four-pole SIW fixed-frequency filter without tuning vias or MEMS varactors.

V_{PI} , V_{MEMS} , as output of the circuit, will be measured to ensure the stability and zero steady-state error. Then, the robustness of the MEMS varactor with closed-loop control will be compared to that with open-loop control at difference ambient temperatures. Finally, the performance of the tunable single-pole SIW resonator realized by the MEMS varactor under closed-loop control will be evaluated. As mentioned before, since dielectric charging in MEMS varactors is not as severe as that in MEMS switches, the robustness of the present

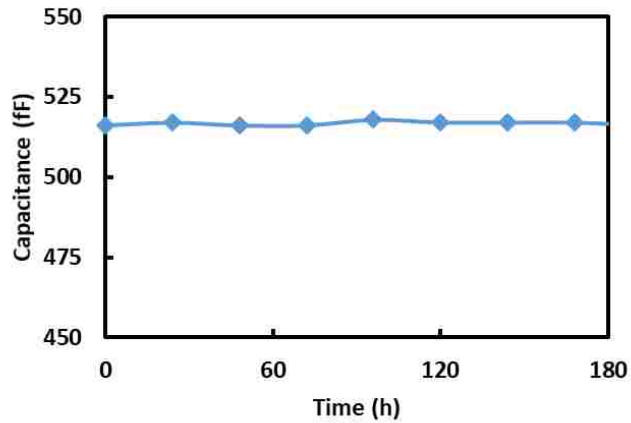


Fig. 4-2. Long-term measurement of the sensor capacitance C_{SENS} under constant MEMS varactor bias V_{MEMS} and at room temperature.

MEMS varactor under closed-loop control was not verified experimentally for dielectric charging issue. However, since the performance of the present CMOS circuit was verified experimentally, with some design modifications and employing intelligent control, it can be used for the MEMS devices whose $C-V$ characteristics significantly suffer from dielectric charging. Fig. 4-2 confirms that the present MEMS varactor shows no obvious dielectric charging. The sensor capacitance C_{SENS} was measured using a precision impedance analyzer while a 70-V constant bias voltage was applied for more than a week while the ambient temperature kept constant. As can be seen in the figure, there is no drift in the measured capacitance over a week whereas the capacitance of the MEMS switches

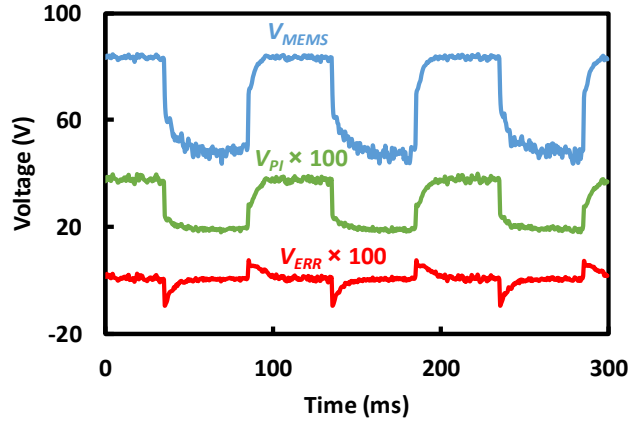


Fig. 4-3. Measured transient response of analog error signal V_{ERR} , PI controller output V_{PI} , and MEMS varactor bias V_{MEMS} when the target capacitance C_{TARG} is changed from 270 fF to 365 fF by tuning voltage V_{TUNE} .

drifts fast under similar tests [3], [4].

4.1 Demonstrated Closed-loop Control

With the control circuit wire-bonded to the MEMS varactor, Fig. 4-3 shows the measured analog error signal V_{ERR} , PI controller output V_{PI} , and MEMS varactor bias V_{MEMS} in response to a change in the tuning voltage V_{TUNE} . From the varactor C - V characteristics, the change in the tuning voltage V_{TUNE} corresponds to a change in the target capacitance C_{TARG} from 270 fF to 365 fF. However, the settling time is as long as 15 ms instead of the simulated 200 μ s shown in Fig. 2-10. The discrepancy is mainly due to the parasitics

introduced in the hybrid assembly of the control circuit with the MEMS varactor. Furthermore, since the actual MEMS varactor was tested unpackaged, it can have high damping ratio which results in slower dynamics in comparison with that assumed in the simulated model. On the other hand, measuring the output signals of the CMOS circuit with oscilloscope, requires probing which can add extra load capacitance to the circuit outputs. For example, bias capacitances of the MEMS varactors were measured to be a few picofarads while the probe used to measure the MEMS varactor bias V_{MEMS} has a capacitance of tens of picofarads. Beside monolithic assembly of the MEMS varactor and CMOS chip, as mentioned before, the fan-out capacity of the outputs in CMOS circuit can be increased to improve the dynamics of the system.

The control circuit chip consumes approximately 6 mW, which is very close to the simulated value of 5.2 mW. The power consumption can be reduced by omitting the extra circuits for monitoring and diagnosing internal-node signals such as Δt , V_{ERR} , and V_{PI} .

As mentioned before, ambient temperature variation causes drift in the C - V characteristics of the MEMS devices which limits their robustness [5]. Fig. 4-4 shows the measured C_{SENS} - V_{MEMS} characteristics of the present MEMS varactor under different ambient temperatures. It can be seen that under the same V_{MEMS} , higher temperatures make

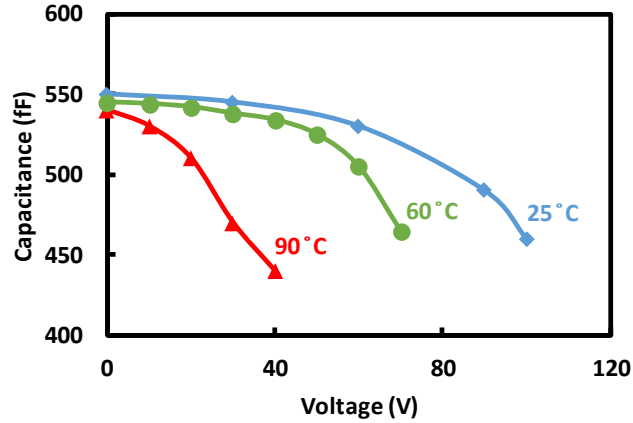
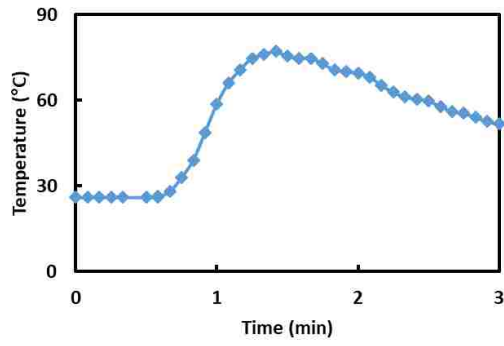
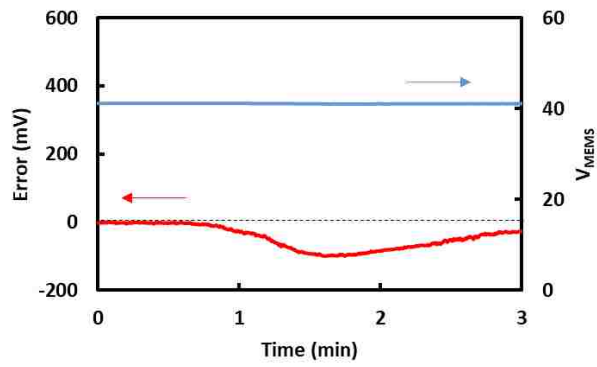


Fig. 4-4. Measured ambient temperature effect on C_{SENS} - V_{MEMS} characteristics of the capacitance sensor.

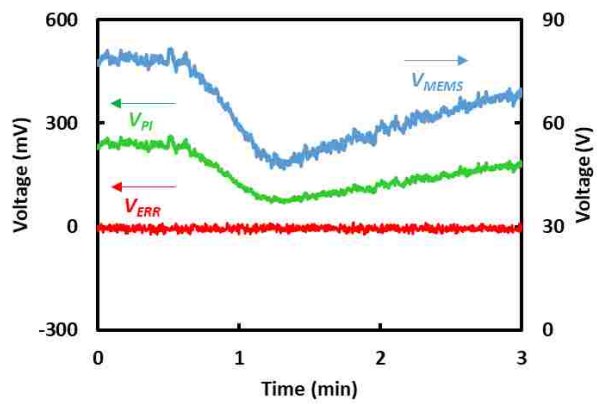
the silicon membrane softer, the bowing greater, and C_{SENS} smaller. However, by sensing the capacitance decrease, the closed-loop control circuit can adjust V_{MEMS} to maintain a constant C_{SENS} . Fig. 4-5 compares the performance of the MEMS varactor with and without closed-loop control for the ambient temperature variation shown in Fig. 4-5(a). As can be seen, for the MEMS varactor under open-loop control, the analog error signal V_{ERR} deviates from zero which means the MEMS varactor capacitance drift from the desired value as the temperature increases. On the other hand, for the MEMS varactor under closed-loop control, the analog error signal V_{ERR} is maintained at nearly zero implying that the MEMS capacitance C_{VARA} is kept nearly constant at 285 ± 5 fF by tuning the MEMS varactor bias V_{MEMS} provided by the CMOS control circuit for an ambient temperature rise from 25 °C



(a)



(b)



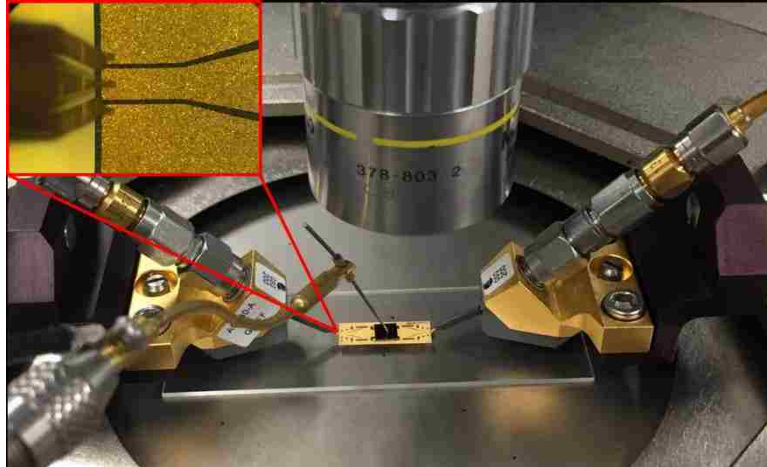
(c)

Fig. 4-5. Measured analog error signal V_{ERR} , PI output V_{PI} , and MEMS varactor bias V_{MEMS} for the MEMS varactor under (b) open-loop and (c) closed-loop control in response to (a) an ambient temperature rise from 25 °C to 80 °C then back down.

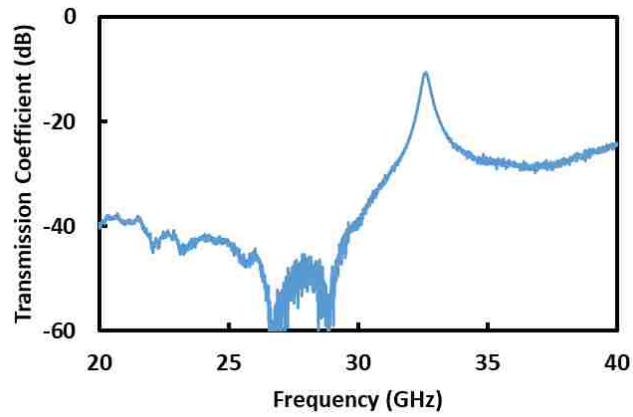
to 80 °C then back down. Furthermore, Fig. 4-5 implies that the control circuit is fast enough to compensate a temperature variation with rate of more than 118 °C/min.

4.2 Demonstrated Resonator Tuning

The closed-loop-controlled MEMS varactor with increased robustness and reliability was used to tune an SIW resonator as shown in Fig. 4-1(a). In order to evaluate the performance of the resonator alone, the frequency response of the resonator loaded with the MEMS varactor and without wire bonding to the CMOS control circuit was measured by Keysight Technologies N5247B PNA-X vector network analyzer and using a commercial RF probe station. As Fig. 4-6(a) shows, the radio-frequency (RF) signals were applied to the resonator using two air coplanar probes (ACP) while the bias voltage was applied to the MEMS varactor by a DC probe. As an example, Fig. 4-6(b) shows the measured frequency response of the resonator for the frequency range of 20 GHz to 40 GHz and under zero volt of MEMS varactor bias. As the figure shows, the resonance frequency lies in K_a band, and the quality factor of the tunable resonator, loaded with MEMS varactor, is on the order of 100, which is an order of magnitude better than that with most electronic MOS varactors [6]. This quality factor can be increased by improving



(a)

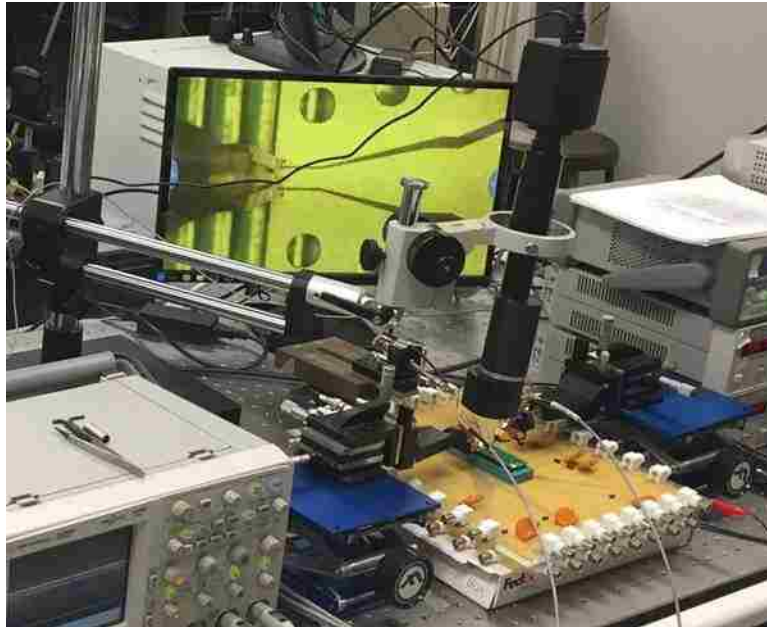


(b)

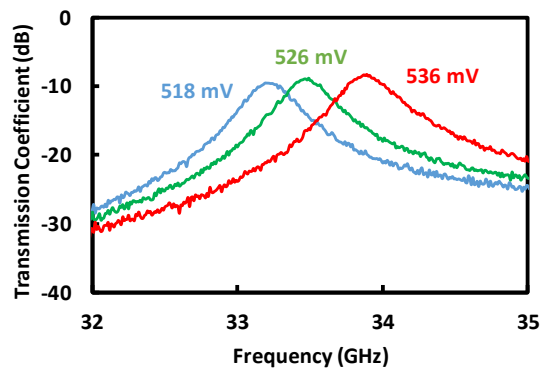
Fig. 4-6. (a) Measurement setup and (b) the measured frequency response of the single-pole SIW resonator with the MEMS varactor flip-mounted.

the contact of the MEMS varactor with the resonator which currency is lightly connected and results in high contact resistance.

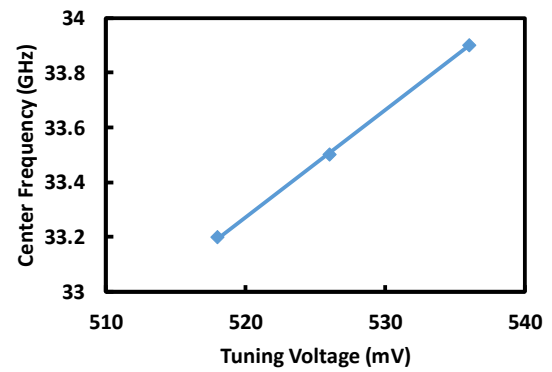
Because of large size of the PCB, the resonator with the MEMS varactor under closed-



(a)



(b)



(c)

Fig. 4-7. (a) Measurement setup including the homemade RF probe station. Measured (b) frequency response and (c) center-frequency shift of the close-loop-controlled resonator under different tuning voltages V_{TUNE} .

loop control could not be measured using the commercial RF probe station. Therefore, a

homemade RF probe station was designed and implemented as shown in Fig. 4-7(a). As can be seen, two laboratory scissor jacks were used to hold and adjust the RF probes along with an industrial microscope camera to monitor the RF probe landing. Fig. 4-7(b) shows the measured frequency response of the resonator with the MEMS varactor under closed-loop control for different values of the tuning voltage V_{TUNE} . Since MEMS varactor capacitance C_{VARA} cannot be measured directly, as mentioned before, the present RF measurement results implies that C_{VARA} is maintained constant around a target capacitance with the control circuit. As Fig. 4-7(c) shows, the center frequency is tunable from 33.2 GHz to 33.9 GHz by changing V_{TUNE} from 518 mV to 536 mV, corresponding to a tunable range of approximately 2%. The tuning range can be expanded by increasing the air gap between the silicon membrane and the silicon bulk or by decreasing the air gap between the silicon membrane and the tuning via. The former increases V_{MEMS} to above 100 V; the latter is challenging for assembly.

Fig. 4-8(a) shows that both the center frequency and quality factor of the MEMS-tuned resonator are nearly constant across an ambient temperature range 25–90 °C. Fig. 4-8(b) compares the center frequency shift of the closed-loop-controlled resonator with that without closed-loop control. It can be seen that, with closed-loop control, the

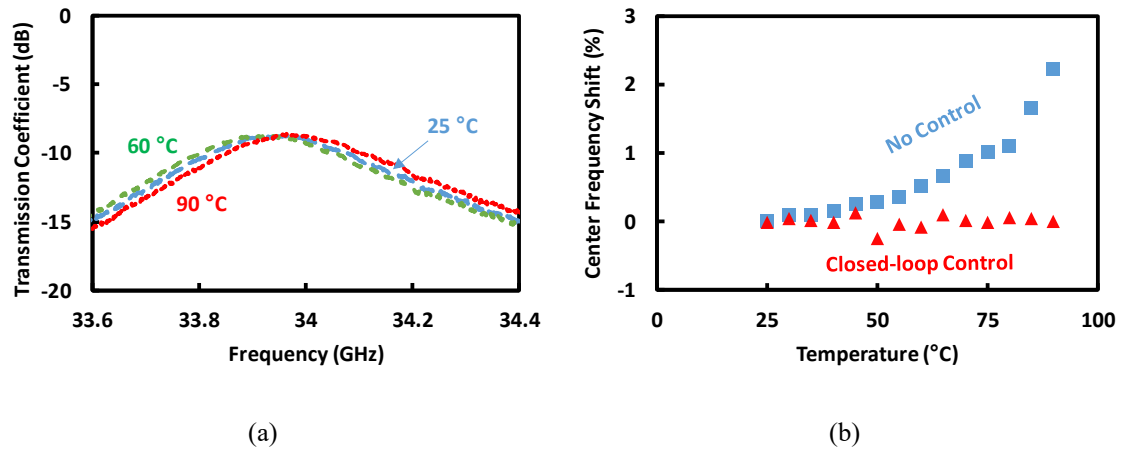


Fig. 4-8. Measured (a) frequency response and (b) center-frequency shift of the close-loop-controlled resonator under different ambient temperatures. In (b), the center-frequency shift of the tunable resonator under a constant bias voltage is included for comparison.

center frequency drift can be compensated to within $\pm 0.1\%$, which is an order-of-magnitude better than that without closed-loop control. With monolithic integration and parasitic reduction, significant improvement in the frequency stability can be expected under the present closed-loop control approach. Monolithic integration should be relatively straightforward, because presently both the control circuit and the MEMS varactor are built in the SOI technology. Additional improvement may result from closed-loop control of the filter frequency instead of the varactor capacitance, albeit at the expense of greater circuit complexity and power consumption.

Table 4-1 Temperature Stability of Closed-loop-controlled MEMS Resonators

Year	2010	2011	2015	2015	2018	2019
Control Mechanism	Ovenized	Electrostatic	Ovenized	Ovenized	Ovenized	Electrostatic
Integration	Hybrid	Hybrid	Monolithic	Monolithic	Hybrid	Hybrid
Temperature Range (°C)	-20 to 80	-10 to 80	-40 to 85	-40 to 80	-25 to 85	25 to 90
Ramp Rate (°C/min)	5	NA	NA	> 10	1.8	> 118
Frequency Stability (ppm)	±1	±2.5	< 120	0.3	±0.3	±1000
Power Consumption (mW)	137	NA	2	31	290	6
Reference	[7]	[8]	[9]	[10]	[11]	This Work

Table 4-1 compares the temperature stability of the present resonator with the state of the art. It is not a fair comparison because we could not find another closed-loop-controlled MEMS-tunable resonator used in a microwave or millimeter-wave filter, and all other resonators listed in Table 4-1 are used in a frequency standard below 1 GHz and mainly for oscillators in accurate timing applications. Furthermore, the reported MEMS control techniques in Table 4-1 are optimized only for temperature compensation whereas the present MEMS control approach can mitigate the effect of other aforementioned reliability issues as well. Nevertheless, it can be seen that although the frequency stability of the

present resonator is inferior to that of the other resonators, it consumes less power and responds faster, which is critical in filters for highly-modulated RF signals in modern wireless communication systems.

As experimentally demonstrated in this chapter, employing a CMOS circuit for controlling a MEMS varactor mounted on a single-pole SIW resonator in K_a band, results in a small, light, robust, reliable and tunable resonator which can be of a great interest for design of tunable filters for 5G wireless communication applications.

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Chapter 5 Conclusions

This dissertation explored the opportunity of CMOS closed-loop control for MEMS varactors. Detailed discussions on modeling, design, simulation, implementation, and experimental verification of the MEMS varactor and CMOS closed-loop control circuit were presented. Critical aspects of the design were highlighted, and novel approaches were introduced to overcome the challenges.

This chapter will conclude the dissertation by summarizing the results and main achievements. In addition, some recommendations for future studies on this topic will be provided.

5.1 Conclusions of This Dissertation

A closed-loop capacitance sensing and control mixed-mode circuit with dedicated sensor electrode and PI controller was designed to have a sensitivity of 1 fF, a settling time of 200 μ s, and a voltage capacity of 90 V. In a hybrid integration with a MEMS varactor, the circuit could control the varactor capacitance from 270 fF to 365 fF with an accuracy of 1.5%. Despite a relatively long setting time, the control circuit was able to maintain the

varactor capacitance to 285 ± 5 fF between 25 °C and 80 °C. Furthermore, with the varactor, as the tuning element of an SIW resonator, the control circuit could tune the resonance frequency from 33.2 GHz to 33.9 GHz, while keep them constant to within $\pm 0.1\%$ over the temperature range 25–90 °C. The control-circuit occupies an area of 1.7 mm² and consumes 6 mW. The implementation of the present closed-loop control of MEMS varactors in a quartz multi-pole SIW is a promising approach to realize tunable, small-size, light-weight, low-cost, robust, and reliable millimeter-wave filters that are critical to 5G and other future-generation wireless communication systems.

Monolithic integration of the control circuit with the MEMS varactor is relatively straightforward as both are built in the SOI technology. In the monolithic integration, simulation showed that the settling time could be improved to 200 μ s and be mainly limited by the mechanical resonance frequency of the MEMS varactor. Monolithic integration can also improve the frequency stability of the MEMS varactor. Additional improvement may result from closed-loop control of the filter frequency instead of the varactor capacitance, albeit at the expense of greater circuit complexity and power consumption. The tuning range of the resonator frequency can be expanded by increasing the air gap between the silicon membrane and the silicon bulk, or by decreasing the air gap between the silicon

membrane and the tuning via. The former increases V_{MEMS} to above 100 V; the latter is challenging for assembly. To handle 150 V, the monolithically integrated level shifter can be enlarged to drive the high-voltage switch to its limit.

5.2 Recommendations for Future Studies

In this dissertation, the closed-loop control technique was based on sensing the capacitance of the MEMS varactor, comparing that with a target capacitance value, and tuning the bias voltage of the MEMS varactor to keep the measured capacitance in a narrow range around the target value. Depending on the application, instead of just sensing the MEMS capacitance, a more effective approach is to measure the ultimate desired parameter, compare with the target value, and adjust the MEMS bias voltage to reach the target. For example, as mentioned before, for the MEMS application in tunable filters, the closed-loop control can be based on frequency response of the filter rather than varactor capacitance. In this way, since the center frequency of the filter itself without the MEMS varactor also drifts with temperature changes [1], the closed-loop control can compensate for that as well and make the frequency response of the filter stable against the temperature variations. There are several studies demonstrating CMOS integrated device

characterization systems [2], [3], and the main concern related to this approach is increased complexity and power consumption.

Another interesting approach is to explore the more advanced techniques of control for the MEMS. As showed in previous chapter, despite the parameters and environment temperature variations, a stable steady-state response without any steady-state error was achieved for the MEMS varactor using PI controller. However, the dynamic response of the MEMS varactor also can be significantly different for each fabricated device. In addition, tuning PI controller for the best dynamics of each MEMS varactor does not guarantee the optimized dynamic response in different temperature. Thus, depending on application requirements, a more advanced approach should be considered for these issues. There have been some studies to develop a learning control algorithm to eliminate the RF MEMS switches bounce in open-loop manner [4]. In this way, the waveform of the actuation voltage for the MEMS switch is tailored according to the iterative responses from the MEMS switch. Employing such techniques in closed-loop control of the MEMS varactor helps to tune the controller adaptively to achieve the fastest dynamic response despite the environment temperature and parameter variations of the MEMS device.

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Vita

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