**Lehigh University**
**Lehigh Preserve**

Theses and Dissertations

2013

# Intelligent CMOS Control of RF MEMS Capacitive Switches

Guanghai Ding
*Lehigh University*

Follow this and additional works at: http://preserve.lehigh.edu/etd

Recommended Citation
Ding, Guanghai, "Intelligent CMOS Control of RF MEMS Capacitive Switches" (2013). *Theses and Dissertations.* Paper 1225.

This Dissertation is brought to you for free and open access by Lehigh Preserve. It has been accepted for inclusion in Theses and Dissertations by an authorized administrator of Lehigh Preserve. For more information, please contact preserve@lehigh.edu.

# Intelligent CMOS Control of RF MEMS Capacitive Switches

by

**Guanghai Ding**

Presented to the Graduate and Research Committee
of Lehigh University
in Candidacy for the degree
of Doctor of Philosophy

in

Electrical Engineering

Lehigh University
January 2013

Approved and recommended for acceptance as a dissertation in partial fulfillment of the requirements for the degree of Doctor of Philosophy.

____________________________

**Date**

__________________________________________________

**Dr. James C. M. Hwang**, Dissertation Advisor, Chair

____________________________

**Accepted Date**

Committee Members

____________________________________

**Dr. Miltiadis Hatalis**

____________________________________

**Dr. Douglas Frey**

____________________________________

**Dr. Charles L. Goldsmith**

____________________________________

**Dr. Cristiano Palego**

# Acknowledgments

This dissertation would not have been possible without the advice, guidance, and encouragement from my advisor Prof. James C. M. Hwang, who has not only provided me with the exposure to a variety of advanced research topics, but also meticulously trained me to be an independent thinker throughout my graduate study at Lehigh. I would also like to thank Prof. Miltiadis Hatalis, Prof. Douglas Frey, Dr. Charles Goldsmith, and Dr. Cristiano Palego for their valuable support and feedback on my dissertation.

I am grateful to my former and current colleagues at Compound Semiconductor Technology Laboratory (CSTL), particularly Dr. Weike Wang, Dr. David Molinero, Dr. Subrata Halder, and Dr. Cristiano Palego who provided valuable contribution to this dissertation. I am also thankful to the help from Dr. Thomas Deng, Dr. Eric Chen, Dr. Steven Peng, Dr. Laura Jin, Dr. Francesco Solazzi, Dr. Caterina Merla, Xi Luo, and Yaqing Ning, who have made my graduate research at CSTL an enjoyable experience. I would also like to express my gratitude to Dr. Charles Goldsmith at MEMtronics Corp. for providing precious device samples and helpful discussions. Meanwhile, I also appreciate the IT support from David Morrisette.

I would like to acknowledge the support and help of Alain Duvallet and Dr. Steven Peng during my internship at Peregrine Semiconductor Corp., where I gained precious knowledge and understanding of silicon-on-insulator RF switch performance.

I owe my deepest gratitude to my family members, my wife Jinhan, my parents and grandparents in China, my aunts, my uncles, and my cousins. Finally, Lord is my light, my strength, and my salvation. Praise him, for he is good, and his love, grace, and faithfulness endure forever.

# Table of Contents

Acknowledgments ..... iii

List of Tables ..... viii

List of Figures ..... ix

Abstract ..... 1

Chapter 1. Introduction ..... 3

1.1 Principles of RF MEMS Capacitive Switches ..... 3

1.2 Solid-State Switches vs. RF MEMS Capacitive Switches ..... 6

1.3 Applications of RF MEMS Capacitive Switches ..... 7

1.4 RF MEMS Capacitive Switch Reliability and Robustness ..... 11

1.5 CMOS-MEMS Integration ..... 20

1.6 Organization of the dissertation ..... 22

References ..... 24

Chapter 2. Design of Integrated Closed-loop CMOS Control of RF MEMS Capacitive switches ..... 29

2.1 Principles of Closed-loop Bipolar Control of RF MEMS Capacitive Switches 30

2.2 Integrated Capacitance Sensing Technique ..... 32

2.3 High-Voltage Switching Technique ..... 38

2.4 Simulated Closed-loop Control ..... 43

References ..... 48

Chapter 3. CMOS Control Circuit Implementation and Verification ..... 51

3.1 Control Circuit Implementation ..... 52

3.2 Measurement Setup ..... 54

3.3 Experimental Verification of Control Circuit Functions ..... 56

References ..... 63

Chapter 4. Experimental Demonstration of Closed-loop Bipolar Control of RF MEMS Capacitive Switches ..... 64

4.1 Capacitance Sensing Results ..... 65

4.2 Capacitance Sensing Discussions ..... 71

4.3 Open-loop vs. Closed-loop Control ..... 73

4.4 Intelligent Bipolar Control ..... 76

References ..... 79

Chapter 5. Conclusions ..... 81

5.1 Conclusions of This Dissertation ........................................................ 81

5.2 Recommendations for Future Study ........................................................ 82

References ........................................................ 84

Publications ........................................................ 86

Vita ........................................................ 88

# List of Tables

Table 1-1 Device Characteristics Comparison of FET and RF MEMS Capacitive Switches........................................................................................................ 6

Table 4-1 Simulated vs. Measured Control-Circuit Performance ................................. 67

# List of Figures

Fig. 1-1. (a) Topview and (b) cross-sectional view of a capacitive coupling RF MEMS switch from Raytheon/Texas Instrument (TI) [1]........................................... 4

Fig. 1- 2. (a) MEMS capacitive switch based tunable low-pass π network with fixed inductor *L* and tunable capacitors *C1*, *C2*, and *C3*. (b) Simulated improvement of transducer gain $\Delta G_T$ (dB) for load reflection coefficient $0.5 \leq |\Gamma_L| \leq 0.9$ and $-180^o \leq \varphi(\Gamma_L) \leq 180^o$ at 700 MHz [10].................................... 9

Fig. 1-3. Measured capacitance-voltage *C(V)* characteristic of a typical RF MEMS capacitive switch in pristine and charged states........................................... 12

Fig. 1-4. (a) Charge injection under an applied voltage. (b) Bulk charges are discharging while surface charges very slowly. (c) After ~20 min, all bulk charges discharge, while surface charges remain [16]. ................................. 14

Fig. 2-1. Block diagram of the integrated closed-loop CMOS control of RF MEMS capacitive switches.......................................................................... 31

Fig. 2-2. (a) Schematics of capacitance-sensing scheme with (b) narrower $V_{COMP}$ pulse

for larger $C_{MEMS}$ due to longer discharging. .................................................. 34

Fig. 2-4. Under constant sensing period $T$ of 1 μs, sensitivity increases with increasing $C_{ISO}$ of (a) 1 pF, (b) 2 pF, (c) 5 pF, and (d) 10 pF. ........................................ 36

Fig. 2-3. At $C_{ISO}$ = 2 pF, sensitivity increases with increasing sensing period $T$ of (a) 0.5 μs, (b) 1 μs, (c) 2 μs, and (d) 3 μs. .......................................................... 37

Fig. 2-5. Schematic of high-voltage switch S, which consists of two twenty-eight 3.3-V PMOS and NMOS transistor stacks to sustain a maximum voltage drop of 80 V for each stack. ...................................................................................... 40

Fig. 2-6. (a) Distribution of 40V on 14 PMOS and NMOS transistors during MEMS a switch actuation/deactuation. (b) Source-drain voltage of each of the 28 PMOS transistors in the stack during MEMS a switch actuation and deactuation. (c) Gate-source control voltage to turn on/off each PMOS transistor in the stack simultaneously. .......................................................... 42

Fig. 2-7. Simulated $V(C)$ (symbols) and $C(V)$ (curves) characteristics by using the CMOS control circuit in conjunction with a large-signal transient model for the present MEMS capacitive switch. ......................................................... 44

Fig. 2-8. Simulated $C_{MEMS}$, $V_{MEMS}$ and $V_{TOGGLE}$ waveforms for closed-loop control of a

MEMS switch around a target capacitance of 570 fF (a) without and (b) with dielectric charging. (c) The same MEMS switch under open-loop constant bias voltage with dielectric charging. .......... 46

Fig. 2-9. Simulated intelligent bipolar control of MEMS switch, during which the sign of $V_{MEMS}$ was flipped whenever it drifted out of a preset boundary indicated by the shadow. $C_{TARGET}$ = 570 fF. .......... 47

Fig. 3-1. Layout schematic of a fraction of the on-chip logic circuit. .......... 53

Fig. 3-2. Optical micrograph of the 3×1.5 $mm^2$ circuit die implemented in 0.5 μm CMOS silicon-on-sapphire technology. .......... 54

Fig. 3-3. Measurement setup for bare CMOS chip probing without MEMS switch wire bonded. .......... 55

Fig. 3-4. (a) Bipolar actuation/deactuation under both $V^+$ and $V^-$ were verified by monitoring the $V_{SENSE}$ waveform. (b) On-chip voltage divider to allow $V_{MEMS}$ being monitored by $V_{SENSE}$ without being significantly perturbed. .......... 57

Fig. 3-5. *Hold* signal becomes logic low to stop the deactuation (a) when $V_{SENSE}$ drops below a reference signal $V_{REF}$ under $V^+$, and (b) when $V_{SENSE}$ ramps above

$V_{REF}$ under $V^{-}$ ........................................................................................ 58

Fig. 3-6. Pulse-width-modulated output of capacitance sensing under positive bias where $t_{PW}_C_{MEMS}$, the pulse width of $C_{MEMS}$, was fixed while $t_{PW}_C_{TARGET}$ kept decreasing as $C_{TARGET}$ kept increasing from the state where $C_{TARGET}$ was (a) much smaller to (b) $C_{TARGET}$ slightly smaller to (c) $C_{TARGET}$ slightly larger to (d) much larger than $C_{MEMS}$. The Charge/Discharge signal *C/D* changed from logic low when $C_{TARGET} < C_{MEMS}$ in (a) and (b) to logic high when $C_{TARGET} < C_{MEMS}$. ........................................................................................ 59

Fig. 3-7. With $C_{TARGET} < C_{MEMS}$, the Charge/Discharge signal *C/D* changed from logic high under (a) positive bias to logic low under (b) negative bias, both as an effort to lower $C_{MEMS}$ to meet $C_{TARGET}$. ........................................................ 60

Fig. 3-8. Verification of intelligent bipolar control based on on-chip logic functions. (a) Surface and bulk charging are detected when peak of $V_{SENSE}$ lies above and below a shadowed region set by two reference voltages $V_{REF_S}$ and $V_{REF_B}$, respectively. Bias polarity *P/N* flipped in the following cycle when the peak of an artificially applied $V_{SENSE}$ waveform lay (b) above $V_{REF_S}$, and (c) below $V_{REF_B}$. *P/N* kept its sign when (c) $V_{SENSE}$ peak lay in-between $V_{REF_S}$ and

$V_{REF_B}$ ........................................................................................................ 62

Fig. 4-1. Measured bias waveform of a MEMS switch under closed-loop control for a targeted capacitance around 438 fF. Insets show two pairs of MEMS switches and control circuits wire-bonded together in a ceramic package. ................. 65

Fig. 4-2. $V(C)$ characteristic (symbols) optimized by closed-loop CMOS control circuit vs. $C(V)$ characteristic (curves) measured by precision impedance analyzer of a MEMS capacitive switch in both pristine (——) and charged (- - -) states. ........................................................................................ 66

Fig. 4-3. (a) Specially modified MEMS switch with additional capacitance-sensing pad under movable electrode between center and ground conductors of a coplanar transmission line. (b) $C_{PAD}$ measured from the sensing pad as a proportional indicator of $C_{MEMS}$ ..................................................................... 69

Fig. 4-4. During an hour-long hold-down test with closed-loop control, $V_{MEMS}$ (♦) of the specially modified MEMS switch increased by approximately 3 V to compensate for dielectric charging while $C_{PAD}$ (■) was kept constant as measured by an impedance analyzer. .......................................................... 70

Fig. 4-5. Open-loop control (curves) vs. closed-loop control (symbols). Under open-loop control with a constant $V_{MEMS}$ of 30 V, $V_P$ increased by 6 V and $C_{MEMS}$ decreased by 90 fF in 12 h due to dielectric charging. Under closed-loop control, $V_{MEMS}$ closely tracked the increase in $V_P$ and maintained $C_{MEMS}$ around a $C_{TARGET}$ of 560 fF. ................................................................ 74

Fig. 4-6. Rate of dielectric charging under closed-loop control (symbols) vs. that under 20, 30, and 40 V DC after the switch was pulled in at 40 V DC. $C_{TARGET}$ = 460 fF. ........................................................................................................ 75

Fig. 4-7. Long-term hold-down test under intelligent bipolar control of a MEMS switch, during which the sign of $V_{MEMS}$ was flipped whenever it drifted out of a preset range of ±30 V. $C_{TARGET}$ = 550 fF. ..................................................... 78

Fig. 5-1. RF MEMS capacitive switch with separate electrodes for (a) RF and DC sensing/biasing, and (b) RF/DC biasing and sensing. .................................. 83

# Abstract

Closed-loop control of RF MEMS capacitive switches was demonstrated by using an intelligent CMOS circuit. The control was based on fine-tuning the bias magnitude of the switches according to the difference between sensed and targeted capacitances. Innovative designs were used to allow the CMOS circuit to sense low capacitance of tens of femto-farats, and to handle high voltage up to ±40 V.

Simulations were carried out to further study and optimize the CMOS circuit performance in terms of control sensitivity, speed, and high-voltage handling capability. A fast actuation/deactuation speed of 15 μs was achieved in simulation, with a capacitance sensing resolution of about 13 fF, which corresponds to a ±1% control accuracy of a switch with 550-fF down-state capacitance.

The control circuit was implemented in 0.5-μm CMOS silicon-on-sapphire technology. The CMOS die occupied an area of 3×1.5 $mm^2$, which was dominated by input/output and voltage regulation/protection circuits; the actual capacitance sense/control circuit was smaller than 0.1 $mm^2$. The entire circuit consumed 0.7 mW of

power during active sense/control, which could be significantly reduced with less frequent sense/control and more advanced CMOS technology.

For expeditious proof of such closed-loop control concept, hybrid integration approach was adopted, which significantly increased the parasitics and degraded the circuit sensitivity. Nevertheless, a control accuracy of ±2.5% was demonstrated on MEMS switches with 550-fF down-state capacitance. Under accelerated dielectric charging test, the circuit could intelligently adjust the bias voltage to compensate the switch dielectric charging effect and hold MEMS switch capacitance at the target value. Intelligence was also programmed to alternate the bias sign when its magnitude required to maintain the targeted capacitance drifted significantly due to dielectric charging. As a result, indefinitely operation of RF MEMS capacitive switch despite dielectric charging could be realized.

Such intelligent control could also be used to compensate for process variation, material creep, ambient temperature change, and RF power loading, which would make MEMS capacitive switches not only more reliable, but also more robust.

# Chapter 1. Introduction

Radio-frequency (RF) micro-electro-mechanical systems (MEMS) are micro-scale devices using mechanical movement to achieve RF functionality. Specifically, RF MEMS capacitive switches take advantage of the dramatic increase of shunt capacitance (from tens to hundreds or thousands of femtofarads) to shunt RF signals to ground when the metallic membrane is pulled down to be in contact with the switch dielectric deposited on the central signal line of a coplanar waveguide (CPW).

## *1.1 Principles of RF MEMS Capacitive Switches*

A typical RF MEMS capacitive switch is shown in Fig. 1-1 [1], where a thin aluminum alloy membrane is suspended over a silicon nitride ($SiN_x$) dielectric layer deposited on top of the bottom/lower electrode, which is also the signal path. The switch has dimensions of 120 μm in width and 280 μm in length. In the membrane up state, or the through state, there is an air gap between the dielectric and membrane, shown in the upper figure of Fig. 1-1(b), resulting in a small shunt capacitance on the order of tens of

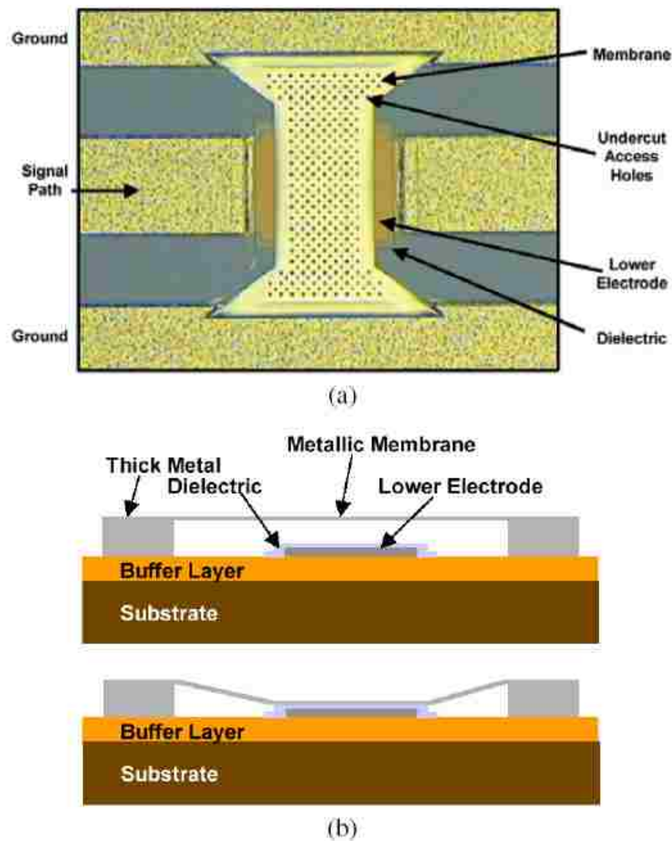



Fig. 1-1. (a) Topview and (b) cross-sectional view of a capacitive coupling RF MEMS switch from Raytheon/Texas Instrument (TI) [1].

femtofarads. As a result, most of the RF signal passes through the coplanar waveguide (CPW) signal line. When an electrostatic potential larger than 20 V is applied between the membrane and the bottom electrode, an attractive electrostatic force pulls the membrane down onto the bottom electrode, as shown in the lower figure of Fig. 1-1(b), causing a much bigger shunt capacitance as large as a few picofarads between the signal line

(bottom electrode) and ground (membrane). This pF capacitance in the down state, or the blocking state, makes the RF signal pass to the ground through the small impedance in-between, and thus blocks the RF signal from passing through the signal line.

A higher ratio of down-state capacitance $C_{\text{on}}$ and up-state capacitance $C_{\text{off}}$ is always preferred. A smaller $C_{\text{off}}$ leads to lower insertion loss in the through state of the switch, but requires a larger gap between the top membrane and bottom electrode, resulting in higher pull-down voltage. A larger $C_{\text{on}}$ is required to achieve higher isolation in blocking state, but requires more intimate contact between the membrane and dielectric film, which is done either by improving fabrication techniques or by applying higher voltage in the down state. However, due to the capacitive coupling nature, these switches are not suitable for low-frequency applications, because at low frequencies, $j\omega C_{\text{on}}$ is not big enough for isolation purpose. As a result, higher frequency will yield better isolation from capacitive coupling switches.

Typical switching time of RF MEMS capacitive shunt switches is about 3.5-5 μs. Though slow compared to FET and p-i-n switches, it is good enough for many radar and communication applications. The actuation voltage for membrane pull-down is 15-50 V, depending on different designs. Insertion loss in the through state is about 0.15 and 0.28

Table 1-1

Device Characteristics Comparison of FET and RF MEMS Capacitive Switches

| Device Characteristics | FET Switch[a] | RF MEMS Capacitive Switch [1] |
|---|---|---|
| Size ($mm^2$) | ~ 1 | ~0.05 |
| Actuation Voltage (V) | ~ 1V | ~ 40 V |
| Insertion Loss (dB) | 1 at 2 GHz | 0.15 at 10 GHz |
| | 2 at 6 GHz | 0.28 at 35 GHz |
| Isolation (dB) | -22 at 2 GHz | -15 at 10 GHz |
| | -20 at 6 GHz | -35 at 35 GHz |
| Power Handling (dBm) | 38 | 25 |
| Linearity ($OIP_3$ dBm) | 55 | > 70 |
| Switching Time (ns) | ~10 | ~ 5000 |
| Lifetime ($10^6$ cycles) | >100000 | ~500 |

[a]Average GaAs MMIC FET switches are used for comparison

dB at 10 and 35 GHz respectively. Isolation is about -15 and -35 dB at 10 and 35 GHz respectively [1].

## *1.2 Solid-State Switches vs. RF MEMS Capacitive Switches*

As stated in Table 1-1, for RF signal over 2 GHz, field-effect transistors (FETs) suffer from great insertion loss (typically larger than 1 dB) in through state, and poor isolation (typically -20 to -25 dB) in blocking state. In contrast, RF MEMS capacitive switches have the advantages of low insertion loss (0.28 dB up to 35 GHz), high isolation (<-40 dB over 35 GHz), near-zero power consumption, high-linearity, and potential for low cost.

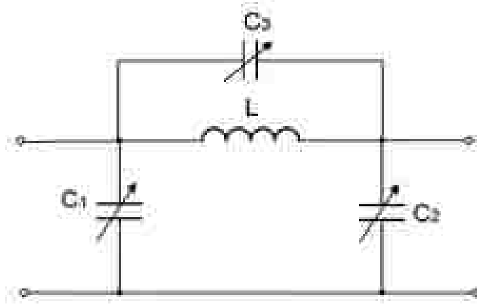
However, RF MEMS capacitive switches also have weakness in terms of switching speed (2-40 μs), reliability (0.1-10 billion cycle), power handling ability (<0.5 W), high-voltage drive (15-60 V), and hermetic packing requirement, which increases the overall cost for a packaged device [2], [3].

### *1.3 Applications of RF MEMS Capacitive Switches*

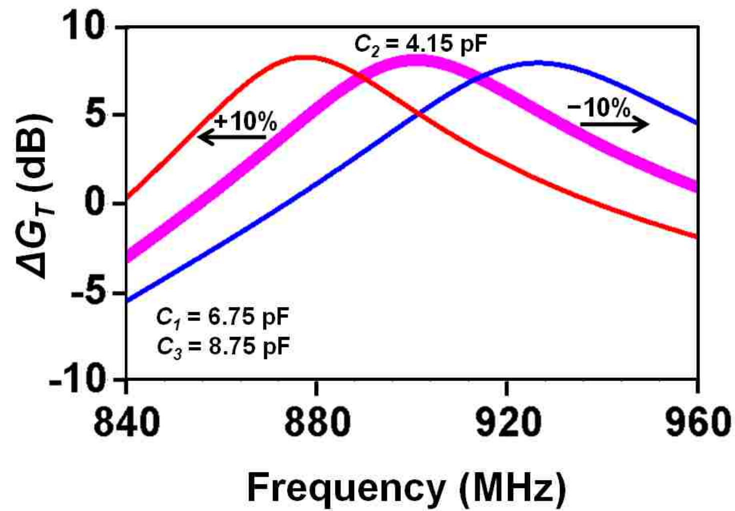
RF MEMS capacitive switches are promising building blocks for many essential components in future communication and radar systems. They have been a research focus since 1990s to replace phase shifters based on monolithic microwave integrated circuits (MMICs) for phased array antennas, a critical component for military, automotive radars, and space communication systems [4-7]. More recently, RF reconfigurable front-end, based on RF MEMS capacitive switches and varactors, has aroused intense interest in mobile handset industry, as the present RF front-end in mobile handsets becomes very bulky, lossy, and costly in order to incorporate multi-band and multi-mode wireless standards, such as GSM, EDGE, CDMA, W-CDMA, LTE, and other popular standards like global positioning system (GPS), Bluetooth, and Wi-Fi. For a conventional

transceiver in mobile handsets, for each new band added, the entire front-end architecture, including filters, power amplifiers (PAs), duplexers, isolators, and antenna matching networks, has to be duplicated. Moreover, antenna mismatch to PA, due to any environmental changes, would cause extra power loss or even damage to mobile handsets. With RF MEMS capacitive switch based digital tuning capacitor arrays in volume production already for antenna tuning and impedance matching in top-of-the-line smart phones and tablet PCs [8], [9], we can foresee more tunable RF components based on similar capacitive tuning principles, such as tunable filters, tunable duplexers, tunable PAs, tunable antennas, to render the conventional RF front-end more compact, power efficient, and cost effective.

Taking impedance matching for cellphone antennas as an example, because of the limited room for antenna in today's cellphone and environmental detuning effects, antenna load impedance is usually far from the ideal 50 Ω, resulting in high VSWR and high mismatch losses. In order to match the complex antenna load impedance to 50 Ω, tunable low-pass π network based on RF MEMS capacitive switches has been used [10]. A typical design of such π network is shown in Fig. 1- 2(a), where inductor $L$ = 6.8 nH, $C_1$, $C_2$, and $C_3$ are digital tunable capacitors, each consisting of seventeen RF MEMS




(a)




(b)

Fig. 1- 2. (a) MEMS capacitive switch based tunable low-pass π network with fixed inductor $L$ and tunable capacitors $C_1$, $C_2$, and $C_3$. (b) Simulated $\Delta G_T$ optimized for 900 MHz with $C_1$=6.75 pF, $C_2$=4.15 pF, and $C_3$=8.75 pF, while degraded matching performance at 900 MHz was shown for $C_2$ variation of ±10%.

capacitive switches with $C_{ON}/C_{OFF}$ = 0.5/0.1 pF, and one switch with $C_{ON}/C_{OFF}$ = 0.25/0.05 pF in parallel. This design makes each digital tunable capacitor in Fig. 1- 2(a) cover a tuning range from 1.75 pF to 8.75 pF with 0.2 pF step. As no MEMS tunable

inductor is practically available currently, in this π network with constant $L$, by tuning $C_3$ the resonance frequency of such parallel inductor-capacitor network can be tuned. Theoretically, with unbounded capacitor tuning range, a π network can provide perfect conjugate match of any impedance in the Smith chart at any frequency. However, for a matching network with finite capacitor tuning ranges, perfect conjugate match without loss only exists within a finite impedance domain in the Smith chart, outside of which, the matching network could still minimize the mismatch loss with limited tuning range.

Fig. 1- 2(b) shows the improvement of transducer gain $\Delta G_T$, or reduction of mismatch losses, due to the use of such π network to match an antenna load impedance $R_L$ = 30+$j$90 Ω to 50 Ω at 900 MHz. With $C_1$=6.75 pF, $C_2$=4.15 pF, and $C_3$=8.75 pF, $\Delta G_T$= 7.85 dB at 900 MHz. However, such ideal matching performance assumes accurate capacitance value at each tuning step as designed, which is still challenging currently due to reliability and robustness issues of RF MEMS capacitive switches. In real situation with process variation, dielectric charging, RF power loading, etc, the capacitance value could easily drift by 10 % from the designed value, causing not only fast detuning from the ideal matching condition, but also reduced tuning ranges, which together diminish the meaning of using such matching network. Fig. 1- 2(b) shows such fast detuning from the

ideal matching condition at 900 MHz due to ±10% variation of $C_2$ only. As a result, $\Delta G_T$ at 900 MHz dropped by about 3 dB. MEMS switches under reliability issues such as dielectric charging not only suffer from performance degradation, but will also eventually fail to operate due to stiction.

## *1.4 RF MEMS Capacitive Switch Reliability and Robustness*

Fig. 1-3 shows a measured capacitance-voltage $C(V)$ characteristic of a typical RF MEMS capacitive switch in both pristine and dielectric charged conditions. The hysteresis in the $C(V)$ is due to the fact that once a pull-in voltage $V_P$ is applied to pull the switch top membrane down, a bias as small as release voltage $V_R$ is enough to hold the membrane in down state. The $C(V)$ slope in down state is due to the presence of contact asperities, dielectric surface roughness, and metal membrane softness. With a larger applied bias, the membrane will be in more intimate contact with the dielectric, hence higher capacitance value. Ideally, one should expect a zero $C(V)$ slope in down state in case of a smooth contact, a metallized dielectric, or a stiff electrode, which is rarely the case in reality. As shown in Fig. 1-3 with the presence of a non-zero $C(V)$ slope in down

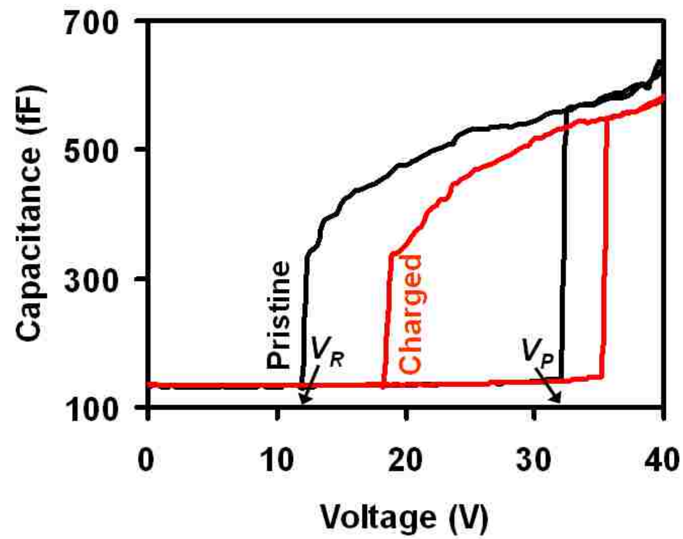



Fig. 1-3. Measured capacitance-voltage *C(V)* characteristic of a typical RF MEMS capacitive switch in pristine and charged states.

state, capacitance value changes with different applied bias. Moreover if a constant bias is applied regardless of *C(V)* shift induced by process variation, material creep [11], ambient temperature change [12], RF power loading [13], [14], dielectric charging [15-19], etc, the resulting capacitance value will drift away from the designed value, placing reliability and robustness issues on RF MEMS capacitive switches. Among all these issues, dielectric charging remains one of the toughest problems to tackle.

Dielectric charging occurs when the metallic membrane is being pulled down and closing the air gap between the dielectric layer and itself. Because of the constant potential applied during the actuation, electric field in the dielectric layer surges up to 3-5

MV/cm, resulting in Frenkel-Poole, Fowler-Nordheim, and other charge injections from metal into the dielectric [15]. The injection can be either from the asperities of the metallic membrane onto the dielectric surface or from the bottom electrode into the bulk of dielectric, causing surface and bulk charging, respectively [16]. Disregarding their polarity, surface charges, injected from metallic membrane onto the dielectric surface, will always increase the pull-down voltage of the membrane; while bulk charges, injected from bottom electrode into bulk of the dielectric, will always have adverse effect of decreasing the pull-down voltage. Consequently, RF MEMS capacitive switches suffering from surface charging will eventually have inadequate control voltage to pull down the membrane, while those suffering from bulk charging will result in stiction between the dielectric layer and metallic membrane, making the membrane unable to be released to the up position. In both situations, the switch fails.

In most cases, surface charging has a greater impact on switch operation than bulk charging. As shown in Fig. 1-4(a) [17], under an applied voltage, surface and bulk charges are injected onto the surface from the asperities of the membrane (movable electrode), and into the bulk of the dielectric from stationary electrode at the bottom, respectively. Upon removal of the applied voltage, shown in Fig. 1-4(b), the membrane

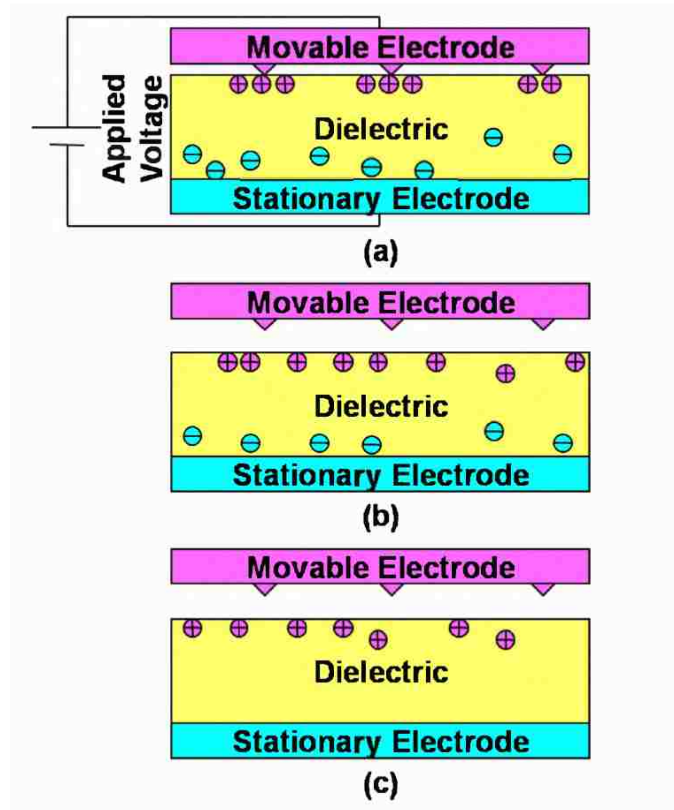



Fig. 1-4. (a) Charge injection under an applied voltage. (b) Bulk charges are discharging while surface charges very slowly. (c) After ~20 min, all bulk charges discharge, while surface charges remain [16].

springs back to its up position, when bulk charges readily discharge through the bottom electrode, whereas the surface charges have to discharge either vertically across the entire thickness of the dielectric or laterally across the entire surface of the dielectric. After approximately 20 minutes, shown in Fig. 1-4(c), all bulk charges discharge, while surface charges remain. It is found that bulk charges generally discharge in seconds or minutes, while surface charges discharge in hours or days. As the control cycle repeats, more and

more surface charges will accumulate on the dielectric surface through the asperities of the membrane.

It has been experimentally confirmed that bulk charging dominates in dry air. But surface conduction increases linearly with humidity which in turn enhances surface charging [18]. Due to the surface roughness of the membrane, injected surface charges can concentrate around asperities. Such concentration can prevent further charging through the same asperities unless it is dispersed. Humidity can enhance the surface charge conduction and allow the charge to migrate along the surface for a short distance (less than half of the distance between asperities). Such redistribution will enhance the surface charging. Since surface charges discharge very slowly and is detrimental to the lifetime of switches, it is critical to not only package switches in <1% relative humidity hermetically, but also optimize the surface chemistry of the switch dielectric to reduce its surface conductivity. Currently, even though hermetic packaging has been developed for RF MEMS capacitive switches, different amounts of moisture may still be inadvertently sealed in packages to impact the switch lifetime differently [19]. Improvement is to be made to the packaging process for more consistent yield.

There are other ways to minimize dielectric charging. For example, $SiN_x$ traps less

charge than silicon dioxide ($SiO_2$). However, it takes longer time to remove trapped charge from $SiN_x$ than $SiO_2$, indicating that charges are trapped at deeper energy levels in $SiN_x$ than in $SiO_2$ [2]. Therefore, their overall performance is comparable. Dielectric-less capacitive switches have also been developed [3]. Although those switches do not involve any dielectric layer subjected to large electric field, they do suffer from residual charging in the substrate that also shifts the pull-in and release voltage [4], [5]. Recently, ultra-nano-crystalline diamond (UNCD) thin films were adopted as the dielectric material for RF MEMS capacitive switches [20]. Experimental studies showed that charging appeared to be in the bulk rather than the surface of UNCD, and had a time constant of 95 μs, 5-6 orders of magnitude faster than that of $SiN_x$ and $SiO_2$. This implies that switches with UNCD dielectric pull down and immediately charge to failure. However, when the applied voltage is removed, the charges leave the dielectric very quickly, followed by the release of the membrane. More recent switches with UNCD dielectric kept in the pull-down state for 100 s will recover to their pristine condition in less than 50 μs. This implies that if switches are cycled off once out of every 100 second, they will be fully recovered to their pristine condition with no charging. Hence, near continuous switch operation without the scourge of dielectric charging is achievable with UNCD dielectric.

However, UNCD thin films currently suffer from high-stress induced delamination, and pin-hole effects. Significant efforts are required to make the material manufacturable with reasonable costs and good mechanical properties.

Another way to reduce dielectric charging is to reduce the actuation voltage of RF MEMS capacitive switches. It has been demonstrated that every 5 V reduction in actuation voltage could contribute to 10 times lifetime improvement [15], since smaller actuation voltages correspond to smaller peak fields at pull-down of membrane, results in exponential decrease of charge injection governed by Frenkel-Poole relation [21]. Nevertheless, low actuation voltage switches must have low spring constant, and thus low resorting (release) force, making it more susceptible to bulk charging. A good comprise is to design switches with actuation (pull-down) voltage about 20 V.

The use of complex control-voltage waveform, such as high-low [15] and bipolar [22] waveforms can also mitigate the dielectric charging problem. Because the actuation voltage is much larger than release voltage for a RF MEMS switch, high-low waveform control uses a voltage higher than the actuation voltage to pull down the membrane, then reduce it to a lower level (still larger than the release voltage) to hold the membrane in down position. The dielectric charging under high-low waveforms was modeled and

characterized with beneficial results compared to control waveforms with fixed amplitude [23]. Bipolar control waveforms work effectively in reducing dielectric charging by flipping the field orientation in each cycle to cancel the charging induced during the last cycle. But due to the subtle difference between positive and negative charging rate, a small amount of charges gradually build up and eventually will lead to device failure [24]. Thus, complete elimination of charging effect is still impossible.

Prior to 2001, the best capacitive switches have just reached 1 billon cycle mark [3]. All tests were done on-wafer, at 1-5 mW RF power, 1-10 KHz switching rate, and in nitrogen or dry-air environment. By 2007, capacitive switches developed by MEMtronics have resulted in stable operation to 100 billion cycles, at which time the test was stopped. The test was done at 0 dBm RF power at 35 GHz, with 30V stress in dry air environment. The switch tested was an unpackaged proximity switch (air-gap) [25], whose insulator is not a continuous sheet of dielectric, but patterned into a series of insulating, hexagonal posts approximately 4 μm across on an 8 μm pitch. The patterned dielectric bumps make the switch utilizing larger percent of air insulator than silicon dioxide, thus reducing the contact area accessible to dielectric charging. However, trade-off was made between $C_{on}$ and switch lifetime. However, great efforts are needed to push the lifetime to meet the

military requirement of 500 billion cycles.

Not only dielectric charging, but ambient temperature, and RF power induced self-heating, could also shift the actuation voltage, imposing a robustness issue on RF MEMS capacitive switches, especially for fix-fix beam capacitive switches shown in Fig. 1-1. As a result, a remarkable reduction in switch lifetime is common when tested at 50-100 mW RF power. The failure mechanism under medium or high power levels relates to heat generated under such RF power, and still needs further investigation. Actuation/pull-down voltage changes over ambient temperature results from the difference in thermal expansion coefficients between metallic membrane and substrate [26]. As the metallic membrane and substrate expand differently according to the temperature change, extra stress on the membrane is induced, and causes pull-down voltage change. More specifically, at membrane deposition temperature, there is a usually a compressive residual stress on the membrane. As the temperature decreases, due to the fact that metal generally has much larger thermal expansion coefficient than dielectric, the compressive stress first drops to zero and then turn to tensile stress, which keeps increasing as temperature drops to room temperature. The larger the tensile stress, the higher is the pull-down voltage of the membrane. But as temperature increases again, the

metallic membrane expands much faster than the dielectric substrate, causing decrease of tensile stress on the membrane, and thus pull-down voltage drop. Similar situation happens when RF power heating up the membrane locally, leading to pull-down voltage drop. There has been effort to replace Al with refractory metals such as molybdenum, which has much smaller thermal expansion coefficient than Al, to achieve ambient temperature robustness [27], at the expense of poorer thermal and electrical conductivity. As a result, RF MEMS capacitive switches with molybdenum membrane do show improved robustness against ambient temperature change, but comparable performance to those with Al membrane against RF power induced self-heating effect, because lower electrical and thermal conductivity of molybdenum membrane make heat being generated more easily and dissipated more difficultly, compensating its advantage in smaller thermal expansion coefficient.

## *1.5 CMOS-MEMS Integration*

Prior to RF switch application, MEMS accelerometers, gyroscopes, microphones, pressure sensors, and digital micro-mirrors have been widely used in automobile and

consumer electronics industry, where the integration of MEMS and integrated circuits (ICs) are essential to the overall performance of such MEMS products. ICs provide signal conditioning by sensing and amplifying the electrical signals generated by MEMS transducer, then converting the analog signals to digital format to interface with the rest of the system. In some cases, a closed-loop control can also be realized with electronic feedback circuitry.

Among different IC technologies, CMOS ICs have been the most popular one. Because most of the MEMS products adopt silicon as the mechanical material, CMOS-MEMS monolithic integration is feasible, which provides many advantages over hybrid integration involving wire bonding, such as much reduced assembly and packaging cost, and much reduced parasitics from bonding wires. However, careful process design is required to take into account the thermal and chemical budget of both CMOS and MEMS processes. Novel techniques are often necessary to reduce the process steps and to make MEMS process compatible to commercial CMOS foundry service.

There are three ways to integrate CMOS and MEMS monolithically, namely post-CMOS [28], intra-CMOS [29], and pre-CMOS [30] scheme, referring to the MEMS process is after, interleaved with, and before the CMOS process, respectively. While most

commercial MEMS inertial sensors adopt the traditional intra-CMOS process, which requires a dedicated BiCMOS process line, there are emerging novel intra-CMOS processes of RF MEMES capacitive switches that make MEMS process completely compatible with commercial CMOS foundries, because of the simple mechanical structures of RF MEMS capacitive switches being realized purely by metal and dielectric layers in conventional CMOS technology [31]. The RF MEMS capacitive switches monolithically integrated with CMOS charge pumps using this novel technique have been in volume production, and being used for antenna impedance matching in top-of-the-line smart phones.

## *1.6 Organization of the dissertation*

This dissertation further explores the advantages of CMOS-MEMS integration by utilizing CMOS circuit to not only actuate/deactuate the RF MEMS capacitive switches, but also sense and fine tune the switch capacitance to the target value despite *C-V* drift induced by dielectric charging, ambient temperature variation, RF power loading, and

process variation. As a result, RF MEMS capacitive switches under such closed-loop CMOS control have experienced much enhanced reliability and robustness.

Although intensive CMOS circuit design is involved, this dissertation focuses on the expeditious proof of the concept of closed-loop CMOS control of RF MEMS capacitive switches. Rigorous optimization of individual circuit component is beyond the scope of this dissertation. For the same reason, hybrid rather than monolithic integration of MEMS and CMOS circuit was adopted for fast concept verification.

The CMOS-MEMS integrated system design and simulation are discussed in Chapter 2, where simulation helped to optimize the circuit performance in accuracy and speed. The simulation results on closed-loop control performance are also presented and discussed in Chapter. Following the simulation, Chapter 3 presents the initial measured results of the fabricated CMOS circuit without MEMS switches wire-bonded, where all designed circuit functions essential for closed-loop capacitance sensing and tuning have been verified experimentally. After assembly, packaging, and wire-bonding, experimental demonstration of closed-loop CMOS control of RF MEMS capacitive switches is presented in Chapter 4, where the performance of such integrated CMOS-MEMS system

under accelerated dielectric charging has been investigated. Finally, the conclusions of this dissertation and recommendations for future research are presented in Chapter 5.

## *References*


1. Z. J. Yao, S. Chen, S. Eshelman, D. Denniston and C. Goldsmith, "Micromachined low-loss microwave switches," *Microelectromechanical Systems, Journal of,* vol. 8, pp. 129-134, 1999.
2. G. M. Rebeiz, "RF MEMS switches: Status of the technology," in *TRANSDUCERS, Solid-State Sensors, Actuators and Microsystems, 12th International Conference on, 2003,* 2003, pp. 1726-1729 vol.2.
3. G. M. Rebeiz and J. B. Muldavin, "RF MEMS switches and switch circuits," *Microwave Magazine, IEEE,* vol. 2, pp. 59-71, 2001.
4. G. M. Rebeiz, Guan-Leng Tan and J. S. Hayden, "RF MEMS phase shifters: design and applications," *Microwave Magazine, IEEE,* vol. 3, pp. 72-81, 2002.
5. S. Barker and G. M. Rebeiz, "Distributed MEMS true-time delay phase shifters and wide-band switches," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 46, pp. 1881-1890, 1998.
6. B. Pillans, S. Eshelman, A. Malczewski, J. Ehmke and C. Goldsmith, "Ka-band RF MEMS phase shifters for phased array applications," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2000. Digest of Papers. 2000 IEEE,* 2000, pp. 195-199.
7. A. Malczewski, S. Eshelman, B. Pillans, J. Ehmke and C. L. Goldsmith, "X-band RF MEMS phase shifters for phased array applications," *Microwave and Guided Wave Letters, IEEE,* vol. 9, pp. 517-519, 1999.

8. J. L. Hilbert, "RF-MEMS for Wireless Communications," *Communications Magazine, IEEE,* vol. 46, pp. 68-74, 2008.

9. Q. Gu and J. R. De Luis, "RF MEMS tunable capacitor applications in mobile phones," in *Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on,* 2010, pp. 635-638.

10. Qizheng Gu, J. R. De Luis, A. S. Morris and J. Hilbert, "An Analytical Algorithm for Pi-Network Impedance Tuners," *Circuits and Systems I: Regular Papers, IEEE Transactions on,* vol. 58, pp. 2894-2905, 2011.

11. M. van Gils, J. Bielen, and G. McDonald, "Evaluation of creep in RF MEMS devices," in *IEEE Int. Thermal, Mech.*, *Multi-Phys. Simulation and Experiments in Micro-Electron. Micro-Syst. Conf. Dig.*, Apr. 2007, pp. 1-6.

12. C. L. Goldsmith, and D. I. Forehand, "Temperature variation of actuation voltage in capacitive MEMS switches," *IEEE Microwave Wireless Components Lett.*, vol. 15, pp. 718-720, Oct. 2005.

13. C. Palego, J. Deng, Z. Peng, S. Halder, J. C. M. Hwang, D. I. Forehand, D. Scarbrough, C. L. Goldsmith, I. Johnston, S. K. Sampath, and A. Datta, "Robustness of RF MEMS capacitive switches with molybdenum membranes," *IEEE Trans. Microwave Theory Techniques*, vol. 57, pp. 3262-3269, Dec. 2009.

14. B. Pillans, J. Kleber, C. Goldsmith, and M. Eberly, "RF power handling of capacitive RF MEMS devices," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2002, pp. 329-332.

15. C. Goldsmith, J. Ehmke, A. Malczewski, B. Pillans, S. Eshelman, Z. Yao, J. Brank and M. Eberly, "Lifetime characterization of capacitive RF MEMS switches," in *Microwave Symposium Digest, 2001 IEEE MTT-S International,* 2001, pp. 227-230 vol.1.

16. Z. Peng, Xiaobin Yuan, J. C. M. Hwang, D. Forehand and C. L. Goldsmith, "Top vs. bottom charging of the dielectric in RF MEMS capacitive switches," in *Microwave Conference, 2006. APMC 2006. Asia-Pacific,* 2006, pp. 1535-1538.

17. Z. Peng, D. Molinero, C. Palego, J. C. M. Hwang, C. Moody, A. Malczewski and B. W. Pillans, "Effect of surface conduction on dielectric charging in RF MEMS capacitive switches," in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International,* 2010, pp. 1250-1253.

18. Z. Peng, C. Palego, J. C. M. Hwang, D. I. Forehand, C. L. Goldsmith, C. Moody, A. Malczewski, B. W. Pillans, R. Daigler and J. Papapolymerou, "Impact of humidity on dielectric charging in RF MEMS capacitive switches," *Microwave and Wireless Components Letters, IEEE,* vol. 19, pp. 299-301, 2009.

19. Z. Peng, C. Palego, J. C. M. Hwang, C. Moody, A. Malczewski, B. W. Pillans, D. I. Forehand and C. L. Goldsmith, "Effect of packaging on dielectric charging in RF MEMS capacitive switches," in *Microwave Symposium Digest, 2009. MTT'09. IEEE MTT-S International,* 2009, pp. 1637-1640.

20. C. Goldsmith, A. Sumant, O. Auciello, J. Carlisle, H. Zeng, J. C. M. Hwang, C. Palego, W. Wang, R. Carpick, V. P. Adiga, A. Datta, C. Gudeman, S. O'Brien and S. Sampath, "Charging characteristics of ultra-nano-crystalline diamond in RF MEMS capacitive switches," in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International,* 2010, pp. 1246-1249.

21. S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices.* Wiley-Blackwell, 2007.

22. J. R. Reid and R. T. Webster, "Measurements of charging in capacitive microelectromechanical switches," *Electronics Letters,* vol. 38, pp. 1544-1545, 2002.

23. X. Yuan, Zhen Peng, J. C. M. Hwang, D. Forehand and C. L. Goldsmith, "A transient SPICE model for dielectric-charging effects in RF MEMS capacitive switches," *Electron Devices, IEEE Transactions on,* vol. 53, pp. 2640-2648, 2006.

24. Z. Peng, Xiaobin Yuan, J. C. M. Hwang, D. I. Forehand and C. L. Goldsmith, "Dielectric charging of RF MEMS capacitive switches under bipolar control-voltage waveforms," in *Microwave Symposium, 2007. IEEE/MTT-S International,* 2007, pp. 1817-1820.

25. C. L. Goldsmith, D. I. Forehand, Z. Peng, J. C. M. Hwang and I. L. Ebel, "High-cycle life testing of RF MEMS switches," in *Microwave Symposium, 2007. IEEE/MTT-S International,* 2007, pp. 1805-1808.

26. C. L. Goldsmith and D. I. Forehand, "Temperature variation of actuation voltage in capacitive MEMS switches," *Microwave and Wireless Components Letters, IEEE,* vol. 15, pp. 718-720, 2005.

27. C. Palego, Jie Deng, Zhen Peng, S. Halder, J. C. M. Hwang, D. I. Forehand, D. Scarbrough, C. L. Goldsmith, I. Johnston, S. K. Sampath and A. Datta, "Robustness of RF MEMS Capacitive Switches With Molybdenum Membranes," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 57, pp. 3262-3269, 2009.

28. W. Yun, R. T. Howe and P. R. Gray, "Surface micromachined, digitally force-balanced accelerometer with integrated CMOS detection circuitry," in *Solid-State Sensor and Actuator Workshop, 1992. 5th Technical Digest., IEEE,* 1992, pp. 126-131.

29. T. Core, W. Tsang, and S. Sherman, "Fabrication technology for an integrated surface-micromachined sensor", *Solid State Technol.*, pp.39 -47, 1993.

30. J. H. Smith, S. Montague, J. J. Sniegowski, J. R. Murray and P. J. McWhorter, "Embedded micromechanical devices for the monolithic integration of MEMS with CMOS," in *Electron Devices Meeting, 1995., International,* 1995, pp. 609-612.

31. S. P. Natarajan, S. J. Cunningham, A. S. Morris and D. R. Dereus, "CMOS integrated digital RF MEMS capacitors," in *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2011 IEEE 11th Topical Meeting on,* 2011, pp. 173-176.

# Chapter 2. Design of Integrated Closed-loop CMOS Control of RF MEMS Capacitive switches

The most critical design of the control circuit concerns sensing of very small capacitance variation (tens of fF) and isolation of high voltages (~100 V). While CMOS circuits for capacitance sensing have been widely used in MEMS sensors, they are usually for lower voltages (a few volts) and higher capacitances (a few pF) than usually encounter in MEMS capacitive switches [1], [2]. The novelty of this design of CMOS control circuit lies in the handling of high voltages by using low-voltage (3.3 V) CMOS technology and a unique capacitance sensing technique that can convert the capacitance value into a pulse-width-modulated digital output with very high accuracy and speed in real time. Besides those novel circuit components, this design has also adopted multiple conventional mixed-signal circuit components such as accurate μA current sources [3], high-gain voltage comparators [4], etc.

In this chapter, we will first illustrate the principles of the closed-loop CMOS control of RF MEMS capacitive switches by examining the system block diagram. Then we will introduce the novel capacitance sensing technique we have developed, followed

by how the design handles the very high control voltage of MEMS switches. Finally, the simulation results of the integrated closed-loop control will be presented, where optimization of system level control performance will be investigated.

## *2.1 Principles of Closed-loop Bipolar Control of RF MEMS Capacitive Switches*

Fig. 2-1 shows the block diagram of the CMOS control circuit, which can bias a MEMS switch by positive or negative $V_{MEMS}$ supplied by $V^+$ or $V^-$. To minimize dielectric charging, the MEMS switch is actually controlled by charge instead of voltage [5]. The MEMS switch is turned on and off by a proportional control signal $V_{TUNE}$. $C_{MEMS}$ is sensed periodically and converted into a pulse-width-modulated digital output, which is then compared to that of $C_{TARGET}$ set by $V_{TUNE}$ in reference to an on-chip capacitor $C_{REF}$. Based on the comparison, switch S toggles between $V^+$ and $V^-$ to increment or decrement $V_{MEMS}$ to hold $C_{MEMS}$ around $C_{TARGET}$. For positive $V_{MEMS}$, if $C_{MEMS} < C_{TARGET}$, then S will momentarily switch to $V^+$ to increment the charge across the MEMS switch, hence, $V_{MEMS}$ and $C_{MEMS}$. If $C_{MEMS} > C_{TARGET}$, then S will momentarily switch to $V^-$ to decrement the charge, hence, $V_{MEMS}$ and $C_{MEMS}$. For negative $V_{MEMS}$, S functions similarly except

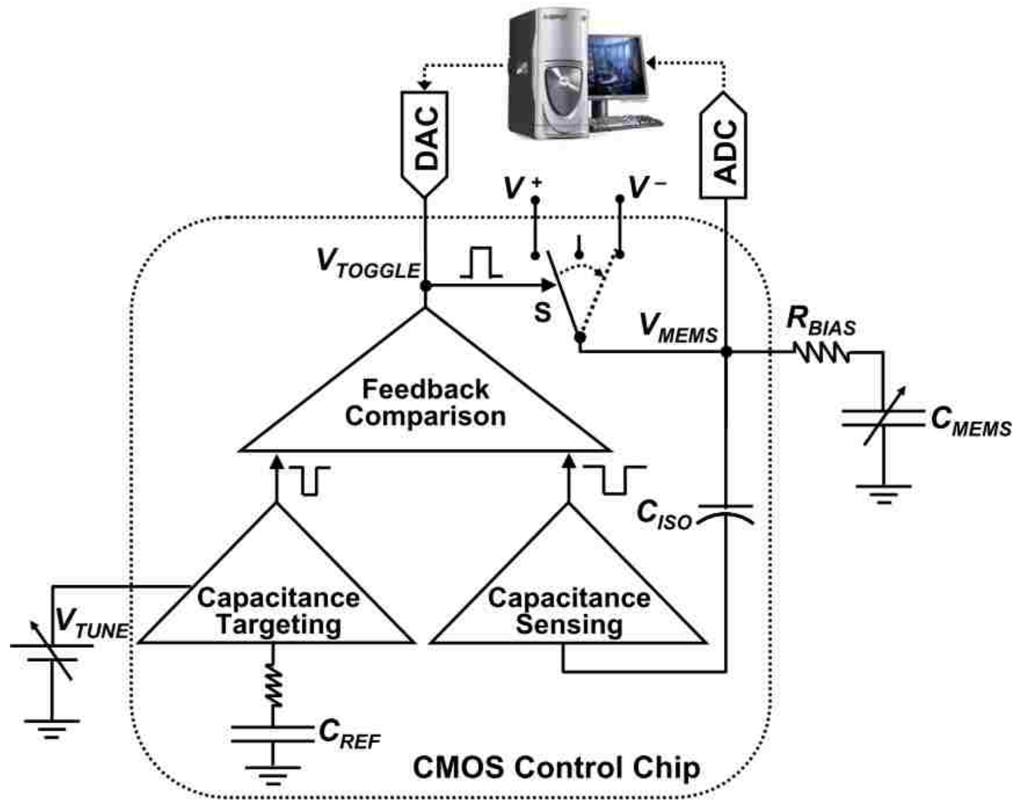



Fig. 2-1. Block diagram of the integrated closed-loop CMOS control of RF MEMS capacitive switches.

switching in the opposite manner. When $V_{TUNE}$ returns to zero, the MEMS switch is turned off by discharging $V_{MEMS}$ to zero.

Due to the closed-loop control, $V_{MEMS}$ magnitude required to hold $C_{MEMS}$ around $C_{TARGET}$ will either increase/decrease upon surface/bulk dielectric charging. By setting a safe operation region while momentarily monitoring the drift of $V_{MEMS}$, once $V_{MEMS}$ drifts out of a preset boundary, the sign of control voltage $V_{MEMS}$ will be flipped to cancel off

the previously accumulated charges in the dielectric. As a result, MEMS switches under such closed-loop bipolar control can operate indefinitely despite dielectric charging. The command of flipping the sign of $V_{MEMS}$ triggered by large enough $V_{MEMS}$ drift can be accomplished either by built-in on-chip logics of CMOS circuit or off-chip analog-to-digital convertor (ADC), digital-to-analog convertor (DAC), and computer programmed intelligence.

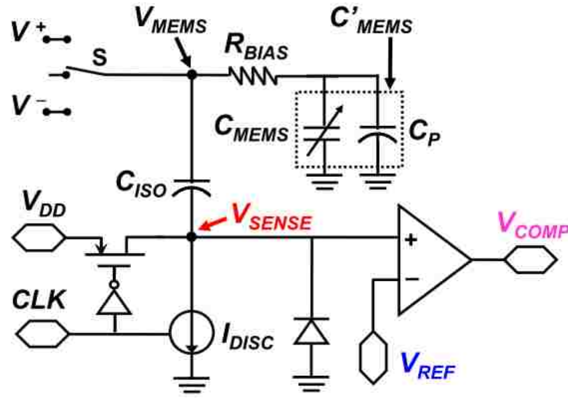
In the present design, $V^{+}$ and $V^{-}$ are provided by off-chip power supplies of ±40 V, which, if necessary, can be replaced by on-chip charge pumps as previously demonstrated [6]. To withstand a maximum voltage of 80 V, switch S comprises stacks of twenty-eight pairs of 3.3-V PMOS and NMOS transistors.

## *2.2 Integrated Capacitance Sensing Technique*

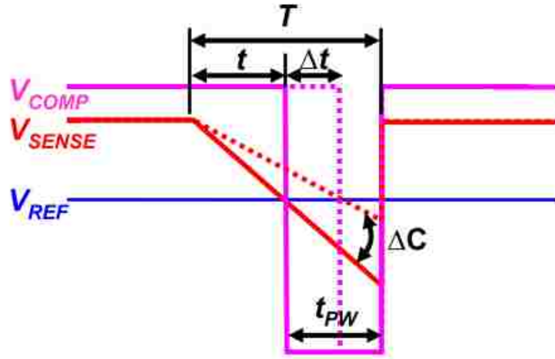
There have been various integrated capacitance sensing approaches by using RC or LC oscillators [7], [8], synchronous demodulators [9], trans-impedance amplifiers [10], capacitive feedback amplifiers [11], and switched-capacitor sampling networks [12], [13], among which the switched-capacitor network is the most widely used architecture due to

its accuracy and compatibility with CMOS technology. However, all of these techniques involve some high-frequency AC signals either applied to or generated by the capacitor under test, which, while causing no problem to MEMS sensors, could cause significant interference to RF switch application. Moreover, most of these listed techniques require a balanced capacitor pair or bridge to enhance sensitivity and suppress electromagnetic interference. While such balanced structures can be easily realized by using interdigitated fingers of MEMS sensors, they are not compatible with RF MEMS switches without significant switch design modifications.

Fig. 2-2(a) illustrates the present capacitance-sensing scheme. The time $T$ it takes to sense $C_{MEMS}$ is only a small fraction of the 1-MHz clock cycle, which is much faster than the mechanical resonance (~100 kHz) of the MEMS switch, so that sensing does not significantly perturb the mechanical state of the switch. During sensing, S is switched off to isolate $V_{MEMS}$ from $V^{+}$ and $V^{-}$, and the clock signal $CLK$ is at logical low to isolate the $V_{SENSE}$ node from the supply $V_{DD}$. Meanwhile, a current source $I_{DISC}$ is turned on to discharge $C_{MEMS}$ (plus any parasitic capacitance $C_P$) through isolation capacitor $C_{ISO}$ with a constant current level of a few micro-amperes. This causes the voltage $V_{SENSE}$ to drop steadily from $V_{DD}$ to the reference voltage $V_{REF}$ in time




(a)




(b)

Fig. 2-2. (a) Schematics of capacitance-sensing scheme with (b) narrower $V_{COMP}$ pulse for larger $C_{MEMS}$ due to longer discharging.

$$t = C_{TOT} \cdot \Delta V / I_{DISC} \tag{2-1}$$

where $\Delta V = V_{DD} - V_{REF}$ is the amount of $V_{SENSE}$ drop before it hits $V_{REF}$, and $C_{TOT} = C'_{MEMS}C_{ISO}/(C'_{MEMS} + C_{ISO})$, where $C'_{MEMS} = C_{MEMS} + C_P$. As illustrated in Fig. 2-2(b), the falling edge of the comparator output $V_{COMP}$ is triggered when $V_{SENSE}$ drops to $V_{REF}$, while

its rising edge is synchronized with the end of the sensing period. Thus, a negative $V_{COMP}$ pulse of width $t_{PW} = T - t$ is formed, with $t_{PW}$ changing by $\Delta t = \Delta C \cdot V_D / I_{DISC}$ when $C_{TOT}$ changes by $\Delta C$.

The sensitivity of such technique is defined as

$$s = \Delta t / \Delta C_{MEMS} \tag{2-2}$$

Assuming only $C_{MEMS}$ is voltage-dependent, and $\Delta C << C_{MEMS}$, we can have

$$s = \frac{\Delta V}{I_{DISC}\left(1 + \frac{C'_{MEMS}}{C_{ISO}}\right)^2} \tag{2-3}$$

According to (2-1), $\Delta V / I_{DISC} = t / C_{TOT}$, therefore the sensitivity can be express as

$$s = \frac{t}{C'_{MEMS}\left(1 + \frac{C'_{MEMS}}{C_{ISO}}\right)} \tag{2-4}$$

According to (2-4), $s$ can be enhanced by increasing $t$ or $C_{ISO}$, while minimizing $C_P$. However, $t$ is bound by the sensing period $T$, while $T$, in turn, is bound by the mechanical resonance of the MEMS switch. Further, too large a $C_{ISO}$ makes switching actually slower than the mechanical resonance. The reference capacitance $C_{REF}$ is sensed in a similar fashion and the resulted $t'_{PW}$ is scaled by $V_{TUNE}$ before comparison with $t_{PW}$ of $C_{MEMS}$ for closed-loop control.

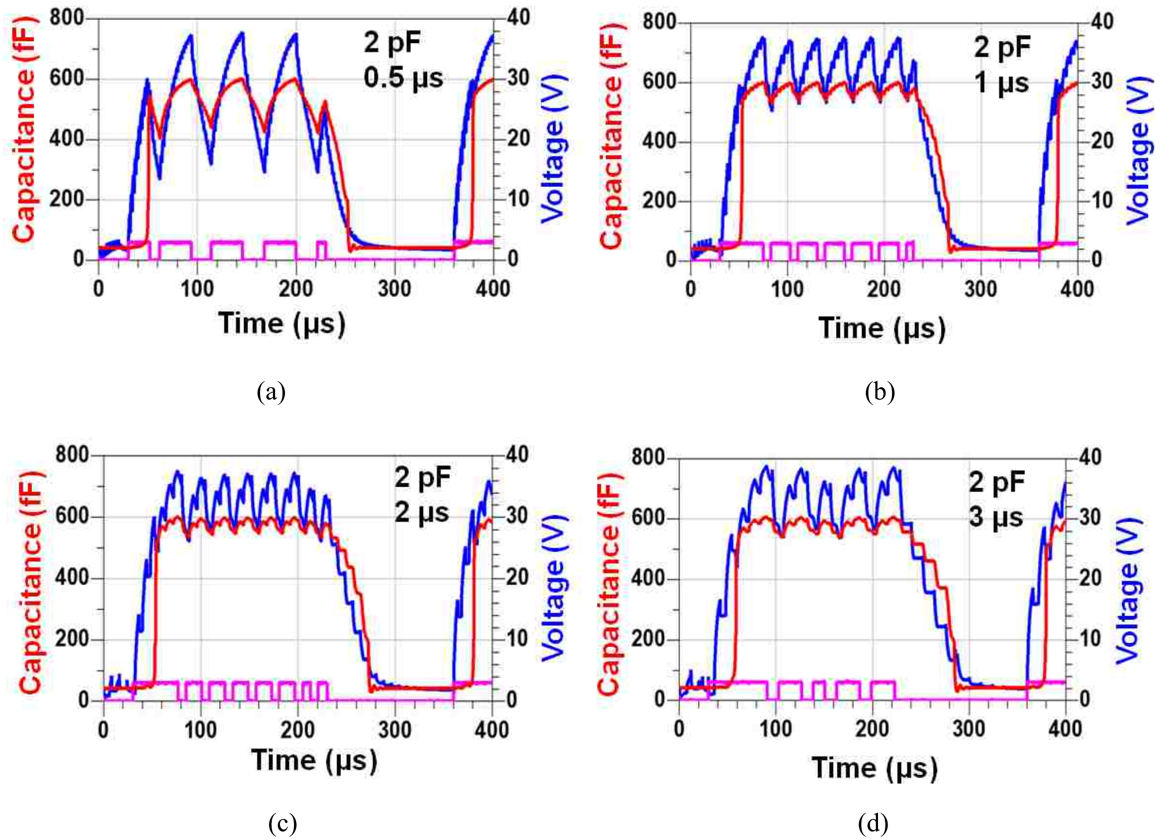



Fig. 2-3. At $C_{ISO}$ = 2 pF, sensitivity increases with increasing sensing period $T$ of (a) 0.5 μs, (b) 1 μs, (c) 2 μs, and (d) 3 μs.

As shown in Fig. 2-4, at constant $C_{ISO}$ of 2 pF, sensitivity improves significantly when sensing period $T$ increases from 0.5 to 1 μs, but followed by marginal improvement from 1 to 3 μs. This is because under a constant discharge current $I_D$, a sensing period around 1 μs already allows $V_{SENSE}$ to linearly decrease to nearly zero. Further increasing sensing period will not make $\Delta V$ even larger. Fig. 2-4 shows when $T$ is fixed at 1 μs,

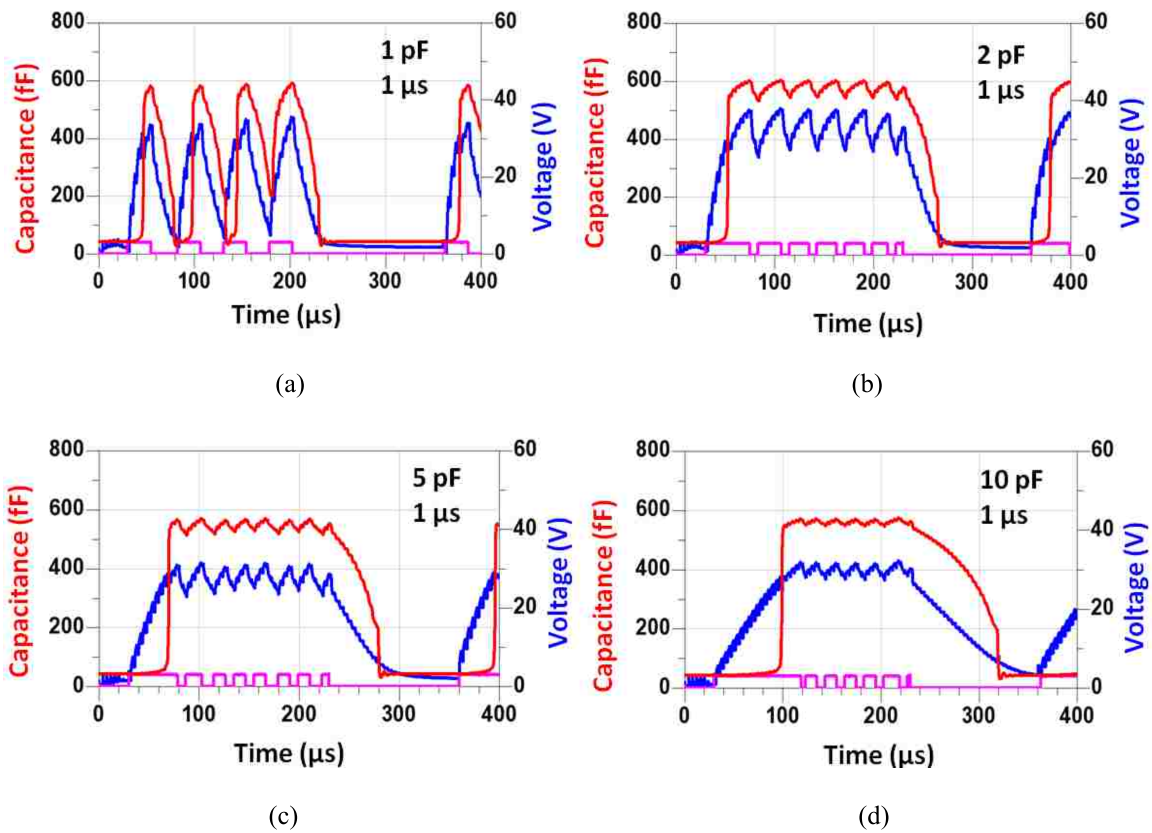



Fig. 2-4. Under constant sensing period $T$ of 1 μs, sensitivity increases with increasing $C_{ISO}$ of (a) 1 pF, (b) 2 pF, (c) 5 pF, and (d) 10 pF.

sensitivity increases significantly when $C_{ISO}$ increases from 1 to 2 pF, but only increases slightly with $C_{ISO}$ further increase, which is in good agreement with the behavior predicted by (2-4). Fig. 2-4 also shows that though a larger $C_{ISO}$ generally leads to better sensitivity, it will slow down the actuation/de-actuation. A choice of $C_S$ =5 pF makes a good compromise between sensitivity and speed.

## *2.3 High-Voltage Switching Technique*

Integrated high-voltage or high-power switches has applications in RF front-ends [14], DC-DC converters, switch mode power supplies, audio amplifiers, LCD and LED drivers, motor controllers, piezoelectric controllers, electrostatic MEMS controllers [15], etc. There are generally two ways to handle on-chip high voltages and high powers: device techniques like HVCMOS [16], [17] or lateral double-diffused MOS (LDMOS) [18] and circuit techniques such as FET stacking [19-22]. With the scaling of MOSFET technology into deep sub-micron regime, device level approach has become less effective and popular because the requirement of high-voltage capability contradicts with more advanced process technology with much thinner gate dielectric, optimized for minimum power consumption, maximum speed and integration density. As most high power/voltage applications require high-voltage actuation with low-voltage control circuitry, monolithic approach would require extra masks, process steps, and design considerations to integrate high-voltage technology with low-voltage sub-micron processes [23], [24].

Depending on different applications, FET stacking can take on different circuit topologies. The most common one works as a voltage leveler, which involves placing

several FETs in series, with one end of the stack grounded and the other at a constant high voltage. However, for current actuation/deactuation of MEMS switches, the FET stack has to work as a current switch in series with MEMS capacitor and high-voltage sources. As a result, while one end of the stack is tied to the constant $V^+$ or $V^-$, the other end butts $V_{MEMS}$, which changes constantly during an active control cycle. Especially, $V_{MEMS}$ ramps up/down drastically during actuation/de-actuation. Those transistors in the stack closest to the MEMS switch are most vulnerable to the fast $V_{MEMS}$ variation, which will cause breakdown if not distributed quickly and evenly throughout the stack.

The detailed schematic of switch S in the block diagram of Fig. 2-1 is shown in Fig. 2-5, where S consists of two PMOS and NMOS transistor stacks, named $S_P$ and $S_N$, respectively. For normal MEMS operation, $V^+$ and $V^-$ of ±40 V are required. In extreme cases when $V_{MEMS}$ reaches supply limit, a net 80 V voltage drop will be imposed on either $S_P$ or $S_N$. In order for $S_P$ and $S_N$ to sustain a maximum voltage drop of 80 V, each stack consists of twenty-eight 3.3-V transistors.

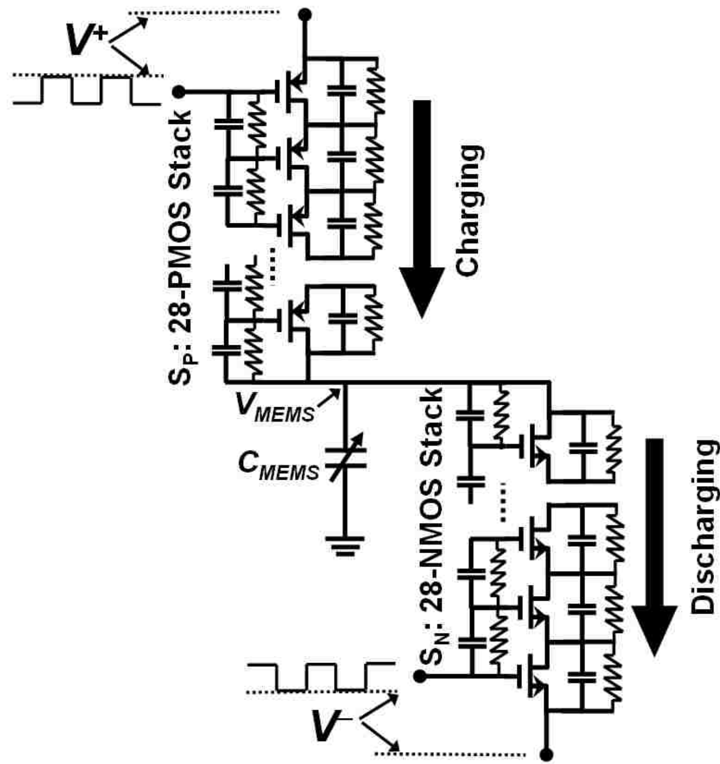


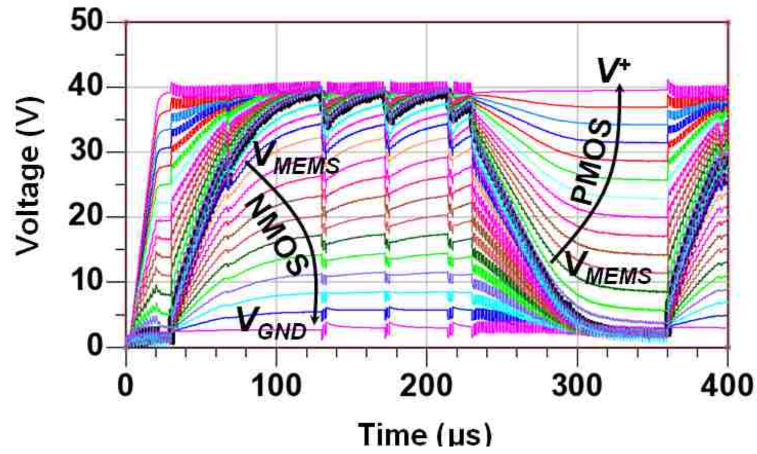

Fig. 2-5. Schematic of high-voltage switch S, which consists of two twenty-eight 3.3-V PMOS and NMOS transistor stacks to sustain a maximum voltage drop of 80 V for each stack.

With the large number of transistors in the stack, it becomes challenging to synchronize the turn-on and turn-off all stacking transistors. If some transistors in the stack are turned on slightly earlier than the others, there will be a transient moment when those transistors been already turned on will have much less voltage drop than the others that still remain off. As a result, a transient voltage exceeding breakdown might impose to

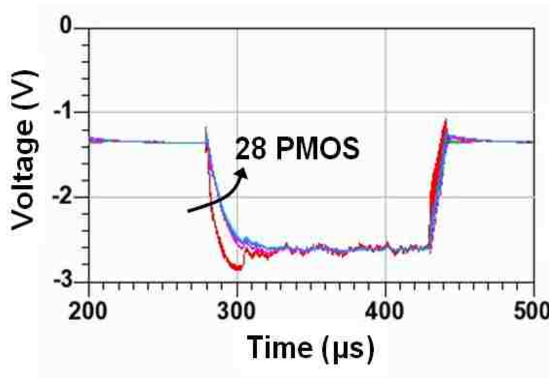
those transistors still in off condition. Similar transistor breakdown will happen if, during a transient moment, some transistors are just turned off when the others still remain on.

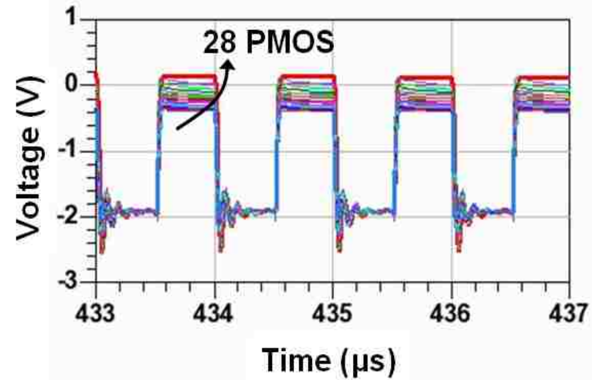
In Fig. 2-5 both resistors and capacitors are used to balance the voltage statically and dynamically. Uniform resistive network helps to maintain a proper biasing condition by distributing static voltage evenly across the stack. Meanwhile, non-uniform capacitive network helps to synchronize the switching of transistors in the stack, and ensure the even distribution of transient voltage. To keep the leakage current through resistive network at minimum, each resistor in Fig. 2-5 has a 3 MΩ value. 28 of them in series will end up with a total 84 MΩ resistance on source-drain and gate sides of each stack. Assuming a 40 V voltage drop on each stack, the total leakage current will be only about 1 μA.

Fig. 2-6(a) shows the unipolar supply voltage of 40 V and 0 V for $V^+$ and $V^-$ are distributed evenly across $S_P$ and $S_N$, which contain only 14 PMOS and NMOS transistors, respectively. Fig. 2-6(b) shows that under bipolar condition with ±40 V supply, the source-drain voltage of each of the 28 PMOS transistors are kept equal and well within 3 V to avoid breakdown. During a hold-down cycle, switch S dithers between $V^+$ and $V^-$ to fine-tune $V_{MEMS}$, which requires $S_P$/$S_N$ to turn on/off or off/on to increment or decrement




(a)




(b) (c)

Fig. 2-6. (a) Distribution of 40V on 14 PMOS and NMOS transistors during MEMS a switch actuation/deactuation. (b) Source-drain voltage of each of the 28 PMOS transistors in the stack during MEMS a switch actuation and deactuation. (c) Gate-source control voltage to turn on/off each PMOS transistor in the stack simultaneously.

$V_{MEMS}$ momentarily. Fig. 2-6(c) shows how the gate voltages of 28 PMOS transistors are synchronized with each other, which makes sure no transient breakdown happens to any

of the transistors in the stack.

### *2.4 Simulated Closed-loop Control*

As a compromise between sensitivity and speed, $T$ = 0.5 µs and $C_{ISO}$ = 5 pF were chosen for the control circuit. A parasitic capacitance $C_P \approx 50$ fF was present during the simulation. According to (2-4), with $C'_{MEMS}$ = 600 fF, t = 0.5 µs, sensitivity s = 0.7 ns/fF. Assuming a timing jitter of 10 ns for the circuit, the sensing resolution is 13 fF.

By using a recently developed large-signal transient model [25] for the MEMS switch, closed-loop capacitance sensing and tuning were simulated. The capacitance–voltage *C(V)* characteristic of the MEMS switch modeled is plotted in solid line in Fig. 2-7, where the pull-in voltage $V_P$ ~ 26 V and release voltage $V_R$ ~ 8V. During the simulation, by sweeping $V_{TUNE}$, $C_{TARGET}$ was varied from 310 fF to 595 fF in 26-fF steps while the corresponding $V_{MEMS}$ was captured, resulting in a voltage-capacitance *V(C)* characteristic as oppose to the conventional *C(V)* characteristic of a capacitive switch. As shown in Fig. 2-7, the simulated *V(C)* characteristic closely resembles the modeled *C(V)* characteristic of the switch.

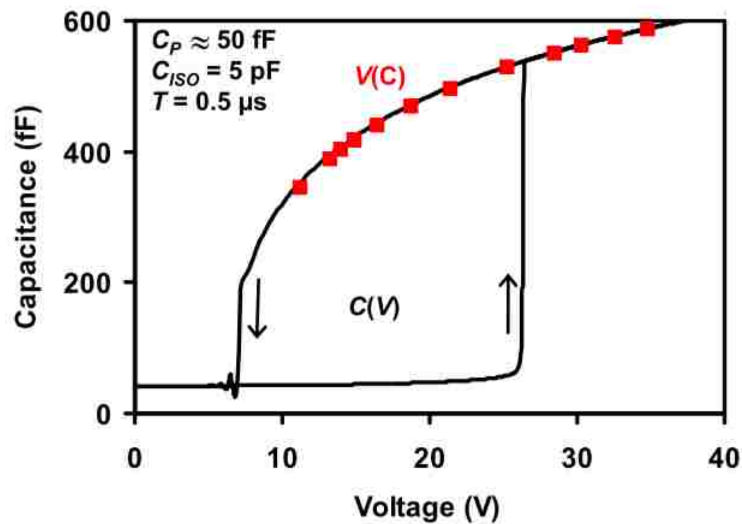
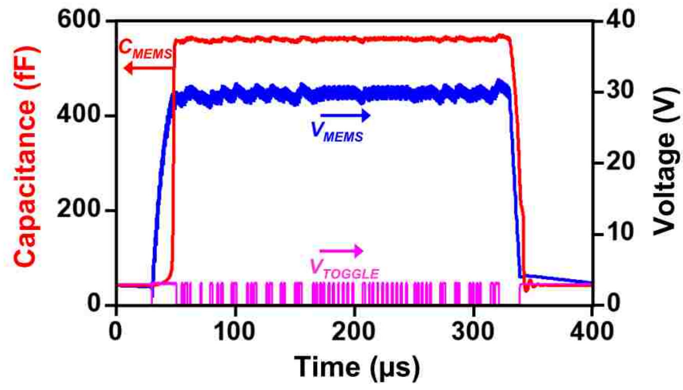


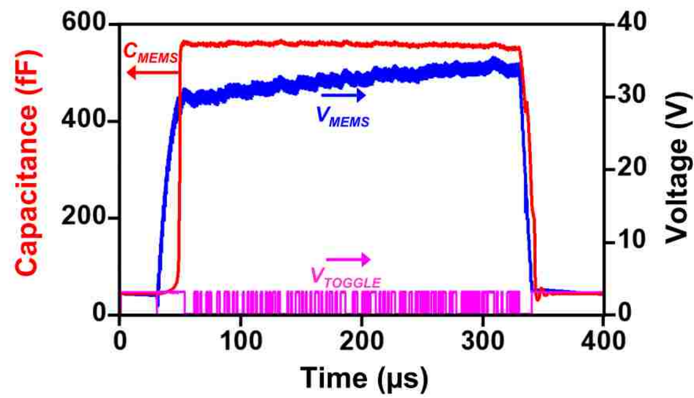

Fig. 2-7. Simulated $V(C)$ (symbols) and $C(V)$ (curves) characteristics by using the CMOS control circuit in conjunction with a large-signal transient model for the present MEMS capacitive switch.

Fig. 2-7 illustrates also that present closed-loop control takes advantage of the slope of the *C(V)* characteristics of the MEMS switch after pull-in. For certain switches with a stiff electrode, a smooth contact, or a metalized dielectric [26], the slope of their *C(V)* characteristics may be reduced thereby limiting the control range. However, a reduced *C(V)* slope also reduces the capacitance drift due to dielectric charging, making frequent dithering less critical. In general, as MEMS capacitive switches become more robust and reproducible with reduced *C(V)* slope in down state, therefore, closed-loop control should be less critical.

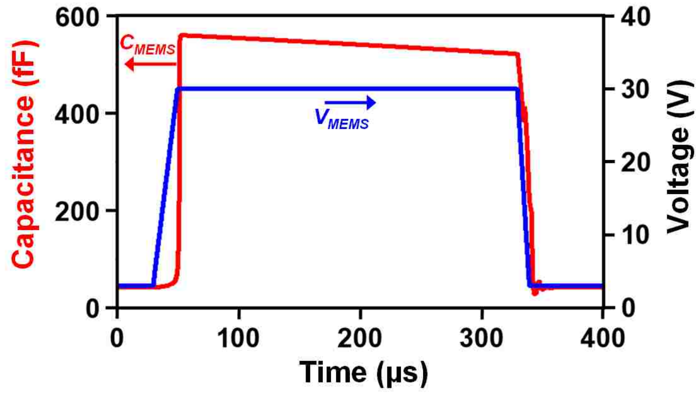
Fig. 2-8(a) and (b) show the simulated $C_{MEMS}$, $V_{MEMS}$ and $V_{TOGGLE}$ waveforms in time domain with and without $C(V)$ drift induced by dielectric charging, $V_{TOGGLE}$ being the signal for S to switch between $V^{+}$ and $V^{-}$. It can be seen that the MEMS switch is turned on in less than 20 μs, then quickly settled within ±6 fF of the 570-fF $C_{TARGET}$ for ~300 μs, before turning off in less than 10 μs. The range of $C_{MEMS}$ deviation is in good agreement with the above-estimated sensing resolution of 13 fF. To quickly evaluate the effectiveness of the control circuit under dielectric charging, a voltage source that ramped from 0 to 6 V in 300 μs was artificially added to the ground terminal of the MEMS switch, which effectively shifted $V_P$ and $V_R$ linearly. (In reality, dielectric charging typically occurs over much longer periods than 300 μs.) Fig. 2-8(b) shows that, in spite of the artificially accelerated dielectric charging, the control circuit was capable of ramping $V_{MEMS}$ from 29 V to 35 V in 300 μs to maintain $C_{MEMS}$ within target. As a comparison, Fig. 2-8(c) shows the MEMS switch with the same charging condition under open-loop constant bias of 30 V. As can be seen, if constant bias is applied regardless of the $V_P$ and $V_R$ increase induced by dielectric charging, the resulting $C_{MEMS}$ will drop.




(a)




(b)




(c)

Fig. 2-8. Simulated $C_{MEMS}$, $V_{MEMS}$ and $V_{TOGGLE}$ waveforms for closed-loop control of a MEMS switch around a target capacitance of 570 fF (a) without and (b) with dielectric charging. (c) The same MEMS switch under open-loop constant bias voltage with dielectric charging.

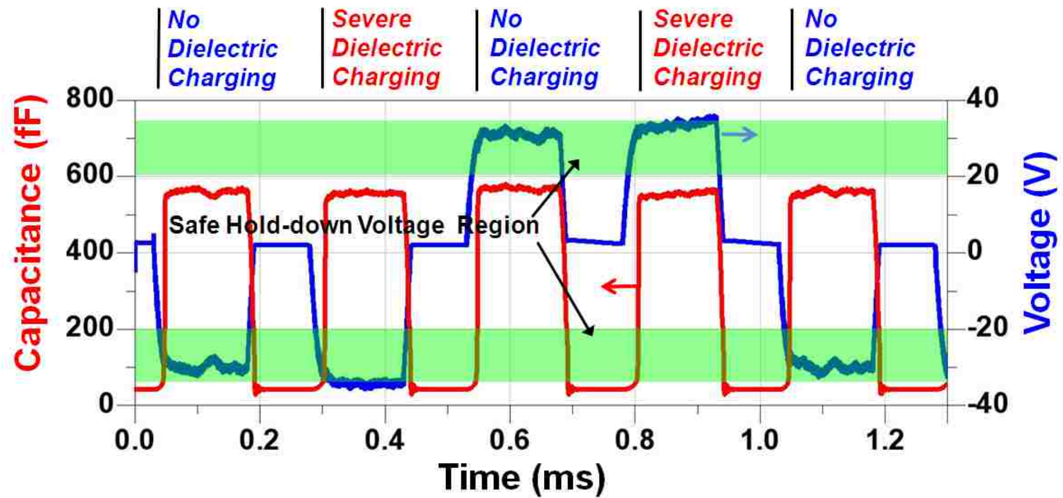



Fig. 2-9. Simulated intelligent bipolar control of MEMS switch, during which the sign of $V_{MEMS}$ was flipped whenever it drifted out of a preset boundary indicated by the shadow. $C_{TARGET}$ = 570 fF.

Fig. 2-9 shows the simulated intelligent bipolar control of MEME switch with dielectric charging artificially added to the second and fourth hold-down cycle, which required larger magnitude of $V_{MEMS}$ to compensate for the charging effect. The on-chip logic functioned in the way that if $V_{MEMS}$ drifted out of a preset range during a hold-down cycle, the bias sign would be flipped for the following cycle to cancel off the previously built-in charges in the dielectric.

## *References*


1. C. Lu, M. Lemkin, and B. E. Boser, "A monolithic surface micromachined accelerometer with digital output," *IEEE J. Solid-State Circuits,* vol. 30, pp. 1367-1373, Dec. 1995.
2. N. Yazdi, and K. Najafi, "An interface IC for a capacitive µg accelerometer," in *IEEE Int. Solid-State Circuits Conf. Dig.,* Feb. 1999, pp. 132–133.
3. R. Nadal-Guardia, A. Dehe, R. Aigner and L. M. Castaner, "Current drive methods to extend the range of travel of electrostatic microactuators beyond the voltage pull-in point," *Microelectromechanical Systems, Journal of,* vol. 11, pp. 255-263, 2002.
4. Wei-Shang Chu and K. W. Current, "A rail-to-rail input-range CMOS voltage comparator," in *Circuits and Systems, 1997. Proceedings of the 40th Midwest Symposium on,* pp. 160-163, vol.1, 1997.
5. J. Pons-Nin, A. Rodriguez, and L. M. Castaner, "Voltage and pull-in time in current drive of electrostatic actuators," *J. Microelectromechanical Systems*, vol. 11, pp. 196-205, June 2002.
6. J. C. M. Hwang, and C. L. Goldsmith, "Robust RF MEMS switches and phase shifters for aerospace applications," in *Proc. IEEE Radio-Frequency Integration Technology Symp.*, Dec. 2009, pp. 245-248.
7. F. N. Toth, G. C. M. Meijer, and H. M. M. Kerkvliet, "A very accurate measurement system for multielectrode capacitive sensors," *IEEE Trans. Instrum. Meas.*, vol. 45, no. 2, pp. 531–535, Apr. 1996.
8. F. M. L. V. Goes and G. C. M. Meijer, "A novel low-cost capacitive-sensor interface," *IEEE Trans. Instrum. Meas.*, vol. 45, no. 2, pp. 536–540, Apr. 1996.
9. M. Tavakoli and R. Sarpeshkar, "An offset-canceling low-noise lock-in architecture for capacitive sensing," *Solid-State Circuits, IEEE Journal of,* vol. 38, pp. 244-253, 2003.

10. G. K. Fedder, “Simulation of Microelectromechanical Systems,” Doctoral Dissertation, Univ. of California at Berkeley, 1994.

11. K. H. -. Chau, S. R. Lewis, Y. Zhao, R. T. Howe, S. F. Bart and R. G. Marcheselli, "An integrated force-balanced capacitive accelerometer for low-G applications," in *Solid-State Sensors and Actuators, 1995 and Eurosensors IX.. Transducers '95. the 8th International Conference on,* 1995, pp. 593-596.

12. S. Lei, C. A. Zorman and S. L. Garverick, "An oversampled capacitance-to-voltage converter IC with application to time-domain characterization of MEMS resonators," *Sensors Journal, IEEE,* vol. 5, pp. 1353-1361, 2005.

13. M. A. Lemkin, M. A. Ortiz, N. Wongkomet, B. E. Boser and J. H. Smith, "A 3-axis surface micromachined ΣΔ accelerometer," in *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International,* 1997, pp. 202-203, 457.

14. Tzung-Yin Lee and Sunyoung Lee, "Modeling of SOI FET for RF switch applications," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2010 IEEE,* 2010, pp. 479-482.

15. N. Dumas, L. Latorre, F. Mailly and P. Nouet, "Design of a smart CMOS high-voltage driver for electrostatic MEMS switches," in *Design Test Integration and Packaging of MEMS/MOEMS (DTIP), 2010 Symposium on,* 2010, pp. 44-47.

16. B. J. Baliga, "Trends in power semiconductor devices," *Electron Devices, IEEE Transactions on,* vol. 43, pp. 1717-1731, 1996.

17. K. Kobayashi, H. Yanagigawa, K. Mori, S. Yamanaka and A. Fujiwara, "High voltage SOI CMOS IC technology for driving plasma display panels," in *Power Semiconductor Devices and ICs, 1998. ISPSD 98. Proceedings of the 10th International Symposium on,* 1998, pp. 141-144.

18. A. Wood, C. Dragon and W. Burger, "High performance silicon LDMOS technology for 2 GHz RF power amplifier applications," in *Electron Devices Meeting, 1996. IEDM '96., International,* 1996, pp. 87-90

19. R. J. Baker and B. P. Johnson, "Stacking power MOSFETs for use in high speed instrumentation," *Review of Scientific Instruments,* vol. 63, pp. 5799-5801, 1992.

20. G. Sung, C. Wang, P. Jui and C. Wang, "A high-efficiency DC-DC buck converter for sub-3×VDD power supply," in *IC Design and Technology (ICICDT), 2010 IEEE International Conference on,* 2010, pp. 164-167.

21. H. L. Hess and R. J. Baker, "Transformerless capacitive coupling of gate signals for series operation of power MOS devices," *Power Electronics, IEEE Transactions on,* vol. 15, pp. 923-930, 2000.

22. E. J. Mentze, H. L. Hess, K. M. Buck and T. G. Windley, "A Scalable High-Voltage Output Driver for Low-Voltage CMOS Technologies," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on,* vol. 14, pp. 1347-1353, 2006.

23. N. Iwamori, S. Mizuno, H. Fujino, and K. Kawarnoto, “Mixed process IC on SOI wafer for automotive application,” *JSAE Rev*., vol. 22, no. 2, pp. 217–219, Apr. 2001.

24. J. Williams, “Mixing 3-V and 5V ICS,” *IEEE Spectrum*, vol. 30, no. 3, pp. 40–42, Mar. 1993.

25. S. Halder, C. Palego, J. C. M. Hwang, and C. L. Goldsmith, “Compact RF large-signal model for MEMS capacitive switches,” in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 2010, pp. 421-424.

26. F. Solazzi, C. Palego, D. Molinero, P. Farinelli, S. Colpo, J. C. M. Hwang, B. Margesin, and R. Sorrentino, “High-power high-contrast RF MEMS capacitive switch,” in *Proc. European Microwave Integrated Circuits Conf.,* Oct. 2012, accepted for publication.

# Chapter 3. CMOS Control Circuit Implementation and Verification

In this chapter, we will first go over how the design was implemented, and why we chose silicon-on-insulator (SOI) as opposed to bulk CMOS technology for circuit implementation. Then we will introduce the test setup used to verify all control functions before packaging and assembly, thanks to the fact that the design of the circuit allowed all critical internal sensing and control signals to be conditioned and output for diagnosis in oscilloscope. Also, in order to verify all design functions without a MEMS switch wire bonded, the design allowed artificially applying an arbitrary $V_{SENSE}$ waveform to a circuit input port by using a function generator. In the final part of this chapter, detailed experimental results will be discussed to address all control circuit functions separately, such as bipolar actuation/deactuation, capacitance sensing and control, and intelligent bipolar control.

### *3.1 Control Circuit Implementation*

Encouraged by the simulated performance, the above-described control circuit was implemented in 0.5-μm CMOS silicon-on-sapphire (SOS) technology [1]. The reason to use SOI technology is to take advantage of the insulating substrate which decouples the body of each transistor and enables the FET stacking to handle high voltages [2]. While SOS, as one particular technology of SOI, has better heat dissipation than silicon dioxide based SOI technology, due to the much higher thermal conductivity of sapphire, which is ideal for high power and high current application [3].

Fig. 3-1 shows the layout schematic of a fraction of the on-chip logic circuitry. The entire design and layout has followed the process design kit (PDK) provided by the foundry. As can be seen from Fig. 3-1, the process technology supports 1 poly (red) and 3 metal layers (blue, pink, and green) for routing. The specific placement and routing of all transistor cells have been done manually, as no automatic layout and routing function has been provided by PDK. While design rules have been strictly followed during the entire layout process, significant effort has been spent to optimize the layout to allow minimum interference on circuit performance from unexpected parasitics, cross-talks, noises, signal

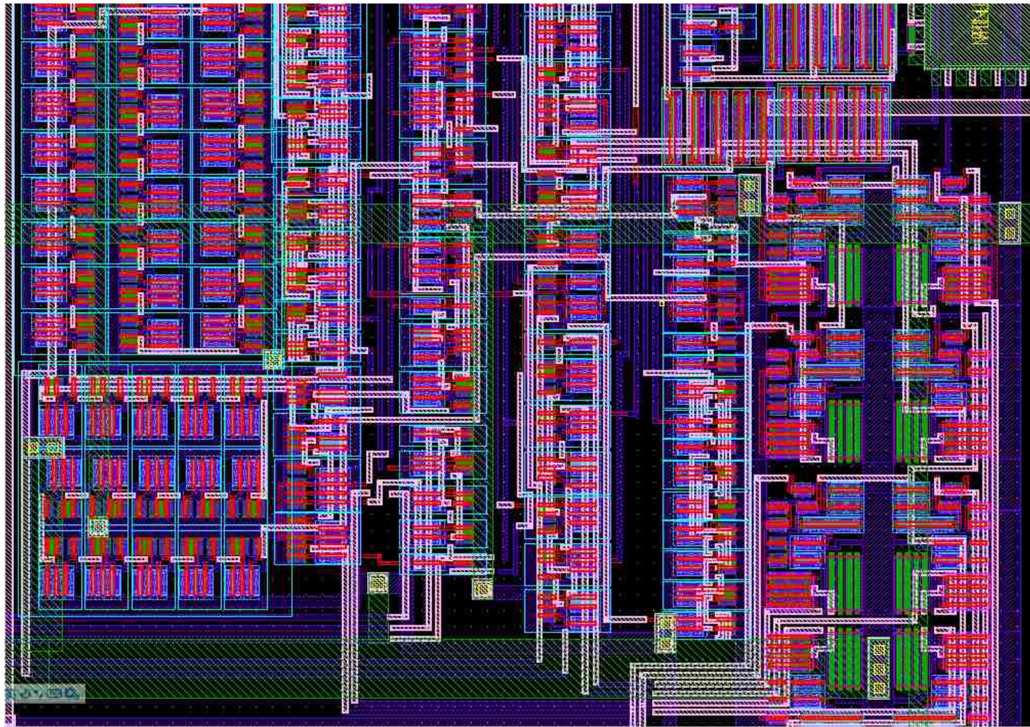


Fig. 3-1. Layout schematic of a fraction of the on-chip logic circuit.

delays, etc. To ensure a one-time pass, after the layout vs. schematic (LVS) and design rule check (DRC) were completed, the entire closed-loop control of RF MEMS capacitive switch was simulated on the layout level with all parasitics extracted. Circuit parameters were fine tuned to take into account any parasitics during the layout simulation.

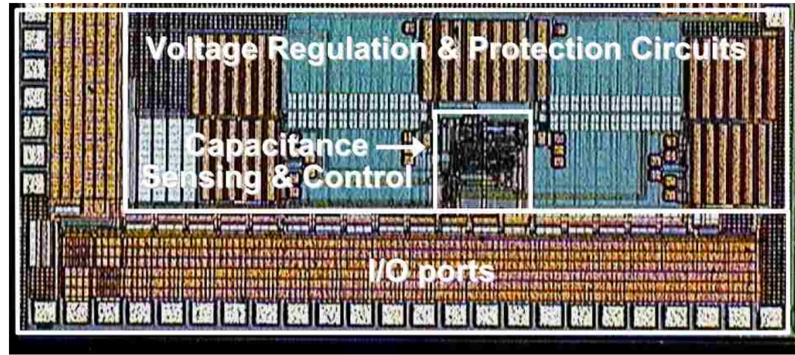



Fig. 3-2. Optical micrograph of the 3×1.5 mm$^2$ circuit die implemented in 0.5 μm CMOS silicon-on-sapphire technology.

Fig. 3-2 shows that the fabricated 3×1.5 mm$^2$ die is dominated by input/output (I/O) ports, voltage regulators and protection circuits for high voltage and electrostatic discharge. The capacitance sense/control circuit occupies only approximately 0.1 mm$^2$ at the center of the die, which is smaller than the size of a typical MEMS capacitive switch, and will add little overhead to the MEMS switch.

### *3.2 Measurement Setup*

In order to verify the fabricated CMOS chip, a customized probe card has been made to probe the bare CMOS chip without MEMS chip wire bonded. As illustrated in Fig. 3-3,

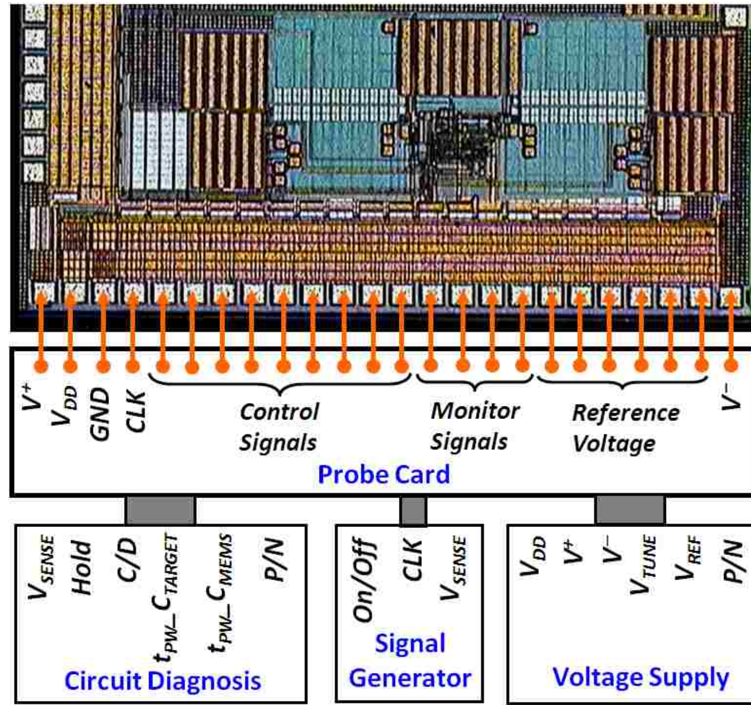


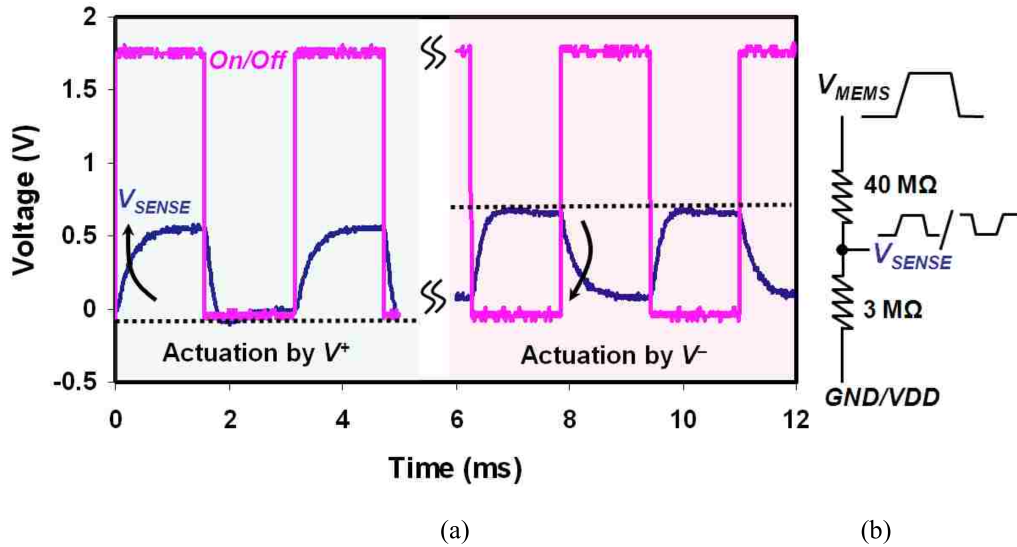

Fig. 3-3. Measurement setup for bare CMOS chip probing without MEMS switch wire bonded.

DC power supplies provided the $V_{DD}$, $V^{+}$, $V^{-}$, and other necessary voltages such as $V_{TUNE}$ for $C_{TARGET}$ tuning, $V_{REF}$ for a preset range for intelligent bipolar control, and *P/N* to designate bias polarity. Meanwhile, signal generators fed the circuit with the clock signal *CLK* and *On/Off* signal for MEMS switch actuation/deactuation. As mentioned earlier, the design allows an artificial $V_{SENSE}$ with arbitrary waveforms from signal generator to be applied for control function verification purpose. A multi-channel oscilloscope monitored output signals from the CMOS chip for various design function diagnosis,

such as $V_{SENSE}$ for actuation/deactuation, *Hold* for deactuation stop, *C/D* for charge/discharge MEMS capacitor $C_{MEMS}$, $t_{PW}_C_{TARGET}$ and $t_{PW}_C_{MEMS}$ for pulse-width-modulated capacitance sensing output, and polarity indicator signal *P/N* for intelligent bipolar control by on-chip logics. Function and meaning of each of those signals will be explained in more detail in the following sections.

### *3.3 Experimental Verification of Control Circuit Functions*

Bipolar actuation by $V^{+}$ and $V^{-}$ were verified by monitoring $V_{SENSE}$ waveform using an oscilloscope shown in Fig. 3-4. An on-chip voltage divider scaled the high-voltage $V_{MEMS}$ to $V_{SENSE}$, which is within the range of VDD, and can be read by an off-chip operation amplifier (op-amp) as a buffer. When actuated by $V^{+}$, the lower end of the 3-MΩ resistor was grounded. However, when actuated by $V^{-}$, in order for the negative $V_{MEMS}$ being read by an op-amp, $V_{DD}$ was applied there, which is automated altered by on-chip logics. In the case of Fig. 3-4, no op-amp was used as a buffer between $V_{SENSE}$ and oscilloscope; therefore, the magnitude of resulting $V_{SENSE}$ was limited by the finite




(a) (b)

Fig. 3-4. (a) Bipolar actuation/deactuation under both $V^+$ and $V^-$ were verified by monitoring the $V_{SENSE}$ waveform. (b) On-chip voltage divider to allow $V_{MEMS}$ being monitored by $V_{SENSE}$ without being significantly perturbed.

load impedance of the oscilloscope. Even though, bipolar actuation could still be seen clearly.

For bipolar actuation/deactuation, the deactuation process has to stop when $V_{MEMS}$ drops to around zero, otherwise, $V_{MEMS}$ will become reverse in polarity, and the switch will be reversely actuated. This function of putting a stop to deactuation is provided by a logic signal *Hold*, as the output of a comparator comparing $V_{SENSE}$ and a reference signal $V_{REF}$. *Hold* will be triggered to become logic low when $V_{SENSE}$ drops below/ramps above $V_{REF}$ under positive/negative bias to stop the deactuation. By artificially applying a $V_{SENSE}$

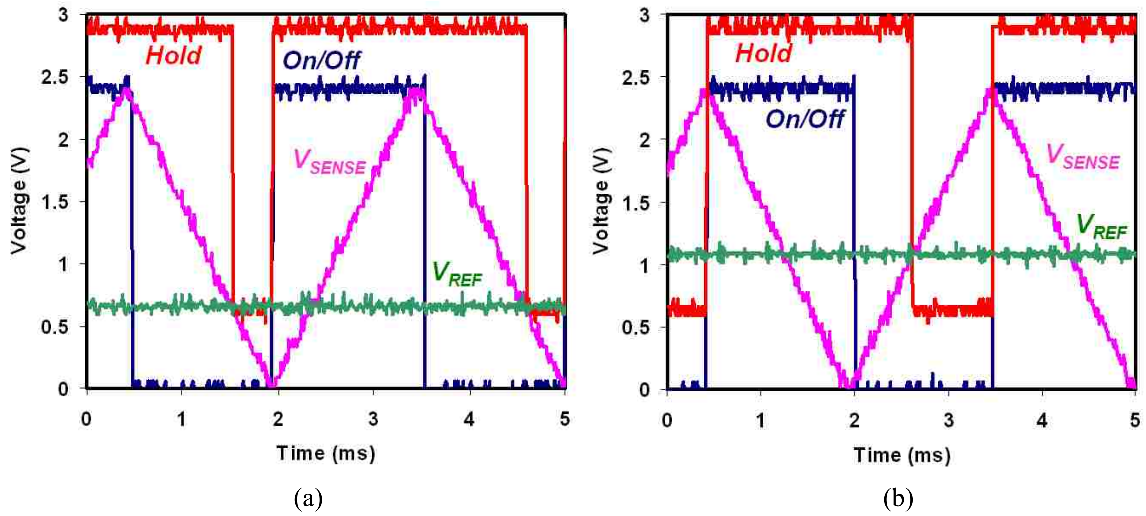



Fig. 3-5. *Hold* signal becomes logic low to stop the deactuation (a) when $V_{SENSE}$ drops below a reference signal $V_{REF}$ under $V^+$, and (b) when $V_{SENSE}$ ramps above $V_{REF}$ under $V^-$.

to a test circuit, this function has been verified under both positive and negative biases, as shown in Fig. 3-5(a) and (b), respectively.

Another important function to verify is the capacitance sensing. Fig. 3-6 shows the pulse-width-modulated capacitance sensing output $t_{PW}_C_{TARGET}$ and $t_{PW}_C_{MEMS}$, with the larger the capacitance, the narrower the pulse width. Fig. 3-6 also shows the clock signal *CLK* and *C/D*, a logic signal commanding switch S to increment/decrement $V_{MEMS}$ to increase/decrease $C_{MEMS}$. Under positive bias, if $C_{MEMS} < C_{TARGET}$, then *C/D* will be logic high to increase $C_{MEMS}$ to meet $C_{TARGET}$, and vice versa for $C_{MEMS} > C_{TARGET}$. In this

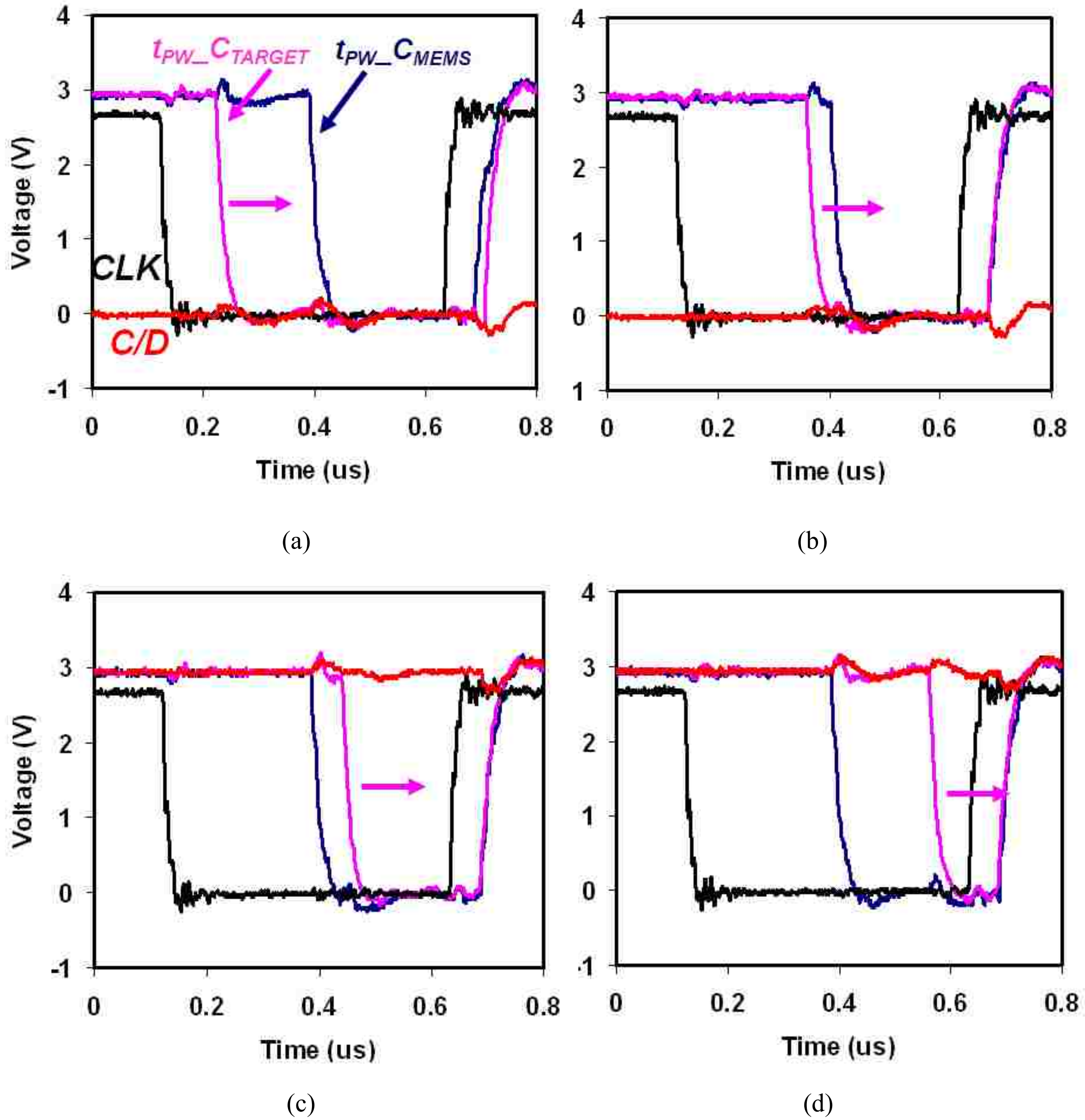



Fig. 3-6. Pulse-width-modulated output of capacitance sensing under positive bias where $t_{PW}_C_{MEMS}$, the pulse width of $C_{MEMS}$, was fixed while $t_{PW}_C_{TARGET}$ kept decreasing as $C_{TARGET}$ kept increasing from the state where $C_{TARGET}$ was (a) much smaller to (b) $C_{TARGET}$ slightly smaller to (c) $C_{TARGET}$ slightly larger to (d) much larger than $C_{MEMS}$. The Charge/Discharge signal *C/D* changed from logic low when $C_{TARGET} < C_{MEMS}$ in (a) and (b) to logic high when $C_{TARGET} < C_{MEMS}$.

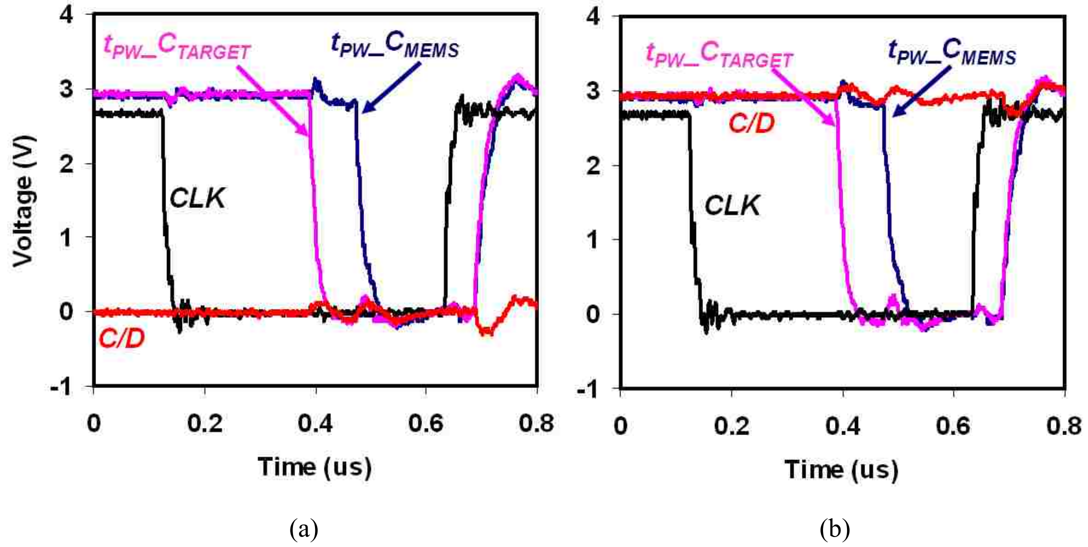



Fig. 3-7. With $C_{TARGET} < C_{MEMS}$, the Charge/Discharge signal *C/D* changed from logic high under (a) positive bias to logic low under (b) negative bias, both as an effort to lower $C_{MEMS}$ to meet $C_{TARGET}$.

measurement setup without MEMS switch wire bonded to CMOS chip, the $C_{MEMS}$ was from parasitic capacitance contributed from circuit components and the fringing capacitance caused by the open contact pads. $C_{TARGET}$ could be tuned by $V_{TUNE}$ in reference to an on-chip capacitor. As shown in Fig. 3-6(a), when $C_{TARGET}$ is much smaller than $C_{MEMS}$, *C/D* is logic low and remains its state in Fig. 3-6(b) when $C_{TARGET}$ increases to be slightly smaller than $C_{MEMS}$. As $C_{TARGET}$ continuously increases, it starts to become larger than $C_{MEMS}$ in Fig. 3-6(c). As a result, *C/D* becomes logic high as an effort to increase $C_{MEMS}$ to meet $C_{TARGET}$. As $C_{TARGET}$ keeps increasing, *C/D* remains logic high in

Fig. 3-6(d). Fig. 3-7(b) shows that if $C_{TARGET} < C_{MEMS}$ under negative bias, *C/D* will be logic high to apply a smaller negative bias to lower $C_{MEMS}$, while under positive bias, *C/D* will be logic low to apply a smaller positive $V_{MEMS}$, as shown in Fig. 3-7(a).

Finally, intelligent bipolar control was verified by artificially applying a $V_{SENSE}$ signal waveform to the CMOS chip and monitoring the bias polarity controlled by on-chip *P/N* signal, with *P/N* logic high meaning positive bias, and vice versa. Fig. 3-8(a) shows a safe operation region defined by two reference voltages $V_{REF_S}$ and $V_{REF_B}$. Under positive bias, surface and bulking charging are detected if the peak of $V_{SENSE}$ lies beyond $V_{REF_S}$ and below $V_{REF_B}$, respectively. Only one out-of-range $V_{SENSE}$ occurrence is needed to flag the polarity control signal *P/N*, which will flip the bias polarity at the beginning of next switch hold-down cycle. Fig. 3-8(b) and (c) show the case when the peak of an artificially applied $V_{SENSE}$ lay beyond and below the shadowed range, the bias polarity got flipped at the beginning of the following hold-down cycle. While Fig. 3-8(d) shows that bias polarity was maintained if $V_{SENSE}$ peak lay within such preset range.

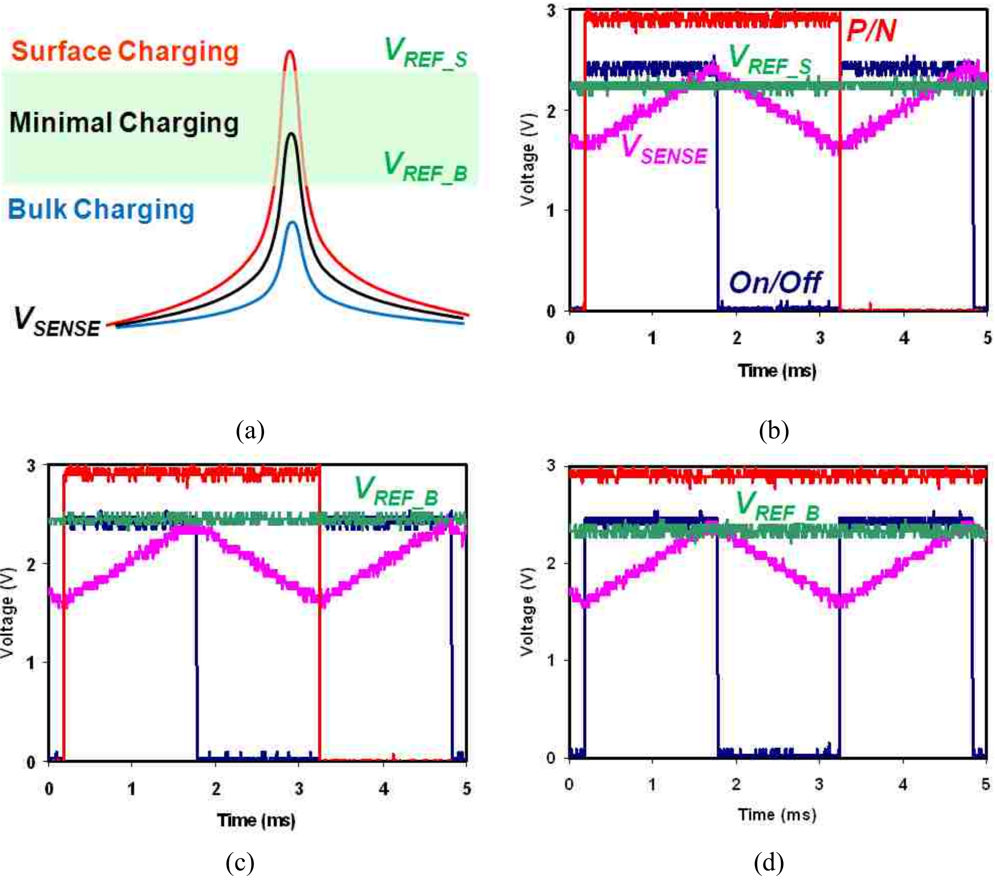



Fig. 3-8. Verification of intelligent bipolar control based on on-chip logic functions. (a) Surface and bulk charging are detected when peak of $V_{SENSE}$ lies above and below a shadowed region set by two reference voltages $V_{REF_S}$ and $V_{REF_B}$, respectively. Bias polarity *P/N* flipped in the following cycle when the peak of an artificially applied $V_{SENSE}$ waveform lay (b) above $V_{REF_S}$, and (c) below $V_{REF_B}$. *P/N* kept its sign when (c) $V_{SENSE}$ peak lay in-between $V_{REF_S}$ and $V_{REF_B}$.

As mentioned earlier, in the present design, intelligent bipolar control can be achieved either by on-chip logics or by off-chip programmed computer intelligence, with

the latter one being more robustness as more complicated algorithm could be programmed to eliminate any false triggering. Furthermore, for future real applications, an FPGA, ASIC, or any embedded processor, which could handle sophisticated signal processing functions, could be used for programmed intelligent bipolar control. The intelligent bipolar control based on simple on-chip flip-flops shown in Fig. 3-8 is only to demonstrate the concept of such integrated solution in the future.

## *References*


1. FC process, UltraCMOS Technology, Peregrine Semiconductor, San Diego, California, USA.
2. R. Wolf, D. Wang, A. Joseph, A. Botula, P. Rabbeni, D. Harame and J. Dunn, “Highly resistive substrate CMOS on SOI for wireless front-end switch applications”, in *CS MANTECH Conference*, May 16th, 2011, Palm Springs, CA, USA.
3. R. A. Johnson, P. R. de la Houssaye, C. E. Chang, Pin-Fan Chen, M. E. Wood, G. A. Garcia, I. Lagnado and P. M. Asbeck, "Advanced thin-film silicon-on-sapphire technology: microwave circuit applications," *Electron Devices, IEEE Transactions on,* vol. 45, pp. 1047-1054, 1998

# Chapter 4. Experimental Demonstration of Closed-loop Bipolar Control of RF MEMS Capacitive Switches

After verification of all circuit functions, to experimentally demonstrate closed-loop CMOS control of RF MEMS capacitive switches, hybrid assembly approach was adopted to mount and wire-bond separate CMOS and MEMS dies in a ceramic package as shown in Fig. 4-1. The package was plugged into the socket of a custom made printed circuit board (PCB), which has numbers of cable connectors on its periphery. As mentioned in Chapter 1.5, compared to monolithic approach, this hybrid assembly approach significantly increased the parasitic capacitance $C_P$ and degraded the control circuit performance as studied in Chapter 2.2. Nevertheless, Fig. 4-1 shows that the control circuit was capable of dithering $V_{MEMS}$ to turn the MEMS switch on and off, as well as to maintain $C_{MEMS}$ around the 438-fF target, albeit with larger $V_{MEMS}$ ripples and longer actuation/deactuation times compared to the simulated performance in Fig. 2-8(a).

In this chapter, experimental results on closed-loop MEMS capacitance sensing and tuning will be first presented, followed by comparisons of MEMS switch performance

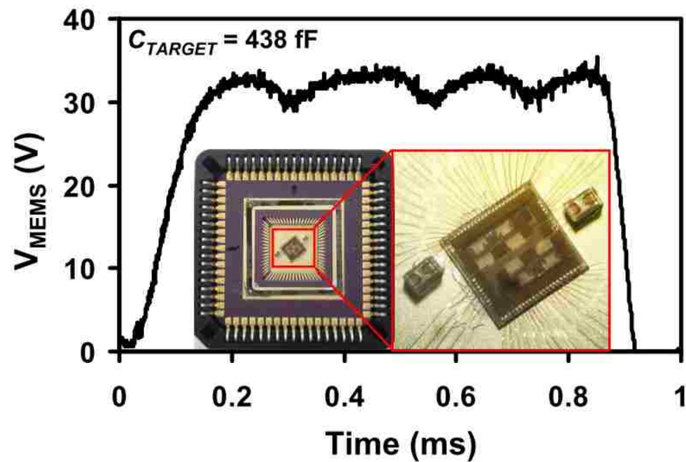



Fig. 4-1. Measured bias waveform of a MEMS switch under closed-loop control for a targeted capacitance around 438 fF. Insets show two pairs of MEMS switches and control circuits wire-bonded together in a ceramic package.

under constant-bias open-loop and closed-loop control with the presence of dielectric charging. Finally, intelligent bipolar control of a RF MEMS capacitive switch was demonstrated, which suggested indefinite operation of MEMS switch despite dielectric charging.

## *4.1 Capacitance Sensing Results*

Under closed-loop control, unlike simulation, $C_{MEMS}$ cannot be directly measured without significantly perturbing the sensing. However, by sweeping $V_{TUNE}$ during the

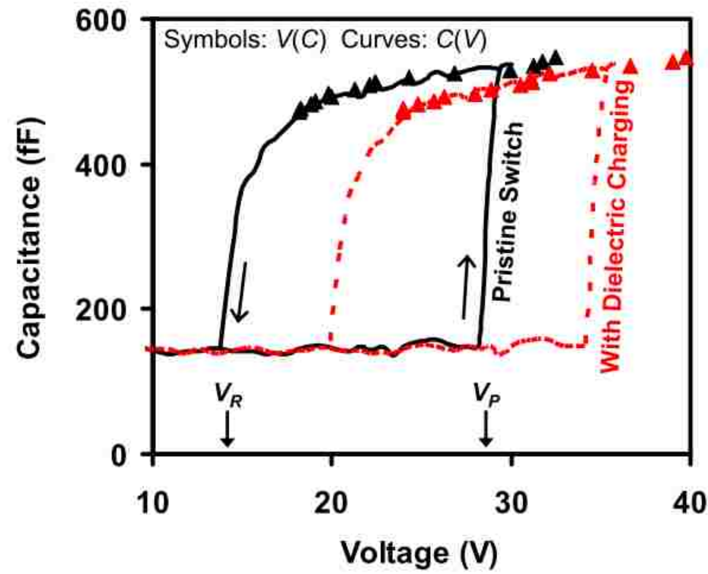



Fig. 4-2. $V(C)$ characteristic (symbols) optimized by closed-loop CMOS control circuit vs. $C(V)$ characteristic (curves) measured by precision impedance analyzer of a MEMS capacitive switch in both pristine (——) and charged (- - -) states.

measurement, $C_{TARGET}$ was varied from 470 fF to 550 fF in 5-fF steps while $V_{MEMS}$ waveform corresponding to each $C_{TARGET}$ was captured and averaged by using an oscilloscope over a 2-ms time period. Fig. 4-2 shows that, in spite of a $C_P$ as large as 400 fF, such a measured $V(C)$ characteristic closely resembles the $C(V)$ characteristic measured by using a precision impedance analyzer (PIA) in both pristine and dielectric charged conditions. Because switch $C(V)$ cannot be measured by PIA after wire bonding, $C(V)$ with dielectric charging was got by artificially shift the switch $C(V)$ measured in

Table 4-1

Simulated vs. Measured Control-Circuit Performance

| | Simulated Monolithic Assembly | Simulated Hybrid Assembly | Measured Hybrid Assembly |
|---|---|---|---|
| Parasitic Capacitance | 50 fF | 400 fF | 400 fF |
| Sensing Resolution | 14 fF | 24 fF | 28 fF |
| Control Accuracy[a] | ±1% | ±2% | ±2.5% |
| Power Consumption | 0.5 mW | 0.5 mW | 0.7 mW |

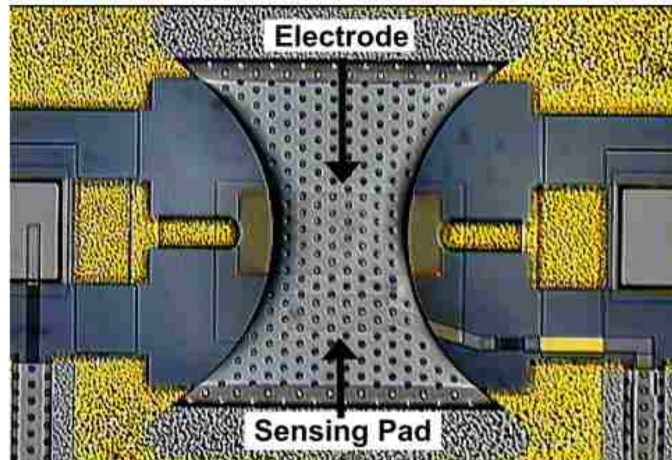
[a]$C_{TARGET}$ ~ 550 fF.

pristine condition before wire bonding.

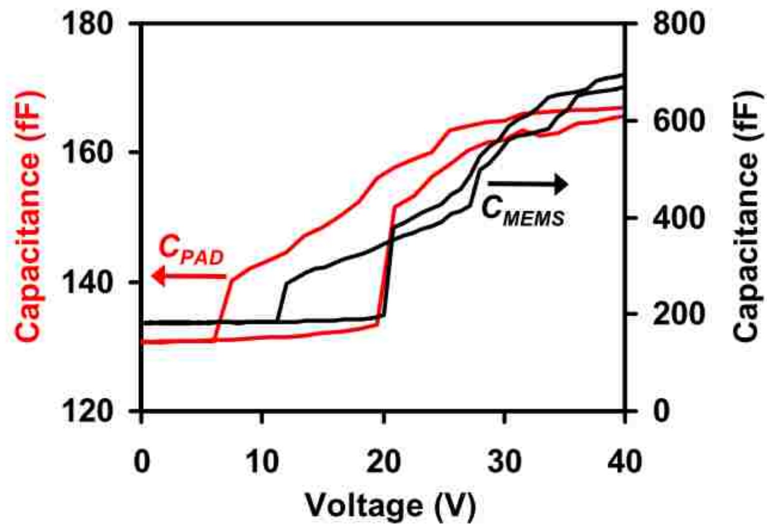
According to (2-4), with $C'_{MEMS} = C_{MEMS} + C_P = 1000$ fF, $t = 0.5$ µs, sensitivity $s$ degraded from 0.7 ns/fF in simulation to 0.4 ns/fF, which leads to an estimated degrade of capacitance-sensing resolution from approximately 14 fF to 24 fF. This is consistent with a standard deviation of approximately 3 V in $V_{MEMS}$ for all targets in Fig. 4-2 and a $C(V)$ slope of approximately 5 fF/V, which translates into a standard deviation of approximately 15 fF for $C_{MEMS}$. As a result, $C_{MEMS}$ can be controlled with ±2.5 % of $C_{TARGET}$. A higher sensitivity and a smaller deviation are expected if $C_P$ can be reduced. The present hybrid integration scheme involving bonding wires causes excessive $C_P$, which could also vary from package to package. To reduce $C_P$, MEMS switches could be monolithically integrated with the present closed-loop CMOS control circuit, as

demonstrated with the previous open-loop CMOS control circuit [1]. With monolithic integration, $C_P$ should decrease by an order of magnitude and $C_{MEMS}$ should be controlled within ±1% as predicted by simulation. Table 4-1 compares the simulated and measured performance of the closed-loop control circuit.

Since the closed-loop control circuit compares $C_{MEMS}$ with $C_{REF}$ instead of outputting $C_{MEMS}$ directly, to verify that $C_{MEMS}$ is indeed well controlled, a MEMS switch on the same wafer as regular MEMS switches was specially modified to include an additional capacitance-sensing pad as shown in Fig. 4-3(a). (This pad is not in the control loop and, hence, not required for closed-loop control of regular MEMS switches.) It can be seen that the capacitance-sensing pad was inserted between the center and ground conductors of the coplanar transmission line and its rectangular outline was faintly discernible when the bowtie-shaped movable electrode was pulled in to contact both the sensing pad and the center conductor. Fig. 4-3(b) shows that the capacitance of the sensing pad $C_{PAD}$ was measured by an impedance analyzer to be 135-167 fF, depending on the position of the movable electrode. Fig. 4-3(b) shows also that, although such a modified MEMS switch does not exhibit ideal $C(V)$ characteristic, it tracks that of the sensing pad. Therefore, by using the modified MEMS switch, $C_{MEMS}$ can be inferred from




(a)




(b)

Fig. 4-3. (a) Specially modified MEMS switch with additional capacitance-sensing pad under movable electrode between center and ground conductors of a coplanar transmission line. (b) $C_{PAD}$ measured from the sensing pad as a proportional indicator of $C_{MEMS}$.

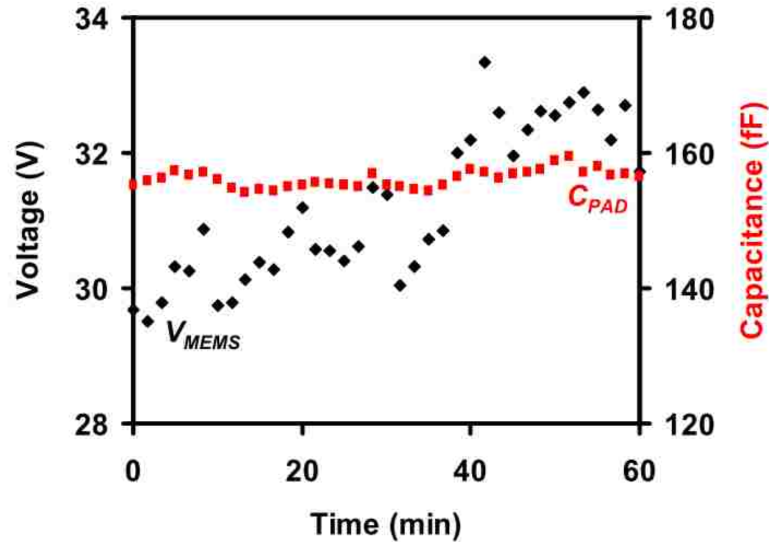



Fig. 4-4. During an hour-long hold-down test with closed-loop control, $V_{MEMS}$ (♦) of the specially modified MEMS switch increased by approximately 3 V to compensate for dielectric charging while $C_{PAD}$ (■) was kept constant as measured by an impedance analyzer.

$C_{PAD}$ measured by an impedance analyzer while the MEMS switch undergoes closed-loop control. Unfortunately, such an assembly further degraded $C_P$ to 800 fF, which severely impacted sensing sensitivity. Fig. 4-4 shows that, under the closed-loop control of the specially modified MEMS switch, $V_{MEMS}$ increased from 29 V to 32 V during an hour-long hold-down test to compensate for dielectric charging and to keep $C_{MEMS}$ constant. As a result of the increase in $V_{MEMS}$, $C_{PAD}$ was held constant around 157 fF, which corresponds to $C_{MEMS}$ = 450 fF.

## 4.2 Capacitance Sensing Discussions

As mentioned earlier in Chapter 2.2, the time $T$ it takes to sense $C_{MEMS}$ is only a small fraction of the 1-MHz clock cycle, which is much faster than the mechanical resonance (~100 kHz) of the switch, so that sensing does not significantly perturb the state of the switch. Perturbation can be further reduced by using a look-up table to store the steady-state $V_{MEMS}$ of each switch for certain $C_{TARGET}$, and update it via capacitance sensing only when the switch is not performing a critical function, such as during the calibration cycle of an RF front end. This is because a well-designed and fabricated MEMS switch drifts very slowly and it is rarely necessary to update $V_{MEMS}$ each time it is turned on. (In this dissertation on expeditious proof of principle, the MEMS switches were tested unpackaged and in room air, which tend to accelerate dielectric charging [2], [3]. Had the switches been properly packaged or tested in dry air, dielectric charging would be less severe and the switches would drift less.) Such infrequent $C_{MEMS}$ sensing and $V_{MEMS}$ updating not only can allow one control circuit to multiplex between several switches, but also can avoid low-frequency noises filtered through the MEMS switches from the control circuit [4]. Low-frequency noises can be further alleviated by using advanced CMOS technology with faster clock cycles and smaller voltage steps.

The MEMS switch consumes little power, so does the control circuit. As listed in Table 4-1, with active sensing and control during every clock cycle, the present control circuit consumes less than 1 mW, among which the actuation/deactuation circuit consumes about 0.1 mW, while the sensing and control circuit consumes about 0.6 mW. Power consumption can be further optimized by using advanced CMOS technology, as well as infrequent sense/control. As shown in the previous open-loop control [1], the die size and power consumption are likely to be dominated by the charge-pump circuit. However, this overhead can be reduced by sharing a charge-pump circuit among many MEMS switches. The present CMOS control circuit was measured to maintain a resolution of better than 30 fF between –40°C and 85°C. Since $C_{REF}$ has a temperature coefficient on the order of 1 ppm /°C [5], $C_{MEMS}$ should be controlled with the same accuracy between –40°C and 85°C.

This dissertation focuses on expeditious proof of closed-loop control principle instead of specific applications. As a digital switch, a MEMS capacitive switch only has to have an off-capacitance below a certain minimum and an on-capacitance above a certain maximum. However, as mechanical devices, these switches are fundamentally analog, and are often used in this manner in more complicated circuits such as impedance

tuners, phase shifters, and band filters. In most of these cases, an on-capacitance variation of less than ±2 % is desired, which would require monolithic integration with advanced CMOS technology.

The present closed-loop control takes advantage of the slope of the $C(V)$ characteristics of the MEMS switch after pull-in. As discussed earlier in Chapter 1.4, for certain switches with a stiff electrode, a smooth contact, or a metallized dielectric [6], the slope of their $C(V)$ characteristics may be reduced thereby limiting the control range. However, a reduced $C(V)$ slope also reduces the capacitance drift due to dielectric charging, making frequent dithering less critical. In general, as MEMS capacitive switches become more robust and reproducible, closed-loop control should be less critical. Additionally, while it is possible to apply the same closed-loop control to variable capacitors as opposed to capacitive switches, the control may have to be more sensitive and accurate, while the noise introduced by the control circuit may have to be further suppressed.

## *4.3 Open-loop vs. Closed-loop Control*

Fig. 4-5 compares closed-loop and open-loop controls of a regular (without

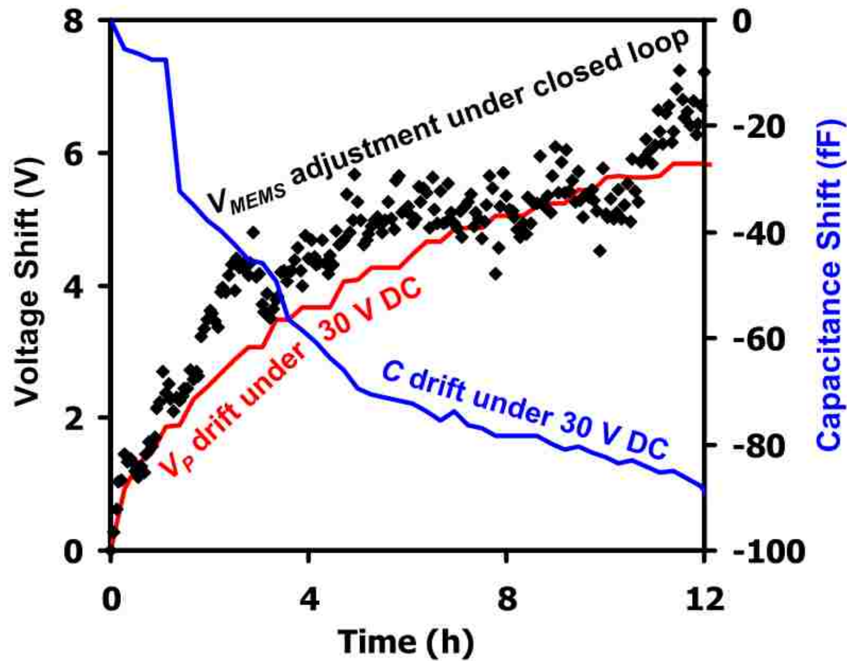



Fig. 4-5. Open-loop control (curves) vs. closed-loop control (symbols). Under open-loop control with a constant $V_{MEMS}$ of 30 V, $V_P$ increased by 6 V and $C_{MEMS}$ decreased by 90 fF in 12 h due to dielectric charging. Under closed-loop control, $V_{MEMS}$ closely tracked the increase in $V_P$ and maintained $C_{MEMS}$ around a $C_{TARGET}$ of 560 fF.

additional capacitance-sensing pad) MEMS switch with similar dielectric-charging characteristics as the specially modified MEMS switch of the same wafer. The open-loop control was performed on-wafer by applying a constant 30-V bias, which was periodically ramped up and down in 1 s to sense the drift in $C_{MEMS}$ and $V_P$. The closed-loop control was performed with $C_{TARGET}$ = 560 fF so that $V_{MEMS}$ would be tuned around 30 V. It can be seen that, over the 12-h hold-down test, $V_P$ of the switch under

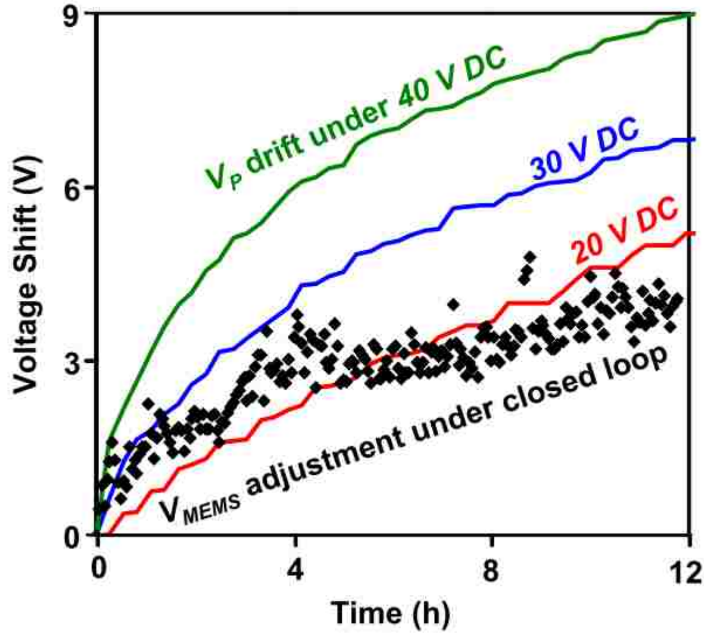



Fig. 4-6. Rate of dielectric charging under closed-loop control (symbols) vs. that under 20, 30, and 40 V DC after the switch was pulled in at 40 V DC. $C_{TARGET}$ = 460 fF.

open-loop control increased by 6 V. As a result, $C_{MEMS}$ at $V_{MEMS}$ = 30 V decreased by 90 fF. By contrast, under closed-loop control, $V_{MEMS}$ closely tracks the increase in $V_P$ to maintain a constant $C_{MEMS}$ in spite of dielectric charging.

Under the present closed-loop control, $V^{\pm}$ = ±40 V provide ample headroom to overdrive the MEMS switch to compensate for $C(V)$ drift while maintaining high $C_{TARGET}$. On the other hand, for low $C_{TARGET}$, the control circuit is sufficiently intelligent to trim $V_{MEMS}$ below $V_P$ so as to minimize dielectric charging. Fig. 4-6 shows another comparison of open- vs. closed-loop control for $C_{TARGET}$ = 460 fF. Based on the rate of $V_{MEMS}$

adjustment, it can be seen that the rate of dielectric charging under closed-loop control is as low as that under 20 V DC. By contrast, under open-loop control, it is impossible to lower the DC bias below $V_P$ unless a high-low waveform is used [7], which would be difficult to optimize in practice. Consequently, open-loop control is likely to suffer from higher rates of dielectric charging as indicated by the curves under 30 V and 40 V DC in the figure.

Presently, MEMS switches are usually designed with open-loop control by a constant voltage much higher than the pull-in voltage (e. g., 40 V vs. 25 V) to accommodate for voltage drifts, but the drifts are actually aggravated by high voltage. This dissertation shows that, with intelligent control, reliable operation can be achieved with minimally required hold-down voltage. However, significantly lower control voltage may require a different actuation mechanism, such as piezoelectric actuation [8], which is beyond the scope of this dissertation.

## *4.4 Intelligent Bipolar Control*

To operate a MEMS switch indefinitely in spite of dielectric charging, intelligent

bipolar control by using the present closed-loop circuit was devised. As mentioned in Chapter 1, a MEMS switch can be equally operated by positive and negative biases, which cause dielectric charging of opposite signs. As the result, non-intelligent bipolar waveforms have been proposed [9] to alternate the bias sign after each switching cycle. However, detailed analysis showed [10] that, due to different on/off times and different charging rates under positive and negative biases, it is difficult to *a priori* specify the waveform for complete elimination of dielectric charging. Using the present closed-loop circuit, intelligent bipolar control can be accomplished by monitoring the drift of $V_{MEMS}$ and limiting it to a range much smaller than $|V_R|$. If $V_{MEMS}$ drifts out of range due to dielectric charging of one sign, the sign of $V_{MEMS}$ will be flipped to induce dielectric charging of the opposite sign to compensate for the charge already accumulated. In this manner, the sign of $V_{MEMS}$ can be flipped as many times as necessary to prolong the life of the MEMS switch.

Fig. 4-7 shows such a long-term hold-down test under intelligent bipolar control, during which the movable electrode was in constant contact with the dielectric except for a short period of approximately 200 μs when the bias sign was flipped. Meanwhile, $V_{MEMS}$ was captured every 10 s from the control circuit by an oscilloscope. Due to

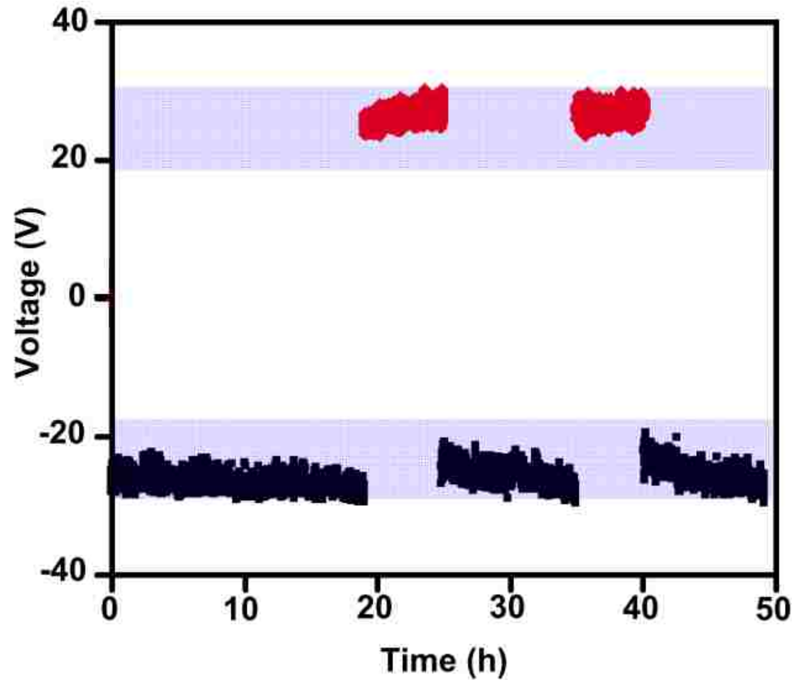



Fig. 4-7. Long-term hold-down test under intelligent bipolar control of a MEMS switch, during which the sign of $V_{MEMS}$ was flipped whenever it drifted out of a preset range of ±30 V. $C_{TARGET}$ = 550 fF.

dielectric charging, the magnitude of $V_{MEMS}$ under both polarities kept increasing until it drifted out of the preset range of ±30 V when the sign of $V_{MEMS}$ was flipped. As a result, the MEMS switch lasted more than 50 h when the test was terminated for convenience.

For the present intelligent bipolar control, the bias polarity cannot be flipped during a hold-down cycle but rather the interval of two consecutive ones or when the switch is not performing a critical function, because the time it takes to flip polarity is longer than the mechanical response time of the switch (~ 5 μs). While this polarity change pattern

can cope with most of the applications, in some extreme cases of a prolonged hold-down cycle, during which the switch state cannot be interrupted, the current capacity of switch S has to be increased so that the bias polarity can be flipped much faster than the mechanical response time of the MEMS switch. In that sense, bias polarity can be flipped anytime without perturbing mechanical state of the switch.

## *References*


1. J. C. M. Hwang, and C. L. Goldsmith, "Robust RF MEMS switches and phase shifters for aerospace applications," in *Proc. IEEE Radio-Frequency Integration Technology Symp.*, Dec. 2009, pp. 245-248.
2. Z. Peng, C. Palego, J. C. M. Hwang, D. I. Forehand, C. L. Goldsmith, C. Moody, A. Malczewski, B. W. Pillans, R. Daigler, and J. Papapolymerou, "Impact of humidity on dielectric charging in RF MEMS capacitive switches," *IEEE Microwave Wireless Components Lett.,* vol. 19, pp. 299-301, May 2009.
3. Z. Peng, C. Palego, J. C. M. Hwang, C. Moody, A. Malczewski, B. W. Pillans, D. I. Forehand and C. L. Goldsmith, "Effect of packaging on dielectric charging in RF MEMS capacitive switches," in *Microwave Symposium Digest, 2009. IEEE MTT-S International,* 2009, pp. 1637-1640.
4. G. M. Rebeiz, "Phase-noise analysis of MEMS-based circuits and phase shifters", *IEEE Trans. Microwave Theory Techniques,* vol. 50, pp. 1316-1323, May. 2002.
5. FC process, UltraCMOS Technology, Peregrine Semiconductor, San Diego, California, USA.

6. F. Solazzi, C. Palego, D. Molinero, P. Farinelli, S. Colpo, J. C. M. Hwang, B. Margesin, and R. Sorrentino, “High-power high-contrast RF MEMS capacitive switch,” in *Proc. European Microwave Integrated Circuits Conf.,* Oct. 2012, accepted for publication.
7. C. Goldsmith, J. Ehmke, A. Malczewski, B. Pillans, S. Eshelman, Z. Yao, J. Brank, and M. Eberly, “Lifetime characterization of capacitive RF MEMS switches,” in IEEE MTTS Int. Microwave Symp. Dig., June 2001, pp. 227-230.
8. Jae-Hyoung Park, Hee-Chul Lee, Yong-Hee Park, Yong-Dae Kim, Chang-Hyeon Ji, Jonguk Bu and Hyo-Jin Nam, “A fully wafer-level packaged RF MEMS switch with low actuation voltage using a piezoelectric actuator”, *Journal of Micromechanics and Microengineering*, vol. 16, no. 11, , pp. 2281-2286, 2006.
9. J. R. Reid, and R. T. Webster, “Measurements of charging in capacitive microelectromechanical switches,” *Electronics Lett.*, vol. 38, no. 24, pp. 1544-1545, Nov. 2002.
10. Z. Peng, X. Yuan, J. C. M. Hwang, D. Forehand, and C. L. Goldsmith, "Superposition model for dielectric charging of RF MEMS capacitive switches under bipolar control-voltage waveforms," *IEEE Trans. Microwave Theory Techniques,* vol. 55, pp. 2911-2918, Dec. 2007.

# Chapter 5. Conclusions

This dissertation explored the opportunity of using intelligent CMOS control circuit to solve the persistent reliability and robustness issues of RF MEMS capacitive switches. By adopting the concept of real-time closed-loop capacitance sensing and tuning, both simulated and measured switch performance were presented and discussed in details. To further explore the merit of such closed-loop control, the concept of intelligent bipolar control has been introduced aiming at indefinite operation of RF MEMS capacitive switches despite the presence of dielectric charging. In this chapter, we will conclude this study and provide recommendations for future studies on this topic.

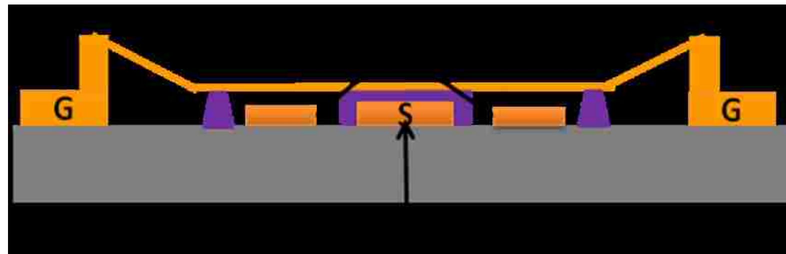
## *5.1 Conclusions of This Dissertation*

Closed-loop control of RF MEMS capacitive switches was successfully demonstrated by using a CMOS circuit. Based on low-voltage (3.3 V) CMOS technology, the circuit has adopted novel techniques of transistor stacking and capacitance sensing to realize high-voltage actuation and sensing of RF MEMS capacitive switches. It was

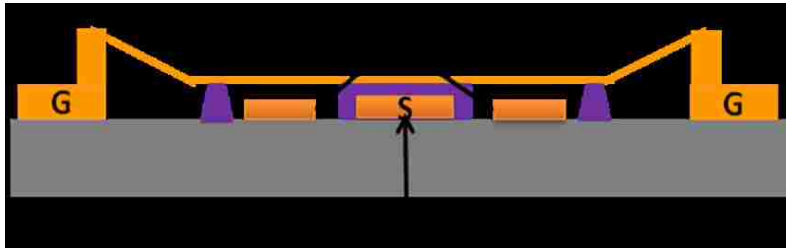
confirmed that the circuit maintained the switch capacitance within ±1% and ±2.5% of the target in simulation and experiment, respectively, by intelligently adjusting the switch bias magnitude to compensate for dielectric charging. Compared to conventional open-loop control where excessive bias is applied, the circuit applies just enough bias magnitude for a given target to minimize dielectric charging. The circuit can also flip the bias sign whenever the bias magnitude drifts out of a preset range because of its compensation for dielectric charging. A 50-hour long term stress test, which was terminated for convenience, demonstrated the possibility to operate the MEMS switch indefinitely in spite of dielectric charging under such intelligent bipolar control. The control circuit adds little overhead to the MEMS switch with a foot print of 0.1 $mm^2$ and power consumption less than 1 mW. Under such closed-loop intelligent bipolar control, MEMS capacitive switches can be much more robust and reliable.

### *5.2 Recommendations for Future Study*

One area for future study is to evaluate the closed-loop control performance under RF stress. Some questions need to be addressed such as if closed-loop sensing and tuning




(a)




(b)

Fig. 5-1. RF MEMS capacitive switch with separate electrodes for (a) RF and DC sensing/biasing, and (b) RF/DC biasing and sensing.

could add substantial noise to the RF signal, and if the RF signal affects the sensing circuit accuracy. The answers to those questions will vary with different closed-loop designs, but has to be address for specific application.

A safer approach is to use separate DC actuation and RF signal paths as shown in Fig. 5-1(a), which means the RF signal is physically separated with the DC control functions, including DC actuation/deactuation, and capacitance sensing/tuning. There are

a couple of examples of RF MEMS capacitive switches using this kind of separate DC and RF path [1], [2].

Another option to explore is to use separate electrodes for capacitance sensing and biasing shown in Fig. 5-1(b), similar with the test structure we used for confirming the closed-loop control in Fig. 4-3(a), but with much larger effective sensing area for better accuracy. The sensing and biasing of the present control circuit share one electrode. As a result, capacitance sensing and tuning take place consecutively in different time divisions. During sensing, any leakage current through biasing part of the circuit could perturb the sensing accuracy if not kept at minimum. Separate sensing and biasing provides a more robust approach, which not only frees the sensing circuit from leakage current, but also requires no isolation capacitor for high voltage isolation. Without a large isolation capacitor, the actuation/deactuation speed would be much faster, and effective sensitivity would also improve.

## *References*

1. G. Dubois, X. Chauffleur, S. Aouba and P. Pons. "MEMS design with separated electrodes for actuation and RF commutation", in *Proceeding of MicroMechanics Europe Conference*, 2009.

2. S. P. Natarajan, S. J. Cunningham, A. S. Morris, D. R. Dereus, "CMOS integrated digital RF MEMS capacitors," *Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2011 IEEE 11th Topical Meeting on* , pp.173-176, Jan. 2011.

# Publications


1. **G. Ding**, W. Wang, S. Halder, C. Palego, D. Molinero, J. C. M. Hwang, and C. L. Goldsmith, "Intelligent bipolar control of MEMS capacitive switches," accepted for publication in *IEEE Trans. Microwave Theory & Techniques*, Dec. 2012.

2. **G. Ding**, W. Wang, S. Halder, C. Palego, D. Molinero, J. C. M. Hwang, and C. L. Goldsmith, "Intelligent CMOS control of RF MEMS capacitive switches," in *Dig. IEEE Int. Microwave Symp.(MTT)*, June 2012.

3. **G. Ding**, J. Deng, L. Zhou, Q. Gan, J. C. M. Hwang, V. Dierolf, F. J. Bartoli, C. Mazuir, and W. V. Schoenfeld, "Al nanogrid electrode for ultraviolet detectors," *Optics Lett.,* vol. 36, no. 18, pp. 3663–3665, Sep. 2011.

4. **G. Ding**, C. Chen, S. Halder, J. C. M. Hwang, J. Kim, and H. Yuan, "Novel technique for determination of actual pixel size in dense arrays of infrared detectors," *IEEE Electron Device Lett.,* vol. 31, no. 8, Aug. 2010.

5. C. Chen, **G. Ding**, B. S. Ooi, L. F. Lester, A. Helmy, T. L. Koch, and J. C. M. Hwang, "Modulation-bandwidth enhancement by stimulated Raman scattering in quantum dash lasers," in *Proc. Conf. Lasers Electro-Optics,* May 2010.

6. C. Chen, **G. Ding**, B. S. Ooi, L. F. Lester, A. Helmy, T. L. Koch, and J. C. M. Hwang, "Modulation of quantum-dash semiconductor lasers by intra-cavity stimulated Raman scattering," *Optics Express*, vol. 18, no. 6, pp. 6211-6219, Mar. 2010.
7. H. Yuan, J. Kim, J. Kimchi, J. Bajaj, **G. Ding**, J. C. M. Hwang, D. Lee, B. Tennant, "Development of large format InGaAs 2D photodetector arrays with very small pixels," in *Proc. Meet. Military Sensing Symp. Detectors and Materials,* Feb. 2010.
8. **G. Ding**, C. Chen, B. S. Ooi, and J. C. M. Hwang, "Integrated waveguide photodetector for DWDM fiber-optic communications," in *Proc. Int. Conf. Materials Advanced Technologies*, 2009.
9. Y. Li, R. Wang, **G. Ding**, J. S. Klamkin, L. Johansson, P. Herczfeld, and J. E. Bowers, "Novel phase modulator linearity measurement," *IEEE Photonics Technology Lett.*, vol. 21, no. 19, pp. 1405-1407, 2009.
10. Y. Li, **G. Ding**, and P. Herczfeld, "Photonic phase-locked-loop linear phase demodulator," *Electronics Lett.,* vol. 44, no. 5, Feb. 2008
11. Y. Li, **G. Ding**, and P. Herczfeld, "Experimental demonstration of a photonic phase locked loop," in *IEEE Int. Topical Meet. Microwave Photonics,* 2007.

# Vita

Guanghai Ding was born on June 8, 1984 in Shanghai, China. He received the B.S. degree in microelectronics from Fudan University, Shanghai, China, in 2006, and the M.S. degree in electrical engineering from Drexel University, Philadelphia, PA, in 2008. He is currently pursuing the Ph.D. degree in electrical engineering at Lehigh University, Bethlehem, PA. During his study at Lehigh University, he had been awarded with Sherman Fairchild Fellowship in Solid State Studies for three consecutive years from 2009 to 2012. In 2008, he was also awarded with Dean's Doctoral Student Assistantship by P. C. Rossin College of Engineering and Applied Science, Lehigh University.

He was an Intern RF Technology Engineer with Peregrine Semiconductor, San Diego, CA, in 2011. His current research interests include modeling and characterization of RF semiconductor, MEMS, and photonic devices, as well as CMOS integrated circuit design.

He is a member of Sigma Xi, and a student member of IEEE Microwave Theory and Techniques Society.