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Characterization of InGaAs Metal-Oxide-Semiconductor Field-Effect Transistors

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Characterization of InGaAs Metal-Oxide-Semiconductor Field-Effect Transistors

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Abstract

After about fifty years of development in silicon metal-oxide-semiconductor field-effect transistor (MOSFET), it has become more and more difficult to continue transistor scaling due to the limitations in lithography, power consumption, and reliability. Recently, great effort has been put into searching for alternative channel structures or materials for future high-performance and low-power logic applications. Considerable progress has been made in the research of several novel devices, such as carbon-nanotube (CNT) field-effect transistors (FETs), silicon nanowire FETs, graphene FETs, and planar FETs with alternative channel materials such as Ge, InAs, InSb, and InGaAs. This dissertation discusses the electrical characterization of the interface traps, analysis of the inversion charge, electron mobility and junction leakage current of $Al_2O_3/In_xGa_{1-x}As$ ($x = 0.53$, 0.65 or 0.75) MOSFETs.

Charge pumping has been used to characterize the interface traps between Al_2O_3 and InGaAs in n-channel inversion-mode MOSFETs. An analysis of the charge pumping current with gate voltage pulses of different rise and fall times has enabled the interface trap density to be extracted across the energy bandgap, with an average value between the mid 10^{12} and low 10^{13} $cm^{-2}eV^{-1}$. The majority of interface traps

in indium-rich InGaAs metal-insulator-semiconductor structures have been identified as donors, which limits the off-state performance of InGaAs MOSFETs such as subthreshold slope, drain-induced barrier lowering, and on/off current ratio. The results obtained in our measurements help explain the promising on-state performance of the Al_2O_3/InGaAs MOSFETs and the need to further improve the interface so that its off-state performance can be on par with that of the Si MOSFET.

The electron mobility in Al_2O_3/InGaAs MOSFETs has been analyzed for scattering by oxide charge as well as interface charge and roughness, and compared with measured transfer characteristics from depletion to inversion. The analysis shows that in strong inversion the electron mobility can be as high as ~ 3000 cm^2/V/s and is mainly limited by interface roughness. The extracted interface roughness from the measured data is two to seven times that of the interface between a high-κ dielectric and Si, assuming the correlation lengths are comparable. Therefore, to fully benefit from the high bulk mobility of InGaAs, its interface roughness with the gate oxide needs to be further improved.

Finally, the reverse junction leakage current has been analyzed by calculating diffusion, generation, and tunneling currents, and compared with measurement at room temperature. We find that the leakage current increases with In mole fraction. Generation and tunneling currents dominate in medium- and high-bias regions, respectively.

Chapter 1

Introduction

The demand of higher speed, reduced power consumption and higher density of integration has pushed the semiconductor industry to aggressively scale the size of the basic element in silicon complementary metal-oxide-semiconductor technology (CMOS) — metal-oxide-semiconductor field-effect transistors (MOSFETs), approaching its physical limits. It is projected that the transistor with a physical gate length of 20 nm in the microprocessor unit will be in production in 2013 (Figure 1.1) [1]. Although several new technologies, such as strained-silicon channels, metal-gate/high-κ stacks and non-planar silicon transistors have been developed to sustain Moore's Law, the continuing scaling of MOSFETs beyond 22-nm node will face serious challenges from lithography, device design and modeling.

Recently, tremendous progress has been made in the research of novel technologies for future nano-electronics, including carbon-nanotube (CNT) field-effect transistors (FETs) [2–6], silicon nanowire FETs [7–12], graphene FETs [13–19], and

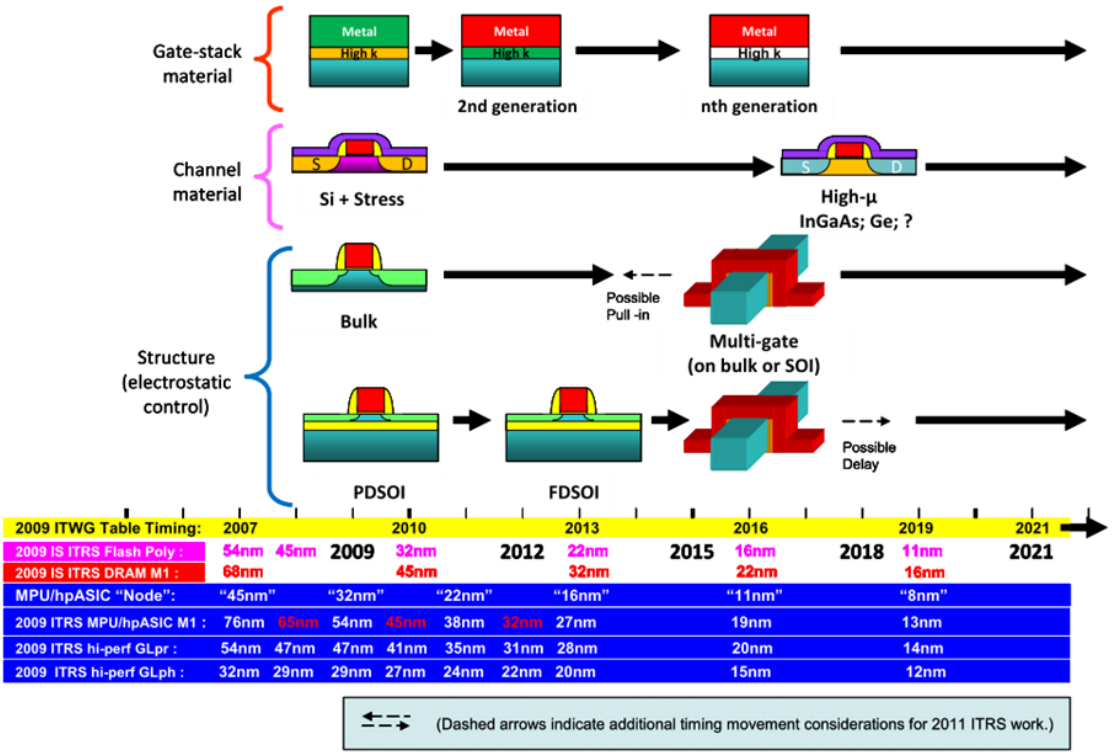

Figure 1.1: Overall roadmap technology characteristics predicted by international technology roadmap for semiconductors (ITRS) [1].

planar FETs with alternative channel materials. Benefiting from high electron mobility, channel materials such as InGaAs [20,21], InAs [22,23], and InSb [24,25] have been demonstrated in high-electron-mobility or quantum-well transistors, achieving superior device metrics. However, high gate leakage current in these transistors limits their application in large scale integration. On the other hand, operating under the same mechanism as silicon MOSFETs, surface channel inversion-type MOSFETs have been demonstrated by integrating high-κ gate dielectrics and alternative channel materials like germanium [26, 27] or InGaAs [28–39], showing promising performance for high-speed low-power logic applications.

1.1 Basic Properties of III-V Semiconductors

Generally, III-V semiconductors are referred as chemical compounds with at least one group III element and at least one group V element in the periodic table of the chemical elements. Various group III and V elements can form different III-V semiconductors, covering a wide range of energy bandgap and electromagnetic spectrum as shown in Figure 1.2. This variety determines their important roles in many electronic and photonic device applications.

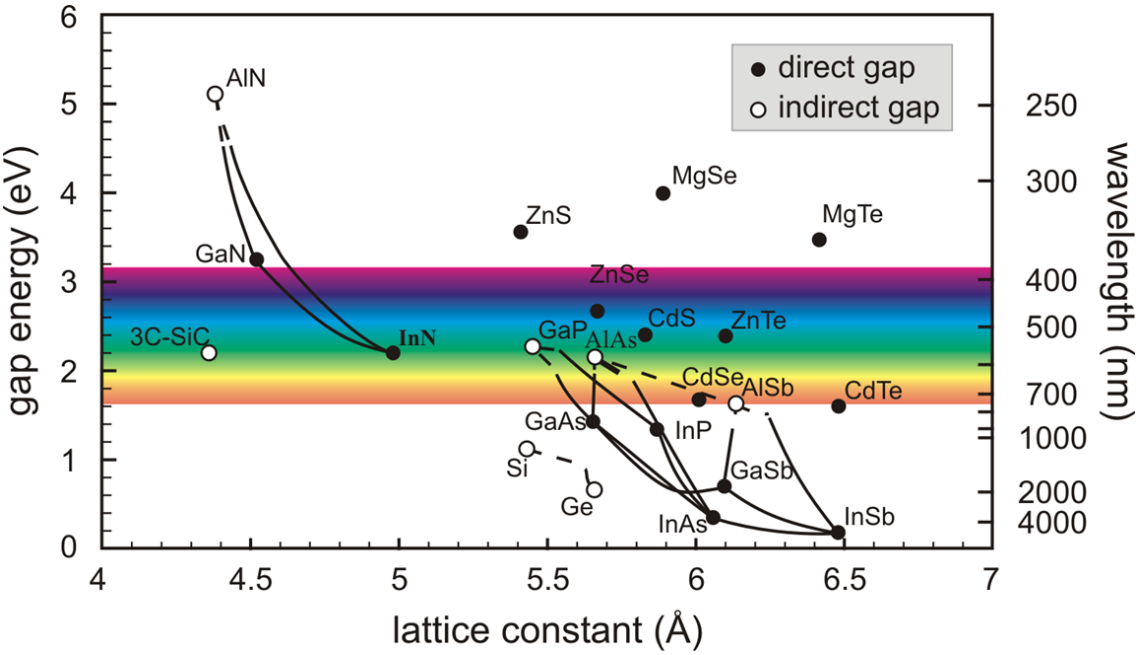

Figure 1.2: The relationship of bandgap energy and lattice constant for common III-V semiconductors [40].

One significant property of III-V semiconductors is that most of them are direct bandgap semiconductors, which means the wave vector k has the same value at the lowest point E_C in the conduction band as at the highest point E_V in the valence

band. Thus no phonon is required for the transition of an electron from the valence band to the conduction band, which makes III-V semiconductors much more efficient photonic material for light emitting diodes (LEDs), semiconductor lasers and photo detectors than silicon. Figure 1.3 compares the band diagrams of GaAs and Si. It is seen clearly that E_{C} and E_{V} points are aligned at the same wave vector k value.

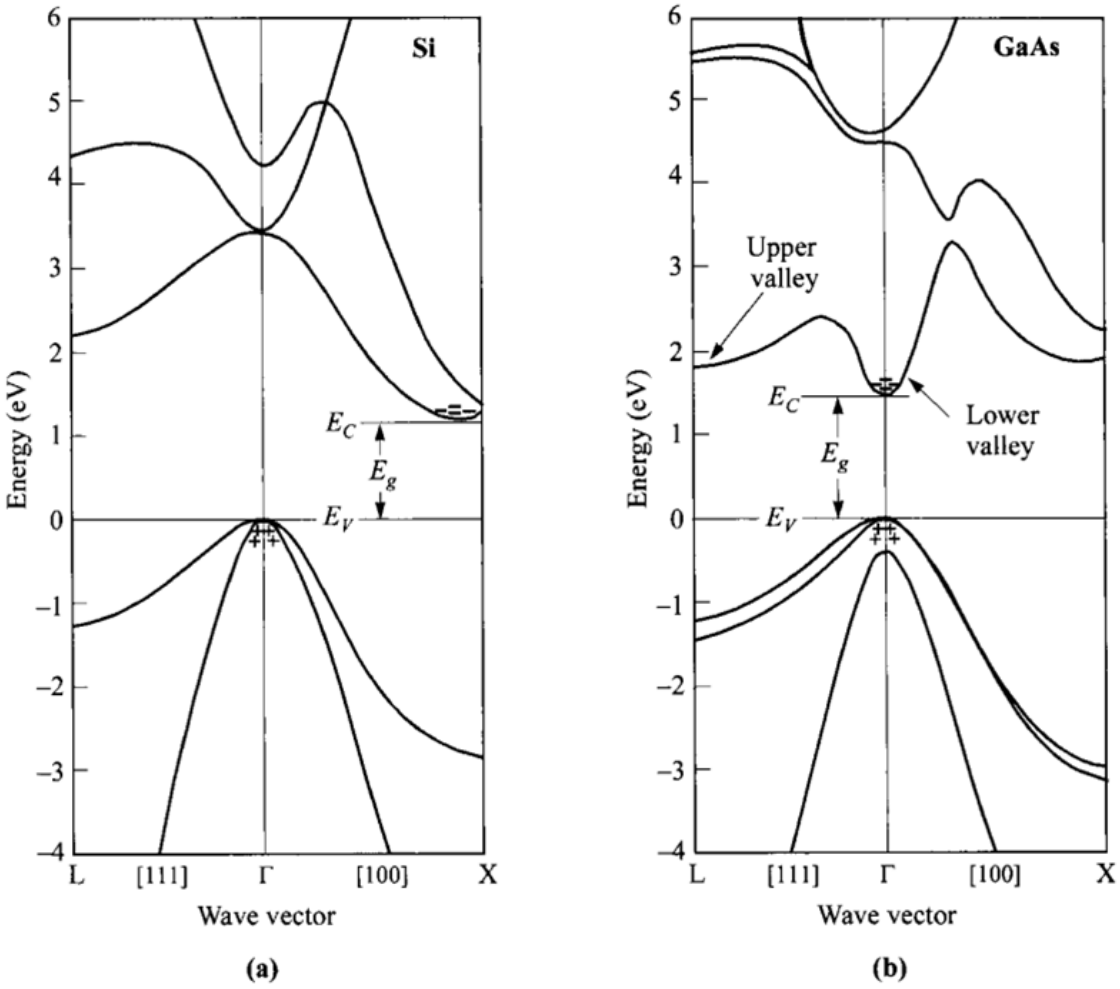

Figure 1.3: Energy band structures of (a) Si and (b) GaAs [41].

Another important advantage is the electron mobility. Many III-V semiconductors have a bulk electron mobility higher than silicon as shown in Figure 1.4. For narrow bandgap semiconductor such as InSb, InAs and indium-rich InGaAs, their bulk electron mobilities can even be well above 10^4 cm^2/V/s, which is more than ten times of silicon, making them good candidates for high-speed low-power applications.

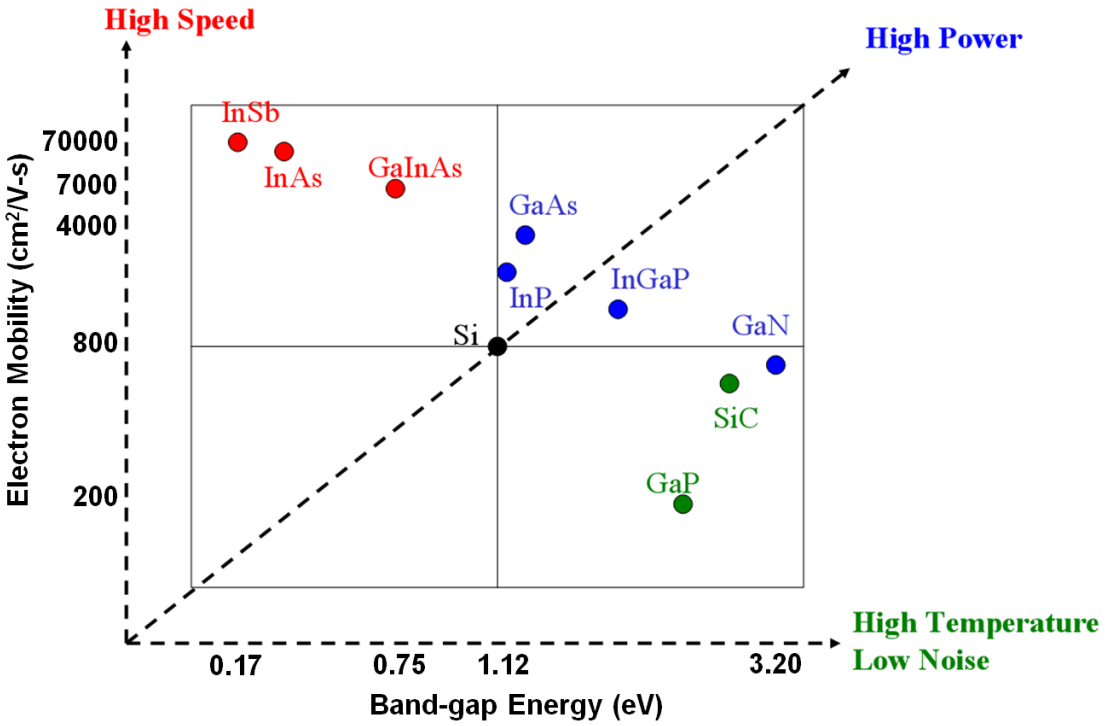

Figure 1.4: Bulk electron mobility of common III-V semiconductors.

Because of the large bandgap difference, various III-V semiconductors are often used to form heterojunctions. A heterojunction means the p-type and n-type regions of a p-n junction are made of different semiconductor materials and thus

has some unique properties. For example, as shown in Figure 1.5(a), in a graded heterojunction bipolar transistor (HBT), the emitter is made of a larger-bandgap material such as AlGaAs while the base is made of a smaller-bandgap material such as GaAs. Therefore the holes in the base experience a much larger energy barrier than electrons in the emitter, which reduces the hole back-injection and increases the emitter injection efficiency. A heterojunction is also usually used in the concept

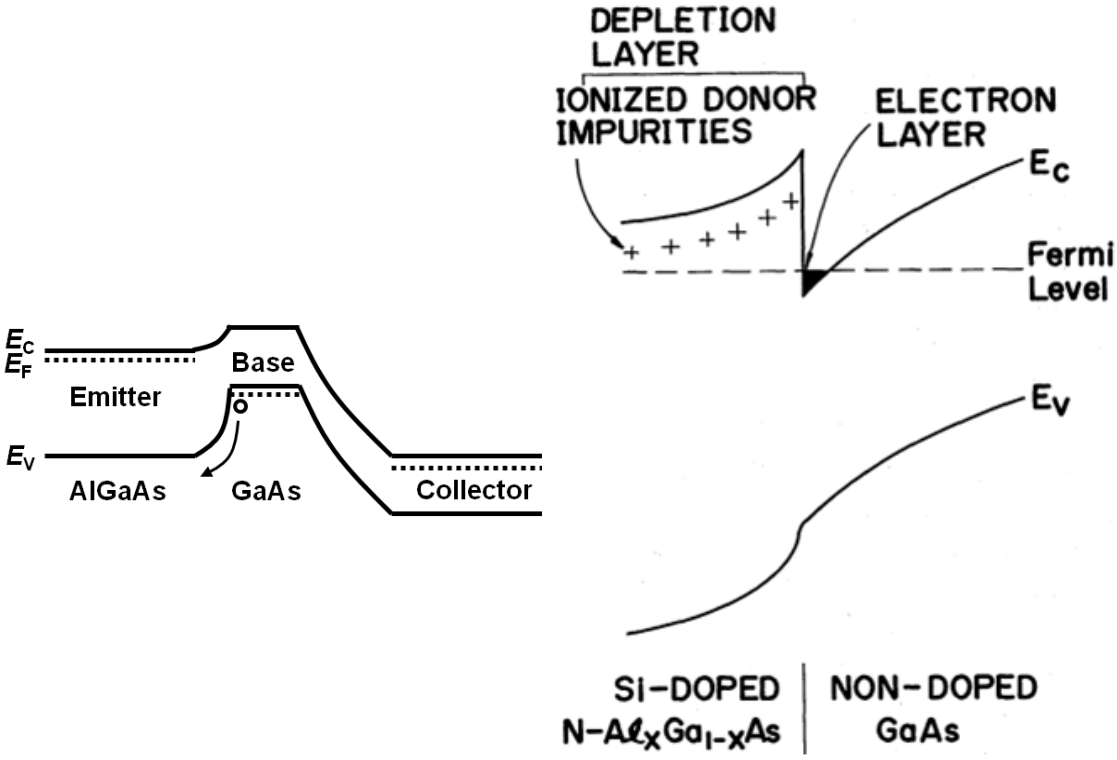

Figure 1.5: Energy band diagram of a graded AlGaAs/GaAs HBT and an AlGaAs/GaAs HEMT [42].

of modulation doping, in which the dopants are separated from the location where

carriers conduct the current. Consequently, the carriers are free from impurity scattering and have a higher mobility. This concept directly results in the invention of high-electron-mobility transistor (HEMT). For example, in a typical HEMT transistor (Figure 1.5(b)), the electrons accumulate in the interface of AlGaAs/GaAs heterojunction and are separated from dopants which are further away inside the AlGaAs layer. The heterojunction device like HBT and HEMT have very important applications in radar and communication systems.

III-V semiconductors also contains another category of materials located on the mid-upper left part of Figure 1.2 — nitride-based wide bandgap semiconductors. These semiconductors have a very wide energy bandgap, usually above 3 eV, corresponding to an emission spectrum in UV range. Thus they are often used in UV LEDs and UV detectors. The wide bandgap also is associated with a large breakdown voltage. The field-effect transistor based on nitride usually can handle much higher power and is being developed for wireless base station and radars.

Table 1.1 summarize several material parameters for common III-V semiconductors as well as silicon.

1.2 Development of III-V MOSFETs

1.2.1 History of III-V MOSFETs

Not long after the first MOSFET was invented by Dawon Kahng at Bell Laboratories in 1960 [43], the first attempt of using GaAs for a MOSFET was made in 1965,

Parameters	InSb	InAs	$In_{0.53}Ga_{0.47}As$	GaAs
k_S	16.8	15.1	13.9	13.1
N_C (cm^{-3})	4.2×10^{16}	8.7×10^{16}	2.8×10^{17}	4.7×10^{17}
N_V (cm^{-3})	7.3×10^{18}	6.6×10^{18}	6.0×10^{18}	7.0×10^{18}
E_G (eV)	0.17	0.35	0.74	1.424
m_e^*/m_0	0.014	0.023	0.041	0.067
μ_n ($cm^2/V/s$)	77000	25000	7000	4000
μ_p ($cm^2/V/s$)	850	500	300	250
v_{SAT} (m/s)	5×10^7	4×10^7	7×10^6	8×10^6

Parameters	InP	GaN[a)]	Ge	Si
ϵ_r	12.6	8.9	16.2	11.9
N_C (cm^{-3})	5.8×10^{17}	2.3×10^{18}	1.0×10^{19}	2.8×10^{19}
N_V (cm^{-3})	1.0×10^{19}	4.6×10^{19}	5.0×10^{18}	1.0×10^{19}
E_G (eV)	1.35	3.4	0.66	1.12[b)]
m_e^*/m_0	0.078	0.2	0.082	0.26
μ_n ($cm^2/V/s$)	3200	1000	3900	800
μ_p ($cm^2/V/s$)	150	30	1900	400
v_{SAT} (m/s)	1.5×10^7	2.5×10^7	1×10^7	8×10^6

[a)]wurtzite crystal structure [b)]indirect bandgap

Table 1.1: Material parameters for common III-V semiconductors, germanium and silicon at room temperature.

reported by Becke and White at the Radio Corporation of America [44]. Working under depletion mode and with pyrolytic deposited SiO_2 as gate dielectric, the devices were successfully operated up to a few megahertz, despite the existence of a large number of interface traps. Although the native oxide of silicon — SiO_2 works as an excellent gate dielectric for silicon MOSFET, the native oxides for III-V materials are usually a complex mixture of cationic and anionic oxides, which are usually not stable and leaky, have a large amount of defects and create significant surface states on the oxide-semiconductor interface. Various approaches to grow native oxides on GaAs, including thermal oxidation, wet-chemical anodization, DC and

RF plasma oxidation, laser-assisted oxidation, vacuum ultraviolet photochemical oxidation and photowash oxidation have been studied and proofed to be non-feasible [45]. On the other hand, a variety of deposited oxides have been investigated as well, including pyrolytically deposited silicon dioxide, silicon nitride, silicon oxynitride and aluminum oxide [45]. It was soon realized that high temperature deposition processes boost the chemical reaction between GaAs and oxygen to form native oxide and vacancies, degrading semiconductor-oxide interface. Later, plasma-enhanced deposition was introduced to reduce the process temperature. However, additional defects at the interface were introduced by plasma induction [45].

While researchers were struggling to find a proper gate dielectric for III-V semiconductor, the discovery of mobility enhancement of a modulation-doped heterojunction superlattice by Bell Laboratories led to the invention of an important type of device — high-electron-mobility transistor (HEMT) by Fujitsu in 1980 [42]. As discussed in the previous section, electrons traveling in the quantum well near the heterojunction interface are free from Coulomb-scattering and therefore can achieve a much higher mobility [46]. HEMTs have become more and more important in many areas such as communication, radar and military systems. However, the high leakage current from the Schottky gate prevents them from a very large scale integration. The research on HEMTs for future logic application is still currently ongoing and HEMTs with different channel materials such as In-rich InGaAs [20,21], InAs [22, 23] and InSb [24, 25] have been experimented and benchmarked for logic applications [47].

In the late 1980s, the Bell Laboratories discovered that sulfur passivation could provide excellent electronic properties for GaAs substrate, which stimulated another cycle of research for suitable dielectrics on GaAs. Later in 1995, MOS structures with low interface traps (D_{it}) on GaAs substrate were reported by Passlack and Hong at the Bell Laboratories. The MOS structure used $Ga_2O_3(Gd_2O_3)$ as the gate dielectric which was deposited by electron-beam evaporation from single-crystal $Ga_5Gd_3O_{12}$ in an ultrahigh-vacuum MBE system. Based on this finding, many new devices, including the GaAs depletion-mode and enhancement-mode MOSFETs, GaAs complementary MOSFETs, InGaAs enhancement mode MOSFETs and GaAs power MOSFETs were demonstrated [45].

1.2.2 Recent Advances of III-V MOSFETs

The intensive research and development activities for high-κ materials on silicon MOSFETs in the mid-1990s and 2000s brought new directions to III-V research. The use of atomic layer deposition (ALD) for high-κ gate dielectric on III-V substrate has offered new approaches to achieve a high quality interface. Starting from 2001, Ye and Wilk at Bell Laboratories or later Agere Systems demonstrated a series of depletion-mode MOSFETs with ALD Al_2O_3 gate dielectric on GaAs and InGaAs substrates [45]. Later, Ye's group at Purdue University continued to integrate ALD gate dielectric with other III-V substrates such as InP [48, 49] and GaN [50]. High-performance enhancement-mode inversion-type InGaAs MOSFETs with a record-breaking drive current were also reported by Ye's group [28, 29]. The scalability of

InGaAs MOSFETs to deep submicron level has been studied as well [30]. The ability of ALD process to unpin the Fermi-level in III-V semiconductors has generated great interest in academia and industry. Many researchers are now working in this direction.

On the other hand, in terms of device design, to increase the gate control of channel and reduce short channel effect, 3D structures, such as FinFET demonstrated for silicon MOSFETs, have also been experimented on III-V substrates, showing an improved electrostatics [38, 51]. Furthermore, substrate orientation plays an important roles in device performance. For example, researchers have shown that the Fermi level is only unpinned on GaAs (111)A surface [52]. Also, InGaAs MOSFETs are reported to have a higher electron mobility on (111)A substrate than that on a (100) substrate [53].

After the successful demonstration of III-V MOSFETs, researchers started to experiment integrating III-V MOSFETs on silicon substrate [39, 54, 55]. Although this technology still faces a lot of challenges, III-Vs MOSFETs are seriously knocking on the door of the CMOS road map.

1.3 Scope of the Dissertation

This dissertation focuses on understanding device performance of $Al_2O_3/In_xGa_{1-x}As$ ($x = 0.53$, 0.65 or 0.75) MOSFETs through electrical characterizations. Chapter 2 discusses the characterization of interface traps using charge pumping technique. The interface trap density is extracted and its property

is discussed. Chapter 3 presents the analysis of electron mobility in terms of scattering by oxide charge as well as interface charge and roughness. Based on the knowledge of Chapter 2 and Chapter 3, the transfer characteristics under low drain bias have been simulated and compared with measurements. Chapter 4 discusses the reverse junction leakage current. By breaking down the leakage current to diffusion, generation, and tunneling currents, a model has been extracted and compared to measurements. Chapter 5 presents the conclusion of this dissertation and recommends future research.

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Chapter 2

Interface Characterization of InGaAs MOSFETs

Researchers have been trying to improve the quality of the interface between gate dielectric and III-V semiconductor for over four decades. A good understanding of the interface states is very important in explaining device operation as well as in device modeling. Since the interface between gate dielectric and III-V semiconductor usually has a much higher interface trap density, some of these techniques (e.g. the conductance method), which work nicely with silicon MOSFETs, will have large errors or need extra efforts when used on III-V MOSFETs. The charge pumping technique, based on the direct measurement of recombination current of interface traps, is the most sensitive and reliable tool to characterize interface trap properties of MOSFETs on various substrates. In this chapter, InGaAs MOSFETs will be introduced and charge pumping will be used to characterize their interface properties.

The results will also be briefly compared with the subthreshold slope technique.

2.1 InGaAs MOSFETs Under Study

2.1.1 Device Structure and Fabrication Process

Figure 2.1 illustrates the structure of the $In_xGa_{1-x}As$ MOSFETs used in this study. A 500-nm layer of $In_{0.53}Ga_{0.47}As$ p-doped to $4 \times 10^{17}cm^{-3}$, a 300-nm layer of $In_{0.53}Ga_{0.47}As$ p-doped to $1 \times 10^{17}cm^{-3}$, and a 15- to 20-nm layer of $In_xGa_{1-x}As$ (x = 0.53, 0.65 or 0.75) p-doped to $1 \times 10^{17}cm^{-3}$ were sequentially grown on p^+-doped InP substrates by molecular beam epitaxy (MBE). An 8- to 10-nm layer of Al_2O_3 with a dielectric constant k_{OX} of 9 was then formed on top of the $In_xGa_{1-x}As$ by atomic layer deposition (ALD) as the gate oxide. The gate was metalized with evaporated Ni and Au. Although only $In_{0.53}Ga_{0.47}As$ is lattice-matched to InP (see Figure 1.2), the channel layer is pushed to $In_{0.75}Ga_{0.25}As$ which is at the limit of pseudomorphic growth to achieve higher electron mobility, because the bulk electron mobility increases with indium mole fraction [1]. Compared to HEMTs, these InGaAs MOSFETs with a gate dielectric can significantly reduce the gate leakage current and therefore reduce the DC power consumption.

The fabrication process starts with surface degreasing and ammonia-based native oxide etching. The wafers were then transferred to an ASM F-120 ALD reactor via room ambient. A 30-nm thick Al_2O_3 encapsulation layer was deposited at a substrate temperature of 300 °C. Source and drain regions were implanted with a

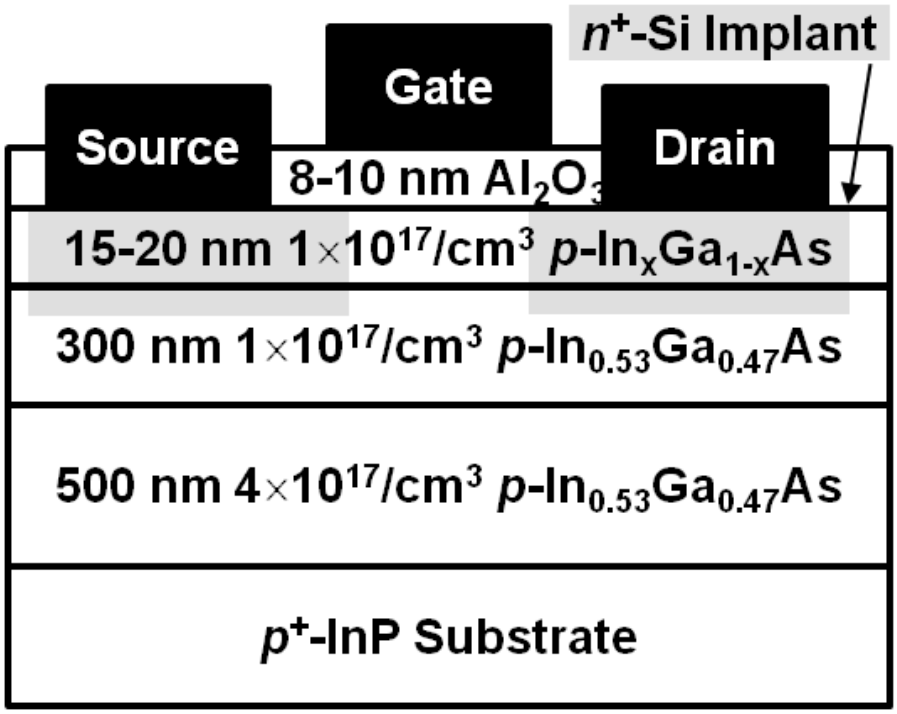


Figure 2.1: Bulk electron mobility of common III-V semiconductors.

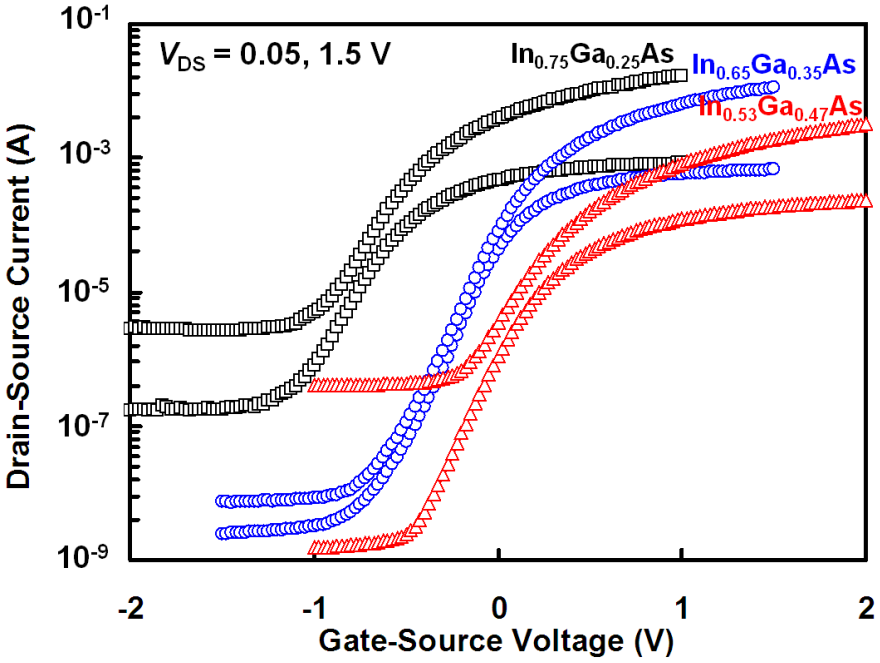
silicon dose of 1×10^{14} cm^{-2} at 30 keV and 80 keV through the Al_2O_3 encapsulation layer and then activated by rapid thermal annealing (RTA) at 700–800 °C for 10 seconds in a N_2 ambient. After removing the encapsulation layer, buffered oxide etching (BOE) and a surface treatment with ammonia sulfide, an 8- to 10-nm Al_2O_3 was regrwon with ALD as the gate dielectric, followed by 400–600 °C post deposition anealing. Then the source and drain contacts were formed with an electron beam evaporation of AuGe, Ni and Au and defined by a lift-off process. After an RTA at 400 °C for 30 seconds in N_2 ambient, the gate electrode was deposited by electron beam evaporation of Ni and Au [2].

2.1.2 Device Characteristics

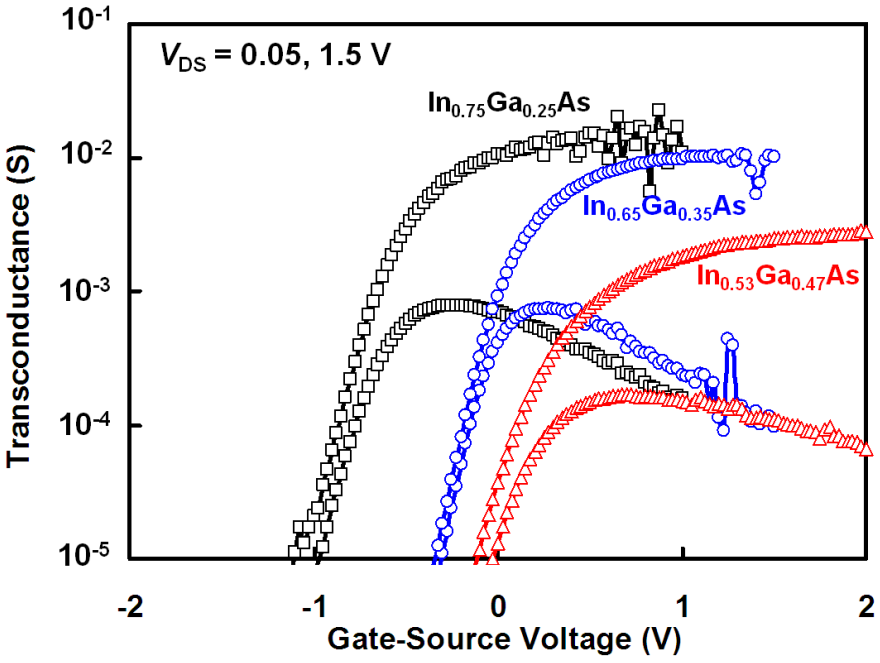
Figure 2.2 shows typical current-voltage characteristics of the $In_xGa_{1-x}As$ MOSFETs with a gate width W of 100 μm and a gate length L of 4 μm at room temperature. All measurements are performed on-wafer by using an Agilent 4156C Precision Semiconductor Parameter Analyzer and a Cascade Summit 12000 Probe Station with a microchamber ambient enclosure with a 0.1 °C temperature control.

We observe that both the maximum drain-source current and transconductance increase with an increas in the indium mole fraction x. One reason is that both the low-field electron mobility and saturation velocity increases with increasing indium mole fraction [3, 4], because of the decreasing electron effective mass. Also, the bandgap energy E_G is proportional to the indium mole fraction, which means the InGaAs channel with higher indium mole fraction requires smaller surface potential (band-bending or the Fermi-level movement) to reach the same density of inversion charges. On the other hand, a smaller E_G means a higher junction leakage current, which will be discussed in Chapter 4.

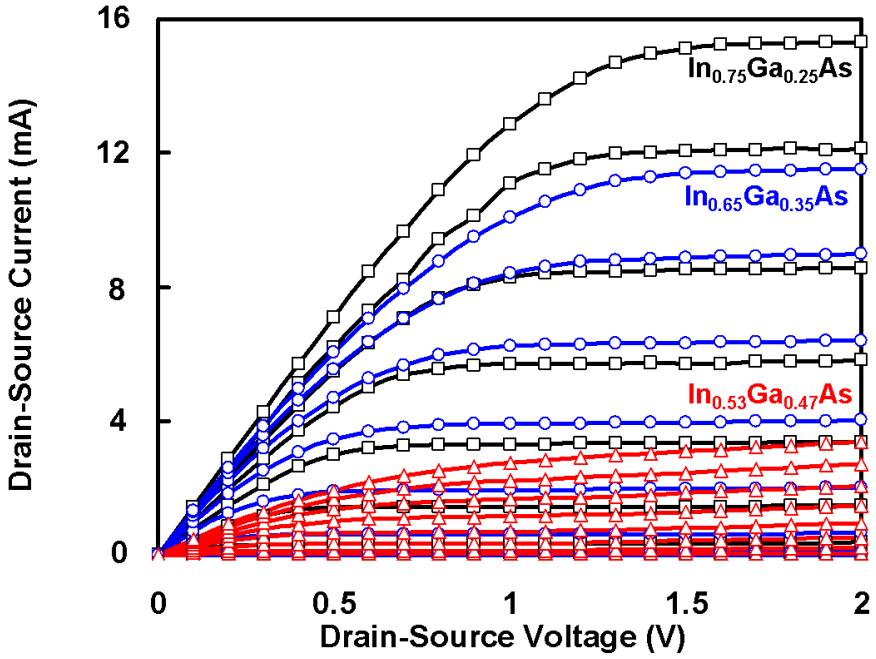
The gate leakage current is less than 10 nA or 2.5×10^{-3} A/cm^2 for all devices in the bias range under test. The subthreshold swings are about 210 mV/decade, 160 mV/decade, and 170 mV/decade for $In_{0.75}Ga_{0.25}As$, $In_{0.65}Ga_{0.35}As$, and $In_{0.53}Ga_{0.47}As$ MOSFETs, respectively. The relative large subthreshold swing is due to high interface trap density and will be discussed in the next section.


V_{DS} = 0.05, 1.5 V
$In_{0.75}Ga_{0.25}As$
$In_{0.65}Ga_{0.35}As$
$In_{0.53}Ga_{0.47}As$
Drain-Source Current (A)
10^{-1}
10^{-3}
10^{-5}
10^{-7}
10^{-9}
-2
-1
0
1
2
Gate-Source Voltage (V)

(a)


V_{DS} = 0.05, 1.5 V
$In_{0.75}Ga_{0.25}As$
$In_{0.65}Ga_{0.35}As$
$In_{0.53}Ga_{0.47}As$
Transconductance (S)
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
-2
-1
0
1
2
Gate-Source Voltage (V)

(b)



(c)

Figure 2.2: (a) (b) Transfer characteristics and (c) output characteristics of $In_{0.75}Ga_{0.25}As$ (□), $In_{0.65}Ga_{0.35}As$ (◯), and $In_{0.53}Ga_{0.47}As$ (△) MOSFETs with a gate width W of 100 μm and a gate length L of 4 μm at room temperature. The transfer characteristics are measured at drain-source voltages V_{DS} of 0.05 V and 1.5 V. The output characteristics are measured at gate-source voltages V_{GS} of −0.75 V to 1 V for $In_{0.75}Ga_{0.25}As$, −0.25 V to 1.5 V for $In_{0.65}Ga_{0.35}As$, and 0.25 V to 2 V for $In_{0.53}Ga_{0.47}As$ with a 0.25 V step size.

2.2 Interface Characterization Techniques

2.2.1 Charge Pumping

Alternative substrates are known to have a poorer quality of insulator-semiconductor interface, usually with an interface trap density of 10^{12}–10^{13} $cm^{-2}eV^{-1}$. The techniques which have worked reliably for silicon MOSFETs for years may easily be

misinterpreted on alternative substrates. For example, if the interface trap capacitance $C_{\rm it} = q^2 D_{\rm it}$ is larger than the oxide capacitance $C_{\rm OX}$, $C_{\rm it}$ will dominate the MOS admittance and the conductance $G_{\rm P}$ is not sensitive to variations of interface trap density as shown in Figure 2.3. Therefore, $D_{\rm it}$ can be underestimated [5]. In this case, the conductance method is not suitable for $D_{\rm it}$ extraction.

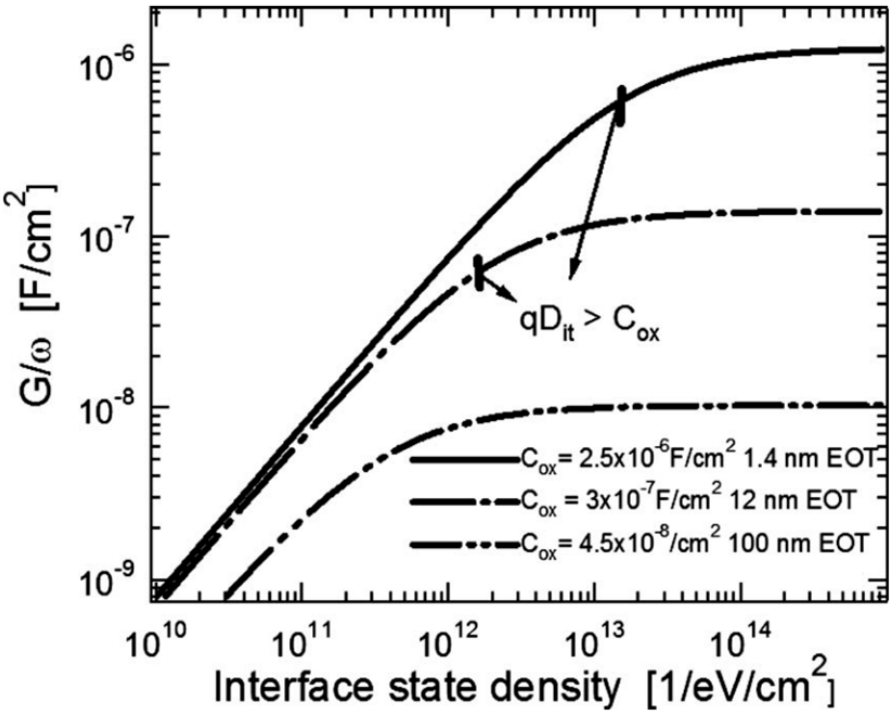


Figure 2.3: The quantity, the parallel conductance divided by the angular frequency $G_{\rm P}/\omega$, used in the conductance method is no longer sensitive to $D_{\rm it}$ after $C_{\rm it}$ is larger than $C_{\rm OX}$ [5].

Proposed by Brugler and Jespers [6], the charge pumping method has become the most reliable and sensitive tool to measure interface trap density on small-geometry silicon MOSFETs, and is still effective on alternative substrates [7–9]. It can measure $D_{\rm it}$ in the order of 10^9 cm^{-2}eV^{-1} or even lower, determine energy

distribution of interface traps, provide information on spatial location of interface trap formation, and measure oxide bulk traps in SiO_2 or high-κ gate stacks [10].

As shown in Figure 2.4, the charge pumping measurement is performed by applying a varying gate voltage and measuring charge pumping current (I_{CP}) from the source and drain or from the substrate. Source and drain are tied together to a slightly reverse biased voltage or just ground and the substrate is grounded. The

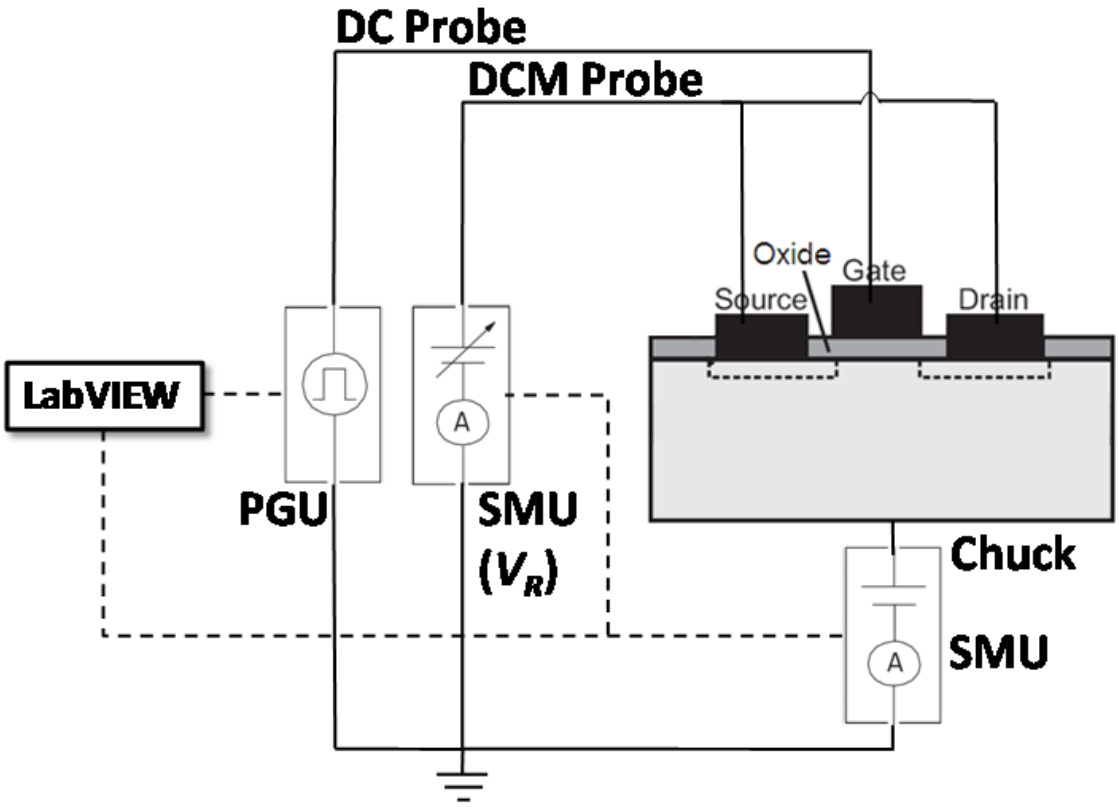


Figure 2.4: A charge pumping test setup.

applied gate voltage can be sinusoidal, square, trapezoidal or triangular as long as it can bring the MOSFET to accumulation and inversion back and forth. Usually

a square or trapezoidal waveform is used as shown in Figure 2.5(a), where the high level (V_{GH}), low level (V_{GL}), amplitude (ΔV_{G}), rise time (t_{R}), fall time (t_{F}), pulse period (T), and pulse frequency (f) are also defined. The measurement scheme can be variable-amplitude by keeping the base voltage constant at accumulation and sweeping pulse amplitude into inversion or variable-base by keeping the pulse amplitude constant and sweeping the base voltage from accumulation to inversion shown in Figure 2.5(b) and (c). In either case, a maximum I_{CP} will be measured when V_{GL} is smaller than the flat-band voltage V_{FB} while V_{GH} is larger than the threshold voltage V_{T}.

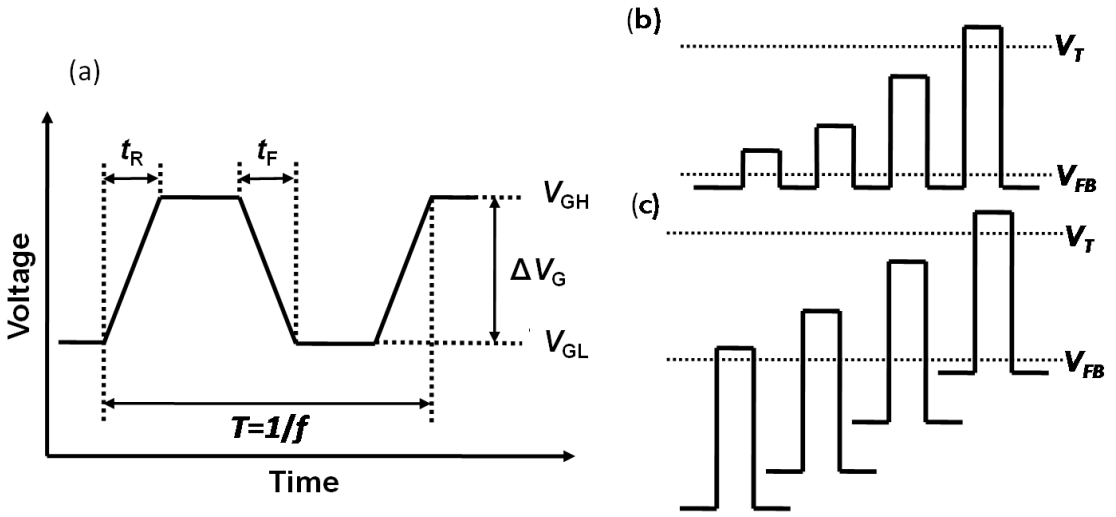


Figure 2.5: (a) Square or trapezoidal waveform used in charge pumping measurement. The pulsing scheme in variable-amplitude charge pumping (b) and variable-base charge pumping (c).

When a MOSFET is switched from inversion to accumulation, the minority carriers in the inversion layer drift to source and drain and those trapped in the interface traps near the band edge are thermally emitted. However, a large part of

the trapped minority carriers on the interface traps deeper in the band gap remains there because they do not have enough time to be emitted. Once the barrier to majority carriers is reduced, the majority carriers, which come from the substrate, will flow to the surface, recombine with minority carriers trapped on the interface traps and finally fill the traps. The inverse process happens when the MOSFET is switched from accumulation to inversion. Most of the majority carriers flow back to the substrate, leaving those trapped in the interface traps. The minority carriers coming from the source and drain, recombine with the trapped majority carriers and fill the interface traps again. The recombination process continues as the MOSFET is switching back and forth, generating a charge pumping current I_{CP} proportional to D_{it}.

Charge pumping current is a result of electron-hole recombination at interface or near-interface traps. But the actual measured current may come from two other sources, gate leakage current and the geometric component. For MOSFETs with thin oxides and low interface traps, gate leakage current can easily surpass charge pumping current and should be subtracted from measured I_{CP}. The geometric component is due to excess minority carriers in the inversion layer unable to be collected by source and drain. Normally, when the gate is pulsed from inversion to accumulation, free minority carriers flow back to source and drain. If this process cannot be completed before majority carriers from the substrate arrive at the surface, for example, due to low mobility [11] or a very long channel length [12], then the remaining free minority carriers will recombine with majority carriers at the surface,

contributing to I_{CP}. In the present InGaAs MOSFET, the gate contact pad is built on top of the same p-doped InGaAs layers and InP substrate as the gate itself without any isolation. Thus the inversion charges coming from the source and drain can travel all the way to the area underneath the gate pad and recombine with majority carriers, giving rise to a high geometric component of charge pumping current. This geometric component is strongly dependent on the falling time of gate pulse and can be mistakenly interpreted as a higher D_{it} existing in the upper bandgap [13] and, therefore, must be eliminated. This is confirmed by a near-zero interception of the linear fitting line of measured I_{CP} after the gate contact pads are physically scribed off as shown in Figure 2.6. All charge pumping measurements discussed later are performed on devices without gate contact pads, by directly probing the effective gate electrodes.

The maximum I_{CP} is given by [14]

$$I_{\mathrm{CP}} = 2q\overline{D_{\mathrm{it}}} f A_{\mathrm{G}} k_{\mathrm{B}} T \ln\left(v_{\mathrm{th}} n_{\mathrm{i}} \sqrt{\sigma_{\mathrm{n}}\sigma_{\mathrm{p}}} \frac{|V_{\mathrm{FB}} - V_{\mathrm{T}}|}{|\Delta V_{\mathrm{G}}|} \sqrt{t_{\mathrm{F}} t_{\mathrm{R}}}\right) \tag{2.1}$$

where A_{G} is the gate area, k_{B} is the Boltzmann's constant, T is the ambient temperature, v_{th} is the thermal velocity, n_{i} is the intrinsic carrier concentration, σ_{n} and σ_{p} are electron and hole capture cross-sections. The average interface trap density $\overline{D_{\mathrm{it}}}$ can be calculated from Equation (2.1).

To extract the energy distribution of D_{it}, the energy range of interface traps involved in the recombination process needs to be scanned. It can be achieved by sweeping t_{R} and t_{F} independently in the trapezoidal waveform applied to the

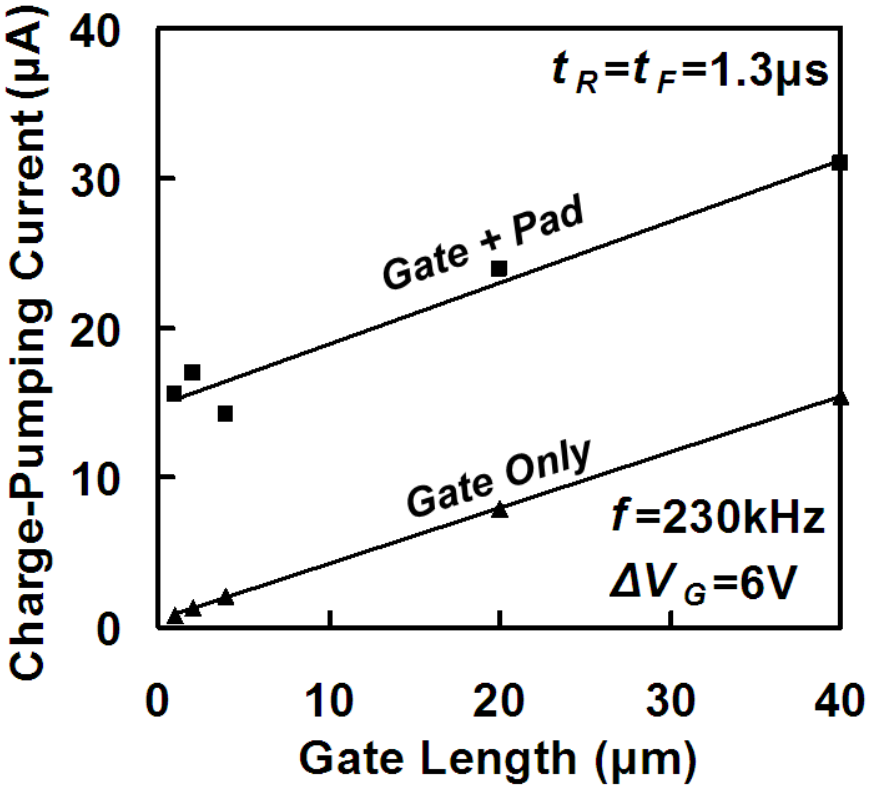
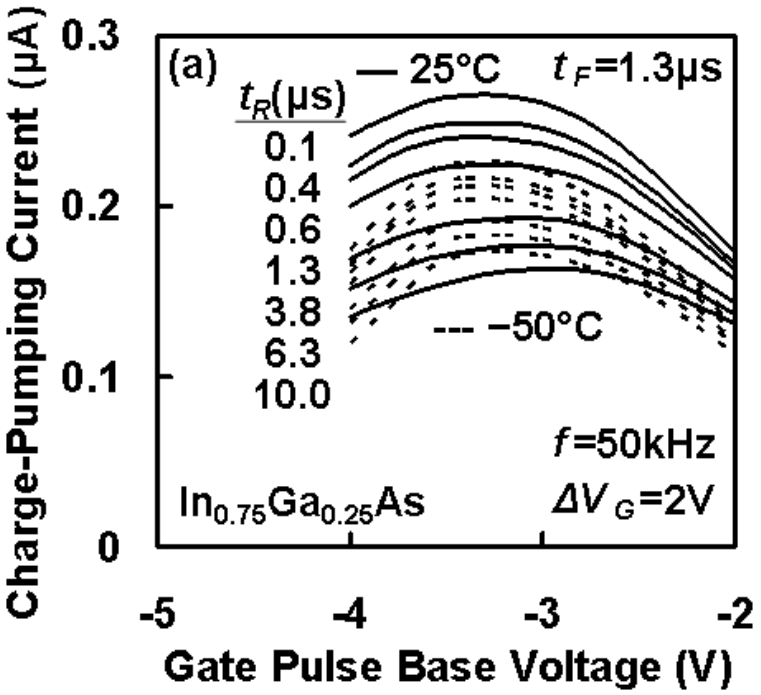
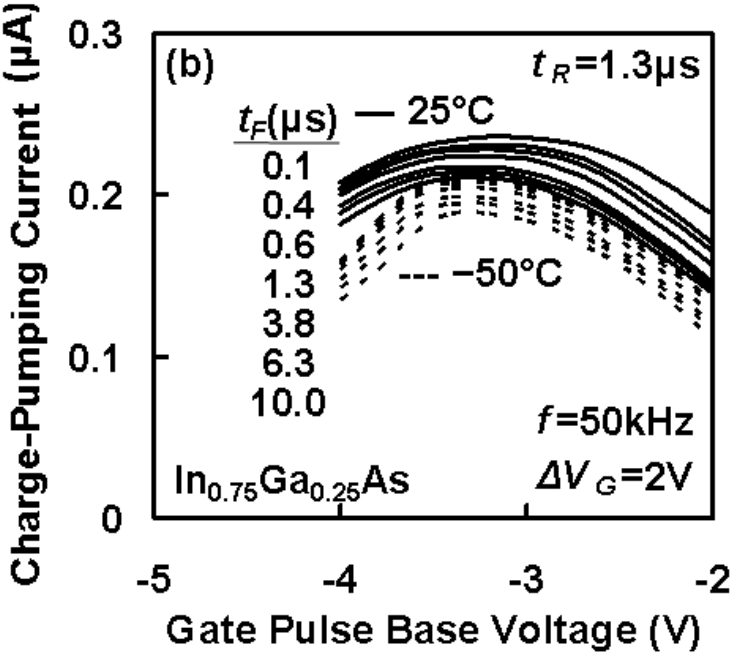


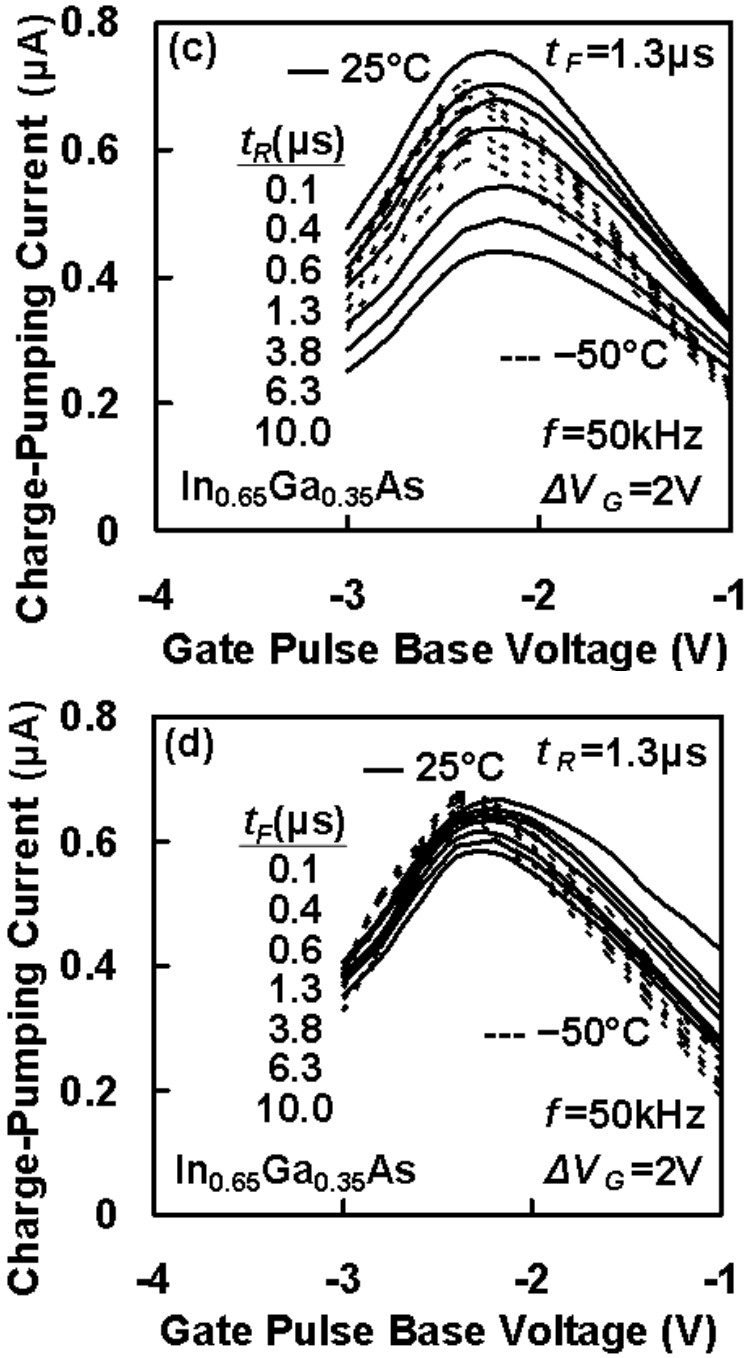
Figure 2.6: Maximum I_{CP} from variable-amplitude measurement on $In_{0.75}Ga_{0.25}As$ MOSFETs with different gate lengths before and after their gate contact pads are scribed off.

gate electrode. Figure 2.7 shows the measured I_{CP} by variable-base charge pumping method on $In_xGa_{1-x}As$ MOSFETs at both room temperature and -50 °C. The charge-pumping measurement was performed by using an Agilent 4156C Precision Semiconductor Parameter Analyzer with an Agilent 41501B Pulse Generator Expander. During the charge-pumping measurement, the 41501B generates gate voltage pulses while the 4156C measures the I_{CP} from the source and drain.

In this case, the maximum I_{CP} is proportional to the amount of interface traps


(a)
— 25°C
t_F=1.3μs
t_R(μs)
0.1
0.4
0.6
1.3
3.8
6.3
10.0
--- −50°C
f=50kHz
$In_{0.75}Ga_{0.25}As$
ΔV_G=2V
Charge-Pumping Current (μA)
0.3
0.2
0.1
0
-5
-4
-3
-2
Gate Pulse Base Voltage (V)


(b)
t_R=1.3μs
t_F(μs)
— 25°C
0.1
0.4
0.6
1.3
3.8
6.3
10.0
--- −50°C
f=50kHz
$In_{0.75}Ga_{0.25}As$
ΔV_G=2V
Charge-Pumping Current (μA)
0.3
0.2
0.1
0
-5
-4
-3
-2
Gate Pulse Base Voltage (V)


(c)
— 25°C
t_F=1.3μs
t_R(μs)
0.1
0.4
0.6
1.3
3.8
6.3
10.0
--- −50°C
f=50kHz
$In_{0.65}Ga_{0.35}As$
ΔV_G=2V
Charge-Pumping Current (μA)
0.8
0.6
0.4
0.2
0
-4
-3
-2
-1
Gate Pulse Base Voltage (V)
(d)
— 25°C
t_R=1.3μs
t_F(μs)
0.1
0.4
0.6
1.3
3.8
6.3
10.0
--- −50°C
f=50kHz
$In_{0.65}Ga_{0.35}As$
ΔV_G=2V
Charge-Pumping Current (μA)
0.8
0.6
0.4
0.2
0
-4
-3
-2
-1
Gate Pulse Base Voltage (V)

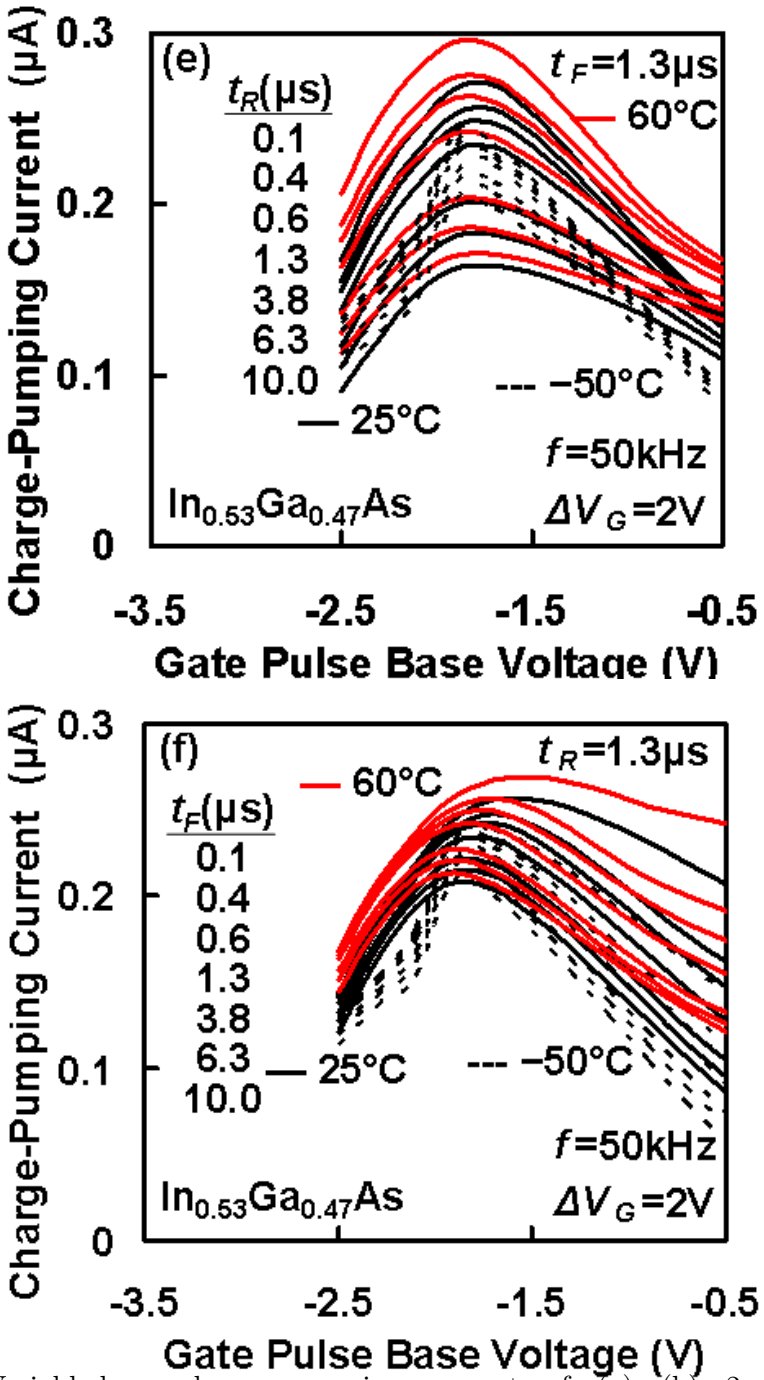


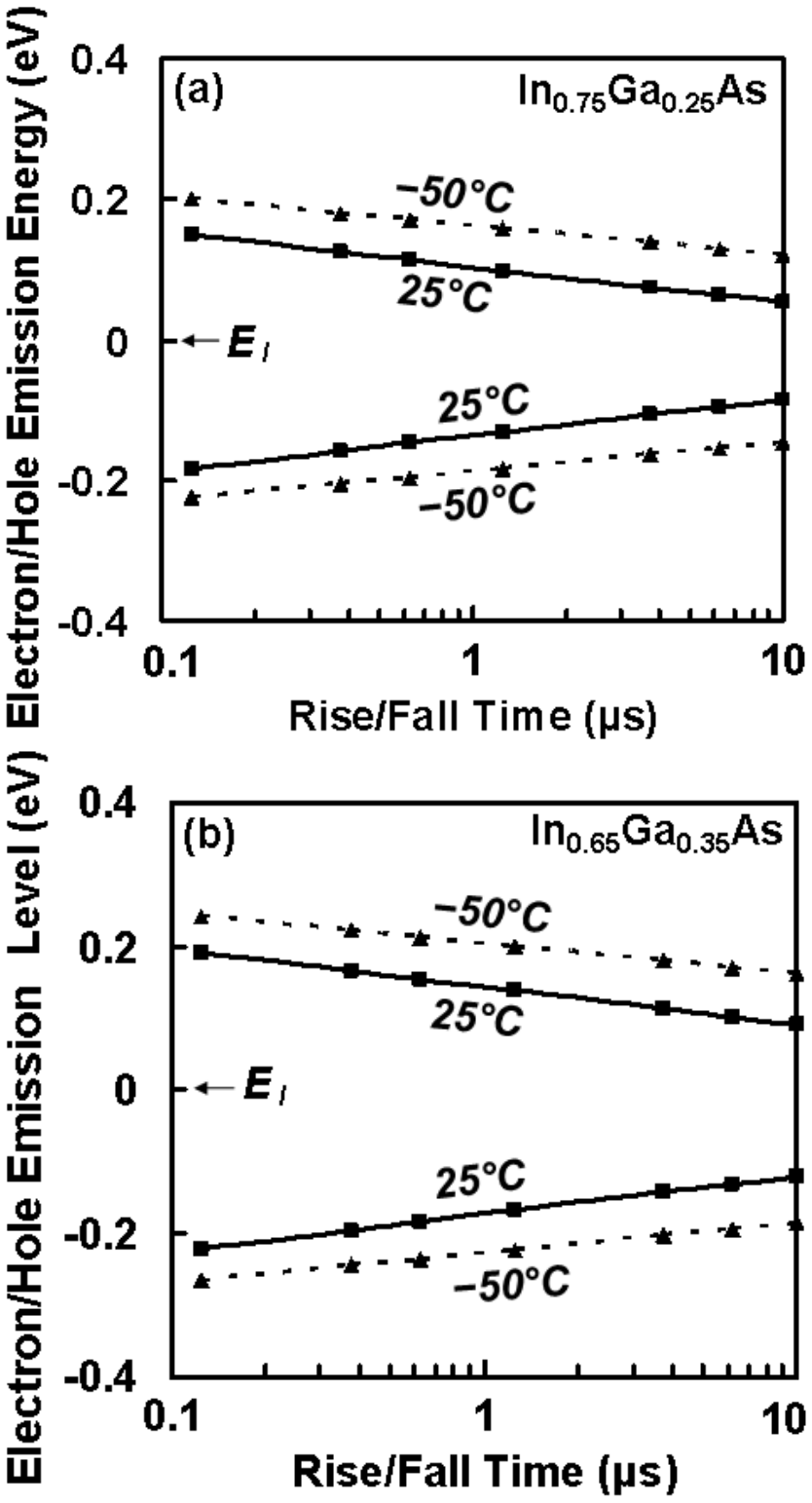
Figure 2.7: Variable-base charge pumping current of (a) (b) 2-μm-gate-length $In_{0.75}Ga_{0.25}As$, (c) (d) 8-μm-gate-length $In_{0.65}Ga_{0.35}As$, and (e) (f) 2-μm-gate-length $In_{0.53}Ga_{0.47}As$ MOSFETs with different (a) (c) (e) t_R and (b) (d) (f) t_F at 25 °C and −50 °C. t_R (t_F) is varied from 0.1 μs, 0.4 μs, 0.6 μs, 1.3 μs, 3.8 μs, 6.3 μs to 12.5 μs (from the top curve to the bottom curve) when t_F (t_R) is fixed at 1.3 μs. f=50 kHz, ΔV_G=2 V, W=200 μm.

located within the electron and hole emission levels defined by t_{R} and t_{F} [14]

$$I_{\mathrm{CP}} = qA_{\mathrm{G}}f \int_{E_{\mathrm{EMH}}}^{E_{\mathrm{EME}}} D_{\mathrm{it}}(E)dE \tag{2.2}$$

where E is the trap energy measured from the intrinsic Fermi-level E_{I}, while E_{EME} and E_{EMH} are calculated electron and hole emission levels. We adopted the emission-level charge pumping theory to calculate E_{EME} and E_{EMH} [10, 15]. The theory is widely used in interpreting charge pumping characteristic of silicon MOSFETs and has been validated for small bandgap semiconductor [9]. Figure 2.8 shows the calculated E_{EME} and E_{EMH} with a transition time range of 0.13 µs to 13 µs at 25 °C and −50 °C for InGaAs MOSFET under test. The basic semiconductor parameters of $\mathrm{In}_x\mathrm{Ga}_{1-x}\mathrm{As}$ in [16] and a trap capture cross section of 10^{-17} cm^{-2} without energy or temperature dependence, are used in the calculation. Fermi-Dirac statistics must be used to calculate band-bending at the surface properly, because the Fermi-level can be within $3k_{\mathrm{B}}T$ of the conduction-band minimum due to the small bandgap of InGaAs. The thermal velocity is defined by $\sqrt{3k_{\mathrm{B}}T/m^*}$, where m^* is the effective mass of the carrier whose capture process is considered. After E_{EME} and E_{EMH} are calculated, the energy distribution of D_{it} is extracted according to Equation (2.2) using measured peak I_{CP} values of Figure 2.7.

Figure 2.9 shows the extracted energy dependence of D_{it} with the trap energy level referred to the conduction band minimum E_{C}. The D_{it} distribution is very similar for different InGaAs channels. It can be seen that D_{it} is 1–3 × 10^{12} cm^{-2}eV^{-1} near E_{C} and peaks at about 3 × 10^{13} cm^{-2}eV^{-1} further down into the bandgap, and follows a Gaussian-like distribution. The majority of interface traps in InGaAs


Electron/Hole Emission Energy (eV)
Electron/Hole Emission Level (eV)
(a)
$In_{0.75}Ga_{0.25}As$
−50°C
25°C
E_I
25°C
−50°C
0.4
0.2
0
-0.2
-0.4
0.1
1
10
Rise/Fall Time (μs)
(b)
$In_{0.65}Ga_{0.35}As$
−50°C
25°C
E_I
25°C
−50°C
0.4
0.2
0
-0.2
-0.4
0.1
1
10
Rise/Fall Time (μs)

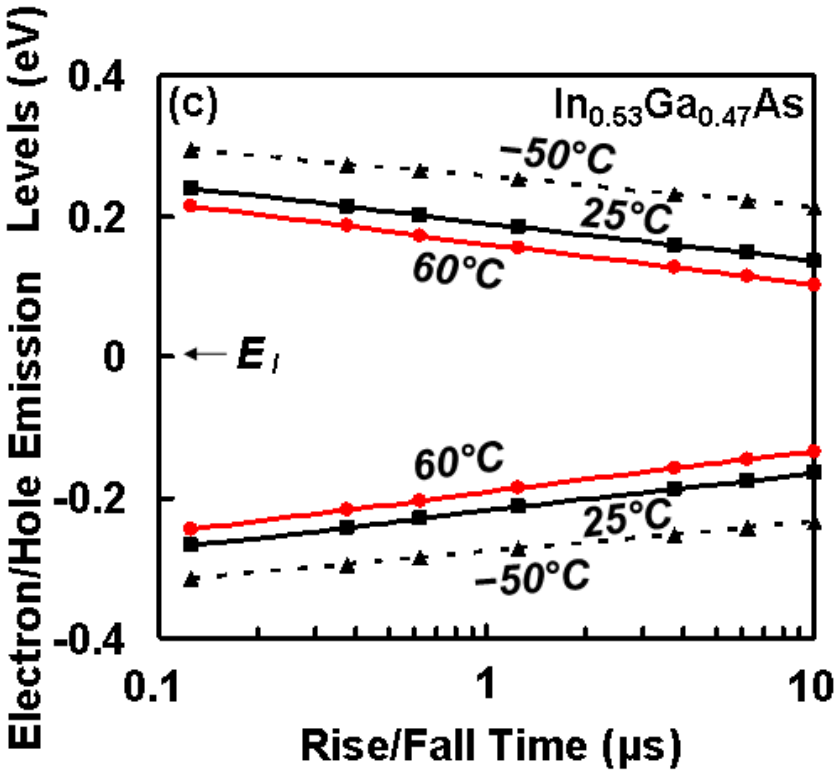


Figure 2.8: Electron and hole emission levels referred to the intrinsic Fermi-level E_{I}, calculated with Fermi-Dirac statistics for (a) $In_{0.75}Ga_{0.25}As$, (b) $In_{0.65}Ga_{0.35}As$, and (c) $In_{0.53}Ga_{0.47}As$ MOSFETs at room temperature (■), −50 °C (▲), and 60 °C (●) ($In_{0.53}Ga_{0.47}As$ only).

MOSFETs have been identified as donors [17]. Figure 2.10 shows a classical calculation of inversion charge density assuming different levels of constant all-acceptor or all-donor D_{it} across the bandgap. It can be seen that the all-acceptor-trap assumption will significantly shift the threshold voltage in the positive direction when D_{it} is increasing, while in the all-donor-trap situation the shift is much less and can better reflect the measured device characteristics. In fact, from various measurement techniques, the charge neutral level E_0 is found to be constant with respect to the vacuum

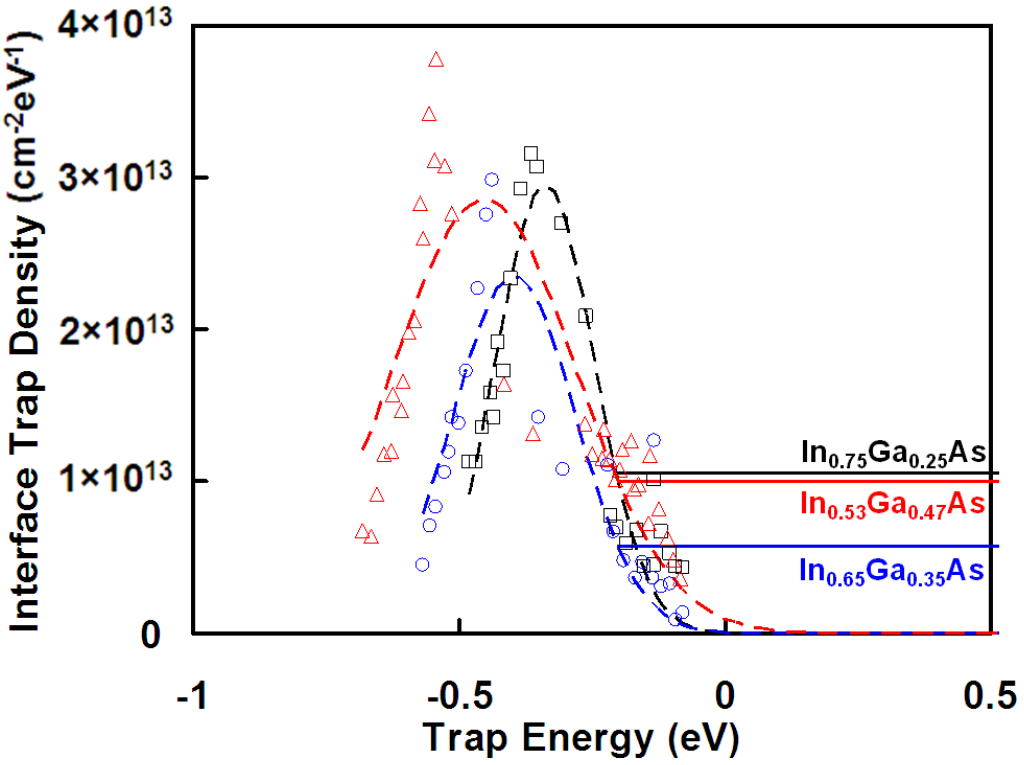


Figure 2.9: Interface trap densities D_{it} in Al_2O_3/$In_{0.75}Ga_{0.25}As$ (□), $In_{0.65}Ga_{0.35}As$ (◯) and $In_{0.53}Ga_{0.47}As$ (△) MOSFETs measured by charge-pumping method across the bandgap. The trap energy is relative to the conduction band minimum E_C. The dashed lines show the Gaussian fit, while the solid lines show the levels fitted with the measured transfer characteristics, which will be discussed in Section 2.2.2.

level [18] and the interface traps are assumed to be donor-like (neutral when filled) below E_0 and acceptor-like (negative when filled) above E_0. Based on this finding, it can be seen that the majority of interface traps are donor-type for indium-rich InGaAs metal-insulator-semiconductor structures. Even though the donor traps are neutralized upon inversion and do not affect the on-state performance of InGaAs

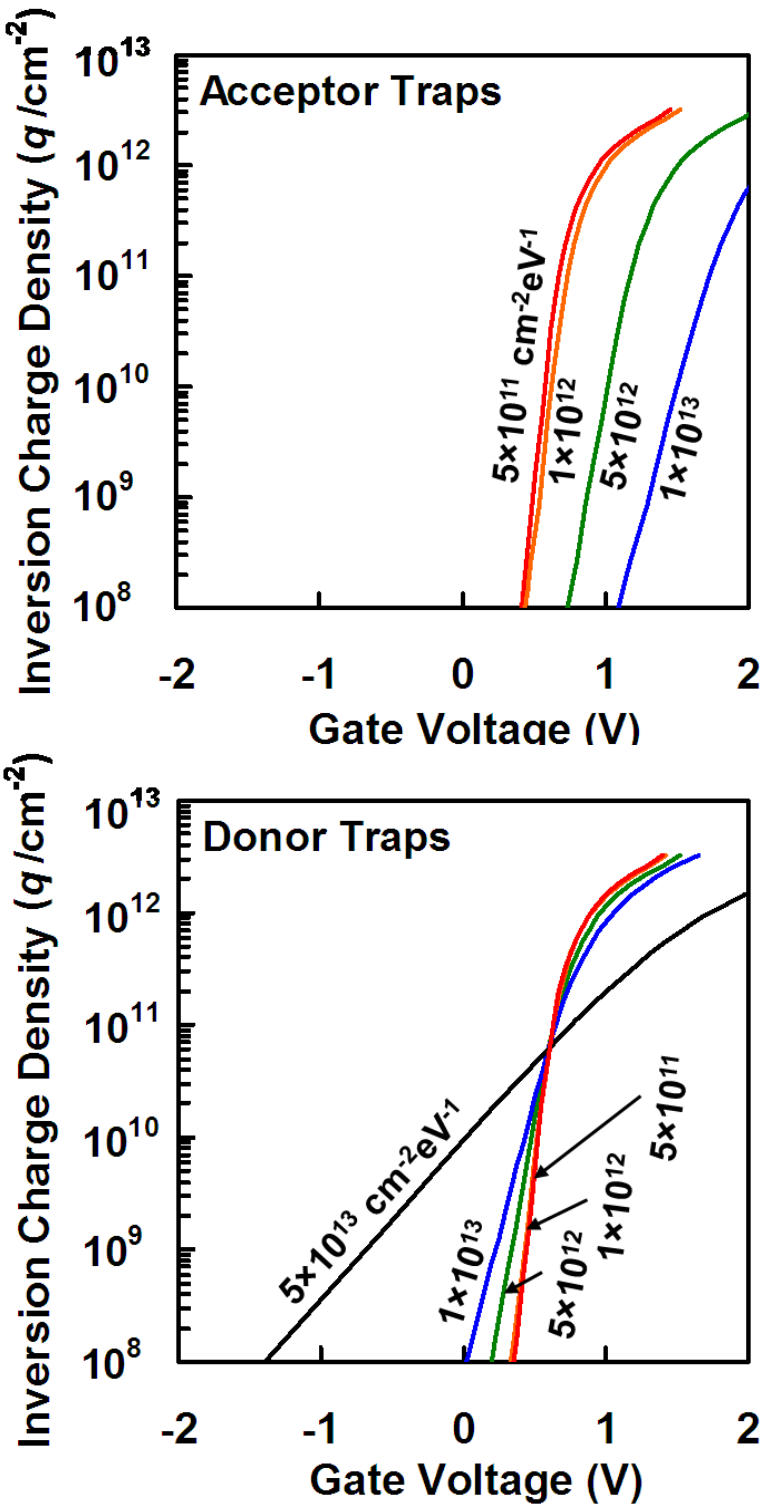


Figure 2.10: Calculated inversion charge density assuming different levels of constant all-acceptor or all-donor D_{it} across the bandgap.

MOSFETs such as threshold voltage and maximum drain current, they limit the off-state performance of InGaAs MOSFETs such as subthreshold slope, drain-induced barrier lowering, and on/off current ratio.

2.2.2 Subthreshold Current

Although charge pumping is a reliable technique to characterize interface traps, the subthreshold current method provides an easier alternative to evaluate D_{it}. It is especially helpful to quickly estimate interface degradation caused by stress.

Subthreshold current method relates the subthreshold swing of a MOSFET to D_{it}. The drain-source current I_{DS} of a MOSFET in subthreshold region is given by [19]

$$I_{\mathrm{DS}} = I_{\mathrm{DS0}} \exp\left[\frac{q\left(V_{\mathrm{GS}} - V_{\mathrm{T}}\right)}{n k_{\mathrm{B}} T}\right]\left[1 - \exp\left(-\frac{q V_{\mathrm{DS}}}{k_{\mathrm{B}} T}\right)\right] \tag{2.3}$$

where I_{DS0} is the scale current which depends on temperature, device dimension and channel doping, n is the ideality factor.

The subthreshold swing, defined by the gate-voltage swing needed to reduce the current by one decade, is

$$S = \frac{\partial V_{\mathrm{GS}}}{\partial \log\left(I_{\mathrm{DS}}\right)} = \frac{\ln(10) n k_{\mathrm{B}} T}{q} \tag{2.4}$$

where $n = 1 + (C_{\mathrm{B}} + C_{\mathrm{it}})/C_{\mathrm{OX}}$, C_{B} is the depletion capacitance, $C_{\mathrm{it}} = q^2 D_{\mathrm{it}}$ is the interface trap capacitance and C_{OX} is the oxide capacitance. D_{it} can be calculated by

$$D_{\mathrm{it}} = \frac{C_{\mathrm{OX}}}{q^2}\left[\frac{qS}{\ln(10) k_{\mathrm{B}} T} - 1\right] - \frac{C_{\mathrm{B}}}{q^2} \tag{2.5}$$

In the InGaAs MOSFETs under study, the carrier quantization effect is considered. Instead of Equation (2.3), the drain-source current is calculated through a quantum mechanical analysis discussed in the next Chapter. The extracted D_{it} is also included in Figure 2.9 for comparison. It agrees well with the charge pumping data.

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Chapter 3

Electron Mobility in InGaAs MOSFETs

Thanks to the relentless shrinking of MOSFET according to the Moore's law, modern integrated circuits based on silicon complementary metal-oxide-semiconductor technology (CMOS) can operate at a much higher speed with a reduced power consumption. As this shrinkage approaches the physical limit of silicon, alternative channel materials such as high-mobility III-V semiconductors have received increasing attention. However, high bulk mobility does not necessarily lead to high surface mobility in an inversion-mode MOSFET. With the recent demonstration of high-performance InGaAs MOSFETs [1–11] and mapping of interface traps across the bandgap of InGaAs [12], their current-voltage characteristics can now be analyzed to determine the difference between surface mobility and bulk mobility. This should complement studies that were based on the capacitance-voltage characteristics of

metal-oxide-semiconductor diodes and generate new insight into the operation of III-V MOSFETs.

3.1 Analysis of Inversion Charge

Despite the high performance of the present InGaAs MOSFETs, their interface trap density is rather high (as will be shown later) and their inversion charge density cannot be measured accurately. Therefore, instead of extracting from the measured current-voltage characteristics the electron mobility as a function of the inversion charge density, we derive the mobility vs. charge density characteristics and reduce them to a few simple parameters to be extracted from the measured current-voltage characteristics as detailed in this chapter.

The electrostatic characteristics of the two-dimensional electron gas in a MOSFET inversion layer can be described by one-dimensional Schrödinger and Poisson equations

$$-\frac{\hbar^2}{2m^*}\frac{d^2\psi_i(z)}{dz^2} + qV(z)\psi_i(z) = E_i\psi_i(z) \tag{3.1}$$

$$\frac{d^2V(z)}{dz^2} = \frac{q}{\epsilon_S}\left[N_A - N_D + n(z) - p(z)\right] \tag{3.2}$$

where $\psi_i(z)$ is the normalized wave function of an electron in the i-th subband, m^* is the effective mass for the electron motion in the z direction perpendicular to the oxide-semiconductor interface, $\hbar$ is the reduced Plank's constant, E_i is the energy level of the i-th subband, q is the electron charge, $V(z)$ is the electrostatic potential, ϵ_S is the semiconductor permittivity, N_A and N_D are the ionized acceptor and

donor concentrations, and $n(z)$ and $p(z)$ are the electron and hole concentrations, respectively. Since we are only dealing with p-type substrate, N_{D} will be omitted in all the following analysis. Equations (3.1) and (3.2) can be solved individually but consistently by assuming the electric field to be constant or the potential well to be triangular near the interface [13].

Under the triangular well approximation, $V(z)$ in Equation (3.1) is replaced by $\xi_{\mathrm{S}} \cdot z$, where ξ_{S} is the surface electric field. Now the differential equation has solutions in the form of an Airy function $\mathrm{Ai}(x)$ defined by

$$\mathrm{Ai}(x) = \frac{1}{\pi} \int_0^\infty \cos\left(\frac{t^3}{3} + xt\right) dt \tag{3.3}$$

The solution of Equation (3.1) is

$$\psi_i(z) = C_{\mathrm{N}} \mathrm{Ai}\left[\left(\frac{2m^* q\xi_{\mathrm{S}}}{\hbar^2}\right)^{1/3} \left(z - \frac{E_i}{q\xi_{\mathrm{S}}}\right)\right] \tag{3.4}$$

where C_{N} is the normalization constant obtained by

$$\int_0^\infty |\psi_i(z)|^2 \, dz = 1 \tag{3.5}$$

and then

$$C_{\mathrm{N}} = \sqrt{\frac{\left(2m^* q\xi_{\mathrm{S}}/\hbar^2\right)^{1/3}}{\mathrm{Ai}'^2\left[\lambda(0)\right] - \lambda(0)\mathrm{Ai}^2\left[\lambda(0)\right]}} \tag{3.6}$$

where $\mathrm{Ai}'(x)$ is the derivative of Airy function with respect to x

$$\mathrm{Ai}'(x) = \frac{d\mathrm{Ai}(x)}{dx} \quad \text{and} \quad \lambda(z) = \left(\frac{2m^* q\xi_{\mathrm{S}}}{\hbar^2}\right)^{1/3} \left(z - \frac{E_i}{q\xi_{\mathrm{S}}}\right)$$

The energy eigenvalues E_i can be obtained by satisfying the boundary condition at $z = 0$: $\psi_i(0) = 0$, which leads to

$$E_i = \left(\frac{\hbar^2}{2m^*}\right)^{1/3} \left[\frac{3}{2}\pi q\xi_{\mathrm{S}} \left(i - \frac{1}{4}\right)\right]^{2/3} \qquad i = 1, 2, 3, \cdots \tag{3.7}$$

The electron density in the i-th subband N_i can be expressed by

$$N_i = \frac{n_{\mathrm{v}} m^* k_{\mathrm{B}} T}{\pi \hbar^2} \ln\left[1 + \exp\left(\frac{E_{\mathrm{F}} - E_i}{k_{\mathrm{B}} T}\right)\right] \tag{3.8}$$

where the Fermi-level E_{F} can be related to the surface potential ψ_{S} — the potential on the semiconductor surface with respect to that in the semiconductor bulk — by

$$E_{\mathrm{F}} = q\psi_{\mathrm{S}} - (E_{\mathrm{G}} + E_{\mathrm{VB}} - E_{\mathrm{F}}) \tag{3.9}$$

where E_{G} is the bandgap energy and E_{VB} is the valence band maximum in the bulk of the semiconductor. Due to the small electron effective mass or low density of states of the conduction band of InGaAs, $E_{\mathrm{VB}} - E_{\mathrm{F}}$ should be evaluated with Fermi-Dirac statistics or at least approximations of the Fermi-Dirac integral such as the Joyce-Dixon approximation

$$\begin{aligned}\frac{E_{\mathrm{VB}} - E_{\mathrm{F}}}{k_{\mathrm{B}} T} = \ln\left(\frac{N_{\mathrm{A}}}{N_{\mathrm{V}}}\right) + \frac{1}{\sqrt{8}}\left(\frac{N_{\mathrm{A}}}{N_{\mathrm{V}}}\right) - 4.95009 \times 10^{-3}\left(\frac{N_{\mathrm{A}}}{N_{\mathrm{V}}}\right)^2 \\ +1.48386 \times 10^{-4}\left(\frac{N_{\mathrm{A}}}{N_{\mathrm{V}}}\right)^3 - 4.42563 \times 10^{-4}\left(\frac{N_{\mathrm{A}}}{N_{\mathrm{V}}}\right)^4\end{aligned} \tag{3.10}$$

The total inversion charge density Q_{N} in the quantum well is just the summation of electrons in all subbands

$$Q_{\mathrm{N}} = -qN_{\mathrm{N}} = -q\sum_i N_i \tag{3.11}$$

The bulk depletion charge density Q_{B} is calculated by [14]

$$Q_{\mathrm{B}} = -qN_{\mathrm{B}} = -\sqrt{2q\epsilon_{\mathrm{S}}\psi_{\mathrm{D}}N_{\mathrm{A}}} \tag{3.12}$$

where the effective band-bending ψ_{D} is

$$\psi_{\mathrm{D}} = \psi_{\mathrm{S}} - \frac{k_{\mathrm{B}} T}{q} - \frac{qN_{\mathrm{N}} z_{\mathrm{avg}}}{\epsilon_{\mathrm{S}}} \tag{3.13}$$

z_{avg}, the average separation of inversion charge away from the semiconductor surface, is

$$z_{\text{avg}} = \sum_i N_i z_i / N_{\text{N}} \quad \text{and} \quad z_i = \frac{2E_i}{3q\xi_{\text{S}}} \tag{3.14}$$

Then the surface electric field can be calculated from inversion and depletion charge

$$\xi_{\text{S}} = q\left(N_{\text{N}} + N_{\text{B}}\right)/\epsilon_{\text{S}} \tag{3.15}$$

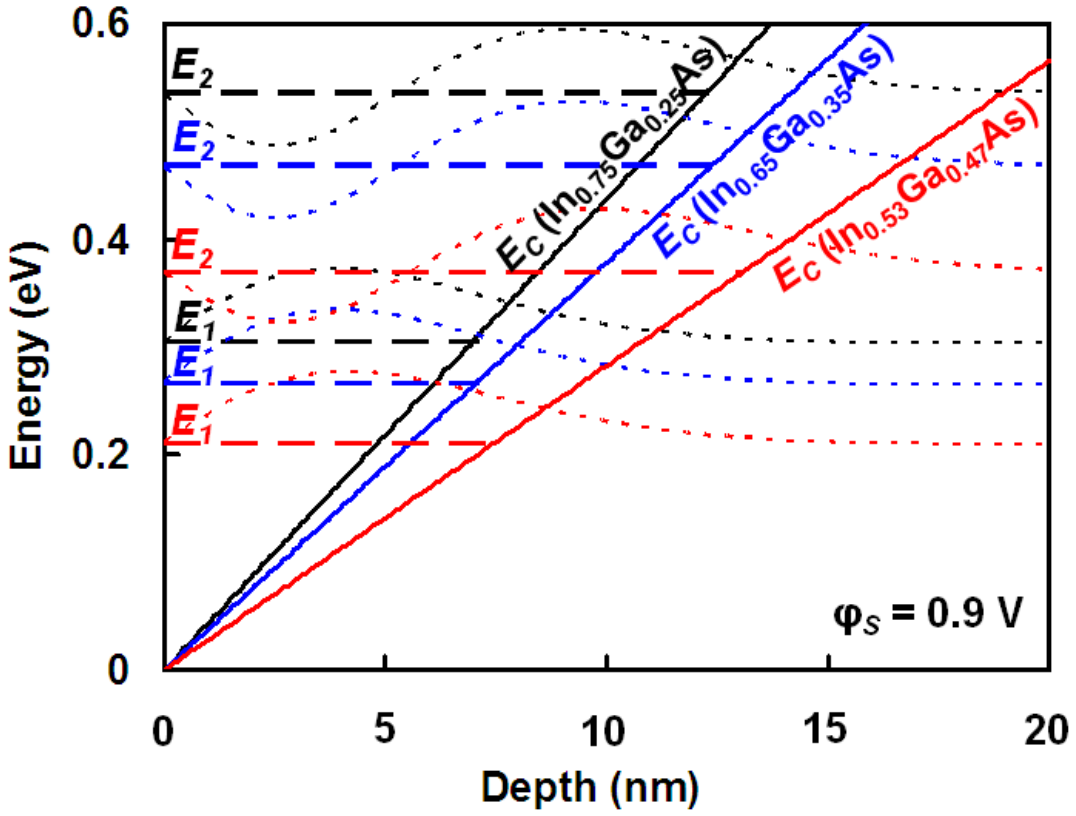


Figure 3.1: Lowest two subbands (E_1 and E_2) and wave functions for InGaAs MOSFETs under strong inversion with surface potential $\psi_{\text{S}} = 0.9\ V$.

By solving Equation (3.7) to (3.15) iteratively, a consistent solution of inversion charge density at a certain surface potential or Fermi-level can be obtained. For

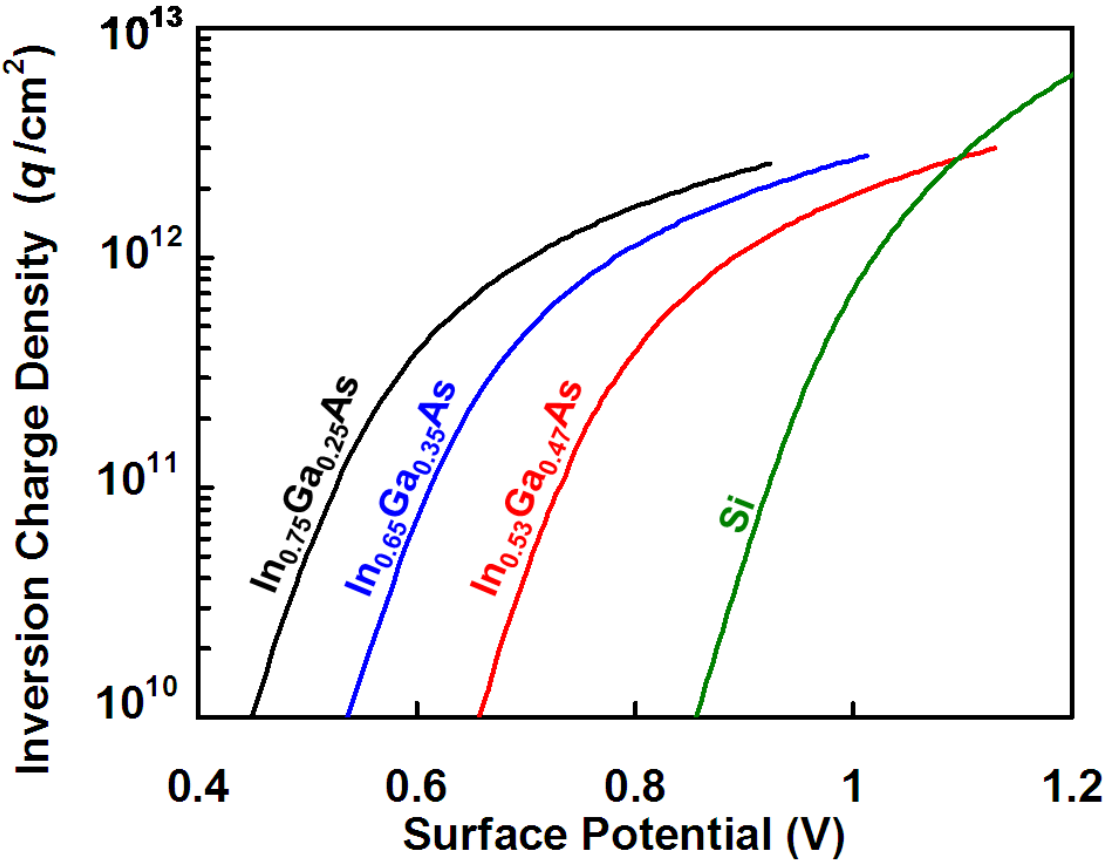


Figure 3.2: Calculated inversion charge densities Q_N are lower for InGaAs MOSFETs than that for a silicon MOSFET due to lower density of states in InGaAs.

the present InGaAs MOSFETs, Figure 3.1 shows the lowest two subbands, E_1 and E_2, and their associated wave functions in the Γ valley under strong inversion, while Figure 3.2 shows the inversion charge density Q_N as a function of the surface potential ψ_S. (In the range of inversion charge density explored in this work, the occupation of satellite valleys is negligible [15].) For comparison, a silicon MOSFET with $N_A = 1 \times 10^{17}$ cm^{-3} and a 10-nm Al_2O_3 gate oxide is also included. It can be seen that in strong inversion, the silicon MOSFET has a higher charge density than

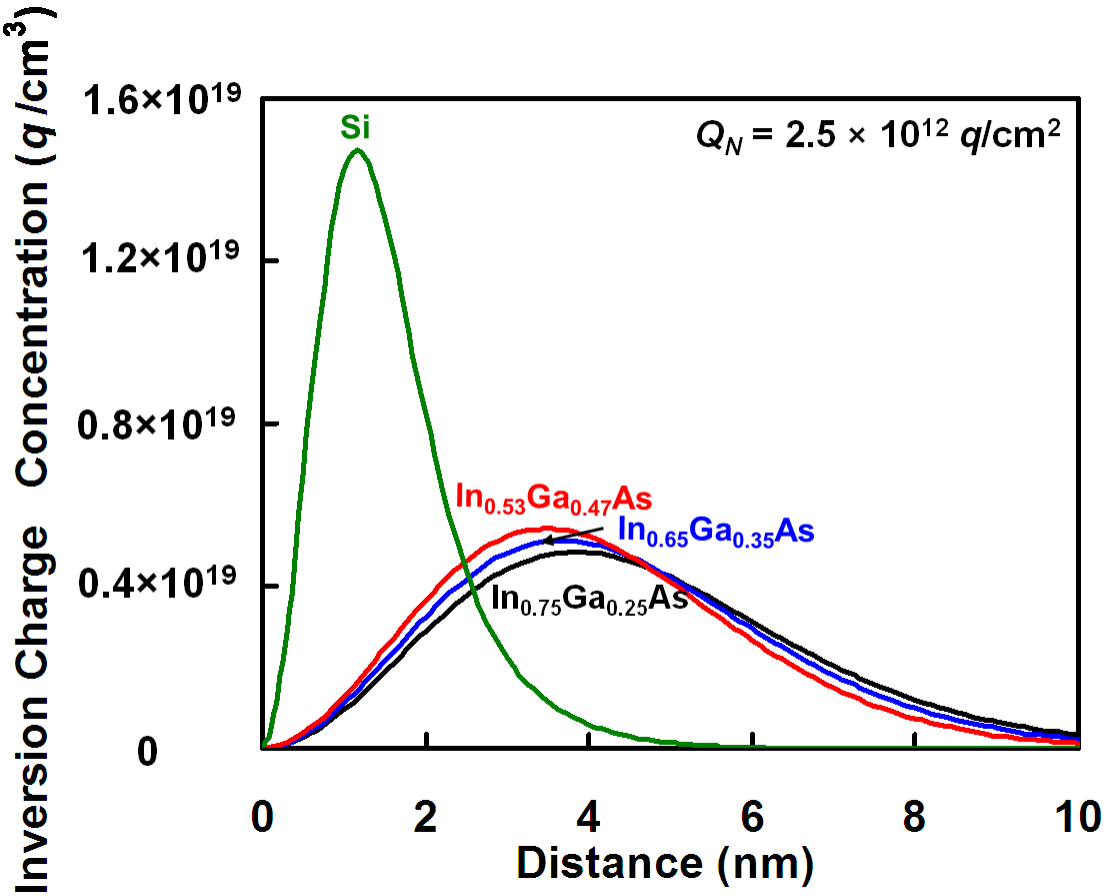


Figure 3.3: The inversion charge distribution in the channel for silicon and InGaAs MOSFETs at a $Q_{\mathrm{N}} = 2.5 \times 10^{12}\ q/\mathrm{cm}^2$.

the InGaAs MOSFETs mainly due to a higher density of states in the conduction band. Figure 3.3 compares the inversion charge distribution in the channel for silicon and InGaAs MOSFETs at the same inversion charge density. With a much larger effective mass, the $(2m^* q\epsilon_{\mathrm{S}}/\hbar^2)^{1/3}$ term in Equation (3.4) for silicon MOSFET is much larger than that for InGaAs MOSFETs. As a result, the wave functions in silicon MOSFET are confined much closer to the semiconductor-oxide interface. As

shown in Figure 3.3, the centroid of inversion charges is much closer to the oxide-semiconductor interface in silicon MOSFET than that in InGaAs MOSFETs. Table 3.1 lists the parameters used in the calculation [16].

Channel	Si	$In_{0.53}Ga_{0.47}As$	$In_{0.65}Ga_{0.35}As$	$In_{0.75}Ga_{0.25}As$
φ_M (V)			5.1	
k_{OX}			9.0	
C_{OX} (F/cm^2)	0.8×10^{-6}	1.0×10^{-6}	0.8×10^{-6}	
k_S	11.7	13.9	14.2	14.4
m^* ($m_0^{a)}$)	$m_T^{b)} = 0.19$	0.041	0.036	0.032
	$m_L^{c)} = 0.98$			
χ (V)	4.05	4.51	4.61	4.69
E_G (eV)	1.12	0.74	0.62	0.53
$E_0 - E_C$ (eV)	-0.50	-0.24	-0.12	-0.04
$E_F - E_{CB}$ (eV)	-0.99	-0.63	-0.51	-0.42
Q_t (q/cm^2)	—	7.4×10^{12}	5.0×10^{12}	7.7×10^{12}
φ_{MS} (V)	0.06	-0.04	-0.02	-0.02
R_{DS} (Ω)	—	14	29	19
μ_0 (cm^{2}V^{-1}s^{-1})	8.0×10^2	1.3×10^3	1.1×10^4	1.3×10^4
λ/Δ^2 (nm^{-1})	4–63	0.2	0.6	0.7
$\overline{D_{it}}$ (cm^{-2}eV^{-1})	4.0×10^{11}	1.0×10^{13}	5.7×10^{12}	1.1×10^{13}

[a)]electron rest mass [b)]electron transverse mass [c)]electron longitudinal mass

Table 3.1: Model parameters.

The gate-source voltage V_{GS} is related to ψ_S by

$$V_{GS} = \varphi_{MS} + \varphi_S - (Q_B + Q_N + Q_{it} + Q_t)/C_{OX} \tag{3.16}$$

where φ_{MS} is the difference between the gate metal work function and the semiconductor work function, Q_{it} is the interface charge density, Q_t is the bulk oxide charge density assumed to be concentrated near the oxide-semiconductor interface, and C_{OX} is the oxide capacitance. Q_B and Q_N are obtained by solving solving Equation

(3.7) to (3.15).

To evaluate V_{GS} according to Equation (3.16), the metal-semiconductor work function difference was calculated by

$$\varphi_{\mathrm{MS}} = \varphi_{\mathrm{M}} - \chi - (E_{\mathrm{CB}} - E_{\mathrm{F}}) \tag{3.17}$$

where φ_{M} is the metal work function, χ is the electron affinity, and E_{CB} is the conduction band minimum in the bulk of the semiconductor. These parameter values were included in Table 3.1.

To calculate the interface charge density Q_{it}, interface trap density D_{it} and charge neutral level E_0 [17] are needed. Figure 2.9 shows the interface trap density between Al_2O_3 and InGaAs across the bandgap as measured by using the charge-pumping method [12]. It can be seen that in general the trap density follows a Gaussian distribution with a peak midgap. Since the trap distribution into the conduction band cannot be directly measured, extrapolation is necessary. However, if the extrapolation follows the Gaussian distribution, very few traps will be in the conduction band and the sub-threshold slope of the transfer characteristics will be much steeper than what is measured. For lack of better understanding, the trap density in the conduction band is assumed to be constant ($\overline{D_{\mathrm{it}}}$) and the same as D_{it} at E_0 as indicated by the solid lines in Figure 2.9. Such a $\overline{D_{\mathrm{it}}}$ fits well with the measured transfer characteristics as will be shown in Section 3.3.

Following [17], the charge neutral level E_0 is assumed to be constant with respect to the vacuum level and the interface traps are assumed to be donor-like (neutral when filled) below E_0 and acceptor-like (negative when filled) above E_0. Figure 3.4

shows the calculated interface charge density $Q_{\rm it}$ according to

$$Q_{\rm it} = -q \int_{E_0}^{E_{\rm F}} D_{\rm it}(E) dE \tag{3.18}$$

where $E_{\rm F}$ is the surface Fermi-level. The agreement with the experimental data is good.

The fixed oxide charge density $Q_{\rm t}$ is obtained by fitting the transfer characteristics as discussed in Section 3.3. $Q_{\rm t}$ mainly shifts the current-voltage characteristics along the voltage axis, while $Q_{\rm it}$ changes their slopes, too.

3.2 Analysis of Electron Mobility

In addition to the inversion charge, low-field electron mobility $\mu_{\rm N}$ is another important parameter critical to the transfer characteristics of n-channel MOSFET. Consider the different scattering mechanisms that limit electron mobility, it can be expressed as [18]

$$\frac{1}{\mu_{\rm N}} = \frac{1}{\mu_0} + \frac{1}{\mu_{\rm R}} + \frac{1}{\mu_{\rm C}} \tag{3.19}$$

where μ_0 is the semiconductor bulk mobility accounting for the scattering of bulk and remote phonons as well as ionized impurities without considering the screening by the inversion charge, $\mu_{\rm R}$ is the interface roughness mobility, and $\mu_{\rm C}$ is the Coulomb scattering mobility due to the oxide charge $Q_{\rm t}$ and the interface charge $Q_{\rm it}$.

The InGaAs bulk mobility has been measured in uniform slabs [19] and only needs to be fine-tuned to fit the subthreshold characteristics of the present InGaAs MOSFETs.

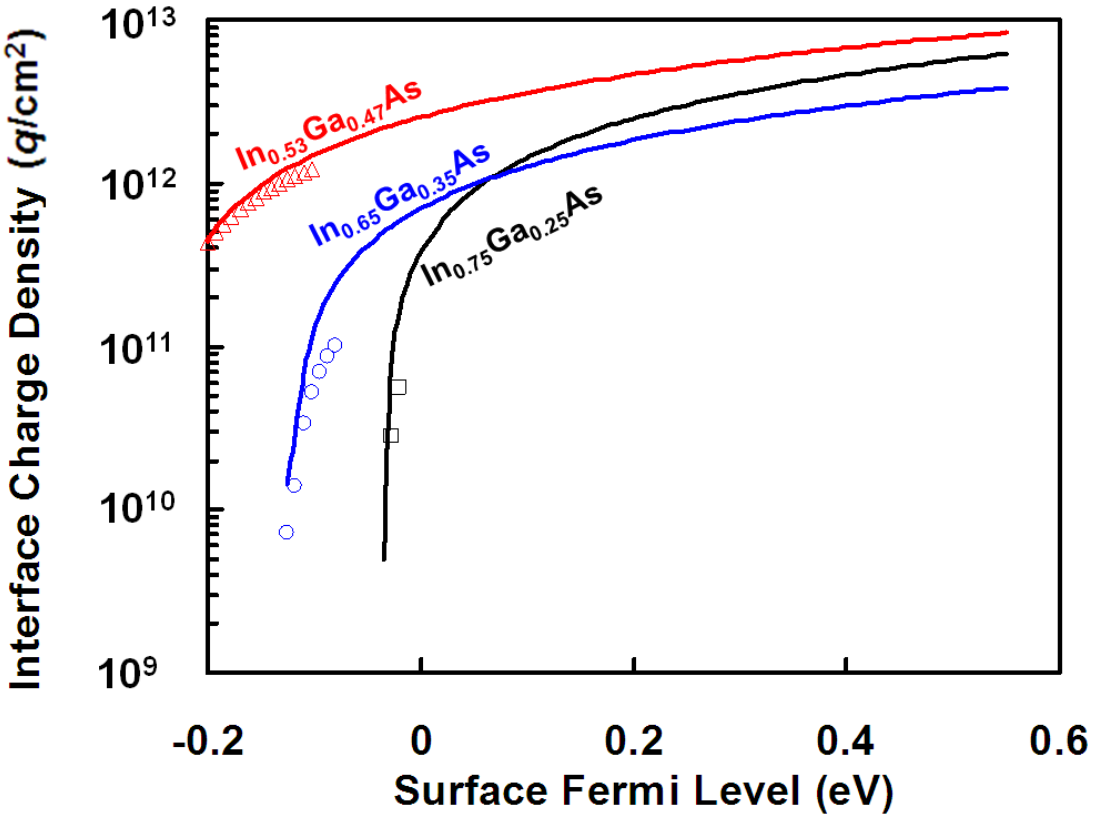


Figure 3.4: Measured (symbols) vs. calculated (curves) interface charge densities $Q_{\rm it}$ for $In_{0.75}Ga_{0.25}As$ (□), $In_{0.65}Ga_{0.35}As$ (◯) and $In_{0.53}Ga_{0.47}As$ (△).

In comparison, the interface roughness mobility needs to be derived by calculating the matrix element of the scattering potential before converting to the scattering rate or relaxation time through the Fermi golden rule. The perturbation potentials for interface roughness scattering $V_{\rm R}$ [20] and Coulomb scattering $V_{\rm C}$ [21] are

$$V_{\rm R} = \frac{1}{4\pi\bar{\epsilon}} \sum_i \frac{\Delta Q_i}{|\vec{r} - \vec{r_i}|} \tag{3.20}$$

and

$$V_{\rm C} = qE(z)\Delta(x, y) \tag{3.21}$$

respectively, where ΔQ_i is the charge of the scattering center, $\bar{\epsilon}$ is the average permittivity, $\vec{r}$ is the position of electron in the inversion layer, $\vec{r_i}$ is the position of the scattering center, $E(z)$ is the electric field, and $\Delta(x, y)$ is the interface roughness, which is assumed to be Gaussian.

Thus, the interface roughness mobility can be expressed as [21]

$$\mu_{\mathrm{R}} = \frac{9\sqrt{\pi}\hbar}{4m^* E_{\mathrm{eff}}} \frac{\lambda}{\Delta^2} \tag{3.22}$$

where λ is the correlation length and Δ is the root-mean-square average height of the assumed Gaussian distribution of the interface roughness, and E_{eff} is the effective electric field at the interface according to

$$E_{\mathrm{eff}} = \frac{|Q_{\mathrm{B}} + Q_{\mathrm{N}}/2|}{\epsilon_{\mathrm{S}}} \tag{3.23}$$

Since Q_{B} and Q_{N} can be calculated as shown in Section 3.1, so that E_{eff} is known and λ/Δ^2 is the only fitting parameter for μ_{R}.

Coulomb scattering can be due to both the fixed oxide charge Q_{t} and the oxide-semiconductor interface charge Q_{it}. The Coulomb scattering mobility with screening by the inversion charge for i-th subband can be expressed as [18]

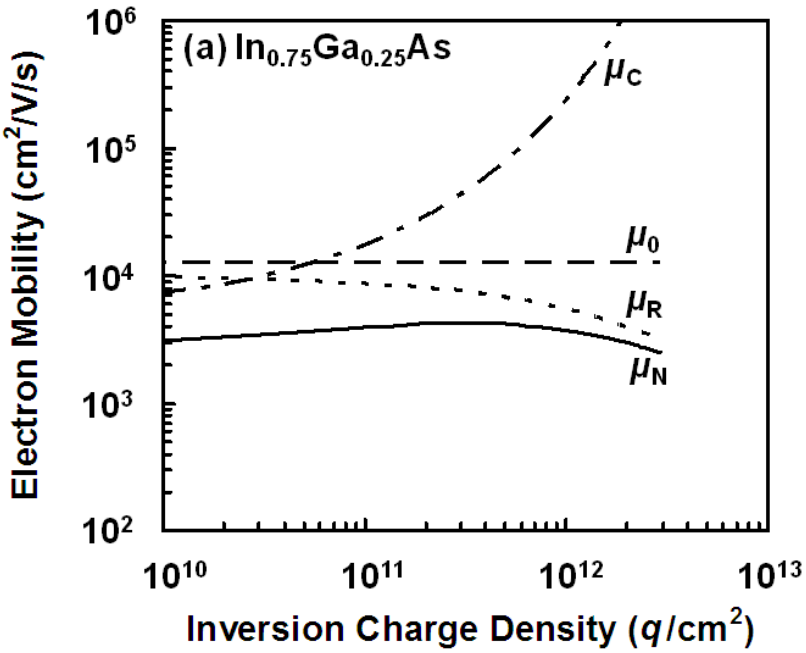
$$\mu_{\mathrm{C}}(E_i) = \frac{8\pi\hbar E_i \left(\bar{\epsilon}/q\right)^2}{m^* \left|Q_{\mathrm{t}} + Q_{\mathrm{it}}\right| \int_0^{\pi/2} \left(1 + a\sqrt{\eta_i}\bar{z}\sin\varphi\right)^{-6} \left(1 + \frac{q|Q_{\mathrm{N}}|}{6k_{\mathrm{B}}T\bar{\epsilon}a\sqrt{\eta_i}\bar{z}\sin\varphi}\right)^{-2} d\varphi} \tag{3.24}$$

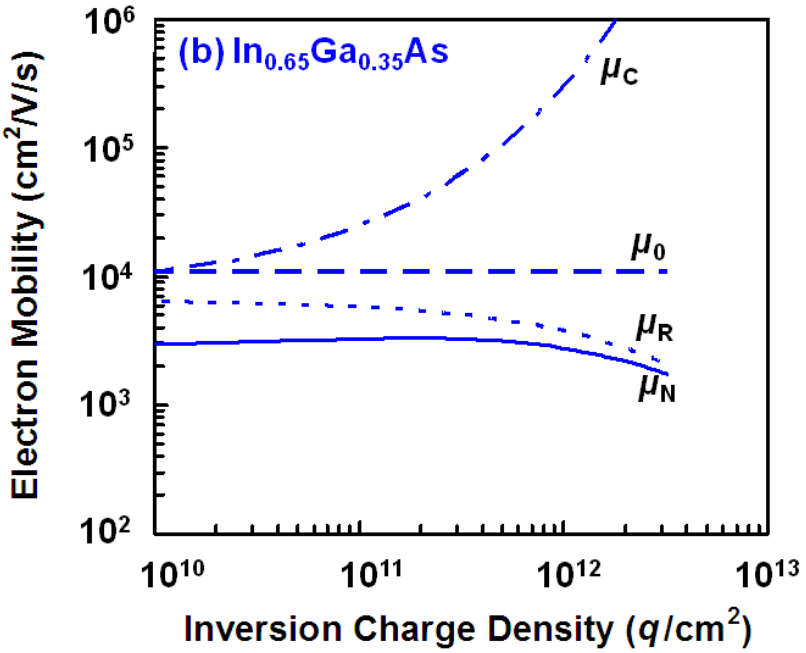
where

$$\bar{\epsilon} = \frac{\epsilon_{\mathrm{OX}} + \epsilon_{\mathrm{S}}}{2}, \quad \eta_i = \frac{E_i}{k_{\mathrm{B}}T}, \quad \bar{z} = 3\left[\frac{12qm^*}{\hbar^2\epsilon_{\mathrm{S}}}\left|Q_{\mathrm{B}} + \frac{11}{32}Q_{\mathrm{N}}\right|\right]^{-1/3}, \quad a = \frac{2\sqrt{2m^* k_{\mathrm{B}}T}}{3\hbar}$$

and k_{B} is Boltzmann's constant. Therefore, according to [18]

$$\mu_{\mathrm{C}} = \frac{\sum_i \mu_{\mathrm{C}}\left(E_i\right) D\left(E_i\right) f\left(E_i\right) E_i}{\sum_i D\left(E_i\right) f\left(E_i\right) E_i} \tag{3.25}$$


(a) In0.75Ga0.25As
μC
μ0
μR
μN
Electron Mobility (cm2/V/s)
Inversion Charge Density (q/cm2)
10^6
10^5
10^4
10^3
10^2
10^10
10^11
10^12
10^13


(b) In0.65Ga0.35As
μC
μ0
μR
μN
Electron Mobility (cm2/V/s)
Inversion Charge Density (q/cm2)
10^6
10^5
10^4
10^3
10^2
10^10
10^11
10^12
10^13

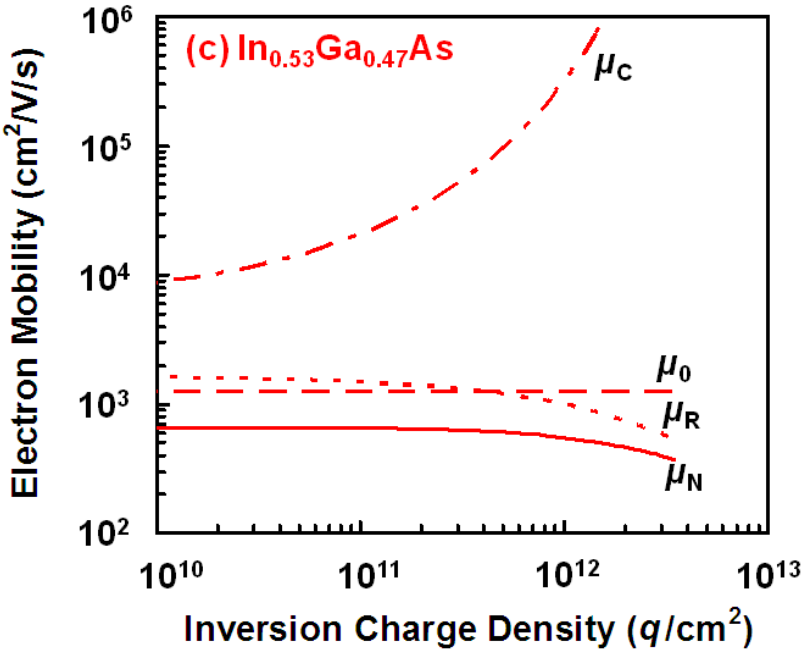


Figure 3.5: Calculated semiconductor bulk mobility μ_0 (– – –), interface roughness mobility μ_R (- - -), Coulomb scattering mobility μ_C (– · –), and total electron mobility μ_N (——) for (a) $In_{0.75}Ga_{0.25}As$ (b) $In_{0.65}Ga_{0.35}As$ and (c) $In_{0.53}Ga_{0.47}As$ MOSFETs at room temperature. In all cases, μ_N is mainly limited by μ_R under strong inversion.

where $D(E_i)$ is the density of states in the semiconductor and $f(E_i)$ is the Fermi-Dirac distribution function. Despite the high interface charge density, the Coulomb scattering mobility in the present InGaAs MOSFETs is calculated to be on the order of 10^4 cm^2/V/s or even higher and, hence, can only affect the total electron mobility in weak inversion. This is probably because in the present InGaAs MOSFETs the inverted electrons are farther away from the oxide than those in a silicon MOSFET as shown in Figure 3.3. Also, in strong inversion, the Coulomb scattering is screened by the inversion charge.

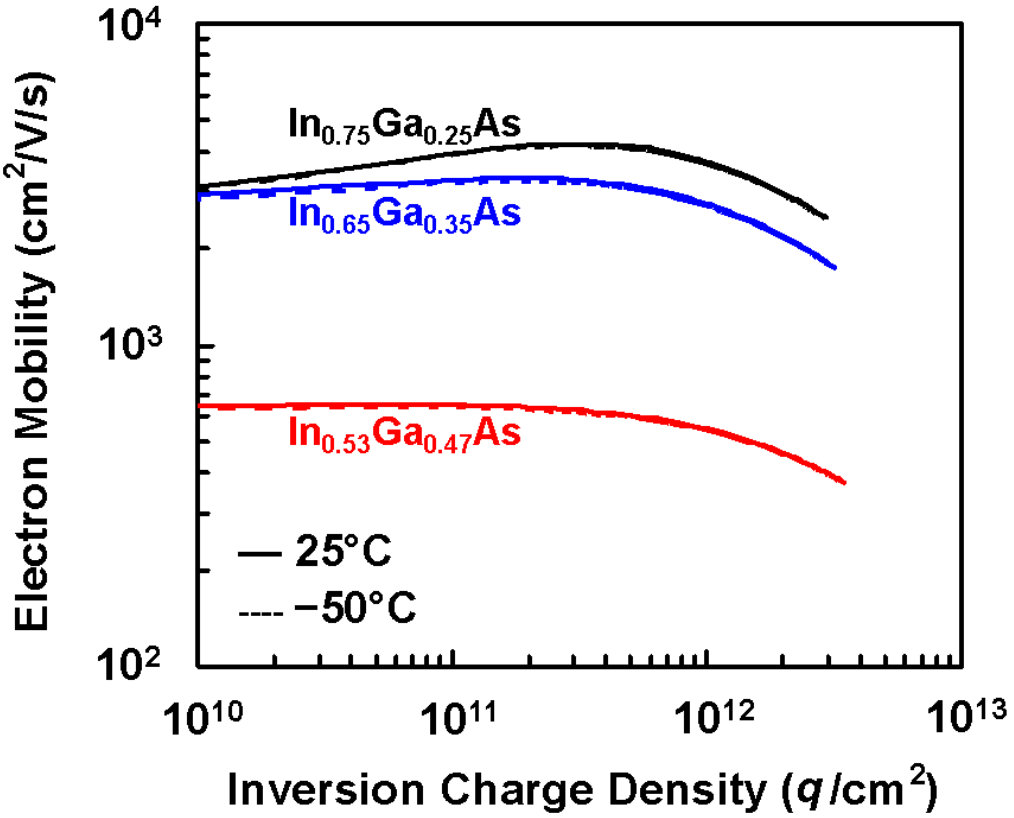


Figure 3.6: Total electron mobility μ_N in InGaAs MOSFETs calculated by using the parameter values listed in Table 3.1, which exhibits little difference between room temperature (——) and −50 °C (- -).

As a summary of the above-described mobility analysis, Figure 3.5 shows the calculated μ_0, μ_R, μ_C and μ_N for the present InGaAs MOSFETs at room temperature. It can be seen that in strong inversion the total electron mobility decreases with increasing inversion charge and is mainly limited by the interface roughness mobility, as the bulk mobility is rather high in the present InGaAs MOSFETs with $L = 4$ μm and $N_A = 1 \times 10^{17}$ cm^{-3}. Even with order-of-magnitude scaling of gate length and doping concentration, the bulk mobility will still be high enough so that

under strong inversion the total mobility will be mainly limited by interface roughness, unless the interface roughness is improved significantly. By contrast, with higher channel doping and generally lower bulk mobility, the total electron mobility in typical silicon MOSFETs is limited by the bulk mobility.

As the interface roughness mobility is not sensitive to temperature, the total electron mobility of the InGaAs MOSFETs exhibits negligible temperature dependence as shown in Figure 3.6. Such temperature insensibility agrees with the experiment data of $In_{0.53}Ga_{0.47}As$ MOSFETs over a much wider temperature range [22]. This confirms that in the present cases, phonon scattering plays a minor role in determining the electron mobility, especially when remote phonons the screening of remote phonons by the metal gate [23–25].

For compact modeling, the total electron mobility of the present InGaAs MOSFETs in moderate-to-strong inversion can be simply fitted to a power law $E_{\text{eff}}^{-0.7}$ as shown in Figure 3.7. Although it is interesting to extrapolate the power law to 1 MV/cm under which most modern Si MOSFETs operate, it may not be valid because under such a high field, the electron wave function will move closer to the semiconductor surface and even penetrate into the oxide to degrade the electron mobility faster than what the power-law predicts. Unfortunately, the present InGaAs MOSFETs cannot be biased to higher gate voltages than that shown in Figure 3.8. For comparison, the Si universal mobility [26] has also been included in Figure 3.7.

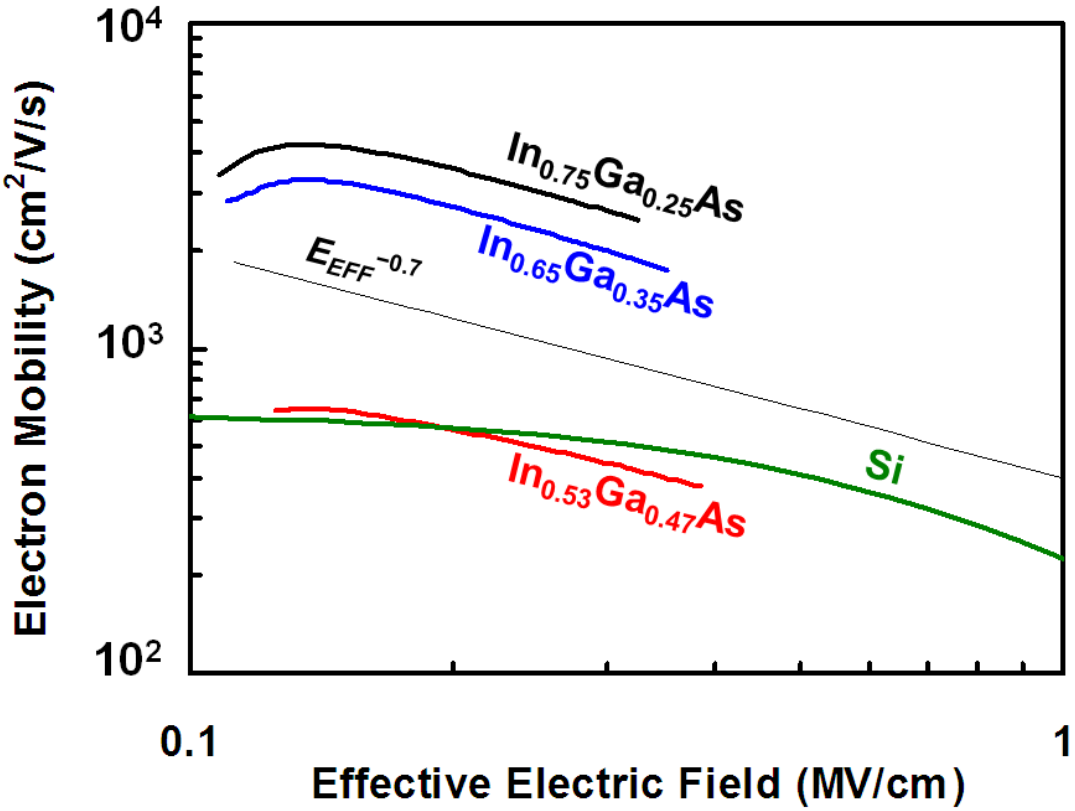


Figure 3.7: Total electron mobility μ_{N} in InGaAs MOSFETs calculated by using the parameter values listed in Table 3.1, which exhibits simple power-law dependence on the effective electric E_{eff} field. The Si universal mobility [26] has also been included for comparison.

3.3 Experiments and Discussions

The transfer characteristics can be modeled by

$$I_{\mathrm{DS}}\left(V_{\mathrm{GS}}\right)=\left[R_{\mathrm{DS}}+\frac{1}{\frac{W}{L}\mu_{\mathrm{N}}\left(V_{\mathrm{GS}}\right)Q_{\mathrm{N}}\left(V_{\mathrm{GS}}\right)}\right]^{-1}V_{\mathrm{DS}} \tag{3.26}$$

where I_{DS} is the drain-source current, and R_{DS} is the drain-source series parasitic resistance. The values of R_{DS} were extracted from measured transfer characteristics

of devices with different gate lengths and then optimized to give the best overall fit. Q_{N} and μ_{N} have been calculated in Section 3.1 and Section 3.2, respectively, with μ_0 and λ/Δ^2 as fitting parameters. The optimized values were listed in Table 3.1. Except for the extraction of source-drain parasitic resistance, current-voltage transfer characteristics were measured under a drain-source voltage V_{DS} of 50 mV on MOSFETs with a gate length L of 4 μm and a gate width W of 100 μm. The low drain-source voltage ensured linear characteristics; the long gate length minimized short-channel effects. Several MOSFETs of the same In mole fraction were measured and the typical characteristics are shown in Figure 3.8. Figure 3.8 also compares in both linear and logarithmic scales the modeled and measured transfer characteristics of the present InGaAs MOSFETs at room temperature and −50 °C. Excellent agreement was achieved from subthreshold to strong inversion.

Table 3.1 shows that the extracted interface roughness parameter λ/Δ^2 for the present InGaAs MOSFETs is significantly smaller than that of the silicon MOSFET, suggesting that the Al_2O_3/InGaAs interface is rougher than the SiO_2/Si interface. The interface roughness of silicon MOSFETs have been characterized through measurements of carrier mobility [20, 27, 28], atomic force microscopy [29], high-resolution transmission electron microscopy [30], and X-ray reflectivity [31]. For the SiO_2/Si interface, λ = 0.6–2.5 nm and Δ = 0.2–0.5 nm. For the interface between high-κ dielectric and Si, λ is usually assumed to be the same, but Δ is slightly larger at 0.3–0.6 nm. Assuming λ is the same for the Al_2O_3/InGaAs interface, too, the extracted λ/Δ^2 implies that Δ = 1.2–2.2 nm, which is approximately two to seven

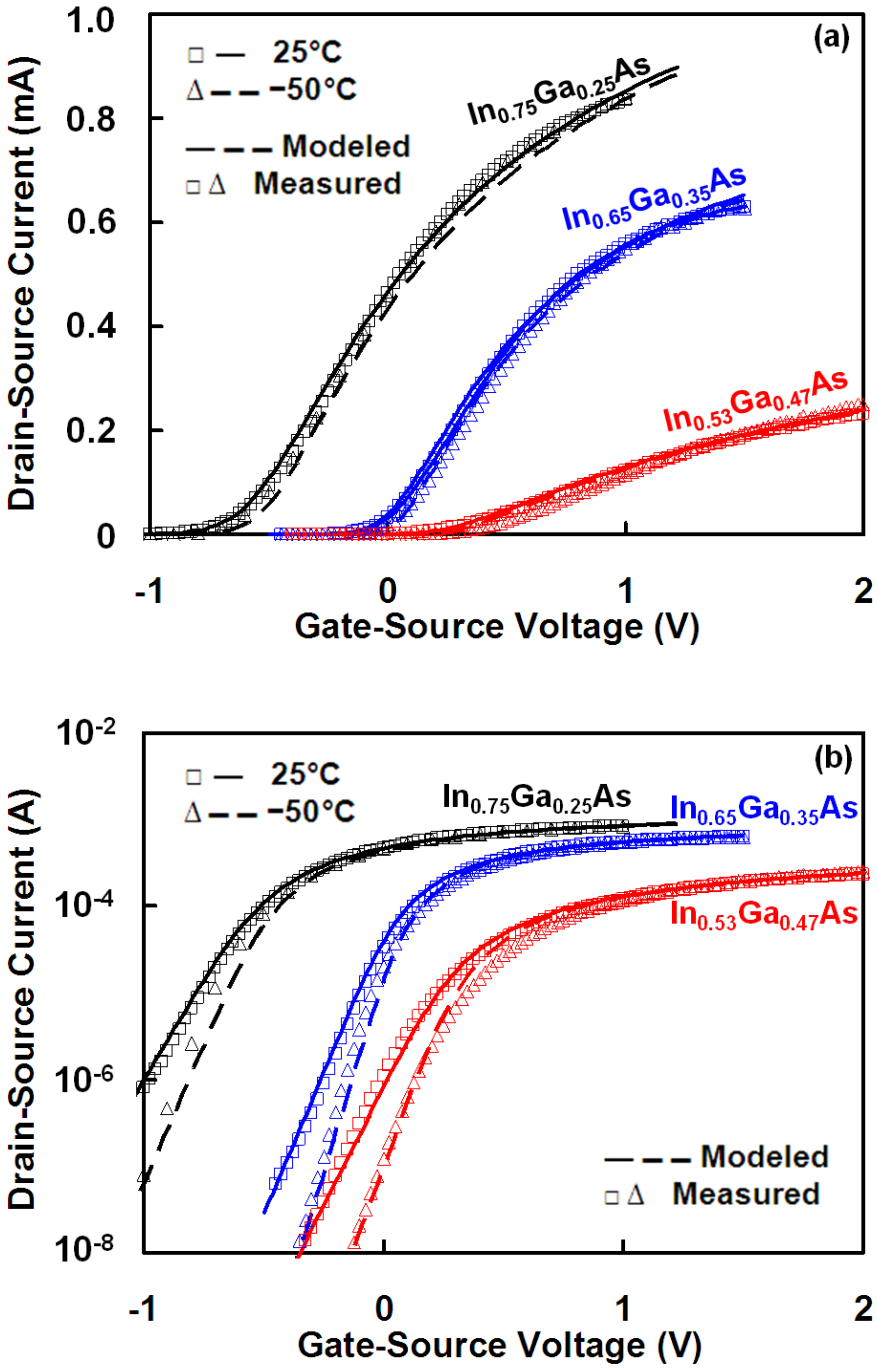


Figure 3.8: Excellent agreement between measured (symbols) and modeled (curves) transfer characteristics of InGaAs MOSFETs at room temperature (□, ——) and −50 °C (△, - - -) plotted in both linear (a) and log (b) scales. $L = 4$ μm. $W = 100$ μm.

times that of the high-κ/Si interface. Table 3.1 shows also that the interface is significantly rougher when the In mole fraction $x \approx 0.5$, which is consistent with poorer transfer characteristics of the $In_{0.53}Ga_{0.47}As$ MOSFET. However, given the limited sample size, uniformity and reproducibility, more statistics are needed before a firm correlation between the interface roughness and the In mole fraction can be established. For the same reason, no firm correlation between interface roughness and interface trap density can be established at the moment. This work would have been more complete had the interface roughness of InGaAs MOSFETs been characterized through measurements of atomic force microscopy, high-resolution transmission electron microscopy, or X-ray reflectivity as in the case of Si MOSFETs mentioned earlier.

Figure 2.9 shows that for the present InGaAs MOSFETs with high In mole fractions, although the interface trap density is of the order of 10^{13} $cm^{-2}eV^{-1}$ midgap, it decreases rapidly toward the conduction band. Since the charge neural level E_0 for high In mole fractions is very close to the conduction band (Table 3.1), inversion-mode operation with good on-state performance is achievable, whereas the off-state performance is still limited by the high interface trap density below E_0. Further, although the on-state performance appears to improve significantly with increasing In mole fraction, since the mobility under strong inversion is mainly limited by the interface roughness, the improved on-state performance cannot be attributed solely to lighter effective mass or higher bulk mobility with increasing In mole fraction. According to Equation (3.22), the interface roughness mobility

is inversely proportional to the effective mass and the approximately 20% lighter effective mass in $In_{0.75}Ga_{0.25}As$ than that in $In_{0.53}Ga_{0.47}As$ is insufficient to cause the mobility in $In_{0.75}Ga_{0.25}As$ to be approximately three times of that in $In_{0.53}Ga_{0.47}As$. Therefore, the better on-state performance with increasing In mole fraction of the present InGaAs MOSFETs is mainly due to better interface roughness.

In Section 3.1, the inversion charge was calculated by assuming a simple triangular well (Figure 3.1). In reality, the potential well in $In_{0.65}Ga_{0.35}As$ and $In_{0.75}Ga_{0.25}As$ MOSFETs contains an additional step between the channel and buffer layers as shown in Figure 3.9. However, it can be seen in Figure 3.9 that the solution of the inversion charge density Q_N for the stepped well is very close to that of the triangular well. This validates the approximation by the triangular well.

Unlike in silicon MOSFETs, the electron mobility in InGaAs MSOFETs in strong inversion was found to be mainly limited by the interface roughness. By extracting the mobility from the measured transfer characteristics, the roughness of the Al_2O_3/InGaAs interface was determined to be two to seven times of that of the SiO_2/Si interface. Therefore, to fully benefit from the high bulk mobility of InGaAs, its interface roughness with the gate oxide needs to be further improved.

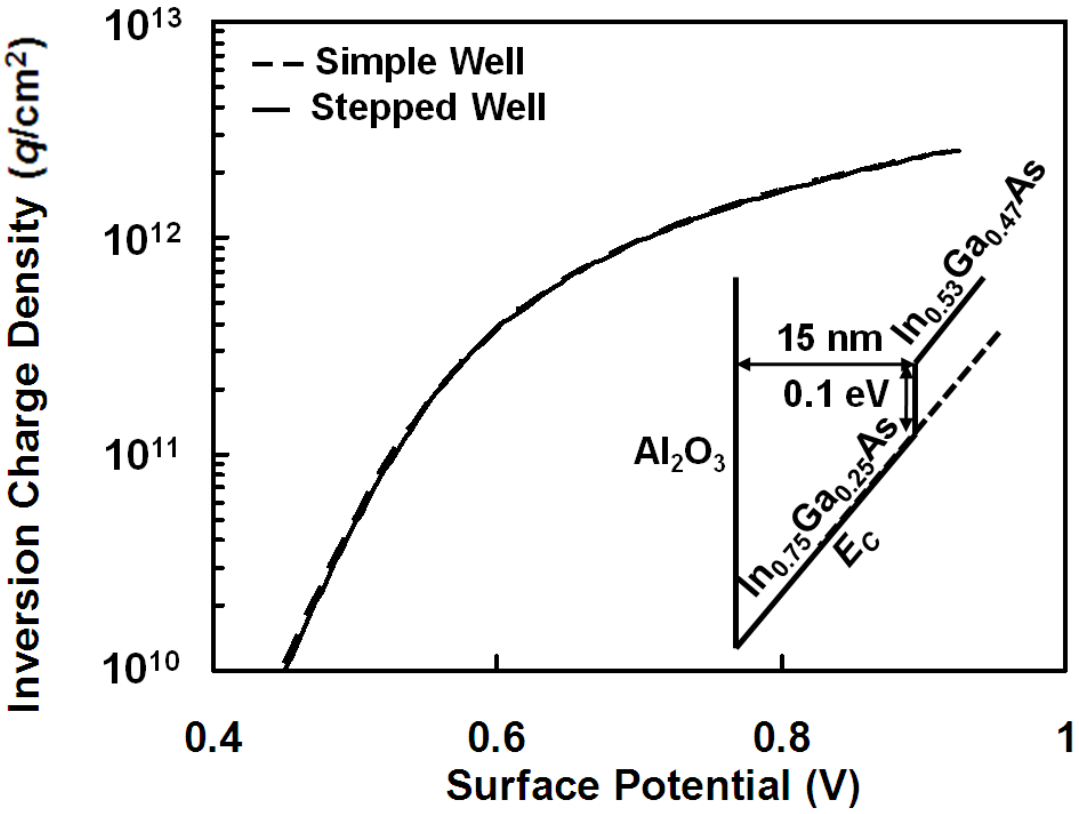


Figure 3.9: Calculated inversion charge density Q_N in $In_{0.75}Ga_{0.25}As$ MOSFETS with simple (– –) and stepped (——) triangular wells.

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Chapter 4

Junction Leakage Current in InGaAs MOSFETs

4.1 Analysis of Junction Leakage Current

The drain junction is reverse-biased during normal operation of a MOSFET. The reverse leakage current consists of the diffusion current I_{diff}, generation current I_{gen}, and band-to-band tunneling current I_{tun}. The total reverse leakage I_{R} current is the summation of all current components

$$I_{\text{R}} = I_{\text{diff}} + I_{\text{gen}} + I_{\text{tun}} \tag{4.1}$$

The diffusion current I_{diff} is governed by Shockley equation in low-injection condition

$$I_{\text{diff}} = I_0 \left[\exp\left(\frac{qV}{k_{\text{B}}T} \right) - 1 \right] \tag{4.2}$$

where I_0 is the scale current, q is the electron charge, V is the applied bias, k_{B} is Boltzmann's constant, and T is temperature. Because of the rapid decaying exponential term, $I_{\mathrm{diff}} \approx -I_0$ and has no bias dependence.

The generation current I_{gen} comes from the electron-hole pairs generated in the depletion region. When a p-n junction is in equilibrium, the generation and recombination process in the depletion region are balanced. When the p-n junction is reversely biased, the electron-hole pairs generated by thermal activation at the generation-recombination centers are swept away by the stronger electric field. The generation process dominates, contributing a net reverse current I_{gen}.

The generation rate U can be expressed by [1]

$$U = -\frac{n_{\mathrm{i}}}{2\tau} \tag{4.3}$$

where n_{i} is the intrinsic carrier concentration and τ is the lifetime of nonequilibrium carriers. The generation current in the depletion region is then given by [1]

$$I_{\mathrm{gen}} = A_{\mathrm{junc}} \int_0^{X_{\mathrm{D}}} q|U|dx \approx A_{\mathrm{junc}} \frac{q n_{\mathrm{i}} X_{\mathrm{D}}}{2\tau} \tag{4.4}$$

where A_{junc} is the junction area. The depletion width X_{D} is expressed by

$$X_{\mathrm{D}} = \sqrt{\frac{2\epsilon_{\mathrm{S}} \left(V_{\mathrm{bi}} - V\right)}{q N_{\mathrm{A}}}} \tag{4.5}$$

where ϵ_{S} is the semiconductor permittivity, V_{bi} is the junction build-in potential, and N_{A} is the acceptor concentration in the lower-doped p-region.

The tunneling current I_{tun} arises from the finite probability of direct transition of electrons from the conduction band into the valence band or vice versa through

the triangular potential barrier as shown in Figure 4.1. When the applied reverse bias is large or the electric field is high, the quantum tunneling probability is high enough so that a significant tunneling current flows.

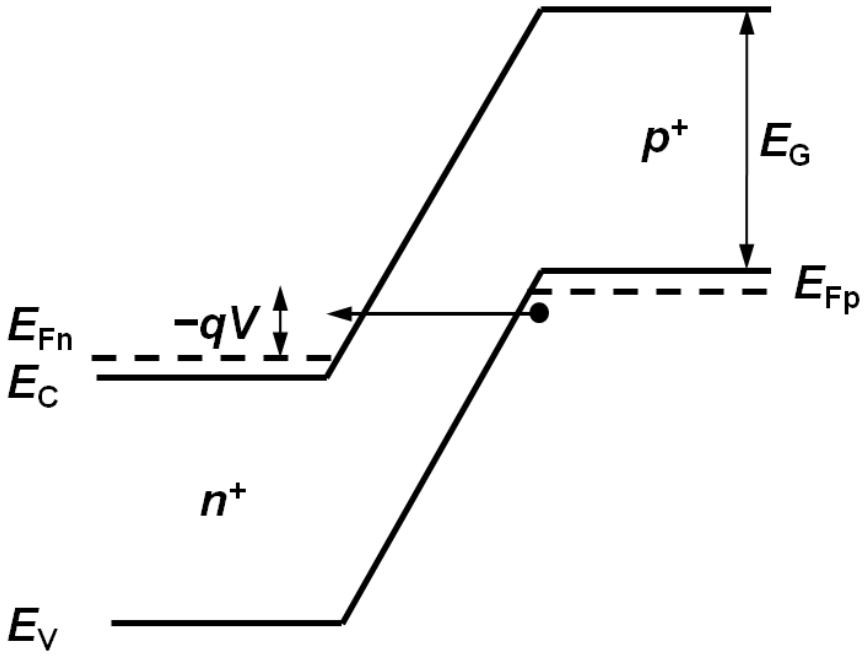

Figure 4.1: Simplified energy diagram of p-n junction at reversed bias.

By using Wentzel-Kramers-Brillouin (WKB) approximation, I_{tun} can be calculated by [2]

$$I_{\text{tun}} = A_{\text{junc}} \sqrt{\frac{2m^*_{\text{tun}}}{E_{\text{G}}}} \frac{q^3 \xi^2 w}{(2\pi)^3 \hbar^2} \exp\left(-\frac{\pi}{4q\hbar\xi}\sqrt{2m^*_{\text{tun}} E_{\text{G}}^3}\right) \tag{4.6}$$

where A_{junc} is the junction area, m^*_{tun} is the reduced effective mass, E_{G} is the bandgap energy, ξ is the electric field, $\hbar$ is the reduced Plank's constant, and w is effective depletion width for the tunneling process. It is assumed that w is 20% of the total depletion width for the tunneling process $w = 0.2X_{\text{D}}$ [2]. The electric field

is given by

$$\xi = \sqrt{\frac{2qN_{\mathrm{A}}\left(V_{\mathrm{bi}} - V\right)}{\epsilon_{\mathrm{S}}}} \tag{4.7}$$

4.2 Experiments and Discussions

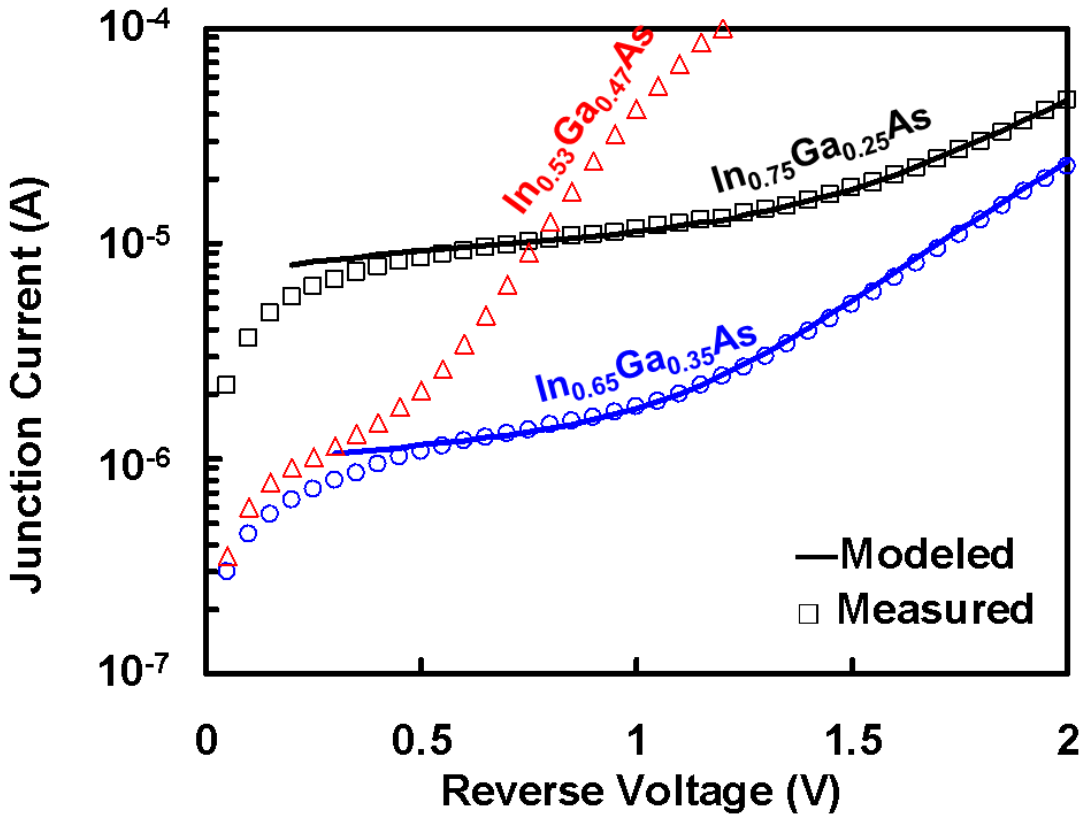

Figure 4.2: Agreement between measured (symbols) and modeled (curves) junction leakage currents of InGaAs MOSFETs at room temperature. The current and voltage are all negative and are plotted in their absolute values for convenience. $In_{0.53}Ga_{0.47}As$ MOSFET does not have a modeled curve because the anomalous increase arising from the residual implantation damage is beyond the scope of discussed mechanisms. Note the model is not accurate in small-bias region ($|V| \lesssim 0.3$ V) because of the non-negligible recombination current.

Figure 4.2 shows the modeled and measured junction leakage currents of the present InGaAs MOSFETs at room temperature. Excellent agreement was achieved from $|V| = 0.3$ V to 2 V for $In_{0.75}Ga_{0.25}As$ and $In_{0.65}Ga_{0.35}As$ MOSFETs. Generally, I_R increases with In mole fraction because I_{diff}, I_{gen}, and I_{tun} all increases. For the same reason, InGaAs MOSFETs have higher junction leakage currents than Si MOSFETs. The junction leakage current of present $In_{0.53}Ga_{0.47}As$ MOSFET has a much steeper anomalous increase beyond the scope of mechanisms discussed above when the applied reverse voltage increases. It is probably due to the residual implantation damage which creates leaky paths inside the junction in this particular wafer. In small-bias region ($|V| \lesssim 0.3$ V), the recombination rate is not negligible compared to the generation rate. In the depletion region, there is a complex balance of generation and recombination currents which cannot be described by simple analytical solutions of Equations (4.3) and (4.4). In medium-bias region ($0.3\text{ V} \lesssim |V| \lesssim 1.4\text{ V}$) the generation current dominants and I_R would have a stronger temperature dependence. In high-bias region ($1.4\text{ V} \lesssim |V|$), the electric field is large enough to produce significant tunneling current which dominates I_R. And I_R has a stronger voltage dependence in this region. Table 4.1 lists the parameters used in the calculation. Other materials parameters can be found in Table 3.1.

Channel	$In_{0.65}Ga_{0.35}As$	$In_{0.75}Ga_{0.25}As$
A_{junc} (cm^2)	780×10^{-8}	
I_0 (A)	1×10^{-9}	1×10^{-7}
τ (s)	6×10^{-11}	4×10^{-11}
m^*_{tun} ($m_0^{a)}$)	0.04	0.05

[a)] electron rest mass

Table 4.1: Model parameters for reverse junction leakage current.

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Chapter 5

Conclusions

This dissertation addresses the electrical characterization of the interface traps, analysis of the inversion charges, electron mobility and junction leakage currents of $Al_2O_3/In_xGa_{1-x}As$ (x = 0.53, 0.65 or 0.75) MOSFETs. Several models have been built to explain the measured characteristics. In this chapter, we will summarize the materials presented in previous chapters.

5.1 Conclusions of This Dissertation

Charge pumping has been used to characterize the interface traps between Al_2O_3 and InGaAs in n-channel inversion-mode MOSFETs. An analysis of the charge pumping current with gate voltage pulses of different rise and fall times has enabled the interface trap density to be extracted across the energy bandgap. The interface trap density $D_{\rm it}$ distribution is very similar for different $In_xGa_{1-x}As$ channels. $D_{\rm it}$ is

found to be 1–3$\times 10^{12}$ cm^{-2}eV^{-1} near E_C and peaks at about 3×10^{13} cm^{-2}eV^{-1} further down into the bandgap, and follows a Gaussian-like distribution. The majority of interface traps in indium-rich InGaAs metal-insulator-semiconductor structures have been identified as donors. Even though the donor traps are neutralized upon inversion and do not affect the on-state performance of InGaAs MOSFETs, such as threshold voltage and maximum drain current, they limit the off-state performance of InGaAs MOSFETs, such as subthreshold slope, drain-induced barrier lowering, and on/off current ratio. The results obtained in our measurements help explain the promising on-state performance of the Al_2O_3/InGaAs MOSFETs and the need to further improve the interface so that its off-state performance can be on par with that of the Si MOSFET.

The electron mobility in Al_2O_3/InGaAs MOSFETs has been analyzed for scattering by oxide charge as well as interface charge and roughness, and compared with measured transfer characteristics from depletion to inversion. The analysis shows that in strong inversion the electron mobility can be as high as ~ 3000 cm^2/V/s and is mainly limited by interface roughness. The extracted interface roughness from the measured data is two to seven times that of the interface between a high-κ dielectric and Si, assuming the correlation lengths are comparable. Therefore, to fully benefit from the high bulk mobility of InGaAs, its interface roughness with the gate oxide needs to be further improved.

Finally, the reverse junction leakage current has been analyzed by calculating diffusion, generation, and tunneling currents, and compared with measurement at

room temperature. We find that the leakage current increases with In mole fraction. Generation and tunneling currents dominate in medium- and high-bias regions, respectively.

5.2 Future Study

It is recently found that GaAs and InGaAs MOSFETs fabricated on (111)A substrates have better performances [1, 2]. It is of great interest to carry out the same study presented in this dissertation on devices fabricated on (111)A substrates and compare it with this work.

Researchers have demonstrate the scaling of InGaAs MOSFETs into deep-submicron level [3]. As the thickness of the gate dielectric is scaled down proportionally, excessive gate leakage current will increase the power consumption and bring serious reliability problems to III-V MOSFETs like in the silicon world. Analysis of gate leakage current in deep-submicron III-V MOSFETs will greatly help researchers optimize the process to solve the problem.

Because of the relative high trap density and high transconductance, III-V MOSFETs have both higher thermal [4] and $1/f$ [5] noises—two major contributions of noise in a FET device—than its silicon counterpart. A noise analysis is important in fully evaluating the performance of III-V MOSFETs.

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