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Sub-nanosecond Pulse Characteristics of InGaP/ GaAs HBTs

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**Sub-nanosecond Pulse Characteristics of
InGaP/GaAs HBTs**

by

Renfeng Jin

Presented to the Graduate and Research Committee
of Lehigh University
in Candidacy for the degree
of Doctor of Philosophy

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Abstract

Using a novel sub-nanosecond pulse current-voltage measurement technique, this dissertation shows that InGaP/GaAs HBTs can survive stronger impact ionization and to have a much larger safe operating area (SOA) than previously measured or predicted. The extension of safe operating area is mainly attributed to the elimination of the self-heating effect due to the short conduction time. To interpret this phenomenon quantitatively, in this dissertation, avalanche breakdown effect is carefully characterized and an empirical model for impact ionization with voltage and current dependence was extracted and added to a commercially available HBT model. The modified model could accurately predict the HBT characteristics across the enlarged safe operating area. Meanwhile, a new method is developed to forecast the ruggedness of CW Class-C power amplifiers by using measured safe operation boundary.

An ultra-wideband pulse generator was designed with the new model and fabricated in GaAs HBT IC technology. The generator includes delay and differential circuits to generate Gaussian impulse from a TTL input signal, and a Class-C amplifier to boost the pulse amplitude while compressing the pulse width. By adjusting the collector bias of the

Class-C amplifier, the pulse amplitude can be varied linearly between 3.5 V and 11.5 V while maintaining the pulse width at 0.3 ± 0.1 ns. Alternatively, by adjusting the base bias of the Class-C amplifier, the pulse width can be varied linearly between 0.25 ns and 0.65 ns while maintaining the pulse amplitude at 10 ± 1 V. Additionally, the amplified impulse signal can be shaped into a monocycle signal by an L-C derivative circuit. These results compare favorably with those of other pulse generators fabricated in CMOS ICs, step-recovery diodes, or other discrete devices.

Chapter 1 Introduction

Gallium Arsenide (GaAs) devices have been preferred in wireless application for military and space service for a few decades because of their superior electron mobility and less parasitics, as compared to Si devices. With the explosive growth in commercial broadband applications and the increasing demand in wireless communication areas (including cellular/PCS handsets and systems), GaAs process technology is now widely accepted as a main technology for the production of high frequency, high power and low noise products for these applications.

There are two major classes of GaAs based devices: heterojunction bipolar transistors (HBTs) and high electron mobility transistors (HEMTs). These devices make use of an innovative growth technique known as molecular beam epitaxy to create sharp transitions in both doping and composition material.

Compared with HEMTs, HBTs suffer from thermal instability, worse noise performance at high frequencies. However, they are still worth the price we pay for [1]: the high transconductance values in HBTs allows them to be operated with small input voltage amplitudes and fast charging of load capacitances in ICs. Their current-handling

capability is dramatically larger than that of HEMTs. For example, a HEMT amplifier generally occupies three times the device area of a HBT amplifier to deliver the same output power. In addition, they exhibit better linearity characteristics than HEMTs, which is important in mobile communication applications.

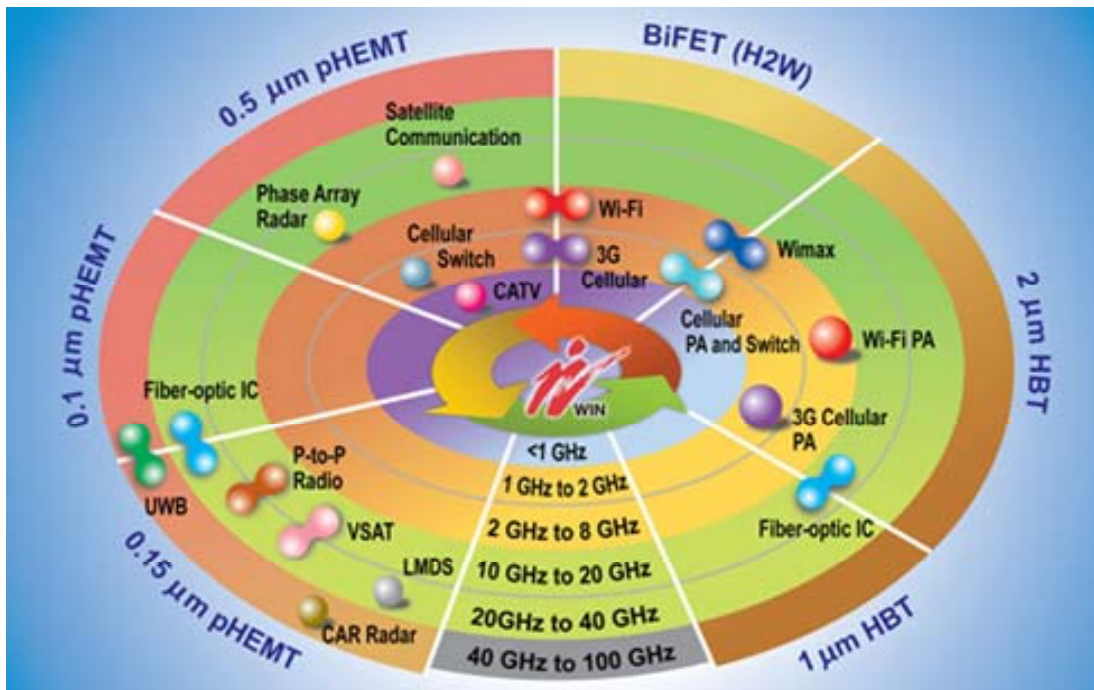


Fig. 1-1 GaAs device technology overview.

1.1. GaAs/InGaP HBT

The emitter of an HBT is made of a wide-bandgap semiconductor material. The fraction of the band gap difference ΔE_G falls into the valence band and prevents holes in the base from back-injecting into the emitter. The larger the valence band discontinuity is, the better the suppression of the hole back injection will be. So the base doping could be

higher than emitter doping without compromising the emitter injection efficiency in the HBTs.

Early HBTs were fabricated based on aluminum gallium arsenide/gallium arsenide (AlGaAs/GaAs) technology. In an $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ HBT, the conduction band discontinuity (ΔE_C) is 0.13 eV and the valence band discontinuity (ΔE_V) is 0.24 eV [1]. The drawback of this technology is the large energy spike formed at the emitter side of the junction. This energy spike will increase the emitter-base turn-on voltage and the ideality factor. One of the possible ways to compress the spike is to gradually change the mole fraction of aluminum in the emitter to make a graded heterojunction. But a very precise control is needed in the process, which further increase the cost of fabrication.

Later, the ordered indium gallium phosphide (InGaP) emitter layer took place of AlGaAs, which makes nearly perfect lattice match between emitter and base avoiding any conduction band discontinuity. Meanwhile, an ordered $\text{In}_{0.51}\text{Ga}_{0.49}\text{P}/\text{GaAs}$ HBT has 0.40 eV valence band discontinuity which can suppress the hole back injection effectively to provide good forward current characteristics. It is worth pointing out the ease of InGaP/GaAs device fabrication. Several common etching solutions can be used to etch InGaP without impacting GaAs, and conversely etch GaAs without impacting InGaP. But

for AlGaAs, overetching will make the base resistance higher than it supposed to be [2].

Table 1-1 summarizes heterojunction parameters at room temperature of different material.

	$\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ /GaAs	$\text{In}_{0.51}\text{Ga}_{0.49}\text{P}$ /GaAs	InP / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	$\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ / $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	Si/ $\text{Si}_{0.8}\text{Ge}_{0.2}$
ΔE_G (eV)	0.37	Ordered: 0.43 Disordered: 0.46	0.60	0.71	Unstrained: 0.078 Strained: 0.165
ΔE_C (eV)	0.24	Ordered: 0.03 Disordered: 0.22	0.23	0.50	
ΔE_V (eV)	0.13	Ordered: 0.40 Disordered: 0.24	0.37	0.21	

Table 1-1 Heterojunction parameters at room temperature

In this dissertation, we will focus on the InGaP/GaAs HBTs.

1.2. Safe operating areas

The safe operation area (SOA) is a region on a collector current *vs.* collector-emitter voltage (I_C - V_{CE}) plane in which a sudden device failure does not occur. SOA is an important concern for HBT power amplifiers when they are used to drive antennas whose impedance varies with the environment. HBTs suffer from various feedback phenomena like all other bipolar devices. These feedback phenomena will cause instability and device failure in certain operating conditions. There are two major phenomena limiting

the SOA of the HBTs: impact ionization and self-heating effect.

The most well known damaging effect is the “thermal runaway” caused by self-heating effect [3][4][5][6]. Thermal conductivity of GaAs (0.46 W/cm° C) and In_{0.51}Ga_{0.49}P is (0.05 W/cm° C) is lower than that of silicon (Si) (1.5 W/cm° C). The In_{0.51}Ga_{0.49}P/GaAs HBTs are therefore prone to self-heating effect. When the device is operated at high powers, the increased junction temperature strengthens the thermionic emission. As a result, the collector current increases. This property is illustrated by an empirical expression relating collector current, base-emitter voltage and junction temperature [1]:

$$I_C = I_0 \cdot \exp \left\{ \frac{q}{\eta k T_A} \left[V_{BE} - I_E R_E - I_B R_B + \phi (T - T_A) \right] \right\} \quad (1-1)$$

Where I_0 is the collector saturation current, V_{BE} is the base-emitter bias, η is the collector current ideality factor, T_A is the ambient temperature, I_E is the current flowing out of emitter, R_E is the emitter resistance, I_B is the current flowing into the base, R_B is the base resistor and T is the actual junction temperature. The degree of the change of the turn-on voltage in response to the junction temperature is characterized by thermal-electrical feedback coefficient ϕ , typically 1.25 mV/° C for GaAs. An effective way to alleviate this problem is to increase the emitter resistance (R_E) or to add a ballast resistor [7][8][9][10]. Then the instability introduced by the positive feedback can be

delayed to higher currents.

Due to their practical relevance in determining the safe operation boundary, electrothermal phenomena in bipolar junction transistors (BJTs) have been intensively studied since 1950s. Initially, research mainly are focused on the analysis of current crowding effects caused by thermal feedback [11][12]. Several models were proposed to describe the mechanisms of hot spot formation and nonuniform temperature and current distribution in the large area devices, which is considered as the main reason of the instability phenomenon [13][14][15]. Recently, with the decreasing of emitter width, the attention was shifted to the analysis of electrothermal instability in single-finger and multi-finger devices and the thermal distribution inside the finger is assumed negligible. Lots of studies have been published which made remarkable achievement in clarifying the electrothermal behavior. Latif and Bryant [16] showed the existence of flyback points in the output characteristics of BJTs when the base-emitter junction was driven by a constant voltage. It was also shown that the flyback points form the boundary of device safe operation area. An analytical equation of self-heating effects inside single-finger was derived by Popescu [17]. The model assumes the parasitic resistances are zero and the base-emitter voltage temperature coefficient is constant. It can correctly predict the

“flyback” behavior of the I_C - V_{CE} characteristics with a constant base-emitter voltage. Heasell [18] established a more complicated model which includes the temperature dependence of thermal conductivity, as well as avalanche effects and parasitic resistances. Liou *et al.* [19] published the model for one- and two-finger heterojunction bipolar transistors (HBTs). The model covers both the constant V_{BE} and constant I_B bias conditions. Rinaldi and Alessandro [3] presented an approach which allows the calculation of both the critical current and collector voltage at the flyback point for a given $V_{BE} = \text{const.}$ characteristic. Overall, there are a large number of literatures on the electrothermal topic and great insight have been developed.

Another important effect that is even more devastating is the impact ionization when the device is operating at high voltage. In an NPN transistor, impact ionization usually happens in the depletion layer of the collector. The avalanche current results in a hole current back injected into the base. If this current is large enough, it will reverse the direction of the base-current, so the third term in Eqn. 1-1 will also act as a positive feedback and leads to device instability. This situation can be much worsened when the Kirk effect happens. To date, the on-state impact ionization has mostly been empirically determined [20] with little theoretical understanding or experimental validation. For

example, [21] considered the reduction of tolerable collector voltage with increasing collector current, [22] modeled the effects of base resistance and ambient temperature on the collector-emitter breakdown voltage, [23] proposed a limit by the flyback (bifurcation) of the collector current due to impact ionization and/or self heating, and [10] considered the effects of both base and emitter resistances on breakdown and defined the SOA by flyback similar to [13].

In this thesis, we will further study both theoretically and experimentally the on-state impact ionization introducing breakdown and its impact on HBT power amplifiers through impulse mode characterization.

1.3. Pulse I-V characterization

Current-voltage (I - V) measurement is usually performed under a DC bias and the characterization procedure usually suffers from several drawbacks, more or less, resulting in inaccuracies of the model. First, the DC power dissipated in the devices causes self-heating effects, so the device internal temperature is not constant [24]. Because most of the device model parameters are temperature dependent, inaccuracies will be introduced during the parameter extraction. Secondly, microwave FET devices have trapping effects that will impact the DC behavior. Sometimes large errors are introduced

in the determination of output conductance and transconductance [25][26]. Thirdly, DC safe operation areas can be quite different from the real safe operation area that can be reached by large RF signal [27][28]. So the real RF power may be underestimated by using the DC boundaries. All those drawbacks drive the development of the pulse mode measurement technique.

Recently, pulse I - V measurements have been performed widely by different groups with 40-500 ns pulses, which significantly reduce self-heating. In [29], Heckmann *et al.* achieved the 500 ns pulse by using a DC pulse generator in series with a resistor. This pulsed measurement setup was used to characterize and model the breakdown effect in HBTs. However, the self-heating effect is only partially eliminated in HBT devices whose thermal time constant is 3 μ s [30]. In [31], Meneghesso *et al.* pulsed the output side through a computer-controlled, three-terminals transmission line pulse (TLP) system with 50 – 100 ns pulse width, while a constant voltage source added at the input side. This TLP system can be used for nondestructive measurements of the on-state breakdown characteristics of GaAs MESFETs and HEMTs up to high values of gate current density. However, constant base-emitter bias will be an obstacle in measuring BJT device in high current region, because both of the base-collector and base-emitter junctions will have

already conducted before the collector pulse is applied. Especially, the base-collector junction is a homo-junction which cannot afford the same high forward bias as the base-emitter (hetero-junction) does. This issue can be improved by replacing the constant voltage source with a current source, e.g. presented by Saleh *et al.* in [32]. But the real device SOA can not be measured by connecting a constant current source at the base [10][21]. Pan *et al.* in [33] quiescently biased the device in the active region before adding voltage pulses at the device collector and base sides. The drawback is that device has already been heated up by DC bias. In our study, we bias the device in the cut-off region. At the collector side, we replace the voltage pulser by a DC voltage source. This will benefit the characterization of the devices with high breakdown voltage since DC voltage source can deliver much higher voltage than voltage pulser can.

1.4. Organization of the dissertation

The work described in this dissertation is an investigation and identification of the SOA of InGaP/GaAs HBTs under isothermal conditions. Chapter 2 will describe the core experimental techniques used in our investigation. The difference between the DC I-V and our sub-nanosecond pulse I-V characteristics is discussed. To gain insight into the problem, a number of measurements under different condition were used. Impact

ionization was confirmed to be the mechanism limiting the sub-nanosecond SOA, but the device could survive beyond the flyback. Later a new impact ionization model is derived to forecast the HBT behavior in the pulse mode. In chapter 3, we will discuss the impact of sub-nanosecond SOA on the HBT power amplifier. Many waveform measurements were used and we found Class-C amplifiers can work beyond the DC or microsecond SOA and are tangential to the sub-nanosecond SOA boundary. This shows that the SOA of the Class-C amplifier is mainly limited by on-state breakdown. The pulse mode characterization results can also be used in building time-domain impulse amplifiers. A tunable pulse generator is built for Ultra-wideband (UWB) application, which will be discussed in chapter 4. Finally, in chapter 5 conclusions will be drawn and suggestions for the future work will be made.

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Chapter 2 Experimental

Compared with pulses in previous work described in chapter 1, the pulses we are using are as narrow as 200 ps. Main benefits of sub-nanosecond pulse measurement are but not limited to: first, the self-heating effect is completely eliminated in the measurement and the measurable safe operation area extends. Secondly, RF performance of the device can be better predicted because the pulse width is comparable to the RF signal. Thirdly, it can help to extract the on-state impact ionization model accurately.

The device under test is a commercially available [1] single-finger n-p-n InGaP/GaAs HBT with an emitter area $A_E = 2 \mu\text{m} \times 20 \mu\text{m}$. Typically, it has a cut-off frequency of 40 GHz, a maximum frequency of oscillation of 60 GHz, a common-emitter open-base breakdown voltage BV_{CEO} of 15 V, and a common-base open-emitter breakdown voltage BV_{CBO} of 30 V. The thermal time constant is approximately 3 μs . To bypass packaging parasitics, all measurements are done on wafer. All results reported in this paper are obtained on the same HBT wafer with better than 3% uniformity.

2.1. Sub-nanosecond Pulse I-V test bench

Fig. 2-1 shows that the sub-nanosecond time-domain measurement setup consists

mainly of an Avtech AVM-2-C 200-ps 10-V pulse generator and an Agilent 86100 50-GHz digital sampling oscilloscope [2]. The pulse generator drives the HBT base through an attenuator and power-divider network to ensure that broadband 50-Ω source impedance is presented to the HBT base. A broadband 2:1 resistive power divider allows the oscilloscope to monitor the input pulse through Channel 1. The oscilloscope samples the output from the HBT collector through Channel 2. The waveforms sampled by the oscilloscope are de-embedded to the HBT base and collector by accounting for the frequency response of the cable assemblies that include bias networks and attenuators.

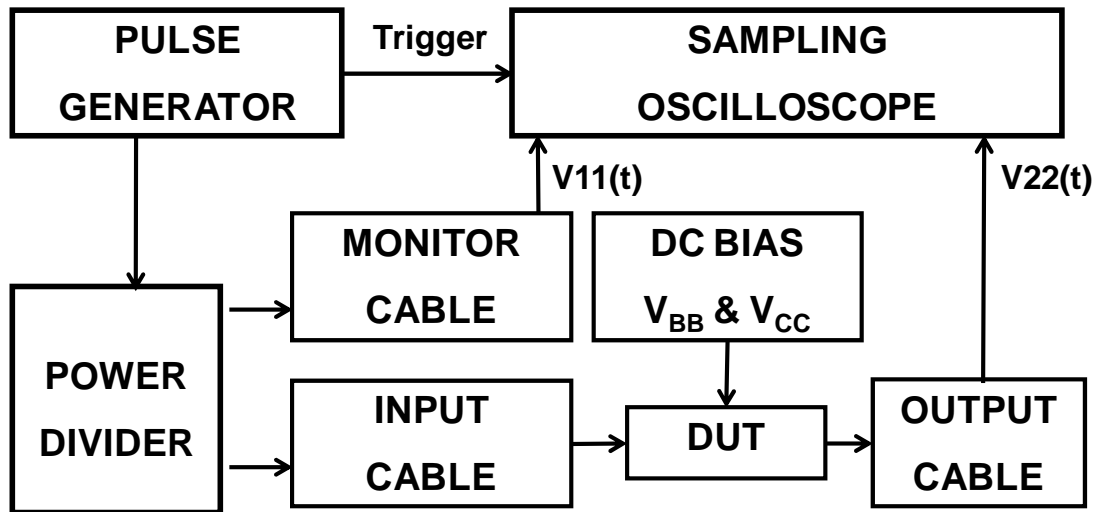


Fig. 2-1 Schematic diagram of the present sub-nanosecond time-domain measurement setup. The cable assemblies include attenuators and bias networks that are not shown.

The resistive power divider has ideal broadband characteristics that resulted in equal response at its two output ports. Thus, the Channel 1 voltage waveform $V_{11}(t)$ represents

the input source voltage across a 50-Ω load and attenuated by the monitor cable loss $S_{21MONITOR}$. S_{11} is not considered because the cable assemblies have >15 dB return loss up to 20 GHz. Therefore, the source electromotive force $V_1(t)$ (in series with a 50-Ω load) at an open load is:

$$V_1(t) = F^{-1} \left(\frac{F(V_{11}(t))}{S_{21MONITOR}} S_{21INPUT} \right) \times 2 \quad (2-1)$$

where F and F^{-1} stand for Fourier and inverse Fourier transforms, respectively. The factor of 2 accounts for the division across two 50-Ω resistors. Similarly, the output voltage $V_{22}(t)$ across a 50-Ω load at the HBT collector is

$$V_2(t) = F^{-1} \left(\frac{F(V_{22}(t))}{S_{21OUTPUT}} \right) \quad (2-2)$$

The above-described calibration procedure was verified by using a “through” standard. Fig. 2-2 shows that similar input and output waveforms de-embedded to both ends of the “through” standard.

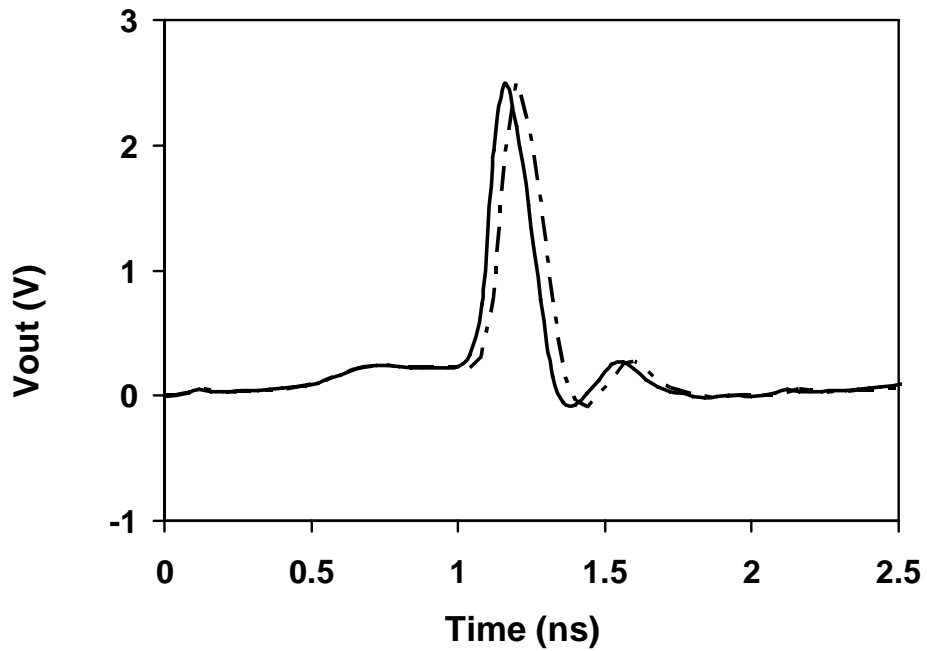


Fig. 2-2 200 ps pulse (—) input and (- -) output voltage waveforms de-embedded to both ends of a “through” standard for verification of the calibration procedure.

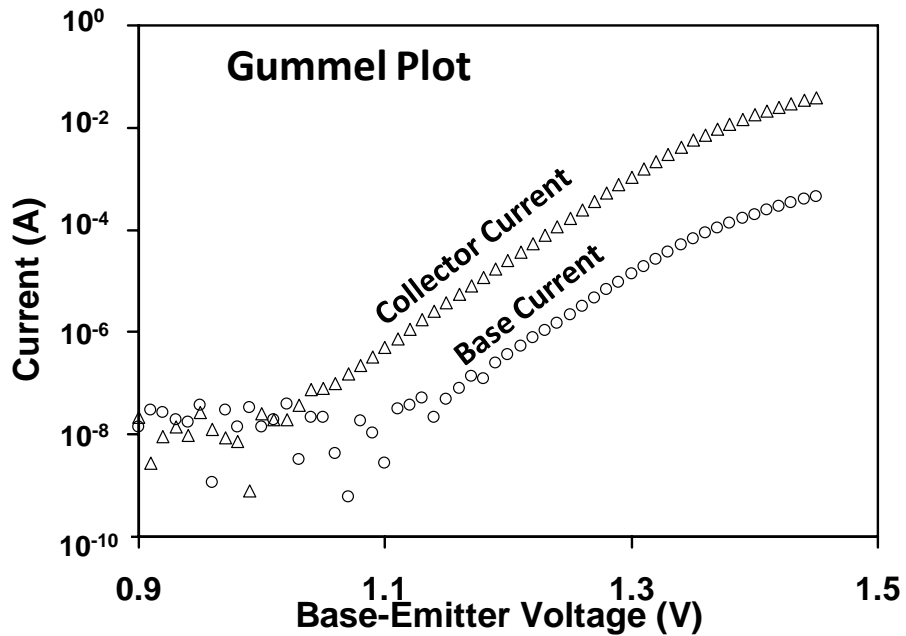


Fig. 2-3 Gummel plot of InGaP/GaAs HBT

Fig. 2-3 is the Gummel plot of InGaP/GaAs HBT. The collector current is 1 mA when

the base-emitter voltage is equal to 1.3V. If the base-emitter voltage is smaller than 1.2V, the collector current is less than 20uA. The tester limitation is 0.01uA, so the base-emitter voltage does not go below 0.9V. In tests below, the maximal quiescent voltage at the base (V_{BB}) is equal to 1.2V and the maximal collector-emitter voltage is less than 30V. The thermal resistance of this HBT is 1200 °C/W. So the rising temperature inside the device due to DC quiescent bias is less than $\Delta T = I_{CE} \times V_{CE} \times R_{TH} = 0.72$ °C, which can be neglected.

The InGaP/GaAs HBT is biased in the common-emitter configuration for Class-C operation in the sub-nanosecond pulse measurement. Fig. 2-4 shows the sampled waveforms. Although the collector bias V_{CC} is constantly applied, the HBT is turned on only when the signal from an Avtech AVM-2-C pulse generator is added to the base bias V_{BB} to raise the base-emitter voltage V_{BE} above the threshold. Therefore, $V_{BE} = V_{BB} + 2V_1$ when the HBT is cut off. When the HBT is turned on, V_{BE} is less than $V_{BB} + 2V_1$ because $2V_1$ is split between the internal resistance of the generator and the base-emitter resistance of the HBT. In this case, V_{BE} can only be simulated by subjecting the input of an HBT model to a pulse generator of $2V_1$ amplitude and 50- Ω internal resistance. The output voltage V_{22} sampled by Channel 2 of the oscilloscope is de-embedded to the HBT

collector as V_2 , so that the collector current $I_C = V_2/50 \Omega$ and the collector-emitter voltage

$$V_{CE} = V_{CC} - V_2.$$

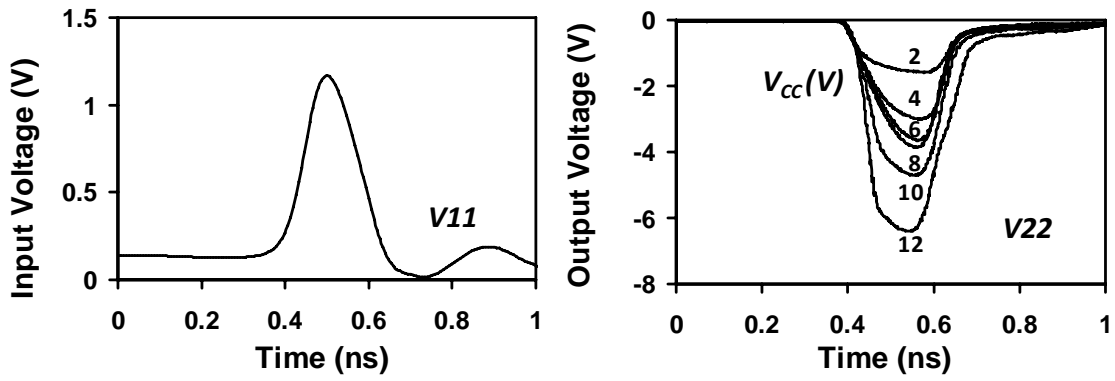


Fig. 2-4 Waveforms sampled by the oscilloscope.

The sub-nanosecond pulse measurement is typically performed with a pulse-repetition frequency of 40 KHz, so that the duty cycle is less than 0.001% and the measurement is truly isothermal. For comparison, microsecond pulse measurement is also performed by using an Agilent 85124A pulse modeling system, while DC measurement is performed by using an Agilent 4156C semiconductor parameter analyzer.

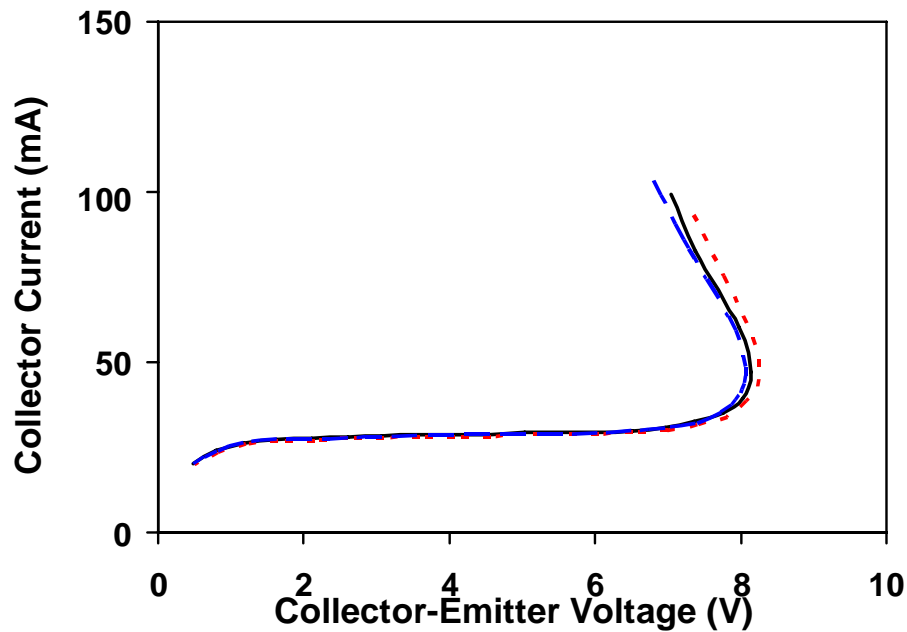


Fig. 2-5 Sub-nanosecond pulse I-V curves from 3 different devices in the same measurement

To verify the uniformity of device performance under sub-nanosecond condition, 3 devices are measured by using the same bias. Those devices are selected from different locations far away from each other on the wafer. And the test results are shown in Fig. 2-5: 3 devices only have less than 4% difference in voltage. So it is reasonable to assume that experiment data from multiple devices can be treated as those from the same device. This is quite important because sometimes the device are driven to die and more than one device are needed to complete one experiment in next sections.

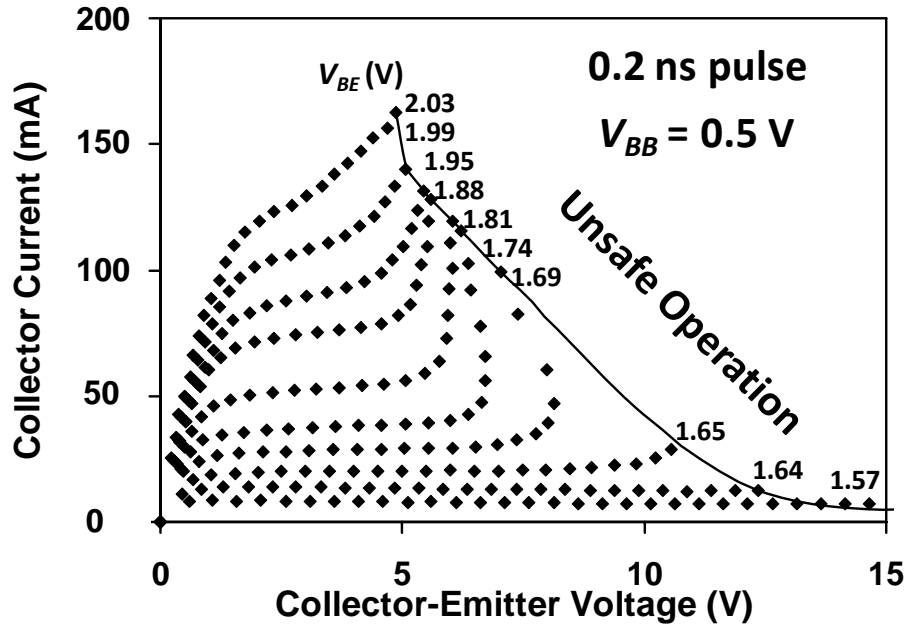
2.2. Sub-nanosecond HBT SOA

2.2.1. Sub-nanosecond SOA vs. Microsecond SOA

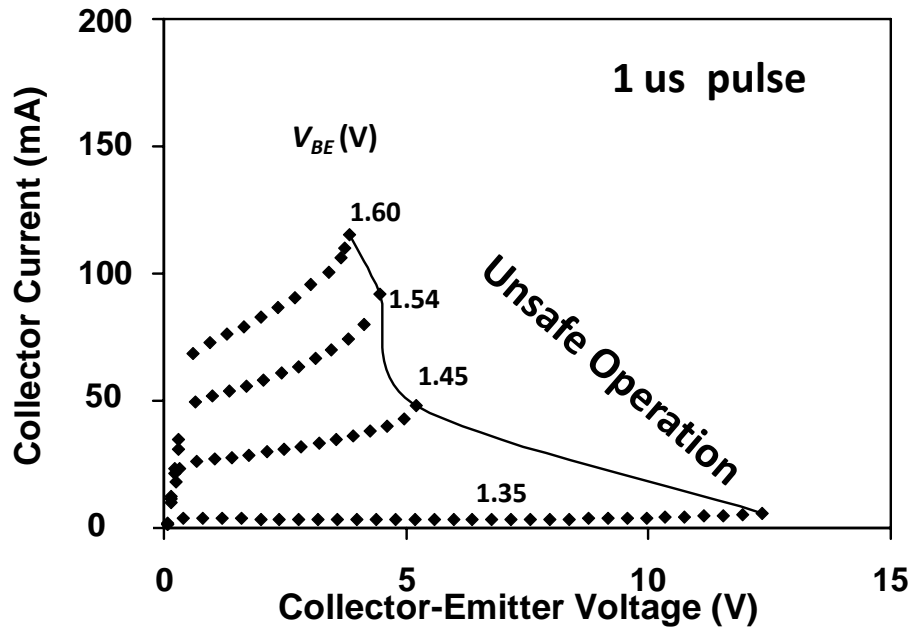
Fig. 2-6 shows that the SOA measured under sub-nanosecond pulses is significantly larger than that measured under DC or microsecond pulses. Each I - V characteristic is obtained by keeping V_{BE} constant while stepping V_{CE} until the HBT dies. For example, approximately 10 HBTs are sacrificed to obtain Fig. 2-6(a). The extreme of all characteristics empirically define the SOA. It can be seen that under sub-nanosecond pulses, measurements are extended to the region where V_{CE} decreases with increasing I_C . Such flyback has long been predicted [3], [4], [5] but rarely measured. This is because conventional microsecond pulse measurements reduce but do not eliminate self heating, so that the HBT would die as soon as flyback appears in the collector current. Thus, the SOA was conventionally defined by the inflection points of flyback and the assumption was that the HBT would die instantly of oscillation at these bifurcation points. The present result suggests that oscillation takes time to build up in strength and the HBT may survive occasional excursion into the flyback region such as under sub-nanosecond pulse operation or above-GHz CW operation. Also, the device-under-test is loaded with 50Ω so that oscillation will not occur simply because the HBT output impedance becomes nil.

Oscillation is possible only when the HBT output impedance is more negative than -50

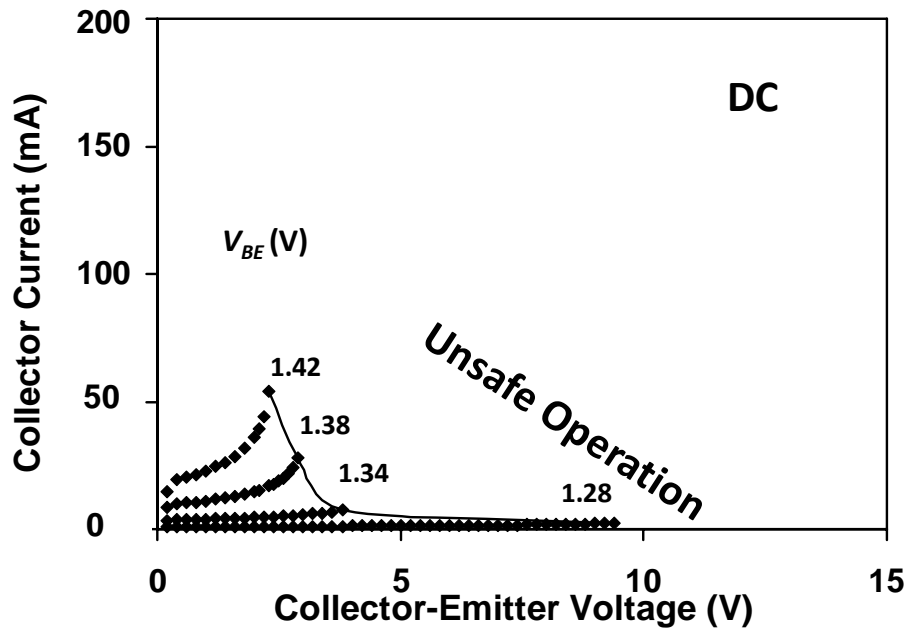
Ω .



(a)



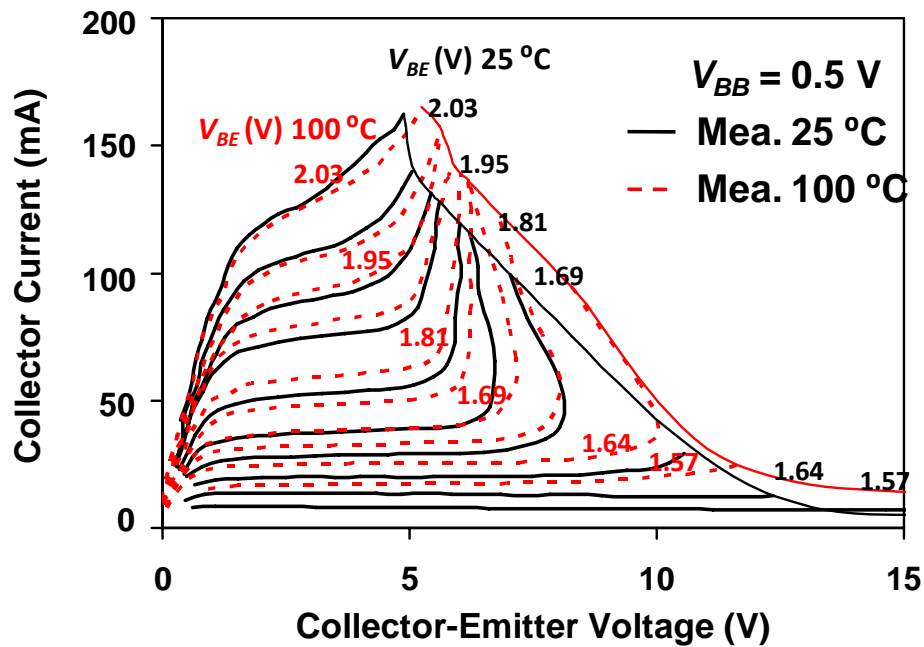
(b)



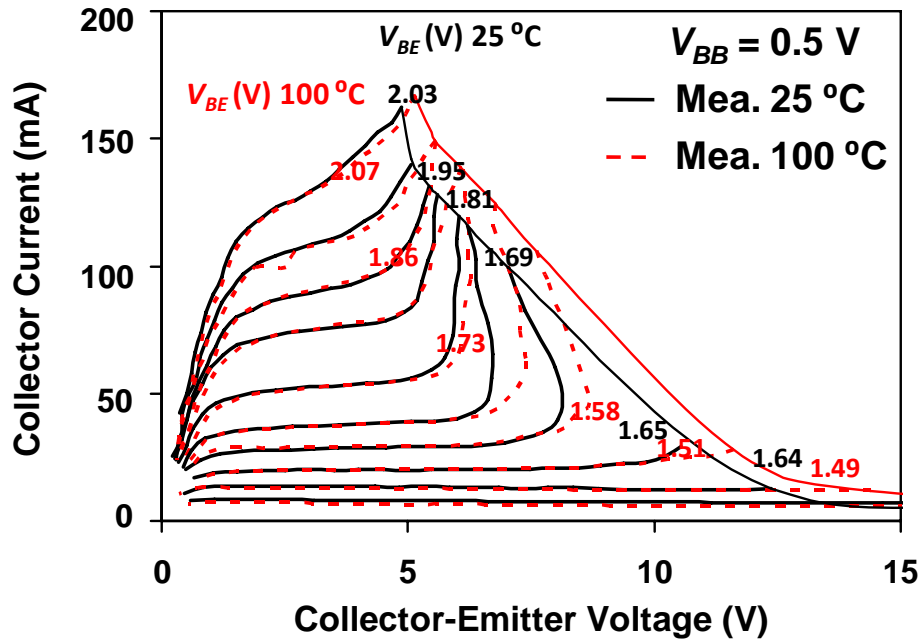
(c)

Fig. 2-6 Measured (a) sub-nanosecond pulse, (b) microsecond pulse, and (c) DC current-voltage characteristics of a common-emitter HBT. Each characteristic is obtained by pulsing to the same V_{BE} while stepping up V_{CE} after each pulse until the HBT dies.

Even under sub-nanosecond pulses, flyback for collector currents lower than 20 mA is usually too sharp to be reliably captured. Above 80 mA, the collector current increases sharply but does not flyback, because in this case the breakdown is heavily influenced by the Kirk effect [2]. Bifurcation has also been predicted [3] for thermally coupled multi-finger transistors. However, although the result shown here is limited to single-finger HBTs, we have measured sub-nanosecond characteristics in multifinger HBTs well beyond flyback, too.



(a)



(b)

Fig. 2-7 Measured sub-nanosecond pulse characteristics under different ambient temperatures with (a) fixed V_{BE} (b) varied V_{BE} to make IC in 100° C the same as that in 25° C

2.2.2. Effect of Temperature on SOA.

Dominated by thermal runaway, DC and microsecond SOAs usually shrink with increasing ambient temperature. However, under sub-nanosecond pulses, the SOA actually expands with increasing ambient temperature thereby confirming that it is limited by avalanche breakdown instead of thermal runaway. Fig. 2-7 (a) shows such dependence between 25°C and 100°C under the same V_{BE} . It can be seen that in both cases, below 80 mA the collector current increases with increasing temperature due to increased thermionic emission. However, above 80 mA the collector current decreases

with increasing temperature due to decreased carrier velocity, which aggravates the Kirk effect [6]. The decreased carrier velocity also retards breakdown and expands SOA. Fig. 2-7 (b) shows the voltage where the flyback happens is delayed in high temperature. This confirms that the flyback is introduced by the impact ionization. The V_{BE} here is adjusted on purpose to make I_C in high temperature the same as that in room temperature in order to compare the flyback voltage easily.

2.2.3. Effects of Pulse Width and Quiescent Bias on SOA

Fig. 2-8 shows that when the pulse width is increased from 0.2 ns to 1.0 ns, flyback sharpens and the SOA shrinks, although the HBT remains isothermal under both 0.2-ns and 1.0-ns pulses. This is because in a common-emitter configuration the avalanche breakdown current is a product of the transport factor across the base and the electron multiplication factor across the collector. While the time constant for electron multiplication is on the order of picoseconds, the time constant for base diffusion is on the order of nanoseconds. Therefore, while the impact multiplication across the collector at 1.0 ns is comparable to that at 0.2 ns, the transport factor across the base is higher at 1 ns than that at 0.2 ns. This shows that the sub-nanosecond pulse measurement can be a powerful technique to characterize not only the breakdown in the collector, but also the

transport in the base.

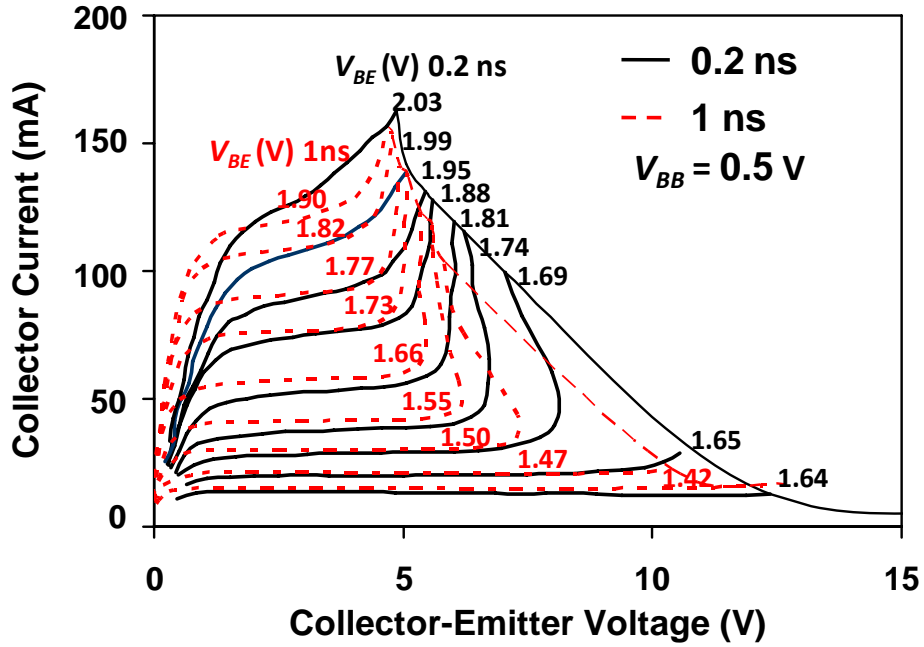


Fig. 2-8 Sub-nanosecond pulse characteristics under different pulse widths.

Fig. 2-9 shows that the 0.2-ns pulse characteristics change little when the quiescent bias V_{BB} is increased from 0.5 V to 1.2 V, which is still below the turn-on voltage of 1.3 V and without self heating. However, the SOA shrinks by approximately the difference in V_{BB} , which is $1.2 \text{ V} - 0.5 \text{ V} = 0.7 \text{ V}$.

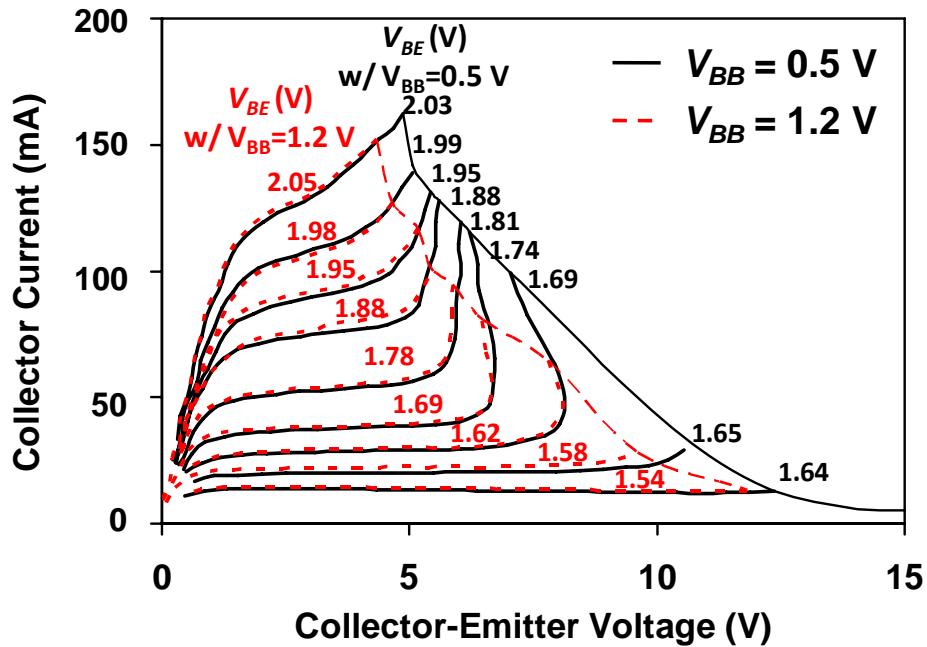


Fig. 2-9 Sub-nanosecond pulse characteristics under different quiescent base biases. The pulse amplitude is adjusted to give the same V_{BE} in both cases.

Again, although not shown, these effects of pulse width and quiescent bias were well captured by the modified HBT model later. Also, although all the impact-ionization model parameters were extracted from the 0.2 ns/0.5 V characteristics, they could just as well be extracted from the 1.0 ns or 1.2 V characteristics without significant differences.

2.3. Fly-forward characteristic in the Pulse I-V curves

Transistors characterized in this work are $90 \mu\text{m}^2$ InGaP/GaAs HBTs from TriQuint Semiconductor Inc.. By using the same set-up as that in the first section of this chapter, devices are characterized by stepping V_{CE} and keeping V_{BE} constant. As shown in Fig.

2-10, at the end of the each curve, current increases sharply due to the impact ionization. In some curves, the impact ionization is so strong that even the collector voltage is decreasing. Different from previous work in the second chapter, we found that the impact ionization is attenuated at a certain current level where voltage stops decreasing. Furthermore, a fly-forward appears after that.

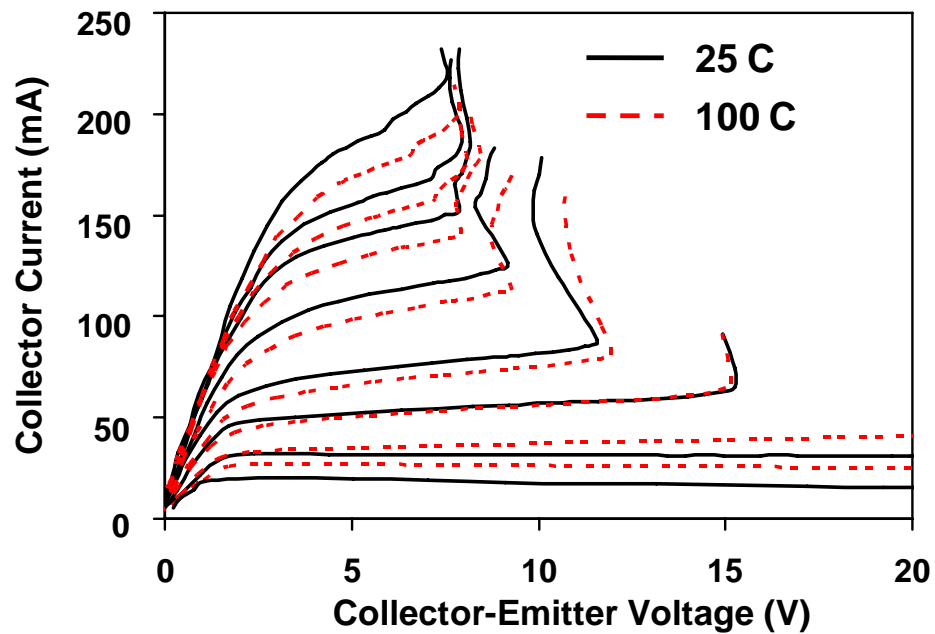


Fig. 2-10 Fly-forward characteristic under different temperature

Before investigating the fly-forward characteristic, we have to figure out how impact ionization introduces the flyback in the $I-V$ curve: when base-collector junction is under high reverse bias, electron-hole pairs are generated in the depletion region of the collector due to impact ionization. Electron will go towards the sub-collector while holes will fly

into the base by the electric field force and become a part of the base current. If we assume the device forward current gain remains the same, then the current will increase due to the additional base current, which means more electrons are swept into the depletion region of collector and impact ionization becomes worse. Sometimes this positive feedback is so strong that large reverse voltage on the base-collector is no longer necessary to give large impact ionization current. So the collector voltage decreases and the flyback appears. In some devices, collector contact resistance is high and epitaxial layer of the collector is thick and lightly doped, so their collector resistance is very large. When collector current becomes large, the resistive voltage drop will be significant, so the final voltage drop on the collector depletion region will be small and will further decrease with the collector current. If this effect overcomes the previous positive feedback, then fly-forward will appear.

To prove the speculation on the fly-forward, collector resistor is extracted by using the hot HBT method [7][8][9]. This is performed by forcing high current through base terminal while leaving collector terminal open. Under this condition both base-emitter and base-collector junctions become forward-biased. This makes differential impedance of both junctions very small. So the collector resistance can be extracted by:

$$R_C = \text{Re}(Z_{22} - Z_{12}) \quad (2-3)$$

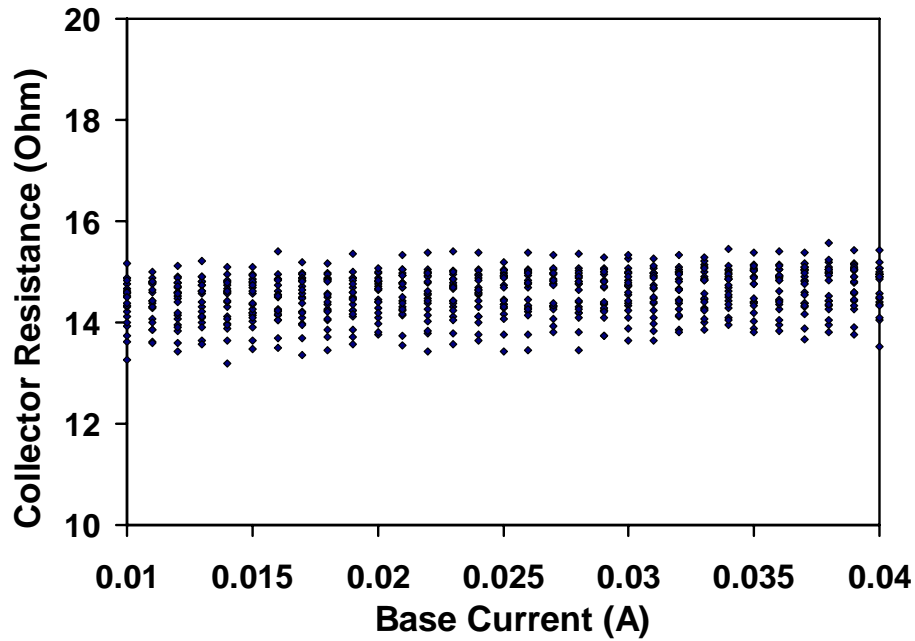


Fig. 2-11 Collector Resistance extracted by using Hot HBT method

The average R_C value extracted by using Hot HBT method is $15.2 \ \Omega$ according to Fig. 2-11. Then the real voltage drop on the base-collector junction is calculated by using: $V'_{CE} = V_{CE} - R_C \cdot I_C$. In Fig. 2-12, we plot the collector current vs. real reverse bias voltage on the collector-emitter junction and find that I - V curves do not fly forward again. So the significant resistance voltage drop on the collector is the main reason of the fly forward characteristic.

Previous researchers have observed the collector current saturation due to quasi-saturation effect [10]: base-collector junction is slightly forward biased because of

the additional resistive voltage drop on the collector. However, the base-collector junction is not necessarily in the forward biased condition to see the fly-forward.

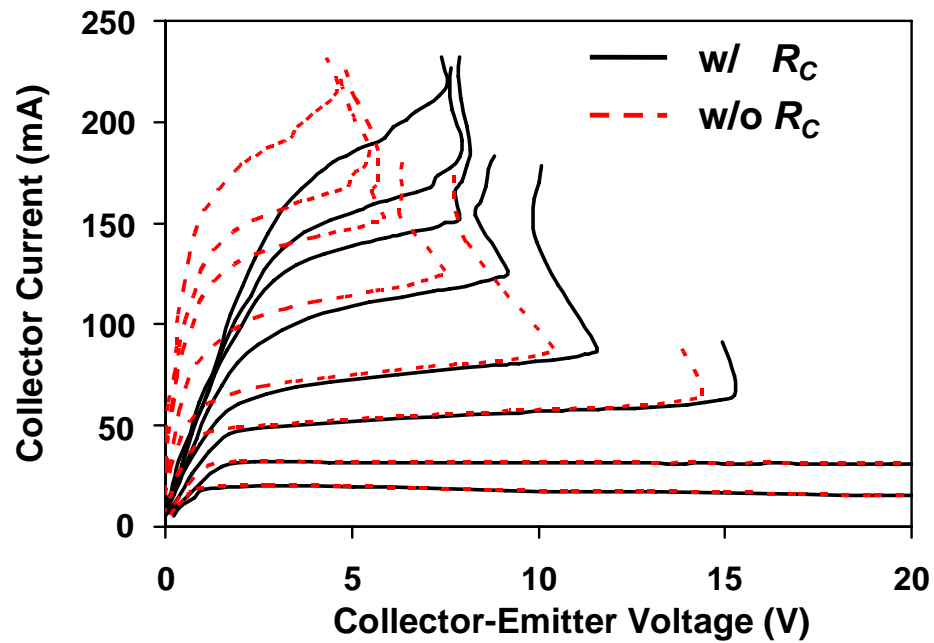


Fig. 2-12 Sub-nanosecond pulse I-V curve before and after the elimination of collector resistance

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Chapter 3 Modified HBT model

Without self heating, high-voltage and high-current device characteristics are mainly governed by impact-ionization and Kirk effects. As shown in Fig. 2-6(a), the gradual increase of the collector current beyond the knee voltage is mainly due to the Kirk effect, whereas the sharp turn up of the collector current beyond the flyback voltage is mainly due to impact ionization.

The industry standard compact BJT models are GP[1], VBIC[2], HICUM[3], MEXTRAM[4], UCSD[5] and Agilent HBT [6]. Most of these models can predict the high current effects, including quasi-saturation and Kirk effect except for GP model. However, the avalanche breakdown models still need improvement to predict the pulse mode I-V curve. The base-collector junction avalanche current equations used in VBIC and HICUM are restricted to model the avalanche effect at low current densities (weak avalanche). Contrary to this, in MEXTRAM a much more complicated avalanche model is used. It is able to calculate both the weak and the high current avalanche effect. UCSD model uses a well-known expression to calculate the multiplication factor inside the base-collector junction. It may be switched on as an optional feature in both MEXTRAM and UCSD model, because the avalanche model will degrade the convergence behavior

of the model.

SGP	N/A
VBIC	$I_{GC} = (I_{TXF} - I_{TZR} - I_{BCJ}) \cdot AVC1 \cdot vI \cdot \exp(-AVC2 \cdot vI^{MC-1})$
HICUM	$I_{AVL} = FAVL \cdot I_{TF} \cdot (VDCI - U_{B'C'}) \exp\left[-\frac{QAVL}{C_{JCI} (VDCI - U_{B'C'})}\right]$
MEXTRAM	$I_{AVL} = I_{C1C2} \frac{G_{EM} \cdot G_{MAX}}{G_{EM} \cdot G_{MAX} + G_{EM} + G_{MAX}}$
UCSD	$I_{AVL} = I_C \frac{1}{1 - (V_{CB}/BV_{CBO})^{NBC}}$
Agilent	N/A

Table 3-1 Base-collector avalanche current in different compact models.

3.1. Numerical Calculation of Multiplication factor

The electron multiplication factor M is a function of not only the collector-base voltage V_{CB} , but also the collector current I_C . This is because I_C perturbs the distribution of space charge and, in turn, the distribution of electric field and carrier velocity in the collector. Since the current and field closely influence each other, complicated integration formula have been developed [7] such as

$$1 - \frac{1}{M} = \int_{X_{TH}}^{X_{DEP}} \left\{ \alpha_E[\varepsilon(x)] \exp\left(-\int_{X_{TH}}^x \{\alpha_E[\varepsilon(x')] - \alpha_H[\varepsilon(x')]\} dx'\right) \right\} dx \cdot \exp\left\{ \int_0^{X_{TH}} \alpha_H[\varepsilon(x)] dx \right\} \quad (3-1)$$

where x is the distance measured from the base into the collector, $\varepsilon(x)$ is the field

distribution in the collector, X_C and X_{DEP} are the physical width and depletion width of the collector, X_{TH} is the dead space where electrons must drift through to acquire the threshold energy E_{TH} for impact ionization, and α_E and α_H are electron and hole ionization coefficients. For GaAs,

$$E_{TH} = q \int_0^{X_{TH}} \varepsilon(x) dx = 1.7 \text{ eV} \quad (3-2)$$

$$\alpha_E [\varepsilon(x)] = 1.899 \times 10^5 \exp \left\{ - \left[\frac{5.75 \times 10^5}{\varepsilon(x)} \right]^{1.82} \right\} \text{ cm}^{-1} \quad (3-3)$$

$$\alpha_H [\varepsilon(x)] = 2.215 \times 10^5 \exp \left\{ - \left[\frac{6.57 \times 10^5}{\varepsilon(x)} \right]^{1.75} \right\} \text{ cm}^{-1} \quad (3-4)$$

where q is the electron charge. For the present HBTs, $X_C \approx 1 \text{ } \mu\text{m}$.

To account for field reversal under the Kirk effect, we modified Eqn. (3-1) and Eqn. (3-2) as in the following

$$1 - \frac{1}{M} = \int_{X_C - X_{DEP} + X_{TH}}^{X_C} \left\{ \alpha_E [\varepsilon(x)] \exp \left(- \int_{X_C - X_{DEP} + X_{TH}}^x \{ \alpha_E [\varepsilon(x')] - \alpha_H [\varepsilon(x')] \} dx' \right) \right\} dx \cdot \exp \left\{ \int_{X_C - X_{DEP}}^{X_C - X_{DEP} + X_{TH}} \alpha_H [\varepsilon(x)] dx \right\} \quad (3-5)$$

$$E_{TH} = q \int_{X_C - X_{DEP}}^{X_C - X_{DEP} + X_{TH}} \varepsilon(x) dx = 1.7 \text{ eV} \quad (3-6)$$

Fig. 3-1 shows the constant M contours according to Eqn. (3-1)-(3-6). It can be seen that

under a V_{CB} between 15 V and 25 V, M first decreases then increases with increasing I_C . Below 15 V, there is no significant impact ionization when the current is less than 20 mA. Above 25 V, M exceeds 1.3 for all currents. The current I_1 when M reaches the minimum corresponds to the threshold current that introduces sufficient space charge in the collector to neutralize the depletion region and to reverse the field there [7]. Accordingly

$$I_1 = A_E N_C q v_{SAT} \quad (3-7)$$

where N_C is the collector doping concentration and v_{SAT} is the saturated electron velocity.

For the present HBTs, $N_C \approx 2 \times 10^{16} \text{ cm}^{-3}$ and $v_{SAT} \approx 8 \times 10^6 \text{ cm/s}$. Therefore, $I_1 \approx 10 \text{ mA}$.

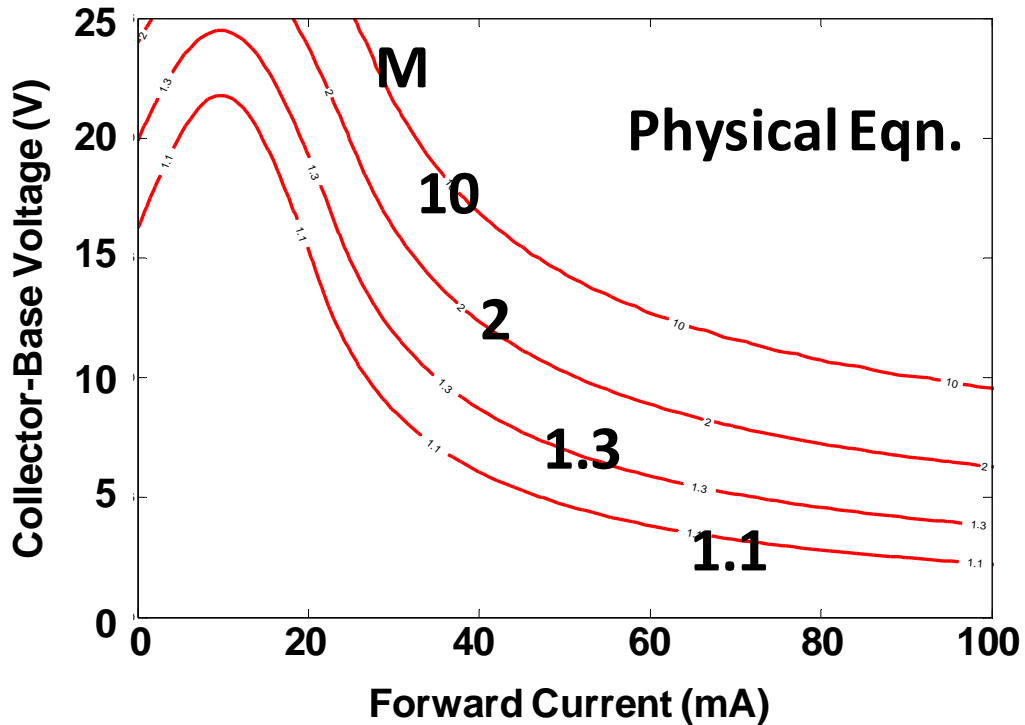


Fig. 3-1 Modeled electron multiplication factors by using physical equations.

However, the numerical calculation is not suitable to compact transistor model. Eqn.

(3-1) and Eqn. (3-5) needs to be simplified. In the low to medium electrical field region, the electron and hole impact ionization rate is close to each other. So the first exponential term in Eqn. (3-1) is assumed to be unity. Then Eqn. (3-1) can be written in the following:

$$1 - \frac{1}{M} = \int_{X_{TH}}^{X_{DEP}} \{\alpha_E[\varepsilon(x)]\} dx \cdot \exp \left\{ \int_0^{X_{TH}} \alpha_H[\varepsilon(x)] dx \right\} \quad (3-8)$$

If we assume the thickness of dead space (X_{TH}) is much smaller than the whole collector width, Eqn. (3-8) can be simplified as:

$$1 - \frac{1}{M} = \int_0^{X_{DEP}} \{\alpha_E[\varepsilon(x)]\} dx \quad (3-9)$$

We use the electron impact ionization rate by Eqn. (3-3), then integrate by substituting the original variable x with electrical field E inside the collector.

$$\begin{aligned} 1 - \frac{1}{M} &= \int_0^{X_{DEP}} 1.899 \times 10^5 \exp \left[- \left(\frac{5.75 \times 10^5}{E(x)} \right)^{1.82} \right] dx \\ &= \left[\frac{1.899 \times 10^5}{-\frac{q}{\varepsilon} \left(N_C - \frac{J_F}{q \cdot v_{SAT}} \right)} \right] \int_{E_1}^{E_2} \exp \left(- \left(\frac{5.75 \times 10^5}{E} \right)^{1.82} \right) dE \end{aligned} \quad (3-10)$$

The resulting integral can be further computed by using integration by parts and eliminating the second term.

$$\begin{aligned}
\int_{E_1}^{E_2} \exp\left[-\left(\frac{5.75 \times 10^5}{E}\right)^{1.82}\right] dE &= \exp\left[-\left(\frac{5.75 \times 10^5}{E_2}\right)^{1.82}\right] \cdot E_2 - \exp\left[-\left(\frac{5.75 \times 10^5}{E_1}\right)^{1.82}\right] \cdot E_1 \\
&- \int_{E_1}^{E_2} \frac{\exp\left[-\left(\frac{5.75 \times 10^5}{E}\right)^{1.82}\right] \cdot (5.75 \times 10^5)^{1.82}}{E^{1.82}} dE \\
&\approx \exp\left[-\left(\frac{5.75 \times 10^5}{E_2}\right)^{1.82}\right] \cdot E_2 - \exp\left[-\left(\frac{5.75 \times 10^5}{E_1}\right)^{1.82}\right] \cdot E_1
\end{aligned} \tag{3-11}$$

Eqn. (3-5) is simplified in a similar way. Finally, M is in the following form:

$$1 - \frac{1}{M} \approx \frac{1.899 \times 10^5}{-\frac{q}{\varepsilon} \left(N_C - \frac{J_F}{q \cdot v_{SAT}}\right)} \left\{ \exp\left[-\left(\frac{5.75 \times 10^5}{E_2}\right)^{1.82}\right] \cdot E_2 - \exp\left[-\left(\frac{5.75 \times 10^5}{E_1}\right)^{1.82}\right] \cdot E_1 \right\}$$

$$\left\{ \begin{aligned}
&E_1 = \sqrt{\frac{2q}{\varepsilon} \left|N_C - \frac{J_C}{q \cdot v_{SAT}}\right| (V_{CB} + \varphi_{CB})}, E_2 = 0 \\
&\quad \text{when } \frac{q \cdot X_C^2}{2\varepsilon} \left|N_C - \frac{J_C}{q \cdot v_{SAT}}\right| \geq V_{CB} + \varphi_{CB} \\
&E_1 = \frac{V_{CB} + \varphi_{CB}}{X_C} + \frac{q \cdot X_C}{2\varepsilon} \left|N_C - \frac{J_C}{q \cdot v_{SAT}}\right|, E_2 = E_1 - \frac{q}{\varepsilon} \left|N_C - \frac{J_C}{q \cdot v_{SAT}}\right| \cdot X_C \\
&\quad \text{when } \frac{q \cdot X_C^2}{2\varepsilon} \left|N_C - \frac{J_C}{q \cdot v_{SAT}}\right| < V_{CB} + \varphi_{CB}
\end{aligned} \right. \tag{3-12}$$

Fig. 3-2 shows the constant M contours according to Eqn. (3-12). M from the new equation is a little bit smaller than that from Eqn. (3-5) due to the elimination of the second term in Eqn. (3-11), although the contour shape is generally agreed with that from the numerical equations. Another drawback is that the piecewise function is still too

complicated to the compact model.

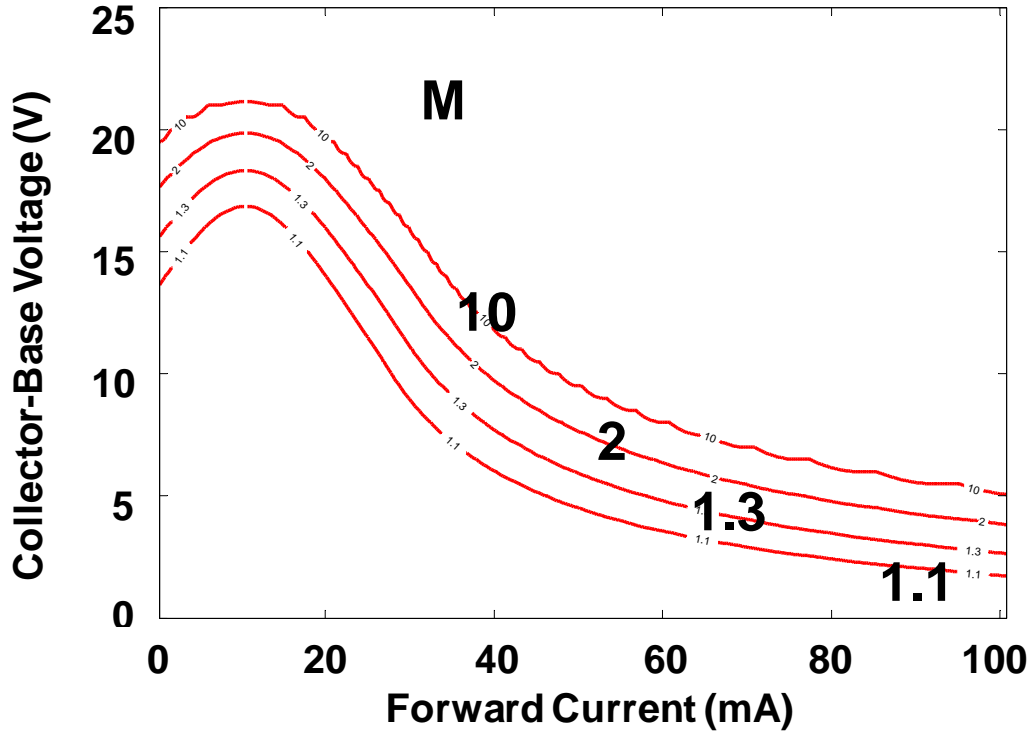


Fig. 3-2 Modeled electron multiplication factors by using simplified analytical equations.

3.2. Proposed multiplication factor model

Since Eqn. (3-1)-(3-6) are too complicated for compact modeling, a simple empirical alternative has been proposed [8]

$$M = 1 + m \tan \left[\frac{\pi}{2} \left(\frac{V_{CB}}{BV_{CBO}} \right)^n \exp \left(-\frac{I_C}{I_0} \right) \right] \quad (3-13)$$

where m , n and I_0 are fitting parameters. However, Eqn. (3-13) decreases monotonically with increasing I_C and fails to allow M to increase after field reversal. To correct this deficiency, we propose a new empirical equation

$$M_0 = 1 + m \tan \left[\frac{\pi}{2} \left(\frac{V_{CB}}{BV_{CBO}} \right)^n \right] \cosh \left[\frac{(I_F - I_1)V_{CBI}}{P} \right] \quad (3-14)$$

where I_F is the forward collector current, V_{CBI} is the internal collector-base voltage after accounting for voltage drops across the external base and collector resistors, and m , n and p are fitting parameters. Compared to Eqn. (3-13), Eqn. (3-14) uses a hyperbolic-cosine function to allow M_0 to both decrease and increase with the collector current. For the present HBT, $m = 0.06$, $n = 3$, and $p = 0.08$ W. Fig. 3-3 shows that Eqn. (3-5) and Eqn. (3-14) agree quite well.

In addition, M is made to depend on temperature as

$$M(T) = M_0 \cdot (T_0/T)^{a - I_F/I_0} \quad (3-15)$$

where T is the junction temperature, $T_0 = 300$ K is the ambient temperature, and a and I_T are fitting parameters. For the present HBTs, $a = 2.2$ and $I_0 = 0.2$ A. This temperature dependence gives reasonable fit to the measured data as shown in Fig. 3-5.

Once M is properly modeled, the collector characteristics can be obtained by

$$I_C = I'_{BC} + MI_F; \quad V_{CE} = V_{CB} + V_{BE} \quad (3-16)$$

where I'_{BC} is the base-collector diffusion current.

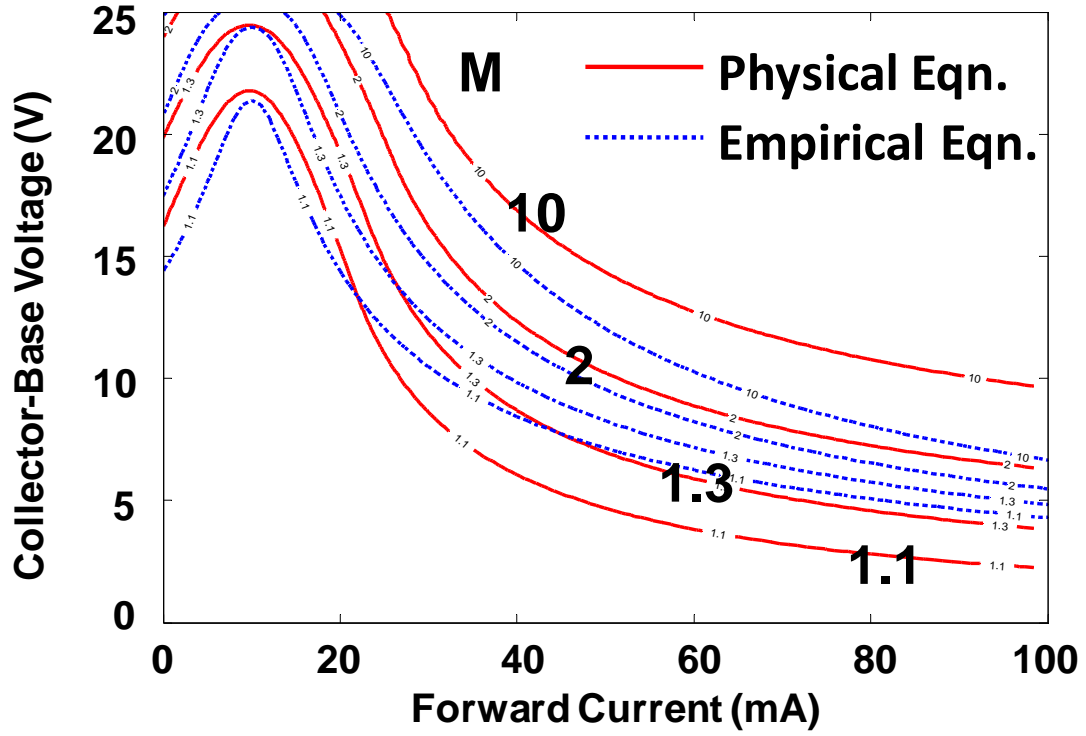
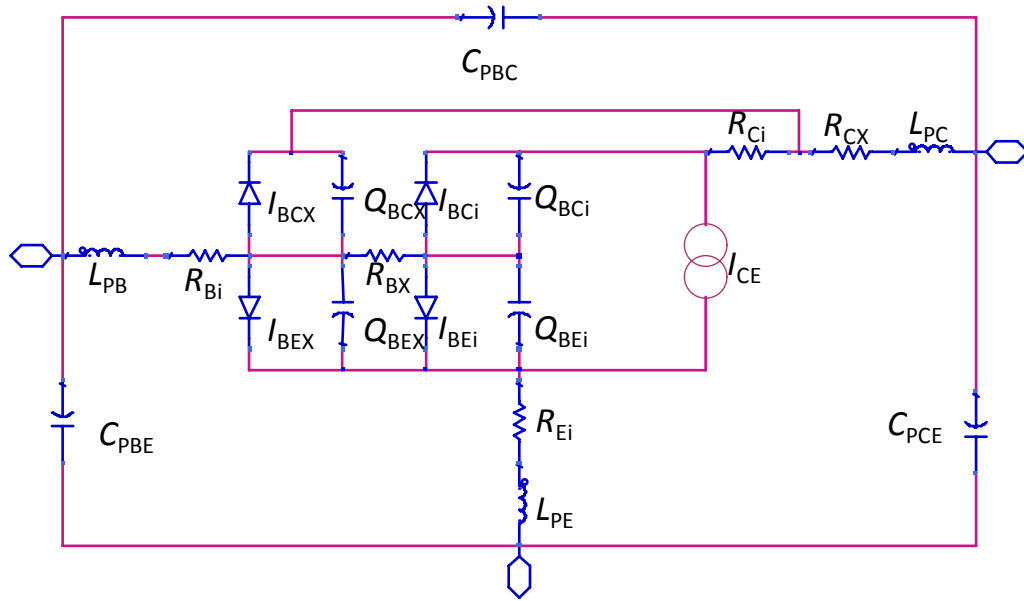


Fig. 3-3 Modeled electron multiplication factors by using physical and empirical equations, respectively.

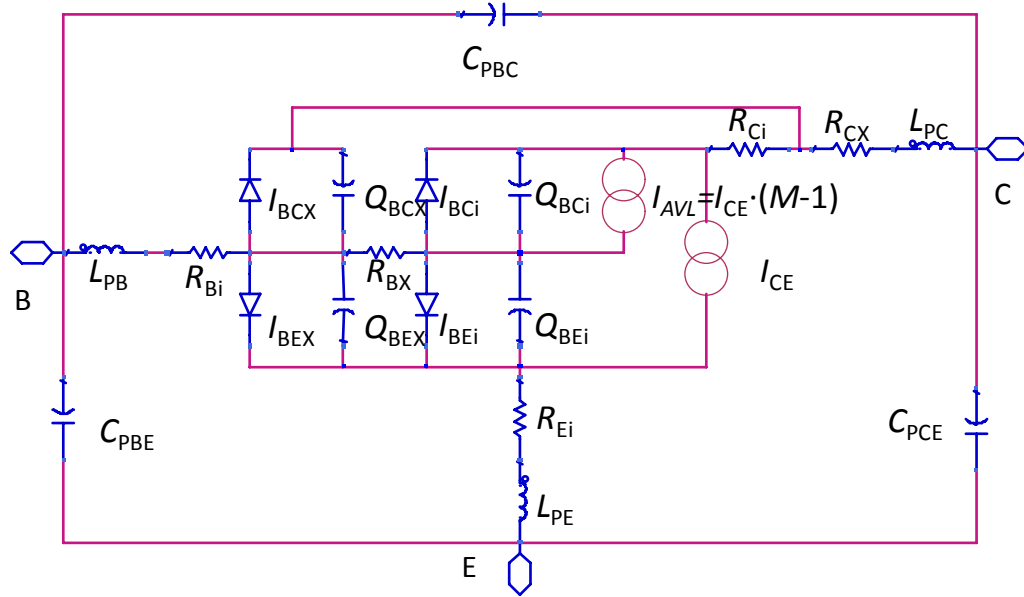
The original Agilent HBT model [6] is plotted in Fig. 3-4(a) and the modified model is plotted in Fig. 3-4(b). Compared with the original model, the new model has an additional current source which represents the impact ionization current. The impedances of the whole network are modified by adding this new branch. For this branch:

$$I_{AVL} = I_F (M - 1) \quad (3-17)$$

where M is from Eqn. (3-15).



(a)



(b)

Fig. 3-4 (a) Original Agilent HBT model (b) Modified Agilent HBT model with additional impact ionization current source

The voltage controlled current source (I_{CE}) (from Eqn. (3-18) to (3-30)) and four diodes (from Eqn. (3-31) to Eqn. (3-34)) including internal base-emitter (I_{BEi}), internal base-collector (I_{BCi}), external base-emitter (I_{BEX}) and external base-collector (I_{BCX}) junctions remain the same as those in original Agilent HBT. Their current values are decided by the voltage drop across the diode. The introduction of the new impact ionization current will change the voltage drop across both the base-collector and base-emitter junctions. So the transconductance of those four branches is different from those in Fig. 3-4 (a) without the impact ionization current. Furthermore, Eqn. (3-35) to Eqn. (3-59) for four charge sources across internal base-emitter (Q_{BEi}), internal base-collector (Q_{BCi}), external base-emitter (Q_{BEX}) and external base-collector (Q_{BCX}) junctions are functions of voltage drop across base-emitter and base-collector. So the capacitance values of those four branches are also different due to the new current source. All the above reasons bring the differences in the waveform, small signal and large signal simulation.

Those key equations for the voltage controlled current source, four junction diodes and four charge sources are listed below.

The collector-emitter current equations are:

$$I_{CE} = I_{cf} - I_{cr} \quad (3-18)$$

$$I_{cf} = \frac{IS \times \left(\exp\left(\frac{qV_{BEi}}{NF \times k \times T}\right) - 1 \right)}{DD \times q3 \text{ mod}} \quad (3-19)$$

$$I_{cr} = \frac{ISR \times \left(\exp\left(\frac{qV_{BCi}}{NR \times k \times T}\right) - 1 \right)}{DD} \quad (3-20)$$

where

$$DD = qb + Ica + Icb \quad (3-21)$$

$$qb = \frac{q1 \times (1 + \sqrt{1 + 4 \times q2})}{2} \quad (3-22)$$

$$q1 = \frac{1}{1 - \frac{V_{BEi}}{VAR} + \frac{V_{BCi}}{VAF}} \quad (3-23)$$

$$q2 = \frac{IS \exp\left(\frac{qV_{BEi}}{NF \times k \times T}\right)}{IK} \quad (3-24)$$

$$Ica = \frac{IS}{ISA} \exp\left(\frac{qV_{BEi}}{NA \times k \times T}\right) \quad (3-25)$$

$$Icb = \frac{IS}{ISB} \exp\left(\frac{qV_{BCi}}{NB \times k \times T}\right) \quad (3-26)$$

$$q3 \text{ mod} = \frac{NKDC \times q3}{(NKDC - 1) + q3} \quad (3-27)$$

$$q3 = \text{trans2} \left(IS \left(\exp\left(\frac{qV_{BEi}}{NF \times k \times T}\right) - 1 \right) \right) - \text{trans}(0) + 1 \quad (3-28)$$

$$\text{trans2}(I) = \frac{IKDC2 \text{Inv} \left(\sqrt{(I - Icrit1)^2 + IKDC1^2} + I - Icrit1 - IKDC1 \right)}{2} \quad (3-29)$$

$$Icrit1 = IKDC3 \left(1 - (V_{BCi} - VJC) \times VKDC \text{Inv} \right) \quad (3-30)$$

In equations, IS is the forward collector saturation current, V_{BEi} is the voltage drop across the internal base-emitter junction, k is the Boltzmann constant, T is the junction temperature, NF is the forward collector current ideality factor, ISR is the reverse emitter saturation current, NR is the reverse emitter current ideality factor, V_{BCi} is the voltage drop across the internal base-collector junction, VAR is the forward early voltage, VAF is the reverse early voltage, IK is the high injection roll off current, ISA is the base-emitter heterojunction saturation current, NA is the base-emitter heterojunction ideality factor, NB is the base-collector heterojunction ideality factor, ISB is the base-collector heterojunction saturation current, $NKDC$ is the maximum value of $q3$, $IKDC1$ is the slope of $q3$ function, $IKDC3$ is the I - V knee effect critical current, VJC is the built-in voltage across the base-collector junction, and $VKDCInv$ is the transition width of base-collector voltage for the knee effect.

Base-emitter and base-collector current equations are:

$$I_{BEi} = (1 - ABEL) \times \left(\begin{array}{l} (q3 \text{ mod})^{GKDC} \times ISH \left(\exp \left(\frac{qV_{BEi}}{NH \times k \times T} \right) - 1 \right) \\ + ISE \left(\exp \left(\frac{qV_{BEi}}{NE \times k \times T} \right) - 1 \right) \end{array} \right) \quad (3-31)$$

$$I_{BEc} = (ABEL) \times \left(\begin{array}{l} (q3 \text{ mod})^{GKDC} \times ISH \left(\exp \left(\frac{qV_{BEc}}{NH \times k \times T} \right) - 1 \right) \\ + ISE \left(\exp \left(\frac{qV_{BEc}}{NE \times k \times T} \right) - 1 \right) \end{array} \right) \quad (3-32)$$

$$I_{BCi} = (1 - ABCX) \times \left(\begin{array}{l} ISRH \left(\exp \left(\frac{qV_{BCi}}{NRH \times k \times T} \right) - 1 \right) \\ + ISC \left(\exp \left(\frac{qV_{BCi}}{NC \times k \times T} \right) - 1 \right) \end{array} \right) \quad (3-33)$$

$$I_{BCx} = ABCX \times \left(\begin{array}{l} ISRH \left(\exp \left(\frac{qV_{BCx}}{NRH \times k \times T} \right) - 1 \right) \\ + ISC \left(\exp \left(\frac{qV_{BCx}}{NC \times k \times T} \right) - 1 \right) \end{array} \right) \quad (3-34)$$

where $ABEL$ is the ratio of base-emitter current allocated to extrinsic region, $GKDC$ is the exponent of $q3$ factor in the base current, ISH is the ideal base-emitter saturation current, NH is the ideal base-emitter current ideality factor, ISE is the non-ideal base-emitter saturation current, NE is the non-ideal base-emitter current ideality factor, $ABCX$ is the ratio between extrinsic and total base-collector regions, $ISRH$ is the ideal base-collector saturation current, ISC is the non-ideal base-collector saturation current, NRH is the ideal base-collector current ideality factor, and NC is the non-ideal base-collector current ideality factor.

The charge source model contains two parts: depletion charge and delay charge. Because the same depletion charge functions are used for the base-emitter and base-collector charges, the following equations apply to both junctions. The variable x is used to denote either base-collector (C) or base-emitter (E).

$$Q_{xd}(V_x) = Q_{jxf} + Q_{jxm} + Q_{jxr} - Q_{jxcorr} \quad (3-35)$$

The depletion capacitance C_{xd} can be derived in a straightforward manner (in concept) by taking the derivative of the total depletion charge (Q_{xd}) with respect to V_x , given by the expression:

$$C_{xd}(V_x) = \frac{dQ_{xd}}{dV_x} = \frac{dQ_{jxf}}{dV_x} + \frac{dQ_{jxm}}{dV_x} + \frac{dQ_{jxr}}{dV_x} - \frac{dQ_{jxcorr}}{dV_x} \quad (3-36)$$

The derivatives of each of the four terms are provided:

$$\frac{dQ_{jxf}}{dV_x} = CxMAX \left(1 - \frac{d(v_{jxr})}{dV_x} \right) \quad (3-37)$$

$$\frac{dQ_{jxm}}{dV_x} = CJx \left(1 - \frac{V_{jxm}}{VJx} \right)^{-MJx} \times \frac{d(V_{jxm})}{dV_x} \quad (3-38)$$

$$\frac{dQ_{jxr}}{dV_x} = C_{jx0r} \left(1 - \frac{v_{jxr}}{VJx} \right)^{-MJxR} \times \frac{d(v_{jxr})}{dV_x} \quad (3-39)$$

$$\frac{dQ_{jxcorr}}{dV_x} = C_{jx0r} \left(1 - \frac{v_{jxm}}{VJx} \right)^{-MJxR} \times \frac{d(v_{jxm})}{dV_x} \quad (3-40)$$

where

$$v_{jxm} = \frac{1}{2} \left(v_{jxr} - V_{jPxi} + \sqrt{(V_{jPxi} + v_{jxr})^2 + V_r^2} \right) \quad (3-41)$$

$$V_r = 0.1V_{jPxi} + 4 \left(\frac{k \times T}{q} \right) \quad (3-42)$$

$$V_{jPxi} = VPT_x - VJ_x \quad (3-43)$$

$$v_{jxr} = -0.5 \left(-V_x - V_{fxi} + \sqrt{(V_{fxi} - V_x)^2 + \left(\frac{k \times T}{q} \right)^2} \right) \quad (3-44)$$

$$V_{fxi} = VJx \left[1 - \left(\frac{CxMAX}{CJx} \right)^{-(1/MJx)} \right] \quad (3-45)$$

$$C_{jx0r} = CJx \left(\frac{VJx}{VPTx} \right)^{1-Mx} \quad (3-46)$$

$$\frac{d(v_{jxr})}{dV_x} = \frac{1}{2} \left(1 - \frac{V_x - V_{fxi}}{\sqrt{(V_x - V_{fxi})^2 + \left(\frac{k \times T}{q} \right)^2}} \right) \quad (3-47)$$

$$\frac{d(v_{jxm})}{dV_x} = \frac{d(v_{jxr})}{dV_x} \times \frac{1}{2} \left(1 + \frac{V_{jPxi} + V_{jxr}}{\sqrt{(V_{jPxi} - v_{jxr})^2 + V_r^2}} \right) \quad (3-48)$$

In the equations above, the variable x is used to denote either base-collector (C) or base-emitter (E). $CxMAX$ is the maximum value of the base-collector (base-emitter) capacitance in forward bias, CJx is the zero-bias base-collector (base-emitter) capacitance, $VPTx$ is the punch-through voltage base-collector (base-emitter) capacitance, VJx is the built-in voltage of base-collector (base-emitter) capacitance, CJx is the zero-bias base-collector (base-emitter) capacitance, and MJx is the grading factor of base-collector (base-emitter) capacitance.

The delay charge equations account for the intrinsic delay of the device. They are grouped into three separate components: base delay charge (Q_{tB}), Kirk effect charge (Q_{krk}), which will be discussed in the next section, and collector delay charge (Q_{tC}).

$$\frac{dQ_{tB}}{dI_{cfq}} = TFB \quad (3-49)$$

$$\left. \frac{\partial Q_{TC}}{\partial I_{cfq}} \right|_{V_{BCi}} = \left(\begin{array}{l} (TFC0(1-VTC0Inv \times trans3(V_{BCi}, VTR0, VMX0))) \\ + 2 \times TCMIN(1-VTCMINInv \times trans3(V_{BCi}, VTRMIN, VMXMIN)) \\ - \frac{TFC0(1-VTC0Inv \times trans3(V_{BCi}, VTR0, VTR0, VMX0)) \times (I_{cfq} - ITC(1-V_{BCi} \times VTCInv))}{\sqrt{(ITC(1-V_{BCi} \times VTCInv) - I_{cfq})^2 + (ITC2(1-V_{BCi} \times VTC2INV))^2}} \end{array} \right) \quad (3-50)$$

$$trans3(x, x_{ir}, x_{max}) = \frac{\sqrt{(x + x_{max})^2 + x_{tr}^2} + x - x_{max}}{2} \quad (3-51)$$

$$I_{cfq} = IS \exp\left(\frac{qV_{BEi}}{k \times T}\right) \quad (3-52)$$

where TFB is the intrinsic base transit time, $TFC0$ is the low current transit time, $VTC0Inv$ is the rate of change of $TFC0$ with V_{CB} , $VTR0$ is the transition width in V_{CB} to $VMX0$, $VMX0$ is the maximum V_{CB} for $TFC0$, $TCMIN$ is the high current transit time, $VTCMINInv$ is the rate of change of $TCMIN$ with V_{CB} , $VMXMIN$ is the maximum V_{CB} for $TCMIN$, $VTRMIN$ is the transition width in V_{CB} to $VMXMIN$, $VTR0$ is the transition width in V_{CB} to $VMX0$, ITC is the midpoint in I_{CE} between $TFC0$ and $TCMIN$, $VTCInv$ is the rate of change of ITC with V_{CB} , $ITC2$ is the width in I_{CE} between $TFC0$ and $TCMIN$, and $VTC2INV$ is the rate of change of $TFC0$ with V_{CB} .

A very simple reverse delay charge is implemented by a constant reverse transit time parameter TR . The charge associated with this delay is equal to:

$$Q_{tR} = TR \times I_{crq} \quad (3-53)$$

Implementations of the base-emitter depletion charge (Q_{Bed}) and the base-collector depletion charge (Q_{BCd}) are straightforward because they solely reside between the base-emitter and base-collector junctions, respectively. Partitioning between the intrinsic and extrinsic portions of the device is accomplished by the parameters $ABEX$ and $ABCX$. Therefore, the intrinsic depletion charges are defined as:

$$Q_{BEid} = (1 - ABEX) \times Q_{Bed} (V_{BEi}) \quad (3-54)$$

$$Q_{BCid} = (1 - ABCX) \times Q_{BCd} (V_{BCi}) \quad (3-55)$$

and in turn, the extrinsic depletion charges are defined as:

$$Q_{BEe} = Q_{BEed} = (ABEX) \times Q_{Bed} (V_{BEe}) \quad (3-56)$$

$$Q_{BCe} = Q_{BCed} = (ABCX) \times Q_{BCd} (V_{BCe}) \quad (3-57)$$

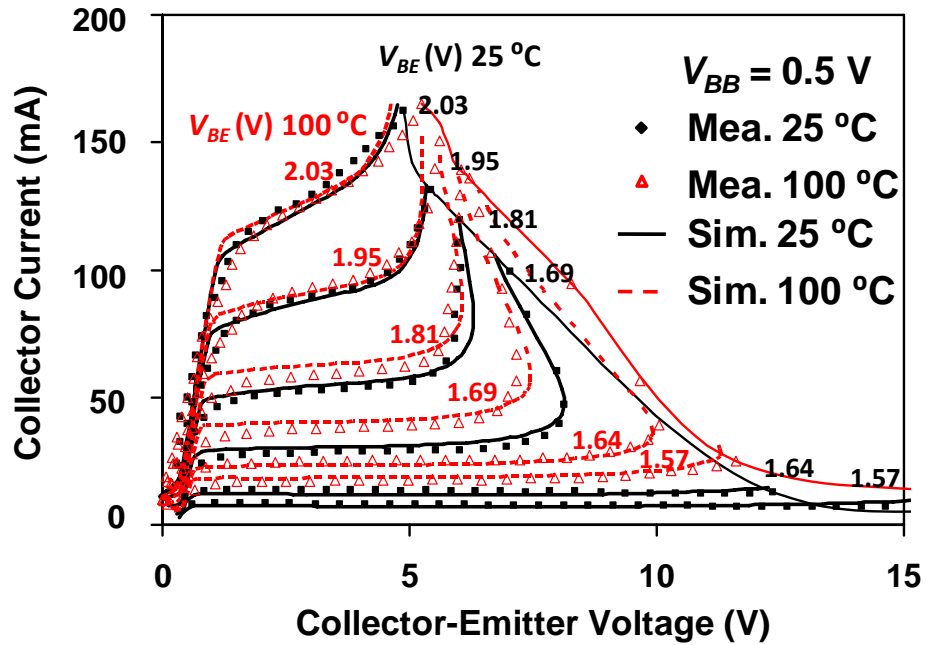
The delay charges (Q_{tB} , Q_{tC} and Q_{krk}) reside only in the intrinsic region of the device (because they physically represent the time it takes for electrons to traverse the intrinsic base region and the intrinsic portion of the collector depletion region). These delay charges can be independently partitioned between the base-emitter and base-collector

junctions by the partitioning factors $FEXTB$, $FEXTC$, and $FEXKE$. These partitioning factors play an important role in defining the phase characteristics of the device at high frequencies.

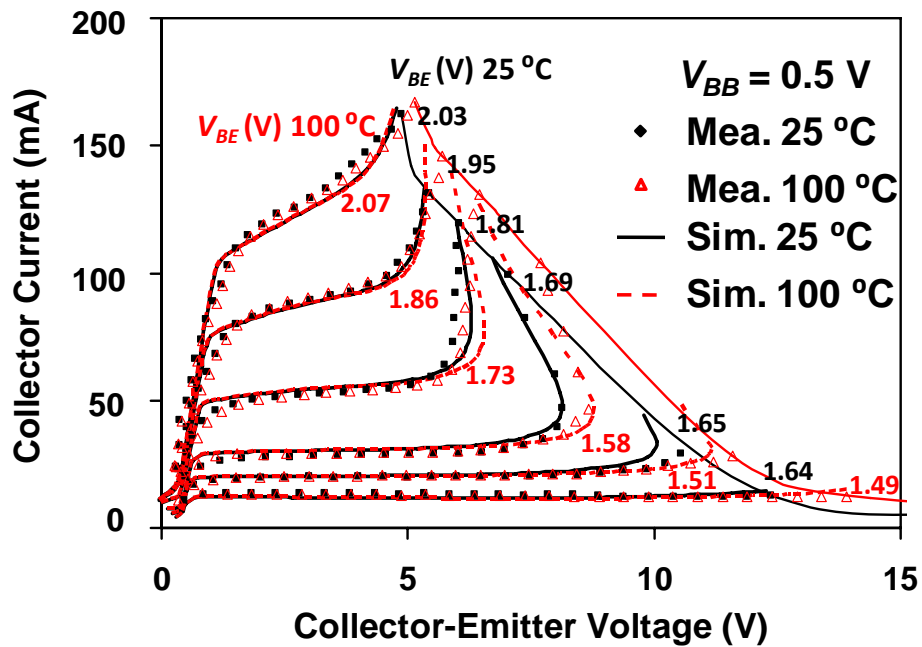
The total intrinsic base-emitter and base-collector charges are defined as:

$$Q_{BEi} = Q_{BEid} + (1 - FEXTB)Q_{iB} + (1 - FEXTC)Q_{iC} + (1 - FEXKE)Q_{krk} \quad (3-58)$$

$$Q_{BCi} = Q_{BCid} + FEXTB \times Q_{iB} + FEXTC \times Q_{iC} + FEXKE \times Q_{krk} + Q_{iR} \quad (3-59)$$



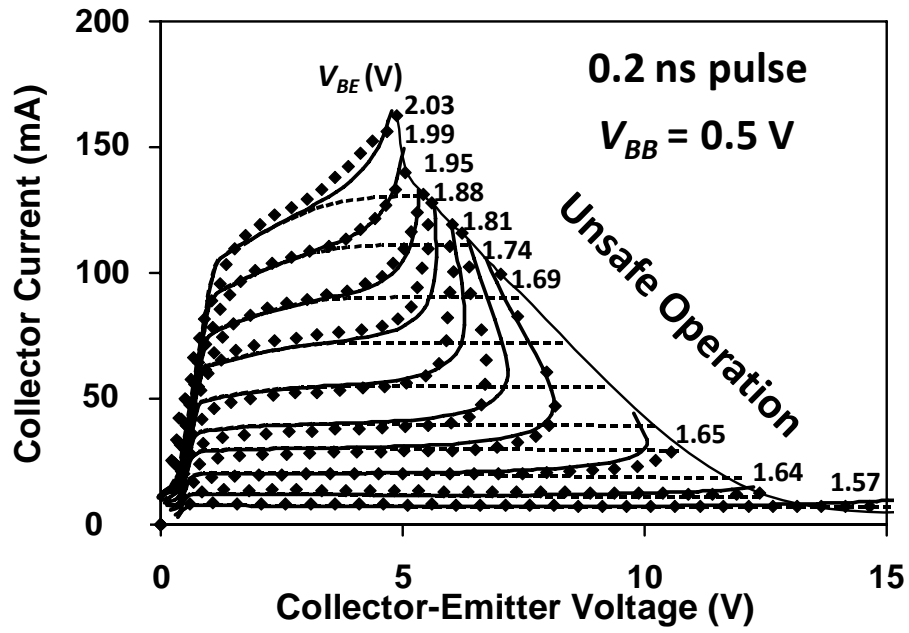
(a)



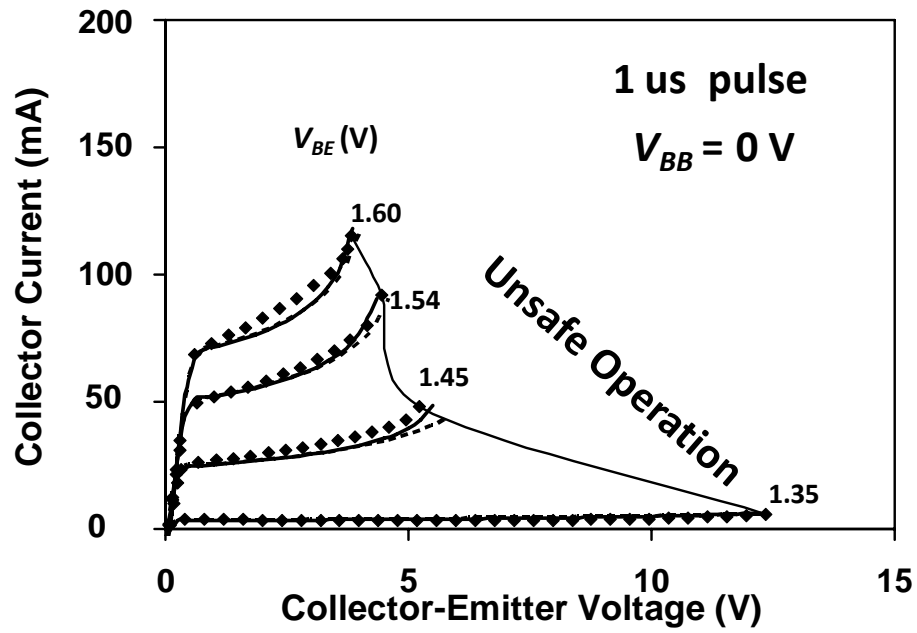
(b)

Fig. 3-5 Measured (symbol) vs. modeled (curve) sub-nanosecond pulse characteristics under different ambient temperatures

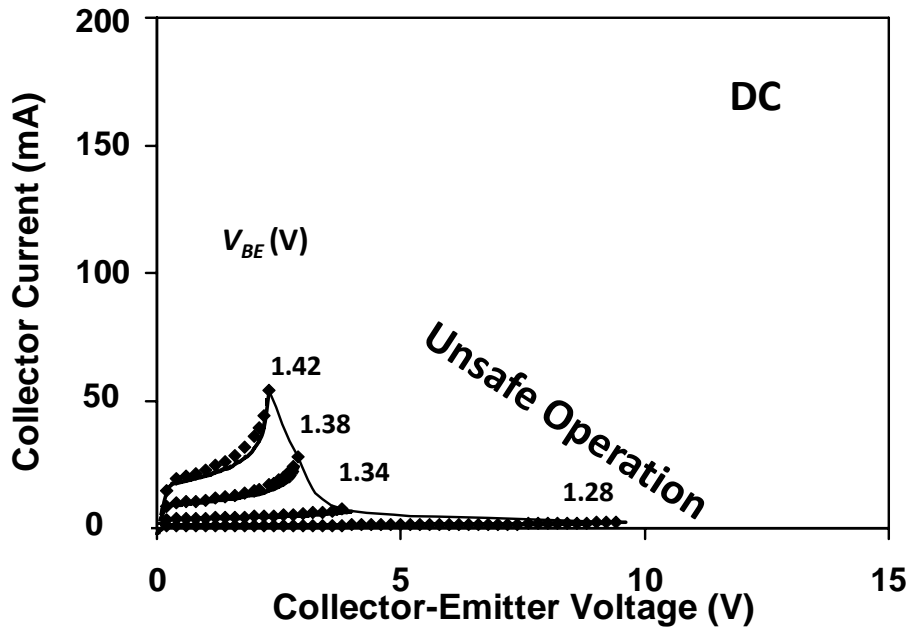
The impact ionization model of Eqn. (3-14)-(3-16) as well as the modified Kirk model [9] were coded in Verilog-A [10] and added to the commercially available Agilent HBT model [6] to simulate sub-nanosecond characteristics under both high voltages and high currents. The modified model is sufficiently robust to ensure convergence near I_1 and BV_{CEO} , with the former helped by the smooth hyperbolic function used in Eqn. (3-14) and the latter helped by the small step size used in simulation.



(a)



(b)



(c)

Fig. 3-6 Measured (a) sub-nanosecond pulse, (b) microsecond pulse, and (c) DC current-voltage characteristics of a common-emitter HBT. Each characteristic is obtained by pulsing to the same V_{BE} while stepping up V_{CE} after each pulse until the HBT dies. Simulated characteristics by using the Agilent model (- -) and the modified Agilent model (—) are included for comparison.

Fig. 3-6(a) shows that the modified model agrees with the measured I - V characteristics across the entire SOA, while the original Agilent model cannot simulate breakdown at all. However, Fig. 3-6(b) and Fig. 3-6(c) show that under much longer pulses or DC conditions, the difference between the Agilent model and the modified model diminishes because failures under these conditions are caused by thermal runaway instead of avalanche breakdown. Fig. 3-7 shows that the modified model agrees with the measured

impulse response under different collector biases, while the original Agilent model saturates prematurely at $V_{CC} = 10$ V. The same model was also successfully used to design and simulate an ultra-wideband pulse generator [11].

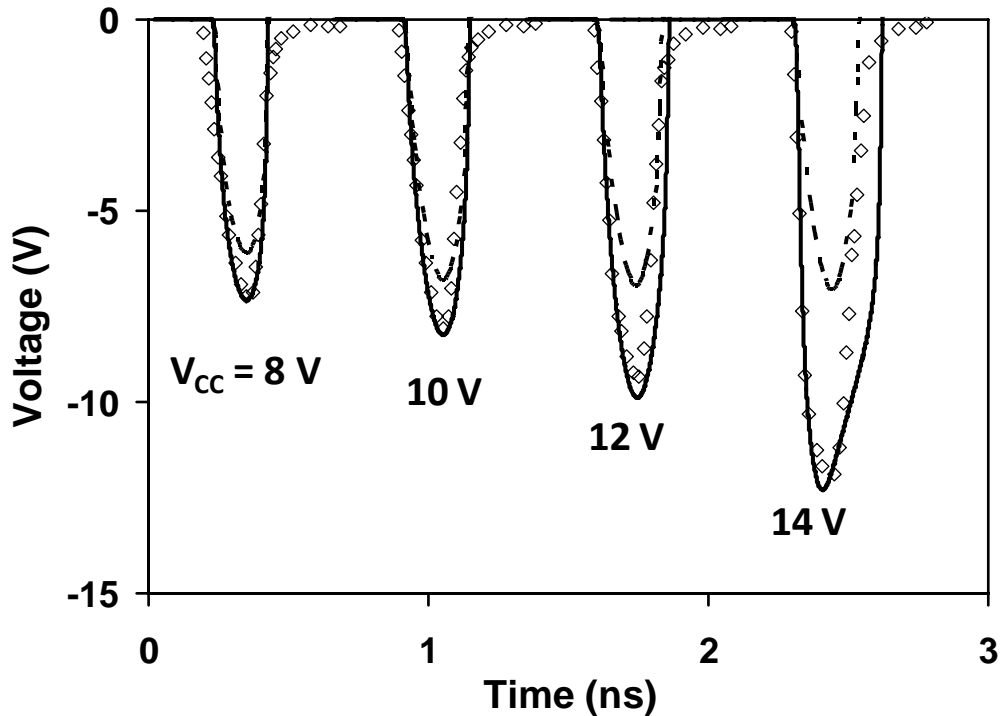


Fig. 3-7 Measured (symbol) impulse response of an HBT vs. that simulated by using the Agilent (---) and modified (—) HBT model. The input pulse is of 1.45 V peak-to-peak and 0.2 ns full width at half maximum. $V_{BB} = 0$. Artificial delays between impulses are added for clarity.

3.3. Modified Kirk Effect Model

Because the commercially available Agilent HBT model [8] includes limited Kirk effect we modified it according to our own formulism, which adds more voltage dependence to the conventional Kirk model.

Specifically, the Kirk charge Q_{krk} in the Agilent HBT model is replaced with the following:

$$Q_{krk} = I_{CE} W_{CIB}^2 / 4D_{NC} \quad (3-60)$$

where I_{CE} is the forward current from the collector to the base, W_{CIB} is the current-dependent extension of base, and D_{NC} is the electron diffusivity in the extended base. W_{CIB} is defined as

$$W_{CIB} = W_C - \sqrt{2\varepsilon V_{CBK} / (I_F / A_E v_{SAT} - qN_C)} \quad (3-61)$$

where W_C is the collector width, ε is the permittivity of GaAs, A_E is the emitter area, v_{SAT} is the saturated electron velocity, q is the electron charge, and N_C is the collector doping. Equation (3-61) follows the conventional form except that V_{CBK} differs from $V_{CB} + V_{BI}$ with a power term to account for high-field effects.

$$V_{CBK} = (V_{CB} + V_{BI}) \left\{ 1 + [(V_{CB} + V_{BI}) / V_{CK}]^{CK} \right\} \quad (3-62)$$

where V_{CB} and V_{BI} are the bias and built-in voltages of the collector-base junction, and V_{CK} and CK are fitting parameters. Meanwhile, D_{NC} is made current-dependent:

$$D_{NC} = D_{NC0} (I_C / I_{KCR})^{-GK} \quad (3-63)$$

where D_{NC0} is the low-field electron diffusivity in the collector, and I_{KCR} and GK are fitting parameters. Finally, following the conventional practice, Q_{krk} is partitioned

between the collector and base:

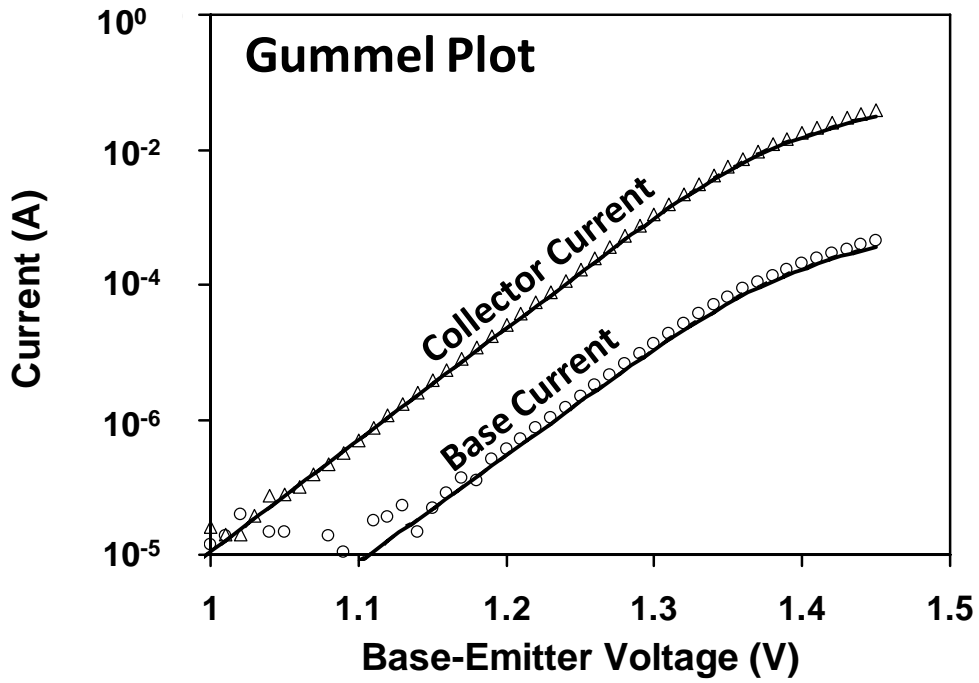
$$Q_{CK} = FEXKE \cdot Q_K; \quad Q_{BK} = (1 - FEXKE) \cdot Q_K \quad (3-64)$$

where *FEXKE* is yet another fitting parameter.

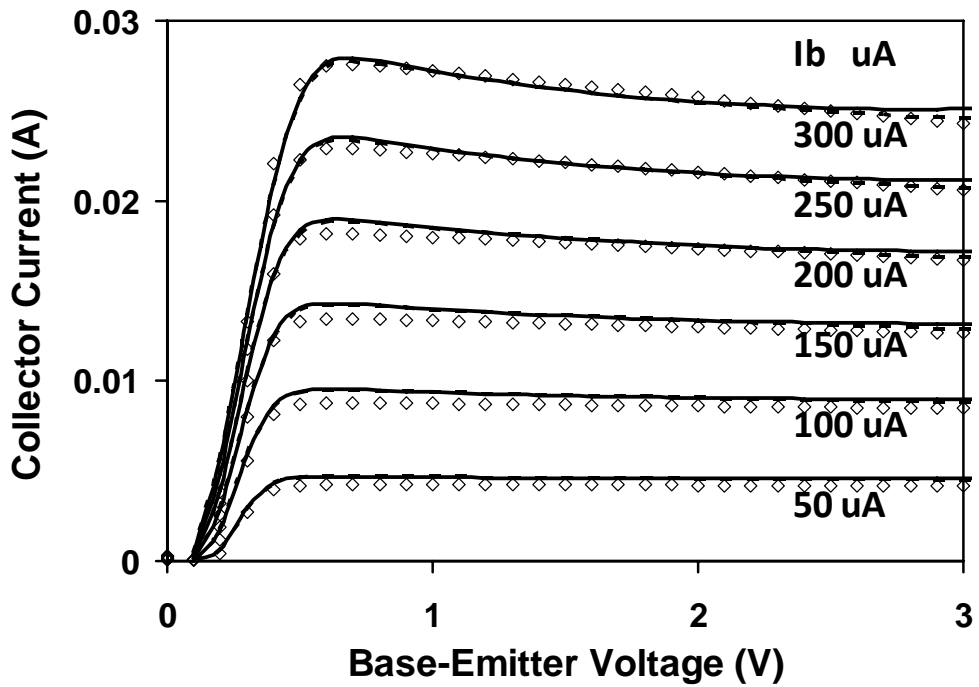
The simulation results in Fig. 3-5, Fig. 3-6 and Fig. 3-7 are obtained from the modified HBT model including both new impact ionization and Kirk effect.

3.4. Model Validation in Non-pulse Condition

To further validate the modified HBT model, it is used to simulate the performance of HBT in DC, small signal and large signal condition. In the large signal test, the transistor is biased in Class C mode with aggressive collector voltage.

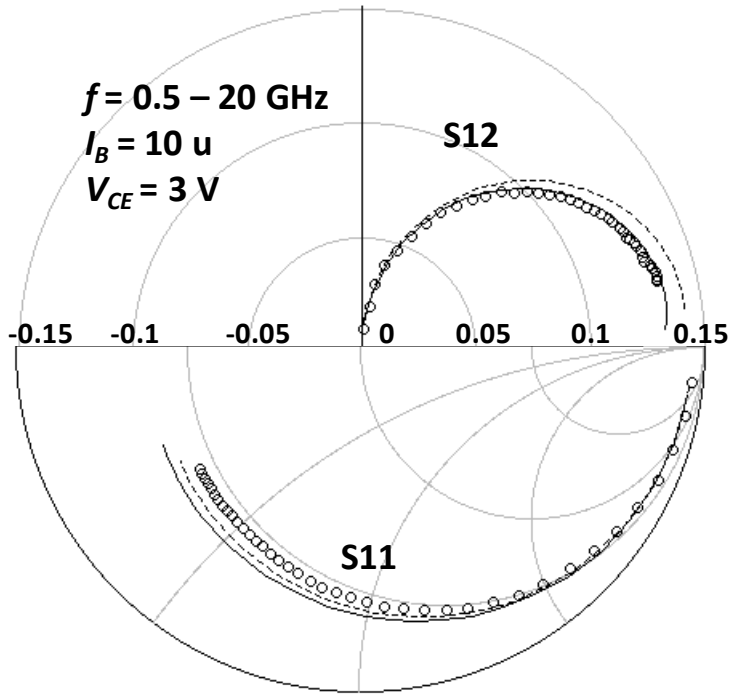


(a)

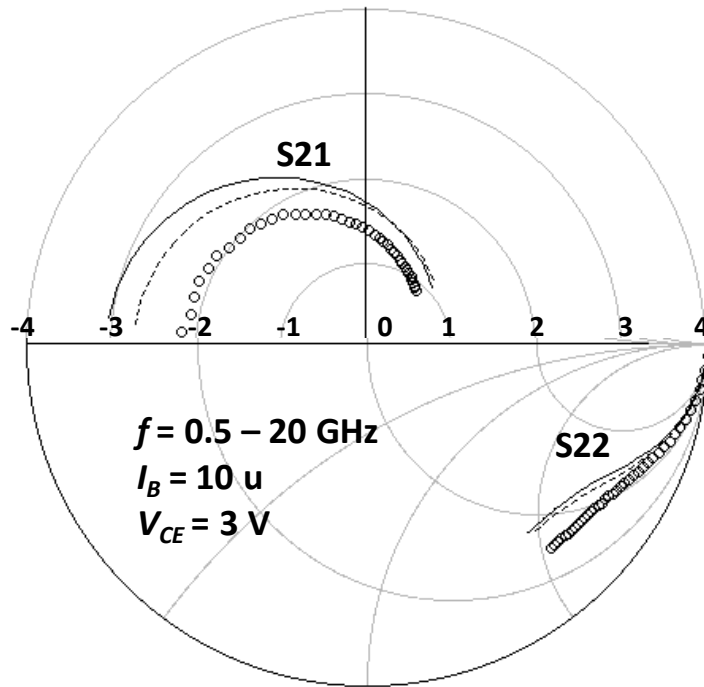


(b)

Fig. 3-8 Measured (symbol) (a) Gummel and (b) forward I-V of an HBT vs. that simulated by using the Agilent (---) and modified (—) HBT model. Agilent model is overlapped by modified HBT model.

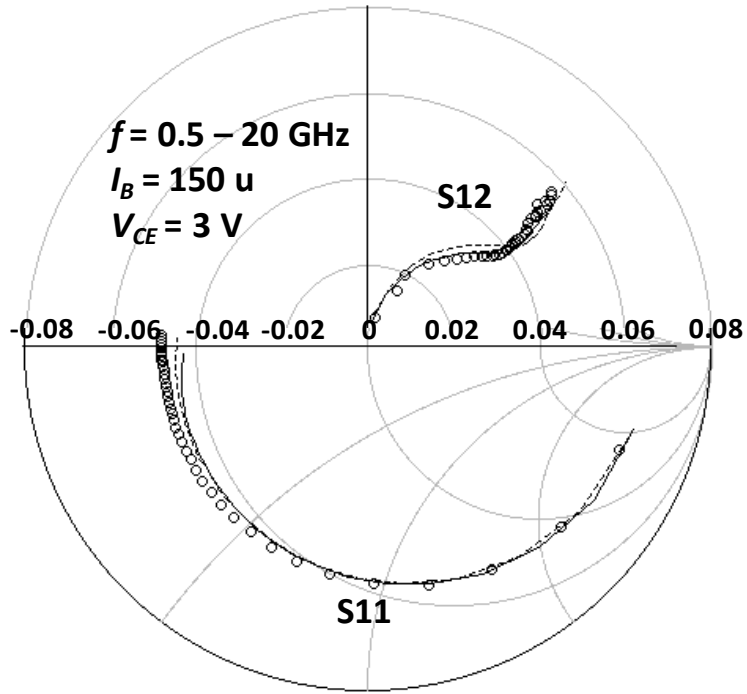


(a)

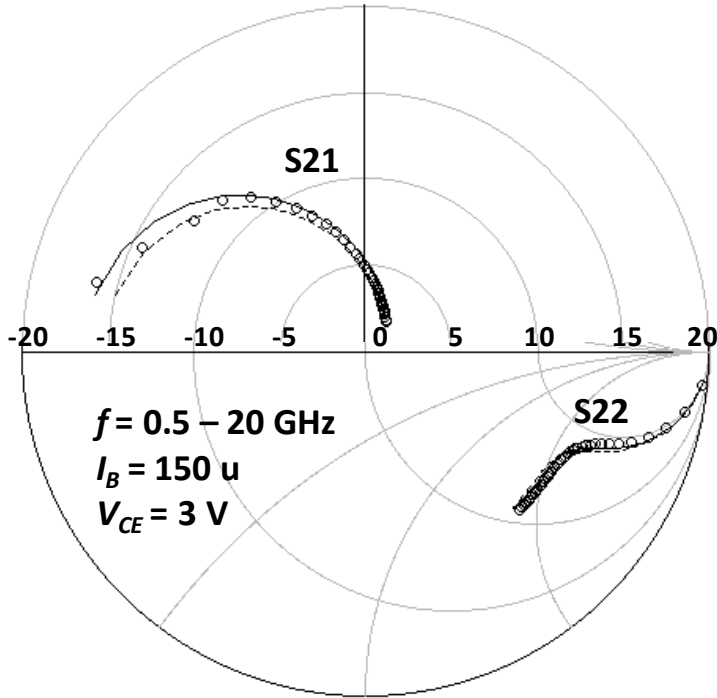


(b)

Fig. 3-9 Measured (symbol) CW S-parameters with low DC base current by using the Agilent (- - -) and modified (—) HBT model



(a)



(b)

Fig. 3-10 Measured (symbol) CW S-parameters under high DC base current by using the Agilent (- - -) and modified (—) HBT model

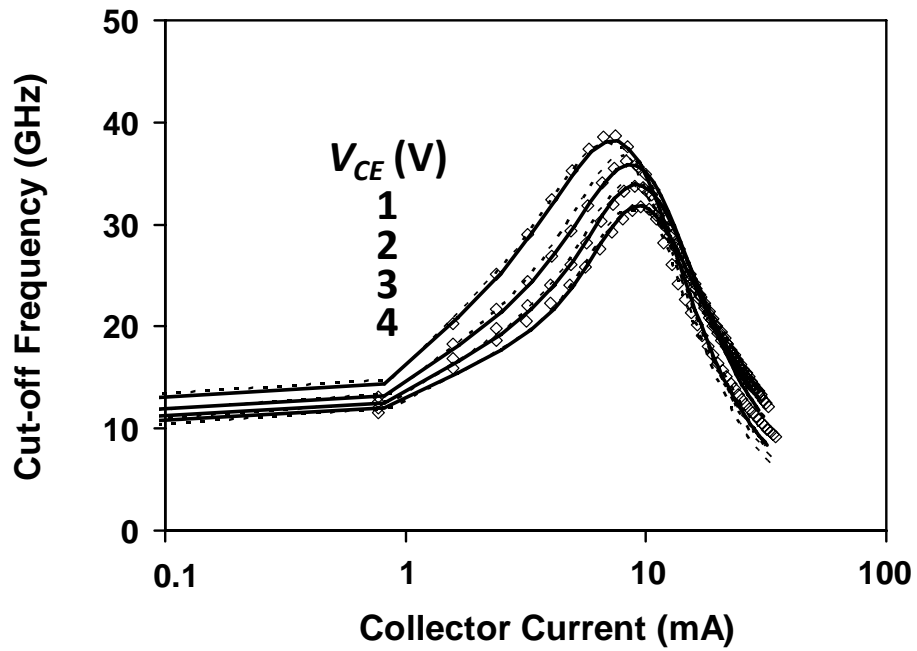
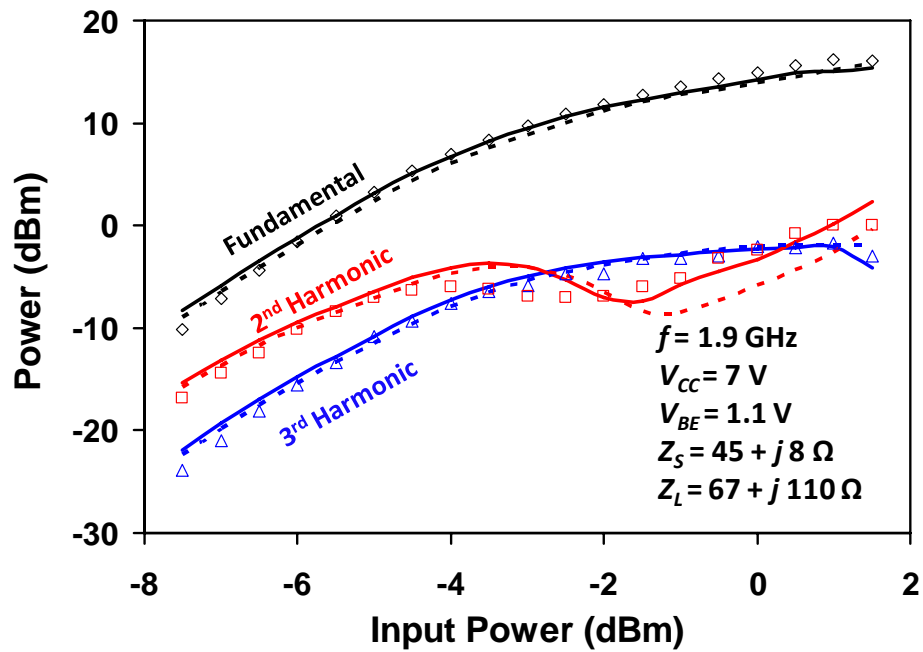
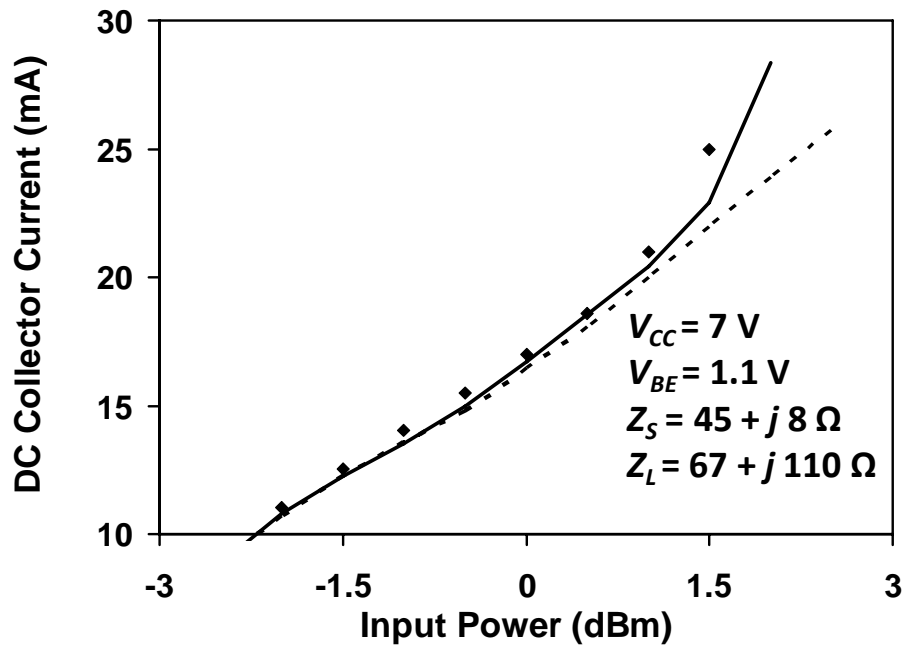


Fig. 3-11 Measured (symbol) CW small-signal forward current-gain cutoff frequency by using the Agilent (---) and modified (—) HBT model



(a)



(b)

Fig. 3-12 Measured (symbol) large-signal (a) fundamental and harmonics output power (b) self-biasing effect of a Class-C single-stage power amplifier vs. that simulated by using the Agilent (- - -) and modified (—) HBT model.

Fig. 3-6 Fig. 3-8 Fig. 3-9 Fig. 3-10 Fig. 3-11 and Fig. 3-12 show that while both the Agilent and the modified models can fit the DC and the small-signal characteristics, the modified model is superior to the Agilent model in simulating large-signal HBT characteristics such as the self-biasing effect.

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Chapter 4 SOA of HBT Power Amplifiers

The on-state breakdown under CW conditions is complicated by self heating. While an SOA model is being constructed to include the effects of temperature, pulse width and quiescent biases as illustrated in Fig. 2-7 Fig. 2-8 and Fig. 2-9, a simple analysis [1] can be used to predict the maximum output power of the amplifier as in the following.

The dynamic load lines of a Class-C amplifier with a conduction angle α can be expressed as

$$I_C = \begin{cases} 0, & -\pi \leq \omega t \leq -\alpha/2 \\ I_Q + I_{RF} \cos \omega t, & -\alpha/2 \leq \omega t \leq \alpha/2 \\ 0, & \alpha/2 \leq \omega t \leq \pi \end{cases} \quad (4-1)$$

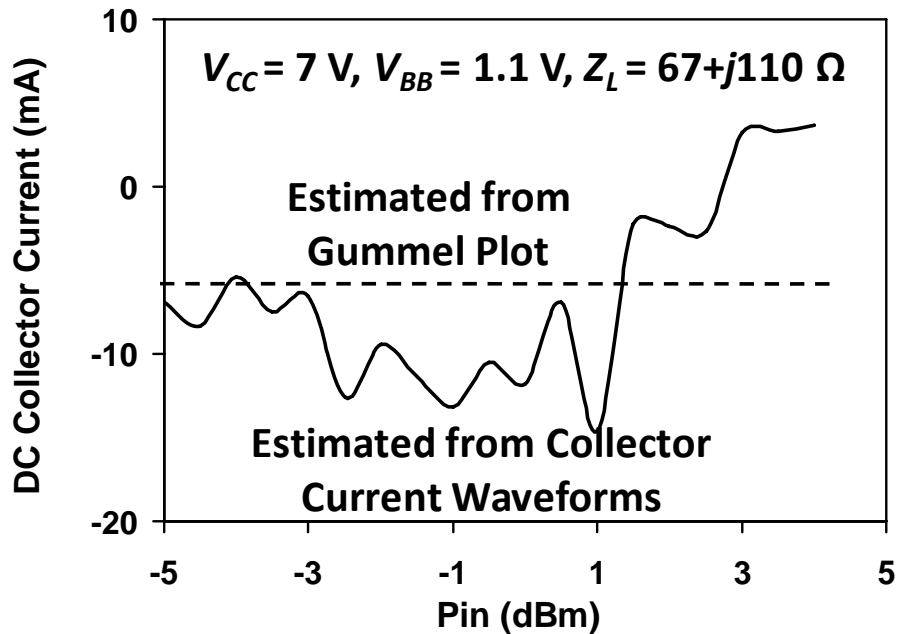
where I_Q is the equivalent quiescent collector current, I_{RF} is the amplitude of a sinusoidal signal of angular frequency ω , and t is time. The corresponding expression in the frequency domain is

$$I_C = I_{CC} + \sum_{N=1}^{\infty} (a_N \cos N\omega t + b_N \sin N\omega t) \quad (4-2)$$

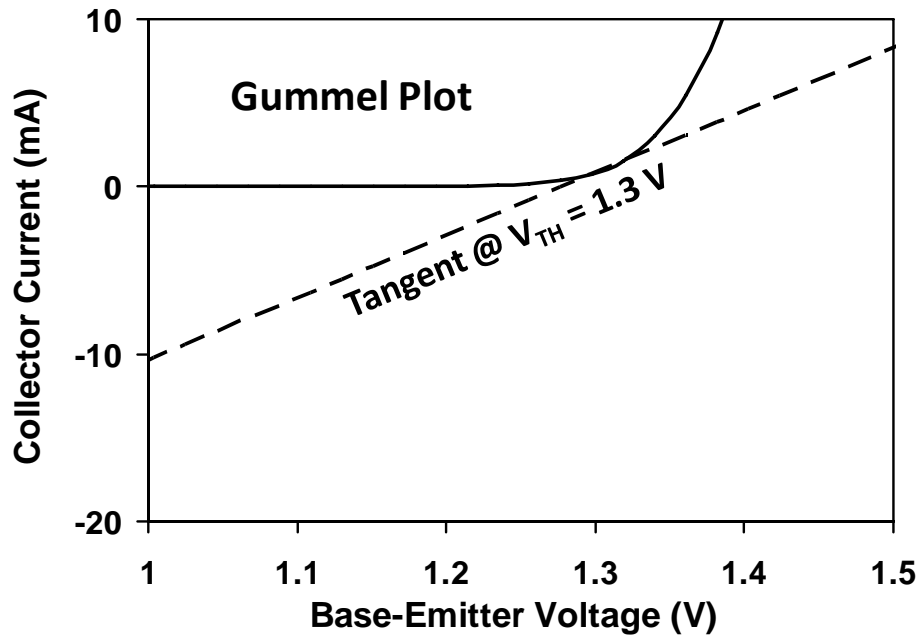
where I_{CC} is the DC component that includes the self-biasing effect as shown in Fig. 3-11(b), N is an integer, and a_N and b_N are amplitudes of fundamental and harmonic currents. (In practice, only five harmonics were used.) Because the waveform of (4-1) is

not sinusoidal, I_{CC} varies with the input power as shown in Fig. 4-1(a). For the sake of convenience, an average I_{CC} of -6 mA can be used for all power levels, which is approximately equal to the collector current extrapolated from the turn-on voltage of 1.3 V to $V_{BB} = 1.1$ V according to the slope at 1.3 V as shown in Fig. 4-1(b). Fig. 4-2 shows the time domain waveforms at the base of transistor. The base voltage is above 1.3V in approximately half of the period. The voltage developed by I_C on a load impedance of magnitude $|Z_{LN}|$ and angle θ_{LN} is

$$V_C = V_{CC} - \sum_{n=1}^{\infty} \left[\begin{array}{l} a_n |Z_{LN}| \cos(N\omega t + \theta_{LN}) \\ + b_n \sin(N\omega t + \theta_{LN}) \end{array} \right]. \quad (4-3)$$



(a)



(b)

Fig. 4-1 DC component of the collector current estimated from (a) non-sinusoidal waveforms and (b) Gummel plot.

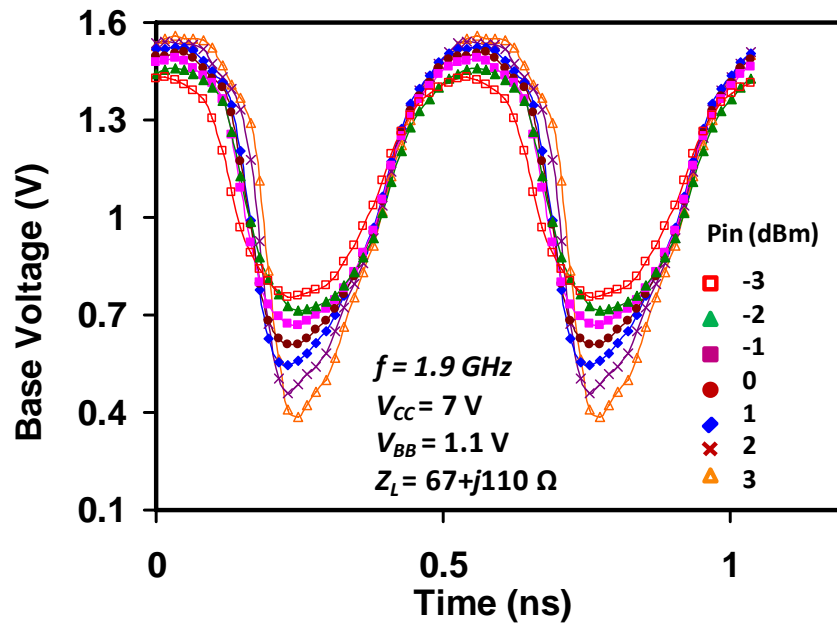


Fig. 4-2 Base voltage waveforms

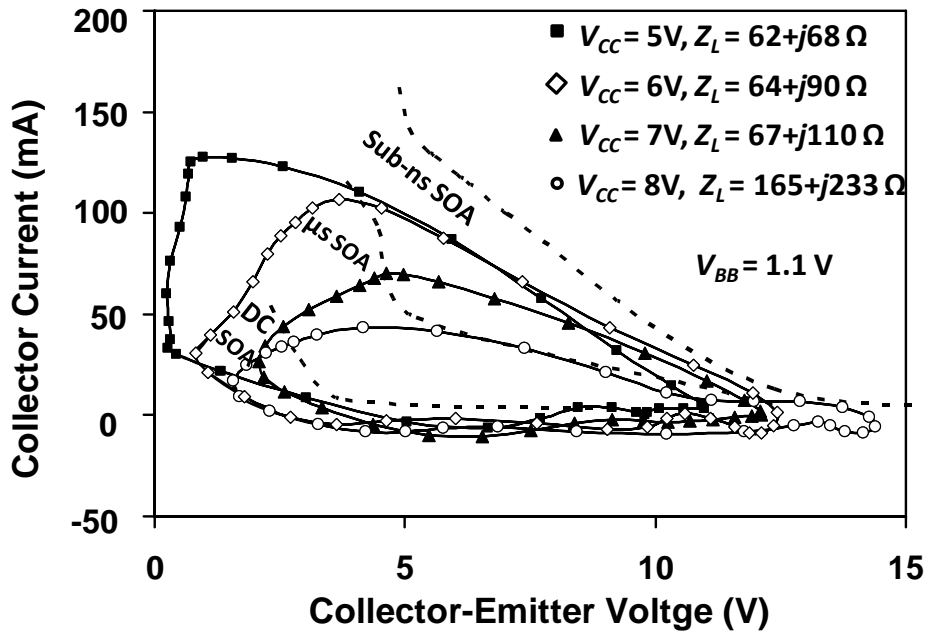
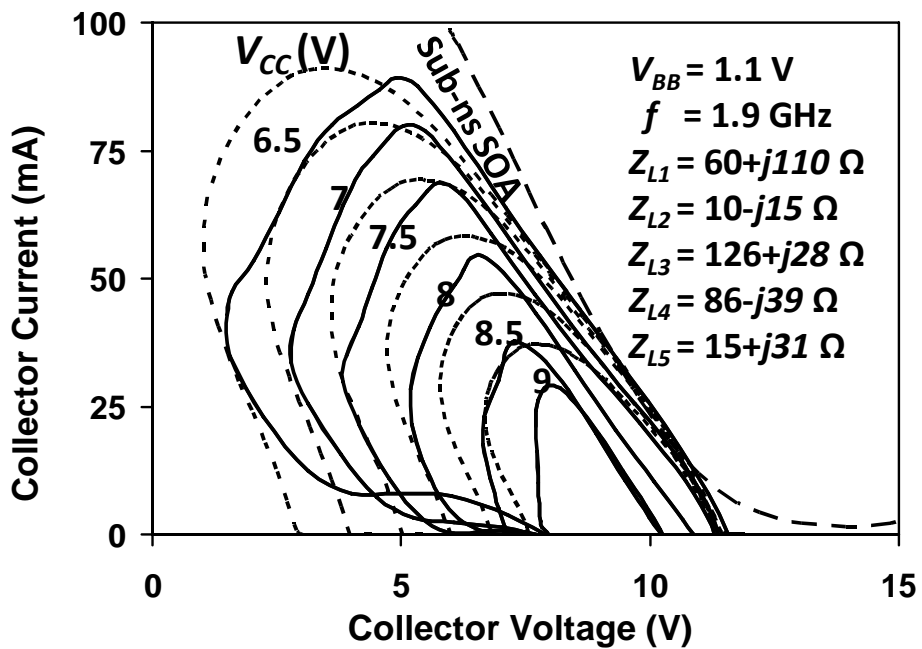


Fig. 4-3 Measured maximum load lines of a CW Class-C single-stage power amplifier under different collector biases and optimum loads for maximum power at 1.9 GHz. SOA boundaries (- - -) under sub-nanosecond pulses, microsecond pulses and DC, respectively, from Fig. 2-6 are included for comparison.

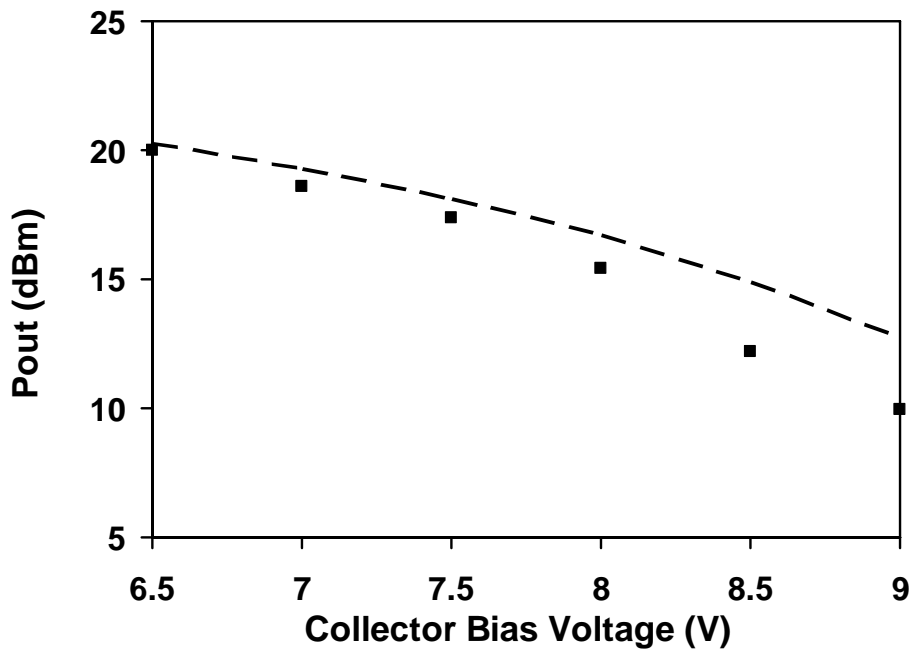
Fig. 4-3 confirms that the measured dynamic load lines of the CW Class-C single-stage power amplifier are limited by the sub-nanosecond SOA instead of the microsecond or DC SOA. Different collector biases are used in the measurement. At each bias, the load impedance is re-optimized for maximum output power while the input power is gradually stepped up until the HBT dies. Only the last load line before the HBT dies is shown in the figure. It can be seen that the maximum load lines for $V_{CC} > 5 \text{ V}$ all exceed the DC or microsecond SOA and are tangential to the sub-nanosecond SOA boundary near cutoff.

This shows that the SOA of the Class-C amplifier is mainly limited by off-state breakdown, which can be reliably characterized by sub-nanosecond pulses.

Fig. 4-4(a) shows that the measured dynamic load lines under the same load but different collector biases are in general agreement with that simulated according to (4-2) and (4-3) when they are tangential to the sub-nanosecond SOA boundary. However, the agreement degrades at higher V_{CC} settings in Fig. 4-4(b). This degradation is better illustrated by plotting the maximum output power at each V_{CC} against that measured. The deviation at high V_{CC} is probably caused by the lower output powers at higher V_{CC} , which decreases power-added efficiency and increases self heating. Notice that the sub-nanosecond SOA is defined by impact ionization alone without self heating. Similarly, Fig. 4-5 shows that the measured load-pull maximum power contours at $V_{CC} = 7$ V are in general agreement with that simulated by using (4-2) and (4-3), but the agreement degrades with increasing mismatch, decreasing output power, and decreasing power-added efficiency.



(a)



(b)

Fig. 4-4 Measured (—, ■) vs. simulated (- - -) maximum (a) dynamic load lines and (b) output powers under the same load but different collector biases.

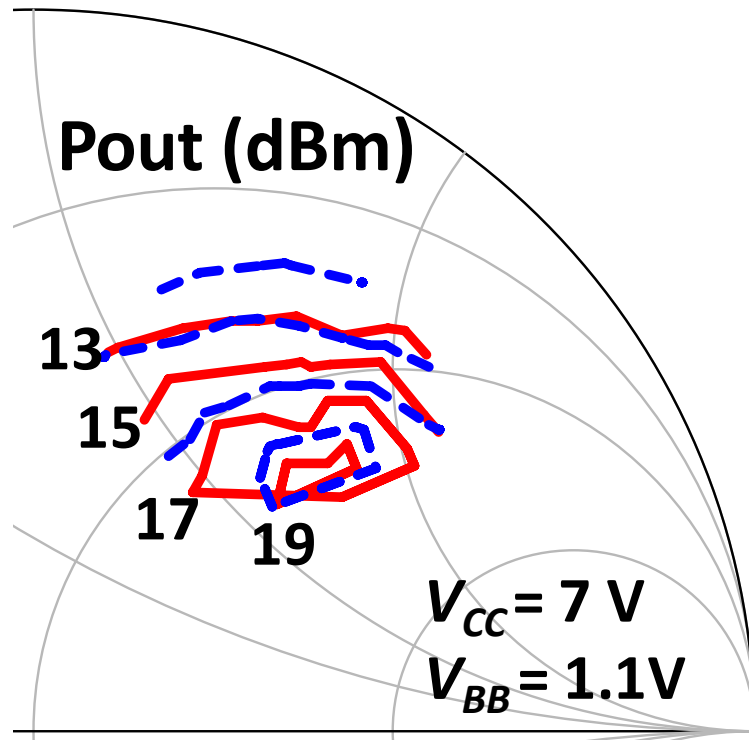


Fig. 4-5 Measured (—) vs. simulated (- - -) load-pull maximum power contours in the first quadrant of the Smith chart.

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Chapter 5 Ultra-Wideband (UWB) pulse amplifier

ULTRA-wideband (UWB) impulse radio [1] is attractive for applications such as through-wall imaging, precision navigation, location and tracking. A UWB impulse radio can be particularly attractive for high-resolution ranging applications, if low-duty-cycle high-peak-power transmitters can be readily assembled from sub-nanosecond high-voltage pulse generators. Additionally, pulse generators capable of tunable amplitude and width can enhance the functionality of the UWB impulse radio. For example, the pulse amplitude can be adjusted according to the range of interest, while the pulse width can be varied to inspect objects at different depths inside a wall.

Sub-nanosecond high-voltage pulse generators are required by low-duty-cycle high-peak-power UWB transmitters to maximize their performance without exceeding the FCC limits of -41.3 dBm/MHz and 0 dBm/50 MHz for average and peak powers, respectively [2]. For pulse-repetition frequencies of 187.5 kHz or lower, the limit for peak power governs. In this case, for a pulse width of 0.5 ns, the pulse amplitude can be as high as 8.9 V on a $50\text{-}\Omega$ load [3]. Considering connector loss, antenna mismatch, etc., sub-nanosecond greater-than- 10-V pulse generators are required.

5.1. Circuit Design

The GaAs HBT IC technology is chosen for not only its superior combination of high-voltage and high-frequency characteristics to that of Si CMOS or BiCMOS IC technology, but also its much enhanced power capacity for low-duty-cycle isothermal operation [4], which helps compact the size of the pulse generator. Because the thermal conductivity of GaAs is three times lower than that of Si, ordinarily, the power capacity of GaAs HBTs is limited by thermally induced current collapse [5]. However, this is not an issue under low-duty-cycle isothermal operation. So the traditional design approach is not suitable to GaAs HBT pulse generator. In our design, the Darlington pair is used to keep the main amplifier isothermal effectively, which greatly increases the output power from the pulse generator. Used in most mobile phones, the GaAs HBT technology is also relatively mature and low cost. In comparison, GaAs HEMTs often suffer from gate lag while GaAs HEMTs are less mature.

Fig. 5-1 shows the tunable pulse generator fabricated by a commercial HBT foundry [6]. The die size is less than $1\text{ mm} \times 1\text{ mm}$, which includes not only all HBTs but also all bias resistors, capacitors, and DC/RF probe pads. To ensure compact size and wideband performance, the pulse generator contains only one small inductor, which is part of the

L-C derivative circuit. Extra probe pads are included for diagnosis but are not required for establishing the circuit performance. The die size could have been at least halved, but was laid out to match the footprint of other circuits.

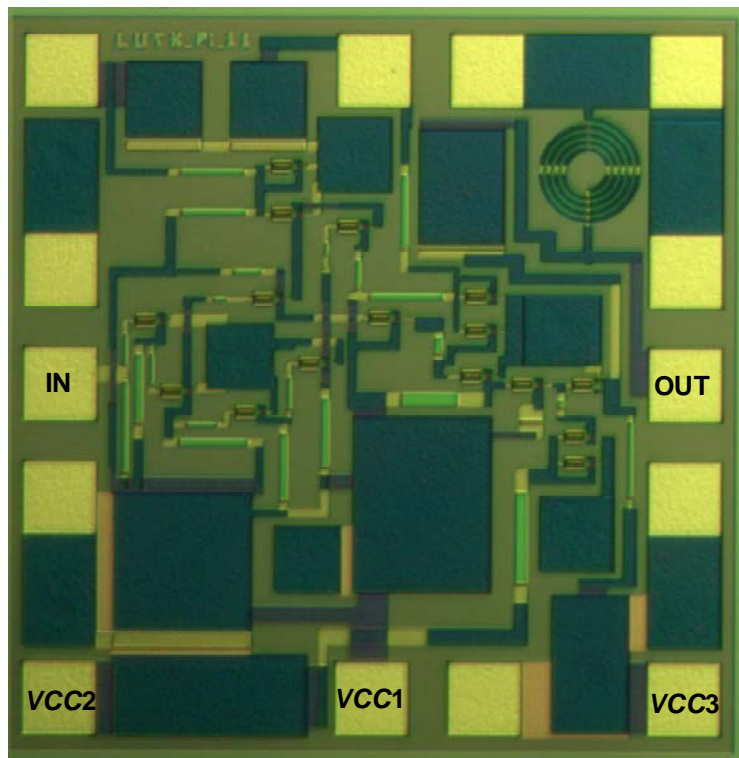


Fig. 5-1 Micrograph of the $\sim 1 \text{ mm}^2$ GaAs HBT IC pulse generator.

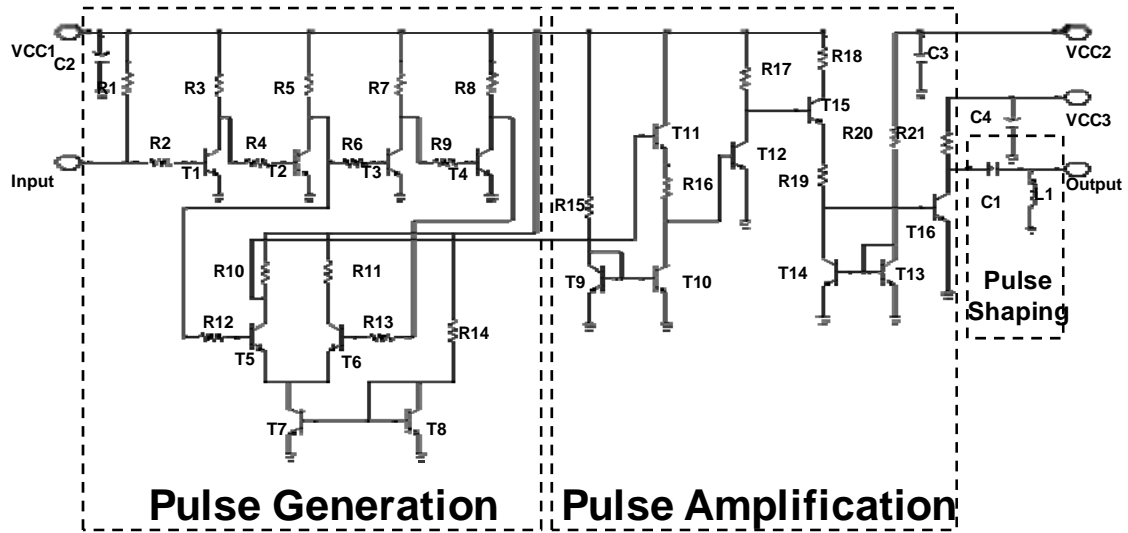


Fig. 5-2 Circuit schematics showing the pulse generator comprises the pulse generation, amplification and shaping blocks.

Fig. 5-2 shows schematically the circuit design of the pulse-generation, pulse-amplification and pulse-shaping blocks of the pulse generator. The pulse-generation block includes a delay chain of HBTs T1, T2, T3 and T4 and a differential amplifier of HBTs T5 and T6. T5 and T6 are driven by T2 and T4, respectively. The delay time τ between T2 and T4 is dominated by the R - C time constant of the load resistance on the collector of each HBT and the load capacitance between the collector of one HBT and the base of the next HBT. For the present HBTs, $R \approx 1000 \Omega$ and $C \approx 0.2 \text{ pF}$. Therefore, $\tau \approx 2RC \approx 0.4 \text{ ns}$ and the pulse-generation block can generate sub-nanosecond positive and negative pulses from the falling and rising edges, respectively, of the TTL input (Fig. 5-3). The input amplitude to T6 is higher than that of T5 because the base current of T3

introduces additional voltage drop over R5. Once T6 is conducting, the output of T5 is clamped at the high voltage whether T5 is conducting or not. This helps maximize the single-ended output of the differential amplifier T5-T6 while suppressing the generation of positive pulses. At the ensuing Class-C pulse-amplification block, the relatively strong negative pulses are further amplified and sharpened while the relatively weak positive pulses are further suppressed.

The pulse-amplification block includes two Darlington pairs, T11-T12 and T15-T16, respectively. T12 is biased in the saturation region so that the first Darlington pair serves as the driver amplifier; T16 is biased in the cutoff region so that the second Darlington pair acts as a Class-C amplifier. The Class-C bias of T16 helps ensure isothermal operation, minimize power consumption, cut off low-voltage ringing, compress pulse width, and prevent oscillation. Current mirrors T9-T10 and T13-T14 limit the currents through T11 and T15, respectively. In the whole amplification block, DC and RF paths are coupled to minimize the die size. T16 is shunted to $VCC3$ through a 1 k Ω resistor instead of an inductor, which provides adequate DC-RF isolation. This resistor consumes no power as T16 is normally off, but it cannot be made much bigger without impacting pulse repetition frequency.

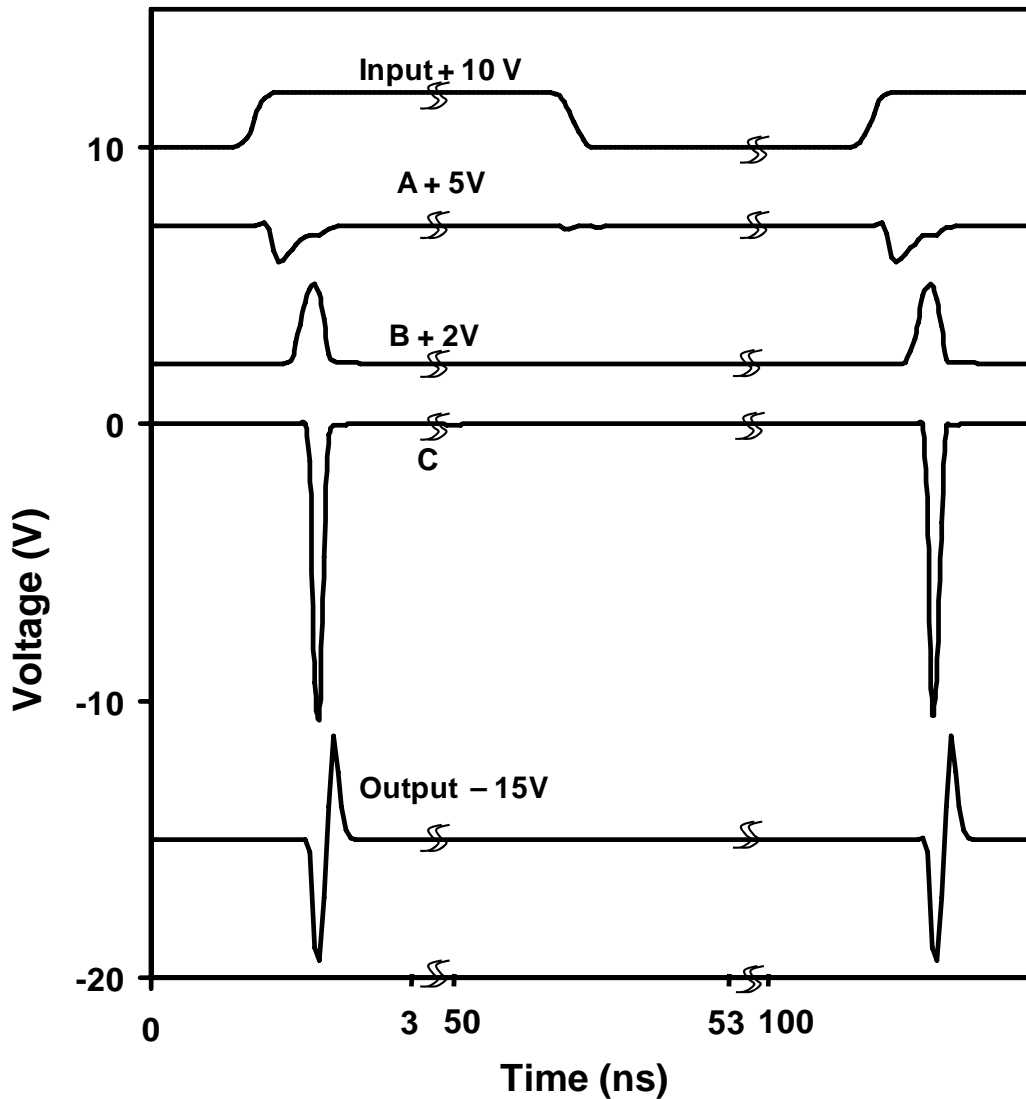


Fig. 5-3 Simulated voltage waveforms at the input and output of the pulse generator as well as the internal nodes A, B and C labeled in Fig. 5-2. The negative pulse generated from the rising edge of the input signal is progressively amplified and shaped, while the positive pulse generated from the falling edge of the input signal is barely discernable at A and is completely suppressed at the output. Artificial offset voltages are added for clarity.

The pulse-shaping block is a simple high-pass L-C derivative circuit. If necessary, higher order derivative circuits can be added to shape the pulse further and to take advantage of the full bandwidth of 3.1-10.6 GHz. C2 and C3 are two big bypass

capacitors and each of them is equal to 24 pF.

All HBTs in the pulse generator are of the same design with an emitter area of $2\ \mu\text{m} \times 20\ \mu\text{m}$, except T16 has an emitter area of $2\ \mu\text{m} \times 20\ \mu\text{m} \times 4$. The collector of T16 is shunted to $VCC3$ through a $1\ \text{k}\Omega$ resistor, which provides adequate DC-RF isolation and helps reduce ringing. Although this resistor consumes little power as T16 is normally off, it cannot be made much bigger without degrading the performance at high pulse-repetition frequencies. When T16 is turned on by the input pulse, the output impedance of T16 quickly approaches $50\ \Omega$, as evidenced by the absence of ringing or other delayed reflections in both simulation and measurement. This large-signal transient impedance can be adjusted by varying the size and bias of T16 to better suit that of the antenna, especially UWB antennas with higher-than- $50\text{-}\Omega$ impedances.

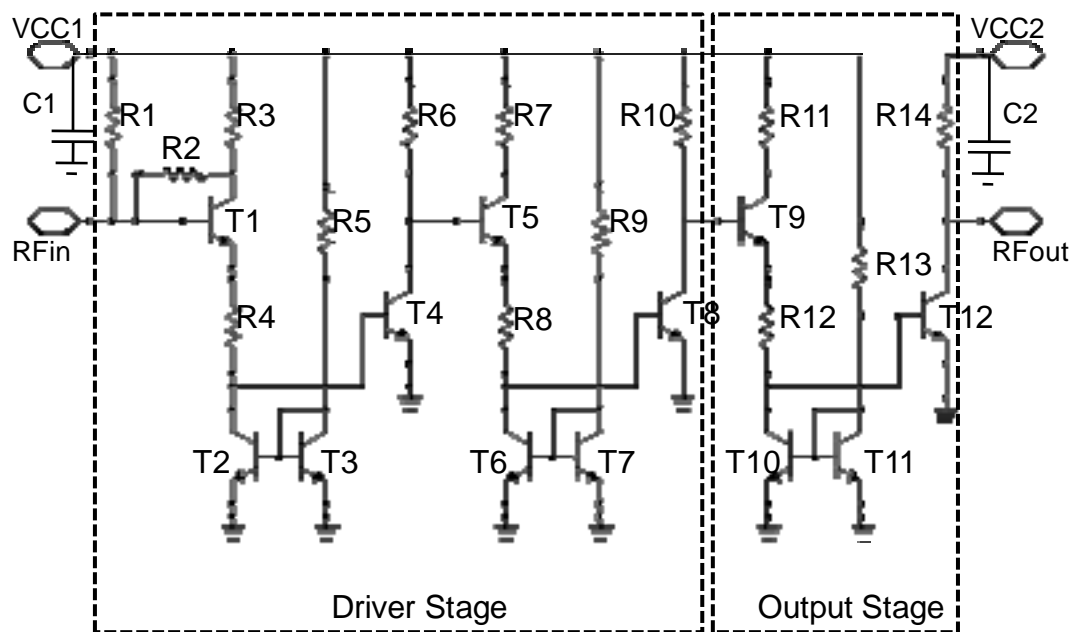
The output pulse width can be tuned by adjusting $VCC2$, which affects the base bias of T16 through R19. The output pulse amplitude can be tuned by adjusting $VCC3$, which affects the collector bias of T16 through R21. Usually, the output pulse amplitude of T16 may be limited by both self heating and avalanche breakdown. For the present low-duty-cycle sub-nanosecond pulse generator, self heating is not a concern because the HBT thermal time constant is on the order of μs [7]. Avalanche breakdown is suppressed

by adding R19 and T14 to the base of T16 [8]. Typically, $VCC1 = 3.3\text{ V}$, $VCC2 = 2\text{-}5\text{ V}$, and $VCC3 = 4\text{-}14\text{ V}$.

Fig. 5-3 shows the simulated voltage waveforms at the input and output of the pulse generator, as well as the internal nodes A, B, and C labeled on Fig. 5-2. It can be seen that at Node A, negative pulses are generated from the rising edge of a 10-MHz square-wave input signal, while positive pulses generated from the falling edge of the input are barely discernable. The negative pulses are then inverted and amplified once at Node B and twice at Node C, while the positive pulses are completely suppressed. Finally, the output signal becomes monocycle after going through the $L\text{-}C$ pulse-shaping block.

In addition to the above-described *monocycle generator*, its individual blocks were also designed, fabricated and tested separately to help analyze the circuit design. For example, an *impulse generator* was designed without the pulse-shaping block, while the pulse-amplification block was designed in two different configurations. Fig. 5-4 shows that in the first pulse- amplification design, a Darlington pair replaces the pulse-generation block to form a *three-stage pulse amplifier*, with the input shunted to $VCC1$ through a $50\ \Omega$ resistor to provide broadband matching. Each amplifier stage works as an inverter, so the output remains negative under a positive input pulse. In the

second pulse-amplification design, a differential amplifier replaces the pulse-generation block as well as the first Darlington pair of the pulse-amplification block to improve linearity and reduce power consumption. However, the gain of the resulted *two-stage pulse amplifier* is lower than that of the three-stage pulse amplifier of the first design. The performance of the fabricated impulse generator, monocycle generator, two-stage pulse amplifier, and three-stage pulse amplifier are described in the following section.



(a)

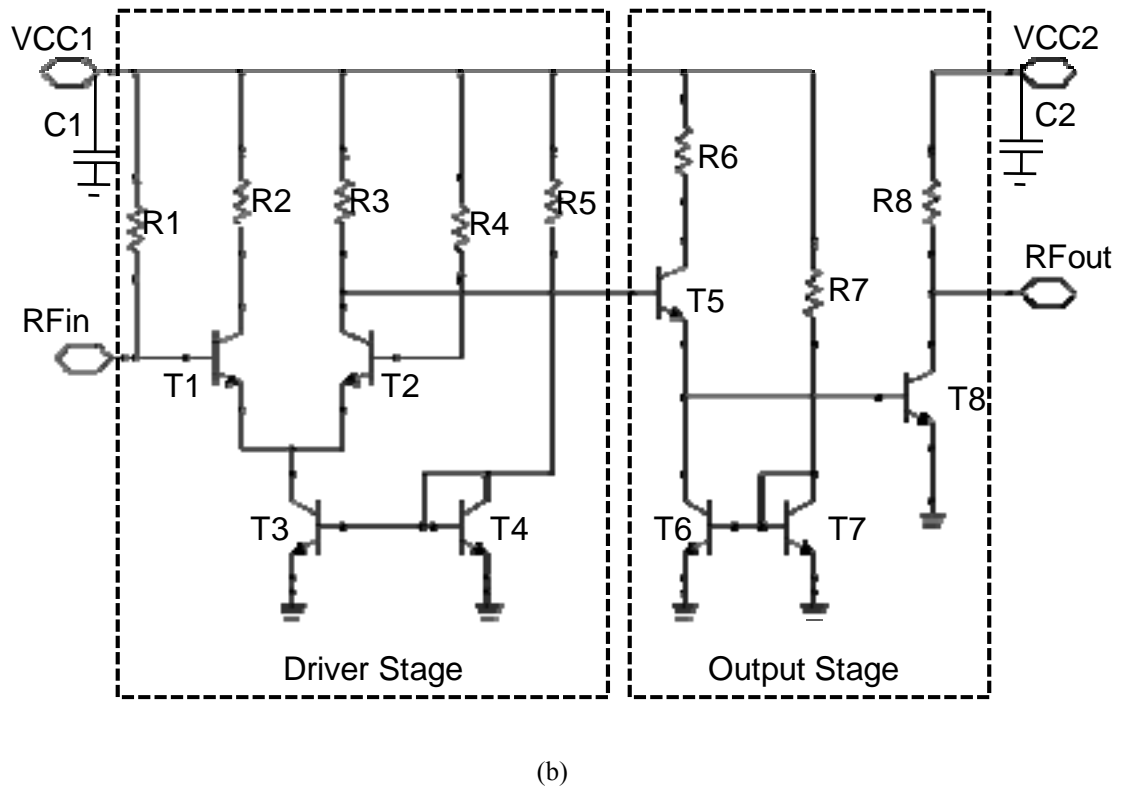


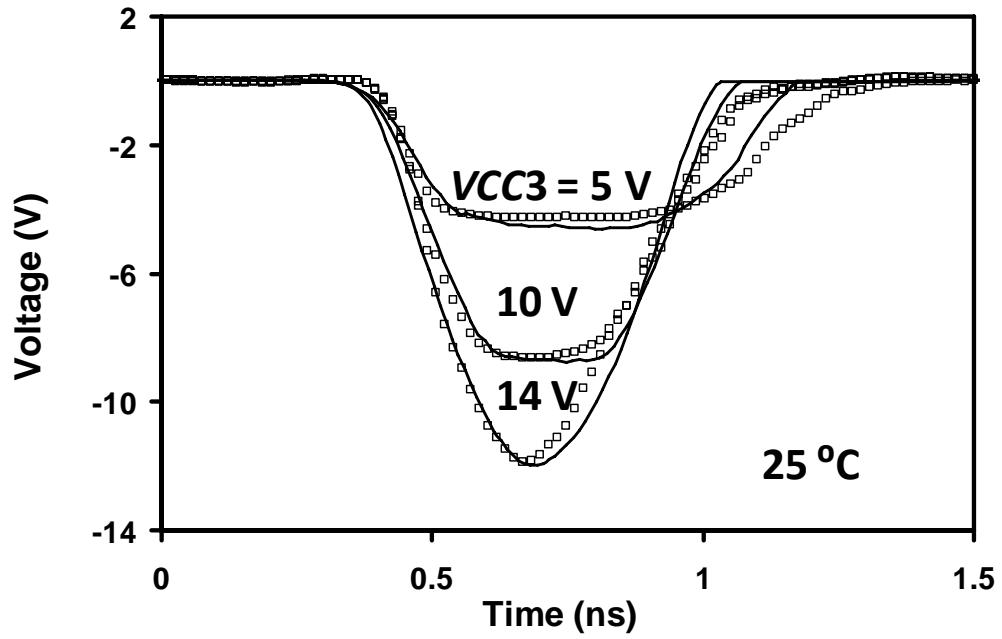
Fig. 5-4 (a) Three- and (b) two-stage pulse amplifiers designed to help analyze the pulse generator.

5.2. Results and Discussion

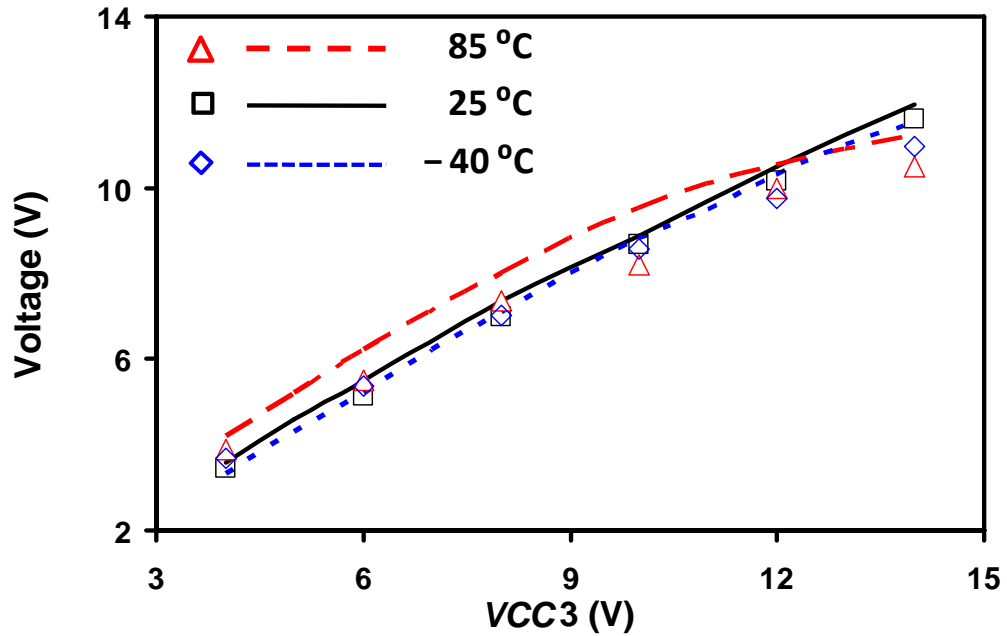
5.2.1. Impulse generator

The fabricated pulse generators were tested by using a previously described setup [9] with the TTL input generated by an HP 8116A function generator. The output waveforms were sampled by an Agilent 86100 oscilloscope and de-embedded to the die input and output pads after accounting for the frequency response of the cable assemblies. Unless otherwise noted, most pulse generators were tested with a 0.5-2.5-V TTL square signal of

10-MHz pulse-repetition frequency (Fig. 5-3), which corresponds to <1% duty cycle for the submicron pulses.



(a)

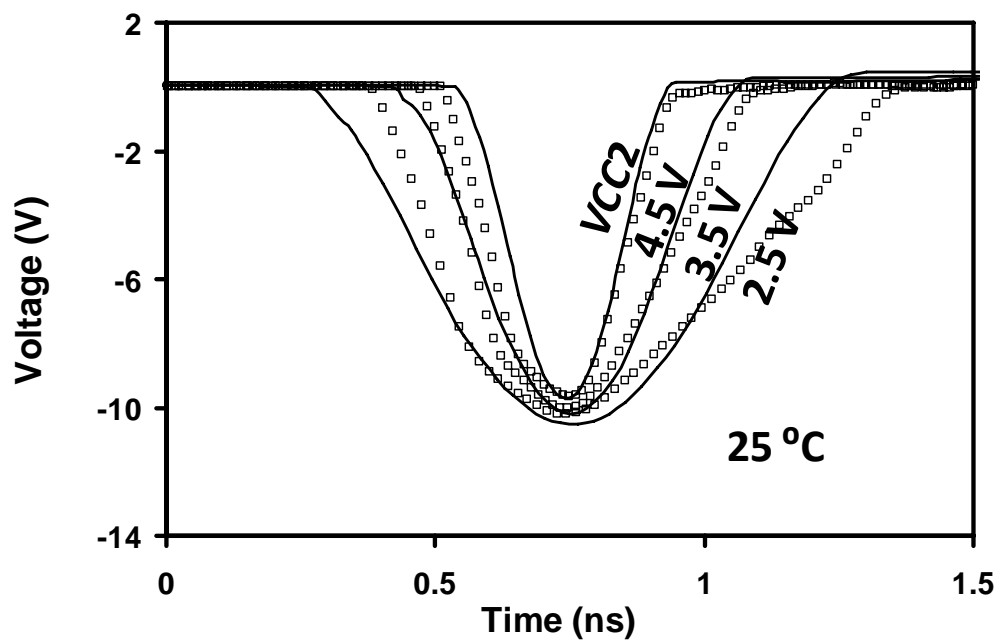


(b)

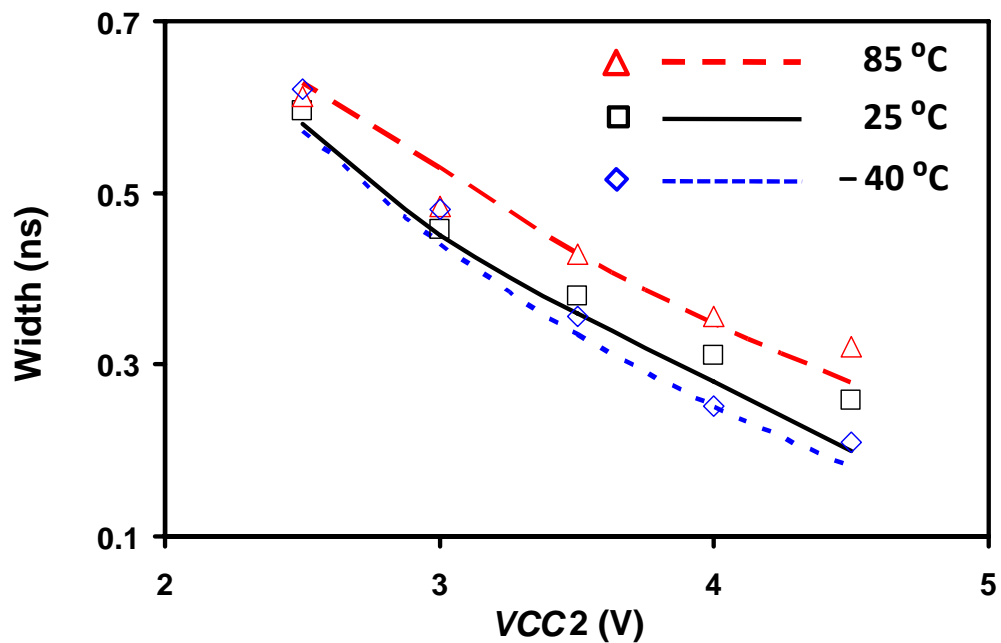
Fig. 5-5 Measured (symbol) vs. simulated (curve) (a) waveform and (b) pulse amplitude at Node C of the pulse generator with $VCC1 = VCC2 = 3.3$ V, and $VCC3 = 4$ -14 V.

As predicted by simulation, Fig. 5-5 shows that the pulse amplitude at Node C of the pulse generator can be tuned linearly between 3.5 V to 11.5 V by varying $VCC3$ from 4 V to 14 V, while maintaining the pulse width within 0.3 ± 0.1 ns. (In this paper, the pulse amplitude is measured peak-to-peak, while the pulse width is the full width at half maximum.) Fig. 5-6 shows that the pulse width at Node C can be tuned linearly between 0.25 ns and 0.65 ns by varying $VCC2$ from 2.5 V to 4.5 V, while maintaining the pulse amplitude at 10 ± 1 V. (Both Fig. 5-5 and Fig. 5-6 include additional temperature-dependent data, which will be discussed later.) Following the pulse-shaping

block, the pulses at Node C are converted to monocycles at the output. Fig. 5-7 shows that with V_{CC2} varying between 2 V and 6 V, the monocycle amplitude varies from 5.1 V to 8.8 V while its width varies from 0.2 ns to 1.0 ns. The positive and negative portions of the monocycle differ mainly due to the low quality factor of the inductor.



(a)



(b)

Fig. 5-6 Measured (symbol) vs. simulated (curve) (a) waveform and (b) width of impulses at Node C of the pulse generator with $VCC1 = 3.3$ V, $VCC2 = 2.5-4.5$ V, and $VCC3 = 12$ V

Fig. 5-8 shows that the output amplitude of the pulse generator is rather stable under different pulse- repetition frequencies between 40 KHz and 25 MHz, which indicates that the isothermal approximation is valid over a wide range of pulse amplitudes and duty cycles. High impedance antennas are often used in UWB systems, so the pulse generator was evaluated by increasing the load impedance from 50 Ω to 200 Ω . No oscillation was observed. Fig. 5-9 shows that under a constant input voltage of 2 V (Fig. 5-3) and a load impedance of 200 Ω , the pulse amplitude at Node C is slightly lower than $VCC3$ by the HBT knee voltage of approximately 1 V. However, at lower load impedances such as 100

Ω and 50Ω , the pulse amplitude saturates at a value much lower than $VCC3$ unless the input voltage is significantly increased to overdrive the pulse generator. In this case, although the pulse generator could output 12 V into the different load impedances, the output power would decrease with increasing load impedance. However, if both the input and bias conditions could be fine-tuned for each load impedance, then the minimum pulse width would decrease with increasing load impedance, too. For example, after such fine tuning, the minimal pulse widths with 10-V pulse amplitude are 0.25 ns, 0.21 ns and 0.20 ns for 50Ω , 100Ω and 200Ω loads, respectively.

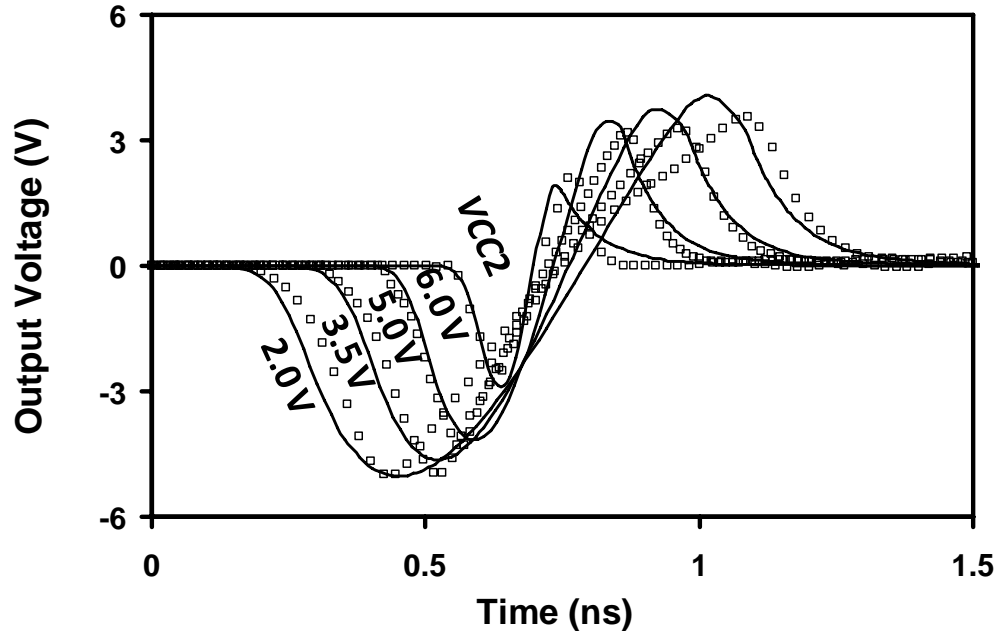


Fig. 5-7 Measured (symbol) vs. simulated (curve) monocycles generated with $VCC1 = 3.3 \text{ V}$, $VCC2 = 2\text{-}6 \text{ V}$, and $VCC3 = 13 \text{ V}$.

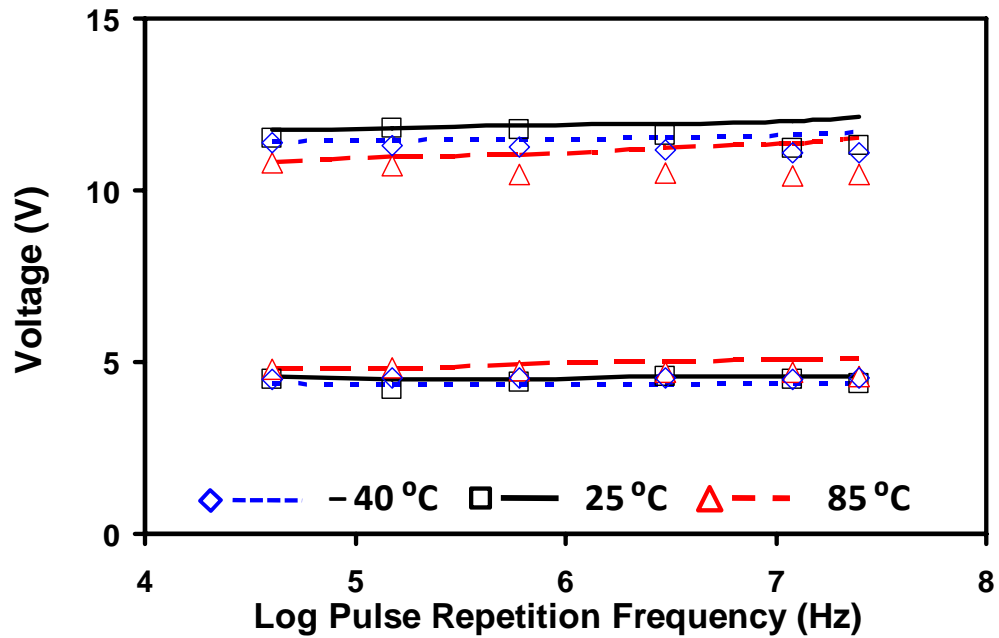


Fig. 5-8 Measured output pulse amplitudes under different temperature as functions of pulse-repetition frequency between 40 kHz and 25 MHz. From the bottom up, the biases for pulse generator are $V_{CC1} = 3.3$ V, $V_{CC2} = 3.3$ V, $V_{CC3} = 14$ V and $V_{CC1} = 3.3$ V, $V_{CC2} = 3.3$ V, $V_{CC3} = 6$ V

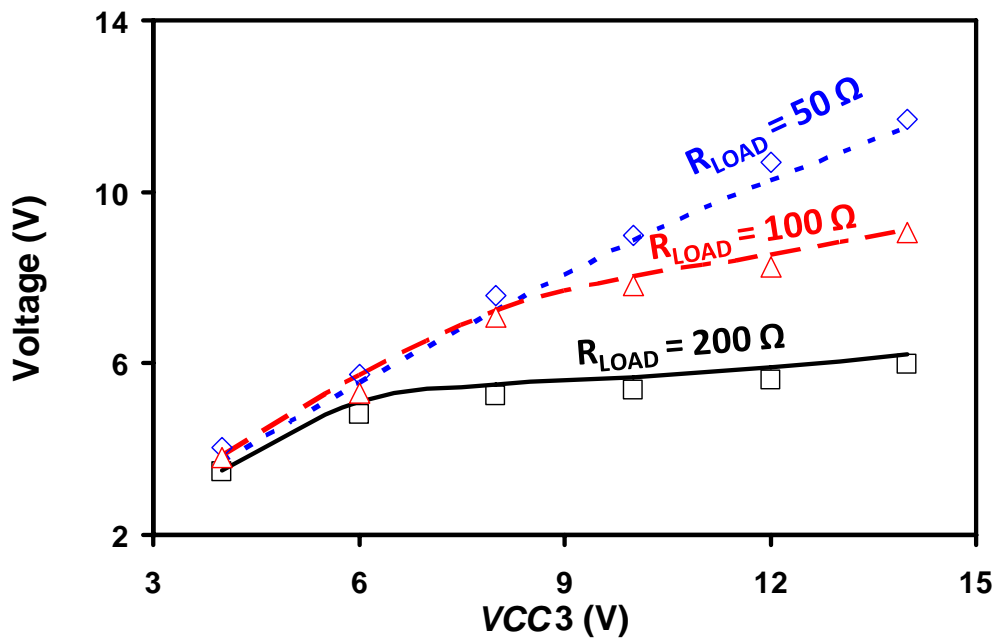


Fig. 5-9 Measured (symbol) vs. simulated (curve) amplitude of impulses generated with $V_{CC1} = 3.3$ V, $V_{CC2} = 6.5$ V, and $V_{CC3} = 4-14$ V.

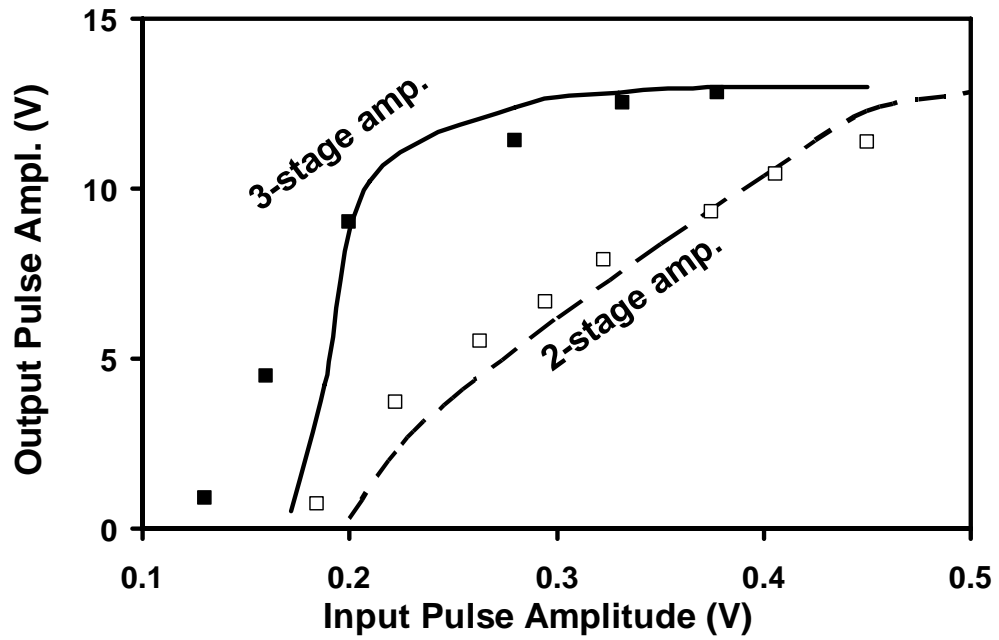
Without adjusting the bias or input conditions, the pulse generator was found to operate similarly well when the ambient temperature was varied from $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$. Fig. 5-5(b) shows that the pulse voltage at Node C is similar at all temperatures except at the highest $VCC3$, when it is limited by the Kirk threshold that decreases with increasing temperature. On the other hand, as shown in Fig. 5-6(b), the minimal pulse width increases with increasing temperature at all $VCC2$ values, because the high-frequency gain decreases with increasing temperature. To further improve the temperature performance of the pulse generator, temperature sensing and compensating circuit can be incorporated to fine tune the bias of the driver stage.

The present pulse generator consumes approximately 120 mW, with 100 mW flowing through the pulse-amplification block. As listed in Table I, the ratio of power consumption over pulse amplitude for the present pulse generator is comparable to that of the pulsed generators made of GaAs HEMTs and Si MOSFETs. The power consumption of the present pulse generator can be reduced by reducing the size of certain HBTs. For example, reducing T1-T8, T9 and T14 from $40\text{ }\mu\text{m}^2$ to $8\text{ }\mu\text{m}^2$ would save 70% of power. Much greater power can be saved by cycling off the pulse amplifier when no pulse is expected. With an on-time of 1 ns and a pulse-repetition frequency of 10 MHz, the power

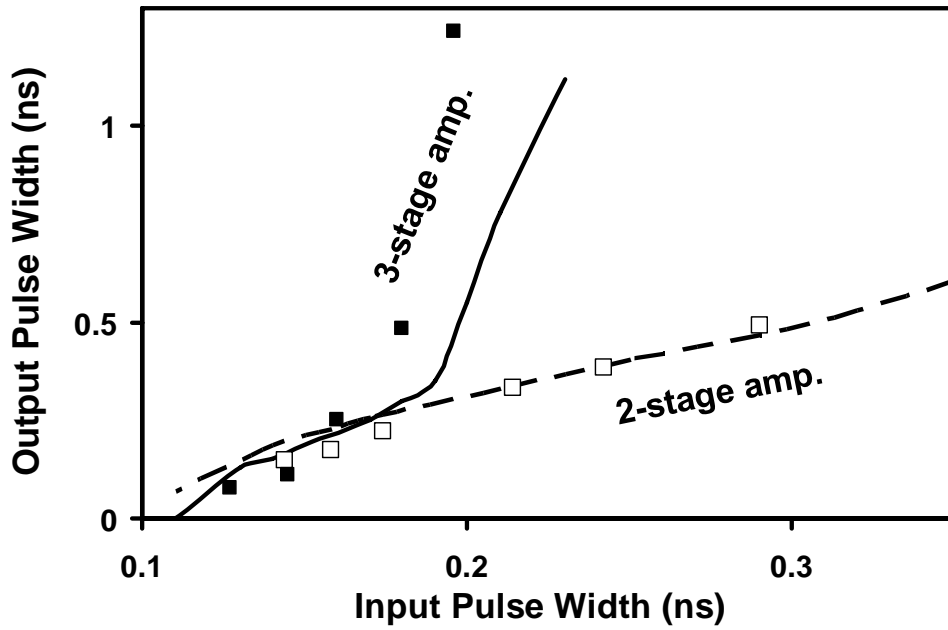
consumed by the pulse amplifier can be reduced by a factor of 100 to approximately 1 mW. The power saving can be even greater at lower pulse-repetition frequencies. At approximately 1 mm², the die costs less than \$1 for volume production.

5.2.2. Multiple-stage impulse amplifier

To help understand the performance of the pulse generators, the performance of the two- and three-stage pulse amplifiers was also evaluated. Fig. 5-10 shows that both pulse amplifiers can deliver more than 11 V of pulse amplitude. The three-stage pulse amplifier has more gain due to the additional stage, but less linearity due to saturation of T8. In contrast, the output amplitude of the two-stage pulse amplifier varies linearly with the input amplitude from 3.7 V to 11.3 V; the output width of the two-stage pulse amplifier varies linearly with the input width from 0.15 ns to 0.5 ns. Fig. 5-11 shows that the output amplitude of the pulse amplifiers is rather stable under different pulse-repetition frequencies between 40 KHz and 25 MHz, which indicates that the isothermal approximation is valid over a wide range of pulse widths and duty cycles. The pulse amplifier is also tested under CW small-signal conditions.



(a)



(b)

Fig. 5-10 Measured (symbol) vs. simulated (curve) (a) output pulse amplitude vs. input pulse amplitude and (b) output pulse width vs. input pulse width. In (a), input pulse width = 0.25 ns. In (b), input pulse amplitude = 0.4 V.

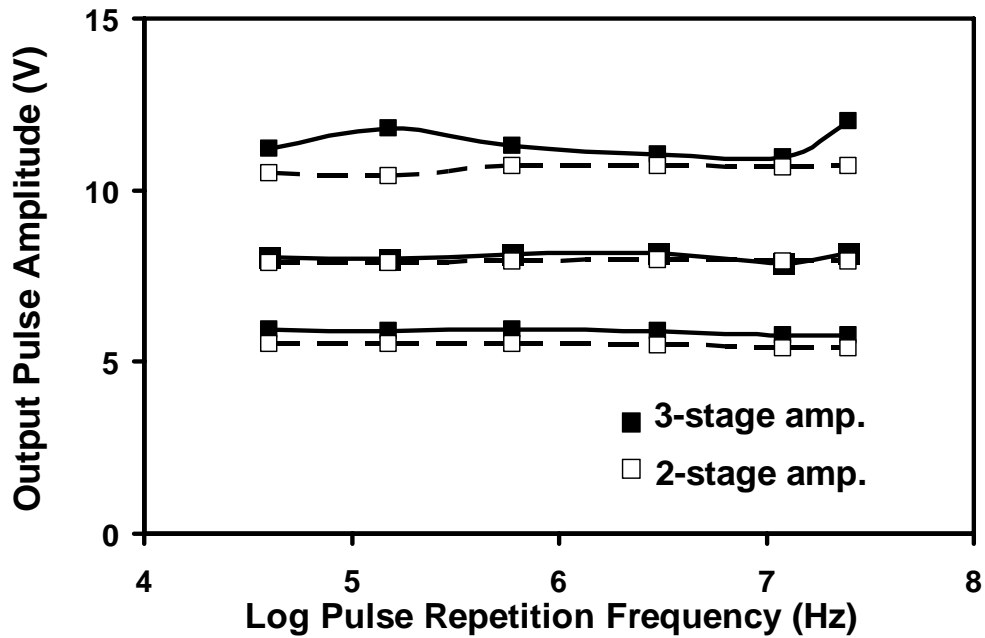


Fig. 5-11 Measured output pulse amplitudes of two- (□) and three-stage (■) pulse amplifiers as functions of pulse-repetition frequency between 40 kHz and 25 MHz. From the bottom up, the inputs for the two-stage pulse amplifier is 0.4 V/0.15 ns, 0.53 V/0.15 ns and 0.4 V/0.2 ns; the input for the three-stage pulse amplifier is 0.27 V/0.24 ns, 0.32 V/0.24 ns and 0.4 V/0.25 ns.

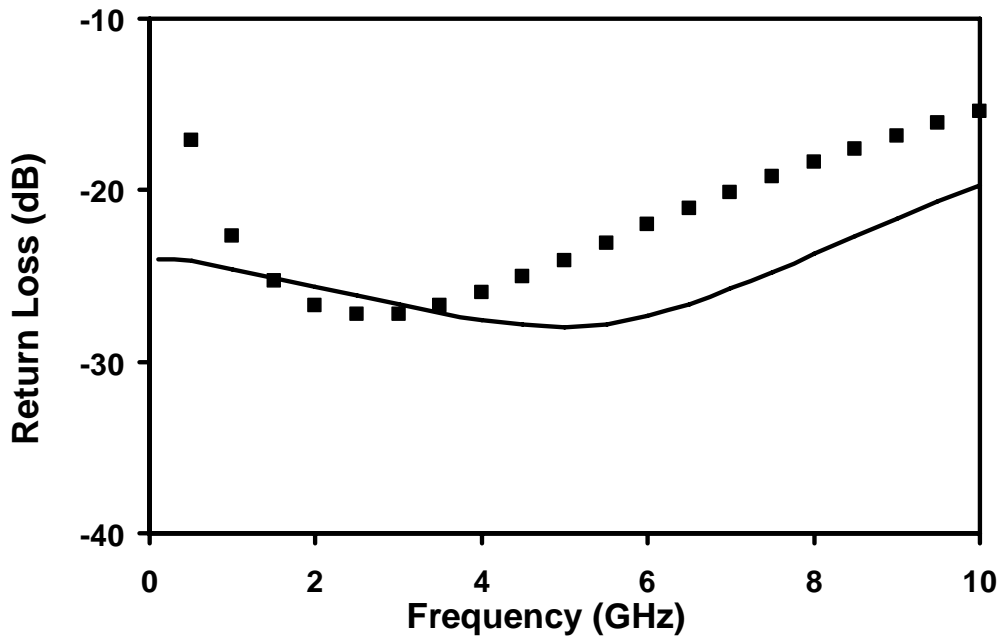


Fig. 5-12 Measured (symbol) vs. simulated (curve) return loss of the three-stage pulse amplifier.

Fig. 5-12 shows that the input return loss of the three-stage pulse amplifier is higher than 15 dB between 0.5 GHz and 10 GHz, which indicates that the 50- Ω shunt resistor indeed helps in wideband matching. The difference between measured and simulated return losses is probably due to underestimation of parasitics. Based on the lessons learned through the pulse amplifiers, the pulse generators achieve high gain and high linearity by incorporating the best features of either pulse amplifier. For example, as shown in Fig. 5-2, the pulse-generation block incorporates the differential amplifier of the two-stage pulse amplifier, while the pulse-amplification block uses two Darlington pairs of the three-stage pulse amplifier.

5.3. Performance Compare

Fig. 5-13 and Table 5-1 compare the performance of the present pulse generators with that of other UWB pulse generators fabricated in GaAs HBTs, GaAs HEMTs, Si BJTs, Si MOSFETs, and Si step-recovery diodes (SRDs). It can be seen that the present pulse generators can generate much higher amplitudes with comparable pulse widths. It was also much more compact than pulsed generators based on step-recovery diodes (SRDs) and other discrete devices.

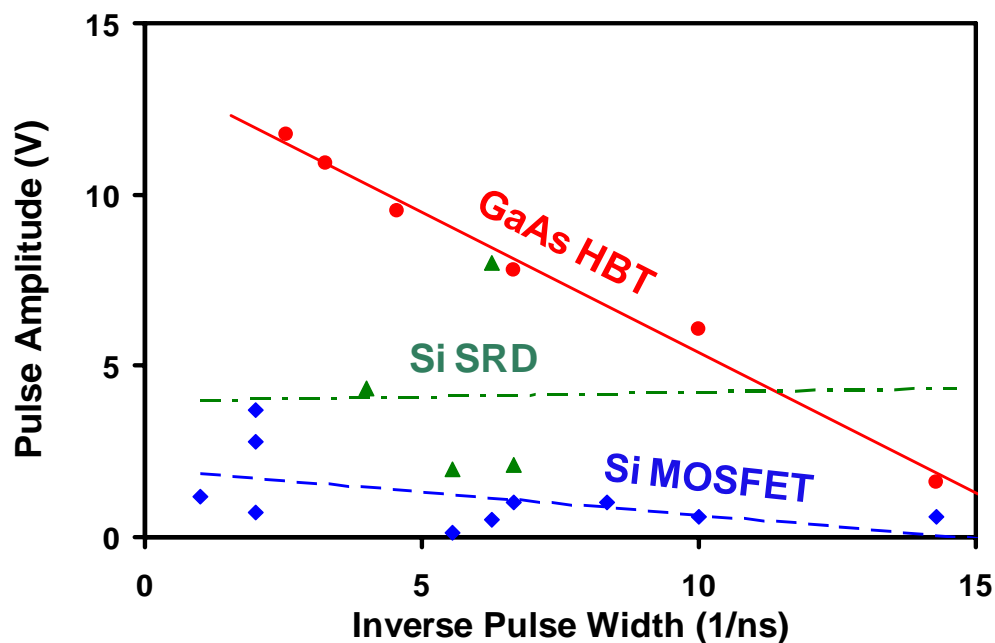


Fig. 5-13 Output pulse amplitude as a function of inverse pulse width for UWB pulse generators of different technologies.

Technology	Waveform	Pulse Amplitude (V)	Pulse Width (ns)	Power Consumption (mW)	Reference
GaAs HBT	Impulse	3.5–11.5	0.25–0.65	120	[3]
	Monocycle	5.1–8.8	0.2–1		
GaAs HEMT	Impulse	0.7	0.06	120	[10]
Si SRD	Impulse	2	0.15–0.7	--	[11]
	Monocycle	8	0.6–1.1	--	[12]
	Impulse	4.35	0.25	--	[13]
Si BJT	Monocycle	1.3	0.5	--	[14]
	Impulse	1.4	0.4	--	[15]
Si MOSFET	Monocycle	0.3–0.6	0.14–0.35	--	[16]
	Impulse	2.8	0.5	--	[17]
	Impulse	1.2	2.0	17	[18]
	Monocycle	3.7	0.5	43	[19]
	Impulse	0.03-0.12	0.07-0.18	0.18	[19]

Table 5-1 Performance of UWB Pulse Generators

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Chapter 6 Conclusion

6.1. Conclusion of dissertation

The pulse mode device characterization and modeling were proposed. The following tasks were accomplished:

- For the first time, GaAs HBTs are characterized under sub-nanosecond pulses. The flyback behavior in the IV curve is observed experimentally, which is only based on the numerical calculation before. Devices can survive in the flyback region which is contrary to previous theory prediction. It is found that the safe operation area under sub-ns pulses is larger than that under μs pulses and DC.
- Based on the measured sub-ns characteristics, current dependence is empirically added to conventional voltage-dependent impact-ionization model, which accurately predicts the pulse I-V behavior and large signal performance under high collector bias condition.
- A method is developed to predict the upper limit of the device maximal output power by using sub-ns SOA boundary. It is experimentally verified that this method is effective in predicting maximal output power for high efficiency amplifier, such as Class C amplifier.
- For low-duty-cycle high-peak-power ultra-wideband applications, a sub-nanosecond greater-than-10-V tunable pulse generator was designed by taking advantage of the

recent discovery of much greater output capacity of GaAs HBTs under sub-nanosecond isothermal operation. The output pulse amplitude can vary linearly between 3.5 V and 11.5 V while maintaining the pulse width at 0.3 ± 0.1 ns. Alternatively, the pulse width can vary linearly between 0.25 ns and 0.65 ns while maintaining the pulse amplitude at 10 ± 1 V. These results show that the present pulse generator has much higher output capacity than those fabricated in CMOS ICs and is much more compact than those fabricated in SRDs or other discrete devices are.

6.2. Recommendation of future research

In chapter 2, all research results are mainly based on a single finger device. In practice, multi-finger device is more widely used in high power and high frequency applications. It has been found that in GaAs-based heterojunction bipolar transistors high power density operation is limited by thermally induced current hogging effects which confine device performance below the theoretical electrical limits[1][2]. By using sub-nanosecond test set-up, we can study other potential issues which may introduce the unbalance between finger and finger besides the self-heating effect. The final result will help the device designer to optimize the device geometry.

In chapter 4, the sub-nanosecond SOA boundary is used to forecast the maximal output power of class C amplifier only. To forecast output power of Class A and Class AB amplifier, we need to combine the impact ionization boundary with the thermal heating

boundary. Because Class AB amplifier has lower efficiency than the Class C amplifier, more heat is generated with the same DC power consumption.

The reliability of GaAs HBTs for power amplifiers can be another direction in future. Impact ionization boundary can be used to forecast the output power. How long the device can work under the maximal output power condition without degradation is also worth investigating [3] [4].

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Appendix I Extracted InGaP/GaAs HBT Device model parameters (Agilent HBT Model)

Tnom=25.0	Vaf=870
Aeal=1	Var=1000
SelfTmod=1	Isa=635.3e6
Re=1.27	Na=1.0
Rci=1.0	Isb=1e7
Rcx=2.9	Nb=1.0
Rbi=1.3	Ikdc1=0.002
Rbx=5.2	Ikdc2Inv=1.315
Is=3.0e-25	Ikdc3=0.00359
Nf=1.02	VkdcInv=0.02
Isr=4.50e-25	Nkdc=1.151
Nr=1.02	Gkdc=0
Ish=2.74e-26	Ik=6.958
Nh=1.066	Cje=5.44e-14
Ise=2.74e-30	Vje=1.27
Ne=1.999	Mje=0.05
Isrh=3.81e-15	Cemax=1.26
Nrh=2.04	Vpte=1.5
Isc=3.6	Mjer=0.05
Nc=2.05	Abex=0
Abel=0	Cjc=4.5

Vjc=0.6	Vktr=1
Mjc=0.1725	Vkmx=10
Ccmax=6.09	Fexke=0.326
Vptc=2	Tr=2.31e-6
Mjcr=0.41	Cpce=3.94e-14
Abcx=0.82	Cpbe=3.39e-14
Tfb=3e-13	Cpbc=1.7e-15
Fextb=0.2	Xrb=0
Tfc0=7.8e-12	Xrc=0
Tcmin=1.25e-12	Xre=0
Itc=0.00245	Tvje=0
Itc2=0.0075	Tvpe=0
Vtc0Inv=0.13	Tvjc=0
Vtr0=0.1615	Tvpc=0
Vmx0=0.17	Tnf=144.6e-6
VtcminInv=0.7128	Tnr=60e-6
Vtrmin=4.496	Ege=1.424
Vmxmin=0.17	Xtis=5.1
VtcInv=0.536	Xtih=3.96
Vtc2Inv=0.02	Xtie=3
Fextc=0.7313	Egc=1.8
Tkrk=4.29e-12	Xtir=3
Ikrk=0.015	Xtic=3
Ikrktr=1e-6	Xtirh=4
Vkrk=4.48	Xtik3=0
Vkrk2Inv=0.001	Eaa=0
Gkrk=1.9193	Eab=0

Xtfb=0	Xth1=5.0
Xtcmin=0	Rth2=0
Xtfc0=0.67	Cth2=0
Xitc=-5	Xth2=0
Xitc2=-3	N=2
Xtkrk=-0.8	BVCBO=27
Xikrk=0.1	MI=10
Xvkrk=5.0	KI=5
Kf=0	IL=0.005
Af=0	
Ffe=1.0	
Kb=0	
Ab=1.0	
Fb=1.0	
Imax=10	
wBvbe=0	
wBvbc=0	
wVbcfwd=0	
wIbmax=0	
wIcmax=0	
wPmax=0	
Version=2.0	
Lpe=3.49e-11	
Lpc=1.35e-11	
Lpb=4.5e-11	
Rth1=1200	
Cth1=7.0e-10	

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