

2007

An integrated transimpedance ion channel current CMOS amplifier

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An Integrated
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Ion Channel
Current CMOS
Amplifier

May 2007

**AN INTEGRATED TRANSIMPEDANCE ION CHANNEL
CURRENT CMOS AMPLIFIER**

by

Akwete S. Bortei-Doku

A Thesis

**Presented to the Graduate and Research Committee
of Lehigh University**

**In Candidacy for the Degree of
Master of Science**

in

Electrical Engineering

Lehigh University

May 2007

This thesis is accepted and approved in partial fulfillment of the requirements for the Master of Science

April 24, 2007
Date

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Acknowledgements

I would like to express my heartfelt gratitude to my advisor, Dr. Marvin White, for his continued support, his much needed guidance and his invaluable words of encouragement during my academic journey. I consider it a great privilege to have had him as my advisor for both my undergraduate and graduate studies at Lehigh University.

I would also like to say a big thank you to my wonderful and beautiful wife, Amerley Bortei-Doku, without whom my academic progress thus far would not have been possible. Her ingenuity and drive have kept me on my feet even when the road has been the roughest. May she keep up her good work.

I would also like to acknowledge all the help and support I have received from my research colleagues and friends, especially Santosh K. Pandey, Eric Winokur and Andrew Potter and Rajiv Mehrotra.

I wish to thank Ps. Gilbert Fleischer, my pastor, for his priceless fatherly advice. Also to the Olives, the church choir I am a part of, and to the instrumentalists at Lighthouse Chapel international, I say a big thank you for all the wonderful time we have had and continue to enjoy together.

Finally, I wish to say a big thank you to my parents, Dr. and Mrs. Samuel Bortei-Doku, and my siblings for all the prayers and encouragement.

My biggest thank you goes to God for everything, for without Him; I am and can do absolutely nothing.

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Figure A1: Screenshot of PCB layout diagram.

Abstract

Ion channels are tiny biological switches embedded in the membrane of biological cells and play a vital role in our body's neural communication. While ion channel research is a number of decades old, the common technique used to measure current flow through these biological switches, called pipette patch clamping, has seen slow progress. Patch clamp amplifiers operate, with a multiplicity of ion channels in the whole-cell mode, by sensing the voltage across a resistor in a transimpedance amplifier. This is a reasonable approach because whole cell currents are typically 1-10nA and can be handled with resistors in the range of 10-100M Ω . However, in the single ion-channel detection mode, the currents are typically 1-5pA and to obtain reasonably large gains for these small currents, the resistors used in these amplifier circuits need to be of the order of a few gigaohms. These resistors are difficult to come by, display instabilities, characterized by large excess noise, and are not available to be incorporated into an integrated circuit.

In this research, we investigate a novel integrated CMOS instrumentation amplifier with an input amplifier that senses the charge on a feedback capacitor – a capacitor that replaces the resistor in a transimpedance amplifier. This is equivalent to performing an integration operation on the input current. The output signal from the input stage is differentiated with discrete differentiation performed on the integrated circuit chip through Discrete Analog Signal Processing (DASP).

The CMOS amplifier, fabricated by MOSIS using AMIS 1.5 μ m n-well CMOS process technology with 1 metal layer and 2 poly layers, achieved amplification for currents as low as 50pA at 2kHz, which is one order of magnitude above our target input

current level. Characterization of the operational amplifier used on chip showed a bandwidth of 1.4MHz, and input referred DC offset voltage of 11 μ V and a slew rate of 0.5V/ μ sec.

This study holds much promise for pharmacological advancements relating to the invention and testing of new and improved drugs. By understanding ion channel reactions to medication administered to the body, drugs can be produced specifically to suit individuals with peculiar traits.

Chapter 1

Introduction to Ion Channels

1.1 Motivation and Objective

Ion channels are minuscule nanopores located in the cell membrane through which electronically charged particles, such as sodium, potassium and calcium enter and exit the cell's body. Ion channels can occur in thousands or tens of thousands on a single cell alone¹. By opening and closing like an electrical switch, ion channels regulate the distribution of ions on the opposite sides of the cell membrane. This mechanism allows the biological cell to communicate with neighboring cells².

The flow of ions through the ion channel can be considered as a measurable electrical current that can be monitored using an experimental technique called *patch clamping*³. These current pulses are challenging to measure because of their minuteness, in the order of 5-10pA at 2-2.5kHz^{4, 5}. The recorded current is amplified using a transimpedance amplifier for further research.

Ion channel research is important because it has been shown that ion channel behavior can adversely affect otherwise seemingly healthy patients. From the examination of patients' genes, researchers have shown that many types of episodic disorders trace their source back to irregular ion channels⁶.

New findings are leading to a better understanding of how ion channels maintain the function of the body and the brain. Since many illnesses are turning out to have dysfunctional ion channels as their common underlying problem, it may be possible to treat a wide array of seemingly diverse ailments by treating one type of ion channel defect. A better understanding, therefore, of the gating mechanisms of ion channels and their response to stimuli could provide breakthroughs in the research and treatment of many diseases. Drugs could eventually be tailored to treat patients with specific ion channel defects as these could be made to target the defective ion channels directly⁷.

Ion channel current sensors integrated with amplifier units exist that replace the traditional patch clamp setup with more efficient current measuring techniques, but these systems suffer from high costs. One of our goals is to develop a small reproducible System-on-Chip (SoC) setup that performs the function of positioning the cell, establishing a bond with the cell, sensing the electrical current and amplifying it to levels that can be studied. This system could be further developed to allow parallel processing of multiple ion channel currents to produce faster ways of characterizing ion channels.

1.2 Outline of the Thesis

This thesis will present a discussion of an innovative CMOS transimpedance amplifier circuit which senses ion channel currents and uses integration and differentiation to amplify the currents to about 100mV where they can be viewed and analyzed. This amplifier will then be integrated with a planar patch clamp system to measure ion channel currents.

Chapter 2 presents a brief discussion on the history of ion channel research as well as different types of ion channels

Chapter 3 focuses on the micropore structure that forms the planar patch clamp used to establish a tight seal with the cell. The fabrication steps involved in making the metal electrode chips will also be explicated. Dielectrophoresis, the technique used for cell positioning, will be described briefly.

Chapter 4 explains how the nine stages of the amplifier chip circuitry work. Also discussed will be the tests and simulations that have been conducted on the amplifier chip so far. The development of the test setup on a Printed Circuit Board will also be discussed.

Chapter 2

Electrophysiology

2.1 History of Ion Channel Research

A cell is the most basic living unit. It possesses in itself the ability to perform all the activities associated with living things, including reproduction, growth and response to stimuli. The cell is surrounded by an outer cell membrane that is permeable to water, but is only partially permeable to other materials like glucose. Owing to the hydrophobic nature of the cell membrane (Figure 2.1), it is impermeable to charged ions which are very important to the cell. Ion channels interspersed all over the cell membrane grant access ions into and out of the cell's body.

Electrophysiology is a term used to describe the study of the electrical properties of a biological cell. The existence of the cell's electrical properties was reasonably well established by the end of the nineteenth century when a Spanish histologist, Ramon Cajal demonstrated the activity of neurons in the body⁸. Techniques were gradually developed to use specially produced microelectrodes to impale the cell to make electrical

measurements. Bert Sakmann and Erwin Neher refined this technique by introducing the use of glass pipettes and suction to make electrical measurements³, and won the Nobel Prize in 1991 for their work. This new technique replaced the sharp electrode with a rounded tip pipette with the ability to adhere to the cell. Using the glass pipette, however, required a skilled technician and produced very low throughput.

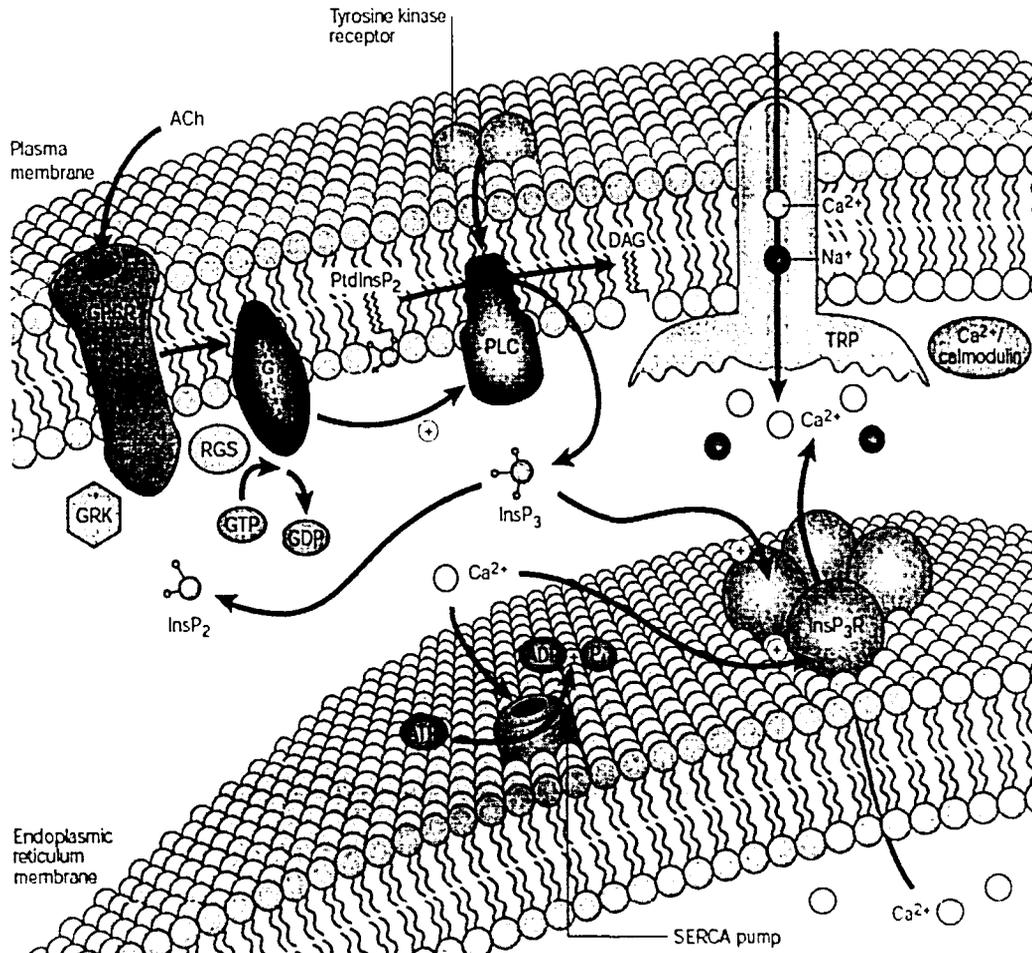


Figure 2.1: Ion channels are embedded in the cell membrane. The outer layers of the cell membrane is hydrophilic while the inner layers are hydrophobic, preventing the passage of ions.

The traditional patch clamp method has been replaced by other setups mainly characterized by a pipette replacement in the form of a microsized hole etched in a planar

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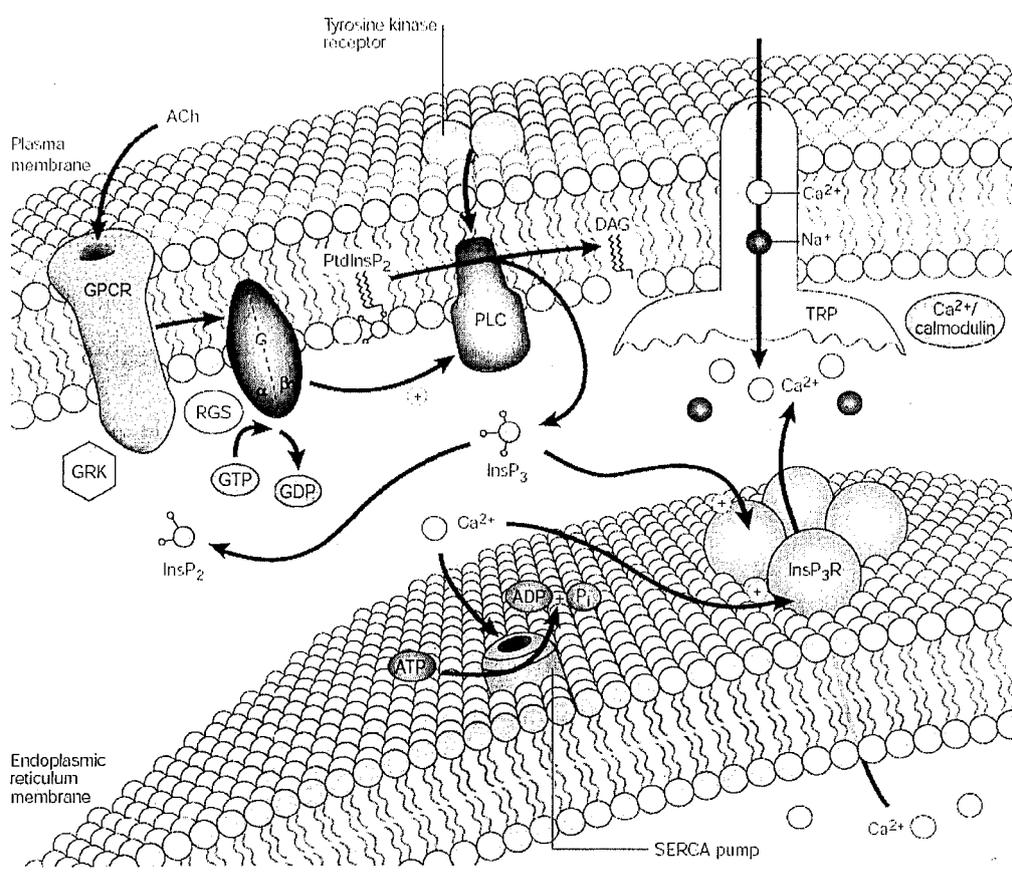


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The traditional patch clamp method has been replaced by other setups mainly characterized by a pipette replacement in the form of a microsized hole etched in a planar

surface. These holes have been etched or micromachined in glass⁹, quartz¹⁰, coated silicon nitride¹¹, and treated elastomers¹².

One advantage of the planar patch clamp system is the ease with which it can be automated. For this reason, several planar patch clamp devices are being developed into commercial products for pharmaceutical drug screening. One example that presents a system different from the hole-in-chip design is a nozzle-like projection fabricated to contact the cell¹³ (Figure 2.2a).

Whereas other methods hinder visual access to the patch, the nozzle structure facilitates the visualization of the patched membranes. The nozzles are created using Deep Reactive Ion Etching (DRIE) in an SOI Wafer. The projection is made from Silicon dioxide and the inner surface is coated with Silicon Nitride for better seal formation. Though this particular study showed ease of formation of gigaseal through the simple application of negative suction pressure, the recorded seal resistance was shown to be very high even after the cells were removed. This high residual seal resistance was believed to be due to the holes being choked with debris.

In another study which takes advantage of the visual monitoring of cells, the platform used was created by micromolding elastomers to form an array of capillaries which was then coated with polydimethylsiloxane (PDMS). A seal is made with cells loitering within 100–200 μ m of the capillary openings in less than 3s by applying 14–21 kPa of negative pressure to the patch channel. The negative pressure is then reduced and replaced with an electrical seal with the patch channel orifice¹⁴ (Figure 2.2b).

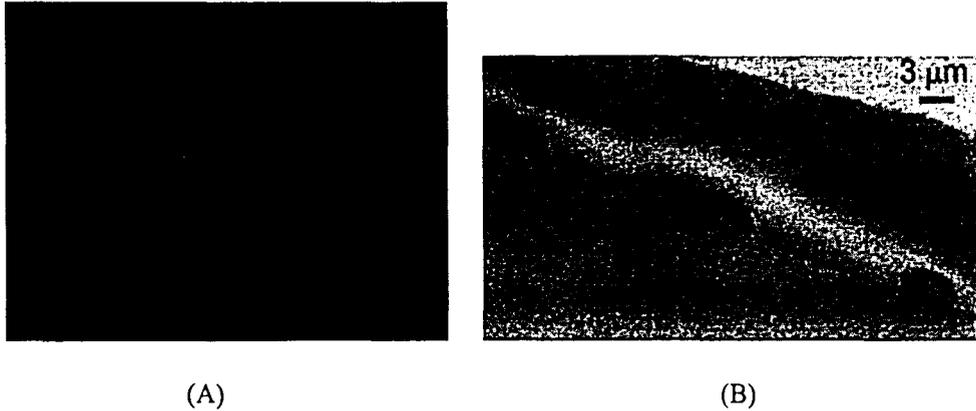


Figure 2.2: (A) Scanning electron micrograph of nozzle and surrounding well. (B) Scanning electron micrograph of three recording capillary orifices

This technique yielded seal resistances of up to $1.2 \text{ G}\Omega$. From the point of view of the objective lens, the trapped cell and the capillary are in the same plane. The main advantage of the above setup is its replacement of the vertical hole with a horizontal one, allowing the use of simple microscopic techniques to be used to monitor the entire experiment from directly above the entire process.

2.2 Types of Ion channels

Ion channels can be viewed mainly as switches which open and close, very much like CMOS switches (Figure 2.3). Most types are selective, allowing passage by only certain specific ions over others while others allow several types of ions through them. Ion channels can be differentiated by their modes of activation. While some ion channels like Sodium and Calcium ion channels found in muscle cells respond to a change in their transmembrane potential, others like Nicotinic Acetylcholine receptors respond to the proximity of specific ligands to the cell membrane.

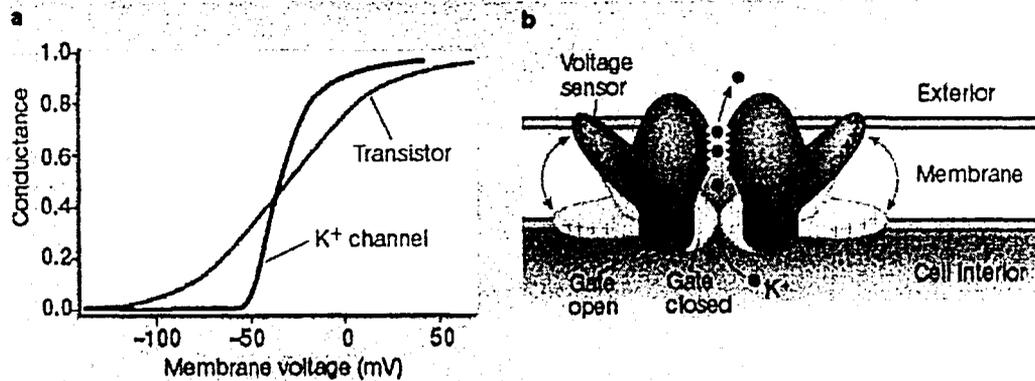


Figure 2.3: Ion channels act as switches which open when the transmembrane potential is increased. They stay shut for voltages smaller than the transmembrane potential.

Our experiments are applicable to voltage gated channels. These usually have a transmembrane resting potential of about 60mV. Maintaining the transmembrane potential below this resting potential keeps the ion channel closed whereas an increase switches the ion channel to the open position. Increasing the transmembrane voltage does not increase the flow of ions or the current through the ion channel, but increases the probability that the ion channel will remain open².

Chapter 3

BioMEMs and Microfluidics

3.1 Patch Clamping

Early methods used to study ion channel currents involved using a sharp microelectrode to impale the cell. This method, called intracellular recording, was replaced by pipette patch clamping³. This newer technique introduced the use of a specially formed glass pipette, which was brought into contact with the cell membrane. Through the use of suction, a section of the cell membrane, called the patch, formed a tight seal with the microscopic pipette tip and allowed recordings to be made.

The use of fine micropipettes allowed the study of single ion channels at a time. Further suction could rupture the patch, exposing the intracellular fluid to the contents of the glass pipette, allowing for whole-cell recordings to be made. The latter technique provides a general picture of the behavior of a large group of ion channels or even the entire cell to environmental changes.

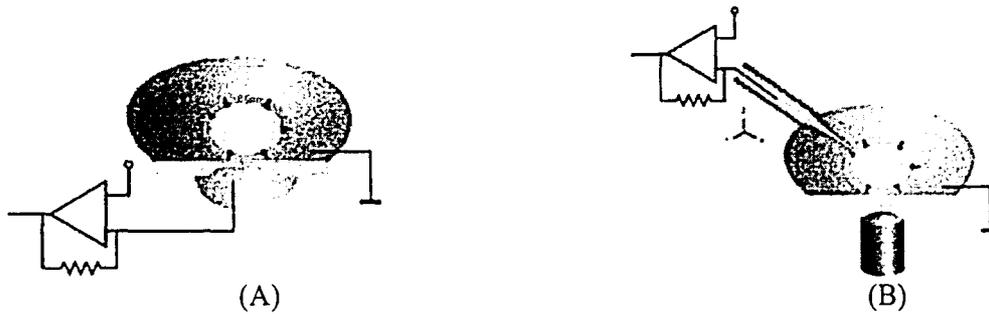


Figure 3.1: (A) Schematic drawing of the classical patch clamp configuration. The patch pipette is moved to the cell using a micromanipulator under optical control. Relative movements between the pipette and the cell have to be avoided in order to keep the cell-pipette connection intact. (B) In planar patch configuration, the cell is positioned by suction. Relative movements between cell and aperture can then be excluded after sealing. An antivibration table is not necessary.

The traditional patch clamp technique has recently been replaced with the planar patch clamp method in which the glass pipette is replaced with a horizontal surface with tiny pores to serve as the pipette tip [reference]. The advantage of the planar patch clamp method is the elimination of highly skilled electrophysiologists required to perform traditional patch clamp experiments. Microfluidics can also be exploited to better control the intracellular bath solutions to match realistic cell environments as best as possible. This newer technique (Figure 3.1b) allows stable recordings to be made and creates the possibility for parallel current processing. Through suction, the cell can adhere tightly to the micropore the same way it adheres to the glass pipette in pipette patch clamping.

3.2 Patch Clamp variations

Patch clamp recording techniques include the cell-attached patch (Figure 3.2a) in which a seal is formed and maintained between the cell membrane and the micropipette tip. This technique is used when studying the effects of drugs on ligand-gated ion channels. The drug to be tested is mixed with the pipette solution before seal formation. Voltage gated channels are also studied this way. The whole-cell recording technique

(Figure 3.2b) involves applying additional suction to rupture the cell membrane. This reduces the resistance between the cell and the electrode and provides better electrical access to the cell.

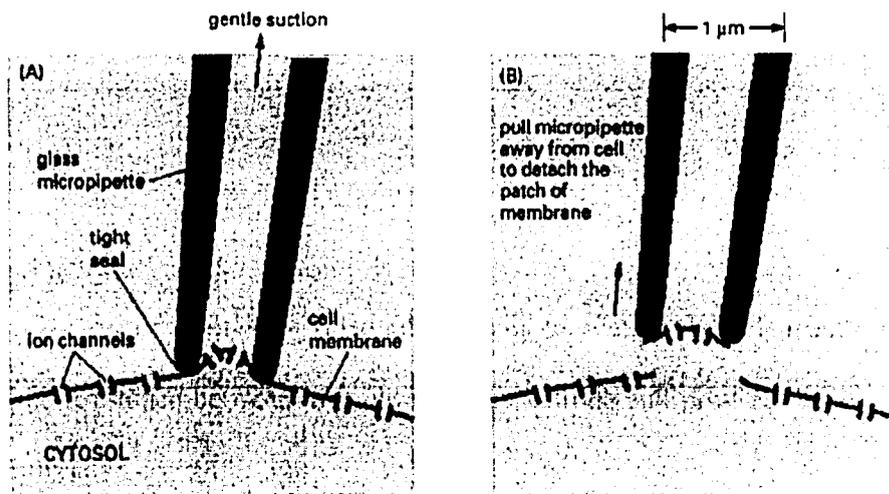


Figure 3.2: The technique of ion channel recording using glass pipettes and suction. Diagram showing (A) cell attached and (B) whole cell cases?

The inside-out patch technique involves quickly lifting the electrode after the initial seal formation to expose the intracellular solution to the extracellular solution. This technique allows researchers to study the effects of environmental changes on ion channel behavior. Ligand-gated ion channels are often studied this way.

In the outside out patch method, the electrode is pulled away from the cell in such a way that the patch left in the pipette rolls up and forms a ball, with the outside of the cell membrane forming the surface of the ball. This is used to study ion channel activity in a protected environment that is different from its usual fluidic environment¹⁵.

3.3 BioMEMs Chip

One of two chips fabricated for this research project is the planar patch clamp chip fabricated in our lab at Lehigh University. This chip serves as the platform on which the cell solution is placed during gigaseal experiments. Normal fabrication procedures could not be followed because these chips were coated with thin strips of metal which melt easily at high temperatures. The fabrication procedure is outlined in the next section.

These chips are impaled to create pores which are a few microns in diameter. The central position of this pore and the four metal electrodes allow the cell to be positioned above the micropore using a technique called Dielectrophoresis. In this process, varying electric fields applied to the electrodes cause the polarizable cells to be drawn either towards or away from the central pore. With this technique, cell trapping can be achieved in a few seconds.

3.3.1 Biochip Fabrication Sequence

The fabrication process begins with a 330 μ m double-sided, (100), p-type, 15 ohm-cm polished silicon wafer¹⁶. The subsequent steps are outlined below.

- Wet, thermal Oxidation at 1000°C for 60 minutes (1200Å of oxide)



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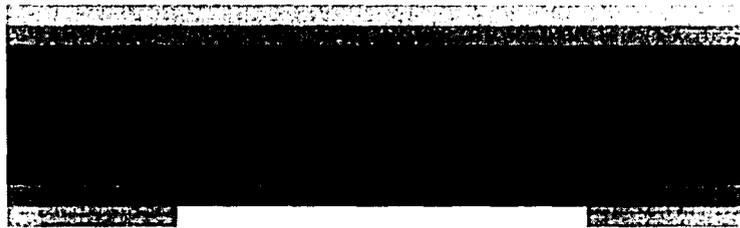
- Wet, thermal Oxidation at 1000°C for 60 minutes (1200\AA of oxide)



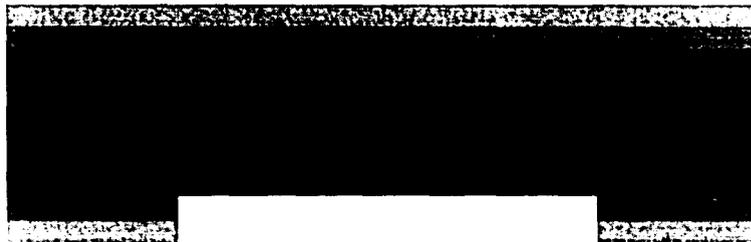
- LPCVD Silicon Nitride Deposition at 800°C for 65 minutes (1200Å of nitride)



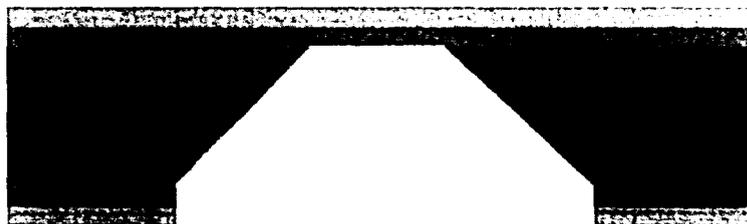
- Plasma Etching of the Silicon Nitride for 300 seconds, which takes away all the nitride at the backside and approximately 200Å from the front side.



- Buffered HF dip of the wafer for 5 minutes to remove the oxide from the backside. The silicon nitride on the front side is relatively unaffected by the buffered HF solution.



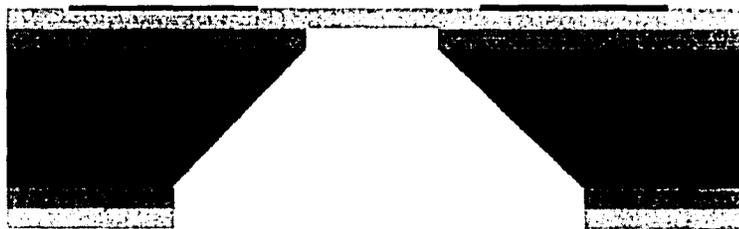
- Silicon etching in 20% KOH at 80°C for 6 hours.



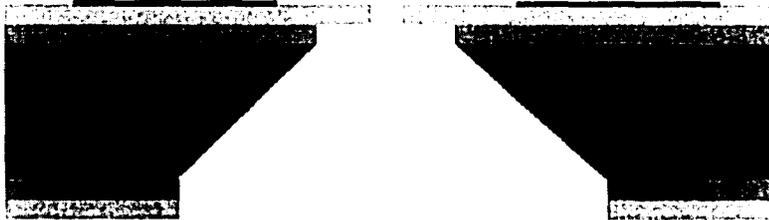
- Buffered HF dip of the wafer (5minutes) to remove the oxide below the nitride.



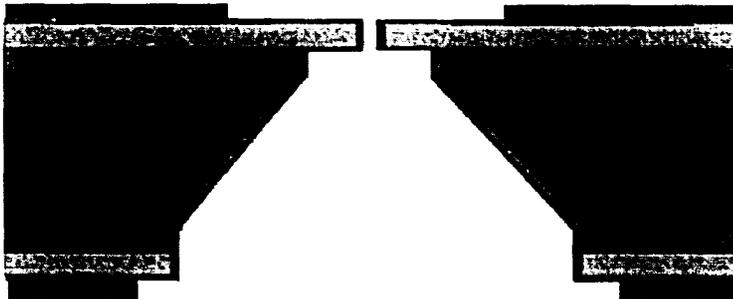
- 200Å Ti/ 800Å Pt deposited as quadruple electrodes on the front-side.



- Micropore drilled through the nitride membrane using Plasma Etch/FIB.



- Silicon oxide deposition through sputtering (300Å of oxide) and a SU-8 layer to form the fluid chambers.



3.3.2 Teflon Block

The BioMEMS chips which serve as the planar pipettes are placed on a Teflon block structure for seal formation and current reading experiments. The structure of a typical planar patch clamp platform is shown in Figure 3.3. Our test setup is shown in Figure 3.4. Using a planar pipette offers better control of the extracellular bath solution during experiments. In our experiments, the internal baths of this block is filled with the same Bovine solution used in preserving the cells.

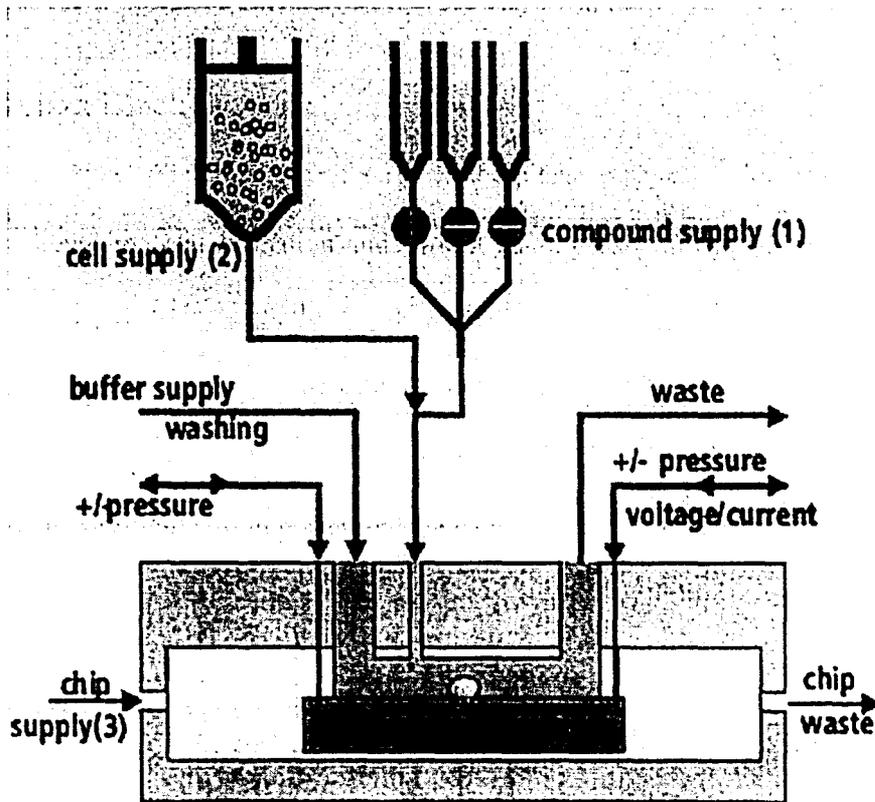


Figure 3.3: Model of a planar patch clamp platform. Bath solutions are recycled to keep solutions fresh and lengthen the duration of experiments.



Figure 3.4: Test setup for planar patch clamp measurements.

One of the goals of this research project is to eventually fabricate a single integrated unit that will combine the cell positioning, seal formation, current measuring and amplification functions into one device that could be produced commercially. This integration will greatly reduce noise due to lead lengths. The Teflon block will serve as a good starting point for housing a prototype of the final product.

Chapter 4

Integrated Transimpedance CMOS Amplifier

4.0 Introduction

This chapter discusses how the nine stage of the amplifier chip work together to amplify the low-level ion channel current to a much higher voltage level. The Printed Circuit Board used in the test process and the modifications made to the latest revisions of the chip will be presented.

4.1 Amplifier chip

Most amplifiers designed for characterizing ion channels use a transresistive amplifier to convert the small ion channel input current to about a hundredth of a volt. This particular configuration poses the problem of needing very high value resistors (in the order of a few gigaohms) to convert very small ion channel current pulses to reasonable levels where they can be studied. The Johnson-Nyquist noise due to a resistor of this magnitude, given by $4kTR\Delta f$, can be high enough to render the input current

undetectable. Large resistances are often characterized by excess noise and instability. Also, due to space constraints, such large size resistors cannot be realized on chip. Developing patch clamp amplifiers on a chip makes it possible to incorporate them in large numbers for automation and parallelization¹⁷. The sizes of capacitors needed to perform the integration functions on the other hand are just small enough to fit on a small portion of the integrated chip (IC).

The chip is fabricated by MOSIS using an AMIS 1.5 μ m n-well CMOS process technology with 1 metal layer and 2 poly layers. A diagram of the amplifier chip is shown in the figure below. This chip is packaged in a 40pin dual in-line package (DIP).

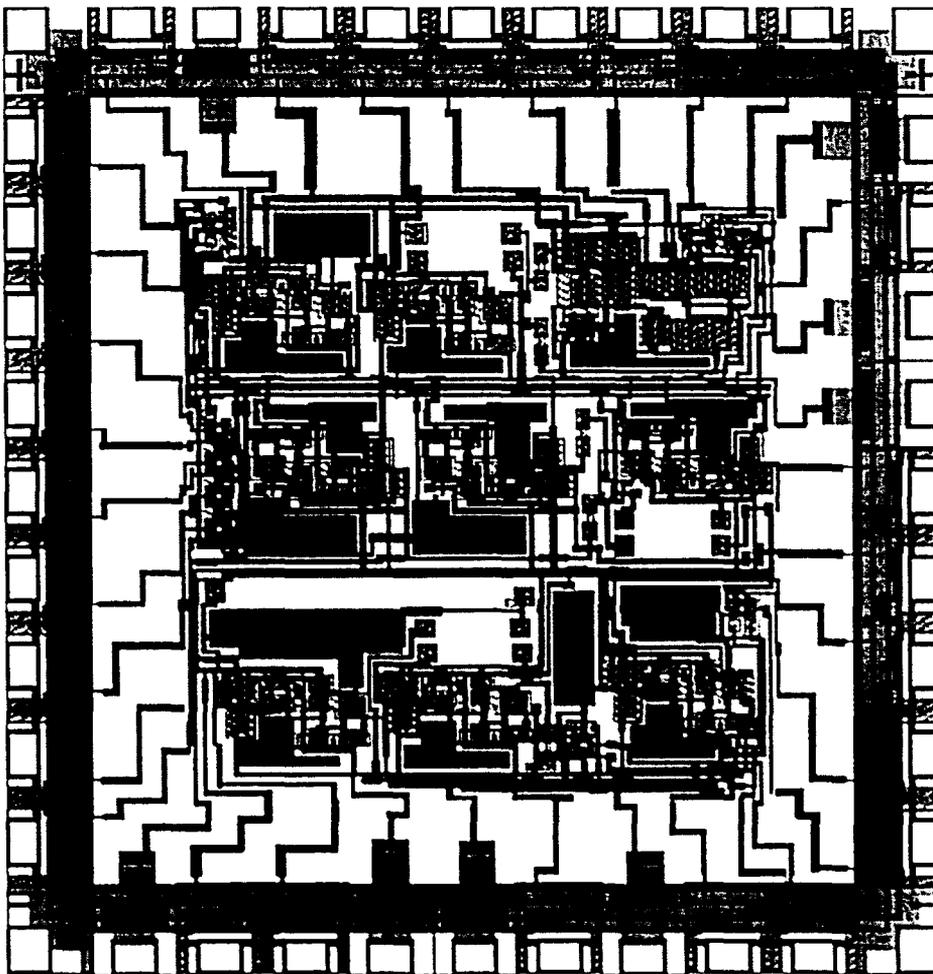


Figure 4.1: CMOS instrumentation amplifier fabricated by MOSIS in their AMI foundry with the SCMOS n-well technology.

4.1.1 Amplifier Stages and their functions

The amplifier circuit is essentially a current to voltage converter, sensing very low currents of about 5-10pA at 2-2.5kHz to voltage levels that can be observed on an oscilloscope¹⁸. Overall, the amplifier can be characterized as a transimpedance converter with 'effective' resistance in the Gigaohm range. A schematic drawing of the amplifier circuit is shown below. I_{SIG} represents the current source which models the current from the ion channel. This input current is integrated by the capacitor C_F when the switches ϕ_C and ϕ_R are closed and open respectively. The value of C_F is chosen to keep the opamp in the headstage from clipping. The size of the capacitor placed on chip is 0.6pF but the effective integrating capacitance is adjusted by connecting an off chip capacitor in parallel with C_F , which determines the overall gain and dynamic range of the amplifier. When the value of the shunt capacitor is made smaller, the integrator sums the current faster and supplies more gain to the input signal.

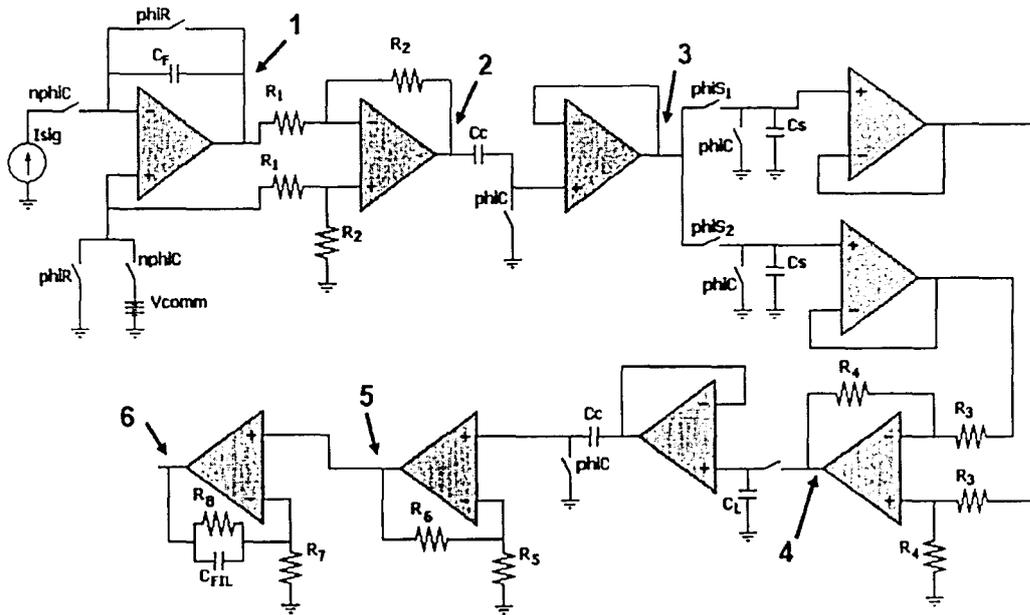


Figure 4.2: Schematic drawing of stages of amplifier circuit.

The value of the shunt capacitor can be varied for different values of the input current, making the amplifier useful for both whole cell and single cell current applications. With an incoming current, the voltage across the integrating capacitor is given by

$$\begin{aligned}
 V_F &= \frac{-1}{C_F} \times \int_{t_{RB}}^t I_{SIG}(T) dT \\
 &= \frac{-I_{SIG}}{C_F \times f}
 \end{aligned}$$

where C_F is the effective feedback capacitor value, ϕ_R , I_{SIG} and f is the sampling frequency. Thus, decreasing the size of the integrating capacitor increases the gain of the headstage. Closing ϕ_R discharges the capacitor and prevents the signal from clipping and therefore resets the amplifier for subsequent readings.

The non-inverting terminal of the headstage is offset by a command voltage which is applied across the cell membrane to activate the voltage gated ion channel. This

DC bias voltage is removed by a subtraction operation in the second stage. The difference stage has a gain of 10 to improve the SNR of the circuit.

The output of the second stage is capacitively coupled to a buffer amplifier where Correlated Double Sampling (CDS) is performed¹⁹. CDS is accomplished in this stage by taking two samples of the incoming signal during each of two clock cycles. Any offset voltages present in the circuit are stored on the clamp capacitor during the first sampling operation and then subtracted from the next sample containing both the signal and the same offset voltages recorded previously. The output of the third stage produces a signal void of any signal degrading offset noise from the preceding stages. To enable the CDS function to be performed effectively, the new set of amplifier chips were modified to have ϕ_C and ϕ_R as two separate clocks, where one is a delayed version of the other.

To recover the original signal, the integrated signal from stage 3 is differenced discretely (sampled) with two alternating high frequency clocks, ϕ_{S1} and ϕ_{S2} , each at 16 kHz. The sample and hold signals from these two clocks are stored on two separate capacitors and passed through two separate buffers. Differentiation is then fully achieved by taking the difference of the two sampled signals in the next stage. The key in this method is to have both capacitances be identical as well as the gains of the buffers. The output of the discrete differentiator is given by

$$V_F = \frac{1}{C_F} * \frac{R_4}{R_3} \int_{t-\Delta t}^{t+\Delta t} I_{sig}(T) dT = \frac{R_4}{R_3} * \frac{I_{sig}}{C_F} \approx \frac{1}{f}$$

The ratio R_4/R_5 is currently set to ten. To retrieve a voltage replica of the input signal, a third sampling operation is carried out using the ϕ_{S3} clock, a delayed version of ϕ_{S1} . This clock samples and holds the peak value of the difference of the two discrete differentiation samples, yielding a pulse, which looks like the original input signal. A

second CDS operation removes any offset voltages due to the opamps in the discrete differentiation stages. The last stage is a low pass filter with cutoff frequency set at 6 kHz to remove high frequency clock feed throughs. This cut-off frequency was too high in our first set of amplifier chips, rendering the filter stages dysfunctional. The final filtering operation had to be performed off chip.

4.2 Test Setup for Evaluation of the CMOS Amplifier

The experimental setup included a Keithley 6221 AC/DC current source capable of sourcing currents as low as 2pA at 100 kHz. So far, we have been able to amplify currents as low as 50pA at 5 kHz. With a custom-designed Printed Circuit Board (PCB) (Figure 4.3), the different subcircuits needed to run tests on the amplifier have been assembled on one portable device, making testing and debugging quicker and much easier. This PCB, fabricated by Advanced Circuits, has four layers and is 4" x 5". It has a voltage regulator section which receives its power source from two 9V batteries installed on the bottom surface of the PCB. There is a clock generation subcircuit and a series of BNC connectors to send the input signal and the clocks ϕ_C and ϕ_R to the PCB as well as outputs from all nine stages of the amplifier to a nearby oscilloscope. The 40-pin ZIF socket used for mounting the CMOS Amplifier IC is shown in Fig. 4.3. The steps involved in designing the PCB are outlined in Appendix A.

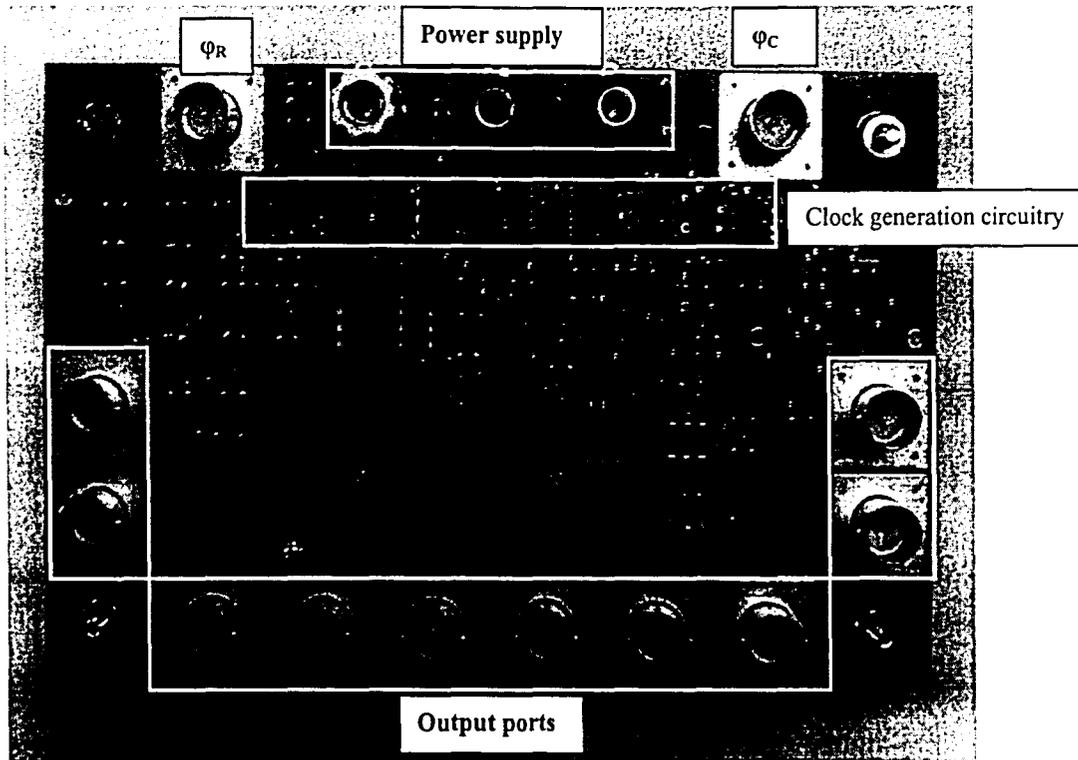


Figure 4.3: PCB employed in the test setup

4.2.1 Faraday Cage

Ambient 60Hz noise picked up by the circuitry drowned out a lot of the signal, making it impossible to detect the signal on the oscilloscope. This problem was addressed by placing the test setup in a 0.25" steel Faraday cage. Figure 4.4 shows how the output of the third stage does not reveal the small voltage ramps from the integrator output when a 60pA current is applied to the circuit because the interfering noise totally swamps out the signal. When the setup is placed in a Faraday Cage however, this interference is eliminated altogether.

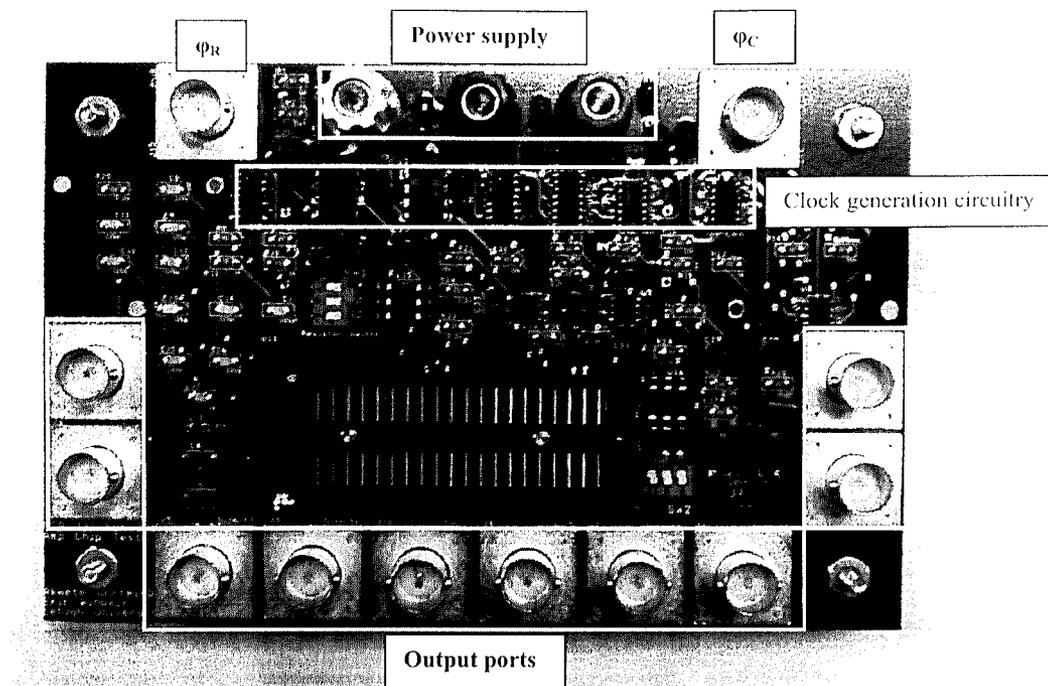
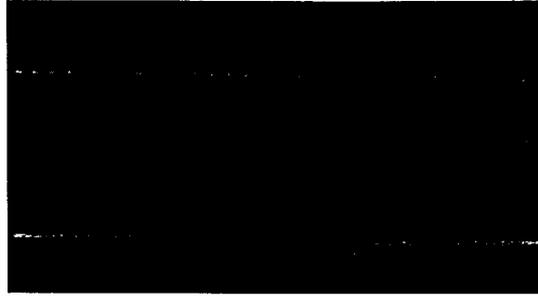


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(A)



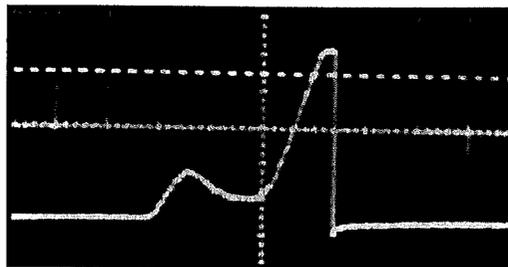
(B)

Figure 4.4: (A) Output without Faraday cage. (B) Output with Faraday cage.

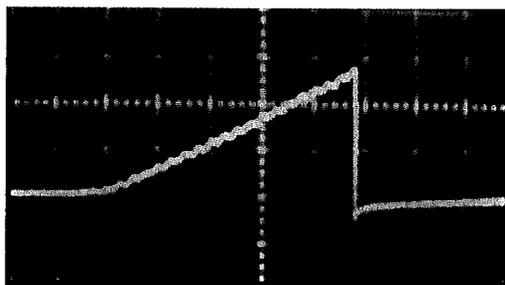
4.2.2 Power supply circuit

The supply rails have posed various challenges during our testing of the chips. The power supply is divided into two separate analog and digital power supply sections. The 9 stages of the amplifier circuit require analog +5V and ground nodes, and the clock circuitry is powered by the digital power supply rails.

The voltage regulator circuit is powered by two 9V batteries. This subcircuit is powered by batteries to eliminate 60Hz noise from AC power lines, a serious problem encountered in a previous version of the test setup. On the first PCB design, a +18V supply voltage was applied to the voltage regulator circuit configuration but failed to work correctly. Replacing this with two 9V batteries, with each separately powering the



(A)



(B)

Figure 4.4: (A) Output without Faraday cage. (B) Output with Faraday cage.

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+5V and the -5V rails, works well. The analog circuitry is less robust to noise and is powered by batteries while the digital clock circuitry is powered by an external HP 6205B dual DC power supply.

4.2.3 Clock Generator Circuitry

The entire circuit uses five different clocks as shown in Table 4.1. The clocks are made from T-switches to nullify any clock feedthroughs from interfering with the signal through the junction capacitance of the opamp. While these clocks were previously generated off chip by a HP 8115A Dual Channel Pulse Generator, the revised PCB includes a section that generates three of the five clocks, making the entire test unit more portable. The HP 8115A is now used to generate only the ϕ_C ϕ_R clocks

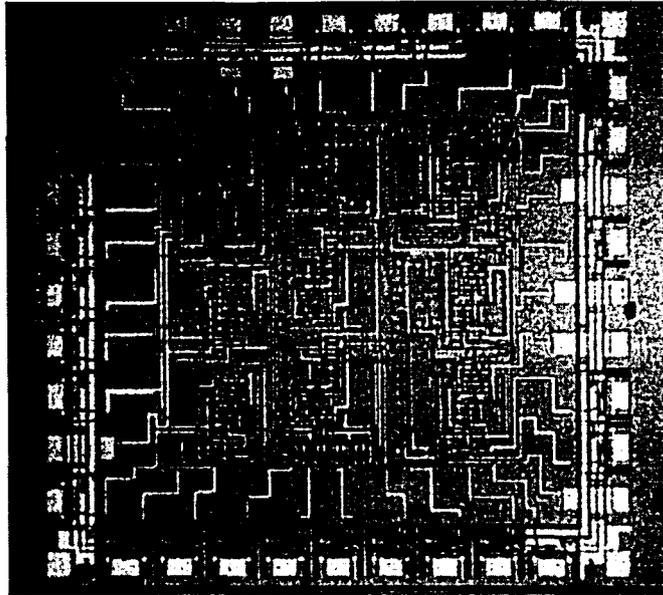
The clocks are generated using a set of logic gates. An astable oscillator, whose frequency can be varied by simply changing the value of a resistor, is used to increment a 4-bit synchronous counter from 0 to 15. Using a set of logic gates, the sampling clocks ϕ_{S1} , ϕ_{S2} and ϕ_{S3} are made to read high when the 4-bit counter reads 0000, 1000 and 0100, respectively. The output of this subcircuit is then fed to the amplifier chip to perform the desired sampling operation.

Symbol	Description
ϕ_R	Reset Clock, used in Stage 1 to reset the integrating capacitor to prevent the output of stage 1 from clipping. Discharging the capacitor makes repeated measurements possible.
ϕ_C	Clamp clock, used in stage 3 to perform correlated double sampling. On the first PCB, $\phi_C = \phi_R$ which did not allow the successful execution of CDS.
ϕ_{S1}, ϕ_{S2}	Sampling clocks used to perform digital differentiation. The two clocks are 3.3V at 16kHz and are phase shifted by 180°.
ϕ_{S3}	Sampling clock used to retrieve amplified signal. Allows sample and hold of signal peaks

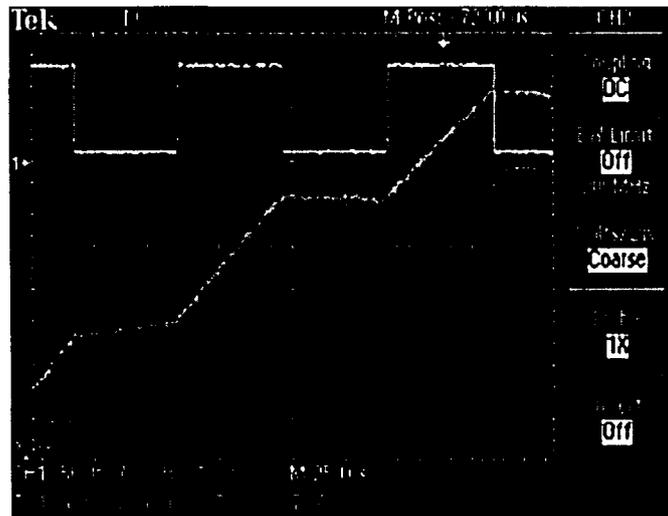
Table 4.1: Clocks and their functions

4.2.4 CMOS Amplifier Evaluation

This ion channel signal processor (Figure 4.5a) achieves low-noise front end, input offset cancellation, ultra-high gain, fast-transient signal processing, and CMOS compatibility¹⁰. The amplifier currently possesses the ability to sense current pulses as low as 50pA. This represents a great improvement on the 500nA current sensing capability of the previous version of the amplifier. This improved sensitivity makes it useful for application in whole cell current experiments, where the current levels are relatively higher. Reducing the sensitivity of the amplifier by one more order of magnitude will make it applicable to single-cell current recordings.

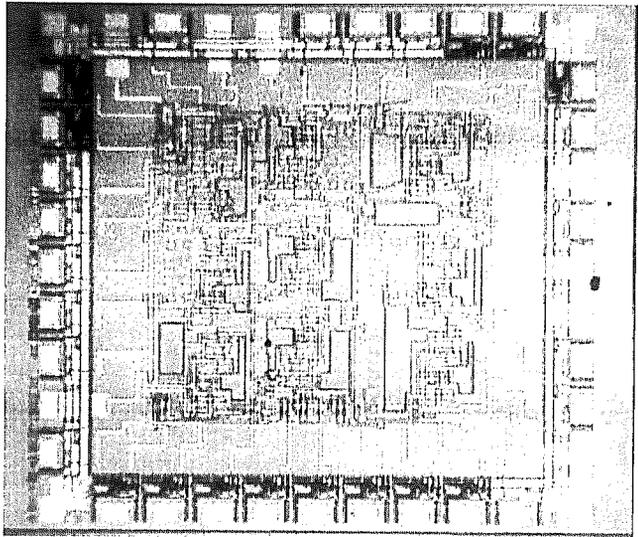


(A)

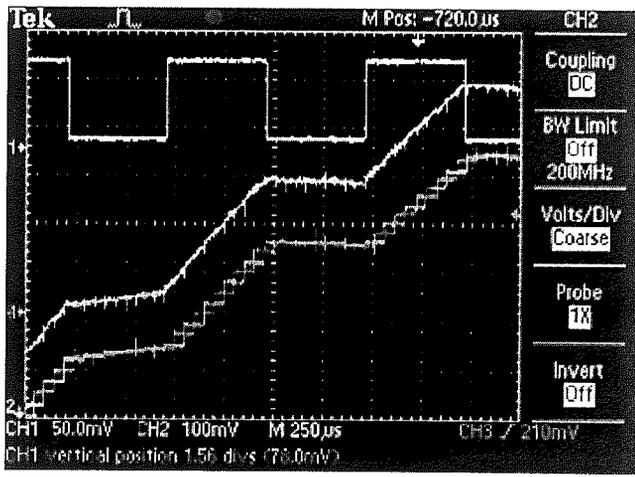


(B)

Figure 4.5: (A) 40pin CMOS amplifier fabricated with SCMOS n-well technology. (B) Snapshots at 3 nodes: input (top), 2nd stage (middle), sampling stage (bottom)

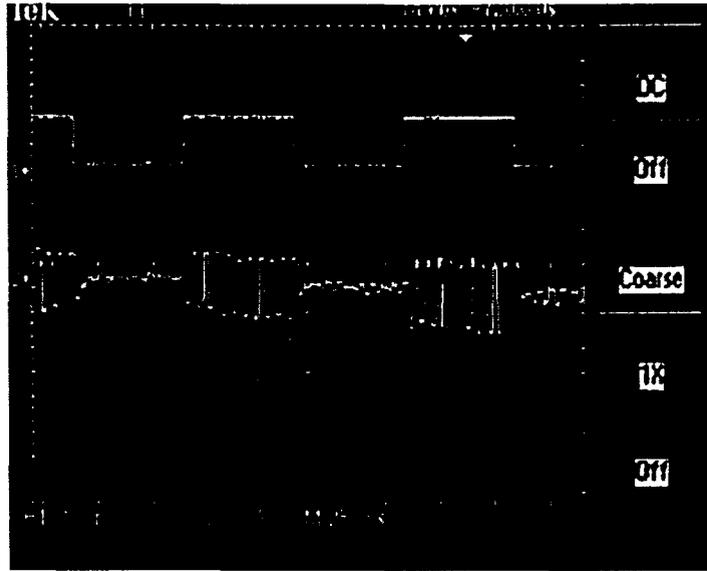


(A)



(B)

Figure 4.5: (A) 40pin CMOS amplifier fabricated with SCMOS n-well technology. (B) Snapshots at 3 nodes: input (top), 2nd stage (middle), sampling stage (bottom)

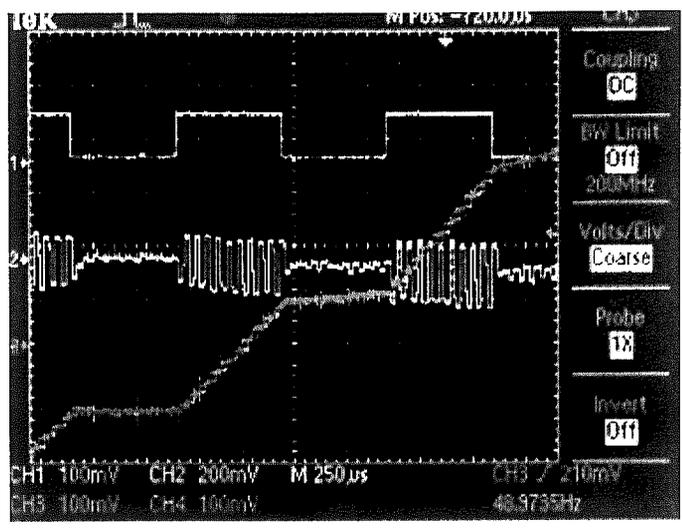


(A)

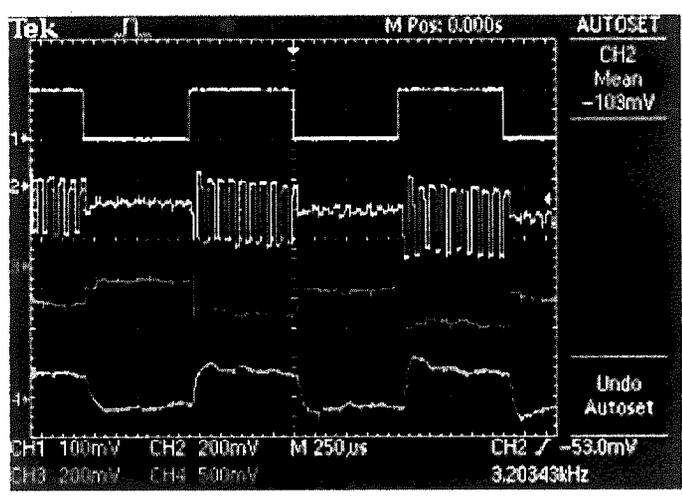


(B)

Figure 4.6: (A) Snapshots at 3 nodes: input (top), postdifferentiation (middle), sampling stage (bottom). (B) Snapshots at 4 nodes: input (top), postdifferentiation, (second), pre-filtering (third), and post-filtering (bottom).



(A)



(B)

Figure 4.6: (A) Snapshots at 3 nodes: input (top), postdifferentiation (middle), sampling stage (bottom). (B) Snapshots at 4 nodes: input (top), postdifferentiation, (second), pre-filtering (third), and post-filtering (bottom).

Conclusion

Patch clamping has become the accepted gold standard for studying ion channel function. The field of ion channel research is underway and will see rapid progress in the near future. Automated patch clamping appears to be the next logical phase of this progression due to industry drive towards process optimization and automation, as well as cheaper costs.

This thesis has provided a summary of our research work till date. With the aid of computer aided simulations, we are currently attempting to obtain a better understanding of the limitations of the amplifiers layout and electrical design. With this understanding, we will be able to revise the amplifier sensitivity to sense currents as low 5pA, making it applicable for single ion channel current recordings.

Work will soon begin towards the final phase of this project where we will attempt to put together an integrated SoC to perform ion channel characterization. With this device, we will be able to contribute significantly to the field of electrophysiology and drug testing.

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Publications

- S. Pandey, Akwete Bortei-Doku, M.H. White, “A Novel CMOS Integrated Amplifier for Sensing Single Ion Channel Current in Biological Cells” International Semiconductor Device Research Symposium, 318-319, Dec 2005
- S. Pandey, Akwete Bortei-Doku, M.H. White, “Modeling Voltage-gated KcsA Ion Channels as Solid-State Nanodevices”, International Semiconductor Device Research Symposium, 66-67, Dec 2005
- S. Pandey, R. Mehrotra, M. Chabalko, Akwete Bortei-Doku, M.H. White “A BioMEMS Platform for Planar Patch Clamping” International Semiconductor Device Research Symposium, 316-317, Dec 2005
- S. Pandey, Akwete Bortei-Doku, M.H. White, “Molecular Dynamics of Biological Ion Channels”, International Semiconductor Device Research Symposium, 310-311, Dec 2005
- S. Pandey, Akwete Bortei-Doku, M.H. White, “Simulation of Biological Ion Channels as Solid-State Nanodevices”, Computer Methods and Programs in Biomedicine, Volume 81 (1), 1-7, 2007

Appendix A

PCB Design in Orcad Layout

The text in this section describes the steps involved in the design of our printed circuit board. This PCB is a four layer board, with the top and bottom layers used as routing layers. The second layer from the top, also called a plane layer, is used as the ground plane. A small region on this ground plane is isolated into what is called a copper pour which is used as a separate ground pin for the digital circuitry. The third layer from the top is +5V power supply plane. A separate copper pour is designated to serve as the positive rail for the digital circuitry.

Designing the PCB involved

1. Drawing the circuit schematic
2. Creating footprints in Layout Library manager
3. Assigning footprints to schematic components
4. Exporting schematic circuit to layout
5. Positioning and routing footprints
6. Performing error checks
7. Exporting layout file to manufacturer

Creating the circuit schematic was fairly straight-forward. Challenges arose when components to be used on the final PCB did not already exist in Capture Schematic. The most important thing in this step was to ensure that both newly created parts and already existing parts had their pin numbers match exactly with the components to be bought for the PCB (Figure A1).

The second step, which is the create footprints in the Layout library was a little more tedious since most of the parts did not already exist in the library Manager. The most dependable way of completing this task was to create all parts by referring directly

to the dimensions specified in the datasheet for each component. Converting between millimeters and inches also posed a challenge because slight errors in conversions between the two systems could translate into components not fitting on the final PCB.

Each component or part had all its pins defined. The Layout program uses the pin 1 on every component as the reference point so it was advisable to make the first pin square and the others round to distinguish the pin 1 of every footprint. Each component was given an outline in the silk screen layer to serve as a deterrent against component overlaps. It was important to specify the diameter of each pin in the top, ground plane, power plane, bottom plane, silk screen, and drill bit planes.

When all the parts were created in Layout, the next step involved going back to Schematic and assigning corresponding part names in Layout to every component in the schematic diagram. This allowed the parts to be exported seamlessly into Layout.

Due to the susceptibility of analog circuit components to noise, the components which process analog signal were routed first and the more durable digital circuit components were later automatically routed. Using the Autoroute feature did not always yield the shortest lead lengths and was therefore permissible for use when routing the digital circuitry. All pins going to ground can be connected vertically downward into the ground plane, minimizing noise due to lead lengths to a bare minimum. Our 4" x 5" printed circuit board was manufactured by Advanced Circuits. A more detailed tutorial describing the design of printed circuit boards in general can be found at

<http://cnx.org/content/m11677/latest/>

<http://cnx.org/content/m11676/latest/>

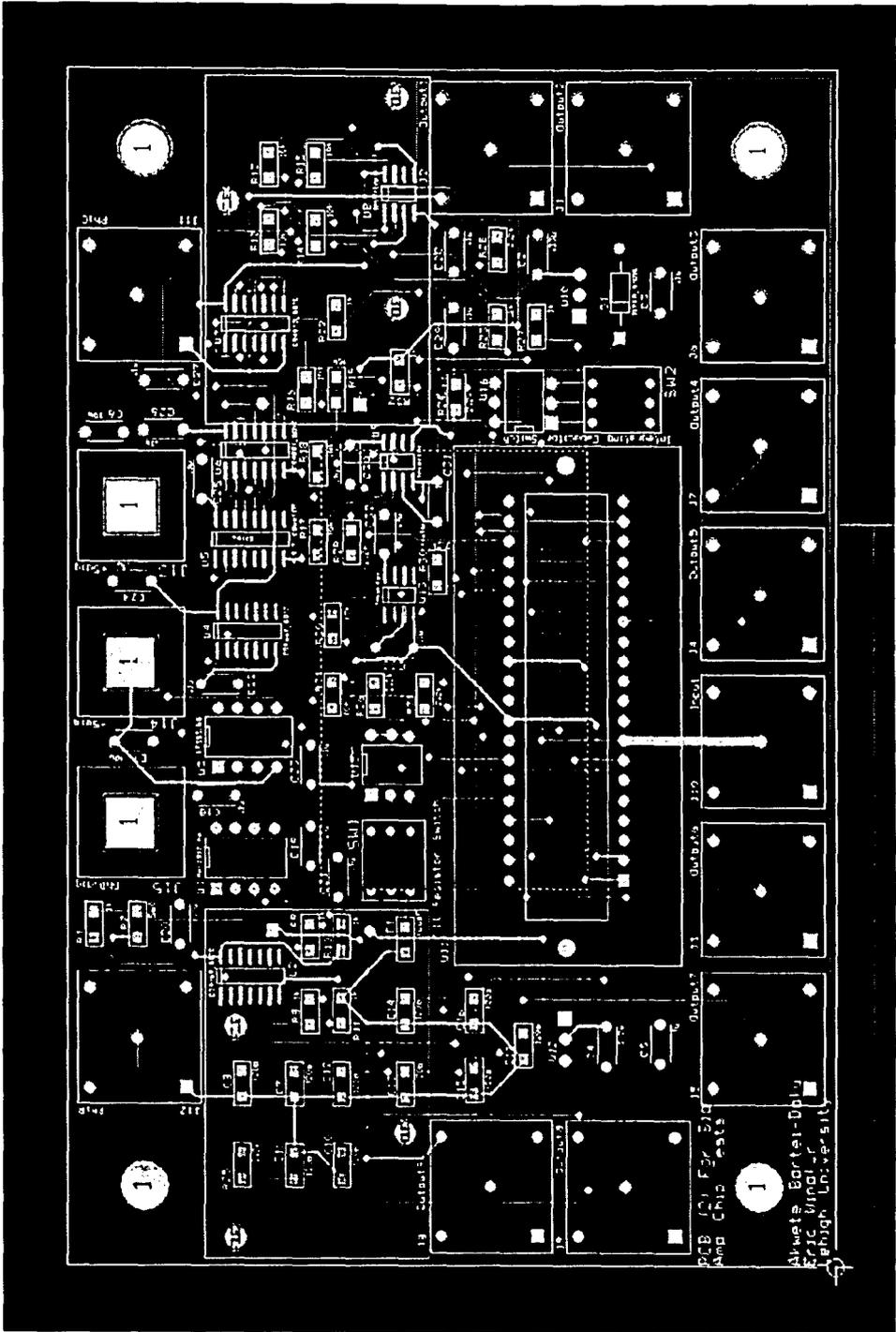


Figure A1: Screenshot of PCB layout diagram.

A Novel CMOS Integrated Amplifier for Sensing Single Ion-Channel Current in Biological Cells

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The membrane of biological cells is embedded with protein macromolecules called ion-channels that regulate the ion flux by unique gating mechanisms. Charged amino acids are present in a voltage-sensitive region of the ion-channel, the movement of which leads to a channel's conformational changes i.e. open and closed states (Fig. 1). Today, electrophysiology tools enable us to record the behavior of these ion-channels: gating, conductivity, specificity, and selectivity [2].

A single ion-channel current can be said to be a random telegraph signal with current fluctuations of ~ 1.5 - 2.5 kHz and open-state current amplitudes of ~ 5 - 8 pA [2]. Sensing and amplifying such low-level currents in a low-noise environment is a challenging task. An amplifier for this purpose should be a sensitive current-to-voltage (I-V) converter, converting ion-channel currents into voltage signals for observation with an oscilloscope or sampled and stored in a computer. Commercial transimpedance amplifiers follow approaches that require the use of large, discrete electrical components, which limits signal-handling bandwidth, incorporates noise and adds to the costs of ion-channel signal processing [3]. To circumvent these problems, there is a drive towards miniaturization, high-throughput and lab-on-chip (LoC) systems and a concomitant need to design an advanced integrated signal processor for single ion-channel recording.

Here, we present a novel integrated CMOS transimpedance amplifier that permits the recording of low-level, single-channel, fast transient ion-channel currents over a wide dynamic range (1–5 kHz). The amplifier consists of an initial integrator stage, a post integrating differential stage with gain $G_{POST-INT}$, a clamp stage, a discrete-time differentiator stage, a pre-filter differential amplifier stage with gain $G_{PRE-FILTER}$, and a low pass filtering stage with gain G_{FILTER} , as shown in Fig. 2. The amplifier operates in three modes: the reset mode, the clamp mode and the normal signal-handling mode. During the reset mode, the reset switch ϕ_{reset} is closed to discharge the integrating capacitor C_{INT} . Subsequently, the clamp mode starts wherein the clamp switch ϕ_{Clamp} stores the offset level. After this reset-and-clamp operation, the normal signal-handling mode begins where the input signal I_{INPUT} is sensed. The integrator integrates the incoming pulses, two clocks ϕ_{S1} and ϕ_{S2} sample the integrated signal, discrete-time differentiation is performed, followed by post amplification and filtering. Offset cancellation and noise suppression is performed with Correlated Double Sampling (CDS) [4]. Clock feed-through in switches is minimized using CMOS transmission-gate switches with small overlap capacitance.

The chip is fabricated by MOSIS using an AMIS $1.5\mu\text{m}$ n-well CMOS process technology with 1 metal layers and 2 poly layers. The chip ($2.2\text{mm} \times 2.2\text{mm}$) is packaged in a 40-pin DIP. Testing is performed with a 5nA current generated by applying 100mV pulses across a $20\text{M}\Omega$ resistor. The results at various nodes of the amplifier circuit are shown in Figs. 3 - 6. A simple calculation shows the output voltage is 300mV , in accordance to the waveform in Fig. 5.

$$V_o = \left(\frac{I_{INFLT}}{C_{INT}} \right) \left(\frac{G_{POST-INT}}{f_{SAMPLING-CLK}} \right) (G_{PRE-FILTER} \times G_{FILTER}) = \left(\frac{100 \text{ mV}}{20 \text{ M}\Omega} \right) \left(\frac{1}{500 \text{ pF}} \right) \left(\frac{10}{10^4} \right) (10)(3) = 300 \text{ mV}$$

This ion-channel signal processor achieves low-noise front end, input offset cancellation, ultra-high gain, fast-transient signal processing, and CMOS compatibility. We have been able to process currents as low as $\sim 200\text{pA}$ operating at 1–5 kHz using our present breadboard setup. However, to test current levels in actual ion-channel recording, we are in the process of developing a PCB to reduce external noise sources. Our goal is to build a lab-on-chip (LoC) for electrophysiology where we will integrate this amplifier design into a BioMEMS platform [5].

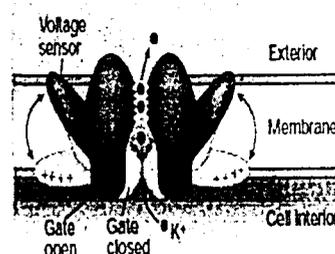


Fig. 1: Opening and closing of a membrane protein ion-channel [1].

Acknowledgements: This work is supported by the National Science Foundation on grant ECS-0524049 and the Sherman Fairchild Foundation of Lehigh University. We thank MOSIS for the chip fabrication.

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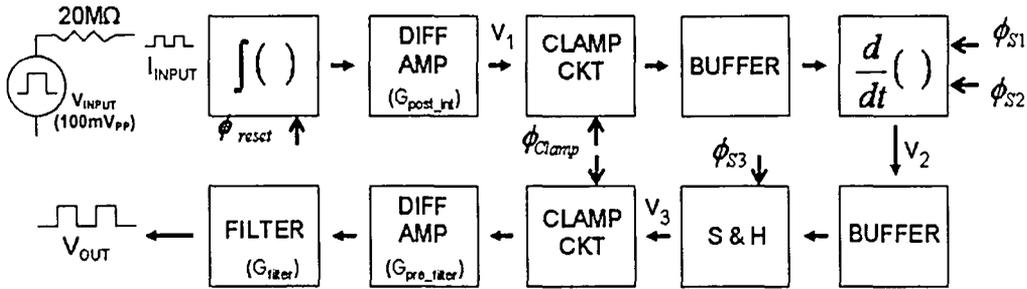


Fig. 2: Block diagram of our CMOS transimpedance amplifier. The input is the simulated current pulses (5nA, 1 kHz) obtained by passing 100mV_{pp} voltage pulses through a 20MΩ resistor. The output is 300mV.

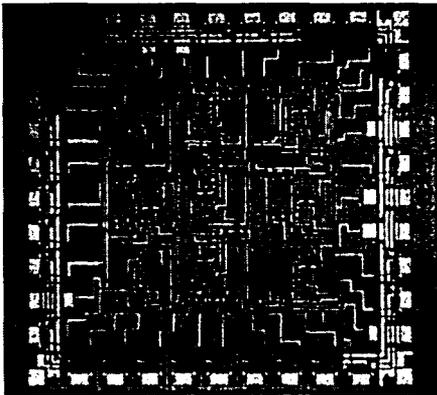


Fig. 3: 40-pin CMOS amplifier fabricated with SCMOS n-well technology. (900μm x 900μm).

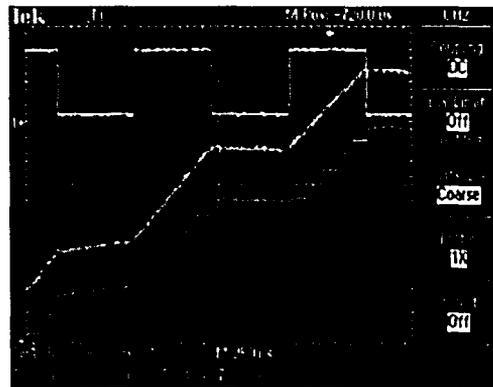


Fig. 4: Snapshots at 3 nodes: input V_{INPUT} (top), 2nd stage V_1 (middle), sampling stage (bottom).



Fig. 5: Snapshots at 3 nodes: V_{INTUT} (top), post-differentiation V_2 (middle), sampling stage (bottom).



Fig. 6: Snapshots at 4 nodes: V_{INTUT} (top), post-differentiation V_2 (second), pre-filtering (third), and post-filtering (bottom).

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References

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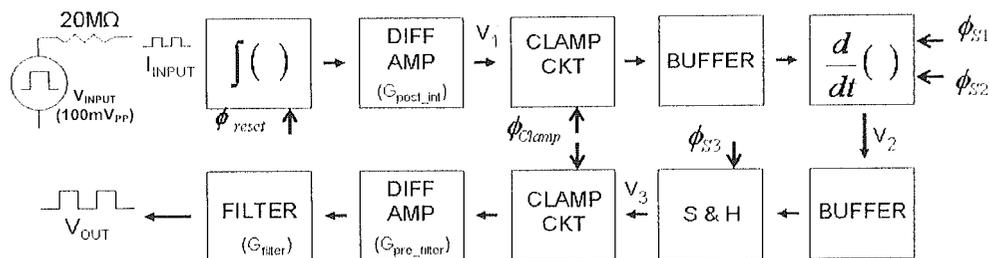


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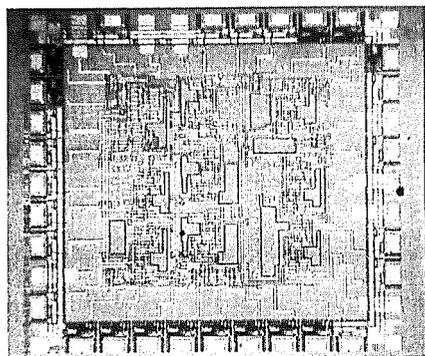


Fig. 3: 40-pin CMOS amplifier fabricated with SCMOS n-well technology. (900μm x 900μm).

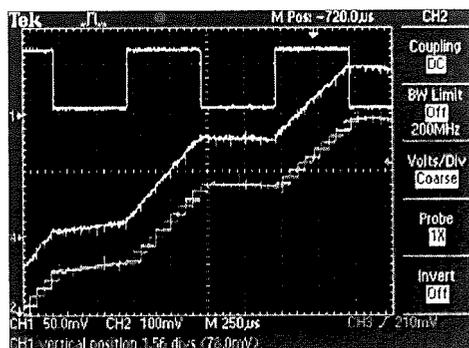


Fig. 4: Snapshots at 3 nodes: input V_{INPUT} (top), 2nd stage V_1 (middle), sampling stage (bottom).

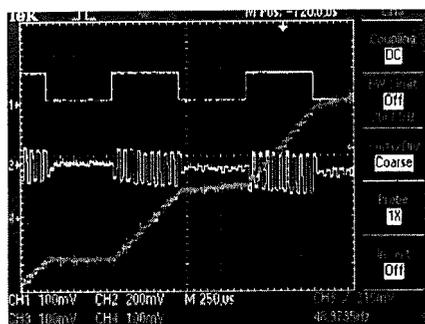


Fig. 5: Snapshots at 3 nodes: V_{INPUT} (top), post-differentiation V_2 (middle), sampling stage (bottom).

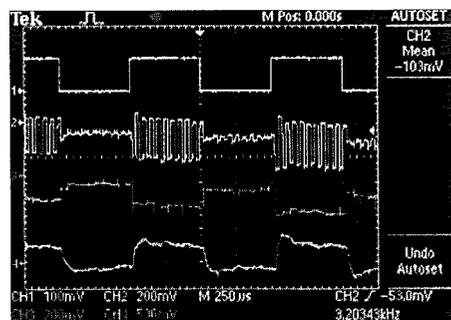


Fig. 6: Snapshots at 4 nodes: V_{INPUT} (top), post-differentiation V_2 (second), pre-filtering (third), and post-filtering (bottom).

Modeling Voltage-gated KcsA Ion Channels as Solid-State Nanodevices

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In this paper, we present a novel method of simulating KcsA ion channels using a TCAD solid-state device simulator [1]. The ion transport in these channels has interesting similarities with the flow of carriers in electronic nanodevices. With this perspective, we have modeled ion channels as solid-state nanodevices and obtained self-consistent solutions of the axial potential and ion fluxes. Models of cylindrical and KcsA channels are built with the TCAD simulation tools and their steady-state characteristics are studied. The simulation results are compared with the reported experimental results in the literature to verify the efficacy of our method. The ability to simulate realistic ion channel models with such computational ease and reasonable accuracy provides a powerful tool for studying the biological functions of these channels with deeper insight.

Ion channels are the ultimate in natural nanotubes that regulate the ion flux across a cell membrane, and thereby play an integral role in cellular signaling mechanisms (Figure 1) [2]. Among the approaches for ion channel modeling, molecular dynamics are the most accurate but presently limited by long simulation times [3]. Continuum electrostatics provides an alternative approach, which involves solving the Poisson-Nernst-Planck (PNP) equations for the charge distribution in the channel. This technique has proven suitable in predicting the behavior of KcsA and Ca^{2+} voltage-gated channels [4].



Fig.1: The seven helices of a KcsA channel span the cell membrane.

We have simulated a cylindrical channel and a KcsA channel made of two materials: silicon to mimic the conducting water continuum and SiO_2 to mimic the non-conducting protein walls. The carrier concentration, degree of ionization, and diffusion coefficients are adjusted in each conducting region to emulate the realistic motion of K^+ ions in the channel's vestibule. Two electrodes are placed at either ends of the reservoirs. The simulations are performed by solving the discretized PNP equations with a computation time ~ 5 sec. Figure 2 shows our TCAD cylindrical channel model (35Å long and 6Å wide). Figure 3 shows a decreased carrier concentration in the channel's vestibule, as also predicted by Brownian dynamics simulations [3]. We also considered the effect of protein surface charges in manipulating the energy profile of an ion traversing a channel. These surface charges are known to influence the gating, conductance, and toxin-binding effects of ion channels. As shown in Figure 4, an energy barrier inside the channel is transformed into a potential well by the inclusion of surface charges, thus increasing the chances of ion permeation through the channel [3].

Based on the KcsA ion channel structure revealed by x-ray crystallography [2], we have built a TCAD KcsA channel model as shown in Figure 5. The KcsA channel is 40Å long, with a narrow selectivity filter (12Å long and 3Å wide). Figure 6 shows the axial potential variation under different electrode voltages. Most of the transmembrane potential drop incurs in the selectivity filter, crucial for the selectivity and permeation of various ions. In Figure 7, we compare the current-voltage (IV) results from our simulations with those from experiments [5]. With accuracy within 3% over 200mV, this degree of agreement with the experimental data is better than those reported elsewhere [6].

Acknowledgements: This work is supported by the National Science Foundation on grant ECS-0524049 and the Sherman Fairchild Foundation of Lehigh University.

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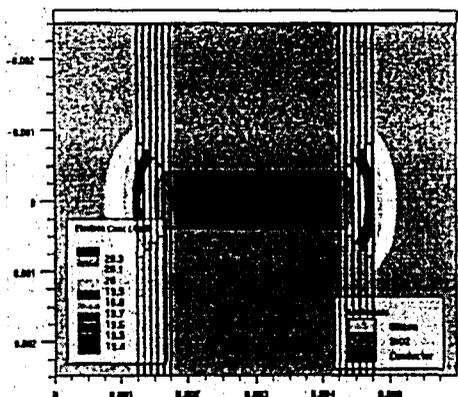


Fig.2: TCAD Cylindrical channel (35Å long, 6Å wide) showing the concentration contours.

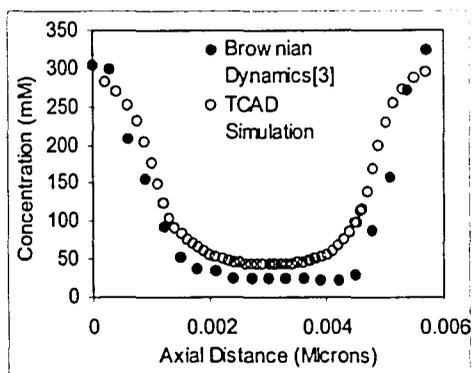


Fig.3: Comparison of the K⁺ concentration in the cylindrical channel: TCAD and BD simulations [3].

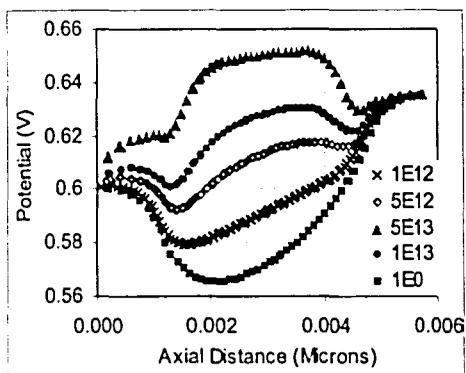


Fig.4: Protein charges counterbalance the energy barrier for carrier transport in ion channels.

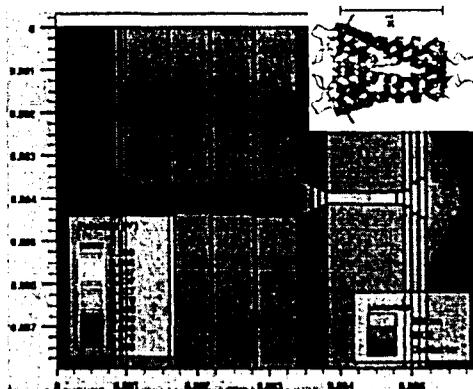


Fig.5: TCAD KcsA channel (40Å long, 3Å wide in selectivity filter). Inset shows real structure [2].

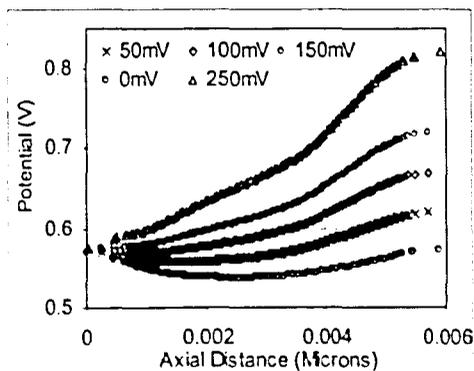


Fig.6: Axial potential variation in the TCAD KcsA channel at varying electrode voltages.

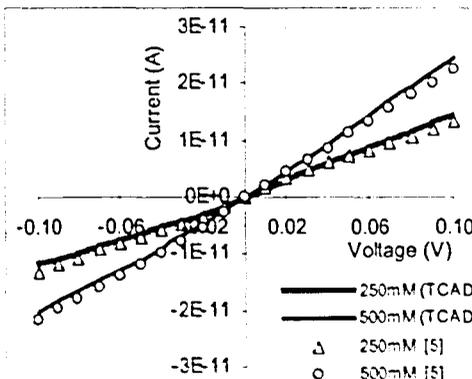


Fig.7: Comparison of the IV curves in a KcsA channel: TCAD simulation and experiments [5].

Molecular Dynamics of Biological Ion Channels

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Introduction: Ion channels are pores through a cell membrane that allow the exchange of specific ions across them. Understanding the atomistic-level ionic flow through these biological channels is crucial for pharmacology and drug discovery [1, 2]. In addition, the marriage of biological cells and nanoelectronics offers the possibility of new devices with the potential to go beyond the limitations of CMOS technology. The study of ion channels is needed to model the interface between nanoelectronics and biological cells.

Ions entering a channel can either return or escape into the channel, traversing it and escaping from the other side. Key quantities that describe the process are the translocation and return probabilities, average lifetime and the power spectral density (an experimentally accessible parameter) of ion number fluctuations [3]. Till recently, theoretical analysis of ion transport has been limited to low-resolution continuum diffusion-based or kinetic-based models [3-5]. Such analytical models fail to include the factors affecting the ionic conduction through ion channels. In this paper, an electro-diffusion model is presented which extends previous models to incorporate the effects of electric field, energy barrier, and rate-limited association/dissociation of ions with protein charges inside the channel. We derive the probability density function (p.d.f.), the correlation function, and the spectral density of ion number fluctuation.

Analytical Model: Consider an ion channel of length L with two bulk reservoirs, the source and the sink. Assume the ions are very few in number inside the channel and mutually non-interacting. The ions can, however, interact with a single surface site in the vestibule through association/dissociation. Let us denote $p(r, t)$, the p.d.f. of a free ion at a distance r and at time t , and $q(r, t)$ as the p.d.f. of finding an ion associated with surface charges. These functions obey the following equations

$$\begin{aligned} \frac{\partial p(r, t)}{\partial t} &= \mathcal{L} p(r, t) - \frac{k_a \delta(r-a)}{\gamma_d r^{d-1}} p(r, t) + \frac{k_d \delta(r-a)}{\gamma_d r^{d-1}} q(r, t) \\ \frac{\partial q(r, t)}{\partial t} &= \gamma_d a^{d-1} \left[\frac{k_a \delta(r-a)}{\gamma_d r^{d-1}} p(r, t) - \frac{k_d \delta(r-a)}{\gamma_d r^{d-1}} q(r, t) \right] \quad \mathcal{L} = D_p r^{1-d} \frac{\partial}{\partial r} r^{d-1} e^{-U(r)} \frac{\partial}{\partial r} e^{U(r)} \end{aligned} \quad (1)$$

where d is the spatial dimension, a is the contact site, k_a is the association rate, k_d is the dissociation rate, $U(r)$ is the potential energy, D_p is the diffusion constant, and $\gamma_d = 1, 2\pi$, and 4π for $d=1, 2$, and 3 respectively. After some steps, the 1-D generalized solution of the p.d.f. in the Laplace-domain is

$$\bar{p}(x, s | x_o) = G(a, s | x_o) \left[1 + s k_a G(a, s | a) / (s + k_d) \right]^{-1} (-s k_a / (s + k_d)) G(x, s | a) + G(x, s | x_o) \quad (2)$$

where $G(x, s | x_o)$ is the Laplace-domain Green function, and $\bar{p}(x, s | x_o)$ denotes the Laplace transform of $p(x, t)$ with an initial condition given at distance x_o . Now, starting with the standard current density-continuity equations, the Green function in the time-domain is obtained as

$$g(x', t) = p_o e^{-t/\tau_p} \left[1 - \frac{x'}{L} - \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{e^{-\beta^2 D_p t}}{n} \sin(\beta x') \right] + \frac{2Q_o e^{-t/\tau_p}}{\pi L} \sum_{n=1}^{\infty} \frac{e^{-\beta^2 D_p t}}{n} \sin(\beta x') \sin(\beta x_o) \quad (3)$$

where $\beta = n\pi/L$, $x' = x - \mu_p \mathcal{E} t$, \mathcal{E} is the electric field, μ_p is the mobility, x_o is the site of initial impulse, Q_o is the impulse amplitude, p_o is the concentration of the source with a perfect sink, and $\tau_p = 1/k_d$ is the recombination time. We plot the time variation of the Green function from equation (3), showing the diffusion-induced (Fig. 1) and the drift-diffusion-induced (Fig. 2) ion flow. Taking the Laplace-transform of equation (3) and plugging it in equation (2) gives the exact p.d.f. of ion number fluctuation. The correlation function (survival probability) $C(t | x_c)$ and spectral density $S(f)$ are related to p.d.f. as

$C(t | x_0) = \int_{x_0}^{x_0} p_1(x, t | x_0) + \int_{x_0}^L p_2(x, t | x_0)$
 $S(f) = 4 \cdot \text{Re} \{ C(s = 2\pi fi | x_0) \}$ (4)

With perfect source/sink and an initial unit impulse at the channel's center, the spectral density $S(f)$ is:

$$S_1(f) = 4 \cdot \text{Re} \left\{ \frac{2(2\pi fi + k_d) \left[\cosh \left(\frac{1}{2} \sqrt{\frac{2\pi fi}{D_p}} L \right) - 1 \right]}{2\pi fi \left[2(2\pi fi + k_d) \cosh \left(\frac{1}{2} \sqrt{\frac{2\pi fi}{D_p}} L \right) + k_d \sqrt{\frac{2\pi fi}{D_p}} \sinh \left(\frac{1}{2} \sqrt{\frac{2\pi fi}{D_p}} L \right) \right]} \right\} \quad (5)$$

It follows from equation (4) that $S(0)$ is four times the mean lifetime of the ion. In Fig. 3 and 4, we plot the spectral densities for different k_a and k_d values. The transition from diffusion-dominated behavior (lower spectra) to a binding-dominated one (upper spectra) is clearly seen. Equation (5) is able to describe the theoretical dependence of the spectra in the full range of the parameters studied. The model can describe other processes (besides ion transport) as charge migration along polymers or DNA chains [3].

Acknowledgements: This work is supported by the National Science Foundation on grant ECS-0524049 and the Sherman Fairchild Foundation of Lehigh University.

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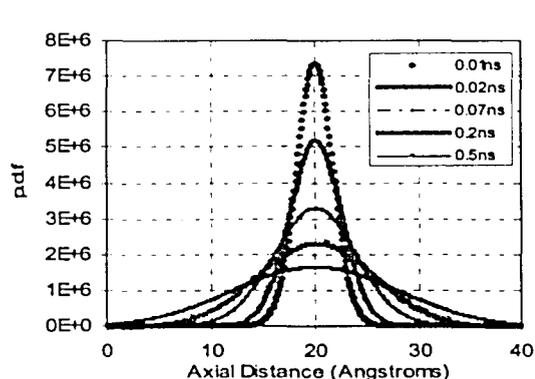


Fig.1: Shows the diffusion-induced time variation of the Green function in a channel

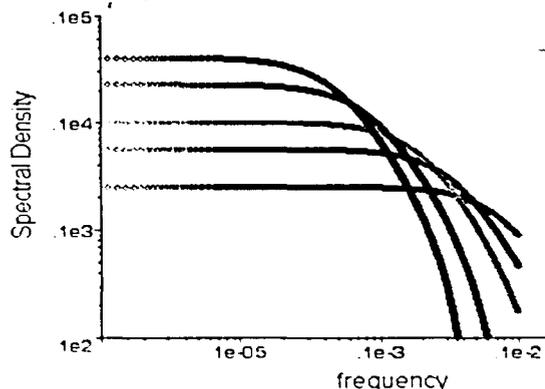


Fig.3: Spectral density of particle number fluctuations with fixed $k_a = 10^{-3}$ and values of k_d (bottom to top): ∞ , $9.91e-3$, $9.97e-3$, $1.01e-3$.

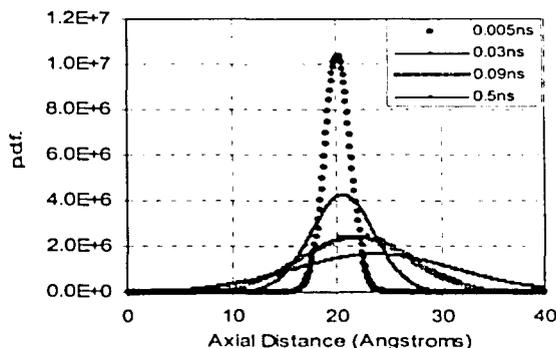


Fig.2: Shows the drift-diffusion induced time variation of the Green function in the same channel as Figure 1.

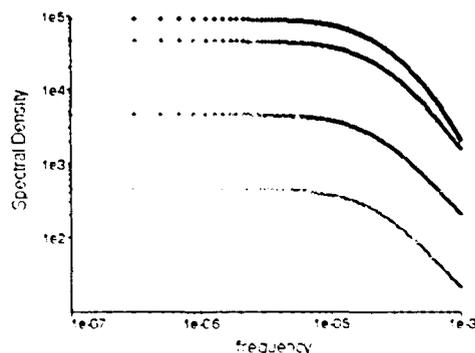


Fig.4: Spectral density of particle number fluctuations with fixed $k_d = 10^{-5}$ and values of k_a (bottom to top): ∞ , $9.93e-5$, $9.96e-5$, $1.01e-3$.

A BioMEMS Platform for Planar Patch-Clamping

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Introduction: The study of cellular functions, so crucial for physiology and pharmacology, is directly related to the opening and closing of micro valves in the cell membrane called ‘ion-channels’ [1, 2]. The patch-clamp technique is considered the ‘gold’ standard for studying the ion-channel behavior. However, because of its very low-throughput and higher costs per data point, there is a dire need for automated high-throughput-screening (HTS) techniques [3]. One of the promising contenders is planar patch-clamping, where the entire electrophysiology lab can be built on a single chip [4, 5]. The planar patch-clamp method requires automatic positioning of a cell on a recording micropore, forming a gigaohm-range seal, accessing the whole cell, and measuring the ionic current in response to voltage stimulation.

Recently, several major categories of planar patch-clamp technologies are being developed [6-8]. With advancements in MEMS and nanofabrication, there is no dearth of available substrates, system topologies, and chemical tools [4]. Here, we present a silicon-based BioMEMS platform for isolating a single cell, bringing it to the micropore, and initial results towards gigaseal formation. Previous approaches of successful planar patch-clamping relied on suction and a hit-and-miss process for this purpose [4]. Experimental results indicate an aperture is inappropriate both for cell positioning by suction and for reliable gigaohm seal formation [8]. As such, we show that on-chip electric fields for cell positioning and suction for tests on seal formation.

Chip Fabrication and Assembly: On a p-doped <100> DSP silicon wafer, 2000Å SiO₂ and 1000Å Si₃N₄ are deposited. Anisotropic KOH etching gives ultra-deep silicon wells with suspended Si₃N₄ membrane. Then, Ti/Pt quadruple electrode structures are patterned. Plasma etching and Focused Ion Beam System are used to drill micropores in the Si₃N₄ membrane. After the entire fabrication sequence, as shown in Fig. 1, the chip consists of a micropore (1-2µm) in a Si₃N₄ membrane (1000Å thick) resting on an ultra-deep well (375µm deep). Both sides of the chips were bonded to 250µm-thick PDMS gaskets. Teflon structures serve as fluid chambers (10-20µl).

Measurements and Results: CHO cell lines are grown in DMEM/F12 medium with 2.2% fetal calf serum. The chip is assembled as shown in Fig. 2, and two Ag/AgCl sensing electrodes are connected to a LabVIEW™ controlled HP4145A Parameter Analyzer. A 20µL cell-free solution (80mM KCl, 2mM HEPES, pH=7.4) and 10µL of CHO cell suspension are pipetted in the bottom and top fluid chamber, respectively. The distance between the two Ag/AgCl electrodes is adjusted to ~50-200µm. A series of a.c. voltages (1V_{pp}, 2MHz) are applied to the Ti/Pt quadruple electrodes, creating lateral nonuniform electric fields [9]. Since the surface of the most native vesicles and cells bear electrical charge, these fields form a ‘cage’ that isolate a single cell and automatically position it on the micropore within ~5 seconds. Thereafter, a step voltage (100mV_{pp}) is applied between the sensing electrodes, negative pressure is applied from underneath the micropore, and the current is monitored. We have monitored currents ~5nA, indicating a seal resistance of ~20MΩ. The targeted seal resistance is ~1GΩ for planar patch-clamping.

The method of creating lateral and longitudinal electric fields for planar patch-clamping is unique to our work. As shown in Fig. 3, by creating longitudinal electric fields around the micropore’s vicinity, CHO cells are attracted towards the aperture and pulled through the aperture, leading to Coulter - like events (cell counting). Fig. 4 illustrates the manner in which lateral electric fields attract a single cell to the micropore and the precise 2D positioning of the cell. Seal resistance is determined to a large degree by the surface characteristics of the Si₃N₄ film and various surface coatings are under consideration to develop a so-called ‘gigaseal’. In addition to surface preparation, localized forces (electric field, gravity, Brownian motion, suction), are employed for planar patch-clamping. This paper will present the basic interaction between biological cells, MEMS microstructures and integrated electronics as a first step towards the development of an integrated 2D patch-clamp laboratory on a chip (LoC).

Acknowledgements: This work is supported by the National Science Foundation on grant ECS-0524049 and the Sherman Fairchild Foundation of Lehigh University.

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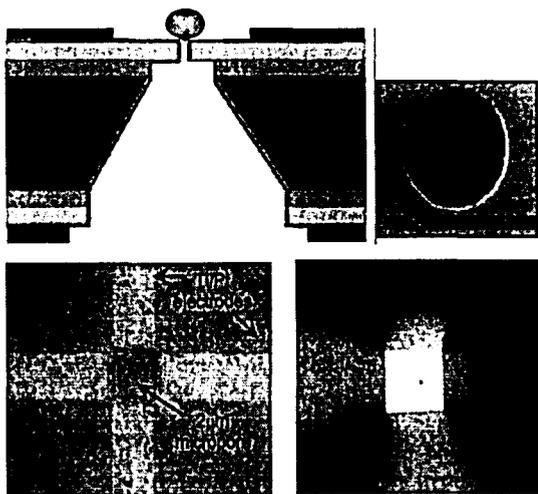


Fig. 1: Fabricated BioMEMS chip. (Top left) Cross-Section, (top right) SEM image of a 1 μ m pore, (bottom left) frontside, and (bottom right) backside.

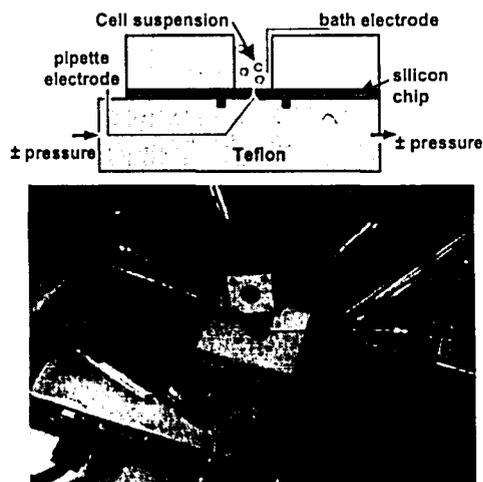


Fig. 2: (Top) Cross Section of the assembly and microfluidics. (Bottom) Picture of the hybrid assembly on a measurement stand.

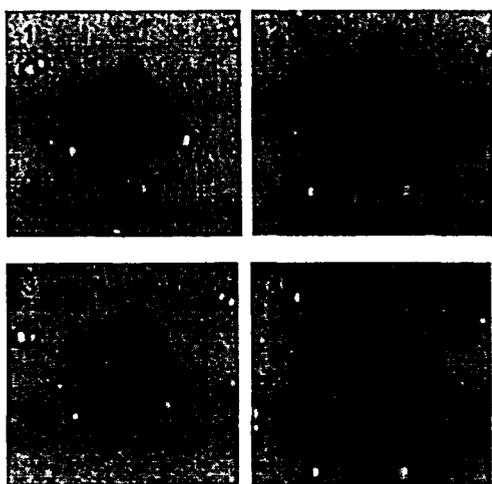


Fig. 3: Four snapshots are taken at time intervals of 1 second. Vertical electrical fields draw cells from the cis-to-trans side of a 10 μ m micropore.

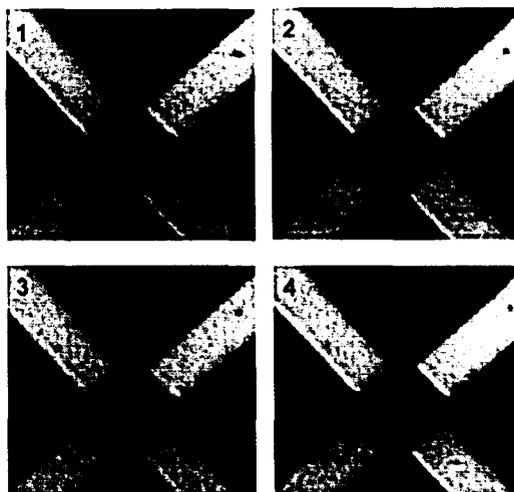


Fig. 4: Four snapshots are taken at time intervals of 1 second. Lateral electrical fields form a trap, bringing a single CHO cell over a 2 μ m micropore.



Simulation of biological ion channels with technology computer-aided design

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ARTICLE INFO

Article history:

Received 5 November 2004

Received in revised form

20 May 2005

Accepted 28 August 2006

Keywords:

Ion channel

KcsA

Poisson–Nernst–Planck

SILVACO

ABSTRACT

Computer simulations of realistic ion channel structures have always been challenging and a subject of rigorous study. Simulations based on continuum electrostatics have proven to be computationally cheap and reasonably accurate in predicting a channel's behavior. In this paper we discuss the use of a device simulator, SILVACO, to build a solid-state model for KcsA channel and study its steady-state response. SILVACO is a well-established program, typically used by electrical engineers to simulate the process flow and electrical characteristics of solid-state devices. By employing this simulation program, we have presented an alternative computing platform for performing ion channel simulations, besides the known methods of writing codes in programming languages. With the ease of varying the different parameters in the channel's vestibule and the ability of incorporating surface charges, we have shown the wide-ranging possibilities of using a device simulator for ion channel simulations. Our simulated results closely agree with the experimental data, validating our model.

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1. Introduction

Biological ion channels are transmembrane proteins that regulate the ion flux through a cell, and thereby play an integral role in cellular signaling mechanisms [1]. Modeling of ion channels has a long history, but the lack of detailed structural knowledge hampered the progress in this field. With advancements in molecular biology and X-ray diffraction techniques, a lot is now known regarding the structural details of ion channels [2].

Ions in solution execute random Brownian motion, and if an electric field is applied, they acquire drift velocity. It is the interaction between the ions and the electric field in the channel that decides the salient features of an ion channel. The effective electric field is a complicated interplay from various sources including the membrane potential, the charge

residues on the wall, the surrounding ions, and the charges induced in the membrane wall by these ions [3].

Among the varied approaches available for ion channel modeling, the most accurate representation of the system is provided by molecular dynamics (MD) simulations, where all the atoms in a system are treated explicitly [4,5]. However, MD simulations are presently limited to simulation times of not more than a few nanoseconds, due to the small timesteps (~femtoseconds) required to resolve individual ion trajectories. Any reliable estimates of steady-state channel currents require simulation time durations of the order of milliseconds, thus preventing an experimental validation of MD simulations [6].

An alternative method is to follow the motion of individual ions using Brownian dynamics simulations [7,8]. Here, it is assumed that the protein structure is fixed and water

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doi:10.1016/j.cmpb.2006.08.007

molecules are treated as a continuum. Collisions between the ions and the surrounding water molecules are mimicked by random fluctuating forces plus an average frictional force. A major advantage of Brownian dynamic approach is the ability to allow direct simulation of ion-ion interaction and calculate an ion's interaction energy with respect to the system during each time step [7]. But this has always been an involved, time-consuming process [9].

Using a mean field approximation, continuum electrostatics provides a rather simplistic alternative to ion channel modeling [10]. It involves solving the Poisson–Nernst–Planck (PNP) equations for the charge distribution inside the channel, and has proven to be very computationally cheap. Even though the PNP method uses a major approximation of reducing the ion–ion interactions to an interaction between an ion and a mean field, its results have shown to be in good agreement with the experimental data [11,12].

In this paper we present a novel method of simulating ion channels based on continuum electrostatics. We have attempted to represent the structure of a KcsA channel as a solid-state device, with its intrinsic material properties similar to that in the realistic case [13,14]. Simulations are performed on a solid-state device simulator, SILVACO International, providing us with the steady-state behavior of the KcsA channel. The simulation results agree well with the available experimental data.

2. Methods

2.1. Poisson–Nernst–Planck (PNP) theory

The PNP approach to ion permeation in membrane channels has been studied in numerous works [10,11,15]. The PNP equations are similar to the drift–diffusion equations that describe the carrier dynamics in semiconductors [16]. The flux J of each ion species is described by the Nernst–Planck (NP) equation, which combines the diffusion due to a concentration gradient with the potential gradient [16,17]:

$$J = -D \left(\nabla n + \frac{ze n}{kT} \nabla \phi \right) \quad (1)$$

where D is the diffusion coefficient, z the valency of the ion, e the electronic charge, k the Boltzmann constant, T the temperature, n the concentration of the ion, and ϕ is the potential. Also, the Poisson's equation is written as [16,17]:

$$\epsilon_0 \nabla \cdot [\epsilon(r) \nabla \phi(r)] = - \sum_{\text{ions}} z e n - \rho_{\text{ex}} \quad (2)$$

where $\epsilon(r)$ is the dielectric constant at an axial distance, r the sum over all ions gives the total mobile charge, ϵ_0 the dielectric constant of free space, and ρ_{ex} represents all the external fixed and induced charges. It is to be noted that, realistically, all the quantities in Eqs. (1) and (2) are varying along the ion channel axis [12,13]. This makes it notoriously difficult to obtain any analytical solution of the PNP equations, besides in some very specific cases [10]. However, it is possible to solve Eqs. (1) and (2) iteratively and obtain self-consistent solutions for the potential, concentrations and fluxes of the ions along the

channel axis [17]. Even though this paper deals with 1D PNP computations, it has been shown that the PNP equations can be extended to 3D with a more realistic channel representation and even closer fits to the experimental data [12].

2.2. The SILVACO simulator

SILVACO is a solid-state process and device simulator that has the general capabilities for numerical, physically based, 2D and 3D simulations of semiconductor devices [18]. It has two components: ATHENA, which is a 2D process simulation framework with software tools for modeling semiconductor fabrication processes, and ATLAS, which predicts the electrical behavior of semiconductor structures and provides insight into the internal physical mechanisms associated with device operation. ATLAS produces outputs in three forms: the run time output as a guide to the progress of the simulations running, log files storing summaries of the electrical output information, and the solution files storing the data related to the values of the solution variables within the device. The numerous carrier transport models, the availability of different material substrates, and the ability to account for other physical effects (e.g. surface charges, lattice heating, generation and recombination) have added greater flexibility to this device simulator.

Semiconductor device operation is modeled in ATLAS by a set of one to six coupled, non-linear partial-differential equations (PDE) [18]. ATLAS provides numerical solutions of these equations by calculating the values of the unknowns on a mesh of points within the device. The original, continuous model (similar to the PNP equations) is converted to a discrete, non-linear algebraic system by an internal discretization procedure. The sets of PDEs, the mesh and the discretization procedure determine the non-linear algebraic problem to be solved. This is solved using an iterative procedure that refines successive estimates of the solution. Different solution procedures (e.g. Gummel, Newton, or block iteration) exhibit different behavior with respect to convergence, accuracy, efficiency and robustness.

2.3. KcsA ion channel simulations with SILVACO

Based on its structure revealed by X-ray crystallography [2,13], we have built a KcsA channel model as shown in Fig. 1. The potassium channel is modeled here as a transmembrane lumen, surrounded by protein walls and with cylindrical reservoirs of potassium and chloride ions at two ends [4–13]. The channel extends from 10 to 50 Å, with a narrow selectivity filter of radius 1.5 Å and length 12 Å and a wider segment of length 23 Å. The selectivity filter extends into the extracellular space, while the wider segment tapers towards the intracellular space. Each reservoir at either end has a radius of 40 Å and a width of around 8 Å.

To replicate the shape of the KcsA channel, the structure is made of two materials: one to mimic the water continuum that is conducting, and the other to mimic the non-conducting protein walls [15,19]. The dielectric constants ϵ of the conducting and non-conducting mediums are set as 80 and 2, respectively. The entire device is constructed from 55 rectangular regions, which is the maximum limit for ATLAS [18]. Each conduct-

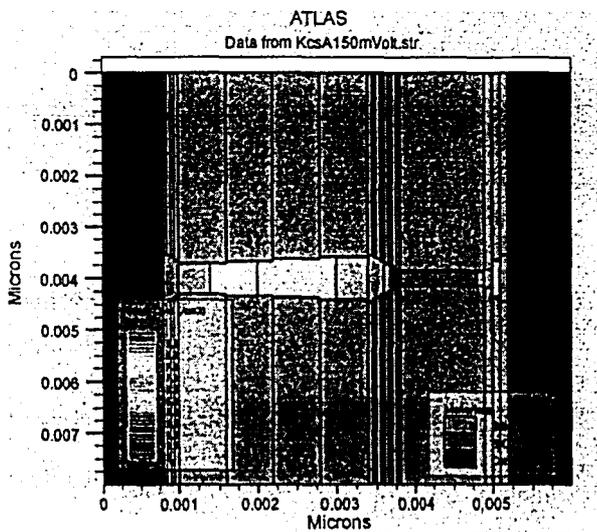


Fig. 1 – The model of a KcsA ion channel built in SILVACO. The channel extends from 10 to 50 Å, with a narrow selectivity filter of radius 1.5 Å and length 12 Å and a wider segment of length 23 Å. The selectivity filter extends into the extracellular space, while the wider segment tapers towards the intracellular space.

ing region has the capability of being defined with its unique material properties. To this end, the carrier doping and their diffusion coefficients are specified in each conducting region as shown in Fig. 2. This allows us to emulate the fact that there are considerably fewer carriers in the vestibule of the channel compared to in the reservoirs. Interestingly, the selectivity filter hardly has four to five ions at one instant [13], which is represented as an undoped region in Fig. 2. After the definition of the device structure, the mesh points are specified to

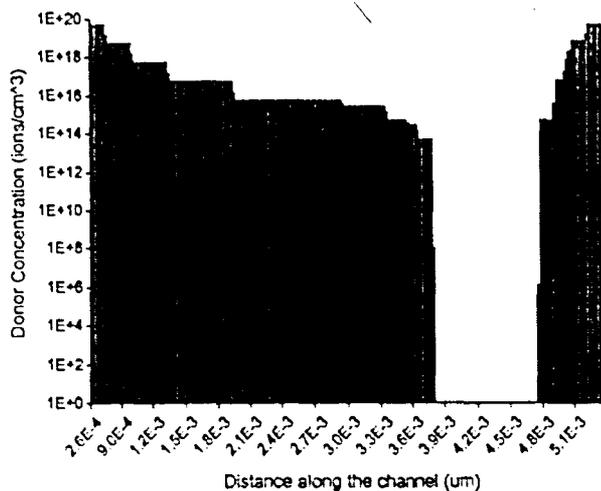


Fig. 2 – The doping profile of the various conducting regions in the KcsA model. The extracellular baths have a symmetric concentration of 100 mM equivalently, while the selectivity filter is left undoped. The profile is chosen to represent the realistic scenario in the vestibule of the channel [13].

denote the locations where solutions are to be determined. The mesh is defined by a series of horizontal and vertical lines and the spacing between them. With a maximum limit of only 9600 mesh nodes in ATLAS [18], it is important to use the mesh lines wisely and in locations which are crucial for the device behavior. Two electrodes, the source and drain, each of length 20 Å are placed at either ends of the reservoirs for applying a potential and measuring the electrodiffusion characteristics of the device.

Despite the fact that ion channels can be modeled as nanoscale electronic devices as discussed above, there are several issues to be addressed in their electrical simulations. The carriers in electronic devices are electrons and holes, while those in ion channels are charged ions bound by hydration shells [10]. The masses and radii of the semiconductor carriers are significantly small compared to those of ions in channels. Furthermore, the diffusion coefficient of electrons is around $500 \text{ cm}^2 \text{ s}^{-1}$, while that of K^+ ions is around $5 \times 10^{-7} \text{ cm}^2 \text{ s}^{-1}$. The energy band structure and crystalline structures of solid-state materials is well known, whereas that of liquids is less known. On the brighter side, the drift-diffusion PNP theory still holds for both solid-state devices and ion channels, providing a simplistic, macroscopic study of the flow of electrons and ions alike [15–17]. With this basis, we have incorporated many of the characteristics of ion flow into our channel model. Even though it is difficult to take into account the large mass and radii of ions, we have adjusted the diffusion coefficients of electrons in each conducting region to describe the slower motion of ions in a channel's vestibule [19]. Also, the net carrier doping and the degree of ionization is specified in a manner to predict decreased concentrations in the channel's vestibule and to obtain realistic current-voltage plots, as shown in Fig. 2. For this purpose, we have used the fact that the carrier doping density (per cm^3) is given by $n = 10^3 N_{\text{AV}} C$, where N_{AV} is the Avogadro's number and C is the concentration of the solution (mol/l). As will be demonstrated in the next section, with these modifications and appropriate mesh definition, it is possible to obtain realistic simulation results.

3. Results

The solid-state KcsA channel model was simulated using the PNP theory under various symmetric bath concentrations and potentials. The discretized PNP equations were solved by ATLAS using Gummel iteration and with each simulation runtime of <30 s.

Figs. 3 and 4 show the potential contours along the channel at a bath concentration of 100 mM and voltages of 100 and 200 mV, respectively. In Fig. 3, for example, a voltage potential of 100 mV was applied to the drain electrode in the reservoir at the right side, while the source electrode at the left side reservoir was kept at ground. The potential drops gradually along the channel, with most of the significant voltage drop occurring within the 12 Å length of narrow selectivity filter. Figs. 5 and 6 plot the electric field contours along the channel axis at 100 and 200 mV, respectively, and a 100 mM bath concentration. The electric field variations can be observed along the channel, with noticeable changes at either mouths of the narrow selectivity filter. The entrance and exit of the channel

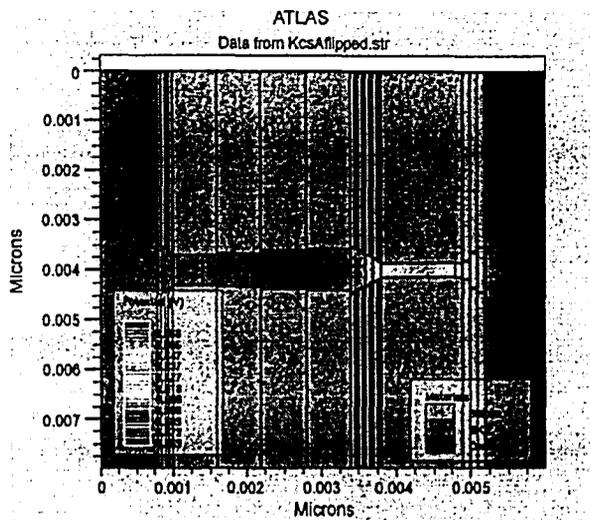


Fig. 3 – The SILVACO contour profile of the potential variation along the channel axis with 100 mV applied across the channel and extracellular bath concentrations of 100 mM.

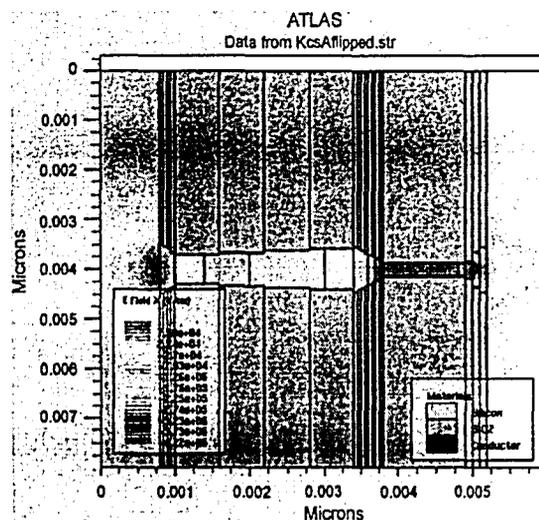


Fig. 5 – The SILVACO contour profile of the electric field variation along the channel axis with 100 mV applied across the channel and extracellular bath concentrations of 100 mM.

are made rounded, as any sharp boundaries cause problems while solving the Poisson's equation and lead to unwanted peaks.

Figs. 7 and 8 plot of the electric fields and potentials, respectively, along the channel for varying drain voltages and a bath concentration of 100 mM. As observed, the simulation program takes into account an inherent built-in potential of the structure, which is around ~ 0.575 V in this case. The origin of this potential is similar to that of Nernst Potential in ion channels as the SILVACO program considers the same Boltzmann energy distribution of carriers [10]. In this case, the bath concentration is $6 \times 10^{19} \text{ cm}^{-3}$ (or 100 mM equivalently) and the inside of the channel has an intrinsic concentration of

10^{10} cm^{-3} . Plugging this in the formula for the built-in potential $V = (kT/q) \ln(C_{\text{bath}}/C_{\text{channel}})$, we get a value of ~ 0.575 V. In Figs. 9 and 10, we plot the electric fields and potentials, respectively, along the channel for a fixed drain voltage of 100 mV and varying symmetric bath concentrations. As expected, the built-in potential increases with increasing extracellular concentrations.

In an attempt to check the validity of our model, we compare the current-voltage (IV) characteristics from our simulations with those of experiments [20]. Fig. 11 shows the corresponding IV plots of a KcsA channel at two symmetric bath concentrations of 250 and 500 mM. Using reverse engineering, the material properties of the solid-state KcsA structure

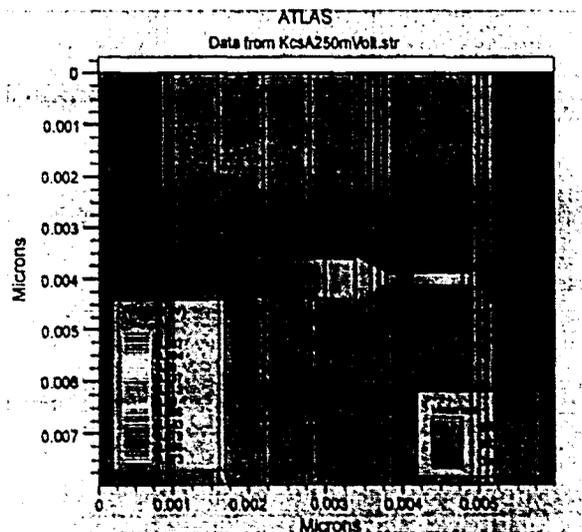


Fig. 4 – The SILVACO contour profile of the potential variation along the channel axis with 200 mV applied across the channel and extracellular bath concentrations of 100 mM.

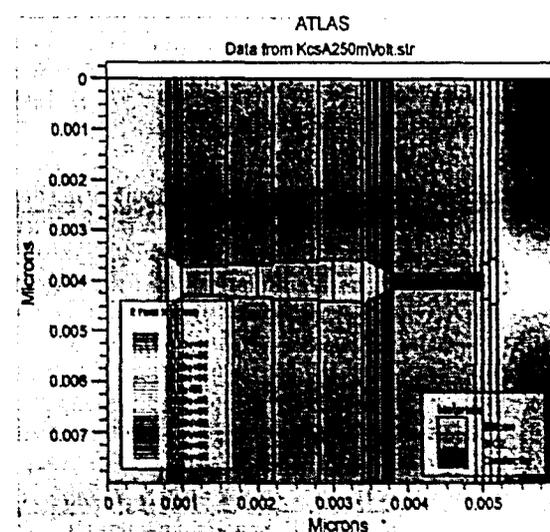


Fig. 6 – The SILVACO contour profile of the electric field variation along the channel axis with 200 mV applied across the channel and extracellular bath concentrations of 100 mM.

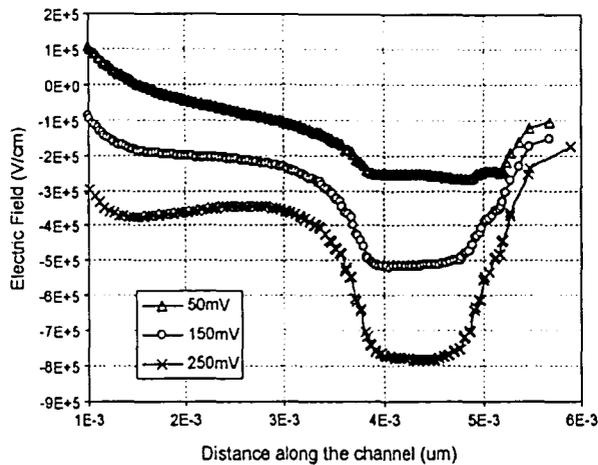


Fig. 7 - Plots of electric field variation along the channel axis at varying voltages applied across the channel and extracellular bath concentrations of 100 mM.

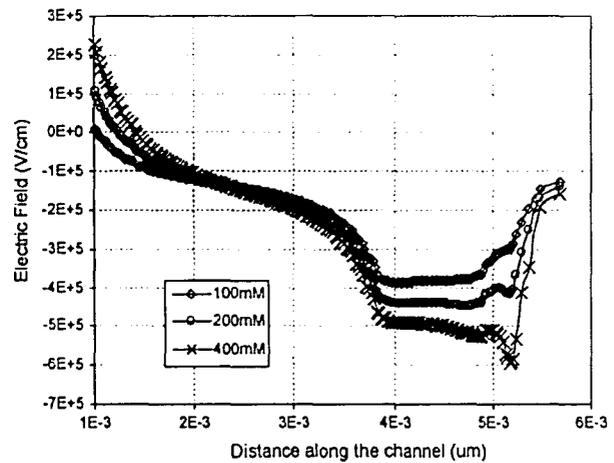


Fig. 9 - Plots of electric field variation along the channel axis at varying extracellular bath concentrations and an applied voltage of 100 mV across the channel. In each case, both the baths are symmetric, having the same concentration.

have been adjusted so as to mimic the realistic ion-channel structure and obtain a good fit between the IV curves. As seen from Fig. 11, the simulated IV curves closely agree with the experimental IV curves until 70 mV. Above this voltage, there is a slight tendency towards saturation in the experimental curves, whereas the simulated IV curves keep rising almost linearly. Nevertheless, this degree of agreement between our simulated results and the experimental IV curves is much better than those reported in the previous literature [9].

Next, we consider the effect of surface charges on the electrical properties of KcsA channels. These surface charges are known to influence the gating, conductance, and toxin-binding effects of KcsA ion-channels, and their actual physical locations are presumed to be in the selectivity filter [21]. Being negatively charged, these surface charges aid the permeation of cations and impede the flow of anions through the KcsA channel. Here, we explored the effects of such charges on ion permeation by placing three positive charges in the selectivity filter at the interface of water and protein walls (at 40, 44,

and 48 Å in Fig. 2). It is worth mentioning that the surface charges in our simulations are positive (each $Q_{SC} = 10^{14} \text{ cm}^{-2}$) since the majority carriers used in our model are electrons. The SILVACO program is versatile in allowing us to incorporate any fixed charges, interface traps, or even bulk traps at the semiconductor-insulator interface and observing their effects on the conduction of a device [18]. Fig. 12 plots the potential variation along the channel with a bath concentration of 100 mM and drain voltages of 0 V, 150 mV and 250 mV. In comparison to its steadily increasing nature in Fig. 7 (with no charges), the axial potential variation in Fig. 12 (with surface charges) has a plateau inside the selectivity filter, with three small humps resulting from the charges at those locations. The simulated IV curves (with and without charges) are plotted in Fig. 13 for a 250 mM bath concentration. Besides the

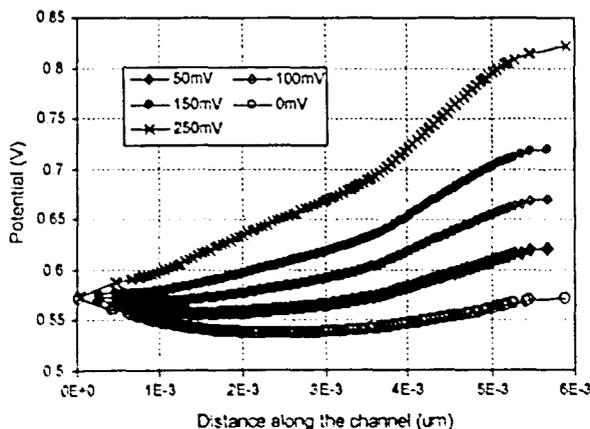


Fig. 8 - Plots of potential variation along the channel axis at varying voltages applied across the channel and extracellular bath concentrations of 100 mM.

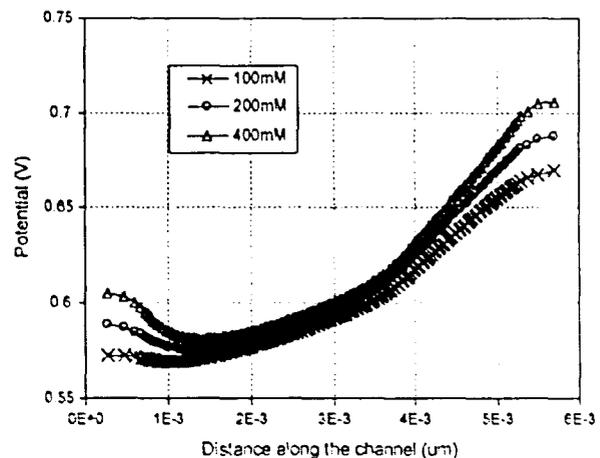


Fig. 10 - Plots of potential variation along the channel axis at varying extracellular bath concentrations and an applied voltage of 100 mV across the channel. In each case, both the baths are symmetric, having the same concentration.

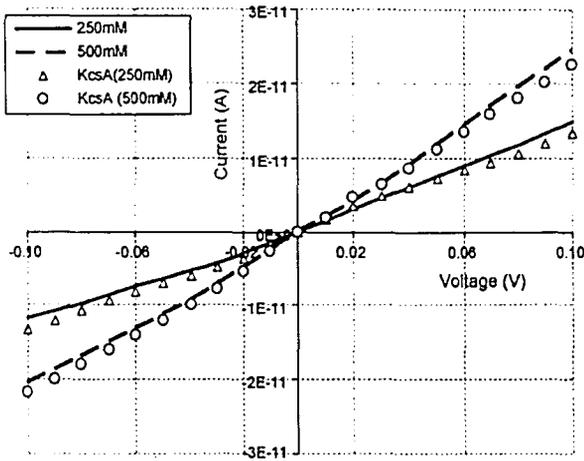


Fig. 11 – The current-voltage characteristics of the KcsA channel model at two different symmetric bath concentrations (250 and 500 mM). Comparison is made between the SILVACO simulated plots (—, 250 mM; ---, 500 mM) and the experimental data (Δ , KcsA: 250 mM; \circ , KcsA: 500 mM).

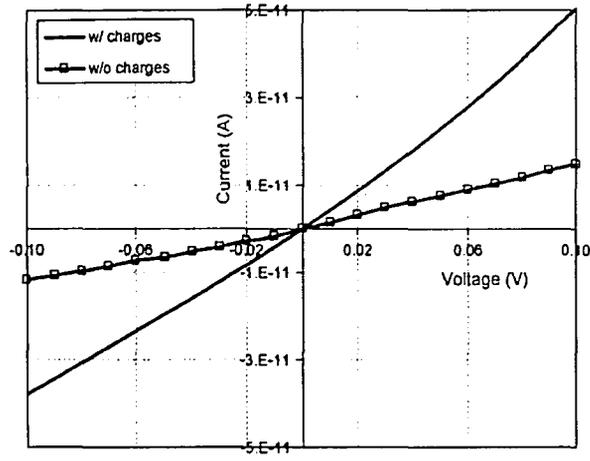


Fig. 13 – The simulated current-voltage characteristics of the KcsA channel model in the presence of surface charges and at two different symmetric bath concentrations (250 and 500 mM). Besides the increase in conductance, there is an enhancement in the majority carrier current and decrease in the minority carrier current. The nature and amount of surface charges is same as that in Fig. 12.

general increase in conductance, there is an added asymmetry in the linearity of the IV curves (in positive and negative voltage ranges) by surface charges. As seen in Fig. 13, the current component due to the majority carriers (electrons) is enhanced much more compared to that due to the minority carriers (holes) owing to the attractive and repulsive forces, respectively, exerted by the surface charges.

4. Discussion

We have demonstrated the possibility of representing a KcsA channel as a solid-state device, and employing a device simu-

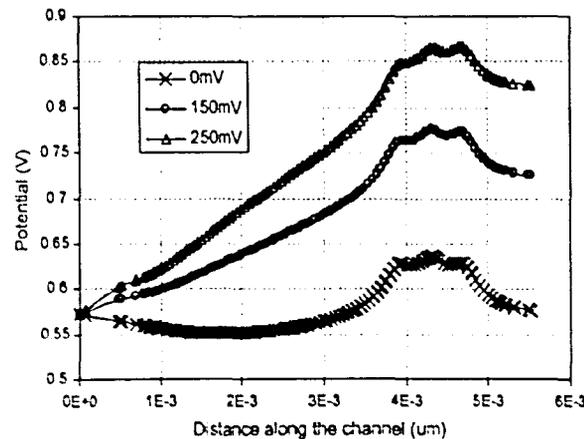


Fig. 12 – Plots of potential variation along the channel axis at varying voltages applied across the channel, in the presence of surface charges, and extracellular bath concentrations of 100 mM. Three pairs of charges (each $Q_{sc} = 10^{14} \text{ cm}^{-2}$) are located inside the selectivity filter at the interface between the water and protein walls (at 40, 44, and 49 Å in Fig. 2).

lator, SILVACO, to simulate its electrical characteristics. With a goal to mimic the realistic and computationally feasible scenario inside an ion channel, we created a model with well-adjusted material parameters and employed SILVACO to obtain self-consistent solutions of the axial potential and ion fluxes. The simulated IV curves closely match the available experimental results, supporting the validity of the model.

Besides giving insight into the general ion permeation mechanisms in a channel's vestibule, the simulation results do open exciting opportunities to extend this work. Additional features can be incorporated in the model to bridge the gap between the nature of a semiconductor-insulator and a water-protein wall interface. In solid-state devices, the interface between a semiconductor and an overlying insulator is sharp and abrupt, while the dielectric boundary at a channel's water-protein wall interface is not so distinctly defined. This dielectric boundary and its curvature is important in deciding an ion's potential energy, which varies as $1/r_{water}$ in the baths and as $1/r_{protein}$ inside the channel [22]. Even though the precise value of $\epsilon_{protein}$ is not crucial, it would better our model to put an additional protein region ($\epsilon_{protein} \cong 10$) at the dielectric boundary to smoothen the sharp water-protein wall interface. Also, it is suspected that the dielectric constant of water decreases inside the channel, and recently Monte Carlo simulations have shown that lowering its dielectric constant in a channel's vestibule alters a channel's selectivity for different ions [5]. Studies can be performed to investigate the effects of changing ϵ_{water} on the channel permeation and its selectivity for monovalent or divalent ions.

Although our model is based on macroscopic drift-diffusion computations, they do describe the experimental IV data surprisingly well. It is, however, tempting to be able to perform simulations at molecular and atomistic levels (Monte Carlo and Brownian dynamics) with the computational ease of FNP programs [19]. In this context, a common platform can

be built which has the capability of running molecular-level simulations for a short timeframe, inferring the ion-transport parameters, and feeding them to the SILVACO program to calculate the ion fluxes within reasonable time. Such a hybrid model would blend the accurate predictions of molecular-level simulations with the computationally cheap macroscopic flux calculations.

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Vitae

Akwete Bortei-Doku was born on 4th June, 1982 in the city of Cape Coast, Ghana. He began his schooling in Abidjan in the Ivory Coast and continued in Accra, the capital of Ghana in 1989. He attended high school at Achimota School, Ghana's top public high school after which he was accepted into Lehigh University in 2001, where he completed his Bachelor of Science degree in Electrical Engineering. He was accepted into the Department of Electrical Engineering and Computer Science Masters program with Dr. Marvin White as his advisor. He has been a Lehigh University Presidential Scholarship recipient and has been on the Sherman Fairchild fellowship for the past year. He completed his studies for the Masters Program in 2007 after which he plans to continue his studies for the PhD program from the same university. He has been a student member of the IEEE for the past four years and is also a member of the Sigma Xi Society.

END OF TITLE