2011

Design of an Integrated Complex Filter System for RF Applications Using Log-domain Filtering

Kanlun Li
Lehigh University

Design of an Integrated Complex Filter System for RF Applications Using Log-domain Filtering

by

Kanlun Li

A Thesis

Presented to the Graduate Research Committee

of Lehigh University

in Candidacy for the Degree of

Master of Science

In

Electrical and Computer Engineering

Lehigh University

August 2011

Thesis is accepted and approved in partial fulfillment of the requirements for the Master of Science in Electrical and Computer Engineering

Design of an integrated complex filter system for RF applications using log-domain filtering

Kanlun Li

_____

Date Approved

_____

Prof. Douglas R. Frey
Thesis Advisor

_____

Prof. Fil Bartoli
Chair of Electrical and Computer Engineering Department

Acknowledgements

Among the many people who have made this thesis possible, I would like to foremost express my gratitude to my academic advisor, Prof. Douglas R. Frey. As a talented circuit designer, he was so inspirational and supportive throughout the duration of my project: he held rigorous attitude toward each detail and always kept my spirits up by giving insightful advice on my design. Studying with him is a precious experience during my stay at Lehigh University, and has made me pretty sure about my career goal for the future ten years. I would also like to thank Prof. Svetlana Tatic-Lucic, for her guidance and support in the first one year and a half of my study at Lehigh University.

And my former lab mates: Gaoshan Jing, Markus Gnerlich, and Umer Izhar; especially Gaoshan, who devoted great patience in training me doing biology experiments and treated me in a nice and straightforward manner.

Finally, I thank my parents for their continuous support, inspiring encouragement and unconditional love; my boyfriend Bo, for understanding, supporting and spoiling me.

Table of Contents

List of Figures

List of Tables

Abstract

This thesis demonstrates the development of a current-mode system that integrates a front end mixer, an intermediate complex filter and a back end demodulator, based on the theory of log domain filtering and the technique of state-space synthesis. The unique features of this system involve: (1) it is realized only with BJTs, current sources, capacitors and no op amps; (2) the intermediate complex filter is designed according to a specific state-space description and it integrates a multiple input multiple output second-order band pass filter that is conveniently and precisely tunable in both Q and f_c; (3) the topology of each block and the whole system is implemented with great symmetry, which is preferable in IC layout.

1. Introduction

1.1Motivation for Current Mode Filter Design

Integrated high-frequency tunable filter design has become a hot research topic in recent years; for example, the design of an electronically tunable anti-aliasing filter for use in digital video was proposed in [1] and [2]-[4] discussed the design of high-frequency filters in both bipolar and CMOS technology. Although a variety of topologies have been studied in these papers, they suffered from the high-frequency limitations of active elements and increasing circuit complexity due to the use of master-slave system configurations. To overcome the frequency limitations of active components, current-mode elements were incorporated in the design. In reference [5]-[8], current conveyors were used as active elements in filter implementations and even switched-capacitor filters have been designed from the current-mode perspective [9]. However, these designs still either contained voltage-mode elements, such as operational amplifiers, or were virtually using configurations to process voltage at some internal nodes and behaving similarly to voltage-mode filters. To tackle the challenge, Roberts and Sedra presented a design in [10] to realize a fundamentally verifiable current-mode filter. Seevinck also proposed an integrator in [11] which was genuine current mode. Despite the effort, neither design was generally applicable or practically implementable.

In summary, filters that are electronically tunable and immune to high-frequency distortion have found application in a variety of RF electronic devices and are promising in modern filter design. Since current-mode filters are superior to voltage-mode filters in many cases, methodologies for current-mode filter design have been intensively studied, and a mature technique that could be adopted to guide the reliable implementation of current-mode filters is in dire need.

1.2 Log Domain Filtering and State-space Synthesis Technique

In 1992, a novel approach to the current-mode filter design that involves applying an exponential mapping to the state-space description of a filter was elaborated by Frey in [12]. Inspired by Adams' 'log-domain' filter that will be discussed in the next section, Frey's implementation strategy only requires the use of transistors, current sources and capacitors in circuit realization, therefore generalizing the design of Adams by introducing a complete distortionless synthesis procedure. Furthermore, state variables defined by this strategy are intrinsically related to current rather than voltage in the resulting circuits due to the exponential mapping. This fact emphasizes the current-mode nature of the design. In [12], a general biquadratic filter section and a seventh-order Chebychev low pass filter were designed using the proposed methodology, and implemented with complementary bipolar processes. Both circuits were shown to be tunable over a two-decade range in frequency without distortion.

1.2.1 Introduction to Adam's Log Filter

The idea of 'log-domain filtering' was first proposed by Adams in 1979[13]. It is claimed that by feeding the natural logarithm of the input current to a 'filter' that only contains diodes, capacitors, current sources and op-amps, it is possible to obtain at some node the natural logarithm of a linearly filtered original input current, in voltage form. Subsequent exponentiation would translate the voltage back into a current and produce an output that is a linearly filtered version of the input current. Simply put, a linear transfer function could be implemented with a highly nonlinear circuit.

A simple example of the log-filtering idea introduced by Adams is given by the network in Fig. 1. The network can be divided into three parts. In the front end, the left-most diode D1 and the voltage follower work together to convert the input current into a voltage signal, whose

value is the natural logarithm of the input current, and send it to the following 'log filter'. The 'log filter' functions as a special low pass filter, whose output- i.e., the voltage across the capacitor-is proved to be the natural logarithm of the low pass filtered input current. The back end consists of a level shifter followed by an exponentiator that implements the voltage-to-current conversion, which is a process of solving for the antilogarithm of the output signal from the preceding 'log filter'.

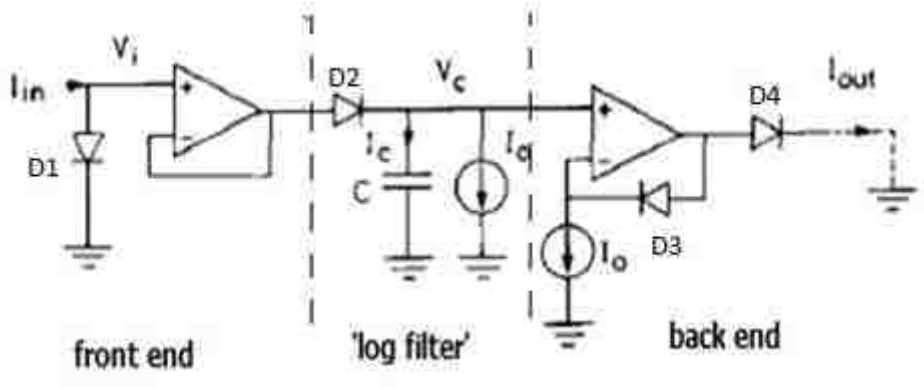


Fig. 1 Adam's basic log-domain filter

The quantitative analysis of such network is shown below, where the diodes are assumed to obey the ideal diode law and is constantly in forward bias.

Front end Input current is converted to a voltage which is a log function of the current:

$$V_i = \frac{1}{k} \ln\left(\frac{I_{D1}}{I_s}\right) = \frac{1}{k} \ln\left(\frac{I_{in}}{I_s}\right) \tag{1}$$

where I_{D1} is the current flowing in the first diode D1;

I_s is the reverse bias saturation current for an ideal diode;

$k = \frac{q}{KT}$ is the inverse of thermal voltage V_T . q is the magnitude of charge on an electron; K is the Boltzmann constant; T is the absolute temperature in Kelvin of the p-n junction.

'Log filter' The output voltage of 'log filter' V_C is related with V_i by the following equation:

$$C\frac{dV_c}{dt} = C\dot{V_c} = I_c = I_{D2} - I_0 = I_s e^{k(V_i - V_c)} - I_0 \tag{2}$$

where I_{D2} is the current of the second diode D2.

Back end Since the current flowing in the level shifter diode D3 is forced to be I_0, the voltage across it could be expressed as :

$$V_{D3} = \frac{1}{k}\ln\left(\frac{I_0}{I_s}\right) \tag{3}$$

Obviously, the voltage applied to the last diode is $V_C + V_{D_3}$, therefore

$$I_{out} = I_s e^{k(V_C + V_{D_3})} = I_0 e^{kV_C} \tag{4}$$

Derivation of transfer function

In order to figure out the relationship between I_{in} and I_{out} , combination and transformation is applied to the obtained equations. By observation, (1), (2) and (4) produces:

$$C\dot{V_c}e^{kV_C} = I_s e^{kV_i} - I_0 e^{kV_C} = I_{in} - I_{out} \tag{5}$$

Define $X = e^{kV_C}$ and get:

$$I_{out} = I_0 X \tag{6}$$

$$\dot{X} = k\dot{V_c}e^{kV_C} = \frac{\dot{I_{out}}}{I_0} \tag{7}$$

$$\dot{I_{out}} = I_0\,\dot{X} = kI_0\dot{V_c}e^{kV_C} \tag{8}$$

Substitute (8) into (5):

$$C\dot{V_c}e^{kV_C} = \frac{C}{kI_0}\dot{I_{out}} = I_{in} - I_{out} \tag{9}$$

(6), (7) and (9) yield the function relationship between I_{in} and I_{out} :

$$C\dot{X} + kI_0 X = kI_{in} \tag{10}$$

$$\dot{I_{out}} + \frac{kI_0}{C}I_{out} = \frac{kI_0}{C}I_{in} \tag{11}$$

From this analysis, it is clear that the network in Fig.1 implements a linear differential equation relating the output to the input in current mode; hence the output is a linearly filtered version of the input. Equation (11) above suggests a transfer function of a one-pole low pass

filter, with cutoff angular frequency at $\frac{kI_0}{C}$. This result could also be achieved by assuming the input to be a small signal added to a DC level. In this case, the diode in the 'log filter' acts as a resistor which equals to the dynamic impedance of a diode with I_0 flowing in it. Therefore the 'log filter' is equivalent to a simple RC low pass filter, with $R = V_T/I_0 = 1/(kI_0)$ and the cutoff angular frequency $w_0 = 1/(RC) = kI_0/C$. Based on the small signal analysis, Adams suggested that any RC active filter should have a log-filter counterpart where resistors are replaced with diodes. However, the nonlinear term in the differential equation is noteworthy since it indicates distortion at the output even under ideal conditions.

Potential merits of the log filter include: First, it is electronically tunable over several decades of frequency by adjusting the magnitude of internal current sources; therefore, such a design strategy might be useful at high frequencies. Second, by comparing the definition of X in large signal analysis with the equation describing the ideal diode law, it is interesting to note that although X is a function of voltage, it intrinsically represents a current. Such a definition relates the voltage across the capacitor in a 'log filter' with a current which could be written as a state variable of the system state equation. Such perspective is appealing in the design of a genuine current-mode filter.

Despite these promising advantages, a major downside in Adam's original design is the absence of a distortionless synthesis procedure, which leaves some uncertainty for designers to evaluate whether a log filter would be acceptable for a given application. Another drawback is the dependence of such network on op amps in the process of logging, level shifting and exponentiating. It would predictably bring forth serious degradation to the filter in practice, due to the non-ideal parameters of the adopted op amps , such as DC offset, DC bias, noise and frequency-response limitations.

1.2.2 State-space Synthesis Technique

The distortionless synthesis procedure proposed by Frey is now introduced for the creation of log filters. Suppose the dynamical equations corresponding to a desired filter function is of the following standard form

State equation: $$\dot{X} = AX + BU \tag{12}$$

Input-output equation: $$Y = CX + DU \tag{13}$$

where $X = (x_1, x_2, \dots, x_n)^T$ is the state vector, U is the scalar input, A is an $n \times n$ matrix, B is an $n \times 1$ vector, C is a $1 \times n$ vector, and D is a scalar. Then, define the change of variables as:

$$x_i = e^{kV_i} \tag{14}$$

$$U = I_{dc}e^{ku} \tag{15}$$

where k is some positive real number, and I_{dc} is some nominal current value. These equations define the mapping from the positive real numbers x_i and $U \subset R^+$ to V_i and $u \subset R$. The following equation is acquired by directly substituting the specific expression of X and U back into the original state equation:

$$k(\dot{V}_1 e^{kV_1}, \dot{V}_2 e^{kV_2}, \dots, \dot{V}_n e^{kV_n})^T = A(e^{kV_1}, e^{kV_2}, \dots e^{kV_n})^T + BI_{dc}e^{ku} \tag{16}$$

Multiplying both sides of (16) by$(C_i/k)e^{-kV_i}$,

$$C_i\dot{V}_i = \left[\sum_{j=1}^{n} \frac{C_i}{k} A_{ij} e^{k(V_j - V_i)}\right] + \frac{C_i}{k} B_i I_{dc} e^{k(u - V_i)} = \left[\sum_{j=1}^{n} I_{aij}\, e^{k(V_j - V_i)}\right] + I_{bi} e^{k(u - V_i)} \; \forall 1 \le i \le n \tag{17}$$

where $I_{aij} = \frac{C_i}{k} A_{ij}$, $I_{bi} = \frac{C_i}{k} B_i I_{dc}$.

Now these equations could be interpreted to be a set of nodal equations, where V_i represents the i^{th} node voltage. Therefore, the left-hand side term $C_i\dot{V}_i$ is the current flowing in a grounded capacitor tied to the ith node, and the right-hand side of the equation can be taken as

the sum of currents entering or leaving this capacitor. The physical meaning and implementation method for terms on the right hand side of eqn.(17) are analyzed as below to prepare for further design.

First of all, categorize the terms from the right-hand side of eqn. (17) into three types and make proper definitions for convenience of the subsequent implementation.

$$I_{aij}e^{k(V_j-V_i)} = I_s e^{k[(V_j+V_{aij})-V_i]} \quad \text{for } I_{aij}>0 \text{ and } i \neq j \quad (18a)$$

$$= -I_s e^{k[V_j-(V_i-V_{aij})]} \quad \text{for } I_{aij}<0 \text{ and } i \neq j \quad (18b)$$

$$I_{aii}e^{k(V_i-V_i)} = I_{aii} \quad (19)$$

$$I_{bi}e^{k(u-V_i)} = I_s e^{k[(u+V_{bi})-V_i]} \quad \text{for } I_{bi}>0 \quad (20a)$$

$$= -I_s e^{k[u-(V_i-V_{bi})]} \quad \text{for } I_{bi}<0 \quad (20b)$$

Then, define $V_{aij} = \frac{1}{k}\ln(|I_{aij}|/I_s)$ (21a)

$$V_{bi} = \frac{1}{k}\ln(|I_{bi}|/I_s) \quad (21b)$$

Compare the definition above with the constitutive law for standard diodes working in forward conduction, i.e., $I = I_s\left(e^{(\frac{q}{KT})V}-1\right) \approx I_s e^{(\frac{q}{KT})V}$ if $I \gg I_s$, where I is the current flowing in the diode, I_s is the reverse bias saturation current for an ideal diode, q is the magnitude of charge on an electron, K is the Boltzmann constant and T is the absolute temperature in Kelvin of the p-n junction. It is easy to discover that as long as $k = \frac{q}{KT}$, V_{aij} (V_{bi}) represents the voltage across a diode with forward current of $|I_{aij}|$ ($|I_{bi}|$) flowing through it. This analogy interprets the physical meaning of the right hand side terms of equation (17) in a straightforward way that they are either a constant current or the current through a 'junction' obeying the standard diode constitutive law.

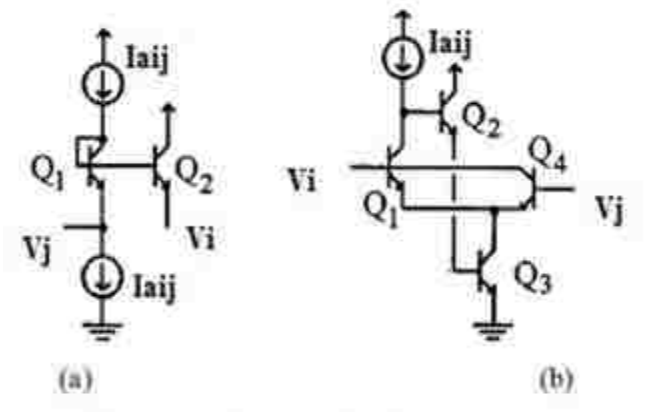


Fig. 2 Circuit implementation for (a) $I_s e^{k[(V_j+V_{aij})-V_i]}$ and (b) $-I_s e^{k[V_j-(V_i-V_{aij})]}$

The term "$I_s e^{k[(V_j+V_{aij})-V_i]}$" in (18a) essentially represents the current flowing through a 'junction' that follows the ideal diode constitutive law and with voltage $V_j + V_{aij} - V_i$ across it. $V_j + V_{aij}$ is achieved by shifting up the j^{th} node voltage V_j by a 'diode' drop of V_{aij}, which could be acquired using a 'logging diode' with a current of I_{aij} flowing in it. To implement this term, assume the 'junction' to be the base-emitter junction of an ideal NPN transistor, which works in active region. Then, the "$I_s e^{k[(V_j+V_{aij})-V_i]}$" is obviously the emitter current of the transistor when its base is connected to $V_j + V_{aij}$ and emitter connected to V_i. Fig. 2a provides a circuit implementation of such term. The current flowing in the emitter of Q2 equals $I_s e^{k[(V_j+V_{aij})-V_i]}$ in ideal condition.

The term "$I_s e^{k[(u+V_{bi})-V_i]}$" in (20a) is similar to the term "$I_s e^{k[(V_j+V_{aij})-V_i]}$" in (18a) and it requires a voltage of $u + V_{bi}$ available at some node. Such voltage, call it u_i, could be mathematically constructed as $u_i = u + V_{bi} = \frac{1}{k}\ln(U/I_{dc}) + \frac{1}{k}\ln(I_{bi}/I_s) = \frac{1}{k}\ln(\frac{I_{bi}}{I_{dc}}U/I_s)$. Therefore, u_i is the voltage across a diode with current $\frac{I_{bi}}{I_{dc}}U$ flowing in it. If set $I_{bi} = I_{dc}$, then $u_i = \frac{1}{k}\ln(U/I_s)$, where U is always a positive real number as defined in eqn. (15). It is easy to

obtain u_i with a 'logging diode' placed at the input of the system. It is noteworthy that each input current needs to be offset to constantly flow in one direction.

The term "$-I_s e^{k[V_j-(V_i-V_{aij})]}$" in (18b) describes a negative current. By "negative" it means that the current is flowing out of some node. Such a term could be implemented by connecting the node to the collector of an ideal NPN transistor whose base is tied to V_j and emitter is connected to $V_i - V_{aij}$, which is achieved by down shifting the voltage at the ith node- i.e.,V_i- by a diode drop of V_{aij}. Fig. 2b gives an example of realizing the negative current. With the help of Q2 and Q3, a current of I_{aij} is forced to flow in Q1. It follows that the collector current of Q4, $I_s e^{k[V_j-(V_i-V_{aij})]}$, is pulled out of node i. The fact naturally results in the negative sign for the current. The term "$-I_s e^{k[u-(V_i-V_{bi})]}$" in (20b) can be avoided by forcing I_{bi} to be constantly positive, for the convenience in circuit design. We hence skip the discussion on the implementation of this term.

Apply the same mapping method and subsequent processing to the input-output equation and we obtain

$$Y = \left(\sum_{i=1}^{n} I_{ci} e^{kV_i}\right) + I_d e^{ku} \tag{22}$$

where $I_{ci} = C_i$ and $I_d = DI_{dc}$. Obviously, each term at the right hand side of eqn. (22) could be implemented using the technique described above.

What is noteworthy is that the above development holds only when the state variables x_i and the input U are constantly positive. Such a constraint calls for further investigation. For U, adding a DC offset component would provide an input that never goes to zero or negative. Since the transfer function from U to Y is linear, this operation simply adds a DC shift to the final output without changing the filter response to the nominal input. For state variables to be always positive, the processing technique is more complex. Forcing appropriate equilibrium conditions

would be the first step, and it will guarantee that when all the capacitors are replaced by open circuits, the transistor-current source network would have a suitable DC solution. For example, assume after a certain state-space transformation to the original dynamical equations, we have in the transformed co-ordinates the state-space equation below:

$$0 = \mathrm{AX} + \mathrm{BU} \Longrightarrow \mathrm{x_i} > 0 \forall \mathrm{i} \text{ whenever } \mathrm{U} > 0 \tag{23}$$

Let the original dynamical equations be expressed as

$$\frac{\mathrm{d}\widetilde{\mathrm{X}}}{\mathrm{dt}} = \widetilde{\mathrm{A}}\widetilde{\mathrm{X}} + \widetilde{\mathrm{B}}\mathrm{U} \qquad \mathrm{Y} = \tilde{\mathrm{C}}\widetilde{\mathrm{X}} + \widetilde{\mathrm{D}}\mathrm{U} \tag{24}$$

Then apply the linear transformation $\mathrm{X} = \mathrm{M}\widetilde{\mathrm{X}}$ and impose the DC equilibrium constraint that $\mathrm{X} = \mathrm{X_0} = (\mathrm{x_{01}}, \mathrm{x_{02}}, \ldots, \mathrm{x_{0n}})^{\mathrm{T}}$ where $\mathrm{x_{0i}} > 0$ when $U = \mathrm{I_{dc}} > 0$.It gives us

$$0 = \mathrm{M}\widetilde{\mathrm{A}}\mathrm{M}^{-1}\mathrm{X_0} + \mathrm{M}\widetilde{\mathrm{B}}\mathrm{I_{dc}} \Longrightarrow -\mathrm{X_0} = \mathrm{M}\widetilde{\mathrm{A}}^{-1}\widetilde{\mathrm{B}}\mathrm{I_{dc}} \tag{25}$$

where $\mathrm{M}\widetilde{\mathrm{A}}\mathrm{M}^{-1} = \mathrm{A}$ and $\mathrm{M}\widetilde{\mathrm{B}} = \mathrm{B}$ in (23).

Eqn. (25) sets a number of constraints on the choice of transformation M. Since the elements of M are generally under-constrained by the equations, one can choose M to optimize the sparsity of the transformed matrices A and B. After transformation, the input-output equations also get new matrices: $\mathrm{C} = \tilde{\mathrm{C}}\mathrm{M}^{-1}$ and $\mathrm{D} = \widetilde{\mathrm{D}}$.

In practice, the fact that the actual circuit implementation will be made with transistors of finite gain guarantees that the currents in the network-i.e. the state variables in the mathematical model-will always remain bounded; therefore, the capacitor voltages can only change at a finite rate. Although it has been verified in simulation that large transients in high-Q networks do cause serious distortion for a period of time, since the bounds on the state-variable excursions can be easily exceeded, designs can nevertheless be made free of problems by appropriately scaling the signals in system.

The general design procedure using the state space synthesis technique is now outlined as follows: First, determine the state-space representation for given filter transfer function. This can be done by using a companion-form approach. Typically, high-order filters are constructed based on a single state-space model, or by a cascade of lower-order state-space models. Then, apply a transformation to the obtained dynamical equations in order to force an appropriate DC operating point for the filter. The transformation should be linear and nonsingular so that the new state-space presentation would implement the same transfer function as the old one does. Such transformation will involve some trial and error to find a best circuit implementation; hence, it requires some intuitive perspective of the whole system. Having determined a transformed linear state equation, the exponential transformation is applied as presented above, resulting in a set of nodal equations in the form of eqn. (17) and eqn. (22). The nodal equations would suggest an interconnection of transistors, capacitors and current sources for the realization of the system.

1.3 Project Introduction

1.3.1 System Block Diagram and Possible Application

The proposed system consists of a mixer block, a complex filter block and a mixer-based demodulator block, as shown in Fig. 3. A quick review of superheterodyne receivers would provide an example for the application of such system.

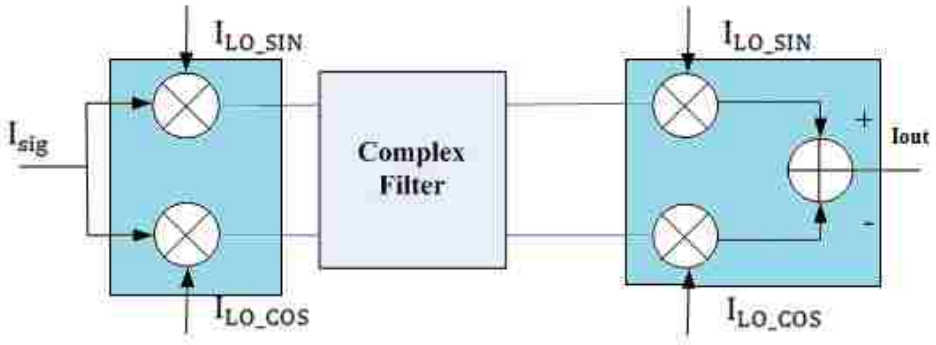


Fig. 3 Block diagram of the proposed complex filter system

Fig. 4 shows the block diagram of a typical superheterodyne receiver: the signal from the antenna is first filtered by a band pass filter with high center frequency for band selection. A local oscillator in the receiver produces a sine wave to mix with the processed signal, shifting it to an intermediate frequency (IF), usually a lower frequency. The output signal of the mixer is then band pass filtered, amplified and possibly processed in additional ways to provide an IF signal with good quality. Then the demodulator uses the IF signal to recreate a copy of the baseband signal. According to Fig. 3, the proposed system in this thesis would perform signal down conversion, IF-centered band pass filtering and FM signal demodulation as an integrated block. Also, the complex filter alone could work individually as a band pass filter for band selection.

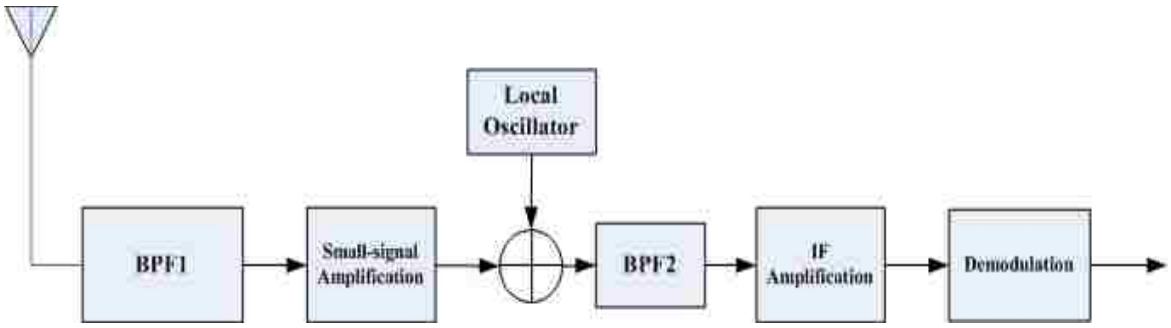


Fig. 4 Block diagram of a typical superheterodyne receiver

1.3.2 Design Spec.

For the convenience in design review, some specs for the system are set in advance.

Input signal: $I_{sig} = A_{sig}\sin(2\pi * f_{sig} * t) = (0.1m)\sin(2\pi * 4MHz * t)$

Signals provided by local oscillator:

$$I_{LO\_SIN} = A_{LO}\sin(2\pi * f_{LO} * t) = (0.1m)\sin(2\pi * 5MHz * t)$$

$$I_{LO\_COS} = A_{LO}\cos(2\pi * f_{LO} * t) = (0.1m)\cos(2\pi * 5MHz * t)$$

Intermediate frequency/ center frequency of complex filter:

$$f_c = IF = |f_{LO} - f_{sig}| = 5MHz - 4MHz = 1MHz$$

Offset DC current for each AC signal: $I_{off} = 0.5m$

1.4 Summary

This thesis starts from the introduction to log domain filtering theory and the state-space synthesis technique given above. Then it discusses in detail the design and implementation procedure of an integrated current-mode complex filter system using such a technique. It is hoped that throughout the study, a better understanding of log domain filtering could be established, and a synthesis technique based on this principle for the design of mixers, filters and other related RF applications can be demonstrated and generalized.

2. Mixer Block Design

In the mixer block, the system input current is separately mixed with two sinusoidal current signals generated by the local oscillator, which are identical in amplitude and frequency but 90 degrees apart in phase. The block performs multiplication in parallel, producing two output currents both with frequency components that present the sum and difference of the mixed frequencies. Quantitative analysis based on the trigonometric identity is given below to describe the function of an ideal mixer. Note that

$$\sin\alpha\sin\beta = -\frac{1}{2}\cos(\alpha+\beta)+\frac{1}{2}\cos(\alpha-\beta) \tag{26a}$$

$$\sin\alpha\cos\beta = \frac{1}{2}\sin(\alpha+\beta)+\frac{1}{2}\sin(\alpha-\beta) \tag{26b}$$

According to the system spec, replacing $\sin\alpha$ and $\sin\beta$ in (26a) with $A_{sig}\sin(2\pi f_{sig}t)$ and $A_{LO}\sin(2\pi f_{LO}t)$, and replacing $\sin\alpha$ and $\cos\beta$ in (26b) with $A_{sig}\sin(2\pi f_{sig}t)$ and $A_{LO}\cos(2\pi f_{LO}t)$, the unscaled current products are formulated below:

$$\begin{aligned} I_1(t) &= A_{sig}\sin(2\pi f_{sig}t) * A_{LO}\sin(2\pi f_{LO}t) \\ &= -\frac{1}{2}A_{sig}A_{LO}\cos[2\pi(f_{sig}+f_{LO})t]+\frac{1}{2}A_{sig}A_{LO}\cos[2\pi(f_{sig}-f_{LO})t] \\ &= -\frac{1}{2}(0.1m)^2\cos[2\pi(4meg+5meg)t]+\frac{1}{2}(0.1m)^2\cos[2\pi(4meg-5meg)t] \\ &= -\frac{1}{2}(0.1m)^2\cos(2\pi*9megt)+\frac{1}{2}(0.1m)^2\cos(2\pi*1megt) \end{aligned} \tag{27a}$$

$$\begin{aligned} I_2(t) &= A_{sig}\sin(2\pi f_{sig}t) * A_{LO}\cos(2\pi f_{LO}t) \\ &= \frac{1}{2}A_{sig}A_{LO}\sin[2\pi(f_{sig}+f_{LO})t]+\frac{1}{2}A_{sig}A_{LO}\sin[2\pi(f_{sig}-f_{LO})t] \\ &= \frac{1}{2}(0.1m)^2\sin[2\pi(4meg+5meg)t]+\frac{1}{2}(0.1m)^2\sin[2\pi(4meg-5meg)t] \\ &= \frac{1}{2}(0.1m)^2\sin(2\pi*9megt)-\frac{1}{2}(0.1m)^2\sin(2\pi*1megt) \end{aligned} \tag{27b}$$

In addition to the sum and difference of the mixed frequencies shown in eqn. (27a) and (27b), the output of a real mixer may contain other frequency components such as DC signal and the original frequencies themselves. It is desired that the mixer block produces as few extra frequency components as possible. On the other hand, to ensure the output of a current mixer to have unit of first power, the product is usually divided by a scale factor in the form of a current. The following sections discuss two approaches to the implementation of the mixer block. The first approach is based on the state-space synthesis technique as discussed in Chapter 1, and the second approach utilizes the variable-transconductance principle [14].

2.1 Design with the State-space Synthesis Technique

Recall that the state-space synthesis technique deals with constantly positive current variables, so a DC offset must be added to each current sent into the mixer. The offset current for any AC signal is set to 0.5mA and is denoted as I_{off} in the system spec. As shown in Fig. 2(a), the product of two positive currents is an exponential function of the sum of two corresponding diode drops provided that the junctions approximately obey the ideal diode constitutive law. Two design issues are noteworthy during the circuit implementation:

1. Properly scaling the current product.
2. Regulating the DC offset of both output signals to be the same

Since the output of the mixer block is a current flowing in certain transistor, the constitutive law governs that the voltage difference between the base and the emitter of the output transistor should be only one diode drop. It implies that the output current is a scaled current product. Another perspective would be that since the output current is supposed to have unit of first power, the result given by (27a) and (27b) has to be divided by a scale factor which is in the form of a current. For convenience, the current for scaling-e.g., I_{sc}- is set to 0.5mA .

Regulating the DC offset of both output signals is important because it would greatly facilitate the subsequent process. As for the following core filter to work properly, it requires its input signals to have the same DC offset. Realizing such regulation requires forcing a proper DC operating point for the circuit.

Based on the discussion above, the output of the proposed mixer block is constructed as below:

$$I_{out1} = \frac{1}{I_{sc}}[(I_{sig} + I_{off})(I_{LOsin} + I_{off}) + (-I_{sig} + I_{off})(-I_{LOsin} + I_{off}) - {I_{off}}^2]$$

$$= \frac{2I_{sig}I_{LOsin} + {I_{off}}^2}{I_{sc}} \quad (28a)$$

$$I_{out2} = \frac{1}{I_{sc}}[(I_{sig} + I_{off})(I_{LOcos} + I_{off}) + (-I_{sig} + I_{off})(-I_{LOcos} + I_{off}) - {I_{off}}^2]$$

$$= \frac{2I_{sig}I_{LOcos} + {I_{off}}^2}{I_{sc}} \quad (28b)$$

Substitute the specific value of each variable into (28a) and (28b),

$$I_{out1} = \frac{2}{0.5m}\left[-\frac{1}{2}(0.1m)^2\cos(2\pi * 9MHz * t) + \frac{1}{2}(0.1m)^2\cos(2\pi * 1MHz * t)\right] + 0.5m$$

$$= -20u\cos(2\pi * 9megt) + 20u\cos(2\pi * 1megt) + 0.5m \quad (29a)$$

$$I_{out2} = \frac{2}{0.5m}[\frac{1}{2}(0.1m)^2\sin(2\pi * 9megt) + \frac{1}{2}(0.1m)^2\cos(2\pi * 1megt)] + 0.5m$$

$$= 20u\sin(2\pi * 9megt) - 20u\sin(2\pi * 1megt) + 0.5m \quad (29b)$$

Inspired by the first-order low pass filter designed in [15], a mixer is designed as shown in Fig. 5. Recall the dynamic equations for a low pass filter with the cutoff frequency at w_0 and unity gain at low frequency:

$$\dot{X} = -w_0X + w_0U \quad (30a)$$

$$Y = X \quad (30b)$$

If the input variable U can be implemented as a scaled current product, then the output Y would represent a low-pass-filtered input. A challenge of applying state-space synthesis technique to the implementation of a mixer is the design of a proper input stage. Specifically, we need to build a circuit with a nodal equation in the form of (30a) and an input that is a scaled current product with proper DC offset. From eqn. (28a) and (28b), the input signal could be taken as the summation of two current products subtracted by the offset current product. It is obvious that two sets of the circuit block in Fig. 2(a) and one set of the circuit block in Fig. 2(b) are needed. In Fig. 5, it is the three subparts formed by Q3, Q4, I_{sh1}; Q7, Q8, I_{sh2}; and Q9,Q10,Q11,Q12, Isc that realize the summing and subtracting of the current products. Note that each subpart has an input voltage that is two-diode drop, denoted by V1, V2 and V3. The implementation of a two-diode drop is simply connecting two NPN base-emitter junctions carrying the current to be multiplied. In Fig. 5, V1 is achieved with Q1, I_{LOsin_pos}, Q2 and I_{sig_pos}; V2 is achieved with Q5, I_{LOsin_neg}, Q6 and $_{Isig\_neg}$; and V3 is achieved with Q15, I_{off}, Q14 and I_{off2}.

To implement the low pass filtering, a capacitor with one end grounded and a current source pulling current from the capacitor is needed. The two components in conjunction determine the cutoff frequency of the filter. The ungrounded end of the capacitor is connected to the emitter of Q4, Q8 and the collector of Q11. The voltage at this node is two-diode drop which is a natural log function of the unscaled output current. The structure that consists of Q9, I_{sc}, Q10 and Q12 forces I_{sc} to flow in Q9, so there is one diode drop of V_{sc} from the base of Q9 to the base of Q13. It follows that the current flowing in Q13 is the scaled current product.

Since VC in Fig. 5 is two-diode drop, the base of Q4 and Q8 should be three-diode drop. Therefore, a one-diode drop shift up from the emitter of Q3 to the base of Q4, and from the emitter of Q7 to the base of Q8 is required, and it involves selecting proper value for I_{sh1}, I_{sh2} and

I_{sh3}. This is accomplished by making DC analysis on the circuit. Assume that all the AC signals are off, then V1, V2 and V3 would have the same value which is a voltage of two-diode drop corresponding to $Ioff^2$. According to KCL, the amount of the current flowing into the capacitor should balance that of the current flowing out of it. A straightforward solution involves setting $I_{sh1}=I_{sh2}=I_{sh3}=I_{sc}=I_{off}$, so that VC would be a voltage of two-diode drop corresponding to $Ioff^2$. Such a solution is not the only one that constructs the DC equilibrium for the mixer. Discussion regarding how to find a proper DC operating point through quantitative analysis is not in the scope of this study.

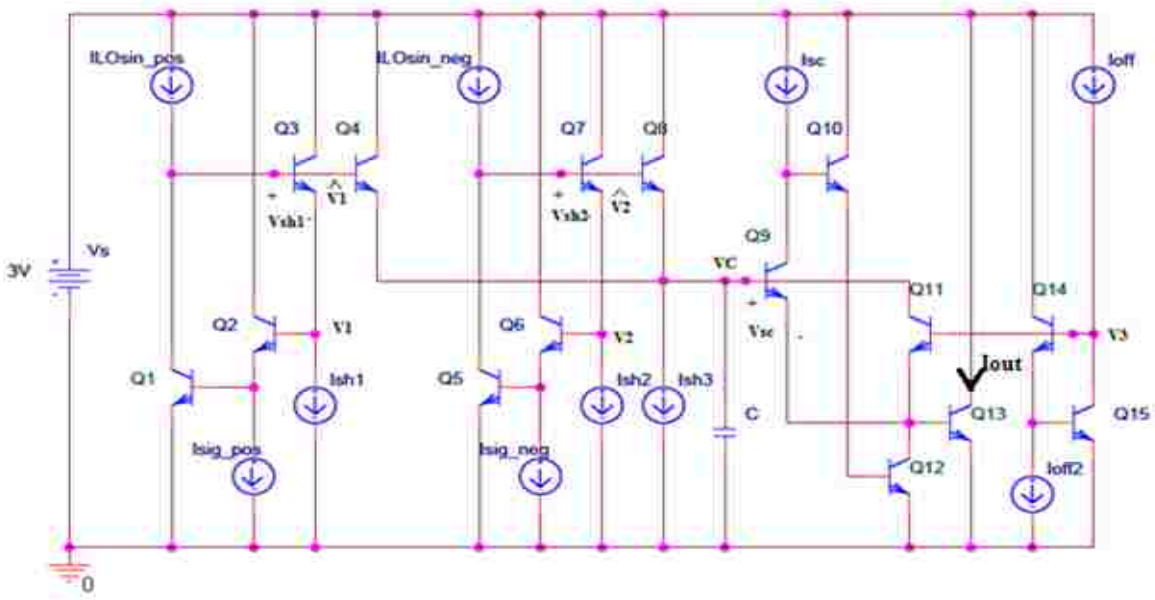


Fig. 5 Schematic of a mixer designed with the state-space synthesis technique

Detailed large signal analysis to the circuit in Fig. 5 is shown below:

Assume: $X = I_s e^{k(V_C - V_{SC})} \quad \Longrightarrow \quad \dot{X} = k\dot{V_C} I_s e^{k(V_C - V_{SC})}$ (31a)

$$U_0 = I_s^2 e^{kV_1} + I_s^2 e^{kV_2} - I_s^2 e^{kV_3} \Longrightarrow$$

$$U_0 = (I_{LO\_sin} + I_{off})(I_{sig} + I_{off}) + (-I_{LO\_sin} + I_{off})(-I_{sig} + I_{off}) - I_{off}^2$$

$$= 2I_{LO\_sin} I_{sig} + I_{off}^2 \quad (31b)$$

$$Y = X = I_s e^{k(V_C - V_{SC})} \quad (31c)$$

The nodal equation describing the current in the capacitor can be written as:

$$C\dot{V_C} = -I_{sh3} + I_s e^{k(\widehat{V_1}-V_C)} + I_s e^{k(\widehat{V_2}-V_C)} - I_s e^{k(V_3+V_{sc}-V_C)} \tag{32}$$

Comparing the left hand side of (32) with (31a), and multiplying both sides of (32) with $\frac{1}{CV_t} I_s e^{k(V_c-V_{sc})}$, we get:

$$\dot{X} = -\frac{I_{sh3}}{CV_t} I_s e^{k(V_C-V_{sc})} + \frac{1}{CV_t} I_s^2 e^{k(\widehat{V_1}-V_{sc})} + \frac{1}{CV_t} I_s^2 e^{k(\widehat{V_2}-V_{sc})} - \frac{1}{CV_t} I_s^2 e^{kV_3}$$

$$= -\frac{I_{sh3}}{CV_t}\frac{I_s^2 e^{kV_C}}{I_{sc}} + \frac{I_{sh3}}{CV_t}\frac{I_{sh1}}{I_{sh3}}\frac{I_s^2 e^{kV_1}}{I_{sc}} + \frac{I_{sh3}}{CV_t}\frac{I_{sh2}}{I_{sh3}}\frac{I_s^2 e^{kV_2}}{I_{sc}} - \frac{I_{sh3}}{CV_t}\frac{I_{sc}}{I_{sh3}}\frac{I_s^2 e^{kV_3}}{I_{sc}} \tag{33}$$

Assume $w_0 = \frac{I_{sh3}}{CV_t}$ and $I_{sh1} = I_{sh2} = I_{sh3} = I_{sc}$,

$$\dot{X} = -w_0 X + w_0\left(\frac{U_0}{I_{sc}}\right) = -w_0 X + w_0 U \qquad \text{where } U = \frac{U_0}{I_{sc}} \tag{34}$$

(34) and (31c) together suggests that the output of the circuit is a low-pass filtered version of the input signal. Since the circuit has a stable DC operating point, the voltage change at the ungrounded end of the capacitor is negligible. Therefore, $\dot{X}$ in eqn. (34) is approximately zero. It indicates that the output of the circuit in Fig. 5 equals the input which is a scaled current product. Fig. 6 shows the schematic of the mixer block that contains two identical mixers proposed in Fig. 5 with different input and without any capacitor. To decrease the hardware cost, two mixers share the offset DC voltage that corresponds to $Ioff^2$. The current flowing in Q20 and Q35 represents the output of the mixer block.

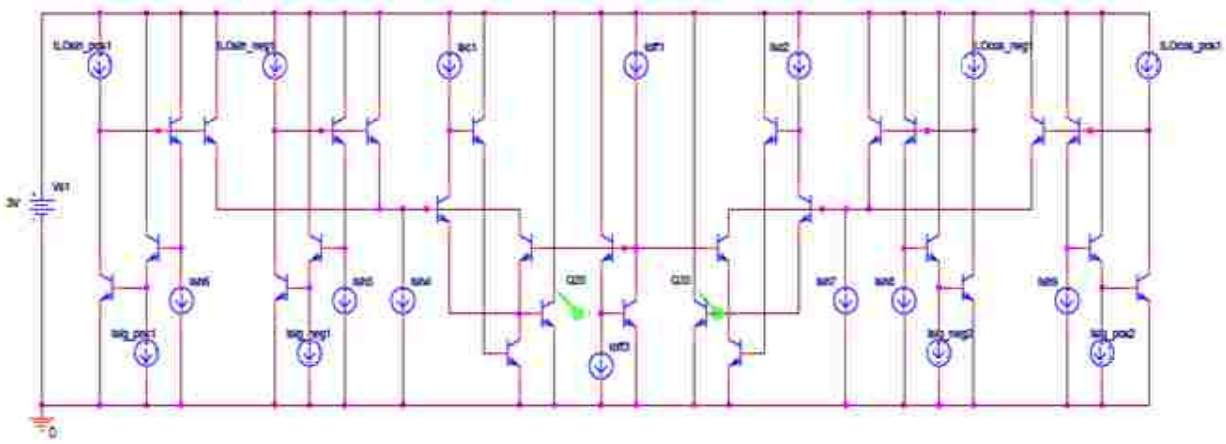


Fig. 6 Schematic of a mixer block designed with the state-space synthesis technique

The value of each current source in the circuit is listed as below:

$$I_{sig\_pos1} = I_{sig\_pos2} = I_{sig} + I_{off} = (0.1\text{m})\sin(2\pi * 4\text{MHz} * t) + 0.5\text{m}$$

$$I_{sig\_neg1} = I_{sig\_neg2} = -I_{sig} + I_{off} = -(0.1\text{m})\sin(2\pi * 4\text{MHz} * t) + 0.5\text{m}$$

$$I_{LOsin\_pos1} = I_{LO\_sin} + I_{off} = (0.1\text{m})\sin(2\pi * 5\text{MHz} * t) + 0.5\text{m}$$

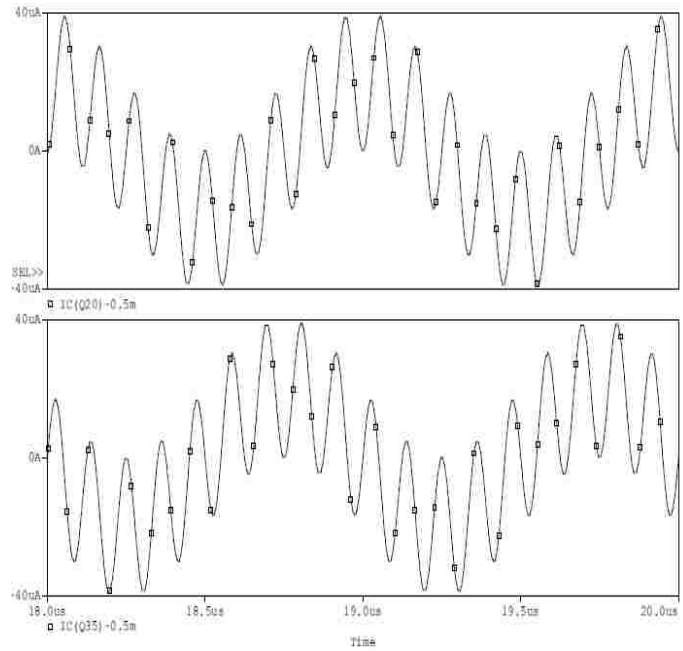
$$I_{LOsin\_neg1} = -I_{LO\_sin} + I_{off} = -(0.1\text{m})\sin(2\pi * 5\text{MHz} * t) + 0.5\text{m}$$

$$I_{LOcos\_pos1} = I_{LO\_cos} + I_{off} = (0.1\text{m})\cos(2\pi * 5\text{MHz} * t) + 0.5\text{m}$$

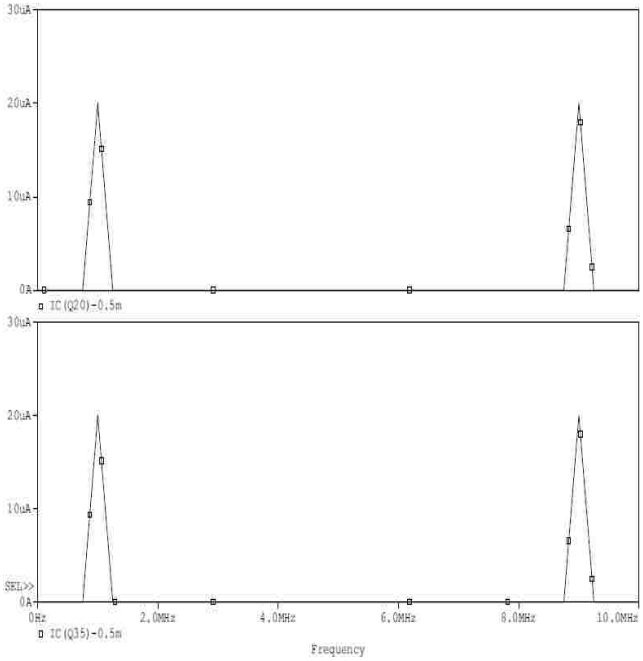
$$I_{LOcos\_neg1} = -I_{LO\_cos} + I_{off} = -0.1\text{m} * \cos(2\pi * 5\text{MHz} * t) + 0.5\text{m}$$

$$I_{sh6} = I_{sh5} = I_{sh4} = I_{sh7} = I_{sh8} = I_{sh9} = I_{off1} = I_{off3} = I_{sc1} = I_{sc2} = I_{off} = 0.5\text{m}$$

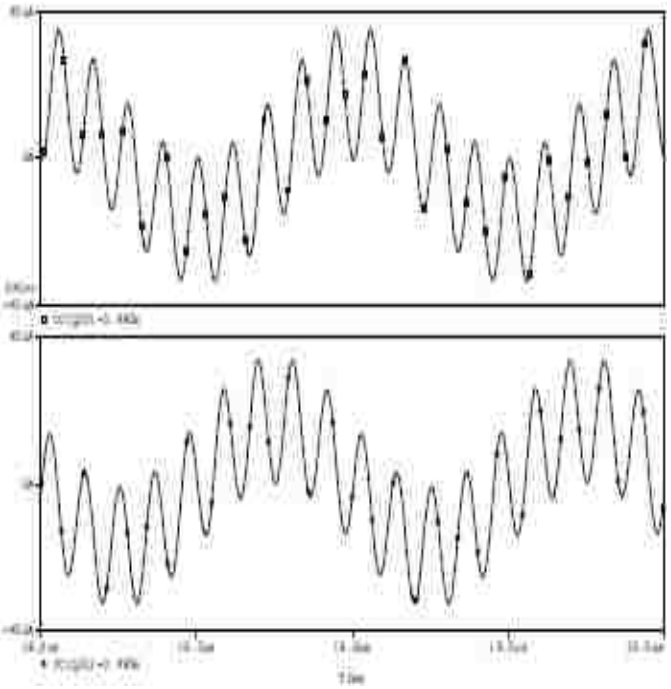
Fig. 7a shows the result of PSpice simulation on the circuit in Fig. 6 with ideal NPN model and Fig. 7b shows the result of the simulation with real NPN model, which is given in the Appendix. The plots in Fig. 7(a1),(a2) agree quite well with eqn. (29a) and eqn. (29b), but the plots in Fig. 7(b1),(b2) display an output with smaller amplitude and unexpected frequency components. Specifically, the output offset is 0.495m which has -1% error compared to 0.5m and the amplitude of both 1MHz and 9MHz components is 17.5uA which has -12.5% error compared to 20uA.



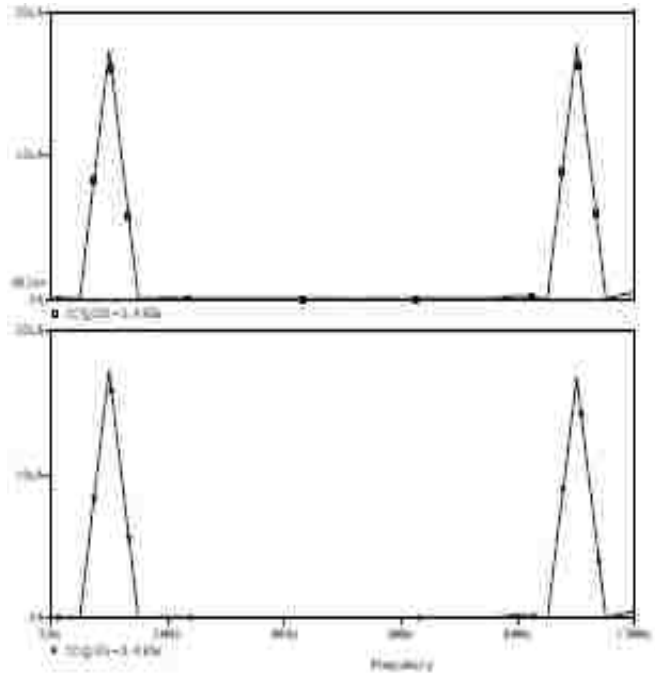
(a1)



(a2)



(b1)



(b2)

Fig. 7

2.2 Design with the Variable-transconductance Principle

Another design approach is based on the variable-transconductance principle. The principle is utilized in the monolithic four-quadrant multipliers to achieve small error over a wide frequency range and is briefly introduced below. In the circuit block shown in Fig. 8, the differential pair Q3-Q4 provides the variable transconductance, and the diode-connected pair Q1-Q2 provides the proper base drive for the former. Assume the BJTs are matched and they all have negligible base currents. By KVL, $V_{BE1} + V_{BE4} - V_{BE3} - V_{BE2} = 0$, so $V_{BE3} - V_{BE4} = V_{BE1} - V_{BE2}$. The logarithmic characteristics of ideal BJTs gives that $V_t \ln \frac{i_3}{i_4} = V_t \ln \frac{i_1}{i_2}$, or $\frac{i_3}{i_4} = \frac{i_1}{i_2}$. This can be rewritten as $(i_3 - i_4)/(i_3 + i_4) = (i_1 - i_2)/(i_1 + i_2)$. Rearrange terms,

$$i_3 - i_4 = (i_1 - i_2)(i_3 + i_4)/(i_1 + i_2) \tag{35}$$

Eqn. (35) indicates the circuit's ability to multiply the current difference $(i_1 - i_2)$ by the total emitter current$(i_3 + i_4)$ and scale the product by $(i_1 + i_2)$. Moreover, the offset current must be added to ensure that i1, i2, i3 and i4 always flow in the same direction.

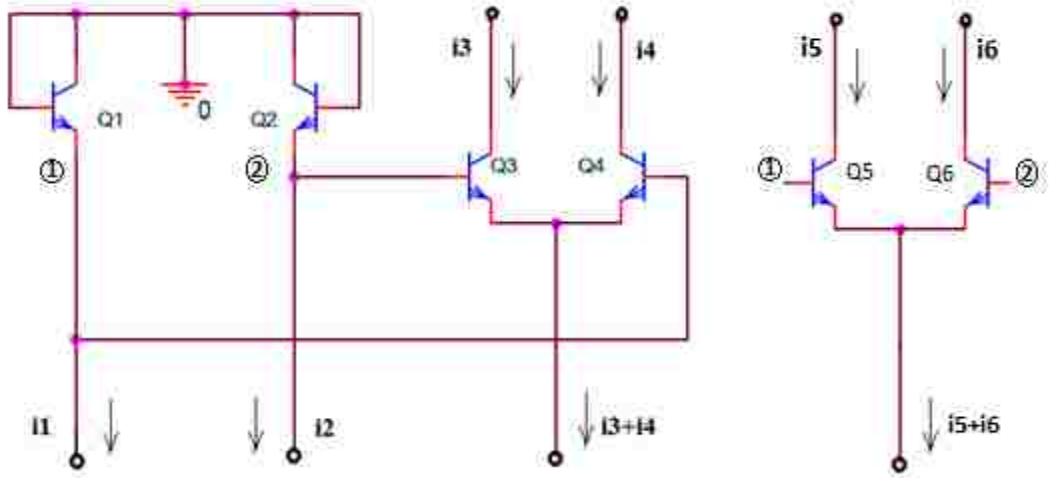


Fig. 8 Linearized transconductance block

Using the variable-transconductance principle to implement a multiplier is not complex if we can first mathematically construct the scaled current product in a proper way. Eqn. (35) naturally suggests the idea of expressing a scaled current product by the combination of current differences. A specific example is given below using the data from the system spec.

$$\text{Assume } "I_1 - I_2" = I_{sig\_pos} - I_{sig\_neg} = (I_{sig} + I_{off}) - (-I_{sig} + I_{off}) = 2I_{sig}$$

$$= 2(0.1\text{m})\sin(2\pi * 4\text{MHz} * t) \quad (36a)$$

$$\text{so } "I_1 + I_2" = I_{sig\_pos} + I_{sig\_pos} = (I_{sig} + I_{off}) + (-I_{sig} + I_{off}) = 2I_{off} = 2 * 0.5\text{m} = 1\text{m} \quad (36b)$$

$$\text{Set } "I_3 + I_4" = I_{LOsin\_pos} = I_{LOsin} + I_{off} = (0.1\text{m})\sin(2\pi * 5\text{MHz} * t) + 0.5\text{m} \quad (37a)$$

Substitute these results into eqn. (35),

$$"I_3 - I_4" = ("I_1 - I_2")("I_3 + I_4")/("I_1 + I_2") = I_{sig}(I_{LOsin} + I_{off})/I_{off} \quad (38)$$

Adding in another current summation $"I_5 + I_6"$ that is similar to $"I_3 + I_4"$ function wise, and

$$\text{setting } "I_5 + I_6" = I_{LOsin\_neg} = -I_{LOsin} + I_{off} = -0.1\text{m}\sin(2\pi * 5\text{MHz} * t) + 0.5\text{m} \quad (39)$$

then by a similar calculation, we get

$$"I_5 - I_6" = ("I_1 - I_2")("I_5 + I_6")/("I_1 + I_2") = I_{sig}(-I_{LOsin} + I_{off})/I_{off} \quad (40)$$

Subtract eqn. (40) from eqn. (38),

$$("I_3 - I_4") - ("I_5 - I_6") = ("I_3 + I_6") - ("I_4 + I_5") = 2I_{sig}I_{LOsin}/I_{off}$$

$$= 2(0.1\text{m})^2\sin(2\pi * 4\text{MHz} * t)\sin(2\pi * 5\text{MHz} * t)/0.5\text{m}$$

$$= -(20\text{u})\cos(2\pi * 9\text{MHz} * t) + (20\text{u})\sin(2\pi * 1\text{MHz} * t) \quad (41)$$

To ensure that the current difference above is constantly positive, it is necessary to offset $"I_3 + I_6"$ with a proper DC current. In the context of given spec, I_{off} is set to 0.5m. Therefore, $"I_3 + I_6"$ in (41) becomes $("I_3 + I_6" + I_{off})$, and the final output is:

$$I_{out1} = ("I_3 + I_6" + I_{off}) - ("I_4 + I_5")$$

$$= -(20\text{u})\cos(2\pi * 9\text{MHz} * t) + (20\text{u})\cos(2\pi * 1\text{MHz} * t) + 0.5\text{m} \quad (42)$$

The other output could be constructed the same way by setting

$$"I_3 + I_4" = I_{LOcos\_pos} = I_{LOcos} + I_{off} = 0.1m * \cos(2\pi * 5MHz * t) + 0.5m \quad (43)$$

$$"I_5 + I_6" = I_{LOcos\_neg} = -I_{LOcos} + I_{off} = -0.1m * \cos(2\pi * 5MHz * t) + 0.5m \quad (44)$$

Conducting similar calculation,

$$I_{out2} = ("I_3 + I_6" + I_{off}) - ("I_4 + I_5")$$

$$= (20u)\sin(2\pi * 9meg * t) - (20u)\sin(2\pi * 1meg * t) + 0.5m \quad (45)$$

Note that the output signals shown in eqn. (42) and eqn. (45) are identical to the outputs of the mixer block proposed in Fig.6, as shown in (29a) and (29b). It indicates the feasibility of using Fig. 8 as a basic unit to implement another mixer block.

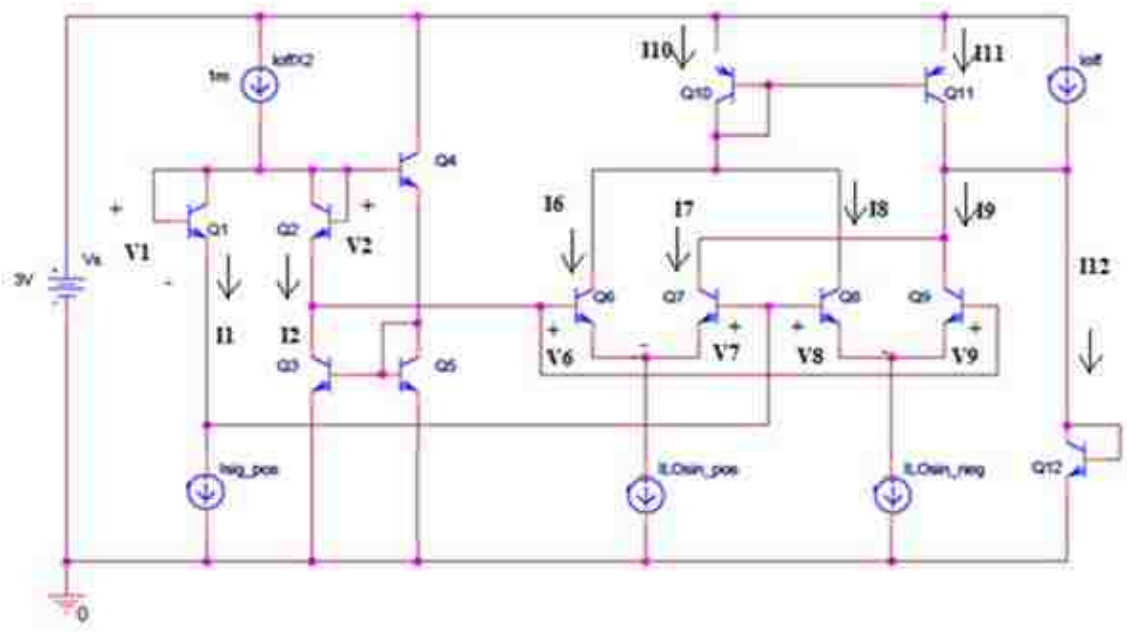


Fig. 9 Schematic of a designed mixer using the variable-transconductance principle

Fig. 9 shows the design of a mixer based on the variable-transconductance principle. Q1, Q2, Q3, Q4, Q5 and the current sources of I_{offX2}, I_{sig_pos} work in conjunction to force I_{sig_pos} flowing in Q1 and I_{sig_neg} flowing in Q2. The two currents correspond to "I_1" and "I_2" in the analysis above. The sum of the currents flowing in Q6 and Q7 is I_{LOsin_pos}, and that of the

currents flowing in Q8 and Q9 is I_{LOsin_neg}. They correspond to "$I_3 + I_4$" and "$I_5 + I_6$" respectively. Apply KCL to the interconnection of Fig. 9,

$$-V1 - V7 + V6 + V2 = 0 \implies V1 - V2 = V6 - V7 \tag{46a}$$

$$-V1 - V8 + V9 + V2 = 0 \implies V1 - V2 = V9 - V8 \tag{46b}$$

Considering the logarithmic relationship between the voltage drop and the current of an ideal PN junction, equations that describe the currents of interest is derived using (46a) and (46b):

$$\frac{I1}{I2} = \frac{I6}{I7} \implies I6 - I7 = (I1 - I2)(I6 + I7)/(I1 + I2) \tag{47a}$$

$$\frac{I1}{I2} = \frac{I9}{I8} \implies I9 - I8 = (I1 - I2)(I8 + I9)/(I1 + I2) \tag{47b}$$

The difference between (I6-I7) and (I9-I8) equals the difference between (I6+I8) and (I7+I9). Therefore, the collectors of Q6, Q8 and Q10 are connected together to force the current sum of (I6+I8) to flow in Q10. The same connection method is applied to Q7, Q9 and Q11 to pull the current sum of (I7+I9) out of Q11. Note that Q10 and Q11 form a current mirror, so the current flowing in Q11 equals (I6+I8). To obtain a constantly positive current difference as the final output, I_{off} is pushed into Q11 to provide a DC offset. I12 is the output of the mixer, which could be formulated as:

$$\begin{aligned} I12 &= (I11 + I_{off}) - (I7 + I9) = (I10 + I_{off}) - (I7 + I9) \\ &= (I6 + I8) - (I7 + I9) + I_{off} = (I6 - I7) - (I9 - I8) + I_{off} \\ &= \frac{(I1-I2)[(I6+I7)-(I8+I9)]}{I1+I2} + I_{off} = \frac{2I_{sig}I_{LOsin}}{I_{off}} + I_{off} \end{aligned} \tag{48}$$

To implement a mixer block with two outputs as formulated in eqn. (42) and eqn. (45), two sets of circuit block in Fig. 9 are connected and modified as shown in Fig. 10. Since the ideal BJT models with high β are used in simulation, the base current of each transistor is negligible. It follows that the left-most block which provides I_{sig_pos}, I_{sig_neg} and the corresponding voltage

drops could be shared by the two subsequent parallel blocks that contain current sources of I_{LOsin_pos}, I_{LOsin_neg} and I_{LOcos_pos}, I_{LOcos_neg} respectively. It decreases the circuit hardware complexity and would not influence the correctness of applying the variable-transconductance principle to the circuit loops of concern. Current flowing in Q53 and Q65 represents the output of the mixer block.

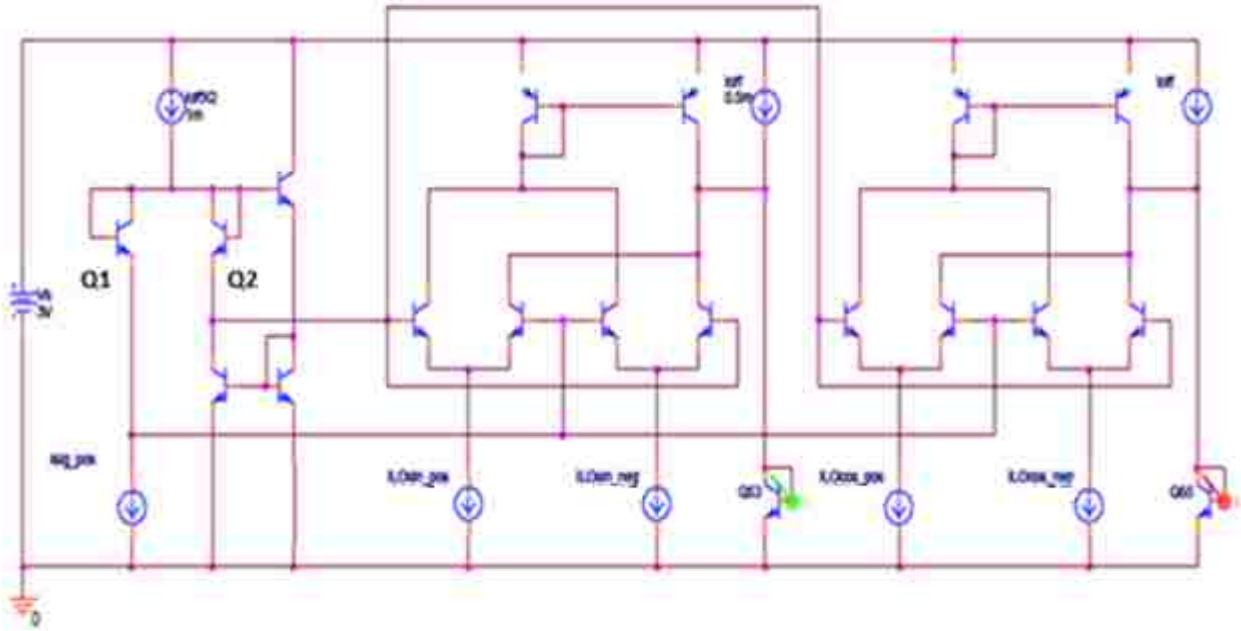
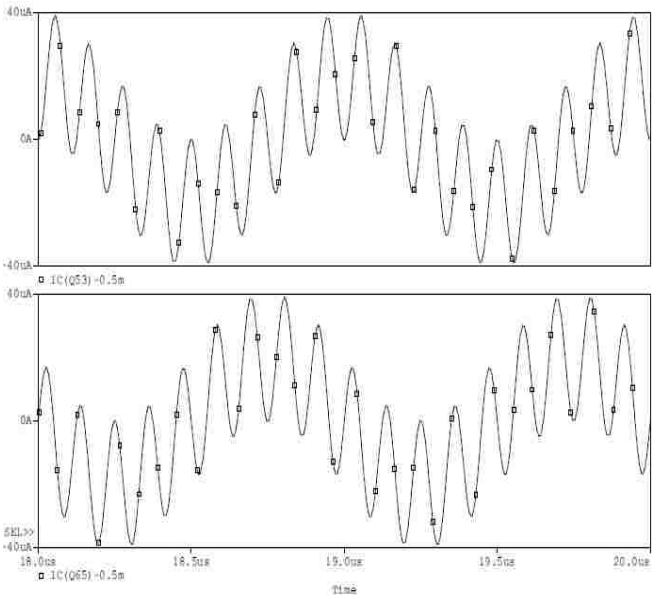
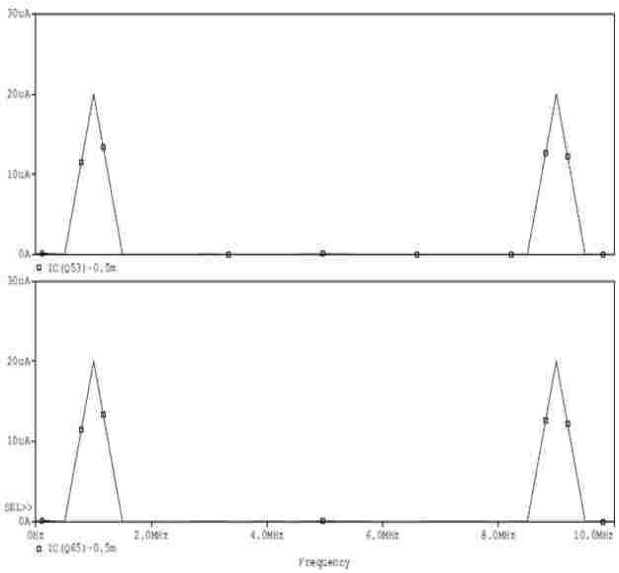


Fig. 10 Schematic of a designed mixer block using variable-transconductance principle

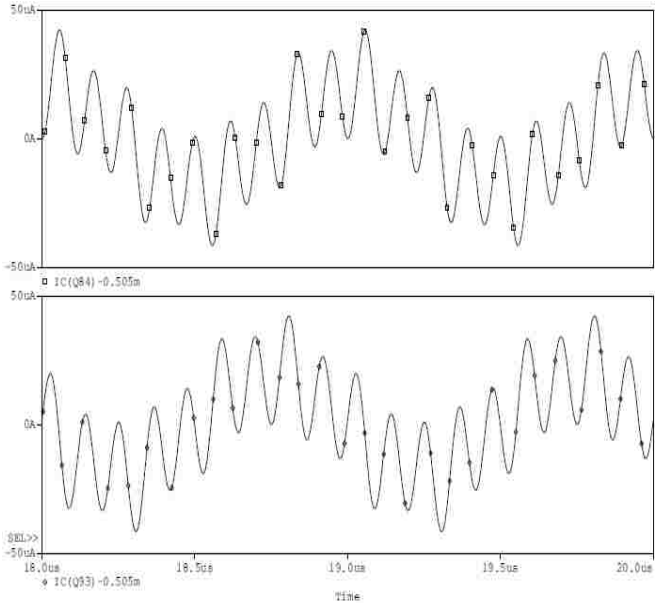
Fig. 11a shows the result of the PSpice simulation on the mixer block proposed in Fig.10 with ideal BJT models, and Fig. 11b shows the result of the simulation with real BJT models. The plots in Fig. 11(a1), (a2) agree quite well with eqn. (42) and eqn. (45). However, the plots in Fig. 11(b1),(b2) display the introduction of an unexpected frequency component of 5MHz with amplitude of 3.938uA, which is brought forth by the difference in the DC offset of the current flowing in Q1 and Q2. In Fig. 11(b2), the amplitude of 1MHz and 9MHz component is 19.162u and the output offset is 0.502mA which has an error of 0.4% compared to the expected 0.5mA.



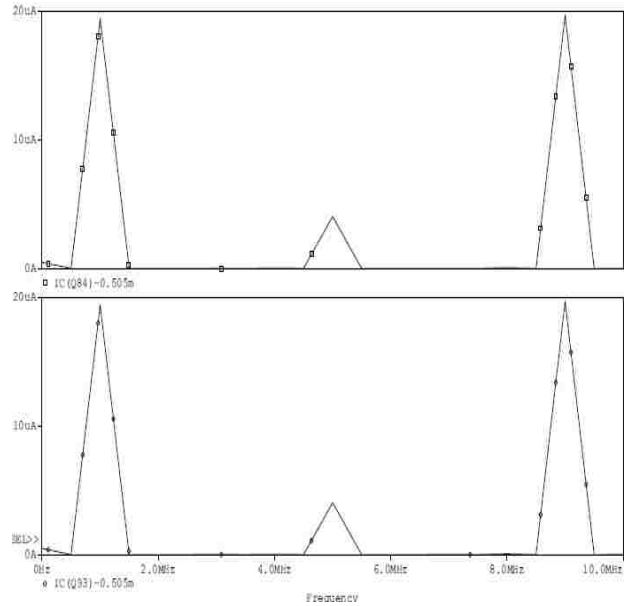
(a1)



(a2)



(b1)



(b2)

Fig. 11

3. Demodulation Block Design

The demodulation block, which is also the back end of the system, consists of a mixer block and a subtractor. The mixer block is very similar to the one discussed in the last chapter. It mixes one of the outputs from the core filter with a sinusoidal signal generated by the local oscillator and the other with another sinusoidal signal. The two sinusoidal signals are identical in amplitude and frequency but 90 degrees apart in phase. The difference of the two mixed signals is achieved with a subsequent subtractor and is the final output of the whole system. Based on the discussion in Chapter 2, the design of the back end block merely requires some modification to the schematic in Fig. 5 or Fig. 10. In this chapter, two designs of the demodulation block are proposed and tested.

3.1 Design with the State-space Synthesis Technique

The design proposed in this section uses the state-space synthesis technique and is very similar to the circuit in Fig.5. As shown in Fig. 12, the blocks in green form an interface between the preceding core filter and the back end stage, providing the input voltages that correspond to Iin1_pos, Iin1_neg, Iin2_pos and Iin2_neg for the demodulation block.

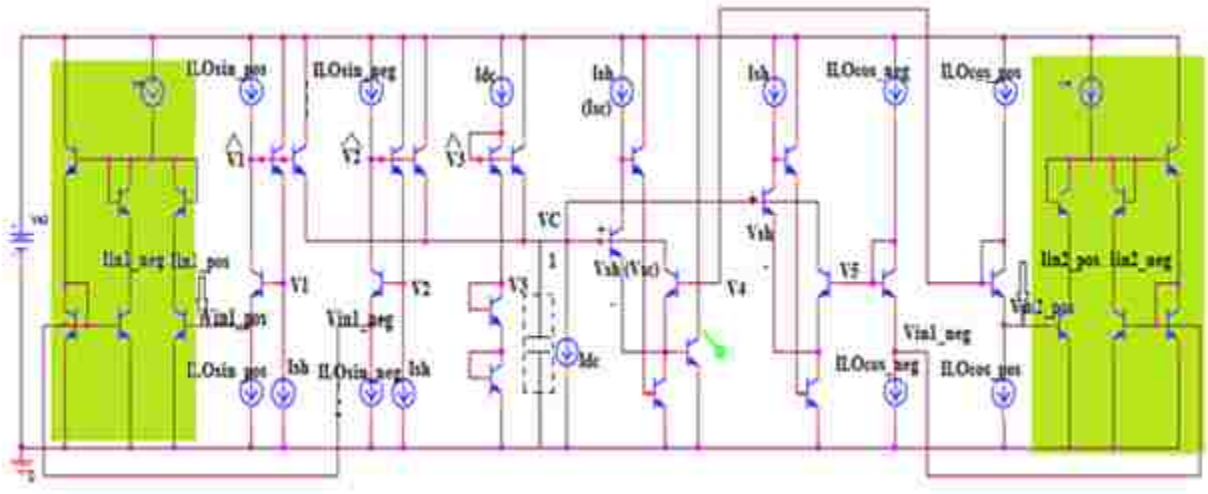


Fig. 12 Schematic of a designed demodulation block using the state-space synthesis technique

Assume: $X = I_s e^{k(VC-Vsc)} \implies \dot{X} = k\dot{V}_c I_s e^{k(Vc-Vsc)}$

$$U_0 = I_s^2 e^{kV1} + I_s^2 e^{kV2} + I_s^2 e^{kV3} - I_s^2 e^{kV4} - I_s^2 e^{kV5}$$

$$= (ILO_{sin} + Ioff)(Iin1 + Ioff) + (-ILO_{sin} + Ioff)(-Iin1 + Ioff) + Ioff^2 -$$

$$(ILO_{cos} + Ioff)(Iin2 + Ioff) — (-ILO_{cos} + Ioff)(-Iin2 + Ioff)$$

$$= 2(ILO\_sin * Iin1 - ILO\_cos * Iin2) + Ioff^2$$

$$Y = X = I_s e^{k(Vc-Vsc)}$$

Suppose there is a capacitor connected between node1 and the ground, then the nodal equation for node 1 could be written as:

$$C\dot{V}c = -I_{dc} + I_s e^{k(\widehat{V1}-Vc)} + I_s e^{k(\widehat{V2}-Vc)} + I_s e^{k(\widehat{V3}-Vc)} - I_s e^{k(V4+Vsh-Vc)} - I_s e^{k(V5+Vsh-Vc)}$$

Multiplying both sides of the above equation by $\frac{1}{CVt} I_s e^{k(Vc-Vsc)}$, we get

$$\dot{X} = -\frac{I_{dc}}{CVt} I_s e^{k(Vc-Vsc)} + \frac{1}{CVt} I_s^2 e^{k(\widehat{V1}-Vsc)} + \frac{1}{CVt} I_s^2 e^{k(\widehat{V2}-Vsc)} + \frac{1}{CVt} I_s^2 e^{k(\widehat{V3}-Vsc)} - \frac{1}{CVt} I_s^2 e^{kV4} - \frac{1}{CVt} I_s^2 e^{kV5}$$

$$= -\frac{I_{dc}}{CV_t} \frac{{I_s}^2 e^{kV_c}}{I_{sc}} + \frac{I_{sh}}{CV_t} \left(\frac{{I_s}^2 e^{kV_1}}{I_{sc}} + \frac{{I_s}^2 e^{kV_2}}{I_{sc}} + \frac{{I_s}^2 e^{kV_3}}{I_{sc}} - \frac{{I_s}^2 e^{kV_4}}{I_{sc}} - \frac{{I_s}^2 e^{kV_5}}{I_{sc}}\right)$$

Set $w_0 = \frac{I_{sh}}{CV_t}$ and $I_{sh} = I_{sc} = I_{off}$,

$$\dot{X} = -w_0 X + w_0 \frac{U_0}{I_{sc}} = -w_0 X + w_0 U \quad \text{where } U = \frac{U_0}{I_{sc}} \tag{49}$$

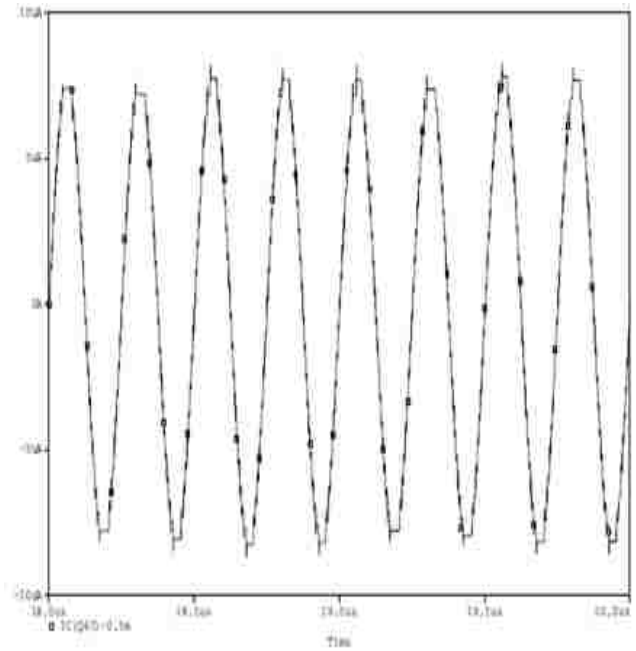
Eqn. 49 indicates that the output of the circuit is a low-pass filtered version of the scaled input. Since the circuit has a stable DC operating point, the voltage change at the ungrounded end of the capacitor is negligible. Therefore, $\dot{X}$ in eqn. (49) is approximately zero. It indicates that the output of the circuit in Fig.12 theoretically equals the scaled input signal. Transient analysis is made with PSpice to test the performance of the demodulation block. According to the system spec, the output signals of the core filter would be $y_1 = (20u)\cos(2\pi * 1MHz * t) + 0.5m$ and $y_2 = (20u)\sin(2\pi * 1MHz * t) + 0.5m$, so two ideal current sources respectively set

to the value of y_1 and y_2 are used as the input for the demodulation block in simulation. Sinusoidal signals generated by the local oscillator and all the DC currents are set to the same value as in the front end mixer block. The PSpice test result for the demodulator proposed in Fig. 12 is shown in Fig. 13. Specifically, Fig. 13 (a1) and (a2) display the result of the simulation with ideal BJT models, and Fig. 13 (b1) and (b2) shows the result of the simulation with real BJT models.

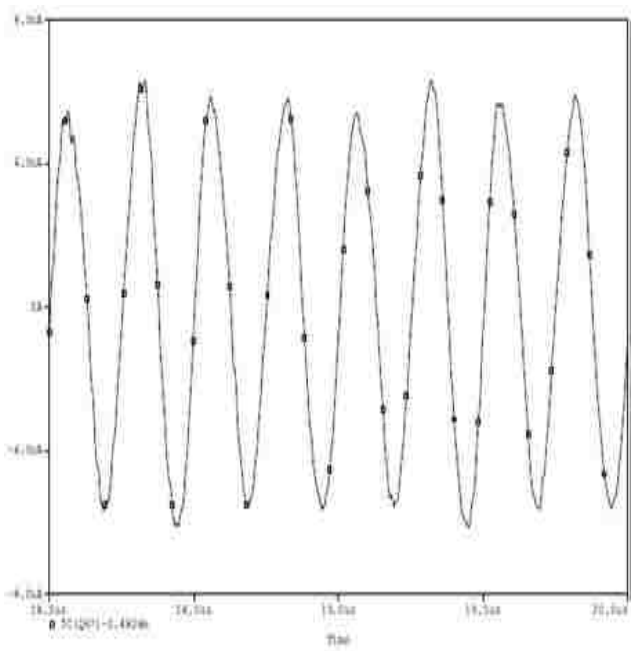
The output of such a block is supposed to be:

$$\begin{aligned} \mathrm{I_{out}} &= \frac{1}{\mathrm{I_{sc}}}[2(\mathrm{ILO_{sin}} * \mathrm{Iin1} - \mathrm{ILO_{cos}} * \mathrm{Iin2}) + \mathrm{Ioff}^2] \\ &= \frac{1}{0.5\mathrm{m}}[2(0.1\mathrm{m})\sin(2\pi * 5\mathrm{MHz} * \mathrm{t}) * (20\mathrm{u})\cos(2\pi * 1\mathrm{MHz} * \mathrm{t}) \\ &\qquad - 2(0.1\mathrm{m})\cos(2\pi * 5\mathrm{MHz} * \mathrm{t}) * (20\mathrm{u})\sin(2\pi * 1\mathrm{MHz} * \mathrm{t}) + (0.5\mathrm{m})^2] \\ &= \frac{(20\mathrm{u})(0.1\mathrm{m})}{0.5\mathrm{m}}[(\sin(2\pi * 6\mathrm{MHz} * \mathrm{t}) + \sin(2\pi * 4\mathrm{MHz} * \mathrm{t}) - \sin(2\pi * 6\mathrm{MHz} * \mathrm{t}) \\ &\qquad + \sin(2\pi * 4\mathrm{MHz} * \mathrm{t})] + (0.5\mathrm{m}) \\ &= (8\mathrm{u})\sin(2\pi * 4\mathrm{MHz} * \mathrm{t}) + 0.5\mathrm{m} \end{aligned} \tag{50}$$

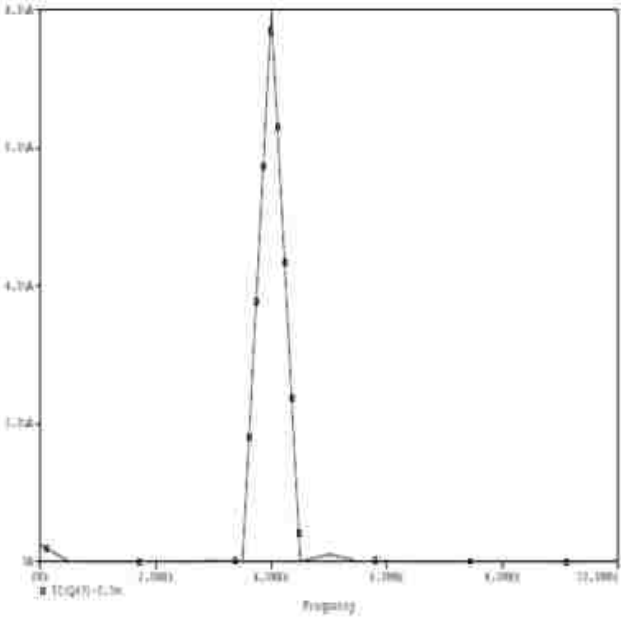
The simulation result of the test using ideal BJT models matches (50) perfectly. For the simulation using real BJT models, the amplitude of 4MHz frequency component is 5.7uA, deviating from the expected 8uA for 28.75%, and the offset of the output current is 0.4826m which has an error of 3.48% compared to 0.5m.



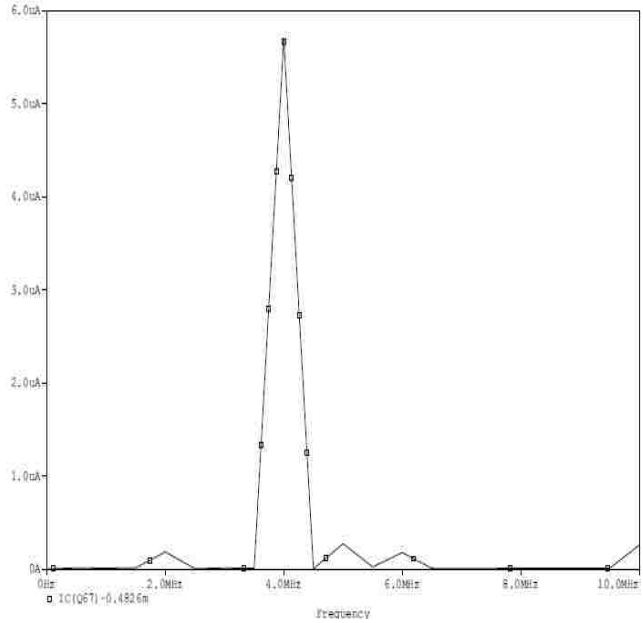
(a1)



(b1)



(a2)



(b2)

Fig. 13

3.2 Design with the Variable-transconductance Principle

Another approach to the demodulator block design is derived from the circuit in Fig.10, as shown in Fig. 14. Similarly, the two blocks in green form the interface between the preceding core filter and back end block, providing $I2 = Iin1\_pos, I1 = Iin1\_neg, I7 = Iin2\_pos, I8 = Iin2\_neg$ as the input signals for the demodulator.

According to the variable-transconductance principle, we have

$$\frac{I_2}{I_1}=\frac{I_3}{I_4} \implies \frac{(I_2-I_1)}{(I_1+I_2)}=\frac{(I_3-I_4)}{(I_3+I_4)} \Rightarrow (I_3-I_4)=(I_2-I_1)\frac{(I_3+I_4)}{(I_1+I_2)}=(I_{in1\_pos}-I_{in1\_neg})\frac{ILOsin\_pos}{2I_{off}}$$

$$\frac{I_2}{I_1}=\frac{I_6}{I_5} \implies \frac{(I_2-I_1)}{(I_1+I_2)}=\frac{(I_6-I_5)}{(I_6+I_5)} \Rightarrow (I_6-I_5)=(I_2-I_1)\frac{(I_6+I_5)}{(I_1+I_2)}=(I_{in1\_pos}-I_{in1\_neg})\frac{ILOsin\_neg}{2I_{off}}$$

$$\frac{I_7}{I_8}=\frac{I_9}{I_{10}} \implies \frac{(I_7-I_8)}{(I_7+I_8)}=\frac{(I_9-I_{10})}{(I_9+I_{10})} \Rightarrow (I_9-I_{10})=(I_7-I_8)\frac{(I_9+I_{10})}{(I_8+I_7)}=(I_{in2\_pos}-I_{in2\_neg})\frac{ILOcos\_pos}{2I_{off}}$$

$$\frac{I_7}{I_8}=\frac{I_{12}}{I_{11}} \Rightarrow \frac{(I_7-I_8)}{(I_8+I_7)}=\frac{(I_{12}-I_{11})}{(I_{12}+I_{11})} \Rightarrow (I_{12}-I_{11})=(I_7-I_8)\frac{(I_{12}+I_{11})}{(I_8+I_7)}=(I_{in2\_pos}-I_{in2\_neg})\frac{ILOcos\_neg}{2I_{off}}$$

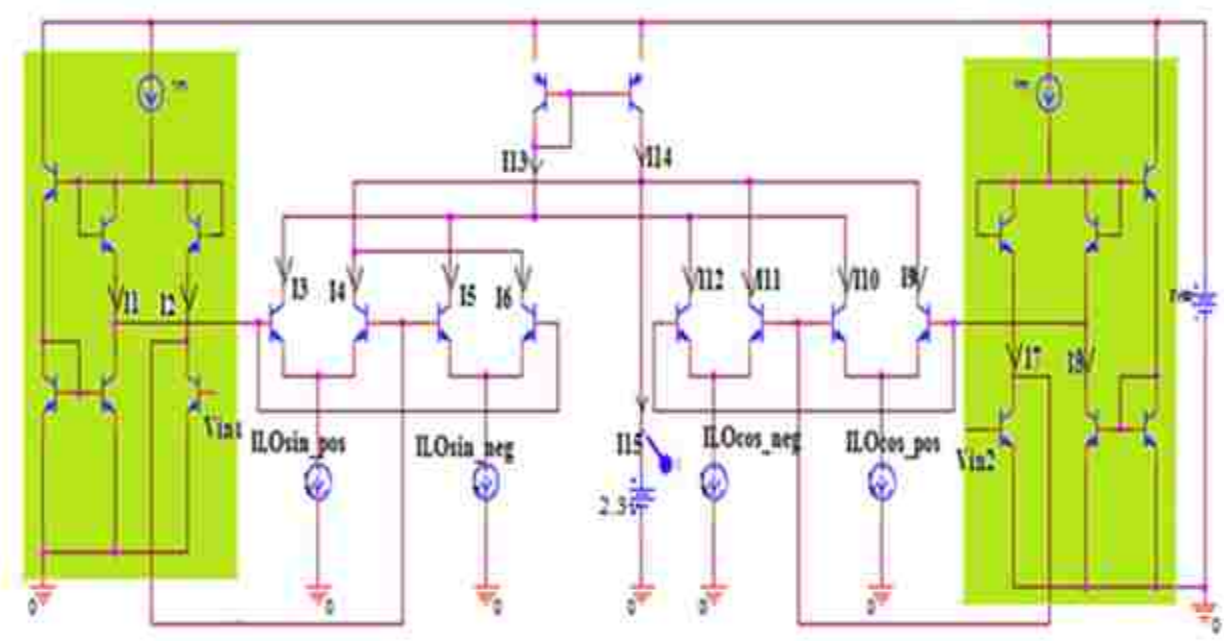


Fig. 14 Schematic of the demodulation block using the variable-transconductance principle

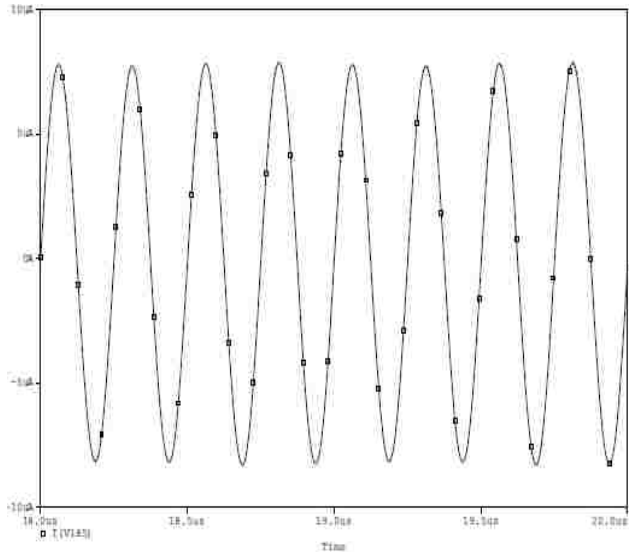
Since the reference current of the current mirror is $I_{13} = I_3 + I_5 + I_{12} + I_{10}$, $I_{14} = I_{13} = I_3 + I_5 + I_{12} + I_{10}$. Therefore, output of the block-i.e. the current flowing in the ideal voltage source-could be written as

$$\begin{aligned} I_{out} &= I_{14} - (I_4 + I_6 + I_{11} + I_9) = (I_3 + I_5 + I_{12} + I_{10}) - (I_4 + I_6 + I_{11} + I_9) \\ &= [(I_3 - I_4) - (I_6 - I_5)] - [(I_9 - I_{10}) - (I_{12} - I_{11})] \\ &= \frac{2}{I_{off}}\left(I_{in1\_pos} - I_{off}\right)(I_{LOsin\_pos} - I_{off}) - \frac{2}{I_{off}}\left(I_{in2\_pos} - I_{off}\right)(I_{LOcos\_pos} - I_{off}) \end{aligned} \quad (51)$$

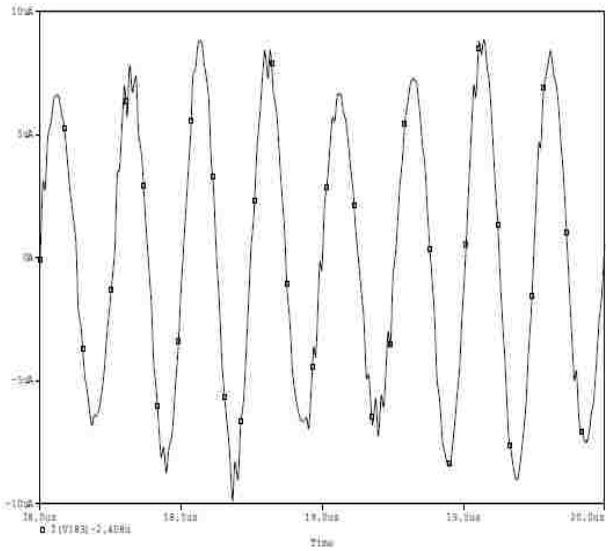
Substitute the specific value into eqn. (51),

$$\begin{aligned} I_{out} &= \frac{2}{0.5m}(20u)\cos(2\pi * 4MHz * t) * (0.1m)\sin(2\pi * 5MHz * t) \\ &\quad - \frac{2}{0.5m}(20u)\sin(2\pi * 4MHz * t) * (0.1m)\cos(2\pi * 5MHz * t) \\ &= (8u)\sin(2\pi * 4meg * t) \end{aligned} \quad (52)$$

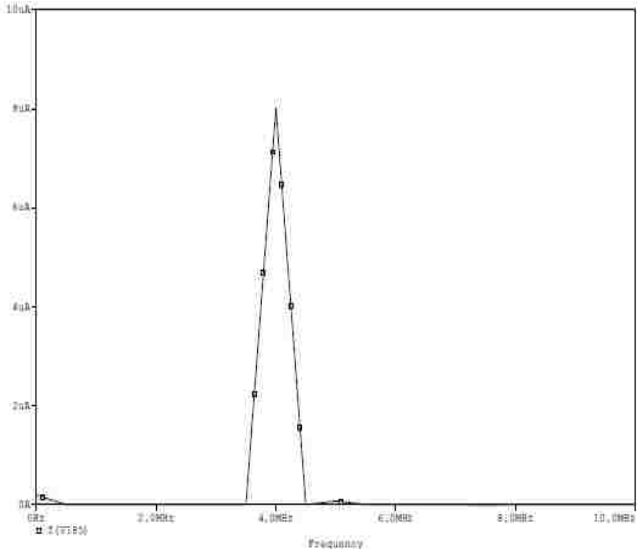
PSpice transient analysis with the ideal BJT models produces an output that agrees quite well with eqn. (52), as shown in Fig. 15 (a1) and (a2). In the test with real BJT models, a "β helper" is added to the current mirror. In order to decrease the influence of Early effect on the output DC offset, the ideal voltage source carrying the output current is set as 1.4V. The FFT frequency spectrum shown in Fig.15 (b2), which shows the result of the test with real BJT models, suggests that the output current has an offset of 2.408uA, and the amplitude of 4MHz is 7.645uA which has an error of -4.438% compared to the expected 8uA. Again, an unexpected frequency component of 5MHz is introduced into the output with amplitude of 1.275uA.



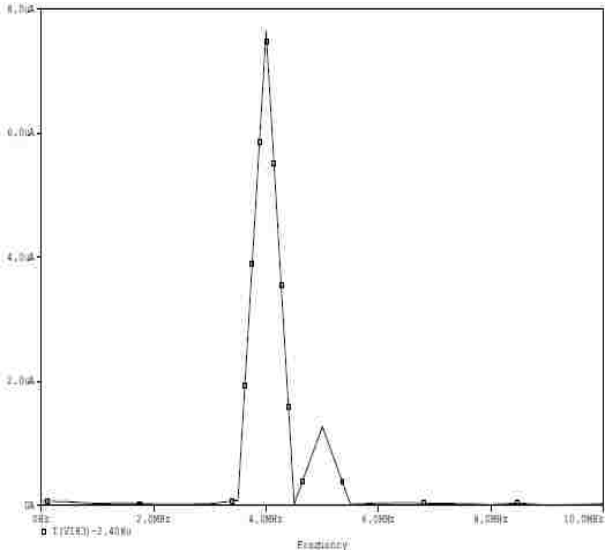
(a1)



(b1)



(a2)



(b2)

4. Complex Filter Block Design

The complex filter proposed in this chapter is a double input double output second-order band pass filter that performs log domain filtering. The filter is electronically tunable both in quality factor Q and center frequency w_0, and has unity gain at the center frequency. The detailed design flow and synthesis procedure is discussed in this chapter. Related parameters are calculated and selected based on the system spec. given at the end of Chapter 1.

4.1 Preliminary Design

4.1.1 Mathematical Model

Assume the state-space description of the complex filter block as:

$$\begin{vmatrix}\dot{x_1}\\ \dot{x_2}\end{vmatrix} = \begin{vmatrix}-\frac{w_0}{2Q} & -w_0\\ w_0 & -\frac{w_0}{2Q}\end{vmatrix}\begin{vmatrix}x_1\\ x_2\end{vmatrix} + \begin{vmatrix}\frac{w_0}{Q} & 0\\ 0 & -\frac{w_0}{Q}\end{vmatrix}\begin{vmatrix}u_1\\ u_2\end{vmatrix} \tag{53a}$$

$$\begin{vmatrix}y_1\\ y_2\end{vmatrix} = \begin{vmatrix}1 & 0\\ 0 & 1\end{vmatrix}\begin{vmatrix}x_1\\ x_2\end{vmatrix} \tag{53b}$$

where u_1 and u_2 are the input variables, x_1 and x_2 are the state variables, and y_1 and y_2 are the output variables.

The transfer functions derived from (53a) and (53b) are given in (54a) to (54b):

$$H_{11}(s) = \frac{y_1}{u_1} = \frac{\left(s+\frac{w_0}{2Q}\right)\left(\frac{w_0}{Q}\right)}{s^2+\frac{w_0}{Q}s+\left(1+\frac{1}{4Q^2}\right)w_0^2} \qquad (u_2 = 0) \tag{54a}$$

$$H_{12}(s) = \frac{y_1}{u_2} = \frac{-w_0\left(\frac{w_0}{Q}\right)}{s^2+\frac{w_0}{Q}s+\left(1+\frac{1}{4Q^2}\right)w_0^2} \qquad (u_1 = 0) \tag{54b}$$

$$H_{21}(s) = \frac{y_2}{u_1} = \frac{-w_0\left(\frac{w_0}{Q}\right)}{s^2+\frac{w_0}{Q}s+\left(1+\frac{1}{4Q^2}\right)w_0^2} \qquad (u_2 = 0) \tag{54c}$$

$$H_{22}(s) = \frac{y_2}{u_2} = \frac{-\left(s+\frac{w_0}{2Q}\right)\left(\frac{w_0}{Q}\right)}{s^2+\frac{w_0}{Q}s+\left(1+\frac{1}{4Q^2}\right)w_0^2} \qquad (u_1 = 0) \tag{54d}$$

To understand the function of this block, typically an AC signal is fed to only one of the input terminals and the other terminal is treated as a "dummy" input driven by a positive DC signal. For example, when u_1 is connected to the input signal, u_2 should be connected to a positive DC signal. In this case, y_1 would represent a band-pass filtered u_1 as expressed in (54a) and $y_2$would represent a low-pass filtered u_1 as suggested in (54c). Similarly, when driving the filter with u_2, the band-pass filtered version and low-pass filtered version of the input at y_2 and y_1 can be obtained respectively. The denominator of the transfer functions above suggests that the two poles of the filter are $p_{1,2} = -\frac{w_0}{2Q} \pm jw_0$. Although the transfer functions given by (54a) and (54d) are not in the standard form for a second-order band pass filter, the center frequency of the band pass filter could be estimated to as $w_{0\_est} = w_0\sqrt{1+\frac{1}{4Q^2}}$. Applying Taylor expansion to the function of w_{0_est} gives the expression $w_{0\_est} = w_0(1+\frac{1}{8Q^2})$ when Q is large. The error between w_{0_est} and w_0 is $12.5(\frac{1}{Q^2})\%$, and a high Q would minimize the error. On the other hand, the magnitude of the two band-pass filtering transfer functions-i.e., (54a) and (54d)-at $s = jw_0$ is $|H_{BP}| = 2\sqrt{\frac{1+4Q^2}{1+16Q^2}}$; therefore, higher Q makes $|H_{BP}|$ closer to unity.

4.1.2 Implementation Procedure

The synthesis procedure starts from making physically meaningful definitions for the state variables. Based on the technique and topology proposed in [15], x_1 and x_2 are defined as the scaled current products that could be implemented with the circuit block in Fig. 2(b). Specifically, V_i is connected to some voltage of two-diode drop that corresponds to the unscaled current product, and I_{aij} is replaced with a DC current source to scale the current product. Since x_1 and x_2 are exponential functions of the voltage across the corresponding one-end-grounded

capacitor, the voltage across each capacitor should be two-diode drop. This indicates that there are definitely some nodes in the circuit connected to the voltage of three-diode drop. The schematic sketch of the filter is proposed in Fig. 12. Large signal analysis is then made by formulating two nodal equations-e.g., (55a) and (55b)-that describe the current in each capacitor.

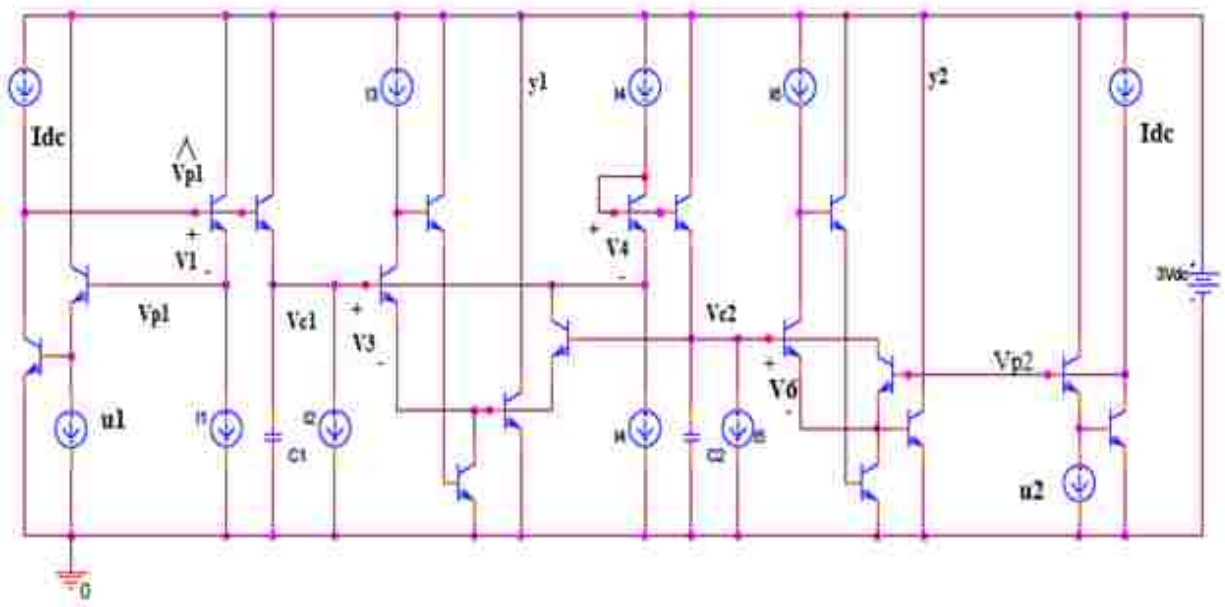


Fig. 16 Schematic sketch for the complex filter

In figure 16 the nodal equations are given by

$$C\dot{V}_{c1} = -I_2 - I_s \exp[(V_{c2} + V_3 - V_{c1})/V_t] + I_s \exp[(V_{p1} + V_1 - V_{c1})/V_t] \quad (55a)$$

$$C\dot{V}_{c2} = I_s \exp[(V_{c1} + V_4 - V_{c2})/V_t] - I_5 - I_s \exp[(V_{p2} + V_6 - V_{c2})/V_t] \quad (55b)$$

Assume: 1. u_1 and u_2 are the two input currents with DC offset Ioff

2. $x_1 = y_1 = I_s \exp[(V_{c1} - V_3)/V_t]$ and $x_2 = y_2 = I_s \exp[(V_{c2} - V6)/V_t]$

3. $I_3 = I_6 = I_{sc} = I_{dc} = I_{off} = I =$ constant DC current

4. $C_1 = C_2 = C$

Note that $\dot{x_1} = (\frac{x_1}{V_t})\dot{V_{c1}}$ and $\dot{x_2} = (\frac{x_2}{V_t})\dot{V_{c2}}$, by multiplying both sides of (55a) and (55b) by $x_1/(CV_t)$ and $x_2/(CV_t)$ respectively, the left hand side of (55a) and (55b) is transformed to $\dot{x_1}$and $\dot{x_2}$.

Specifically, the two nodal equations could now be rewritten as:

$$\dot{x_1} = -\frac{I_2}{CV_t}x_1 - \left(\frac{I_6}{CV_t}\right)x_2 + \frac{I_1}{CV_t}u_1 \tag{56a}$$

$$\dot{x_2} = +\left(\frac{I_4}{CV_t}\right)x_1 - \frac{I_5}{CV_t}x_2 - \frac{I_{dc}}{CV_t}u_2 \tag{56b}$$

In matrix form,

$$\begin{vmatrix}\dot{x_1}\\ \dot{x_2}\end{vmatrix} = \begin{vmatrix}-\frac{I_2}{CV_t} & -\frac{I_6}{CV_t}\\ \frac{I_4}{CV_t} & -\frac{I_5}{CV_t}\end{vmatrix}\begin{vmatrix}x_1\\ x_2\end{vmatrix} + \begin{vmatrix}\frac{I_1}{CV_t} & 0\\ 0 & -\frac{I_{dc}}{CV_t}\end{vmatrix}\begin{vmatrix}u_1\\ u_2\end{vmatrix} \tag{56c}$$

In order for (56c) to be equivalent to (53a), each corresponding entity must be equalized:

$$\frac{w_0}{2Q} = \frac{I_2}{CV_t} = \frac{I_5}{CV_t} \implies I_2 = I_5 = \frac{CV_t w_0}{2Q} \tag{57a}$$

$$w_0 = \frac{I_6}{CV_t} = \frac{I_4}{CV_t} \implies I_4 = I_6 = CV_t w_0 = I \tag{57b}$$

$$\frac{w_0}{Q} = \frac{I_1}{CV_t} = \frac{I_{dc}}{CV_t} \implies I_1 = I_{dc} = \frac{CV_t w_0}{Q} = \frac{I}{Q} \tag{57c}$$

It is easy to note that (57b) and (57c) could not simultaneously hold when Q≠1. The reason for this defect is that I_6 is used in both input level shifting and output scaling for the input variable u_2. A simple solution is to add in another set of circuit block in Fig. 2(b) so that the input level shifting and the output scaling for u_2 would depend on different current source. The modified schematic is shown in Fig. 13. Based on the assumption made on page 39, the state-space description for the new circuit could be obtained by making slight modifications to eqn. (56). The nodal equation for the left capacitor remains the same as eqn. (55a), but that for the right capacitor is now reformulated as

$$\dot{CV_{c2}} = \quad I_s \exp[(V_{c1} + V_4 - V_{c2})/V_t] - I_5 - I_s \exp[(V_{p2} + V_7 - V_{c2})/V_t] \tag{58}$$

Multiplying both sides of (58) by $x_2/(CV_t)$, i.e., $I_s \exp[(V_{c2} - V6)/V_t]/(CV_t)$,

$$\dot{x_2} = +\left(\frac{I_4}{CV_t}\right) x_1 - \frac{I_5}{CV_t} x_2 - \frac{I_7}{CV_t} u_2 \tag{59}$$

Substitute (59) back into (56c) gives

$$\begin{vmatrix} \dot{x_1} \\ \dot{x_2} \end{vmatrix} = \begin{vmatrix} -\frac{I_2}{CV_t} & -\frac{I_6}{CV_t} \\ \frac{I_4}{CV_t} & -\frac{I_5}{CV_t} \end{vmatrix} \begin{vmatrix} x_1 \\ x_2 \end{vmatrix} + \begin{vmatrix} \frac{I_1}{CV_t} & 0 \\ 0 & -\frac{I_7}{CV_t} \end{vmatrix} \begin{vmatrix} u_1 \\ u_2 \end{vmatrix} \tag{60}$$

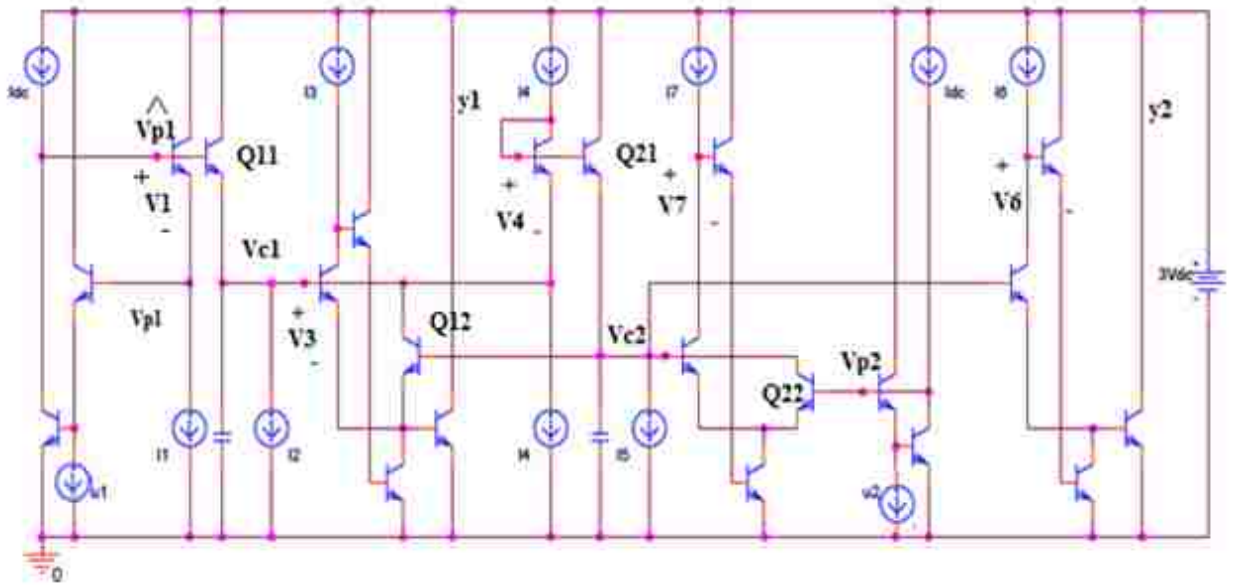


Fig. 17 Modified schematic sketch for the complex filter

To match (60) with (53a), set:

$$\frac{w_0}{2Q} = \frac{I_2}{CV_t} = \frac{I_5}{CV_t} \implies I_2 = I_5 = \frac{CV_t w_0}{2Q} = \frac{I}{2Q} \tag{61a}$$

$$w_0 = \frac{I_6}{CV_t} = \frac{I_4}{CV_t} \implies I_4 = I_6 = CV_t w_0 = I \tag{61b}$$

$$\frac{w_0}{Q} = \frac{I_1}{CV_t} = \frac{I_7}{CV_t} \implies I_1 = I_7 = \frac{CV_t w_0}{Q} = \frac{I}{Q} \tag{61c}$$

Correlate (61a), (61b) and (61c) with the assumption on page 34 and the system spec, a summary on the value for each component in Fig. 17 is listed below:

1. $I_4 = I_6 = I_3 = I_{sc} = I_{dc} = I = CV_t w_0 = 0.5\text{m}$; $I_2 = I_5 = \frac{CV_t w_0}{2Q} = \frac{0.25\text{m}}{Q}$; $I_1 = I_7 = \frac{0.5\text{m}}{Q}$.

2. $C = \frac{0.5\text{m}}{V_T w_0} \approx \frac{0.5\text{m}}{25.8\text{m}*2\pi*1\text{meg}} = 3.084\text{nF}$.

Consider the error of $12.5(\frac{1}{Q^2})\%$ for w_0, the value of C needs slight adjustment during the simulation in order to obtain the center frequency of 1MHz.

According to the large signal analysis, the design in Fig. 13 completes the implementation of the complex filter block. However, another important issue to consider is that whether the circuit has DC equilibrium. To clarify this point, DC analysis to the circuit will be discussed in the following section.

4.2 Small-signal Analysis and Design Modification

4.2.1 Gm-C counterpart and AC analysis

For convenience in AC analysis, another perspective of the circuit shown in Fig. 17 is developed at block level by introducing the Gm-C equivalent circuit. Note that the circuit blocks in Fig. 2(a) and Fig. 2(b) could virtually be modeled as transconductance amplifiers with positive and negative g_m, respectively. The positive transconductance pushes current into the output terminal of the amplifier while the negative one pulls current from the output terminal. The transconductance equals the inverse of the dynamic resistance of certain forward biased b-e junction in the block, value wise. The dynamic resistance could be expressed as $r_d = \frac{v_T}{I_d}$, where v_T is the thermal voltage and I_d is the current flowing in the junction at some DC operating point. Based on this concept, the Gm-C counterpart of the circuit in Fig. 17 is shown in Fig. 14. For convenience in the following AC analysis, several simplifications are applied to the circuit:

1. Each input of the filter is denoted by a voltage of two-diode drop corresponding to the product of the input current $u_1(u_2)$ and the DC current I_{dc}.

2. Output blocks are removed.

3. Blocks for the voltage level shift in Fig. 13 are replaced by ideal DC voltage sources.

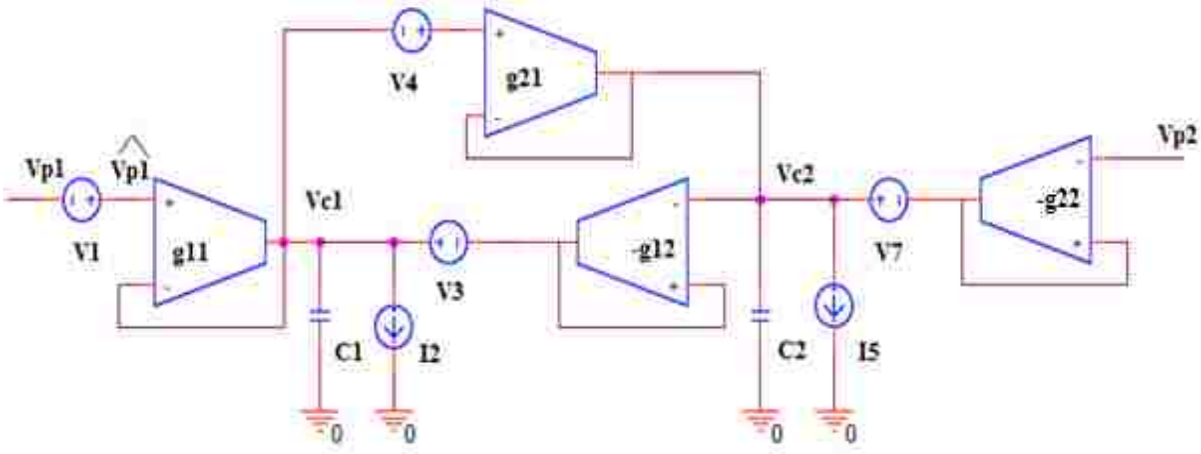


Fig. 18 Gm-C counterpart of the design in Fig. 17

The transconductance of each amplifier in Fig. 18 equals the reciprocal of the dynamic resistance of the related transistor in Fig. 17; therefore, $g_{11} = \frac{1}{r_{d\_Q11}} = \frac{I_{d\_Q11}}{V_T}$, $g_{21} = \frac{1}{r_{d\_Q21}} = \frac{I_{d\_Q21}}{V_T}$, $-g_{12} = \frac{-1}{r_{d\_Q12}} = -\frac{I_{d\_Q12}}{V_T}$, $-g_{22} = \frac{-1}{r_{d\_Q22}} = \frac{I_{d\_Q22}}{V_T}$, where each current term represents the current flowing in the junction at some DC operating point. Based on the equivalent circuit shown in Fig. 18, AC analysis could be made with great convenience. Specifically, short all the DC voltage sources and open all the DC current sources, then write nodal equations for the two capacitors with the labeled parameters. By inspecting the current condition at node1 and node2, the nodal equations could be formulated as:

$$\begin{vmatrix} \dot{V}_{C1} \\ \dot{V}_{C2} \end{vmatrix} = \begin{vmatrix} -(g_{11}-g_{12})/C & -g_{12}/C \\ g_{21}/C & -(g_{21}-g_{22})/C \end{vmatrix} \begin{vmatrix} V_{C1} \\ V_{C2} \end{vmatrix} + \begin{vmatrix} g_{11}/C & 0 \\ 0 & -g_{22}/C \end{vmatrix} \begin{vmatrix} V_{p1} \\ V_{p2} \end{vmatrix} \qquad (62)$$

where V_{p1} and V_{p2} are the voltage variables that are natural logarithm of the corresponding input current product, and both are of two-diode drop. Note that eqn. (62) has the same form as (53a); it provides a necessary condition for the circuit to perform as expectation.

Another appealing feature of the Gm-C filter in Fig. 18 is that each amplifier has its inverse or non-inverse input terminal directly connected to the output terminal, rather than to the ground as is the case in many other Gm-C filters. Such a feature is exclusive to the Gm-C counterpart of a log-domain filter, which greatly facilitates the AC analysis. The equivalent circuit where either input terminal of each transconductance amplifier is grounded is shown in Fig. 19 to provide another perspective of the circuit in Fig. 18.

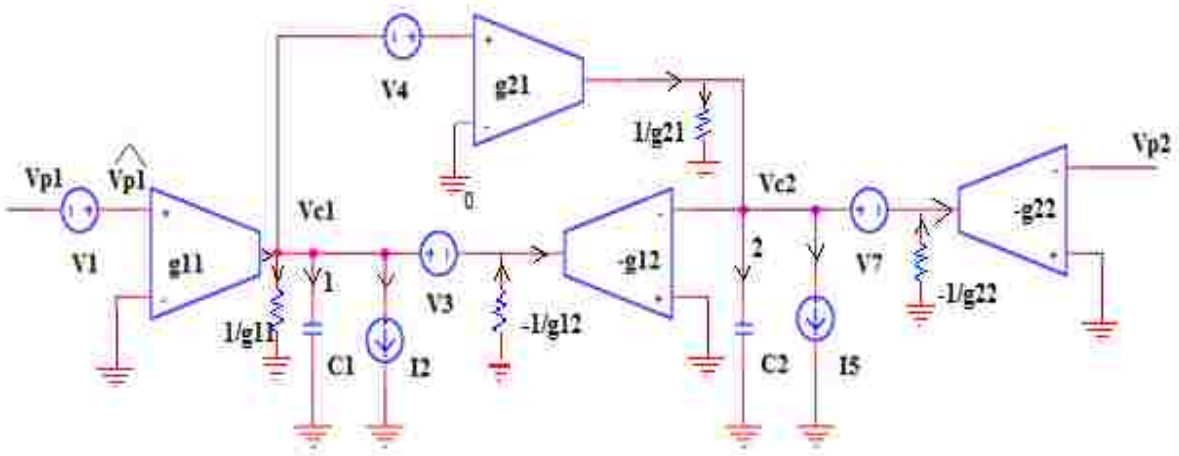


Fig. 19 The equivalent circuit of Fig. 18 where either input terminal of each transconductance amplifier is grounded

4.2.2 DC analysis and Circuit Modification

Eqn. (62) alone is not sufficient to guarantee the performance of the circuit in Fig. 17. The other indispensable piece for a reliable design is to realize DC equilibrium and find for the circuit a proper DC operating point, which will be discussed in the following section.

In DC analysis, AC signal is assumed to be nonexistent in the circuit. Specifically, two capacitors will behave like open circuit and the AC component in V_{p1} and V_{p2} is replaced by DC component. For simplicity, V_{p1} and V_{p2} are connected to the voltage of two diode drops corresponding to I_{dc}^2, i.e.,$2V_t \ln\left(\frac{I_{dc}}{I_s}\right)$. Again, the nodal equations are derived based on Fig. 18

for node1 and node2, where the left hand side represents the current(s) flowing into the node and the right hand side represents the currents(s) flowing out of the node:

$$(V_{p1} + V_1 - V_{c1})g_{11} = I_2 + (V_{c2} + V_3 - V_{c1})g_{12} \quad (63a)$$

$$(V_{c1} + V_4 - V_{c2})g_{21} = I_5 + (V_{p2} + V_7 - V_{c2})g_{22} \quad (63b)$$

For a proper DC operating point, it is desired that both V_{c1} and V_{c2} are two-diode drop and are independent on Q. To check out whether the circuit meets such criteria, (63a) and (63b) are solved for V_{c1} and V_{c2}. Assume

$$V_{c1} = 2V_t \ln\left(\frac{I}{I_s}\right) + V_{x1},\ V_{c2} = 2V_t \ln\left(\frac{I}{I_s}\right) + V_{x2}$$

$$V_{x1} = V_T \ln x_1, \qquad V_{x2} = V_T \ln x_2$$

According to eqn. (61a)-(61c) and the schematic in Fig. 13, (63a) and (63b) are simplified as

$$\frac{I}{x_1 Q} = \frac{I}{2Q} + \left(\frac{x_2}{x_1}\right)I \quad (64a)$$

$$\left(\frac{x_1}{x_2}\right)I = \frac{I}{2Q} + \frac{I}{x_2 Q} \quad (64b)$$

Solve for x_1 and x_2 in (64a) and (64b),

$$x_1 = \frac{2(2Q+1)}{4Q^2+1},\quad x_2 = \frac{2(2Q-1)}{4Q^2+1} \quad \Longrightarrow \quad V_{x1} = V_t \ln\frac{2(2Q+1)}{4Q^2+1},\ V_{x2} = V_t \ln\frac{2(2Q-1)}{4Q^2+1}$$

Note that both V_{x1} and V_{x2} are functions of Q; therefore, the circuit does not have a stable DC operating point and it needs further modification.

The modification procedure involves: First, force the circuit in Fig.13 to be in DC equilibrium by assuming $V_{c1} = V_{c2} = V_{p1} = V_{p2} = 2V_t \ln\left(\frac{I}{I_s}\right)$ in DC analysis. Second, list the nodal equations and identify extra terms that are needed to hold the equations true. Third, synthesize the extra terms and add the blocks to the schematic in Fig. 17.

Nodal equation set for the circuit in Fig. 17 under the assumed DC equilibrium can be written as:

$$I_1 = I_2 + I_3 \iff \frac{I}{Q} = \frac{I}{2Q} + I \tag{65a}$$

$$I_4 = I_5 + I_7 \iff I = \frac{I}{2Q} + \frac{I}{Q} = \frac{3I}{2Q} \tag{65b}$$

One of the most straightforward methods to hold the above equations true is:

1. Add $\left(1 - \frac{1}{2Q}\right)$ I to the left hand side of (65a).

2. Add $\frac{3I}{2Q}$, I to the left hand side and the right hand side of (65b) respectively.

To maintain the voltage level of two diode drops at both nodes, the implementation of the new terms must to obey the following rules: 1. For a block that pushes current into any node, the base voltage of the output transistor should be three-diode drop and the emitter should be connected to the corresponding node. 2. For a block that pulls current out of a node, the base voltage of the output transistor is two-diode drop and the collector should be connected to the corresponding node.

The modified circuit is shown in Fig. 20, where there are three added blocks that provide the needed DC currents with proper voltage level to force the DC equilibrium of the circuit. The Gm-C counterpart is shown in Fig. 21, where each colored block corresponds to the block with same color in the circuit in Fig. 20. The value of each component in Fig. 21 is given below:

$$V_1 = V_7 = V_t \mathrm{In}\left(\frac{I/Q}{I_s}\right), V_3 = V_4 = V_t \mathrm{In}\left(\frac{I}{I_s}\right), V_{dc1} = V_t \mathrm{In}\left(\frac{(1-1/2Q)I}{I_s}\right), V_{dc2} = V_t \mathrm{In}\left(\frac{3I/2Q}{I_s}\right)$$

$$V_{dc3} = V_t \mathrm{In}\left(\frac{I}{I_s}\right),\ 2V\_I = 2V_t \mathrm{In}\left(\frac{I}{I_s}\right)$$

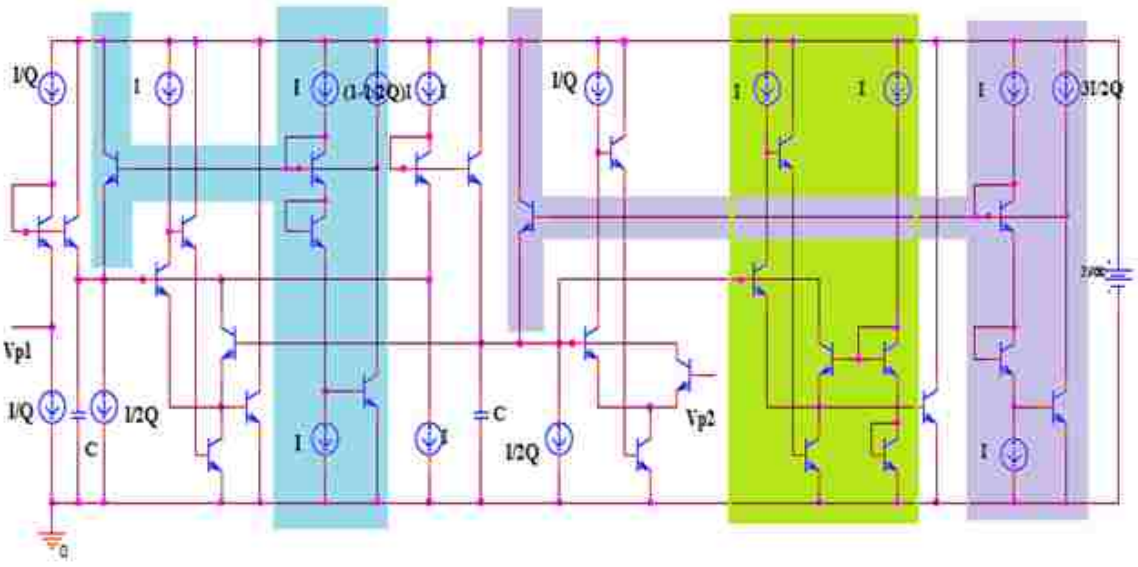


Fig. 20 Modified schematic version of the circuit in Fig. 17

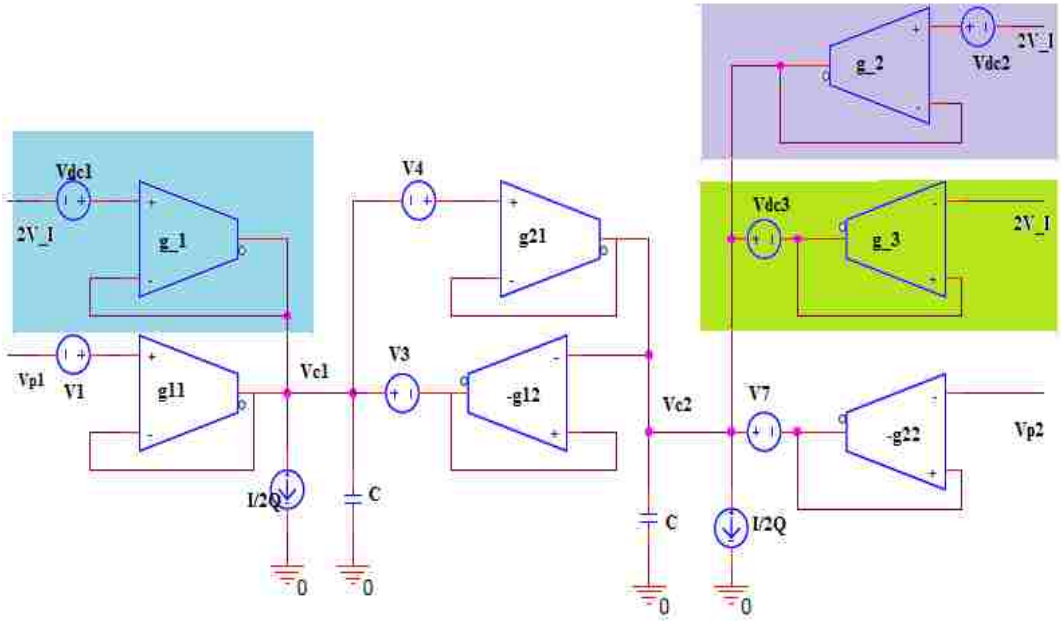


Fig. 21 Gm-C counterpart of the circuit in Fig. 20

4.4 Design Test I

In this section, AC analysis and DC analysis are made to testify whether the modified circuit shown in Fig. 20 has obtained both necessary condition and sufficient condition to perform as expectation. Then, AC test is run in PSpice to show the Bode plots and relevant measurement result of the circuit.

Since the added blocks only introduce DC signals into the old circuit, the AC analysis to the circuit in Fig. 20 would achieve an equation identical to eqn. (62). In DC analysis, assume $V_{P1} = V_{P2} = 2V_t \ln\left(\frac{I}{I_s}\right)$ and both capacitors are open circuit. Two nodal equations describing the currents in the capacitors in Fig. 21 are formulated as:

$$(V_{P1} + V_1 - V_{c1})g_{11} + (2V\_I + V_{dc1} - V_{c1})g_1 = \frac{I}{2Q} + (V_{c2} + V_3 - V_{c1})g_{12} \tag{66a}$$

$$(V_{c1} + V_4 - V_{c2})g_{21} + (2V\_I + V_{dc2} - V_{c2})g\_2 = \frac{I}{2Q} + (V_{P2} + V_7 - V_{c2})g_{22} + (2V\_I + V_{dc3} - V_{c2})g\_3 \tag{66b}$$

To solve the nodal equation set of (66a) and (66b) for V_{c1} and V_{c2}, assume

$$V_{c1} = 2V_t \ln\left(\frac{I}{I_s}\right) + V_{x1},\ V_{c2} = 2V_t \ln\left(\frac{I}{I_s}\right) + V_{x2}$$

$$V_{x1} = V_t \ln x_1,\ V_{x2} = V_t \ln x_2$$

Similarly, (66a) and (66b) are simplified as

$$\frac{I/Q}{x_1} + \frac{(1-1/2Q)I}{x_1} = \frac{I}{2Q} + \frac{x_2}{x_1} I \tag{67a}$$

$$\frac{x_1}{x_2} I + \frac{3I}{2x_2 Q} = \frac{I}{2Q} + \frac{I/Q}{x_2} + \frac{I}{x_2} \tag{67b}$$

Solve eqn. (67a) and (67b),

$$x_1 = x_2 = 1 \Longrightarrow V_{c1} = V_{c2} = 2V_t \ln\left(\frac{I}{I_s}\right) \tag{68}$$

The result mathematically proves that the circuit in Fig. 20 has a stable DC operating point independent on Q. Eqn. (62) and eqn. (68) together establish the necessary and sufficient

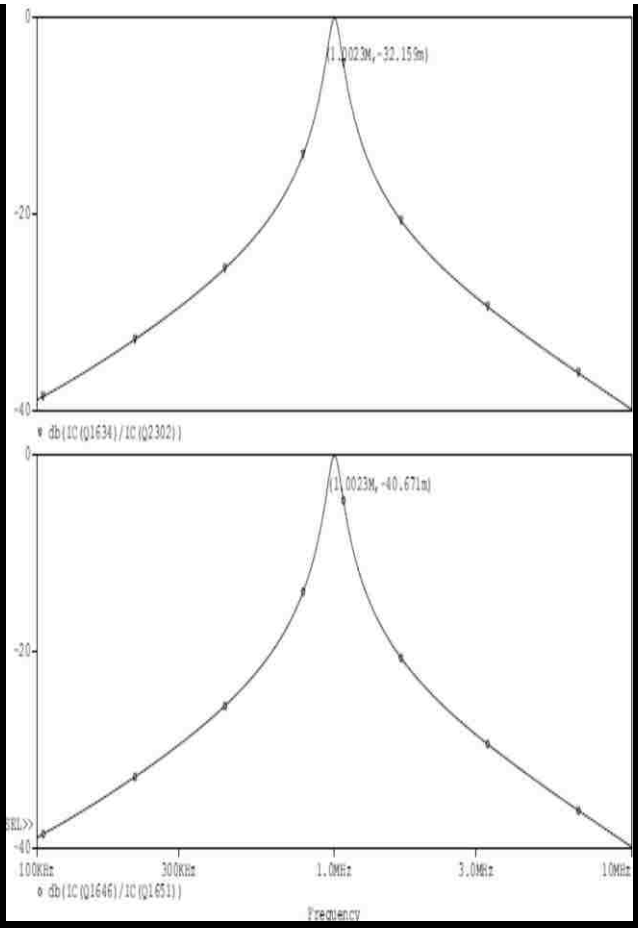
condition for the circuit in Fig. 20 to implement the state-space description given in (53a) and (53b) with reliability. Therefore, the circuit could be a candidate for the complex filter block design.

To test the performance of the circuit, AC analysis is made by PSpice simulation. The simulation contains two parts: single-ended AC test and double-ended AC test. In the single-ended test, only one input terminal is connected to an offset AC current, while the other is driven by some DC current at a proper voltage level. In the double-ended test, both input terminals are simultaneously connected to the offset AC signals. The right input signal (corresponding to V_{p2} in Fig. 20) should lead the left input signal (corresponding to V_{p1} in Fig. 20) 90 degrees in phase, and they are identical in amplitude and frequency. This setting models the output generated by the front end mixer block as discussed in Chapter 2.

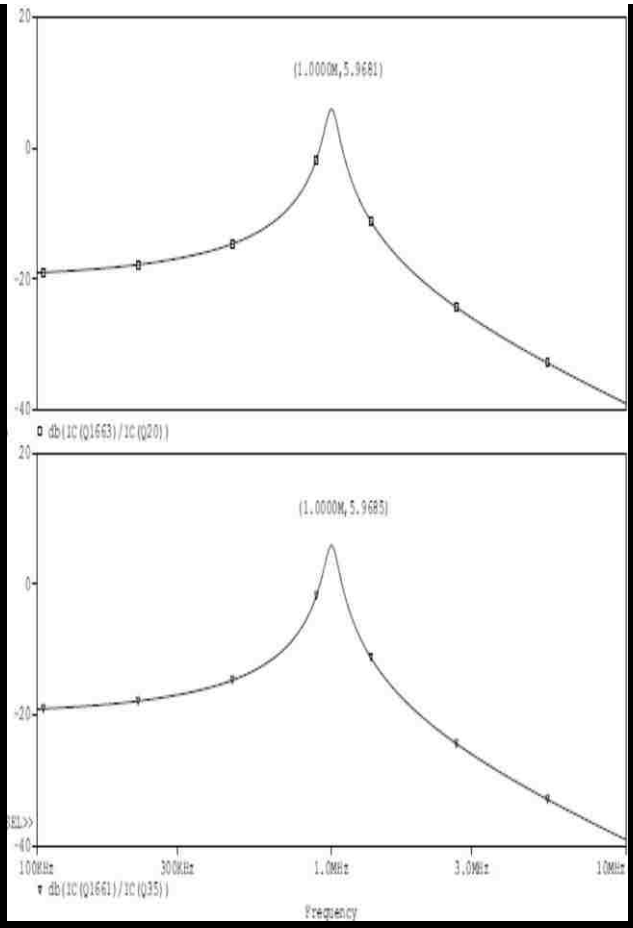
Set $Q = 10$ and $I = 0.5\text{m}$, so $I/Q = 0.05\text{m}, \frac{I}{2Q} = 0.025\text{m}, \left(1 - \frac{1}{2Q}\right) I = 0.475\text{m}, \frac{3I}{2Q} = 0.075\text{m}$. The filter is expected to have a center frequency that equals the frequency difference between the system input signal and the signal generated by the local oscillator, e.g., 1MHz. Therefore, $C = \frac{I}{2\pi f_c V_t} = 3.084\text{nF}$. In the simulation, ideal NPN model and ideal current or voltage sources are used. According to the test result, C is adjusted to 3.075nF to move f_c closer to 1MHz.

Simulation result is given in Fig.22. For both tests, the upper plot represents the left output and the bottom one represents the right output. The measured f_c and Q agree quite well with expectation. Bode plots in the same column are almost identical, indicating that two inputs of the circuit are band-pass filtered with good balance. In the single-ended test, unity gain is achieved at center frequency, while in the double-ended test the gain at the center frequency is around 6dB due to AC signal superposition. Moreover, the plots from the single-ended test

display better low frequency suppression and overall symmetry than that from the double-ended test.



Evaluate	Measurement	Value
☑	Q_Bandpass(db(IC(Q1634)/IC(Q230...	9.986
☑	Q_Bandpass(db(IC(Q1646)/IC(Q165...	9.986



Evaluate	Measurement	Value
☑	Q_Bandpass(db(IC(Q1663)/IC(Q20)),3)	9.962
☑	Q_Bandpass(db(IC(Q1661)/IC(Q35)),3)	9.963

Fig. 22

4.5 Design Improvement

The PSpice simulation has testified the band-pass filtering function of the circuit in Fig. 20. Defects of the design lies in the lack of symmetry in topology, complicated tuning process, and non-unity gain at the center frequency in the double-ended AC test. This section discusses a solution to the defects.

4.5.1 Topology Symmetry Improvement

Inspect Fig. 20 or Fig. 21, there are altogether three added blocks that help force the DC equilibrium of the circuit. Specifically, there is one block injecting certain amount of DC current into the left capacitor and there are two other blocks respectively pushing and pulling current at the ungrounded end of the right capacitor. If such a circuit could be truncated so that only one block is attached to the right side capacitor, the topology would be more symmetric. Recall eqn. (65b), in DC analysis on the circuit in Fig. 17, the current flowing into and out of node 2 is I and $\frac{3I}{2Q}$ respectively. Among the current leaving node 2, $\frac{I}{Q}$ is provided by the right input signal and $\frac{I}{2Q}$ is provided by the added block. If the right side input block is modified to reverse the direction of the current of $\frac{I}{Q}$, then the total amount of the current flowing into the right side capacitor becomes $(1+\frac{1}{Q})I$ and that of the current flowing in the opposite direction becomes $\frac{I}{2Q}$. In this case, only one block that sucks the current amount of $\left(1+\frac{1}{2Q}\right)I$ from the right side capacitor is needed.

Fig. 23 shows a truncated schematic for the filter block. Note that the phase of the right input signal has been shifted with 180 degrees due to the modification to the right side input block. To maintain the sign of the output that corresponds to the right input signal, a 180-degree phase shift should be applied to the AC component of the right input. Moreover, a block that

performs proper scaling is added in, which is the right most block with the current source I, to keep the amplitude of the output signal correct. The Gm-C counterpart for the new design is shown in Fig. 24, which is much simpler and more symmetric in topology compared to the circuit in Fig.21.

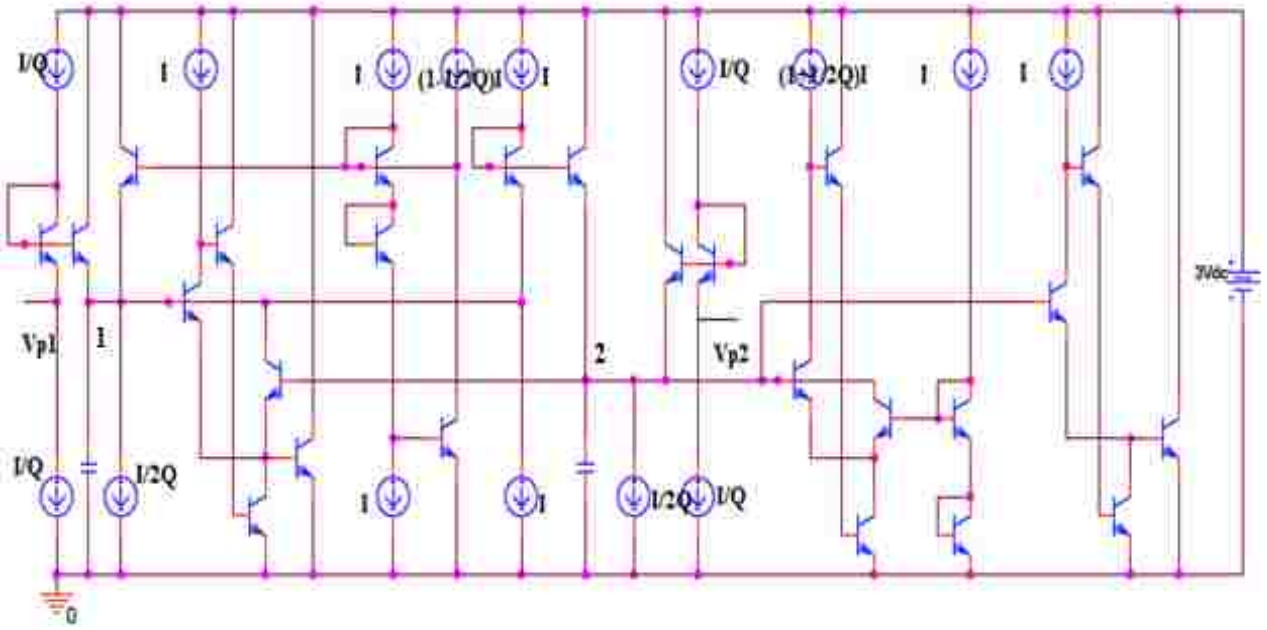


Fig. 23 Truncated version of the circuit in Fig. 20

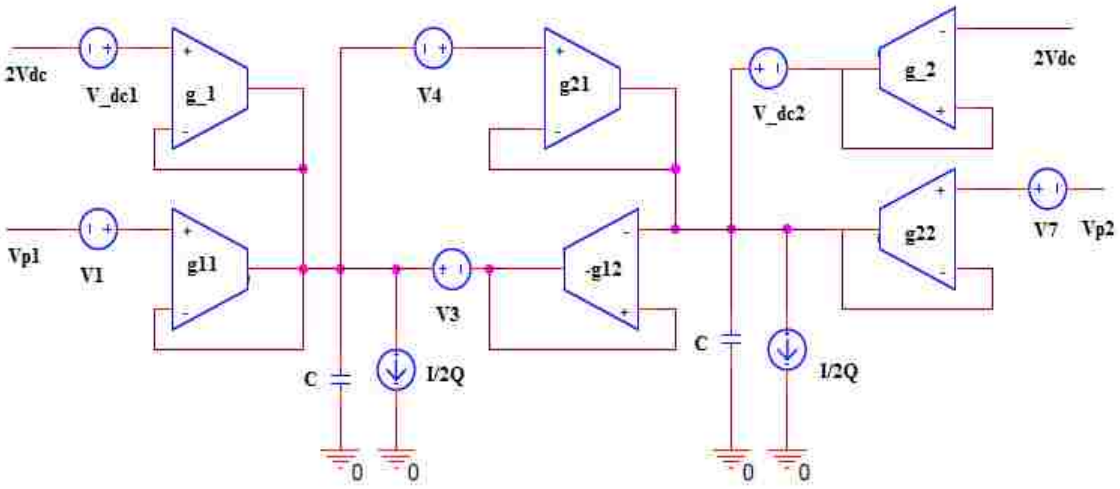
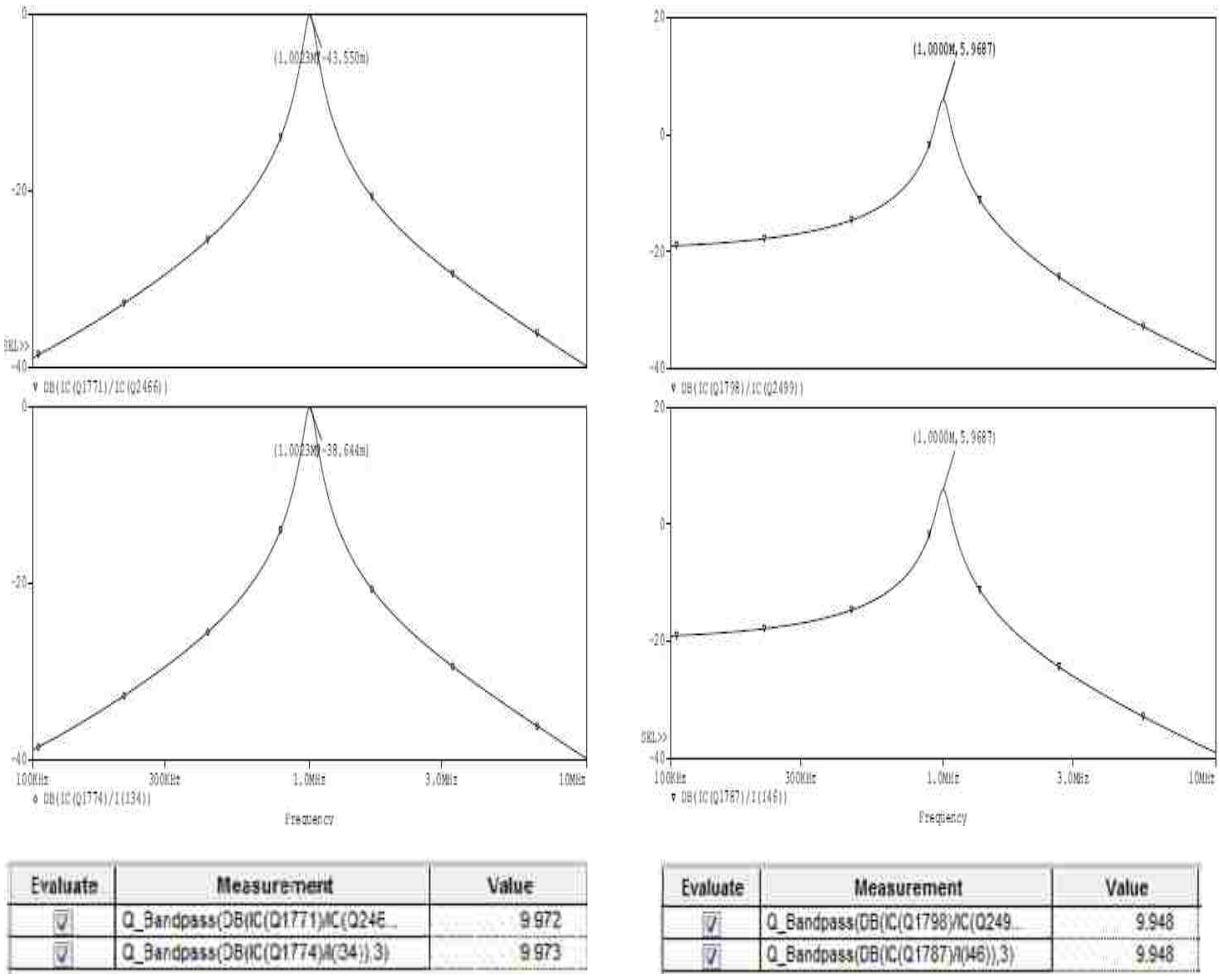


Fig. 24 Gm-C counterpart of circuit in Fig. 23

Single-ended and double-ended AC test is run in PSpice on the circuit in Fig. 23. For simplicity in comparing the test result with Fig. 22, parameters for the truncated circuit are set almost the same as they are in the test on the circuit in Fig. 20: $\mathrm{Q} = 10,\ \mathrm{I} = 0.5\mathrm{m},\ \mathrm{I/Q} = 0.05\mathrm{m},\ \frac{\mathrm{I}}{2\mathrm{Q}} = 0.025\mathrm{m},\ \left(1 + \frac{1}{2\mathrm{Q}}\right)\mathrm{I} = 0.525\mathrm{m},\ \mathrm{C} = \frac{\mathrm{I}}{2\pi \mathrm{f_c V_t}} = 3.075\mathrm{nF}$. In the double-ended test, two input signals are identical in amplitude and frequency, but the right input is set to lag the left input by 90 degrees in phase. All the components used in the simulation are assumed to be ideal.

The test result is shown in Fig. 25. Bode plots and the measured parameters such as quality factor, center frequency and peak gain, are very close to the results displayed in Fig. 18. It indicates that the modification to the circuit does not influence the performance of the circuit. For both tests, the upper Bode plot represents the left output and the bottom one represents the right output. In the single-ended test, unity gain is achieved at center frequency, while in the double-ended test the gain at center frequency is around 6dB due to the AC signal superposition. Additionally, Bode plots from the single-ended test show better low frequency suppression and better overall symmetry than that given by the double-ended test.



Evaluate	Measurement	Value
☑	Q_Bandpass(DB(IC(Q1771)/IC(Q246...	9.972
☑	Q_Bandpass(DB(IC(Q1774)/I(134)),3)	9.973

Evaluate	Measurement	Value
☑	Q_Bandpass(DB(IC(Q1798)/IC(Q249...	9.948
☑	Q_Bandpass(DB(IC(Q1787)/I(146)),3)	9.948

(a) (b)

Fig. 25 AC test result for the circuit in Fig. 23. (a) Single-ended test result. (b) Double-ended test result.

4.5.2 Tunability Improvement and Design Optimization

Although the design in Fig. 23 has better topology symmetry, other two defects such as inconvinience in tuning and non-unity gain at the center frequency still exist. The complexity in tuning is due to the fact that Q is determined by current sources tagged with $\frac{I}{Q}$, $\frac{I}{2Q}$, $\left(1-\frac{1}{2Q}\right)I$ and $\left(1+\frac{1}{2Q}\right)I$. The downside is obvious: First, hardware inefficiency. Second, at least two parameters-e.g., $\frac{I}{Q}$ and $\frac{I}{2Q}$-need to be figured out in the tuning of Q. To facilitate the tunning, we could adjust the value of the current source connected in parallel with each capacitor, from $\frac{I}{2Q}$ to $\frac{I}{Q}$. To maintain the DC equilibrium, the current sources tagged as $\left(1-\frac{1}{2Q}\right)I$ and $\left(1+\frac{1}{2Q}\right)I$ in Fig. 23 should change to I. After the parameter adjustment, the tunning of Q becomes much simpler because the current sources that determine Q are currently of the same value, denoted by $\frac{I}{Q}$. Since $\left(1+\frac{1}{2Q}\right)I$ has been adjusted to I, the task of scaling the output that corresponds to the right input could be done by the block containing such a current source. Therefore, the right most block in Fig. 23 is no longer needed. In this case, the parameter adjustment above also simplifies the schematic of the filter. The modified circuit is shown in Fig. 26 and the Gm-C counterpart remains the same as is shown in Fig. 24.

After the above adjustment, the state-space description for the filter becomes

$$\begin{vmatrix}\dot{x_1}\\ \dot{x_2}\end{vmatrix} = \begin{vmatrix}-\frac{w_0}{Q} & -w_0\\ w_0 & -\frac{w_0}{Q}\end{vmatrix}\begin{vmatrix}x_1\\ x_2\end{vmatrix} + \begin{vmatrix}\frac{w_0}{Q} & 0\\ 0 & \frac{w_0}{Q}\end{vmatrix}\begin{vmatrix}u_1\\ u_2\end{vmatrix} \tag{69a}$$

$$\begin{vmatrix}y_1\\ y_2\end{vmatrix} = \begin{vmatrix}1 & 0\\ 0 & 1\end{vmatrix}\begin{vmatrix}x_1\\ x_2\end{vmatrix} \tag{69b}$$

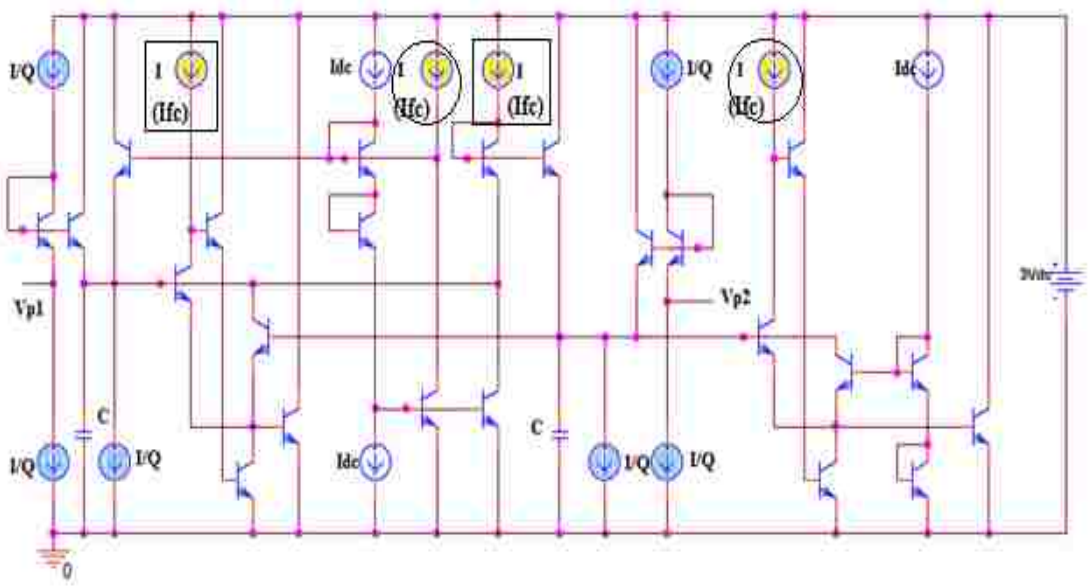


Fig. 26 Final version of the schematic for the complex filter block

Four transfer functions for the system are deduced as:

$$H_{11}|_{u_2=0} = H_{22}|_{u_1=0} = \frac{\left(\frac{w_0}{Q}\right)(S+\frac{w_0}{Q})}{S^2+2\left(\frac{w_0}{Q}\right)S+(1+\frac{1}{Q^2})w_0^2} \tag{70a}$$

$$H_{21}|_{u_2=0} = -H_{12}|_{u_1=0} = \frac{w_0\left(\frac{w_0}{Q}\right)}{S^2+2\left(\frac{w_0}{Q}\right)S+(1+\frac{1}{Q^2})w_0^2} \tag{70b}$$

According to the denominator polynomial of H_{11} and H_{22}, the two poles of both band pass filters are solved as $p_{1,2} = -\frac{w_0}{Q} \pm jw_0$. An approximation could be made that $w_{0\_est} = w_0\sqrt{1+\frac{1}{Q^2}} \approx w_0(1+\frac{1}{2Q^2})$, which indicates an error of $50(\frac{1}{Q^2})\%$ between w_{0_est} and w_0. Note that the coefficient of S in the denominator polynomial is $2\left(\frac{w_0}{Q}\right)$, it suggests that the current sources denoted as "$\frac{I}{Q}$" in the circuit virtually correspond to $\frac{Q}{2}$. That is to say, when set the current sources tagged "$\frac{I}{Q}$" in both Fig.23 and Fig.26 to the same value, the obtained quality factor of the former filter is twice as much as that of the latter one.

For both band pass filtering functions, the amplitude at the center frequency is calculated to be

$$|H_{11}|_{w=w_0} = |H_{22}|_{w=w_0} = \sqrt{\frac{1+Q^2}{1+4Q^2}}$$

When Q is big enough, $|H_{11}|_{w=w_0} = |H_{22}|_{w=w_0} = \left(20\log\sqrt{\frac{1}{4}}\right)\text{dB} = -3.01\text{dB}$. The result suggests that in the single-ended AC test the peak gain is around -3dB and in the doubled-ended AC test, unity gain could be obtained due to the signal superposition. At this point, the third problem is solved.

The tunability of Q and f_c is discussed below:

1. To tune the value of Q, adjust the current sources denoted with "$\frac{I}{Q}$" in Fig. 26. It is the current value of $\frac{I}{2Q}$ that corresponds to Q. The process of tuning Q is fairly simple when I is set.

2. Recall that $I = CV_T w_0$, it follows that all the current sources in Fig. 26 except the ones tagged with "I_{dc}" have to be tuned in order to vary the center frequency of the filter block. Such process is not only cumbersome; it even involves adjusting the current sources that affect the value of Q. Inspect eqn. (69a) and the circuit, it is easy to see that w_0 is dominantly determined by the current sources framed with rectangle. It indicates that during the tuning of f_c, one only needs to adjust the value of these two current sources plus two other ones that are framed with circle, to maintain the circuit DC equilibrium.

3. The tuning of Q and f_c does not impact each other because the two parameters are determined by two current source groups with no interaction. Specifically, the value of Q depends on the current sources in blue and the tuning of f_c involves adjusting the current sources in yellow.

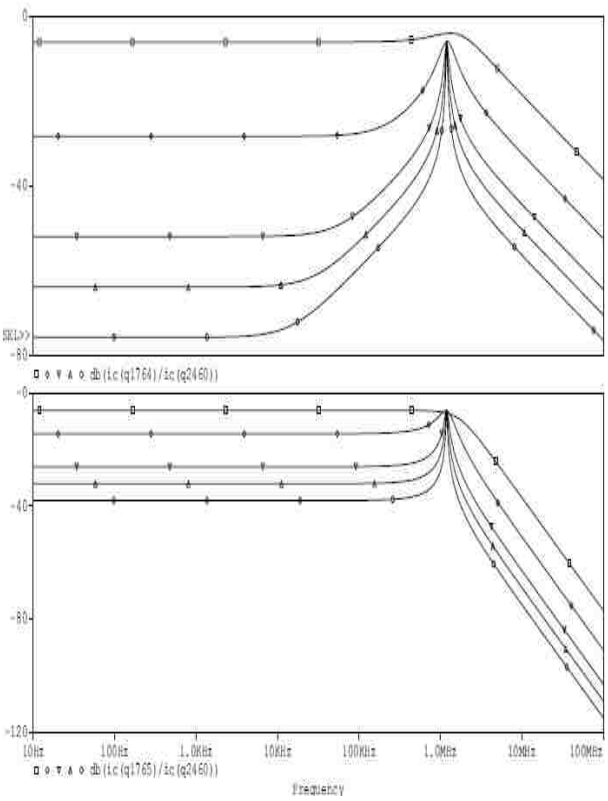
4.6 Design Test II

The test of the complex filter block proposed in Fig. 26 is run in PSpice, including:

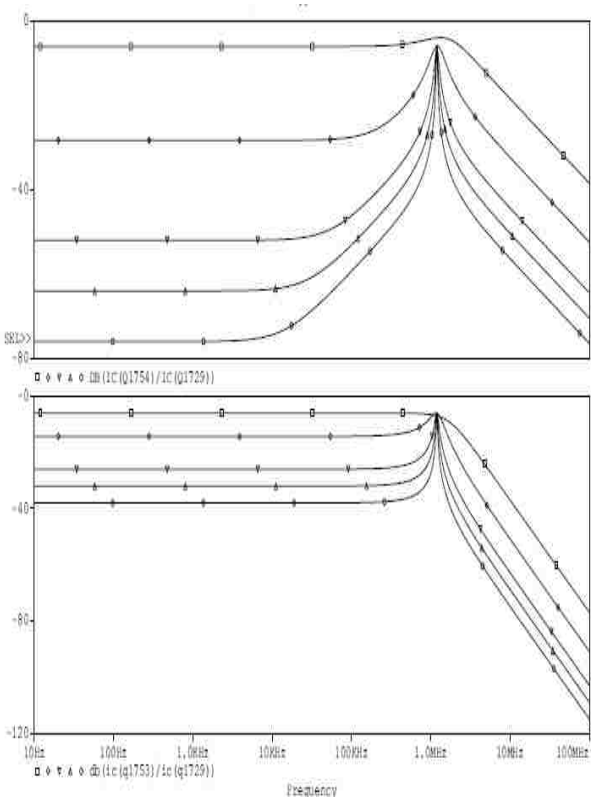
1. Transfer function test.
2. Tunability test.
3. Accuracy test.

Page 60 to Page 66 show the result of the test with ideal transistor model and C=3.075nF. Page 67 to Page 71 display the result of the test with real model and C=2.589nF.

Verification of the transfer function implementation (test with ideal BJT models)

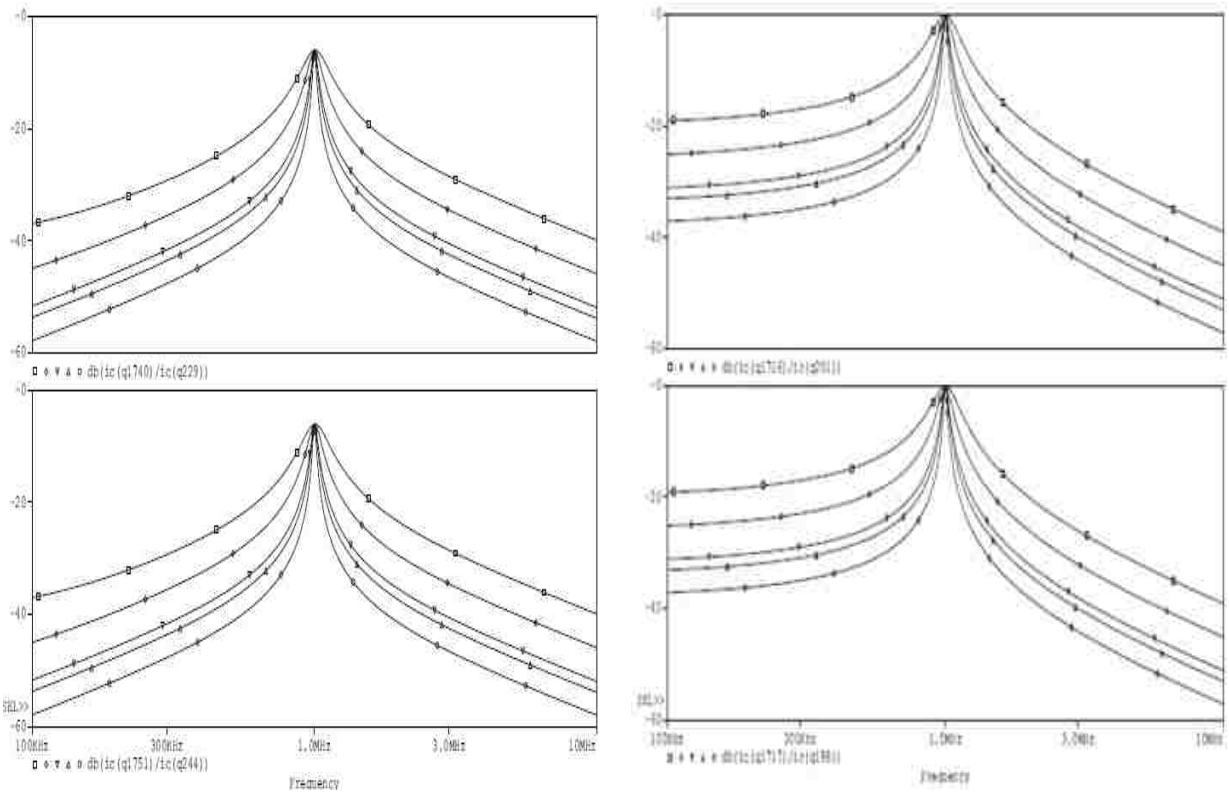


(a)



(b)

Tunability of Q (test with ideal BJT models)



(a) (b)

[redacted]

In the simulation, set $I_{fc} = I = 0.5m$ and sweep $\frac{I}{Q}$ at discrete value of 0.05m, 0.025m, 0.0125m, 0.01m, 0.0625m. It is expected to obtain in each plot a cluster of curves that represent the band pass filtering function, centered at 1MHz and with Q varying from 5 to 40. Simulation result agrees quite well with expectation. During the sweep, the peak gain of the filter block almost stays the same. For double-ended test, unity gain is obtained at center frequency. Relevant measurement data is given as below.

Table 1 Measurement result of Q, peak gain and fc when Ifc=0.5m and Q=0.05m,0.025m,0.0125m,0.01m,0.0625m. For (a) single-ended test and (b) double-ended test.

param::iq	0709.sim::q_bandpass(db(ic(q1740)/ic(q229)),3)	0709.sim::q_bandpass(db(ic(q1751)/ic(q244)),3)
5e-005	5.050	5.050
2.5e-005	10.007	10.007
1.25e-005	19.881	19.881
1e-005	24.794	24.794
6.25e-006	39.397	39.397

param::iq	0709.sim::max(db(ic(q1740)/ic(q229)))	0709.sim::max(db(ic(q1751)/ic(q244)))
5e-005	-5.995	-5.996
2.5e-005	-6.045	-6.045
1.25e-005	-6.092	-6.092
1e-005	-6.110	-6.110
6.25e-006	-6.166	-6.166

param::iq	0709.sim::centerfrequency(db(ic(q1740)/ic(q229)),1p)	0709.sim::centerfrequency(db(ic(q1751)/ic(q244)),1p
5e-005	1004615.790	1004615.790
2.5e-005	1002305.238	1002305.238
1.25e-005	1000000	1000000
1e-005	999999.999	999999.999
6.25e-006	999999.999	999999.999

(a)

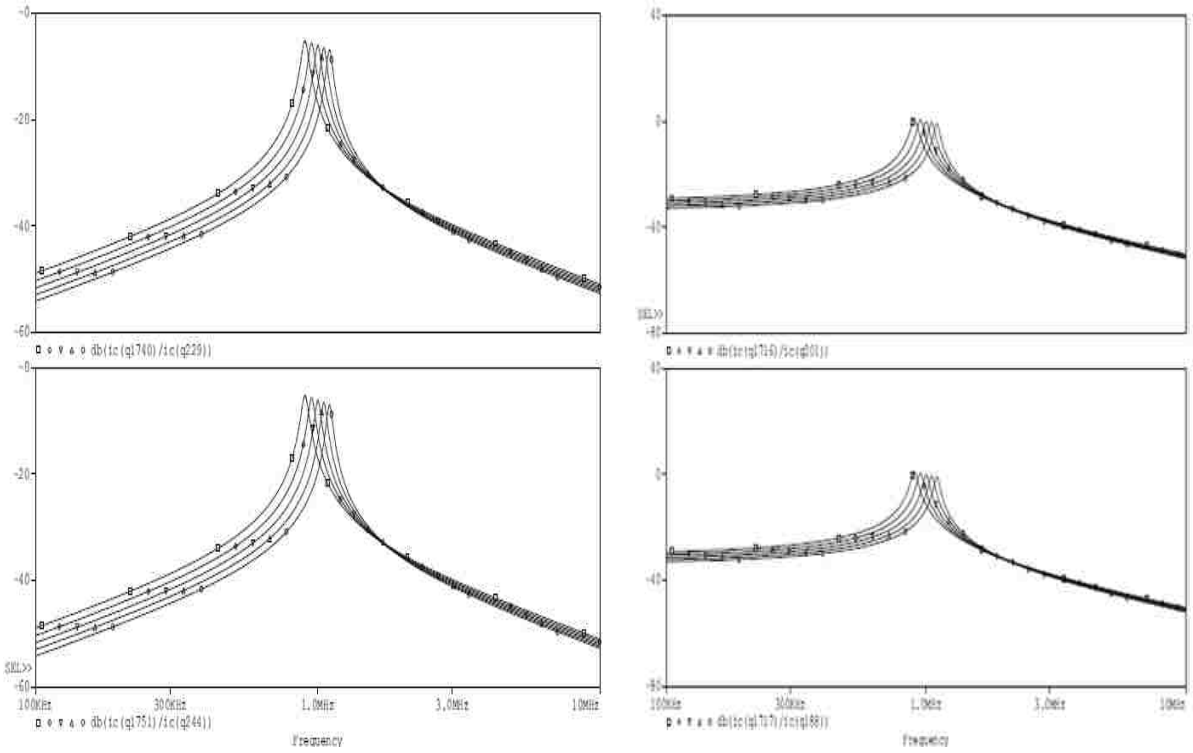
param::iq	0709.sim::q_bandpass(db(ic(q1716)/ic(q201)),3)	0709.sim::q_bandpass(db(ic(q1717)/ic(q188)),3)
5e-005	5.001	5.001
2.5e-005	9.982	9.982
1.25e-005	19.881	19.881
1e-005	24.798	24.798
6.25e-006	39.411	39.411

param::iq	0709.sim::max(db(ic(q1716)/ic(q201)))	0709.sim::max(db(ic(q1717)/ic(q188)))
5e-005	-0.018	-0.018
2.5e-005	-0.035	-0.035
1.25e-005	-0.071	-0.071
1e-005	-0.089	-0.089
6.25e-006	-0.144	-0.144

param::iq	0709.sim::centerfrequency(db(ic(q1716)/ic(q201)),1p)	0709.sim::centerfrequency(db(ic(q1717)/ic(q188)),1p)
5e-005	1000000	1000000
2.5e-005	1000000	1000000
1.25e-005	999999.999	999999.999
1e-005	999999.999	999999.999
6.25e-006	999999.999	999999.999

(b)

Tunability of f_c (test with ideal BJT models)



(a) (b)

[redacted]

In the simulation, set $I_Q = 0.0125\text{m}$, sweep I_{fc} from 0.45m to 0.55m with step of 0.025m. It's expected that each plot displays a cluster of curves representing the band pass filtering function, with a constant Q of 20 and a moving center frequency in $\pm 10\%$ range of 1MHz. Simulation result testifies the tunability of f_c. During the sweep, the quality factor and the peak gain vary in $\sim\pm 10\%$ range of the center value in opposite direction: higher I_{fc} results in higher Q and lower peak gain. Relevant measurement data is given below.

Table 2 Measurement result of fc, Q and peak gain when IQ=0.0125m and Ifc=0.45m,0.475m,0.5m,0.525m,0.55m. For (a) single-ended test and (b) double-ended test.

param::ifc	0709.sim::centerfrequency(db(ic(q1740)/ic(q229)),1p)	0709.sim::centerfrequency(db(ic(q1751)/ic(q244)),1p)
0.00045	901571.137	901571.137
0.000475	950604.793	950604.793
0.0005	1000000	1000000
0.000525	1051961.673	1051961.673
0.00055	1101539.309	1101539.309

param::ifc	0709.sim::q_bandpass(db(ic(q1740)/ic(q229)),3)	0709.sim::q_bandpass(db(ic(q1751)/ic(q244)),3)
0.00045	17.916	17.916
0.000475	18.917	18.917
0.0005	19.881	19.881
0.000525	20.837	20.837
0.00055	21.843	21.843

param::ifc	0709.sim::max(db(ic(q1740)/ic(q229)))	0709.sim::max(db(ic(q1751)/ic(q244)))
0.00045	-5.166	-5.166
0.000475	-5.637	-5.637
0.0005	-6.092	-6.092
0.000525	-6.526	-6.526
0.00055	-6.930	-6.930

(a)

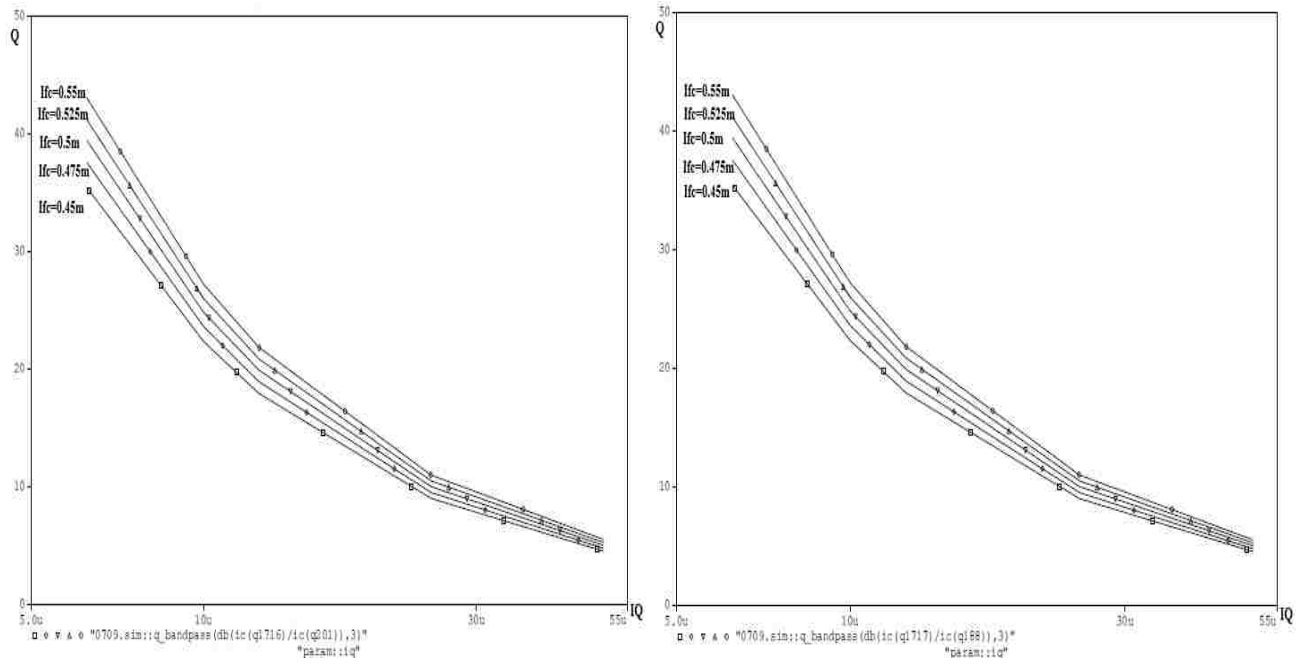
param::ifc	0709.sim::centerfrequency(db(ic(q1716)/ic(q201)),1p)	0709.sim::centerfrequency(db(ic(q1717)/ic(q188)),1p)
0.00045	899497.581	899497.581
0.000475	950604.793	950604.793
0.0005	999999.999	999999.999
0.000525	1049542.428	1049542.428
0.00055	1101539.309	1101539.309

param::ifc	0709.sim::q_bandpass(db(ic(q1716)/ic(q201)),3)	0709.sim::q_bandpass(db(ic(q1717)/ic(q188)),3)
0.00045	17.896	17.896
0.000475	18.904	18.904
0.0005	19.881	19.881
0.000525	20.840	20.840
0.00055	21.814	21.814

param::ifc	0709.sim::max(db(ic(q1716)/ic(q201)))	0709.sim::max(db(ic(q1717)/ic(q188)))
0.00045	0.849	0.849
0.000475	0.386	0.386
0.0005	-0.071	-0.071
0.000525	-0.505	-0.505
0.00055	-0.915	-0.915

(b)

Influence of I_{fc} on Q (test with ideal BJT models)

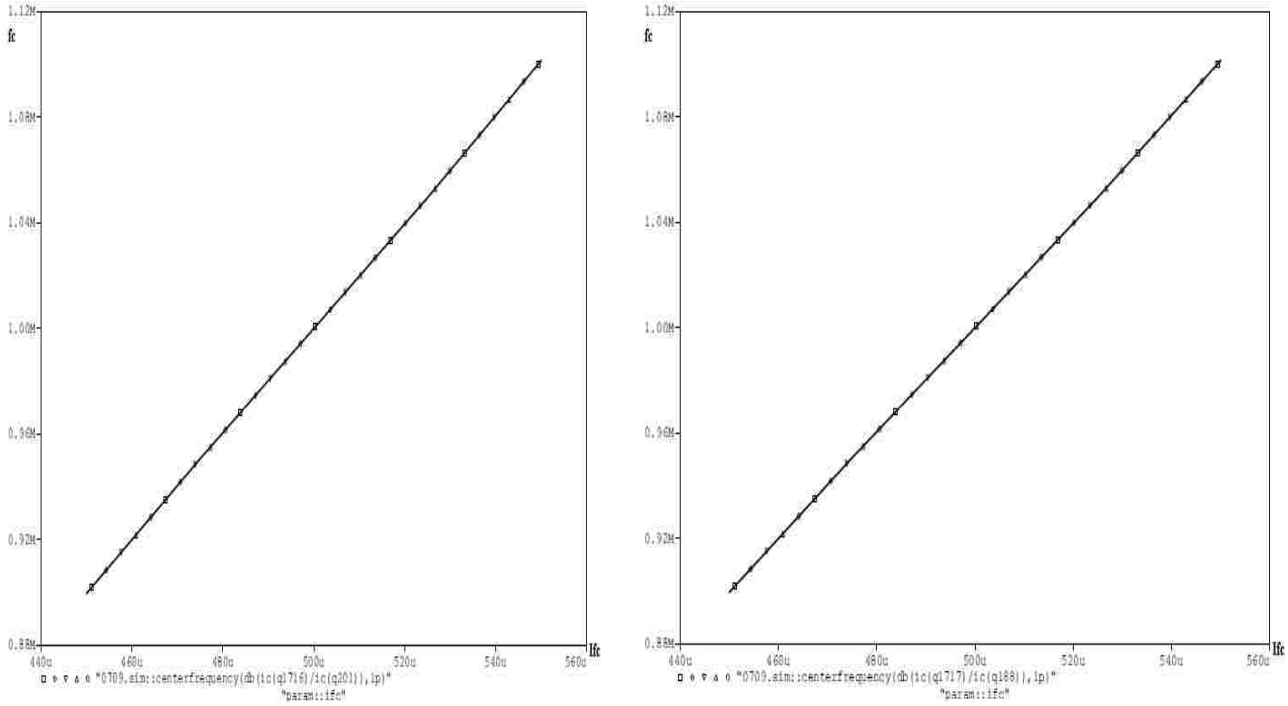


(a) (b)

param::iq	param::ifc	0709.sim::q_bandpass(db(ic(q1716)/ic(q201)),3)	0709.sim::q_bandpass(db(ic(q1717)/ic(q188)),3)
6.25e-006	0.00055	43.027	43.027
1e-005	0.00055	27.160	27.160
1.25e-005	0.00055	21.814	21.814
2.5e-005	0.00055	10.970	10.970
5e-005	0.00055	5.499	5.499
6.25e-006	0.000525	41.162	41.162
1e-005	0.000525	25.975	25.975
1.25e-005	0.000525	20.840	20.840
2.5e-005	0.000525	10.476	10.476
5e-005	0.000525	5.250	5.250
6.25e-006	0.0005	39.411	39.411
1e-005	0.0005	24.798	24.798
1.25e-005	0.0005	19.881	19.881
2.5e-005	0.0005	9.982	9.982
5e-005	0.0005	5.001	5.001
6.25e-006	0.000475	37.531	37.531
1e-005	0.000475	23.586	23.586
1.25e-005	0.000475	18.904	18.904
2.5e-005	0.000475	9.487	9.487
5e-005	0.000475	4.752	4.752
6.25e-006	0.00045	35.412	35.412
1e-005	0.00045	22.315	22.315
1.25e-005	0.00045	17.896	17.896
2.5e-005	0.00045	8.987	8.987
5e-005	0.00045	4.503	4.503

Table 3 Measurement result of Q in the doubld-ended AC test when IQ=0.00625m,0.01m,0.0125m,0.025m,0.05m and Ifc=0.45m,0.475m,0.5m,0.525m,0.55m.

Influence of I_Q on f_c (test with ideal BJT models)



(a) (b)

Fig. 31

param::iq	param::ifc	0709.sim::centerfrequency(db(ic(q1716)/ic(q201)),1p)	0709.sim::centerfrequency(db(ic(q1751)/ic(q244)),1p)
6.25e-006	0.00055	1101539.309	1101539.309
1e-005	0.00055	1101539.309	1101539.309
1.25e-005	0.00055	1101539.309	1101539.309
2.5e-005	0.00055	1101539.309	1101539.309
5e-005	0.00055	1101539.309	1104078.619
6.25e-006	0.000525	1049542.428	1049542.428
1e-005	0.000525	1049542.428	1049542.428
1.25e-005	0.000525	1049542.428	1051961.873
2.5e-005	0.000525	1049542.428	1051961.873
5e-005	0.000525	1049542.428	1054388.896
6.25e-006	0.0005	999999.999	999999.999
1e-005	0.0005	999999.999	999999.999
1.25e-005	0.0005	999999.998	1000000
2.5e-005	0.0005	1000000	1002305.238
5e-005	0.0005	1000000	1004815.790
6.25e-006	0.000475	950604.793	950604.793
1e-005	0.000475	950604.793	950604.793
1.25e-005	0.000475	950604.793	950604.793
2.5e-005	0.000475	950604.793	952798.164
5e-005	0.000475	950604.793	954992.588
6.25e-006	0.00045	899497.581	899497.581
1e-005	0.00045	899497.581	901571.137
1.25e-005	0.00045	899497.581	901571.137
2.5e-005	0.00045	899497.581	901571.137
5e-005	0.00045	899497.581	905732.600

Table 4 Measurement result of fc in the double-ended AC test when IQ=0.00625m,0.01m,0.0125m,0.025m,0.05m and Ifc=0.45m,0.475m,0.5m,0.525m,0.55m.

Tunability of Q (test with real BJT models)

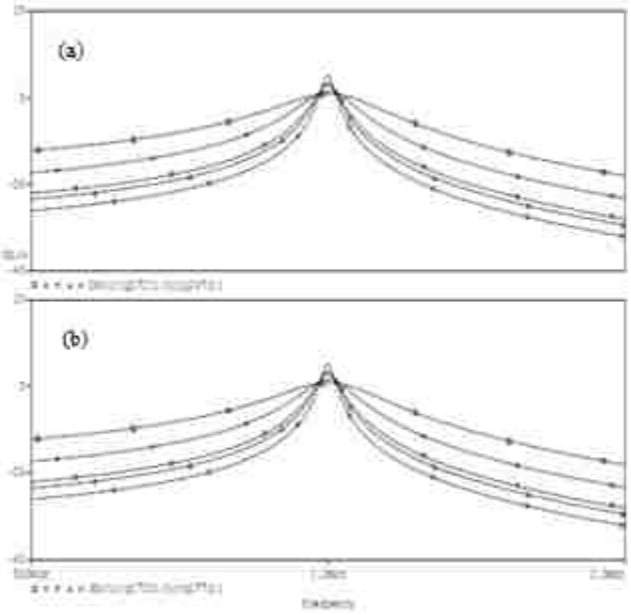


Fig. 32

param::iq	0710.sim::q_bandpass(db(ic(q1721)/ic(q2473)),3)	0710.sim::q_bandpass(db(ic(q1722)/ic(q1771)),3)
(a)		
5e-005	4.412	4.411
2.5e-005	8.800	8.800
1.25e-005	17.745	17.745
1e-005	22.297	22.297
6.25e-006	36.239	36.239

param::iq	0710.sim::max(db(ic(q1721)/ic(q2473)))	0710.sim::max(db(ic(q1722)/ic(q1771)))
(b)		
5e-005	0.659	0.672
2.5e-005	1.577	1.595
1.25e-005	2.880	2.901
1e-005	3.474	3.496
6.25e-006	5.079	5.101

param::iq	0710.sim::centerfrequency(db(ic(q1722)/ic(q1771)),1p)	0710.sim::centerfrequency(db(ic(q1721)/ic(q2473)),1p)
(c)		
5e-005	1002305.238	1002305.238
2.5e-005	999999.999	999999.999
1.25e-005	999999.999	999999.999
1e-005	999999.999	999999.999
6.25e-006	999999.999	999999.999

Table 5 Measurement of (a) Q, (b) peak gain and (c) fc in the Q tunability test

Tunability of f_c (test with real BJT models)

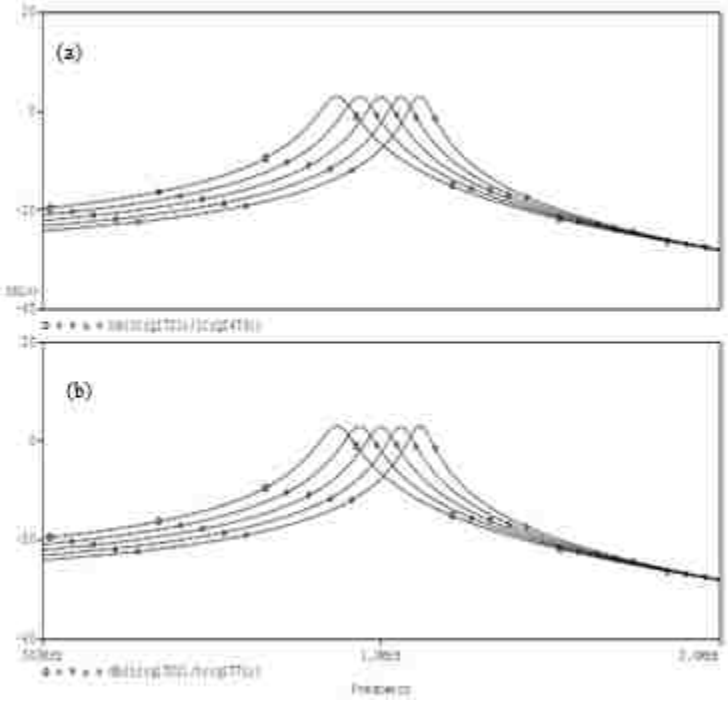


Fig. 33

param::ifc	0710.sim::centerfrequency(db(ic(q1722)/ic(q1771)),1p)	0710.sim::centerfrequency(db(ic(q1721)/ic(q2473)),1p)
(a)		
0.00045	914113.241	914113.241
0.000475	957194.071	957194.071
0.0005	999999.999	999999.999
0.000525	1042317.429	1042317.429
0.00055	1081433.951	1081433.951

param::ifc	0710.sim::q_bandpass(db(ic(q1721)/ic(q2473)),3)	0710.sim::q_bandpass(db(ic(q1722)/ic(q1771)),3)
(b)		
0.00045	15.093	15.093
0.000475	16.345	16.345
0.0005	17.745	17.745
0.000525	19.328	19.328
0.00055	21.173	21.173

param::ifc	0710.sim::max(db(ic(q1721)/ic(q2473)))	0710.sim::max(db(ic(q1722)/ic(q1771)))
(c)		
0.00045	3.033	3.041
0.000475	2.927	2.941
0.0005	2.888	2.901
0.000525	2.896	2.923
0.00055	2.987	3.022

Table 6 Measurement of (a)fc, (b)Q and (c)peak gain in the fc tunability test.

Influence of I_{fc} on Q (test with real BJT models)

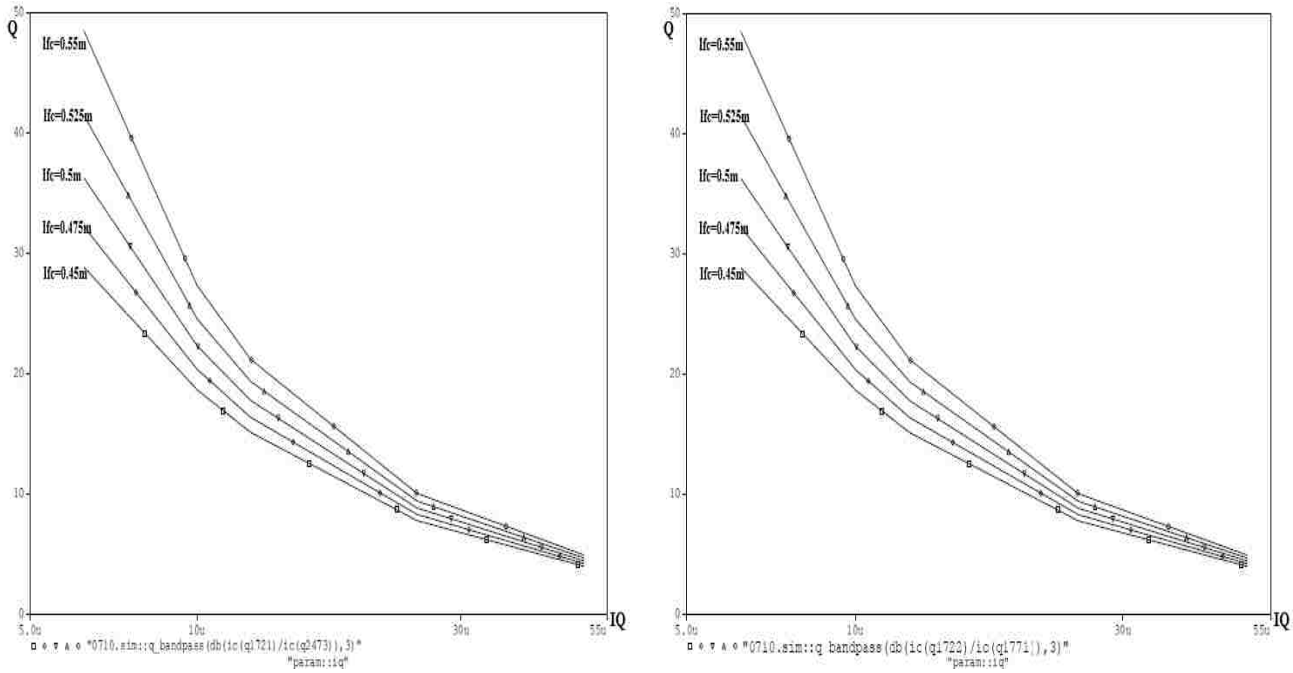
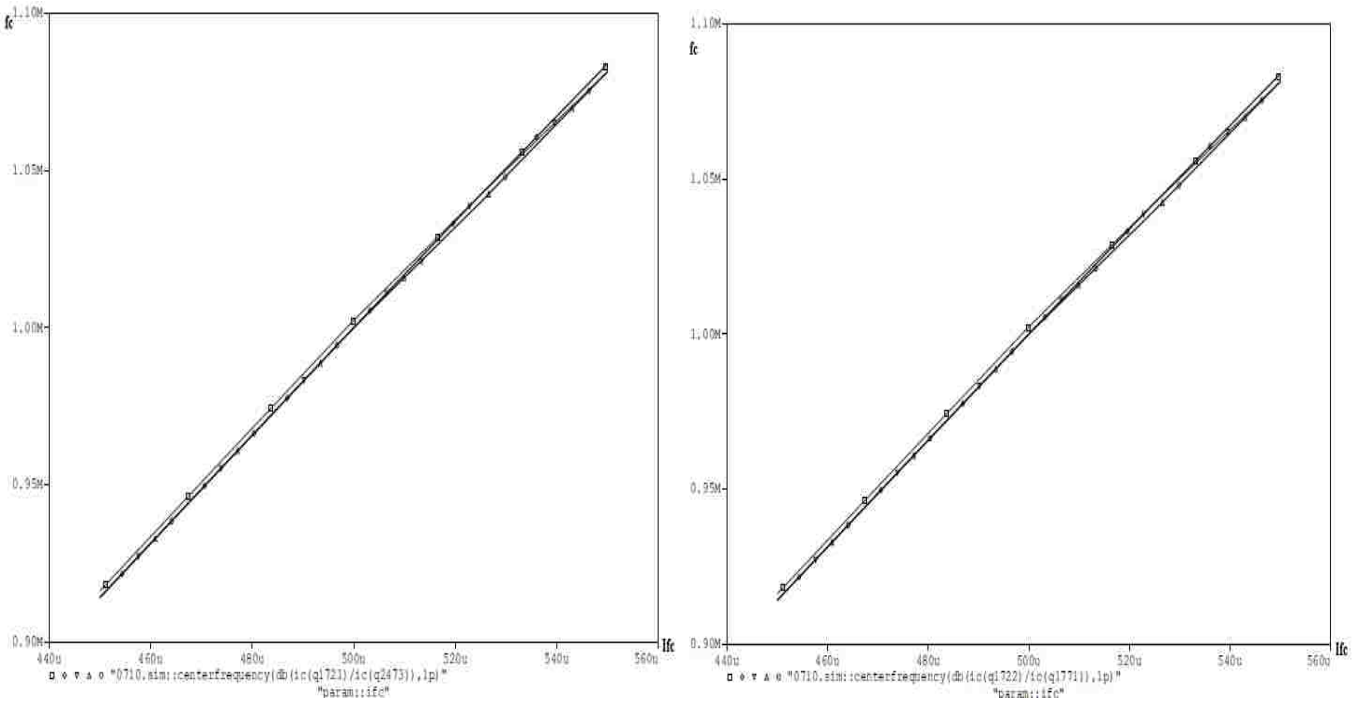


Fig. 34

param::iq	param::ifc	0710.sim::q_bandpass(db(ic(q1722)/ic(q1771)),3)	0710.sim::centerfrequency(db(ic(q1721)/ic(q2473)),1pt)
5e-005	0.00045	3.953	918220.490
5e-005	0.000475	4.179	969400.631
5e-005	0.0005	4.411	1002306.238
5e-005	0.000525	4.651	1042317.429
5e-005	0.00055	4.900	1083926.914
2.5e-005	0.00045	7.749	914113.241
2.5e-005	0.000475	8.256	957194.071
2.5e-005	0.0005	8.800	999999.999
2.5e-005	0.000525	9.379	1042317.429
2.5e-005	0.00055	10.002	1083926.914
1.25e-005	0.00045	15.093	914113.241
1.25e-005	0.000475	16.345	957194.071
1.25e-005	0.0005	17.745	999999.999
1.25e-005	0.000525	19.328	1042317.429
1.25e-005	0.00055	21.173	1081433.951
1e-005	0.00045	18.644	914113.241
1e-005	0.000475	20.350	957194.071
1e-005	0.0005	22.297	999999.999
1e-005	0.000525	24.551	1039920.165
1e-005	0.00055	27.329	1081433.951
6.25e-006	0.00045	28.623	914113.241
6.25e-006	0.000475	32.196	957194.071
6.25e-006	0.0005	36.229	999999.998
6.25e-006	0.000525	41.445	1039920.165
6.25e-006	0.00055	48.460	1081433.951

Table 7 Measurement of Q in the tuning of both Ifc and IQ.

Influence of I_Q on fc (test with real BJT models)



(a) (b)

Fig. 35

param::iq	param::ifc	0710.sim::centerfrequency(db(ic(q1722)/ic(q1771)),1p)	0710.sim::centerfrequency(db(ic(q1721)/ic(q2473)),1p)
5e-005	0.00045	915220.480	915220.480
5e-005	0.000475	959400.631	959400.631
5e-005	0.0005	1002305.238	1002305.238
5e-005	0.000525	1042317.429	1042317.429
5e-005	0.00055	1080926.914	1080926.914
2.5e-005	0.00045	914113.241	914113.241
2.5e-005	0.000475	957194.071	957194.071
2.5e-005	0.0005	999999.999	999999.999
2.5e-005	0.000525	1042317.429	1042317.429
2.5e-005	0.00055	1080926.914	1080926.914
1.25e-005	0.00045	914113.241	914113.241
1.25e-005	0.000475	957194.071	957194.071
1.25e-005	0.0005	999999.999	999999.999
1.25e-005	0.000525	1042317.429	1042317.429
1.25e-005	0.00055	1081433.951	1081433.951
1e-005	0.00045	914113.241	914113.241
1e-005	0.000475	957194.071	957194.071
1e-005	0.0005	999999.999	999999.999
1e-005	0.000525	1039820.185	1039820.185
1e-005	0.00055	1081433.951	1081433.951
8.25e-006	0.00045	914113.241	914113.241
8.25e-006	0.000475	957194.071	957194.071
8.25e-006	0.0005	999999.999	999999.999
8.25e-006	0.000525	1039820.185	1039820.185
8.25e-006	0.00055	1081433.951	1081433.951

Table 8 Measurement of fc in the tuning of both Ifc and IQ.

5 System Test

In this chapter, the mixer block, the complex filter block and the demodulator block are connected to form the whole system. System function is then tested by transient analysis. Since there are two approaches to front end and back end block design, two schematics for the system are presented and tested. Lastly, the image frequency rejection of the system is tested by tuning Q of the complex filter and comparing the output of a pair of input signals with image frequency of 5MHz.

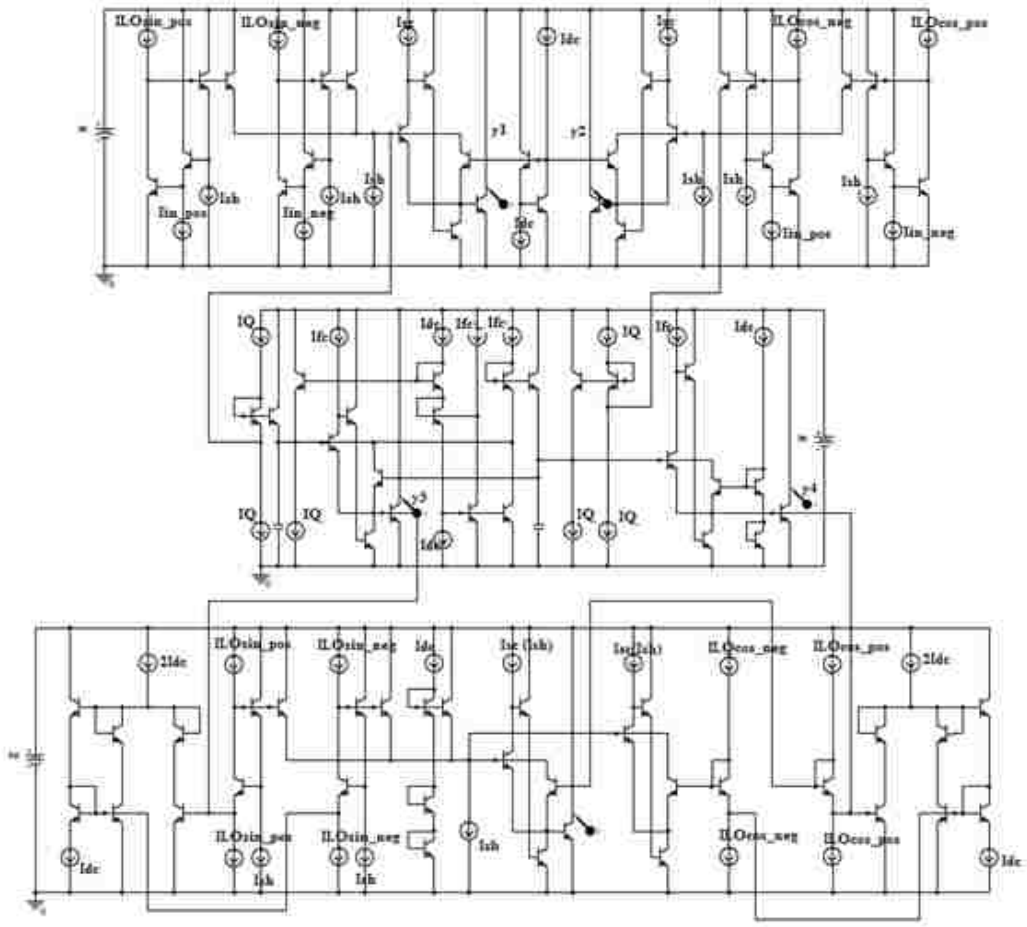
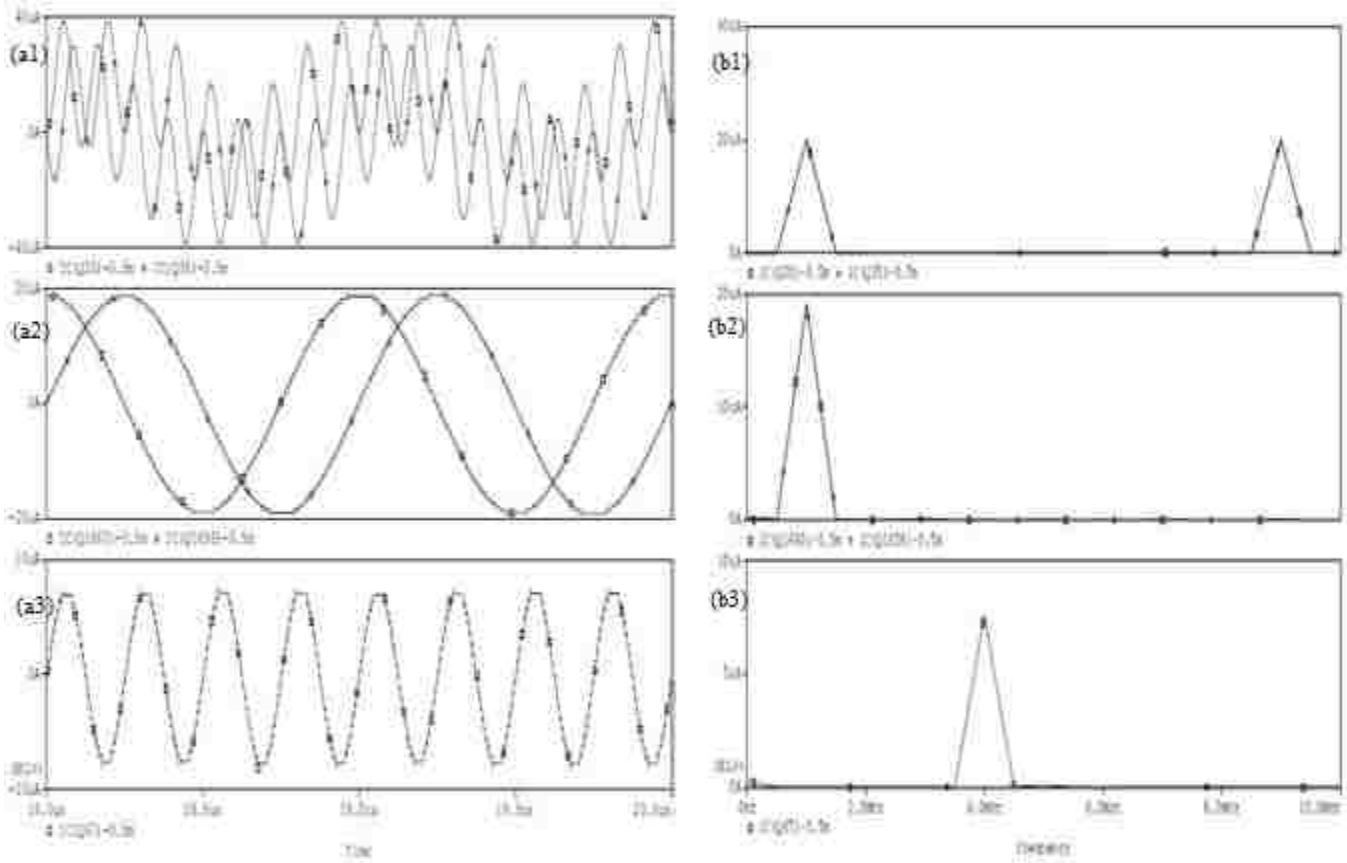


Fig. 36 System schematic I.

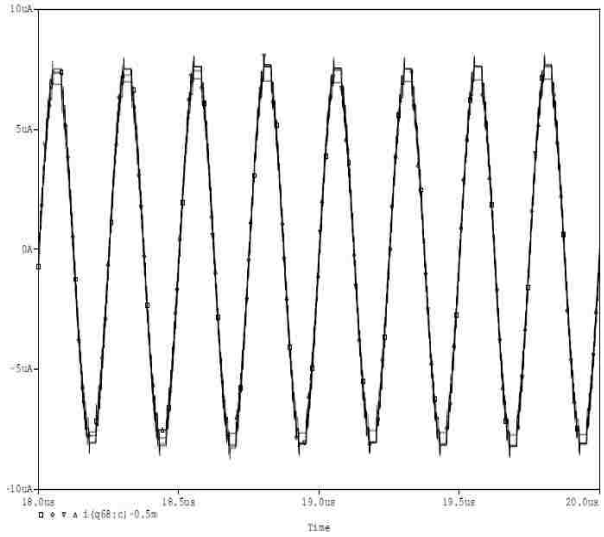
System function test



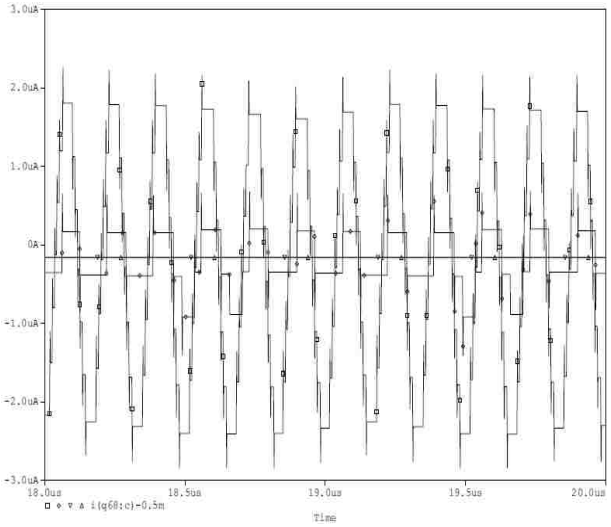
[redacted]

[redacted]

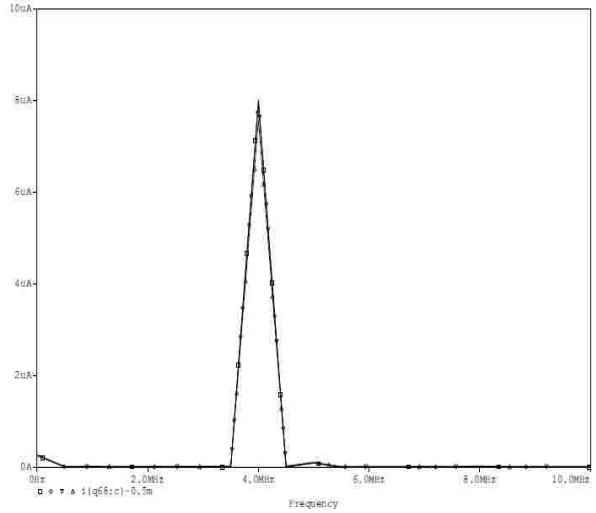
Image frequency rejection test



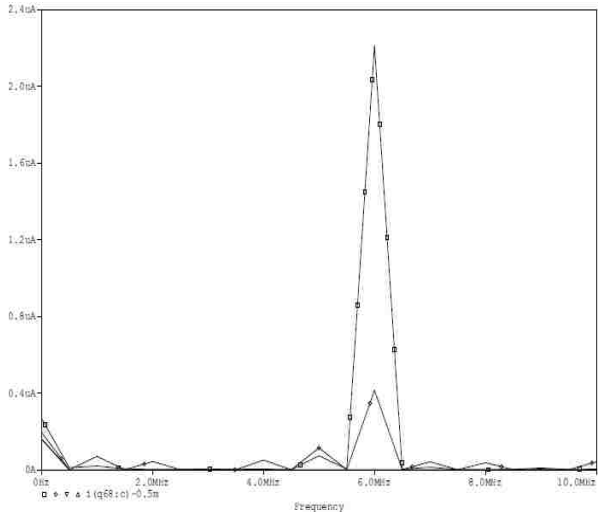
(a1)



(b1)



(a2)



(b2)

[redacted]

[redacted]

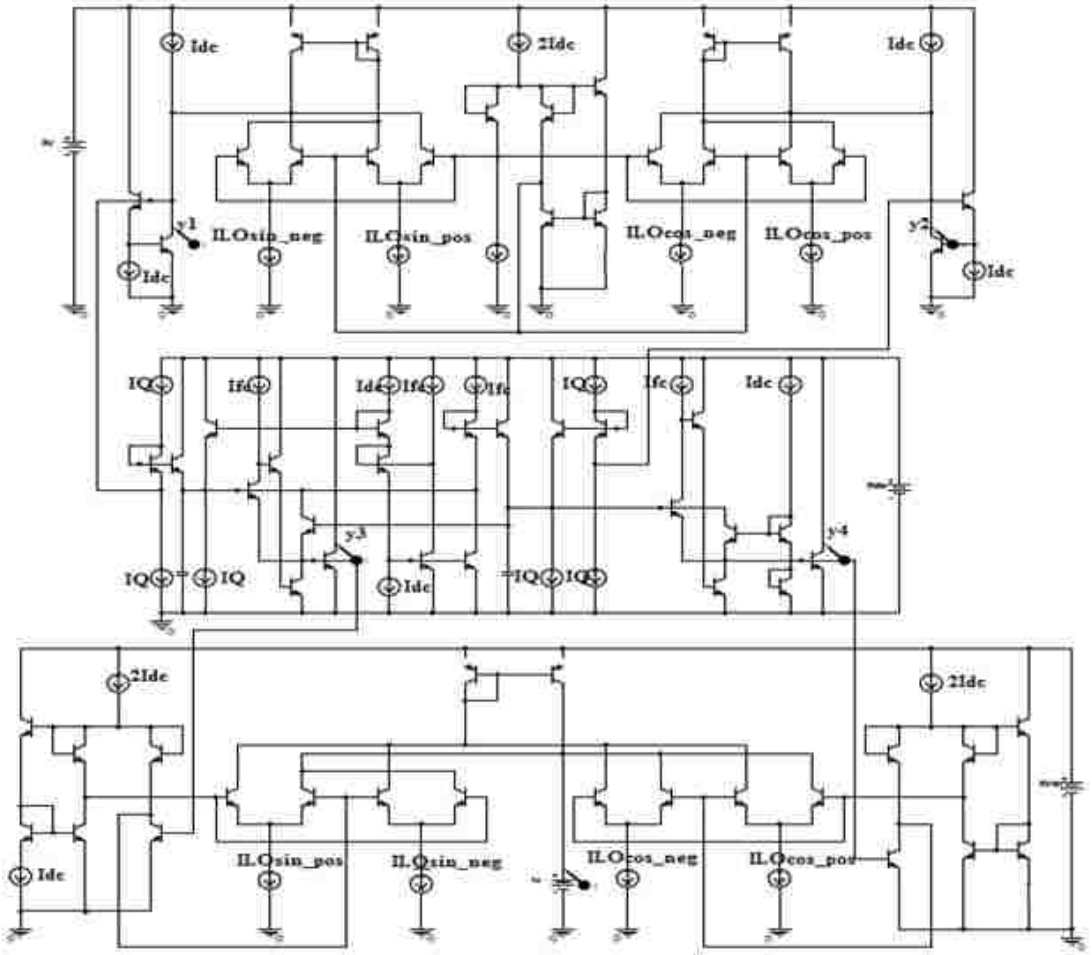


Fig. 39 System Schematic II.

System function test

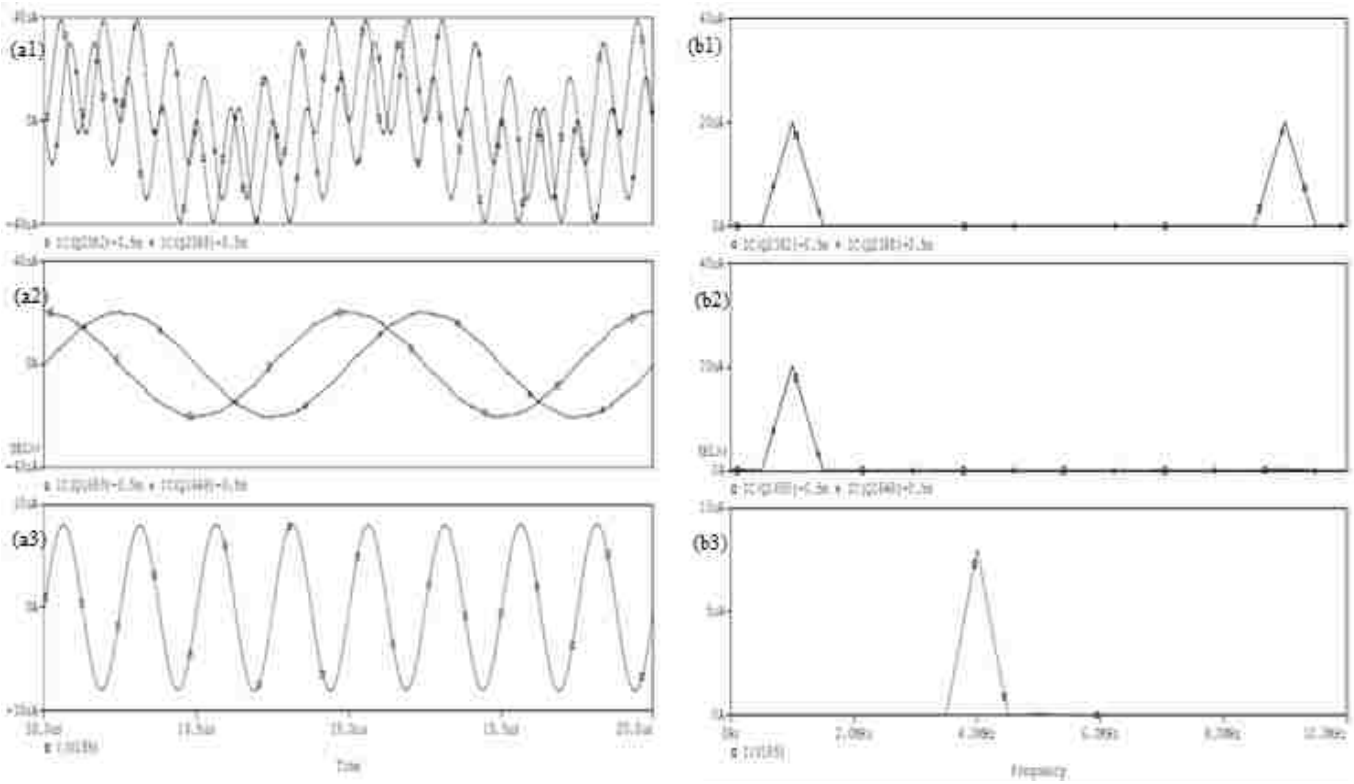
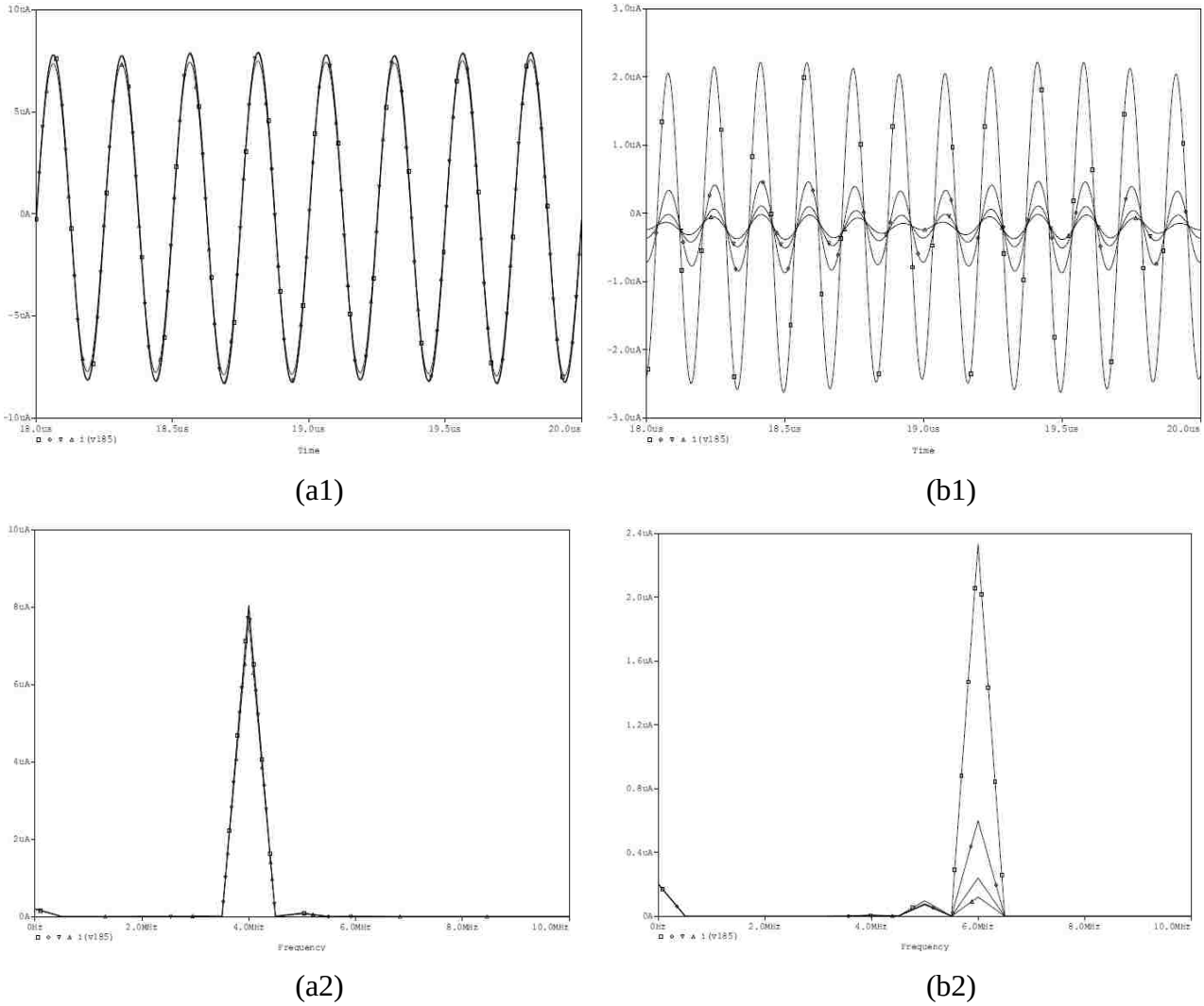


Fig. 40

Image frequency rejection test



(a1) (b1)

(a2) (b2)

Fig. 41

Sweep IQ in the core filter at discrete values of 0.25m, 0.0625m, 0.025m, 0.0125m, (corresponding to Q=1, 4, 10,20). As Q increases, the amplitude of the output for the 4MHz input remains the same, while the amplitude of the output for the 6MHz input continues decreasing. Compare Fig. 40 to Fig. 37, the overall performance of system II is better than that of system I.

6 Conclusion and Future Work

6.1 Study Conclusion

In this study, the principle of log domain filtering and the state-space synthesis technique is reviewed. An integrated current-mode complex filter system including a front end modulation block, a core filter block and a back end demodulation block is designed using BJTs and ideal current sources. The system does not contain any op amp, therefore would effectively avoid serious degradation in practice.

Two methodologies are used in the design of both front end and back end block, based on the state-space synthesis technique and the variable transconductance principle respectively. The design that uses the state-space synthesis technique virtually constructs a low pass filter with a stable DC operating point. The input variable in the state-space description of the filter is a scaled offset current product which is formed by the combination of several current products. The output variable equals the state variable, which is a current related to the voltage across the "capacitor". The DC equilibrium of the filter is achieved by forcing the currents flowing into and out of the "capacitor" node to strictly obey KCL. Transient test is run in PSpice using both ideal and real BJT models. The test with ideal models shows result that perfectly matches the theoretical evaluation. However, for the test with real models, the amplitude and offset of the output current is smaller than the theoretical value. The former parameter has an error of 10% and the latter parameter has an error of 1%. FFT frequency spectrum of each test suggests that the circuit performs properly as a mixer block.

The design for core filter starts from the state-space description of the block. After making proper definitions for the state variables and the input/output variables, a

schematic is developed to realize the corresponding nodal equations. Gm-C counterpart of the schematic is introduced to illustrate the filter at block level. DC analysis of the circuit is made by formulating nodal equation that describes the current condition at each capacitor, and extra DC currents are intentionally added in order to force the DC equilibrium. To enhance the topology symmetry and schematic conciseness, the circuit is then truncated. A direct result is that to constantly obey KCL, the ungrounded node of each capacitor requires only one block that provides additional DC current. For the simplicity in tuning Q and f_c, the original state-space description of the filter is slightly modified. The modification greatly improves the tunability by explicitly assigning the task of tuning Q and tuning f_c to two current source groups with no interaction. Moreover, each current source in the same group technically share the same adjustment parameter during the tuning. AC simulation is run in PSpice, using both ideal and real BJT models. Simulation result shows the successful implementation of a double-input-double-output second-order band pass filter which is electronically tunable in both Q and f_c, with unity gain at center frequency. Adjusting I_Q has little influence on f_c when f_c varies in the range of $\pm 10\%$; however, large Q is sensitive to the tuning of f_c .

Two schematics of the whole system are proposed. Transient test using ideal transistor model shows excellent agreement with the theory, thus verifies the system function of modulation, band pass filtering, and demodulation. Image frequency rejection capability of the system is also tested. In the test, Q of the core filter is set to 1,4,10 and 20 successively. FFT frequency spectrum of the test suggests that the increase of Q effectively improves the image rejection ability of the system.

6.2 Future Work

The transient test of the system using real transistor model does not produce a satisfactory output in the simulation. This opens up the opportunity for further study on the analysis and design detail of each block and the interface between them.

Second, throughout the study, we explore the method to assist DC equilibrium for each designed block by observing the current condition at each interested node and making simple quantitative analysis. A more general technique that involves transforming the given state-space description and implementing extra circuit block could be studied.

Last but not least, given an input to the current system, the tuning of Q and f_c requires manual adjustment. Future study would research the design and implementation of a system with self-tuning ability, or with time-varying Q and f_c that are automatically tuned according to the input signal.

Appendix

Spice model for NPN transistor and PNP transistor used in simulation

AT&T ALA400 - CBICR MODELS TYPICAL CASE 8/31/87 REVISION I

NPN TRANSISTORS

```
*NR100N - 1X NPN TRANSISTOR
.MODEL NX1 NPN RB=524.6 IRB=0 RBM=25 RC=50 RE=1
+IS=121E-18 EG=1.206 XTI=2 XTB=1.538 BF=137.5
+IKF=6.974E-3 NF=1 VAF=159.4 ISE=36E-16 NE=1.713
+BR=.7258 IKR=2.198E-3 NR=1 VAR=10.73 ISC=0 NC=2
+TF=.425E-9 TR=.425E-8 CJE=.214E-12 VJE=0.5
+MJE=.28 CJC=.983E-13 VJC=0.5 MJC=0.3 XCJC=.034
+CJS=.913E-12 VJS=0.64 MJS=0.4 FC=0.5
```

PNP TRANSISTORS

```
*PR100N - 1X PNP TRANSISTOR

.MODEL PX1 PNP RB=327 IRB=0 RBM=24.55 RC=50 RE=3
+IS=73.5E-18 EG=1.206 XTI=1.7 XTB=1.866 BF=110.0
+IKF=2.359E-3 NF=1 VAF=51.8 ISE=25.1E-16 NE=1.650
+BR=.4745 IKR=6.478E-3 NR=1 VAR=9.96 ISC=0 NC=2
+TF=.610E-9 TR=.610E-8 CJE=.180E-12 VJE=0.5
+MJE=0.28 CJC=.164E-12 VJC=0.8 MJC=0.4 XCJC=.037
+CJS=1.03E-12 VJS=0.55 MJS=0.35 FC=0.5
```

Reference

1. GOPINATRAN. V., *et al*.: 'Design considerations for high-frequency continuous-time filters and implementation of an anti-aliasing filter for digital video', *IEEE J. Solid-State Circuits*,1990, **25,** pp. 1368-1378
2. KHOURY, J.M.: 'Design of a 15 MHz CMOS continuous-time filter with on-chip tuning', *IEEE J. Solid-State Circuits*, 1991, **26,** pp. 1988-1997
3. WANG. Y.-T. and ABIDI, A.A.:'CMOS active filter design at high frequencies; 3 *um* process realization of fourth order bandpass filter', *IEEE J. Solid-State Circuits*, 1990, **25,** pp. 1562-1574
4. CHIOU,C.-F., and SCHAUMANN, R.: 'Design and performance of a fully integrated bipolar 10.7 MHz analog bandpass filter', *IEEE J. Solid-State Circuits*, 1986, **SC-21,**pp.6-14
5. WILSON, B.: 'Recent developments in current conveyors and current-mode circuits', *IEE Proc. G*, 1990,**137,**(2),pp. 63-77
6. TOUMAZOU, C., and LIDGEY,F.J.: 'Universal active filters using current conveyors', *Electron. Lett*., 1986,**22,**(12), pp. 662-664
7. RATHORE, T.S., and DASGUPTA, S.M.: 'Current-conveyor realization of transfer function', *IEE Proc. G*, 1975, **122**, pp. 1119-1120
8. DUNNING-DAVIES, J., and STEPHENSON, J.W.: 'Sensitivity optimization of active filters containing conveyors and controlled sources', Int. J. Electron., 1980, **48,** pp. 283-289
9. HAIG,D.G., TAYLOR,J.T., and SINGH, B.: 'Continuous-time and switched-capacitor monolithic filters based on current and charge simulation', IEE Proc. G., 1990, **137,** (2). pp. 147-155
10. ROBERTS, G.W., and SEDRA, A.: 'All current-mode frequency selective circuits', *Electron. Lett.*, 1989,**25,** (12). pp. 759-761
11. SEEVINCK. E.: 'Companding current-mode integrator: a new circuit principle for continuous-time monolithic filters', *Electron. Lett.*, 1990, **26,** (24), pp. 2046-2047
12. D.R. Frey, 'Log domain filtering: an approach to current mode filtering,' in *Proc. Inst. Elec. Eng.* Pt. G, vol. 140, no. 6, pp. 406-416, Dec. 1993
13. ADAMS, R.W.: 'Filtering in the log domain'. Presented at 63rd AES Cof., New York , May 1979, Preprint 1470
14. S. France, 'Design with operational amplifiers and analog integrated circuits'
15. D.R. Frey, 'Log Domain Filtering for RF applications', IEEE *J. Solid-State Circuits* **31,** (10), pp. 1468-1475,1996

Vita

Kanlun Li was born in 1986 in Changsha, China to Mr. Jiancheng Li and Mrs. Daili Zhu. She received her B.S. degree in Electronic Science and Technology from Huazhong University, Wuhan, China in 2008. In August 2008, she joined Prof. Svetlana Tatic-Lucic's group as a research assistant in Electrical and Computer Engineering Department at Lehigh University. During her study in the group, she has been awarded Sherman Fairchild Fellowship. Since January 2010, she started to study with Prof. Douglas R. Frey, focusing on analog and mixed signal circuit design. Her research interests include filter design for various applications.