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Metal Oxide Thin Film Transistors on Paper Substrate: Fabrication, Characterization, and Printing Process

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Metal Oxide Thin Film Transistors on Paper Substrate: Fabrication, Characterization, and Printing Process

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Abstract

Flexible electronics is an emerging next-generation technology that offers many advantages such as light weight, durability, comfort, and flexibility. These unique features enable many new applications such as flexible display, flexible sensors, conformable electronics, and so forth. For decades, a variety of flexible substrates have been demonstrated for the application of flexible electronics. Most of them are plastic films and metal foils so far. For the fundamental device of flexible circuits, thin film transistors (TFTs) using poly silicon, amorphous silicon, metal oxide and organic semiconductor have been successfully demonstrated. Depending on application, low-cost and disposable flexible electronics will be required for convenience. Therefore it is important to study inexpensive substrates and to explore simple processes such as printing technology.

In this thesis, paper is introduced as a new possible substrate for flexible electronics due to its low-cost and renewable property, and amorphous indium gallium zinc oxide (a-IGZO) TFTs are realized as the promising device on the paper substrate. The fabrication process and characterization of a-IGZO TFT on the paper substrate are

discussed. a-IGZO TFTs using a polymer gate dielectric on the paper substrate demonstrate excellent performances with field effect mobility of ~20 cm^2 V^{-1} s^{-1}, on/off current ratio of ~10^6, and low leakage current, which show the enormous potential for flexible electronics application. In order to complement the n-channel a-IGZO TFTs and then enable complementary metal-oxide semiconductor (CMOS) circuit architectures, cuprous oxide is studied as a candidate material of p-channel oxide TFTs.

In this thesis, a printing process is investigated as an alternative method for the fabrication of low-cost and disposable electronics. Among several printing methods, a modified offset roll printing that prints high resolution patterns is presented. A new method to fabricate a high resolution printing plate is investigated and the most favorable condition to transfer ink from a blanket to a cliché is studied. Consequently, a high resolution cliché is demonstrated and the printed patterns of 10μm width and 6μm line spacing are presented. In addition, the top gate a-IGZO TFTs with channel width/length of 12/6μm is successfully demonstrated by printing etch-resists.

This work validates the compatibility of a-IGZO TFT on paper substrate for the disposable microelectronics application and presents the potential of low-cost and high resolution printing technology.

Chapter 1

Introduction

1.1 Research motivation

Flexible electronics is an emerging area with possible applications in displays, sensors, medical electronics, identification tags, smart cards, and so forth [1-3]. Advantages of the flexible electronics are bendable, conformally shaped, lightweight, unbreakable, and roll-to-roll manufacturable. Therefore, they have the potential to accomplish novel applications that are not restricted by the use of rigid substrates.

In most cases, flexible electronics includes a flexible substrate and essential circuits that consist of several thin film devices. A variety of flexible substrates, including metal foil, thin glass, and plastic film have been investigated for the application of flexible electronics [4, 5]. Plastic substrate is generally transparent and flexible, so the research of flexible substrates has been focused on plastic substrates for a long time. However, most of them have critical drawbacks, such as large thermal expansion causing the misalignment of layer to layer during the TFT process and low process temperature impeding the performance of the TFT device. Thin glass (~100μm) is stable up to 500℃,

so high performance TFT device can be fabricated on it. Furthermore, it does not require any gas barrier or planarization layer. However, handling thin glass substrate is challenging due to its fragile nature. Metal substrate such as stainless steel foil offers excellent thermal stability and high mechanical strength, but it involves planarization process and opaque nature. The cost of the introduced flexible substrates so far is typically higher than the commercial liquid crystal display (LCD) glass substrate. Compared to those substrates, paper substrate offers attractive advantages, such as low-cost, disposability, renewability, and abundant natural resource [6], which are appropriate for low-cost and novel application such as disposable electronics. The coefficient of thermal expansion (CTE) of paper substrate is approximately 2-16 ppm, smaller than that of most plastic substrates excluding polyimide (PI) film [7]. Besides, it turns yellow at 150^{o}C, which is similar to the Tg value of most plastic substrates. Table 1.1 shows the cost and CTE comparison of commercially available flexible substrates. Compared to the other flexible substrates, the cost per unit area of paper substrates is 10% or less [7].

Table 1.1 Cost and CTE comparison between paper and representative flexible substrates.

Substrate	Cost per unit area ($/m^2)	CTE (ppm/°C)
Stainless steel foil	50~100	10
Polyimide film	100~120	14~20
Coated paper	~ 5	2~16

Organic thin film transistors (TFTs), amorphous silicon (a-Si) TFTs, low temperature poly silicon (LTPS) TFTs, and oxide TFTs have been realized on the flexible substrates [8-10]. Even though organic TFTs are one of the best candidates for flexible electronics due to their flexibility, there is still a need for flexible electronic materials that would offer more improved carrier mobility and long-term reliability [11]. LTPS and a-Si TFTs need to overcome process temperature issues since most flexible substrates require low process temperature [12, 13]. Thanks to high mobility, low processing temperature, and simple process, oxide TFTs, especially amorphous indium gallium zinc oxide (a-IGZO TFTs) have been studied for active matrix liquid crystal displays and active matrix organic light emitting diodes [14].

Meanwhile, many researchers have fabricated flexible electronics by using conventional photolithography process. However, free standing flexible substrate is obviously not applicable to mass-production, as robots generally handle the substrates in the fabrication plant (FAB). For this reason, a few handling techniques available in the FAB have been introduced. For the plastic substrate application, Philips Research Lab proposed EPLaR (Electronics on Plastic by Laser Release) in figure 1.1 [15]. After spin-coating polyimide on glass substrate, a conventional TFT is fabricated on PI coating under 300°C. After fabricating all devices, the backside of glass is exposed to UV laser for the delamination. a-Si TFT and a-IGZO TFT can be fabricated on PI films by using this method. LG Display proposed the metal etching process to fabricate a metal foil based flexible substrate. A 600μm thick metal substrate is utilized to build TFT and display devices in conventional FAB, and the backside of metal substrate is etched by

chemical up to around 100μm after finishing all processes as illustrated in figure 1.2 [16]. Printing is the ultimate process for low cost flexible electronics. However, the printing technology is still not matured to realize high resolution and high quality device since the inaccurate registration of printing causes the misalignment of layer to layer and the printable materials are not satisfying the requirements of device characteristics. On the other hand, this printing process is an excellent choice for low-cost applications, such as electronic newspaper, RFID, battery, simple sensor, and disposable electronic business card. Therefore printing process for paper substrate is investigated in chapter 5 for low-cost process.

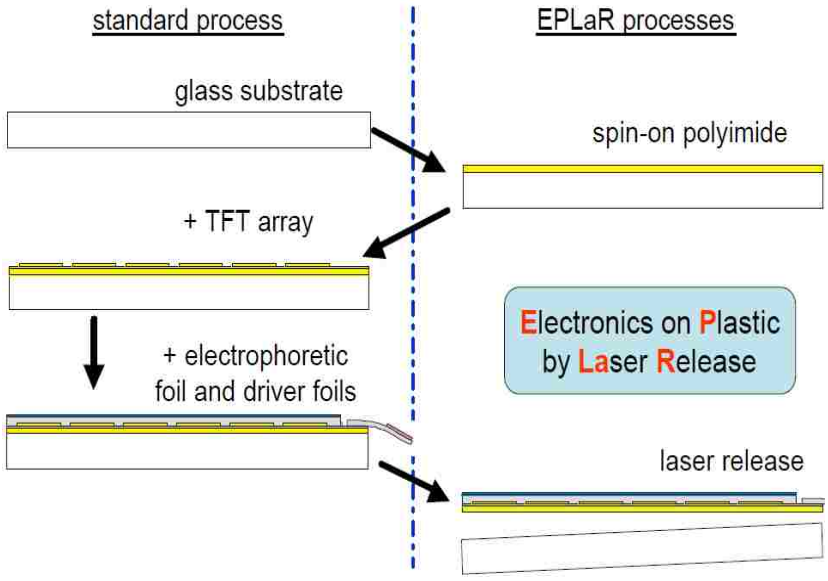

Fig. 1.1 EPLaR process to fabricate flexible electronics [Adapted from Ref. 15].

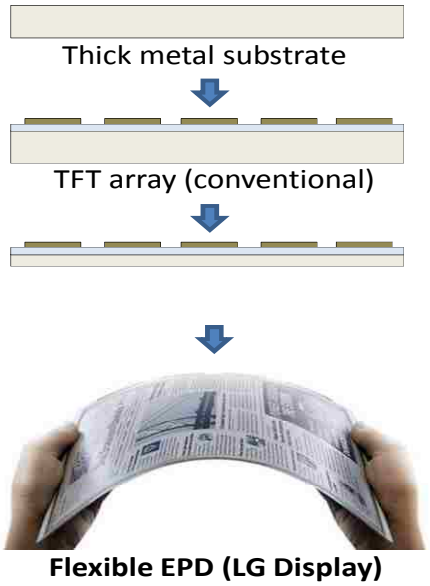

Fig. 1.2 Backside etching process of a metal substrate for flexible electronics.

According to the requirements of each application, flexible electronics can be categorized into high-end and low-cost application as shown in figure 1.3. The combination of conventional TFT fabrication process and metal foil or PI substrate is preferable to high-end application. The combination of printing process and paper substrate is appropriate to the application requiring low-cost and disposable electronics.

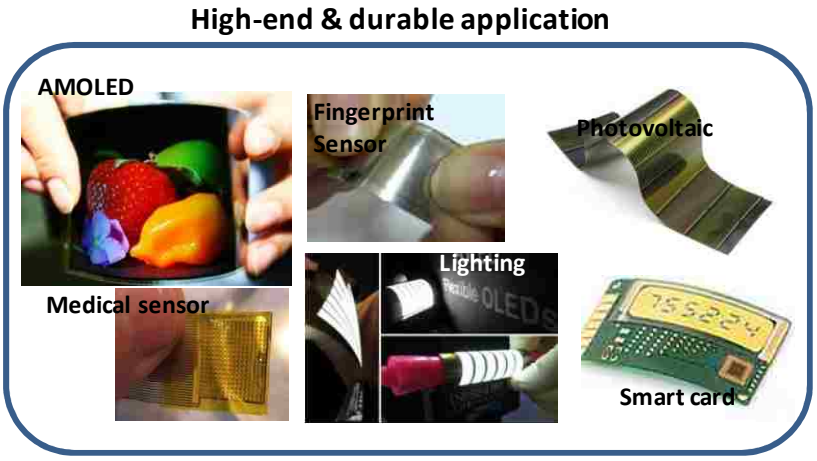

Fig. 1.3 High-end and low-cost application of flexible electronics.

Recently, a-IGZO TFTs on a paper substrate have been reported with the potential for the new flexible electronics, as shown in figure 1.4 [17]. However, the morphology of the paper used in reference [17] was too rough for the fine featured TFTs; furthermore, low mobility and high gate leakage current were presented due to the gate dielectric of low temperature SiO_2 and rough surface. In order to verify the realization of high quality TFT device on paper, this work focuses on achieving high performance device on paper substrate and printing technology is also researched for low-cost process. Challenges in this study are 1) to identify and optimize a suitable paper substrate for TFT process, 2) to achieve high performance a-IGZO TFTs on the paper substrate at a low process temperature (≤150°C), 3) to explore p-channel oxide TFTs in order to complement the n-channel a-IGZO TFTs and then enable CMOS circuit architectures, and 4) to improve roll printing technology as an alternative method for low cost TFT fabrication.

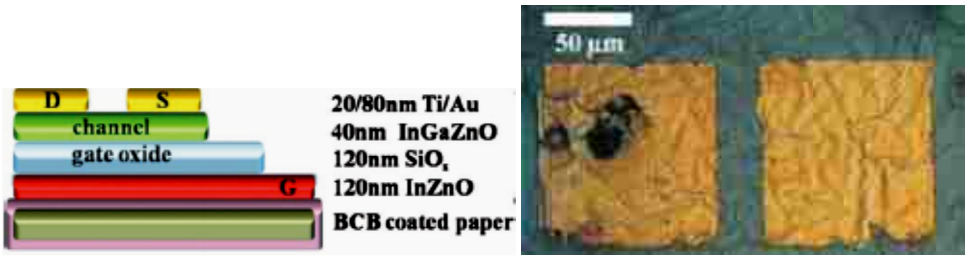

Fig. 1.4 Schematic diagram and InGaZnOx TFT image on paper substrate [Adapted from Ref. 17].

1.2 Dissertation Goals

The first goal of this dissertation is to understand and optimize the paper substrate for microelectronics fabrication in order to achieve novel flexible electronics. The second goal is to validate a-IGZO TFT with excellent device performance on the paper substrate through studying polymer gate dielectric. The last goal is to investigate and improve printing technology to reduce manufacturing cost for the realization of flexible and disposable electronics. In addition, a new p-type metal oxide material is explored to attain CMOS circuit with a-IGZO TFT.

1.3 Overview of the thesis

In Chapter 2, the paper making process and the properties of paper substrate are introduced. Among various commercially available paper substrates, a promising candidate is selected. Thermal behavior and planarization process are explored for microelectronics fabrication. Patterning characteristics using photolithography is

examined on the paper substrate. In the final part of this chapter, the realizable fabrication methods of flexible display are presented. Chapter 3 focuses on the fabrication and characterization of a-IGZO TFT devices on the paper substrate. Study of polymer gate dielectric is detailed and an approach to characterize the key parameters of TFT is discussed. P-type oxide semiconductors compatible with low process temperatures have been rarely studied due to limited and elusive material resources. Therefore, the cuprous oxide of p-type semiconductor is studied for the realization of CMOS with N-channel a-IGZO TFT in Chapter 4. Chapter 5 focuses on printing technology enabling to reduce manufacturing cost for the realization of low-cost flexible and disposable electronics. Principal printing technologies are introduced at first section and then a modified offset roll printing is investigated in detail. Chapter 6 summarizes the results of this thesis, provides conclusion and discusses the area of future research.

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Chapter 2

Paper substrate for flexible and disposable electronics

In this chapter, paper is introduced as a promising substrate for flexible and disposable electronics. First main components and fabrication process of paper are presented, and then the properties of paper substrates are discussed and compared with different substrates, such as metal foil and plastic. In the last part of this chapter the surface roughness of paper substrate and planarization layer are discussed for the realization of micron size features. Glossy paper planarized by acrylate polymer is introduced as a new low cost flexible substrate and its rms surface roughness of 1nm is comparable to commercial glass substrate.

2.1 Paper structure and papermaking process

Paper is one of very familiar substrates for human being for a long time, and it has been utilized as material for packaging, exhibiting and storing information. In addition, paper is the most inexpensive flexible substrate in daily life due to abundant natural resources, and eco-friendly since it is composed of renewable material. For these

advantages, paper has recently been explored as a potential substrate for low-cost and disposable electronics [1-3]. Paper is made by pressing and drying process of pulp, which is a mixture of cellulose fibers [4]. Cellulose fiber with the molecular formula of $(C_6H_{10}O_5)_n$ consisted of de glucose is the structural component of the cell wall of wood as described in figure 2.1 [5]. Wood also contains a dark element, lignin that binds the cellulose fibers together [5]. The exposure of lignin to air and sunlight turns paper yellow because of oxidation; lignin molecules react and become less stable [6]. To eliminate lignin for a fine white paper, a chemical solvent process is utilized. The paper made without lignin is white and resists yellowing.

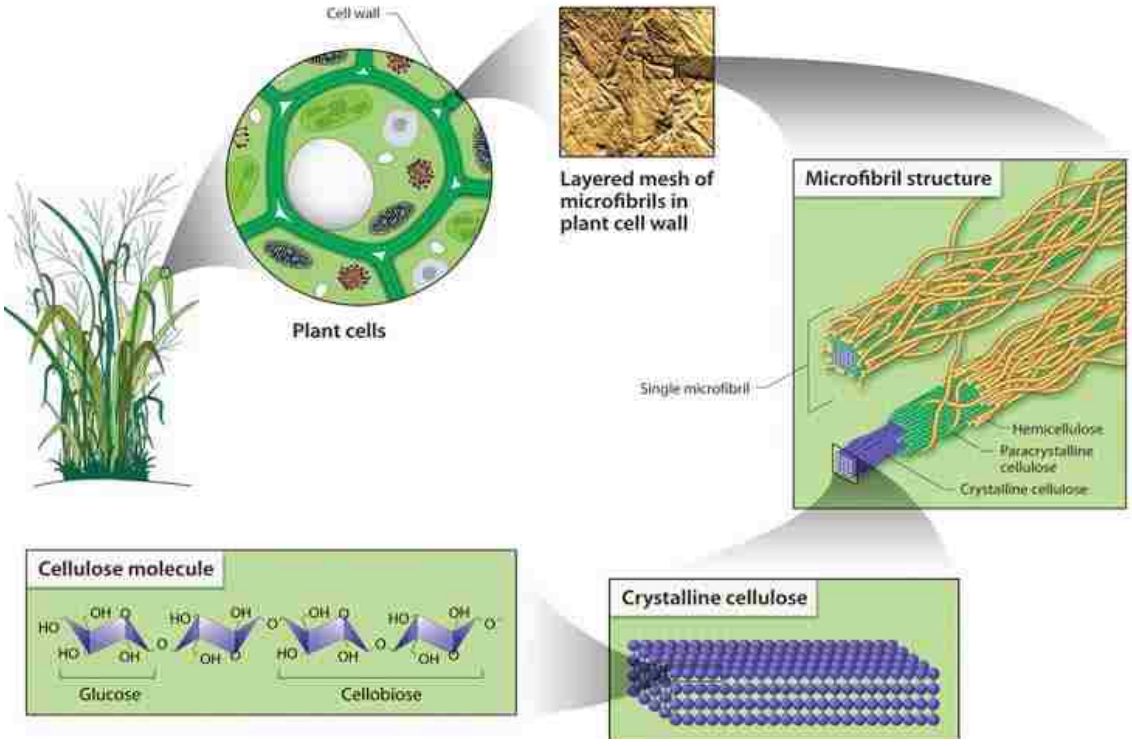


Fig. 2.1 Structure of cellulose. Cellulose is the main component of paper [Copyright; US DOE. 2005. Genomics : GTL Roadmap].

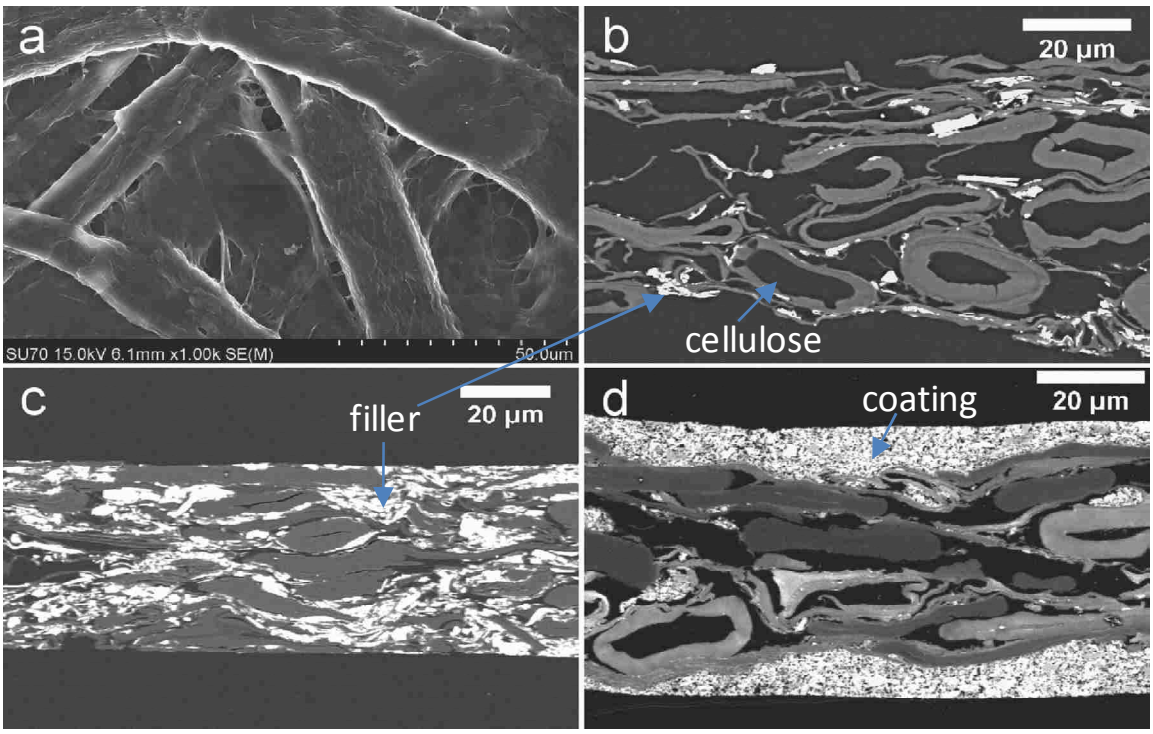


Fig. 2.2 SEM micrographs of (a) cellulose fiber (b) the cross-section of newsprints (c) supercalendered paper (d) coated paper [Adapted from Ref. 7].

Figure 2.2 is the SEM images of various paper substrates [7]. The cellulose fibers in paper are bound by hydrogen bonding and the fiber matrix is filled by fillers including calcium carbonate (CaCO3), chalk, and clay, which increase the uniformity of surface and brightness of paper [8, 9]. The surface of supercalendered paper and coated paper is smooth so it offers excellent potential for the fabrication of microscale electronics on paper. Figure 2.3 shows the papermaking process that consists of the paper forming section, the press section and the drying section to reduce the moisture [10]. At the beginning of the process, wood logs are chipped after debarking process. Heating in digester vessel with chemicals to dissolve the lignin makes the cellulose fibers suspended

in water. Then the pulp is washed to eliminate the chemicals and is passed through refiner after bleaching process. The refiner coarsens the surface of the cellulose fibers so they adhere together when shaped into a sheet. Dyes and additives are added to give the desired properties in additive tank. Wet pulp then moves to the forming fabric that makes the fibers linked and forms a mat of paper. The paper passes through a series of heated cylinders after pressed between water-absorbing textiles. Then a size press supplies a starch solution to both sides of the paper to prevent ink absorption into paper during printing. After another drying, the paper travels through a series of hard pressure rollers located at the end of a papermaking process, which is named as a calendering process that provides a smooth surface of the paper.

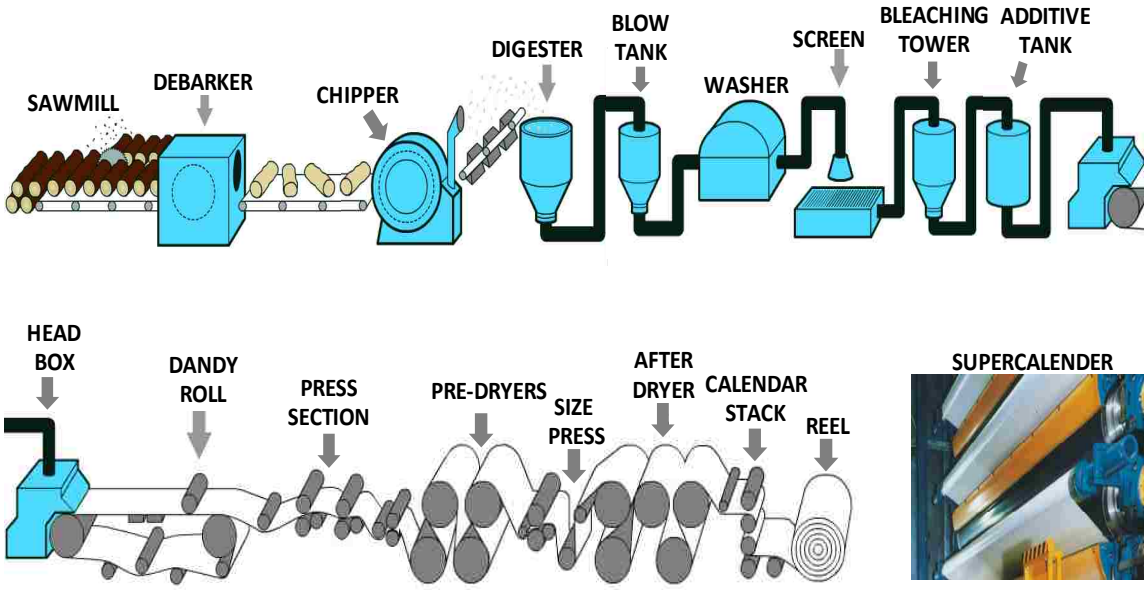


Fig. 2.3 Paper making process [Copyright; Lindenmeyr Munroe & International Paper].

2.2 Properties of paper substrate

The advantages and drawbacks of paper substrate are compared with stainless steel foil and plastic substrate in Table 2.1, and the material properties of typical flexible substrates are summarized in Table 2.2. Most of plastic substrates have demerits of high coefficient of thermal expansion (CTE) that causes thermal stress between thin film and substrate attributed to thermal TFT process. The high CTE and low T_g are also problems in the curing step of printed organic material in printing process, thus finally deforms the substrate. The deformation induces the misalignment of layer to layer and the peeling defect of thin film. Among plastic substrates in table 2.2, polyethylene naphthalate (PEN) and polyimide (PI) would be possible choices due to their thermal (CTE of ~20ppm) and chemical reliability [11]. The stainless steel substrate such as SUS 304 and SUS 430 offers the strong advantages of low CTE (~10ppm) and high process temperature (~600°C), which can integrate the high quality device on it. However the stainless steel foil contains the surface roughness from 0.1 to 1μm related to rolling direction and irregular particulate inclusion. Surface polishing and planarization coating are the common approach to attain the smooth surface. However, the use of organic planarization layer that only withstands below 300°C restricts the process temperature through TFT fabrication.

Compared to stainless steel and plastic substrate, the strongest merits of paper substrate are human-friendly and low-cost attributed to easy recycling and abundant natural resources. Recycled pulp that unwanted components are removed by chemical is also used as raw material in paper fabrication process [12]. The main challenge of paper

substrate is to control the surface roughness and to prevent any absorption of solvents and chemicals. Supercalendaring process that is a stack of calenders consisting of alternating rolls is recommended to increase paper's density, smoothness and gloss after the paper making process [13]. In addition, it is necessary to minimize particulate inclusion through maintaining the clean roll process. Polymer coating on both side of paper is beneficial to planarize the rough surface and to avoid the absorption of solvents or water.

Table 2.1 Advantages and drawbacks of each substrate for flexible electronic application [7, 15].

Substrates	Advantages	Drawbacks
Paper	Inexpensive, disposable, renewable, abundant natural resource, low CTE	Opaque, rough surface, low process temperature, weak resistance to chemical absorption
Plastic	Transparent, smooth surface	High CTE, low process temperature, moisture and gas barrier
Stainless steel foil	Low CTE, strong resistance to chemicals, impermeability, high process temperature	Opaque, rough surface

Thermal resistance also needs to be considered as the important characteristic of paper substrate for the TFT application since substrates are exposed to thermal step during photolithography and printing process. Normal paper turns yellow at 150°C and ignites at 233°C [14]. Yellowish temperature of 150°C is similar to the Tg value of most plastic substrates, except for PI and polyether sulfone (PES). Compared to polymer

substrates that offer high CTE of 20~70ppm, the paper substrate presents relatively lower CTE of 2~16ppm and thus is expected to offer dimensional stability through the TFT fabrication process [7].

Table 2.2 Material properties of typical flexible substrates.

Substrate Type	Properties			
	Tg (℃)	Chemical compatibility	Transmittance (%)	CTE (ppm/℃)
LCD Glass [15]	600	Good	~92	5
Stainless Steel Foil [15]	>600	Good	-	10
PET (Polyethylene terephthalate, Melinex®) [16]	78	Weak		20-25
PC (Poly Carbonate, Lexan®) [16]	~150	Weak (in stripper)	~90	60~70
PES (Polyether sulfone, Sumilite®) [16]	~220	Weak (in stripper)	~90	~50
PEN(Polyethylene Naphthalate, Teonex®) [16]	121	Good	~90	18~20
PI (Polyimide, Kapton®) [17]	~370	Good	Yellow	14~20
Paper (cellulose) [7]	~150	Weak	-	2~16

2.3 Paper selection for TFT fabrication

Among commercially available paper substrates, a silicone coated parchment paper is known to withstand temperature up to ~200°C and also prevents the absorption of water and solvent due to its hydrophobic surface. To prevent unnecessary misunderstandings, parchment paper is different from parchment, animal skin [18]. The present parchment paper is made by paper pulp followed by silicone coating with high density, stability, heat resistance, and low surface energy. Thus it offers non-stick

property for baking in an oven. However, its surface is too rough to fabricate fine featured TFTs, even after planarization coating, since it is produced for baking, not electronic device application. In order to successfully fabricate a silicone coated parchment paper for electronic device application, silicone needs to be coated after supercalendering process. This approach can be achieved by paper making company which possesses all equipments.

In this study, two kinds of glossy printable papers are examined due to its smooth surface. One is the inkjet printable photo paper (HP products) in figure 2.4 consisting of top coating (receptive coating and polyethylene), cellulose paper, and back side coating of polymer. The receptive coating is designed to absorb ink quickly so it absorbs water and solvents during TFT process. The other paper is a glossy laser jet paper designed to offer a higher heat resistance to prevent the deformation of the paper during printing. Gloss is achieved by the calendaring process with highly polished chromium cylinder on a coated surface. Figure 2.5 shows the results of thermal stability of each paper. The color of papers is not changed by the thermal annealing of 150°C for 30min, but become brownish at 180°C.

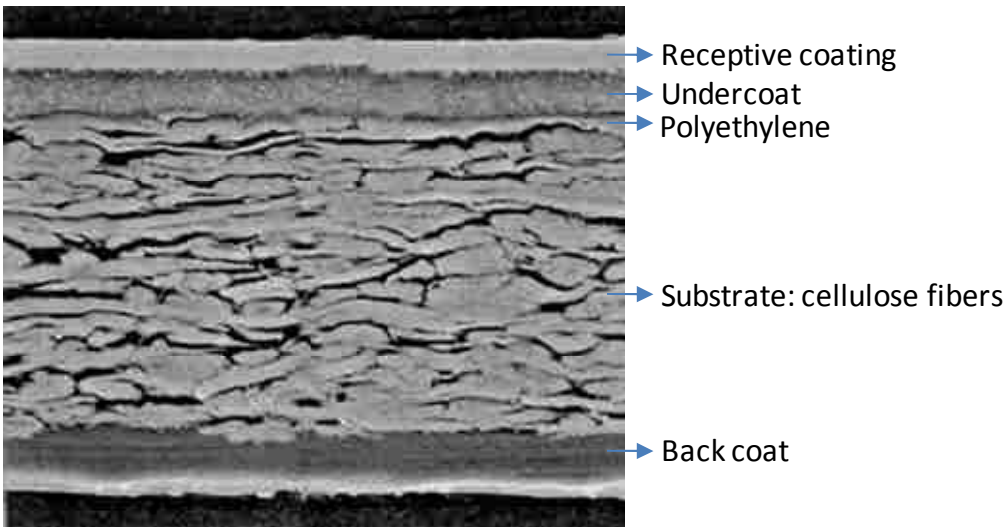
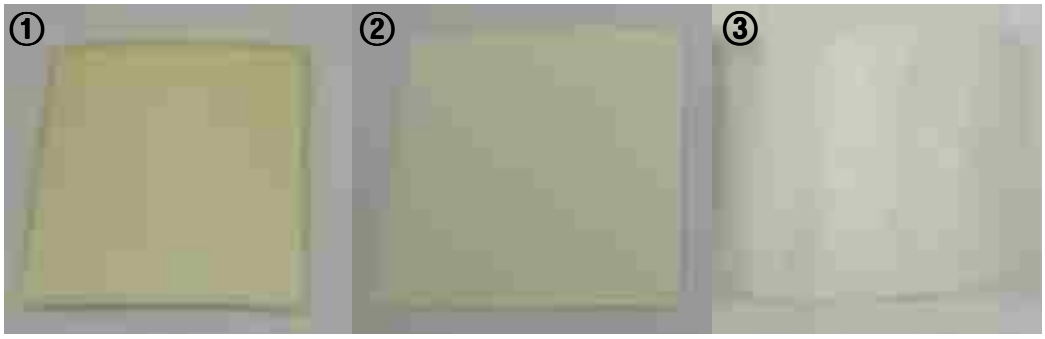


Fig. 2.4 SEM cross-section of an inkjet printable photo paper [Copyright; HP].



		Thermal stability	Surface roughness
①	Inkjet printable photo paper (HP)	150℃/30min: stable 180℃/30min: brownish	Smooth (some flake)
②	Glossy laser jet paper (HP)	150℃/30min: stable 180℃/30min: brownish	Smooth
③	Parchment paper	180℃/30min: stable	Rough

Fig. 2.5 Optical images of each paper after annealing.

For coating test, an inkjet printable paper and a parchment paper are compared after planarization coating. Metal layer of molybdenium is deposited in sputter at room temperature and SiO_2 is deposited in PECVD at 140°C. In figure 2.6, a parchment paper presents the rough surface wrinkled by the strain of the deposited Mo layer. On the other hand, the inkjet printable paper shows excellent heat resistance in PECVD and smooth surface. Even after the deposition of Mo and SiO_2 double layer, the substrate is stable as shown in figure 2.6 (b).

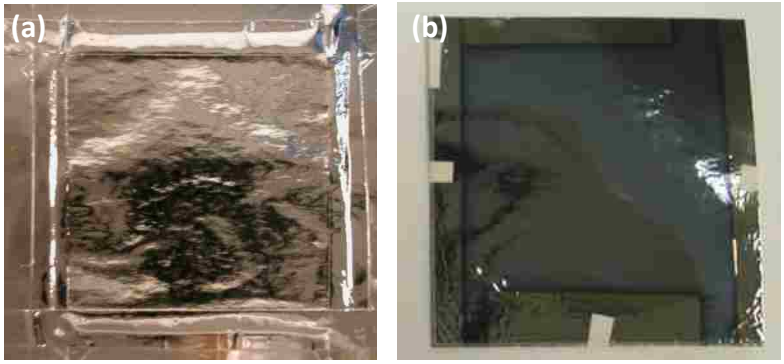


Fig. 2.6 Optical images of (a) Mo on a silicone coated parchment paper (b) Mo and SiO_2 on an inkjet printable paper. Before deposition, planarization layer was coated on both papers.

2.4 Planarization and patterning properties

In order to realize thin film based devices on a paper substrate, it is necessary to demonstrate that micron size features can be patterned on it. Compared to the commercial glass and silicon wafer substrate, the surface of typical papers is too rough to fabricate thin film electronics and thus planarization using polymer coating is considered to

improve the surface morphology of papers in this chapter. The planarization layer has been typically prepared by spin coating and curing method. However, the spin coating on paper is not simple since paper is not rigid as much as glass and metal substrate. Therefore the suggested approach is to coat the planarization polymer at the coating process which already exists in the papermaking process. Some of papermaking processes, such as roll coating and calendar, need to be modified for electronic paper application. Table 2.3 shows the available planarization materials utilized to planarize the rough surface of metal foils and passivate the TFT [19]. These materials have been proven to be stable in all chemical used in TFT fabrication. Acrylate (AC818 from Kolon Chemical) is one of most popular material to planarize and passivate the color filter of LCD. Photoacryl (PC403 from JSR co.) is used as the passivation of TFT for high aperture ratio LCD. The recommended curing temperature of the two materials is 230°C for 30min. Cyclotene (BCB) is known to offer excellent planarization property, however it requires the long annealing time of 5 hr at 250°C.

Table 2.3 Commercially available planarization materials.

Material	Model	Uses
Acrylate	AC818	Planarization of LCD color filter
Photoacryl	PC403	Passivation of LCD backplane
Cyclotene	BCB	Passivation of LCD backplane

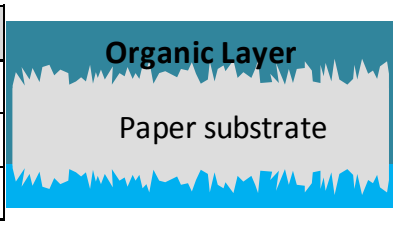


Figure 2.7 is the optical microscopic surface images of each paper substrate, and figure 2.8 presents atomic force microscopy (AFM) images of plain paper, inkjet

printable paper, and glossy laser jet paper. The inkjet printable paper offers smooth surface but it contains some microscopic cavities suspected to be created in papermaking process. A glossy laser jet paper doesn't include any cavity but it is rougher than the inkjet printable paper in AFM result. In case of a silicone coated parchment paper, the surface is very rough so it could not be measured by AFM. Even though the two printable papers present a good surface roughness, they are still rough for microelectronic fabrication and also need to be protected from any water and solvents absorption. Therefore, 3μm thick epoxy acrylate copolymer (AC-818 from Kolon Chemical) and photoacryl were coated on top side of two papers respectively and followed by curing at 150°C for 1hr. Surface roughness was analyzed by AFM before and after planarization. The glossy inkjet-printable paper and glossy laser jet paper substrates offer root-mean-square (RMS) roughness of 8.4nm and 18.8nm before planarization coating. However, they are reduced to 1~2nm after planarization in figure 2.9. These are quite analogous to the roughness (1~4nm) of typical glass substrate (Corning 1737). A glossy inkjet printable paper was selected to evaluate the patterning characteristics on it, because the thick glossy inkjet printable paper of 300μm is more useful for handling and spin-coating than thin laser jet paper of 100μm. After planarization, liftoff resist and photoresist were sequentially spin-coated on the paper and followed by baking process in oven at 150°C and 100°C, respectively. Then the substrate was exposed with a mask that contains resolution chart with known widths and spacing ranging from submicron to 13μm. Both positive and negative fine patterns were formed by photolithography on the planarized paper, and width and spacing of each pattern are well defined from 13μm to 1μm as

shown in figure 2.10. This result is also comparable to the typical TFT channel length of 4~6μm for LCD. In addition, molybdenum (Mo) was deposited on the substrate in sputter chamber for liftoff process and patterned in edge bead removal (EBR) solution. Mo is also successfully formed on paper substrate as shown in figure 2.11.

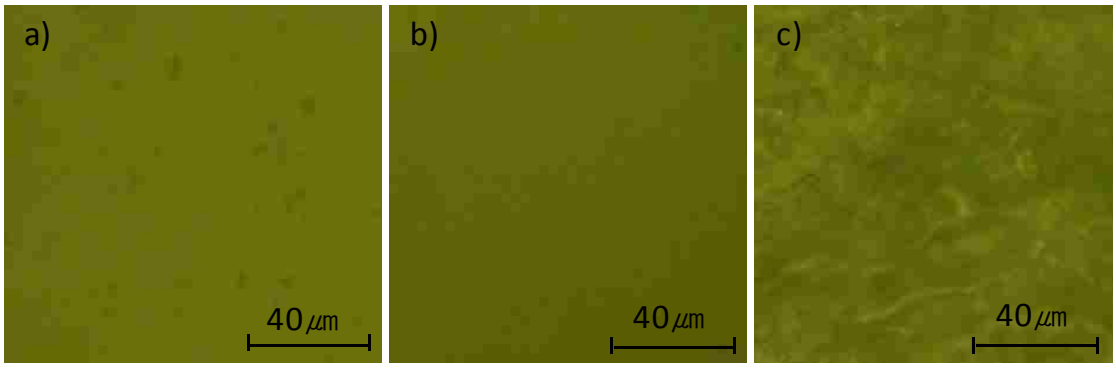
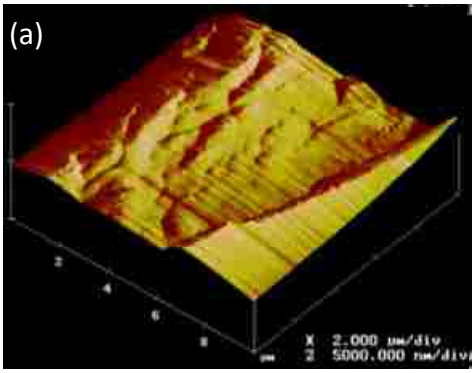
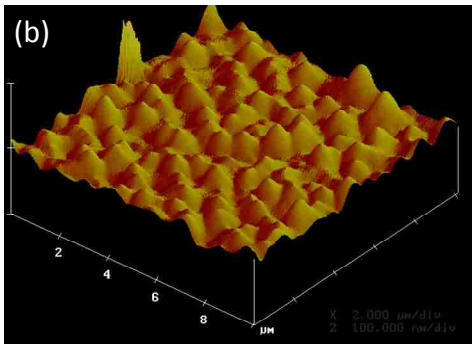


Fig. 2.7 Optical microscopic images of paper surface a) inkjet printable paper, b) glossy laser jet paper, c) a silicon coated parchment paper.

Sample (10μm×10μm)	Ra (nm)	Rms (nm)	Rmax (nm)
Plain paper	285	346	2710
I-paper	6.6	8.4	107.8
L-paper(130g)	14	18.8	252.9
Glass (corning 1737)	-	1~4	-

I-paper: inkjet printable paper
L-paper: glossy laser jet paper





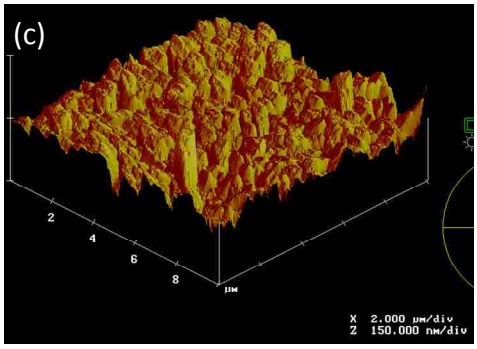


Fig. 2.8 3D AFM images of (a) plain paper (b) glossy inkjet-printable paper (c) glossy laser jet paper.

Sample (10μm×10μm)	Ra (nm)	Rms (nm)	Rmax (nm)
I-paper + AC818	1.0	1.2	7.4
I-paper + PC403	0.3	0.5	15.6
L-paper + AC818	0.9	1.7	27.7
L-paper + PC403	1.6	2.0	16.9
Glass (corning 1737)	-	1~4	-

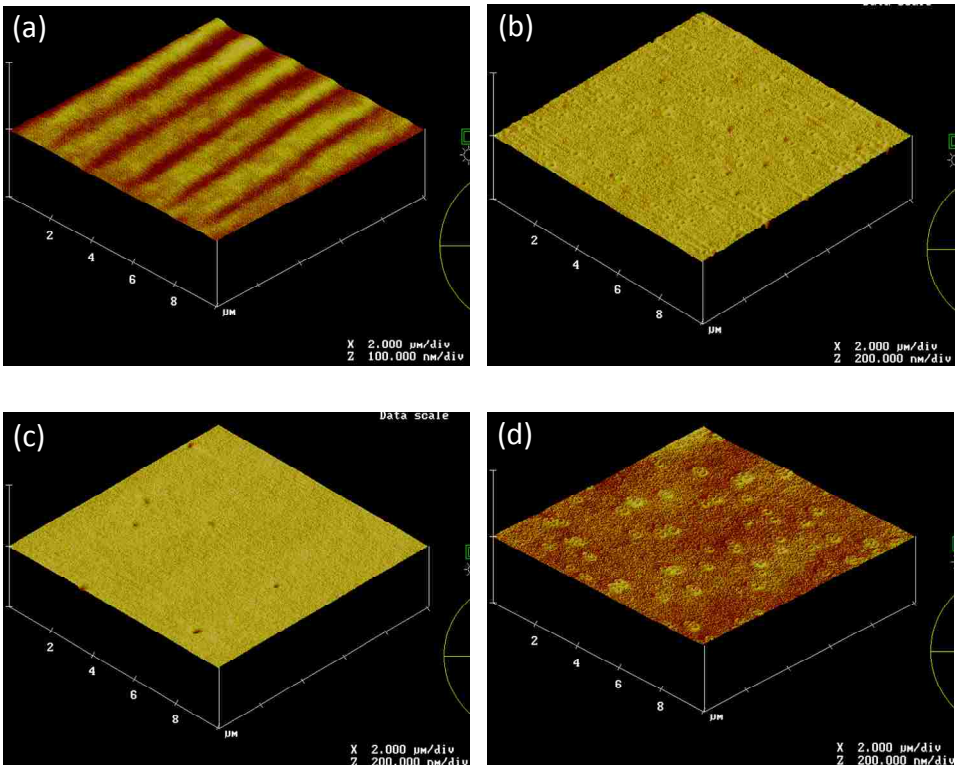


Fig. 2.9 AFM images (a) acrylate (AC818) coated inkjet printable paper, (b) acrylate (AC818) coated glossy laser jet paper, (c) photoacryl (PC403) coated inkjet printable paper, (d) photoacryl (PC403) coated glossy laser jet paper.

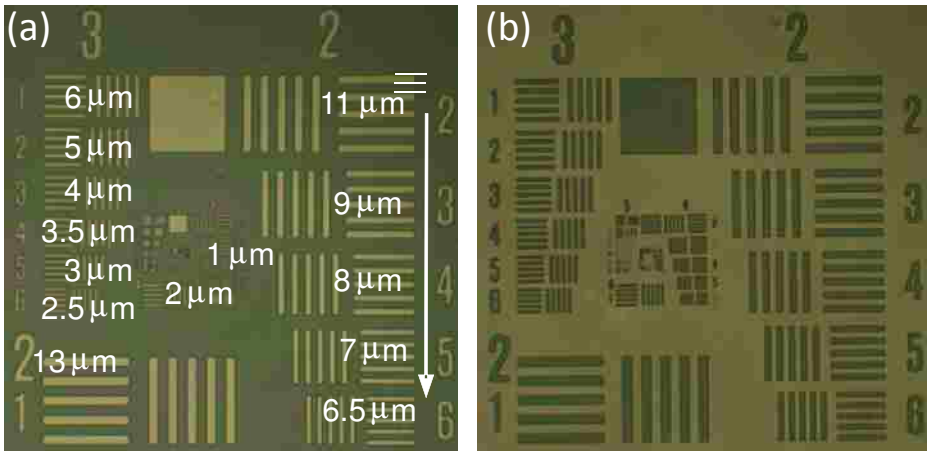


Fig. 2.10 Optical microscopic images of photolithographically patterned resolution chart with known widths and spacings on planarized glossy paper. (a) positive patterns (b) negative patterns

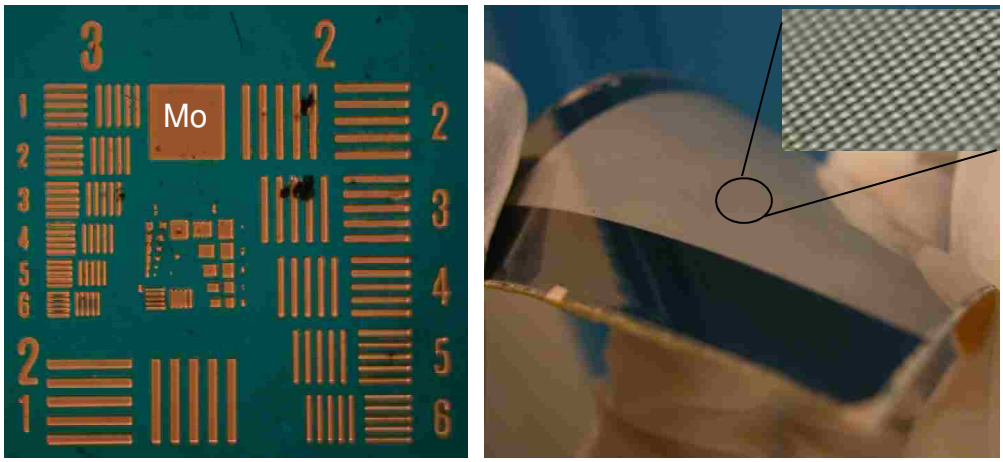


Fig. 2.11 Molybdenum patterns on a paper substrate by using liftoff process

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Chapter 3

N channel a-IGZO TFT on paper substrate

a-IGZO TFTs is explored as the possible TFT technology on paper substrate in this chapter. First the fabrication approach of a-IGZO TFT on paper substrate is presented, and then polymer gate dielectric is discussed as the gate dielectric of a-IGZO TFT on paper substrate since paper only withstands up to 150°C. In addition, characterization method and results of the a-IGZO TFTs are detailed in the last part of this chapter. In summary, a-IGZO TFTs with methyl-siloxane based gate dielectric is fabricated on a glossy paper substrate at low processing temperature (≤150°C). Compared to the silicon dioxide gate dielectric deposited at 140°C in PECVD, a-IGZO TFTs using a methyl-siloxane based dielectric demonstrates excellent performances with field effect mobility of ~20 cm^2 V^{-1} s^{-1}, on/off current ratio of ~10^6,and low leakage current, which show the enormous potential for flexible electronics application.

3.1 TFTs on paper substrate

The development of electronics on paper substrate dates back to 1960s as Brody and colleagues at Westinghouse reported a TFT of tellurium on a strip of paper [1]. After this approach, TFTs on paper substrate have rarely reported for the past decades. Since the early 2000s, flexible electronics using plastic and metal foil substrate have been investigated by several research groups [2-7]. In 2004 Eder et al. presented pentacene TFT on paper with carrier mobility of 0.2 $cm^2V^{-1}s^{-1}$ [8]. Even though organic TFT and a-Si:H TFT have been demonstrated on flexible substrates, device performance is limited by the low mobility and poor reliability (mobility of organic TFT; 0.1~3$cm^2V^{-1}s^{-1}$, a-Si:H; 0.5~1 $cm^2V^{-1}s^{-1}$). After Hosono et al. presented a-IGZO TFT with the mobility of 10$cm^2V^{-1}s^{-1}$ on PET substrate in 2004 [9], a-IGZO TFT has been extensively studied for microelectronics application owing to high mobility, low processing temperature and simple process. In 2008, Fortunato et al. introduced the GIZO TFT using cellulose-fiber-based paper as gate dielectric [10]. Table 3.1 compares the properties of each TFT device available for microelectronics.

N-type amorphous oxide semiconductors such as a-IGZO have large electron mobility since the bottom of conduction band in these materials is mainly composed of spatially spread metal *s* orbitals that facilitate carrier transport. The magnitude of direct overlap between adjacent metal s orbitals is relatively large, and is not affected even in an amorphous structure because metal-oxygen-metal bonds is retained in amorphous state that distorts the chemical bonds, as illustrated in figure 3.1. Therefore, carriers transport through the path of metal cation's ns orbitals. These features are completely different

from conventional silicon semiconductor that has carrier transport path composed of highly directional sp^3 orbitals [9].

Table 3.1 Comparison of TFT devices

	a-Si TFT	Oxide TFT	Organic TFT	Poly-Si TFT
Deposition Process	PECVD	Sputter	Printing	CVD & Excimer Laser Annealing
Max. process temperature (step)	150~350°C (GI)	≤350°C (GI)	150~200°C (curing)	≤500°C (activation)
TFT mobility	0.5~1cm^2/Vs	5~10cm^2/Vs	0.1~3cm^2/Vs	100~200cm^2/Vs
On/off current ratio	~10^6	~10^6	~10^6	~10^6
TFT reliability	excellent	excellent	not enough	excellent
Type	mostly n-type	mostly n-type	mostly p-type	n and p-type

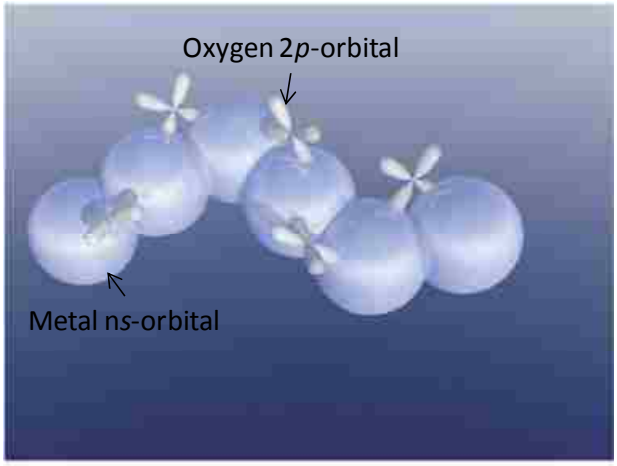


Fig. 3.1 Orbital drawing of ionic amorphous oxide semiconductor [Adapted from Ref. 9]

3.2 Low temperature gate dielectric

A low temperature TFT process is required for TFTs on paper since the temperature tolerance of a paper substrate is approximately 150^{o}C. The highest temperature of typical oxide TFTs is around 350^{o}C and it mainly results from the PECVD deposition temperature of SiO_2 dielectric. One of the objectives of the proposed works is to investigate a suitable gate dielectric at less than 150^{o}C. a-IGZO TFTs with SiO_2 dielectric on paper substrate have been reported by Lim et al. and its electrical characteristics are shown in figure 3.2 [11]. However, low mobility and high gate leakage current were observed due to its low temperature SiO_2 (<100^{o}C) and rough surface. In the work reported in reference [11], two critical problems exist. One is cracking of the inorganic gate dielectric, and the other is high gate leakage current. As shown in the transfer curve of figure 3.2, the gate leakage current (I_g) nearly overlaps with source-drain current (I_{DS}). It implies that the I_{DS} in the graph is not the exact drain current and it may include gate leakage current, $I_{DS} = I_{channel} + I_g$. In general, it is known that SiO_2 deposited at low temperature exhibits high interface trap density and very low charge to breakdown [12]. The low mobility and high subthreshold swing of a-IGZO TFTs with low temperature SiO_2 are mainly attributed to charge trapping caused by high interface trap density.

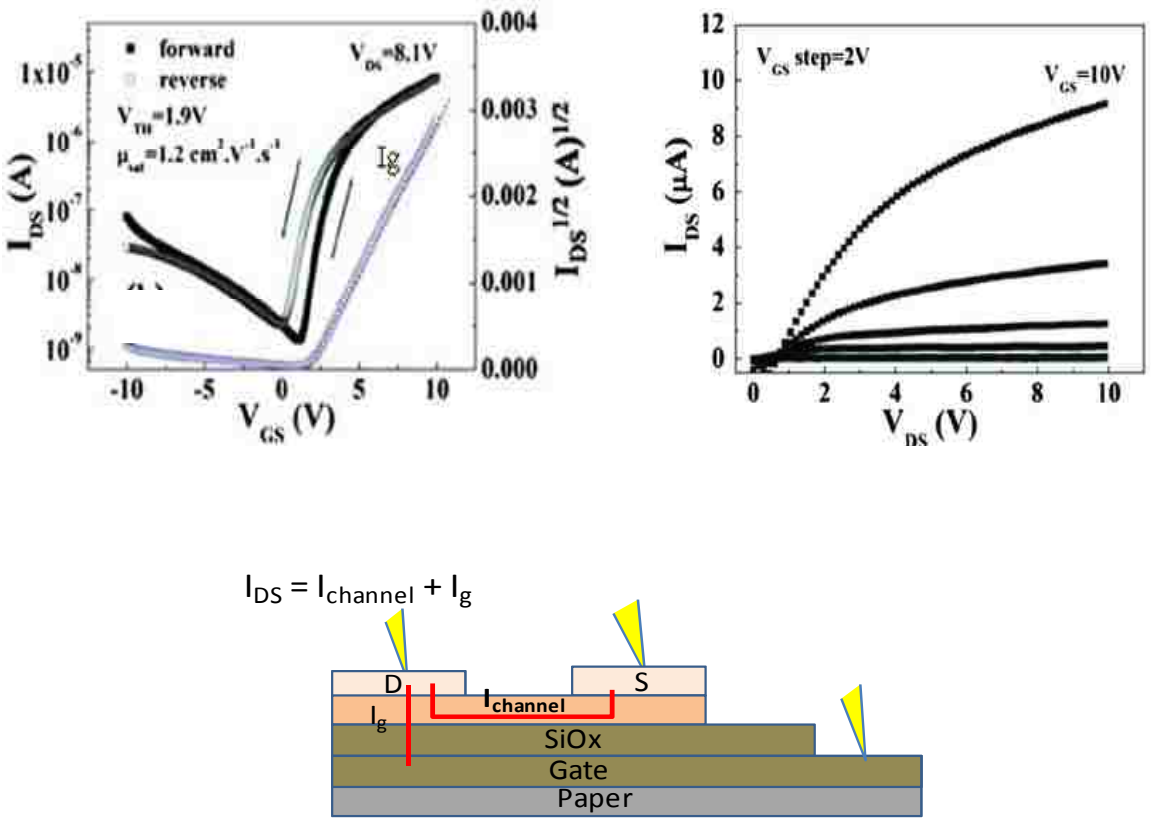


Fig. 3.2 Transfer and output characteristics of InGaZnO4-based TFTs fabricated on a paper substrate [Adapted from Ref. 11]

In order to improve device characteristics and process stability, polymer gate dielectric has been investigated in this study. Fluoropolymer (CYTOP), polyvinylphenol (PVP), and poly methyl methacrylate (PMMA) are known as the successful gate dielectric of organic TFTs in another study [13]; and methyl-siloxane based dielectric (Spin-on-glass (SOG) from Honeywell), which contained 15 wt% CH_3 (methyl) groups bonded to Si atoms in the Si-O backbone as illustrated in figure 3.3, is known to have high crack resistance, excellent planarization effect, as well as strong chemical resistance

[14]. In this study, both SOG and PMMA were initially evaluated as possible dielectrics. SOG cured at150ºC for 3hrs was stable in all chemicals used in TFT process but PMMA was dissolved in stripper and EBR solvent, as summarized in Table 3.2.

Table 3.2 Chemical stability of SOG and PMMA.

Polymer	Stripper (10min)	Developer (5min)	EBR (5min)	DI:HCl=20:1 (10min)	Acetone (10min)
Methly siloxane	O	O	O	O	O
PMMA	X	O	X	O	O

(O: stable, X: dissolved)

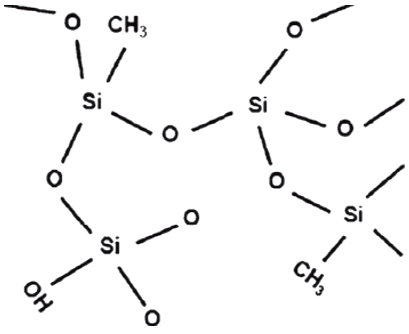


Fig. 3.3 Chemical structure of SOG.

In low temperature dielectric, the gate leakage current is a main issue. Thus understanding dielectric leakage current is essential to develop a new dielectric. Gate leakage current can be interpreted by several mechanisms such as Schottky emission, hopping, Fowler Nordheim Tunneling, and Poole-Frenkel effect [15]. DC conduction in a dielectric can be mainly interpreted by Schottky emission and Poole Frenkel effect. In Schottky emission, the presence of an electric field at the barrier modifies the emission

current as it reduces the potential barrier between the two materials [16]. In Poole-Frenkel effect, the insulator can conduct electricity by electric field that enhances the excitation of electrons trapped in localized states into the insulator conduction band [17]. Poole Frenkel results from lowering of the potential barrier at donor-like sites under an applied electric field. Schottky and Poole Frenkel emission are expressed by [18],

$$\text{Schottky emission: } J = AT^2 \exp\left(\frac{q}{kT}\sqrt{\frac{qE}{4\pi\varepsilon_o\varepsilon}} - \frac{q\Phi_s}{kT}\right) \tag{3.1}$$

$$\text{Poole-Frenkel emission: } J = BE \exp\left(\frac{q}{kT}\sqrt{\frac{qE}{\pi\varepsilon_o\varepsilon}} - \frac{q\Phi_{PF}}{kT}\right) \tag{3.2}$$

where J the current density, A and B are constant, E, $q, \Phi_s, \Phi_{PF}, \varepsilon, \varepsilon_o, k$, *and* T are applied electric field, electronic charge, barrier height for the injecting electrons (Schottky emission), voltage barrier (in zero applied electric field), permittivity, permittivity in vacuum, Boltzmann constant, and temperature, respectively.

If Schottky emission is dominant, the ln(J) vs. $E^{1/2}$ plot shows a straight line, while when Poole-Frenkel emission is the main mechanism, the ln(J/E) vs. $E^{1/2}$ plot shows a straight line. Figure 3.4 shows the plotted ln(J/E) vs. $E^{1/2}$ of SOG insulator. The dominant conduction mechanism in this field range is considered to be a Poole-Frenkel emission.

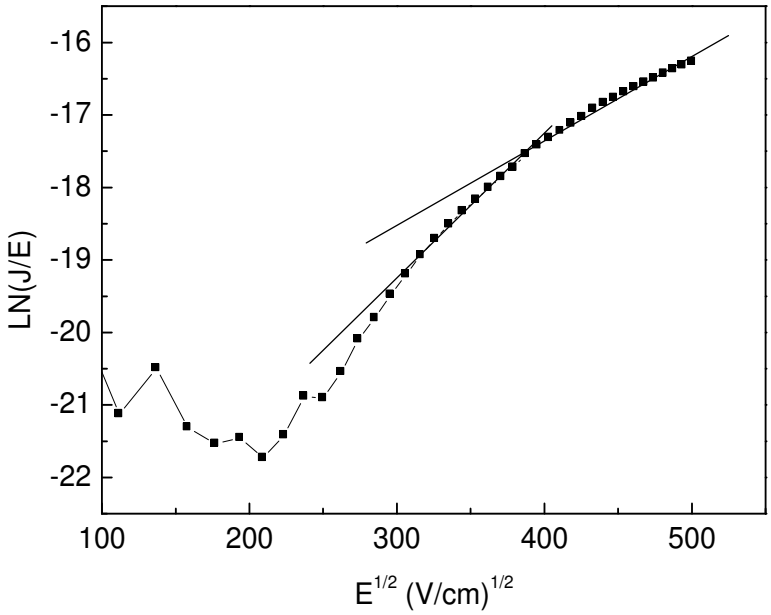


Fig. 3.4 The logarithmic current density over electric field vs. electric field$^{1/2}$ (Poole-Frenkel emission) for 600nm thick SOG insulator.

3.3 Fabrication of a-IGZO TFT on paper substrate

In this work, HP inkjet printable photo paper (coated paper) with the roughness of 8.4nm was used as the substrate for a-IGZO TFT fabrication. From a 210 mm by 297 mm square paper sheet, 50mm by 50mm was simply cut by using scissors. The inkjet printable photo paper presents relatively smooth surface than other paper candidates and the rear side of it is anti-absorbing due to a polyethylene coating. Top side of this paper usually has an inkjet receptive coating designed to absorb ink quickly, so it also absorbs water and solvents during TFT process. In order to prevent any absorption and improve surface roughness, 3μm thick epoxy acrylate copolymer (AC-818KL from Kolon Chemical) that has been used as planarization material in LCD was coated on top side of

the paper and followed by curing at 150ºC for 1 hr. Then 100nm thick SiO_2 was deposited in sputter at room temperature to prevent outgassing from planarization layer. Two different gate dielectrics were compared; a) low temperature PECVD deposited SiO_2, and b) methyl siloxane based dielectric. Bottom gate inverted staggered a-IGZO TFTs having PECVD SiO_2 dielectric were first fabricated on the planarized paper. AlNd/Mo double layer as gate and source-drain electrodes were patterned by liftoff process. AlNd plays a role in low resistivity electrode and Mo prevents the formation of Al_2O_3 on AlNd surface. 200 nm thick SiO_2 deposited with a rate of 4.8nm/min at 140°C by PECVD was used as gate dielectric. Cracks were observed on the entire substrate after SiO_2 deposition as shown in figure 3.6 (a). These cracks are attributed to thermal expansion mismatch between organic planarization layer and SiO_2 because one side coated paper substrate by organic layer is heated up during PECVD process, so it bends, and then the expanded organic layer tries to recover during cooling in contrast with SiO_2 trying to maintain its dimension. We used double side adhesive film that is designed to bond and debond flexible substrate on carrier substrate, to restrict the expansion of organic layer on paper substrate. The adhesive films consist of a centered PI film and adhesive layers at double side. A strong adhesive is stuck on a carrier substrate and a paper substrate is bonded on a weak adhesive side by a laminator as shown in figure 3.5. This approach withstands up to approximately 200°C and is stable in photolithography chemicals.

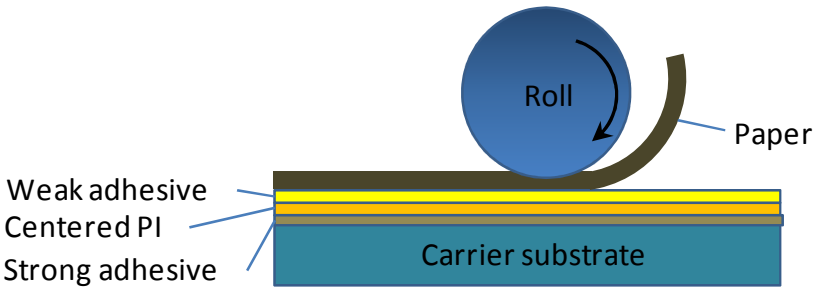


Fig. 3.5 Bonding & debonding process using double side adhesive film.

By using this approach, we finally reduced cracking as shown in figure 3.6 (b). 60 nm thick a-IGZO film as active semiconductor layer was deposited by RF magnetron sputtering at room temperature in Ar and O_2 ambient. The carrier concentration in optimized a-IGZO films was around 10^{17} cm^{-3}. After source-drain process, TFTs were annealed in nitrogen ambient at 100ºC for 1 hr. The leakage current (Ig) of the SiO_2 deposited at 140ºC is too high as discussed in the following chapter. Therefore, in order to reduce the gate leakage current and improve device performance, polymer dielectrics were investigated. Methyl-siloxane based dielectric (Spin-on-glass (SOG) from Honeywell) was selected since it contains the Si-O backbone with a chemical structure very much akin to that of SiO_2. SOG polymer was filtered and spun coated on gate electrode. The thickness of the gate dielectric was carefully controlled to be around 600 nm. After curing at 140°C for 2.5 hr, no obvious cracks were observed unlike ones on PECVD SiO_2 dielectric. All other processes were exactly same as those of a-IGZO TFTs with PECVD SiO_2 dielectric. Figure 3.7 (a) shows a schematic cross section of fabricated a-IGZO TFT, and figure 3.7 (b) is a photograph of a-IGZO TFT array using methyl-

siloxane based gate dielectric on paper substrate. Detailed process condition is described in Appendix B.

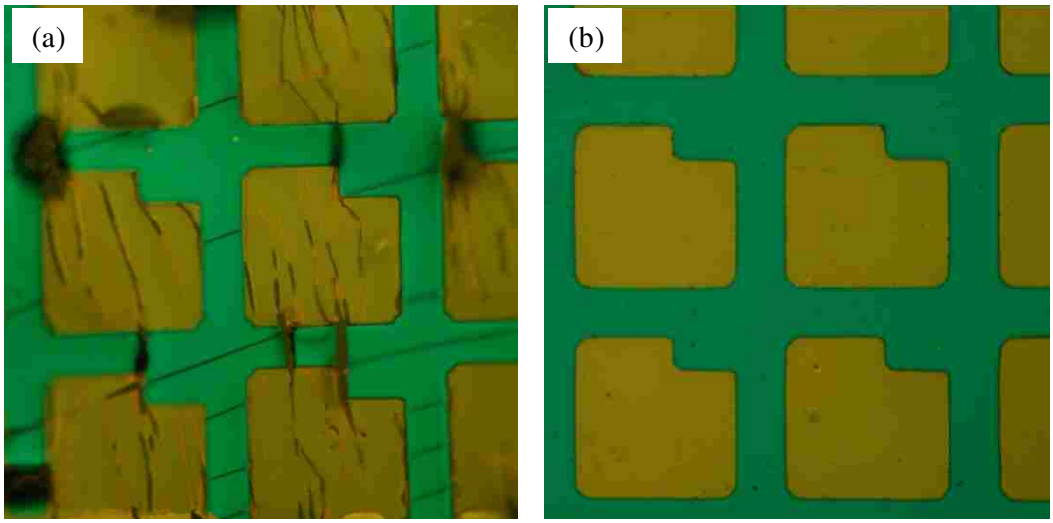
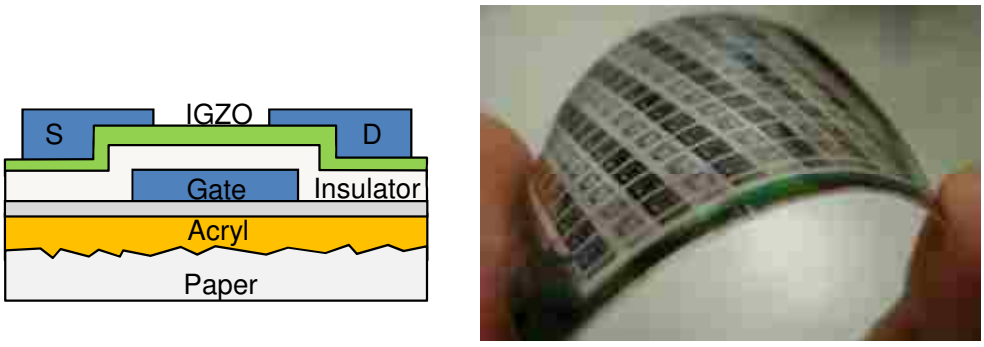


Fig. 3.6 Optical micrograph of the patterns on a paper substrate after PECVD SiO_2 deposition (a) paper substrate without bonding on carrier substrate, (b) paper substrate bonded on carrier substrate by the adhesive film.



(a) (b)

Fig. 3.7 (a) Schematic cross section of the fabricated a-IGZO TFT and (b) photograph of a-IGZO TFT array with methyl siloxane based gate dielectric on the planarized paper.

3.4 Electrical characterization techniques of TFT

In this chapter, basic techniques of electrical characterization of TFT are introduced. Field effect mobility, threshold voltage, subthreshold swing, interface trap density, and output characteristics are fundamental parameter to evaluate the TFT device.

3.4.1 Mobility & threshold voltage

Mobility characterizes how quickly carriers such as electron and hole move through a semiconductor by an applied electric field. There are two methods to determine the mobility of MOS transistor; one is saturation mobility and the other is field effect mobility. The field effect mobility is determined by the transconductance, $g_m = \partial I_D / \partial V_{GS}$. For MOS transistor, the drain current can be defined by [19]

$$I_D = \frac{W}{L}\mu_{eff} C_i (V_{GS} - V_T) V_{DS} \tag{3.3}$$

When the field effect mobility is determined, the transconductance is expressed as

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{W}{L}\mu_{eff} C_i V_{DS} \qquad (V_{DS}\text{: constant}) \tag{3.4}$$

When this expression is solved for the mobility, the field effect mobility μ_{FE} is given by

$$\mu_{FE} = \frac{L g_m}{W C_i V_{DS}} \tag{3.5}$$

Figure 3.8 shows the transfer and field effect mobility curve of n-channel a-IGZO TFT (V_{DS}=1V, C_i =1.33E-8F/cm^2) with 600nm thick SOG gate dielectric. The mobility curve are only representative when V_{GS}-V_T is greater than V_{DS}.

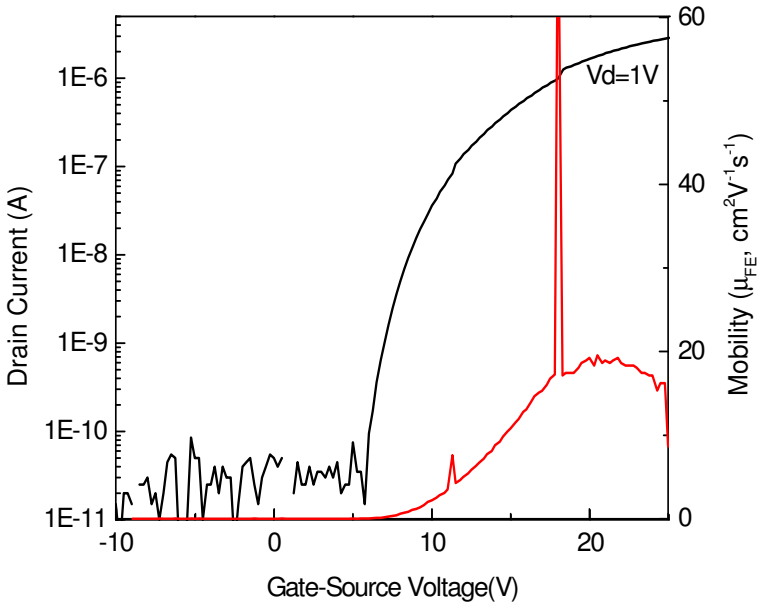


Fig. 3.8 Transfer and field effect mobility curve of a-IGZO TFT with 600nm thick SOG gate dielectric on paper substrate; W/L=30µm/30µm.

The saturation mobility is derived from the drain current with the device in saturation. The drain current in MOSFET saturation regime can be written as

$$I_{D,sat} = \frac{mW}{L}\mu_{eff}C_i(V_{GS} - V_T)^2 \tag{3.6}$$

Where *m* is a function of doping density; it approaches 0.5 for low doping densities. When Eq. (3.6) is solved for mobility, the saturation mobility is defined by

$$\mu_{sat} = \frac{2L}{WC_i}\left[\frac{d\sqrt{I_D}}{dV}\right]^2 \tag{3.7}$$

Figure 3.9 shows the transfer and saturation mobility curve of n-channel a-IGZO TFT (V_{DS}=15V, C_i =1.33E-8F/cm^2) with 600nm thick SOG gate dielectric. The mobility curve are only representative when V_{DS} is greater than V_{GS}-V_T.

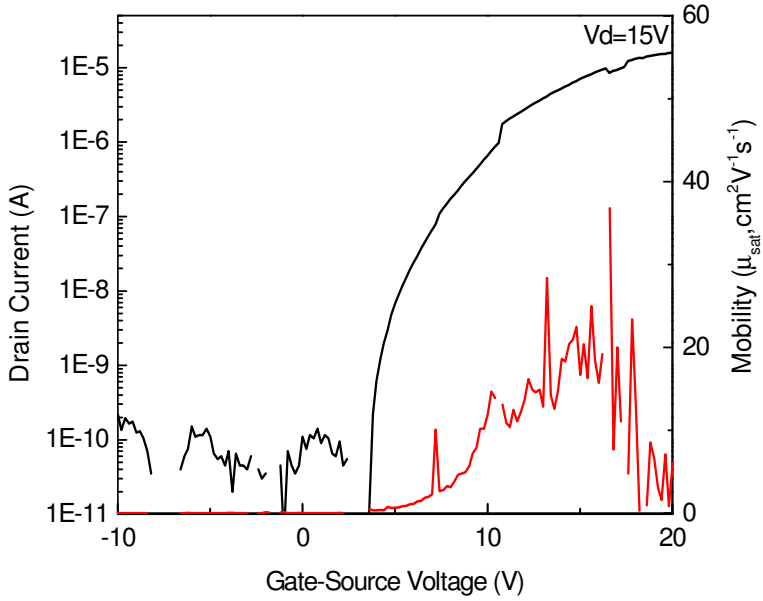


Fig. 3.9 Transfer and saturation mobility curve of a-IGZO TFT with 600nm thick SOG dielectric on paper substrate; W/L=30μm/30μm.

The saturation extrapolation technique was used to measure the threshold voltage. V_T is determined by plotting $I_D^{1/2}$ versus V_{GS} through extrapolating the curve to zero drain current at the point of maximum slope. Setting V_{GS}=V_{DS} ensures operation in the saturation region. Figure 3.10 shows the V_T determination of a-IGZO TFT on paper substrate. V_T of a-IGZO TFT with 600nm thick SOG gate dielectric is approximately 5V.

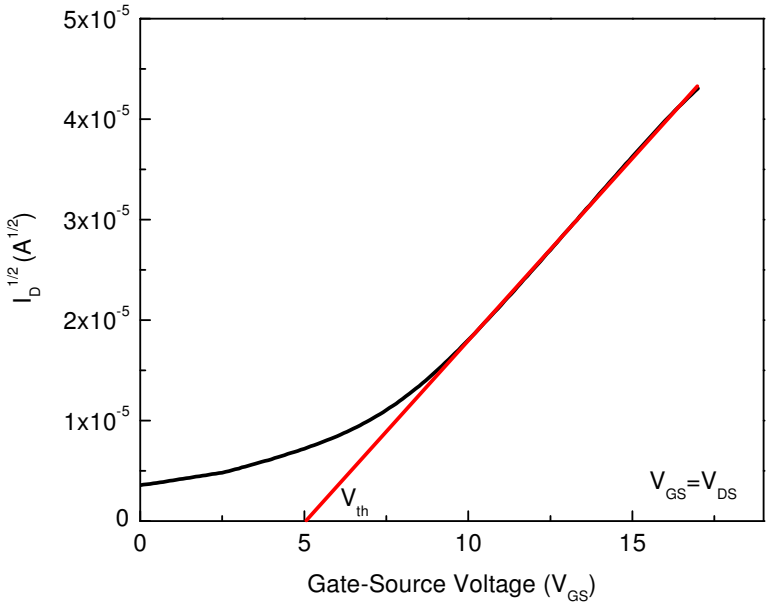


Fig. 3.10 Threshold voltage determination of a-IGZO TFT by the saturation extrapolation technique (600nm thick SOG dielectric, W/L=30μm/30μm).

3.4.2 Subthreshold swing and interface trap density

Subthreshold swing is the gate voltage required to change the drain current by one decade, and is expressed by

$$S = \frac{dV_{gs}}{d(\log I_{ds})} \tag{3.8}$$

A plot of $\log(I_{ds})$ versus V_{gs} with fixed V_{ds}, exhibits approximately linear behavior in the $V_{gs} < V_T$ region. Its slope is the subthreshold slope. The inverse of this slope is usually referred to as subthreshold swing (S), given in units (mV/decade). A small value of S denotes that a small change of gate bias can alter the drain current significantly. The

smaller value of S presents the better switching transistor. In addition interface trap density (N_{it}) can be calculated by the following equation from subthreshold swing [20],

$$N_{it} = [S \log e/(kT/q) - 1]Ci/q \quad (3.9)$$

where S is subthreshold swing, k is Boltzmann constant, T is temperature, C_i is the capacitance per unit area of gate dielectric, and q is the unit charge.

3.4.3 Output characteristics

The output characteristics of the device is obtained by plotting the drain current I_D versus drain voltage for several value of gate voltage (Vgs). For $V_D < (V_G - V_T)$, the transistor is operated in linear region since the drain current increases linearly with the drain voltage; the drain current in the linear region is given by equation 3.3. For $V_D > V_G - V_T$, the drain current does not increase with the drain voltage so the saturated portion becomes flat in output curve. This flat portion defines saturation region; the drain current in the saturation region is then given by equation 3.6.

3.5 Electrical characteristics of a-IGZO TFT on paper

Electrical characterization was done by using HP 4145B semiconductor parameter analyzer. High frequency (1MHz) Capacitance-Voltage (C-V) measurement was performed to characterize the gate dielectrics. Figure 3.11 shows the transfer characteristic of a-IGZO TFTs with SiO_2 gate dielectric deposited at 140°C on the planarized paper. a-IGZO TFTs with SiO_2 gate dielectric in device dimensions of 40 µm width and 8 µm channel length demonstrates the field effect mobility of ~6 $cm^2\ V^{-1}s^{-1}$,

on/off current ratio of ~10^4, threshold voltage of ~2V, and subthreshold swing of ~1 V/decade. The leakage current (Ig) of the low temperature SiO_2 is too high as shown in Figure 3.11. This high gate leakage current not only affects off and on current level of resulting transfer curve of TFTs but also make a device unstable. The capacitance of the 200nm thick SiO_2 is approximately 70 nF/cm^2, providing an effective k value of 16 that is higher than the known 3.9. The high dielectric constant results from the low temperature (140°C) deposition of PECVD, and similar results were reported in another study [21].

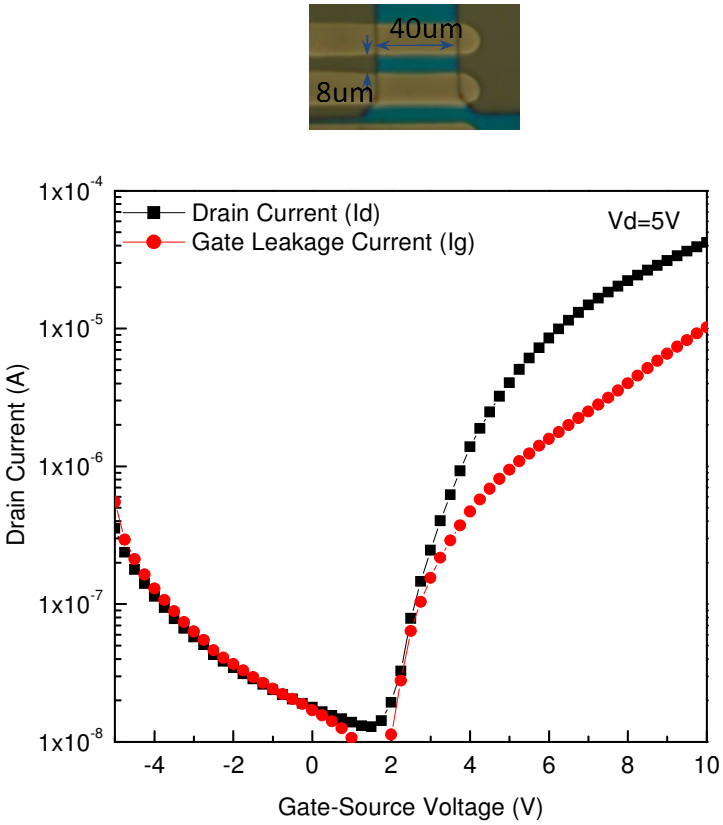


Fig. 3.11 Transfer characteristics and gate leakage current of a-IGZO TFT with low temperature (140°C) 200nm thick SiO_2 on the planarized paper substrate.

IGZO TFTs having methyl siloxane based gate dielectric was developed in order to reduce the gate leakage current and improve device stability. The initial measurement of a-IGZO TFTs having SOG gate dielectric was unstable and showed high gate leakage current when plotted as initial_Ig in figure 3.12, even though it was lower than that of the SiO_2 in figure 3.11. The leakage current of methyl siloxane based dielectric can be interpreted by hopping effect. It has been suggested that silanol (Si-OH) group can provide trap sites which electrons are trapped to form a SiO^- [22]. Insulator can conduct electricity by field enhanced excitation of electrons trapped in localized states into the insulator conduction band [17]. Thus, current can flow due to hopping from trap to trap in the presence of electric field. Through a heat treatment, methyl siloxane based dielectric is condensed, so its silanol groups, which are suggested as a trap site, gradually decrease and Si-O-Si bond increase [14, 23]. In order to reduce the trap sites of dielectric, we annealed the device in nitrogen ambient at 150°C, restricted by paper substrate, for 2 hr after initial measurement. Gate leakage current (Ig) was significantly reduced and all extracted TFT parameters show improved electrical properties as shown figure 3.11 and Table 3.3. Ig is compared when V_{GS} is 10V for convenience. We believe that the gate leakage current is mainly improved by decreasing internal trap sites of dielectric, and the high mobility and low subthreshold slope are attributed to low interface trap density when compared to the low temperature SiO_2. Interface trap density (N_{it}) was calculated by using subthreshold swing. N_{it} of a-IGZO TFT with 140ºC SiO_2 is $7\times10^{12}/cm^2$, and that of methyl siloxane based dielectric shows the lower interface trap density of $4.7\times10^{11}/cm^2$. Unlike methyl siloxane based dielectric, 150°C annealing didn't improve

the leakage current of SiO_2 due to different leakage current sources. SiO_2 deposited at low temperature is known to show unstable barrier, high interface trap density and very low charge to breakdown [14, 21].

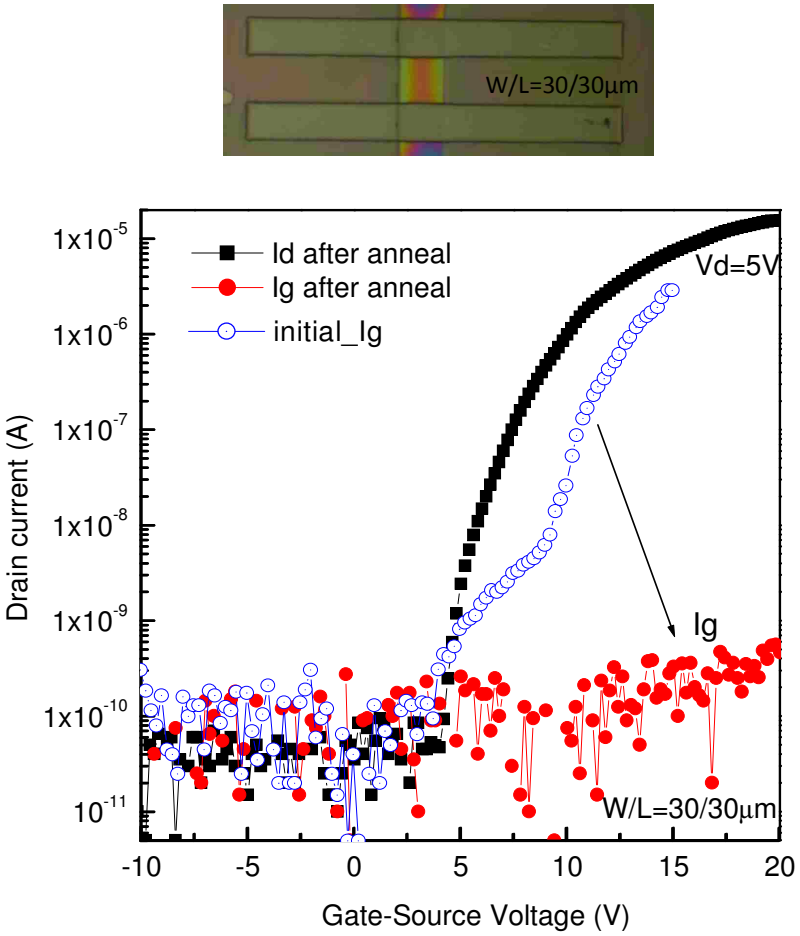


Fig. 3.12 Transfer characteristics and gate leakage current of a-IGZO TFT methyl siloxane gate dielectric on planarized paper substrate.

Table 3.3 summarizes the electrical properties of a-IGZO TFTs with the SiO_2 and methyl siloxane based dielectric, respectively, on paper substrate. These results suggest that

methyl-siloxane based dielectric can be a suitable candidate for a-IGZO TFTs on paper substrate.

Table 3.3 Electrical properties of a-IGZO TFTs on paper substrate

Dielectric	μ_{FE} ($cm^2V^{-1}s^{-1}$)	μ_{sat} ($cm^2V^{-1}s^{-1}$)	Vth (V)	S.S. (V /dec)	I_{on}/I_{off}	Nit ($/cm^2$)	Ig (at Vg=10V, mA/cm^2)
SiO_2	~6	-	2.2	~1	~10^4	7x10^{12}	1590
Methyl Siloxane	~20	20~22	5	~0.4	~10^6	4.7x10^{11}	0.01

Figure 3.13 and 3.14 present the output characteristics of a-IGZO TFT with SiO_2 deposited at 140ºC and SOG cured at 140ºC for 2.5hrs respectively at various gate voltages. In figure 3.13, initial drain current is high at even zero drain voltage because the drain current originates from the gate leakage current of poor SiO_2. Therefore, initial drain current at zero drain voltage increases gradually according to the growth of gate voltage. Figure 3.14 shows small current crowding in low drain current zone. In general, current crowding derives from the increase of contact resistance between semiconductor and metal. In this case, however, it is likely to originate from dipole groups inside SOG dielectric which can be slowly reoriented by an applied electric field, and also gate leakage current. Output characteristics of a-IGZO TFT with SOG dielectric cured at 150°C for 3hrs and post-annealed for 1hrs at 150°C shows the improved characteristics in figure 3.15.

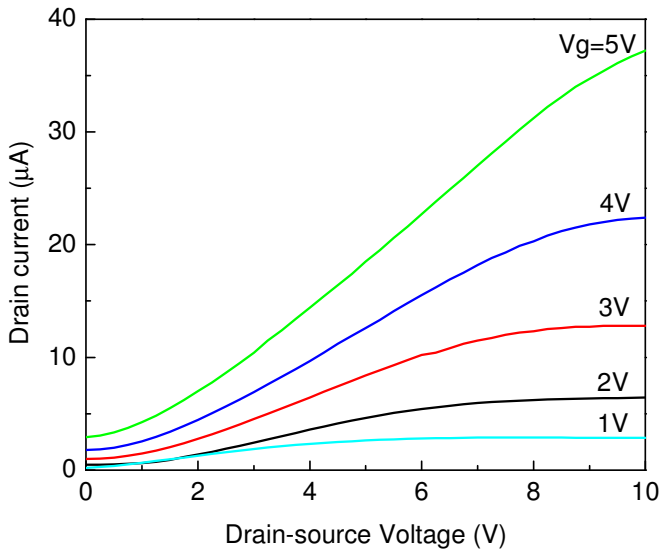


Fig. 3.13 Output characteristics of n-channel a-IGZO TFT with W/L=40μm/8μm. Gate dielectric is 200nm thick SiO_2 deposited at 140°C.

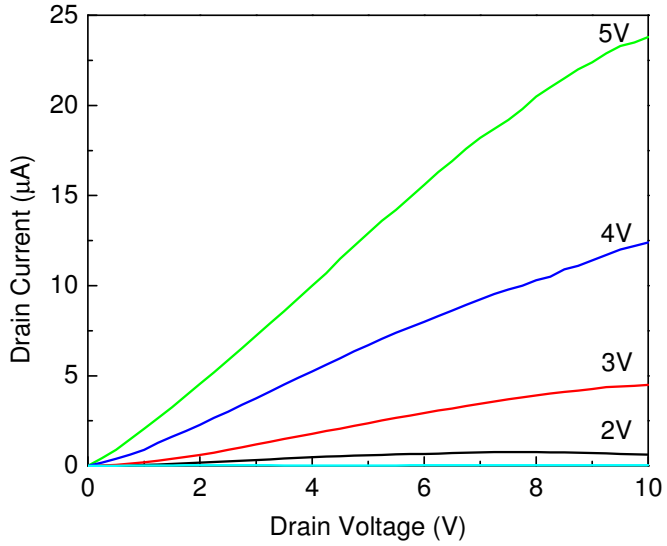


Fig. 3.14 Output characteristics of n-channel a-IGZO TFT with W/L=30μm/30μm. Gate dielectric is 600nm thick SOG cured at 140°C for 2.5hrs.

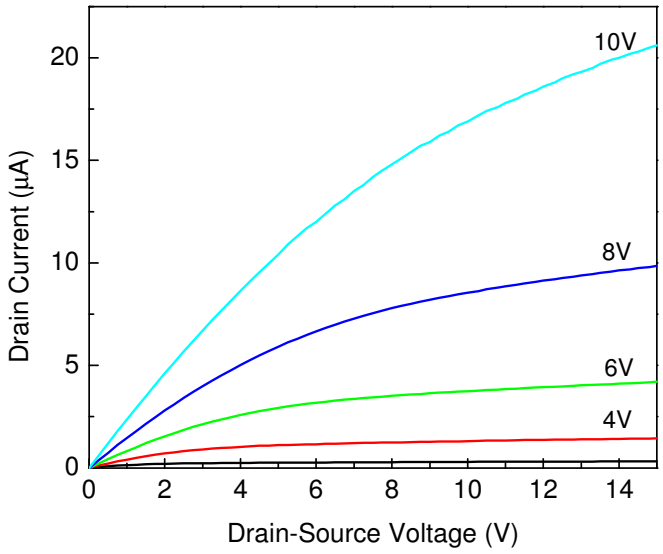


Fig. 3.15 Output characteristics of n-channel a-IGZO TFT with W/L=8μm/8μm. The device was fabricated on oxidized Si wafer and gate dielectric was 600nm thick SOG cured at 150°C for 3hr. After fabrication, post annealing was performed at150°C for 1hrs.

3.6 Electrical characteristics of methyl siloxane gate dielectric

3.6.1 Thickness effect

In order to investigate the thickness effect of methyl siloxane dielectric (SOG), transfer curve and Ig of 600nm thick SOG are compared with those of 170nm in figure 3.16. SOG was diluted by 2ml IPA and 1ml acetone to control the thickness, as shown in figure 3.17. The thickness reduction shifts threshold voltage to negative direction, but Ig is unchanged and it remains equally low to the thick SOG at the same annealing condition. From the output characteristics in figure 3.18, thin gate dielectric tends to increase drain current compared to thick dielectric. This result is attributed to the increase of capacitance and the decrease of threshold voltage in Eq. (3.3). For the investigation of

dielectric strength, breakdown voltage was measured in both 170nm and 600nm thick SOG with metal-insulator-metal (MIM) structure. Both were post-annealed at 150ºC for 4hrs. In figure 3.19, the 170nm thick SOG is partially conductive because of residual silanol (Si-OH) group that provides trap sites (explained in chapter 3.5), and then breakdowns at 2.3MV/cm. The 600nm thick SOG exhibits lower leakage current and it doesn't breakdown under the allowed maximum voltage of 40V in HP4145 analyzer.

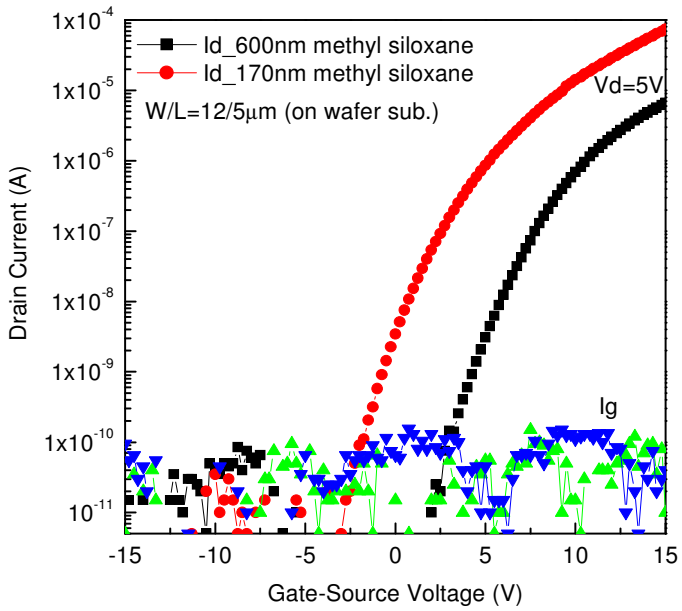


Fig. 3.16 Transfer curve of a-IGZO TFT according to the thickness variation of methyl-siloxane (SOG). The devices were fabricated on oxidized Si wafer. SOG dielectric was cured at 150°C for 3hrs and post-annealed at150°C for 2hrs after fabrication.

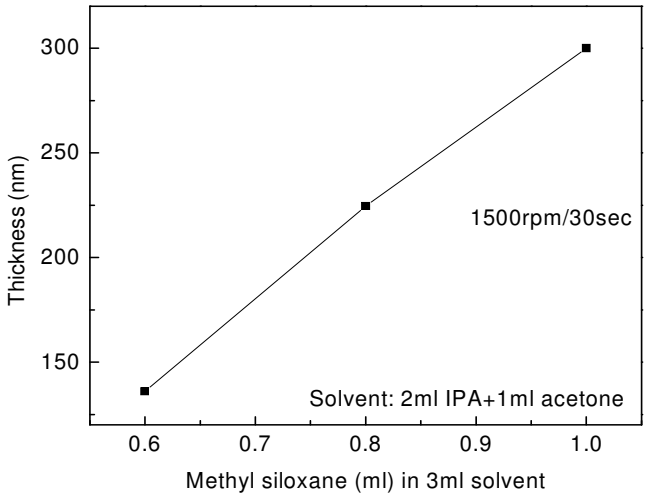


Fig. 3.17 Thickness variation according to the amount of SOG in 2ml IPA and 1ml acetone.

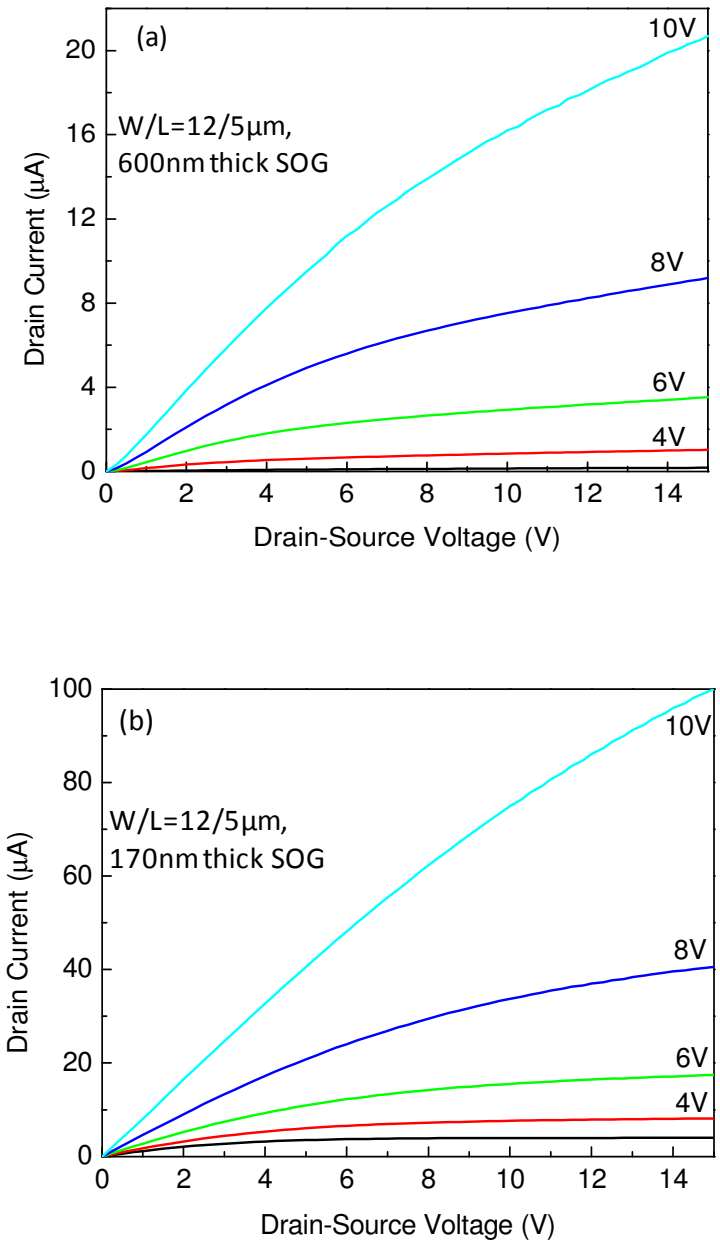


Fig. 3.18 Output characteristics of a-IGZO TFT according to the thickness variation of methyl-siloxane (SOG). The devices were fabricated on oxidized Si wafer. SOG dielectric was cured at 150°C for 3hrs and post-annealed at150°C for 2hrs after fabrication.

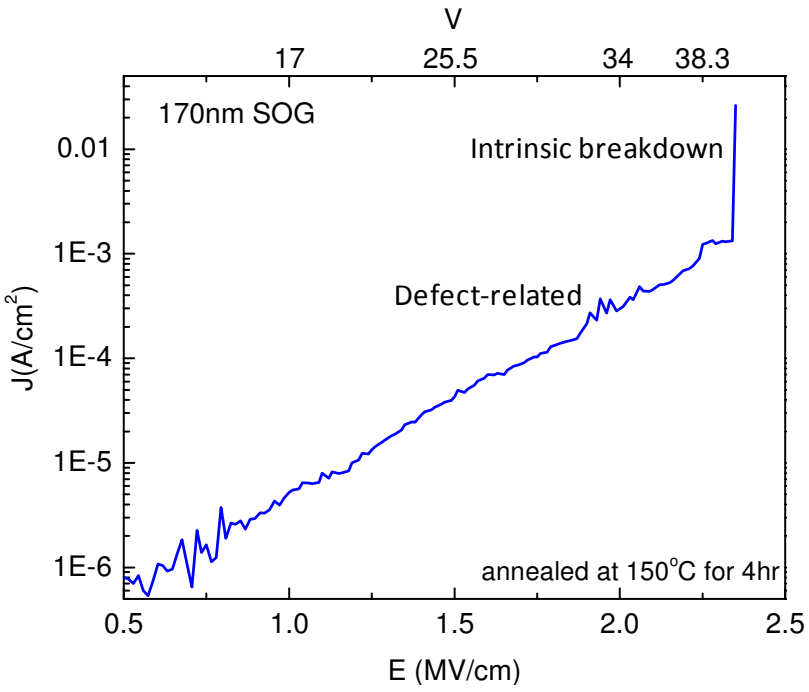


Fig. 3.19 J-E curve of 170nm thick SOG annealed at 150°C for 4hr.

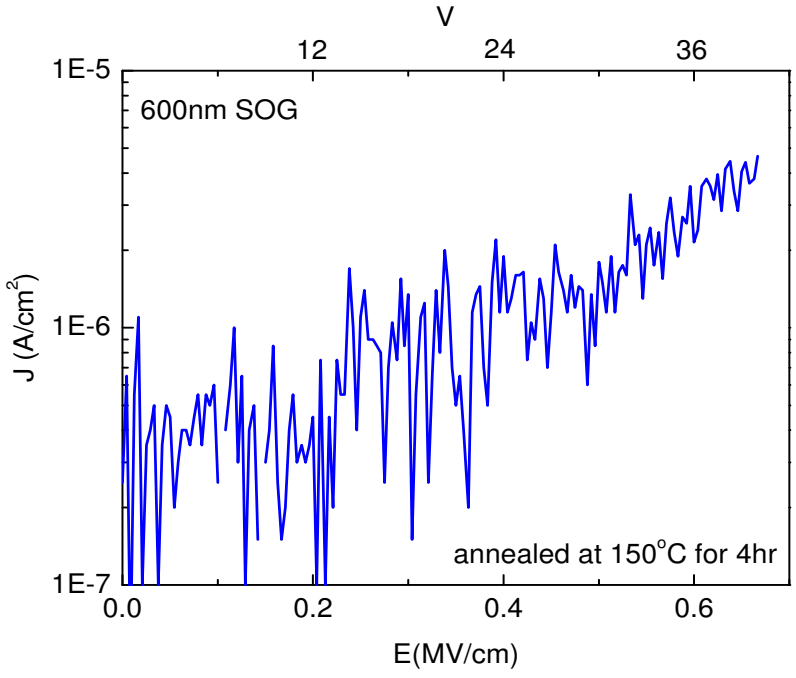


Fig. 3.20 J-E curve of 600nm thick SOG annealed at 150°C for 4hr.

3.6.2 Annealing effect

In section 3.5, after the spin coating of methyl siloxane (SOG) dielectric on gate electrode, it is cured at 140°C for 2.5hr and then post-annealing step at 150°C for 2hr in N_2 ambient is necessary to reduce the gate leakage current of a-IGZO TFT on paper substrate. In this section, it is investigated how the curing condition of SOG and post-annealing affect the property of gate dielectric and TFT device. The leakage current of 600nm thick SOG with different annealing conditions is compared by using MIM structure with the area of $10^4 \mu m^2$. Slightly longer time and higher temperature of curing are effective to attain the low leakage current in J-V curve of figure 3.21. Curing condition of 150°C/3hr shows much lower leakage current than 140°C/2.5hr curing, and the additional post-annealing doesn't change the leakage current level of 600nm thick SOG. Nevertheless we need post-annealing not only to decrease the leakage current of gate dielectric but also to obtain the uniform steady device characteristics. Post annealing generally stabilize the a-IGZO device through the reduction of interfacial traps and defect sites [24]. Particularly in case of SOG dielectric in this study, post annealing can reduce the amount of dipole that affects device stability.

Figure 3.22 presents the transfer curve of a-IGZO after 1hr and 2hrs post-annealing at 150ºC. Transfer curve is slightly enhanced according to the increase of annealing time; explicitly the subthreshold swing decreases from 1.4 to 1. The longer annealing time of 4hrs doesn't alter the transfer characteristics.

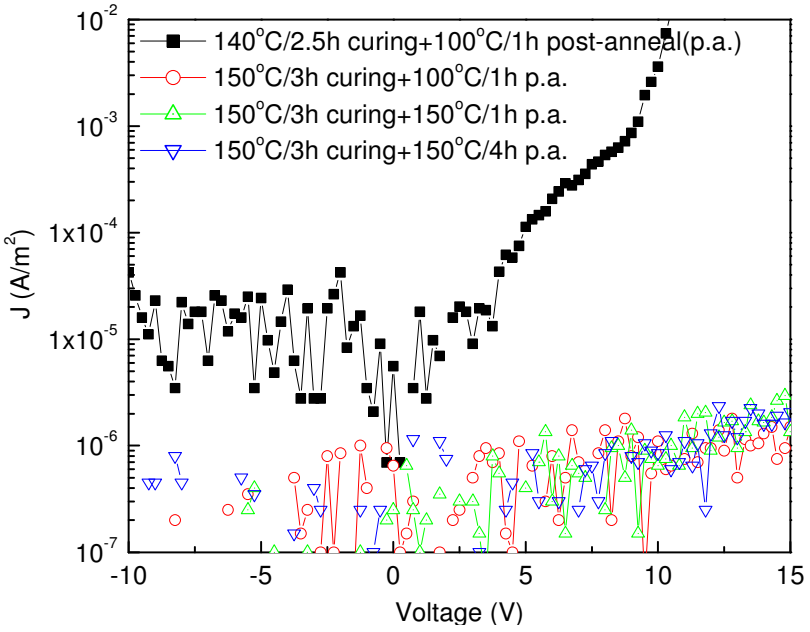


Fig. 3.21 J-V characteristics of 600nm thick methyl siloxane in Metal-Insulator-Metal structure according to thermal budget.

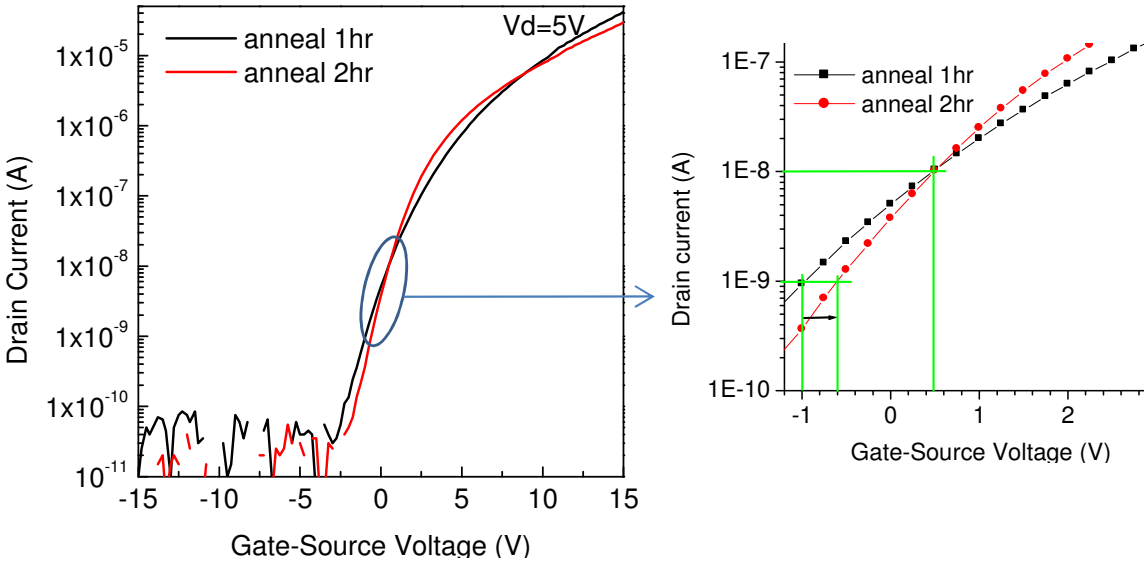


Fig. 3.22 Transfer characteristic according to annealing time; a-IGZO TFT with W/L=8 μm/8μm; 150nm thick methyl siloxane on oxidized wafer

Hysteresis characteristic of a-IGZO TFT with SOG gate dielectric is presented in figure 3.23. I-V curve is first measured forward direction from –V to +V, and then reversed from +V to –V. In case of a-IGZO TFT annealed at 150°C for 1hr, Vth shifts to the negative direction with approximately 10V. There are two mechanisms to explain the origin of hysteresis. One is often associated with the electrons trapped to hydroxyl groups (OH) at channel/dielectric interface. The other mechanism is related to dipole groups that exist in polymer dielectric materials as illustrated in figure 3.24, which can be slowly reoriented by an applied electric field. The recommended curing process of SOG (methyl siloxane based dielectric) is 350°C in literature review. In this study, the curing temperature of SOG is 140°C or 150°C due to the restriction of paper substrate. Therefore, it can be estimated that silanol (Si-OH) and hydroxyl (OH) groups inside the immaturely cured SOG induce residual dipole groups causing slow polarization in the bulk organic dielectric [25]. The longer annealing in figure 3.23 (b) offers smaller Vth shift of 6.5V, explaining that the residual dipolar groups are decreased by additional annealing process. Hysteresis induced by slow polarization should be dependent on the amount of dipolar groups in the bulk SOG dielectric, so thinner dielectric material reduces the dipole amount that affect device characteristics [26]. In addition, it is reported that low polarity material (mostly low-k) enhances the hysteresis and mobility characteristic of organic TFT [13]. In principle, we strongly believe that the low polarity material improves the device characteristics of a-IGZO TFT on paper substrate.

Propylene, ethylene, isobutylene, and fluoropolymer are applicable candidates for this application.

As a function of post-annealing time, the dielectric capacitance variation is measured by High frequency (1MHz) Capacitance-Voltage (C-V) in figure 3.25(a), and then the dielectric constant variation is calculated by

$$\varepsilon_r = \frac{C}{A} \cdot \frac{d}{\varepsilon_0} \tag{3.10}$$

Where ε_r is the dielectric constant, C is the capacitance, A is the area of overlap of the two plates, ε_0 is the vacuum permittivity ($\varepsilon_0 \approx 8.854\times10^{-14}$ F cm^{-1}), d is the distance between the plates.

The dielectric constant of 600nm thick SOG is relatively stable with annealing time in figure 3.25(b), but that of 170nm thick SOG is decreased by longer annealing time. Furthermore, the dielectric constant is altered by the variation of C-V measurement area. Compared to the dielectric constant of 7 in area of 4×10^{-4}cm^2, the area of 1×10^{-4}cm^2 exhibits the smaller dielectric constant of 3.3 that is similar to the original value of 3.2. This low dielectric constant is related to the amount of dipole that affects the magnitude of polarization achievable, which comprises the dielectric constant [27]. Materials with dipoles have larger dielectric constants than non-polar materials.

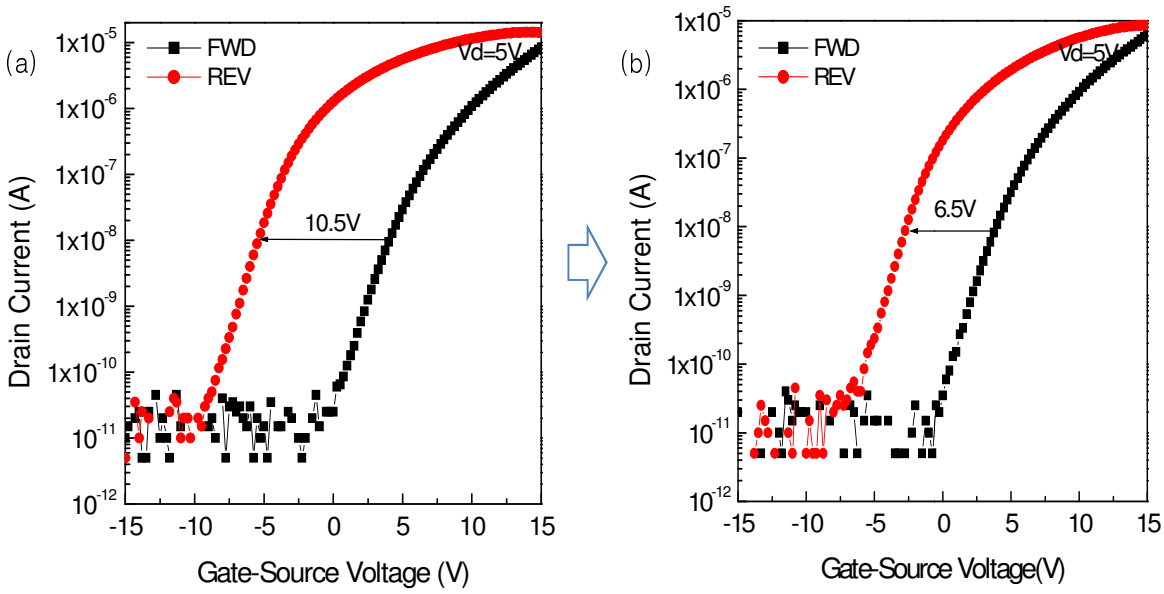


Fig. 3.23 Hysteresis characteristics of a-IGZO TFT after (a) 1hr and (b) 2hr post annealing at 150º; a-IGZO TFT with 170nm thick SOG gate dielectric on oxidized silicon wafer.

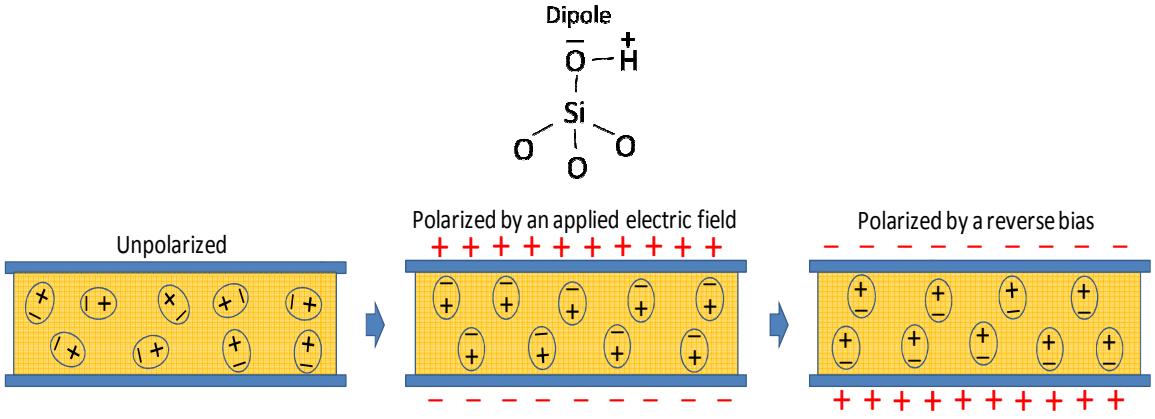
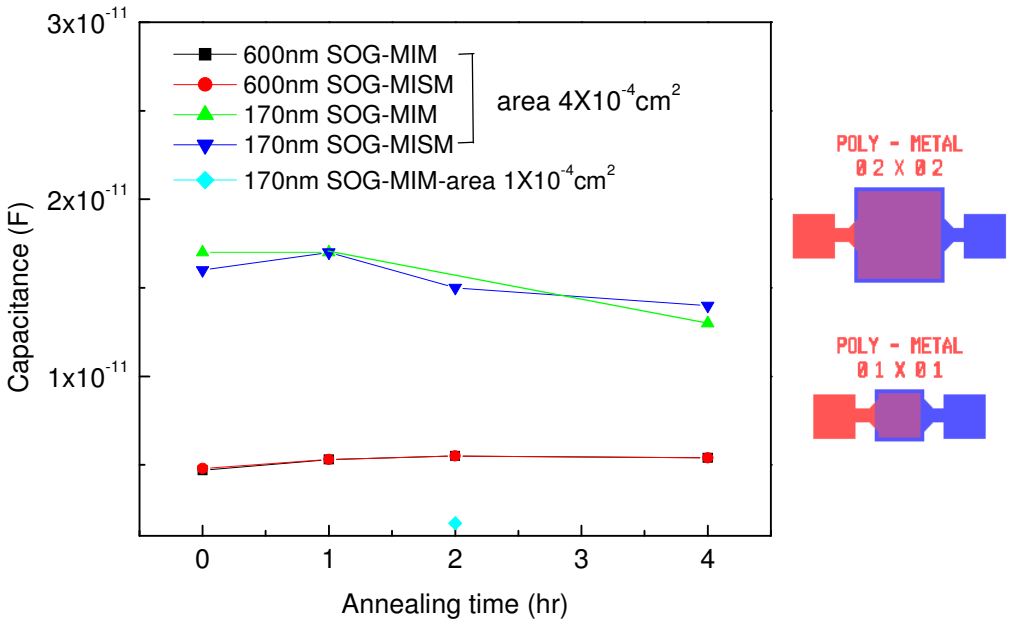
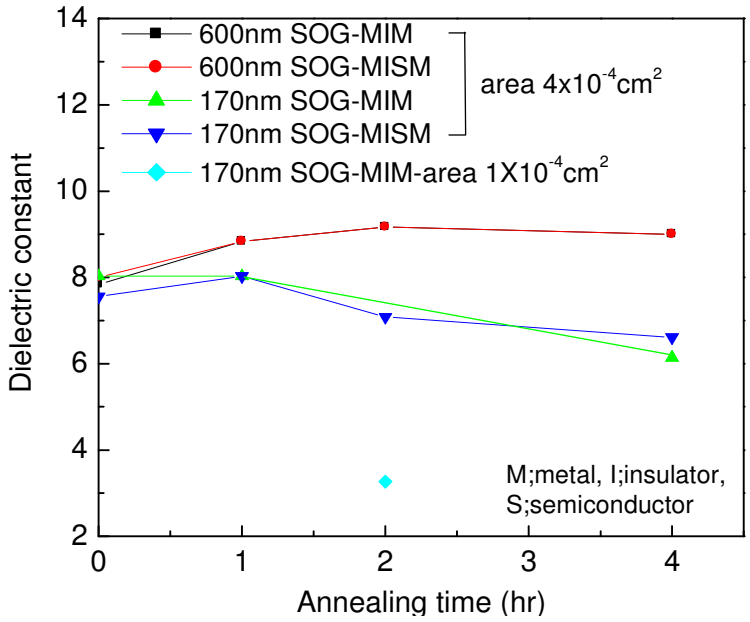


Fig. 3.24 Schematic of dipole polarization in organic dielectric.



(a)



(b)

Fig. 3.25 (a) Measured capacitance (b) calculated dielectric constant as a function of annealing time. Annealing temperature is 150°C.

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Chapter 4

P channel Cu_2O thin film transistor

In order to complement the n-channel a-IGZO TFTs for CMOS circuit architectures, p-channel oxide TFTs need to be developed. This study focuses on cuprous oxide (Cu_2O) as a promising material for p-channel TFTs. In this work, RF sputtering with 99.99% Cu_2O target has been used for the deposition of Cu_2O films instead of applying the reactive sputtering with pure Cu target. Deposition power, Ar partial pressure, and deposition temperature have been investigated as variable process parameters to achieve optimal growth conditions, and the properties of Cu_2O thin films were analyzed by optical bandgap, resistivity, Hall mobility, XPS, and TEM. Post-annealing (in air, nitrogen, and vacuum), plasma treatment (oxygen, N_2O, hydrogen), and reactive sputtering with oxygen and nitrogen have been performed to enhance the modulation characteristics of TFT. However, we have not obtained desired results. Nevertheless, it is validated that 1) the sputtered Cu_2O films are p-type with a poly-crystalline structure, 2) only a small modulation of Cu_2O TFT is observed due to the high conductivity of the prepared films, 3) Cu_2O is easily transformed to Cu (reduction) and

CuO (oxidation) by post-treatment, and 4) as-deposited Cu_2O film obtained by Cu_2O target includes Cu^{2+}. Despite the lack of satisfactory results of p-channel Cu_2O TFTs, significant progress was achieved on Cu_2O-IGZO P-N junction diode. Such devices were demonstrated on paper substrate thus showing potential for disposable electronics application.

4.1 Cu_2O TFT

The n-type property of metal oxide semiconductors including ZnO and IGZO originates from anion deficient, while the p-type property of metal oxide semiconductors is created by cation deficient. Few materials, as shown in Table 4.1, have been studied as p-type metal oxide semiconductor so far. Furthermore, the reported performances are inferior to those of n-channel a-IGZO TFTs. SnO is p-type with a Hall mobility of ~2$cm^2V^{-1}s^{-1}$. TFTs in SnO have been reported with a low field effect mobility of ~1 $cm^2V^{-1}s^{-1}$ and small on/off current ratio of 10^2 [1]. ZnO is a wide-bandgap n-type semiconductor due to oxygen vacancies. It has been reported that nitrogen-doped ZnO (ZnO:N) is p-type with a Hall mobility of 1~10 $cm^2V^{-1}s^{-1}$ [2]. However, TFTs with ZnO:N have not yet been realized. Copper oxides (Cu_2O, CuO) had been studied several decades ago and recently reevaluated as possible p-type semiconductors [3-6]. The p-type behavior of copper oxide stems from copper vacancies, which introduce acceptor level as illustrated in figure 4.1 [3]. The optical bandgap of Cu_2O, which has the cubic structure shown in figure 4.2, is 2.0~2.6eV, and its Hall mobility is reported to be approximately 100$cm^2V^{-1}s^{-1}$ [4, 5]. Zou et al. recently reported TFTs having saturation mobility of 4.3

$cm^2V^{-1}s^{-1}$ and $I_{on/off}$ of $3x10^6$, with polycrystalline Cu_2O using pulsed laser deposition (PLD) and high-k HfON gate dielectric [6]. These results are quite promising for the realization of p-channel metal oxide TFTs. However, the deposition temperature was too high (500°C), which is not suitable for low temperature substrates. Furthermore, the PLD process has several disadvantages, such as small area limited uniformity and target surface modification. In this study, we have investigated the sputtering method to deposit Cu_2O, which is easy to scale to large substrate sizes with good uniformity. Unlike previous reports, which used Cu as a target and utilized reactive sputtering to form the copper oxide, 99.99 % Cu_2O target have been used in order to achieve better stoichiometry.

Table 4.1 P-type oxide semiconductor materials

Materials	Hall mobility($cm^2 V^{-1}s^{-1}$)	Device properties
SnO [1]	~2.4	Mobility: 0.24~1.5$cm^2V^{-1}s^{-1}$, $I_{on/off}$:10^2
Cu_2O [4-6]	~100	Mobility:0.2~4.3$cm^2V^{-1}s^{-1}$, $I_{on/off}$:10^2~10^6
ZnO (doped) [2]	1~10	-
NiO [7]	<1	Mobility:1.6×$10^{-4}cm^2V^{-1}s^{-1}$, $I_{on/off}$:10^2

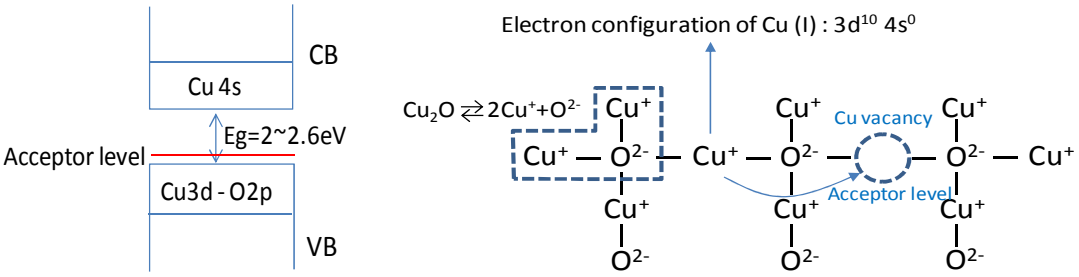


Fig. 4.1 Schematic energy-level structure and conduction mechanism for Cu_2O.

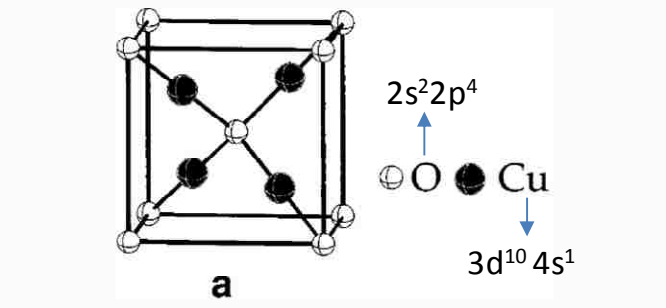


Fig. 4.2 Crystal structure Cu_2O [Adapted from Ref.4]

4.2 Properties of Cu_2O thin films

4.2.1 Optical bandgap

Absorbance and transmittance were measured by Cary 500 spectrophotometer to determine the optical bandgap energy of Cu_2O thin film. The optical bandgap energy (E_g) of the Cu_2O can be extracted by Tauc's plot from the optical absorption coefficient (α) [8].

$$\alpha h\nu = B\left(h\nu - E_g\right)^n, \text{ where } \alpha = \frac{A}{t_{eff} \times \log_{10} e} \tag{4.1}$$

where B is constant, h is Planck's constant (4.136×10^{-15}eV·s), v is the photon frequency, E_g is the optical band gap, t_{eff} is the film thickness, A is absorbance, and n=1/2 for direct bandgap.

The optical bandgap is determined from the intercept of the extrapolation of $(\alpha h\nu)^2$ versus $h\nu$. Figure 4.3 presents the $h\nu$ dependence of $(\alpha h\nu)^2$ according to deposition conditions including RF power, Ar gas flow rate, and temperature. The

calculated bandgap energies of Cu_2O range from 2.43eV to 2.58eV, which is consistent with the reported data, 2.0-2.6eV [4, 5]. Considering the margin of error, there is no distinct variation of bandgap according to deposition conditions. The color of deposited Cu_2O films is yellow for a thin layer and becomes darker for a thicker film as shown in figure 4.4.

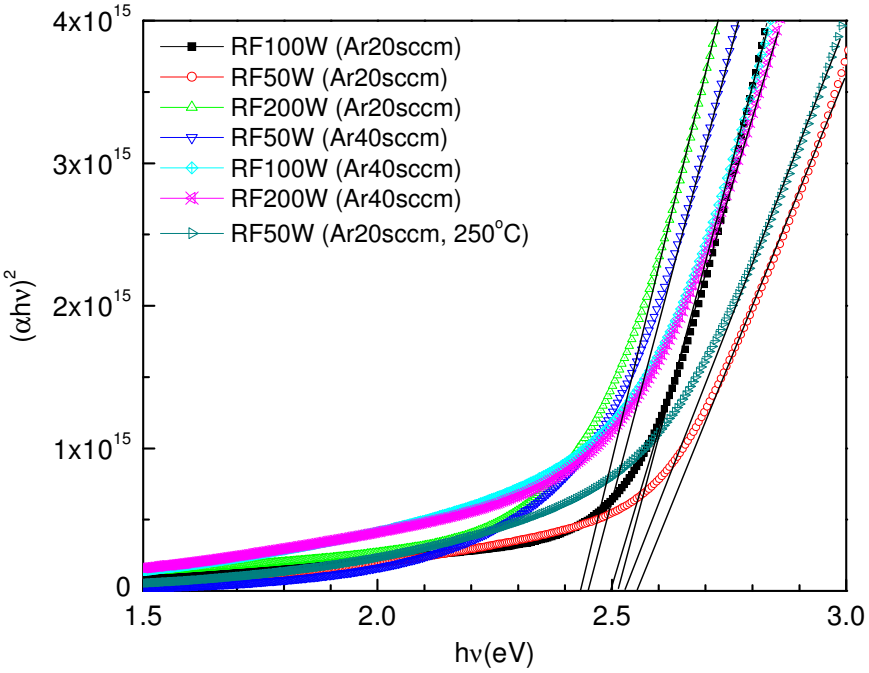
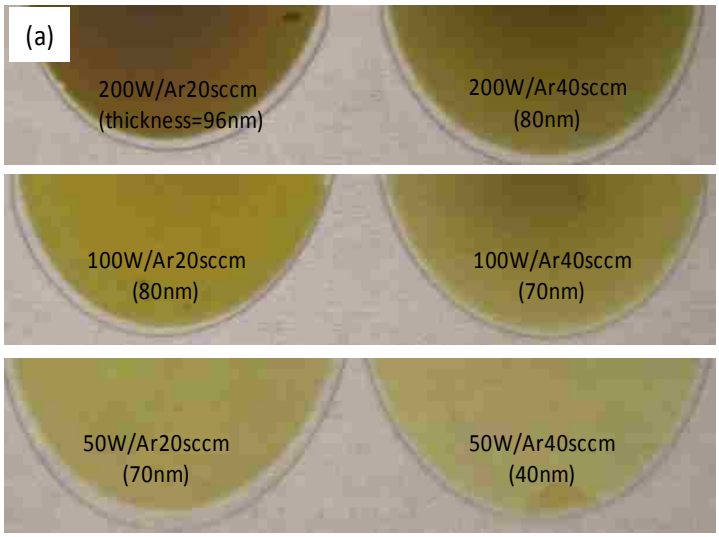


Fig. 4.3 The hν dependence of $(\alpha h\nu)^2$ of Cu_2O thin film according to deposition conditions. Note that the intercept with hν axis indicates the bandgap energy of Cu_2O.



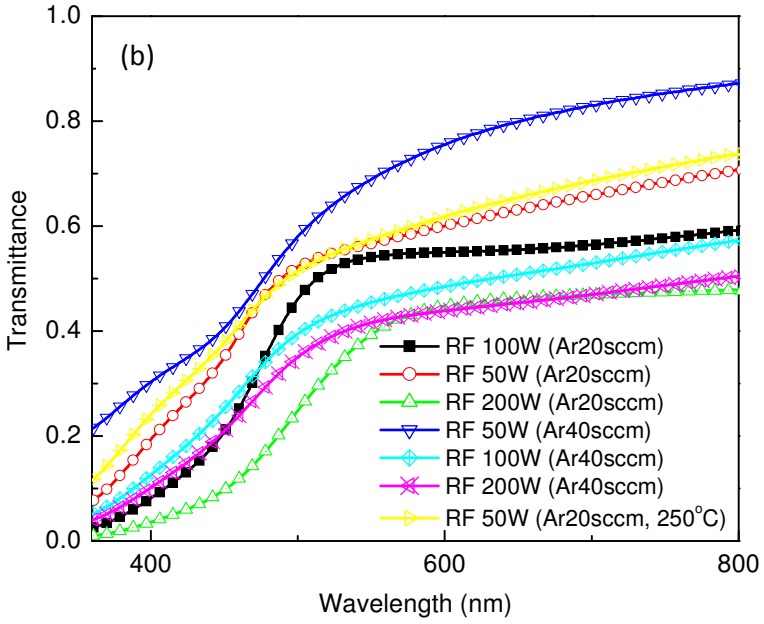


Fig. 4.4 (a) Photographs and (b) transmittance of Cu_2O thin film according to deposition conditions.

4.2.2 Hall mobility

Hall effect measurement is used to determine majority carrier type, resistivity, carrier concentration, and Hall mobility. These are crucial parameters to evaluate thin film semiconductor for active channel layer in TFTs. Hall coefficient (R_H) is defined as

$$R_H = \frac{tV_H}{IB} = \frac{1}{Nq} \tag{4.2}$$

where t is thickness of sample; V_H is Hall voltage; I is current; B is magnetic field strength; and N is carrier concentration. When R_H is negative, the film is n-type, while for positive R_H, it is p-type. Hall mobility (μ_H) is obtained by $\mu_H = |R_H| / \rho$ (ρ is resistivity) [9]

For Hall measurement, a 250nm thick Cu_2O film was deposited on a glass substrate with RF power of 50W in Ar ambient for 80min at room temperature. Hall effect measurement was established by a set current (I) of 100μA and a target voltage (V) of 20mV. Table 4.2 is the data repeatedly measured from one sample. The result indicates that the as-deposited Cu_2O is p-type with high carrier concentration having extremely low mobility. The low mobility is considered to be attributed to the scattering of high density carriers and multi-phase of CuO and Cu_2O which is explained by XPS analysis in section 4.4. Due to the instability of Hall measurement, the optimization of Cu_2O deposition has been performed by the measurement of resistivity and characterization of TFT devices.

Table 4.2 Hall effect measurement results of Cu_2O thin film.

Repeated measurement	Sheet resistance (Ω/)	Bulk resistivity (Ω-cm)	Sheet carrier concentration (cm^{-2})	Bulk carrier concentration (cm^{-3})	Hall mobility ($cm^{-2}V^{-1}s^{-1}$)
1st	$1.6x10^6$	41	1.3E+14	5.1E+18	0.03
2nd	$1.6x10^6$	40	1.5E+14	6E+18	0.026
3rd	$1.6x10^6$	40	2.5E+14	1E+19	0.016

4.3 Fabrication and optimization of Cu_2O TFT

4.3.1 Fabrication of Cu_2O TFT

The bottom gate and bottom contact TFT structure shown in figure 4.5 has been used to evaluate and optimize the device characteristics. In a previous study involving the use of Al_2O_3/Cu_2O material structure, it was shown that metallic Cu was present at the interface indicating the presence of a chemical reaction with AlO_x on surface of Al_2O_3[10]. We believe that the poor Cu_2O TFT performance is directly related with the formation of a Cu interfacial layer. In case of SiN_x and SiO_x, the reaction of oxygen with Cu_2O can be minimized because the Gibbs free energies of Si-N and Si-O are stronger than those of Cu_xO_y as shown in Table 4.3. In this study, SiO_2 has been utilized as a standard gate dielectric for the bottom gate structure since it has been proven that SiO_2 is stable dielectric for Cu_2O TFT in another study [11]. Au electrode (work function: 5.1eV) has been used as source-drain electrodes to minimize contact problems with Cu_2O (work function: ~4.84eV).

The fabrication process of Cu_2O TFT with bottom gate and bottom contact structure is described in figure 4.6. First, 200nm thick Mo layer as gate electrode is deposited by DC magnetron sputtering and patterned by liftoff process, and then 100nm thick SiO_2 gate dielectric is deposited at 320°C by PECVD. Ti/Au double layers as source-drain electrode are deposited by evaporator and patterned by liftoff process. Ti is used as an interlayer to prevent the peeling of Au that has weak adhesion with SiO_2. For the formation of semiconductor pattern, liftoff resist is coated and patterned on source-drain electrodes as shown in figure 4.6 d). Cu_2O film as an active semiconductor layer is deposited by RF magnetron sputtering in Ar ambient at room temperature.

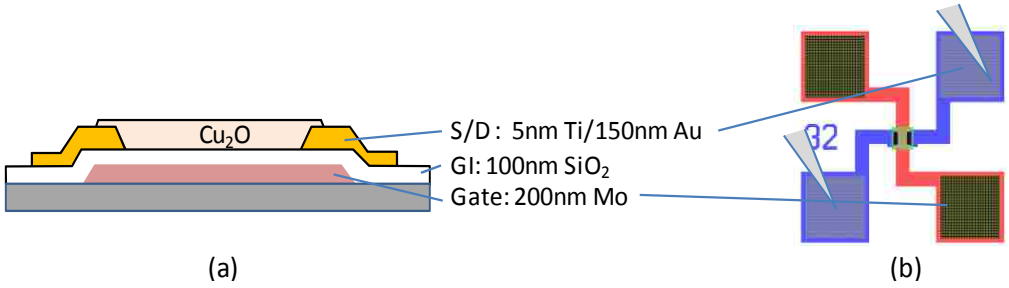


Fig. 4.5 (a) Bottom gate and bottom contact TFT structure, (b) measurement of channel resistance.

Table 4.3 Standard Gibbs energy of formation at 298.15K in J/mol.

	ΔG°(kJ/mol)		ΔG°(kJ/mol)
Si-O	-805	CuO	-129.7
Si-N	-470	Cu_2O	-146.0
AlO	65.3		

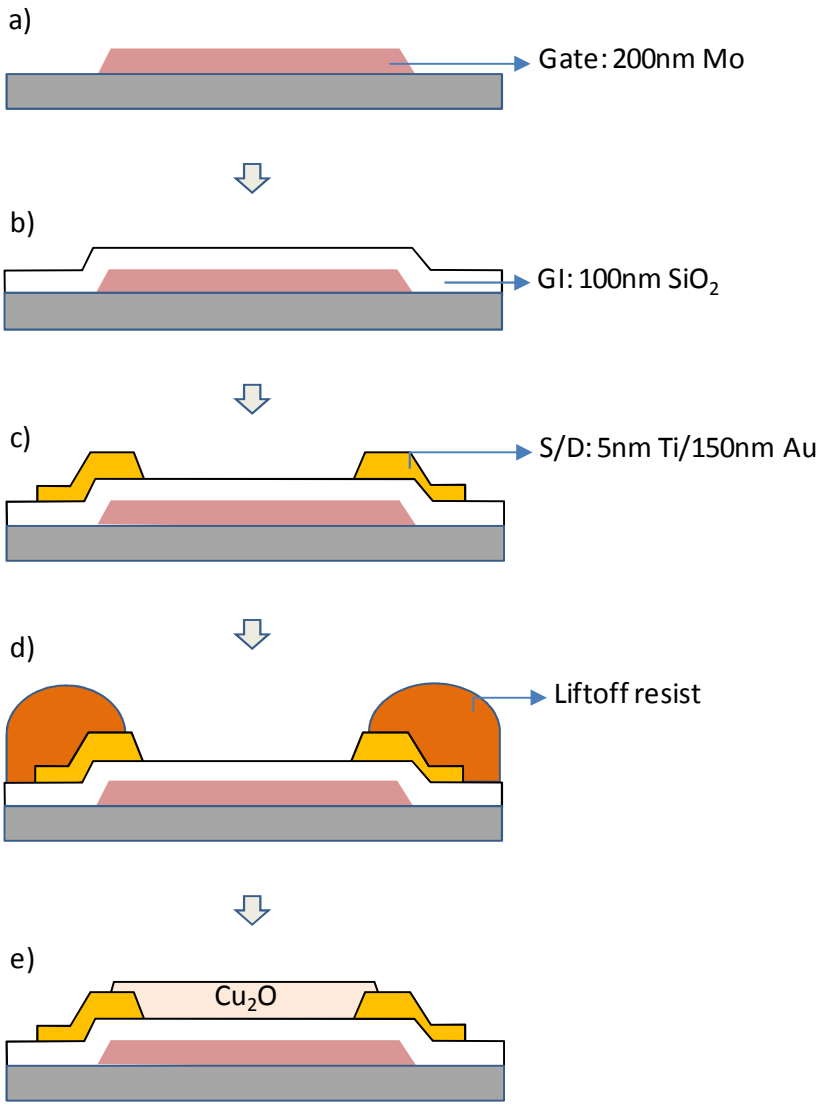


Fig. 4.6 Cross-sectional view of Cu_2O TFT fabrication step by step

4.3.2 Effect of deposition condition

Main parameters in sputter deposition are power, pressure (Ar flow rate), and temperature. In addition, the reactive sputtering using O_2 and N_2 was also investigated. Figure 4.7 shows the sputter deposition rate as a function of RF power and Ar pressure.

The pressure of 40sccm Ar is relatively high (11mtorr), so 20sccm Ar (process pressure: 5.8mTorr) was utilized in the following experiments.

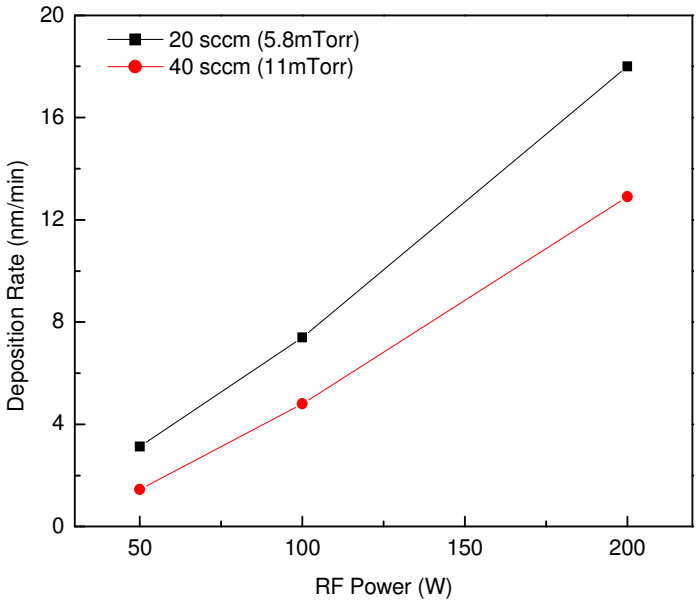


Fig. 4.7 Deposition rate according to RF power and Ar gas flow rate

Figure 4.8 shows the effect of deposition power on the resistivity of Cu_2O channel material and on the transfer curve of Cu_2O TFT. Channel resistance was measured as described in figure 4.5 (b), and the resistivity was calculated by [12]

$$\rho = R \cdot t \cdot \frac{W}{L} \tag{4.3}$$

where ρ is resistivity, R is resistance, t is film thickness, W is width, and L is length. Table 4.4 shows the actual Cu_2O resistivity extracted from the I-V characteristics shown in figure 4.8 (a). The samples were pretreated by oxygen plasma (100W/10sec in RIE mode dry etch) to eliminate any organic impurity before Cu_2O deposition; these samples

were also compared with samples without any oxygen pretreatment. The oxygen plasma tends to increase the resistivity of channel, and decrease the drain current of TFTs as shown in figure 4.8. A small modulation is apparently in the transfer and output characteristics of Cu_2O TFT deposited with RF 50W and pretreated by oxygen plasma as shown in figure 4.9. The TFT is modulated by the sweep of gate bias but the on/off current ratio is only 1.4. Gate leakage current is low with level of 10~100pA. Thus this behavior verifies that the device is a p-type TFT.

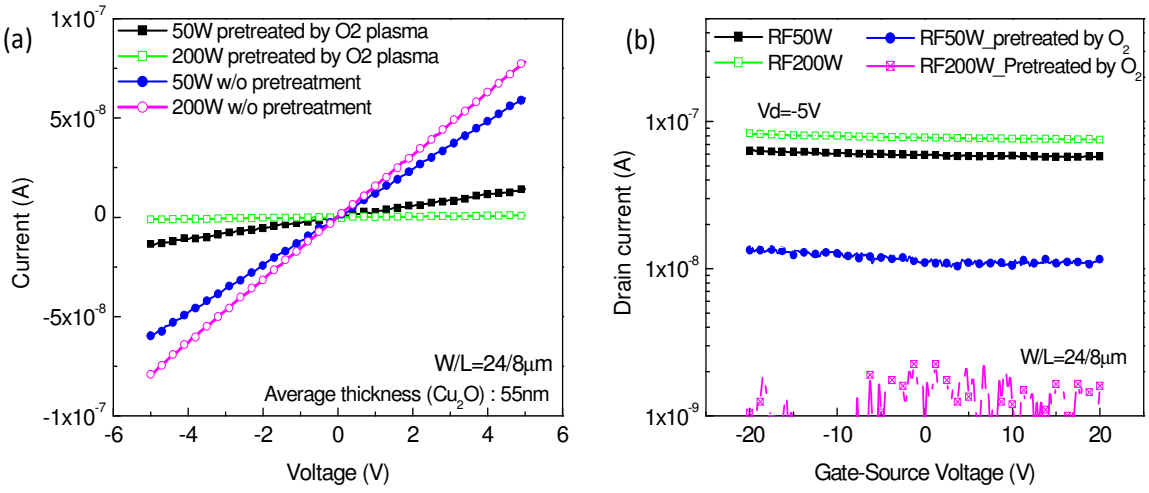


Fig 4.8 Effect of deposition power and oxygen plasma pretreatment on Cu_2O TFT. (a) Channel I-V characteristic (b) transfer curve (W/L=24/8μm)

Table 4.4 Cu_2O resistivity extracted from the I-V characteristics shown in figure 4.8 (a)

Resistivity(Ω-cm)			
With O_2 plasma		Without O_2 plasma	
50W	200W	50W	200W
5330	66316	1222	1033

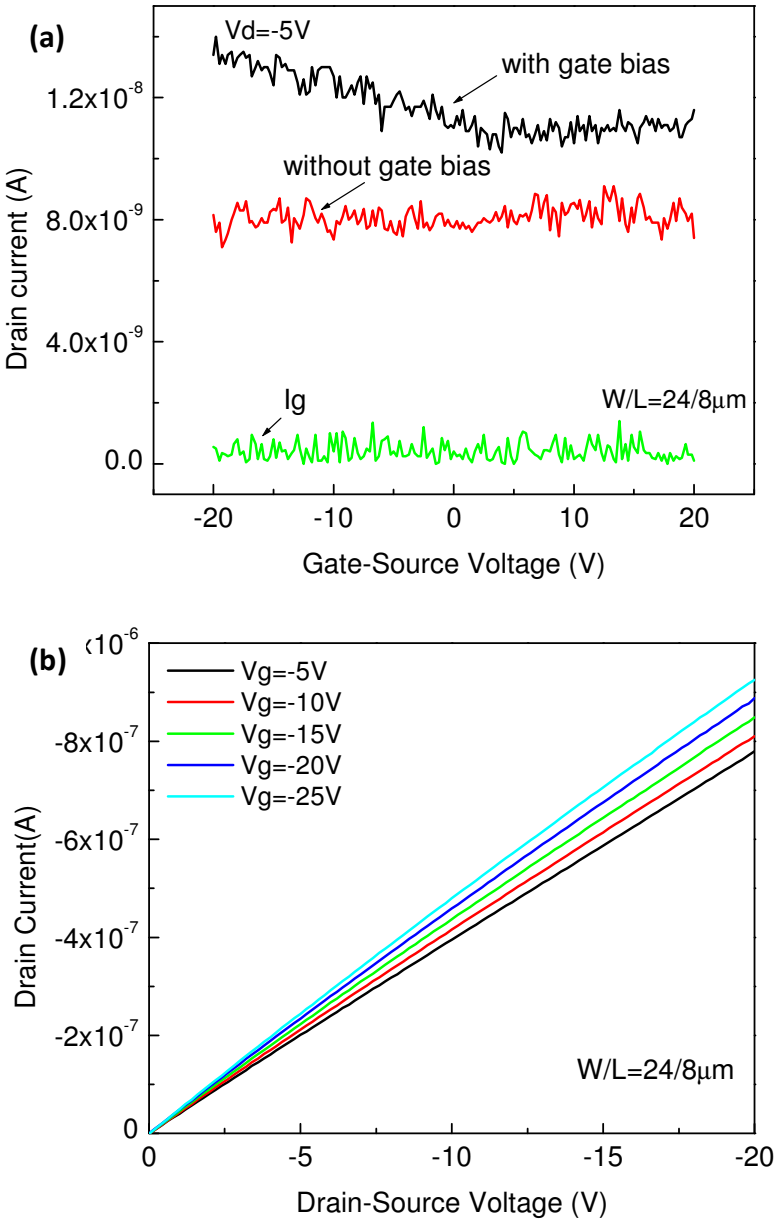


Fig. 4.9 (a) Transfer curve, (b) output characteristics of Cu_2O TFT (RF 50W, thickness; 55nm)

Since active Cu_2O layer was patterned by liftoff process in this study as described in figure 4.6, channel resistances are compared before and after liftoff process as shown in figure 4.10 (a). All characteristics are identical. Accordingly, it is concluded that liftoff process does not affect Cu_2O layer. In addition, figure 4.10 (b) presents the effect of channel thickness. The resistivity increases when thickness is reduced, however there is no big difference in the modulation of transistors. The transfer curve in figure 4.8(b) shows TFTs having 55nm thick Cu_2O.

In order to investigate the effect of oxygen and nitrogen reactive sputtering, O_2 or N_2 gas was introduced and the reactive gas flow was controlled along with that of Ar gas during Cu_2O sputtering. At low oxygen concentration, the resistivity of Cu_2O decreases, and then tends to increase with increasing oxygen concentration as shown in figure 4.11 (a). No modulation was observed in the transfer characteristics of TFTs in Cu_2O deposited under different $Ar:O_2$ ratios as shown in figure 4.11 (b). It is estimated that the decrease of resistivity is attributed to the reduction of defect density [13] and the increase of resistivity originates from the reduction of oxygen vacancies that contribute to conductivity [14]. Meanwhile, resistivity and transfer curve were not distinctly changed by N_2 reactive sputtering as shown in figure 4.12.

To examine the substrate temperature dependence during Cu_2O deposition, the substrate without liftoff patterns was annealed at 200°C for 10min in sputter chamber just before Cu_2O deposition. 55nm thick Cu_2O was deposited with RF power of 50W, and then 30nm thick Si was sequentially deposited as passivation layer in same sputter chamber. However the TFT did not work well as shown in figure 4.13 (c). In another

experiment, Cu_2O TFT was fabricated with the structure of figure 4.14 (a). 200nm thick ITO as gate electrode was formed by RF magnetron sputtering without patterning process, and then 100nm thick SiO_2 gate dielectric was deposited at 320°C by PECVD. The substrate was annealed at 500°C for 5min in sputter chamber just before Cu_2O deposition, and then 55nm thick active Cu_2O layer was deposited by RF magnetron sputtering with 50W in Ar ambient at room temperature. 200nm thick ITO layer was deposited as source-drain electrodes and patterned by liftoff process. The color of the as-deposited Cu_2O was light blue and the TFT characteristic was similar to the 200°C TFT, as shown in figure 4.14 (c). The observed low resistivity in figure 4.13 (a) and 4.14 (a) can be explained by the results reported by W. Yang [15]. According to W. Yang [15], Cu peak appears in the XRD spectra of Cu_2O films when increasing the substrate temperature (200°C) during Cu_2O deposition as shown in figure 4.15. The Cu_2O film in that report was obtained by sputtering from a Cu_2O target. It is estimated that Cu originates from the reduction of Cu_2O in vacuum.

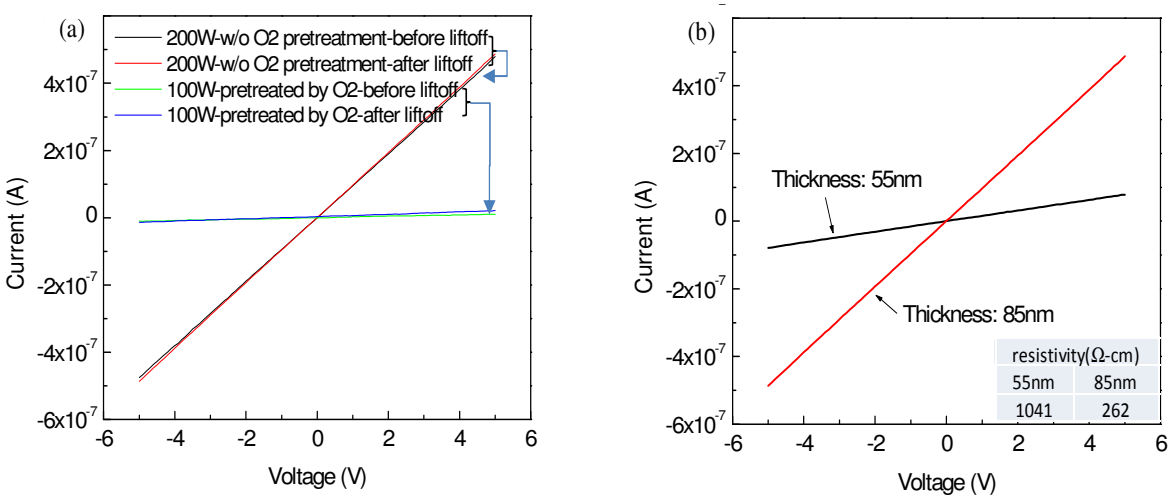


Fig. 4.10 I-V characteristics of Cu_2O (a) before and after liftoff process, and (b) according to channel thickness variation.

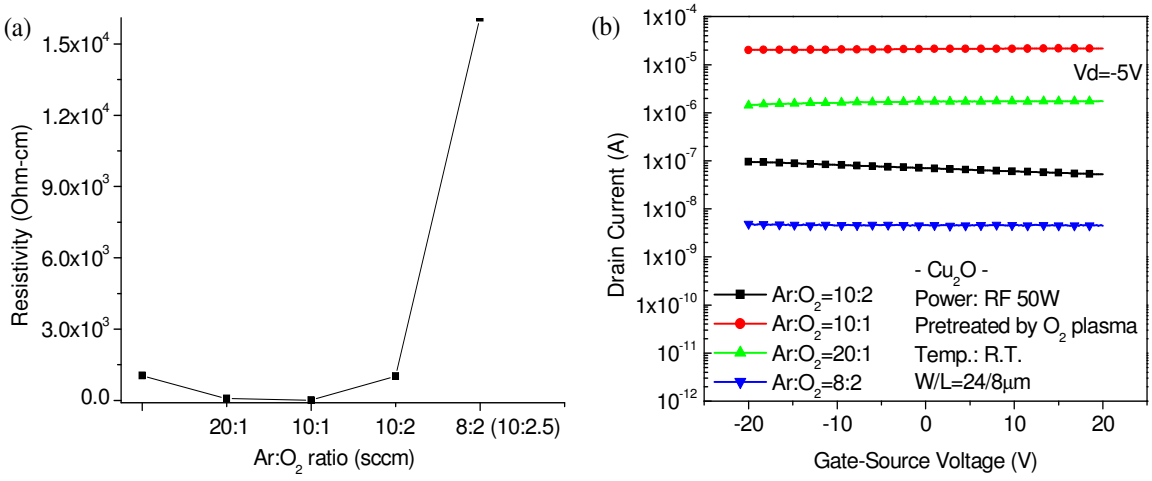


Fig. 4.11 According to the variation of $Ar:O_2$ ratio during sputtering process, (a) resistivity variation of Cu_2O, (b) transfer curve of Cu_2O TFTs.

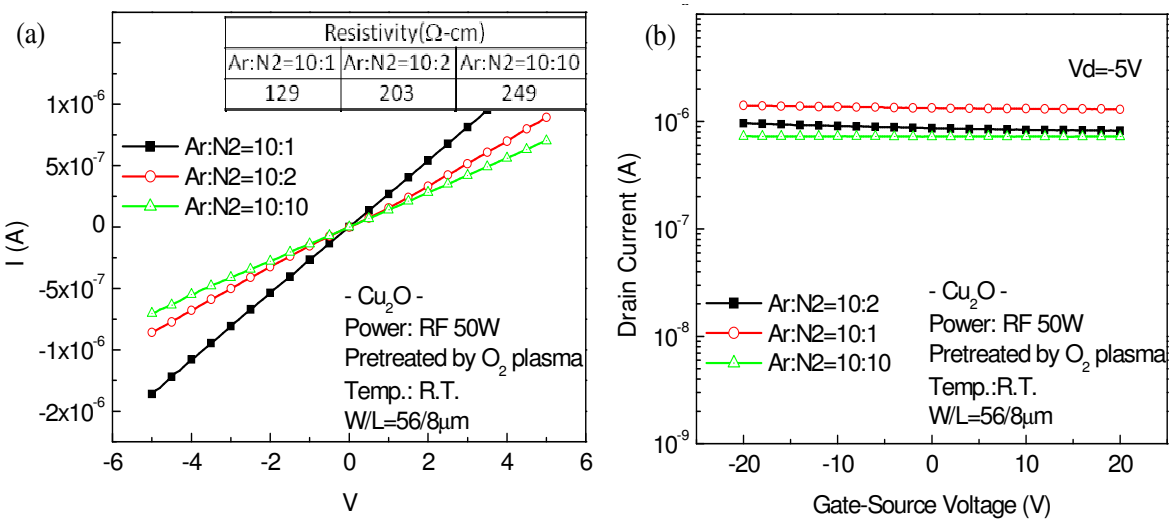


Fig. 4.12 According to the variation of $Ar:N_2$ ratio during sputtering process, (a) I-V characteristics and (b) transfer curve of Cu_2O TFT.

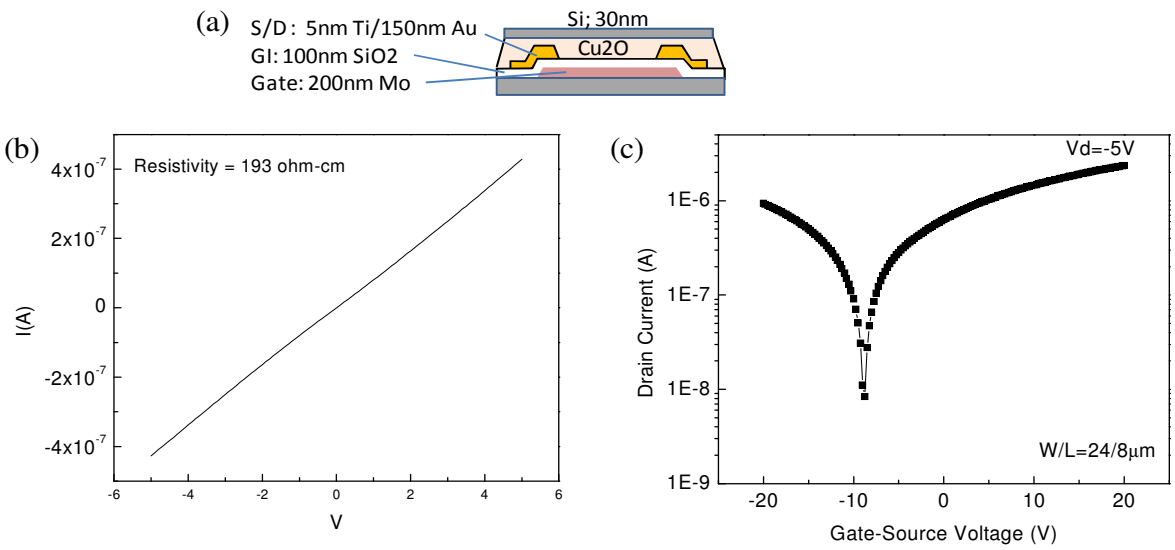


Fig. 4.13 (a) TFT structure, (b) I-V characteristic, and (c) transfer curve of Cu_2O TFT.

Substrate was annealed at 200°C for 10min before Cu_2O deposition.

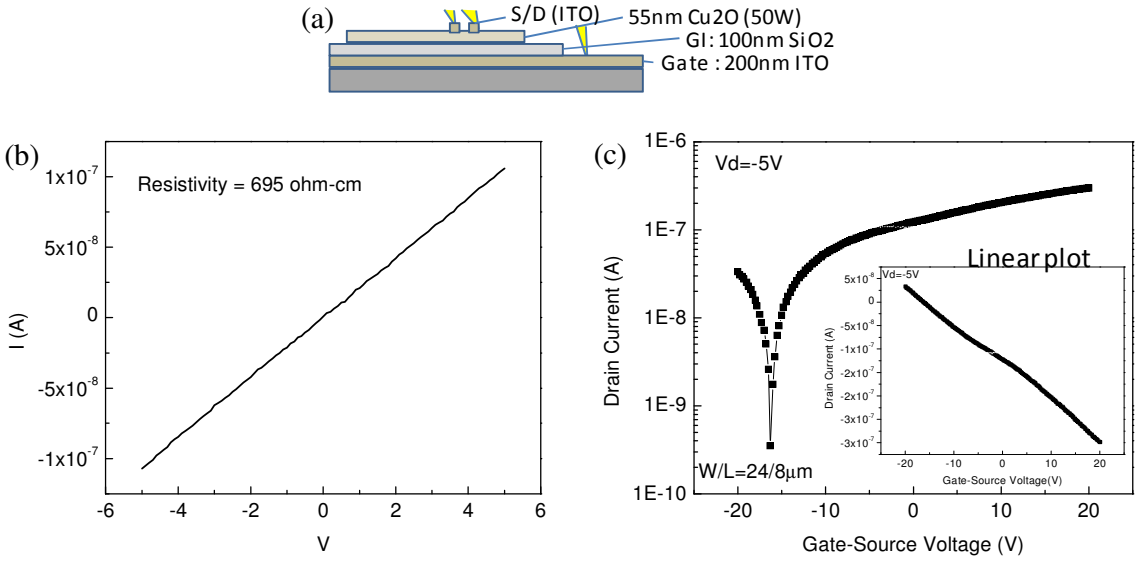


Fig. 4.14 (a) TFT structure, (b) I-V characteristic, and (c) transfer curve of Cu_2O TFT.

Substrate was annealed at 500°C for 5min before Cu_2O deposition.

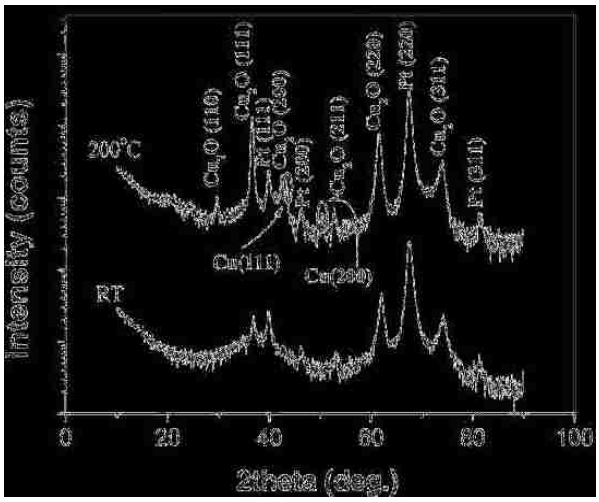


Fig. 4.15 (a) XRD peaks for Cu_2O films according to deposition temperature (room temperature (R.T.) and 200°C). [Adapted from Ref.15].

4.3.3 Post-annealing effect

Post-annealing treatments in air and N_2 ambient have been studied to enhance the poor characteristics of Cu_2O TFTs. The effect of post-annealing process on the transfer curve of TFTs and resistivity of material is presented in figure 4.16 and 4.17.

Sung et al. reported TFTs using CuO active layer with bandgap energy of 1.4eV by annealing Cu_2O films obtained from Cu_2O target [16]. In his report, post-annealing in air at 300°C for 10hr transformed an as-deposited Cu_2O to CuO phase [16]. We had attempted to reproduce the device with same process and structure of figure 4.14 (a), however the result was not reproducible. Thus, in order to find optimal condition of annealing in air, various conditions of temperature and time were additionally evaluated by using the device structure of figure 4.5. Annealing at 200°C was first investigated with the duration time of 1hr and 3hrs, and then annealing at 300°C was examined with the

duration time of 5hrs and 10hrs. While post-annealing in air at 200°C for 1hr decreases the resistivity of Cu_2O, which is attributed to the formation of partial CuO phase by oxidation, post-annealing at 300°C for 5hrs increases the resistivity and changes the color of Cu_2O to bluish, as shown in figure 4.17 and 4.18 (b). This high resistivity might come from the damage of Cu_2O layer by severe oxidation.

Post-annealing in N_2 ambient was explored to prevent any oxygen reaction of Cu_2O layer during annealing. Cu_2O TFTs was prepared without passivation (structure: figure 4.5) and with SiO_xN_y passivation. In case of Cu_2O TFTs without passivation, the resistivity of Cu_2O decreases with the increase of temperature up to 300°C as shown in figure 4.17, which corresponds to the presence of Cu and CuO peaks in XRD results of figure 4.19. However, the resistivity at 400°C is increased to $10^4\Omega$-cm and the color of the Cu_2O becomes reddish as shown in figure 4.18 (c). In case of Cu_2O TFTs with SiO_xN_y passivation, 30nm thick SiO_xN_y was sequentially deposited after deposition of Cu_2O in same sputter chamber to avoid any exposure of Cu_2O layer to air. SiO_xN_y layer was formed by reactive sputtering using SiO_2 target with the mixed gas of Ar (20sccm) and N_2 (20sccm). The characteristic of device was not improved as shown in figure 14.16 (c), and a number of voids occurred after post-annealing in N_2 ambient at 300°C for 1hr as shown in figure 4.18 (d). These voids were also visible by TEM analysis discussed in section 4.4.

In summary, it is estimated that the low resistivity of area (A) in figure 4.17 is attributed to the formation of $Cu^0 + Cu^{2+}$ for N_2 and Cu^{2+} for air annealing. The high resistivity of area (B) in figure 4.17 mostly stems from voids occurred during the

annealing and the reduction of oxygen vacancies. Therefore, post-annealing process is not recommendable for Cu_2O film obtained from Cu_2O sputter target.

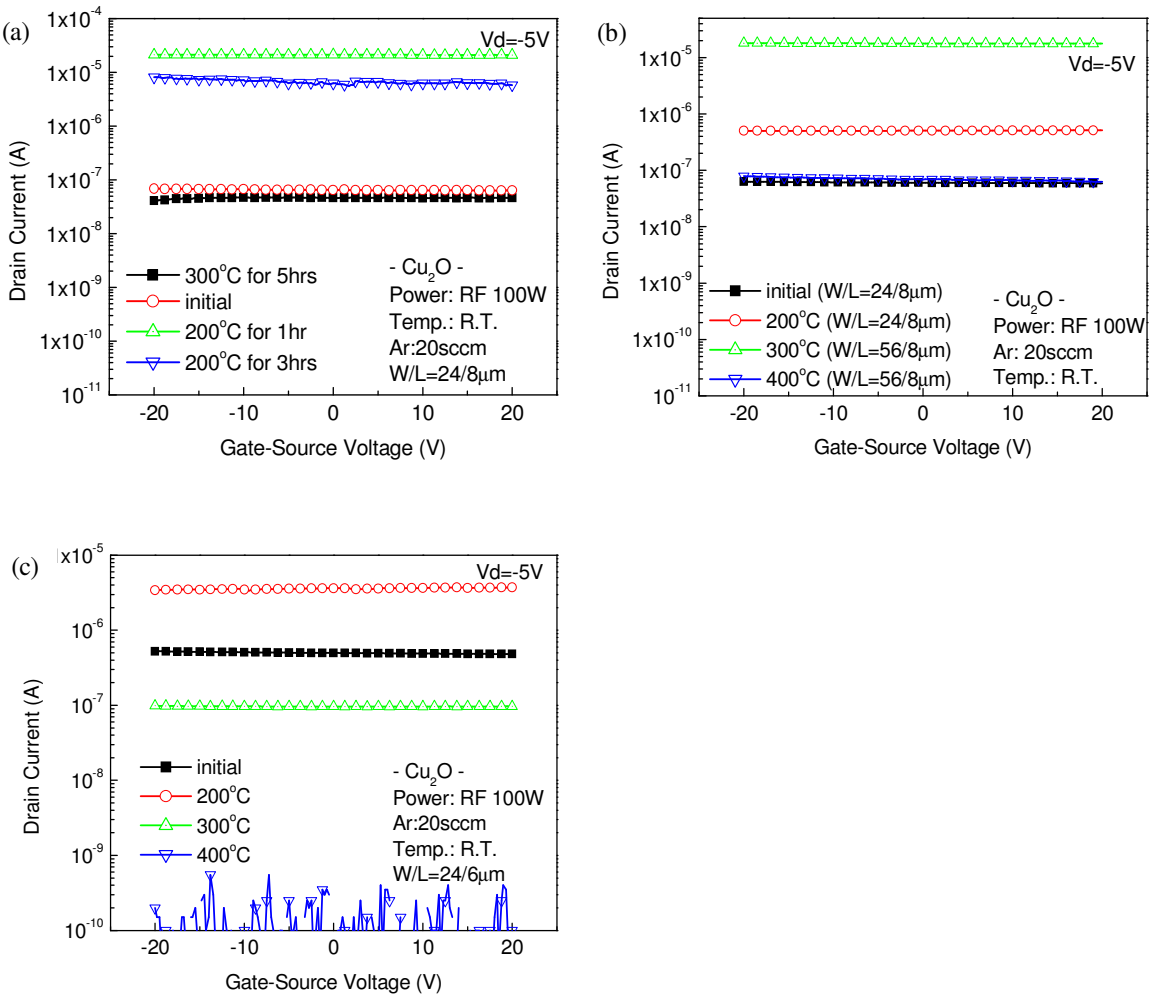


Fig. 4.16 Transfer curve of Cu_2O TFT according to annealing conditions. (a) in air (b) in N_2 (c) in N_2 (TFT with SiOxNy passivation).

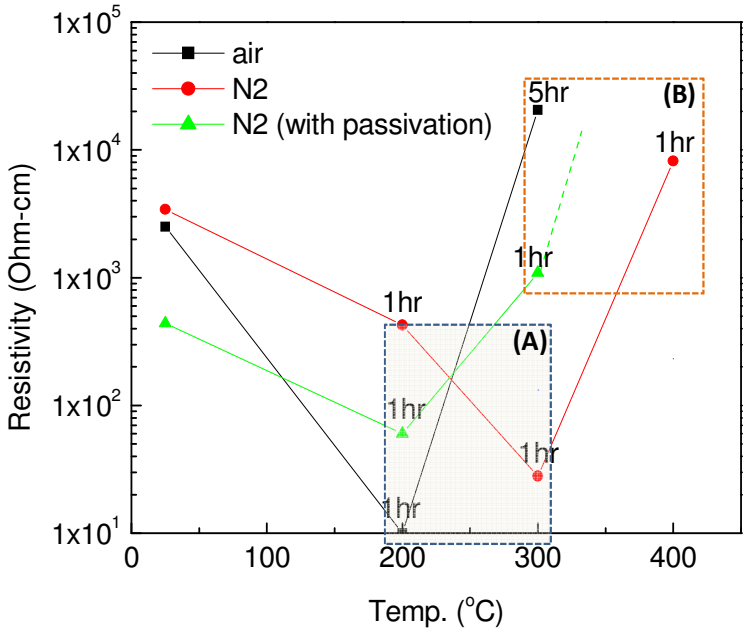


Fig. 4.17 Resistivity variation of Cu_2O layer as a function of annealing time in air and N_2

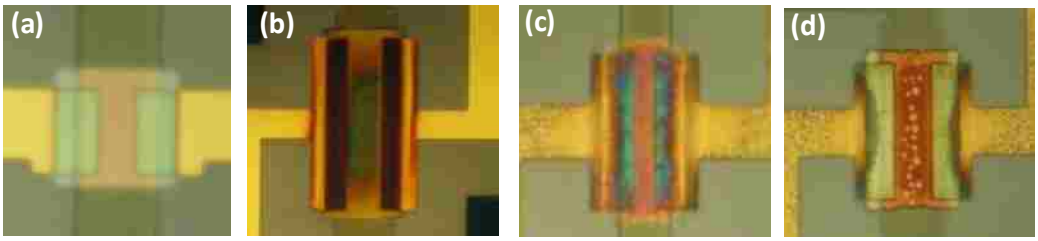


Fig. 4.18 Optical images of Cu_2O TFTs (a) as-fabricated, (b) after annealing in air at 300°C for 5hrs, (c) after annealing in N_2 at 400°C for 1hr, (d) after annealing in N_2 at 300°C for 1hr (with SiO_xN_y passivation)

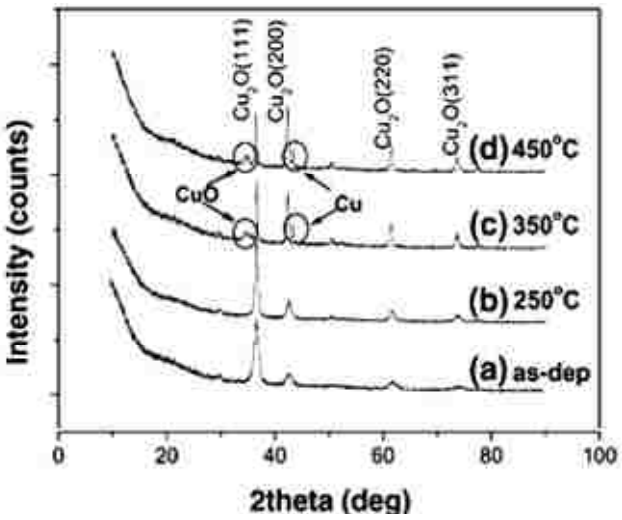


Fig. 4.19 XRD peaks of Cu_2O with the annealing temperature in N_2 ambient for 1min [Adapted from Ref.15].

4.3.4 Plasma treatment

The effect of plasma treatment in O_2, N_2O, and H_2 has been investigated. Resistivity of Cu_2O increased when the time of O_2 plasma increased as shown in figure 4.20 (a), however it did not improve the modulation characteristics of TFTs shown in figure 4.20 (b). The increase of resistivity might originate from the reduction of oxygen vacancies by the reaction of oxygen ions in plasma. N_2O plasma annealing at a power level of 50W or 200W was performed on the surface of Cu_2O TFTs at 100°C for 10min. Cu_2O annealed at 50W N_2O plasma exhibits low resistivity of 16Ω-cm as shown in figure 4.20 (c), presumably due to the reduction of defect density. In contrast, a high resistivity of 1500 Ω-cm was observed in Cu_2O annealed at 200W N_2O plasma which may originate from the reduction of oxygen vacancies [14]. None of the TFTs showed any modulation in their transfer characteristics as shown in figure 4.20 (d).

Tabuchi et al. reported the effect of atomic hydrogen to control excessive oxygen atoms that cause the conductivity of Cu_2O [17]. In this study, H_2 plasma was investigated to control oxygen vacancies and trap sites. The resistance of Cu_2O layer was abruptly decreased with the increase of H_2 plasma power at 25°C and 100°C, and I-V characteristic of Cu_2O shows metallic behavior as shown in figure 4.21 (a) and (b). It is assumed that hydrogen partially induces metallic Cu in bulk film by the reaction with the oxygen of Cu_2O and CuO as shown in the schematic of figure 4.21 (c) [18, 19]. The activation energy of CuO is approximately 14.5 kcal/mol, while that of Cu_2O is 27.4 kcal/mol. Therefore, the reduction of CuO to metallic Cu is easier than that of Cu_2O under H_2 plasma conditions [19].

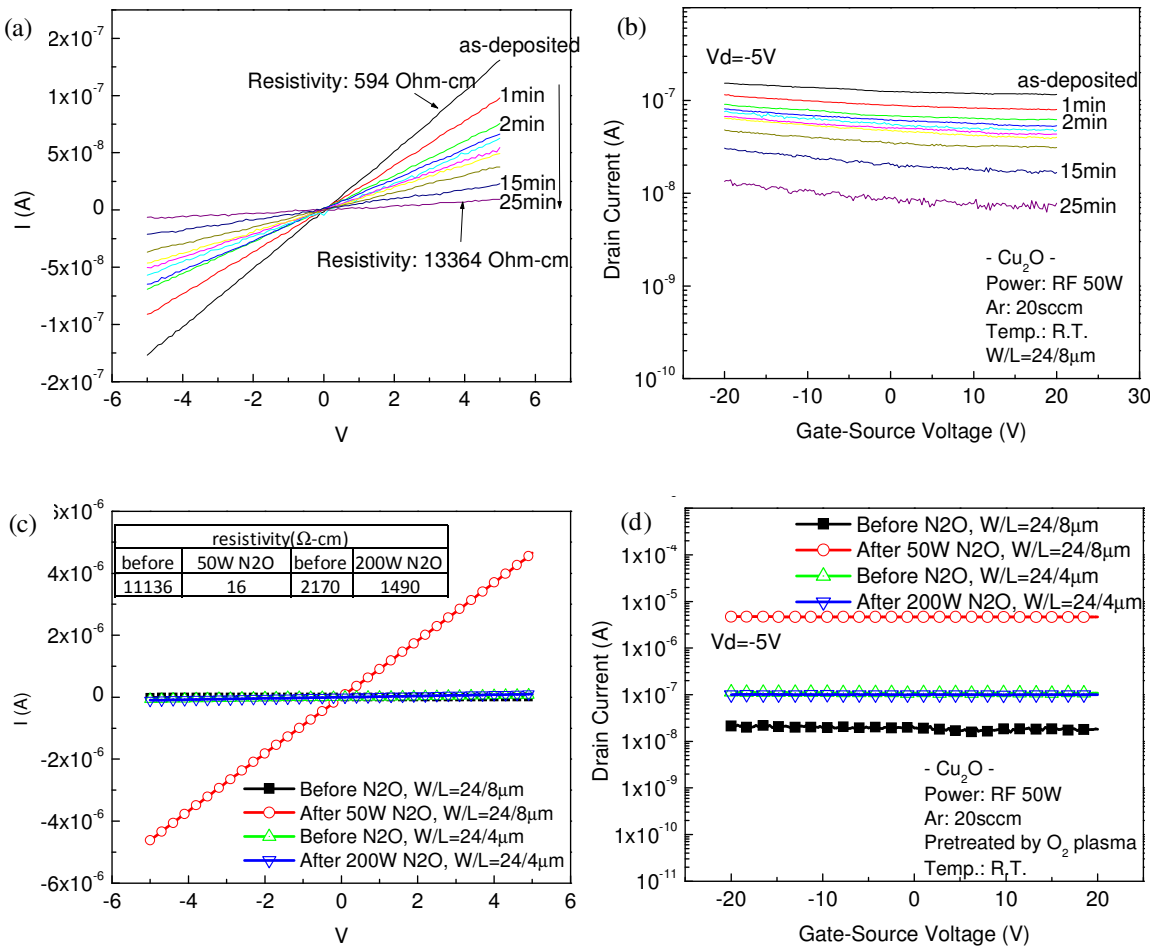


Fig. 4.20 (a) and (c): I-V characteristics, (b) and (d): transfer curve of Cu_2O TFT. (a) and (b): oxygen plasma with 100W RF power. (c) and (d): N_2O plasma with 50W and 200W RF power.

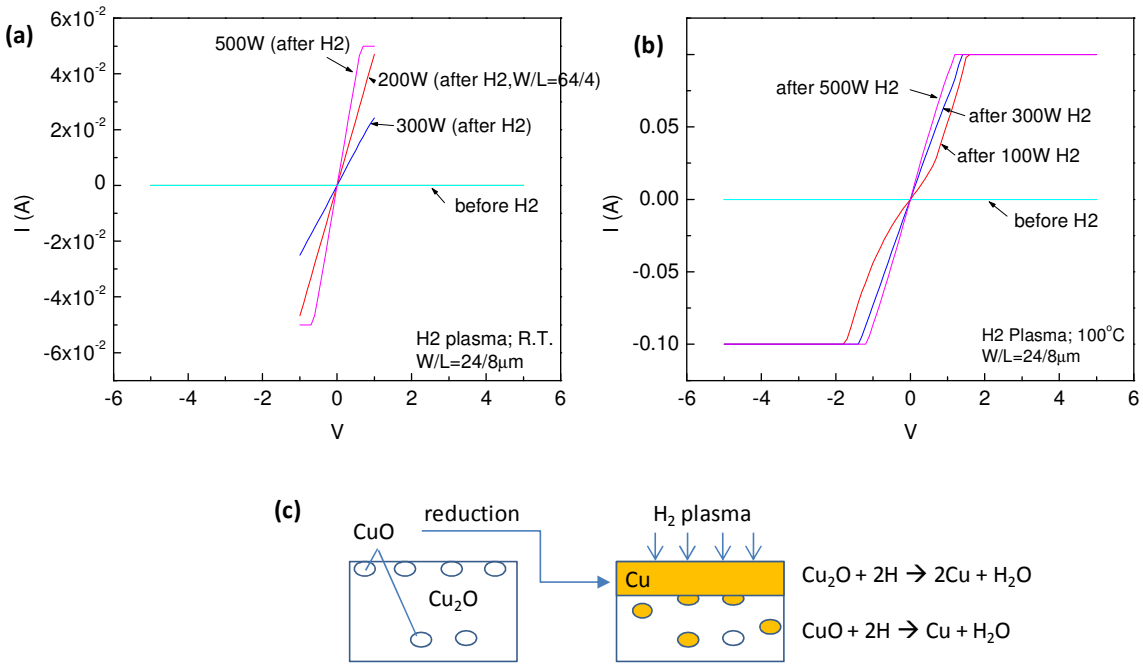


Fig. 4.21 I-V characteristics of Cu_2O films after H_2 plasma. (a) at room temperature for 1min, (b) at 100°C for 1min. (c) is a schematic of H_2 plasma effect on Cu_2O film including CuO phase

4.4 Material analysis of Cu_2O thin film

The results from all experiments presented in section 4.3 have shown that the Cu_2O films, obtained from the Cu_2O sputter target used in this study, are not suitable for an active semiconductor of TFT. In order to find the cause of the poor TFT characteristics, Cu_2O films obtained from this Cu_2O sputter target were analyzed by X-ray photoelectron spectroscopy (XPS) and transmission electron microscope (TEM).

In XPS, incident X-rays eject photoelectrons from a sample, and the measured energy of the ejected electron at a spectrometer (E_{sp}) is related to binding energy (E_b) by

$E_b = h\nu - E_{sp} - q\phi_{sp}$, where $h\nu$ is the energy of X-rays and ϕ_{sp} is the work function of the spectrometer [9]. Figure 4.22 presents XPS results of Cu_2O thin films that are deposited in sputter with RF power of 200W and 50W respectively. Through quantification analysis using CasaXPS, we caculated the ratio of Cu^+ and Cu^{2+}. It is known that the binding energy of Cu $2p_{3/2}$ is 932.4±0.2 eV for Cu_2O (Cu^+) [20], and CuO(Cu^{2+}) having $3d^9$ configuration shows shake-up satellite feature on the higher binding energy of the Cu $2p_{3/2}$ spectrum [21]. The Cu_2O deposited at 200W offers Cu^+ of 73% and Cu^{2+} of 27%, and the Cu_2O deposited at 50W includes Cu^+ of 66% and Cu^{2+} of 34%. From these results, it is estimated that the source of the Cu^{2+} is one of 1) contamination of sputter target and 2) natural oxidation while transporting samples from sputter to XPS.

Powder from our 99.99% Cu_2O sputter target was obtained by scraping the target in glove box with N_2 ambient, and then analyzed by XPS. In figure 4.23, Cu^{2+} of 31~40% similar to the Cu_2O thin film deposited with 50W RF power was observed from the powder. Therefore, we can assume that the CuO phase occurs during the fabrication process of Cu_2O target since Cu^+ is easily oxidized to Cu^{2+} by heat and air condition; it is interesting to note that Cu_2O target is made by cold pressing of Cu_2O powder at several MN/m^2 load followed by sintering at high temperature [22].

Annealing at 400°C for 30min in XPS vacuum chamber reduced the CuO phase from ~30% to ~15%, and Cu_2O phase relatively increased as shown in figure 4.24 (a) and (b). The samples exposed to air for 26 hrs after vacuum annealing was reoxidized to CuO; accordingly the CuO phase was increased again to ~30% in figure 4.24 (c) and (d), which indicates that Cu_2O is oxidized in air condition. In order to reduce the CuO phase and

prevent any air exposure of Cu_2O layer, Cu_2O TFT with structure of figure 4.5 was annealed in vacuum for 30min at 300°C and 400°C respectively, and then an intrinsic Si layer was deposited as passivation after annealing in same sputter chamber. The results are not satisfactory as shown in figure 4.25. Even though vacuum annealing can reduce the CuO phase, CuO phase still exists and voids occur when annealing at a temperature higher than 300°C as observed by TEM.

TEM was utilized to investigate the crystallinity of Cu_2O thin films deposited by Cu_2O sputter target. 55nm thick Cu_2O film was deposited on a copper grid for TEM preparation. As shown in figure 4.26, the as-deposited Cu_2O film has a poly-crystalline structure with grain sizes ranging from 10-20nm; the selected area diffraction (SAD) pattern in TEM also proves its polycrystalline structure. Micrographs obtained by TEM are shown in figure 4.27 from a 55nm thick Cu_2O film annealed at 300°C in a vacuum chamber with a base pressure of 9×10^{-7} Torr. The grain size grew from 10~20nm to 100nm, however numerous voids occurred in the film. These voids became larger by annealing at 500°C and finally made Cu_2O film discontinuous in the channel area of TFT.

In conclusion, in this study, Cu_2O films obtained from a Cu_2O sputter target exhibited high concentration of Cu^{2+} when analyzed by XPS. This is associated with the presence of CuO phase. This multi-phase is not easy to be controlled by additional treatments such as annealing and plasma, since Cu_2O easily transforms to different phase of Cu^0 or Cu^{2+} by reduction and oxidation. From literature reports, it is estimated that Cu_2O having Cu^0 or Cu^{2+} possess trap states in the bandgap [5, 14]. In addition, it is reported that Cu_2O contains multiple levels of donor and acceptor-type traps caused by

copper and oxygen vacancies [23, 24]. Through the literature review [15, 23, 24], the energy band structure of Cu_2O, Cu and CuO are depicted in figure 4.28. The oxygen vacancies in Cu_2O introduce donor level (E_d) in figure 4.28 and contribute to the conductivity of Cu_2O [23]. Therefore, in order to improve TFT performance, it is essential 1) to create Cu_2O single phase, 2) to minimize oxygen vacancies in Cu_2O film, and 3) to prevent any oxidation and reduction by heat and oxygen.

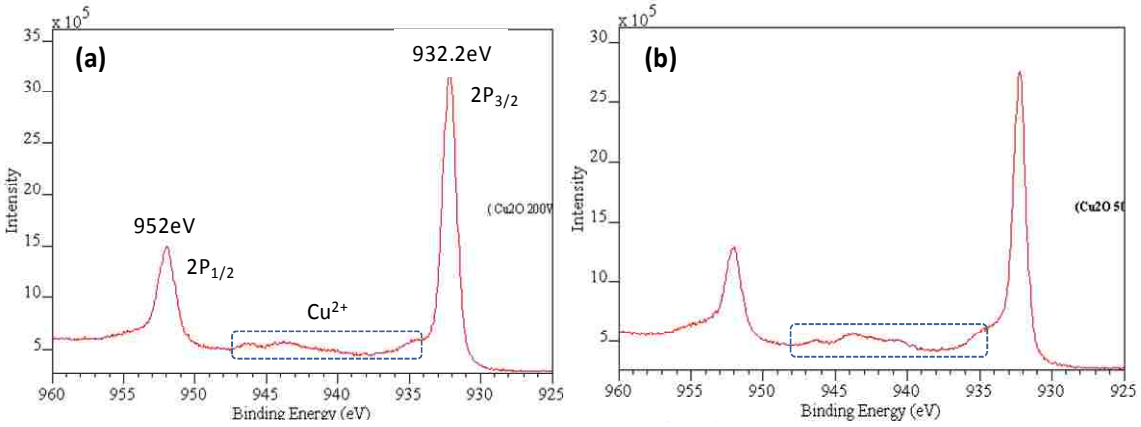


Fig. 4.22 XPS analysis of Cu_2O films. (a) RF deposition power of 200W, and (b) 50W.

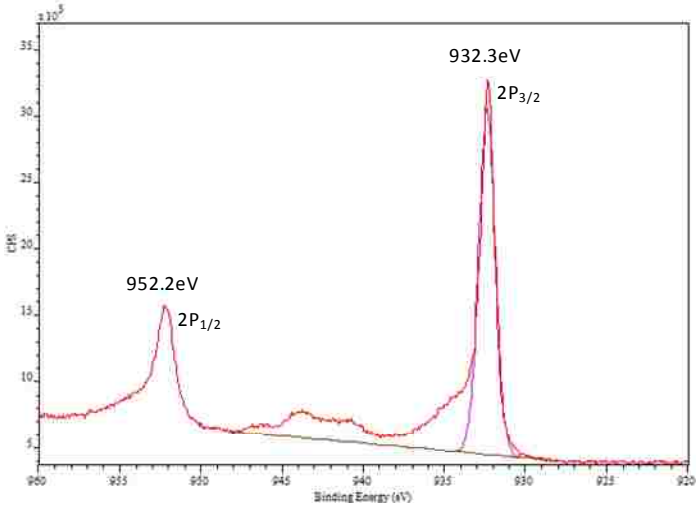


Fig. 4.23 XPS analysis of Cu_2O powder obtained from 99.99% Cu_2O sputter target.

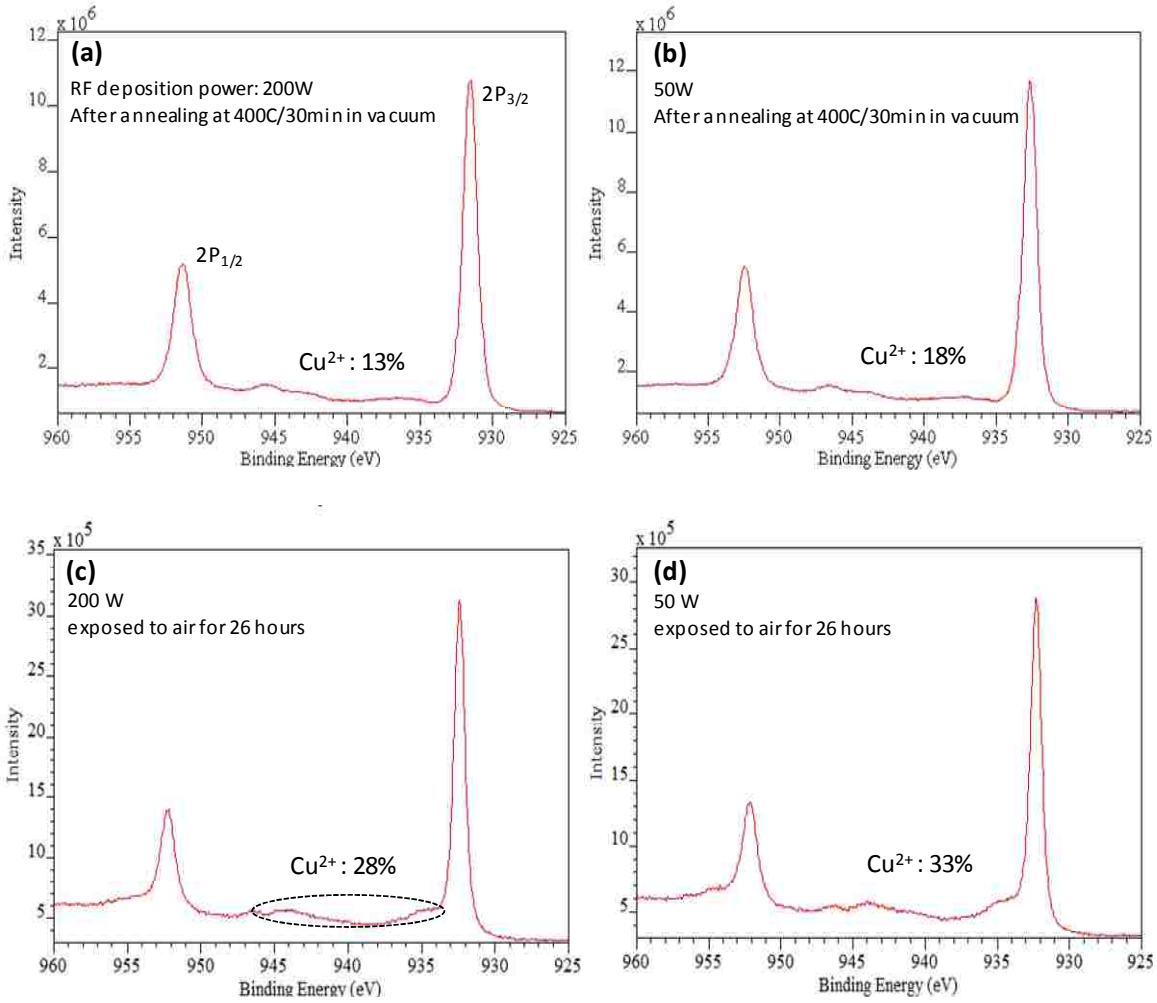


Fig. 4.24 XPS analysis of Cu_2O films. (a), (b) after annealing in vacuum at 400°C for 30min, and then (c), (d) exposed to air for 26hrs.

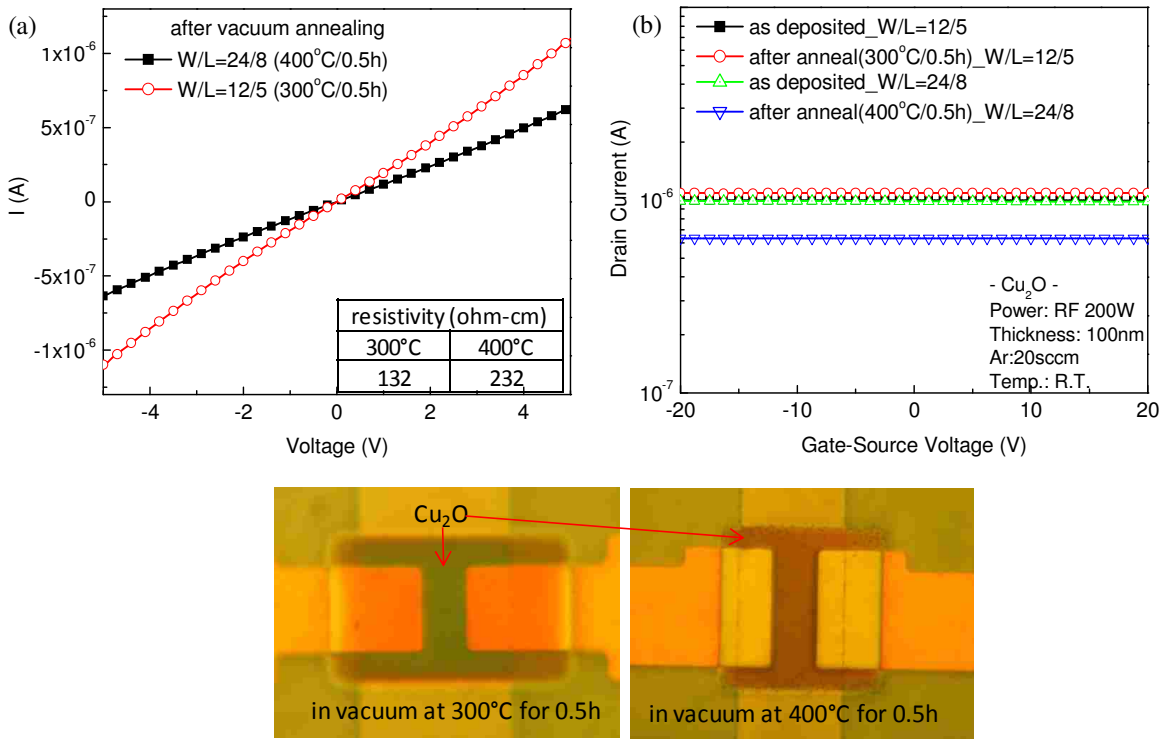


Fig. 4.25 Effect of vacuum annealing. (a) I-V characteristic, (b) transfer curve of Cu_2O TFT

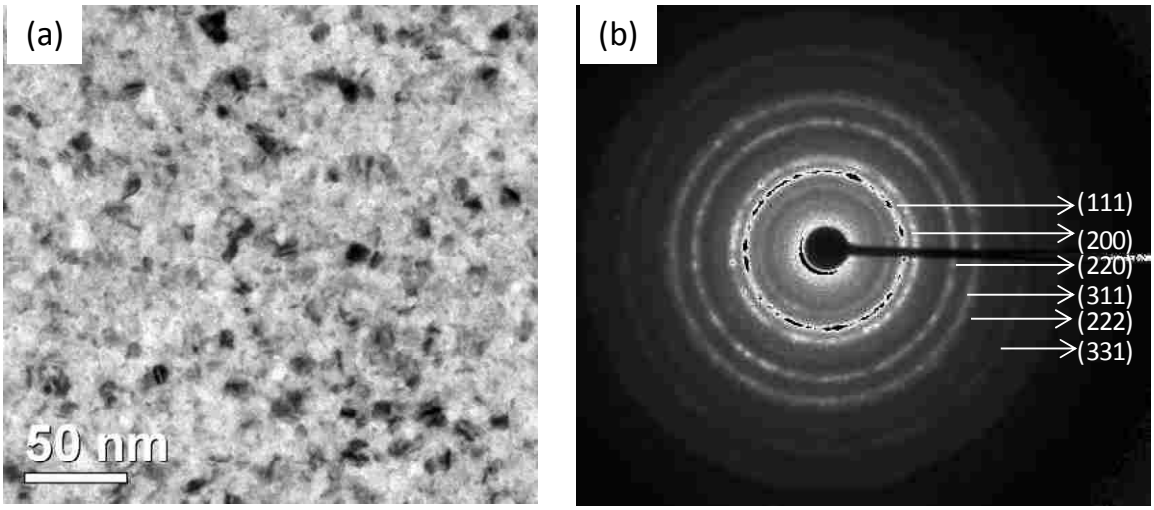


Fig. 4.26 (a) TEM image and (b) SAD patterns of the as-deposited Cu_2O film

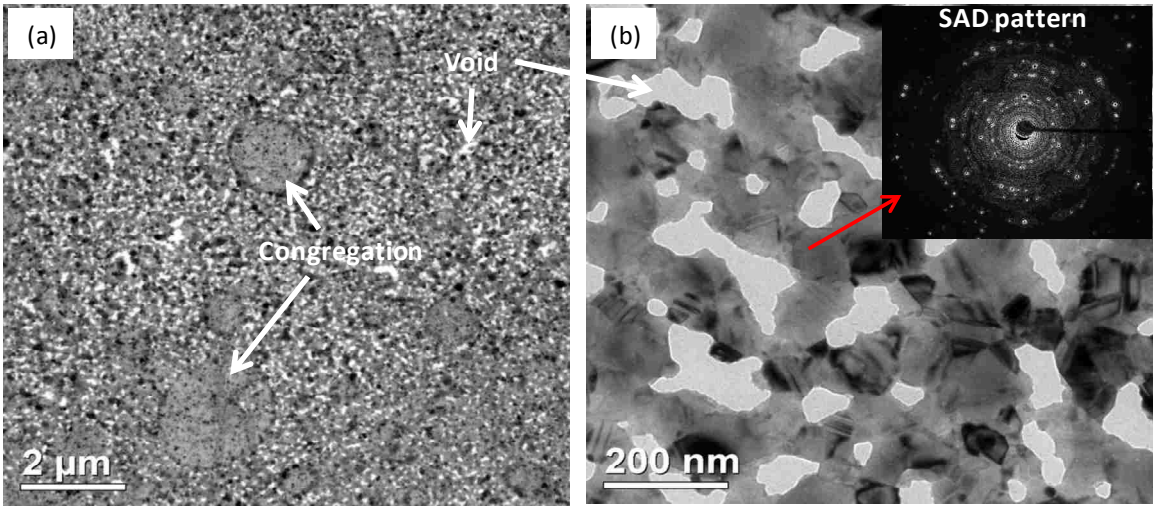


Fig. 4.27 (a), (b) TEM image of the Cu_2O film annealed at 300°C for 30min in vacuum (base pressure; 9×10^{-7} Torr)

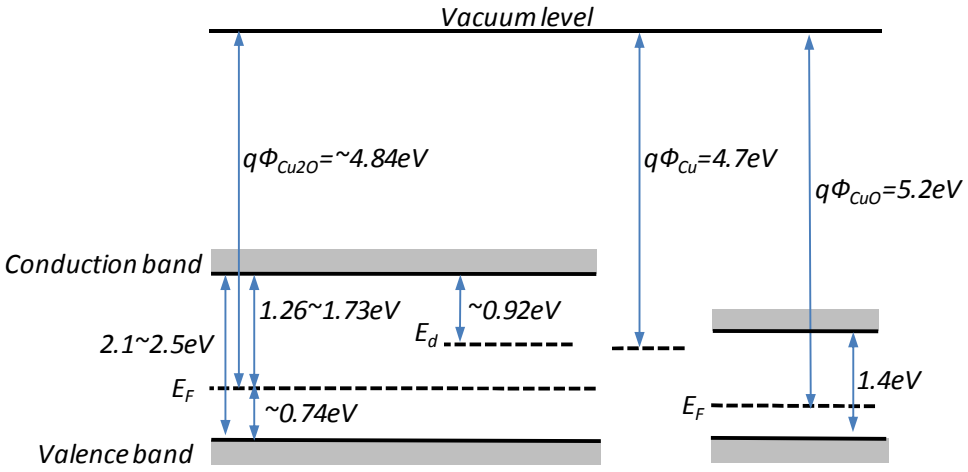


Fig. 4.28 Energy band structure of Cu_2O, Cu and CuO

4.5 P-N diode on paper substrate

In a p-n junction, the potential barrier is altered by the polarity and magnitude of applied voltage (V_a). When forward bias is applied to a p-n diode as shown in figure 4.29 (a), depletion width is reduced and potential barrier is decreased from qV_{bi} (built in voltage) to qV_{bi}-qV_a and high current flows through the diode. When reverse bias is applied, depletion width is increased and potential barrier is increased to qV_{bi}+$q|V_a|$, as shown in figure 4.29 (b), and small reverse saturation current flows until breakdown [12]. Based on this property, p-n diode can be used in rectifier and switching applications.

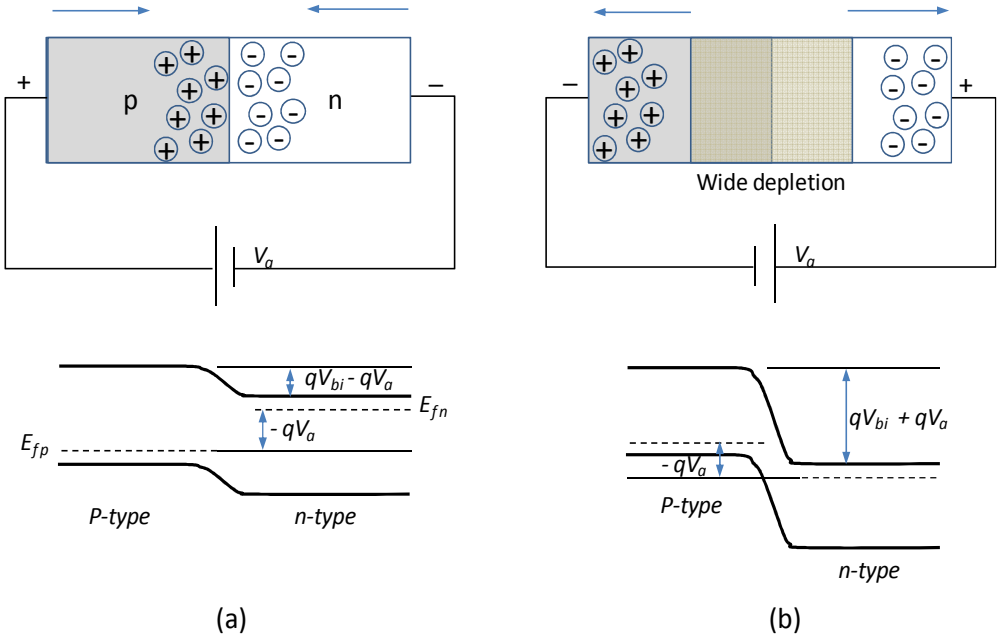


Fig. 4.29 Schematic space-charge model for p-n junction and energy-band diagram (a) forward bias (b) reverse bias.

Narushima et al. reported amorphous oxide p-n heterojunction diodes by using p-type $ZnO{\cdot}Rh_2O_3$ and n-type $InGaZnO_4$ on a plastic sheet for the application of flexible electronics [25]. In this study, the Cu_2O thin film deposited by sputtering of Cu_2O target presents p-type behavior. Even though it is not yet applicable to TFT device, this material can be utilized as the p-type semiconductor of thin film P-N diode especially for flexible substrates, due to its low process temperature. a-IGZO is a good n-type material that can be deposited at room temperature as explained in chapter 3. The carrier concentration in optimized a-IGZO films is around 10^{17} cm^{-3} and Hall mobility is approximately $20cm^2V^{-1}s^{-1}$.

In order to realize P-N diode on a paper substrate, the paper was planarized with same method in chapter 3. By using shadow mask, 100nm ITO/100nm Cu_2O/60nm a-IGZO/100nm Mo were sequentially deposited on the paper substrate by sputter system. ITO, Cu_2O, and a-IGZO were deposited with radiofrequency (RF) sputtering power of 100W, 200W, and 100W respectively at room temperature, and Mo was deposited by DC sputtering. Ohmic contact between a-IGZO and Mo and between Cu_2O and ITO is reported by another study [26, 27]. The Cu_2O-IGZO P-N diode fabricated on a paper substrate is shown in figure 4.30 (a), and the cross-section and energy-band diagram are described in figure 4.30 (b). Work-function and band-gap of ITO [28, 29], Cu_2O [30], IGZO [31, 32], and Mo [33, 34] have been obtained from literature review. Figure 4.31 presents the current density-voltage (J-V) characteristics of the P-N diode. The device demonstrates distinct rectifying characteristics with the turn-on voltage of 0.6V.

The current of diode is express by [9]

$$I = I_o(e^{qV_A/nkT} - 1) \tag{4.4}$$

Under forward bias, the exponential term is much larger than -1, therefore

$$I = I_o e^{qV_A/nkT} \tag{4.5}$$

From this equation, we can find ideality factor (n),

$$n = \frac{1}{\ln(10)SkT/q} = \frac{1}{2.3SkT/q} \tag{4.6}$$

From figure 4.32 (a), we can find the slope (S),

$$S = \frac{d\log(I)}{dV} \tag{4.7}$$

The ideality factor of Cu_2O-IGZO P-N diode on paper substrate was calculated to 1.8. When n=1, diffusion current is dominant, and when n=2, space charge recombination current is dominant [12]. Therefore, it is concluded that the prevailing current of Cu_2O-IGZO P-N diode is recombination current of carriers in the space charge region, which is induced by non-radiative recombination centers induced by dangling bond on the surface of polycrystalline Cu_2O [35].

At a high current level, the bulk resistance of the diode creates considerable voltage drop. Furthermore the contact between metal electrode and semiconductor provides a series resistance as well. The sum of these two resistances is the diode's series resistance (Rs). The Rs can be found by the plot of the voltage drop from ideal (ΔV) versus current on a linear plot as shown in figure 4.32 (b). Series resistance of this diode is 53kΩ.

When the ITO electrode is grounded, high current flows through the diode when negative bias is provided to Mo metal electrode that makes contact to the n-type IGZO

material as this induces a forward bias. On the other hand, low current of 1~100nA level flows when positive bias is provided to this Mo electrode. Thus the realized P-N diode can be utilized as a simple switching device on disposable paper substrate.

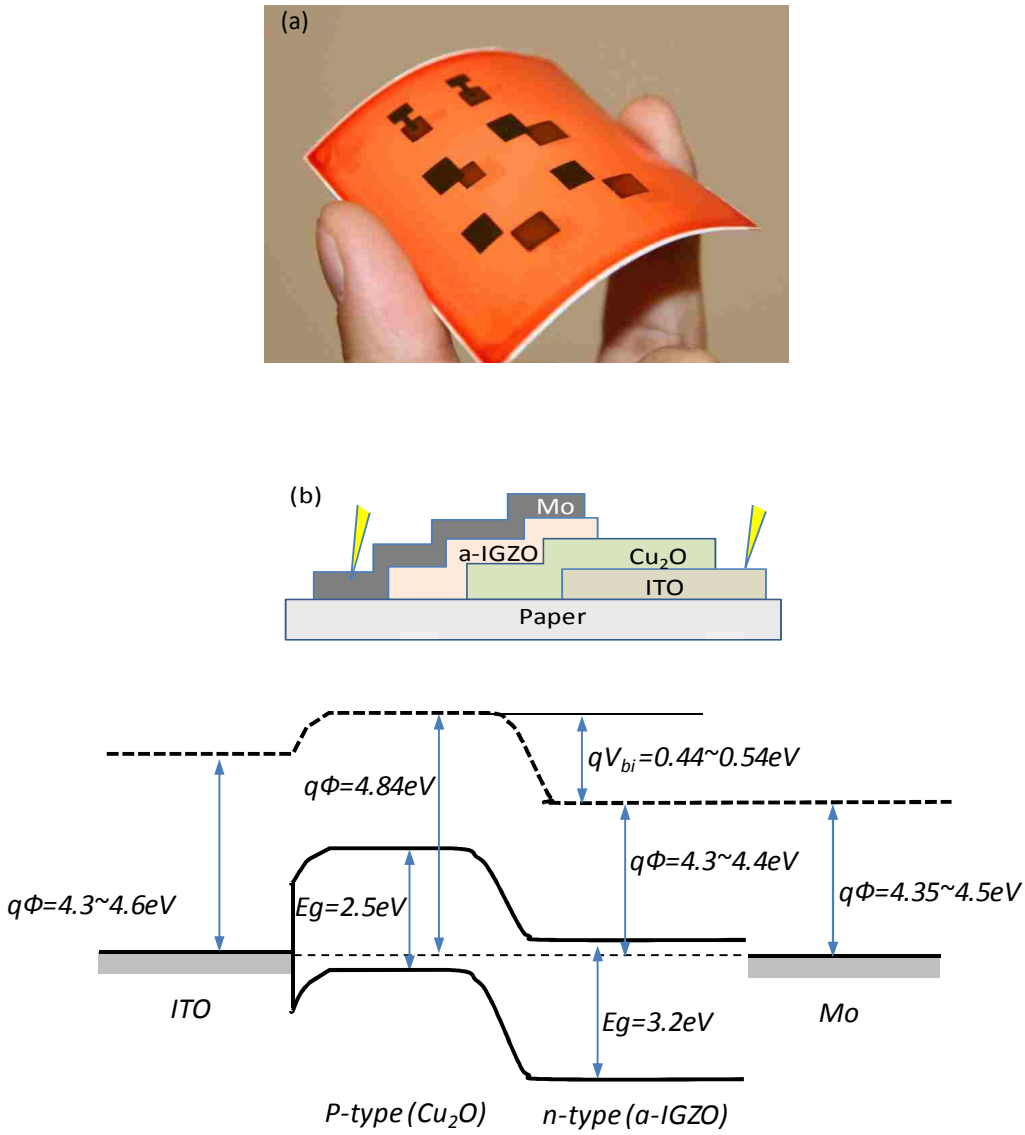


Fig. 4.30 (a) A photograph and (b) cross-section and energy band diagram of Cu_2O-IGZO P-N diode on paper substrate.

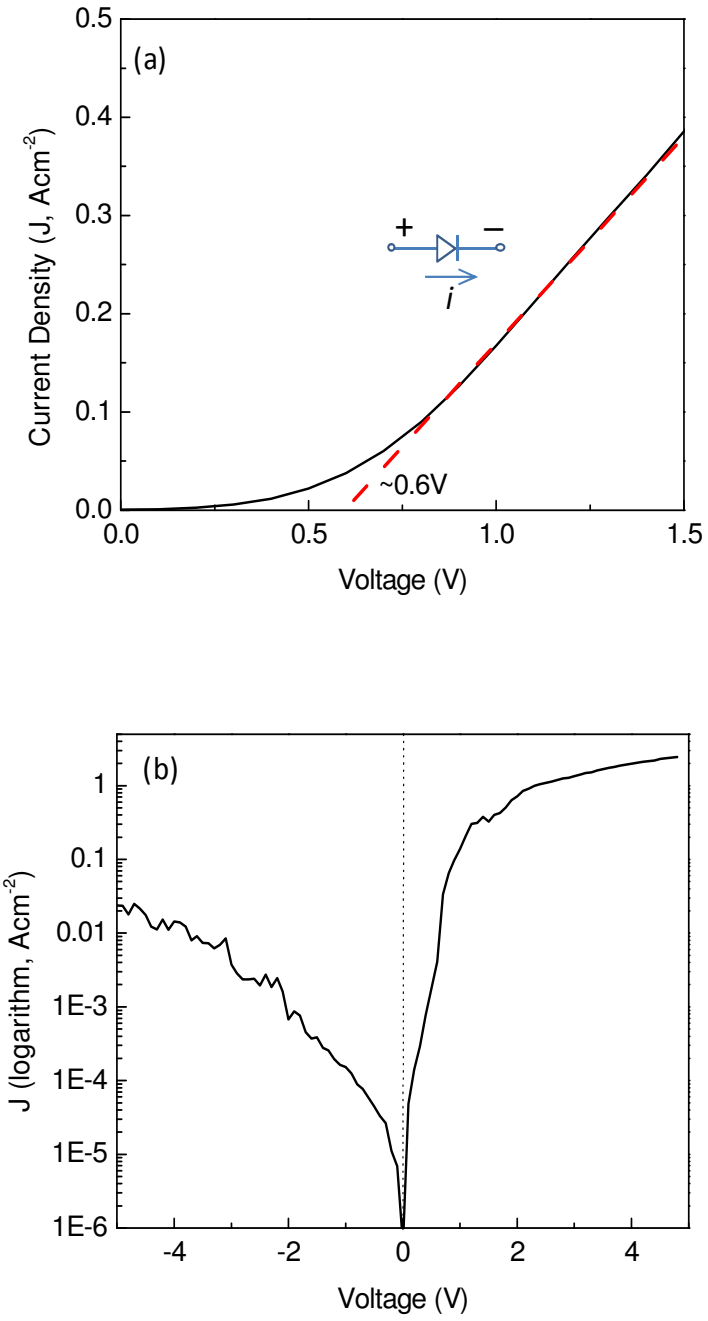


Fig. 4.31 J-V characteristics of Cu_2O-IGZO P-N diode on paper substrate, (a) linear plot (b) logarithmic plot.

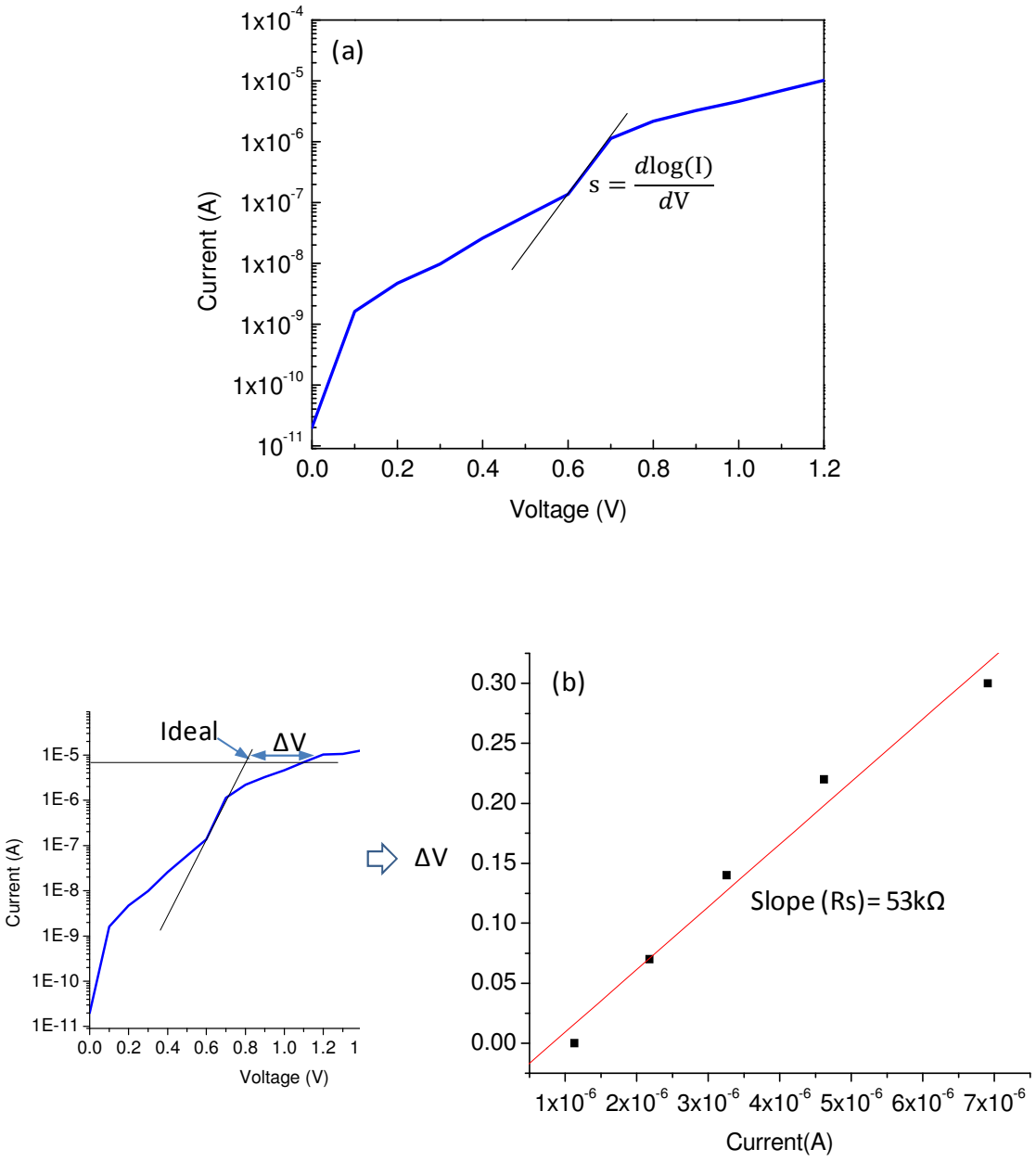


Fig. 4.32 (a) Log(I) versus V (b) ΔV versus I plot to determine Rs for Cu_2O-IGZO P-N diode.

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Chapter 5

Study of offset roll printing for thin film transistor application

It is essential to reduce manufacturing cost for the realization of flexible and disposable electronics using paper substrate. In this chapter several printing methods are introduced, and the modified offset roll printing is studied in order to realize a high resolution and high throughput printing method for thin film transistor application. A finite element analysis was done to predict the blanket deformation and to find the optimal angle of cliché's sidewall. Various etching methods were investigated to obtain a high resolution cliché and the surface energy of the blanket and cliché was analyzed for ink transfer. A high resolution cliché with a sidewall angle of 90° and an intaglio depth of 13μm was fabricated by the deep reactive ion etching method. Based on surface energy analysis, we extracted the most favorable condition to transfer ink from a blanket to a cliché. Through controlling roll speed and pressure, two inks, etch-resist and silver paste, were printed on a rigid substrate, and fine patterns of 10μm width and 6μm line spacing

were achieved. By using this printing process, top gate amorphous indium-gallium-zinc-oxide TFTs with channel width/length of 12μm/6μm were successfully fabricated by printing etch-resists.

5.1 Printing technologies

Printed electronics are being intensively pursued to decrease the manufacturing cost through the reduction of process steps and investment savings arising by the elimination of expensive equipment, such as vacuum and optical exposure systems. Photolithography in semiconductor process consists of 3 steps; 1) photoresist coating, 2) exposure with mask, and 3) develop process. In case of replacing the expensive photolithography process by printing etch-resist, the manufacturing cost can be reduced by approximately 30% through the exclusion of the expensive optical exposure system and the reduction of processing steps associated with conventional photolithography, as shown in figure 5.1 and Table 5.1.

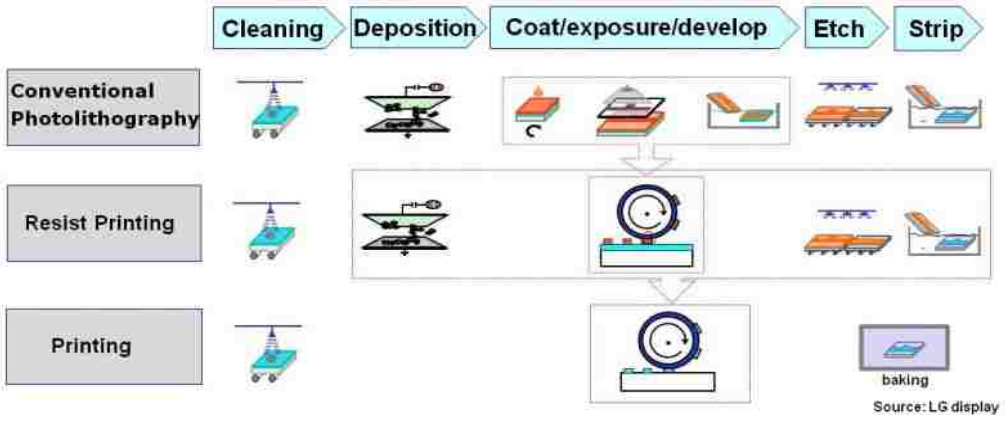


Fig. 5.1 Process schematic of photolithography, resist printing, and direct printing process [Adapted from Ref. 1].

Directly printing all layers, including electrode, semiconductor, and insulator may reduce the processing cost by more than 50%, but the material cost may significantly increase due to the use of functional inks. Inkjet, screen, gravure, stamping, and offset printing have been typically investigated for the applications of large area electronics, such as display, RFID, photovoltaic, battery, flexible electronics, and so forth [2-4]. Some of them were attempted for the mass-production of the color filter of liquid crystal display (LCD) and the electrode of plasma display. However, there is still a need for a high resolution printing method to print thin film transistors (TFTs), the basic elements of large area electronics. In Table 5.2, various printing methods are introduced and compared for printed electronics application.

Table 5.1 Manufacturing cost comparison between conventional photolithography and printing process.

	Cost reduction	Equipment	Material	Process step
Photolithography (4 Mask TFT)	-	Cleaner + CVD or SPT + PR coater + aligner + etch system	Inexpensive (gas or target + chemicals + PR)	Long (7steps/layer)
Resist printing	30%	Cleaner + CVD or SPT + printer + etch system	Inexpensive (gas or target + chemicals + PR)	Medium (5steps/layer)
Printing	50%	Cleaner + printer + oven	Expensive (functional inks)	Short (3 steps/layer)

Table 5.2 Comparison of typical printing process

Printing method	Viscosity (Pas)	Layer Thickness (μm)	Feature size (μm)	Registration (μm)	Throughput (m^2/S)
Gravure	0.01-0.2	0.1-8	75	>20	3-60
Offset	5-100	0.2-2	10-50	>10	3-30
Screen	0.5-50	0.015-100	20-100	>25	2-3
Inkjet	0.001-0.04	0.05-20	20-50	5-20	0.01-0.5

5.1.1 Gravure printing

In gravure printing, an ink fountain coats the surface of a gravure cylinder with ink. The patterns of the gravure cylinder have been etched by laser or photolithography to grasp inks in the grooves. Any excess ink in the grooves is eliminated by the doctor blade to identify the patterns before transferring ink to a substrate. According to the depth of the grooves, the amount of ink can be controlled in different locations on the substrate. The advantage of gravure printing is the high speed process using low-viscosity materials. However, the fabrication of a printing roll is costly. The metallic cylinder is very durable and it can withstand most of solvents. However, the low resolution of grooved patterns is a critical challenge.

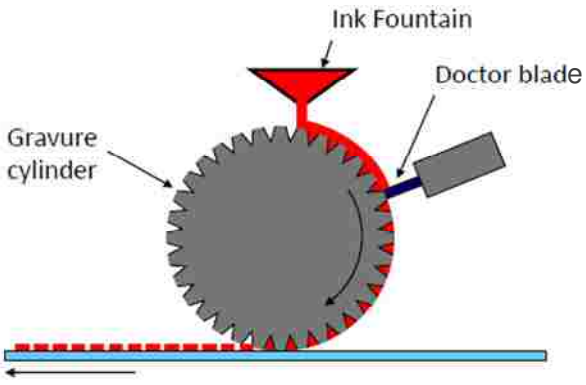


Fig. 5.2 Schematic of gravure printing [Adapted from Ref. 5].

5.1.2 Offset printing

The printing plate of offset printing consists of hydrophobic and hydrophilic areas. Hydrophobic ink is transferred to the hydrophobic area of the printing plate containing pattern images that are supposed to be printed on a substrate. Plate cylinder in figure 5.3 is wrapped with thin metal plate inscribed with the hydrophobic desired pattern images. Hydrophobic ink and water are coated on the surface of the plate cylinder in figure 5.3. The hydrophobic ink is only coated on hydrophobic surface of metal plate. Then the ink is transferred to blanket cylinder, and sequentially to the substrate. This printing technique has merits of high throughput, accurate registration, and high resolution. Therefore, display, sensor, and circuit board have been demonstrated by using this printing technique. However, hydrophobic ink development for electronic application, such as semiconductor, metal nanoparticle, and insulator are the most difficult issue.

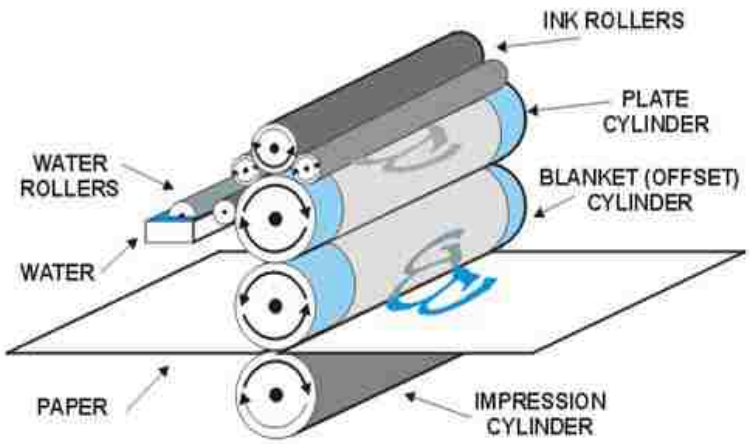


Fig. 5.3 Conventional offset lithography [Copyright; 2009 Design in the Mind].

5.1.3 Screen printing

Screen printing is a relatively simple and inexpensive method to print thick inks. High viscosity ink is used for this printing, and some conductive inks have been printed by this method in mass production. Drawback of screen printing is the limited resolution of 20~100μm. Figure 5.4 shows the example of screen printing. Screen mesh, which is usually made of stainless steel foil, is placed over the substrate. After ink is applied to the screen, a squeegee moves across the mask and forces the meshed mask to contact on a substrate. Then ink passes through the meshed mask in the open areas.

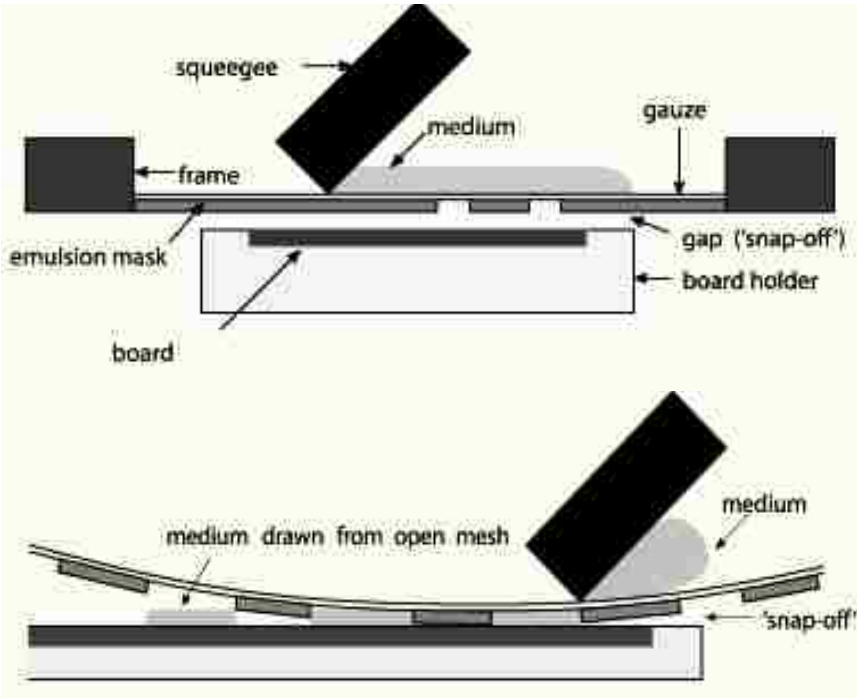


Fig. 5.4 Schematic of screen printing [Copyright; University of Bolton].

5.1.4 Inkjet printing

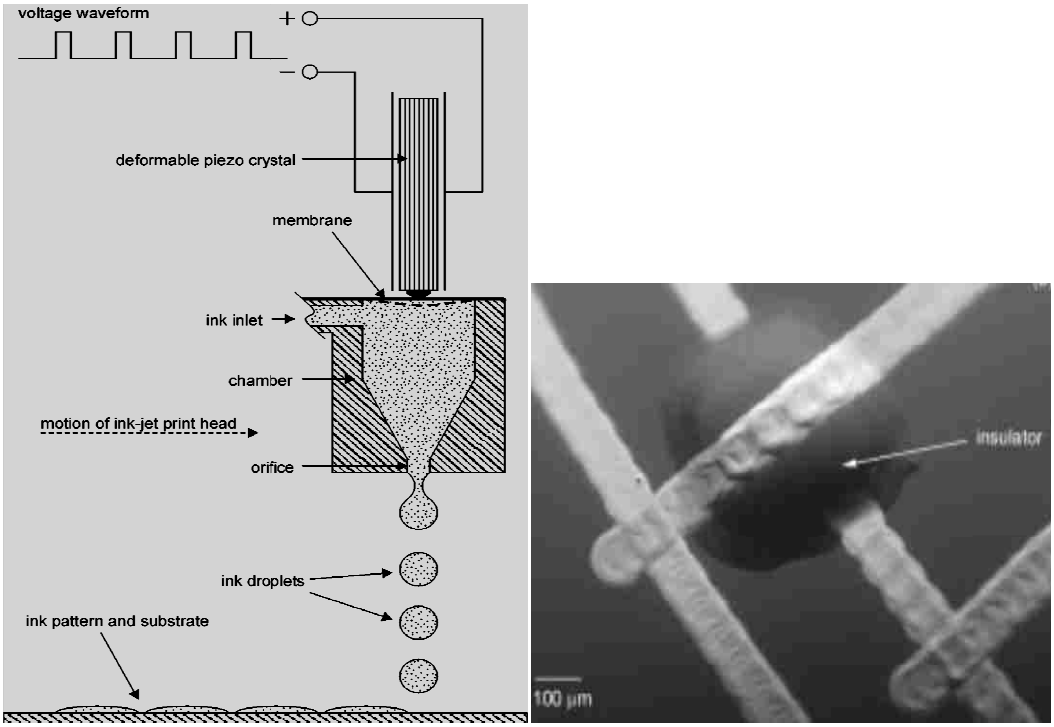


Fig. 5.5 Schematic of the piezo inkjet printing system and optical image of printed electrode and insulator [Adapted from Ref. 6].

Unlike the printing techniques introduced in previous sections of this document, inkjet printing is a non-contact printing method, which minimizes ink's contamination attributed to the mechanical contact printing. In addition, this method can reduce the waste of expensive functional inks since it only drops inks on the required areas. It is also operated by using a computer without a printing mask and thus it is less restricted by substrate shape and morphology. Several inkjet inks including metal nanoparticles and semiconductor materials have been developing for application in thin film devices. The

serious drawback of inkjet printing is the low pattern resolution of 20~50μm and wave-like edge of printed patterns as shown in optical image of figure 5.5. Therefore, the application is expected to be limited to print low resolution patterns such as the active semiconductor layer of a TFT, since the active semiconductor layer has typically a big rectangular pattern. Figure 5.5 shows piezo drop-on-demand inkjet printing system. A piezo-crystal expands according to electrical signals, and it distorts the contacted membrane causing a pressure impulse. The pressure forces a single droplet out from the orifice, and ink in the chamber is refilled by capillary action. The printed pattern is formed by multiple droplets on a substrate.

5.2 A modified offset roll printing for TFT application

In 2009, LG Display Co. proposed a modified offset printing technology in order to replace the expensive photolithography process which requires several steps to pattern one layer, and successfully demonstrated a 15" LCD where all etch-resists were printed [7]. The advantages of this method include the ability to print thin and uniform ink, and to form fine printed features and small line spacing (short channel length of TFT). However, the resolution of printed patterns is still limited by the printing plate formed by isotropic wet etch. In this study, we focused on fabricating a high resolution printing plate without pattern loss and analyzed the surface energy of blanket and printing plate for ink transfer in this modified offset roll printing. We also investigated various process issues and demonstrated the ability to print patterns and devices. The principle of this modified offset roll printing is explained in figure 5.6. An ink-coated roll blanket with low surface

energy is pressed against a printing plate with high surface energy, and undesired ink is transferred to the printing plate so that the desired patterns remain on the roll blanket. Then the patterns are printed on the substrate from the blanket by rolling. Figure 5.7 shows a modified offset roll printing system; all printing data in this study were obtained from this equipment.

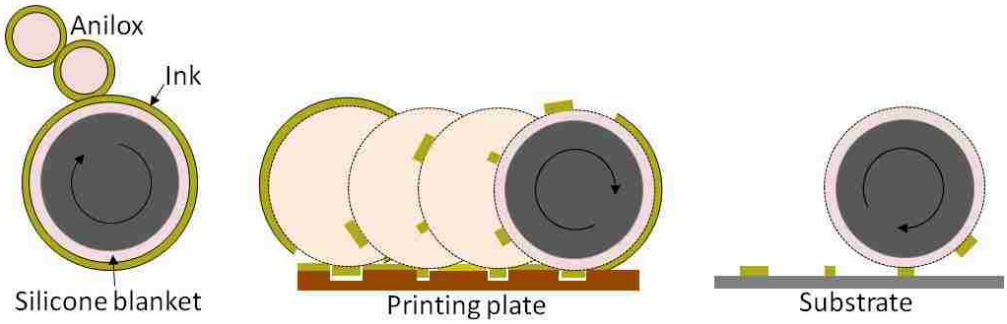


Fig. 5.6 Schematic of a modified offset roll printing.

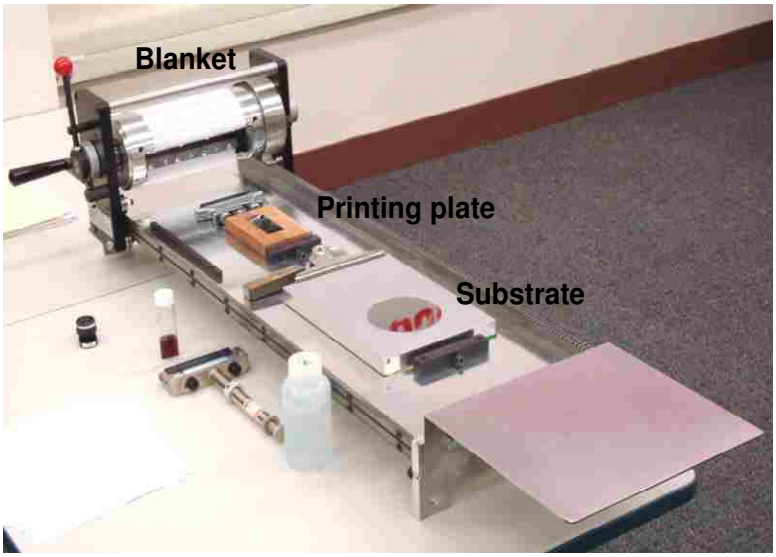


Fig. 5.7 Modified offset printing system.

5.2.1 Blanket

The blanket of this printing system needs to have a low surface energy in order to transfer the undesired ink to a printing plate with high surface energy. The blanket reported by Nam et al. consists of 3 layers as shown in figure 5.8. Polydimethylsiloxane (PDMS) with low surface energy is the outermost layer which transfers the ink; middle layer is the supporter which reduces the distortion of blanket while the cushion layer compensates printing pressure during the process. High hardness more than 50Hs and uniform thickness less than 300μm are preferred for high position accuracy in figure 5.9 [8]. Instead of soft PDMS, silicone elastomer (methyl vinyl silicone) with high hardness (~ 70Hs) was utilized as a blanket material in this study. Surface energy was measured by dynamic sessile drop method, described in section 5.2.3. The surface energy of methyl vinyl silicone is lower than PDMS for distilled water (polar) and higher for diiodometane (nonpolar, hydrophobic) solution.

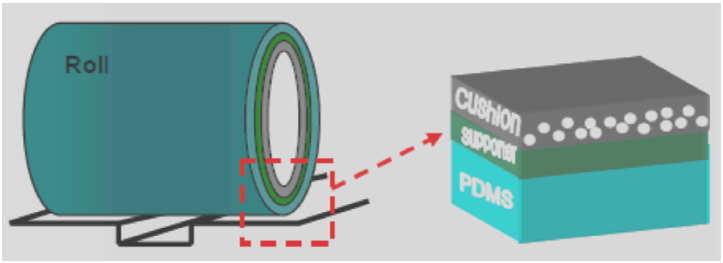


Fig. 5.8 Structure of 3 layer blanket [Adapted from Ref. 8].

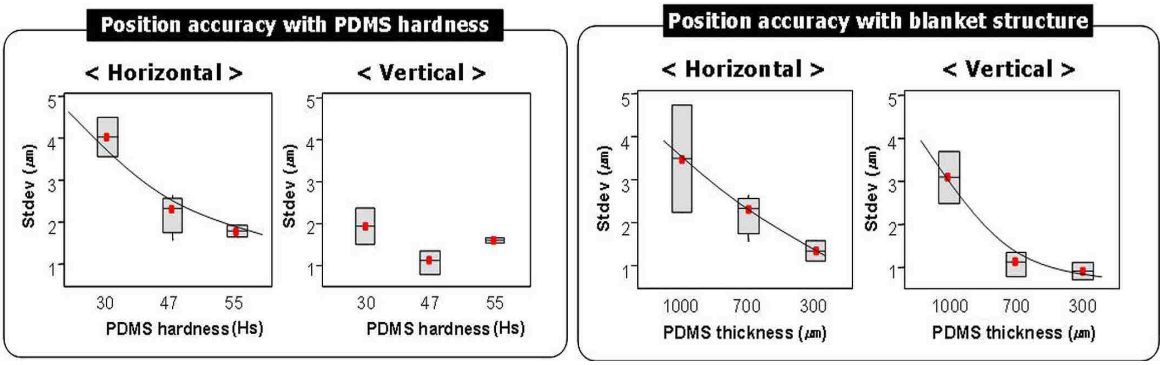


Fig. 5.9 Variation of position accuracy with PDMS hardness and thickness [Adapted from Ref. 8].

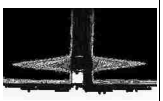
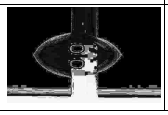
	DI water (Surface tension: 72mN/m)	Diiodomethane (Surface tension: 50.8mN/m)
Methyl vinyl silicone	*Surface Energy=7mN/m* 	*Surface Energy=16mN/m* 
PDMS(Sylgard184)	*Surface Energy=12mN/m* 	*Surface Energy=14mN/m* 
Mo	*Surface Energy=71mN/m* 	*Surface Energy=50mN/m* 
Si wafer	*Surface Energy=50mN/m* 	*Surface Energy=38mN/m*

Fig. 5.10 Surface energy measured by dynamic sessile drop method. Distilled water (polar) and diiodemethane (nonpolar, hydrophobic) are used as standard test liquids.

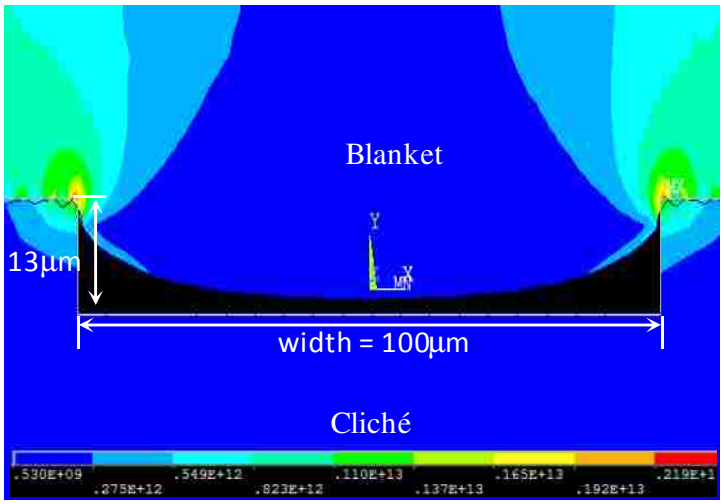
5.2.2 Printing plate (Cliché)

The printing plate (cliché) in the modified offset roll printing requires high surface energy, uniform and deep intaglios, and 90° or negative angle of intaglio sidewalls in order to print accurate patterns. Typical substrates, such as glass, quartz, and Si wafer, are available candidates for the cliché of the modified offset roll printing. In

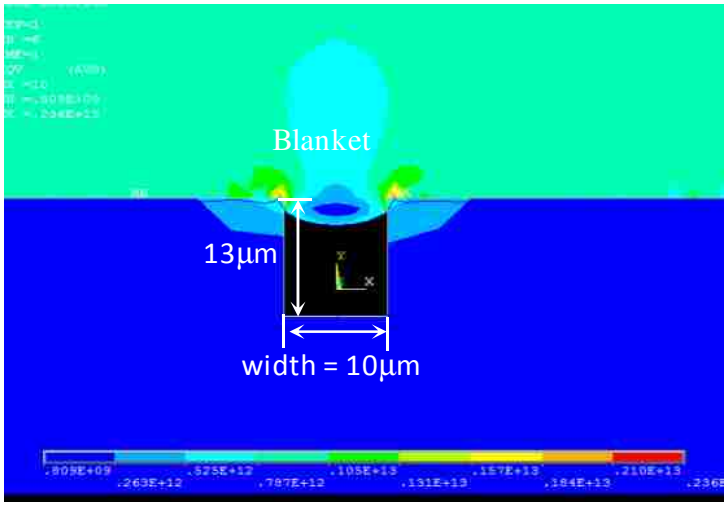
general, a soda-lime glass is inexpensive, so it has the merit of low cost; however, the etch rate and uniformity of soda-lime glass by wet etch and plasma etching cannot be well controlled due to its impurities [9]. In case of quartz, it is relatively easy to control the etch uniformity due to single crystal phase but a quartz-cliché is too brittle against roll press during the printing process [10]. On the other hand, a Si-cliché is a good choice, due to its strength during roll press and easy-etch by the wet and dry method. A positive angle of an intaglio sidewall and a shallow intaglio induce loss in the fidelity of printed patterns due to the contact of cliché's intaglio and blanket. Therefore, cliché with a deep and steep angle is quite essential in order to realize fine printed patterns and high pattern fidelity in accordance with the designed feature sizes.

A finite element analysis using ANSYS 12.1 [11] has been done to predict the contact area of the cliché sidewall with a blanket, as a function of the pressure of a roll and the angle of an intaglio sidewall. During actual experiments, the pressure used in the simulation was regulated by controlling the height of a stage located under the cliché. Figure 5.11 explains that a small pattern of 10μm produces the lesser deformation of a blanket compared to a large pattern of 100μm. Thus the largest pattern width of 100μm in a typical TFT design is selected for the simulation of an unfavorable condition in figure 5.11 and 5.12. According to the finite element analysis of the contact shown in figure 5.12(b) and 5.13(a), the conventional cliché having positive sidewall angle (θ) of 45° and 60° isn't able to print fine featured patterns because intaglios can contact the blanket due to pressure during rolling; thus cliché's intaglio takes ink off from the blanket. Accordingly, the edges of printed pattern are not clear and the size of printed patterns is

smaller than the designed one. A sidewall angle of 90° only overlaps 0.8μm, but 60° and 45° overlap 2.1μm and 3.8μm respectively in the pattern width of 100μm under the pressure induced by a 5μm vertical motion of the stage towards the blanket, as shown in figure 12 and 13(a). When blanket contacts both sidewalls, then the sidewall angle of 90° causes a pattern dimension loss of 1.6μm, but 60° and 45° lose 4.2μm and 7.6μm respectively in the width of the actual printed patterns. Meanwhile, the maximum stress of a blanket contacted with a cliché reveals negligible difference in figure 13(b). Consequently, it is obvious that the sidewall angle of 90° is advantageous for printing accurate patterns in this modified offset roll printing method.

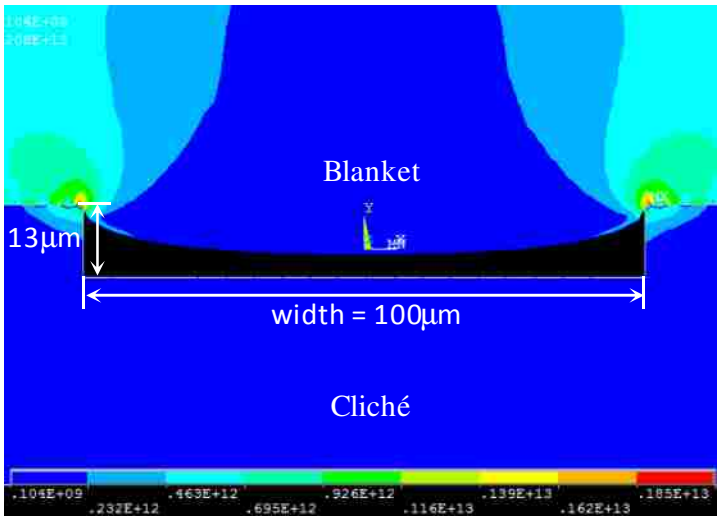


(a)

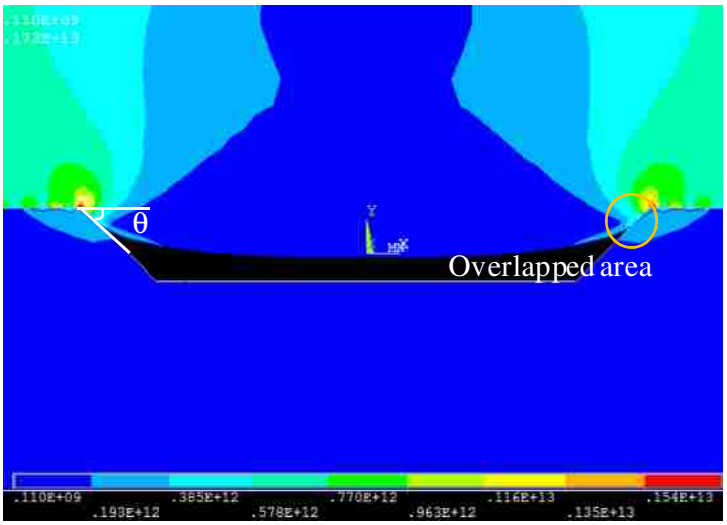


(b)

Fig. 5.11 Finite element analysis to investigate blanket deformation with the variation of cliché width (a) 100µm (b) 10µm, under 10µm vertical motion of the stage towards the blanket.



(a)



(b)

Fig. 5.12 Finite element analysis to investigate overlapped area between a blanket and the sidewall of cliché with the variation of sidewall's angle (θ) (a) θ = 90° (b)θ = 45° (conventional cliché angle), under 5µm vertical motion of the stage towards the blanket.

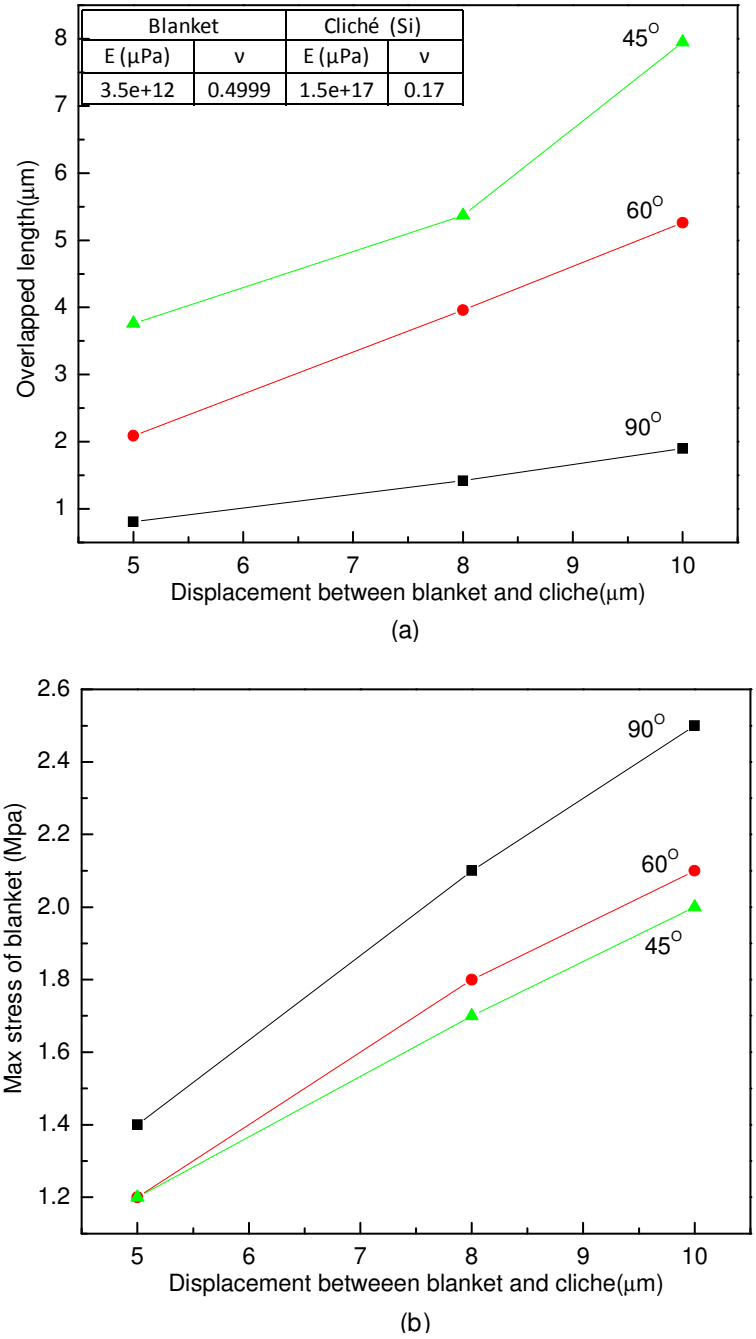


Fig. 5.13 Finite element analysis (a) overlapped length between a blanket and the sidewall of cliché (b) the maximum stress of the blanket contacted with a cliché as a function of roll pressure (controlled by the height of cliché stage). The angle of sidewall of a cliché split with 45°, 60°, and 90°. The pattern width used for simulation is 100μm.

Chang et al. reported the fabrication method of a fine cliché using a glass substrate that was etched in two steps using HF solution as shown in figure 5.14. This etching method is isotropic, thus it induces pattern losses in lateral directions, resulting in cliché patterns that are larger than the designed patterns. In addition, the depth of the cliché is limited to 5μm as shown in figure 5.14, which requires careful pressure control during the printing process [7].

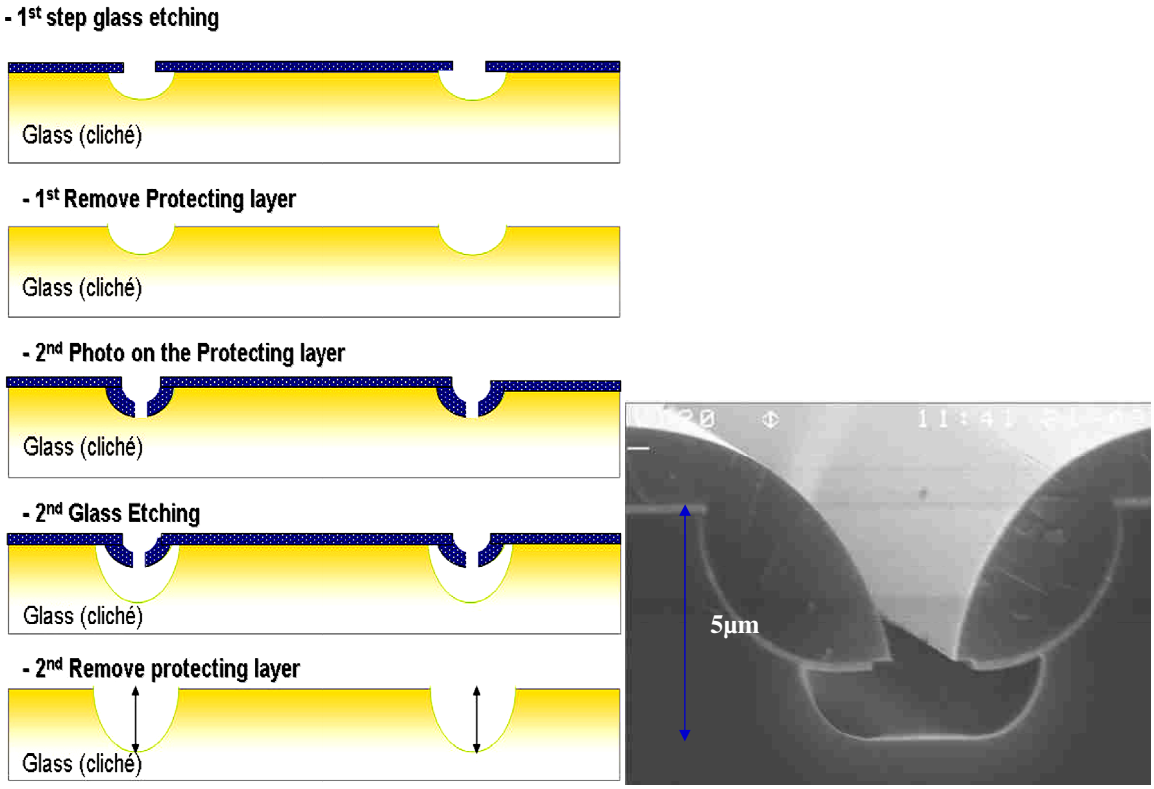


Fig. 5.14 The process step to fabricate the glass printing plate by using two step etching and a cross sectional view of the multi-etched cliché plate [Adapted from Ref. 7].

Table 5.3 Etching methods and results for Si-cliché.

Etch methods	Results
Laser	- Etch profile is not clear but rough due to cracking by thermal stress
Photolithography + Wet etch	- Pattern loss (isotropic etch) - Etch depth limitation
Photolithography + Dry etch(PE)	- Pattern loss (isotropic etch) - Etch depth limitation
Photolithography + Deep RIE	- No pattern loss - Angle 90°, depth(up to tens of micron)

In order to overcome these problems and obtain a steep angle, various etch methods, such as wet etch, laser ablation, and dry etch, were investigated to pattern a Si-cliché. The results are summarized in Table 5.3. Laser ablation induces cracks by the rapid heating during laser processing, which causes large temperature gradients near the Si surface [12]. Wet and plasma etching (PE) present isotropic etch, so there is the pattern loss in lateral direction. Figure 5.15 is the example of PE dry-etched cliché. Metal layer (Al) was deposited and patterned to be used as the etch-mask. Etched depth is approximately 6μm, and metal and SiO_2 layers are maintaining their dimensions even though the Si layer underneath them is isotropically etched; the Si layer exhibits a dimensional loss of 3μm as shown in figure 5.16(b). However, the overhang of the patterns was collapsed after roll printing as shown in figure 5.15(b), so this cliché cannot be used repeatedly. Among these techniques, the deep reactive ion etching (RIE) exhibits excellent results with a sidewall angle of 90° and an intaglio depth of 13μm just by using simple photolithography, as shown in figure 5.16(c) and 5.16(d). Deep RIE is known to

etch deep cavities with relatively high aspect ratio through fluoropolymer that passivates and protects the sidewalls [13]. Compared to the designed features, there is no pattern loss and the angle of intaglios is approximately 90°. These results are quite appropriate for the cliché of the modified offset roll printing method.

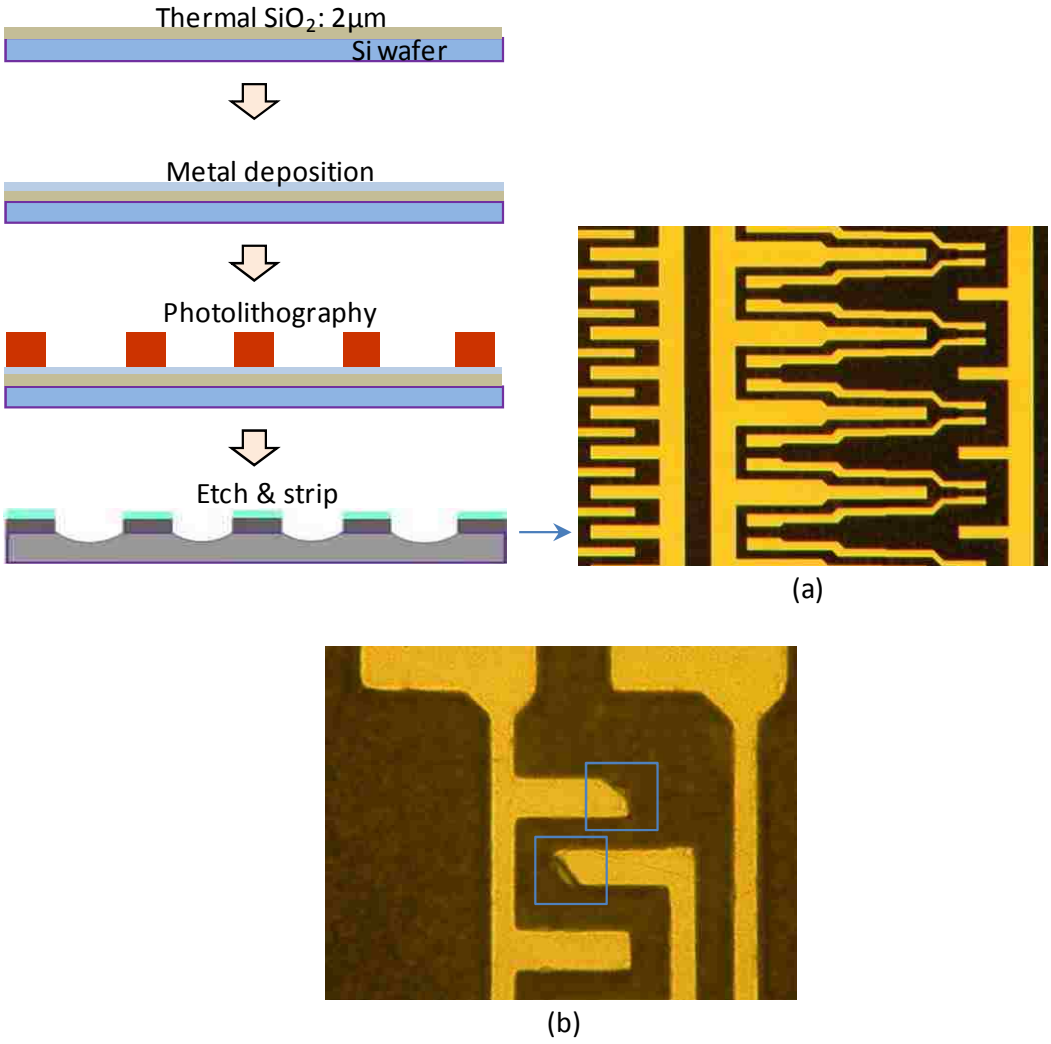


Fig. 5.15 Schematic of cliché fabrication method by using PE mode dry-etch (a) Optical image of cliché (b) shoulder of metal layer worn out after rolling

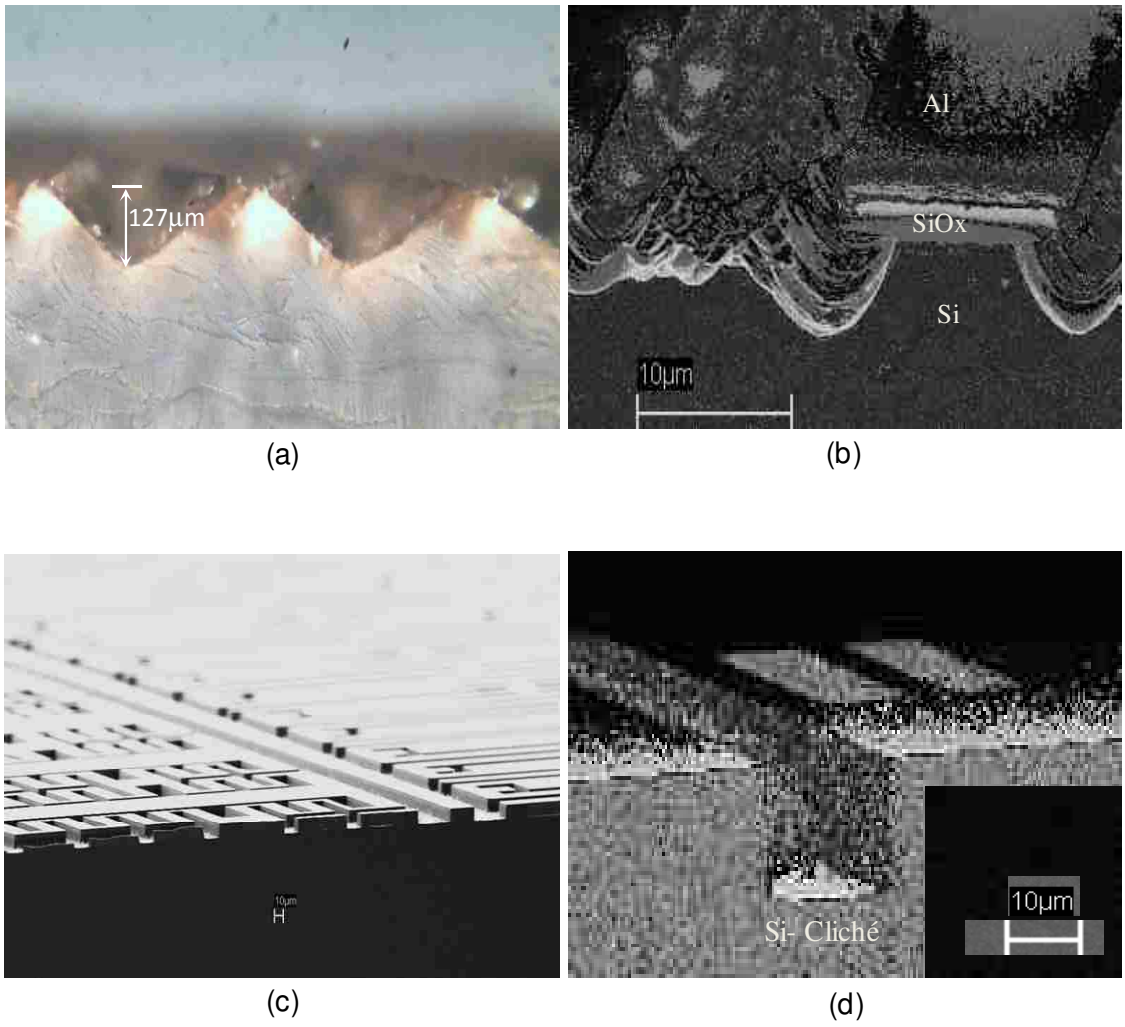


Fig. 5.16 (a) Optical cross-section of a conventional flexo plate, (b) SEM image of the Si-cliché etched by PE mode dry-etch, (c) and (b) SEM images of the Si-cliché etched by the deep RIE.

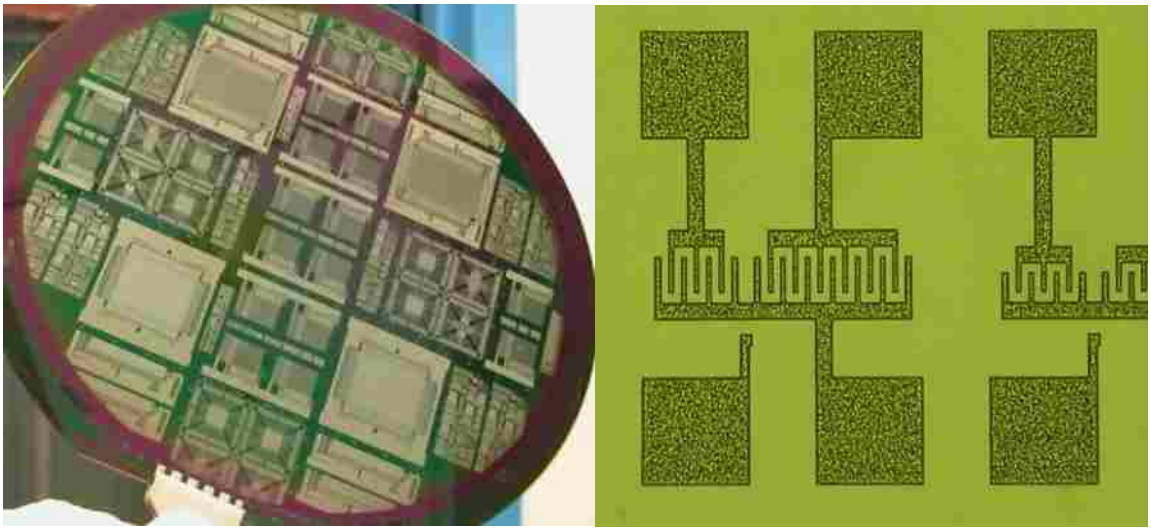


Fig. 5.17 Optical images of the Si-cliché etched by the deep RIE.

5.2.3 Surface energy analysis

In the modified offset roll printing, a cliché contacts the ink of the rolling blanket, and then the ink separates from the blanket. The main principle of this printing is to use the surface energy difference of a cliché and a blanket with ink. A strong adhesion between a cliché and ink is required to transfer ink from a blanket to a cliché. Therefore, we measure the surface energies of each material and interpret the relationship between two surfaces, cliché and blanket, to efficiently print ink. The dynamic sessile drop method in figure 5.18 using contact angle hysteresis is utilized to measure the surface energy of blanket, cliche, and thin films. Distilled water (polar) and diiodemethane (nonpolar, hydrophobic) are used as standard test liquids [14]. Table 5.4 shows measurement results and their surface energy calculated by using following equation [15],

$$\gamma_{sl} = \gamma_{lv}(\cos\theta_r - \cos\theta_a)\frac{(1+\cos\theta_a)^2}{(1+\cos\theta_r)^2 - (1+\cos\theta_a)^2} \tag{5.1}$$

where γ_{sl}; solid-liquid surface energy, γ_{lv}; liquid-vapor surface tension, γ_{sv}; solid-vapor surface tension θ_a; advancing contact angle, and θ_r; receding contact angle.

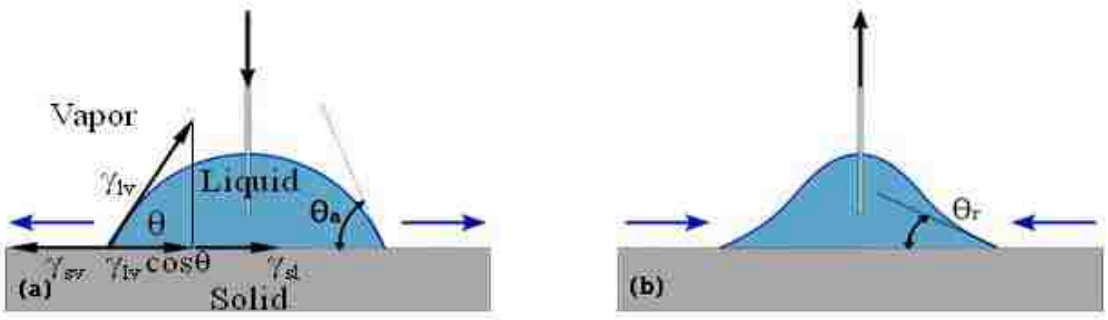


Fig. 5.18 Dynamic sessile drop method.

Table 5.4 Advancing and receding contact angles on blankets (Methly-vinyl-silicone, PDMS), cliché (Si), and thin film (Mo, SiO_2) and their surface energy measured by the water droplet. α is defined by $\gamma_{lv}(1+\cos\theta_{a(s1)})$, β is defined by $\gamma_{lv}\cos\theta_{a(s2)}$.

Materials	Distilled water (surface tension:72mN/m)					Diiodomethane (surface tension:50.8mN/m)				
	advancing angle (°)	receding angle (°)	surface energy (mN/m)	α	β	advancing angle (°)	receding angle (°)	surface energy (mN/m)	α	β
Methyl vinyl silicone	123	44	7	33		95°	46°	16	46	
PDMS (Sylgard184)	117	75	12	39		101°	50°	14	41	
Mo	13	9	71		70	11°	7°	50		50
SiO_2	14	12	71		70	46°	37°	42		35
Si wafer	64	60	50		32	54°	41°	38		30

In Table 5.4, methyl-vinyl-silicone and polydimethylsiloxane (PDMS) are blanket candidates; Si is a cliché; and molybdenum (Mo) and silicon dioxide (SiO_2) are thin films used to modify the surface energy of a Si-cliché. The blanket materials of methyl-vinyl-

silicone and PDMS retain low surface energy, and the surface energy of Si-cliché is higher than that of the blanket materials. For an ink to be separated from a blanket, we need to consider the adhesion strength between ink and the blanket. Surface energies are linked with the failure of adhesive bond. Adhesion failure involves the creation of new surfaces. The adhesion strength between two materials can be defined by the required energy to separate two materials [16]. When separating two materials, their interface changes into two new surfaces creating new surface energies with air. Thus the strength of adhesion (*Wa*) can be expressed by the surface energy difference between the two status; specifically, by subtracting the surface energy of contacted two materials from the surface energies of separated two surfaces [16],

$$Wa = (\gamma_{sv} + \gamma_{lv}) - \gamma_{sl} \tag{5.2}$$

When ink is transferred from s1 (blanket's surface) to s2 (cliché's surface) in the modified offset roll printing of figure 5.19, the surface tension of ink (s3, γ_{lv}) should be considered to separate the ink from the remaining ink on the blanket. Thus the adhesion energy between ink and s2 surface should be stronger than the total energy of blanket side, the sum of surface tension of ink (γ_{lv}) and the adhesion energy between ink and s1 surface. So the surface energy relationship to transfer ink from a blanket to a cliché can be expressed by the following equation,

$$(\gamma_{s1v} + \gamma_{lv} - \gamma_{s1l}) + \gamma_{lv} < \gamma_{s2v} + \gamma_{lv} - \gamma_{s2l} \tag{5.3}$$

From Young's equation [17], $\gamma_{sv} = \gamma_{sl} + \gamma_{lv}\cos\theta_a$, this equation can be simplified as follows:

$$\alpha = \gamma_{lv}(1 + \cos\theta_{a(s1)}) < \gamma_{lv}\cos\theta_{a(s2)} = \beta \tag{5.4}$$

When this condition is satisfied, ink will be effectively transferred from a blanket to a cliché under rolling. Through this equation, it is found that the β value of a Si-cliché is smaller than the α value of blanket materials in Table 5.4, so we can estimate that the surface energy of Si itself is insufficient to remove ink from the blanket, but the β value of Mo and SiO_2 thin films is sufficient to transfer ink. In the case of diiodomethane, only the β value of Mo is bigger than the α value of the blankets. Therefore, in order to increase the surface energy of the Si-cliché, we deposited a Mo thin film on the top of the Si-cliché. The Si-cliché with a Mo coating clearly removed ink from the blanket when we printed etch-resist ink as shown in the next section, but a Si-cliché without Mo coating couldn't remove ink well.

After moving over the cliché, any remaining ink on the blanket can be transferred easily to substrate as shown in figure 5.19(b) if the adhesion between substrate and ink is stronger than the adhesion between blanket and ink. It is important to note that in both transfer cases, i.e. from blanket to cliché and from blanket to substrate, the surface tension of the ink should be larger than the adhesion between the blanket and ink, otherwise, the ink may be split before transferred.

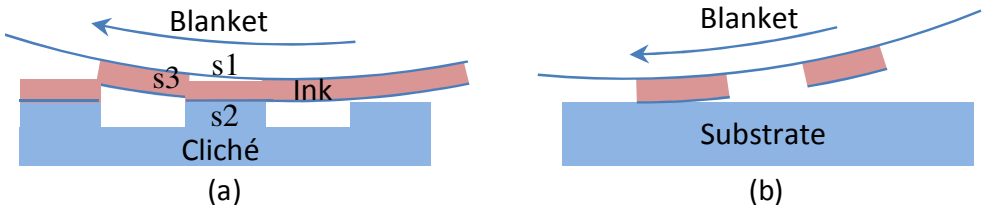


Fig. 5.19 Concept of ink transfer (a) from a blanket to a cliché, (b) from a blanket to a substrate.

5.2.4 Design of test patterns

In order to identify the printing capability, test patterns, including line width and space resolution, straightness, and directional and shape dependence, need to be designed. In the following figure 5.20, the line width resolution (x,y direction) of 2~100 ㎛, space resolution between lines of 2~100 ㎛, contact hole of 2~40 ㎛, maximum line length & straightness of 100~4000 ㎛, and resolution of "Γ" shape of 2~50 ㎛ were designed for offset roll printing.

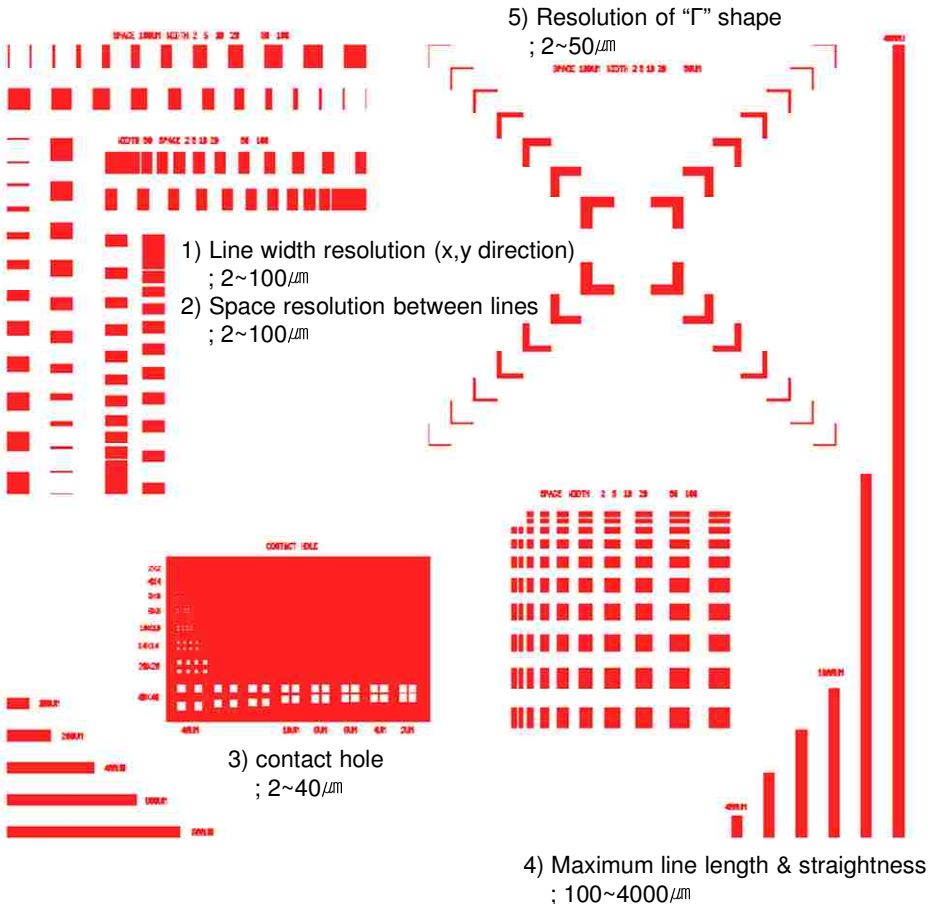


Fig. 5.20 Design of test patterns for a modified offset roll printing.

5.2.5 Ink

Ink in the modified offset printing should be easily separated by the surface energy difference between a blanket and a printing plate. Furthermore, after roll press, the ink needs to be clearly removed from the blanket. At the stage of developing inks, adhesion force relationship among blanket, ink, and cliché needs to be analyzed by using surface energy measurement as described in chapter 5.2.3. Metal nanoparticle ink, organic dielectric, and etch-resist are more applicable than semiconductor materials for the modified offset roll printing; since those materials are not very susceptible to minor contamination attributed to contact type printing and require the excellent patterning property. Considering that inkjet printing is non-contact type method, inkjet printing could be suitable for the printing of active semiconductor layer. However, the inkjet materials have not satisfied the requirement of device characteristics so far. Instead of inkjet printable semiconductor materials, a-IGZO deposited at room temperature by sputter is utilized in this work.

Figure 5.21 shows the concept of the proposed TFT process using the modified offset roll printing and the liftoff process of oxide semiconductor. In order to realize this concept, printing etch-resist and silver paste are explored at the following section. Instead of developing a new ink, commercial resists (AZ 5214, AZ N4035) with 25% Novolak resin were utilized as a printable etch-resist. In order to maintain the solution condition during roll printing process, this resin was modified by mixing a high boiling point solvent (dibutyl phthalate, boiling point 340^{o}C) to retard the fast drying rate of the ink. In addition, silver paste was also evaluated as the direct metal patterning.

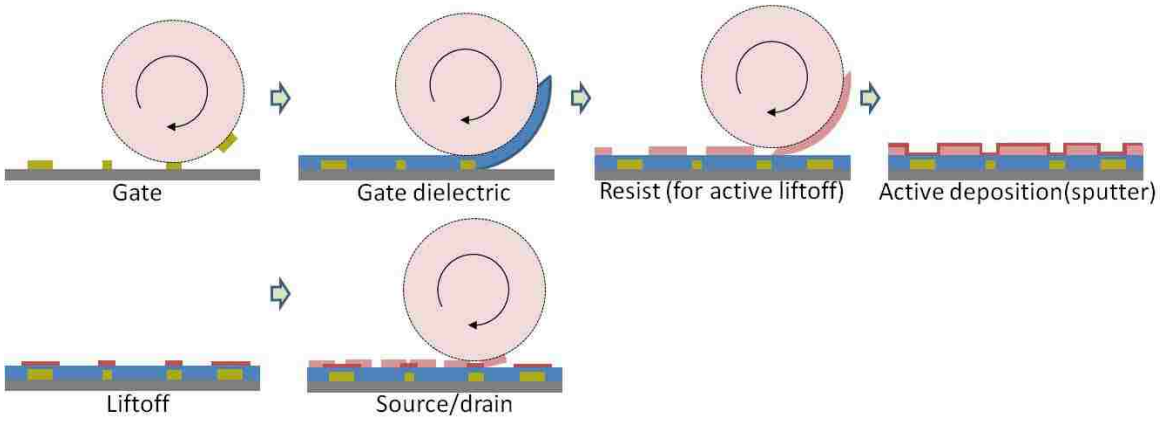


Fig. 5.21 Concept of TFT fabrication process using the modified offset roll printing and the liftoff of semiconductor.

5.2.6 Printing process optimization and results

The main process parameters in the modified offset roll printing are roll speed and pressure. A fast rolling speed induces a high rolling resistance [18]. Therefore, the pattern's edge of vertical direction with rolling direction is wave-like unlike the parallel patterns, as shown in figure 5.22(a). This is attributed to the temporary deformation of a soft blanket by the increase of friction due to the high speed rolling(~100mm/sec). The deceleration of the roll speed (~10mm/sec) decreases this defect by reducing the friction of the blanket. The other important factor is roll pressure. Figure 5.22(b) shows blank areas in the center of square patterns in the left side, but squares are gradually filled with ink toward the right side. The result orginates from the non-uniform pressure of a roll when the roll blanket contacts a cliché; explicitly, the blanket contacts the intaglios of a cliché by hard pressure in the left side, thus the ink supposed to remain on the blanket is

transferred to the cliché, not to the substrate. Therefore, we regulated the presssure by controlling the height balance of a stage located under the cliché.

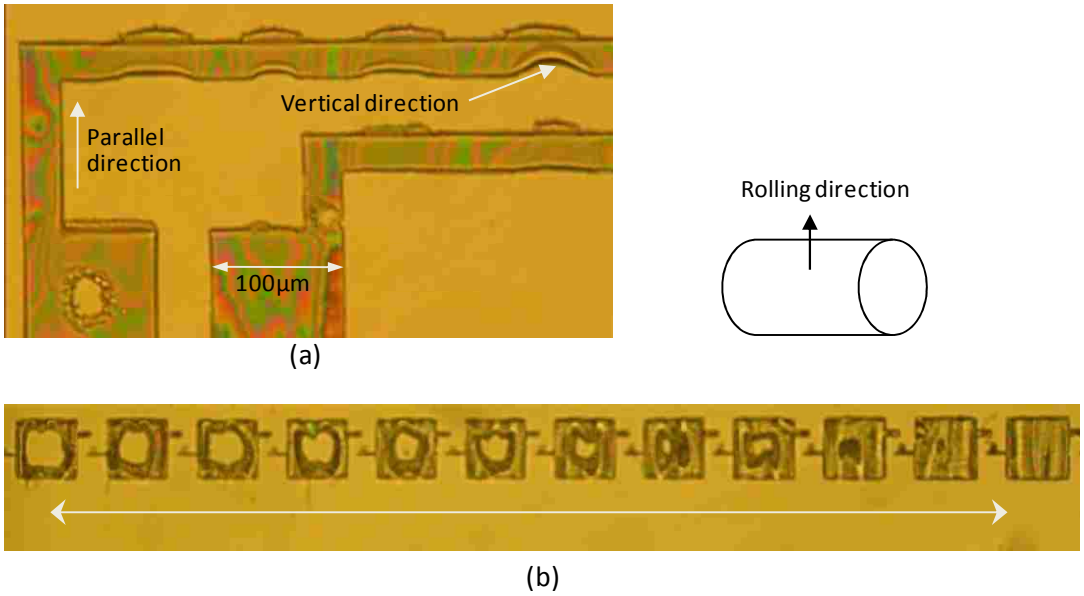


Fig. 5.22 (a) Edge shape according to the rolling direction under high rolling speed (~100mm/sec) (b) missing patterns by non-uniform rolling pressure.

Through controlling roll pressure and speed, we successfully printed etch-resist-ink at a high resolution: line width of 10μm and line spacing of 6μm. The edge of printed patterns are relatively clear and the size of printed patterns is similar to the designed one as shown in figure 5.23. Figure 5.24(a) presents the printed etch-resist-ink and figure 5.24(b) shows Mo patterns by using this etch-resist printing. Consequently, we were able to reduce 3 steps (coating, exposure, and develop) of photolithography to one printing step. The direct printing of an electrode ink, such as silver paste, was also evaluated.

Patterning characteristics of the silver paste as shown in figure 5.25 are excellent but the silver paste agglomerated in some areas. We believe that this is the property of silver paste and that a nanoparticle silver ink can solve this issue. By using the resist printing method, we successfully fabricated a-IGZO TFTs (channel width/length= 12/6μm) having the electrical transfer curve shown in figure 5.26. This result shows the promising potential of the modified offset printing.

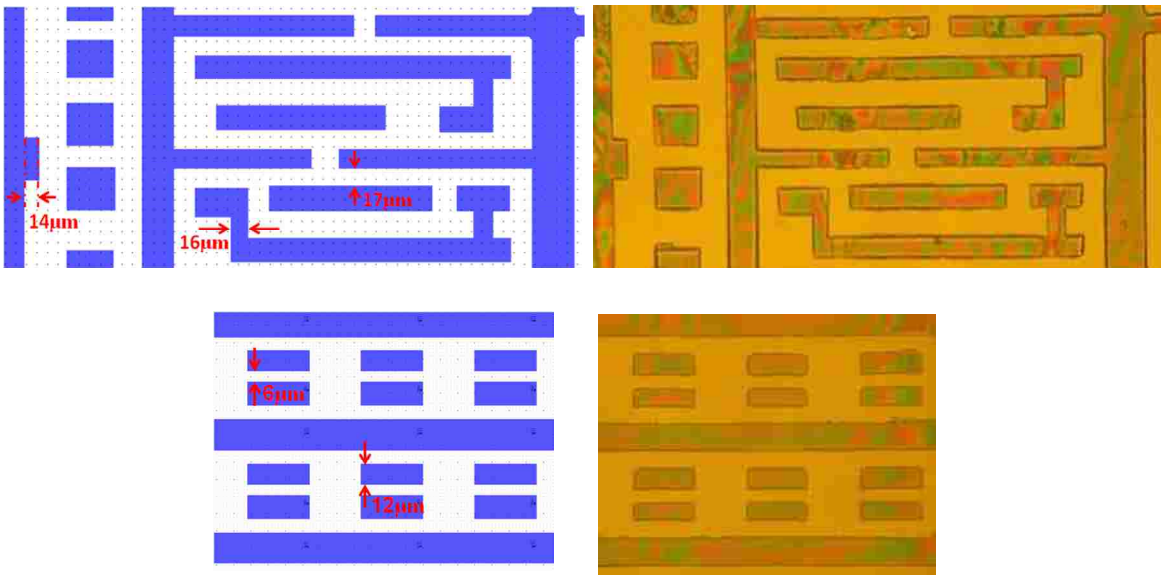


Fig. 5.23 Design of patterns (left) and corresponding printed etch-resists (right).

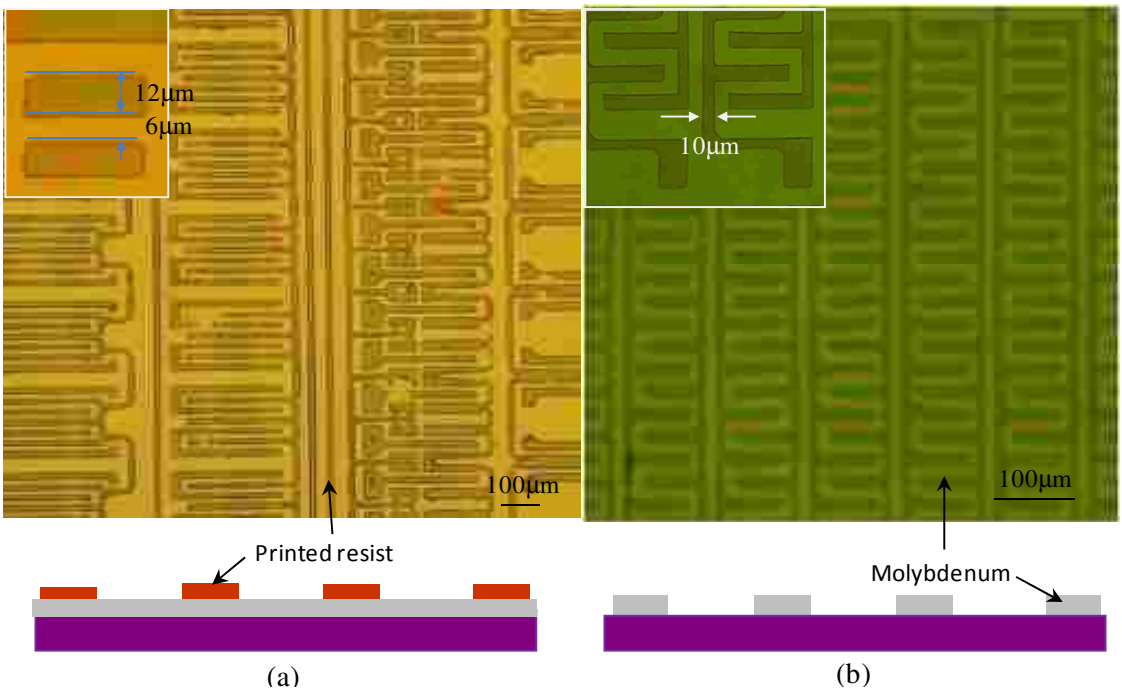


Fig. 5.24 (a) Printed etch-resist (b) molybdenum pattern using the printed etch-resist.

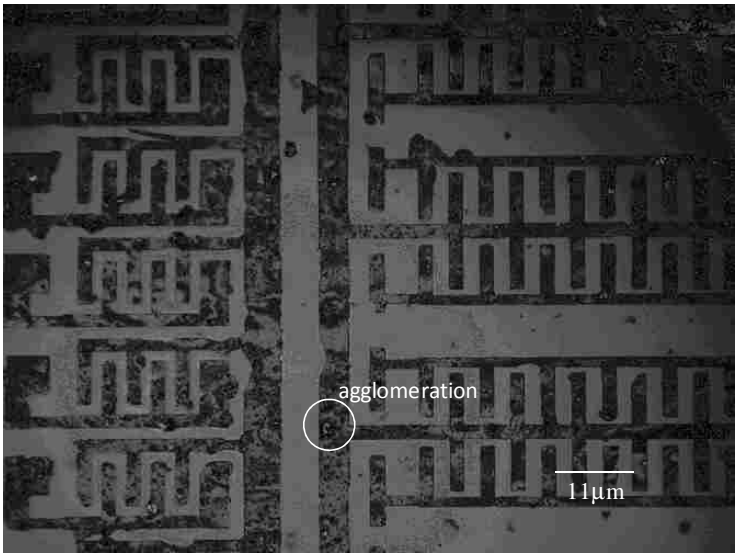


Fig. 5.25 Optical microscope image of printed silver-paste.

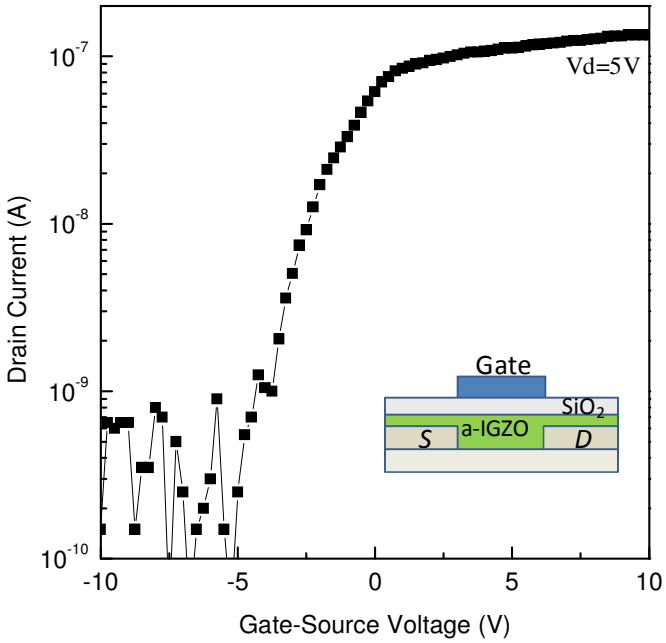


Fig. 5.26 Electrical transfer curve of a-IGZO TFT fabricated by using the printed etch-resist.

5.3 A novel imprint lithography

It is known that imprint lithography offers excellent resolution at submicron level, as shown in SEM image of figure 5.27. However, most of research has focused on the patterning of UV curable etch-resist. A mould with desired patterns presses the UV curable polymer and then the polymer is cured by UV exposure. After releasing the mould, dry etch is used to eliminate the residue of polymer. Since materials in this printing method are exposed to plasma during dry etching to remove the residue of printed patterns, materials affected by plasma (mostly oxygen plasma) can not be used in impint lithography. In principle, metal or semiconductor layer is deposited on a substrate and UV curable polymer is coated on the layer.

The disadvantages of this process are 1) difficulty to develop UV curable funtional inks such as metal and semiconductor inks, 2) necessity of dry etch to remove the residue of polymer. In this chapter, a novel imprint lithography depicted in figure 5.28. The new method is proposed for the application of a variety of materials. The principle of the proposed method is similar to the modified offset roll printing in the section 5.2. Ink is coated on the surface of PDMS stamp and then pressed on the cliché with undesired pattern area. Undesired ink is removed by hydrophilic cliché from hydrophobic PDMS, and then desired patterns on the PDMS stamp is transferred to substrate by another stamping. The merit of this process is easy to align layer to layer.

In order to fabricate hydrophobic stamp, PDMS (Sylgard 184) was coated on a wafer substrate. PDMS was mixed by a hardening agent with the ratio of 10:1 and then diluted by toluene with the ratio of 1:1, since it is difficult to spin coat PDMS on the wafer due to high viscosity of 4000mPa·s. The diluted PDMS was filtered to eliminate any particle and spin coated with 3000rpm/30sec. Uniform 6μm thick PDMS was coated on wafer and cured at room temperature for 2 days. In case using hot plate or oven to cure PDMS, small voids were generated in PMDS. For the fabrication of cliché, 1μm thick aluminum was deposited on an oxidized wafer and patterns were created by photolithography using dry etch with the mixed gas of CF_4 and O_2.

Resist ink (AZ 5214) with 25% Novolak resin was evaluated by this principle on a rigid substrate. Patterning characteristics were excellent as shown in figure 5.28. However, it was difficult to obtain uniform images in whole area due to the presence of a void between the two plates.

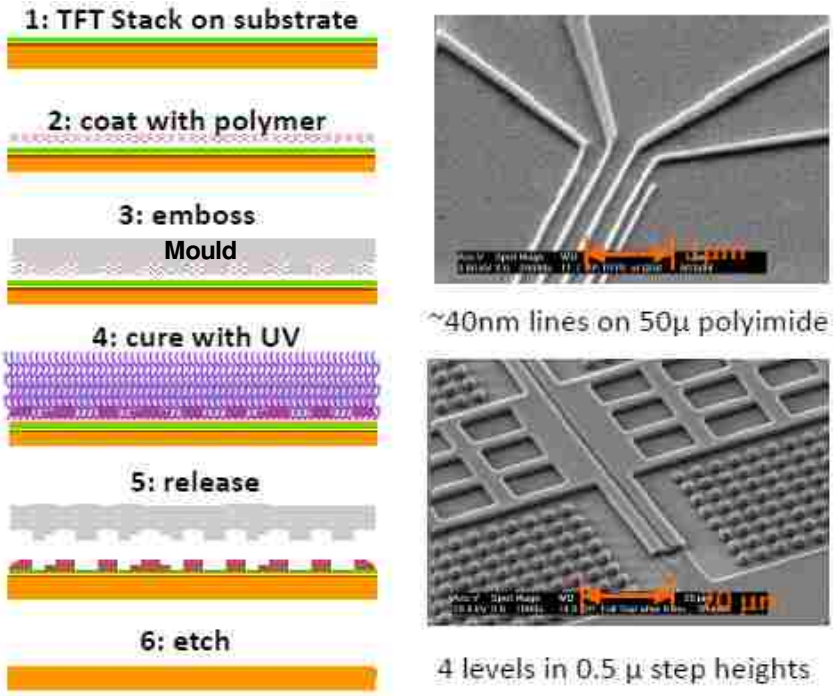


Fig. 5.27 Imprint lithography process [Adapted from Ref.19].

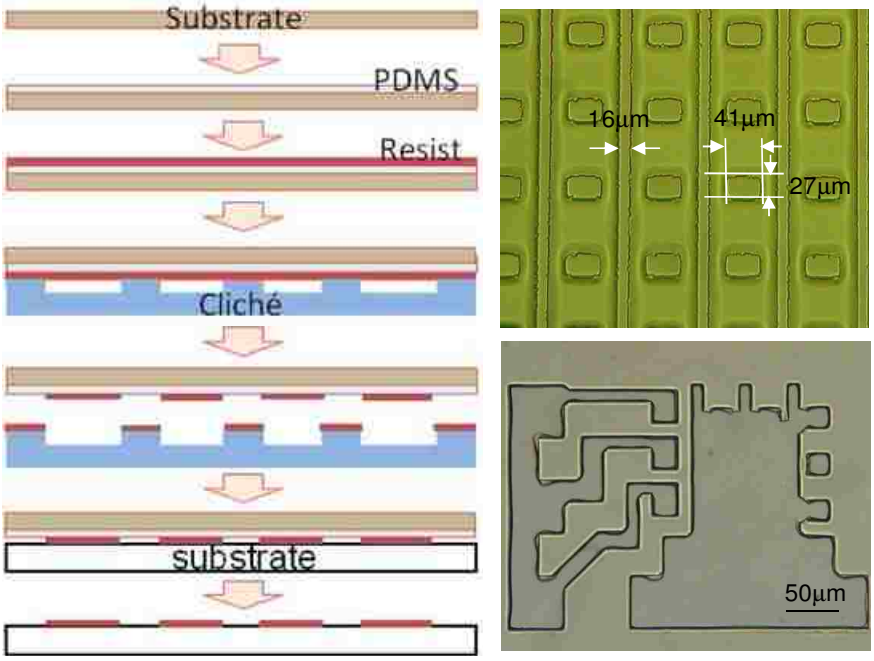


Fig. 5.28 Novel imprint lithography process and printed polymer patterns.

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Chapter 6

Conclusions

6.1 Conclusion of this work

Paper substrate is introduced as a promising substrate for flexible and disposable electronics. Amorphous indium gallium zinc oxide thin film transistors (a-IGZO TFTs) with methyl-siloxane based gate dielectric were successfully fabricated on glossy paper substrate at low processing temperature (≤150^{o}C). Glossy paper planarized by acrylate polymer was introduced as a new low cost flexible substrate and its rms surface roughness of 1nm was comparable to that of a commercial glass substrate. Both positive and negative fine patterns were formed by photolithography on the planarized paper and width and spacing of each pattern are well defined from 13μm to 1μm, comparable to the typical TFT channel length of 4~6μm for LCD. a-IGZO TFTs with SiO_2 (≤150^{o}C) gate dielectric demonstrated the field effect mobility of ~6cm^{2}V^{-1}s^{-1}, on/off current ratio of ~10^4, threshold voltage of 2.2V, and subthreshold slope of ~1V/decade. The leakage current (Ig) of the low temperature SiO_2 is too high. Compared to low temperature SiO_2,

a-IGZO TFTs using a methyl-siloxane based dielectric on the paper substrate demonstrated improved performances with field effect mobility of ~20$cm^2V^{-1}s^{-1}$, on/off current ratio of ~10^6, and low leakage current, which show the enormous potential for flexible electronics application. Through the analysis of methyl-siloxane gate dielectric, the low dipolar polymer material was suggested as the new gate dielectric for paper electronics.

P-type cuprous oxide (Cu_2O) semiconductor was introduced to enable CMOS circuit with the n-channel a-IGZO TFTs. RF sputtering with Cu_2O target has been investigated for the deposition of Cu_2O films. The deposition power, the argon partial pressure, and the deposition temperature have been controlled to achieve optimal growth conditions. The properties of Cu_2O thin films were analyzed by optical bandgap, resistivity, Hall mobility, XPS, and TEM. Post-annealing and plasma treatments have been also investigated to improve the device characteristics. Through these analysis and experiments, it is revealed that the sputtered Cu_2O films are p-type, however only a very small modulation of Cu_2O TFT is observed. Material analysis performed on Cu_2O sputter target material indicated presence of undesirable CuO phase that rendered all films highly conductive, not useful for TFTs. However an application for P-N diodes was explored by using this p-type Cu_2O and n-type a-IGZO, P-N junction diode was realized on paper substrate at room temperature process. This result provides the potential of simple switching device on a disposable paper substrate.

In order to realize a high resolution and high throughput printing method for thin film transistor application, a modified offset roll printing was studied. This roll printing

chiefly consists of a blanket with low surface energy and a printing plate (cliché) with high surface energy. In this study, a finite element analysis was done to predict the blanket deformation and to find the optimal angle of cliché's sidewall. Various etching methods were investigated to obtain a high resolution cliché and the surface energy of the blanket and cliché was analyzed for ink transfer. A high resolution cliché with the sidewall angle of 90° and the intaglio depth of 13μm was fabricated by the deep reactive ion etching method. Based on surface energy analysis, we extracted the most favorable condition to transfer ink from a blanket to a cliché, and thus thin films were deposited on a silicon-cliché to increase the surface energy. Through controlling roll speed and pressure, two inks, etch-resist and silver paste, were printed on a rigid substrate, and the fine patterns of 10μm width and 6μm line spacing were achieved. By using this printing process, the top gate amorphous indium-gallium-zinc-oxide TFTs with channel width/ length of 12/6μm were successfully fabricated by printing etch-resists. In addition, a novel imprint lithography was also proposed for the application of a variety of materials and demonstrated excellent patterning characteristic.

6.2 Recommendation for future research

Low polarity polymer dielectric for paper electronics.

In this research, the a-IGZO TFT on paper substrate was fabricated by using methyl siloxane based dielectric. This material is recommended to cure at high temperature of 350°C to eliminate dipolar molecules which degrades the characteristics of gate dielectric of a-IGZO TFT. It is believed that the low polarity material will

enhance the device characteristic of a-IGZO TFT on the paper. A few materials with low polarity have been applied to organic TFT and demonstrated high mobility and excellent hysteresis. Propylene, ethylene, isobutylene, and fluoropolymer are recommendable as the low polarity materials for this application.

Fig. 6.1 Transfer curves of top gate P3HT TFT (a) PMMA and (b) CYTOP (low polarity dielectric) as the dielectric [Ref.: J. Veres, Chem. Mater. 16, 4543, 2004].

Printed electronics

The fine patterns of metal nanoparticle ink (electrode), organic dielectric, and etch-resist can be printed by a modified offset roll printing. However, this contact type printing may not be suitable for the printing of semiconductor layer that requires pure material property. Inkjet printing is a non-contact printing method, which minimizes ink's contamination and reduces the waste of expensive functional inks since it only

drops ink on the demanded area. The drawback of inkjet printing is the low pattern resolution and wave-like edge of printed patterns. Therefore, inkjet is recommended for the printing of active semiconductor. Through the combination of the modified offset roll and inkjet printing as shown in figure 6.2, the high resolution circuits on a flexible substrate can be realized.

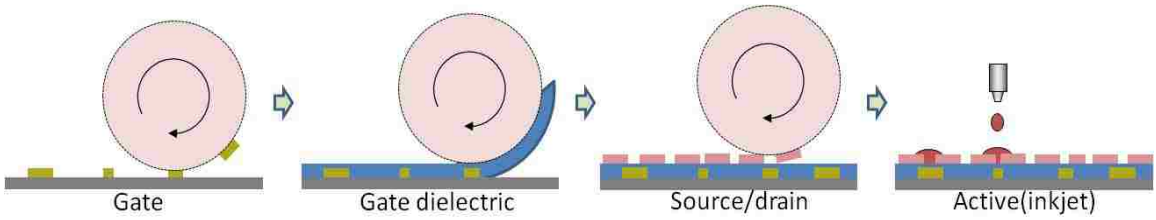


Fig. 6.2 Combination of an offset roll printing and inkjet printing for TFT fabrication.

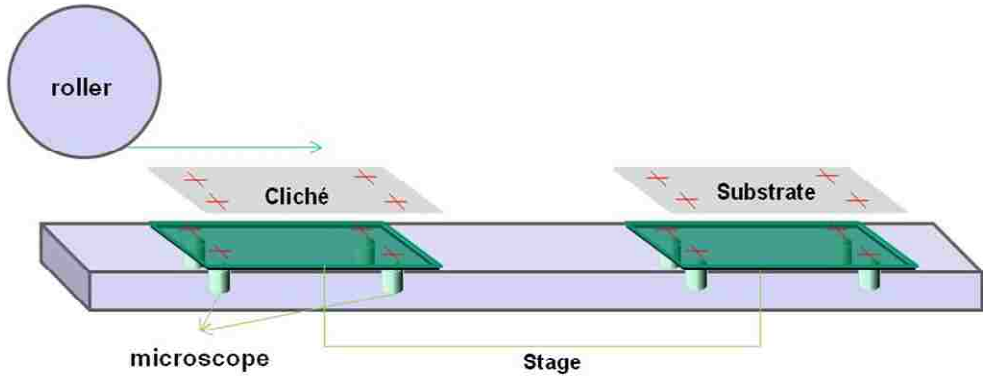
Circuits on paper substrate

A stand-alone TFT and a P-N diode on paper substrate were demonstrated in this study. In order to realize possible applications, integrated circuits on paper substrate are essential. Conventional TFT process is not suitable for the paper substrate due to its flexibility and moisture absorption. Therefore, organic TFT and printing technology need to be considered as potential device and process. The majority of organic TFT is p-type and thus n-type organic semiconductor or printable inorganic semiconductor needs to be developed for the realization of printable electronics.

Appendix A

Registration for the modified offset roll printing

Registraion is very important since thin film transistor consists of several layers, such as gate, source-drain, and active layer. We couldn't install very sophisticated alignment system in our home-built printing tool, but we propose the method to align each layer by using optical microscope system as the following schematic. Optical microscopes are located under the each stage with align keys. Each cliché and substrate also has align keys. Through the microscope, the substrate is mechanically aligned with the keys on the stage.



Appendix B

Process/Parameter for TFT fabrication

1. Process flow for a-IGZO TFT on paper substrate

1) **Planarization**

1-1) Spin-coating of AC818 with 600rpm/30sec (Model of spin coater: P-6000)

1-2) Soft bake at 80ºC for 10min in an oven (oven model: Blue G01305A) or at 90ºC for 10min on a hot plate

1-3) Hard bake at 150 ºC for 1hr in an oven

2) **Outgassing barrier**

: Deposition of 100nm thick SiO_2 in sputter with RF power of 100W and Ar flow of 20sccm (sputter model: Kurt J. Lesker)

3) **Gate**

3-1) Spin-coating of LOR 10B (Lift Off Resist from Microchem) with 2000rpm/30sec

3-2) Soft bake at 80ºC for 2min in an oven

3-3) Hard bake at 150ºC for 10min in an oven

3-4) Spin-coating of photoresist (AZ MiR 703) with 3000rpm/30sec

3-5) Soft bake at 100ºC for 2min in an oven

3-6) Exposure with a gate mask. Exposure energy:130mJ (Lithography System, Micralign)

3-7) Develop for 45sec in mixed developer (AZ MIF300) with DI water (developer:DI water=2:1)

3-8) Deposition of gate metal (600nm AlNd / 30nm Mo) in sputter with DC power of 100W and Ar flow of 20sccm

3-9) Liftoff process in EBR (Edge Bead Removal from Microchem) solution

3-10) Dry at 80ºC for 5min in oven

4) Gate dielectric

4-1) Spin-coating of organic dielectric (SOG) with 7000rpm/30sec

4-2) Soft bake at 80ºC for 10min

4-3) Hard bake in N_2 ambient at 140ºC for 2.5hr

5) Active

: Deposition of 60nm thick a-IGZO in sputter with RF power of 100W ($Ar:O_2$=9:1)

6) Source-drain (S/D)

6-1) Same liftoff process with 3) Gate, by using S/D mask.

6-2) Deposition of S/D metal (500nm AlNd/30nm Mo) in sputter with DC power of 100W and Ar flow of 20sccm, and then liftoff in EBR

7) Annealing

: Annealing in N_2 ambient at 100℃ for 1hr

2. PECVD system

Process	Gas (sccm)	Power (W)	Temp (℃)	Pressure (Torr)	Dep rate (Å/Min)
Gate SiO_2	SiH_4 (120), N_2O (720), HE (2000)	400	300	1	50

3. PVD system (Sputter)

Process	Gas (sccm)	Power (W)	Temp (℃)	Pressure (mTorr)	Dep rate (Å/Min)	Time (min)
Al deposition	AR(10)	320 (DC)	RT	8~9	140	N/A
Mo deposition	AR(15)	250 (DC)	RT	8~9	400	N/A
IGZO deposition	AR(12) O2(4)	100 (RF)	RT	5	50	N/A
Cu2O deposition	AR(10)	200 (RF)	RT	6	170	N/A

3. Dry etching system - TECHNICS PEII-A plasma system

Process	Gas (sccm)	Power (W)	Pressure (Torr)	Etch rate (Å/Min)
Si etching	CF4 (15), O2 (5)	100	0.2	500

O2 plasma for surface treatment	O2 (20)	100	0.15	N/A

4. Photolithography process

4.1 Positive PR for etching

1. Dehydration bake on hot plate at 150°C for 5 min, cool down to room temperature for 5 min

2. HMDS spin coating at 3000rpm for 30sec. Bake on hot plate at 150ºC for 1 min then cool down for 5 min to room temperature.

3. Photoresist (AZ MiR 703) spin-coating at 3000rpm for 30sec. Softbake on hot plate at 90ºC for 1 min

4. Expose (pattern) the PR coated wafer by aligner (I line source). Develop the PR by using developer (AZ MIF300) for 1 min. Rinse and dry the wafer for inspection.

5. Hard bake the pattern PR at 110ºC for 1 min before etching.

4.2 Positive PR with LOR for lift-off

1. Dehydration bake on hot plate at 150°C for 5 min, cool down to room temperature for 5 min.

2. LOR 10B (Microchem) spin coating at 2000rpm for 30sec. Bake on hot plate at 170ºC for 5 min then cool down for 5 min to room temperature.

3. Photoresist (AZ MiR 703) spin-coating at 3000rpm for 30sec. Softbake on hot plate at 90ºC for 1 min.

4. Expose (pattern) the coated wafer by aligner (I line source). Develop the PR by using developer (AZ MIF300) up to 1 min,based on the pattern of double border. Rinse the wafer by DI wafer.

4.3 PR stripping process

Use 2 step stripping approach. Put the wafer in 1st bath of stripper (AZ 400T) for 5 min. Rinse the wafer with DI and dry up the wafer by N_2 purge. Put the wafer in 2rd bath of stripper (clean) for another 5 min. Rinse the wafer with DI and dry up the wafer by N_2 purge.

4.4 Lift-off process

1. Put wafer in EBR (Microchem) solution in glass tank and put the tank in ultrasonic bath.

2. Turn on the ultrasonic with 100% output power for 5~10 min until 90% area is done.

3. Rinse the wafer by DI quickly and put the wafer into 2nd bath of EBR in ultrasonic for another 5~10 min or until all patterns are well defined.

4. Rinse and dry the wafer.

Vita

Nackbong Choi was born in South Korea. He obtained a BS in material science from Dong-A University in 1999 and a MS in material science from Pusan National University in 2001. His master thesis was titled *"Fabrication and Thermal Stress Analysis of Electronic Packaging Materials"*. After graduation, he joined LG Display R&D Center in 2001, where he led several projects, such as amorphous silicon TFT technology, flexible AMOLED, flexible color EPD (Electrophoretic Display), and organic TFTs. He was a senior research engineer in LG Display R&D Center before joining the doctoral program of Lehigh University in September of 2008. He is the author of 8 scientific papers in peer-reviewed journals and has 20 patents registered in US, all related to flat panel displays. He is currently a member of IEEE (Institute of Electrical and Electronics Engineers), FlexTech (Alliance for Display & Flexible, Printed Electronics), TMS (The Minerals, Metals & Materials Society), AMFPD (Active-Matrix Flat Panel Displays and Devices) and SID (Society for Information Display), and a peer reviewer of the Electrochemical and Solid-State Letters.

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