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This thesis is accepted and approved in partial fulfillment of the requirements for a Master of Sciences.

Date: April 20th 2018

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Wafer-scale Fabrication and Characterization of Recessed-channel $PtSe_2$ MOSFETs with Low Contact Resistance and Improved Gate Control

By

Lei Li

A Thesis

Presented to the Graduate and Research Committee

of Lehigh University

in Candidacy for the Degree of

Master of Sciences

in

Electrical Engineering

Lehigh University

May 2nd 2018

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Abstract

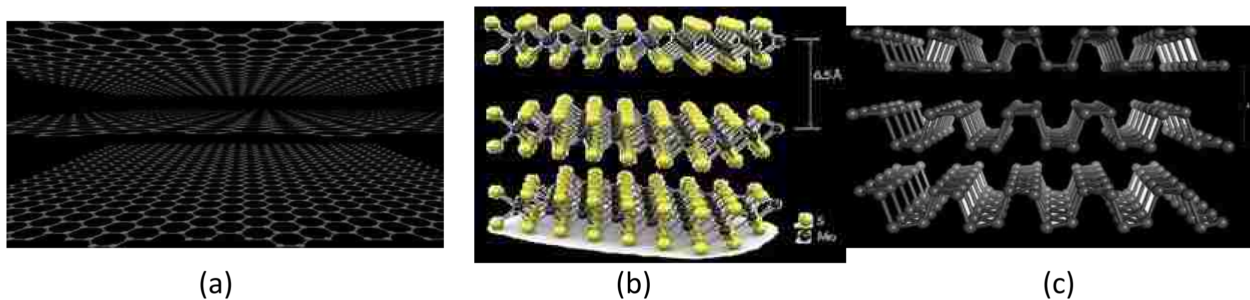
For the first time, wafer-scale fabrication of $PtSe_2$ MOSFETs was demonstrated by photolithography. The on $PtSe_2$ is grown by thermally assisted conversion (TAC) of Pt films under Se vapor at 400 °C. Taking advantage of the unique property of $PtSe_2$ to transition from semiconductor to semimetal as its thickness increases beyond a few monolayers, channel recess was adapted for improving gate control while keeping the contact resistance as low as 0.008 Ω·cm. The wafer-scale fabrication resulted in uniform device characteristics so that average vs. best results were reported, as well as RF vs. DC characteristics. For example, the drain current at V_{GS} = −10, V_{DS} = −1 V were 25 ± 5, 57 ± 8, and 618 ± 17 μA/μm for 4-, 8-, and 12-nm-thick $PtSe_2$, respectively. The corresponding peak transconductances were 0.20 ± 0.1, 0.60 ± 0.05, and 1.4 ± 0.1 μS/μm. The forward-current cut-off frequency of 12-nm-thick $PtSe_2$ MOSFETs was 42 ± 5 MHz, whereas the corresponding frequency of maximum oscillation was 180 ± 30 MHz. These results confirmed the application potential of $PtSe_2$ for future generation thin-film transistors.

Chapter 1: Introduction

This chapter first presents a brief introduction of two dimensional (2D) materials. Following that, the major challenges are introduced and possible solutions are proposed. Lastly, the physical and electrical properties of $PtSe_2$ and introduced.

1.1 Introduction of Two Dimensional Materials

The Discovery of graphene [1] started a new research area: single atomic layer materials, which is also termed as two dimensional (2D) materials. The electrons and holes are restricted to the in-plane 2D transport which is fundamentally different from traditional 3D semiconductors such as silicon and gallium arsenide. The most investigated 2D materials are graphene [2], MoS_2 [3], and black phosphorus [4], as shown in Fig. 1-1 (a) [5], (b) [6], and (c) [7], respectively. As the CMOS techniques continue to shrink, bulk materials will be limited by the quantum effects as their thickness reduces. 2D materials are ideal candidates for future electronics for their naturally thin body, remarkable electronic and optoelectronic properties.



(a) (b) (c)

Fig. 1-1. Crystical structure of (a) graphene, (b) MoS_2, and (c) black phorphorus.

1.2 Challenges of Two Dimensional Materials

Though rapid progress has been made on 2D material growth, devices, and applications, challenges remain ahead. Firstly, for both digital and high-frequency applications, larger current capacity I_{ON} and *on/off* ratio, which are related to the gain and power dissipation, are desired. However, we have to compromise between the carrier mobility (or current capacity) and gate modulation when choosing proper 2D materials as the channel materials for FETs. Specifically, 2D transistors with high carrier mobility and large current capacity such as graphene FETs usually suffer from the poor gate modulation, or *on/off* ratio. On the other hand, 2D transistors with high *on/off* ratio such as MoS_2 FETs usually have low mobility and large contact resistance. Black phosphorus FETs show high carrier mobility and acceptable *on/off* ratio, but they are not stable in air.

Secondly, being absent of effective doping such as ion implantation, most 2D devices show large contact resistance due to the Schottky barrier, interface states, and van der Waals gap. The idea of channel recess has been proved to help reduce the contact resistance and improve the *on/off* ratio for silicon-on-insulator (SOI) [8] and GaAs MESFETs [9]. Adapting the similar idea, the dilemma of 2D materials FETs with either low *on/off* ratio or small I_{ON} can be solved by channel recess of $PtSe_2$ FETs, so that we can engineer its bandgap and carrier density through by controlling the thickness. Though most 2D materials including MoS_2 and black phosphorus are known to have thickness dependent bandgaps, $PtSe_2$ is the only known 2D material whose bandgap changes from zero to 1.2~2 eV. An intuitive thinking is that if we can make the $PtSe_2$ FETs channel thin enough (< 1 nm) to have the desired bandgap 1.2 eV to make sure we can turn

the FET off, while keeping the $PtSe_2$ under the source and drain contacts thick enough (> 5 nm) to be metallic with pretty high carrier density, we are supposed to have FETs with high gate controllability with low contact resistance. By taking advantage of the material's own property, we can achieve high doping at the contact regions without using exterior donor or acceptor ions. As a result, the process cost is much lower compared with that of ion implant.

1.3 Platinum Diselenide ($PtSe_2$)

Dating back to 1980s, several pioneering theoretical and experimental works [10], [11], [12], [13], on layered platinum dichalcogenides PtS_2, $PtSe_2$, and $PtTe_2$ confirmed that, bulk PtS_2 is a semiconductor with a bandgap and bulk $PtTe_2$ is a metal while bulk $PtSe_2$ is in between and is a semimetal with a slight overlap of conduction and valence band and high intrinsic carrier density up to $3.3\times10^{20}cm^{-3}$. In recent works, it has been proved theoretically [14] and experimentally [15] [16] that the metallic bulk PtSe2 transforms to a semiconductor when the thickness reduces to a few atomic layers. Specifically, different from the metallic bulk $PtSe_2$, the monolayer $PtSe_2$ has a bandgap of 1.2 eV, which is close to silicon. And $PtSe_2$ thickness increases, its bandgap drops and gradually transits from a semiconductor to a semimetal [16]. In addition, semiconducting single crystalline $PtSe_2$ was predicted to have a room-temperature carrier mobility higher than 1,000 cm^2/Vs [17]. It was experimentally measured to be up to 210 $cm^2/V\cdot s$ [14], which is comparable with other better developed 2D materials like MoS_2. Furthermore, different from other TMDs and black phosphorus, the pristine $PtSe_2$ material and FETs are found to be stable for more than one year without noticeable electrical change [14]. Notably, wafer-scale polycrystalline $PtSe_2$ has been synthesized using thermally assisted conversion (TAC) at 400°C [18], which is well suited for integration with mainstream Si-based complementary metal-oxide-semiconductor (CMOS)

process because the conversion occurs below 450°C, the temperature limit of the back- end-of-line (BEOL) process.

The unique properties of $PtSe_2$ including sizeable bandgap, semimetal-to-semiconductor transition, high mobility, long-term stability, and large scale CMOS compatible process make $PtSe_2$ stand out among other 2D materials, and suggest it is promising for high performance field effect transistors (FETs) and applications. Recent studies have also shown that this material exhibits appreciable transport properties and interesting spin physics [19], motivating further studies of its transport properties.

TABLE I
COMPARISON OF $PtSe_2$ MOSFETS

Thickness (nm)	R_{SH} (Ω/□)	On/off Ratio	R_C (Ω·cm)	Material Preparation	Device Fabrication	Reference
2	$<1\times10^8$ [a]	10^6		Exfoliated	E-Beam Lithography	[14]
8	$<1\times10^5$ [a]	10^3				
11	$<2\times10^4$ [a]	10^2				
64	<25 [a]	1				
2	1×10^5	10^5	$<10^4$	Exfoliated	E-Beam Lithography	[15]
7	1.6×10^3	1.2	0.02			
14	400	1	7×10^{-3}			
2	2×10^6	1.7	40	Thermal Conversion	E-Beam Lithography	[18]
8	1×10^4	1	0.1			
20	500	1	4×10^{-3}			
4	2.1×10^4	1.9	0.3	Thermal Conversion	Photo-Lithography	This Work
8 [b]	1.1×10^4		0.04			
8	3.4×10^3	1.5	0.04			
12	1.7×10^3	1.1	8×10^{-3}			

Room-temperature data except data from [15] were measured at 10 K

[a]Upper bound from total series resistance $R_T = R_{SH}L_{CH} + 2R_C$

[b]With channel recess

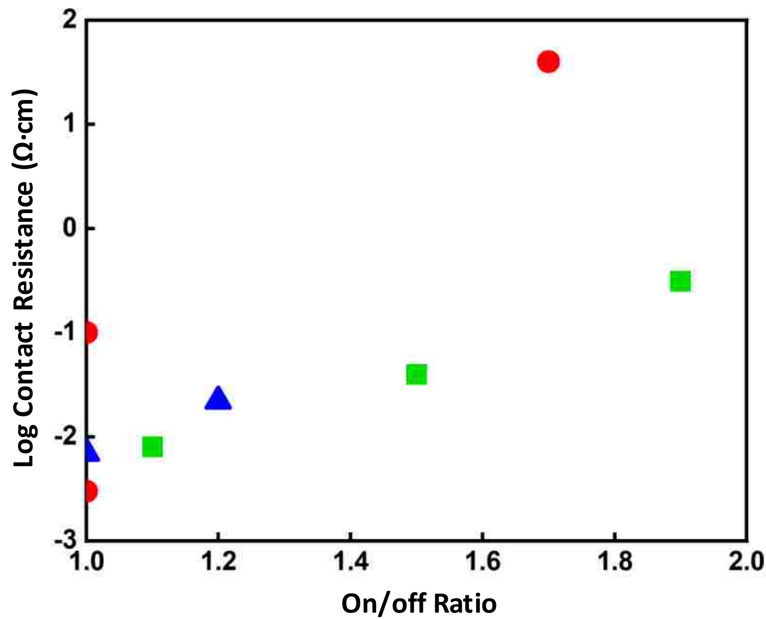


Fig. 1-2. Contact resistance vs. *on/off* ratio of $PtSe_2$ MOSFETs from [15] (▲), [18] (●), and this work (■).

Table I compares the $PtSe_2$ MOSFETs fabricated to date, including those by photolithography from this work. It can be seen that, by taking advantage of the thickness-dependent transition of $PtSe_2$ from semiconductor to semimetal, *on/off* current ratio as high as 10^6 could be obtained on thin (~ 1 nm) $PtSe_2$, whereas contact resistance below 0.01 Ω·cm could be obtained on thick (~ 10 nm) $PtSe_2$. However, since for practical applications a MOSFET must have high *on/off* ratio and low contact resistance simultaneously, this presents a dilemma as shown in Fig. 1-2. To solve the dilemma, this work incorporates a recessed channel in $PtSe_2$ MOSFETs, so that the channel can be thick under the source and drain for low contact resistance, but thin under the gate for effective control. Note that traditionally, to reduce the contact resistance, ion implantation is used in Si MOSFETs to increase not only the doping, but also the thickness of the channel under the source and drain contacts. On the other hand, to increase the gate control, etching is used in GaAs MESFETs and HEMTs to decrease the channel thickness under the gate [9]. Similar channel etching process has also been adapted for silicon-on-insulator

MOSFETs [8]. Lacking effective ion implantation or chemical doping technique for 2D materials, the channel of $PtSe_2$ MOSFETs is etched in this work.

1.4 Thesis Organization

This thesis is focus on the electrical characterization of $PtSe_2$ MOSFETs. First, the wafer-scale fabrication of $PtSe_2$ MOSFETs is introduced. Second, a TCAD mode is used to simulate the electrical behavior of a $PtSe_2$ MOSFET, and it proves the feasibility of channel recessed MOSFETs. Following that, the channel recessed $PtSe_2$ MOSFETs are characterized, including their contact resistance, sheet resistance, transfer and output characteristics, electron mobility, and forward cut off frequency. The thesis ends with the conclusion and future perspective to move on.

Chapter 2: Electrical Characterization of Recessed-Channel $PtSe_2$ MOSFETs

Though most 2D materials including MoS_2 and black phosphorus are known to have thickness dependent bandgaps, $PtSe_2$ is the only known 2D material whose bandgap changes from semiconducting to metallic. An intuitive thinking is that if we can make the $PtSe_2$ FETs channel thin enough (< 1 nm) to have the desired bandgap 1.2 eV to make sure we can turn the FET off, while keeping the $PtSe_2$ under the source and drain contacts thick enough (> 5 nm) to be metallic with pretty high carrier density, we are supposed to have FETs with high gate controllability with ultra-low ohimc contact resistance. By taking advantage of the material's own property, such FETs can achieve high doping at the contact regions without using exterior donor or acceptor ions. This work demonstrates, for the first time, wafer-scale fabrication of $PtSe_2$ MOSFETs. Channel recess is adapted for improved gate control while keeping contact resistance low. Average vs. best results are reported, so are RF vs. DC characteristics. The details are described in the following.

2.1 Wafer Scale Fabrication of $PtSe_2$ MOSFETs

Wafer-scale fabrication of $PtSe_2$ MOSFETs in this work includes three major steps: (A) formation of buried gate, (B) deposition of $PtSe_2$, (C) definition of active and contact regions, which are similar to our published work on MoS_2 MOSFETs [20]. To facilitate $PtSe_2$ deposition experiment, although step A was performed on a 200-mm high-resistivity (10 kΩ·cm) Si wafer, it was subsequently diced into approximately sixty 25 mm × 15 mm chips before steps B and C.

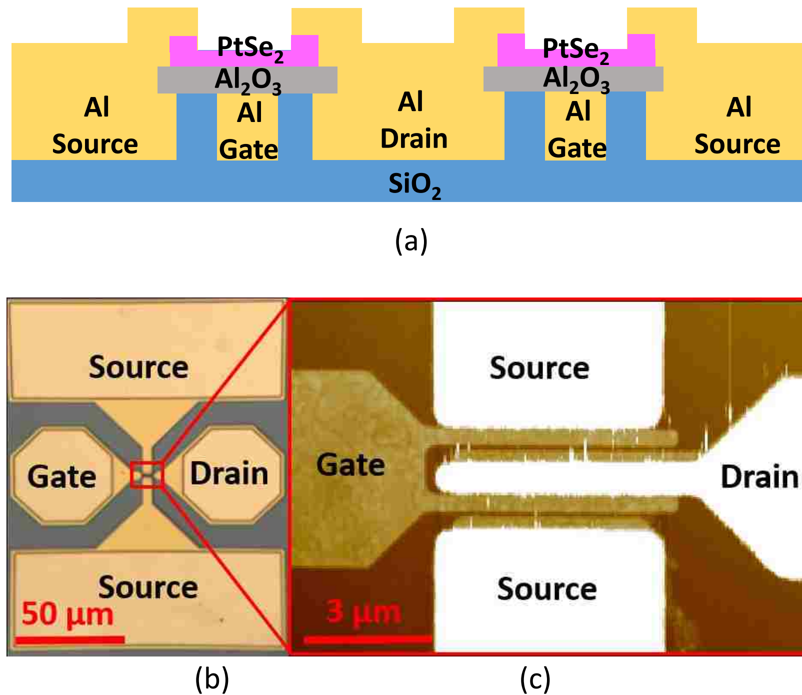


Fig. 2-1. (a) Cross section schematics, (b) top-view micrograh, and (c) atomic-force micrograph of a probable dual-gate RF $PtSe_2$ MOSFET.

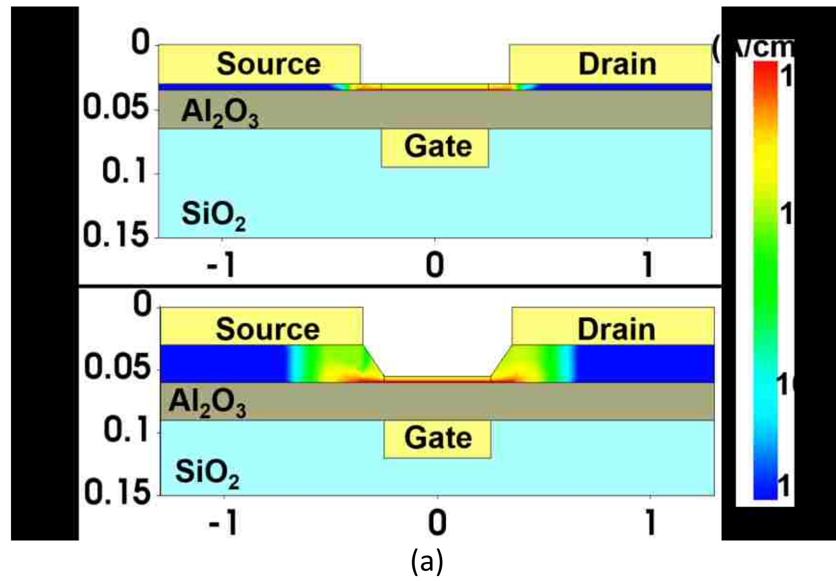
In step A, a one-mask stepper photolithography process was used to form Al gates buried in SiO_2, before deposition of gate oxide and $PtSe_2$. This way, gate oxide could be deposited at a relatively high temperature without damaging $PtSe_2$. To this end, state-of-the-art CMOS processes are capable of not only submicron gate and high-quality gate oxide, but also flat surface through chemo-mechanical polishing. Specifically, the BEOL process of the IHP SG13S foundry technology was chosen. Through step A, each 25 mm × 15 mm chip contained approximately 1500 individually probable RF MOSFETs (Fig. 2). Each MOSFET has two buried gates with a total gate width of approximately 10 µm. The gate length and thickness are approximately 0.4 µm and 0.5 µm, respectively. Following chemo-mechanical polishing, 40-nm Al_2O_3 gate oxide was deposited by atomic layer deposition at 300 °C.

In step B, nanocrystalline $PtSe_2$ thin films were grown using thermally assisted conversion as detailed in [18]. Briefly, Pt films 1-, 2-, and 3-nm thick, respectively, were sputtered onto the chips fabricated through step A. The Pt-coated chips were then selenized at 400 °C to form 4-, 8-, and 12-nm-thick $PtSe_2$, respectively.

In step C, active and contact regions were defined by a two-mask photolithography process. The active region was defined by dry etching $PtSe_2$ with CF_4/O_2 and wet etching Al_2O_3 with buffered HF. Source and drain contacts were formed by electron-gun evaporated Ni and Al with thicknesses of 10 nm and 290 nm, respectively. After contacts were formed, they were used as a self-aligned mask for channel recess as illustrated in Fig. 2-1(a). Channel recess was performed by CF_4/O_2 dry etching for 10 s. Along with the MOSFETs, transmission-line-method (TLM) test structures were fabricated to extract contact and sheet resistances. The TLM structures were 7-µm wide with channel lengths of 1.7, 3.7, 6.7, 9.7, and 13.7 µm, respectively. The contact length was 4 µm, which was much greater than the transfer length, estimated to be on the order of 0.1 µm, as will be shown later.

2.2 TCAD Simulation of Channel Recessed $PtSe_2$ MOSFETs

A TCAD model is used to validate the idea of channel recessing. Before moving to that, the geometry (thicker contact region) effects on the drain current is studied, while keeping the bandgap to be a constant. In Fig. 2-2 (a), the top and bottom devices are exactly same except the material thickness under the contact regions. The top geometry is commonly used in most 2D



(a)

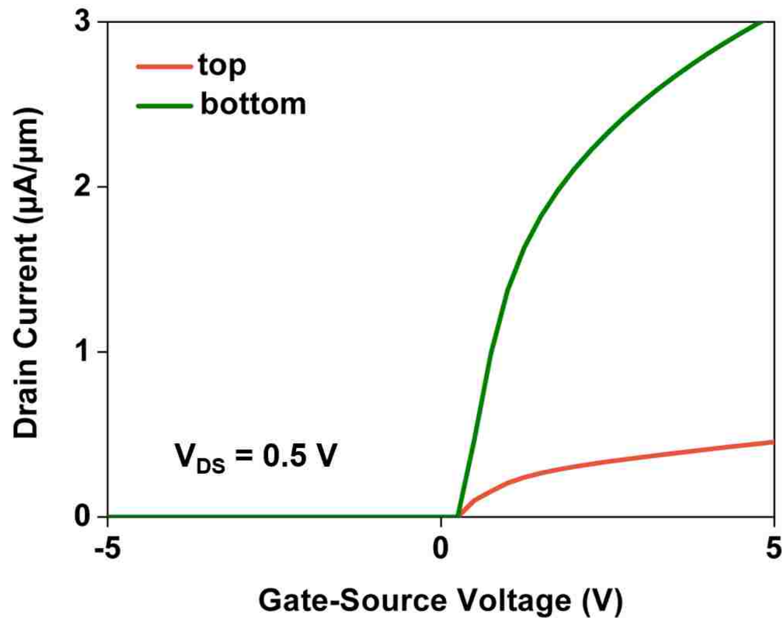


Fig. 2-2. (a) Flat (top) and channel recessed (bottom) devices and total current density color map in the channel. The gate-source voltage V_{GS} = - 5V and the drain-source voltage V_{DS} = 0.5 V (b) Drain current of a top (orange) and bottom (green).

FETs. For the top device, in both the channel and contact regions the material thickness is 5 nm. While for the bottom device, the channel is 5 nm and the material under the contacts is 30 nm thick. Other simulation parameters are set to be the same as the monolayer $PtSe_2$ with 1.2eV bandgap and 4.3 eV electron affinity [21]. The intrinsic carrier density is supposed to be low due

to the large bandgap, so the material is doped with 10^{15} cm^{-3} n-type dopant for simulation purpose. Since different contact metals will influence the simulation results, here we set the contacts to be ohmic to eliminate the contact influence. For simulation purpose we use 5 nm channel thickness instead of atomic layer 0.5 nm to ensure the meshing accuracy and numerical convergence. To create such a recessed structure using wet etch, we will end up with a slope instead of a vertical wall, due to the nature of isotropic etching. For that reason, we set the access regions between source/drain contacts and gate with a slope. With these statements in mind, the color map in Fig. 2-2 (a) shows the total current density of both devices with V_{GS}= 5 V and V_{DS} = 0.5 V. Compared with the flat device (top), the current extends further under the contacts in the recessed device. In other words, the recessed structure can relax the current crowding effect and has larger transfer length and smaller contact resistance. As confirmed by the simulated current vector path, in the flat (top) device of Fig. 2-2 (a), most current flows horizontally at the contact edge, while in the channel recessed device, current flows both horizontally and vertically. The vertical flow spreads the current thus it can extend further under the contacts. Fig. 2 (b) shows that drain current of both devices when V_{DS} = 0.5 V. It shows that the recessed structure has current five times larger than that of flat structure (top).

After understanding the geometry influences on FETs performance, the thickness dependent bandgap is analyzed. The cross section is indicated in Fig. 2-3. There has not been any theoretical calculation yet about the actual band structure and how it changes horizontally for such structures. However, intuitively, we can imagine that near the center of channel, it is not influenced by the van der Waals force from other layers, so that bandgap is expected to be 1.2 eV. As it moves to the edge, the van der Waals force from higher layers starts to influence the

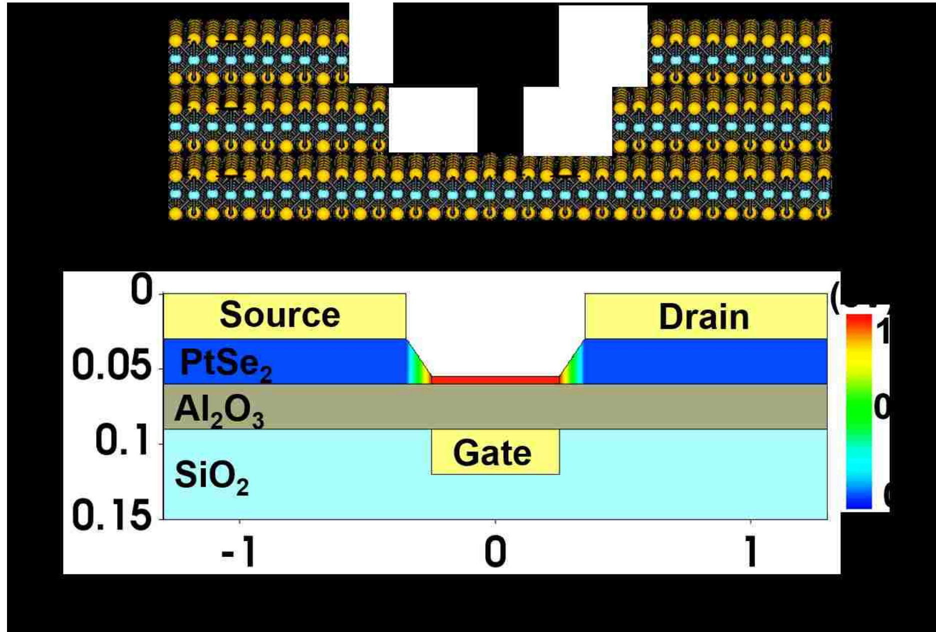


Fig. 2-3. A channel recessed $PtSe_2$ MOSFET with thickness-modulated-bandgap

electron orbits and the band structure starts to change. Though DFT based calculations predict that the bandgap drops significantly when $PtSe_2$ monolayer turns into bilayers or thicker, that's not true for this horizontal case. As we move towards the edge, the $PtSe_2$ bandgap starts to drop continuously and smoothly, since the distance is continuous, which is different from the vertical case with step-function like van der Waals gaps. The bandgap gradually drops from 1.2 eV to 0 eV and a hyperbolic-tangent-like transit of bandgap is expected. Here, for simulation purpose, we used 0.05 eV instead of 0 eV. For simplicity, the first order linear bandgap transit is used, which is a reasonable approximation to the hyperbolic-tangent without losing the generality. Based on these assumptions, the bandgap is set to be a constant of 1.2 eV above the gate and starts to drop linearly from the channel edge to 0.05 eV at the source/drain contact edges. The channel bandgap color map and device geometry are shown in Fig. 2-3. Using the exact same channel recessed geometry, three different situations are simulated in Fig. 2-4: a constant

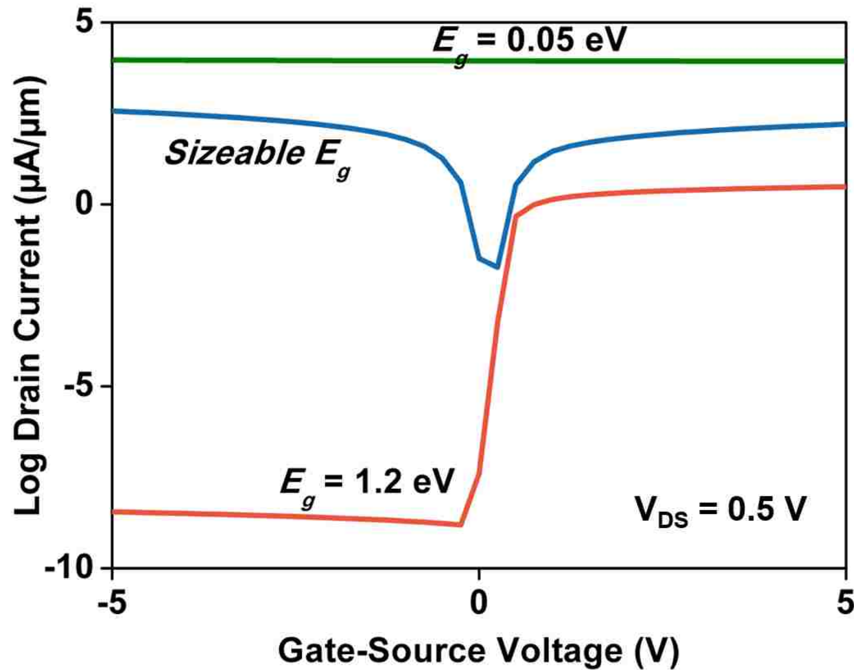


Fig. 2-4. Simulation results of drain current of channel recessed MOSFET in Fig. 2-3 with different bandgaps: thickness-independent constant bandgap 0.05 eV (green,), thickness-dependent bandgap with 1.2 eV in the channel and 0.05eV under the contacts (blue), and thickness-independent constant bandgap 1.2 eV (orange).

bandgap 0.05 eV (thick $PtSe_2$), $PtSe_2$ with thickness dependent bandgap drops from 1.2 eV to 0.05 eV, and a constant bandgap 1.2 eV (monolayer $PtSe_2$). As shown in Fig. 2-4, the constant 0.05 eV device has very large current capacity but very poor *on/off ratio* ~ 1 due to the high carrier density. As will be shown later, this simulation agrees with the measurement. In contrast, the constant 1.2 eV (monolayer $PtSe_2$) device is similar to [14], [15], which has very high *on/off* ratio ~ 10^7, but the current capacity is very small. The real $PtSe_2$ device, whose bandgap changes with the thickness, is the combination of these two case: with both high current capacity up to 300 μA/μm and *on/off* ratio up to 10^5. The simulation proves the feasibility of high performance $PtSe_2$ FETs through bandgap engineering by channel recess. Note that since the material is n-type doped with 10^{15} cm^{-3} in the simulation, the hole concentration in the ungated regions are

negligible for the constant 1.2 eV bandgap device. When V_{GS} is negative, the gate induced holes in the channel forms a barrier with the electrons in the contact regions, resulting in lower current as V_{GS} goes negative. However, for the thickness- dependent-bandgap device whose bandgap drops to zero in the ungated regions, where both hole and electron density are on the order of 10^{20} cm^{-3}, there is no such a barrier and the transport is ambipolar, as shown in Fig. 2-4.

2.3 Contact and Sheet Resistances

Fig. 2-5 plots the total resistance RT measured on TLM structures of different $PtSe_2$ thicknesses before channel recess. For each thickness, the measurement was repeated on at least ten randomly chosen TLM structures. The resulting standard deviation was very small due to the uniform nature of wafer-scale fabrication. For visibility, data from 8-nm and 12-nm $PtSe_2$ were multiplied by 5, although their standard deviations are still barely discernable. Nevertheless, it can be seen that all data exhibit a linear thickness dependence, which when extrapolated to zero thickness intercept near the origin. This implies a constant sheet resistance R_{SH} and a low contact resistance R_C. According to [22]

$$R_T = R_{SH} L_{CH} + 2R_C, \qquad (1)$$

where L_{CH} is the channel length and all quantities are normalized by the channel width of 7 µm.

Assuming $PtSe_2$ is uniformly semimetallic so that the channel resistivity ρ_{CH} is independent of the channel thickness t,

$$R_{SH} = \rho_{CH}/t. \qquad (2)$$

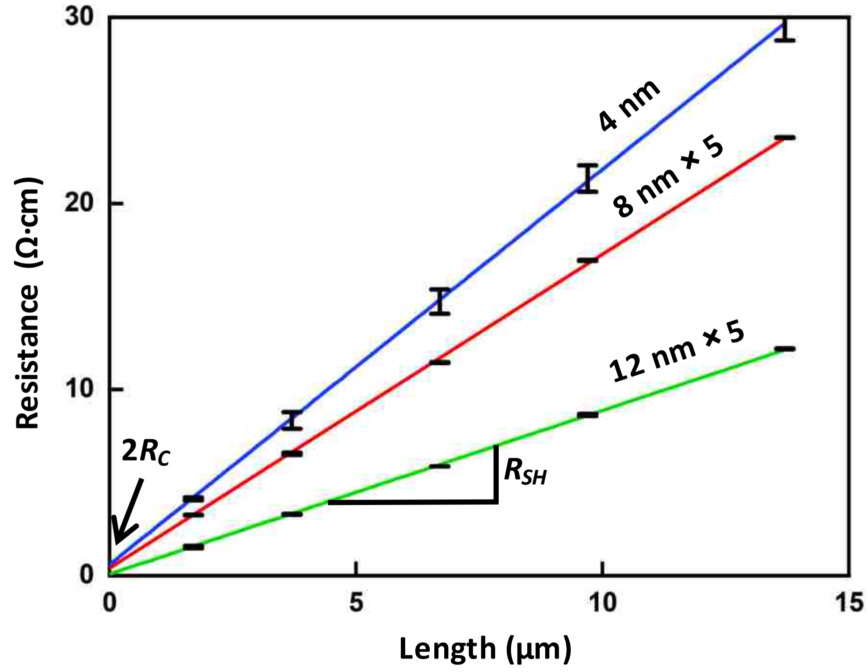


Fig. 2-5. Total resistance R_T measured on TLM structures of different channel lengths and $PtSe_2$ thicknesses.

The assumption is valid only when t >> 1 nm, because, as mentioned before, $PtSe_2$ turns semiconducting when t is reduced to one or two monolayers, with each monolayer approximately 0.6 nm thick.

Assuming further that the contact transfer length L_{TF} is much smaller than the physical contact length

$$R_C = \sqrt{\rho_C R_{SH}} \approx \sqrt{\rho_C R_{CH}/t}, \qquad (3)$$

where ρ_C is the surface contact resistivity. The transfer length can be estimated by

$$L_{TF} = \sqrt{\rho_C / R_{SH}} \approx R_C / R_{SH}. \qquad (4)$$

Based on the experimentally extracted R_C and R_{SH} for t = 4, 8, and 12 nm (Table II), $L_{TF} \approx$ 0.14, 0.12, and 0.05 μm, respectively, which are all much smaller than the contact length of 4 μm. Note that as the channel length and thickness are scaled, the contact resistance and length

need to be scaled, too. A contact resistance on the order of 0.01 Ω·cm with a transfer length on the order of 0.1 μm is compatible with nanometer MOSFETs.

Fig. 2-6 shows that the thickness dependence of the present R_{SH} and R_C are in general agreement with that of [15] and [18] despite different ways in $PtSe_2$ preparation. However, (2) and (3) imply R_{SH} and R_C are inversely dependent on t and $t^{0.5}$, respectively, but experimentally they fit $t^{-1.7}$ and $t^{-3.6}$, respectively. This invalidates the assumption that ρ_{CH} is independent of t. In fact, the best fit can be obtained if $\rho_{CH} \approx t^{-0.7}$ and $\rho_C \approx t^{-5.5}$. Such strong thick dependence of ρ_{CH} and ρ_C will be discussed further later.

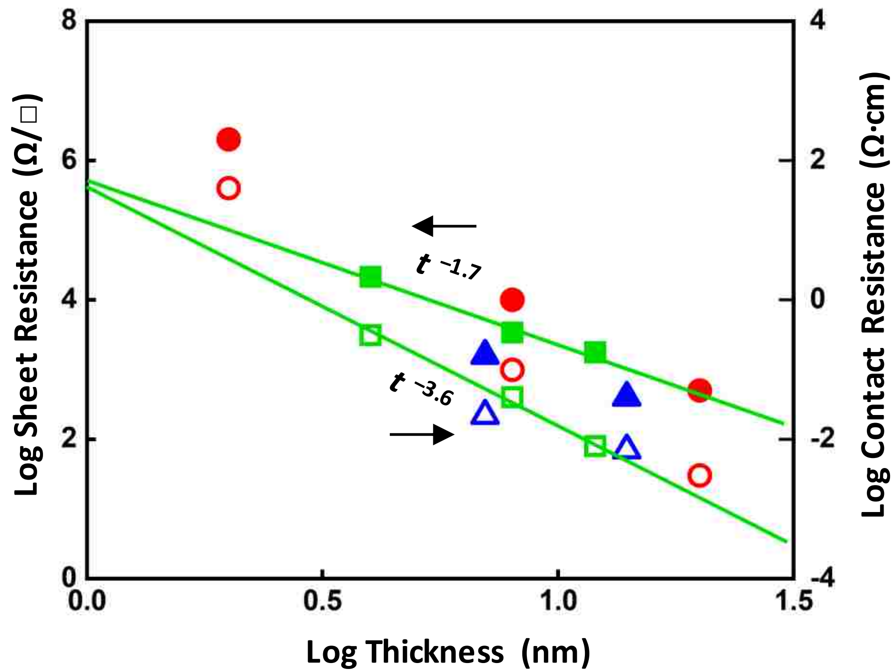


Fig. 2-6. Sheet resistance R_{SH} (solid symbol) and contact resistance R_C (empty symbol) vs. channel thickness t from [15] (▲, Δ), [18] (●, ○), and this work (■, □).

TABLE II
EXTRACTED SHEET AND CONTACT RESISTANCES

$PtSe_2$ Thickness t (nm)	Sheet Resistance R_{SH} (Ω/□)	Channel Resistivity ρ_{CH} (Ω·cm)	Carrier Density n (cm^{-3})[a]	Contact Resistance R_C (Ω·cm)	Contact Resistivity ρ_C ($\Omega\cdot cm^2$)
4	2.1×10^4	8.0×10^{-3}	7.0×10^{19}	$(3.1\pm1.4)\times10^{-1}$	4.6×10^{-6}
8	3.4×10^3	2.7×10^{-3}	2.3×10^{20}	$(4.0\pm 0.1)\times10^{-2}$	4.7×10^{-7}
12	1.7×10^3	2.0×10^{-3}	3.0×10^{20}	$(8.0\pm0.3)\times10^{-3}$	3.8×10^{-8}

[a]Assuming drift mobility $\mu_D \approx 10$ $cm^2/V\cdot s$

Table II lists the ρ_{CH}, ρ_C, and n values calculated from R_{SH} and R_C, where n is the carrier density so that

$$\rho_{CH} \approx 1/qn\mu_D, \qquad (5)$$

where q is the electron charge and μ_D is the drift mobility (assumed to be approximately 10 $cm^2/V\cdot s$ as will be shown later). The calculated ρ_{CH} values, on the order of 10^{-3} Ω·cm, are approximately an order of magnitude higher than that of bulk $PtSe_2$ [10], [14], reflecting the poorer quality of present $PtSe_2$ films.

On the other hand, the extracted n values, on the order of 10^{20} cm^{-3}, are consistent with that of bulk $PtSe_2$ [11], [14], implying the higher ρ_{CH} of the present $PtSe_2$ films is mainly due to lower μ_D instead of lower n. Note that synthesized 2D films typically exhibit lower mobility than that of exfoliated films of the same material, before the synthesis technique is gradually improved. Additionally, the extracted n values are comparable for t = 12 nm and 8 nm but decrease drastically for t = 4 nm. According to [16], $PtSe_2$ ceases being a semimetal and develops a bandgap when $t \approx 1.2$ nm. In reality, the semimetal-semiconductor transition may not be so

abrupt, so the density of states near the band edge may start to decrease before the bandgap appears [23]. This will cause the carrier concentration to decrease before $t \approx 1.2$ nm. Additionally, [15] speculates that there may even be a small bandgap when $t \approx 2$ nm, and [14] shows from optical absorption measurement that even 12-nm $PtSe_2$ has a bandgap. Lastly, present $PtSe_2$ has a surface RMS roughness of 1~2 nm. When the average thickness is reduced to 4 nm, part of the film may be as thin as 2 nm, which will also decrease the average carrier density.

The extracted ρ_C values, on the order of 10^{-8} to 10^{-6} $\Omega\cdot cm^2$, are excellent for typical semiconductors. Usually ρ_C depends on the carrier density immediately under the contact, which presumably is similar for the $PtSe_2$ thin films of different thicknesses. However, when the film thickness approaches the mean free path, ρ_C has been observed to be inversely dependent on the film thickness mainly due to increased surface scattering [24]. Since the mean free path of metals and heavily doped semiconductors are both on the order of 100 nm [25], [26], even 12-nm $PtSe_2$ will suffer from significant surface scattering. However, it will be very challenging to recess a channel from 100 nm to 1 nm so that the aspect ratio of a recessed channel needs to be carefully traded off.

2.4 Recessed Channel

As mentioned before, for channel-recess experiments, TLM structures with $t = 8$ nm wereas dry etched by CF_4/O_2 for 10 s using source/drain contacts as a self-aligned mask. Fig. 2-7 shows that after channel recess R_{SH} increased from 3.3×10^3 Ω/□ to 1.1×10^4 Ω/□, the latter corresponding to t $\approx$ 5 nm according to Fig. 2-6. However, R_C remained at 4×10^{-2} $\Omega\cdot cm$. This implied that low contact resistance could be maintained by keeping $PtSe_2$ thick under the

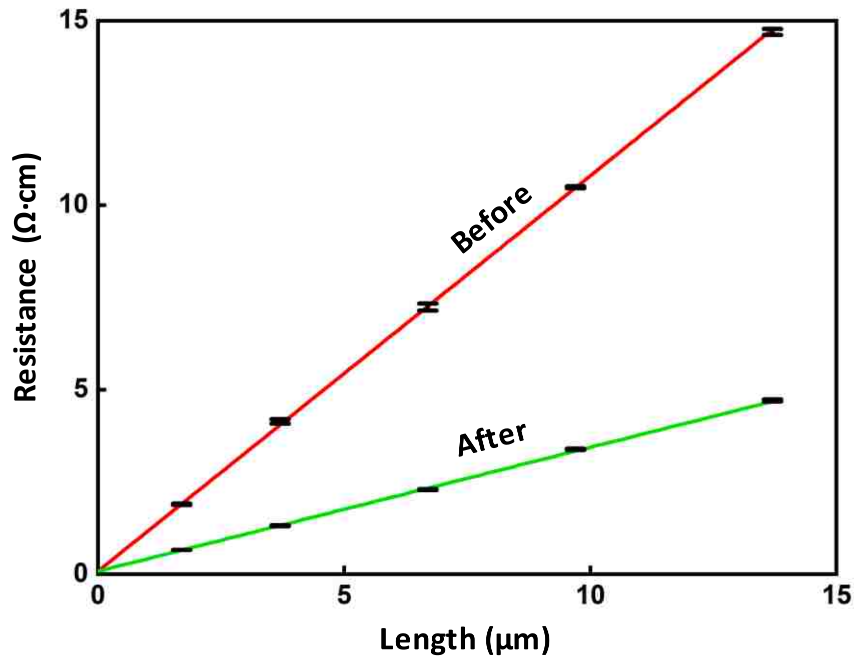


Fig. 2-7. Total series resistance R_T before and after channel recess of TLM structures with initial $PtSe_2$ thickness t = 8 nm.

contacts, but the current *on/off* ratio could be improved by thinning $PtSe_2$ between the contacts. However, with $t \approx 5$ nm the corresponding MOSFETs were inferior to that with a uniform channel of t = 4 nm. Recessing of the 8-nm-thick TLM structures beyond 10 s increased R_{SH} to infinity, implying the channel was discontinuous by then, probably due to surface roughness and etching damage. For similar reasons, 10-s channel recess of 4-nm-thick TLM structures resulted in no working devices. Note that similar channel recess has been successfully used to improve the *on/off* ratio of MoS_2 MOSFETs by three orders of magnitude while maintaining low contact resistance.

2.5 $PtSe_2$ MOSFET DC Characteristics

Fig. 2-8 and Fig. 2-9 show the transfer and output characteristics of typical $PtSe_2$ MOSFETs with t = 4, 8, and 12 nm. The MOSFETs all exhibit p-channel depletion-mode behavior. Their linear dependence on V_{DS} confirms that the contacts are indeed ohmic. Again, random sampling of at least ten MOSFETs of each thickness revealed uniform characteristics. For example, the drain current at V_{GS} = −10, V_{DS} = −1 V are 25 ± 5, 57 ± 8, and 618 ± 17 μA/μm for t = 4, 8, and 12 nm, respectively. The corresponding peak transconductances are 0.20 ± 0.1, 0.60 ± 0.05, and 1.4 ± 0.1 μS/μm. It can be seen that the drain current at V_{GS} = 0, V_{DS} = −1 V decreases much faster than the decrease in t, so that the drain current for t = 4 and 8 nm need to be multiplied by a factor of 11 and 33, respectively, to be clearly visible. However, with V_{DS} = −1 V and V_{GS} = −20 V to 20 V, the

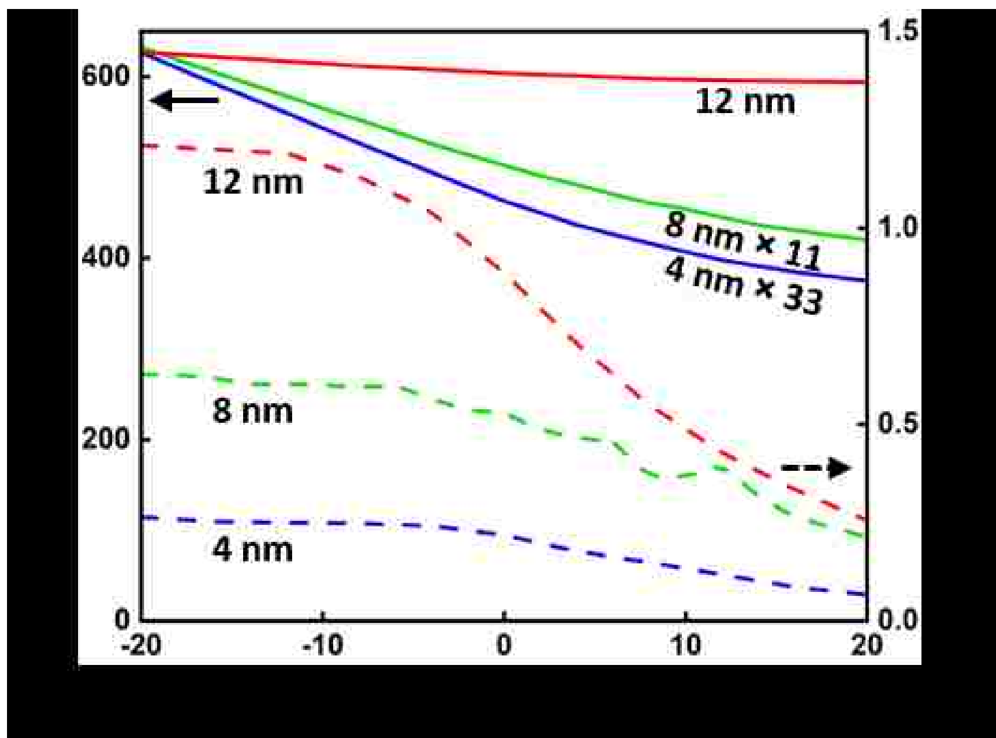


Fig. 2-8. Transfer characteristics measured on typical $PtSe_2$ MOSFETs with channel thickness t = 4, 8 and 12 nm. V_{DS} = −1 V.

on/off ratio is 1.9, 1.5 and 1.1 for t = 4, 8, 12 nm, respectively. This trend of decreasing current with increasing *on/off* ratio is consistent with [14], [15], [18] as shown in Table I and Fig. 1. From Fig. 6(a), the field-effect mobility μ_{FE} is extracted according to [22]

$$\mu_{FE} \approx L_{CH} G_M / W_{CH} C_{OX} V_{DS}, \quad (6)$$

where G_M is the peak transconductance and C_{OX} is the unit-area gate capacitance. Thus, $\mu_{FE} \approx 3$, 5, and 10 cm2/V·s, for t = 4, 8, and 12 nm, respectively. Note that μ_{FE} is sensitive to the channel-oxide interface and can differ significantly from the drift mobility μ_D. Nevertheless, lacking better data for μ_D, 10 cm2/V·s was used in (5) to estimate n as described previously.

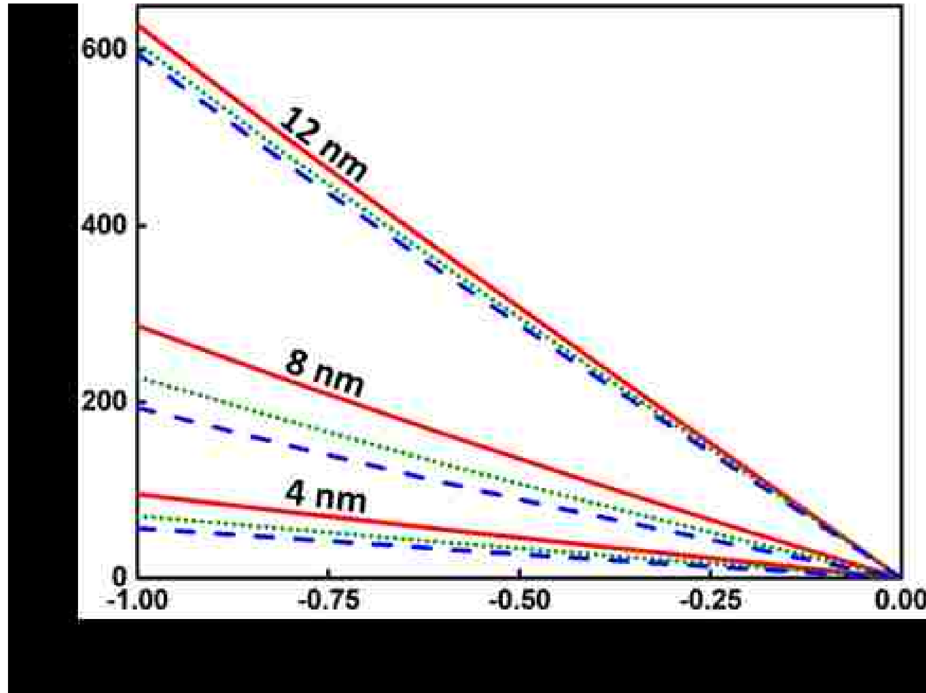


Fig. 2-9. Output characteristics measured on typical $PtSe_2$ MOSFETs with channel thickness t = 4, 8 and 12 nm. V_{GS} = −20 V (▬), 0 V (• • •), and 20 V (- - -).

2.6 $PtSe_2$ MOSFET RF Characteristics

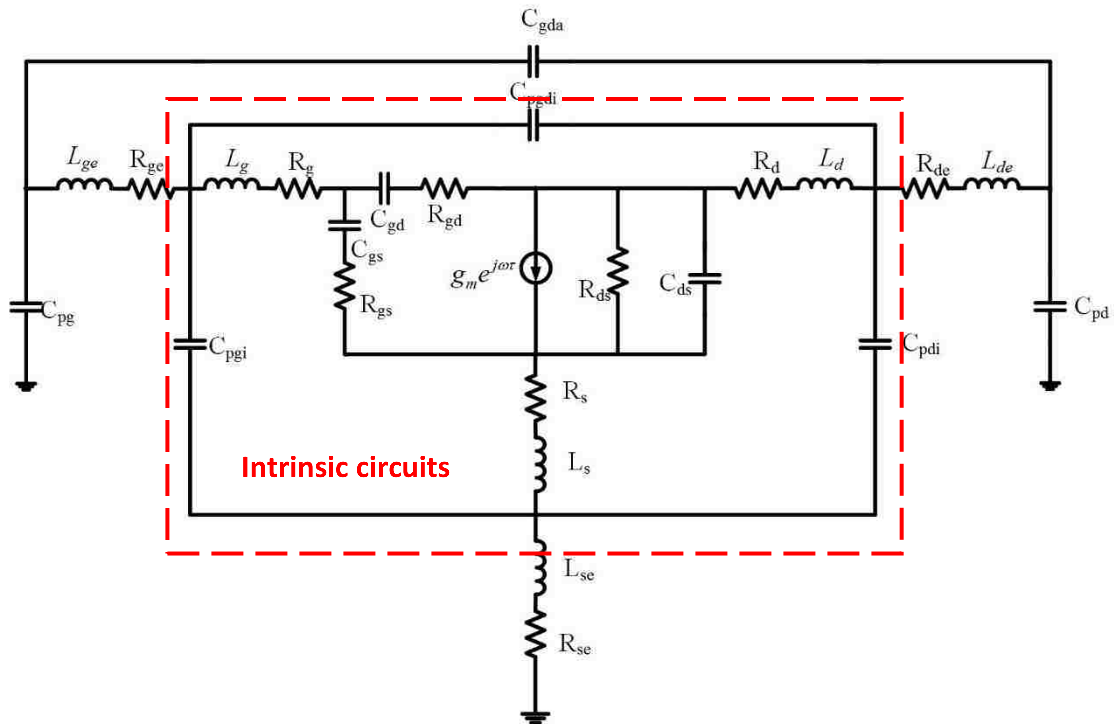


Fig. 2-10. Circuit model of a MOSFET, where C_{pg}, L_{ge}, R_{ge}, C_{pda}, C_{pd}, L_{de}, R_{de}, L_{se}, R_{se} are external parasitic elements, which can be de-embedded to get into the intrinsic circuits in red dotted line. Lg, Rg, R_d, L_d, R_s, L_s, C_{pgdi}, C_{pdi}, C_{pgi}, C_{gd}, C_{gs}, C_{ds}, R_{gs}, R_s, L_s, R_{gd}, R_d, g_m are intrinsic parameters.

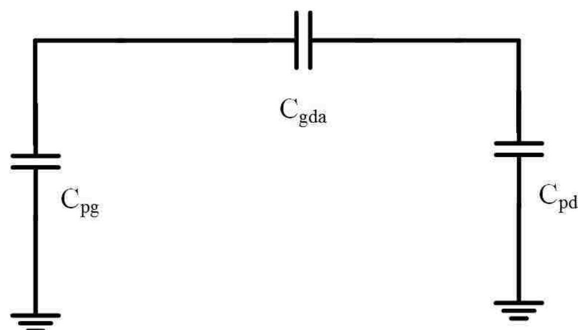


Fig. 2-11. Open structure equivalent circuit

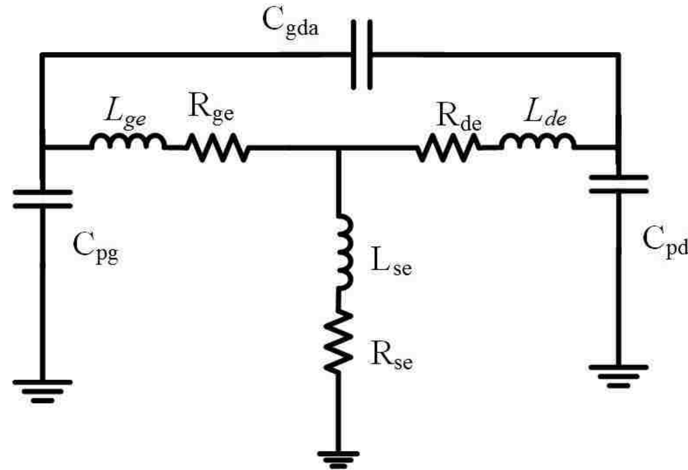


Fig. 2-12. Short structure equivalent circuit

Fig. 2-10 shows a small signal circuit model of a MOSFET, including both the external and internal parasitics. To get the real forward cut off frequency f_T and f_{MAX}, we should first de-embed the external parasitics using the open and short test structures. Fig. 2-11 and 2-12 show the circuit model of open and short test structures. By subtracting them from Fig 2-10, we can get rid of those undesired parasitics. ω is the frequency and Z is the Short structure *z-parameter* de-embedded from open structure. The overall de-embedding flow is show below:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \xrightarrow{S \to Y} \begin{bmatrix} Y_{11} - j\omega(C_{pgi} + C_{pgdi}) & Y_{12} - j\omega(-C_{pgdi}) \\ Y_{21} - j\omega(-C_{pgdi}) & Y_{22} - j\omega(C_{pdi} + C_{pgdi}) \end{bmatrix}$$

$$\Big\downarrow Y \to Z$$

$$\begin{bmatrix} Sint_{11} & Sint_{12} \\ Sint_{21} & Sint_{22} \end{bmatrix} \xleftarrow{S \leftarrow Z} \begin{bmatrix} Z_{11} - (R_g + R_s + j\omega L_s + j\omega L_g) & Z_{12} - (R_s + j\omega L_s) \\ Z_{21} - (R_s + j\omega L_s) & Z_{22} - (R_g + R_s + j\omega L_s + j\omega L_d) \end{bmatrix}$$

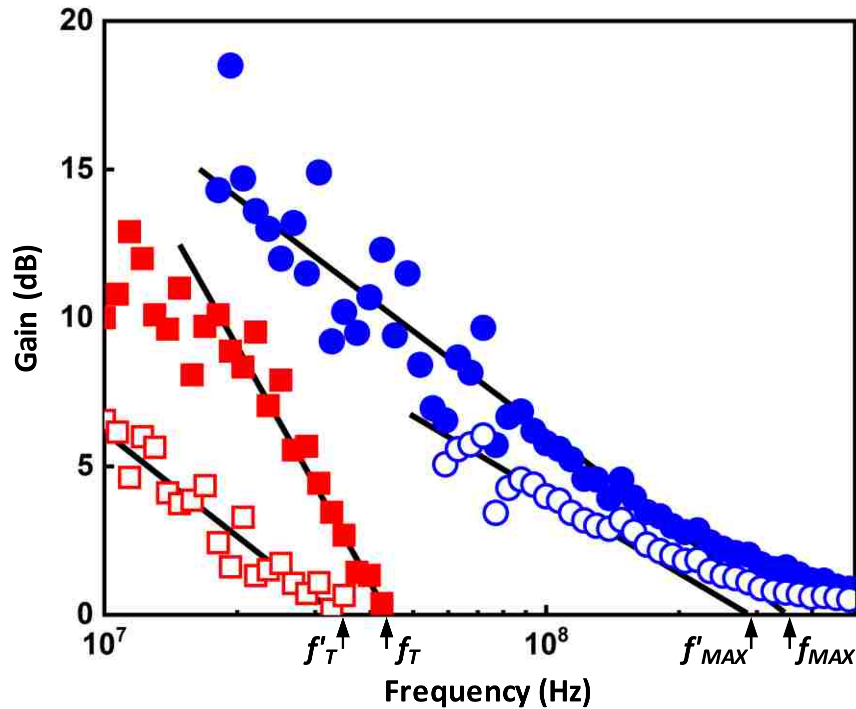


Fig. 2-13. Forward current cutoff frequency f_T and maximum frequency of oscillation f_{MAX} measured on a MOSFET with 12-nm-thick $PtSe_2$. f'_T and f'_{MAX} are corresponding values before probe-pad capacitances are de-embedded. $V_{GS} = -15$ V. $V_{DS} = -1$ V.

where *S* is the as measured *S-parameter* of a $PtSe_2$ MOSFET and *Sint* is the de-embedded *S-Parameter*. Fig. 2-13 shows the RF characteristics of a MOSFET fabricated on 12-nm-thick $PtSe_2$ without channel recess. As measured, the forward-current cut-off frequency f'_T is 32 MHz, whereas the maximum oscillation frequency f'_{MAX} is 180 MHz. Using open and short calibration structures fabricated on the same chip for de-embedding probe-pad capacitances, the de-embedded f_T and f_{MAX} are 45 MHz and 250 MHz, respectively. By random sampling of ten devices, standard deviations are such that $f_T = 42 \pm 5$ MHz and $f_{MAX} = 180 \pm 30$ MHz. Since most thin-film transistors are operated below 100 MHz, this confirms the potential of $PtSe_2$ MOSFETs for practical applications. Note that this is the first time RF characteristics are reported, since [14],

[15] and [18] all used the entire conducting substrate as a back gate which would have too much parasitic capacitances to operate at RF.

2.7 Summary

The emerging two dimensional (2D) material platinum diselenide ($PtSe_2$) is promising in high performance electric and optoelectronic devices for its high mobility, sizeable bandgap, stability, and ultra-low ohmic contact resistance. Thickness-dependent carrier transport and electrical contacts are studied. Semimetal-to-semiconductor property is observed and utilized in the channel recessed $PtSe_2$ MOSFETs, which provide a feasible way for 2D FETs with both low contact resistance and high *on/off* ratio. Wafer-scale fabrication of $PtSe_2$ MOSFETs was demonstrated by photolithography on Pt thermally assisted converted (TAC) under Se vapor at 400 °C. Ultra-low contact resistance $PtSe_2$ FETs was achieved, which is among one of the best 2D FETs. $PtSe_2$ thickness dependent gate modulation and semimetal-to-semiconductor transition were studied. Channel recessed $PtSe_2$ MOSFETs are promising which have low contact resistances with high *on/off* ratio. To further improve the gate modulation, controllable wet etching is desired to thin the channel. Taking advantage of the unique property of $PtSe_2$ to transition from semiconductor to semimetal as its thickness increases beyond a few monolayers, channel recess was adapted for improving gate control while keeping the contact resistance as low as 0.008 Ω·cm. The drain current at V_{GS} = −10, V_{DS} = −1 V were 25 ± 5, 57 ± 8, and 618 ± 17 μA/μm for 4-, 8-, and 12-nm-thick $PtSe_2$, respectively. The corresponding peak transconductances were 0.20 ± 0.1, 0.60 ± 0.05, and 1.4 ± 0.1 μS/μm. The forward-current cut-off frequency of 12-nm-thick $PtSe_2$ MOSFETs was 42 ± 5 MHz, whereas the corresponding frequency of maximum oscillation was 180

± 30 MHz. These results confirmed the application potential of $PtSe_2$ for future generation thin-film transistors.

Chapter 3: Conclusion

For the first time, wafer-scale fabrication of $PtSe_2$ MOSFETs was successfully demonstrated by photolithography on Pt thermally converted under Se vapor at 400 °C, which resulted in very uniform device characteristics. Taking advantage of the unique property of $PtSe_2$ to transition from semiconductor to semimetal as its thickness increases beyond a few monolayers, channel recess was adapted for improved gate control while keeping the contact resistance low. The contact and sheet resistances were in general agreement with that of MOSFETs individually crafted by direct-write electron-beam lithography on exfoliated $PtSe_2$ flakes. In all cases, the stronger-than-expected thickness dependence of the contact and sheet resistances confirmed that the semiconductor-semimetal transition was gradual and $PtSe_2$ a few nanometers thick might have small bandgap Despite successful demonstration of wafer-scale fabrication of $PtSe_2$ MOSFETs, much process improvement is needed. Thermal conversion of $PtSe_2$, although convenient with a low thermal budget, currently results in a mobility approximately an order of magnitude lower than the bulk value. This is typical of synthesized 2D films before the synthesis technique is gradually improved. For example, the thermally converted $PtSe_2$ is nanocrystalline, so its grain size and alignment may be improved by patterning Pt before conversion. Similarly, although metal sputtering is conforming and widely available, uniform sputtering of monolayer Pt is very challenging. Either the sputtering technique needs to be improved or atomic layer deposition of Pt needs to be developed despite being a noble metal. The current dry etching process for channel recess is too rough and damaging to thin the $PtSe_2$ to 1 nm. In the future, channel recess may be achieved by an addition instead of subtraction process. For example, 1-

nm-thick Pt can be deposited uniformly first. Pt 10-nm-thick Pt can then be selectively deposited in the source and drain regions through a lift-off process. Finally, such a recessed Pt structure can be thermally converted altogether as [18] has shown that even 20-nm Pt can be nearly 100% converted thermally.

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Vita

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