5-2011

Peripheral soldering of flip chip joints on passive RFID tags

Md Syful Islam
University of Nevada, Las Vegas

PERIPHERAL SOLDERING OF FLIP CHIP JOINTS

ON PASSIVE RFID TAGS

by

Md Syful Islam

Bachelor of Science in Mechanical Engineering
Bangladesh University of Engineering and Technology, Dhaka
1986

Master of Science in Mechanical Engineering
Bangladesh University of Engineering and Technology, Dhaka
1990

Master of Science in Mechanical Engineering
Tuskegee University, Tuskegee
2001

A thesis submitted in partial fulfillment
of the requirements for the

Doctor of Philosophy in Mechanical Engineering
Department of Mechanical Engineering
Howard R. Hughes College of Engineering

Graduate College
University of Nevada Las Vegas
May 2011

UNIVERSITY OF NEVADA LAS VEGAS

THE GRADUATE COLLEGE

We recommend the dissertation prepared under our supervision by

Md Syful Islam

entitled

Peripheral Soldering of Flip Chip Joints on Passive RFID Tags

be accepted in partial fulfillment of the requirements for the degree of

Doctor of Philosophy in Mechanical Engineering

Zhiyong Wang, Committee Chair

Brendan O'Toole, Committee Member

Woosoon Yim, Committee Member

Vellore Venkatesh, Committee Member

Rama Venkat, Graduate Faculty Representative

Ronald Smith, Ph. D., Vice President for Research and Graduate Studies
and Dean of the Graduate College

May 2011

ABSTRACT

Peripheral Soldering of Flip Chip Joints on Passive RFID Tags

by

Md Syful Islam

Dr. Zhiyong Wang, Examination Committee Chair
Associate Professor of Mechanical Engineering
University of Nevada, Las Vegas

Flip chip is the main component of a RFID tag. It is used in billions each year in electronic packaging industries because of its small size, high performance and reliability as well as low cost. They are used in microprocessors, cell phones, watches and automobiles. RFID tags are applied to or incorporated into a product, animal, or person for identification and tracking using radio waves. Some tags can be read from several meters away or even beyond the line of sight of the reader. Passive RFID tags are the most common type in use that employ external power source to transmit signals. Joining chips by laser beam welding have wide advantages over other methods of joining, but they are seen limited to transparent substrates. However, connecting solder bumps with anisotropic conductive adhesives (ACA) produces majority of the joints. A high percentage of them fail in couple of months, particularly when exposed to vibration.

In the present work, failure of RFID tags under dynamic loading or vibration was studied; as it was identified as one of the key issue to explore. Earlier investigators focused more on joining chip to the bump, but less on its assembly, i.e., attaching to the substrate. Either of the joints, between chip and bump or between antenna and bump can fail. However, the latter is more vulnerable to failure. Antenna is attached to substrate, relatively fixed when subjected to oscillation. It is the flip chip not the antenna moves

during vibration. So, the joint with antenna suffers higher stresses. In addition to this, the strength of the bonding agent i.e., ACA also much smaller compared to the metallic bond at the other end of the bump.

Natural frequency of RFID tags was calculated both analytically and numerically, found to be in kilohertz range, high enough to cause resonance. Experimental investigations were also carried out to determine the same. However, the test results for frequency were seen to be in hundred hertz range, common to some applications. It was recognized that the adhesive material, commonly used for joining chips, was primarily accountable for their failures. Since components to which the RFID tags are attached to experience low frequency vibration, chip joints fail as they face resonance during oscillation. Adhesives having much lower modulus than metals are used for attaching bumps to the substrate antennas, and thus mostly responsible for this reduction in natural frequency. Poor adhesive bonding strength at the interface and possible rise in temperature were attributed to failures under vibration.

In order to overcome the early failure of RFID tag joints, Peripheral Soldering, an alternative chip joining method was devised. Peripheral Soldering would replace the traditional adhesive joining by bonding the peripheral surface of the bump to the substrate antenna. Instead of joining solder bump directly to the antenna, holes are to be drilled through antenna and substrate. S-bond material, a less familiar but more compatible with aluminum and copper, would be poured in liquid form through the holes on the chip pad. However, substrates compatible to high temperature are to be used; otherwise temperature control would be necessary to avoid damage to substrate. This S-

bond would form metallic joints between chip and antenna. Having higher strength and better adhesion property, S-bond material provides better bonding capability.

The strength of a chip joined by Peripheral Soldering was determined by analytical, numerical and experimental studies. Strength results were then compared to those of ACA. For a pad size of 60 micron on a 0.5 mm square chip, the new chip joints with S-bond provide an average strength of 0.233N analytically. Numerical results using finite element analysis in ANSYS 11.0 were about 1% less than the closed form solutions. Whereas, ACA connected joints show the maximum strength of 0.113N analytically and 0.1N numerically. Both the estimates indicate Peripheral Soldering is more than twice stronger than adhesive joints.

Experimental investigation was carried out to find the strength attained with S-bond by joining similar surfaces as those of chip pad and antenna, but in larger scale due to limitation in facilities. Results obtained were moderated to incorporate the effect of size. Findings authenticate earlier predictions of superior strengths with S-bond. A comparison with ACA strength, extracted from previous investigations, further indicates that S-bond joints are more than 10 times stronger.

Having higher bonding strength than in ACA joints, Peripheral Soldering would provide better reliability of the chip connections, i.e., RFID tags. The benefits attained would pay off complexities involved in tweaking.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ACKNOWLEDGMENTS

First of all, the author is grateful to Almighty God Who has enabled him to conduct this research. The author expresses his gratitude to his advisor, Dr. Z. Wang, for his guidance and suggestions as well as informal inspiration that directed toward the successful completion of the research. The author also expresses his gratefulness to Dr. Brendan O'Toole and Department Chair Dr. Woosoon Yim for their support and help for carrying out this research. The author expresses his gratefulness to Dr. Venkatesh for editing a journal paper. The author cordially remembers the cooperation of Dr. Hartmann of Harry Reid Center and Kevin Nelson of machine shop. The author is thankful to other peers including Department Secretary Joan Conway who helped in different issues during the research. The author appreciates providing free ACF samples by Roxanne Jang of 3M and RFID tag samples by Texas Instruments. The author recognizes the sacrifices of his family members for this research. Finally the author expresses his thanks to the committee members for their suggestions and review.

CHAPTER 1

INTRODUCTION

Flip chips or silicon chips are used in billions every year primarily in electronic packaging industries. They are being used in microprocessors, cell phones, watches and automobiles. The boom in flip chip packaging results both from the advantages in its small size (fraction of a millimeter), high performance, wide flexibility, good reliability, and low cost over other packaging methods and from the widening availability of flip chip materials, equipment, and services. This chapter discusses about their different types and methods of joining to substrates.

1.1 RFID tags

RFID stands for Radio Frequency Identification. RFID tags are applied to or incorporated into a product, animal, or person for identification and tracking using radio waves. Some tags can be read from several meters away and beyond the line of sight of the reader. Barcodes, on the other hand, should be visible and only can be scanned from a distance of a foot or less. RFID chips are very similar to barcodes in the sense that a certain amount of data is contained within them, and then transmitted to a reading device which then processes and utilizes the information. They can be scanned through clothes, wallets, and even cars.

There are generally three types of RFID tags: active RFID tags, which contain a battery and can transmit signals autonomously, passive RFID tags, which have no battery and require an external source to provoke signal transmission, and battery assisted passive (BAP) RFID tags, which require an external source to wake up but have significant higher forward link capability providing greater range. The passive type is the

mostly used one; it contains an antenna in which a current induced in it when within range of the RFID reader. The tag then uses that electricity to power the internal chip, which bounces the data back out through the antenna, from where reader picks it up. RFID tags for animals represent one of the oldest uses of RFID technology. Originally meant for large ranches and rough terrain, since the outbreak of Mad Cow Disease, RFID has become crucial in animal identification management. Libraries use RFID tags in the form of square book tag, round CD/DVD tag and rectangular VHS tag. RFID tags are used in enterprise supply chain management to improve the efficiency of inventory tracking and management. Card companies are now looking for payment solutions for adding contactless payment cards to any mobile phone using RFID technology. Governments use RFID applications for traffic management, while automotive companies use various RFID tracking solutions for product management. Many of these solutions may work together in the future, though privacy regulations prevent many initiatives from moving forward at the same pace that technology allows. RFID can be used in a variety of applications, such as: access management, tracking of goods and RFID in retail, tracking of persons and animals, toll collection and contactless payment, machine readable travel documents, smart dust (for massively distributed sensor networks), location based services, tracking sports memorabilia to verify authenticity, airport baggage tracking logistics etc. Some RFID tags are shown in Fig. 1 below.

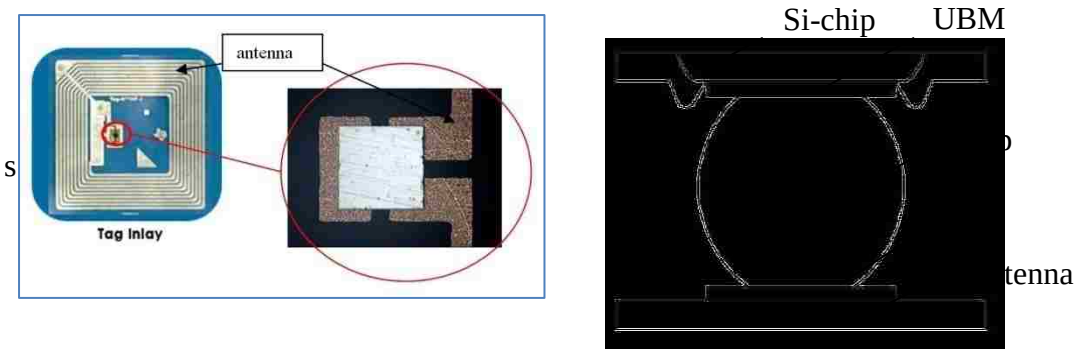
Fig. 1: RFID tags

1.2 Common problems

Some common problems with RFID are reader collision and tag collision. Reader collision occurs when the signals from two or more readers overlap. The tag is unable to respond to simultaneous queries. Systems must be carefully set up to avoid this problem. Tag collision occurs when many tags are present in a small area; but since the read time is very fast, it is easier for vendors to develop systems that ensure that tags respond one at a time. Moreover some tags fail in few months when subjected to vibrations.

1.3 Flip chip joints

Flip chips (integrated circuit chips / dies) are the main component of RFID tags. Flip chip joints are microelectronic assembly in which direct electrical connection of face-down (hence, "flipped") chips are made onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip bond pads. Flip chip components are predominantly semiconductor devices; however, components such as passive filters, detector arrays, and micro electro-mechanical systems (MEMs) devices are also beginning to be used in flip chip form. A schematic view of chip joint is shown in Fig. 2.



(a) RFID tag sketch (b) Cross sectional view of (a)

Fig. 2: Schematic view of a flip chip joint structure

1.4 Bonding steps

Flip chips are joined in three steps: (a) forming UBM (under bump metallization), (b) forming bump, and (c) attaching to antenna (circuit board). In most applications the substrate is integrally connected to the antenna that increases signal reception distance of a chip. Usually the remaining space between the chip and antenna is filled with non-conductive adhesives. Chips are provided with two bonding pads for contacting to external circuit. Some methods avoid the second step, thus join chip UBM directly onto substrate with adhesives with or without the application of bonding compression while others use formation of bump (commonly solder bump) on the UBM and then joining it.

1.4.1 Making UBM

The final metal layer of most IC bond pads is aluminum, providing a satisfactory surface for conventional wire bonding. Unfortunately, this surface is inhospitable to most conductive bumps. Aluminum forms an oxide immediately upon exposure to air, and this native oxide is an electrical insulator. Aluminum does not provide a readily solderable surface: neither wettable nor bondable by most solders. Aluminum may corrode over

time when not protected from the environment. Consequently, successful bumping must first replace the oxidized aluminum surface with a more hospitable material, the UBM.

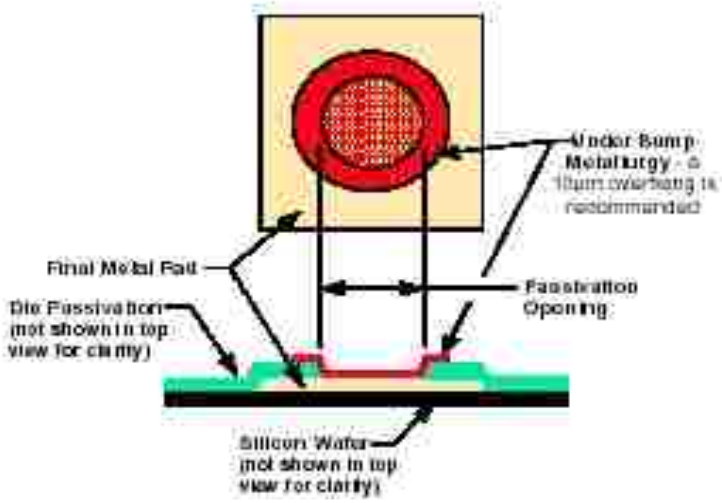


Fig. 3: UBM design

This UBM must meet several requirements. It must provide a strong, stable, low resistance electrical connection to the aluminum. It must adhere well both to the underlying aluminum and to the surrounding IC passivation layer, hermetically sealing the aluminum from the environment. The UBM must provide a strong barrier to prevent the diffusion of other bump metals into the IC. The UBM must be readily wettable by the bump metals, for solder reflow. Meeting all these requirements generally requires multiple layers of different metals, such as an adhesion layer, a diffusion barrier layer, a solderable layer, and an oxidation barrier layer. The UBM layers must be compatible metals, which in combination have low internal mechanical stresses. The composite UBM should result from processes that are relatively simple, inexpensive, and easily reproducible in volume production. The design of the UBM should provide a metal layer

that adequately defines and limits the applied bump (hence called, the "bump-limiting metal") while overlapping the die passivation. Fig. 3 shows a typical design layout for UBM relative to the original pad. The IC pad aluminum oxide may be removed by sputter etching, plasma etching, ion etching, or by a wet chemical treatment. Successive UBM layers may be vacuum deposited by evaporation or sputtering, or be chemically plated. UBM deposition processes generally require wafers of IC die, rather than individual die. The wide and growing array of UBM compositions (e.g. Cr:Cr-Cu:Cu, Ti:Ni-V, Ti:Cu, Ti:W: Au, Ni: Au) results in part from the desired bump material and characteristics, in part from the intended end use application, and in part from the experience and the invested capital base of the manufacturer. The required metallurgies are part art, part science, and part accumulated experience. About 75% of UBM currently produced consists of multi-metal layers evaporated or sputtered in a vacuum system. A typical process sequence would be:

1. Sputter etches the native oxide to remove oxide and expose fresh aluminum surface.
2. Deposit 100 nm Ti / Cr / Al as the adhesion layer.
3. Deposit 80 nm Cr: Cu as the diffusion barrier layer.
4. Deposit 300 nm Cu / Ni: V as the solder-wettable layer.
5. Deposit 50 nm Au as the oxidation barrier layer (optional).

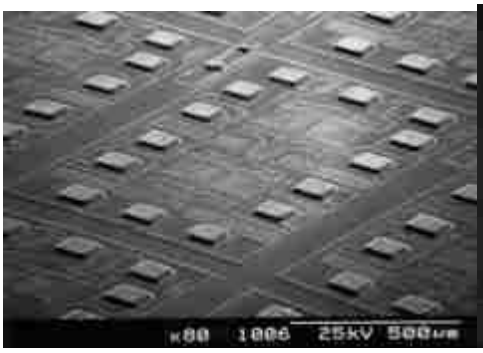


Fig. 4: Wafer with UBM

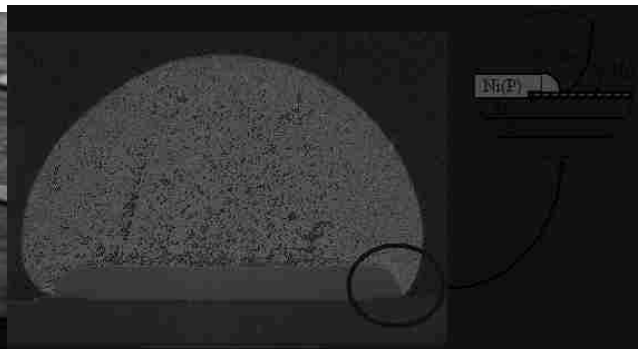


Fig. 5: Solder bump with UBM covering passivation

Electroless nickel UBM is unique in being a wet-chemical process that requires neither vacuum processing nor masking. Fig. 4 shows a wafer with electroless nickel UBM on the bond pads. The aluminum oxide is chemically etched, and replaced with zinc seed crystals. Nickel is electrolessly plated over the zinc as a barrier layer and solderable layer, and immersion gold is plated over the nickel as an oxidation barrier. The bump normally entirely covers the UBM, concealing it from view. The size of the UBM controls the spread, and therefore affects the resulting height, of a solder bump. Fig. 5 is a cross-section of a solder bump showing the underlying electroless nickel-gold UBM overlapping the die passivation (Si_3N_4).

The robustness of a particular UBM depends on its composition, deposition process, and the skills of the manufacturer. Low stress, stable films are desired, and the deposition process governs the initial tensile or compressive stresses within the layers. However, crystalline changes and grain growth within in the metals can change the characteristics of the film throughout its lifetime. For example, the aluminum, nickel, and copper constituents can undergo substantial re-crystallization at temperatures below 150^0C, changing the structure and stresses. Higher temperatures during reflow or subsequent

processing can cause dissolution of UBM materials. There is no perfectly optimal UBM, and practical UBM formulations require tradeoffs between competing constraints. For example, high temperature or high power applications would benefit from a high copper content, but copper dissolves readily and has a high re-crystallization rate. Electroless nickel UBM is a relatively low cost wet chemical process, but electroless nickel has almost ten times re-crystallization rate of sputtered nickel. The entire UBM/ bump system must reflect a balancing of capabilities and costs. A growing number of suppliers can provide UBM, bumping, or technology transfer and licensing of those skills. While most flip chip users need not and probably should not start out by depositing their own UBM; they should be aware of the tradeoffs to be evaluated in seeking a source to provide UBM. They should also be aware that the related metallurgy depends heavily on experience, and that producing good, reproducible, stable UBM requires more than just a chemistry set and a cookbook.

1.4.2 Making bumps

Solder bumps may be formed or placed on the UBM in many ways, including evaporation, electroplating, printing, jetting, stud bumping, and direct placement. The results of these methods may differ in bump size and spacing (pitch), solder components and composition, manufacturing time, cost, equipment required, assembly temperature, and UBM. The bump serves several functions in the flip chip assembly. Electrically, the bump provides the conductive path from chip to substrate. It also offers a thermally conductive path to carry heat from the chip to the substrate. In addition, the bump gives part of the mechanical mounting of the die to the substrate. Finally, it endows with a spacer, preventing electrical contact between the chip and substrate conductors, and

acting as a short lead to relieve mechanical strain between board and substrate. A process chart for the formation of UBM and bump is shown in Fig. 6.

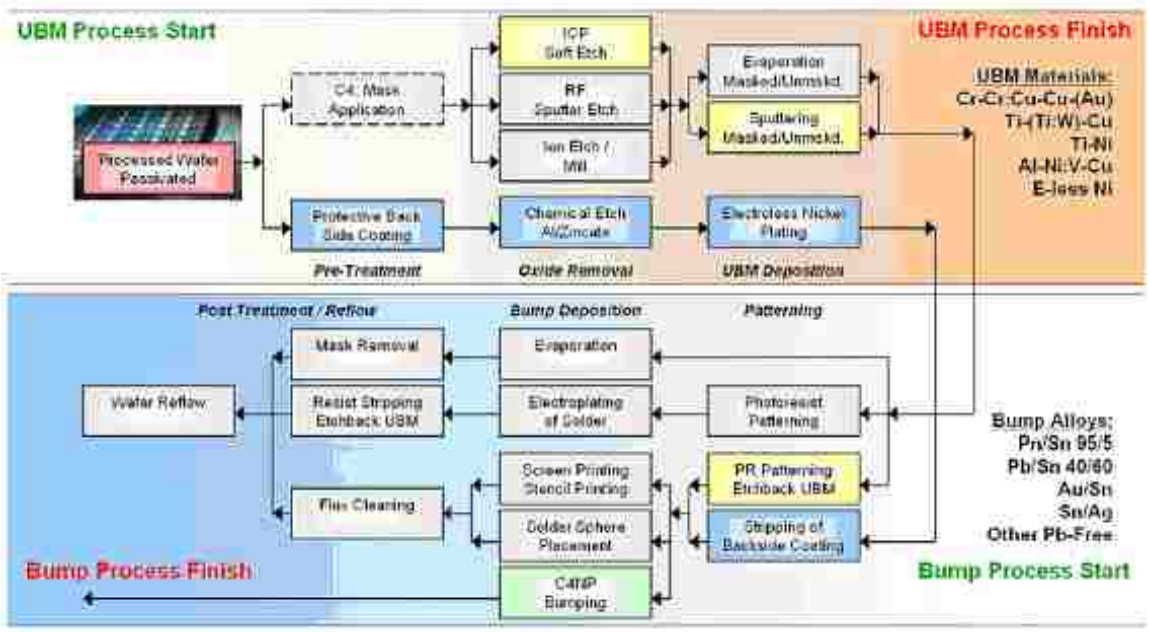


Fig. 6: A process chart for UBM and bump formation

1.4.2.1 Evaporated UBM / Evaporated solder

The pioneering IBM controlled collapse chip connection (C4) process was based on evaporation of the UBM and the solder onto the cleaned wafer pads. A metal mask aligned with and mechanically clamped to the wafer at a controlled spacing that defines evaporated deposits. The UBM evaporation is followed by evaporation of high lead solder to form the bumps. Low lead eutectic solder cannot be evaporated because of the difference in vapor pressures of lead and tin. Bump size and shape is determined by the mask openings and spacing. The evaporated solder (Fig. 7, 8) is reflowed to form a spherical solder bump. The evaporated bump allows good control of the alloy and

uniform bump heights. The process is limited to high lead solders with binary (two-component) alloys. It cannot be easily scaled up to larger wafers, and has a limited throughput, high capital equipment costs and high licensing fees.

1.4.2.2 Sputtered UBM / Electroplated solder

Electroplating of solder (Fig. 9) was developed as a less costly and more flexible method than evaporation. The UBM is sputtered or evaporated over the entire surface of the wafer, providing a good conduction path for the electroplating currents. Bumping begins with photopatterning and plating a copper minibump on the bump sites. This thick copper allows the use of high tin eutectic solders without consuming the thin copper UBM layer. A second photopatterning and plating of the solder alloy over the minibump forms the solder bump. The photoresist is then removed from the wafer and the bump is reflowed to form a sphere. Electroplated bumping processes generally are less costly than evaporated bumping. Plating can allow closer bump spacing (up to 50 microns) than other methods of bump formation. It is popular for high bump count (>3,000) chips because of its small feature size and precision. However, plating bath solutions and current densities must be carefully controlled to avoid variations in alloy composition and bump height across the wafer.

1.4.2.3 Sputtered UBM / Printed solder

This method was developed in combination of thin film UBM with printed solder bumps by Delco and others to overcome some of the limitations of evaporated and electroplated bumps. Typically, the UBM consists of sputtered aluminum as the adhesion layer, nickel as a solder-wettable barrier layer, and copper as wetting layer. These layers except over the bond pad opening are removed by Photopatterning and etching.

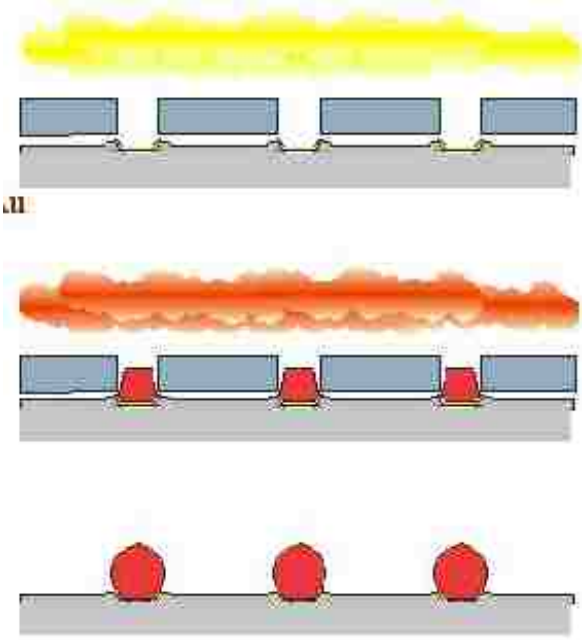


Fig.7: Evaporation through mask

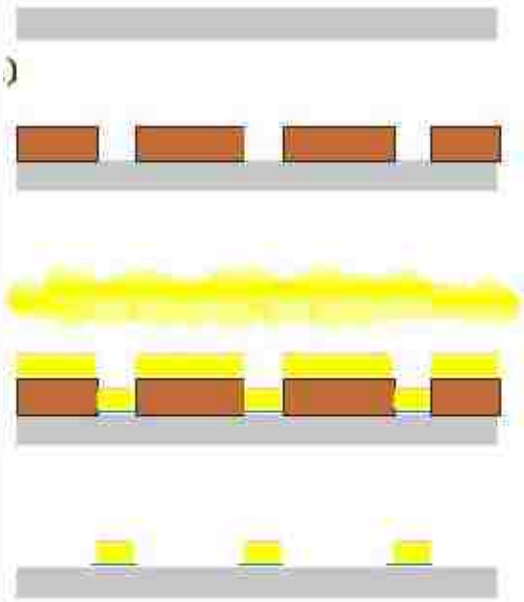


Fig. 8: Evaporation with photoresist

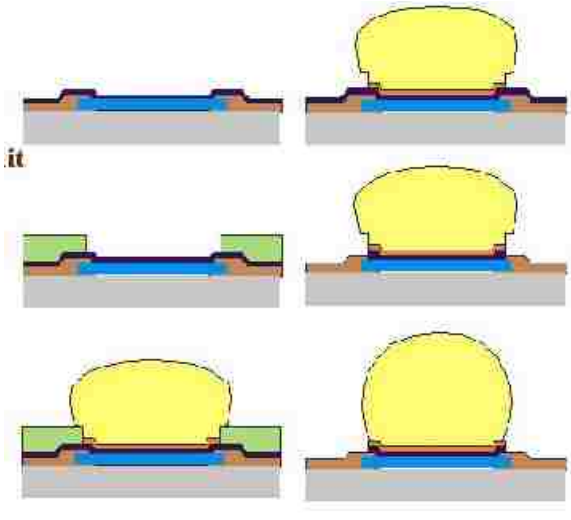


Fig. 9: Electroplated bump

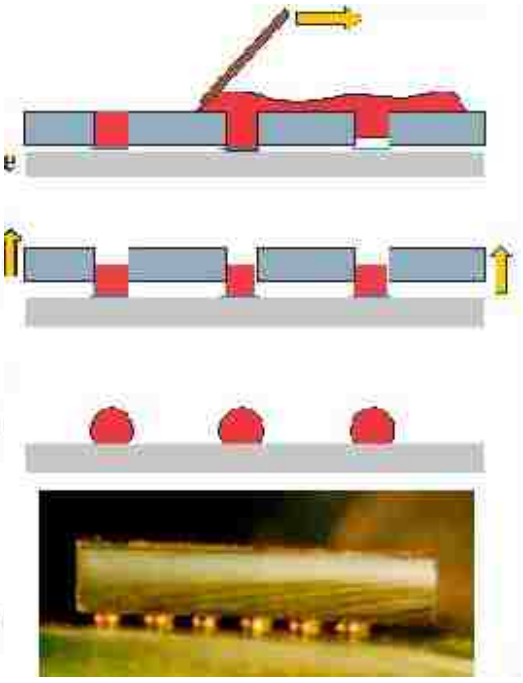


Fig. 10: Screen printing

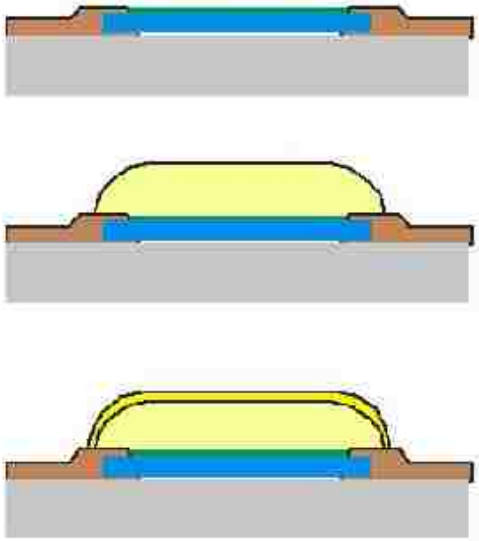


Fig. 11: Electroless plating

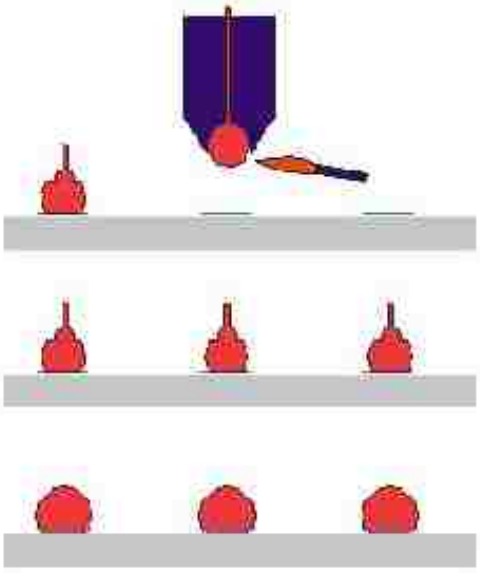


Fig. 12: Stud bumping

Solder is deposited by printing solder (Fig. 10) paste onto the UBM by stencil or other openings and reflowing the solder paste to form a spherical solder bump. Solder paste gives good control of the bump composition, and allows a variety of alloys to be used, including eutectic, lead-free, non-binary, and low alpha particle solders. The resulting process is less costly than evaporated processes, and comparable in cost to electroplating. The UBM adheres well to the bond pad and passivation, protecting the aluminum pad. Printed solder bumps cannot achieve the close spacing of plated bumps, with current production typically limited to 150 micron or greater spacing. Processing of larger (300 mm) wafers will require more costly sputtering equipment.

1.4.2.4 Electroless UBM / Printed solder

Electroless plated UBM promises to be the lowest cost approach to solder bumping (Fig. 11), because it eliminates thin film and masking steps and permits batch processing.

The UBM is formed by selective chemical plating, in a wet chemical, maskless process. A protective layer of resist first covers the wafer backside. An alkaline zincate solution removes the bond pad aluminum oxide layer and etches the surface. An electroless plated nickel layer forms the barrier and wettable layer. It is protected from oxidation by an immersion gold layer. The electroless nickel may also be plated higher to form a bump for adhesive or other non-solder flip chip assembly. Electroless Ni-Au UBM requires that all exposed metal other than the pads be passivated or covered with resist. The plating baths must be carefully controlled and kept free of contaminants to insure uniform plating. Solder bump deposition is by stencil printing of solder paste (Fig. 10). The solder bump is reflowed and flux residues are removed. The cost advantages of the electroless UBM solder bump process result from eliminating the masking and metal sputtering required by other methods, and allowing parallel batch processing of multiple wafers, which increases throughput and reduces costs. The solder dispensing process, not the UBM process, limits pitch.

1.4.3 Other solder bumping methods

Less common methods of solder bumping include solder bump bonding with solder wire, solder jetting with molten solder, and solder ball placement directly onto the UBM. Solder bump bonding (SBB) uses solder wire in a modified wire bonder to place a ball of solder directly onto the bond pad. The scrubbing action of the wire bonder causes the solder ball to bond to the bond pad. The solder wire is broken off above the bump, leaving the bump on the pad, where it can be reflowed. SBB is a serial process, producing bumps one by one at rates up to about 8 per second. It has advantages in allowing closer spacing than printed bumps. Solder jetting places solder bumps on Ni-Au UBM by

controlling a stream of droplets of molten solder. Demand mode jetting systems use piezoelectric or resistive heating to form droplets in much the same manner as an ink-jet printer. Mechanical positioning directs the droplet placement. Continuous mode jetting systems use a continuous stream of solder droplets with electrostatic deflection of the charged droplets to control placement. Solder ball placement bumping depends on directly placing micro-spheres of solder on the UBM, similar to methods well developed for ball-grid array (BGA) and chip scale packages (CSP).

1.4.3.1 Stud bump flip chip

Since stud bumping (Fig. 12) can be done on a wire bonder, it does not require wafers UBM. Single, off-the-shelf die can be bumped and flipped without pre-processing. This makes stud bump flip chip fast, efficient, and flexible for product development, prototyping and low to medium volume production. Because stud bumping is a serial process, the bumping time required increases with the number of bumps. However, high-speed equipment now can place as many as 12 bumps per second. Stud bump assemblies demand more precise die placement equipment and are less tolerant of placement errors than self-aligning solder assemblies.

Gold stud bumping process creates conductive gold bumps on the die bond pads, and connects the die to the circuit board or substrate with adhesive or ultrasonic assembly. Stud bumping requires no under-bump metallization (UBM), and thus does not require wafer processing; individual die can be stud bumped as easily as they can be wire bonded. Gold stud bumps are placed on the die bond pads through a modification of the ball bonding process used in conventional wire bonding. In ball bonding, the tip of the gold bond wire is melted to form a sphere. The wire-bonding tool presses this sphere

against the aluminum bond pad, applying mechanical force, heat, and ultrasonic energy to create a metallic connection. The wire bonding tool next extends the gold wire to the connection pad on the board, substrate, or lead frame, and makes a stitch bond to that pad, finishing by breaking off the bond wire to begin another cycle. For gold stud bumping, the first ball bond is made as described, but the wire is then broken close above the ball. The resulting gold ball, or stud bump remaining on the bond pad provides a permanent, reliable connection through the aluminum oxide to the underlying metal. The pull-off gold bumps were realized using a Panasonic wire-bonding machine with 1 mil (25 µm) gold wire. This resulted in approximately spherical bump of 75 and 50 µm in diameter and height respectively. After placing the stud bumps on a chip, they may be flattened (or coined) by mechanical pressure to provide a flatter top surface and more uniform bump heights, while pressing any remaining wire tail into the ball. Immediately after forming, a tool may coin each bump or all bumps on the die may be simultaneously coined by pressure against a flat surface in a separate operation following bumping.

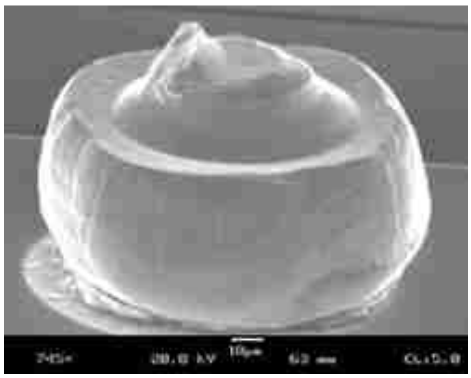


Fig. 13: A copper stud bump

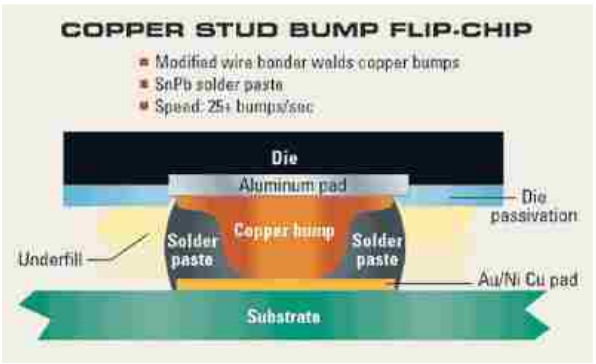


Fig. 14: Flip chip assembly of copper bumped wafers

Gold stud bump can easily achieve pitches of less than 100 microns and be placed on pads of less than 75 microns. A die may be attached by adhesives, or by ultrasonic assembly without adhesive, depending on the die size and the application temperature requirements. Assemblies with gold-to-gold connections may not require undefilling.

Copper stud bumps provide a base for solder-adhesion without requiring UBM or electroless nickel/gold bumps, simplifying the process because they do not require additional wafer fabrication or plating operations. Copper stud bumps are formed with a modified automatic wire bonder at high speeds. Fig. 13 shows a copper stud bump, and Fig. 14 illustrates the assembled structure. The formation of stud bumps is a variation of the wire bonding process. The wire bonder forms a ball on the tip of a wire protruding from the capillary which then descends to the work surface and bonds the ball. Instead of moving on to form a wire loop, as in a typical wire bond, the capillary rises and terminates the wire above the ball before forming a new ball and repeating the process. In the case of the copper stud bump, additional motions occur during the wire termination to produce a flat-shaped bump, preferable for flip-chip. Once the solder is screened on the stud, the chip is placed on the pre-fluxed site on the substrate and reflowed. The capillary underfill is dispensed and cured after the cleaning of the solder residue. The stud bump can alternatively be assembled using no flow underfill (NFU). NFU enables a single reflow that simultaneously attaches the bump to the substrate and cures the underfill. Copper stud bumps typically have shear strength of ~110 MPa, comparable with that of the aluminum bond pad. Even though the copper bump is a high-strength interconnection, the solder (tensile strength, 37 MPa; creep strength, ~3 MPa) remains the weak link mechanically. Underfill bonds to both the chip and substrate, mechanically strengthening

the integrity of the joint for improved fatigue strength during thermal cycling. However, thermal-cycle failures have been observed which were attributed to problems at the copper bump/ aluminum bond pad interface.

1.5 Joining to antenna/ substrate (assembly)

Bumps are bonded to antenna mostly by adhesives; heating also used in combination. Some methods employ heat without adhesives**.**

1.5.1 Adhesive joining

Some methods join UBM with antenna directly with adhesives. But majority of the joints are made with bumps joined to antenna with anisotropic conductive film (ACF) or paste (ACP). For direct adhesive bonding, isotropic conductive adhesive (ICA) is dispensed by stencil printing onto the substrate bond pads, or the bumped die may be dipped into a thin layer of adhesive, coating only the bumps with adhesive. Stenciled isotropic adhesive assembly provides a larger quantity of adhesive than dipped assembly, making a mechanically stronger bond. The additional adhesive compensates to some degree for bump height variations. A panelized array of substrates may be simultaneously stenciled in one operation, speeding up assembly. The stenciled adhesive can be inspected or measured before die mount to insure uniformity. However, stenciling requires a high-precision stencil printer and stencils. After the isotropic conductive adhesive is heat cured, a non-conducting underfill adhesive is applied to completely fill the under-chip space. Dipping requires a thin, precisely controlled layer of adhesive and co-planarity of the die and adhesive during the dipping process. Since dipping places adhesive only on the bump surface, the minimum bump spacing is smaller than for stenciling, to pad pitches of 60 microns or less (Riley, 2000). Dipping does not require

additional equipment as stenciling does, since the die mount aligner bonder can be used for dipping. However, dipping requires careful control of the adhesive layer thickness, and dipping is a serial process, lengthening throughput time. A non-conductive adhesive is dispensed or stenciled at the die location on the substrate. The bumped die is pressed against the substrate pads with enough force give compressive dispersion of the adhesive, allowing no adhesive to remain between the stud bump and substrate pad mating surfaces. This pressure is maintained while the assembly temperature is elevated for sufficient time to at least partially cure the adhesive. The chip is mechanically bonded to the substrate by the cured adhesive, with metal-to-metal contact between the bumps and substrate pads. No separate underfill adhesive is required. Non-conductive adhesive has advantages for assembly onto flexible substrates, since the adhesive is cured while in the aligner-bonder, keeping the die fixed in location thereafter. Dispensing the adhesive properly and repeatability requires automated equipment, and the aligner-bonder throughput is determined by curing time, including ramping up and down from the curing temperature.

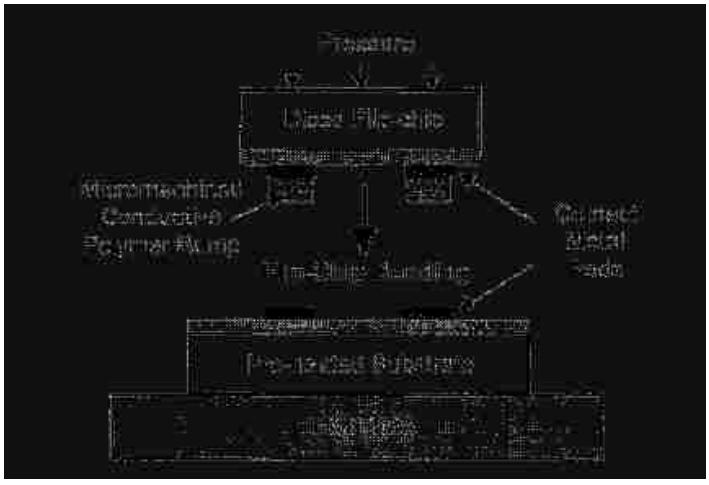


Fig. 15: Joining of an unbumped chip with adhesive

Underfill adds mechanical strength to the assembly and protects the connections from environmental hazards. However, its most important purpose is to compensate for any thermal expansion difference between the chip and the substrate. Underfill mechanically locks together chip and substrate so that difference in thermal expansion does not break or damage the electrical connection of the bumps. Underfill adhesive may be dispensed along one or more edges of the die, being drawn into the space under the die through capillary action. Heat-curing the underfill adhesive completes the assembly process.

Anisotropic conductive adhesives (film and paste- ACA: ACF/ACP)) consist of an epoxy adhesive with dispersed conductive particles. They are used as electrical–mechanical interconnecting materials for flip-chip to flexible substrates and flip chip to glass substrates. Underfill is also used with ACA. Contact resistance and adhesion strength are two important features of anisotropic conductive adhesive joints. Contact resistance is affected by the curing degree of the adhesive, the bump characteristics, the reflow process and the environmental application conditions. Adhesion strength is affected by bonding temperature, bonding pressure, bubbles in the joints and particle characteristics (Wang et al., 2008).

1.5.2 Thermosonic joining

Prior to the thermosonic bonding, co-planarity of the die and the substrate is carefully aligned to achieve good bonding (Cheah et al., 2001). The bonding procedure begins with the substrate sitting on a heated stage. A vacuum holds the substrate in place. The temperature of the substrate is maintained at 150 °C. The chip is held by the bonding tool with vacuum and is brought into contact with the substrate. When the bonding force is reached a certain level, ultrasonic vibration is applied through the ultrasonic tool for a

predetermined length of time to complete the process. This method is mostly suitable for gold bumps.

1.5.3 Joining with heat

For low melting point bumps, chips are placed in flux or solder paste on the substrate and the assembly is reflowed. The joint is formed through the melting of bump, and the paste, where applicable. The high melting point bumps are joined to the substrate by melting either the solder paste or a low melting alloy on the bumps or on the conductors on the substrate (Boustedt, 1998). Joining with heat is simple, but has the inherent danger of chip damage due to shortening of terminals or overheating.

1.6 Objectives

Objectives of the present research are:

(a) to identify the problems in present flip chip joints,

(b) to suggest an alternate technique for solving existing problems,

(c) to study the feasibility of the proposed method, and

(d) to compare the strength of the new method with existing ones.

CHAPTER 2

LITERATURE REVIEW

Researchers develop new flip chip joining methods/ patterns every year; each has a differing set of strengths and limitations, which suit them for differing applications. This chapter discusses about the findings of some earlier investigators.

2.1 Research related to the formation of UBM and bump

Mangold and Lance (1998) developed a process for fabricating a solder bump having an improved geometry that included the steps of evaporatively depositing a first metallization system to form a post having a predetermined volume onto an integrated circuit having a passivation layer defining a die pad window, wherein the length of the post was greater than the width of the post, and wherein the length of the post extended beyond the die pad window over the passivation layer, and evaporatively depositing a second metallization system onto the post to form a cap also having a volume, wherein the first metallization system forming the post and the second metallization system forming the cap, when reflowed, formed an eutectic solder bump.

Yap and Lawyer (2004) developed solder bump structure that included a multi layer UBM having a major upper surface with solder wettable cap-layer for containing a solder bump, the multi layer UBM projecting from the substrate with an exposed sidewall; a thin of metal selected from a group consisting of titanium, chrome, titanium-nickel-titanium composite, a titanium-nickel-chrome composite, a titanium-platinum-titanium alloy, and a titanium-nickel-oxidized silicon composite deposited over or under the multi layer UBM and covering the exposed sidewall of the multi layer UBM. The completed solder bump structure was formed by subsequently heating the substrate to

melt the solder and wet it back. Another portion of the solder bump structure was initially formed on a separate substrate that was subsequently bonded to the first substrate by means of solder, preferably by using heat.

Yoon et al. (2008) investigated the formation of Au–20 wt. % Sn flip chip solder bumps using sequential electroplating method with Sn and Au. They obtained eutectic Au–20Sn solder bumps with a diameter of 100 μm on the patterned silicon wafer. After reflowing and aging at 150 ^{0}C for up to 1000 h, they investigated the interfacial reaction between the Au–20Sn solder and Ni under bump metallization (UBM). The Au–Ni–Sn, ternary, intermetallic compound (IMC) layer was formed, and the resettlement of δ-phase was confirmed during aging. The shear force was also measured to evaluate the effect of the interfacial reactions on the mechanical reliability as a function of aging time. The shear force was stable and the fracture occurred on the Ti/Cu metallization layer independent of the aging time. It was claimed that the results from their study confirmed the mechanical robustness of the Au–20Sn/Ni flip chip solder joint.

Kloeser et al. (2000) developed low cost bumping method by stencil printing. Their experimental work on fine pitch printing showed that, the printing down to 200 μm pitch could be performed without quality and yields reduction, with optimized stencil design and solder pastes. This technology was seen suited for high volume applications, and experiences with solder paste printing down to 150 μm pitch showed that the printable pitch could be decreased down to pad configurations for wire bonding technology.

Chen et al. (2004) proposed a flip chip bumping method for fabrication of solder bumps on a semiconductor wafer for flip chip application that was intended to a plurality of chip regions which were delimited from each other by a predefined cutting line each of

which was formed with a plurality of aluminum or copper based bond pads, and was characterized in the provision of a plating bus over and along the cutting line and connected to each bond pad. By means of this plating bus the required UBM fabrication and solder-bump fabrication could be both carried out through plating. They claimed that it would reduce the cost; since plating process was considerably lower in cost than sputtering or etching process.

Nam et al. (2007) fabricated a flip chip solder bump using a thin dewetting mold and the ultrasonic filling method. The process consisted of filling the cavities of a stainless steel mold with lead-free solder using ultrasonic vibration, and transferring the solder bump pattern of the mold to a substrate using reflow soldering. Pressures, induced by ultrasonic and mold vibration, were predicted analytically, and the ultrasonic pressure was larger than the pressure induced by the surface tension, which trapped the vapor at the mold cavity. Contact and non-contact modes were used to fill the through-hole and blind-hole molds, and the solder bump patterns of the mold were transferred to the Cu pads of a polyimide film through reflow soldering.

Schreiber and Le (1998) invented an integral copper column with a solder bump flip chip. They formed long bumps by connecting the contact pad on chip and the raised feature of the antenna to form an integral copper column. But it required special mandrel to shape the antenna into raised feature.

Chen and Xiao (2007) invented a series of processes and methods to manufacture solder bumps on the wafer, which shrunk the space and reduce the cost of manufacturing. A design method and relevant manufacturing processes were introduced to form an organic material or metal layer, called a Bump-Reflow Control Layer. The pad patterns

could be defined by this method. A mechanical part was designed with a hermetic cover to improve the photoresist process. A series of photolithography process including the designing of related mask was introduced to achieve high quality and thick photoresist.

Boustedt (1998) found that, when soldering flip chips, the surface tension of the molten solder pulled the chip to its correct position, i.e., the chip self-aligned. This meant that the mounting did not had to be extremely precise. The solder could only wet to the metal surfaces on the substrate, and as long as the chip and bump were in contact with the correct pad on the surface, the chip self-aligned. Trials with silicon chips showed that the chip could be dislocated as much as 50% of the pad diameter and still resulted in good alignment.

Jiang et al. (2004) developed indium bump fabrication based on both evaporation and electroplating method. Their indium evaporation method was based on a unique positive lithography process and achieved high resolutions whereas electroplating method produced acceptably uniform indium bumps suitable for infrared (IR) focal plane arrays (FPAs) applications. The electroplating method could also be extended to produce high aspect ratio indium bumps or even variable height and diameter indium bumps by a new ‘‘multi-stack’’ technique. The fabrication of multi-color IR FPAs could potentially benefit greatly from this ‘‘multi-stack’’ method. They also proposed an indium bump transfer technique that simplified bump fabrication at a reduced cost. However, Olver (2004) pointed that these indium bumps could damage the devices due to the compression required for assembly. Moreover, they could not be reworked easily.

2.2 Studies cognate to stud bumping

Zhong (2001a) evaluated the stud bump bonding (SBB) process for a flip chip in package application. An SBB packaging process, having a reduced number of process steps compared with the typical SBB process, was proposed. The two separate steps of curing of conductive adhesive and underfill epoxy, which for the application targeted in this study needed a total of four hours for curing plus further time for cooling, were not required. It was claimed that the proposed process resulted in a reduced packaging time.

Chaudhuri et al. (2006) mentioned, copper stud bumping using a high-speed automatic wire bonder with the addition of a kit to enable copper ball formation in a protective atmosphere, had the potential to significantly lower the cost of ownership for the flip-chip process. For low- to medium-I/O devices such as or double-data-rate three synchronous dynamic random access memory (DDR3 SDRAM), automotive applications, and sensors, copper stud bumping was significantly less expensive than conventional sputter/print solder paste or electroless plating methods. Incorporating wire bond technology, as a part of the flip-chip bumping process was attractive because existing facilities and infrastructures could be used without the high capital costs required by more expensive sputter/plating facilities.

Osborne et al. (2005) reviewed stud bumping technology and its application along with various bumping material options. It was based on wire bonding technology, using Au and Cu wires. They claimed that cost effectiveness of stud bumping could provide an alternate solution for slim form factor packaging (stacked die, image sensors and LCDs) and for other packaging applications requiring high reliability with high current carrying capability and high use temperature. They found that wire type selection (chemistry,

elongation) could affect bump shape and strength. More ductile wire increased tail height variation and decreased coplanarity. Commercially available flip chip attachment was considered suitable for assembly with either gold or copper stud bumps.

2.3 Investigations linked to assembly process

Zakel et al (2003) found that the majority of contemporary flip chip bonders were derived from modified surface mount devices (SMD) – equipment respectively from modified die bonder equipment. The majority of the flip chip assembly processes were based on soldering, however adhesive attach was having a stronger and more important impact in flip chip technology. Adhesive attach was especially interesting in applications on flexible circuits, like LCD drivers and smart cards. The methods of flip attach were all using thermal energy by either reflow convection ovens or a thermal based on heated tools (thermode). They showed a new approach of using laser for a selective attach of Flip chip and surface mount technology (SMT) – type of components. The advantage of laser instead of direct thermal heating was given by extreme high selectivity and by using a localized heat with an extremely good time control in the millisecond range. This minimized the thermal stress induced in the package, and on the substrate minimized allowing implementation of new substrates and new IC's, which were thermally more sensitive. Their paper showed applications of laser flip chip Attach for soldering and for adhesive curing of underfill material, ACF and NCF or NCP – materials. The laser soldering allowed processing of a high variety of solder alloys including eutectic tin lead, lead free SnAgCu and SnAg together with AuSn.

Jung et al. (1995) realized flip chip interconnections to organic substrates using different techniques: soldering using mechanical solder ball bumps and adhesive bonding

with isotropic conductive adhesive. Both approaches used an electrolessly deposited nickel gold under bump metallization. While soldering with PbSn solder, restrictions came from the necessary temperature for the reflow process and the requirement of flux. Using alloys with lower melting temperature resulted in higher material costs. Adhesive bonding offered lower process temperatures and was inherently flux less. However, no self-alignment effect was present; precise bonding equipment was needed. Except for the bonding with nonconductive adhesive films, the measured contact resistances were larger than for the soldered ones. Concerns about the environmental impact of lead in the solder did not affect the adhesive. By adjusting the gap distance between chip and substrate, they expected to achieve as reliable interconnections as with soldered ones, because mainly the properties of the underfill determine the performance when subjected to thermal cycling. Failure analysis of the under filled assemblies showed that a fracture along the interface between chip and undefiller occurred. Thus the bumps were separated from the chip, resulting in a complete loss of conductivity. While the under filled assemblies using the mechanical bumps withstood more than 1000 thermal cycles (chip size 7.5 x7.5 mm^2, test conditions $-55^0C/+125^0C$,) without significant increase in contact resistance; the under filled devices with electroplated bumps showed first defects after 750 thermal whereas non-under filled chips showed failure after 10 thermal cycles

Cheah et al. (2001) developed a thermosonic flip chip bonding process using conventional equipment. These were: (i) Gold wire bonder to form pull-off bump on silicon die with gold wire bondable aluminum pads, (ii) Thick or thin film ceramic substrate, (iii) Conventional flip-chip bonder with optional ultrasonic tool to provide alignment, heated stage, thermo-compression loading, ultrasonic power and controllable

duration to perform the flip-chip thermosonic flip-chip assembly, and (iv) Conventional dispensing system for underfilling dispensing. The thermosonic flip-chip bonding process was proven to be useful for die with dimension up to 5 x 5 mm and up to 68 input-outputs (I/Os). The following steps were taken to verify the reliability of the process: (i) Die shear test was performed to meet the specified criteria of military standard (MIL-STD-883) with 5 g/bump. (ii) Cross-section of the die to ascertain gold-to-gold diffusion interface. (iii) Thermal cycle and pressure cooker tests to verify the bonding.

Ishii and Aoyama (2004) directly bonded bare flip chip to the substrate. Successful connections were achieved by using a 0.05Au-0.95Sn solder bump and a hydrogen-plasma reflow technique. Because the method eliminated the need for any process on the chip wafer, it was very useful in fabricating flip-chip connections for low-cost packaging. The pre-reflow bonded assembly was inserted into the hydrogen-plasma chamber and exposed to the plasma for 2 min at 220°C. After the plasma treatment, the connection between the chip and substrate was examined. Failure observed in SEM view of bump cross section. SiO_2 separation film formed on the Au-Sn interface.

Tuetsu et al. (2005) found that short-pulsed laser generated localized heat and induced minimal thermal stress on the area beyond the joined surfaces, on the chip and substrate, and the interconnections that join them. The exact amount of thermal energy required could be provided in one short-duration laser pulse, in the areas of interest. It was not necessary to heat an entire substrate up to reflow temperatures to melt and reflow an interconnection of a few microns. Additionally, that same ability could be applied to the rapid thermal curing of materials, such as underfill, commonly associated with flip chip assembly. However, Kordas et al. (2006) mentioned difficulties arouse with the laser

soldering process when flip-chips or other tile-type components were mounted, since the joints formed were between the component and the PCB. In such cases, the laser beam had to be applied from the side (parallel to the PCB) or either through the component or through the PCB (both perpendicular to the PCB). Due to simple optical reasons, the first option (illumination from the side) enabled soldering along the perimeter of the component. Considering a numerical aperture of 0.1 mm for the focusing optics (which was already a rather small value) and a typical flip chip and PCB distance of 100 μm, maximum soldering distance from the side of the chip was ~1 mm. Therefore, in the case of large chips/ arrays, the inner joints could not be realized. The second alternative for laser soldering—with a beam through the component— was dismissed due to scattering of the beam on the metal patterns of the chip and due to the high risk of a possible component failure caused by the high-intensity laser beam. Since the only feasibility criterion for illumination through the PCB is high transparency of PCB dielectrics at the wavelength of the laser beam, the third option appears to be the obvious one.

Jokinen and Ristolainen (2002) made flip chip interconnections on very flexible polyethylene naphthalate substrates using anisotropic conductive film. Two kinds of chips were used: chips of normal thickness and thin chips. The thin chips were very thin, only 50 μm thick. Due to the thinness of the chips they were flexible and the entire joint was bendable. The reliability properties of the interconnections established with these two different kinds of chips were compared. In addition, the effect of bending of the chip and joint area on the joint reliability was studied. Furthermore, part of the substrates was dried before bonding and the effect of that on the joint performance was investigated. The pitch of the test vehicles was 250 lm and the chips had 25 μm high gold bumps. For

resistance analysis there were two four-point measuring positions in each test vehicle. For finding the optimal bonding conditions for the test vehicles, the bonding was done using two different bonding pressures, of which the better one was chosen for the final tests. Furthermore, the test vehicles were subjected to thermal cycling tests between -40 and +25 ^{0}C (half-an-hour cycle) and to a humidity test (85%/85 ^{0}C). Part of the test vehicles was bent during the tests. Finally, the structures of the joints were studied using scanning electron microscopy.

Rasul and Olson (2005) developed an unbumped flip chip on paper assembly technology using ACA that reduced processing steps by eliminating screen-printing for the wafer bumping. Combined with elimination of thermal curing, the process enabled high throughput and lower overall cost.

2.4 Findings connected to joint characterization

Nicewarner (1999) compared several flip-chip interconnection methods by measuring interconnect resistance before and after exposure to environments including pre-conditioning, 85^{0}C/85% RH exposure, 150^{0}C storage, and 0±100^{0}C temperature cycling. It was seen that solder bumps over electroless nickel had lower bond pad resistance than electroplated solder over Cr/Cr-Cu/Cu UBM and the performance was as well or better when exposed to temperature cycling, high temperature storage, or humidity. Silver filled epoxy adhesive did not achieve consistent low resistance connections when assembled and failed to survive humidity exposure. Gold stud bumps with thermoplastic adhesive exhibited a significant increase in resistance over temperature due to a high thermal expansion coefficient. Gold stud bumps with thermoset adhesive had electrical and environmental test behavior similar to solder. Aluminum bond pads showed a small

increase in resistance due to environmental exposure while electroless nickel-plated pads remained stable.

Wang et al. (2006) applied carbon nano tubes in integrated circuit packaging, as the bump interconnection for flip chip, due to their special electrical, mechanical and thermal properties, which might promote both the performance and reliability of the flip chip packaging. Moreover, carbon nano tubes could be formed according to a precisely predefined small-scale pattern, which made extremely high-density interconnection possible. Vertically aligned carbon nano tubes were grown on silicon in the form of square arrays of different sizes, heights and pitches. Attempts to use thermal compression and anisotropic conductive adhesive to bond chips carrying carbon nano tube bumps with ceramic substrates were also executed. Mechanical testing was performed afterward to determine the strength of the bonding interfaces. The strength of the bonding by thermal compression was very weak, in the range from 1.9 to 7.0 g/mm^2. The bonding by anisotropic conductive adhesive was much stronger, indicating a possible approach to bond chips carrying carbon nano tube bumps.

Koo et al. (2008) investigated the effect of displacement rate and intermetallic compound growth on the shear properties of the electroplated Sn–37Pb (wt.%) flip-chip solder bumps with Cu UBM after multiple reflows. The compounds Cu6Sn5 and Cu3Sn were formed at the interface after one reflow, and their thick nesses increased with increasing reflow number up to 10. The shear properties peaked after four reflows, and then decreased with increasing reflow number. Increasing displacement rate increased the shear force, but decreased the displacement until fracture. The tendency toward the brittle

fracture characteristics was intensified with increasing displacement rate and reflows number.

Zhong (2001b) evaluated flip chip on flame retardant (FR-4) and ceramic substrates using gold bumps with ACF, ACP or NCA. Flip chips were assembled on test vehicles for temperature cycling and humidity tests. The reliability performance of the process was compared. It was seen that adhesives could give satisfactory reliability when bonding parameters were optimized.

Using laser ultrasonic system, Erdahl et al. (2008) measured the free vibration response of the chips attached to the printed circuit board. The algorithm of mode isolation (AMI) was applied to the vibration response data in order to extract the modal parameters of the chip. They estimated the first natural frequency to be about 101 kHz. They were able to identify the presence of open solder bumps between a flip chip and the circuit board. The most basic approach of monitoring the natural frequency and damping ratio was not definitive in detecting open solder joints because the natural frequencies of the chips with open solder joints were too similar to those for chips without open solder joints relative to experimental scatter. On the other hand, the first mode shape was seen to be significantly different between the reference and damaged chips, so that one could discern many of the damaged chips by comparing the first mode shape of each with the average reference shape. The variation in the shape of a higher frequency mode was also studied, revealing that this mode was not sensitive to damage relative to experimental scatter. The observation that a higher frequency mode was less sensitive to open joints than the first mode indicated that the stiffness of the solder joints became negligible relative to the stiffness of the chips at higher frequency.

Lau et al. (1996) determined the mechanical and vibration responses of 225-pin, 324-pin and 396-pin plastic ball grid array (PBGA) solder joints. Bending and twisting experiments determined the effects of overload environmental stress factors on the mechanical responses of the solder joints. The effects of shipping and functional environmental stress factors on the vibration responses of the solder joints were determined by out-of-plane vibration experiments and a mathematical analysis. They found that natural frequencies were ranging from 95 Hz to 105 Hz and the average measured value of these four measurements is about 100 Hz. These values were very close to those predicted by the simple analytical model.

Zhou and Dasgupta (2006) studied flip chip joints for both Sn3.9Ag0.6Cu (SAC) and Sn37Pb (SnPb) assemblies, under vibration loading. The natural frequencies and mode shapes were extracted from the FEA modal analysis and compared with experimental results. The dominant modes from experiment and simulation were compared. The first fundamental natural frequency both from experiment and FEA was found to be 72 Hz. By matching the fundamental natural frequency from simulation, the boundary stiffness for the rotational spring was calibrated to be 9N-m/Rad. Using this rotational spring constant, the simulation results for the remaining mode shapes and natural frequencies were found to agree well with experiment results. The natural frequency of the second dominant mode is 411Hz from experiment and 415Hz from simulation. Simulation and experiment provide the same mode shape for these modes.

Basaran et al. (2002) presented a test program that was performed to study inelastic behavior of solder joints of ball grid array (BGA) packages. The test data showed that solder joints responded elastically at room temperature under either shock or sine

vibration loading. Inelastic deformation might be still accumulating, albeit very slowly. At elevated temperature, both shock and vibration induced significant inelastic shear deformation in solder joints, thus shortening the fatigue life of solder joints. The solder joints suffered more severe damage at lower vibration frequencies than at higher ones. At 100°C, the test data showed that dynamic loading with frequencies higher than 1,000 Hz had little effect on the solder inelastic response. They found that solders behaved elastically for higher frequencies and inelastically for lower frequencies. At lower frequencies the period of the loading was higher. The time-dependent inelastic deformations were directly related to the period of the load. When the load had a longer period, the material had more time to creep. Consequently for vibrations with small frequencies, creep dominated the response. It was concluded that contrary to popular belief, the solder alloy did not remain in the elastic region regardless of the frequency of loading and the acceleration level. With a low melting point (183°C) and high visco-plastic characteristics, an eutectic solder alloy showed creep behavior during dynamic loading processes, which could not be underestimated in solder joint fatigue life prediction.

Basaran and Chandaroy (1998) studied low and high cycle fatigue behavior of a solder joint between a leadless ceramic chip carrier and a printed wiring board. It was observed that damage experienced due to vibrations could be significant. When the material was in the elastic range, the higher frequency led to higher damage in each cycle. But when the solder behavior was inelastic, lower frequency vibrations caused higher damage in each cycle than in higher frequency loads. Vibrations could lead to

quick accumulation of fatigue damage. This was due to a high repetition of the vibration cycles in each thermal cycle.

Zhou et al (2009) examined interconnect durability of SAC305 electronic assemblies under harmonic and random vibration test loads and compared to that of Sn37Pb assemblies. Under constant-amplitude harmonic loading, a comparison was drawn between SAC305 and Sn37Pb assemblies when similar specimens were excited at their natural frequency. The natural frequency of the test printed wire board (PWB) was identified by measuring its dynamic response to "white noise" excitation, with an accelerometer located at the center of the PWB. The fast Fourier transform (FFT) of the measured accelerometer response indicated that the first natural frequency of the PWB was168 Hz. Isothermal vibration durability generally decreased as the temperature increases, for both Sn37Pb and SAC305 assemblies. Increasing the duration of pre-aging at a constant elevated temperature decreased the time to failure (TTF) for both Sn37Pb and SAC305 assemblies when they were exposed to vibration durability testing. The influence appeared to be more severe for Sn37Pb than for SAC305. There were at least two competing failure sites: one in the bulk of the solder material in the join, and another in the copper trace/pad on the PWB below the solder joint. The SAC305 assemblies were found to be generally less durable than the Sn37Pb assemblies at the load levels examined in this study, but there appeared to be crossover amplitude beyond which the SAC305 assemblies might be more durable.

Ratchev et al (2003) studied the reliability and failure modes of eutectic Sn-Ag-Cu solder joints and compared to eutectic Sn-Pb-Ag ones. There occurred two different failure modes: brittle fracture and fatigue. The results showed that with a Ni/Au surface

finish the reliability of Sn-Ag-Cu solder was much better than the one of Sn- Pb-Ag solder. First of all, when the joint was deformed at high strain, the chance of brittle fracture at the NiAu interface was significantly reduced when using Sn-Ag-Cu solder. The reason was a reduced formation of the brittle $(AuNi)Sn_4$ intermetallic at the UBM interface, responsible for the brittle fracture mode. Second, after deformation at low strain, both solders failed due to solder fatigue, but the Sn-Ag-Cu showed a better lifetime. This better reliability of the Sn-Ag-Cu solder was attributed to a new solder fatigue mechanism: the crack propagates through the bulk of the solder in a web-fashion way, linking the Au containing particles, formed in the volume. This was beneficial for the joint reliability as it hindered the crack propagation.

Kadioglu and Adams (2008) showed that ductile adhesives had potential uses in structural applications, and such adhesives might have some advantages over traditional structural adhesives especially for some applications where considerably high stress concentrations were to be found. The mechanical properties of the structural bonding tape (SBT) showed low maximum stress but high strain to failure, which implied the ability to tolerate the stress concentrations and so to contribute to the joint strength, and to show high damping performance in structures. Such materials could be of potential use for the matrix of fiber-reinforced composites.

Chiang et al. (2008) investigated the mechanical behavior and failure mechanisms of non-conductive adhesive (NCA) joints exposed to accelerated testing environments. Their study revealed that moisture preconditioning induced a rapid and drastic decrease in the mechanical strength and modulus of NCA joints. Recovery experiments indicated that the loss in modulus was reversible upon re-drying, but nonetheless more irreversible

damage did occur at NCA joints due to hydrolysis. A hydrolytic degradation mechanism at the NCA/ polyimide interface was proposed.

Che and Pang (2009) developed vibration fatigue test and analysis methodology for flip chip solder joint fatigue life assessment by performing vibration tests with constant G-level and varying G-level input excitation. The linear cumulative damage analysis method (Miner's rule) predicts non-conservative result for vibration fatigue life of flip chip solder joint. FEA using a global-local-beam modeling method was used to calculate the natural frequency and were compared to experimental data. A quasi-static FEA method was developed to investigate solder joint stress strain behavior for solder joint vibration fatigue life prediction. Harmonic finite element analysis was also carried out to predict solder joint fatigue life. Results from quasi-static analysis and harmonic analysis were compared. Based on Miner's rule and stress amplitude results from FEA results, different assumed cumulative damage index (CDI) factors were investigated in fatigue life prediction. They recommended that a cumulative damage index (CDI) value of 0.5 had to be used for the FCOB solder joint for the vibration tests investigated from 3G to 10 G.

Che et al. (2007) used bump shear to characterize interface strength of Cu/low-k structure using finite element modeling technique. From the parametric study with 3 different low-k structures, different shear ram height, high Pb solder vs. Pb-free solder, different UBM thickness, block layer modulus effect they found that the shear force decreased with shear ram height, and the critical stress decreased with the number of layer of low-k structure. Higher shear force occurred for SnAg solder bump than SnPb

one. They predicted that reducing UBM thickness could help improve the low-k structure reliability.

Sood et al. (2008) performed failure mode mechanism and effect analysis (FMMEA) on passive RFID tags using scanning electron microscopy (SEM), energy dispersive spectroscopy (EDS) and focused ion beam (FIB) etching. Based on results of SEM inspection of cross-sections, they found instances of inadequate physical contact between the silver antenna material and bumps of the die. Chemical de-capsulation of the die from the tag and inspection revealed that certain bumps of die from stressed tags were not attached to the die, this was potentially caused due to poor adhesion of the bump to the die metallization or failure of the materials during processing or accelerated tests. Based on FIB etching, they found fractures in the passivation layer and delamination between semiconductor bump and internal metallization of the die. Recommendations provided to the manufacturer based on these findings led to implementation of several design and assembly process changes, which could resulted in significant improvements in reliability and performance of RFID tags.

Clech (1998) proposed volume correction factor to predict the solder reliability solution in chip scale packaging. The effect of solder volume on solder joint fatigue was validated with ceramic CSP failure data. Hwang (2008) incorporated non-conductive silica fillers into ACFs to control the coefficient of thermal expansion (CTE) of ACF materials. He studied their size effect on cure kinetics and thermo-mechanical properties and investigated the reliability of flip chip assembly. It was seen that in accordance with increasing filler content, curing peak temperature and storage modulus increased. But CTE decreased as the filler content increased. The effect of filler size on composite

properties and assembly reliability showed similar tendency with the filler content effect. The smaller filler size was applied, the better composite properties and reliability were obtained. Conclusively, incorporation of non-conductive fillers, particularly in case of smaller size and higher content, in ACFs improved the material properties significantly, and as a result, flip chip assembly using ACFs was resulted in better reliability.

Choi et al. (2003) studied electromigration of eutectic SnPb flip chip solder joints and their mean-time-to-failure (MTTF) in the temperature range of 100 to 140 °C with current densities of 1.9 to 2.75 x 10^4 A/cm^2. In these joints, the under-bump-metallization (UBM) on the chip side was a multilayer thin film of Al/Ni(V)/Cu, and the metallic bond-pad on the substrate side was a very thick, electroless Ni layer covered with 30 nm of Au. When stressed at the higher current densities, the MTTF was found to decrease much faster than what was expected from the published Black's equation. They found that failure occurred by interfacial void propagation at the cathode side, and was due to current crowding near the contact interface between the solder bump and the thin-film UBM. Besides the interfacial void formation, the intermetallic compounds formed and the Ni(V) film in UBM were found to dissolve completely into the solder bump during electromigration. So the electromigation failure was explained as a combination of the interfacial void formation and the loss of UBM. Eutectic SnAgCu flip chip solder joints also showed similar failures.

Kown and Paik (2004) investigated the mechanism of shrinkage and contraction stress and the relationship between these mechanisms and the thermo-mechanical properties of ACFs. Both thickness shrinkages and modulus changes of four kinds of ACFs with different thermo-mechanical properties were experimentally investigated.

Contraction stresses of ACFs developed along the thickness direction were estimated, found to be significantly developed by the cooling process from the glass-transition temperature to room temperature. The increasing rate of contraction stresses below glass transition temperature (Tg) was strongly dependent on both thermal expansion coefficient (CTE) and elastic modulus (*E*) of ACFs. A linear relationship between the experimental increasing rate and *E* X CTE revealed that the build-up behavior of contraction stress was closely correlated with the ACF material properties: thermal expansion coefficient, glassy modulus, and Tg.

CHAPTER 3

RESEARCH APPROACH

This chapter deals with identifying the problems in existing flip chip joints. It also evaluates some alternative strategies and suggests one to overcome them. The existing joining process could be modified and a new bump bonding technique can be implemented to attain the better reliability of the assembly.

3.1 Problem identification

Although many types of flip chips are available, none of them is a perfect one. Flip chip joints formed by laser beam are limited to special categories (Kordas, 2006); even it is advantageous over other joining methods. However, joining solder bumps with adhesives forms majority of the joints. A high percentage of them fail in couple of months, particularly when exposed to vibration. Although there are differences in findings (Erdahl et al., 2008), many previous researchers (Zhou et al., 2009; Zhou & Dasgupta, 2006; Lau et al. 1996) found natural frequency of flip chip joints were in the hundred hertz range. Since components to which the RFID tags are attached to experience low frequency vibrations in some applications, chip joints fail as they face resonance during oscillation. Adhesives having much lower modulus are used for attaching bumps to the substrate antennas, and thus likely to be responsible for this reduction in natural frequency. Bonding directly by heating and reflowing the solder may damage the chip during bonding.

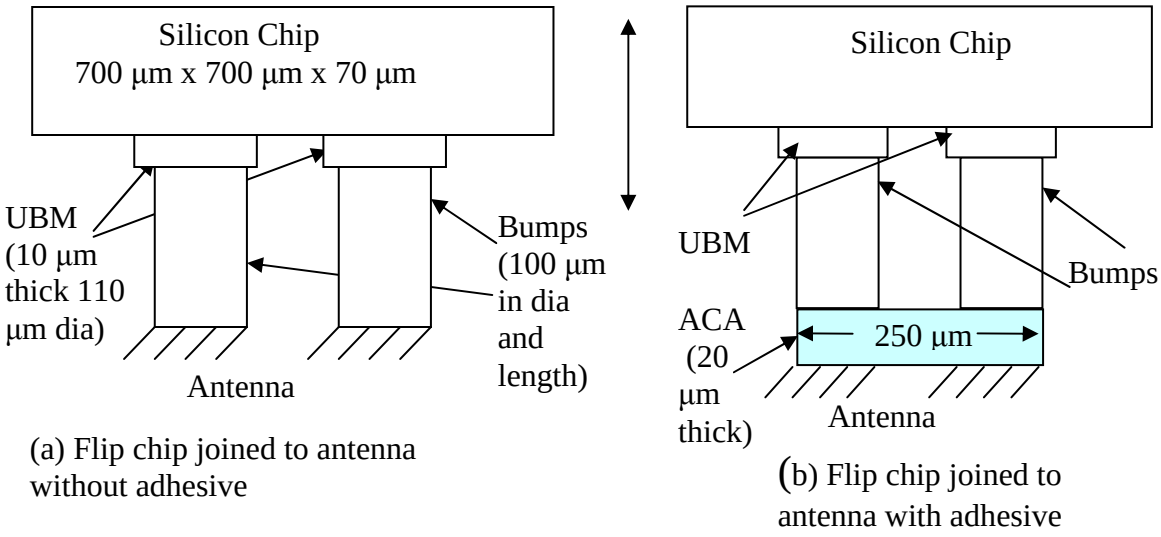
Earlier investigators focused more on joining chip to the bump, but less on its assembly, i.e., attaching to the circuitry. Either of the joints, between chip and bump or between antenna and bump can fail. However, the latter is more vulnerable to failure.

Antenna is attached to substrate; can be considered relatively fixed when subjected to oscillation. It is the flip chip not the antenna moves during vibration. So, the joint with antenna suffers higher stresses. In addition to this, the strength of the bonding agent i.e., adhesive is also much smaller compared to the metallic bond at the other end of the bump (Fig. 2b). It can be pointed that although aluminum is an abundant and cheap material with reasonably good properties, researchers did not show interest on its use as a bump material.

From the above discussions it is clear that failure of the flip chip joints due to vibration is a key issue to explore. The joint between bump and antenna would be given attention. Aluminum bumps can be examined in this study.

3.2 Vibration modeling

Natural frequency of a flip chip joined to antenna with or without anisotropically conductive adhesive (ACA) was studied both analytically, and numerically by finite elements analysis (FEA) using ANSYS 11.0 for out of plane vibration. Since antenna being attached to substrate remains fixed, its mass or stiffness parameter does not come into the estimation of natural frequency of the models. Fig. 16a shows a simplified model of chip joined to antenna without ACA and Fig. 16b shows that with ACA. Component dimensions are mentioned in the figures; drawings are not made to scale. Material properties used and dimensions are mentioned in Tables 1 and 2 respectively.



(a) Flip chip joined to antenna without adhesive

(b) Flip chip joined to antenna with adhesive

Fig. 16: Vibration models

3.2.1 Analytical formulation

Natural frequency of oscillation for both the cases of bumps bonded to the antenna with or without adhesive can be simplified to a single degree of freedom vibration. The equations used for calculations are taken from texts (Ramamurti, 2000; Shabana, 1996) as follows:

$$\omega = \sqrt{\frac{k}{m}} \quad rad/sec; \qquad f = \frac{\omega}{2\pi} \quad Hz: \qquad k = \frac{AE}{L} \quad N/m$$

Without adhesive:

$$k = \left[\frac{1}{k_{bump}} + \frac{1}{k_{ubm}} \right]^{-1} \quad N/m; \qquad m = m_{chip} + 1/\ (m_{bump} + m_{ubm}) \quad kg$$

With adhesive:

$$k = \left[\frac{1}{k_{aca}} + \frac{1}{k_{bump}} + \frac{1}{k_{ubm}} \right]^{-1} \quad N/m; \qquad m = m_{chip} + \frac{1}{3}(m_{aca} + m_{bump} + m_{ubm}) \quad kg$$

3.2.2 FEA modeling

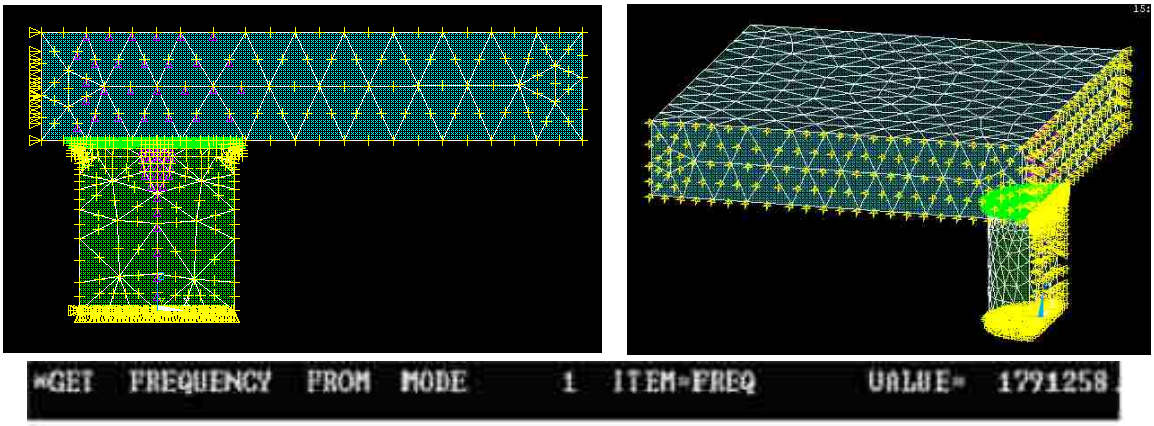


Fig. 17: FEA model of a flip chip joint without adhesive

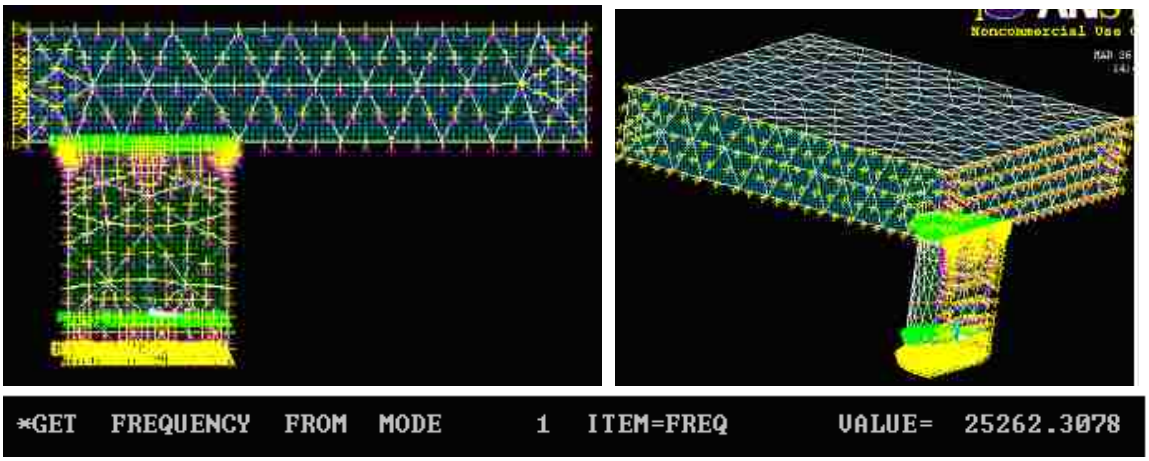


Fig. 18: FEA model of a flip chip joint with adhesive

Finite element models were made with volume creation followed by mesh generation using element type Solid 92, a 10-node 3-degree of freedom (dof) element. One quarter of a flip chip assembly was modeled due to symmetry in geometry. A total of 3197 elements and 5654 nodes were formed for the model without adhesive, and 3337 elements along with 5991 nodes were formed for the model with adhesive. Bottom

surface of the bump (without adhesive, Figure 17) or that of ACA (with adhesive, Figure 18) was fixed for all dof. On the front surface (y = 0), displacement in the y-direction (U_y) was set to zero for all nodes due symmetry. On the left surface of the chip (x = -75), displacement in the x-direction (U_x) was set to zero for all nodes because of symmetry. Nodes at the interface of chip and UBM were coupled for all dof. In case of the model with adhesive, interface nodes of bump and ACA were coupled for all dof. Master dof was selected for nodes mostly above the bump on the top surface of the chip. Non-linear geometry effect did not affect the modal (frequency) solution significantly. Results are shown in Table 3.

Table 1: Material properties used in vibration models

Material	Elastic Modulus (GPa)	Density (kg/ m^3)	Poisson's Ratio
Aluminum	70	2700	0.33
Silicon	131	2300	0.3
ACA	0.00258	1000	0.4

Table 2: Materials and dimensions of components

Component	Material	Geometry	Dimension (μm)
Flip chip	Silicon	Block	700 x 700 x 70
UBM	Aluminum	Cylindrical	110 x 10 (Diameter x Length)
Bump	Aluminum	Cylindrical	100 x 100 (Diameter x Length)
Adhesive	ACP	Cylindrical	100 x 20 (Diameter x Length)

Table 3: Results comparison for natural frequency

Method	Analytical (without adhesive)	FEA (without adhesive)	Analytical (with ACA)	FEA (with ACA)
Frequency (Hz)	1.788 M	1.791 M	25.25 k	25.26 k

From Table 3 it is seen that the natural frequency of a flip chip assembly without adhesive is about 1.79 MHz and that with adhesive is about 25 kHz. Analytical and FEA results are close for each category. These frequency ranges are considerably high enough in the sense that chips usually do not exposed them, so resonance is unlikely to occur. But unfortunately flip chip joints in RFID tags fail. In order to understand the nature of their physical failure and the underlying reasons, it is necessary to examine the actual failure closely. An experimental investigation was carried out in collaboration with Shanghai Maritime University, China.

3.2.3 Vibration experiment

The experiment illustrated in Fig. 19, below, was carried out in an anechoic room in order to reduce interference from background vibrations. A pair of glass panels was used to sandwich a 13.56 MHz passive RFID tag between them, four bolts and nuts were used on each corner of the panel to mount the test apparatus to a sound wave generator; two more bolts and nuts with cushions were used near the center of the glass panels to provide firm contact between the RFID tag and the panels. In the center of the panels, there was a through hole of 12 mm in diameter, which exposed the chip-antenna assembly of the RFID tag to air on both sides of the panels. Sound waves in the frequencies of 0-200 Hz and 10-500 Hz were directly introduced to the test apparatus. A laser sensor was pointed to the RFID chip to pick up vibration amplitudes during the test, and results in time-domain and frequency domain were collected, shown in Fig. 20 (Wang et al., 2011).

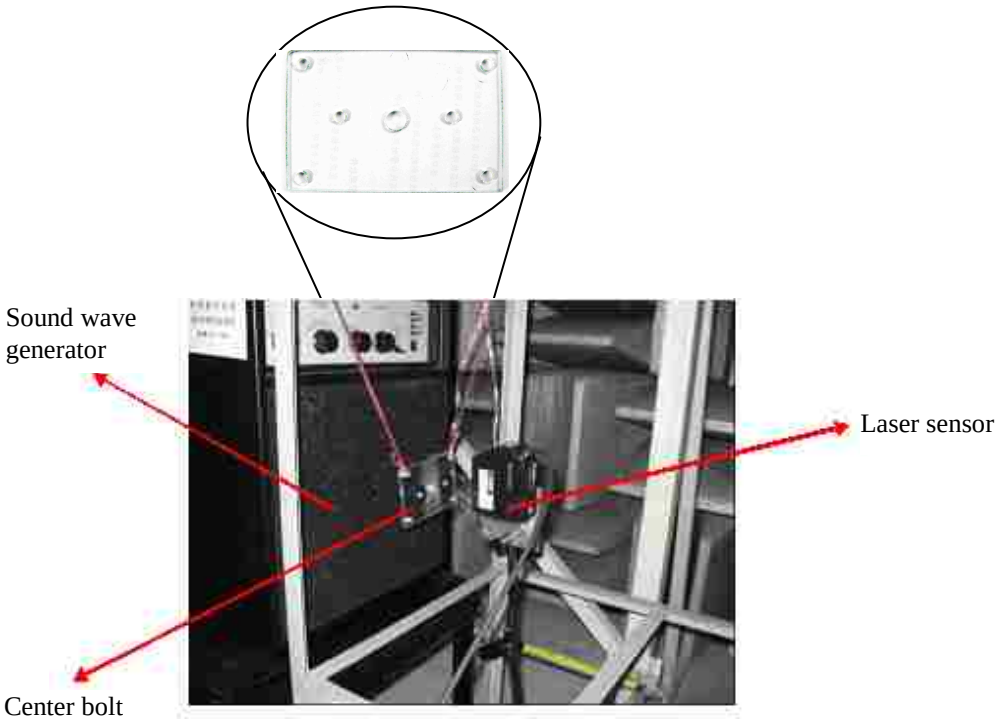
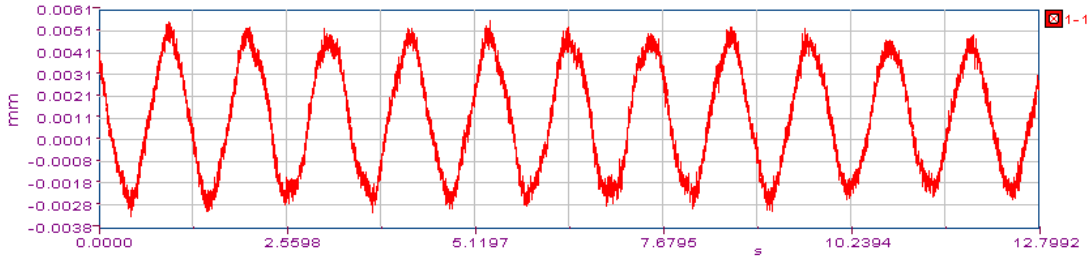
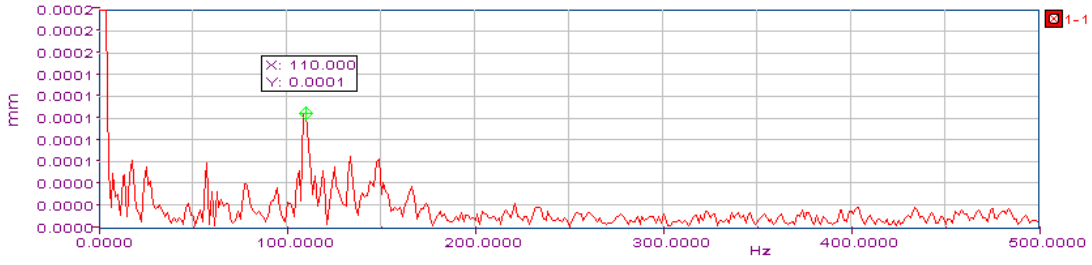


Fig. 19: Vibration experimental set up



(a) Vibration amplitude study

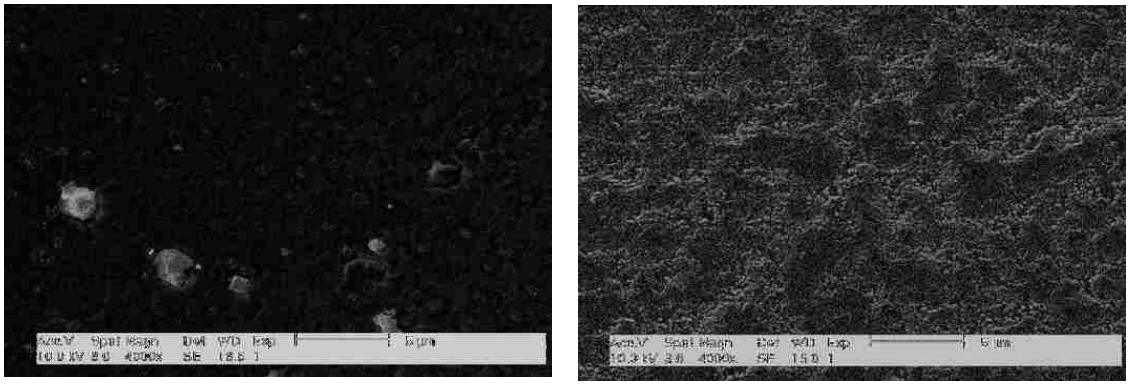


(b) Vibration frequency study

Fig. 20: Vibration analysis of passive RFID tags

3.3 Results interpretation

More tests were conducted, the results of the first fundamental natural frequency was between 108.75 and 110 Hz. The experimental results were more in line with the tests of Zhou et al., (2009), Zhou & Dasgupta, (2006), and Lau et al., (1996) rather than with those of Erdahl et al. (2008). Figure 20b shows that natural frequency of a flip chip bonded to the antenna with ACP is about 110 Hz, although analytical or FEA prediction was about 25 kHz. In order to find out the causes behind the frequency mismatch, SEM picture of an aluminum bump was studied and compared to that of a gold bump at the same magnification (Chiang et al., 2008) shown in Figure 21.

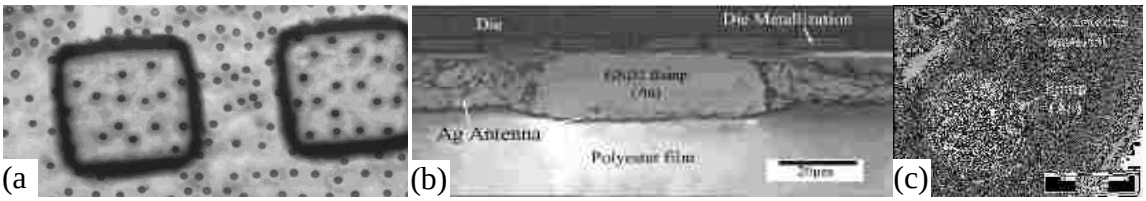


(a) Flip chip bumps with ACF (b) Gold bump surface

Fig. 21: Surface integrity of aluminum and gold bumps

It reveals that aluminum has much less surface roughness compared to gold, therefore, providing less contact area and weaker interlocking force with adhesive surface. A bonding adhesive, i.e., ACP or ACF is epoxy resin mixed with 2-10 μm sized silver or other metallic particles. Figure 22a shows the sizes of two flip chip bumps and multiple silver particles (black dots) trapped under the bumps. Figures 22b and 22c are

SEM pictures (Sood et al., 2008) showing cross sectional views of a bump-antenna assembly in two perpendicular directions. The low values in first fundamental natural frequency in tested RFID tags are likely due to the low bonding strength of ACP and the smooth surface of aluminum bumps, which lead to loosening of those silver particles that are trapped between the bump and the adhesive interface. Predicted models assumed perfect interface bonding.



(a) Aluminum bump surface (b), (c) Cross section of bump-antenna assembly

Fig. 22: Flip chip bump assembly with adhesive

Temperature can also play an important role in reducing RFID tag's natural frequency. Calculations in analytical and FEA models were done using material properties of ACF adhesive 7313 provided by 3M (2004) at room temperature. Increase of temperature in the adhesive layer is not unlikely when flip chips are subjected to vibration, although suspended particles would transfer some portion of the heat generated by the repeated inelastic deformation of epoxy due to oscillation. For better comparison, the natural frequency was calculated analytically corresponding to the changes in temperature. This is presented in Table 4 and Fig. 23.

Table 4: Effect of temperature on ACA modulus and tag frequency

Temperature (^{0} C)	25	37	50	62	75	87	100	112	125
ACA Modulus	2.58E6	1.99E6	1.46E6	1.12E6	7.84E5	2.80E5	1.09E4	1400	840
Frequency (Hz)	25242	22164	18985	16628	13913	8315	1640	558	456

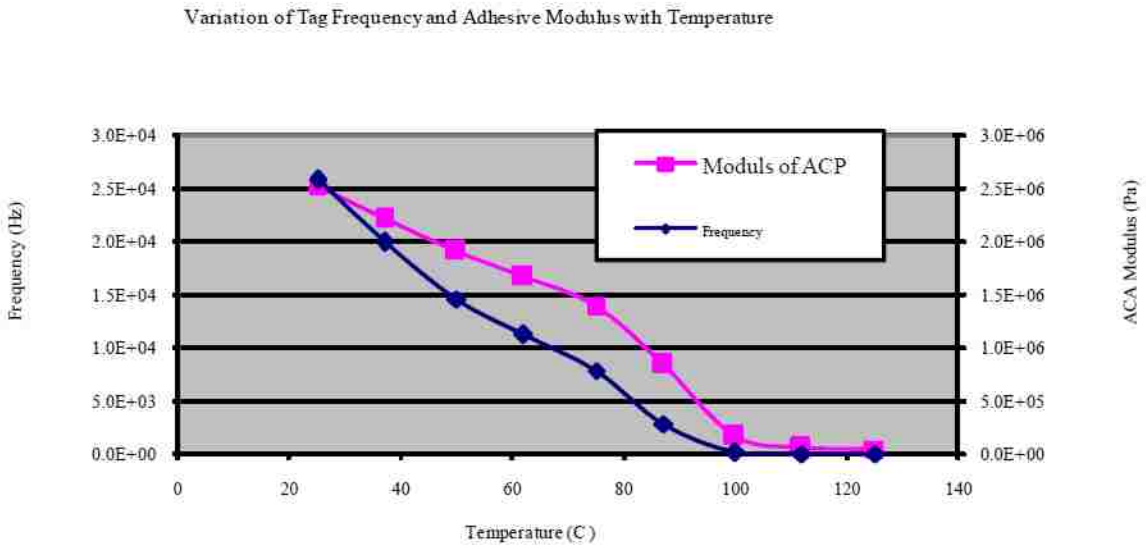


Fig. 23: Effect of temperature on frequency and adhesive modulus

From Table 4 it is seen that for a rise in temperature from 25^{0}C to 100^{0}C, frequency drops from about 25 kHz to 1.6 kHz. This may not completely explain the true reasons for the drop in natural frequency in actual situations. However, it is evident that the combined effect of poor bonding of bumps with adhesive and a rise in temperature play a significant role in the lowering down of the frequency.

From these studies it can be concluded that using aluminum bump is not a better alternative and chip joining with adhesive (ACA) should be avoided to prevent the drop

in natural frequency of the assembly. The next challenge is to devise a joining method without them.

3.4 Alternative joining methods

Although aluminum does not provide strong bonds with other metals or ACA, top layer of UBM i.e., chip pad is aluminum. It is also a preferred material for antenna due to its conducting properties, low density and cost effectiveness. An alternate method calls for metallic joint between the chip pad and antenna. This can be attained either penetrating a bump through the antenna or solidification of liquid bump metal. For both cases antenna has to be drilled. Diamond and carbide dills are commercially available to sizes as small as 30 μm (Figure 24). UKAM Industrial Superhard Tools, Drill Bit City, Atom Precision of America, Inc., and Titex Tools are some of the suppliers.

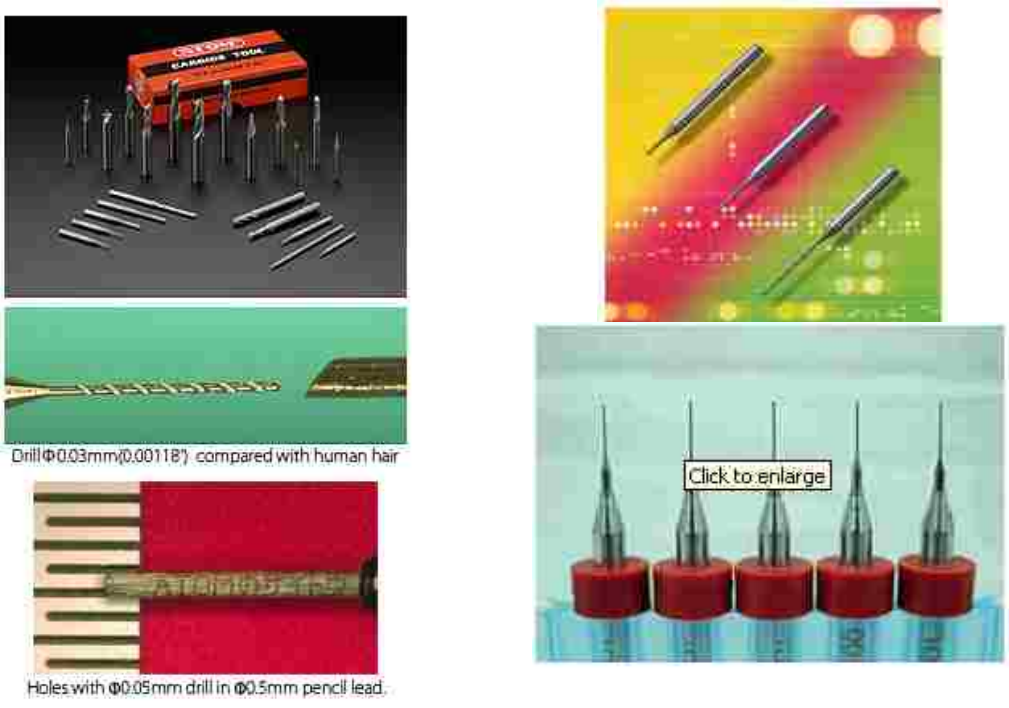


Fig. 24: Some micro drill bits

In the first case traditional lead-tin solder material can be used. The bumps should be long enough to form effective anchor with antenna when bent. In the other case liquid solder material can be inserted from the opposite side through substrate and antenna. Bond would be made by solidification of liquid solder material poured. Bonding can be established with antenna in two ways: (i) connecting the cylindrical outer surface of the bump inserted, (ii) just liquid solidification without bump insertion. In both cases peripheral soldering takes place. However, a suitable solder alloy has to be found that would provide adequate bonding strength with aluminum. The alloy must not have low modulus to prevent lowering of natural frequency as seen for an adhesive.

3.4.1 Long bump bending

This is just like a stapler pin that is penetrated when pressed against paper. The feasibility of long bump bending is considered first. For a long solder bump, the bending effect developed is at maximum at the root (where it is attached) of the bump because of the longest moment arm (Fig. 25). For a typical long bump of 250 μm length and 100 μm diameter, the force necessary to cause bending failure has been calculated from the following equations:

$$M = FL$$

$$\sigma = \frac{Mc}{I} = \frac{FL\frac{d}{2}}{\frac{\pi}{64}d^4} = \frac{32FL}{\pi d^3} = \frac{32x250x10^{-6}}{\pi(100x10^{-6})^3} \approx 2546.473x10^6 F \qquad (1)$$

$$F = \frac{\sigma}{2546.473x10^6}$$

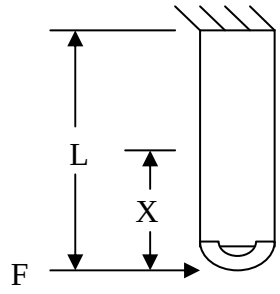


Fig. 25: Sketch of a bump attached to chip pad

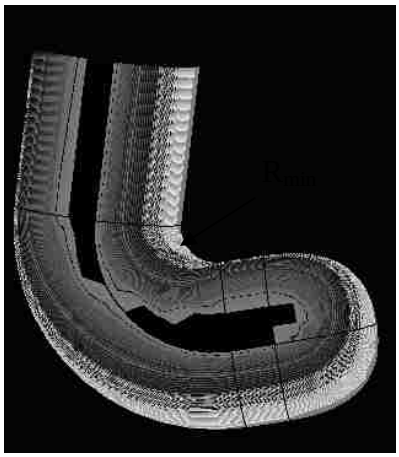


Fig. 26: Long bump bending

This bending stress σ, should be less than ultimate strength to avoid failure. In the limiting case they are equal. So, $\sigma \leq \sigma_u$. For eutectic solder (63Sn37Pb), $\sigma_u \approx 50\ MPa$. Using these values of stresses in equation (1), the force (*F)* required to bending failure becomes about 0.02 N for eutectic solder. Actual force required is less because of the combined effect of bending and shear related by Mohr's circle. Maximum shear stress to cause failure is half of ultimate strength ($\tau_u = \sigma_u/2$).

$$\tau = \frac{F}{A} = \frac{F}{\frac{\pi}{4}d^2} = \frac{4F}{\pi d^2} = \frac{4F}{\pi(10^{-4})^2} = \frac{400F}{\pi} x10^6 = 127.3Fx10^6$$

$$\tau_{\max} = \left(\left(\frac{\sigma}{2}\right)^2 + \tau^2\right)^{1/2} \qquad (2)$$

Making this adjustment and using (2), the forces required to cause failure becomes 0.0195 N. This magnitude is very low.

According to the present estimates, for a 100 micron diameter bump its length should be at least 250 microns. Since 100-unit of this 250 is to be kept straight, going through

the antenna hole, remaining 150 micron takes part in bending. Because of the uniform cylindrical dimension, no stress concentration factor is necessary to calculate the bending stress. Again in order to bend a bump elastically at a distance of 150 microns from the fixed end (100 micron remains inside the antenna) about 10.5 N transverse bending force is required for a eutectic tin-lead bump. This is found with backward substitution of bending stresses in equation (1) using 100 micron as the moment arm.

However, stress developed along both the inner and outer surfaces at the bent zone is much high. Present geometry shows a bend radius of 20 micron (R_{min}) at inner surface (Fig. 26). Thus the stress for elastic bending would be:

$$\sigma = E\frac{r}{R} \tag{3}$$

where, r and R are the radii of the bump and its bent neutral axis, and E is the elastic modulus respectively. With these equation and dimensions, the bending stress is found to be about 10.5 *GP*a. As the bending stress developed is much higher than the material strength, bending is not feasible.

On the other hand from back calculation using σ = 50 *MP*a, E = 15 *GP*a, and r = 50 micron, R is found to be 21000 micron i.e., 21 mm for solder. These are too high to get bent. The above equation (3) can be re-written as: $\frac{r}{R} = \frac{\sigma}{E}$; or $\frac{r}{R_{\min} + r} = \frac{\sigma}{E}$; so, $d = 2r = 2R_{\min}\left(\frac{\sigma}{E - \sigma}\right)$. Thus with the present material properties (taking $\sigma = \sigma_u$) and bend radius, the bump diameter becomes 0.13 micron for solder. This is impractical from manufacturing as well as strength point of view. For a very thin bump like this, a very little force ($F_s = \tau\pi\frac{d^2}{4} \approx 0.34$ μN) would cause shear failure (using $\tau \approx 0.5\sigma_u$).

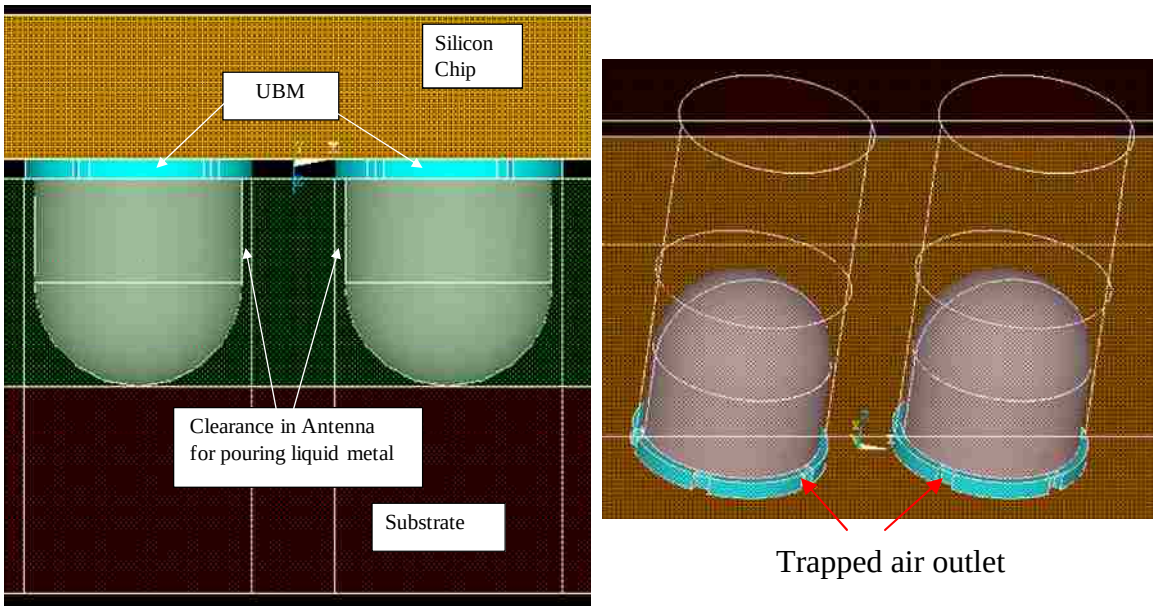
Again for a moderate rise in temperature (about 150^0 C), recrystallization would take place reducing the modulus of solder, but the decrease in strength is more significant. This would expedite the failure of bump due to bending (Jones et.al, 1998). Thus it is found that in addition to the complexity in erecting long bumps; the local stress concentrations at the bent section would cause to fail them; as they experience high curvature. Manufacturing limitations restricts the minimum bent radius (R_{min}); for a typical bump diameter the stress developed becomes much more than the strength of the material. So the attempt was discarded as being not feasible.

3.4.2 Joining by liquid solidification

As already mentioned, junction can be formed with or without the insertion of bumps in the drilled antenna. Bonds are formed on the peripheral surfaces in both cases. They require pouring of a suitable bonding material through the hole drilled through antenna and substrate from the opposite side of the chip.

3.4.2.1 Connecting bumps with antenna

In this case bumps are first erected on the chip pad and then inserted in the holes made through antenna and substrate. Chip pad (UBM) design needs to be modified to remove trapped air that might create voids. This is shown in Fig. 27. Bonding alloy should be poured in upside down position. Close observation reveals that complexities would arise in cutting the slots on UBM because of microscopic dimensions in addition to erecting straight bumps and causing molten metal to flow through very narrow clearance. So, this technique may not qualify as a better alternate and will be rejected.



(a) Regular position

(b) Upside down position

Fig. 27: Inserted bump-antenna assembly

3.4.2.2 Connecting directly by bonding agent

Since the connection between antenna and bump is achieved with the third bonding agent which is S-bond, it is further examined whether joint can be formed with this agent only without bumps. Once liquid bonding agent/ alloy gets solidified it would connect to chip pad and to antenna around the holes, forming peripheral connection. It would be termed as “Peripheral Soldering”. It appears to be feasible from manufacturing point of view, although some relevant demands are to be met. This method is discussed in detail in the following chapter.

CHAPTER 4

CHIP JOINING BY PERIPHERAL SOLDERING

4.1 Fabrication of peripheral joint

A new chip joining strategy that connects chip pad directly to antenna with a suitable bonding alloy (S-bond) as mentioned in Chapter 3 will be further analyzed here to verify its feasibility and reliability. Manufacturing challenges involve drilling micro holes, aligning chip pads with holes drilled, maintaining proper temperature for the liquid S-bond material and squeezing it through the metal stencil printer. For manual assembly, microscopic help is a must. Fig. 28 shows the alignment of chip pad with holes made through antenna and substrate, left pad assembled to antenna in left picture and bottom one assembled in right picture. For better illustration zoomed views of a flip chip connection with S-bond (S-Bond Technologies, 2010) are shown in Fig. 29.

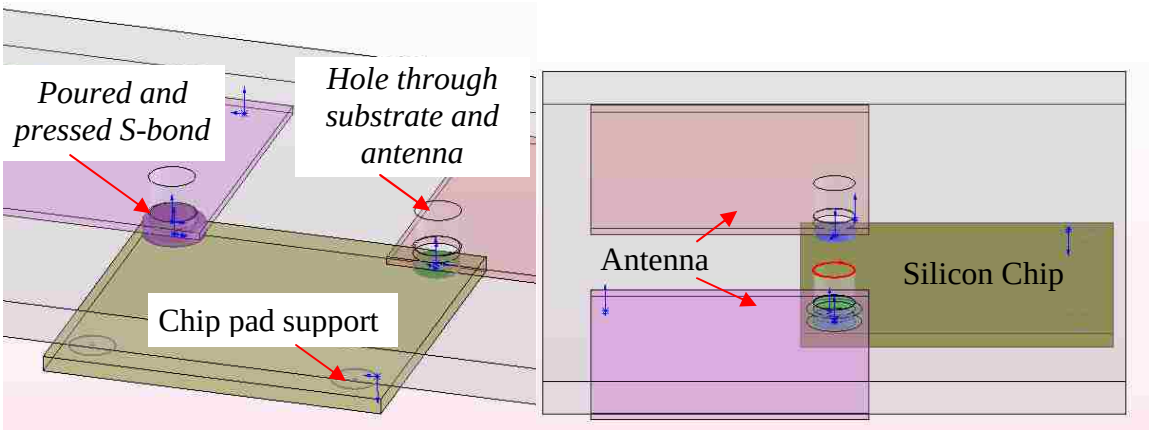
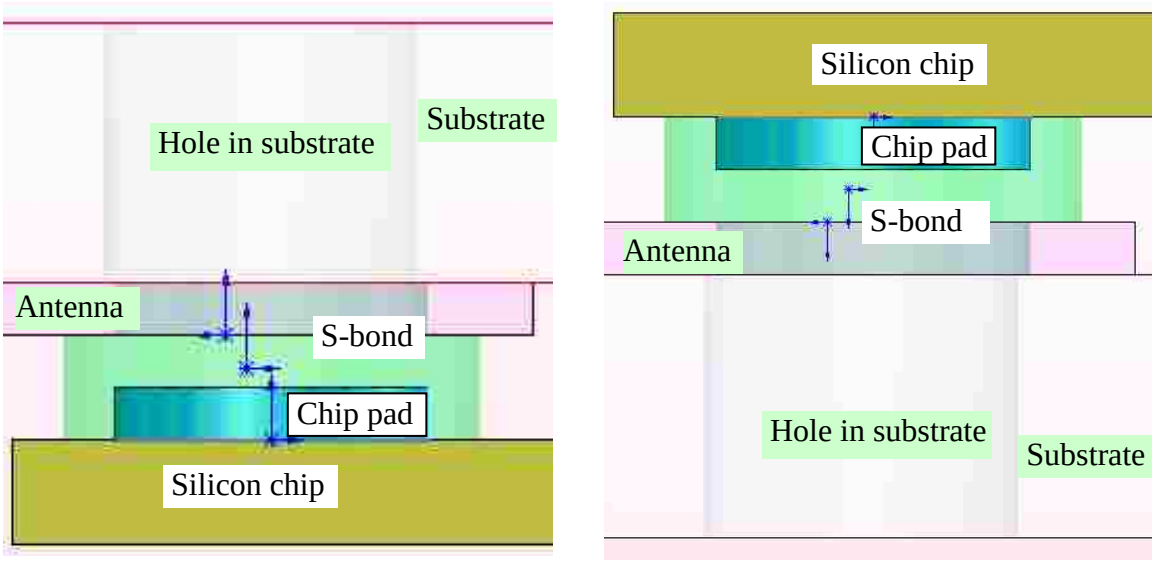


Fig. 28: Tilted views of chip joint with antenna connected to chip pad by S-bond.



(a) Assembly position (b) Regular (chip up) position

Fig. 29: Zoomed views and components of a chip joint

Due to oxide formation on aluminum surfaces, the traditional tin-lead solder does not work well. S- bond 220-50 (a lead free alloy of tin, silver, titanium etc.) is a substitute that works fairly well with aluminum and copper. The antenna (flexible circuit) and substrate together are aligned with chip pad after holes are made through them. Liquid S-bond can be poured on the chip pad through the hole preferably using metal mask stencil printer (Fig. 10, Chapter 1). A little agitation or scrubbing on the pad and antenna drilled surface facilitates joining with S-bond. The PET (polyethylene terephthalate) substrate has a melting point slightly higher (about 265^0 C) than that of S-bond (232^0 C). However, since the recommended bonding temperature is 250^0 C, precautions should be taken to control the temperature to avoid damage in substrate material. Pressing of the antenna against chip pad has to be done quickly to ensure rapid bonding between the pad and antenna, both of aluminum. A little spread out of S-bond around the hole strengthens the bonding between the antenna and S-bond. Due to small thickness of antenna, the bonding

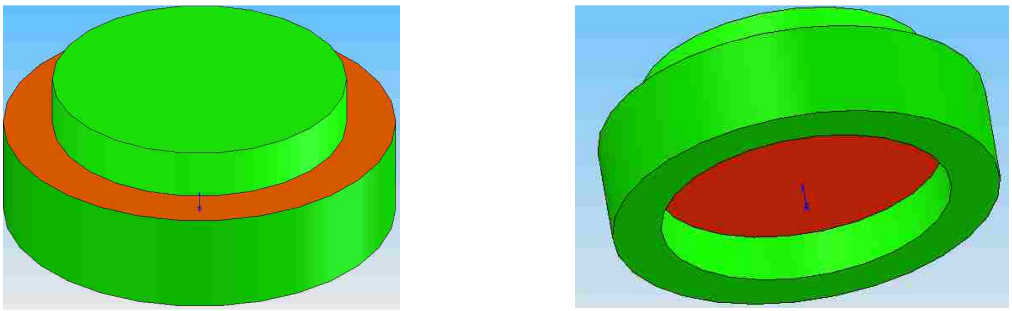
on the annular cylindrical surface may not yield enough bonding strength. The joint with chip pad is established by the S-bond itself. However, the spread out of S-bond around the pad may not provide bonding strength. Thus the junction is formed in two separate faces; with chip pad and S-bond, and with S-bond and antenna.

Since, the drill sizes are small (60 micron typical), dropping S-bond (liquid metal) through an individual hole can cause problem due to the surface tension of the liquid. With manual or semiautomatic printers, S-bond can be placed manually on the stencil/ screen with the print squeegee at one end of the stencil. In automatic printers, S-bond can be dispensed automatically. During the printing process, the print squeegee presses down on the stencil to the extent that the antenna bottom almost touches the top board surface. S-bond is printed on chip pads through the openings in the stencil/ screen when the squeegee traverses the entire image area length etched in the metal mask. After the S-bond has been deposited, the screen peels away or snaps off immediately behind the squeegee and returns to its original position.

4.2 Design of Peripheral Soldering joints

Joining of silicon chips to the substrate antenna would be accomplished by soldering. As it is intended to connect the top layer of the chip pad which is aluminum to the aluminum antenna, micro drills are made through the substrate and antenna to pour soldering material to go through them and come in contact with chip pad. Since aluminum is not readily bondable to traditional solder material (lead-tin), S-bond material should be used. In this case soldering takes place upon solidification of S-bond. Bonding with chip pad and S-bond is possible directly on the mating surface, Fig. 30(b), as the S-bond material is squeezed and pressed through the hole. Depending on the chip size and

antenna thickness the pressure might vary from 2 to 10 psi. Bonding of S-bond with the other component antenna cannot be made directly under the hole. So the joining depends on the spread out of the liquid S-bond material around the hole as the mating components are pressed against each other; thus on peripheral soldering. This spread out depends on manufacturing (hole tolerance, squeezing pace and pressure etc.), it is difficult to estimate its exact size. On the average 10- 20 micron radial spreading can be expected. A 10-micron radial spread out for a 60-micron diameter hole can be considered minimum based on experience. This would render an outer diameter of 80 microns for the S-bond compressed against antenna surface. The bonding surface here is ring shaped with an inner diameter of 60 microns, shown in Fig. 30 (a). Although the shape of a chip pad is almost square, the circular drill does not cause any manufacturing problem. However, this spread out may not provide any bonding strength outside the chip pad i.e., on the bulk chip as there is no metal there. A thin coating of stop-off or high temperature masking on chip can prevent over spreading.



(a) S-bond face joins with antenna (red) (b) S-bond face joins with chip pad (red)

Fig. 30: Faces of S-bond bonding with antenna and chip pad

Chip pads resting on chip supports need not be joined by solder. They can be attached by nonconductive adhesives, the primary purpose of these supports is to provide rigidity, not to complete the electric circuit. Drilling and soldering for them in same way as for the conducting pads will of course add to strength, but may not justify the extra effort.

A chip size of about 1mm x 0.65 mm is common in many applications, but recent trend leads to smaller chips. A pad size of 75 square micron is seen in a typical chip, but 60 square micron in smaller chips. For illustration, enlarged views of silicon chips are shown in Figs. 31 and 32. Manufacturing restrictions require that pads with less spacing (a vertical pair in Figs. 31 and 32) be across the antenna cut out and the other vertical pair is usually used for mechanical support of the chip. Use of underfill material between the chip circuitry and antenna / substrate counterpart provides extra strength and is optional.

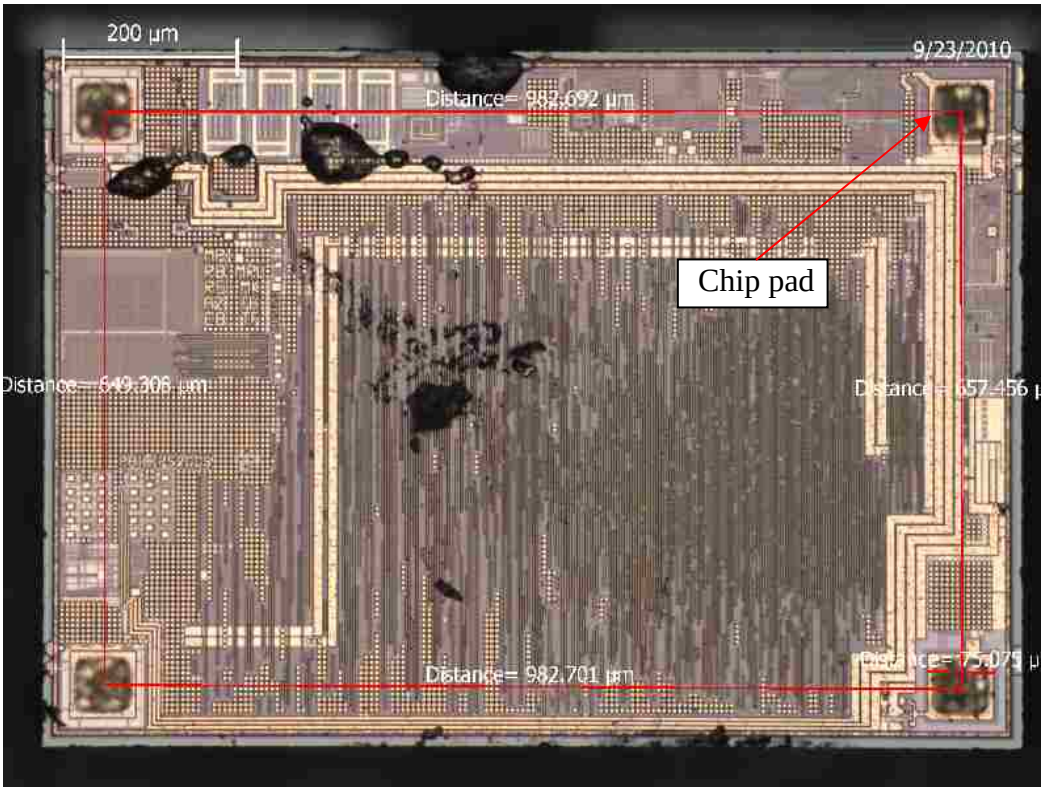


Fig. 31: A large size silicon chip

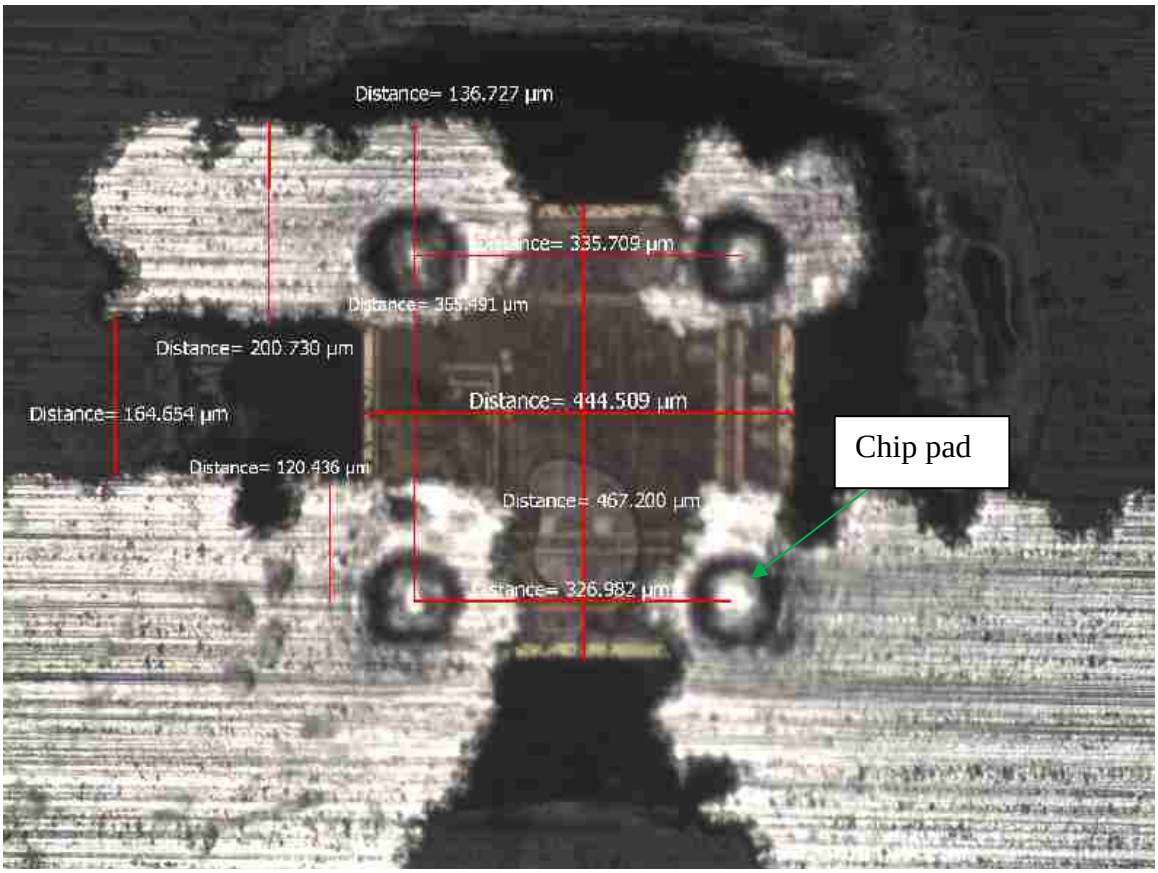


Fig. 32: A small size chip connected to antenna

Although the joining method focused here is manual; it is not limited to that. Auto dispensing of S-bond material through the holes can be performed once they are aligned with stencil printers. Precise control of temperature for avoiding substrate damage would require an additional arrangement, preferably hot air supply which is difficult with soldering gun. Using substrate materials compatible for high temperature like BN300, polyimide, cyanate ester etc. could be an alternative option. Materials should be allowed to cool to 30° C below the joining temperature before removing press-weight or moving components.

4.3 S-bond activation process

The activation process for S-bond products is different from ultrasonic soldering. The oxide layer being broken in S-bond joining is very thin, only on the solder material, requires very little energy to be disrupted, and does not remain as part of the bond. A feature of S-bond products is that they do not flow or wick into openings like conventional solders. Unless pushed, materials stay where they are placed. This is useful for precision joining. S-bond products work with the addition of titanium and/or rare earth elements to conventional solder alloy bases (Electronic Materials, 2006). These active elements migrate to any interface and react with the opposing material surface to remove oxides and nitrides and transport them into the bulk of the solder as an inert material. This process occurs while the material is molten (250^0C), and once the thin "skin" that forms on the surface of the molten solder is broken, it allows contact between the bulk solder and the aluminum or copper surface. The breaking of this skin is referred to as "activation" and is done by application of a low level of mechanical shearing action at the interface between the S-bond material and the contact surface. The level of shear required is small and can be delivered by brushing or scraping the surface, sliding the joining surfaces relative to one another, or application of high frequency vibration to the parts to be joined. Once the skin layer has been disrupted, the bulk solder Sn-Ag-Ti, reacts almost instantaneously and forms a molecular bond, irreversibly with the contact surfaces, creating a tightly held layer of solder on the base metals. The resulting joint may be disassembled and reassembled simply by re-heating above the melting temperature of the S-bond and then re-joining the parts with some additional activation to insure reaction with the new solder. The bonded layer at the substrate surface will not be

affected, so good interfacial bond strength is maintained and re-activation is not required. The other joining mechanism that operates at regular joining temperatures (250°C) is one of adhesion or attraction of surfaces with opposite electronic charges. Since metals such as titanium and stainless steel have very thin 'dielectric' protective oxides such as TiO_2 or Cr_3O_2, they provide an insulator layer that the S-bond active elements and the elements in the base metals attract across.

S-bond processing (Fig. 33) is more like a “gluing” than soldering or brazing. S-bond joining technology first places and spreads S-bond alloys, and then holds them together while bonding is mechanically and thermally activated. S-bond alloys can be applied by many techniques, including: brushing, thermal spraying, friction transfer, ultrasonic bath / dipping, foil / press etc.

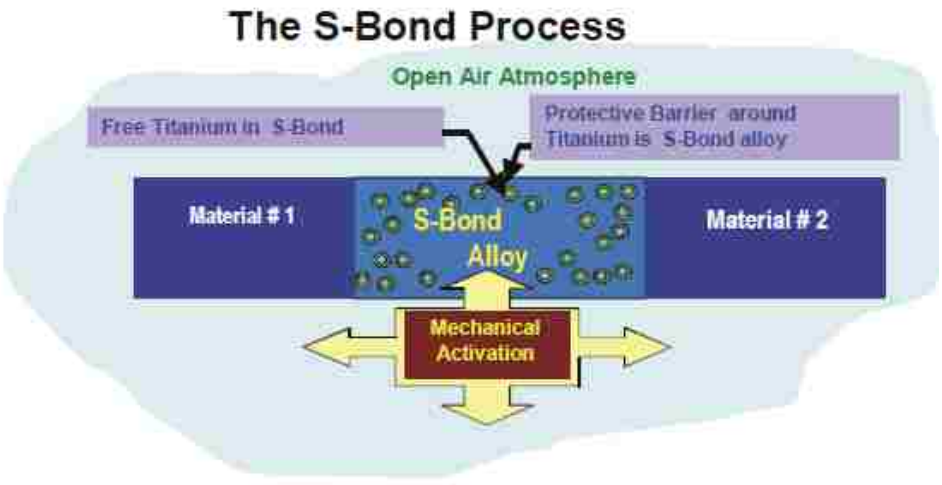


Fig. 33: Illustration of S- bond processing

S-bond joining is fluxless, and requires that in the absence of chemical fluxes the oxides forming on the molten surfaces must be disrupted by mechanical means to enable

wetting and bonding. The mechanical activation at the tips of tools such as brushes, spreaders, vibrapeen tools, or ultrasonic horns and/or soldering irons, are very effective for this.

4.3.1 Vibrapeen wetting

Fig. 34 illustrates the spreading of S-bond alloys by vibrapeen spreaders onto surfaces in preparation for bonding. First, the parts are heated up to 250°C (480°F) +/- 10°C (~20°F). The S-bond alloy is typically applied / melted onto the part surfaces using the wire, foil or pellet forms. Once the alloy is molten it sits as a pool and held by its own surface tension, until mechanically activated using the tip of a spreader, like that of a vibrapeen. Using the spreader edge, the vibrapeen tool is turned to maximum intensity and pressed onto the molten surface of the S-bond alloy pool. Then with a stroking action and firm pressure at the tip of the tool, the molten alloy is spread and brushed over the entire surface to be wetted. It has to be ensured 100% coverage with the tip of the tool since S-bond only wets and adheres to the surface areas that are mechanically disrupted (activated).

Fig. 34: Spreading S-bond with vibrapeen tool

Once the S-bond alloy is completely spread and wetted the sample is ready to be joined to a similarly wetted substrate surface. When the two surfaces are joined, they must be moved to sweep the oxides off the molten. The tip of the vibrapeen tool, for small parts may be an effective tool for this as well.

Micro drilling through the antenna and substrate can be avoided if wetting can be assisted with vibrapeen tool. However, the chip should be positioned on the flipped face onto the correct position of antenna with S-bond spread on both of the surfaces. This would be a difficult task. In this case instead of peripheral, regular soldering would take place. The present title is aimed at joining chip without the aid of extra tools.

4.4 Strength analysis of Peripheral Soldering

The whole purpose of the present joining technique is to improve the bonding strength of the assembly. So it is necessary to investigate how much strength can be provided by the present method. A comparison of strength attained with the traditional ACA (anisotropic conductive adhesive) bonding should also be made. Both analytical and numerical methods will be considered. Since there are holes just above the chip pads, the majority of the bonding strength in the present method is provided by that between S-bond spread out and antenna at one plane (Fig. 30a) and between S-bond and chip pad top at the other plane (Fig. 30b) as mentioned before. The analytical estimate would count the strength offered by the bonding faces between the cylindrical surfaces with S-bond in the hole and around the chip pad. However, the actual strength would be less due to not only on the difficulty of proper wetting on these surfaces, but also on the problem of scrubbing or agitation on curved aluminum surfaces. It is already mentioned that aluminum oxides are removed by the agitation, and the S-bond joint strength is greatly

affected by this. Due to very thin and microscopic scale of dimensions for both the chip pad height and antenna thickness, it is hard to disrupt the cylindrical surfaces unlike the flat surfaces of chip pad top or antenna face. Thus the bonding strength offered by the cylindrical faces will be neglected for analytical calculation. In addition to that the joint strength offered by the bottom face of the S-bond in contact with chip outside chip pad will be neglected; due to lack of metallic contact there, even it is a flat surface. This would compensate strength drop due to fabrication irregularity to some extent.

4.4.1 Analytical strength estimation

With the simplification discussed above, the bonding strengths are offered by the S-bond on two faces (Fig. 30). These faces experience normal tensile stresses for out of plane loading. 53 MPa will be used as the tensile strength of S-bond material and that for ACA will be taken as 20 MPa. Adhesive strength varies a wide range from about 1 MPa to maximum 22 MPa; 20 MPa is close to the maximum end. As both chip pad and antenna material is aluminum, and its strength is much more (>200 MPa) than that of S-bond, minimum contact face area of S-bond (with antenna; Fig. 30a) governs the joint vigor. Thus bonding force offered by the antenna and S-bond interface limits joint strength. This is an annular area with the opening for hole. So force that a S-bond joint can tolerate,

$$F_{S-bond} = \sigma \frac{\pi}{4}(d_o{}^2 - d_i^2) = 53x10^6 x \frac{\pi}{4} x\left(\left(80x10^{-6}\right)^2 - \left(60x10^{-6}\right)^2\right) \approx 0.11655 \text{ N}$$

The total force that a chip can endure is 0.233 N (2 bumps). In comparison, for ACA

$$F_{ACA} = \sigma \frac{\pi}{4} d^2 = 20x10^6 x \frac{\pi}{4} x(60x10^{-6})^2 = 0.05655 \text{ N}$$

Thus, $\frac{F_{S-bond}}{F_{ACA}} = \frac{0.11655}{0.05655} \approx 2.06$

This shows that the new joint is 2.06 times stronger than ACA joint. Here only the normal strengths are compared. Strength in the tangential direction is much higher for S-bond connection; as in this case both shear area and strength are more.

4.4.2 Strength estimation by FEA

Fig. 35 shows the FEA model for S-bond joint using Solid 45 elements in ANSYS 11.0. A quarter of a chip with a pad has been taken for modeling to take the advantage of geometrical symmetry. The size of both antenna-hole and chip-pad is taken as 60-micron in diameter. The outside diameter of S-bond, contacting antenna, is considered as 80 microns. As the antenna is bonded to the substrate, all degrees of freedom for the antenna nodes other than those removed by drill were restrained. In order to avoid any unwanted local damage, the chip was assumed rigid; all nodes on the chip and chip pad interface were coupled for all degrees of freedom. The chip-pad top and S-bond interface nodes were coupled together, for each degree of freedom. Also, nodes of the S-bond and antenna-bottom interface were coupled separately for each degree of freedom.

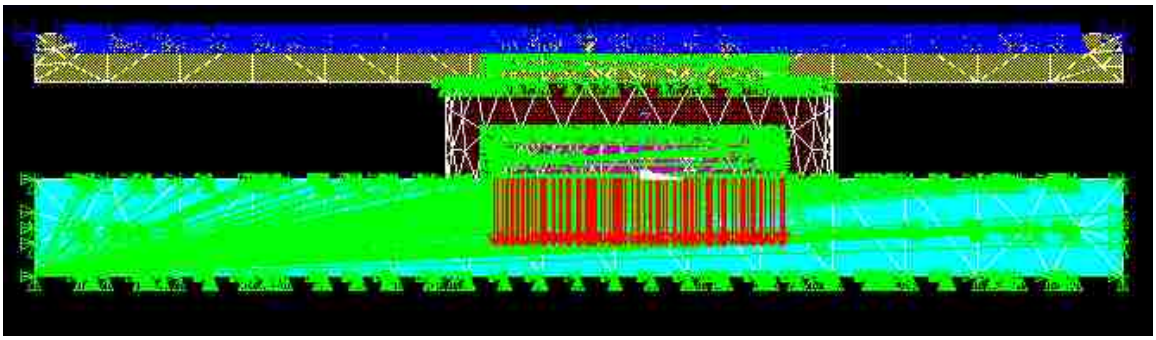


Fig. 35: FEA model of a chip and antenna connection with S-bond

Cylindrical contact surfaces of S- bond are also coupled with antenna, and with chip pad. These were neglected in analytical calculation for simplicity. A vertical downward force of 0.67 milli-Newton has been applied on each of the 172 nodes of chip-pad at the interface with chip (thus making a total of 0.11524 N). The corresponding analytical average stress is about 52.4 (52.403) MPa.

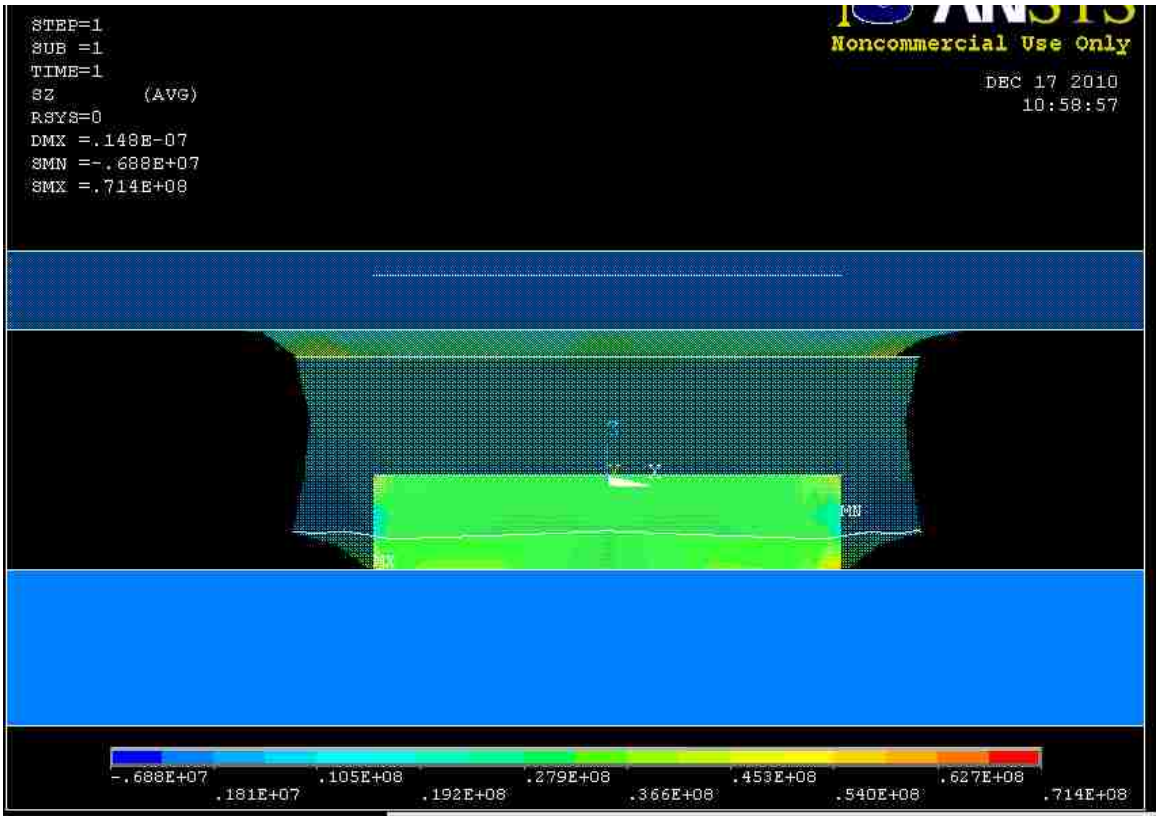


Fig. 36: Stress distribution in a chip connection with S-bond

Fig. 36 shows the stress distribution and maximum stress using ANSYS analysis. However, the FEA shows the maximum stress as about 70 (69.438) MPa in material 2 at node 700, which is on the chip-pad at the interface with chip. This is due to fact that

closed form solution estimates just the average uniform stress without stress risers. Since material 2 is aluminum, this stress level is safe enough. The close observation of the stress listing indicates that node 1376 has the maximum stress (52.951 MPa) in material 3, which is S-bond (Fig. 37). As 53 MPa is the tensile strength of S-bond, the load applied can be fairly considered as the limiting figure.

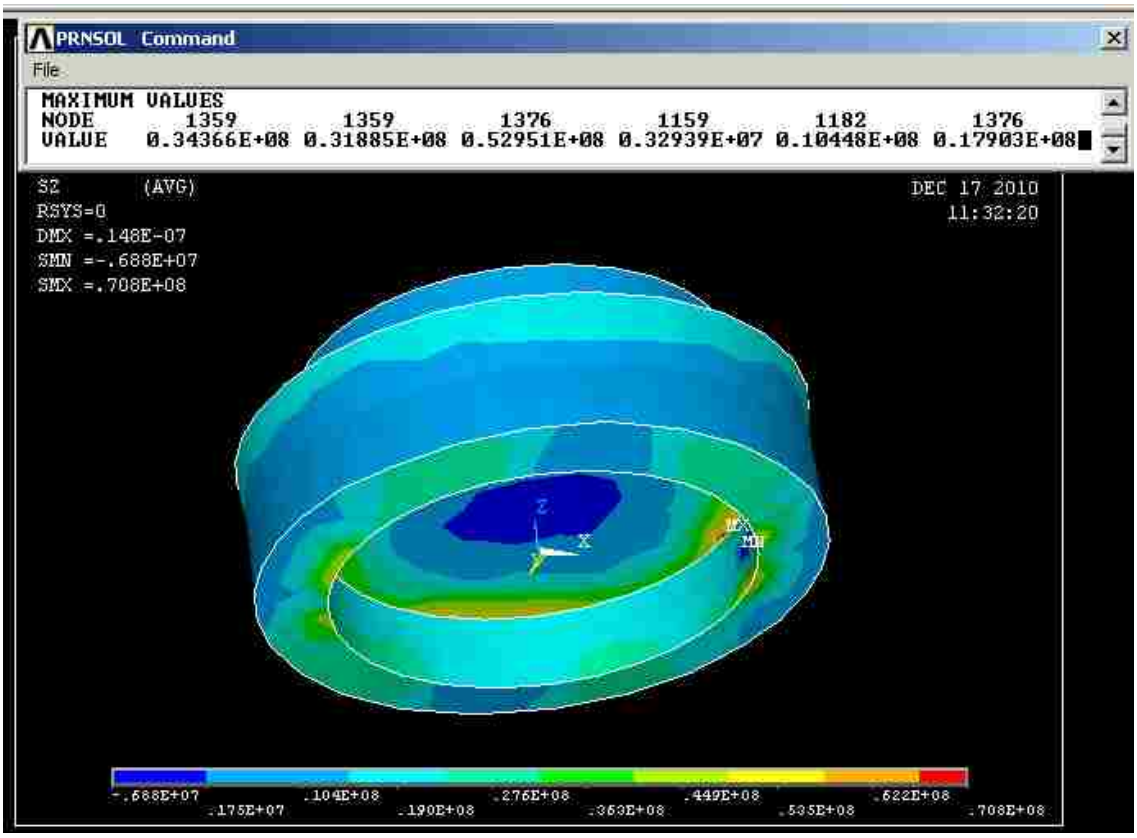


Fig. 37: Stress distribution in S-bond material

This estimates a force capacity of 0.2304 N on the chip. Thus ANSYS determines the joint strength that is about 1% less than that was found analytically.

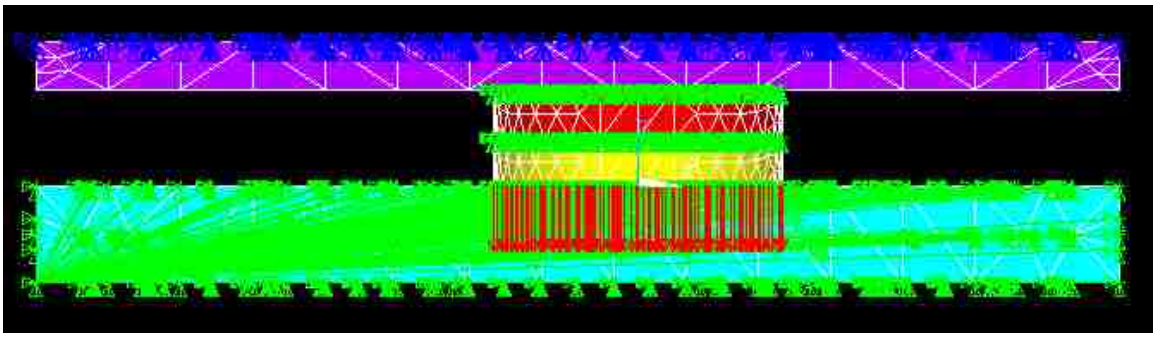


Fig. 38: FEA model for a chip connection with ACA

Fig. 38 shows the chip connection model with ACA. It was modeled in the same way as in the case of S-bond except that here there was no hole. All the nodes of the antenna were kept fixed. Each of the two interfaces of ACA was coupled with three sets for different degrees of freedom.

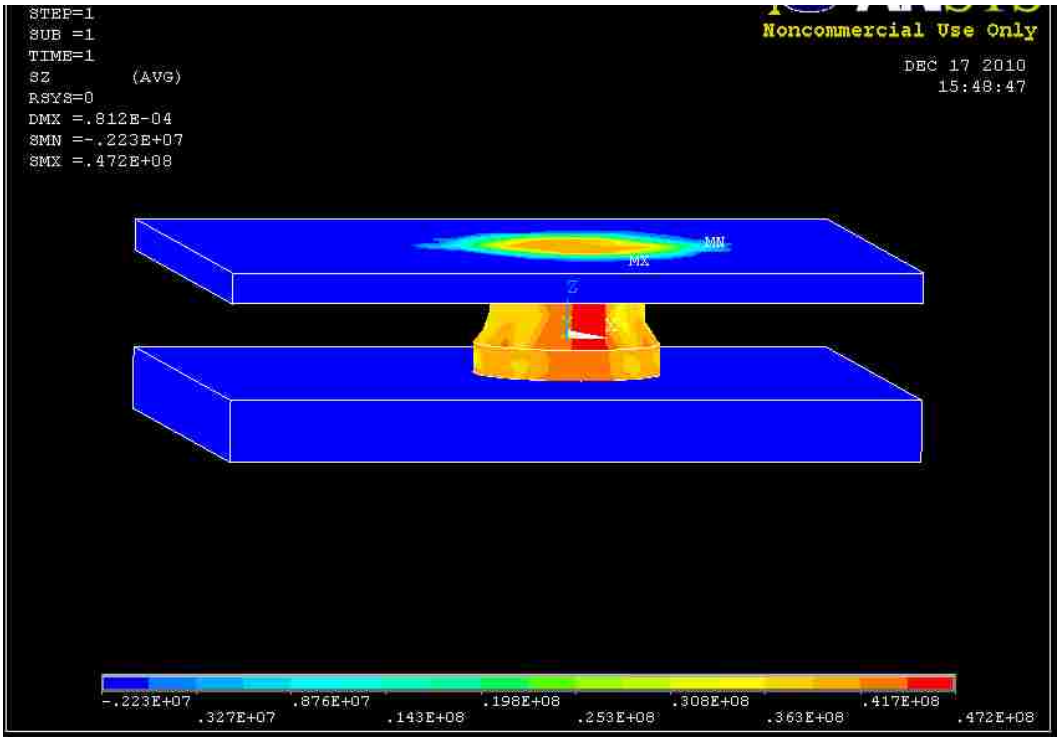


Fig. 39: Stress distribution of an ACA-connected chip for similar loading as in S-bond

Fig. 39 shows the stress distribution and maximum stress in case of ACA joining for the same load as in S-bond. Here the maximum stress (46.051 MPa) is seen to be at node 1201, in ACA (material 3). Although the maximum stress in this case is lower than that for the S-bond, having lower strength (maximum 20 MPa) than S-bond, ACA cannot tolerate this loading.

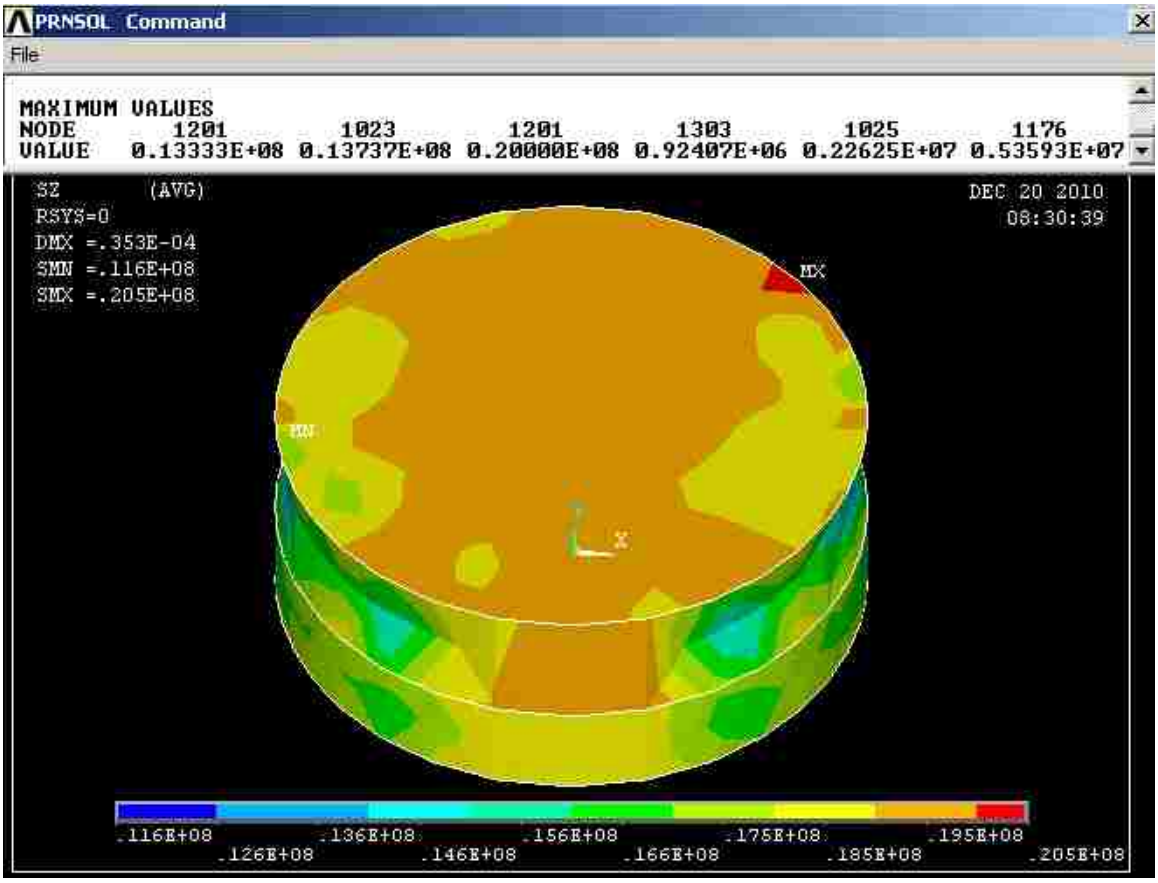


Fig. 40: Stresses in an ACA-connected chip joint with maximum allowable loading

Fig. 40 shows the maximum stress in ACA is 20 MPa that correspond to a load of 0.368 milli - Newton on each of the 136 nodes. This accounts to 0.05 N for a joint, i.e.,

0.1 N on the chip. Thus FEA figures out that the chip joint with S-bond is about 2.3 times(0.23/ 0.1 = 2.3) stronger than that with ACA. The results are shown in Table 5.

Table 5: Bonding strength comparison for a chip connection

Joining Method	Joint Strength (N)		Ratio (%) (FEA/ Analytical)
	Analytical	FEA	
S-bond	0.233	0.230	98.7
ACA	0.113	0.100	88.5
Ratio (S-bond/ ACA)	2.06	2.30	

Table 5 compares the strength of a chip joint by S- bond and ACA both analytically and numerically. FEA strength estimate is about 1% less than that of analytical for joining with S-bond, whereas the corresponding figure is about 11.5% less for ACA joint. Both analytical and FEA estimates show the ratios of S-bond strength to ACA strength are more than 2. Thus it can be concluded that, a chip connection with S-bond is more than twice stronger than that with an ACA.

4.5 Experimental validation

Due to limitations in provision for joining miniature components like a commonly used silicon chip, similar surfaces but in larger dimensions will be manually bonded both with S-bond. Test strengths for S-bond joints will be compared to chips joined by ACA. The effect of size and details of physical experimentation are mentioned in the following chapters.

CHAPTER 5

ANALYSIS OF SIZE EFFECT

This chapter evaluates the effect of chip pad size and gap size i.e., thickness of the bonding material (adhesive or solder) on the strength and reliability of a joint. It primarily discusses the findings of earlier researchers and selects a model that matches best for this research. Although it has some resemblance with Chapter 2, it is being mentioned separately due to its relevance to present work. Because of lack of facilities, tests are to be done with large specimens, as already mentioned in Chapter 4.

5.1 Effect of size on reliability

It has been observed that for wafer level packaging, pad size has no effect on the fatigue life for thermal cycling, high temperature and humidity tests and 4-point bending tests (Jang et al. 2005). In another study with controlled collapse chip carrier connection (C5) joints, it is seen that packages with thinner substrates and a larger C5 pad size have better reliability than packages with thicker substrate and smaller C5 pad size. If the solder pad size on one side is much smaller than the pad size on the other side, the C5 ball usually fails due to fatigue on the side with the smaller solder pad (Mercado et al. 2000). An independent study on the influence of printed circuit board (PCB) parameters on chip scale package assembly and reliability indicates that smaller pads generally give higher reliability while larger pads have a higher yield (Primavera, 2002). It is suggested that the pads on the package and device should be of the same size to allow a uniform joint shape to be formed. It is seen that longer bumps require thicker ACA layers for better reliability (Persson et al. 1998). By investigating solder bump flip chip on printed circuit board, Lau and Lee (2000) explore that for solder bumped Flip chip assembly

without underfill, the stress and strain increase as the chip size increases but for assembly with perfect underfill, the chip size does not affect the solder joint reliability. Also, the stress and strains are much smaller than those without underfill.

For the present investigation, reliability is of secondary importance; specimens are not being tested by cyclic loading. It is likely that chips would have proper underfill in real application. Other parameters like void content, substrate thickness, bonding pressure and time etc. can contribute considerably to both reliability and strength of a chip joint.

5.2 Effect of size on strength

Both solder and adhesive joint strengths are affected by the dimensions of the chip or the gap size.

5.2.1 Effect of size on solder strength

In a study of specimen size effect on the in-plane shear properties of silicon carbide/ silicon carbide composites, it is seen that maximum shear strength is nearly constant with no relation to the specimen gauge area. However, it tends to increase as the aspect ratio, width to thickness, decreases in case of the constant volume in the gauge section (Nozawa et. al. 2001). It is seen that when the aspect ratio increases from 1 to 3, strength is reduced by about 30%, but for the increase of 3 to 5 it is reduced by only 4% then it becomes almost constant; i.e., with increasing aspect ratio, shear strength converges into some constant value. This means that size dependency of the in-plane shear strength is considered due to the geometric effect. Therefore composites with small aspect ratio have a strength increase regardless of specimen size (Fig. 41).

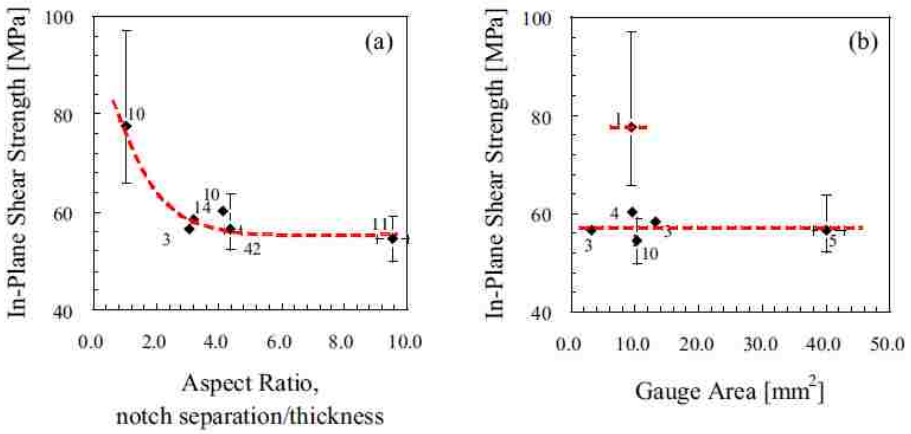


Fig. 41: Effect of shear stress on size
(Note: numbers in figures (a) and (b) mean gauge area and aspect ratio, respectively)

Using ball shear testing for solder mask defined (SMD) and non-solder mask defined (NSMD) copper ball pads, it is reported (Lim et al. 2003) that solder shear strength increases almost linearly with solder pad diameter (Fig. 42).

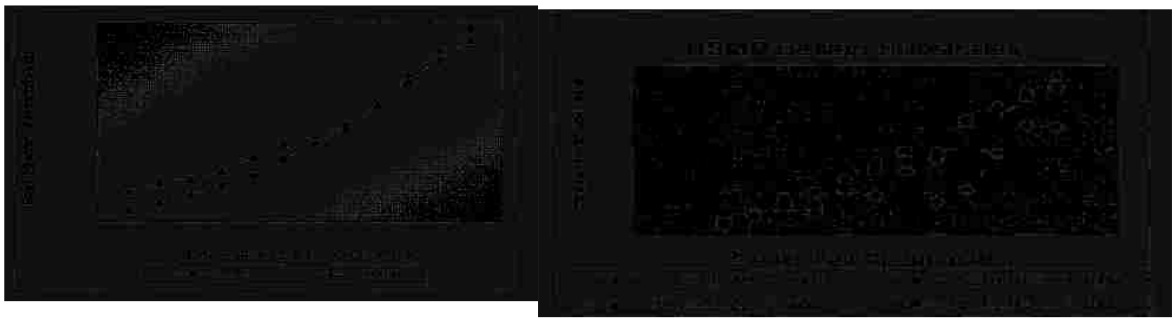


Fig. 42: Variation of solder shear strength with pad diameter

From a study it is found (Rogers and Hillman 2004) that at the printed circuit board interface solder ball shear strength (g_f) is linearly related to bonded surface area; solder pad geometry does not appear to affect the shear strength if pad areas are equal. Performing tensile tests on solder joints with different gap sizes it has been pointed out

(Zimprich et al. 2008) that the mechanical constraints leads to a strong increase of ultimate tensile strength with decreasing gap size and a simultaneous decrease of fracture strain. This is due to the development of three dimensional stresses in thinner joints, depending on diameter and thickness of the soldered joint. By investigating model solder joints of Sn3.5Ag /Cu and Sn10InAg / Cu with gap sizes varying 50 - 800 μm it is seen that tensile strength strongly depends on the gap size (Fig. 43).

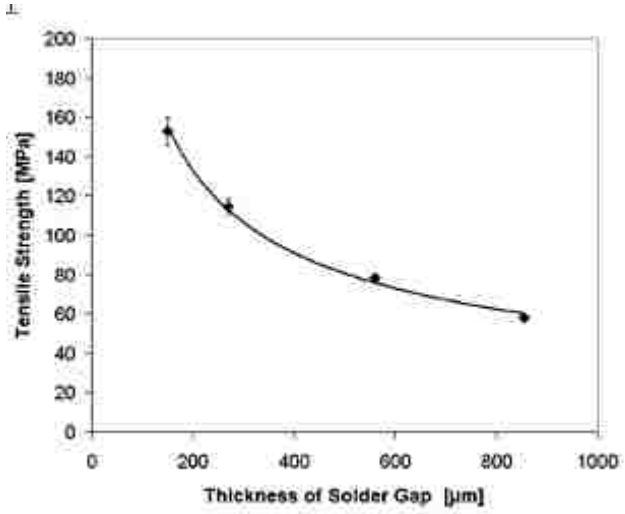


Fig. 43: Dependency of solder tensile strength with thickness (Betzwar-kotas et al., 2006)

Investigating the fracture behavior of solder joints to copper wire, Yin et al. (2009) show that the joint strength increases with decreasing thickness of the solder joint, and the strength of these joints is higher than that of bulk solders (45 MPa for Sn-3.0Ag-0.5Cu, 35 MPa for Sn-37Pb bulk solders) and the evaluation by the Orowan approximation equation in the form $\sigma_j = \sigma_{UTS}\{1 + d/(6t)\}$, where σ_j is the tensile strength

of the joint and σ_{UTS} is the ultimate stress of the bulk solder, and *d* and *t* are the diameter and thickness of the solder respectively. Their data support Betzwar-kotas findings.

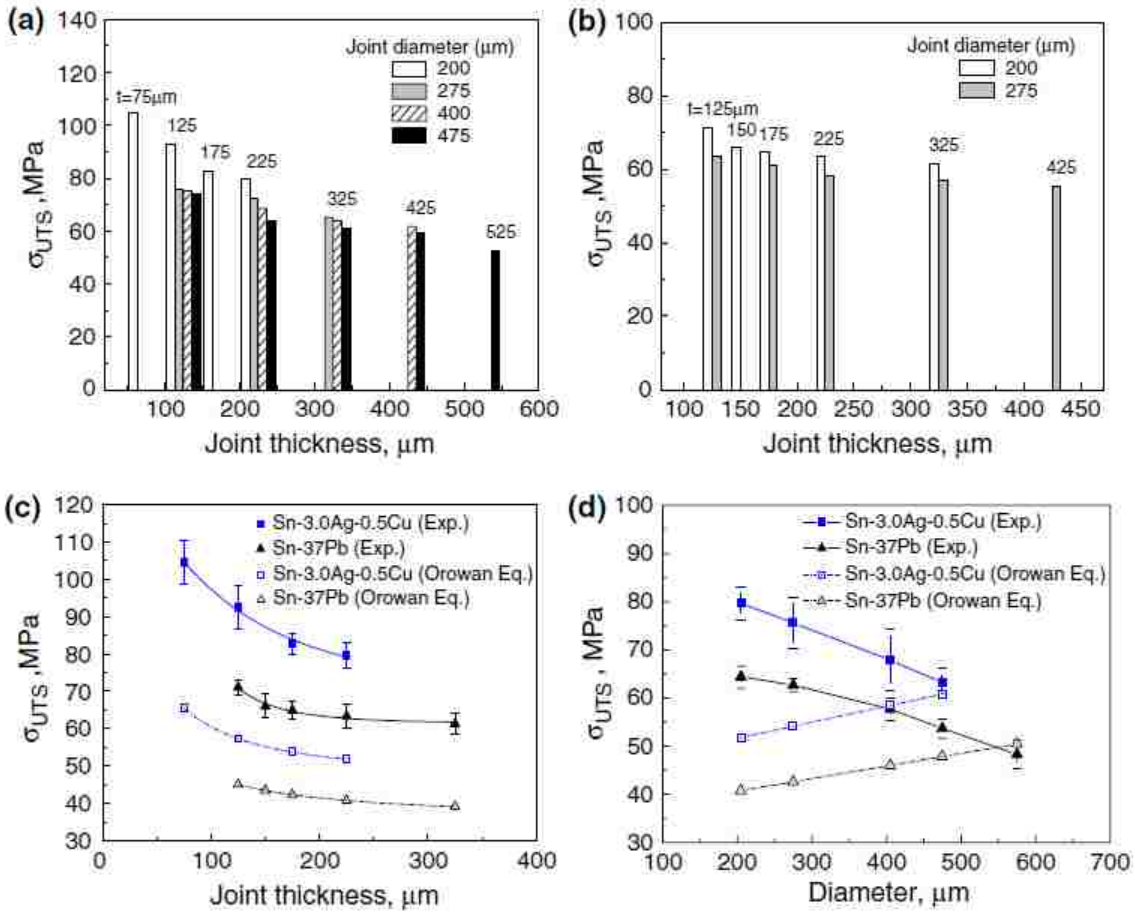


Fig. 44: Variation of tensile strength with bump thickness and diameter

However, the increase of the diameter of solder joints with constant thickness (e.g., 125 μm, 225 μm, and 325 μm) brings about a decreaseof their strength (Fig. 44 a, b, d); that is, the decrease of the thickness-to-diameter ratio of a joint results in a decrease of the joint tensile strength, which may be called an opposite size effect i.e., the joint strength does not always increase with increasing mechanical constraint of the joint. The

interfacial stress σ_r develops at the solder/ copper interfaces owing to the occurrence of a change to a triaxial stress state from the initial uniaxial stress state as shown in Fig. 45.

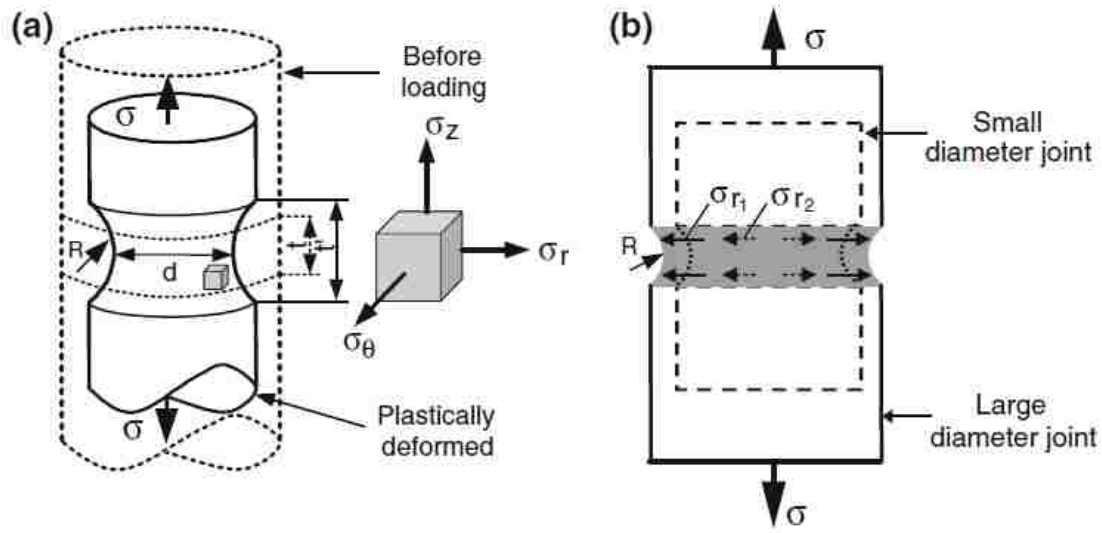


Fig. 45: Triaxial stress state and interface stresses in solder joints (a) geometry of the joint and triaxial stresses after plastic deformation; (b) interface stresses developed

The lower the joint thickness-to-diameter ratio *t*/*d*, the greater the interfacial stress σ_r and the maximum value of the interfacial stress can reach half the ultimate tensile strength of the solder, $\sigma_{r\max} = \sigma_{UTS}/2$. The maximum stress triaxiality in the joint can be given by

$$\sigma_m / \sigma_{eff} = 1/3 + \ln(1 + d/R) \tag{5.1}$$

where σ_m is the average stress, σ_{eff} is the effective stress, d is the diameter of the minimum cross-sectional area, and R is the radius of the outer notch formed after deformation, as shown in Fig. 45. For a joint with a small thickness, the *R* value may be a constant regardless of the diameter of the joint. It is easy to see that, the smaller the

diameter, the lower the stress triaxiality, and the interfacial stress σ_r follows the rule $\sigma_{r1} > \sigma_{r2}$, where σ_{r1} and σ_{r2} denote the interface stress of joints with large and small diameter, respectively. The high interface stress may trigger cracking in inter metallic compound layers of the joint and result in brittle fracture along the joint interfaces. For joints with a small diameter, the solder part deforms plastically and no crack occurs. For the joint with a large diameter (575 μm) accompanying the plastic deformation of the solder, cracks initiate and grow along the interfaces, and the final fracture takes place at the interfaces or across the solder at an angle of 45^0.

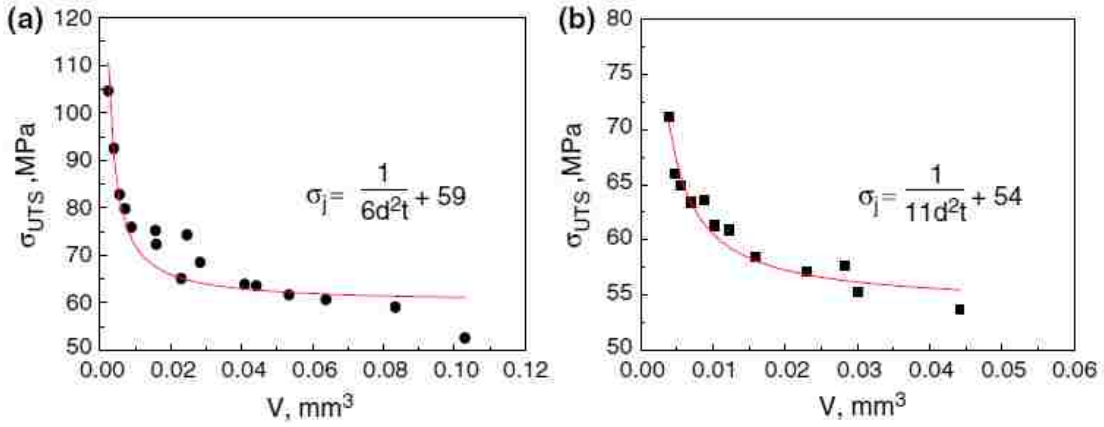


Fig. 46: Tensile stress variation with solder volume (a) Sn-3.0Ag-0.5Cu; (b) Sn-37Pb

Based on the analysis of a large amount of data, a solder joint volume effect on the tensile strength has been found (Fig. 46), that is, the strength of the solder joint increases with decreasing solder joint volume V ($V = \frac{\pi}{4} d^2 t$), and the correlation between joint

stress, σ_j and V can be well described by an inverse proportion function equation, i.e.,

$$\sigma_j = \frac{1}{A_1 V} + B_1 \text{ or } \sigma_j = \frac{1}{A_2 d^2 t} + B_2 \tag{5.2}$$

5.2.2 Effect of size on adhesive strength

From the study of peeling strength of tape carrier packaging and chip scale packaging, Yen and Lin (2007) have found that peeling strength (g_f /mm) linearly decreases with width (mm) of test vehicle. A reduction of about 22% in strength is observed (Fig. 47) for a width which is six times that of the original for tests with Toray-7100 and Tomoegawa-x adhesives.

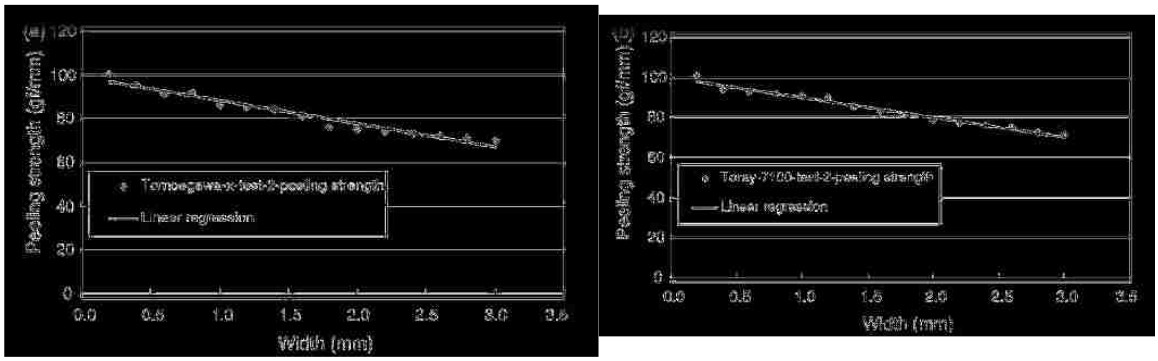


Fig. 47: Variation of adhesive peeling strength with width

In a separate reporting it is seen that for a 9 times increase in adhesion thickness (from 0.71 mm to 6.17 mm) for button type specimen tensile strength decreases to about 11% (from 1430 N to 156 N). This is almost linear reduction of strength with thickness (Minford 1993).

Another study of the effect of size shows that experimental data of tensile stresses of adhesive-bonded circular or rectangular joint can be predicted analytically under peeling

or bending load (Matsui 1990). The four different types of failure occur in an adhesive-bonded joint: cohesive failure in the adherents, interfacial failure, cohesive failure in the adhesive layer, and adhesive failure. These criteria of failure can be summarized in four formulae, given below. The nominal ultimate tensile stresses of the joints with a given geometric size and a given mechanical property of both the adherent and the adhesive have been evaluated using the four formulae. The formulae are presented in two different ways: (i) using the effective length of overlap or (ii) the thickness of adherent. Nomenclature used for the analysis is as follows:

b	width of joint	D_O	outside diameter of adherent
d	thickness of adhesive layer	E_a	modulus of adherent layer
d_m	thickness of adhesive layer where $d_m = (d)_{\alpha=1}$	I_N	Second moment of inertia about centroidal axis
G_a	transverse modulus of adhesive	I	second moment of inertia about
E	modulus of elasticity of adherent	K	coefficient
l	effective length of overlap	L	actual length of overlap
M_B	bending moment needed for failure	P	applied load
P_B	load needed to produce failure	t	thickness of adherent
β	coefficient	x	Distance from the immovable axis
α	tensile stress concentration factor: $\alpha = \sigma_{aB}/\sigma_{ui}$	t_1	adherent thickness defined in Fig. 45(e)
σ	tensile stress	σ_{aB}	tensile strength of adhesive
σ_B	tensile strength of adherent	σ_u	ultimate tensile stress (uts) of adhesive joint to produce failure
σ_{ud}	uts for cohesive failure of adherent	σ_{ui}	uts for interface failure

σ_{us}	uts for cohesive failure of adhesive	σ_{ut}	uts for adhesive failure
τ_1	Shear strength of adherent	τ_u	ultimate shear stress of adhesive-bonded lap joint under tension shear

A representation of a section of each of the unloaded joints studied is shown in Fig. 45. The two joined adherents with circular or rectangular sections are considered to be of equal outside diameter (D_o), equal width (b), equal thickness (t), equal tensile strength (σ_B) and equal modulus of longitudinal elasticity (E). The two adherents are sometimes scarf-butt joined and at other times lap joined over a given length (l). The bond between the two adherents is established by means of the adhesive layer having a given thickness (d), a given glued area (A), a given tensile strength of adhesive (σ_{aB}) and a given modulus of transverse elasticity (G_a).

In Fig. 48a, the cross-section of adhesive layer is assumed to rotate about the upper left axis (O) perpendicular to the plane of the figure, so that the tensile strains of the adhesives are proportional to the distance (x) from the immovable axis (O). The distribution of these tensile stresses is shown. The stress in any fiber is proportional to its distance from the immovable axis. Then the following equations are obtained:

$$\sigma / \sigma_u = x / l$$

$$M_B = aP_B / 2 = \int \sigma x dA = (\sigma_u / l) \int x^2 dA = (\sigma_u / l) \int x^2 dA$$

$$\sigma_u = M_B l / \int x^2 dA = M_B / (I / l)$$

Here, $\int x^2 dA = I$ is the second moment of area, and $I = I_N + A\bar{a}^2$ by the parallel axis theorem. A is the glued area, $\bar{a}$ is the distance from the centroidal axis to the immovable axis, and I_N is the second moment of the area about the centroidal axis.

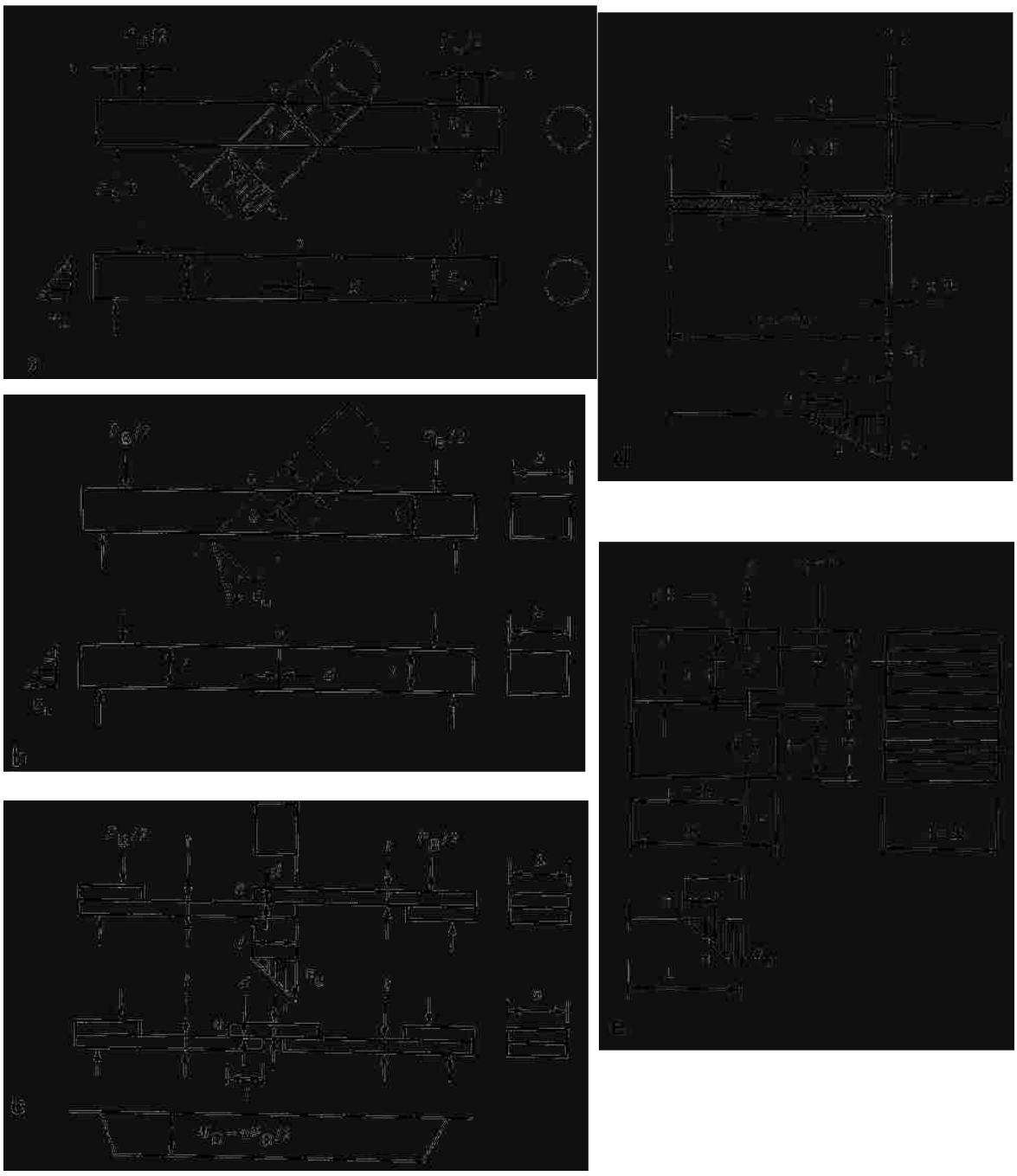


Fig. 48: Adhesive-bonded joints (a) circular butt joints; (b) rectangular butt joints; (c) rectangular lap joints; (d) T-type peel strength specimen; (e) cleavage strength specimen; (dimensions in mm)

In the case of a circular scarf butt joint (Fig. 48a):

$$I = l^3 D_o(\pi/64) + lD_o(\pi/4)(l/2)^2 = l^3 D_o(5\pi/64);$$

$$\sigma_u = M_B / l^2 D_o(5\pi/64); \qquad \text{(a)}$$

$$M_B = aP_B/2$$

In the case of a rectangular scarf butt or single lap joint (Figs. 48b and c):

$$I = l^3 b/12 + (lb)(l/2)^2 = l^3 b/3$$

$$\sigma_u = M_B/(l^2 b/3) = (M_B/b)(3/l^2) \qquad \text{(b)= (c)}$$

$$M_B = aP_B/2$$

In the case of T-type or cleavage type joints (Fig. 48d and e),

$$I = l^3 b/12 + (lb)(l/2)^2 = l^3 b/3$$

$$M_B = lP_B$$

$$\sigma_u = M_B/(l^2 b/3) = (P_B/b)(3/l) \qquad \text{(d) = (e)}$$

The relations among nominal ultimate tensile stress σ_u, peel strength P_B/b, ultimate bending moment M_B, and effective length of overlap l, are defined by the above equations. When the actual length of overlap L is considerably long ($L > l$), compressive stresses occur in the extremely narrow zone ($x < 0$). However, the effects of the compressive stresses on the failure are assumed to be negligible in comparison with the effects of the nominal ultimate tensile stress. The length of overlap l is called the effective length of overlap. As can be seen from Fig. 48d and e, sometimes $L > l$; in these cases, L is the actual length of overlap. In Fig. 48a, b and c mostly $l = L$.

In the case of interface failure tensile stress correction factor α is assumed as

$$\alpha = \sigma_{aB}/\sigma_u = 3.6\left[(G_a/E)(l/d)^2\right]^{1/2}$$

then, the nominal tensile stress in case of interfacial failure is given by

$$\sigma_{ui} = \sigma_{aB} / \alpha = (\sigma_{aB} / 3.6)\left[(E / G_a)(d / l)^2\right]^{1/2}$$

Here, l is the effective length of overlap. G_a, σ_{aB} and d represent modulus of transverse elasticity, tensile strength and thickness respectively, of the adhesive; E represents modulus of longitudinal elasticity of the adherent.

Cohesive failure in adherents occurs when the ultimate bending moment divided by the section modulus (in Fig. 48a, b and c) or the ultimate tensile load divided by the cross-sectional area. $P_B/(bt)$, (in Fig. 48d), reaches the tensile strength of the adherent σ_B. In Fig. 48e, the cohesive failure in the adherent occurs when the ultimate load divided by the cross-sectional area. $P_B/(bt_1)$, reaches the shear strength of the adherent (τ_l). The nominal ultimate tensile stress in the case of cohesive failure in the adhesive layer is given by:

$$\sigma_{us} = \sigma_{ud} d_m / d$$

$$d_m = (d)_{\alpha=1}$$

5.2.2.1 Failure criteria using effective length of overlap

The nominal ultimate tensile stresses of adhesive bonded joints are calculated from the four formulae, given below.

(a) Cohesive failure in the adherents:

$$\sigma_u = M_B / \left\{l^2 D_o (5\pi / 64)\right\},\ \sigma_B = M_B / \left\{D_o^3 (\pi / 32)\right\}$$

$$\sigma_{ud} = \left\{\sigma_B D_o^3 (\pi / 32)\right\} / \left\{l^2 D_o (5\pi / 64\right\} = 0.4\sigma_B (D_o / l)^2 \qquad 5.3(a)$$

$$\sigma_u = M_B / (l^2 b / 3),\ \sigma_B = M_B / (t^2 b / 6)$$

$$\sigma_{ud} = (\sigma_B t^2 b / 6) / (l^2 b / 3) = (\sigma_B / 2)(t / l) \qquad 5.3(b) = 5.3(c)$$

$$\sigma_u = (P_B / b)(3/l),\ \sigma_B = P_B / (bt)$$

$$\sigma_{ud} = (\sigma_B bt / b)[3/l = 3\sigma_B t / l]$$

$$(P_B / b) = \sigma_B t \qquad 5.3(d)$$

$$\sigma_u = (P_B / b)(3/l),\ \tau_1 = (P_B / bt_1),\ \sigma_{ud} = (\tau_1 bt_1 / b)(3/l) = 3\tau_1 t_1 / l$$

$$(P_B / b)_e = \tau_1 t_1 \qquad 5.3(e)$$

(b) Interracial failure:

$$\sigma_{ui} = \sigma_{aB} / \alpha = (\sigma_{aB} / 3.6)[(E / G_a)(d / l)]^{0.5} \qquad 5.4(a) \sim 5.4(e)$$

$$(P_B / b)_i = (\sigma_{aB} / 10.8)[(E / G_a) ld]^{0.5} \qquad 5.4(d) = 5.4(e)$$

(c) Cohesive failure in the adhesive layer:

$$d_m = (d)_{a=1} = (3.6)^2 (G_a / E) l$$

$$\sigma_{us} = \sigma_{ud} d_m / d = \{0.4\sigma_B (d/l)^2\}\{(3.6)^2 (G_a / E) l\} / d = 5.2\sigma_B (G_a / E)\{D_o^2 / (ld)\} \qquad 5.5(a)$$

$$\sigma_{us} = \sigma_{ud} d_m / d = \{(\sigma_B / 2)(t/l)^2\}\{(3.6)^2 (G_a / E) l\} / d$$

$$= 6.5\sigma_B (G_a / E)\{t^2 / (ld)\} \qquad 5.5(b) = 5.5(c)$$

$$\sigma_{us} = \{3\sigma_B t / l\}\{(3.6)^2 (G_a / E) l\} / d = 39\sigma_B (G_a / E)(t / d),\ (P_B / b)_s$$

$$= 13\sigma_B (G_a / E)(tl / d) \qquad 5.5(d)$$

$$\sigma_{us} = \{3\tau_1 t_1 / l\}[(3.6)^2 (G_a / E) l] / d = 39\tau_1 (G_a / E)(t_1 / d)$$

$$(P_B / b)_s = 13\tau_1 (G_a / E)(t_1 l / d) \qquad 5.5(e)$$

(d) Adhesive failure:

$$\sigma_{ut} = \sigma_{aB} \qquad (5Aa) \sim (5Ae)$$

$$(P_B / b)_t = \sigma_{aB} l / 3 \qquad (5Ad) = (5Ae)$$

Equations (5.3a), (5.4a), (5.5a) and (5Aa) represent the four criteria of the adhesive-bonded circular scarf butt joint (shown in Fig. 48a). Equations (5.3b), (5.4b), (5.5b) and (5Ab) represent the rectangular scarf butt joint (Fig. 48b). Equations (5.3c), (5.4c), (5.5c) and (5Ac) represent the single lap joint (Fig. 48c). Equations (5.3d), (5.4d), (5.5d) and (5Ad) represent the T-type peel joint (Fig. 48d) and Equations (5.3e), (5.4e), (5.5e) and (5Ae) the cleavage-type joint (Fig. 48e).

5.2.2.2 Failure criteria using adherent thickness

In the case of T-type peel strength or cleavage strength a theoretically minimum peeling force (acting perpendicularly to the adhesive layer and just sufficient to cause failure) is given as follows

$$P_B / b = 0.29 t^{0.75} \sigma_{aB} \left[\left(E / G_a \right) d \right]^{0.5} \tag{5.6}$$

By making a comparison between two equations (5.4) and (5.6) it is seen that they have a substantial difference. Equation (5.4) has not a thickness of adherent (t), but an effective length of overlap (l). However, Equation (5.6) has not l but t. In the case of $l < L$, both of them are assumed to be valid. If Equation (5.4) is equal to Equation (5.6), then the effective length of overlap is expressed as:

$$l = 10 \left[\left(G_a / E \right) \left(t^3 / d \right) \right]^{0.5} \le L \tag{5.7}$$

In the case of $l < L$, substituting Equation (5.7) in Equations (5.3d), (5.4d), (5.5d) and (5Ad) the following relations are obtained:

$$\left(P_B / b \right)_d = \sigma_B t \tag{5.3d′}$$

$$\left(P_B / b \right)_i = 0.29 t^{0.75} \sigma_{aB} \left[\left(E / G_a \right) d \right]^{0.5} \tag{5.4d′}$$

$$\left(P_B / b \right)_s = 130 t^{2.5} \sigma_B \left\{ G_a / \left(E d \right) \right\}^{1.5} \tag{5.5d′}$$

$$\left(P_B / b\right)_t = \left(10/3\right)t^{1.5}\sigma_{aB}\left[G_a /\left(Ed\right)\right] \qquad \text{(5Ad′)}$$

In addition, substituting Equation (5.7) in Equations (5.3e), (5.4e), (5.5e) and (5Ae) the following relations are obtained:

$$\left(P_B / b\right)_d = \tau_1 t_1 \qquad \text{(5.3e′)}$$

$$\left(P_B / b\right)_i = 0.29t^{0.75}\sigma_{aB}\left[\left(E / G_a\right)d\right]^{0.5} \qquad \text{(5.4d′) = (5.4e′)}$$

$$\left(P_B / b\right)_s = 130t^{1.5}t_1\tau_1\left\{G_a /\left(Ed\right)\right\}^{1.5} \qquad \text{(5.5e′)}$$

$$\left(P_B / b\right)_t = \left(10/3\right)t^{1.5}\sigma_{aB}\left[G_a /\left(Ed\right)\right] \qquad \text{(5Ad′) = (5Ae′)}$$

By utilizing the single-lap shear test with epoxy, Kahraman et al. (2008) show that adhesive strength decreases when thickness exceeds a certain range (Fig. 49).

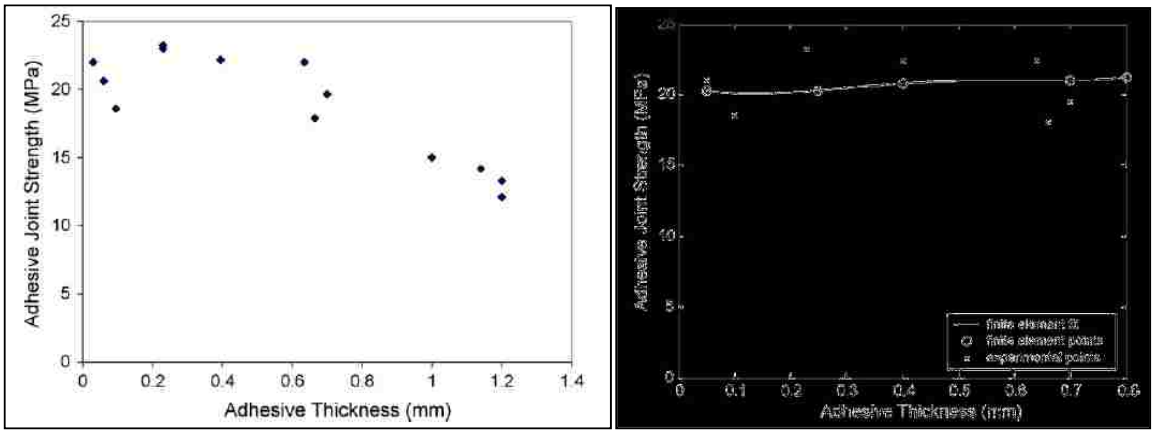


Fig. 49: Variation of adhesive strength with thickness

5.3 Model selection for present work

The correlation mentioned in equation (5.2) can be taken as a guide for estimation of joint strength. It takes into account both size and thickness effects. Some other models

could be incorporated in it. However, the constants that appear in this equation are specific for a particular type of solder; they are to be evaluated for S-bond material. Thereupon equivalent strength in shear could be found. Since the shear tests being performed, strengths estimated by this equation are to be cross-checked with models in Fig. 41 and Fig. 42. For joints with ACA, both Yen and Lin's (2007) model (Fig. 47) and Kahraman et al. (2008) findings would lead to estimate the effect of size for shear tests. Matsui models (1999) can be employed to verify the bond vigor.

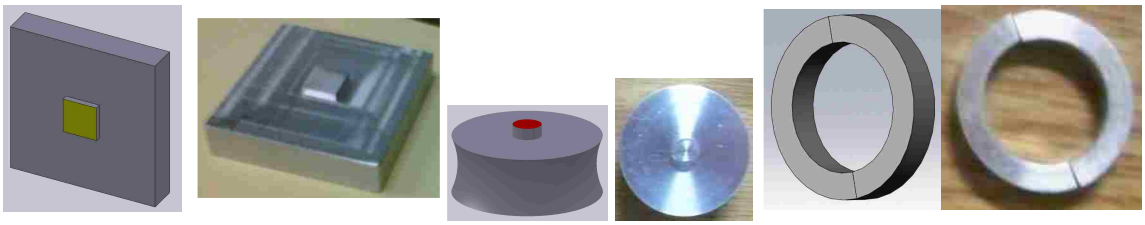
CHAPTER 6

EXPERIMENTAL VERIFICATION

Bonding strengths of aluminum surfaces joined by S-bond will be presented and be compared to those of ACA in this chapter. Since both the top of chip pad and antenna are of aluminum, joints formed between them should have similar characteristics as those formed between two aluminum surfaces. Due to shortage in provisions, these surfaces have been joined and tested manually for shear in milli-meter scale rather than micro-meter scale as used in a real chip. Since the actual manufacturing environment, as discussed in Chapter 4 could not be attained, flat surfaces were used in order to simplify the process. Results found have further been treated to incorporate the effect of size as discussed in Chapter 5. Effects of other parameters like surface finish, bending etc. are also examined.

6.1 Fabrication of test specimens

Components were prepared by machining rods and plates of aluminum (Fig. 50). The fixed plate was a 45 mm x 45 mm x 7.4 mm block with a 9 mm x 9 mm x 2.5 mm plateau (base) on it. The pulley had a pin height of 2 mm to 2.5 mm with maximum and minimum pulley diameters of 19 mm and 18.2 mm and a thickness of about 6 mm. The spacers had 20 mm outer diameter and 13 mm inner diameter with about 5.5 mm thickness. The pulley was attached to the fixed plate on the top surface of the protrusion of each. When the components were assembled, a gap existed between the base and the tip of pulley (Fig. 51) pin. Spacers helped to align the surfaces being joined and to maintain a specific gap that could be filled out by S-bond.



(a) Fixed plate (reduced scale) (b) Pulley (c) Spacers

Fig. 50: Components of a test specimen (right picture for each kind is photographed)

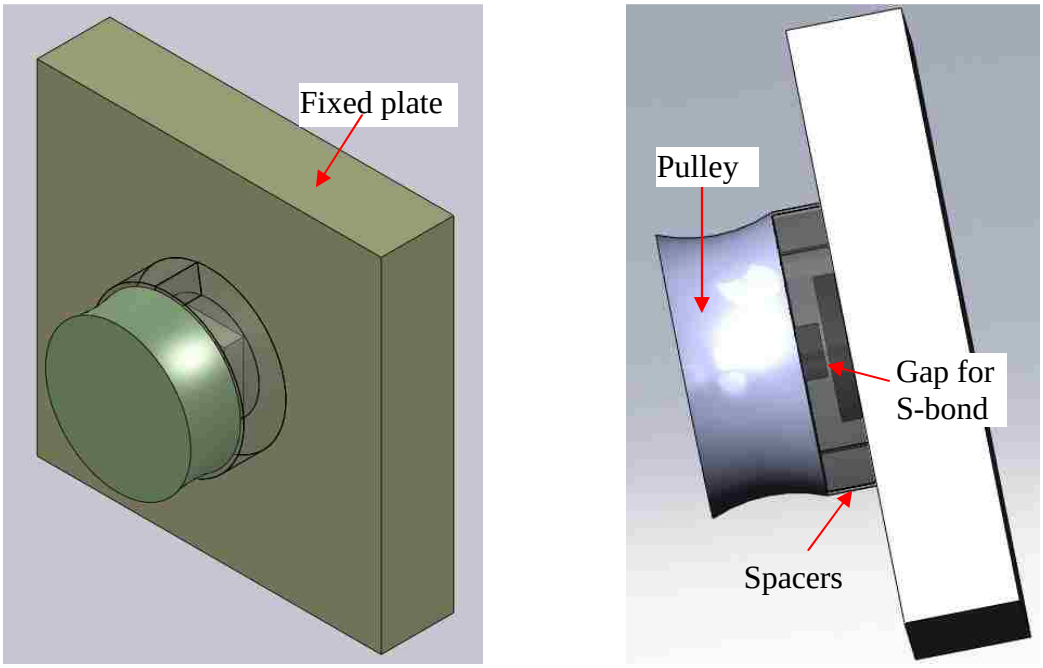


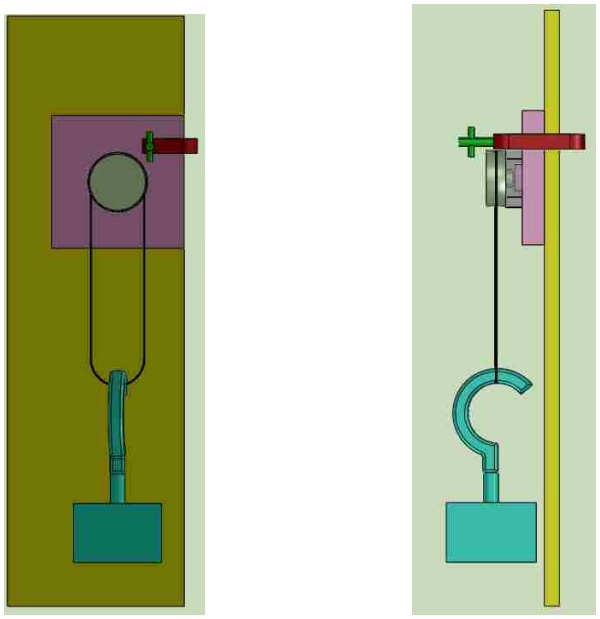
Fig. 51: Views of a specimen

Propane gas was used to heat both the fixed plate and the pulley. When temperature reached above the melting range, solid S-bond wire was melted on both the protruded surfaces being joined. Then the pulley was flipped up and positioned on the fixed plate base. A little excess S-bond material could be moved and flattened by the little movement

of the pulley on the spacer. It also helped remove oxides formed on the surfaces as mentioned in Chapter 4. When the pulley was positioned, a suitable weight could be placed on the top of pulley until the assembly cools down. With this the specimen was formed upon attachment of the pulley top to the plateau of fixed plate and was ready for testing. The specimen then could be hanged by clamping on the fixed plate to a suitable vertical surface on its valley around the assembled pulley and spacers. Weights could be suspended on the pulley.

6.2 Strength tests

Shear strengths were tested by hanging masses (Fig. 52) with a stiff chord on the pulley upon attaching the assembly to a rigid support. Masses were suspended gradually until the pulley sheared off from the assembly. Shear strength has been found by dividing the failure load by the top area of the pin (protrusion) on the pulley i.e., contact area.



(a) Front view (b) Side view

Fig. 52: Shear testing of a specimen joined with S-bond

6.3 Test parameters

Tests were performed by varying the diameter (area) of the pin tip and the thickness of the bonding material (S-bond) on the same size bases. Pin diameters tested were 0.65 mm, 0.98 mm, 1.52 mm and 1.97 mm. Gap sizes used were 0.2 mm, 0.4 mm, 0.6 mm and 0.8 mm.

6.4 Test results and analysis

In the beginning another pulley having larger diameter (6.01 mm) of the pin was joined to the fixed plate by S-bond material and was tried to find its strength, but it did not fail even due suspending high weight (15 kg). However it failed by a twist later on; failure load could not be estimated. Tests were performed with different pin diameters for a gap (i.e., S-bond thickness) of 0.6 mm. Three tests were done for each kind. Pulley weight was added with the hanged ones to get the total shear off load. Weights were added at an increment of 10 gram which incurred a maximum error of 0.3 MPa for the shear strength tested. Data reported here are the average values which have the maximum standard deviation of 1.7 MPa. Results are presented in Table 6 and in Fig. 53 for further illustration.

Table 6: Bonding strength variation with pin diameter for joining with S-bond

Pin diameter (mm)	0.65	0.98	1.52	1.97
Contact area (mm^2)	0.332	0.754	1.816	3.048
Shear off load (kg)	0.964	2.098	4.850	7.985
Failure load (N)	9.45	20.58	47.58	78.33
Shear strength (MPa)	28.5	27.3	26.2	25.7

It is seen from Table 6 and Fig. 53 that strength increased by about 11% for the smallest diameter tested. The trend is similar to the size effect as discussed in Chapter 5. However, the author noted that the strength increment could be attributed to other parameters too. As the pin diameter decreased, little bending of the pin was likely.

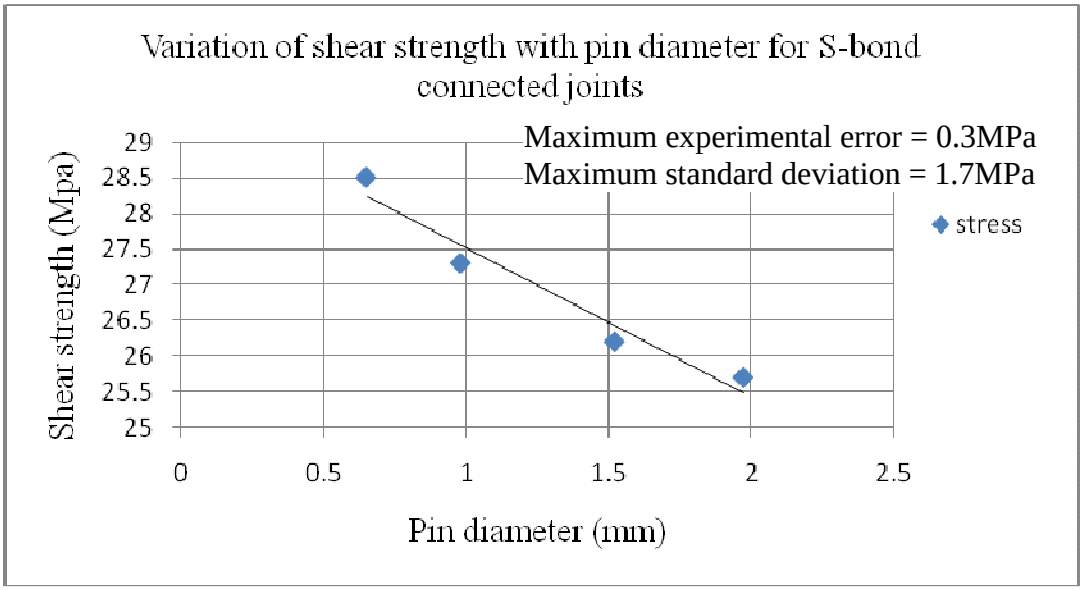


Fig. 53: Shear strength variation with contact pin diameter for S-bond connected joints

Moreover, leveling the top surface of the liquid S-bond with pin tip during bonding became more difficult for small diameter pins; minor dipping of the pin in the liquid was inevitable. Since the tensile strength of the S-bond material is 53 MPa, shear strength figures should not exceed 26.5 MPa by the maximum shear stress theory; it is a ductile material. The extrapolation of strength to the chip scale range would lead to worse, unacceptable values. As the diameter of the pin decreased, normal strength mode was contributing to the failure by a greater percentage; failure was not dictated by shear only.

Additional tests were performed with different gap sizes using the pulley-pin-tip diameter of 1.52 mm. The pin had greater diameter at the base than that at the top to avoid the effect of bending. This diameter was selected as it provided a strength figure that was closest to that expected. Moreover, small diameter pins caused greater fabrication problems. Because of same loading increment as before (10 gram) but greater pin diameter, this time error for stress estimation was 0.05 MPa only; but maximum standard deviation was more, about 2.2 MPa. As before, values specified here are the averages of three tests. Results are shown in Table 7 and in Fig. 54 for further analysis.

Table 7: Bonding strength variation with thickness of S-bond material

Gap thickness (mm)	0.2	0.4	0.6	0.8
Shear off load (kg)	4.785	5.100	4.850	4.620
Failure load (N)	46.94	50.03	47.58	45.32
Shear strength (MPa)	25.8	27.6	26.2	25.0

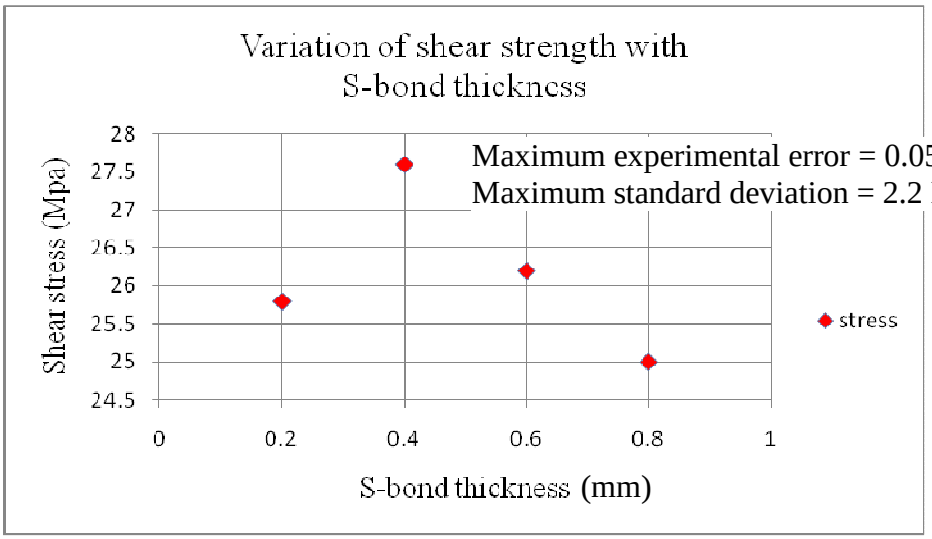


Fig. 54: Shear stress versus gap size plot for joints with S-bond

It is seen from the Table 7 and Fig. 54 that for the decrease of thickness from 0.8 mm to 0.4 mm strength has been increased by about 10%. But it then drops by about 6.5% for 0.2 mm thickness. However, the variation is not excessive. This leads to the conclusion that the variation of strength with thickness is insignificant. Again, the downward trend of last three data points indicates that for large gap size joint strength is reduced. It is also observed that for 0.4 mm thickness, the strength value is higher than material's limit.

Getting uniform thickness is difficult for small thickness; fabrication imperfection rather than thickness effect could be attributed for this. Another option is the statistical nature of the data; mentioned values are average figures. An extrapolation of the results for chip scale would not affect the strength. For very small thickness like that for a real chip, surface roughness would come into picture. Since the aluminum provides much smoother surface as seen in Chapter 3; it might not play a dominant role in the reduction of strength. Analyzing the results, it can be concluded that a properly bonded chip would exhibit enough strength as dictated by the material property.

6.4.1 Results affected by size effect

It has been seen in Chapter 5 that for the decrease of both bonding contact area and thickness, joint strength increases. However, the joint strength should not exceed the shear strength of the materials being joined. It is dictated by the minimum value, here by the strength of S-bond. Usually when chips are bonded the full strength are not attained; maximum values could be found for a combination of contact areas and thicknesses. But for the present data the maximum has already been observed; values even exceeded due to other parameters as already mentioned. Unlike traditional cases, S-bond makes a metallic bridge between other two metal components both of aluminum. Results are not

drastically affected by size, upon treating for size as mentioned in Chapter 5. So, the chip scale strength (about 30 fold less than present sizes) would not change considerably.

6.4.2 Analysis of moment effect

Due to the placement of spacers between the fixed or base plate and the pulley, bending moment offered by the hanging masses is not transferred to the pulley pin tip at S-bond interface; rather the moment is resisted by the spacers. The maximum moment occurs at the pin root. Since the pin root has greater diameter than at the tip, particularly for thinner pins, the stress induced by the moment does not play a vital role in shearing of the pulley from S-bond. The bending stress can be calculated by $\sigma = \frac{Mc}{I} = \frac{32Fx}{\pi d^3}$; where, F is the shear off load, x is the distance which is approximately half of pulley thickness in this case and d is the pin diameter at the base. Substituting the pertinent parameters, the maximum stress comes up about 70 Mpa. This is safe enough for the aluminum pin.

6.4.3 Relation between shear and normal strengths

Since the materials used for joining are all ductile metals, their normal strengths can be fairly taken as twice those in shear. Although there are different failure theories, it is an established principle applied by most design engineers that failure is dictated by the mode in which a material is weak. For ductile materials failures occur when the maximum shear stress (on a plane 45^0 to the plane of loading) due to uniaxial tensile stress exceeds certain limits (shear strengths). This can be verified with a Mohr's circle that indicates maximum stress is the radius of the circle (Beer et al., 2001).

6.4.4 Relation between static and fatigue strengths

Failure of chip joints under vibration is caused by repeated loading, thus dictated by the fatigue strength of the weakest member in connection. Since S-bond strength is less

than aluminum or other metals being joined, it governs the life of a chip connection under dynamic loading. The number cycles that a joint would survive depends on the level of stress to which it is subjected to. It is seen from early researches (EPI, 2011) that when a material is subjected to a stress level which is about 50% of its ultimate stress, it can survive for an indefinite number of cycles (Fig. 55).

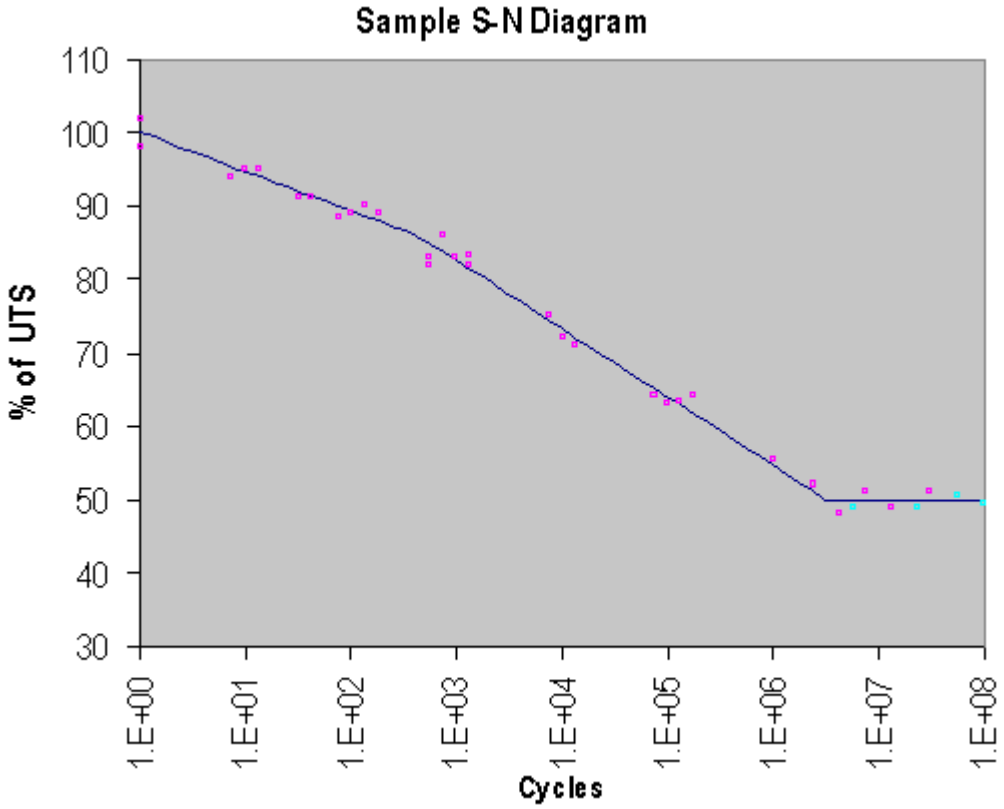


Fig. 55: Stress versus number of cycles to failure for a metal

This relation is consistent for most ductile metals including tin and titanium. S-bond consists of about 94% tin and 2% titanium (also 4% silver and a very small percentage of gallium, cerium etc.); it must have similar characteristics. Having higher static strength,

S-bond material possesses greater endurance or fatigue strength in comparison with ACA which is weak in fatigue too (Fig. 56) due to its viscoplastic properties (Dorn, 1994).

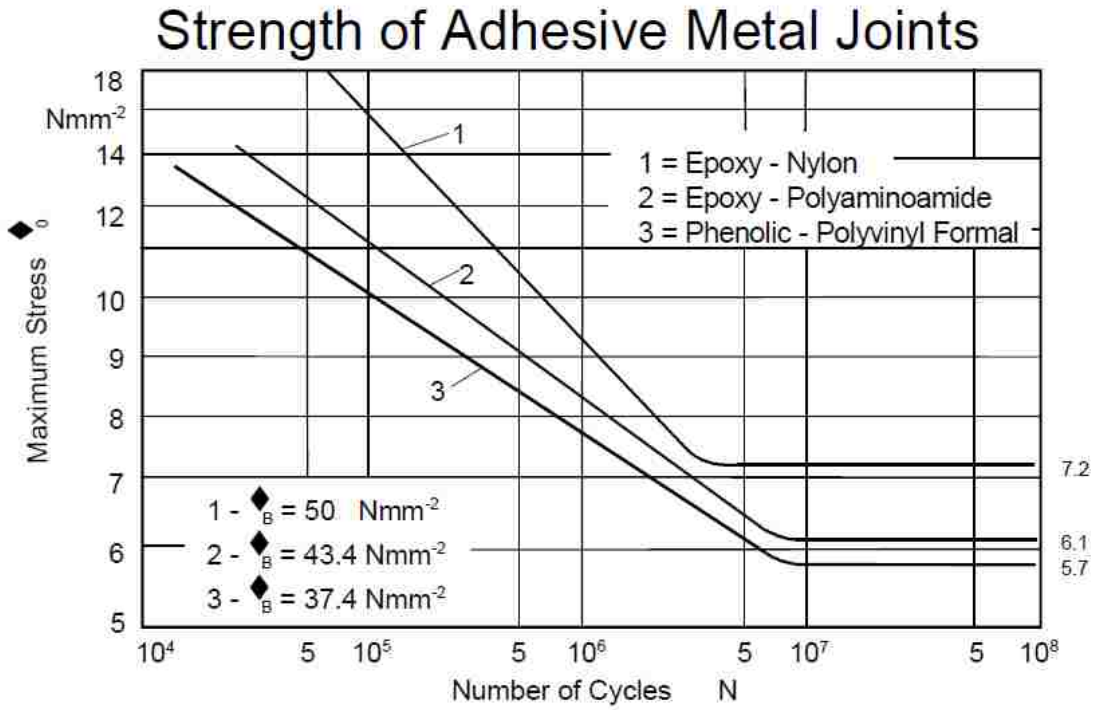


Fig. 56: Fatigue strength of adhesive layers under repeated stress

6.4.5 Effect of surface finish on joint strength

In case of joining with an adhesive (ACA), roughness of the surfaces being joined plays a vital role in determination of the strength of the connection as mentioned in Chapter 3. Here a rougher surface provides greater strength due to better adhesion with ACA and enhanced interlocking with the suspended conductive micro particles. Because of small dimensions of the components, surface finish of both UBM or chip pad and antenna is very high. This adversely affects the bond strength especially under oscillatory movements. On the other hand, S- bond establishes connection by chemical reaction,

converting aluminum oxide into the oxides of rare earth elements. Surface roughness is secondary here. The wetting of surfaces are affected by mechanical activation by moving these oxides from the surface into the bulk liquid S-bond, as mentioned in Chapter 4. However, earlier studies (Nergiz et. al., 2004) indicate about 13% reduction in bonding strength for aluminum surfaces when average surface roughness was reduced by 55% to 50 micron. Average roughness of the surfaces used in present experiments was about 10 micron; almost double that in a typical substrate antenna. Considering the surface finish as used in a real antenna, a 25% reduction in shear strengths could be incurred. This would render the shear bonding strength to about 20 MPa.

6.4.6 Comparison of chip strengths joined by S-bond with those by ACA

Joint strengths for ACA bonded chips are mostly dictated by adhesive strengths which vary over a wide range as already mentioned in Chapter 4. Typical shear strengths are about 10 MPa. On an average, 20-22% reduction in strength takes place when treated for chip-scale size as directed in Chapter 5. This would render strength figures to 8-10 MPa. Thus it is seen that S-bond joints are about 2 to 2.5 times stronger than ACA joints. The higher bond strength is attained due to higher material strength property and better adhesion characteristics of liquid S-bond than those of ACA. It supports the strength predictions by analytical and numerical methods as mentioned in Chapter 4.

The components of a test specimen other than spacers, as shown in Fig. 50, were attempted to join with ACF (3M 7303). The bonding process required application of about 300 psi pressure at about 140^0 C for 25 seconds. Spacers were not necessary as the film had a specific thickness of 100 microns. In most cases attempts were unsuccessful. Pulleys having thinner pins got their pin bent when was pressed between the chucks of a

vice. The pulley with 6.01 mm pin diameter was bonded to the fixed plate, but the bond strength was so low that it could not tolerate the self-weight of the pulley. Only the pulley with 1.97 mm pin diameter could be joined with the fixed plate. However, it was tilting due to its self-weight (4.9 gram); fell off during handling. Assuming the pulley weight as the bonding capacity, the joint strength was estimated to about 0.4 MPa considering the combined effect of shear and bending. This was more than hundred times less than S-bond strength.

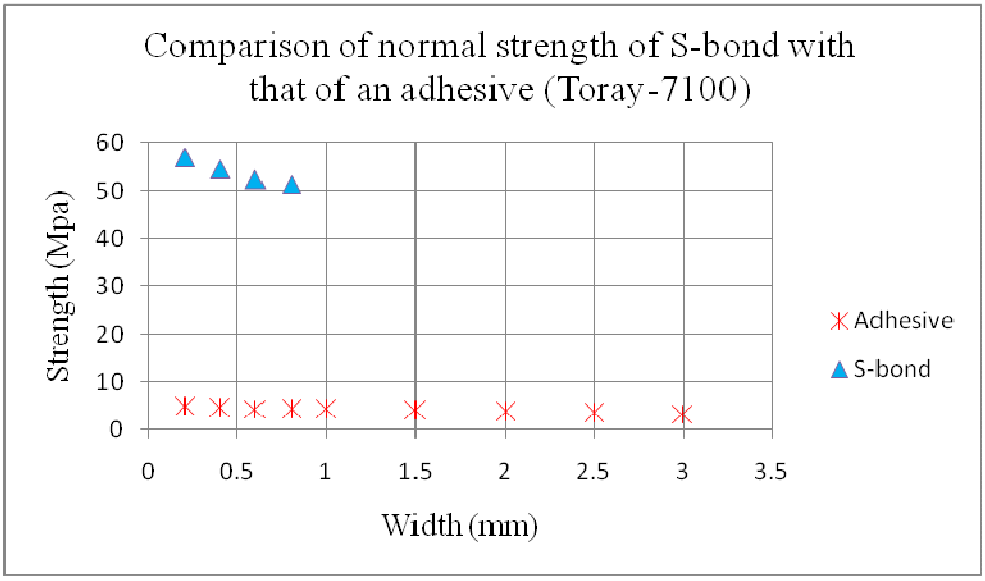


Fig. 57: Normal strength comparison of S- bond with an adhesive

As already mentioned, normal strengths of the S-bond joints can be assumed as the double of shear strengths found. They can be compared with the strengths of adhesives. However, the later should be reduced to per unit area form. Fig. 57 shows such a comparison; where adhesive strengths have been derived from Fig. 47 (Chapter 5). It is seen that S-bond joint strengths are more than ten times stronger than those of adhesives.

From Fig. 57 the reduction (≈25%) of adhesive strength with increase of width is not evident because of condensed ordinate. The graph with other adhesive (Tomoegawa-X) in Fig. 47 would be similar with 5-10% variation in numbers, not shown here because of clarity. For S-bond strength, it is not ascertained whether the downward nature with increasing width will be maintained till 3 mm. If it were the case, the strength would have been reduced to 50%. However, this is not the focus of present study; extrapolation toward right is unnecessary. On the other hand, extrapolation toward left leads to higher values as in case of shear strength. Apparently it would indicate that strength of S-bond is more than what manufacturer's data sheet shows. The reason underlying this could be attributed to manufacturing imperfection stated earlier; a small portion of cylindrical surface of the pin gets adhered by liquid S-bond material in addition to the flat end.

Even if there were increase in strength for ACA at small thickness, it had been within the maximum value which is much smaller than the strength of S-bond.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

7.1 Conclusions

Flip chip is the major component of a RFID tag. Although chip joints formed by laser beam have wide advantages over other methods of joining, they are seen limited to transparent substrates. However, in most applications these bonds are formed by joining solder bumps to the substrate antenna with adhesives (ACA). A high percentage of them fail in couple of months, particularly when exposed to vibration. Since components to which the RFID tags are attached to experience low frequency vibration, chip joints fail as they face resonance during oscillation.

Present research studies the problems associated with the mechanical failure of RFID tags, especially those subjected to vibrations. It is detected that the bonding strengths of silicon chips played major role in the failures. Adhesives having much lower modulus are mostly responsible for the reduction in natural frequency. Since adhesives have low strength in addition to modulus as well as low thermal conductivity, repeated oscillation causes them to run at elevated temperatures. As a result fatigue used to control over their survival.

Earlier investigators focused more on joining chip to the bump, but less on its assembly, i.e., attaching to the substrate. Either of the joints, between chip and bump or between antenna and bump can fail. However, the latter is more vulnerable to failure. Antenna is attached to substrate, relatively fixed when subjected to oscillation. It is the flip chip not the antenna moves during vibration. So, the joint with antenna suffers higher

stresses. In addition to this, the strength of the bonding agent i.e., adhesive also much smaller compared to the metallic bond at the other end of the bump.

Failure of flip chip joints was studied under vibration conditions; as it was identified as one of the key issue to explore. Natural frequency was calculated both analytically and numerically, and found to be in kilohertz range, reasonably high. Experimental investigations were also carried out to determine the same. However, the test results for frequency were seen to be low enough (about hundred hertz) to experience resonance. The author found that aluminum, the mostly used material for both chip pad and antenna, had low bonding capability with metals and adhesives. Due to the formation of oxide on a surface, it did not readily bond with mate with traditional solders. Its relatively smoother surface provided less entrapping for the suspended silver particles in ACA, yielding low bonding strength. Thus poor adhesive bonding at the interface and possible rise in temperature were attributed to failures under vibration.

A new joining method for the silicon chips has been suggested in this work. Instead of joining solder bump directly to the antenna, holes are drilled through antenna and substrate. S-bond material, a less familiar but more compatible with aluminum and copper, is poured in liquid form through the holes on the chip pad. However, temperature control is necessary to avoid damage to substrate; otherwise substrates compatible to high temperatures should be used. This S-bond forms metallic joints between chip and antenna, leading to “Peripheral Soldering”. Having higher strength and better adhesion capability, these joints with S-bond material provides better bonding vigor.

The strength of the Peripheral Soldering joints has been calculated both analytically and numerically and has been compared to those of ACA. It is ascertained that the

present joints are twice stronger in comparison to the traditional joints. This has been verified by an experimental investigation by joining similar surfaces as those of chip pad and antenna. Higher joining strength would provide better reliability and longer life for the chip connections, i.e., RFID tags.

7.2 Recommendations

Due to lack of facilities the proposed joining technique was verified by joining similar surfaces instead of a real chip, at a magnified scale. Industrial testing is advisable before jumping into mass scale production. Although present method apparently seems to incur more cost than the usual ones, its better reliability due to higher strength would pay off. Moreover, with large scale manufacturing the processing cost is like to drop down considerably.

REFERENCES

Basaran, C., & Chandaroy, R. (1998). Mechanics of Pb40/Sn60 near-eutectic solder alloys subjected to vibration. Applied Mathematical Modeling, 22, 601-627.

Basaran, C., Cartwright, A., Zhao, Y., & Dishongh, T. (2002). Reliability of BGA solder bumps. Advanced Packaging, 7(11), 47-56.

Beer, F.P., Johnston, E.R., & DeWolf, J.T. (2001). Mechanics of Materials. (3rd ed.) McGraw-Hill, New York, ISBN 9780073659350

Betzwar-Kotas, A., Khatibi, G., Ziering, A., Zimprich, P., Groeger, V., Weiss, B. & Ipser, H. (2006). Size effects in lead free solder-joints. Fracture and Fatigue at the Micro and Nano scales, 645-646. Retrieved Jan 15, 2011 from http://www.springerlink.com/content/j1hr62t68174816u/fulltext.pdf

Boustedt, K. (1998). GHz flip chip-an overview. Electronic Components & Technology Conference, 25-28 May, 48th IEEE, 297-302. Retrieved March 11, 2009 from http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=678709&isnumber=14953

Chaudhuri, A., Levine, L., & Frank, S. (2006). Copper stud bumping for flip chip apparatus. Semiconductor International, June. Retrieved Nov. 22, 2009 from http://mobile.semiconductor.net/article/200147Copper_Stud_Bumping_for_Flip_Chip_Applications.php

Che, F.X., Zhu, W.H., Zhang, X., & Chai, T.C. (2007). Reliability assessment for Cu/low-K structure based on bump shear modeling and simulation method. IEEE 9th Electronics Packaging Technology Conference, Singapore, Dec., 27-31. Retrieved Oct. 14, 2009 from http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=04469781

Che, F.X., & Pang, J.H.L. (2009). Vibration reliability test and finite element analysis for flip chip solder joints. Microelectronics Reliability, 49, 754–760.

Cheah, L. K., Tan, Y. M., Wei, J., & Wong, C. K. (2001). Gold to gold thermosonic flip-chip bonding. Electronics Packaging Group, Singapore. Retrieved April 7, 2009 from http://www.flipchips.com/apnotes/CheahArt.pdf

Chen, C.S., Yuan, P.H., Chiu, S.K, Chien, F.L., & Yang, K.C. (2004). Flip-chip bumbing method for fabricating solder bumps on semiconductor wafer. United States Patent. US 6,692,629; Feb. 17.

Chiang, W.K., Chan, Y.C., Ralph, B., & Holland, A. (2008). Adhesive strength of flip chip packages. International Journal of Adhesions & Adhesives, 28, 109-119.

Choi, W.J., Yeh, E.C.C., & Tu, K.N. (2003). Mean-time-to-failure study of flip chip solder joints on Cu/Ni(V)/Al thin-film under-bump-metallization. J. of Applied

Physics, 94(9), Nov., 5665-5671. Retrieved Jan. 28, 2009 from http://www.seas.ucla.edu/ethinfilm/paper/JAP05665.pdf

Clech, J.P. (1998). Flip-chip/ CSP assembly reliability and solder volume effects. Proceedings, Surface Mount International Conference, San Jose, CA, Aug. 23-27, 315-324. Retrieved Jan. 11, 2010 from http://www.jpclech.com/clech_SRS_Model_smi98.PDF

Dorn, L. (1994). Factors influencing the strength of adhesive joints. TALAT Lecture 4702, EAA, Retrieved Feb. 5, 2011 from http://www.eaa.net/eaa/education/talat/lectures/4702.pdf

Electronic Materials Pte Ltd. (2006). S-bond solder products: How they work. Retrieved Oct. 10, 2010 from http://www.elecmat.biz/index_files/Page648.htm

EPI. Inc. (2011). Metal Fatigue. Accessed on March 7, 2011 from http://www.epi-eng.com/mechanical_engineering_basics/fatigue_in_metals.htm

Erdahl, D.S., Allen, M.S., Ume, I.C., & Ginsberg, J.H. (2008). Structural modal analysis for detecting open solder bumps on flip chips. IEEE Transactions on Advanced Packaging, 31(1), Feb., 118-126.

Hwang, J.S. (2008). Filler size and content effects on the composite properties of anisotropic conductive films (ACFs) and reliability of flip chip assembly using ACFs. Microelectronics Reliability, 48, 645–651. doi:10.1016/j.microrel.2007.10.004

Ishii, T., & Aoyama, S. (2004). Novel micro-bump fabrication for flip-chip bonding. Journal of Electronic Materials, 33(11), L21-L23. Retrieved Jan.15, 2009 from http://www.springerlink.com/content/n58566284666t413/fulltext.pdf

Jang, S.Y., Park, T.S., Kim, Y.S., Jeong, J.W., Bang, J.J. & Kang, D.K. (2005). Wafer level package solder joint reliability study for portable electronic devices. 55th IEEE Electronic Components and Technology Conference. Lake Buena Vista, FL, 31 May - 3 June.

Jiang, J., Tsao, S., O'Sullivan, T., Razeghi, M., & Brown. G.J. (2004). Fabrication of indium bumps for hybrid infrared focal plane array applications. Infrared Physics & Technology, 45, 143–151.

Jones, W.K., Liu, Y., Shah, M., & Clarke, R. (1998). Mechanical properties of Pb/Sn , Pb/In and Sn-In solders", Soldering & Surface Mount Technology, 10(1), 37–41. http://www.emeraldinsight.com/Insight/viewPDF.jsp?contentType=Article&Filename=html/Output/Published/EmeraldFullTextArticle/Pdf/2190100107.pdf

Jung, E., Aschenbrenner, R., Ostmann, A., Zakel, E., & Reichl, H. (1995). Flip chip soldering and adhesive bonding on organic substrates. Electronic Manufacturing

Technology Symposium, Proceedings of Japan 18th IEEE/CPMT International, 4- 6 Dec., 67-71. Retrieved Feb. 4, 2009 from http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=540996&isnumber=11576

Kadioglu, F., & Adams, R. (2008). Non-linear analysis of a ductile adhesive in the single lap joint under tensile loading. J. of Reinforced Plastics and Composites. July 31, 1-10. Retrieved Oct. 14, 2009 from http://jrp.sagepub.com/cgi/rapidpdf/0731684408093455v1.pdf

Kahraman, R., Sunarb, M., & Yilbas, B. (2008). Influence of adhesive thickness and filler content on the mechanical performance of aluminum single-lap joints bonded with aluminum powder filled epoxy adhesive. Journal of Materials Processing Technology 205, 183–189

Kloeser, J., Heinricht, K., Jung, E., Lauter, L., Ostmann, A., Aschenbrenner, R., & Reichl, H. (2000). Low cost bumping by stencil printing: process qualification for 200 μm pitch. Microelectronics Reliability, 40, 497-505.

Koo, J.M., Kim, Y.N., Yoon, J.W., Kim, D.G., Noh, B.I., Kim, J.W., Moon, J.H., & Jung, S.B. (2008). Effect of displacement rate on bump shear properties of electroplated solder bumps in flip-chip packages. Materials Science and Engineering A, 483–484, 620–624.

Kordas, K., Pap, A.E., Toth, G., Pudas, M., Jaaskelainen, J., Uusimaki, A., & Vahakangas, J. (2006). Laser soldering of flip-chips. Optics and Lasers in Engineering, 44, 112–121.

Kwon, W.S., & Paik, K.W. (2004). Contraction stress build-Up of anisotropic conductive films (ACFs) for Flip-Chip Interconnection: effect of thermal and mechanical properties of ACFs. J. of Applied Polymer Science, 93(6), 2634–2641. Retrieved Feb. 7, 2009 from http://www3.interscience.wiley.com/cgi-bin/fulltext/109087789/PDFSTART

Lau, J., Gratelo, K., Schneider, E., Marcotte, T., & Baker, T. (1996). Solder joint reliability of large plastic ball grid array assemblies under bending, twisting, and vibration conditions. Circuit World, 22(1), 27-32.

Lau, J.H. & Lee, S.W.R. (2000). Effects of underfill delamination and chip size on the reliability of solder bumped flip chip on board. Int. J. of Microcircuits and Electronic Packaging, 23(1); 33-39.

Lim, A.C.P., Kheng, L.T., Alamsjah, A. & Happy (2003). The effect of ball pad designs and substrate materials on the performance of second-level interconnects. 5th Electronics Packaging Technology Conference . 10-12 Dec. Singapore, 563-568.

Mangold, R.L., & Lance, J.G. (1998). Process for fabricating a solder bump for a flip chip integrated circuit. United States Patent, US 5,759,910; Jun. 2.

Matsui, K. (1990). Effect of size on nominal ultimate tensile stresses of adhesive-bonded circular or rectangular joints under bending or peeling load. Int. Journal of Adhesion and Adhesives. 10(2), 90-98.

Mercado, L.L., Sarihan, V., Guo, Y. & Mawer, A. (2000). Impact of solder pad size on solder joint reliability in flip chip PBGA packages. IEEE Transactions on Advanced Packaging, August, 23(3), 415-420.

Minford, J.D. (1993). Effect of adhesive thickness on average failure load for button-type specimens pulled intension. Handbook of aluminum bonding technology and data. 1st ed. New York: Dekker.

Nam, D.J., Lee, J.H., & Yoo, C.D. (2007). Fabrication of a flip chip solder bump using a thin mold and ultrasonic filling. J. Micromechanics and Microengineering, 17, 1863–1869. doi:10.1088/0960-1317/17/9/015

Nergiz, I., Schmage, P., Herrman, W. & Ozen, M. (2004). Effect of alloy type and surface conditioning on roughness and bond strength of metal brackets. American J. of Orthodontics & Dentofacial Orthopedics, 125(1), 42-50.

Nicewarner, E. (1999). Interconnect resistance characteristics of several flip-chip bumping and assembly techniques. Microelectronics Reliability, 39, 113-121. doi:10.1016/S0026-2714(98)00161-9

Nozawa, T., Curzio, E.L., Katoh, Y., Snead, L.L. & Kohyama, A. (2001). Specimen size effect on the in-plane shear properties of silicon carbide/silicon carbide composites. 35-39, Accessed on Feb. 6, 2011 from http://www.ms.ornl.gov/fusionreactor/pdf/dec2001/02.1%20-%2035-39%20NOZAWA.pdf

Olver, K.A. (2004). Evaporated indium bumps for flip chip assembly. Tutorial 38 – Feb. Retrieved Sept. 25, 2009 from http://www.flipchips.com/tutorial38.html

Osborne, M., Ling, J., Huynh, C., Qin, I., & McTaggart, V. (2005). Stud Bumping for flip chip – an alternative strategy. IMAPS Device Packaging Conference, March, Session 3. Retrieved Feb. 12, 2009 from http://www.kns.com/UPLOADFILES/DGALLERY/6001.PDF

Persson, K., Lai, Z., Zribi, A., Liu, J. & Willander, M. (1998). Effect of bump height on flip-chip joint reliability using ACA. Proc. of 3rd International Conference on Adhesive Joining and Coating Technology in Electronics Manufacturing, Binghamton, NY, Sep. 28-30, 132-136

Primavera, A.A. (2011). Influence of PCB parameters on chip scale package assembly and reliability. Proc. SMTA Int. Conf., Sep. 12, 1999. Accessed Feb. 6, 2011 from

http://universalinstruments.com/wcms/images2.nsf/(GraphicLib)/csp_bgapaper.pdf/$File/csp_bgapaper.pdf

Ramamurti, V. (2000). Mechanical vibration practice with basic theory. New York: CRC Press.

Riley, G.A. (2000). Stud bump flip chip. Tutorial 3, Dec. Retrieved April 4, 2009 from http://www.flipchips.com/tutorial03.html

Rogers, K. & Hillman, C. (2004). The effects of plating materials, bond pad size and bond pad geometry on solder ball shear strength. SMTA International Conference Proceedings, Rosemont, IL, Sep. 26-30, 421-428.

S-Bond Technologies. (2010). Property Bulletin. Retrieved Oct. 13 from http://www.s-bond.com/cms/files?Prop_Bull_SB220_ID51697.pdf

Schreiber, C.M ,& Le, B. (1998). Integral copper column with solder bump flip chip. United States Patent, US 5,790,377; Aug. 4.

Shabana, A.A. (1996). Theory of vibration: an introduction. 2nd ed. New York: Springer.

Sood, B., Das, D., Azarian, M., Pecht, M., Bolton, B., & Lin, T. (2008). Failure site isolation on passive RFID tags. Proc. of the 15th IEEE International Symposium on Physical and Failure Analysis of Integrated Circuits, July 7-11, Singapore, 337-341. Retrieved Nov. 11, 2009 from http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=4588216&isnumber=4588140

Tan, C.W., Cha, Y.C., & Yeung, N.H. (2003). Behavior of anisotropic conductive joints under mechanical loading. Microelectronics Reliability, 43, 481–486.

Teutsch, T., Zakel, E., & Azdasht, G. (2008). Pulsed-laser heating for flip-chip assembly. Advanced Packaging, 1-5. Retrieved March 18, 2009 from http://pactech.com/files/48%20Pulsedlaser%20Heating%20for%20Flip%20Chip%20Assembly.pdf

Wang, Z.Y., Islam, M.S., Dong, L.H., & Dong, Y.H. (2011). Failure study of micron-sized flip-chip joints on passive RFID tags. Int. J. Precision Technology, 2(1), 81-92.

Wang, T., Jonsson, M., Campbell, E.E.B., & Liu, J. (2006). Development of carbon nanotube bumps for ultra fine pitch flip chip interconnection. Electronics System Integration Technology Conference, Dresden, Germany, 892-895.

Wang, W., Chan, Y.C., & Pecht, M. (2008). Anisotropic conductive adhesive for flip-chip interconnects. J. Adhesion Science and Technology, 22, 871-892.

Yang, S.Y., & Lee, S.B. (2002). Analytical approach to evaluate shear stress in flip chip interconnection using NCA/ACF. 4th Int'l Symposium on Electronic Materials and Packaging, IEEE, 4-6 Dec., 204-209. doi: 10.1109/EMAP.2002.1188838

Yap, D., & Lawyer, P.H. (2004). Precision electroplated solder bumps and method for manufacturing thereof. United States Patent, US 6,828,677 B2; Dec. 7.

Yen, Y.T & Lin, Y.C. (2007). Study peeling strength of tape carrier packaging and chip scale packaging. Sensors and Actuators A, 139, 330–336.

Yin, L.M., Zhang, X.P. & Lu, C. (2009). Size and volume effects on the strength of microscale lead-free solder joints. Journal of Electronic Materials. 38(10), 2179-2183

Yoon, J.W.; Chun, H.S., & Jung, S.B. (2008). Reliability evaluation of Au–20Sn flip chip solder bump fabricated by sequential electroplating method with Sn and Au. Materials Science and Engineering A, 473, 119–125.

Zakel, E., Azdasht, G., Teutsch, T., & Blankenhorn, R.G. (2003). Laser assisted flip chip assembly for LCD applications using ACP and NCP adhesive joining. Packaging Technologies,1-8. Retrieved Feb. 20, 2009 from http://pactech.com/files/29%20ICEP%202003%20Japan%20Paper%2004_2003.pdf

Zhong, Z. (2001a). Stud bump bond packaging with reduced process steps. Soldering & Surface Mount Technology,13(2), 35-38.

Zhong, Z. (2001b). Flip chip assembles using gold bumps and adhesives. Microelectronics International, 18(3), 15-19.

Zhou Y., & Dasgupta, A. (2006). Vibration durability investigation for SAC and SnPb solder: based on JCAA/JG-PP lead-free solder project test results. Report by CALCE Electronic Products and Systems Center, University of Maryland, College Park. Retrieved Sept. 12, 2009 from http://www.teerm.nasa.gov/LFS%20Reliability/JGPP%20report_final_10_25_2006%20(2)_.pdf

Zhou, Y., Plaza, G., Dasgupta, A. & Osterman, M. (2009). Vibration durability of Sn3.0Ag0.5Cu (SAC305) solder interconnects: harmonic and random excitation. J. IEST, 52(1), 63-86.

Zimprich, P., Betzwar-Kotas, A., Khatibi, G., Weiss, B. & Ipser, H. (2008). Size effects in small scaled lead-free solder joints. J Mater Sci: Mater Electron,19: 383–388

3M. (2004). Anisotropic conductive film adhesive 7313 bonding process development. 3M Technical Bulletin, 8(4), Aug. 78-9236-7051-3. Retrieved Jan. 27, 2009 from http://multimedia.3m.com/mws/mediawebserver?mwsId=SSSSSu7zK1fslxtU48_Zmxteev7qe17zHvTSevTSeSSSSSS--

VITA

Graduate College
University of Nevada, Las Vegas

Md Syful Islam

Degrees:

Bachelor of Science, Mechanical Engineering, 1986
Bangladesh University of Engineering and Technology, Dhaka

Master of Science, Mechanical Engineering, 1990
Bangladesh University of Engineering and Technology, Dhaka

Master of Science, Mechanical Engineering, 1990
Tuskegee University, Tuskegee

Publications:

1. Wang, Z.Y., **Islam, M.S**., Dong, L.H., & Dong, Y.H. (2011). Failure study of micron-sized flip-chip joints on passive RFID tags. Int. J. Precision Technology, 2(1), 81-92.
2. Mahfuz, H., **Islam, S.,** Saha, M., Carlsson, L., & Jeelani, S. (2005). Buckling of Sandwich Composites; Effects of Core-Skin Debonding and Core Density. Applied Composite Materials, 12, 73-91.
3. Mahfuz, H., **Islam, S**., Carlsson, L., Kardomateas, G., & Jeelani, S. (2001). Buckling Response of Sandwich Composites: Effect of Core Density and Implanted Interface Cracks. 13th Int. Conference on Composite Materials (ICCM-13), June 25-29, CD Proceedings, Paper ID: 1452.
4. Mahfuz, H., **Islam, S**., Carlsson, L, Atkins, M., & Jeelani, S. (2000). Effect of Implanted Delamination and Core Density on the Buckling Behavior of Sandwich Composites. ASME, AD-Vol. 62, AMD-Vol. 245, Mechanics of Sandwich Structures, 143-150.
5. **Islam, M.S**., Hossain, M.I. & Sarkar, M.A.R. (1993). Effect of Pressure on Natural Convection Heat Transfer from an Inclined Cylinder. J. of the Institution of Engineers (India), August 74, 50-55.

Dissertation Title: Peripheral Soldering of Flip Chip Joints on Passive RFID Tags

Dissertation Examination Committee:
Chairperson, Zhiyong Wang, Ph. D.
Committee Member, Brendan O'Toole, Ph. D.
Committee Member, Woosoon Yim, Ph. D.
Committee Member, Vellore Venkatesh, Ph. D.
Graduate Faculty Representative, Rama Venkat, Ph. D.