7-9-2008

Semiconductor yield analysis and prediction using a stochastic layout sensitivity model

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SEMICONDUCTOR YIELD ANALYSIS AND PREDICTION USING A STOCHASTIC LAYOUT SENSITIVITY MODEL

By

Rani S. Ghaida

B.E., Computer Engineering, Lebanese American University, 2006

THESIS

Submitted in Partial Fulfillment of the
Requirements for the Degree of

Master of Science
Computer Engineering

The University of New Mexico
Albuquerque, New Mexico

May, 2008

ACKNOWLEDGEMENT

I would like to cordially acknowledge Prof. Payman Zarkesh-Ha, my advisor and thesis chair, for being an outstanding teacher in the classrooms and for his never-ending encouragement and support of my research.

I thankfully recognize Prof. Chaouki Abdallah, my department chair and thesis honorary committee member, who was kind enough to provide many insightful observations and valuable comments. I am deeply grateful to him for his wisdom and support and for giving me every opportunity to succeed.

I am also grateful to Prof. Chuck Hawkins, thesis honorary committee members, for his in-depth reviews of this manuscript and for his exceptional and valuable teachings. He is one of my most influential academic teachers.

I gratefully acknowledge Prof. Samer Saab, for giving me motivations to pursue my graduate studies and for recommending me to UNM graduate school. A special thank goes to Prof. Iyad Ouaiss who left an everlasting and valuable mark on me.

It is a pleasure to express my gratitude to Joud Khoury, my friend, for helping me getting settled in Albuquerque and making my graduate studies much easier.

This thesis is dedicated to my parents, Nabila El-Kadi and Said Abou Ghaida. Their endless love and support made the completion of my graduate studies possible. Sincere thanks to Houssam, Rania, and Hickmat for being supportive and caring siblings.

Finally, I convey many thanks to all my friends for filling my life with love and happiness.

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ABSTRACT OF THESIS

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ABSTRACT

Spot defects represent the main challenge for enhancement of semiconductor manufacturing yield. As a result, the yield of modern integrated circuits is associated with the layout sensitivity to defects. The term "layout sensitivity" is defined as the ratio of "critical area", i.e. part of the layout in which a defect must be placed to cause a functional failure of the device, to the overall layout area. Semiconductor yield models are traditionally based on the analysis of the "critical area". Such models give accurate results; however, critical area analysis requires massive computations that render these models effort and time consuming. The stochastic method of yield modeling presents a much faster and easier approach. This thesis contributes to the stochastic method of yield modeling by offering an efficient model that predicts the layout sensitivity to defects using very basic layout information.

The model has some imperative applications that can expedite the yield analysis and prediction for modern VLSI designs. The prime application is pre-layout yield prediction. Using the proposed model, yield prediction can be performed even before starting the costly phase of layout design. Another application is yield forecasting and prediction of defect density requirements for future manufacturing technologies not yet developed. Fi-

nally, the simplicity of the model allows its use during automatic cells placement to enhance the yield. A “yield-aware automatic cells placement tool” is implemented.

This thesis tackles also the subject of semiconductors reliability. We derive a model that predicts the layout sensitivity to interconnect “narrow defects”, i.e., missing material defect causing the formation of a narrow site in the victim interconnect without resulting in a disconnection in a signal path. Narrow defects favor electromigration, a major interconnect failure mechanism, that makes narrow interconnects very likely to cause functional failure during operation in the field. The model is used to estimate the average number of narrowing defects in the layout.

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Nomenclature

Acronyms

ADC	Automatic Defect Classification
Al	Aluminum
CMP	Chemical Mechanical Planarization
Cu	Copper
DFM	Design For Manufacturability
EM	Electromigration
HEPA	High Efficiency Particle Air
idf	Interconnect Density Function
ILD	Interconnect Layer Dielectric
ITRS	International Technology Roadmap for Semiconductor
LER	Line Edge Roughness
MTTF	Mean-Time-To-Failure
pdf	Probability Density Function
PRS	Placement and Routing Software
SEM	Scanning Electron Microscope
ULPA	Ultra Low Penetration Air
YA-PRS	Yield-Aware Placement and Routing Software

Variables

A	Layout area
A_c	Critical area

A_r	Area of routing channel
α	Cluster parameter
β	Parameter used in yield-aware placement algorithm
γ	Parameter relating number of nets to number of tracks in routing channel
d	Channel density
D	Metal density
D_0	Average defect density
f_λ	probability density function of average defect density
f_s	Defect size distribution
H	Routing channel height
L	Total wire length
λ	Average number of defects
m	Number of channels covered by a defect
n	Fab cleanliness parameter
P_f	Probability of failure
P_n	Probability of narrows
P_s	Probability of failure
r	Defect size
r_0	Critical defect size
S	Defect/layout sensitivity
S_n	Layout sensitivity to narrows
S_{open}	layout sensitivity to open defects
S_{short}	layout sensitivity to short defects

s	Wire spacing
w	Wire width
w_n	Critical wire width
Y	Semiconductor manufacturing yield
Y_{AP}	Yield of assembly and packaging stage
Y_{BI}	Yield of burn-in process
Y_{FAB}	Fabrication yield
Y_{MFT}	Manufacturing yield

Chapter 1

Introduction

1.1. Preliminaries

The move to advanced deep submicron technologies and the ever increase in functionality of semiconductor devices raise serious challenges to the manufacturability and productivity of semiconductors. The standard metric of manufacturability is semiconductor manufacturing yield, defined as, the ratio of devices performing properly, to the total number of devices of the produced wafers. Semiconductor manufacturing yield is a major factor affecting the fabrication cost. Hence, maintaining a certain acceptable yield is a necessity. Acceptable manufacturing yield is actually a constraint for the move toward smaller feature sizes.

Enhancement of manufacturing yield is required for maintaining a competitive position in the rapidly advancing international semiconductor industry. However, yield enhancement faces non-stopping challenges as technology advances. The major everlasting challenge to yield enhancement is the occurrence of spot defects during the manufacturing process. Spot defects are extra or missing material generating circuit failures. Spot defects can also cause the deformation of interconnects without creating a circuit failure. In case the deformation is a missing material defect, then we name it a “narrow defect”. Narrow defects, similar to other types of spot defects, have an effect on yield, but also, have an impact on reliability of IC chips. There are many sources of spot defects including: deposition of particles present in the air on the surface of the wafer during manufac-

turing, problems in lithography, and other imperfections in the evermore complex fabrication process. Basically, spot defects are random phenomena occurring on ICs with certain spatial distribution, size, and frequency of occurrence per unit area [1]. To study the effects of spot defects on manufacturing, analysis of the "critical area" is needed. Critical area is part of the IC layout in which the center of a spot defect must be placed to cause a functional failure of the device [2]. Another measure is also being used and is given by the ratio of critical areas to the die area, also known as the "layout sensitivity" [3]. In essence, layout sensitivity to spot defects characterizes the robustness of an IC.

Yield modeling is necessary for yield enhancement and cost projection. In particular, "random yield" modeling studies the effect of spot defects on IC functionality which makes it very important for defect management, and consequently, achieving reliability, yield, and cost objectives [4]. Yield forecasting, which is based on some statistical information about the layout, is also necessary in studying the economical feasibility of new products, and therefore, it can be used to determine whether or not a design would meet its cost objectives [1], [5].

1.2. Problems Statement

1.2.1. Complexity of Critical Area Analysis

Semiconductor manufacturing yield is mainly affected by spot defects. As a result, yield modeling is traditionally based on the analysis of critical area. However, as the functionality of ICs grows and feature dimensions are scaling down, modern VLSI devices are becoming evermore complex and analysis of their critical areas becomes more effort- and

time-consuming. Performing critical area analysis in modern VLSI designs can easily take several days [6]. This can greatly affect the time-to-market of VLSI products.

1.2.2. Necessity of Yield Prediction and Inaccuracy of Current Methods

Yield prediction for designs before the actual generation of its layouts is getting more and more important. In fact, as technology advances, layout generation of modern VLSI devices is becoming extremely complicated due to the increase in routing and architectural complexities, meeting more severe timing requirements, and dealing with manufacturability consideration at the design stage with design for manufacturability (DFM) techniques. As a result, time and cost required for layout generation has become a real burden. Therefore, if yield prediction can be used to determine whether or not a product will meet its cost objective before generating the actual layout, then this would avoid the costly phase of redesign.

Accurate cost estimates require accurate yield predictions since cost is very dependent on the manufacturing yield as discussed earlier [7]. However, existing yield prediction methods lacks accuracy.

1.2.3. Existing Models for Narrow Defects

Narrow defects can seriously affect the reliability of IC products. Specifically, narrow defects favor electromigration, the major interconnect failure mechanism, which will have direct implications on reliability of IC products. Moreover, this type of defects is ex-

pected to present a serious challenge for yield enhancement with the ever decreasing feature size [5]. Models that include the effect of narrow defects in predicting the yield are very rare and existing ones are ineffective. In addition, to the best of our knowledge, there are no existing methods for prediction the number of narrows in VLSI design.

1.3. Objective and Scope of this Thesis

The stochastic method for yield modeling addresses the first two stated problems. This method relies on statistical information about the layout to model and predict semiconductor manufacturing yield. Introduced by Stapper since 1983 [8], it was not until the beginning of the 21st century that researchers became interested in the stochastic method for yield modeling. Yet, this method could not resolve the addressed problems because of its lack of accuracy.

This thesis contains important contributions to the stochastic method of yield modeling. The work presented in this thesis enhances the accuracy of the stochastic modeling. In particular, we propose an efficient method that can model and predict the layout sensitivity to spot defects with good accuracy. Some innovative and very beneficial applications of the model are also offered. The model is then extended to develop a method to estimate the average number of narrow defects in the layout. Applications of the new method are also presented.

Chapter 2 provides some background knowledge about spot defects, critical area, layout sensitivity to defects, and yield modeling. It also gives an overview of the existing contributions to the stochastic method of yield modeling. In Chapter 3, the stochastic layout sensitivity model is derived, tested and validated. Several innovative and valuable ap-

plications are proposed in the same chapter. “Yield-aware cells placement”, which is another application of the layout sensitivity model, is presented in Chapter 4. Chapter 5 tackles the subject of semiconductor reliability. The chapter emphasizes on the effects of narrow defects on aggravating electromigration that have direct implications on reliability of IC products. In addition, the model predicting the layout sensitivity to narrow defects is derived using the previous model presented in Chapter 3. The model is then validated through testing and comparisons with simulated and actual data extracted from real layouts. Applications of the layout sensitivity model predicting narrows are also proposed in the same chapter.

Chapter 2

Backgrounds and Related Works

This chapter provides some background knowledge and brings in some concepts needed for the understanding of the work presented in this thesis. We define and discuss the subjects of spot defects, critical area, layout sensitivity to defects, and yield modeling. We also discuss the different approaches for yield modeling and give an overview of the existing contributions to the stochastic method of yield modeling.

2.1. Spot Defects and Defect Management

2.1.1. Sources of Spot Defects

Spot defects are mainly caused by: chemical and airborne particles, metallic impurities, and lithography and process imperfections. Chemical or airborne particles with a size of 0.5 to 0.33 of the size of the minimum feature can result in a defective die [9]. Such particles, especially airborne particles, are abundant which makes them a serious concern for semiconductor manufacturability. Metallic impurities originate from the etching involved in many steps of the fabrication process. An example of process imperfection that may cause defect is chemical mechanical planarization (CMP). CMP is a technique performed on the wafer to “planarize” the surface before each step of metal deposition. Because of non-uniform metal density on the wafer, CMP causes metal dishing and erosion [10] which may induce defects at higher metallization layers. Problems with lithography may

also cause defects. The minimum feature size in semiconductors is limited by the resolution of lithography. Specifically, it is proportional to the wavelength of the light source, and, inversely proportional to the aperture of the lens [11], [12]. To reduce costs, it is common to have a minimum feature size smaller than lithography wavelength in today's fabs [13]. This worsens line edge roughness which can induce significant variation to line widths, and may even cause defects. Line edge roughness is expected to be more severe as technology scales down [14]. This is because the minimum feature size is approaching molecular dimensions and scaling of lithography is very likely to be restricted by physical limits and cost constraints [15].

2.1.2. Classification of Spot Defects

Spot defects are classified according to their location, size, and the deformation they induce [16]. The first classification is into intra- and inter-layer defects. Inter-layer defect occurs when the defect is located between two adjacent layers. Intra-layer defects occur when features of a single layer are affected. According to the deformation they cause, spot defects can be also classified into missing and extra material. Based on their size and location, spot defects can be classified into catastrophic and non-catastrophic defects. Catastrophic defects result in immediate circuit failure, i.e., open or short circuit. Whereas, non-catastrophic defects do not affect the functionality of the circuit at fabrication, however, may cause a chip failure during the burn-in process[*] or operation in the

[*] A process of exposing manufactured devices to harsh thermal and electrical stresses in order to reject any device that has escaped previous tests performed under normal conditions.

field. Consequently, catastrophic defects affect the semiconductor yield, while, non-catastrophic defects affect reliability of IC products. Throughout this thesis, inter-layer defects are not considered in the presented analyses. Figure 2.1 illustrates the classification of defects into missing vs. extra material and catastrophic vs. non-catastrophic. In Figure 2.1, defect 1 is an extra material catastrophic defect that causes a short circuit between the two wires. On the other hand, defect 2 is a missing material catastrophic defect that causes an open circuit in the top wire. Defects 3, 4, and 5 are non-catastrophic since they do not induce a circuit failure instantly.

Based on these classifications, we identify three types of spot defects: open, short, and narrow defects.

An open defect or cut is a catastrophic missing material defect. It occurs when a non-

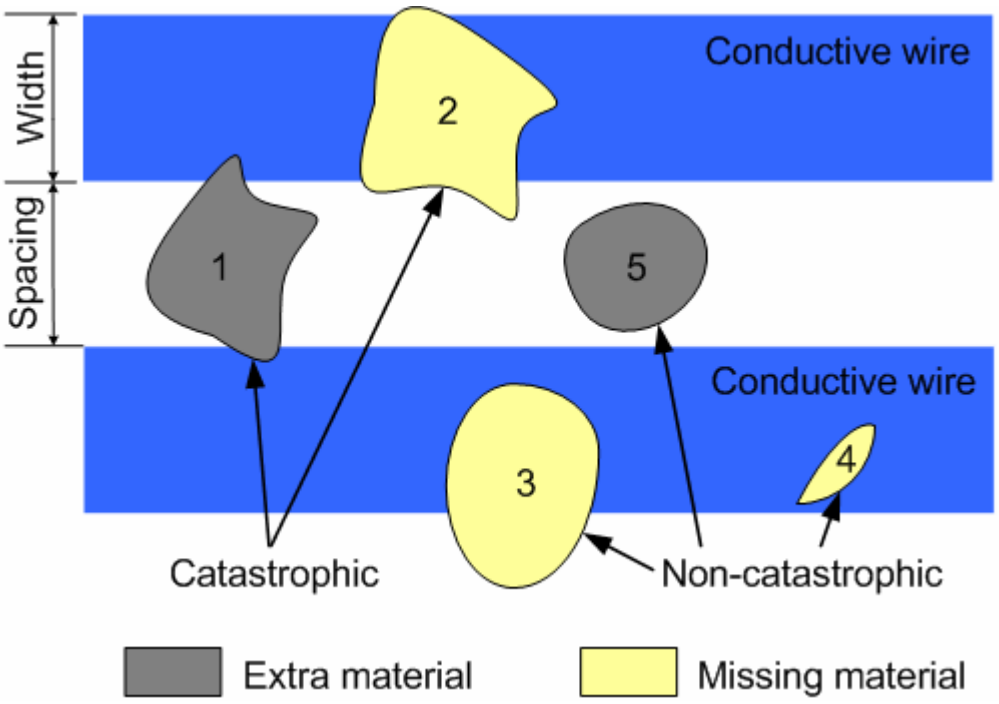


Figure 2.1. Missing vs. extra material and catastrophic vs. non-catastrophic defect classifications.

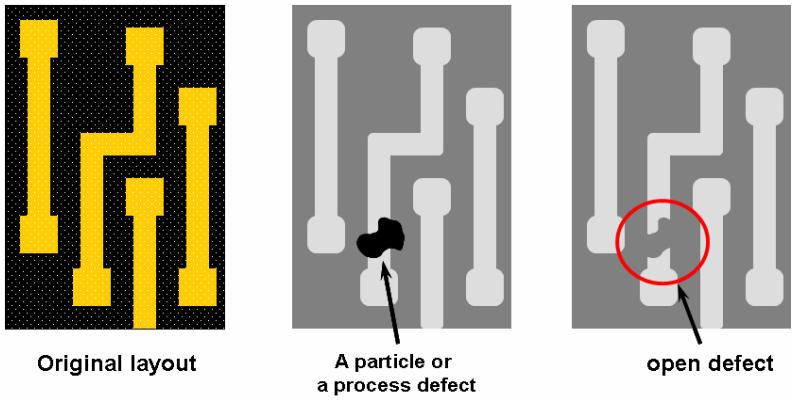


Figure 2.2. Sample of a layout showing an open defect

conductive defect creates an electrical "break" or disconnection in a signal path. Figure 2.2(c) illustrates an example of an open defect for the layout in Figure 2.2(a). Figure 2.2(b) shows the location of a particle or a spot defect that can create such an open failure.

In traditional manufacturing processes, where positive resist was used for lithography, open defects occurred less often. However, in modern damascene processes, the higher probability of failure due to open defects has become a challenging issue [17]. Moreover, open defects are usually complex and hard to diagnose during test procedures [18], [19].

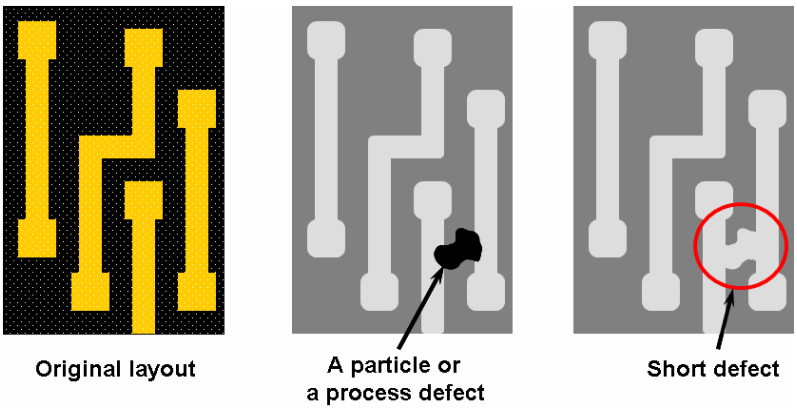


Figure 2.3. Sample of a layout showing a short defect.

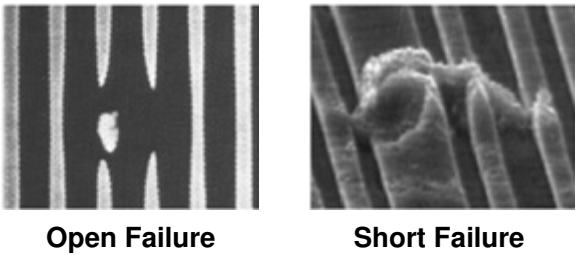


Figure 2.4. Spot defect photographs (Photograph used with permission of *EE Times*, a CMP Media LLC publication) [20].

A short or bridge defect is catastrophic extra material defect. It occurs when a conductive defect creates an electrical connection between two neighboring wires. Figure 2.3(c) illustrates an example of a short defect for the layout in Figure 2.3(a). Figure 2.3(b) shows the location of a particle or a spot defect that can create such a short failure. Figure 2.4 shows photographs of open and short defects in a real manufacturing process [20].

A narrow defect is a non-catastrophic missing material defect. Narrow defect occurs when a non-conductive defect creates a narrow site in a conducting wire without causing an electrical "break" or disconnection in a signal path. The victim conductive wire or interconnect is called "narrow interconnect". Figure 2.5 illustrates an example of a narrow defect.

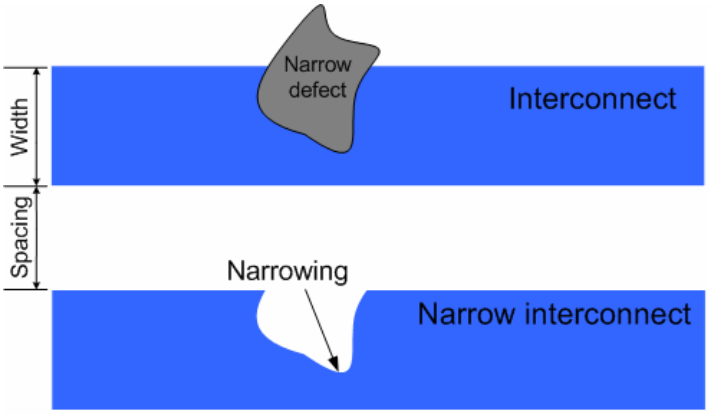


Figure 2.5. Example of a "narrow defect" resulting in the formation of a "narrow interconnect".

2.1.3. Defect Management

Semiconductor manufacturing is very susceptible to spot defects. Hence, defect management is very important to enhance yield and reliability of ICs. Controlling spot defects is a very difficult process. It includes defect inspection, defect classification, and defect management. Defect inspection is performed by scanning the wafer with a bright light or a laser tool to detect defects, followed by a review step executed optically or by scanning electron microscope (SEM) [21]. Another technique for defect inspection is electron beam inspection. This technique is very precise, however, it is very time consuming and extremely expensive which limit its usage in semiconductor fabrication lines. Defect classification is achieved using automatic defect classification (ADC). ADC usually resides on the inspection tool. Defect management consists of different techniques. One method is to reduce the probability of defect occurrence by controlling contamination levels. Semiconductor manufacturers have employed cleanliness techniques in order to reduce the probability of particle deposition, and consequently, increase the manufacturing yield. Specifically, the manufacturing process is performed in clean rooms equipped with high efficiency particle air (HEPA) and ultra low penetration air (ULPA) filters. The filters are capable of eliminating almost every particle in the air larger than a few hundredth of a micron [22]. However particles of smaller size still float abundantly in the fabrication environment. With the ever scaling down of the smallest IC feature size, such tiny particles can cause chip failure. The probability of defect occurrence can also be reduced by controlling defects related to lithography and other process imperfections. For instance, defects due to line edge roughness are reduced as higher resolution lithographic technologies are developed [15], [23].

Another widely used practice to reduce the probability of defect occurrence is design for manufacturability (DFM) techniques. DFM consists of a set of exercises that designers apply to have a manufacturing friendly layout [24]. In essence, as C. Maly *et al*. describes, DFM is the "maximization of manufacturing volume achievable for lowest possible cost" [25]. Here, cost includes execution time, effort spent, and sometimes a reduction in performance. An example of DFM technique is wire spreading. It consists of increasing the separation between neighboring wires if space is available. This method reduces significantly the probability of failure due to defects [26].

2.2. Critical Area and Layout Sensitivity

The term, "critical area", was first introduced by C. Stapper in 1976 [2]. Since then, critical area has become a widely accepted measure of the sensitivity of VLSI design to random defects occurring during the manufacturing process.

By definition, critical area is the area of a layout where the occurrence of a defect would cause a functional failure. Depending on the defect size, there are only certain regions in the layout that the placement of defect could result in a failure. For instance, the region highlighted in Figure 2.6(a) shows the area at which the placement of the center of a defect would cause a short failure. Similarly, the region highlighted in Figure 2.6(b) shows the area at which the placement of the center of a defect would cause an open failure. The area of these highlighted regions is the critical area.

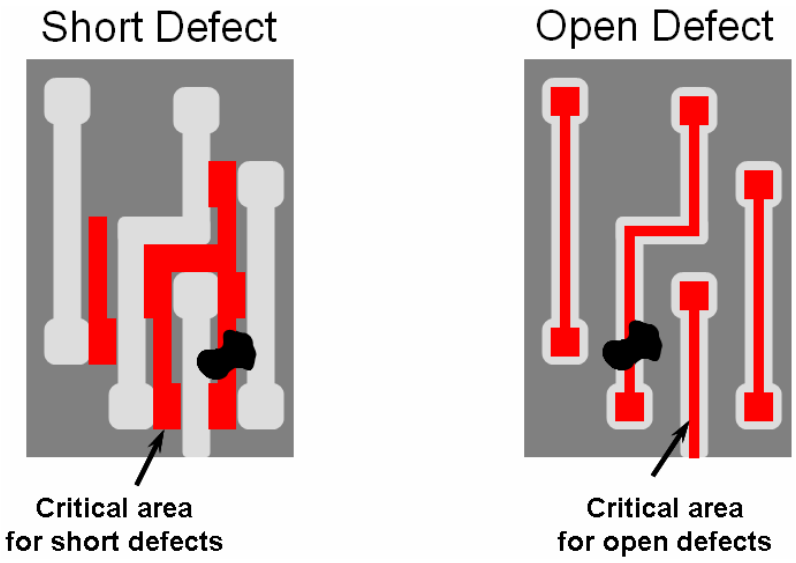


Figure 2.6. Critical area for (a) short defects and (b) open defects.

Critical area depends on the defect size. Larger defect size creates a larger critical area. For instance, the critical area of a very large defect can be the entire layout area if the placement of such defect anywhere on the layout causes a failure. Obviously, the larger the critical area (highlighted regions in Figure 2.6), the more sensitive the layout becomes to the defect.

The layout sensitivity is defined as the ratio of critical area to the layout area. Layout sensitivity, therefore, ranges from 0.0 to 1.0.

To perform yield analysis, the critical area must be computed at each level of metal layer for a range of defect sizes over the entire chip layout. Considering the modern VLSI designs with billions of interconnect segments, this would require an extensive computational effort, including expanding and shrinking polygons and finding overlaps. Performing critical area analysis in today's VLSI designs can easily take several days [6].

2.3. Yield Modeling

2.3.1. Poisson and Negative Binomial Yield Models

Semiconductor production is a long and complex procedure consisting of a series of manufacturing stages. The procedure includes the following consecutive stages: wafer production, device fabrication with lithography, assembly and packaging, and burn-in process and testing. Each stage contributes differently to the overall manufacturing yield which is calculated as follows:

$$Y_{MFT} = Y_{WP} \times Y_{FAB} \times Y_{AP} \times Y_{BI}\,, \tag{2.1}$$

where Y_{MFT} is the manufacturing yield and Y_{WP}, Y_{FAB}, Y_{AP}, and Y_{BI} are, respectively, the wafer production, fabrication, assembly and packaging, and built-in process yields. The major factor affecting the manufacturing yield is the yield of device fabrication. In this thesis, we focus on the device fabrication yield, and yields of all other stages are assumed to be equal to 1. As a result, the manufacturing yield is considered to be equal to the yield of device fabrication stage, and would be denoted by Y throughout the thesis. Based on this assumption semiconductor manufacturing yield is given by:

$$Y = \frac{Average\ \ number\ \ of\ \ \ good\ \ \ chips\ \ \ per\ \ \ wafer}{Total\ \ number\ \ of\ \ \ chips\ \ \ per\ \ \ wafer} \times 100\%\,. \tag{2.2}$$

Studies about spot defects indicate that their sizes follow a specific distribution. A well established probability density function of defect size is of the form [8]:

$$f_s(r) = \begin{cases} \dfrac{2(n-1)r}{(n+1)r_0^2} & 0 \le r \le r_0 \\ \dfrac{2(n-1)r_0^{n-1}}{(n+1)r^n} & r > r_0 \end{cases}, \tag{2.3}$$

where r is the defect size, r_0 is the defect size at the peak density, and n is a parameter that depends on the cleanliness of the fabrication line and is typically equal to 3 [8]. Figure 2.7 depicts the plot of (2.3) for 65 nm technology nodes in a typical fabrication line.

The defect density can be inferred from the probability density function (pdf) of defect sizes as follows:

$$D(r) = D_0 \times f_s(r), \tag{2.4}$$

where D_0 is the average defect density of the die.

The critical area of defect size r for a defect type j, where j is either "open" or "short", is given by:

$$A_{c,j}(r) = S_j(r) \times die\ area, \tag{2.5}$$

where $S_j(r)$ is the sensitivity to defect type j of size r. The average critical area of all defect sizes can be determined by:

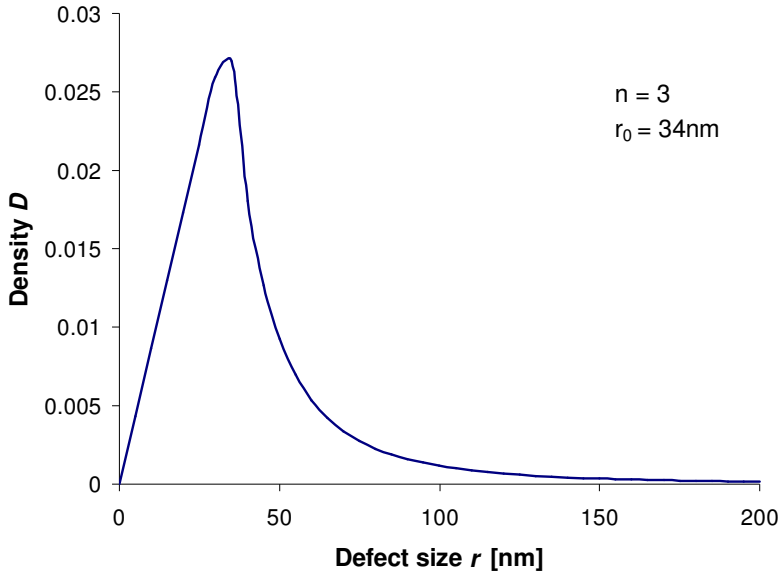


Figure 2.7. Defect size distribution for 65nm technology nodes in a typical fabrication line.

$$A_{c,j} = \int_0^{\infty} A_{c,j}(r) \times f_s(r) \cdot dr \,. \tag{2.6}$$

The average number of defects of type *j*, denoted by λ_j, can be computed using the following equation:

$$\lambda_j = \int_0^{\infty} A_{c,j}(r) \times D(r) \cdot dr$$

$$= D_0 \int_0^{\infty} A_{c,j}(r) \times f_s(r) \cdot dr$$

$$= D_0 A_{c,j} \tag{2.7}$$

Now, the average number of defects, λ, of all types can be expressed as:

$$\lambda = \sum_j D_0 A_{c,j} \tag{2.8}$$

The manufacturing yield due to random defects can be evaluated using the Poisson model as follows:

$$Y_m = e^{-\lambda}, \tag{2.9}$$

where Y_m is the yield for metal layer *m*.

The yield due to random defects of the whole die, *Y*, is given by:

$$Y = \prod_{m=1}^{M} Y_m \,, \tag{2.10}$$

where *M* is the maximum number of metal layers.

The Poisson model is known to give pessimistic results when applied to actual designs. The pessimistic results are caused by the fact that defects tend to group in clusters, and are not assumed to have a uniformly random distribution over the die as in the Poisson

model [16]. The common approach for resolving this issue is by considering the average defect density, λ, as a random variable instead of a constant. In this approach, λ becomes a random variable with values l and a density function $f_\lambda(l)$. Hence, the compounded Poisson yield model is expressed as:

$$Y = \int_0^\infty e^{-l} f_\lambda(l) \cdot dl \,. \tag{2.11}$$

Yield models differs by the choice of the density function, $f_\lambda(l)$, also called *compounder function* [27], [28], [29]. A comparison of yield models is presented in [30] and [31].

The most widely used model is the negative binomial yield model offered in [29]. The model employs a Gamma distribution for the compounder function and is given by [31]:

$$Y = \left(1 + \frac{\lambda}{\alpha}\right)^{-\alpha}, \tag{2.12}$$

where α is the cluster parameter, also called clustering factor, determines the degree of defect clustering. A smaller value of α indicates more clustering. Typical values range between 0.3 and 5 [16], [31]. The International Technology Roadmap for Semiconductor (ITRS)[†] adopts also the negative binomial yield model and uses a cluster parameter of 2 [32].

There are various methods for calculating the critical area. These are examined in the next subsection.

[†] A group of international semiconductor industry experts that forecasts the directions of semiconductor technology and its research requirements in the near- and long-term future

2.3.2. Critical Area Extraction

Critical area has become a widely accepted figure of merit that describes the layout sensitivity to spot defects. Because the manufacturing yield is very dependable on device failure caused by spot defects, critical area analysis is becoming extremely popular and necessary for yield modeling and prediction.

There are different approaches for extracting the critical area from the layout. These can be categorized into four types [33]: Monte Carlo simulation, geometric method, virtual artwork approach, grid method, and the stochastic method.

All the listed methods are based on a critical area analysis except for the Monte Carlo simulation [34] that consists of randomly placing a large number of virtual defects on the layout, and checking for device failure for each defect. The probability of failure is then determined by dividing the number of defects causing a failure by the total number of defects that was placed. This method is only accurate when the number of sampling defects is very large. However, in this case, the simulation takes weeks for large and complex VLSI designs.

An early contribution to the geometric method is offered in [35]. This method is based on the computation of the critical areas for different intervals of defect size. These critical areas are typically computed by applying a shape-contraction on the layout, followed by a shape-expansion, and then a subtraction of the resulting layout from the original one [36]. For instance, considering open defects of size between 50 and 100 nm, all lines less than 50 nm wide are sensitive to such defects. To compute the critical area associated with these defects, we start by applying a shape-contraction by 25 nm of every rectangular shape in the layout. This will erase all lines less than 50 nm wide. Then, we apply a shape

expansion which will restore the original shape of the lines greater than 50 nm wide. And finally, we subtract the area of the resulting layout from the original layout area to obtain area of lines sensitive to the defects i.e. the critical area. The drawback of this method is that is requires huge amount of computations and is very time consuming when applied to modern VLSI designs.

The virtual artwork approach is proposed by W. Maly in [37]. It consists of computing the critical area of a virtual layout, extracted from the original one, that allows an easy determination of a histogram of interconnect widths and spacings as well as the interconnect lengths of specific widths. This approach lacks accuracy especially when applied to complex VLSI designs.

The grid method is proposed in [38]. The critical area is approximated by using a grid over the layout and determining, at every point of the grid, the radius of the smallest defect that causes a failure. The time consumption and accuracy of this method depends on the grid density.

Due to extensive computational requirement in extraction of critical area from the layout, yield modeling approaches becomes inefficient when they require critical area analysis. The stochastic method of yield modeling is a different approach that does not require the analysis of critical area.

2.3.3. Stochastic Method of Yield Modeling

The stochastic method models of the critical area using basic information about the layout. The earliest contribution to this method is offered by C. Stapper in 1983-84 [8], [39].

In his work, C. Stapper used a linear approximation to model the critical area as a function of defect size. His model utilizes basic layout information such as the interconnect widths, spacings, and lengths as well as the total number of interconnects. Another method that uses linear approximation to model the critical area is offered by Ferris-Prahbu in [40]. His model is very similar to Stapper's model but rather decomposes the range of defect sizes into intervals and uses a different linear approximation for each interval. A more recent contribution to the stochastic method is made by P. Christie and J. de Gyvez in [41], where information about interconnect length distribution and interconnect widths were used to model the critical area as a function of the defect size. The stochastic method is not as accurate as yield modeling approaches involving critical area analysis; however, it has very important advantages. In particular, the simplicity of this method in determination of the yield is one important advantage that expedites the yield computation process.

In this work, we develop a stochastic method for critical area analysis by offering an accurate model for predicting the layout sensitivity that can significantly expedite the yield analysis and prediction for current and future complex VLSI designs.

Chapter 3

Yield Prediction Based on a Stochastic Layout Sensitivity Model

3.1. Introduction

In this chapter, we contribute to the stochastic method for critical area analysis by offering an accurate model for predicting the layout sensitivity that can significantly expedite the yield analysis and prediction for current and future complex VLSI designs. The model uses very basic information about the layout. Yet, its outcomes are shown to have good accuracy. The efficiency of the model allows its application to different subjects including: pre-layout yield prediction, yield forecasting and prediction of defect density requirements for future technologies, yield-aware placement and routing tools, and layout diagnosis and yield enhancement.

The model is derived in Section 2. In Section 3, the model is tested and its outcomes are compared to actual layout sensitivity for a modern microprocessor as well as simulated data extracted from real designs. Section 4 proposes several applications of the layout sensitivity model addressing different subjects.

Most of the material presented in this chapter appears also in the published works of [3], [42], and [43].

3.2. Derivation of the Model

3.2.1. Assumptions

Some assumptions are made in order to simplify the derivation of the model. First, we assume that interconnect routing is performed using a grid based approach. The layout grid consists of channels that can be either empty or occupied by interconnects. We also assume that the routing of different interconnects are independent of each other. These assumptions are made without loss of generality of the model since the same assumptions are also made in most yield analysis tools to perform critical area studies.

3.2.2. Parameter Definitions

We define channel density, d, as the probability of a random channel to be filled. Therefore, the probability of a random channel to be empty is given by $(1 - d)$. Channel density, d, can be deduced from the metal density, D, using the following expression:

$$D = d\frac{w}{w+s}, \tag{3.1}$$

where w and s are the interconnect width and spacing respectively.

Since w and s are preset by the fabrication technology and D can be easily computed from the layout, the channel density is easily determined.

Also, we define m as the number of channels covered by a defect and r as the defect size.

3.2.3. Layout Sensitivity Model for Open Defects

For the derivation of the layout sensitivity for open defects, we consider a defect of size:

$$r = m(w+s)+w-\varepsilon\,, \tag{3.2}$$

where ε is an infinitesimal distance. ε is included in (3.2) to make sure that exactly m channels can contribute to an open defect in case it occurs. This is illustrated by Figure 3.1 where $m=2$. All m consecutive channels must be empty for the device to overcome the defect. Therefore, the probability of the device survival is

$$P_s = (1-d)^m. \tag{3.3}$$

Consequently, the probability of the device failure is given by:

$$P_f = 1-P_s = 1-(1-d)^m. \tag{3.4}$$

The layout sensitivity to open defects is in fact the probability of failure due to an open defect. Hence, by substituting m in (3.4) by its value from (3.2) and neglecting ε, the layout sensitivity model for opens becomes:

$$S_{open} = 1-(1-d)^{(r-w)/(w+s)}. \tag{3.5}$$

This model for layout sensitivity to open defects uses very basic layout information i.e. defect size r, wire width w, wire spacing s, and the channel density d.

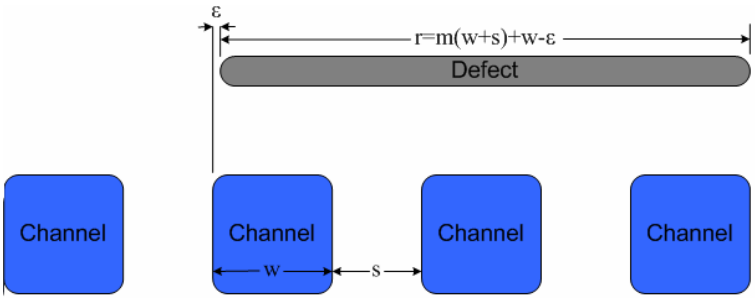


Figure 3.1. An example of an open defect covering 2 channels.

3.2.4. Layout Sensitivity Model for Short Defects

For the derivation of the layout sensitivity for short defects, we consider a defect of size:

$$r = m(w+s) - w - \varepsilon\,, \tag{3.6}$$

where ε is an infinitesimal distance. ε is included in (3.6) to make sure that exactly m channels can contribute to a short defect in case it occurs. This is illustrated by Figure 3.2 where $m = 2$. For the device to overcome the defect, either all m consecutive channels must be empty, or *only one* channel is filled and the remaining channels are empty since a defect involving a single interconnect cannot create a short circuit.

The probability of having m consecutive empty channels, P_1, is

$$P_1 = (1-d)^m\,, \tag{3.7}$$

and the probability of having one filled channel and m-1 empty channel, P_2, is

$$P_2 = md(1-d)^{m-1}\,, \tag{3.8}$$

where the coefficient m accounts for arbitrary location of the filled channel in m different positions. Consequently, the probability of the device survival is given by:

$$P_s = P_1 + P_2 = (1-d)^m + md(1-d)^{m-1}\,, \tag{3.9}$$

and the probability of failure, P_f, is then:

$$P_f = 1 - P_s = 1 - (1-d)^m - md(1-d)^{m-1}\,. \tag{3.10}$$

It can be also written as:

$$P_f = 1 - \left[1 + (m-1)\cdot d\right]\cdot(1-d)^{m-1}\,. \tag{3.11}$$

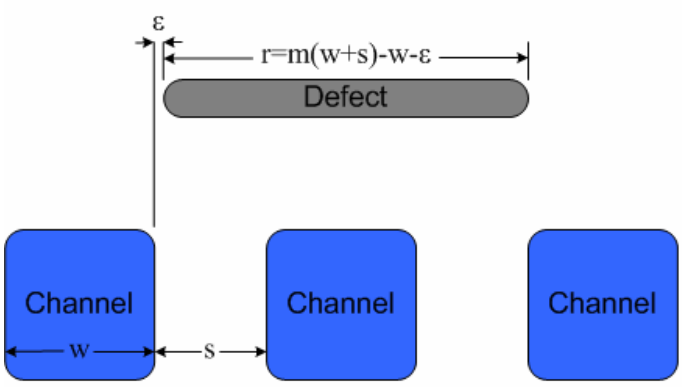


Figure 3.2. An example of a short defect covering 2 channels.

The layout sensitivity to short defects is in fact the probability of failure due to a short defect. Hence, by substituting *m* in (3.11) by its value from (3.6) and neglecting *ε*, the layout sensitivity model for shorts becomes:

$$S_{short} = 1 - \left[1 + \left(\frac{r-s}{w+s}\right) \cdot d\right] \cdot (1-d)^{(r-s)/(w+s)} \tag{3.12}$$

This model for layout sensitivity to short defects uses very basic layout information i.e. defect size *r*, wire width *w*, wire spacing *s*, and the channel density *d*.

3.3. Results and comparison with measured data

The sensitivity model for short and open defects was tested for 0.32µm technology node with an interconnect density of 0.6. Figure 3.3 and Figure 3.4 shows the result of testing the layout sensitivity model for open and short defects respectively, and a comparison with the sensitivity extracted from an actual layout as well as the previous stochastic model offered in [41]. The average percent errors of the model's outcomes when

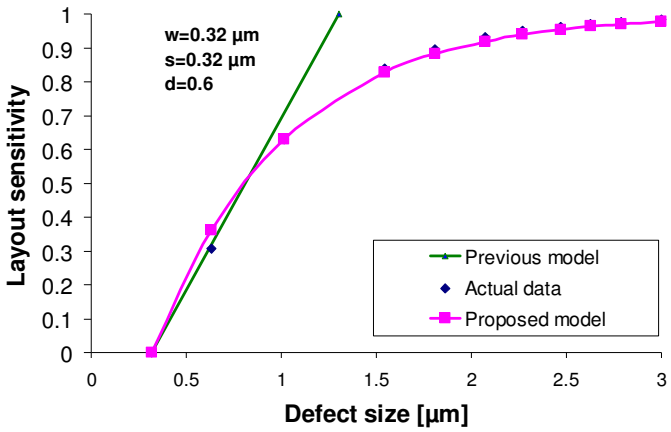


Figure 3.3. Comparison of the proposed sensitivity model with extracted layout sensitivity and a previous sensitivity model [41] for open defects.

compared to actual data was found to be 2.4% for opens and 6.2% for shorts, which is an indication of the high fidelity of the model. The sensitivity model for shorts was again tested for 1µm technology node and compared in Figure 3.5 to actual data extracted from a microprocessor design [44]. In the plots of Figure 3.5, $w = s = 1\mu m$ for all metal layers, and d = 0.3, 0.15, 0.12 and 0.09 for metal layers M2, M3, M4, and M5 respectively. The

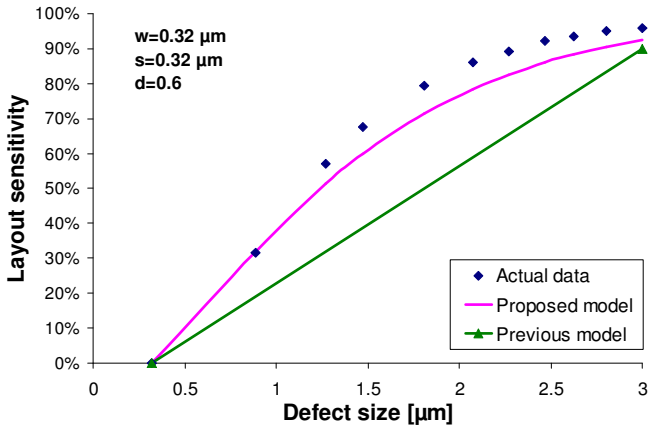


Figure 3.4. Comparison of the proposed sensitivity model with extracted layout sensitivity and a previous sensitivity model [41] for short defects.

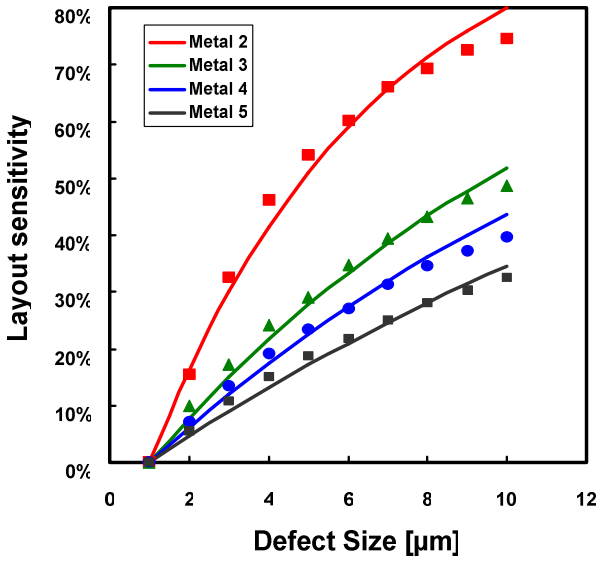


Figure 3.5. Comparison of the proposed model with layout sensitivity for shorts extracted from a real micro-processor chip [44].

channel densities for the different metal layers were chosen to have the best fit of the model to the extracted data. This was done because of the absence of information about the channel or metal densities for the data in [44].

The sensitivity model for short and open defects was also tested on actual designs with a 45nm technology node. This is performed using PRS, a placement and routing software previously developed in [45]. PRS is used to create the layout of a small circuit (52 logic gates) that computes the absolute value of the difference between two 2-bit numbers. The channel density is then extracted from the layout and provided to the predictive model for shorts and opens. Results were compared then to the outcomes of simulations. These simulations were performed by expanding PRS tool to generate defects and check for the resulting open (or short) circuits. A large number of defects with different sizes (100,000 defects per defect size) are randomly placed on the layout and the number of resulting opens (or shorts) for a single metal layer is determined. The probability of failure associ-

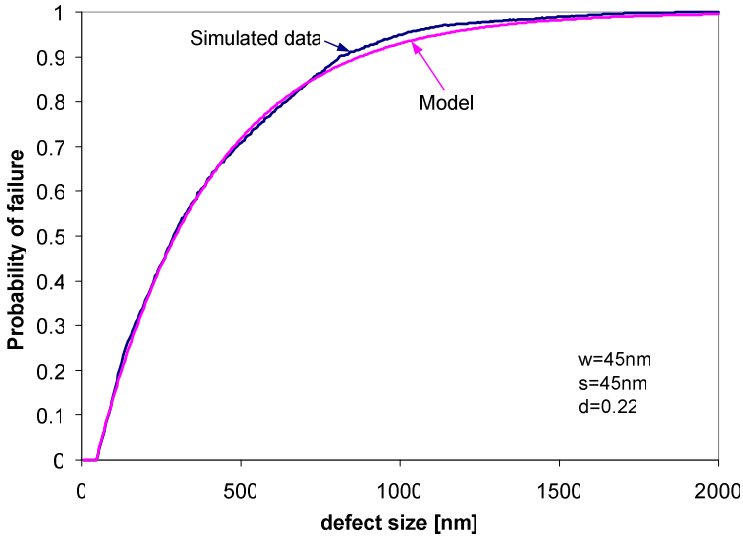


Figure 3.6. Comparison between the probability of failure estimated by the layout sensitivity model for open defects and probability of failure due to open defects extracted from an actual design.

ated with each defect size is then obtained by the ratio of the total number of resulting opens (or shorts) to the total number of generated defects for each defect size. Figure 3.6 and Figure 3.7 present comparisons between the simulated and predicted probabilities of failure of open and short defects, respectively, for different defect sizes. Results show the

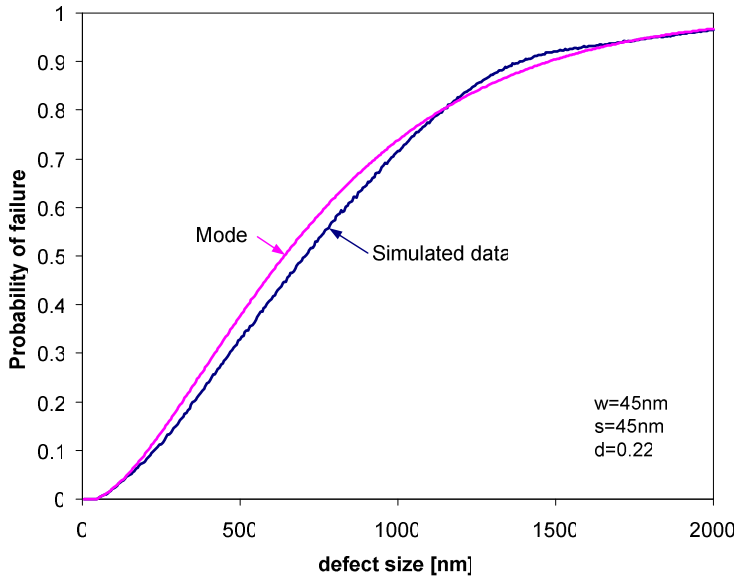


Figure 3.7. Comparison between probability of failure estimated by the layout sensitivity model for short defects and probability of failure due to short defects extracted from an actual design.

accuracy of the model in predicting open and short defects i.e. 1.4% error for opens and 6.2% for shorts.

3.4. Applications

3.4.1. Pre-Layout Yield Estimation

The layout sensitivity to spot defects can be predicted using the model presented in this paper. The only unknown variable in the model is the channel density *d* which can be inferred from the metal density *D* using (3.1). The metal density is usually available through post-layout extraction tools for use in other applications such as metal thickness variation analysis. In case the metal density is not available, it can be calculated from the layout using information about interconnects length. The metal density can also be estimated even before coming up with the actual layout. Specifically, this can be performed for designs that belong to a family of products using statistical information. Also, the metal density can be predicted using a heuristic approach [46] based on an estimation of interconnect length distribution derived in [47]. Consequently, implementation of the model to predict the layout sensitivity of a product becomes very easy and can be done even before starting the design phase. Since the layout sensitivity to spot defects is defined as the ratio of critical area to the overall layout area, the yield can be estimated using any of the existing yield models that are based on a critical area analysis [48].

It is very important to be able to predict if a design meets the acceptable device yield at a very early stage. This will ensure that the design decisions, such as number of metal layers, are made such that the layout meets the yield requirement after the design comple-

tion. This reduces the time consuming application of post-layout modifications such as design for manufacturability (DFM) techniques and wire spreading [20], since the layout sensitivity is considered at early phase of design cycle. Post-layout modification procedures are necessary for achieving acceptable yield [49], especially when the yield enhancement faces non-stopping challenges as the number of transistors per die is exponentially growing and the minimum feature size in semiconductor fabrication is exponentially scaling down.

3.4.2. Yield Forecasting for Future Technologies

As discussed in Chapter 2, it has been verified that spot defects follow a specific distribution based on their sizes. A widely acceptable pdf of the defect size distribution is given by (2.3). For the convenience of the reader, this pdf is repeated once again:

$$f_s(r) = \begin{cases} \dfrac{2(n-1)r}{(n+1)r_0^2} & 0 \le r \le r_0 \\ \dfrac{2(n-1)r_0^{n-1}}{(n+1)r^n} & r > r_0 \end{cases}, \tag{3.13}$$

where r is the defect size, r_0 is critical defect size, i.e., the defect size with the peak density, and n is a parameter that depends on the cleanliness of fabrication line. As long as a manufacturer is employing the same cleanliness standards, n remains constant independent of the fabrication process technology. For a specific fabrication line, the value of n is easily determined from data of previously manufactured products. Values of n ranges between 2 and 4, and is approximated to 3 for a typical fabrication line [1]. Experimental results show that the critical defect size r_0 is less than the minimum lithographic feature

[1], [32]. According to the International Technology Roadmap for Semiconductor (ITRS), r_0 is expected to represent a certain fixed percentage, around 80%, of the minimum lithographic feature at least for the next decade [32]. Hence, the defect size distribution can be accurately estimated for future technologies. Figure 3.8 depicts the plot of (3.12) for 90, 68, 45, 32, and 22 nm technology nodes in a typical fabrication line, i.e. n=3, and where r_0 are chosen in accordance with the ITRS [32].

Section 2.3.1 showed how to determine the manufacturing yield using the defect size distribution. To forecast the manufacturing yield for future process technology, two more quantities need to be estimated: the average defect density D_0, and the average critical area A_c for all types of defects. D_0 rarely changes with the advent of technology. According to ITRS, D_0 is expected to remain unchanged until 14 nm technology node is achieved in the year 2020 [32]. The layout sensitivity model proposed in this chapter can be used to predict the sensitivity to defects. Consequently, the critical area for future technology nodes is inferred using (2.5). This possible because the total chip area, typically, remains constant for several consecutive technologies. The only missing parameter

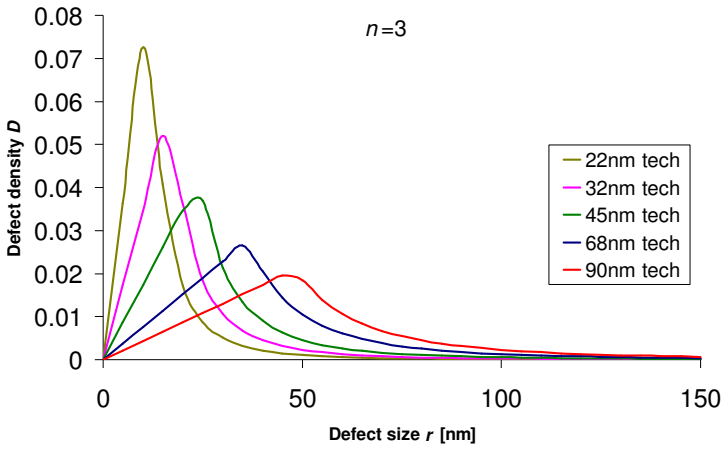


Figure 3.8. Defect size distribution for 90, 68, 45, 32, and 22nm technology nodes in a typical fabrication line.

in order to apply the model is the channel density *d*. Again, *d* depends mostly on the routing efficiency and the architecture of the design but not on the process technology. For a specific design, *d* can be approximated to the channel density at the current technology node. The procedure to determine the manufacturing yield presented in Section 2.3 can now be performed with no difficulty. Hence, yield forecasting for future technologies can be performed once an accurate estimate of either the channel density *d* or the metal density *D* (refer to (3.1)) is available.

3.4.3. Predicting Defect Density Requirements for Sub-45nm Technologies

The proposed layout sensitivity model is applied to a fictitious design with 90, 68, 45, 32, and 22 nm technology nodes. The channel density is chosen to be the same for all metal layers and is equal to 0.6. The technology nodes, and therefore interconnect width *w* and spacing *s*, as well as the maximum number of metal layers and the number of metal layer per tier were chosen in accordance with ITRS [32] (refer to TABLE 3.1). The normalized layout sensitivities to spot defects associated with the different technology nodes are

TABLE 3.1. PARAMETERS USED IN COMING UP WITH THE RESULTS OF THIS SUBSECTION

Technology node [nm]	90	68	45	32	22
***w* & *s* for local wires [nm]**	90	68	45	32	22
***w* & *s* for semi-global wires [nm]**	200	140	90	64	44
***w* & *s* for global wires [nm]**	300	210	135	96	66
r_0 [nm]	45	34	22.5	16	11.5
Chip size [mm^2]	111	n/a	140	n/a	140
Number of metal layers	11	11	12	13	13
Number of metal layers for local/semi-global/global tiers	4/4/3	4/4/3	4/4/4	5/4/4	5/4/4
Channel density for all metal layers	0.6	0.6	0.6	0.6	0.6

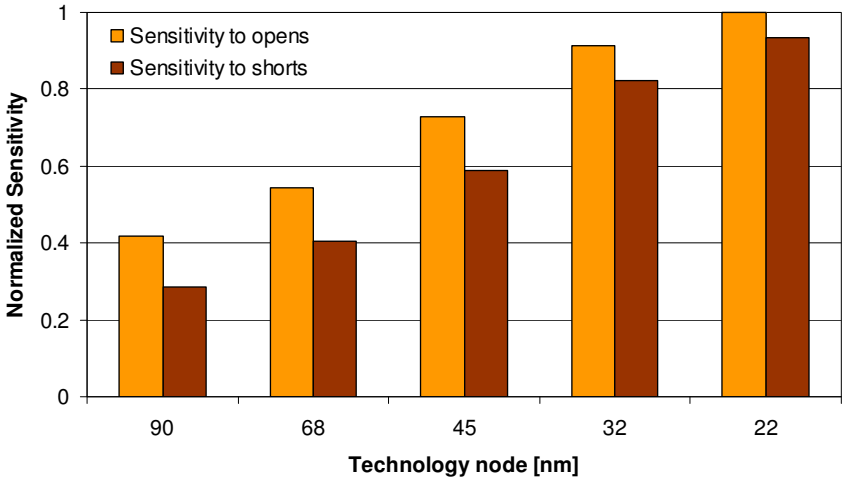


Figure 3.9. Normalized sensitivity to open and short defects of a fictitious layout with 90nm, 65nm, 45nm, and 32nm technology nodes.

shown in Figure 3.9.

The chart of Figure 3.9 shows that the layout sensitivity to defects almost doubles every 3 technology generations. And because the manufacturing yield is directly dependent on the sensitivity to defects and defect density, then reduction in defect density is necessary in order to achieve acceptable yield for sub-45nm technologies. This is achieved by defect reduction in process equipment that remains paramount to achieving defect density goals.

The procedure for setting requirements of defect density for future technologies is illustrated by a case study for some current and future technology nodes. We start by determining the critical area using (2.6). To do this, the critical defect size, r_0, for which the defect size distribution peaks, is required. This parameter can be easily estimated because its scaling is uniform as technology node scales down. By applying the procedure of Section 2.3.1, we determine the manufacturing yield associated with the av-

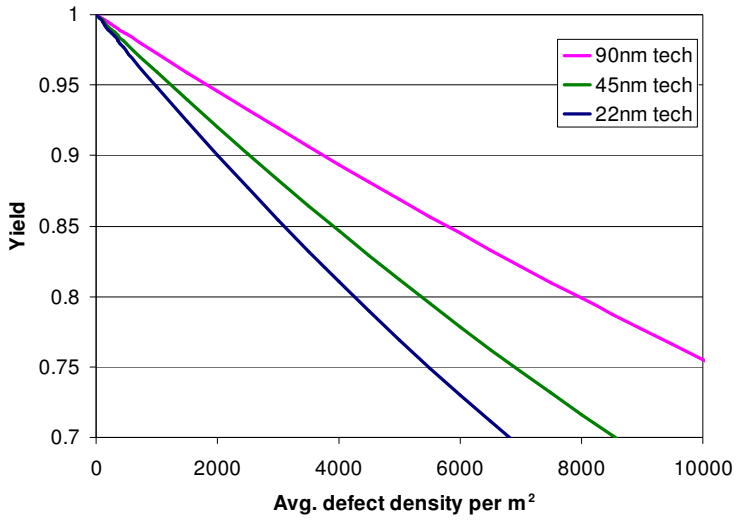
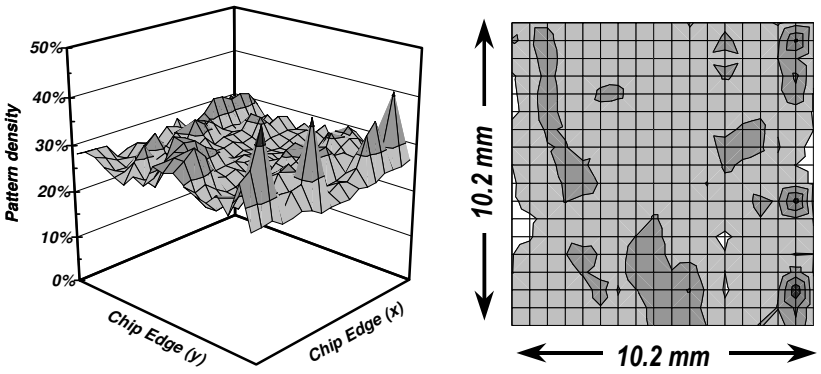


Figure 3.10. Plot of manufacturing yield as a function of average defect density for 90, 45, and 22nm technology nodes.

erage defect density for different technology nodes. The chip area is required for that. So, it was chosen in accordance with ITRS. TABLE 3.1 summarizes all parameters used to come up with the results shown in this subsection. Figure 3.10 plots the manufacturing yield versus the average defect density for 90, 45, and 22nm technology nodes. Now, requirements of the defect density can be set according to the targeted yield. For instance, if the minimum acceptable yield is 90%, then the minimum average defect density is 3800, 2500, and 2000 faults/m^2 for 90, 45, and 22nm technology nodes respectively.

3.4.4. Layout Diagnosis and Yield Enhancement

Layout modification techniques for yield enhancement, such as wire spreading and nets re-routing, are extremely time-consuming if applied to the entire layout. The layout sensitivity model offers a solution for this problem. In particular, the layout sensitivity of the different parts of the circuit can be determined using the model. Then, layout sensitivity



(a) (b)

Figure 3.11. Pattern density distribution in 3D (a), and in 2D (b).

patterns can be generated and only the parts having a high sensitivity to spot defects are marked for diagnosis and application of layout modifications for yield enhancement. An example is illustrated in Figure 3.11 and Figure 3.12. Figure 3.11 shows the metal density patterns extracted from a real design using *Quickcap* tool [70]. Figure 3.12 shows the layout sensitivity patterns inferred from the metal density patterns of Figure 3.11 using the layout sensitivity model.

Traditionally, the layout sensitivity is determined using post-layout extraction tools.

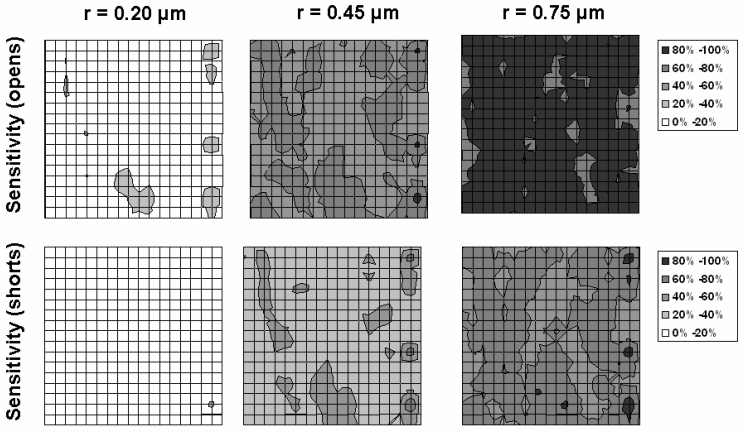


Figure 3.12. Layout sensitivity patterns in a real design using the proposed layout sensitivity model i.e. equations (3.5) and (3.12).

This is extremely time-consuming since it requires performing expansion, shrinkage, and overlap of polygons, where there exists billions of interconnect segments (polygons) on the chip. Moreover, it must be performed for a range of defect sizes and at each metal level. Typically, computation of the sensitivity of the entire layout of a modern VLSI design takes several days [41]. On the other hand, the process becomes efficient when the layout sensitivity is estimated using the accurate and extremely fast model described in this paper.

Yield enhancement can also be performed during the placement of cells as it will be demonstrated in Chapter 4. This is another important application of layout sensitivity model.

Chapter 4

Yield-Aware Automatic Cells Placement

4.1. Introduction

The usage of tools performing an automatic placement of cells and routing of nets is essential in most modern VLSI designs. Moreover, designs are expected to be more dependable on such tools as functionality and complexity of designs become more important [50]. The primary objectives of most placement and routing algorithms are to minimize the total wire length and layout area. Some other placement and routing algorithms have the objective of minimizing the delay of critical paths in order to increase performance. These are called performance driven algorithms [51].

The move to advanced nanometer nodes and new process materials is diminishing semiconductor designer's ability to estimate and realize device yields. As a result, yield enhancement is becoming evermore dependent on the design, not just improvement of the manufacturing process. One method proposed in [52] consists of increasing the robustness of the design by performing some minor modifications to the layout. Such modifications include: addition of redundant vias and increase of via size to increase the chances of maintaining a connected signal path, wire spreading that consists of increasing the separation between neighboring wires if space is available to reduce the probability of short defects, and wire widening if space is available to reduce the probability of open defects. Another layout modification technique consists of adding redundant interconnects as backup of the original ones [53]. Experimental results in [53], [54], [55], and [56]

shows that layout modification techniques can significantly improve the manufacturing yield. Automatic CAD tools that perform the discussed layout modifications are also available. Examples of such tools are presented in [57], [58], and [59].

Several efforts to consider reduction of yield loss at routing stage were reported in [60], [61], [62], [63], and [64]. The first automatic router to optimize yield loss due to spot defects was offered in [64]. An attempt to optimize the yield at the floorplanning stage is presented in [65] and [66]. In year 2000, the first and only attempt to incorporate the optimization of yield loss due to spot defects at the cell placement stage was reported in [67]. However, the proposed methodology is inefficient which prevented its application and development. This attempt is discussed thoroughly later in this paper.

In essence, reducing yield loss due to spot defects by applying layout modifications and using routing algorithms that takes yield into consideration has succeeded to a great extend. Yet, yield enhancement brought by these techniques is constrained by a fixed cells placement. This limitation gives motivations for efficiently incorporating yield loss optimization at the cells placement stage. In this paper, we offer a yield-aware automatic cell placement tool that optimizes the placement of cells to have a minimal layout area and wire length, while taking yield into consideration in doing so. The yield-awareness of the tool is possible because of the use of the recently developed layout sensitivity model of Chapter 3 that can predict the yield with a reasonable accuracy before performing the actual routing.

In Section 2, a methodology for incorporating yield loss optimization in conventional cell placement tools is proposed. An actual implementation on conventional automatic cell placement tool is presented in Section 3. The outcomes of the original placement tool

are compared to the outcomes of the yield-aware version of the tool in Section 4. In Section 5, a detailed comparison of the implemented yield-aware cell placement tool with a similar tool developed earlier is performed.

4.2. Methodology for Yield Enhancement during Cells Placement

4.2.1. Critical Area Optimization

Cell placement algorithms can be classified into constructive and iterative placement. Constructive placement algorithms are much faster than iterative algorithms, however, the former lead, in general, to poorer quality layouts. This allowed iterative placement algorithms to be more popular. Also, a combination of both algorithms is very much in use. Combinatorial algorithm starts with an initial constructive placement and then performing iterative placement improvements. We will focus in this paper on including yield loss optimization in iterative placement algorithms that will allow yield enhancement in most placement tools.

Conventional automatic cell placement tools minimize a certain cost or objective function. This function consists of the total estimated wire length and various penalties such as the layout area and some design violations [68]. In some cases, the layout area is predetermined and the placement tool would only have to minimize the wire length while making sure the layout area is not violated. Nevertheless, the optimization of placement tools is not limited to the minimization of total wire length. As a result, the optimal solution of the objective function does not necessarily have an optimal yield. It is true that the optimization of the yield is very dependent on the optimization of the total wire length,

because, a smaller wire length lead to a smaller critical area for opens defect, which is at least 3 times higher than the critical area for short defects [1], and would practically determine the yield. Yet, the yield of distinct placements can be very different from the associated cost function. Hence, manufacturing yield is not taken into consideration by conventional cell placement algorithms.

We believe that yield-aware cell placement can lead to better optimal solutions. To prove our point of view, we have performed several runs of a non-deterministic standard cell placement tool on a real design with 52 cells and compared the solutions found at each run. The tool, which is called PRS, was developed in a previous work [45]. Figure 4.1 plots the normalized cost function as well as the normalized critical area of the different solutions.

The plots of Figure 4.1 show that the critical area, and consequently the yield, is somehow independent from the cost of the different solutions. Moreover, the plots prove that, by optimizing just the cost function, the placement algorithm is prevented from possibly reaching better solutions for yield. This is illustrated by some examples. In Figure 4.1,

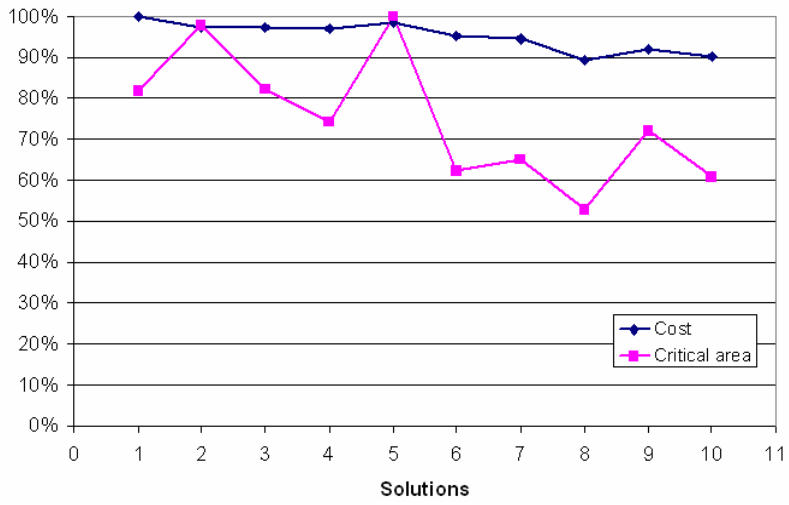


Figure 4.1. Comparison of normalized costs and critical areas of different solutions found by PRS

solutions 2, 3, and 4 have the same cost, yet, solution 3 has a smaller critical area than solution 2 and solution 4 has the least critical area. A conventional cell placement tool such as PRS cannot distinguish the difference between the three solutions and may lead to the solution with the worst critical area among all areas. Besides, solution 2 of Figure 4.1 has a slightly better cost than solution 1, but also, solution 2 has a much worse critical area than solution 1. In practice, solution 1 may be more desired than solution 2 which will be chosen by conventional cell placement algorithm as the optimal solution, where the cost is the only objective.

We propose a method to incorporate yield enhancement into cell placement algorithms. In this new algorithm, which is based on simulated annealing, once a new solution is found, the critical area for that solution is predicted. For the new solution to be accepted, one of the following two conditions has to be met. 1) The first condition is to have a new solution with a cost better than the cost of the optimal solution achieved so far, and also, the critical area penalty in the new solution must not exceed the benefit of cost. 2) The second condition is to have a new solution with a cost worse than the cost of the optimal solution achieved so far, and also, the critical area benefit in the new solution must exceed the penalty of cost. If any of the two conditions is not met, then the new solution is rejected. Specifically, this is described by the pseudo-code of Figure 4.2. In this pseudo-code, *Temp* stands for *Temporary* and denotes the new solution, *Best* denotes the optimal solution achieved so far, *Cost( )* is a function that evaluates the cost of a particular solution, $A_c( )$ is a function that evaluates the critical area of a particular solution, and β is a parameter that describe how important the yield optimization is compared to the optimization of the cost function. The choice of β is straight forward and is independent

1 If $(Cost(Temp) < Cost(Best)$ and $\beta \times \frac{Cost(Best) - Cost(Temp)}{Cost(Best)} > \frac{A_c(Temp) - A_c(Best)}{A_c(Best)})$

or $(Cost(Temp) > Cost(Best)$ and $\frac{A_c(Best) - A_c(Temp)}{A_c(Best)} > \beta \times \frac{Cost(Temp) - Cost(Best)}{Cost(Best)})$

2 $Best = Temp$ *//New solution accepted*

3 else

4 Reject($Temp$) *//New solution rejected*

Figure 4.2. Pseudo-code for including yield optimization during placement of cells

of the design. For $\beta = 1$, both optimizations have the same importance. $\beta > 1$ gives preference of optimization of cost function over optimization of the yield. $\beta < 1$ gives preference of optimization of yield over optimization of the cost function. In most cases, the optimization of total wire length and layout area is more important than the optimization of yield. Any choice of $\beta > 3$ does not affect the optimization of total wire length and layout area significantly.

Such placement algorithm still optimizes the cost function. Here, yield enhancement is performed in two ways. First, the algorithm will avoid accepting solutions that have a slight benefit in cost, but, have a large penalty in critical area. This is guaranteed by the first condition of the "If statement" at line 1 of the algorithm. Second, the algorithm will allow a solution having a much better critical area and a relatively small penalty in cost. This is assured by the second condition of the "If statement" at line 1 of the algorithm.

The challenge of this method is to predict the critical area at an early stage of the design phase, and specifically, before interconnect routing. The recently developed layout sensitivity model of Chapter 3 was shown to accurately predict the layout sensitivity to

defects. The critical area is easily deduced from the layout sensitivity using the following equation:

$$S = \frac{A_c}{A}. \tag{4.1}$$

The model requires some basic information about the layout including wire width, *w*, wire spacing, *s*, and the channel density, *d*. Wire width and spacing being set by the manufacturing process technology, the problem is cut down to estimating the channel density. Accurate yield prediction requires accurate channel density estimation.

Channel density, *d*, can be estimated using statistical data for designs belonging to the same family of the processed design. In case this statistical data are not available or cannot result in accurate estimations of *d*, then the channel d is estimated as follows.

Channel density, *d,* can be deduced from the metal computed, *D,* using the following expression:

$$d = \left(\frac{w+s}{w} \right) \times D. \tag{4.2}$$

D is determined as follows:

$$D = \frac{L \times w}{A}, \tag{4.3}$$

where *L* is the total wire length and *A* is the overall layout area. At this stage, the area of cells is available. So, estimation of *A* is reduced to estimation of the area of the routing channels. The area of a routing channel *i* is given by:

$$A_{r,i} = H_i \times L_{c,i}, \tag{4.4}$$

where $A_{r,i}$ is the area, H_i is the height, and $L_{c,i}$ is the length of routing channel *i*. L_i is automatically determined from the placement of cells. H_i is computed as follows:

$$H_i = N_{T,i} \times (w + s) + s, \tag{4.5}$$

where $N_{T,i}$ is the number of tracks in the channel. $N_{T,i}$ can be statistically related to the number of nets in channel i. Specifically, the number of tracks per channel increases monotonically with the number of nets in the channel. When the number of channel in the design is considerably large, this increase can be assumed to be linear for a particular router with a constant slope, γ. Hence, γ of a particular router is approximated to the average ratio of number of tracks to the number of nets per channel for previously generated layouts. Therefore, $N_{T,i}$ is approximated to the number of nets to be routed in channel i multiplied by γ.

Now that we have determined a method for estimating the area of the layout A, estimation of the channel density still requires the approximation of the total wire length L for each metallization layer. Based on Rent's rule, the interconnect density function (idf) of the design can be determined using the model offered in [47]. This model allows accurate pre-layout estimation of the idf, and, in doing so, requires some basic information about the layout including the number of cells, Rent's parameters, and the average fan-out. Once the placement is performed, the number of cells is known, Rent's parameters are almost constant for similar types of design or family of designs, and the average fan-out can be predicted before the routing using the model developed in [69] which requires no extra parameters. Each net is considered to be composed of a vertical and a horizontal wire. Using the semi-perimeter method, lengths of vertical and horizontal wires are estimated. All wires are then assigned to the different metal layers based on their lengths and the idf. In general, each metal layer contains wires of specific lengths belonging to a predetermined range. Wire length ranges of metal layers are easily calculated using the lay

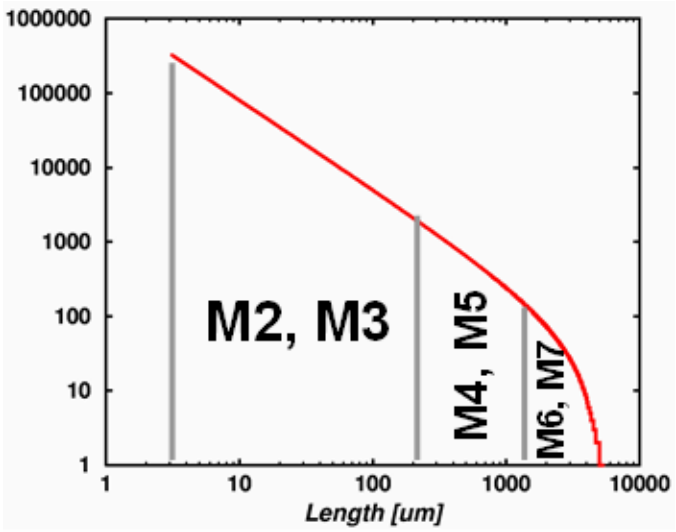


Figure 4.3. idf for a real design of 75 million gates and 55.6 million nets and metal layer allocation based on wire lengths.

out area, *A*, and the routing efficiency. This is illustrated in Figure 4.3. This figure shows the idf of a design with 75 million gates and 55.6 million nets as well as metal layer allocation based on wire lengths. TABLE 4.1 shows the exact values of wire length ranges associated with metal layers for the same design used in Figure 4.3.

Yield-aware automatic placement tools are expected to be more time-consuming then conventional ones because of the added steps of predicting the critical area at every iteration in yield-aware placement tools. However, the additional time is expected not to be significant because of the usage of the efficient stochastic layout sensitivity model in predicting the critical area.

TABLE 4.1. WIRE LENGTH RANGES ASSOCIATED WITH METAL LAYERS FOR THE SAME DESIGN USED IN Figure 4.3.

Metal layer	Minimum length [µm]	Maximum length [µm]
M2/M3	1.14	102
M4/M5	102	557
M6/M7	557	5100

4.2.2. Avoiding Yield-Violating Layouts

Another benefit of yield-aware cell placement tools is that they can be used to avoid placements that violate the yield requirements. In fact, if a layout violates the yield requirement, the design may not meet its cost objective. It would be beneficial for the designer to know this information at an early stage so that he can find solutions to enhance the yield before proceeding with following time-consuming and costly stages of redesign. This is implemented in cell placement tools as follows. Once the tool has determined the optimal final solution, the critical area of the final placement is predicted using the method discussed earlier. The predicted critical area is compared to the targeted one. If the critical area of the solution is larger than the required critical area, then the placement cannot lead to a layout that meets the yield requirement. At this stage, either the whole cell placement is repeated, or the tool is forced to run for more iterations in order to find a placement that meets the yield requirements. If again the tool cannot find a solution that meets the yield requirement, then the designer may decide to modify some design parameters, such as number of metal layers, wiring density, wiring width and spacing, before routing to make sure the design meets its cost objectives.

4.3. Actual Implementation of a Yield-Aware Automatic Cell Placement Tool

Actual implementation of yield-aware automatic cells placement is performed on PRS, which is a conventional placement and routing software developed in a previous work [45]. PRS is presented a set of standard cells and a net list. The tool generates the layout

by placing the cells in rows and routing nets while minimizing overall layout area and total wire length. PRS uses three metal layers: two for horizontal wires and one, which is metal layer 2, for vertical wires. PRS uses an iterative approach for cells placement. It starts with an initial non-optimized placement and applies iterative cell displacements using a simulated annealing algorithm. The pseudo-code of the simulated annealing algorithm of PRS is shown in Figure 4.4.

The algorithm minimizes a cost, or objective, function that depends on the total wire length and the layout area. A placement perturbation, or cell displacement, is performed at every iteration using the function *PerturbPlacement*. The resulting placement is referred to as *Temporary* placement. The cost of the *Temporary* placement, given by the function *Cost(Temporary)*, is then compared to the optimal placement ever achieved referred to as the *Best* placement. If *Temporary* placement has a better cost compared to *Best* placement, then *Best* placement is set to *Temporary* placement. In case

```
1    Alfa = InitialAlfa
2    Time = InitialTime
3    Temperature = InitialTemperature
4    Best = InitialPlacement
5
6    while Time>0
7        Current = Best
8        for M=InitialM, M>0, M--
9            Temporary = PerturbPlacement(Current)
10           if Cost(Temporary) < Cost(Current)
11               Current = Temporary
12               if Cost(Temporary) < Cost(Best)
13                   Best = Temporary
                                  _ (Cost(Temporary)−Cost(Current)) / Temperature
14           else if random() < e
15               Current = Temporary
16       Time--;
17       Temperature = Temperature×Alfa
```

Figure 4.4. Pseudo-code of simulated annealing algorithm used in the conventional automatic cell placement tool, PRS.

the cost of *Temporary* placement has a worse cost compared to *Best* placement, before discarding the displacement, *Temporary* placement may still be chosen as *Current* placement according to a probability function. This function depends on the current temperature of the algorithm, as well as, the difference between the cost of the objective function for the new placement, and the cost of the objective function for the actual Current placement. This technique allows the tool to avoid getting stuck at local minima and increases the chances of reaching the optimal placement with minimum cost.

Based on PRS, we implement yield-aware PRS (YA-PRS). This is performed by incorporating the pseudo-code of Figure 4.2 into the simulating annealing algorithm in PRS. This consists of a slight modification of the simulating annealing algorithm. In particular, line 12 and 13 of the algorithm in Figure 4.4 is replaced by line 1 of the pseudo-code in Figure 4.2. Prediction of the critical area, represented by $A_c( )$ in the added code, is now required. Using the layout sensitivity model, the prediction of critical area is cut down to the prediction of the layout area and the total wire length. In YA-PRS, the layout area is predicted exactly as discussed in Section 2. However, total wire length prediction is performed differently than the method discussed earlier. In particular, semi-perimeter method and Rent's rule modeling are only accurate for chip-size designs. Since PRS supports only small layouts, the total wire length is predicted by estimating the length of each interconnect based on the distance separating its ends and their side locations with respect to the routing channels.

4.4. Testing and Results of the Implemented Tool

In order to validate the implementation, the yield-aware version of PRS, YA-PRS, is tested on an actual design. The design is a combinational logic network that computes the absolute value of the difference between two 2-bit numbers. The design constitutes of 52 gates and 75 nets. First, the accuracy of critical area estimation is tested. According to the layout sensitivity model of Chapter 3, critical area is a function of layout area and total wire length as discussed in Section 2.1.

Accuracy of the estimations of the total wire length and layout area was tested. Average estimations were very close to the actual quantities. Results are shown in TABLE 4.2. The outcomes of the YA-PRS are compared to the outcomes of the original version of the tool, PRS. Figure 4.5 shows the output display of YA-PRS when run on the real design described earlier. Both tools are run several times on the same design. At each run, total wire length, layout area, and critical area for metal layer 2 of the final placement are measured. Figure 4.6 depicts a comparison between the average measurements for placements generated by YA-PRS and placements generated by PRS. On average, placements resulting from YA-PRS have 27.6%, 14.6%, and 35.8% improvements in total wire length, layout area, and critical area, respectively, over placements resulting from conventional PRS. These improvements come at the cost of 45.1% added runtime.

TABLE 4.2. COMPARISON BETWEEN ACTUAL AND ESTIMATED VALUES OF TOTAL WIRE LENGTH AND LAYOUT AREA IN YA-PRS.

	Actual	**Estimated**	**% error**
Layout area [nm^2]	85874533	8.4E+07	2.7%
Wire length [nm]	154375	156014	1.1%

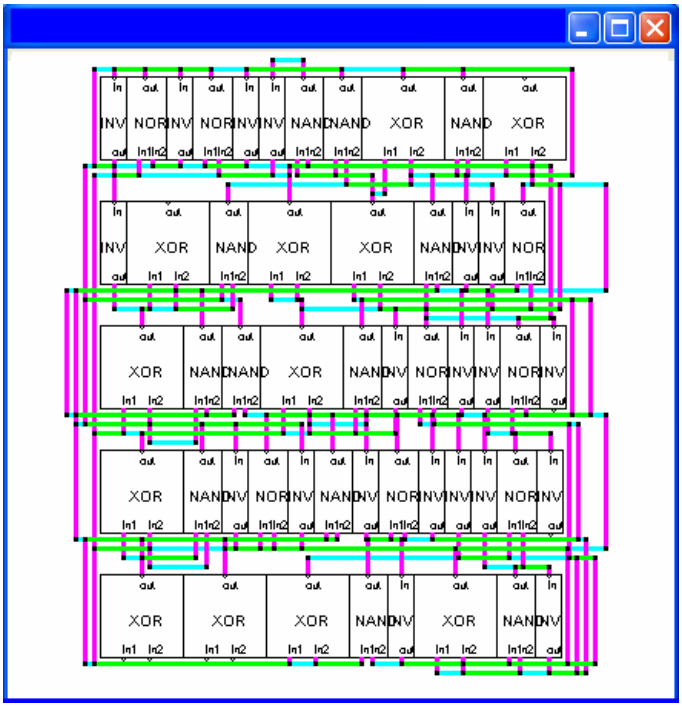


Figure 4.5. Output display of YA-PRS when run on real design of 52 gates

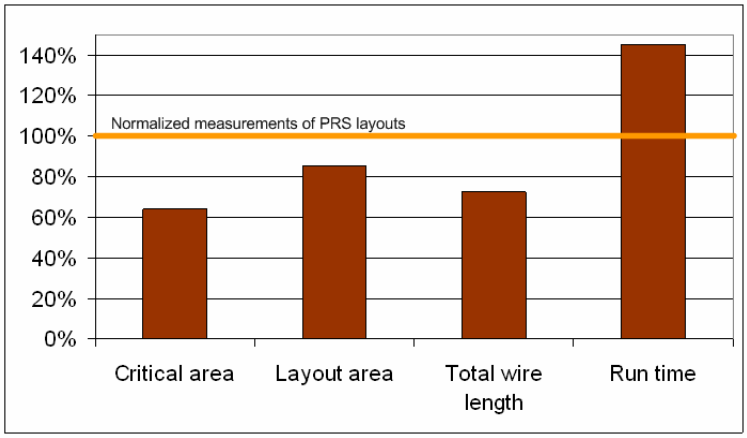


Figure 4.6. Comparison of average critical area for metal layer 2, layout area, total wire length, and run time for layouts generated by PRS and YA-PRS.

This reduction of critical area significantly enhances the yield. If the same percent reduction of critical area applies on a modern VLSI design in 65 nm technology node with chip area of 1 cm^2, then using the negative binomial yield model with a cluster parameter

TABLE 4.3. SUMMARY OF PARAMETERS USED TO TRANSFORM REDUCTION IN CRITICAL AREA TO REDUCTION IN YIELD USING THE NEGATIVE BINOMIAL MODEL.

Technology node [nm]	65
Average defect density D_0 [defect/m^2]	1395
Number of metal layers	11
Chip area [cm^2]	1
Cluster parameter	2

of 2, the reduction of critical area improves the yield by 6.9%. TABLE 4.3 summarizes all parameters used in this calculation.

The effect of the choice of β on the optimization of total wire length and critical area is also studied. YA-PRS was run on the same design with different values of β. Figure 4.7 and Figure 4.8 depict, respectively, average critical area for metal layer 2 and total wire length of the generated layouts for different values of β.

When β is set to a very large value, the tool no more optimizes the critical area and behaves as conventional cells placement tools. Figure 4.7 and Figure 4.8 show that the value of β can be optimized to minimize the critical area and total wire length concur-

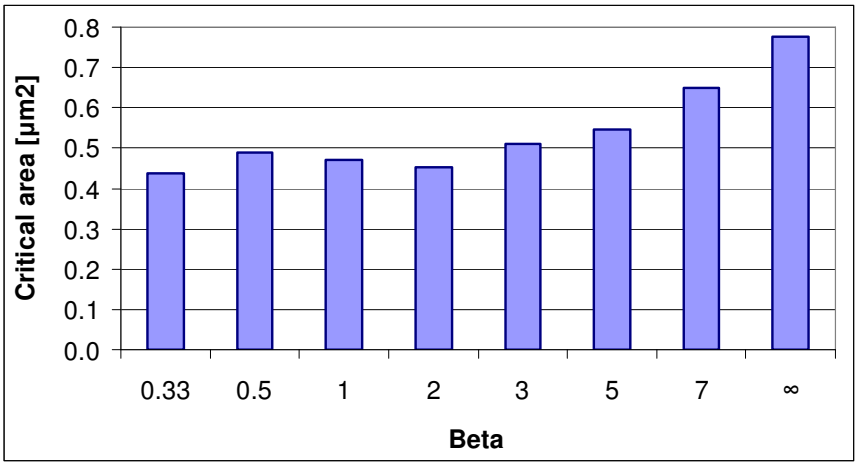


Figure 4.7. Critical area for metal layer 2 of generated layouts with different β.

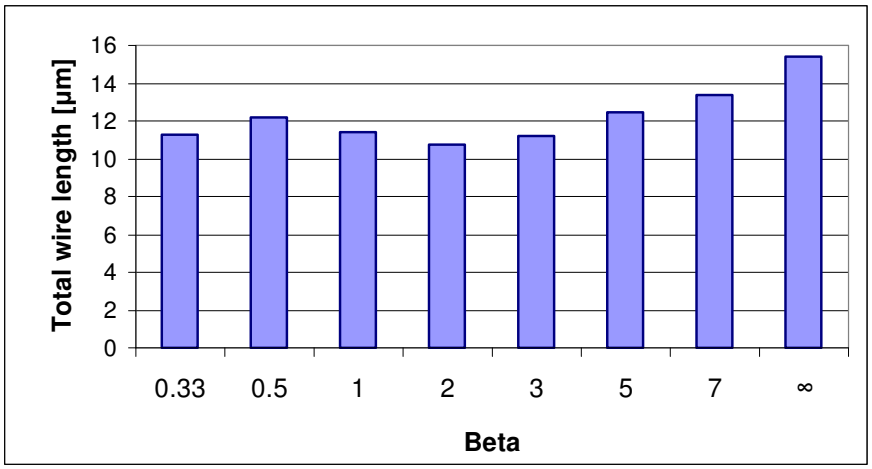


Figure 4.8. Total wire length for generated layouts with different β.

rently. These two figures demonstrate also that any choice of β will not lead to results worse than conventional placement in terms of critical area and total wire length. Hence, yield-aware placement tool does not risk optimization of performance.

4.5. Comparison with a Previous Work

Yield consideration during the cell placement and layout design is a promising technique to enhance manufacturability of nanometer CMOS technology, however only a few works has been done in this area. For instance the methodology to include yield enhancement proposed in [67] uses the inaccurate critical area model during the simulated annealing. The drawback of this technique is that it can only be applied to a very specific case, i.e. simulated annealing algorithm. On the other hand, the methodology proposed in this paper is more general and can be applied to any iterative placement algorithm for any type of cells.

Besides, the authors in [67] modify the cost function, in the simulated annealing algorithm, to include an extra term that consists of the estimated yield multiplied by some

weight factor. The choice of the yield weight can drastically affect the optimization of the other metrics in the cost function. Yet, the authors do not propose any method to choose this weight that apparently does not exist even in the case where one metric is much more important than the other. For instance, if the yield optimization is the first objective, then having a large value for beta would result in extremely low quality layout in terms of performance and placement would have no control over the optimization of the other objectives. Another drawback of modifying the cost function, which is the core of the simulated annealing algorithm, is that weights of all metrics need to be re-optimized so that the tool can achieve layouts with good quality. In contrast, our methodology does not require a modification of the core objective function of the placement algorithm, and, can be used to incorporate the yield enhancement into any iterative or combinatorial placement algorithm.

Chapter 5

Layout Sensitivity Model for Estimating Narrow Interconnects

5.1. Introduction

An interconnect narrowing random defect occurs when a defect intervenes the lithographic printing of interconnects causing missing material of interconnects without causing a complete cut of the interconnect. We define the critical width, w_n, as the minimum acceptable width of interconnect at the narrow site. Therefore, only defects resulting in the formation of narrow sites having widths less than the critical width at their narrow sites will be considered as narrow defects. Interconnect victims of defect intervention are shown in Figure 5.1. In Figure 5.1(a), the defect results in the formation of a narrow site with a width larger than the critical width, and consequently, the defect can be neglected. In Figure 5.1(b), a narrow site with a width smaller than the critical width is formed by the defect, and consequently, the defect is considered as a narrow defect and the victim interconnect is called a narrow interconnect. These narrow interconnects are very vulnerable to electromigration (EM) failure mechanism and can cause a chip failure in the field.

Semiconductor yield enhancement faces non-stopping challenges as the number of transistors per die exponentially grows and the minimum feature size of the manufacturing process exponentially scales down. Formation of open and short circuits caused by the intervention of spot defects during the fabrication process represent the major challenge to yield enhancement. As a result, yield modeling is traditionally based on the

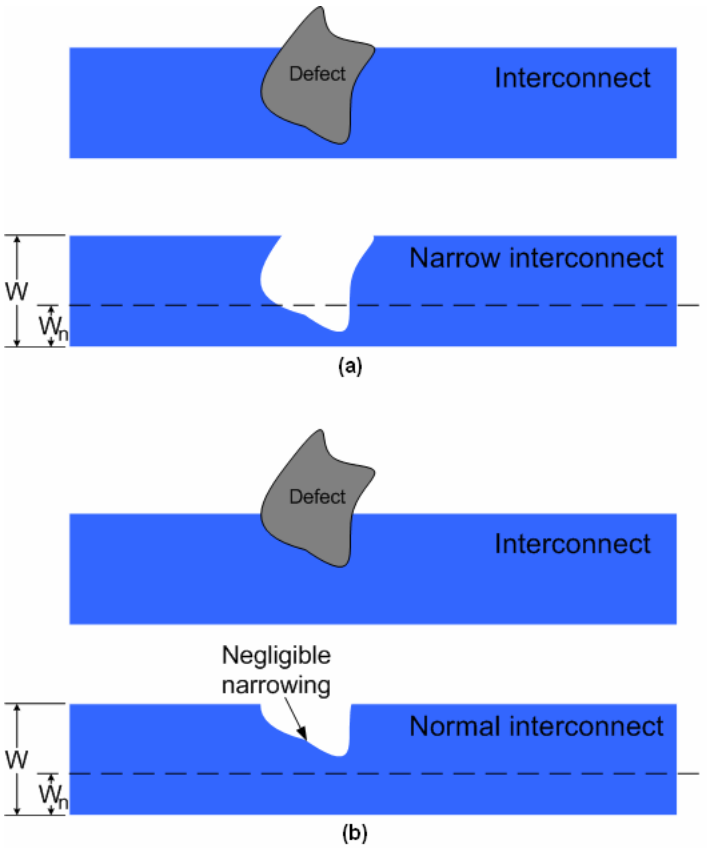


Figure 5.1. Example of particle deposition on wafer. (a) Particle deposition interfering with the formation of an interconnect. (b) A narrow interconnect.

analysis of the critical area. In this chapter, we contribute to the stochastic method of critical area analysis by presenting a layout sensitivity model that includes the effects of the narrowing defect in the analysis and prediction of the manufacturing yield.

Section 2 emphasizes on the effects of narrow defect on aggravating electromigration. The model predicting the layout sensitivity to narrow defects is derived in Section 3. In Section 4, the model is validated through testing and comparisons with simulated and actual data extracted from real layouts. Applications of the layout sensitivity model accounting for narrows are proposed in Section 5.

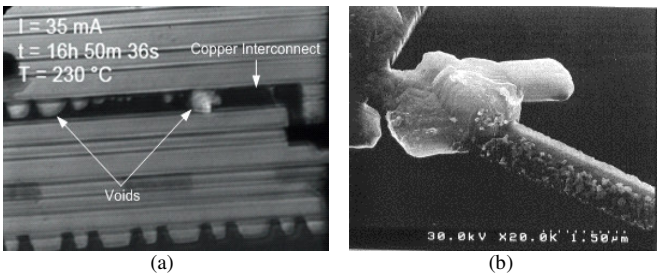
The most of the material presented in this chapter appears also in the published works of [5] and [71].

5.2. Effects of Narrow Interconnect on Electromigration

Narrow interconnects represent a risk of chip failure in the field. Such interconnects are almost impossible to detect during IC testing by the manufacturer. This makes the effect of narrow interconnects even more severe. In this section, electromigration-induced chip failure in narrow interconnects is analyzed.

5.2.1. Electromigration Aggravation

Electromigration (EM) is an interconnect failure mechanism that is considered as a foremost challenge for semiconductor manufacturing [72], [73]. EM is the mass movement of metal caused by the flow of electrons in conducting wires at high temperature [74], [75]. In particular, it is the transfer of momentum from electrons to thermally active metal atoms causing the transport of metal, away of its original site, in the direction of the electron flow [18]. Possible failures induced by EM are the formation of open circuit as a result of metal migration as in Figure 5.2(a), and the formation of a short circuit in consequence of metal atoms exerting a pressure at a site and breaking the passivation layer [18] as shown in Figure 5.2(b).



(a) (b)

Figure 5.2. Examples of EM induced failure. (a) Open circuit resulting from formation of voids due to EM in a line interconnect [76]. (b) Extrusion of metal through the passivation layer [77].

Copper (Cu), instead of aluminum (Al), has recently been employed in semiconductor manufacturing for the interconnect material because Cu has a smaller resistivity and better opposition to electromigration than Al [78], [79]. In Cu interconnect fabrication process, a barrier layer is deposited on the bottom and sidewalls of the interconnect while a dielectric film is added on top [72], [80]. The barrier layer is used to prevent Cu diffusion in the interconnect layer dielectric (ILD). Studies have shown that Cu interconnect are still vulnerable to EM [78], [81]. In particular, EM occurs at the interconnect top surface since it is not covered by the barrier layer [72]. However, as reported in [80], EM can also occur at the interface of Cu and barrier layer. It has been even reported in [82] that Cu interconnects, in some particular cases, demonstrate less lifetime than Al interconnects. Therefore, EM is expected to continue to be the primary reliability concern for interconnects and a leading challenge for IC reliability.

A typical metric used in the analysis of EM is the interconnect mean time to failure (MTTF). An empirical model describing MTTF caused by EM is derived by Black in [83], and for MTTF of a single interconnect, Black's law is stated as follows [84]:

$$MTTF = A\frac{wt}{J_e^2}e^{E_a/kT}, \tag{5.1}$$

where w and t are the interconnect width and thickness respectively, k is the Boltzmann's constant, T is the interconnect temperature, A is a constant embodying physical properties of the metal in use, J_e is the electron current density, E_a is the activation energy for EM failure. Replacing the current density J_e by $I/(w\times t)$, where I is the average current flowing in the interconnect and the term $(w\times t)$ represents the area of the interconnect cross section, Black's law can be written as:

$$MTTF = A\frac{wt}{I^2/w^2t^2}e^{E_a/kT} = A\frac{t^3w^3}{I^2}e^{E_a/kT}, \tag{5.2}$$

(5.2) shows that for a narrow interconnect having width of w/K at its weakest point (narrowed region), where w is the width of the normal interconnect and K is defined as the narrowing factor, the MTTF is reduced by a factor of K^3. In practice, the coefficient of J_e is not exactly 2 as in Black's original equation, but, it varies between 1 and 2 [72], [85]. Therefore, the MTTF in this case is reduced by a factor between K^2 and K^3. Using (5.2), the MTTF of narrow interconnect as a function of the width of its narrow site for three different technology nodes is depicted in Figure 5.3. The plot shows that the impact of interconnect narrowing on MTTF becomes more severe as technology node scales down.

Another factor that aggravates EM in narrow interconnects is the rise of temperature at the narrowed region. Specifically, the narrowed site represents a region of high resistance compared to other parts of the structure; consequently, more energy dissipation is gener-

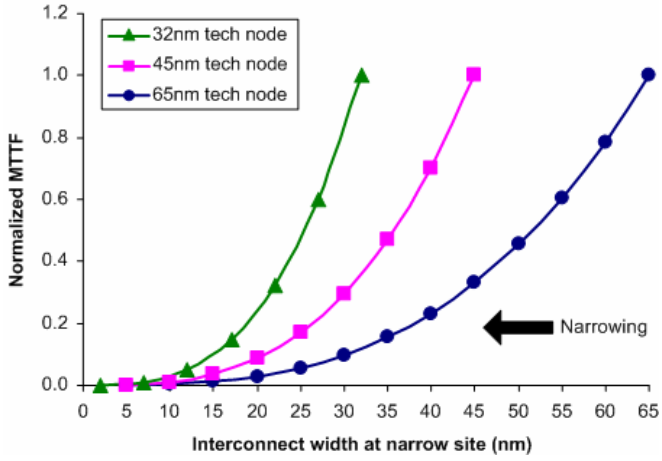


Figure 5.3. Plot of normalized MTTF vs. interconnect width at narrow site for 65nm, 45nm, and 32nm technology nodes.

ated and higher temperature is observed at the narrow site. As shown in (5.2) the MTTF decreases exponentially by increasing temperature. Thus, the increase of temperature in the narrow region dramatically reduces the MTTF of the interconnect.

5.3. Predictive Model for Narrow Interconnects

In this section, a stochastic layout sensitivity model for narrow defects is derived. The model is based on the layout sensitivity model offered in Chapter 3 (also in [3]). The section starts by deriving the model for layout sensitivity, and then, a methodology for inferring the probability of narrow interconnects is proposed.

5.3.1. Derivation of a Layout Sensitivity Model Accounting for Narrows

Spot defects represent the main challenge for enhancement of manufacturing yield. Thus, researchers have developed layout sensitivity models for such defects in order to estimate the manufacturing yield. Moreover, pre-layout yield estimation is believed to be necessary for determining whether or not new products can meet their cost objectives [1].

Maly offered in [37] a model for predicting the critical area and consequently the manufacturing yield by considering narrow interconnects that have a width less than a predefined minimal width as open defects. However, his model is not extended to predict narrow interconnects and lacks accuracy in predicting the probability of failure caused by spot defects. An attempt to estimate the probability for a single interconnect to become narrowed as a result of spot defects is offered in [86]. Yet, the suggested analysis is extremely complicated even when applied to a very simple structure [86] and becomes

nearly impossible to apply to actual layouts. The rareness of the models that accounts for narrowing defects in predicting the yield and the inefficiency of the ones that do account for this type of defect represented the primary motivation for developing a layout sensitivity model that considers narrowing defects in predicting the yield.

The new model is based on layout sensitivity model developed in Chapter 3 (also in [3]). The main difference between the two models is that the new one uses a probabilistic approach in determining the number of channels covered by a defect; whereas in the old model a deterministic approach is used and a defect of specific size r is assumed to cover a fixed number of channels. The probabilistic approach of the new model allows us to include the narrowing defects in calculating the probability of failure for opens. The complete derivation of the model follows.

Some assumptions are made in order to simplify the derivation of the model. First, we assume that interconnect routing is performed using a grid based approach. The layout grid consists of channels that can be either empty or occupied by interconnects. We also assume that the routing of different interconnects are independent of each other. These assumptions are made without loss of generality of the model since the same assumptions are also made in most yield analysis tools to perform critical area studies.

It is important to note that a defect of a specific size r does not always cover the same number of channels. In fact, the number of channels covered by a defect depends on the size of the defect as well as its location. Therefore, to determine the probability for a defect of size r to cause an open defect, we need to find out the possible number of channels that can be covered and the chances for each case to occur. This is achieved by moving the defect a distance of $(w + s)$ away from its original location, with steps equal to the

smallest unit of distance, while checking the number of covered channels for every different location. The probability for the defect to cover a certain number of channels, N, is the ratio of all locations at which the defect covers N channels to the distance $(w + s)$[‡] i.e. the total number of possible locations of the defect.

Let m be the minimum number of channels covered by the defect. It is recommended to refer to Figure 5.4 for a better understanding of the derivation of the model. The defect covers a minimum number of channels when its leftmost (rightmost) edge coincides with the right (left) edge of the interconnect with the minimum width, w_n, units of distance to the right (left) of the left (right) edge of a particular channel. At this point, the partially covered channel (channel B in example of Figure 5.4) is not considered as a cut channel

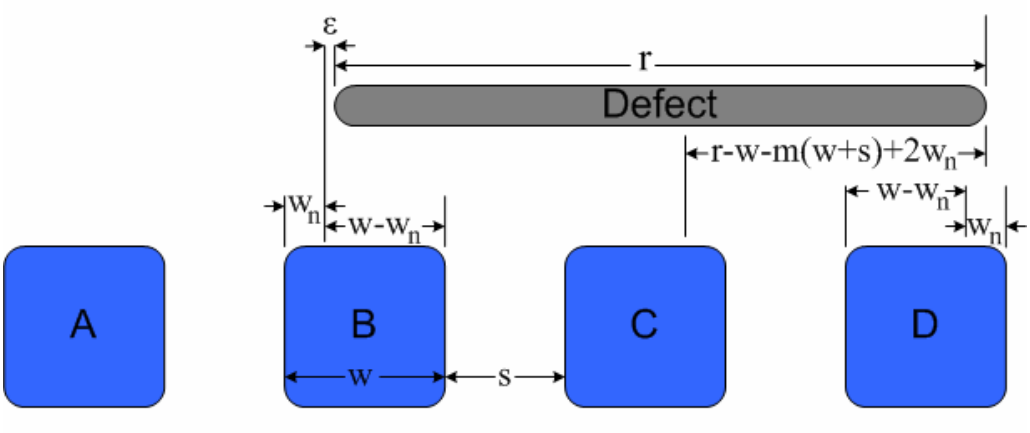


Figure 5.4. Example of a defect at a location covering the minimum number of channel *m*. In this case, the defect covers channels C and D, and therefore, *m* is equal to 2.

[‡] If the particle is moved furthermore, then the same positioning with respect to the channels would be repeated. Thus, moving the particle up to a distance of $(w + s)$ would include all possible locations that a particle can have.

and will be referred to as the first channel. A part of the defect with distance ($w - w_n$) is needed to cover the first channel and the remaining part of distance ($r - (w - w_n)$) is to cover the minimum number of channels, m (refer to Figure 5.4).

The last channel (channel D in the example of Figure 5.4) needs a distance of ($w - w_n + s$) to be covered. Other channels i.e. excluding first and last channels that we call m_1, needs a distance of ($w + s$) to be covered by the defect and cause a channel cut. The number of channels, m_1, which can be covered by the width ($r - (w - w_n)$) of the defect is determined as follows:

$$m_1 = \left\lfloor \frac{r-(w-w_n)}{w+s} \right\rfloor, \tag{5.3}$$

For the remaining part of the defect that neither covers one of the m_1 channels nor covers the first channel, which is equal to $r - (w - w_n) - m_1(w + s)$, we check if it cuts an additional channel (the last channel). The additional channel is considered as cut if the defect covers more than ($w - w_n$) of its total width. Therefore, m can be written as follows:

$$m = m_1 + \left[\left\lfloor \frac{r-(w-w_n)-m_1(w+s)}{w-w_n+s} \right\rfloor > 0 \right]$$

$$= \left\lfloor \frac{r-(w-w_n)}{w+s} \right\rfloor + \left[\left\lfloor \frac{r-(w-w_n)-\left\lfloor \frac{r-(w-w_n)}{w+s} \right\rfloor (w+s)}{w-w_n+s} \right\rfloor > 0 \right], \tag{5.4}$$

where [x] is Iverson's convention that evaluates to 1 if x is true, and 0 if x is false.

Now we start moving the defect toward cutting the first channel with steps equal to the smallest unit of distance. We assume that the movement is always made to the left to simplify the explanation. At this stage, ($m + 1$) channels are cut, i.e. the first channel as well as all other channels that were considered in the minimum number m of channels. (m

+ 1) channels remains cut for a distance of $r - (w - w_n) - (w + s - w_n) - (m - 1)(w + s)$, i.e. width of defect minus width of defect to cover first channel minus width of defect needed to cover the last channel minus width of defect needed to cover all other channels (m – 1 channels) as depicted by Figure 5.4. This distance can be expressed by $r - w - m(w + s) + 2w_n$.

After the defect is moved $r - w - m(w + s) + 2w_n$, the last channel that was considered in the m channels will be uncovered instantly. There will be m cut channels until the left (right) edge of the defect coincides with the right (left) edge of the interconnect with the minimum width i.e. w_n units of distance to the right (left) of the left (right) edge of the channel neighboring the first channel to its left (right). The defect would have moved for $(w + s) - (r - w - m(w + s) + 2w_n)$, which evaluates to $2w + s + m(w + s) - r - 2w_n$.

Thus, the defect either covers m channels with a probability of

$$\frac{2w + s + m(w + s) - r - 2w_n}{w + s}, \tag{5.5}$$

or (m + 1) channels with a probability of

$$\frac{r - w - m(w + s) + 2w_n}{w + s}. \tag{5.6}$$

The probability for the chip to overcome a defect that covers N channels is the probability for the N consecutive channels to be empty, which is $(1 - d)^N$. Therefore, in the general case, the probability for the chip to overcome a defect of size r, i.e., the probability of survival, referred to as P_s, is the product of the probability of a defect to cover a number N of channels by $(1 - d)^N$ summed up for all possible number of channels that the defect can cover. Since the defect can either cover m channels or (m + 1) channels as demonstrated earlier, then P_s is computed as follows:

$$P_s = \frac{2w + s + m(w+s) - r - 2w_n}{w+s} \times (1-d)^m + \frac{r - w - m(w+s) + 2w_n}{w+s} \times (1-d)^{m+1}. \quad (5.7)$$

The layout sensitivity S_n is defined to be the probability of chip failure P_F. Thus, the layout sensitivity is modeled as:

$$S_n = P_F = 1 - P_s = 1 - \left(\frac{2w + s + m(w+s) - r - 2w_n}{w+s} \times (1-d)^m + \frac{r - w - m(w+s) + 2w_n}{w+s} \times (1-d)^{m+1} \right). \quad (5.8)$$

5.3.1. Methodology for Predicting Narrows

The sensitivity model determines the probability of having an interconnect with a width less than the critical width. In other words, the model includes open as well as narrow defects. The value of the critical area specified by the manufacturer determines the narrows to include in the model. For instance, setting of the critical width to zero leads to the exclusion of narrow defect from the model and reduce its outcome to the layout sensitivity to opens. Therefore, the probability of having a narrow interconnect with width less than a specific critical width, w_n^*, is equal to the outcome of the model when the critical width is set to w_n^* minus the outcome of the model when the critical width is set to zero. In the general case, the probability of narrow interconnect having the width between w_{n1} and w_{n2} can be obtained by subtracting the outcomes of the model when critical width is set to w_{n2} and when critical width is set to w_{n1}.

5.4. Results and Comparison with Measured Data

The sensitivity model was tested for 0.32µm technology node with an interconnect density of 0.6 and a critical width of 0 (i.e. excluding narrow defects). Figure 5.5 shows the result of testing and a comparison with the sensitivity extracted from an actual layout in [41].

The percent error of the model's outcomes when compared to actual data was calculated. The average percent error was found to be 1.7%, which is an indication of the high fidelity of the model.

Because of the absence of layout analysis data for narrow interconnects in real design, the model was compared with results extracted from simulations. The testing of the model is performed using PRS, a placement and routing software previously developed in [45]. PRS was used to create the layout of a small circuit that computes the absolute value of the difference between two 2-bit numbers using a 45nm technology node. The

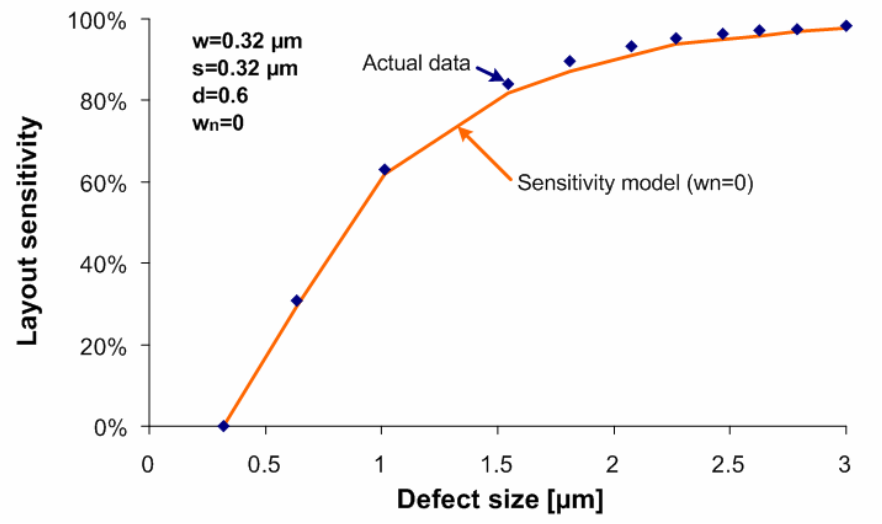


Figure 5.5. Comparison of sensitivity model with actual extracted layout sensitivity for open defects.

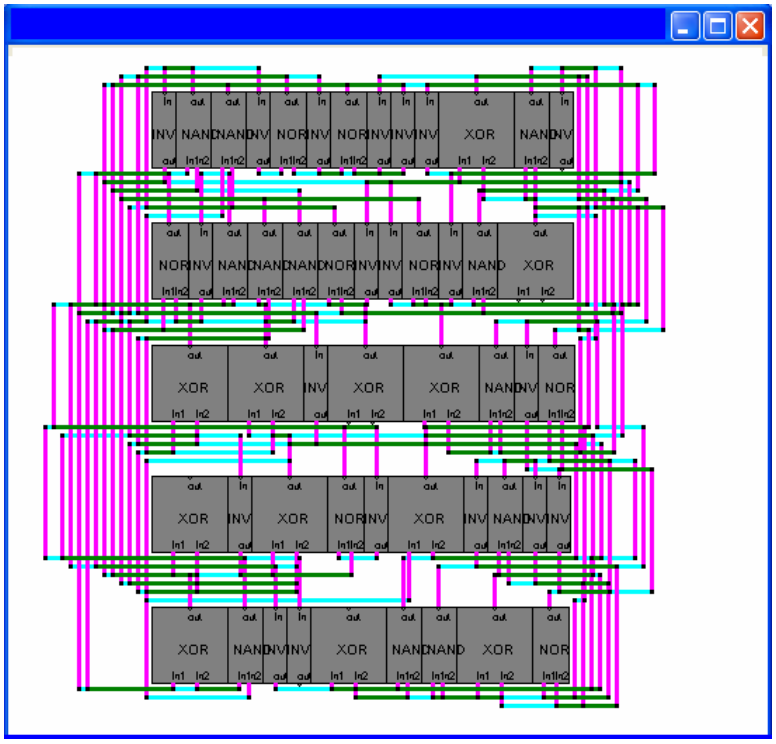


Figure 5.6. PRS displaying the layout of a circuit that computes the absolute value of the difference between two 2-bit numbers.

generated layout is exhibited in Figure 5.6.

We expanded PRS tool to generate defects and check for the resulting narrows and opens. A large number of defects with different sizes (20,000 defects per defect size) were placed randomly on the layout and the number of resulting narrows and opens for a single metal layer is computed for different critical widths, w_n. The probability of failure associated with each defect size is then obtained by the ratio of the total number of defects resulting in narrows or opens to the total number of generated defects for each defect size.

The channel densities and total area are then extracted from the layout and provided to the model. Figure 5.7 presents a comparison between the simulated and predicted probabilities of failure for different defect sizes and different critical widths, w_n. Results show

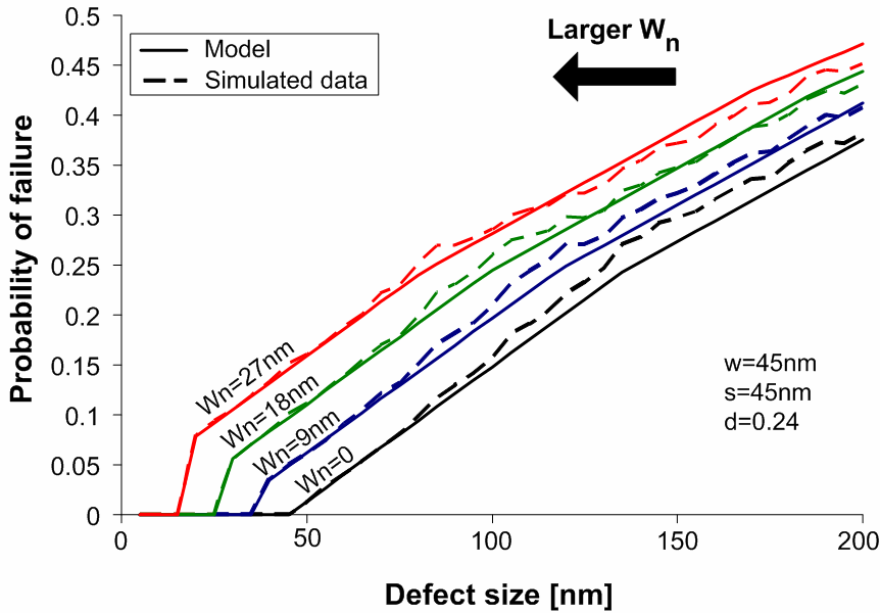


Figure 5.7. Comparison of modeled and simulated probabilities of failure due to open and narrow defects for different critical widths, w_n.

the accuracy of the model in predicting narrow and open defects and are summarized in TABLE 5.1.

TABLE 5.1. SUMMARY OF PERCENT ERRORS OF NARROWS PREDICTIVE MODEL WHEN COMPARED TO SIMULATED DATA FOR DIFFERENT VALUES OF CRITICAL WIDTH

critical widths w_n [nm]	**Average percent error of model when compared to simulated data (%)**
0	5.6
4.5	4.7
9	3.9
13.5	3.0
18	2.3
22.5	2.4
27	2.6

5.5. Application

In this section, some applications of the predictive model of narrowing defects are examined.

5.5.1. Prediction of Probability of Failure Caused by Narrows for Future Technologies

The probability for a defect of specific size r to cause the formation of an open or narrow interconnect with a width less than some width w_n is determined using the sensitivity model described in the previous section. Consequently, the average probability P_n for a defect of any size to induce a narrow interconnect with a width less then w_n can be calculated as follows:

$$P_n\left(w < w_n\right) = \int_0^\infty f_s(r) \times \left(S_n\left(w_n, r\right) - S_n\left(w_n = 0, r\right)\right) \cdot dr, \tag{5.9}$$

where $f_s(r)$ is the defect size distribution, and $S_n(w_n, r)$ is the probability of the formation of an open or narrow interconnect having width less than w_n given in (5.8).

$S_n(w_n, r)$ is a function of interconnect width w, spacing s, and density d as well as the critical width, w_n, and defect size r (See (5.8)). Since w and s are predetermined by the manufacturing process and d is preset by the design of the layout, then $S_n(w_n, r)$ is only a function of w_n and r variables. According to (5.9), the probability of interconnect narrowing, P_n, is therefore only a function of w_n.

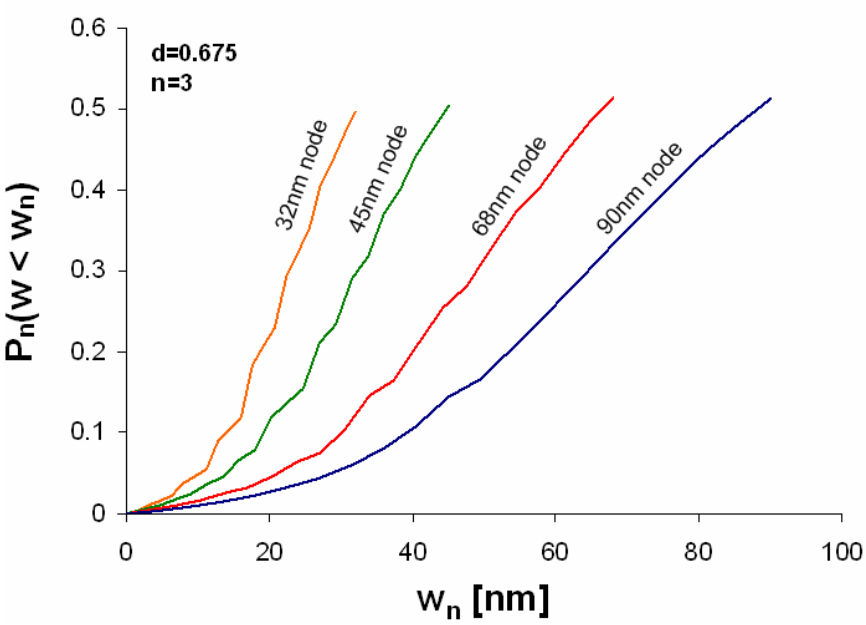


Figure 5.8. Plots of probability P_n of formation of an open or narrow as a function of the critical width, w_n, for 90nm, 68nm, 45nm, and 32nm technology nodes.

Figure 5.8 illustrates the probability of narrowing, P_n, versus critical width, w_n, for different technology nodes. In this plot, the interconnect width w and spacing s as well as the critical defect size r_0, for which the defect size distribution peaks, were chosen in accordance with ITRS [32]. Manufacturing is assumed to be performed in a typical fabrication line with n=3, and the channel density d is assumed to be 0.675 considering constant Rent's parameters for all technology nodes [87].

The narrow site represents the weakest points of a defective interconnect. Consequently, failure of a narrow interconnect will most probably occur at its narrow site. In this case, the interconnect time to failure is the time for the narrow site to fail, which can be calculated using Black's law by replacing w with w_n. If an interconnect MTTF less than a predefined threshold is considered as a failure, then the plots of Figure 5.8 can be transformed into plots of the probability of failure P_f as a function of the mean time to

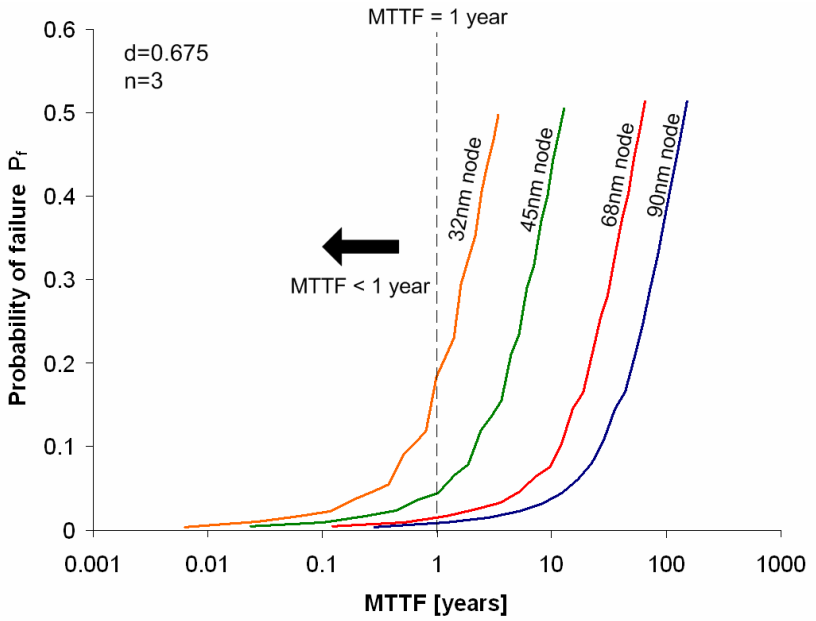


Figure 5.9. Plots of probability of failure P_f of formation of an open or narrow as a function of the critical width, w_n, for 90nm, 68nm, 45nm, and 32nm technology nodes.

failure of a narrow site having a width of w_n, MTTF(w_n). Figure 5.9 shows the plots of P_f as a function of MTTF where a realistic current density exponent of 1.1 was used in Black's equation to find the MTTF associated with w_n.

The plots of Figure 5.9 reveal the dramatic increase of the probability of failure due to narrowing defects as technology advances toward smaller lithographic nodes. For instance, the plots show that, for a MTTF threshold of 1 year, the probability of failure due to narrow defects (excluding open defect) is 0.9%, 1.5%, 4.5%, and 18.5% for 90nm, 65nm, 45nm, and 32nm technology nodes, respectively. Note the exponential increase of the probability of failure due to narrows as technology scales down. This is an indication that the considering narrow defects in yield analysis would be a must for future technology nodes.

5.5.2. Enhancement of Cost and Reliability Analyses

The predictive model of narrow interconnects can be employed in cost and reliability analyses of newly developed products. In particular, narrow interconnects can induce early chip failure affecting the reliability as well as the cost of a product. Hence, more precise reliability and cost estimations can be obtained by including the effects of narrows in the analyses of these measures. Moreover, a more trusted reliability analysis allows manufacturers to better approximate the warranty period to be offered for a particular product.

Chapter 6

Conclusions

Typically, modeling of semiconductor manufacturing yield is either based on spot defect simulations or an analysis of the critical area. Simulations of spot defects on modern VLSI designs take weeks to complete if a good accuracy is necessary. Besides, performing critical area analysis in today's VLSI designs can easily take several days [41]. The stochastic method of critical area analysis was introduced to overcome this limitation and to make yield modeling a much easier and faster task. The first contribution to this method was offered by Stapper in 1983-84 [8], [39]. His model used a simple linear approximation of the critical area as a function of defect size. Few other contributions were provided in [40] and [41]. These adopt Stapper's model and make some modifications to it. Yet, existing models of the stochastic approach for critical area analysis lacks accuracy.

On the other hand, the layout sensitivity model presented in this thesis can, in few seconds, approximate the critical area with good accuracy. The efficiency of the sensitivity model makes its application in modeling, predicting, and enhancing the semiconductor manufacturing yield very beneficial. Another main advantage of the layout sensitivity model is its ability to predict the yield of a particular product even before coming up with its actual design. This is very crucial in studying the economical feasibility of products. It can be used to check whether or not a product can meet its cost objectives before starting the design phase that is time-consuming and very costly.

We demonstrated that yield enhancement can be performed during cells placement using the layout sensitivity model described in Chapter 3. Moreover, we show that yield and performance optimization can be realized concurrently. The concept of "yield-awareness" during cells placement is introduced. An actual "yield-aware cell placement tool", called YA-PRS, was presented. The tool significantly reduces the critical area, and consequently, the yield. This reduction comes at no cost in terms of total wire length; however, the cost is an increase in the run time of the placement algorithm. Yield-aware cell placement represents an innovative method of yield enhancement during the design phase.

Another part of the thesis presents a model for "narrow defects", which is a new type of failure mechanism in advanced semiconductor manufacturing. We define "narrow defects" as non-catastrophic missing material spot defects causing the formation of a narrow site at the victim interconnects. Interconnect victims of such a defect favor electromigration that may lead to interconnect open and short defects and consequently a chip failure. The induced failure may occur during the different stages of manufacturing and affect the yield, but also, the failure may occur in the field and affect the product's reliability. We expect narrowing defects to present a serious challenge for IC reliability with the ever decreasing feature size. Models that accounts for narrow interconnects in predicting the manufacturing yield are very rare and existing ones are ineffective. In this thesis, we proposed a very simple yet efficient methodology to predict the probability of narrow interconnects in any layout given some basic information such as interconnect width, spacing, and density. Subsequently, the probability of chip failure due to narrowing de-

fects can be inferred and narrows can be considered in modeling of semiconductor manufacturing yield and reliability analysis.

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Vita

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