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SEMICONDUCTOR DEVICE MODELING, SIMULATION AND FAILURE PREDICTION FOR ELECTROSTATIC DISCHARGE CONDITIONS

by

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B.S. Sichuan University, 2013
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A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy
in the Department of Electrical and Computer Engineering
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

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Major Professor: Kalpathy B. Sundaram

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ABSTRACT

Electrostatic Discharge (ESD) caused failures are major reliability issues in IC industry. Device modeling for ESD conditions is necessary to evaluate ESD robustness in simulation. Although SPICE model is accurate and efficient for circuit simulations in most cases, devices under ESD conditions operate in abnormal status. SPICE model cannot cover the device operating region beyond normal operation.

Thermal failure is one of the main reasons to cause device failure under ESD conditions. A compact model is developed to predict thermal failure with circuit simulators. Instead of considering the detailed failure mechanisms, a failure temperature is introduced to indicate device failure. The developed model is implemented by a multiple-stage thermal network.

P-N junction is the fundamental structure for ESD protection devices. An enhanced diode model is proposed and is used to simulate the device behaviors for ESD events. The model includes all physical effects for ESD conditions, which are voltage overshoot, self-heating effect, velocity saturation and thermal failure. The proposed model not only can fit the I-V and transient characteristics, but also can predict failure for different pulses.

Safe Operating Area (SOA) is an important factor to evaluate the LDMOS performance. The transient SOA boundary is considered as power-defined. By placing the failure monitor under certain conditions, the developed modeling methodology can predict the boundary of transient SOA for any short pulse stress conditions. No matter failure happens before or after snapback phenomenon.

Weibull distribution is popular to evaluate the dielectric lifetime for CVS. By using the transformative version of power law, the pulsing stresses are converted into CVS, and TDDB under ESD conditions for SiN MIMCAPs is analyzed. The thickness dependency and area independency of capacitor breakdown voltage is observed, which can be explained by the constant ΔE model instead of conventional percolation model.

To my fiancée Wenjing Feng, my parents Aiping Wu and Yongsheng Li

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LIST OF ACRONYMS

ADS	Advanced Design System
BCD	Bipolar-CMOS-DMOS
BJT	Bipolar Junction Transistor
CDM	Charged Device Model
CMC	Compact Model Coalition
CMOS	Complementary Metal-Oxide-Semiconductor
CVS	Constant Voltage Stress
DMOS	Double Diffusion Metal-Oxide-Semiconductor
DUT	Device Under Test
EOS	Electrical Overstress
ESD	Electrostatic Discharge
ESOA	Electrical Safe Operating Area
GGNMOS	Grounded-Gate N-type MOSFET
HBM	Human Body Model
HMM	Human Metal Model
HPPI	High Power Pulse Instrument
HV	High Voltage
IC	Integrated Circuit
IPD	Integrated Passive Device

LDMOS	Lateral Double Diffusion Metal-Oxide-Semiconductor
LVTSCR	Low Voltage Triggering Silicon Controlled Rectifier
MIMCAP	Metal-Insulator-Metal Capacitor
MM	Machine Model
PCB	Printed Circuit Board
PECVD	Plasma-Enhanced Chemical Vapor Deposition
SCR	Silicon Controlled Rectifier
SiN	Silicon Nitride
SPICE	Simulation Program with Integrated Circuit Emphasis
SOA	Safe Operating Area
TCAD	Technology Computer Aided Design
TDR	Time Domain Reflectometry
TDT	Time Domain Transmission
TLP	Transmission Line Pulsing
TSOA	Thermal Safe Operating Area
TVS	Transient Voltage Suppressor
VFTLP	Very Fast Transmission Line Pulsing

CHAPTER 1 INTRODUCTION

1.1 What Is ESD

Electrostatic discharge (ESD) is an event that charges suddenly transfer between two objects at different static potentials [1]. An ESD event can be caused by directly contact or induced by electrical field. Very high current may pass through the two objects in an extreme short period of time. Lightning is one type of ESD with large scale in everyday life. And a human body can carry more than ten thousand volts of ESD in a dry environment [2].

ESD failure is one of the main reliability problems in integrated circuit (IC) industry. When an electronic device or microelectronic system is subject to an ESD event, damages may happen because the ESD generated energy is not able to be dissipated quickly enough, shown in Figure 1-1 [3]. It is estimated that about 35% of all damaged microchips are ESD related, resulting in more than 84 billion dollars lost profits per year [4]. The side effects of poor ESD robustness include delay on product releases, competitive disadvantages, and engineering resource drain. The main damage mechanisms of ESD failure include junction thermal failure, oxide rupture, charge injection, and metal burn-out. Figure 1-2 gives the images for mainstream ESD induced damages.

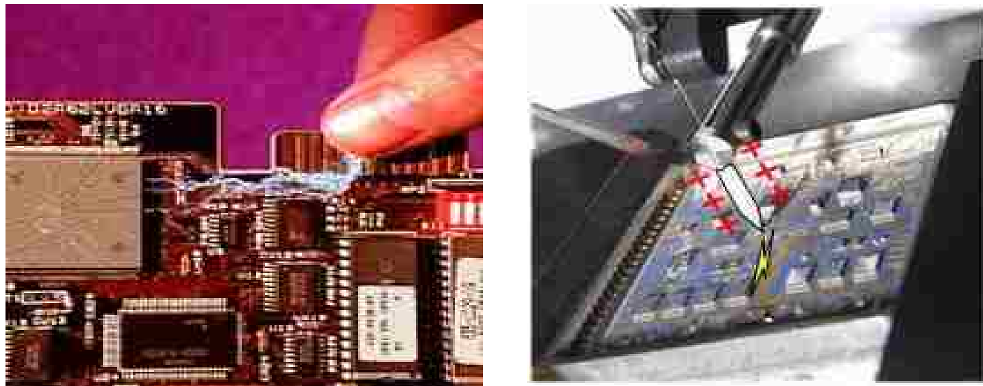
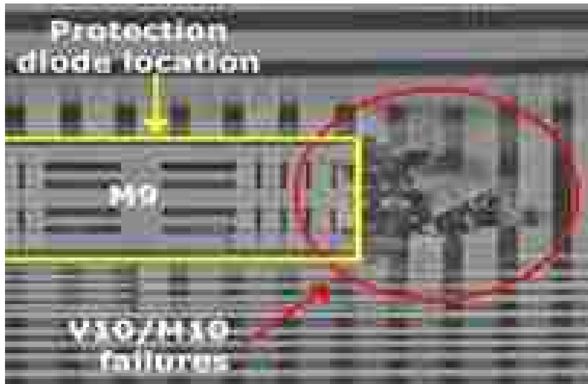
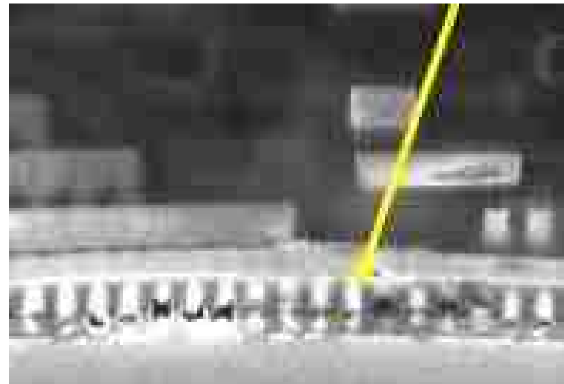


Figure 1-1 Example of ESD on Microelectronic systems.

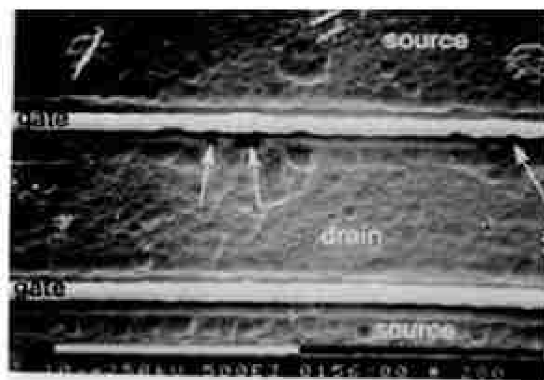


(a)



(b)

(c)



(d)

Figure 1-2 ESD induced damages (a) interconnect burn-out, (b) metal fusing, (c) crystal structure change, (d) junction thermal failure.

1.2 ESD Protection Design Concepts

The basic two aspects for ESD protection are dissipating ESD current quickly enough to keep core circuit safe, and clamping voltage lower than the breakdown voltage of core circuits. Both two objectives can therefore minimize the prospect of ESD-induced damages to the core circuit. The general ESD protection design window is shown in Figure 1-3.

ESD protection strategy include off-chip protection and on-chip protection. The off-chip protection is implemented by using different printed circuit board (PCB) components in the ESD protection network. Off-chip protection uses the technology of isolation, filter, or transient voltage suppressor (TVS) components [5]. A general on-chip ESD protection scheme is shown in Figure 1-4. On-chip protection cells should be placed around the core IC, and the cells can be single directional or bidiertional depends on the designed scheme. And the ESD protection devices in the protection cells should be dessgned based on the design windown in Figure 1-3.

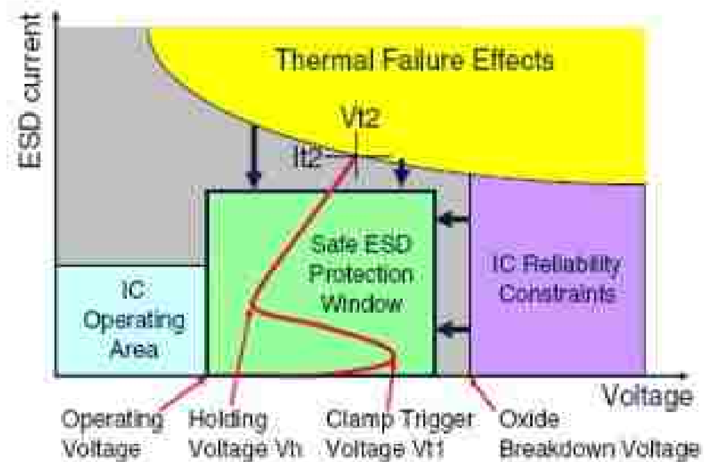


Figure 1-3 General ESD protection design window.

For full on-chip ESD structures, each pin to pin combination should be considered, which means there must be an ESD protection cell for ESD energy dissipation along the path between any pair of pins. A good ESD protection element should have the following features, clamp ESD voltage and shunt ESD current; turn on faster than the core circuit; have low on -resistance; have minimum parasitic capacitance; be robust and offer protection for different ESD stresses; not interfere with the IC's functional testing; occupy minimum area; not cause latch-up or EOS failures; be in off-state during the normal operation and return off-state after the ESD event [6].

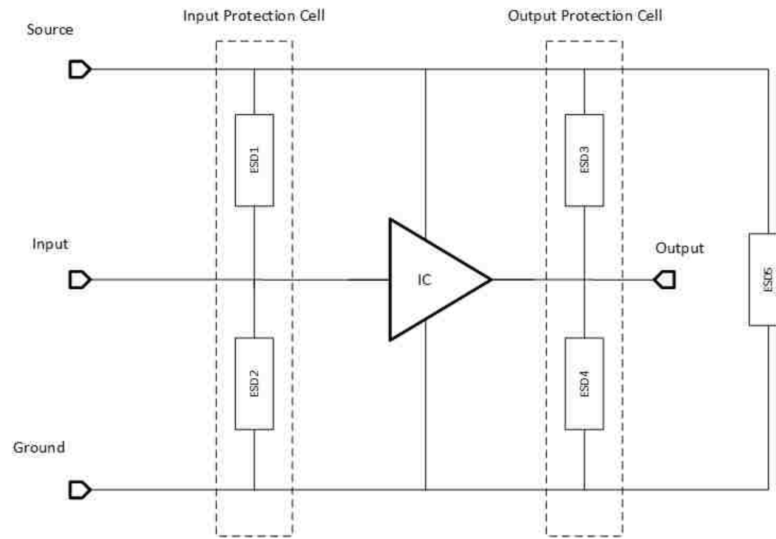


Figure 1-4 General on-chip ESD protection scheme.

As IC process technology has been in the node of sub-micro meter even nanometer, transistors keep shrinking with each advanced process technology generation. ESD protection design is becoming increasingly challenging. With the process technology scaling, the supply voltage and oxide breakdown voltage decrease faster than the ESD cells' trigger and holding voltages, and the core circuit is becoming more sensitive to the ESD protection circuit's parasitic effect, making the design window much narrower [6].

1.3 ESD Models and Testing Techniques

ESD models are developed to mimic different types of ESD events. Generally, ESD models can be divided into two categories, which are component level ESD model and system level ESD model. Component level ESD model is used to evaluate the reliability of electronic components, for example, ICs, while system level ESD model is used to determine whether the electronic system can survive during daily use. The mainstream component level ESD models include

Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM). On the other hand, the popular system level ESD models include the standard International Electrotechnical Commission (IEC), and the Human Metal Model (HMM).

1.3.1 Human Body Model

The Human Body Model (HBM) is used to mimic an ESD event when a charged person touches the IC and discharges with the finger. The HBM equivalent schematic is shown in Figure 1-5. The capacitor C_{HBM} = 100pF is discharged through the resistor R_{HBM} = 1500 Ω, where the resistor represents the human body resistor. C_1, L_1 and C_B represent the parasitic elements of testers, and the values depend on the type of testing equipment. The rise time for HBM is from 2ns to 10ns, typically, and decay time is 150 ns, respectively [7]. The robustness level varies from 500V to 8kV depending on the different environments and applications.

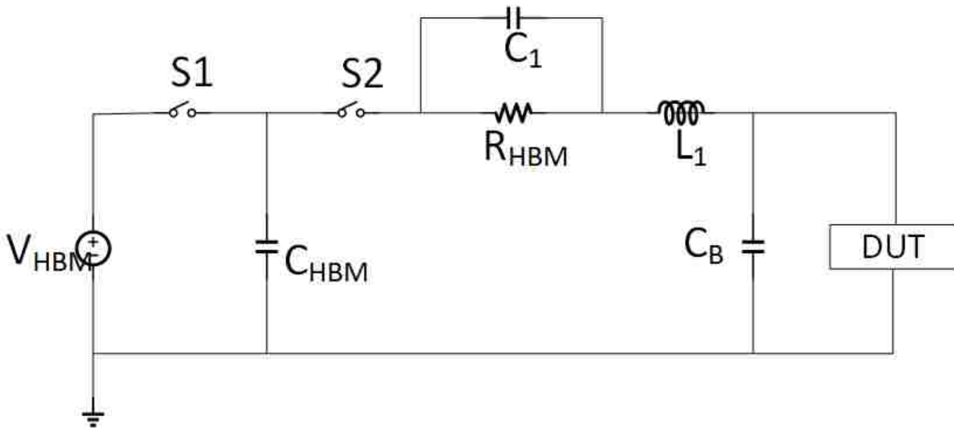


Figure 1-5 HBM equivalent schematic.

1.3.2 Machine Model

The Machine Model (MM) is developed to represent the worst case of HBM, which is used to mimic the ESD event when discharges happen through metal equipment. The 1500 Ω resistor is removed compared with HBM. The MM equivalent schematic is shown in Figure 1-6, where

the discharge capacitor C_{MM} = 200pF, the inductor L_1 = 0.75 µH and resistor R_1 is between 0 to 10 Ω [8]. The robustness level of MM is higher than 200V, however, the Indurtry Council propose to ruduce the MM robustness level to 30V.

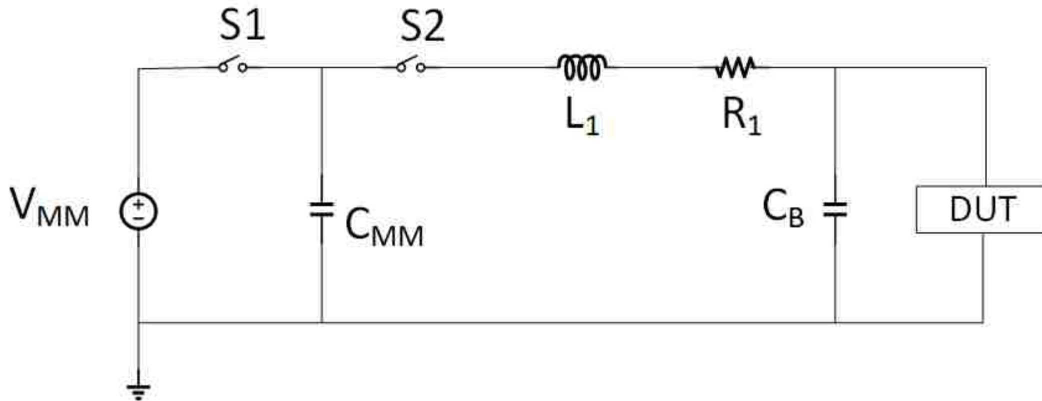


Figure 1-6 MM equivalent schematic.

1.3.3 Charged Device Model

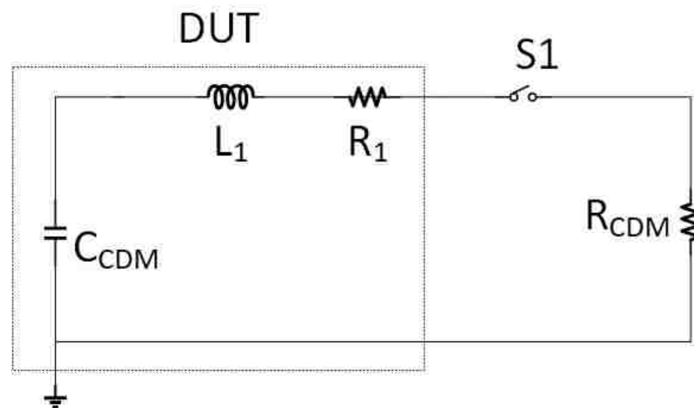


Figure 1-7 An equivalent circuit of CDM.

Charged Device Model (CDM) is another important model to represent the field caused ESD failures. The equivalent circuit of CDM is shown in Figure 1-7, note than the discharged capacitor C_{CDM} is part of the device under testing (DUT). R_1 and L_1 are 10Ω and 10nH, respectively.

And the resistor R_{CDM} represents the resistance along the discharge path [9]. The CDM model has a very fast rise time which is shorter than 500ps, short duration which is several nanoseconds and high value peak current. The safe level for CDM is usually higher than 250V.

1.3.4 System Level ESD Models

IEC61000-4-2 is a widely used standard to qualify the reliability of electronic systems stressed by system level ESD events. IEC 61000-4-2 standard usually has a rise time of 1ns and duration of 80ns [10], [11].

Human Metal Model (HMM) is developed in Japan recently, which is used to mimic the ESD event when a person is touching a grounded electronic device with metal arms [12]. The waveform of HMM is like a peak current following an HBM like transient. HMM is used to address the gap between component level ESD model and system level ESD model.

1.3.5 Transmission Line Pulsing Tester

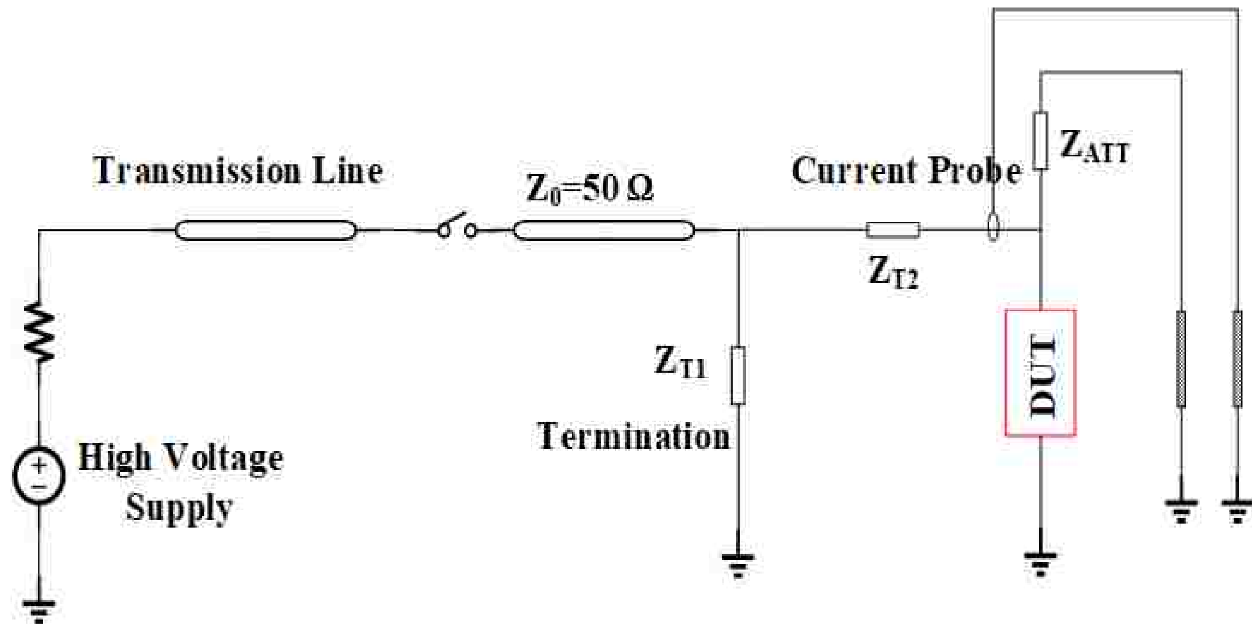


Figure 1-8 Transmission Line Pulsing (TLP) tester principle.

Transmission Line Pulsing (TLP) testing technique is used to correlate to other ESD models, such as HBM and CDM. During a TLP testing procedure, a piece of transmission line is charged to a voltage level, then discharge through another transmission line with 50Ω impedance, stressing on the DUT. So, the charged transmission line is able to generate a square waveform. The transient voltage and current on the DUT are measured by probes. Each waveform is captured with a back-ended oscilloscope, and the associated quasi-static I-V characteristics are generated by averaging the voltage and current transient waveforms in the stable region, always from 60% to 80%. One TLP configuration is shown in Figure 1-8.

The TLP testing schematic can be both Time Domain Reflectometry (TDR) and Time Domain Transmission (TDT) with different configurations [6]. The standard TLP system has the duration of 100ns and rise time of 0.2ns, 1ns and 10ns. The 100ns duration 10ns rise time TLP is usually used as correlation of HBM. Very Fast TLP (VFTLP) has the pulse width from 1ns to 10ns, and rise time of 200ps, which is used to correlate CDM. Note that the VFTLP testing system is usually configured with high-quality high-speed RF probes to reduce parasitic effects [6].

1.4 Basic ESD Protection Device

In this section, several basic ESD protection devices are introduced briefly, including diode, Grounded-gate NMOS (GGNMOS), and Silicon Controlled Rectifier (SCR). Based on the operating mode, ESD protection devices can be divided into passive devices and active devices; based on polarity, ESD protection devices can be divided into single direction devices and bidirectional devices; based on characteristics, ESD protection devices can be divided into snapback devices and non-snapback devices.

1.4.1 Diode

Diode is fundamental and efficient device for ESD protection, and P-N junction structure widely exists in mainstream ESD protection devices. As an example, the cross section of an STI N+/Psub diode is shown in Figure 1-9. For forward bias condition, diodes can exibit good ESD protection performance, including low on-resistance, low turn-on voltage and high current handle capability. However, for reversed bias condition, diodes have high on-resistance and poor robustness [13]. Morever, one of the main disadvantages of diode-based ESD protection devices is that the area occupation is usually larger than other devices, which means higher parascitic effect, making diodes not good for protection of RF applications. The detailed diode physics mechnisms under ESD conditions and diode comprehensive modeling are discussed in Chapter 3.

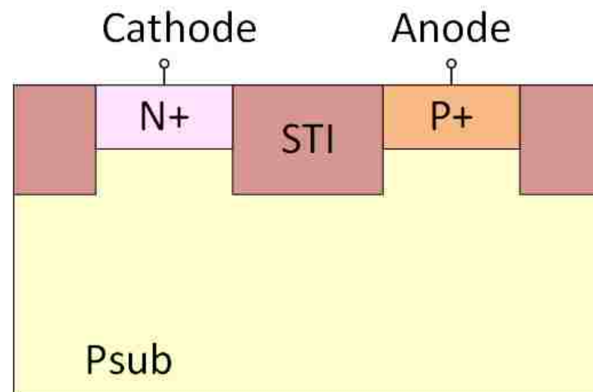
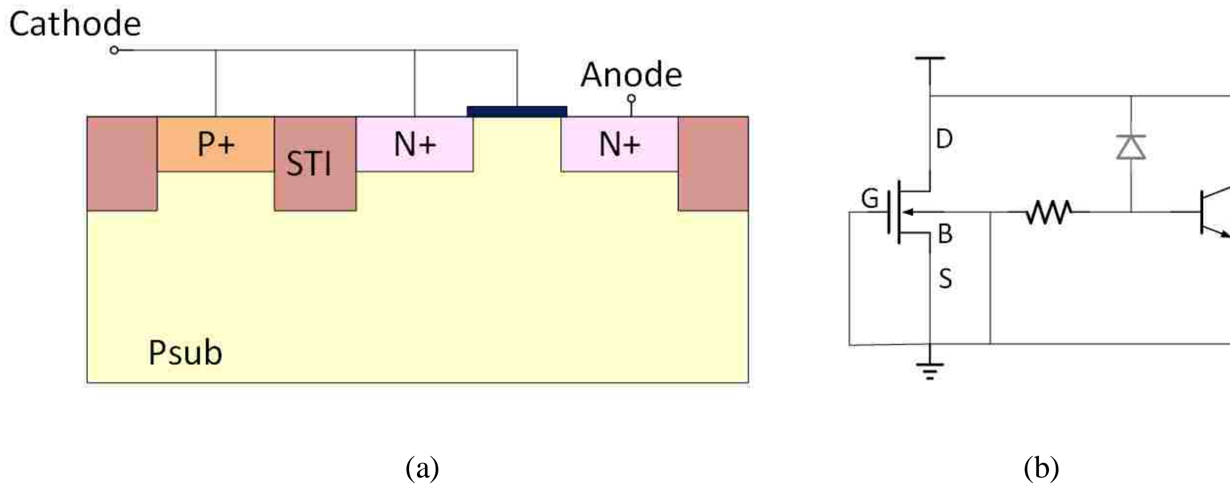


Figure 1-9 Cross section of the N+/Psub diode.

1.4.2 Grounded-gate NMOS

Grounded-gate NMOS (GGNMOS) is one of the most popular and simple ESD protection devices, in which the Gate (G), Source (S) and Body (B) are connected together as device Cathode, shown in Figure 1-10. Under normal operating regions, the GGNMOS is in off-state because the gate is zero biased.



(a) (b)

Figure 1-10 GGNMOS (a) cross section view; (b) equivalent circuit.

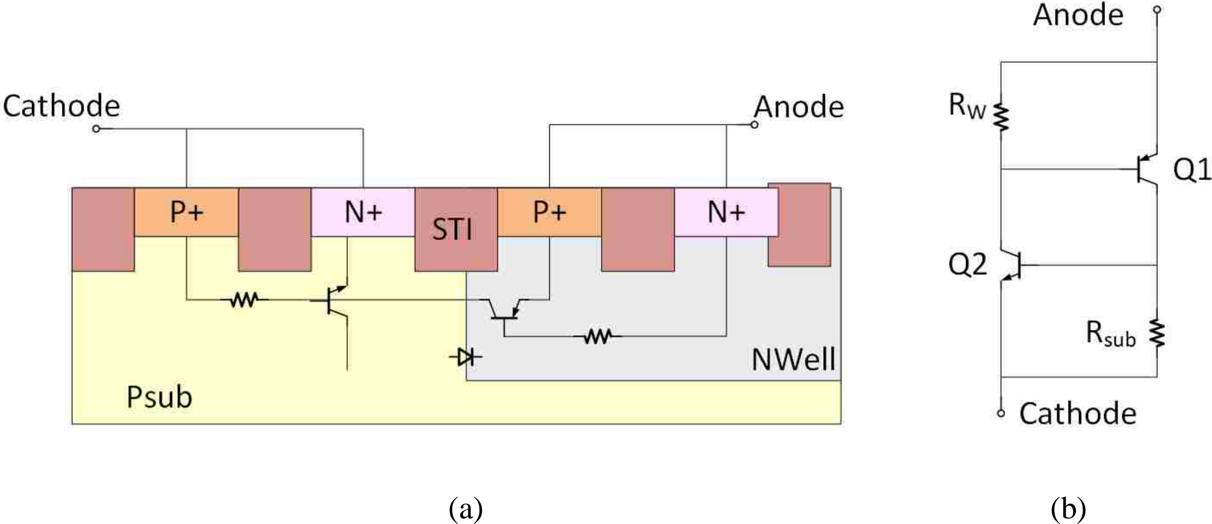
Since the Drain/Body junction is under reversed bias condition, when the voltage across the junction is high enough to its breakdown which may happen during a positive ESD event from the Anode to the Cathode, avalanche multifaction occurs at the junction. As a result, electron-hole pairs are generated and current can flow into the body, passing through the body parasitic resistors. When the voltage drop across the body resistor is higher than 0.7V, the parasitic Bipolar Junction Transistor (BJT) is turned on and operate in amplifier region, making the BJT dominating the current conduction [13]. As a result, a positive feedback mechanism is formed, and the GGNMOS is pushed into a negative resistance region, namely, snapback. After snapback, the GGNMOS forms a low-resistance discharge path, dissipating the ESD current safely. For negative ESD stresses, the Body/Drain junction is forward bias, and the body-drain diode functions as ESD current dissipation path [14]. Based on the discussion above, the GGNMOS is a bidirectional ESD protection device.

In real designs, the GGNMOS usually has large size, which is implemented with multiple finger structure. Non-uniformed turn-on of each figure could be a main problem of multiple finger

structure. In order to solve the issue, a silicide-block layer is introduced in the layout design to create a series resistor at drain region. The resistor is used to force the fingers to be turned on simultaneously, however, the side effect is increasing on-resistance.

1.4.3 Silicon Controlled Rectifier

Silicon Controlled Rectifier (SCR) is one of the most efficient and most robust ESD protection devices. Like the GGNMOS device, SCR is another snapback device with positive feedback mechanism. The PNPN thyristor consists of a parasitic PNP transistor and a parasitic NPN transistor, as shown in Figure 1-11. When positive stress is applied on the SCR, the NWell/P-junction is reversed bias. Avalanche breakdown happens at the junction when the positive voltage is higher than the junction breakdown voltage. Electron-hole pairs are generated in the junction area and electron current flows to the NWell and anode, while hole current flows to the PWell and cathode [13]. When the voltage drop across the Psub resistor is higher than 0.7V, the thyristor is turned on, initiating the SCR latching. The positive feedback mechanism is formed [15].



(a) (b)

Figure 1-11 SCR (a) cross section view; (b) equivalent circuit.

However, due to the lightly doped NWell (or Nsub) and PWell (or Psub), the junction breakdown voltage is usually higher than the gate oxide breakdown voltage of core circuit [16]. Moreover, the holding voltage is usually lower than the operating voltage, leading to possible latch-up issues in normal operating region [17]. In order to making SCR available in most ESD protection cases, triggering and holding engineering are required, which introduces techniques to decrease trigger voltage and increase holding voltage. Diode Triggered SCR (DTSCR) and Low Voltage Triggering SCR (LVTSCR) are examples of triggering engineering, while modifying BJT base distance and doping profile can be holding engineering [15].

1.5 ESD Device Modeling

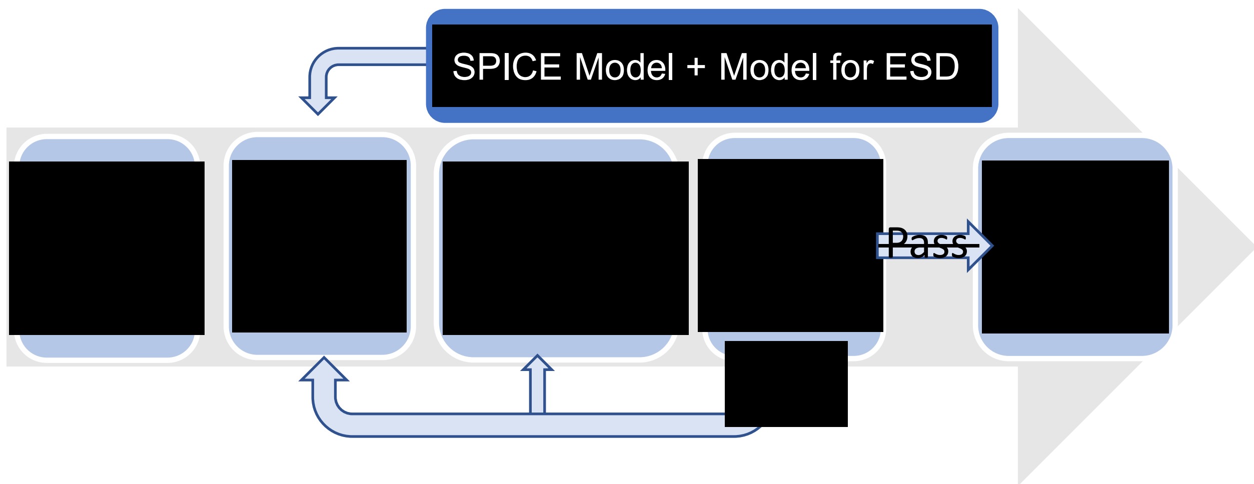


Figure 1-12 Developing procedure of ESD device model.

Device behavior modeling under ESD conditions is an important method to evaluate the performance of ESD protection devices. With accurate model, the developing time for advanced

process and designs can be reduced. Good modeling techniques can enable the designers to evaluate the ESD robustness of their designs and discover the design flaws in simulation. The ESD protection induced core-circuit performance degradation and core-circuit's impact on ESD cells can also be simulated. The procedure to develop a model is shown in Figure 1-12.

Accurate ESD model is difficult, since the model should be able to reproduce a number of special effects and aspects under ESD stress conditions, including high-current, high-voltage operating region, snapback discontinuity, avalanche breakdown, electro-thermal coupling, etc [13].

1.5.1 ESD Failure Modeling

Failure model is a helpful method in ESD protection design, which offers the information to predict possible failure. The failure modeling should start from heat equation [18],

$$\frac{\partial T}{\partial t} - D' \cdot \nabla(T) = \frac{q(t)}{\rho C_p} \tag{1.1}$$

Where ρ is the semiconductor density, C_p is the specific heat, D' is the thermal diffusion constant, and q(t) is the rate of heating per unit of heat source.

An approximate solution for the heat equation is expressed as [18],

$$P_f = \left(\frac{A}{t_f} + \frac{B}{\sqrt{t_f}} + \frac{C}{lgt} + D\right)(T_f - T_0) \tag{1.2}$$

Where T_f is the critical temperature to ESD failure, T_o is the ambient temperature, P_f is defined as power-to-failure, which represents the power required to cause ESD failure under a specific ESD transient stress, t_f is defined as the time-to-failure which represents the time required to cause ESD failure for a specific injecting power. The dependence of power-to-failure P_f on time-to-failure t_f is shown in Figure 1-13, which is the most famous four-segment ESD failure model. The power-to-failure function is given by [18],

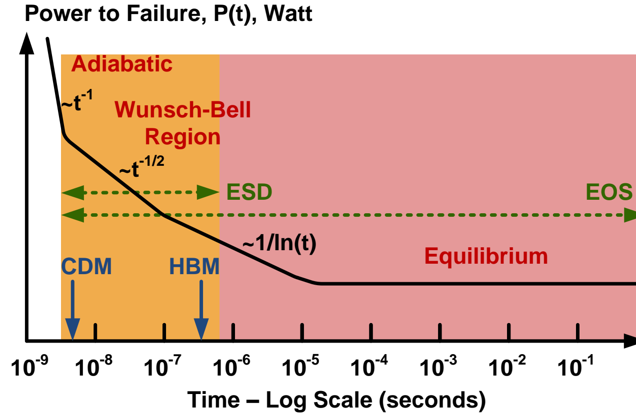


Figure 1-13 Power-to-failure dependence on power-to-time, four-segment ESD failure model.

$$t_a = \frac{a^2}{4\pi D'} \tag{1.3}$$

$$t_b = \frac{b^2}{4\pi D'} \tag{1.4}$$

$$t_c = \frac{c^2}{4\pi D'} \tag{1.5}$$

Where a, b, c are dimension dependent parameters, and D' is the thermal diffusion constant.

$$P_f(t_f) = \frac{\rho C_p abc \cdot (T_f - T_0)}{t_f}, 0 < t_f < t_c \tag{1.6}$$

$$P_f(t_f) = \frac{ab\sqrt{\pi K \rho C_p} \cdot (T_f - T_0)}{\sqrt{t_f} - \frac{\sqrt{t_c}}{2}}, t_c < t_f < t_b \tag{1.7}$$

$$P_f(t_f) = \frac{4\pi K a \cdot (T_f - T_0)}{\ln(\frac{t_f}{t_b}) - 2 - \frac{c}{b}}, t_b < t_f < t_a \tag{1.8}$$

$$P_f(t_f) = \frac{2\pi K a \cdot (T_f - T_0)}{\ln\left(\frac{a}{b}\right) + 2 - \frac{c}{2b} - \sqrt{\frac{t_a}{t_f}}}, t_a < t_f \tag{1.9}$$

Equation 1.9 represents the equilibrium status, in which the power-to-failure is approximately a constant, while equation 1.7 is the Wunsch-Bell equation, and the corresponding curve is Wunsch-Bell plot which matches the ESD timeframe [19]-[21].

1.5.2 ESD Protection Device Modeling

ESD protection devices may exhibits snapback characteristics, which means that the avalanche breakdown effect, impact ionization effect and negative resistance region need to be included in the device modeling. The discontinuity at snapback is the main issue for modeling, causing convenience problem during simulation.

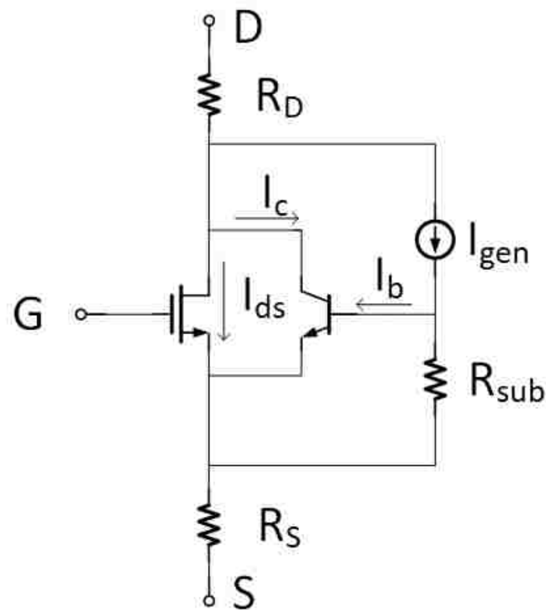


Figure 1-14 Schematic of ESD compact MOSFET model.

As an example, the MOSFET ESD compact model is shown in Figure 1-14, the avalanche current or/and impact ionization current is modeled by I_{gen} [22],

$$I_{gen} = (M - 1) \cdot (I_{ds} + I_c) \tag{1.10}$$

Where M is the multiplication factor, Ids is the MOS surface current, Ic is the BJT collector current, the multiplication factor M can be expressed as [23],

$$M = \frac{1}{1-K1\cdot exp(-\frac{K2}{V_d-V_{dsat}})} \quad (1.11)$$

Where K1, K2 are fitting parameters. However, this M equation may cause convergence problem due to the discontinuity. To address the discontinuity problem, an exponential version M equation is introduced. Equation (1.12) is used to model the snapback [24],

$$M = exp[k1(V_d - V_{dsat} - d1)] + exp[k2(V_d - V_{dsat} - d2)] \quad (1.12)$$

1.5.3 Electro-thermal Coupling Modeling

Electro-thermal coupling effect should be included in ESD device model. It is not a good idea to assume the electronic factors are independent of temperature, since electronic characteristics depends on temperature strongly. Heat is generated from power dissipation and dissipated through substrate and/or surface, both of heat generation and dissipation should be included in modeling procedure. The popular method to model the electro-thermal coupling effect is thermal circuit with thermal capacitors and thermal resistors, and the circuit varies based on the geometry sensitivity [13]. An example MOSFET thermal circuit is shown in Figure 1-15.

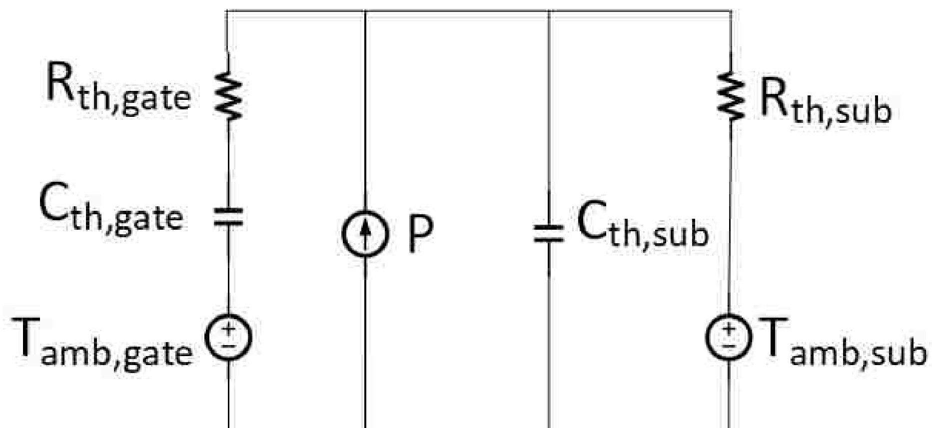


Figure 1-15 An example MOSFET thermal circuit.

1.6 Dissertation Outline

This dissertation will focus on device modeling under ESD stress conditions. Models are developed to address the unique ESD features. The proposed models are able to correlate the simulation with measured results well and can be used to predict device failure under ESD conditions.

Chapter 1 gives a brief introduction about the ESD definition and fundamentals, ESD protection design methodologies and challenges, basic ESD protection devices, and conventional ESD model examples and concepts. Chapter 2 discusses a compact thermal failure model for devices under ESD conditions. With the proposed model, thermal failure can be predicted for any type of ESD stresses. Chapter 3 introduces a comprehensive compact diode model, which is able to address all physical mechanisms including self-heating, velocity saturation, voltage overshoot and thermal failure. The power-defined transient SOA of LDMOS is discussed in this chapter. The boundary of LDMOS SOA is power defined instead of voltage defined, and for extreme short pulsing stresses, snapback can occur. Chapter 5 investigates the characteristics of SiN MIM capacitors. The capacitor lifetime (TDDB) is analyzed. By using the transformative version of power low, the pulsing stresses can be converted into CVS stress. Chapter 6 give a summary of the dissertation and propose the outlooks.

CHAPTER 2 COMPACT JUNCTION THERMAL FAILURE MODEL FOR DEVICES UNDER ESD STRESSES

2.1 Introduction

Thermal failure and dielectric breakdown are two main reasons for semiconductor device failures [25]. Thermal failure usually occurs at the junction area and is heating generation and/or dissipation related [26]. While dielectric breakdown is always associated with gate oxide rupture, and dielectric breakdown usually occurs at the beginning of the ESD event when electrical field is higher than the critical value [27].

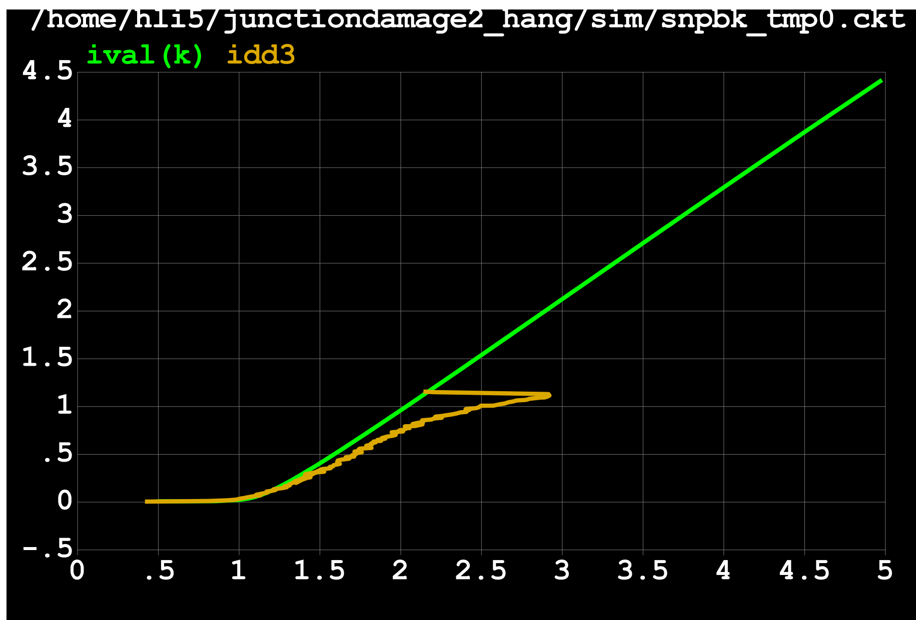


Figure 2-1 Diode measurement and simulation without failure monitor.

To evaluate the performance of ESD protection devices and robustness of devices under ESD stress conditions in simulation, a failure model is necessary. Thermal failure can be observed during measurement, failure voltage and failure current obtained from measurement can be used

to indicate thermal failure. However, the thermal failure prediction is not available during simulation. As an example, the diode measurement and simulation without failure monitor model is shown in Figure 2-1.

Technology Computer Aided Design (TCAD) is an available method to implement the simulation for heat conduction, in which finite element analysis is used to implement the simulation [28]. However, TCAD simulation is time consuming and the TCAD mixed mode is only valid for small scale circuit simulation. Moreover, the heat diffusion function can be solved by using Green Function to obtain the relation between power to failure and time to failure [18]. However, the complex computation makes it impractical to integrate the calculation into simulators. In addition, the energy to failure is introduced as the indicator of thermal failure. The corresponding failure power is obtained by averaging the transient voltage and current waveforms [29]. However, this method is only valid for rectangle pulsing stresses with special pulse widths.

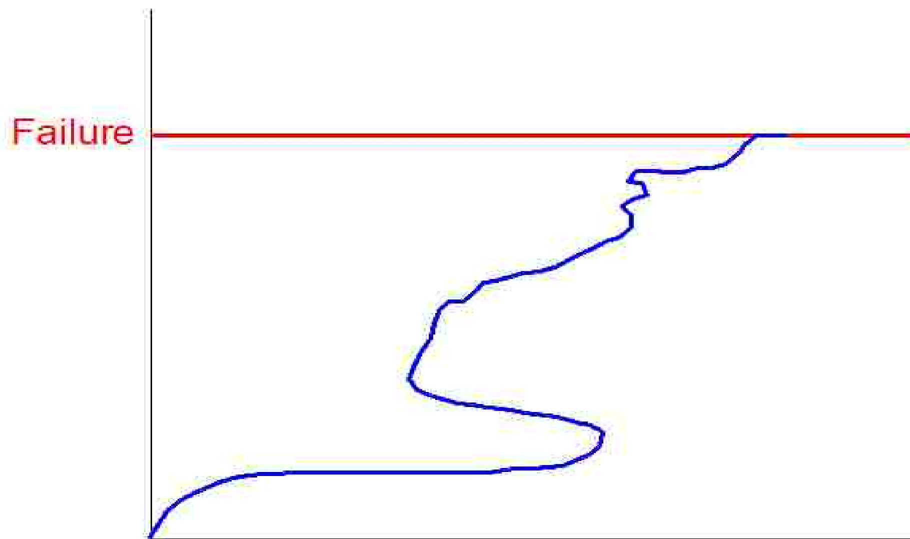


Figure 2-2 Modeling concept of thermal failure monitor.

In this chapter, a thermal failure monitor model is proposed to indicate thermal failure for any types of ESD stresses. The model is implemented with a multiple-stage thermal network and is valid for different pulse widths. By ignoring the detailed failure mechanisms, a fixed failure temperature is introduced as the criteria of thermal failure. The discussed modeling concept is shown in Figure 2-2.

2.2 Thermal Monitor Modeling Methodology

Heating generation, diffusion, and the dissipation efficiency highly depend on the device geometry. Since most thermal failure always happens at the junction area, the TCAD thermal simulation for a P-N junction is implemented, shown in Figure 2-3 [30], [31]. As Figure 2-3 describes, the heat is generated from the current flowing through the juntion, and dissipated from the hotspot to the body deep cooler region, namely, from the junction area to the deep silicon region. The temperature gradient reprsent the heat dissipation efficiency between two adjacent regions. Morever, thermal failure always occurs at the hotspot firsly [32].

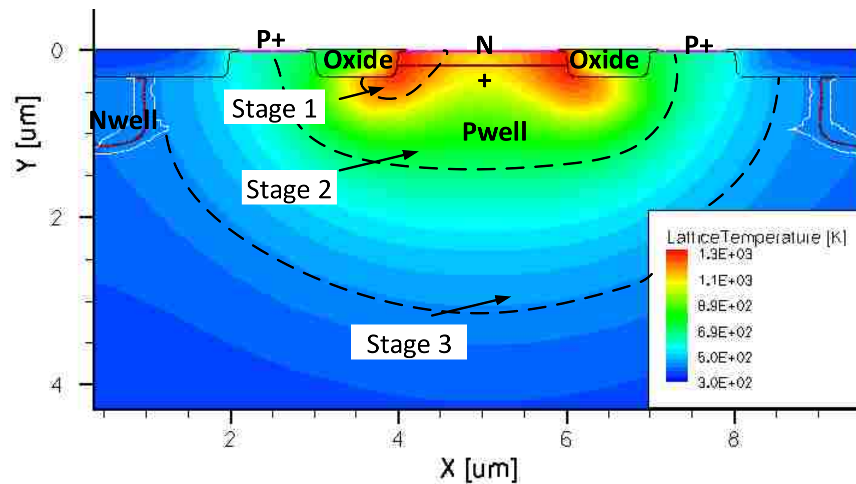


Figure 2-3 TCAD simulation for a reversed bias P-N junction.

To develop a circuit simulator available thermal failure monitor model, the physical phenomenon discussed in last paragraph needs to be transferred to electrical circuit elements. A popular method for the physics/circuit conversion is to employ a thermal network. The thermal capacity of thermal region is similar to the electron capacity of capacitors, whereas the heat dissipation is similar to that the current flows through a resistor [33], [34]. The thermal/electro analogy relation is shown in Figure 2-4. The proposed thermal network can be used as temperature detector [35]. The voltage on capacitor in each stage represents the temperature rise in each thermal region. By reading the votlage on capacitors, the temperature can be mapped into electronic information and available for circuit simulation.

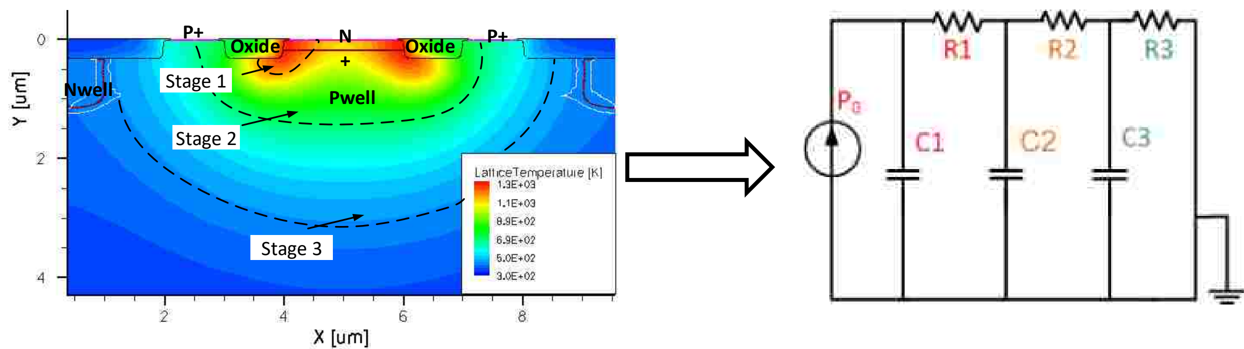


Figure 2-4 Thermal-Electro analogy.

As shown in Figure 2-4, the current source represents the heat generation source. The capacitors represent different silicon regions which can store different levels of thermal energy. And C1 has the smallest value, while has the highest temperature rise, namely, C1 represents the hot-spot region. Outside C1, C2 and C3 have larger values, but lower temperature rise, which represent the deep silicon region. Based on the discussion above, we can reach a boundary conditon C1<C2<C3 [30].

Between two capacitors, the resistor represents the heat dissipation efficiency between two adjacent thermal regions. Smaller resistor means faster heat dissipation, while larger resisitor means slower heat dissipation [30]. For most simulation cases, one stage themral network is enough to monitor the temperature rise. However, for fast transient ESD conditions, one stage is not enough to reproduce the temperature gradient and simulate the temperature rise accurately, while more stages can offer more accurate simulation results but induces more computation complexity. To balance the simulation accuracy and computation complexity, 3-stage thermal network is selected [31].

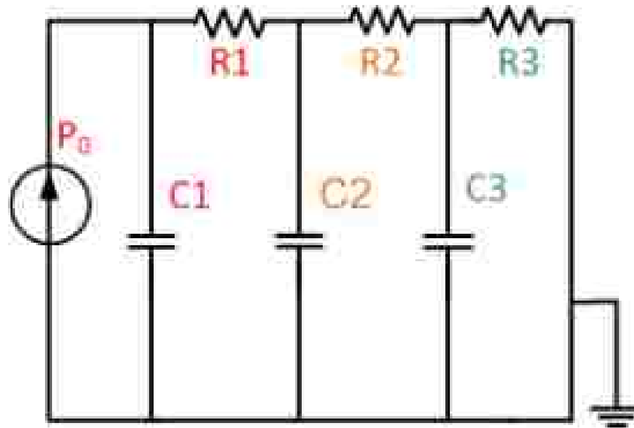


Figure 2-5 3-stage thermal network.

Based on the circuit theory and mapping relation discussed above, the thermal network is shown in Figure 2-5, and the heat conduction procedure can be expressed as,

Heat power inject into stage i is Pi,

$$Pi = Ci\frac{d(Ti)}{dt} + \frac{(T_i - T_{i+1})}{R_i} \tag{2.1}$$

Heat stored on stage i is,

$$Ci\frac{d(Ti)}{dt} \tag{2.2}$$

And the heat flows to adjacent stage is,

$$\frac{(T_i - T_{i+1})}{R_i} \tag{2.3}$$

As the P-N junction diode conducting ESD current, the temperature in device rises with current flowing through the junction due to the self-heating effect. Many side effects occur with the increasing temperature, finally, thermal failure will happen at the hotspot. Note that the device may fail before temperature reaching the silicon or metal melting temperature, this is because that ionization induced carrier may alter the doping profile at the junction area at a high temperature, making the junction malfunctional.

As discussed in Section 1.5.1, the power-to-failure (P_f) dependence on time-to-failure (t_f) is described in detailed. ESD timeframe locates in the Wunsch-Bell curve region, namely, P_f is with linear dependence of $t_f^{1/2}$. To realize the failure prediction in simulation, a fixed failure temperature is introduced to indicate thermal failure. Whatever the failure mechanisms, once the temperature on C1, namely the temperature at hotspot reaches the preset failure temperature, the thermal network will rise a flag for failure. In this dissertation, it is assumed that the device temperature without electrical stress is 0, and the failure temperature is 1000.

In order to extract the parameters inside the thermal network, at least six different pulse widths are required as constraint conditions to obtain the resistor and capacitor values. In this dissertation, the pulse widths of 5ns, 10ns, 50ns, 100ns, 200ns, and 500ns are used to characterize the device thermal failure. The measurement is implemented with a High Power Pulse Instrument (HPPI) and Kelvin connection configuration. To ensure the devices fail at the end of pulse, the

step for measurement is set small enough. So, the time-to-failure (t_f) can be determined as the pulse widths. The power to failure can be exacted from measurement, in which the product of failure voltage (Vt2) and failure current (It2) is used to determine the power-to-failure. The extraction for Vt2 and It2 is shown in Figure 2-6. Table 2-1 lists the power-to-failure for each pulse width with forward and reversed bias condition for the P-N junction.

$$P_f = It2 \times Vt2 \tag{2.4}$$

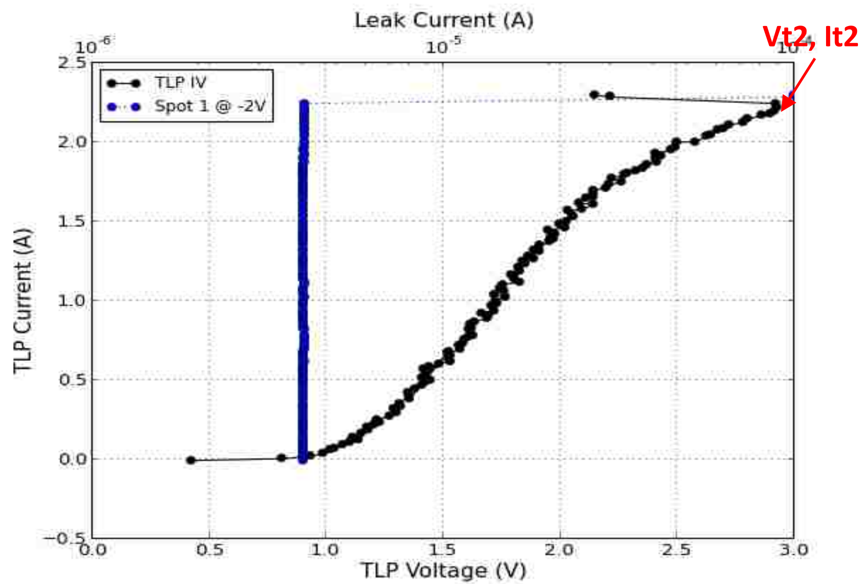


Figure 2-6 Example of Vt2, It2 extraction.

Table 2-1 Power-to-failure for different pulse widths.

Pf vs t	5ns	10ns	50ns	100ns	200ns	500ns
forward	24.83	17.27	8.29	5.96	3.95	3.11
reversed	7.50	6.74	5.01	4.35	3.96	3.63

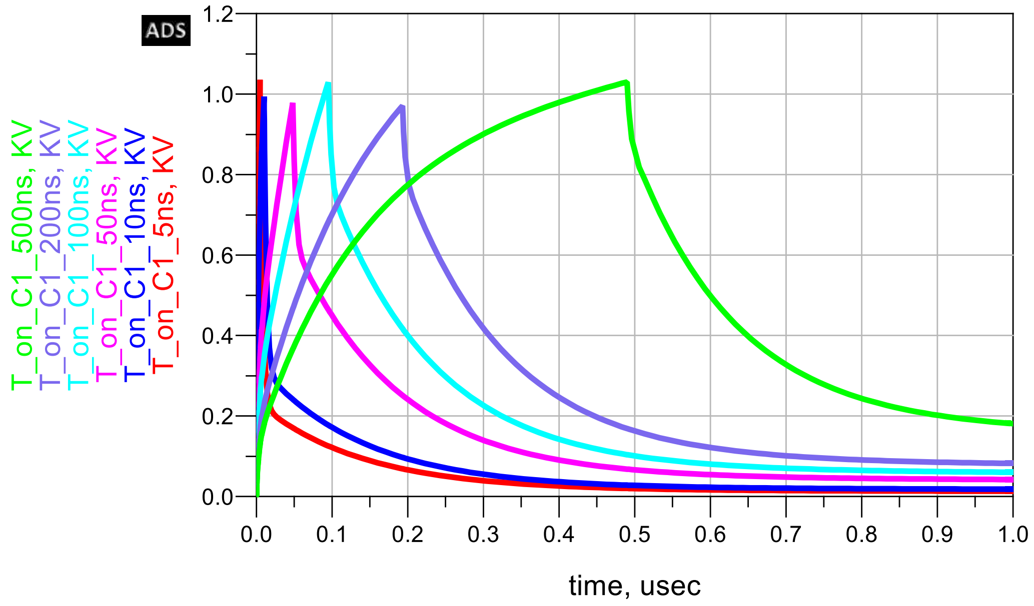
The power-to-failure (P_f) values are used as the input power of the thermal network P_0, and the pulse widths are used as the time-to-failure (t_f). Since it is observed that thermal failure happens at the end of each pulse, the P_0 and pulse widths are used as boundary conditions. Then the values of capacitors and resistors can be determined with an optimized method and Advanced Design System (ADS) software. The extracted capacitor and resistor values are listed in Table 2-2.

Table 2-2 Comparison of devices on key ESD parameters.

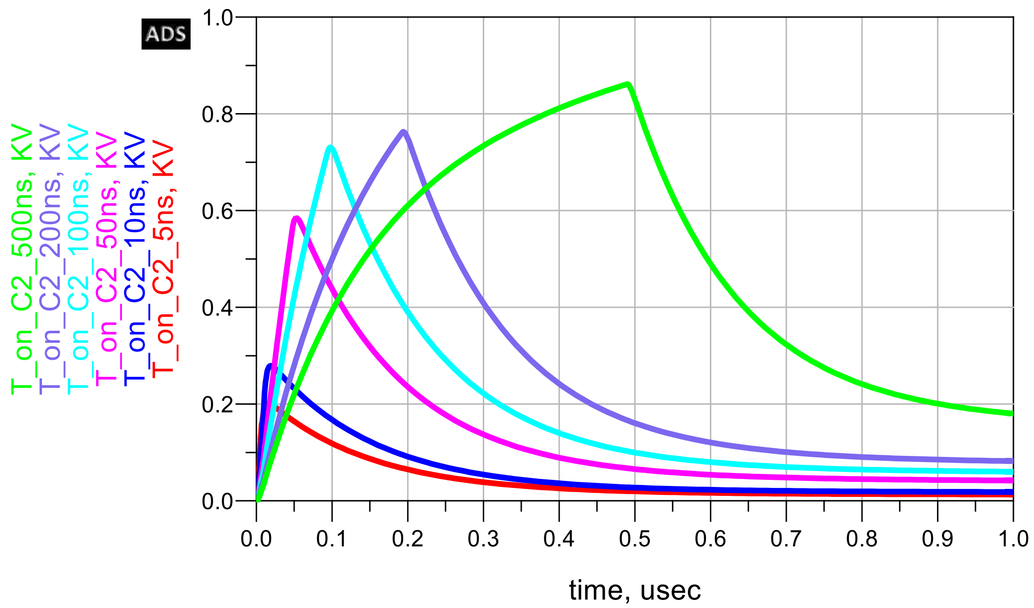
Parameters	C1	R1	C2	R2	C3	R3
forward	0.0703	54.81	0.492	262.15	8.306	964.11
reversed	0.0107	71.04	0.404	108.66	7.203	131.58

2.3 Modeling Validation

With the boundary conditions of pulse widths and power-to-failure, and the extracted capacitor and resistor values in Table 2-2, the device thermal failure can be evaluated as power-to-failure at a time-to-failure. The temperature simulation ressults on capacitor C1, C2 and C3 are shown in Figure 2-7(a), (b) and (c), respectively. From the simulation results in Figure 2-7, it can be shown that the temperature distribution matches the physical mechenisms. Namely, the temperature on C1 reaches the preset failure temperature 1000 at each pulse end, and the temperature on C2 and C3 are higher for longer pulses. It can be proved that the mapped electrical circuit has good correlation with the physics.



(a)



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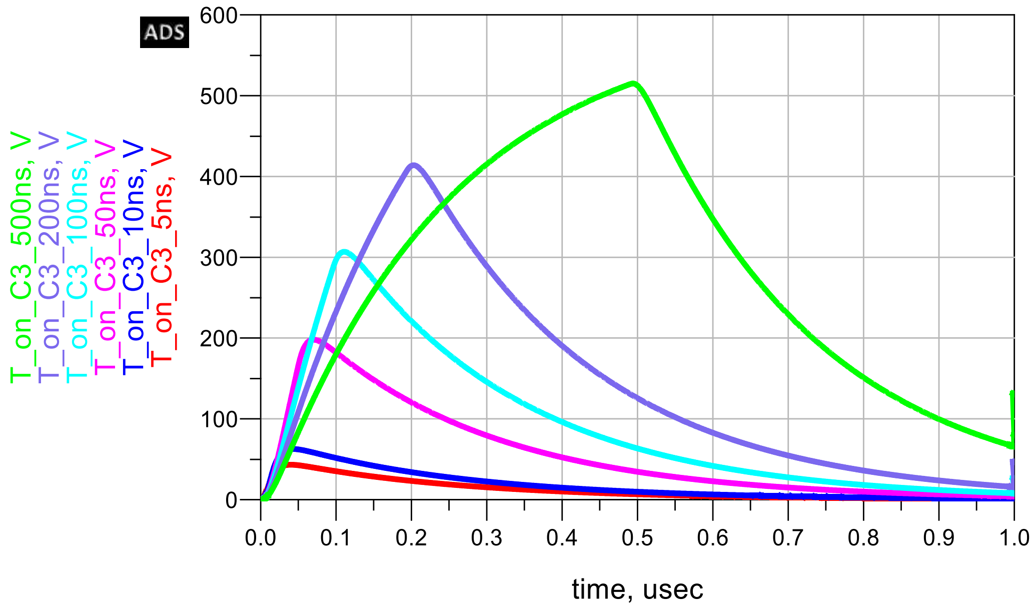


(c)

Figure 2-7 Temperature simulation results on C1 (a), C2 (b), and C3 (c).

The thermal failure model can be implemented with Verilog-A, and enable to be integrated in SPICE model simulators. As an example, the diode schematic with thermal failure monitor model embedded is shown in Figure 2-8. The thermal monitor model has three terminals. PIV and NV are used to sense the votlage across the devcie, while PIV and PI are used to sense the current flow through the device. The sensed votlage and current are used to generate the input power of the thermal network. Since the diode in forward bias condition is much more complex due to the physical effects in high-current and high-voltage region, the P-N junction diode is connected as reversed bias to verify the thermal failure model. When the monitored temperature reaches the preset failure temperature, the failure monitor will make the bypass switch to be closed. Then a low resistance path is formed from the diode anode to the cathode.

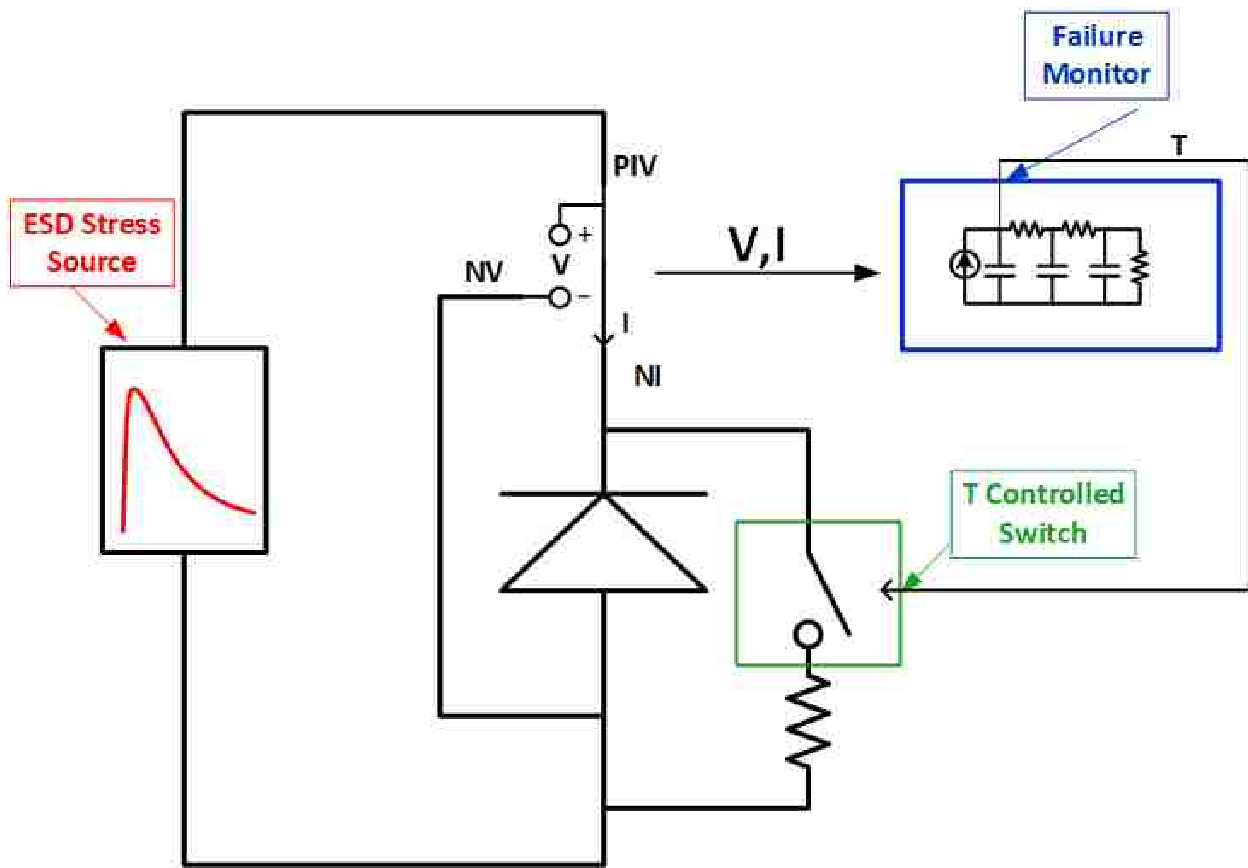


Figure 2-8 Diode schematic for simulation with thermal failure monitor model embedded

The simulated and measured voltage and current transient waveforms of the P-N junction diode and the simulated temperature on C1, C2 and C3 of the thermal network are shown in Figure 2-9. The pulse widths using for modeling verification is 50ns. In the schematic, a standard induraty diode model is used for verification, as shown in Figure 2-10. And the thermal network is implemented with Verilog-A. As the simulated results shows, the voltage drop suddenly while the current increase dramatically at the momment of 38ns. On the other hand, the temperature on C1 reaches the preset failure temperature 1000, indicating failure at the time point. The thermal failure model is valid for any types of transient stress waveforms.

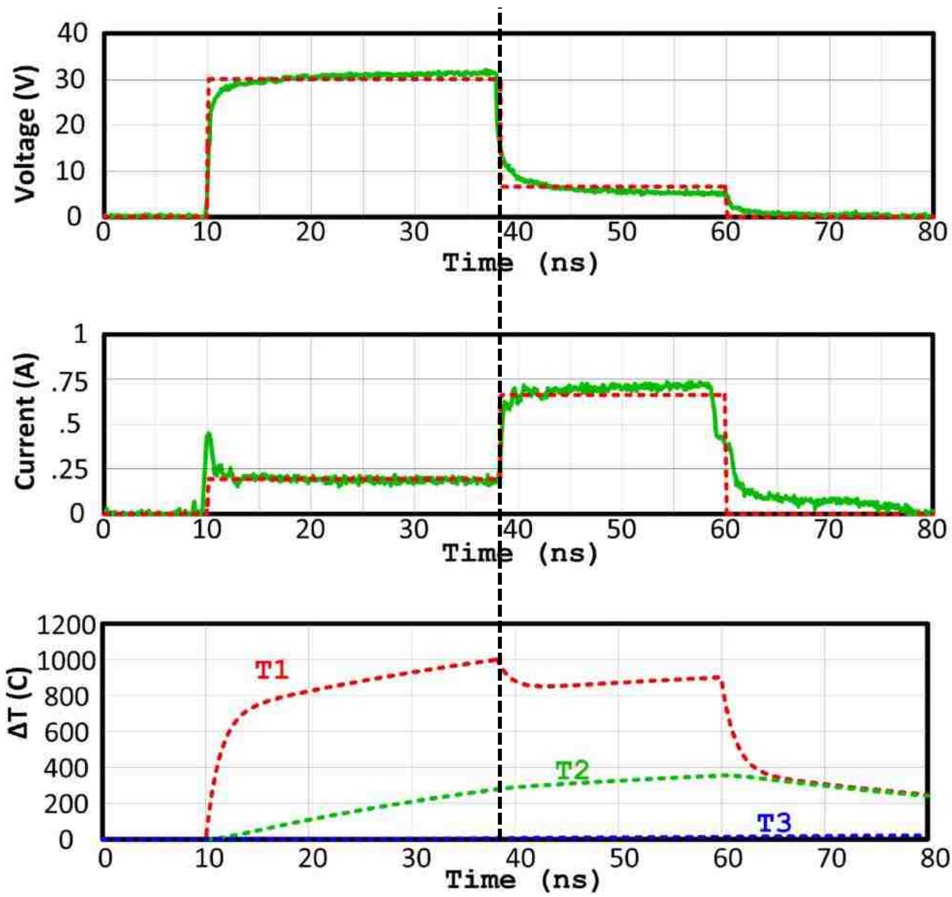


Figure 2-9 Simulated and Measured voltage & current transient waveforms, and simulated temperature on capacitors of the thermal network.

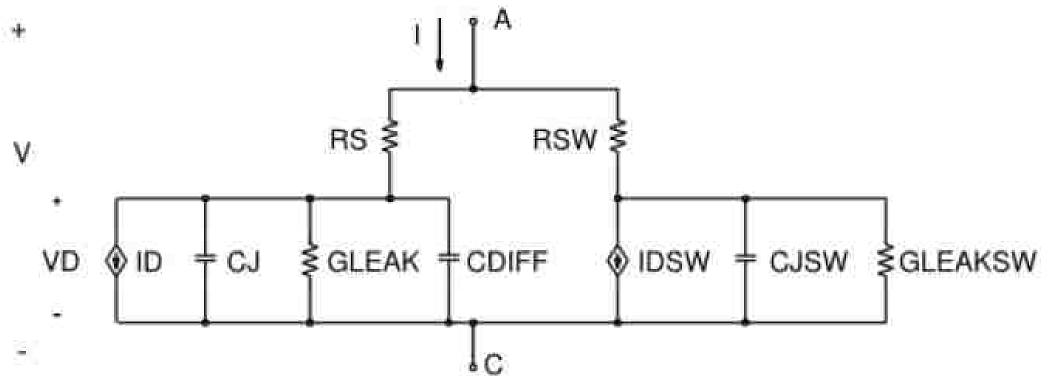


Figure 2-10 Diode industry available model.

2.4 Conclusion

In this chapter, a compact model is developed to predict the device thermal failure under ESD stress conditions. The model is based on the heat diffusion equation and is able to match the physical mechanisms. The failure model is implemented with a 3-stage thermal network, and the associated parameters are extracted with an optimized based methodology. The device geometry is accounted for by the 3-stage thermal network. The proposed model can not only monitor the temperature rise, but also predict the thermal failure at the hotspot under ESD stress conditions. The proposed failure model is compatible with industry SPICE models and can be used in the mainstream SPICE simulators. Moreover, the proposed failure model is valid for any types of ESD transient stresses, from CDM to HBM timeframe.

CHAPTER 3 MODELING AND SIMULATION OF COMPREHENSIVE DIODE BEHAVIOR UNDER ESD STRESSES

3.1 Introduction

Although SPICE models are available in industry circuit simulators and are enough to reproduce the device performance in most circuit design cases, simulations under ESD stress conditions are still difficult [36]. Since under ESD stress conditions, devices do not operate in the normal operating regions. Instead, the devices are pushed into a high-voltage, high-current operating region, in which many physical effects impact. However, standard SPICE models do not include the ESD-unique characteristics [37]-[42].

Diodes are efficient and simplest ESD protection devices, and P-N junction structure widely exists in ESD protection devices. Since diode has the basic capability for ESD energy dissipation and P-N junction is the fundamental part in most ESD protection devices, it is first to be modeled for ESD conditions.

Under high-current high-voltage stress conditions, the device performance will degrade. If the simulation during design stage is implemented with conventional device models, the designed ESD protection cell is not reliable [43]. It has observed that in high voltage and/or high current region, the diode on-resistance will increase dramatically. With the increasing stress level, the device eventually reaches the thermal failure point and irreversible damage happens [44]. The diode model for ESD stress conditions should be able to include the on-resistance variation. For transient stresses with fast rise time, the voltage overshoot is observed at the beginning of the stress [44]. The modeling for overshoot phenomenon is significant, since the peak voltage may damage the core circuits if the ESD protection cells cannot be turned on fast enough [45].

In order to reproduce the on-resistance variation in high current region, M. Stockingger and M.G. Khazhinsky proposed a diode model including self-heating effect with embedding the temperature detector and replace the series resistor in diode model by a various resistor which is controlled by the temperature detector [46]-[48]. However, the on-resistance variation cannot be explained by the self-heating effect only, especially for the short pulse stresses. Moreover, the voltage overshoot phenomenon cannot be packaged into one single model.

In this chapter, the developed diode comprehensive model is discussed. The model is built with several compact model elements, and it is able to simulate all physical phenomena for ESD stress conditions. The voltage overshoot phenomenon is modeled by the diode turn-on delay; the on-resistance variation is modeled with self-heating effect and velocity saturation; by introducing a failure temperature and adding a thermal failure monitor model, the diode thermal failure can be predicted during simulation.

3.2 Diode Comprehensive Modeling Methodology

To include all the physical phenomena for ESD conditions, voltage overshoot, dynamic on-resistance, and junction thermal failure are modeled. Figure 3-1 shows the overall equivalent schematic of the proposed comprehensive diode model. The overall schematic consists of a primary diode model element, a non-linear resistor model element, a thermal network and a short-circuit resistor. The primary diode model is a large signal diode model, and the equivalent circuit is shown in Figure 3-2. The primary diode model is used to simulate the diode behavior from low current to high current region. And the overshoot phenomenon is also modeled within the primary diode model element with the series resistor Rs.

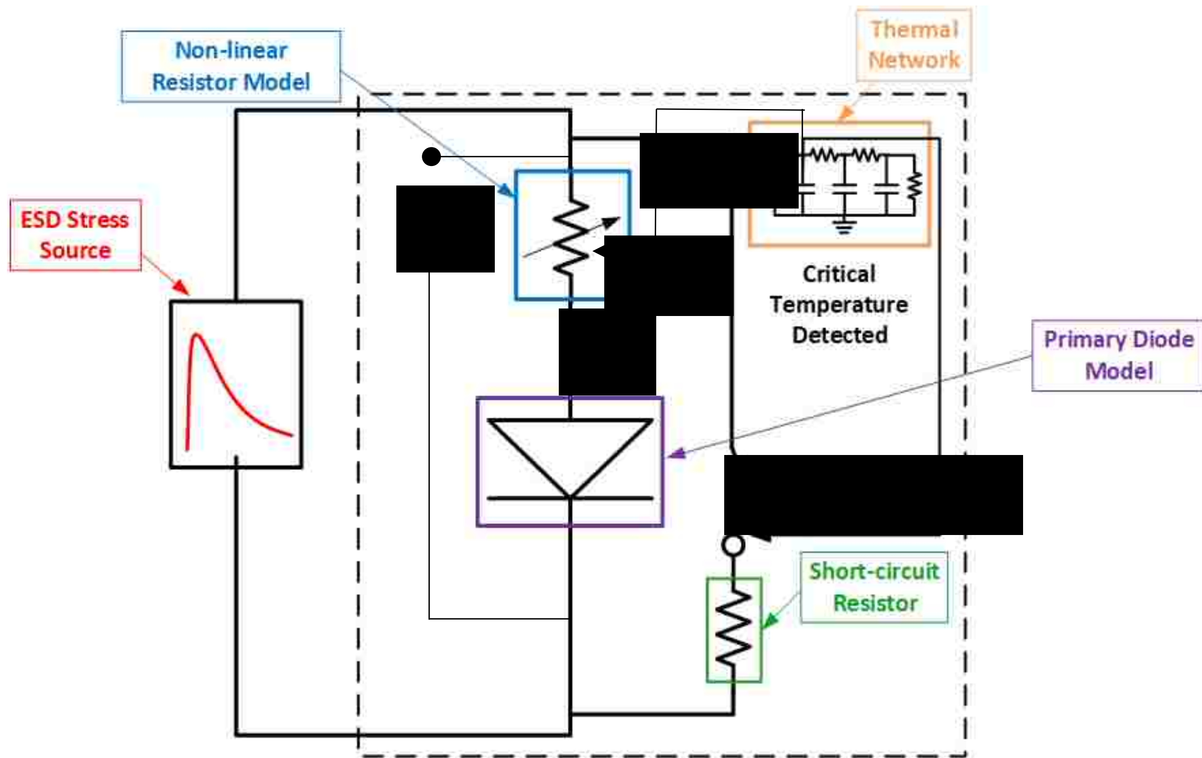


Figure 3-1 Overall equivalent circuit for the comprehensive diode model.

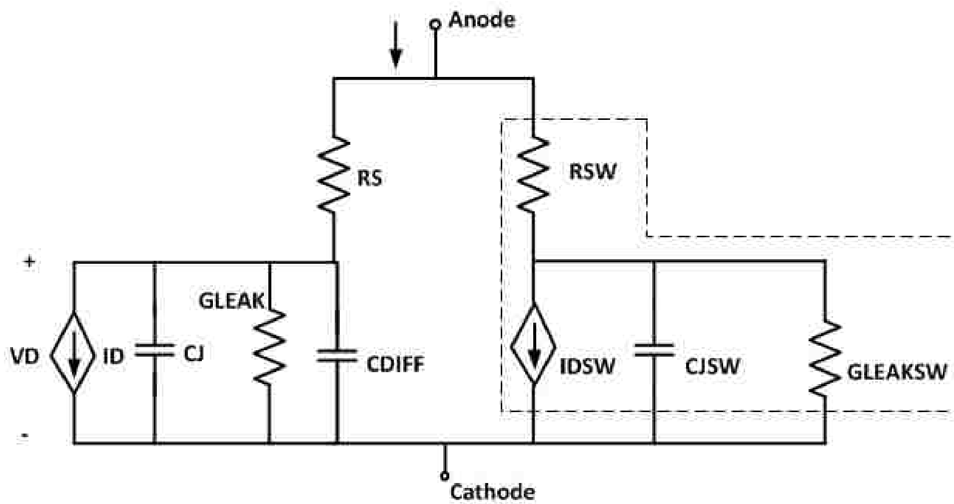


Figure 3-2 Equivalent circuit of primary diode model.

The non-linear resistor is a 3-terminal variable resistor with velocity saturation packed inside, controlled by the temperature signal, which is used to address the dynamic on-resistance in high current region. The thermal network is the 3-stage thermal network introduced in Chapter 2, and the circuit is shown in Figure 2-5. The thermal network is employed to detect the self-heating effect, namely, temperature rise, and monitor thermal failure during ESD stresses.

3.2.1 Modeling of Voltage Overshoot at Diode Forward Turn-On

The voltage overshoot phenomenon is caused by the turn-on delay of the diode [49], [50]. Due to the conductivity modulation in the diode quasi-neutral region, the diode cannot be turned on immediately. The turn-on delay is modeled by introducing the series resistor Rs [51],

$$R_S = R_{S0} + \frac{R_{SM}}{1 + {Q_M}/{Q_0}} \tag{3.1}$$

Where R_{s0} is the constant resistance part to account for the resistance of metal, interconnections and P+ and N+ region. The second part on the right hand is the modulated resistance, the modulated region is lightly doped Nwell for a P+/Nwell diode. Before conductivity modulation, the resistance is R_{SM}. Q_0 is the threshold charge for conductivity modulation, Q_M is the modulated charge in the quasi-neutral region. The modulated charge is linked with transit time and conduction current [52],

$$Q_M = \tau \cdot I_d \tag{3.2}$$

$$Q_0 = \gamma q N_A w A \tag{3.3}$$

Where τ is the carrier transit time in the neutral region, I_d is the junction conduction current, w and A are dimension parameters, N_A is the doping concentration in the lightly doped region, γ represents the average distance between N+ and P+ doped region. When the fabrication parameters

are not available, the corresponding parameters can be extracted by fitting the simulated results to the measurement. The diode current is modeled by three components, a junction conduction current I_d, a diffusion current I_{diff} corresponding to the charge in the well region, and a displacement current I_{dep} due to the depletion capacitance. I_{dep} has no impact in the conductivity modulation. When the diode is switched on initially, I_d is very small and I_{diff} is the dominant current, the modulated charge Q_M cannot be established before conductivity modulation [53]. Therefore, the voltage overshoot is built up across the junction due to the initial low conductivity in the lightly doped region. The peak voltage value is defined as R_{S0}+R_{SM}.

$$I_d = I_s\left(\exp\left(\frac{V_D}{V_T}\right) - 1\right) \tag{3.4}$$

$$I_{diff} = \frac{d(Q_D)}{dt} \tag{3.5}$$

$$I_{dep} = C_J\frac{d(V_D)}{dt} \tag{3.6}$$

3.2.2 Failure Prediction and Temperature Monitor

As discussed in Chapter 2, the device temperature rises due to self-heating effect during the ESD stress. If the temperature keeps rising, thermal failure will be reached at the hotspot finally. It is helpful to monitor the device temperature rising and predict the thermal failure during simulation, since it will reduce the design cycle time and design cost. And the robustness of ESD protection cell can be evaluated by SPICE simulator.

The thermal network in Figure 2-5 is used as the temperature monitor and failure prediction. For short transient ESD stresses, the silicon region cannot be heated evenly, so multiple-stage structure is used to model the heating gradient. And to balance the computational complexity, 3

stages are employed. As discussed in Chapter 2, the diode can be divided in to 3 thermal regions, and the capacitors C1, C2 and C3 reprent the 3 thermal regions. The failure tempreture is preset as 1000. When the temperature on C1 reaches the critical value, flag rises that the device is damaged. With the boundary conditions of input power and pulse widths, the values of capacitors and resistors are obtained with the optimization based parameter extraction methodology [54].

3.2.3 On-resistance Variation

As shown in Figure 3-3, the diode on-resistance is not always a constant. However, the on-resistance increases in high current operaitng region, causing the I-V characteristics bending. It can be observed that the on-resistance increases dramatically near the failure point. A number of TLP measurements are performed with different pulse widths from 5ns to 500ns, the diode shows up different saturation characteristics. For long pulse TLP stresses, the curve bending starting point is earlier than the short pulse ones.

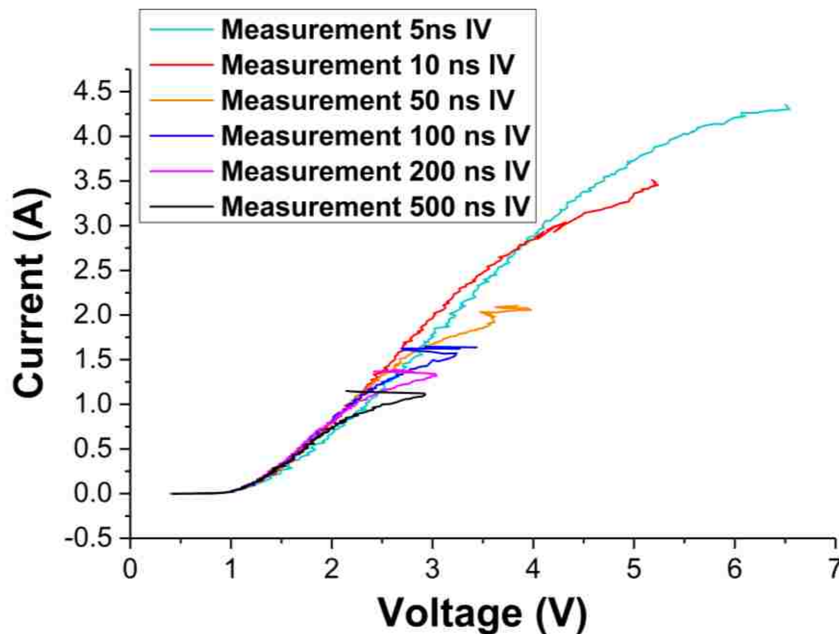


Figure 3-3 Measured TLP I-V curves under different pulse widths, ranging from 5ns to 500ns.

In previous research work, the on-resistance variation is modeled by self-heating effect. However, the I-V curve saturation cannot be explained by self-heating effect only. For short pulse stresses, there is no significant self-heating effect, so it is not appropriate to model the dynamic on-resistance for short pulses. It is believed that there are two main mechanism accounting for the I-V saturation, one is self-heating effect, the other is velocity saturation at high electrical field. As an example, the 500ns TLP measured voltage transient waveform is shown in Figure 3-4. The votlage ramps up with time, indicating the on-resistance increasing obvioiulsy. For the long pulse stress, self-heating effect is the dominant reason resulting the on-resistance variation.

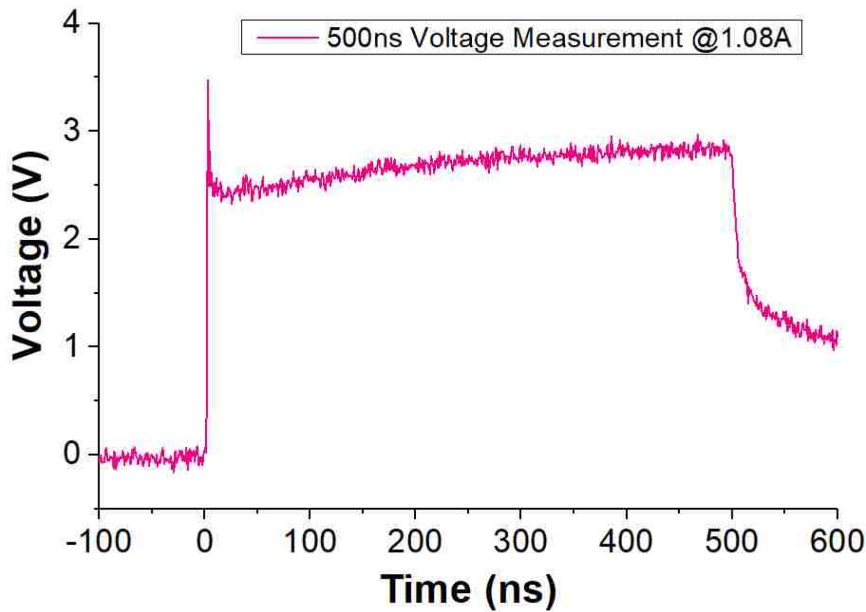
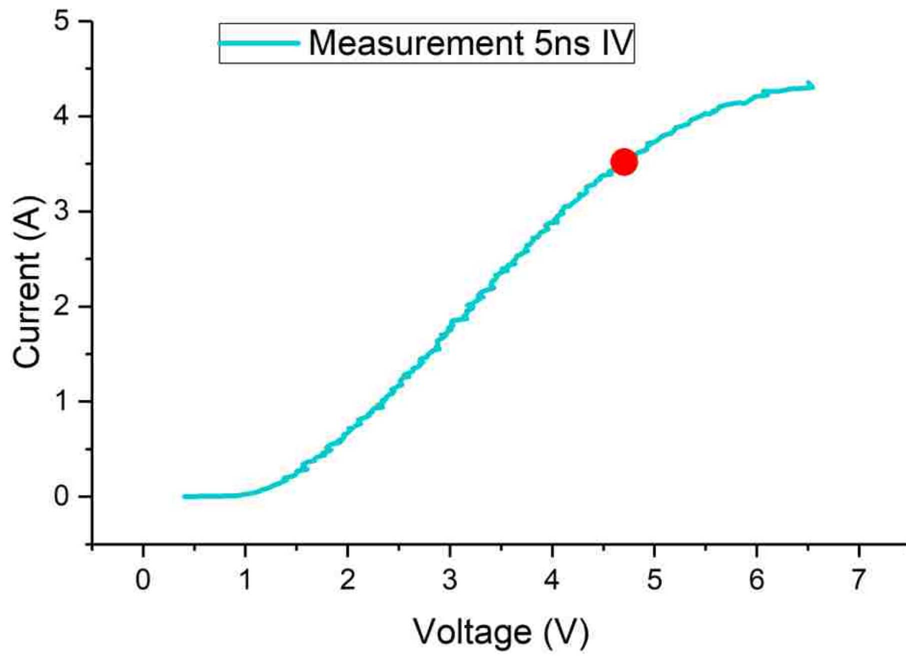
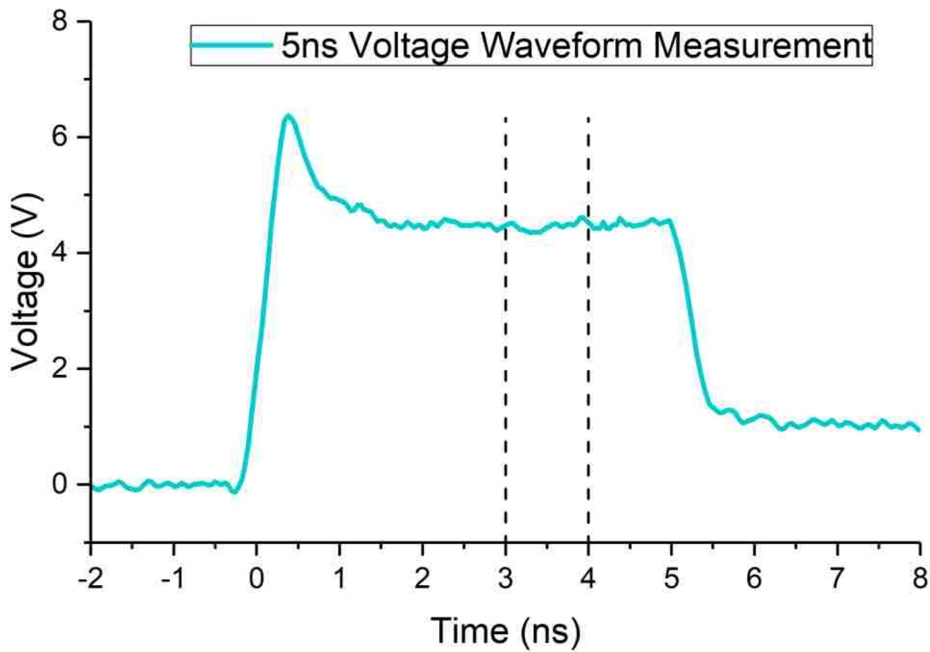


Figure 3-4 500ns TLP measured transient voltage waveform.

On the other hand, the velocity saturation can be observed for short pulse stresses. As an example, a 5ns TLP measured quasi static I-V characteristic is shown in Figure 3-5(a). obvious bending can be observed after 4V. The voltage transient waveform corresponding to the red point is shown in Figure 3-5 (b).



(a)

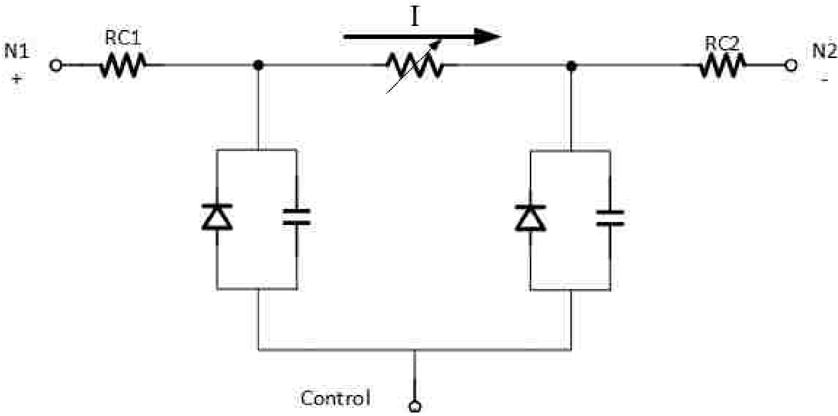


(b)

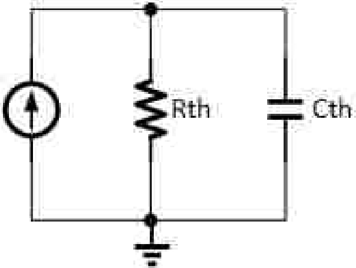
Figure 3-5 (a) Measured TLP I-V curve for 5ns pulse width stress, (b) measured transient voltage waveform for the red point.

From Figure 3-5 (b), the transient voltage waveform corresponding to the red point is flat after overshoot, which does not agree with the self-heating effect. Since self-heating effect is time dependent. Therefore, it can be proved that there is no significant self-heating effect for the 5ns pulse width stress. So, the I-V curve bending, namely, the on-resistance variation for short pulse stress is because of velocity saturation.

The self-heating and velocity saturation are packed into the non-linear resistor model element, shown in the overall equivalent schematic. The non-linear resistor model element is built based on CMC-R3 resistor model. The three terminal resistor model is shown in Figure 3-6 [55].



(a)



(b)

Figure 3-6 (a) Equivalent schematic of CMC-R3 model, (b) Thermal monitor for CMC-R3 model.

The 3-terminal resistor is controlled by the temperature signal, the diodes and capacitors are used to model the parasitic effect of diffusion resistor and poly resistor, respectively. In this chapter, the thermal monitor is replaced by the 3-stage thermal network described in Chapter 2. The input of the thermal network is the current flow through the diode and the voltage across the diode, on the other hand, the output of the thermal network is the temperature signal which is used to control the variable resistor inside the 3-terminal resistor model.

An empirical equation is introduced to estimate the resistance dependency on temperature,

$$R = R_0 \cdot (1 + \alpha \cdot \Delta T + \beta \cdot \Delta T^2) \tag{3.7}$$

Where R_0 is the normalized resistance at the ambient temperature without any electrical stresses. ΔT is the temperature increment in the device. α and β are linear and quadratic temperature coefficients, and both of them are fitting parameters. Both α and β are positive parameters, because the lattice vibration is enhanced when temperature increases, leading to higher ionic scattering. As a result, the carrier mobility degrades [56].

As to the velocity saturation, it is because the probability of carriers scattered by lattice at the high electrical field increase, making the carriers' mobility to degrade. After the critical value of velocity saturation is reached, the mobility of carriers cannot move faster even higher voltage is applied. To model the velocity saturation, a parameter named effective mobility reduction factor is introduced [57].

$$\mu_{red}(E) = \mu_0 / \mu(E) \tag{3.8}$$

When the electrical field E=0, $\mu(0) = \mu_0$, and $\mu_{red}(0) = 1$. As described in CMC-R3 model, the mobility reduction factor can be modeled with an empirical equation, and the degradation of conductivity is expressed as [58],

$$g = \frac{1}{R_0} \cdot \frac{1}{\mu_{red}} \tag{3.9}$$

$$\mu_{red} = 1 + \sqrt{\left(\frac{E-E_{C,eff}}{2E_{crit}}\right) + \frac{DU \cdot E_{C,eff}}{E_{crit}}} + \sqrt{\left(\frac{E+E_{C,eff}}{2E_{crit}}\right) + \frac{DU \cdot E_{C,eff}}{E_{crit}}} - \sqrt{\left(\frac{E_{C,eff}}{E_{crit}}\right)^2 + \frac{4 \cdot DU \cdot E_{C,eff}}{E_{crit}}} \tag{3.10}$$

$$E_{C,eff} = \sqrt{E_{corn}^2 + \left(2 \cdot DU \cdot E_{crit}\right)^2} - (2 \cdot DU \cdot E_{crit}) \tag{3.11}$$

Where E_{crit} is the critical value of electrical field to cause the velocity saturation, $E_{C,eff}$ is the effective electrical filed across the junction, E_{corn} is the velocity saturation corner field strength, DU is fitting parameter.

As discussed above, with both self-heating effect and velocity saturation included, the non-linear part of the resistor can be expressed as,

$$R_{non-linear} = R_0(\alpha \cdot \Delta T + \beta \cdot \Delta T^2) + R_0(\mu_{red} - 1) \tag{3.12}$$

The TLP I-V curves are obtained by averaging the transient voltage and current waveforms in the static region. Long pulse stresses can heat the device long time, causing the temperature at the pulse end is higher than the short pulse stresses. Shown in the I-V curves, the long pulse curve bends earlier than the short ones. On the other hand, for short pulse stresses, the velocity saturation is the dominant reason for on-resistance variation.

3.3 Measurement and Simulation Validation

In order to verify the validity of the proposed comprehensive diode model. An STI diode is fabricated on a baseline 0.18μm CMOS technology process. The diode is an N+/Pwell diode with single finger structure, and the area of diode is 25 μm × 25 μm, and the space between N+ and P+ is 0.6 μm. The measurement is conducted with a High Power Pulse Instrument (HPPT)

TLP system with 50Ω impedance. The rise time is fixed to 0.3 ns, and pulse widths vary from 5ns to 500ns. On the other hand, simulation is conducted with a SPICE like simulator. Since the model proposed is targeted on the transient waveforms, So the simulation is just like the TLP measurement. A sequence of TLP pulses are applied on the device, and the I-V curves are extracted by averaging the transient waveforms.

To verify the voltage overshoot modeling, a 10ns pulse width 0.3ns rise time TLP testing is performed. The corresponding parameters are obtained by fitting the measured results with simulation. Figure 3-7 shows the comparison of simulated and measured current – peak voltage characteristics. Note that the simulation is able to reproduce the measurement, which means that the overshoot model is vaild in the whole operating region. Note that the I-peak V curve starts bending after point B, this can be explained with velocity saturation.

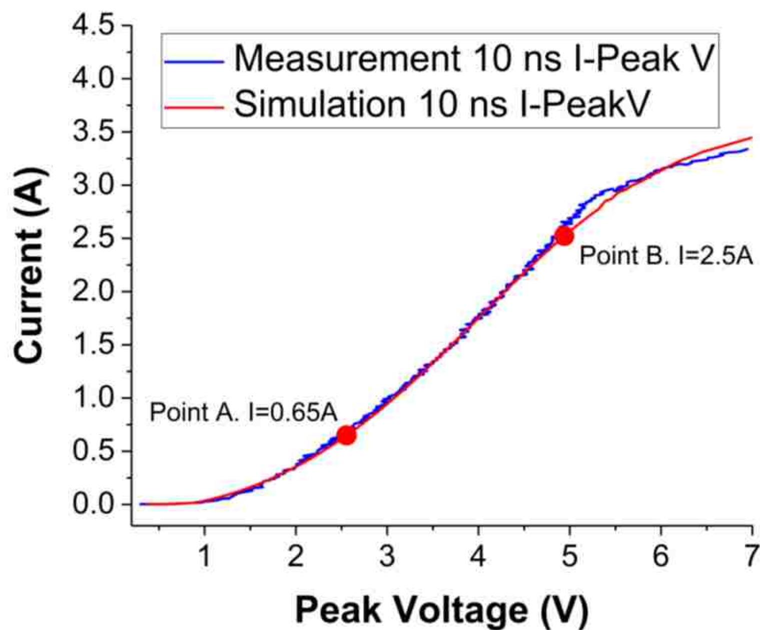
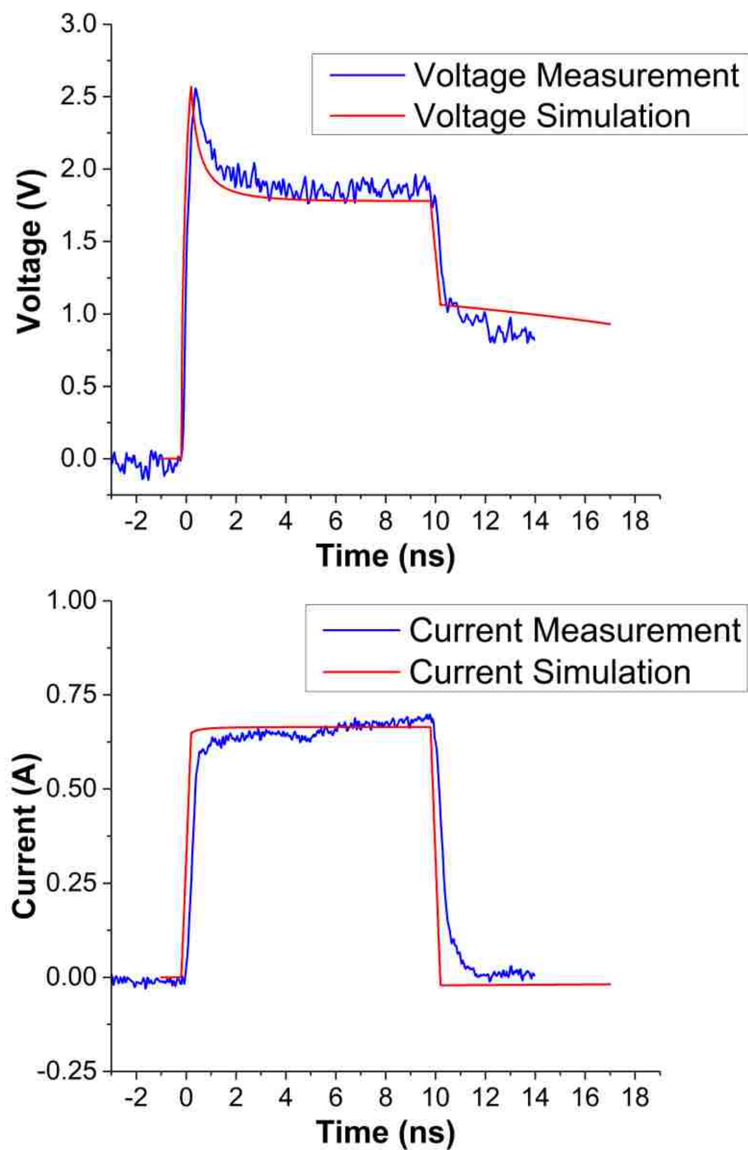
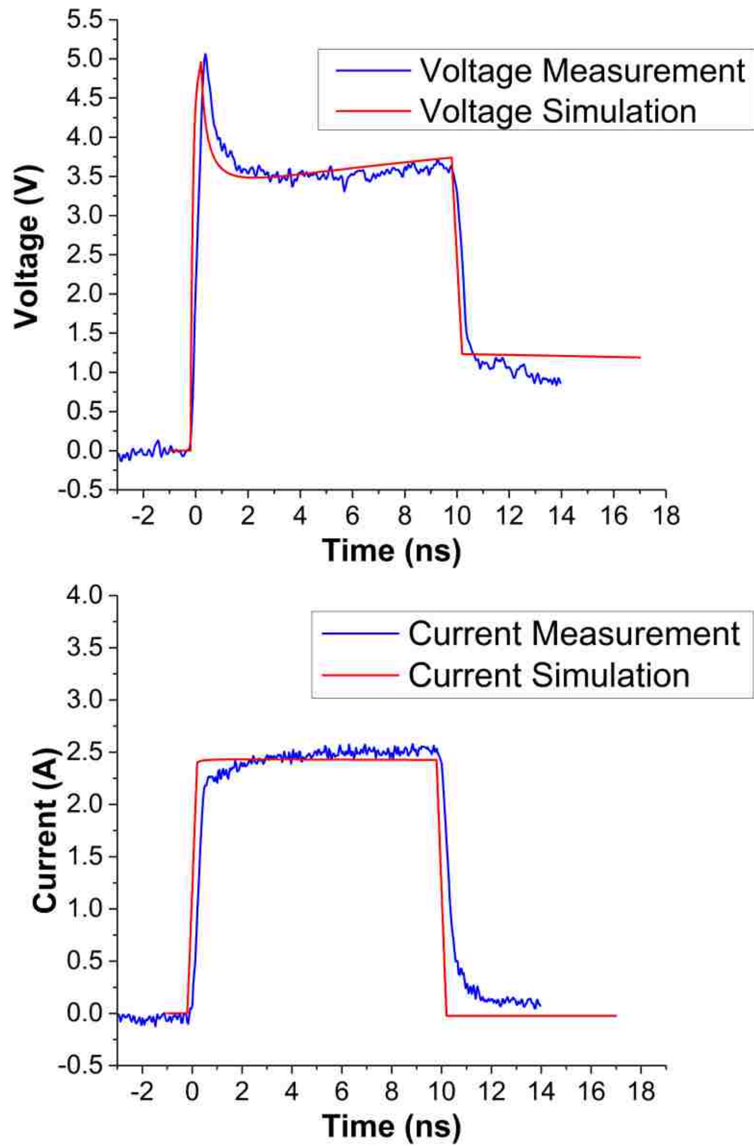


Figure 3-7 TLP current-peak voltage characteristics simulation fit with measurement, Point A at the current of 0.65A, Point B at the current of 2.5A.

The measured and simulated voltage and current transient waveforms associated with Point A and Point B in Figure 3-7 are shown in Figure 3-8 (a) and Figure 3-8 (b), at current level of 0.65A and 2.5A, respectively. The voltage overshoot can be reproduced well. The voltage peak begins at the beginning of waveform and lasts about 1ns. After overshoot, the waveform goes to flat, and the peak voltage is around 40% higher than the static region.



(a)



(b)

Figure 3-8 Measured and simulated transient voltage (upper) and current (lower) waveforms with voltage overshoot peak, (a) waveform at Point A, when current is 0.65A, (b) waveform at Point B, when current is 2.5A.

As discussed above, for long pulse widths (50ns – 500ns), self-heating effect will be dominant to cause I-V curve saturation; on the other hand, for short pulse widths (5ns, 10ns),

velocity saturation needs to be considered to model the on-resistance variation. To fit the I-V characteristics well, both self-heating effect and velocity saturation need to be included in the model, and model should be able to valid from low current conduction to high current region. Moreover, the model should be valid for the whole ESD timeframe.

The measured and simulated transient voltage waveforms in high current region for a long pulse stress of 500ns are shown in Figure 3-9. The real time on-resistance variation can be observed, which appears as the voltage ramp-up with time. The on-resistance increasing is more obvious for higher current level.

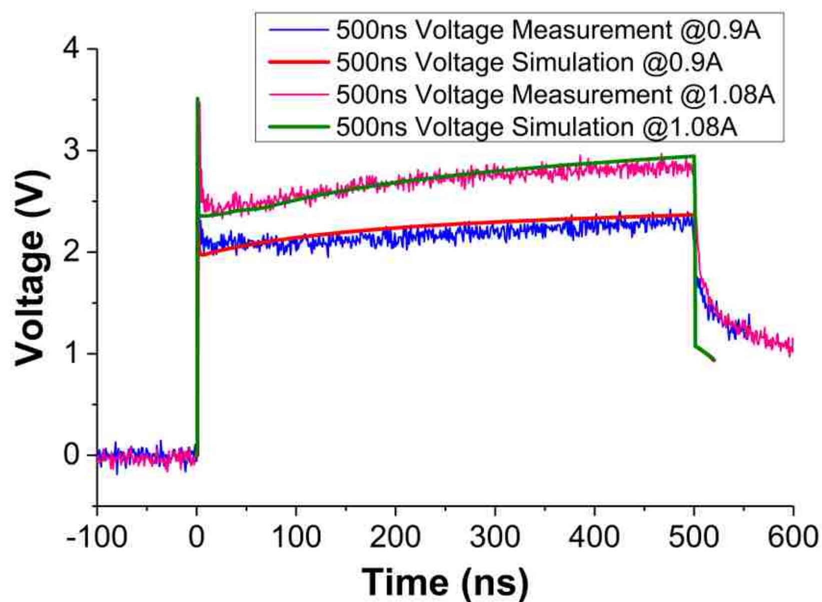
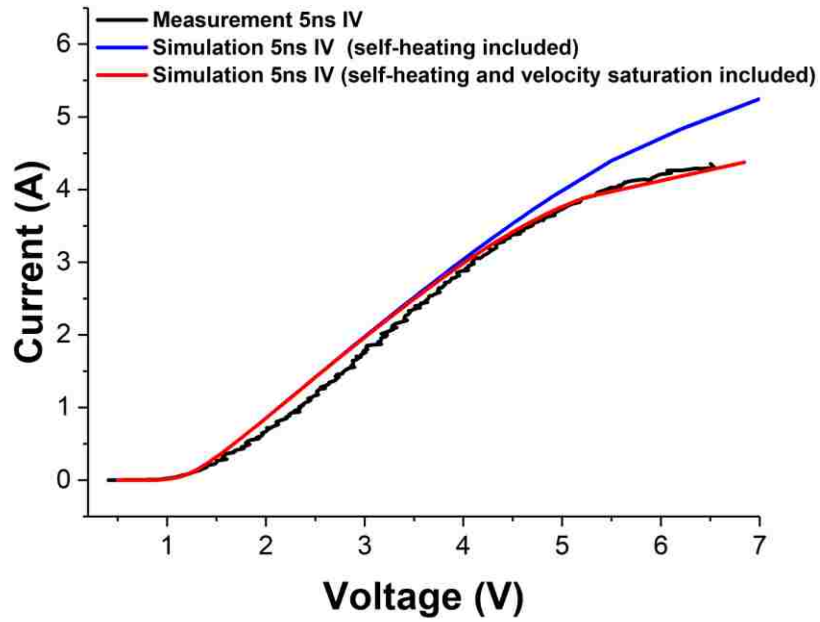
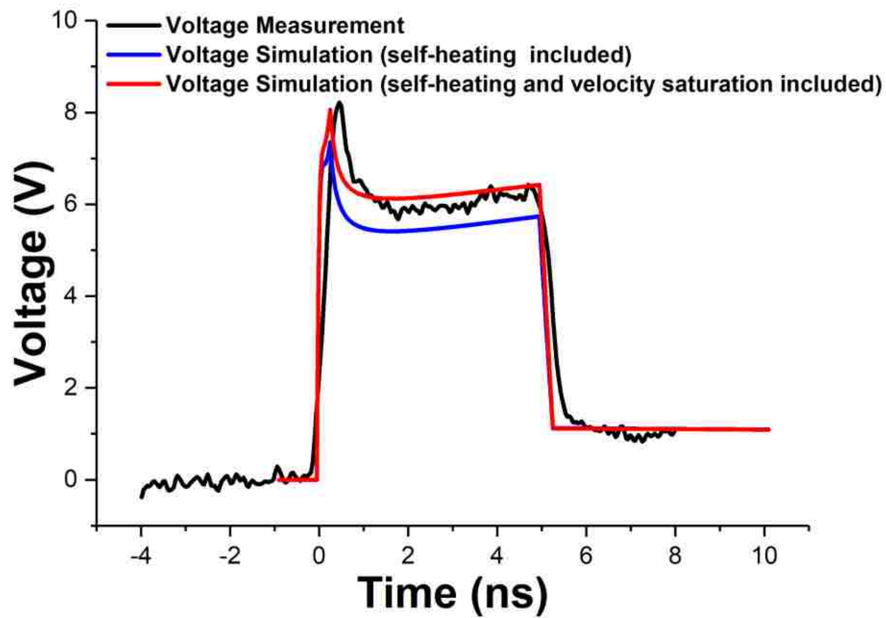


Figure 3-9 Measured and simulated transient voltage in high current region for 500ns TLP, with on-resistance variation.

On the other hand, the on-resistance for short pulse stresses cannot be reproduced by self-heating effect alone. The measured and simulated I-V characteristic for 5ns pulse width is shown in Figure 3-10 (a), the corresponding waveforms is shown in Figure 3-10 (b).

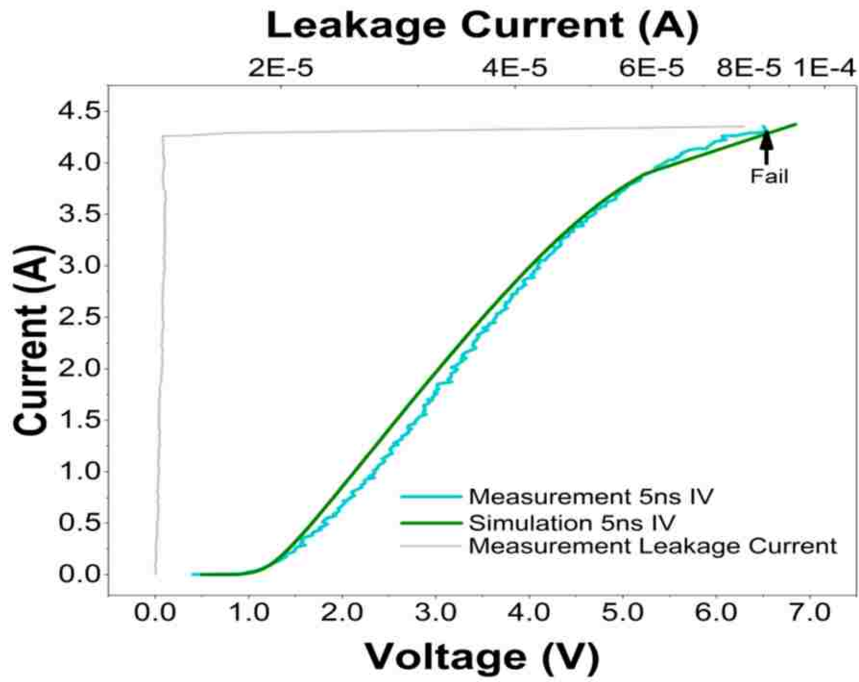


(a)

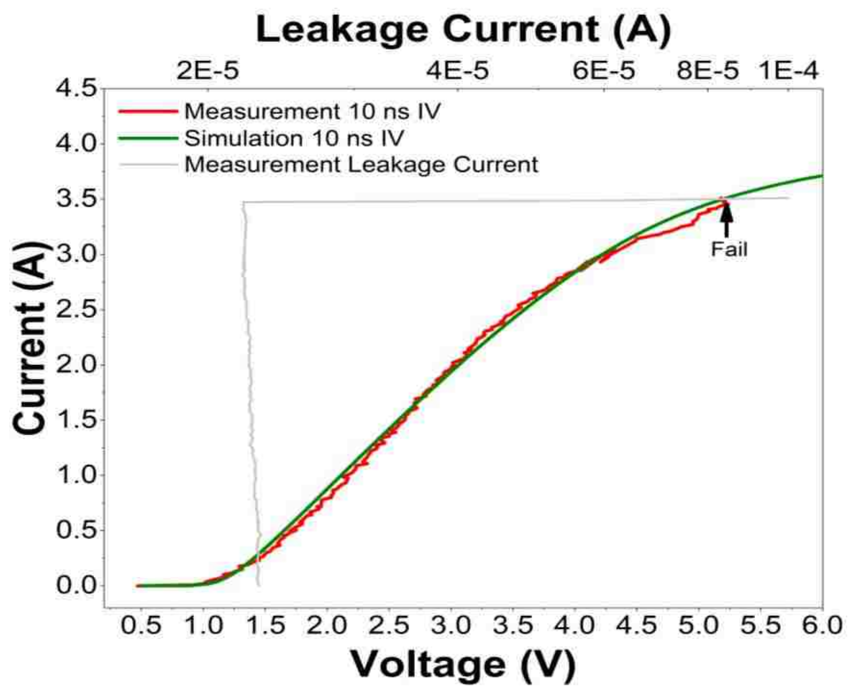


(b)

Figure 3-10 Measured and simulated results only with self-heating effect included and both self-heating and velocity saturation effects included (a) TLP I-V characteristics, (b) voltage waveform at the current level of 4.2A.



(a)



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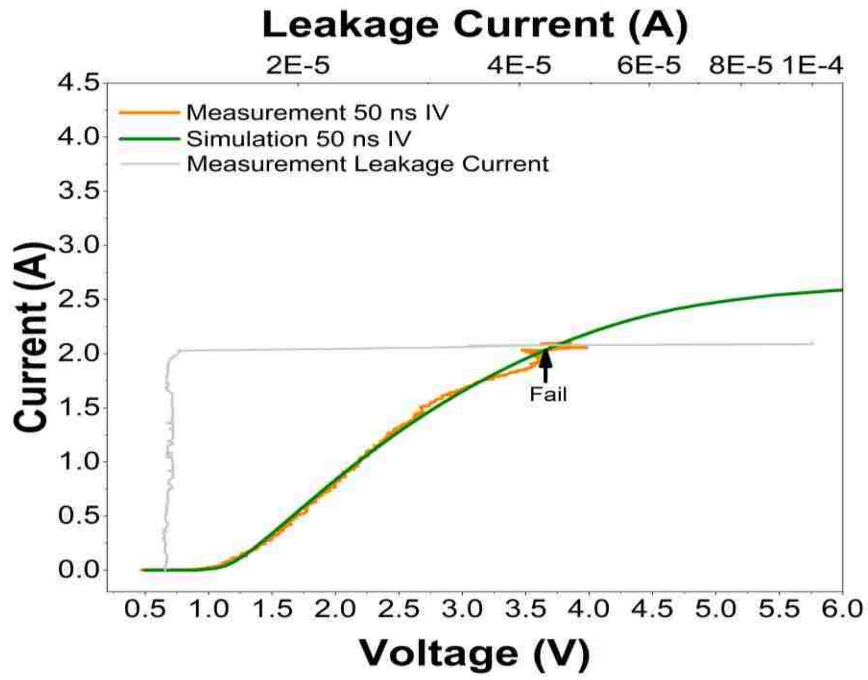
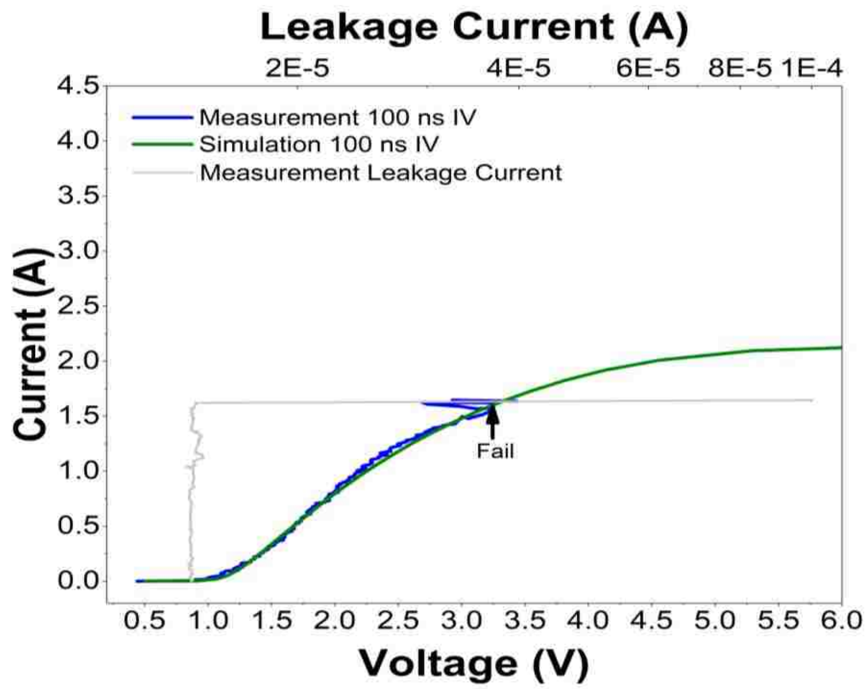
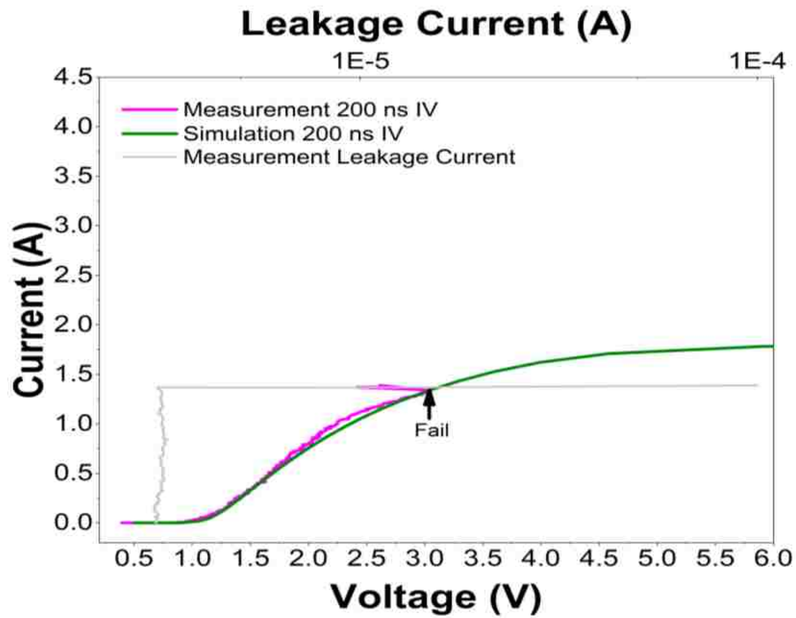


(c)



(d)



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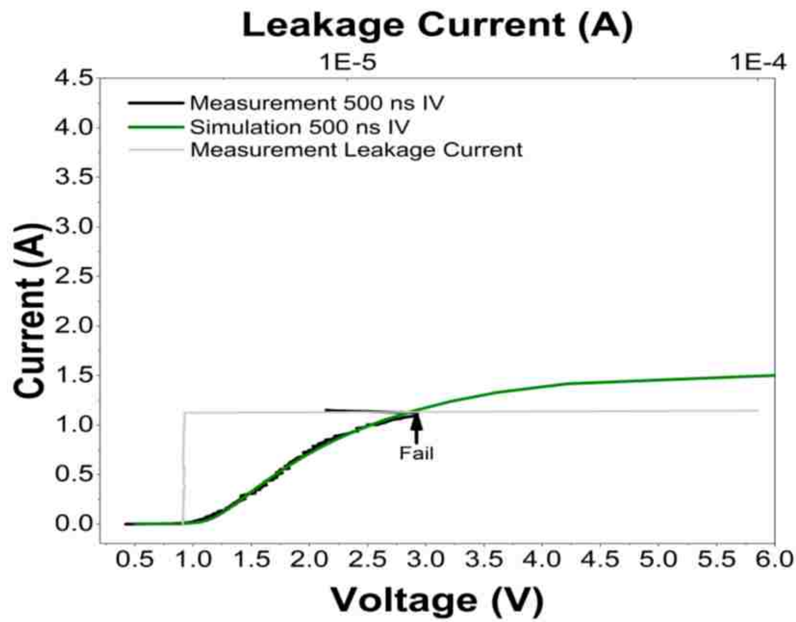


(f)

Figure 3-11 Simulated TLP I-V curve fit with measurement, ranging from 5ns to 500ns.

Figure 3-11 shows the simulated and measured I-V characteristics for different pulse widths, ranging from 5ns to 500ns. With self-heating effect and velocity saturation included, the I-V characteristics with on-resistance variation can be reproduced. The measured leakage current is also shown in Figure 3-11 to indicate the irresistible failure.

To verity the thermal failure monitor, the temperature increment at each pulse end versus voltage is simulated, shown in Figure 3-12. When the temperature at the pulse end reaches the failure temperature 1000, flag is rose to indicate thermal failure. The failure points in measurements is indicated by testing the leakage current after each TLP pulse. When the leakage current increases by several orders, thermal failure is observed. From the results in Figure 3-12, the simulated failure points are able to match the measurement. Figure 3-13 shows the simulation comparison between using standard SPICE model and the proposed diode model.

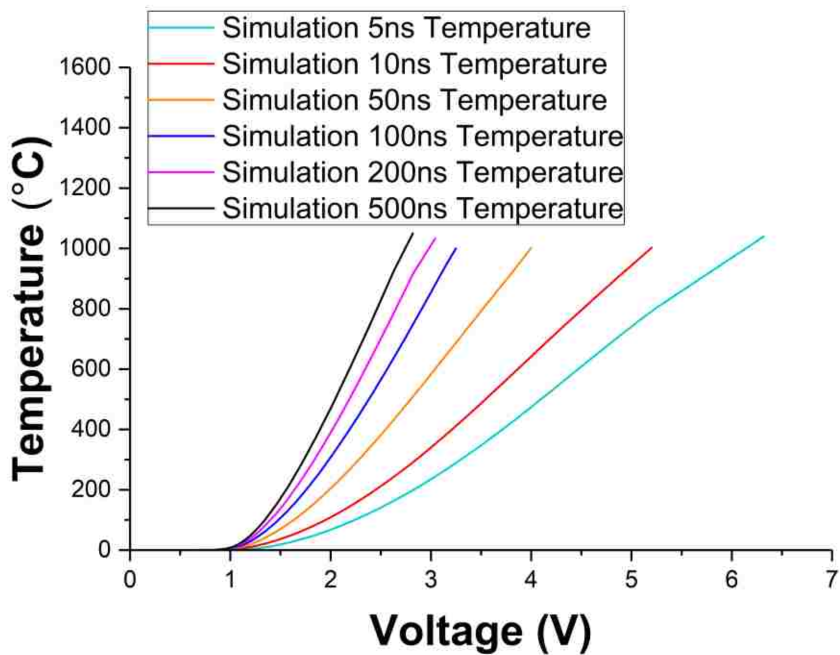
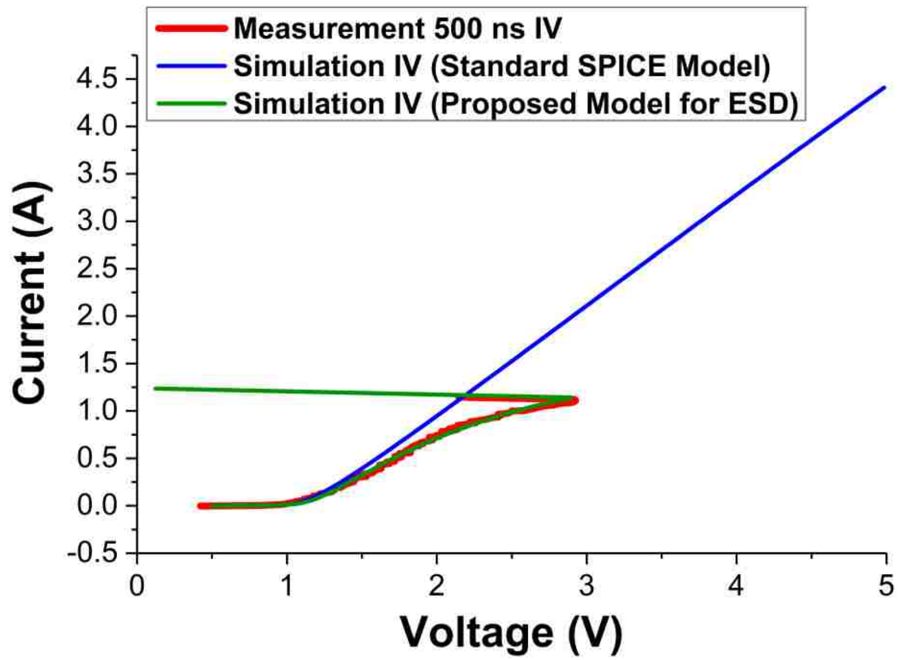
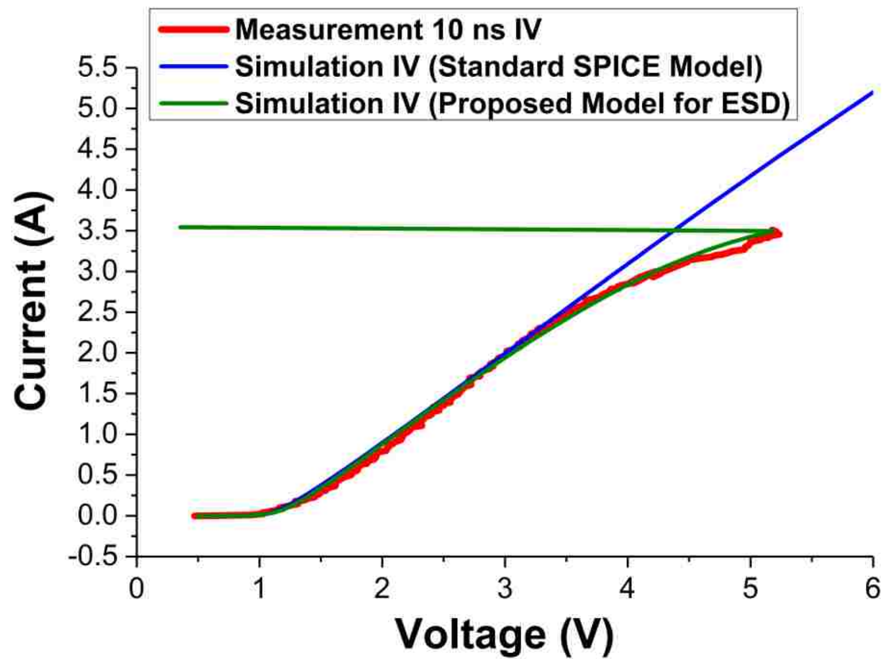


Figure 3-12 Simulated temperature vs. voltage for different pulse widths at the pulse end, the temperature reaches preset failure temperature 1000



(a)



(b)

Figure 3-13 Comparison of simulated I-V curves with standard SPICE model and proposed diode model, (a) long pulse (b) short pulse

3.4 Conclusion

In this chapter, a comprehensive diode model for high current transient event is proposed. The proposed model is verified by fitting the measured results with simulation.

The model is constructed with several compact model elements, including a primary diode model which is a large signal industry available Diode2 model. Inside the primary diode model, the voltage overshoot phenomenon is also packed by introducing a series resistor to reproduce the forward recovery. It is important to simulate the voltage overshoot phenomenon, because the overshoot peak voltage may cause damage to the core circuit if the ESD protection cell does not response quickly enough. The voltage overshoot results from the device turn-on delay, and the overshoot model is able to monitor possible damage caused by the overshoot peak voltage.

With self-heating effect and velocity saturation included in the model, the diode I-V characteristics can be reproduced from turn on, low current normal conduction region to high current region. The on-resistance variation can be modeled in the whole ESD timeframe, like CDM and HBM.

By adding the thermal failure monitor element, the enhanced comprehensive diode model cannot only fit the I-V characteristics well, but also can simulate and predict thermal failure for different pulse widths.

CHAPTER 4 CHARACTERIZATION, MODELING, AND SIMULATION OF POWER-DEFINED TRANSIENT SAFE OPERATING AREA IN LDMOS TRANSISTORS

4.1 Introduction

Safe operating area (SOA) is one of the most important factors to evaluate the performance of the high-voltage transistors. SOA is defined as the region in the I_{ds}-V_{ds} plane in which the high-voltage transistors is able to operate without any damages. The design triangle of high-voltage transistors is shown in Figure 4-1 [59], [60].

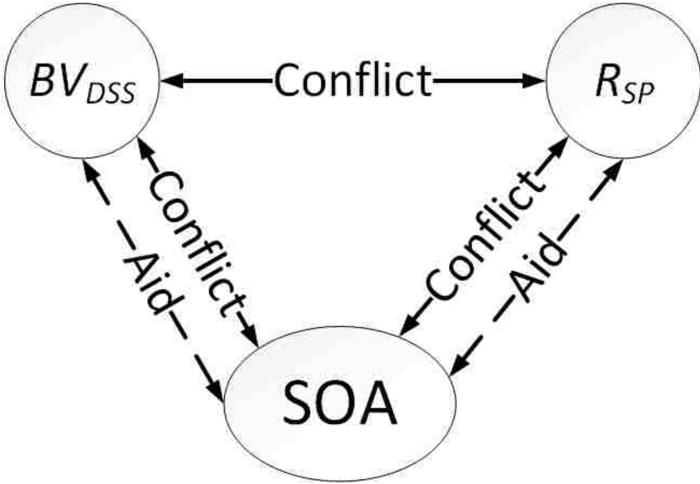


Figure 4-1 Design triangle for high-voltage transistor

The trade-off between the device breakdown voltage (BV_{DSS}) and on-resistance (R_{SP}) has been widely studied, shown in the up "conflict" line in the design triangle. Increasing the device breakdown voltage can improve the high-voltage performance, while the on-resistance will also increase with higher breakdown voltage. As discussed above, improving BV_{DSS} can also improve SOA with penalty of R_{SP}. However, a new technology named "adaptive resurf" can achieve a better shaped SOA by adding a lightly doped n-region to the drain, which is aiding to R_{SP} and conflicting

BV_{DSS} [61]. In order to determine the boundary of SOA, both electrical, thermal and electro-thermal coupling effects needs to be considered [62].

Lateral Double Diffusion MOSFEF (LDMOS) transistors are widely used in power applications and mixed-signal applications due to the good high-voltage performance. Compared with the vertical DMOS structures, LDMOS is easier to be integrated into IC process technology and more compatible to CMOS technologies [63], [64]. The LDMOS high-voltage devices exhibit different characteristics to low voltage MOSFET [65]-[68]. This is because the asymmetrical nature of LDMOS devices results from the existence of low doped drift region. In previous research, it was considered that snapback phenomenon cannot be observed for LDMOS devices, instead, irreversible damage happens immediately at snapback [69]. Moreover, some researchers consider the boundary of LDMOS SOA is approximately voltage-defined, shown in Figure 4-2.

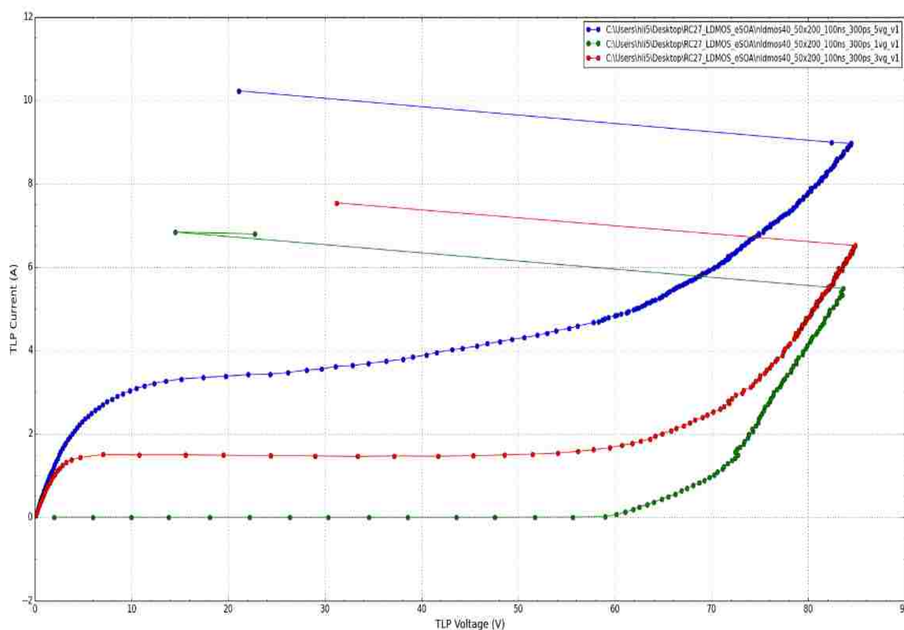


Figure 4-2 Example of voltage-defined SOA boundary

To explain the time-dependence SOA boundary, the concepts of electrical SOA (ESOA) and thermal SOA (TSOA) are introduced. ESOA boundary represents the device failure caused by electro-thermal instability, which is used for short pulse stresses; while TSOA boundary represents the device failure caused by thermal-electro instability. However, these concepts do not accord with the physics in reality, since the junction failure mechanism would be thermal failure no matter electro-thermal instability or thermal-electro instability. And it is difficult to determine the cutting-line of the so-called ESOA and TSOA.

Moreover, snapback phenomenon is observed in LDMOS devices during experiment, when the LDMOS is stressed by TLP techniques, especially for short pulsing stress (<100ns). Under such a short pulsing stress, the LDMOS can snap back and operate in the negative resistance region. Since the self-heating effect would be much less remarkable compared with long pulse conditions, making the device survive post snapback. Even though this snapback was not considered in previously proposed compact models for this type of devices, the snapback can result in misleading simulation results and prevent the proper prediction of the protection device effectiveness in preventing damage in LDMOS drivers. This snapback characteristics can result in substantially reduced protection capability due to competing turn-on characteristics between the LDMOS and the conventional high voltage protection clamps [71].

In this chapter, the boundary of LDMOS transient SOA for short pulse stresses is characterized, including the conditions with or without snapback phenomenon. Unlike the thermal SOA concept for long pulse stresses described previously [59], the transient SOA boundaries for short pulse discussed in this chapter is governed by thermal failure at the junction no matter the device failure occurs before or after snapback. Note that for both long pulse and short pulse stresses,

the device fails because of thermal effect. However, MOS surface current causes failure mainly for long pulses, while drain/body junction current is the main reason of failure for short pulses. A compact LDMOS model is proposed in this chapter. The LDMOS model is constructed with several industry standard circuit elements, including MOS model and BJT model. By adding the thermal failure monitor discussed in Chapter 2, the modeling approach cannot only reproduce the device characteristics, but also can predict the boundary of transient SOA for LDMOS.

4.2 Device Structure and Measurement Discussion

In order to demonstrate the modeling methodology, a 60V and a 125V n-type LDMOS device is measured, analyzed and modeled in this section. The cross-sectional view of the LDMOS device is shown in Figure 4-3.

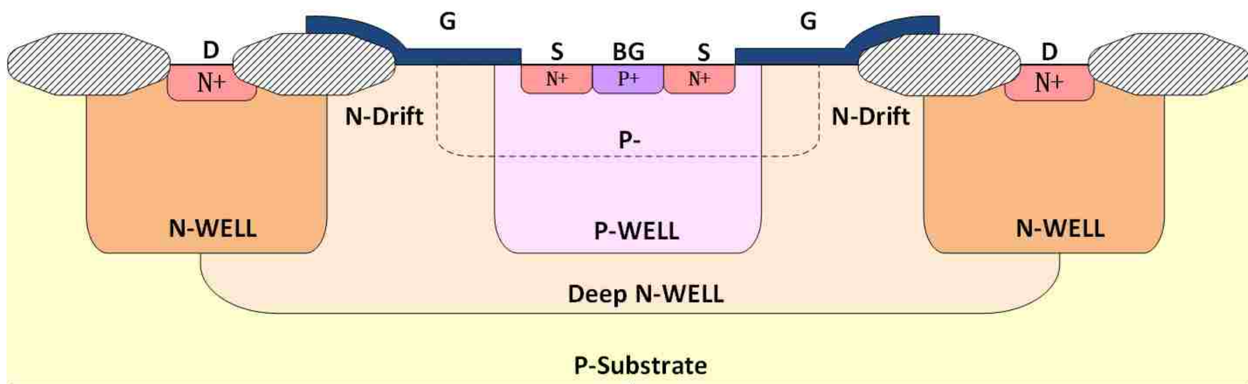


Figure 4-3 Cross sectional view of the LDMOS transistor

The poly gate is deposited on the top of thin gate oxide and overlaps part of the thick field oxide. The Source (N+) and Back-Gate (P+) are shorted together and enclosed by a P-well. The P-well extends to the region under the poly gate with a lightly-doped P- diffusion. The N-well and

deep N-well are used to form the drift region. The structure is designed to sustain high voltage between the drain and source, and the device can be driven by a low gate voltage. The width of the LDMOS is 200 μm. A High Power Pulse Instrument (HPPI) transmission line pulsing (TLP) system with 50Ω impedance is used to characterize the SOA boundary of LDMOS devices. The setup of the SOA measurement is shown in Figure 4-4. The gate bias was varied from 1V to 5V. Pulse widths of 10ns, 25ns, 50ns, 75ns and 100ns were used to complete the characterization of the transient response.

In order to characterize the gate bias dependence of the LDMOS studied in this chapter, a sequence of TLP pulses is employed to stress the 60V LDMOS transistors. And the gate bias varies as 1V, 3V and 5V. The measurement results for normal operating region before snapback and whole region including snapback are shown in Figure 4-5.

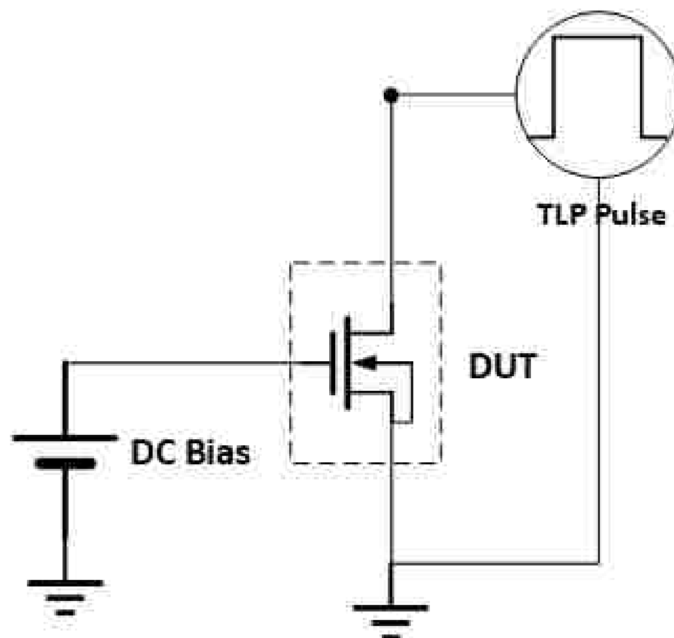
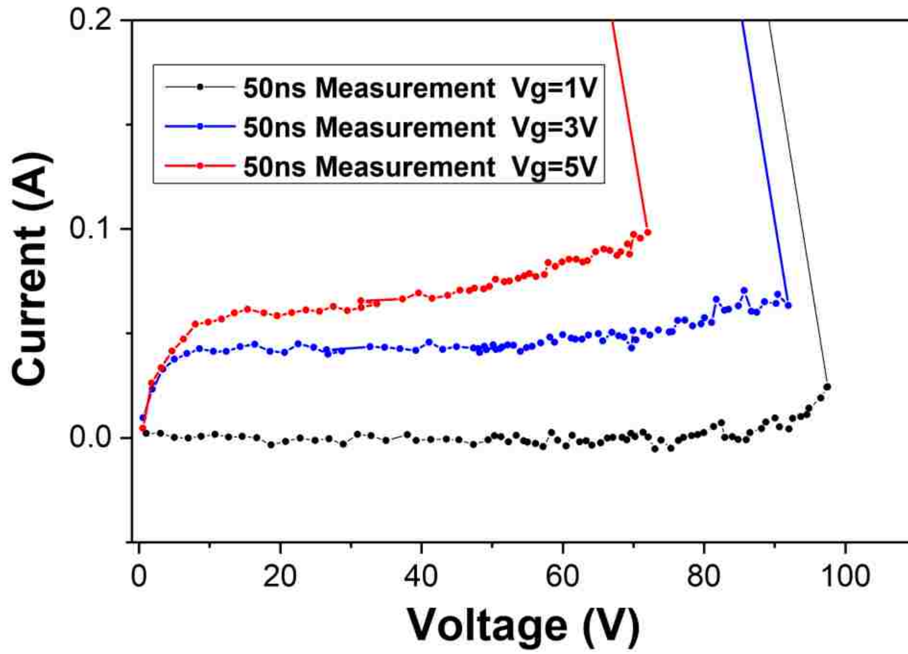
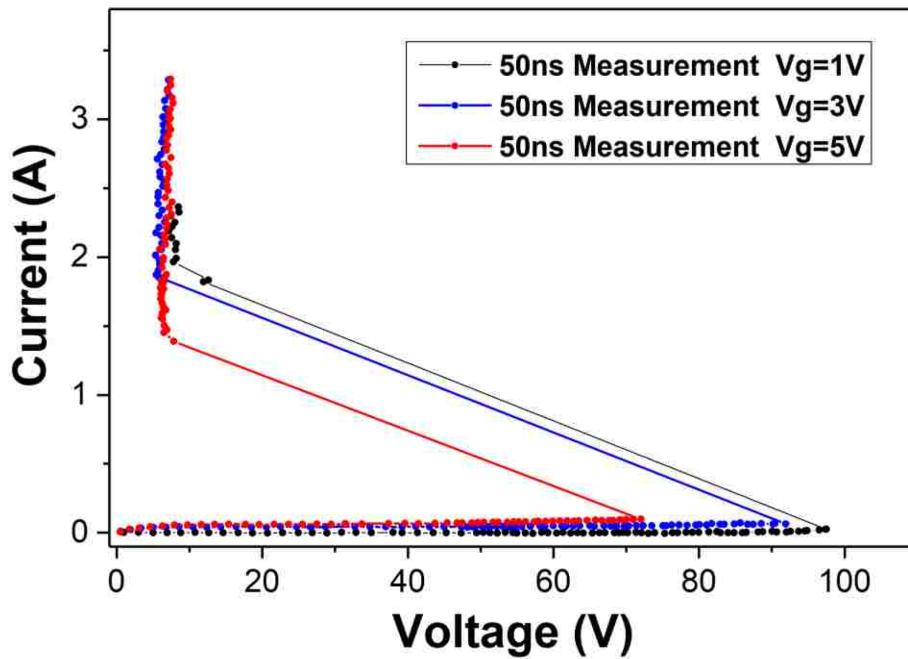


Figure 4-4 Measurement setup for SOA by HPPI TLP system



(a)



(b)

Figure 4-5 50ns TLP quasi-static I-V characteristics of the LDMOS device with different gate biases (a) before snapback, (b) snapback included.

From Figure 4-5, it can be observed that the thermal failure points are independent of gate bias after snapback, this is because the parasitic Bipolar Junction Transistor (BJT) is fully turned on and take over the dominant current conduction. Compared with the BJT current, the MOS surface current can be ignored. On the other hand, the snapback trigger voltages decrease with increasing gate bias voltages. This is due to the fact that the MOS substrate current is part of the total current flowing through the device body [70]. And the MOS substrate current mainly comes from impact ionization at the drain/bulk junction area. For higher gate biases, the MOS substrate current is higher, leading to lower junction breakdown current required for conductivity modulation, hence lower snapback trigger voltage.

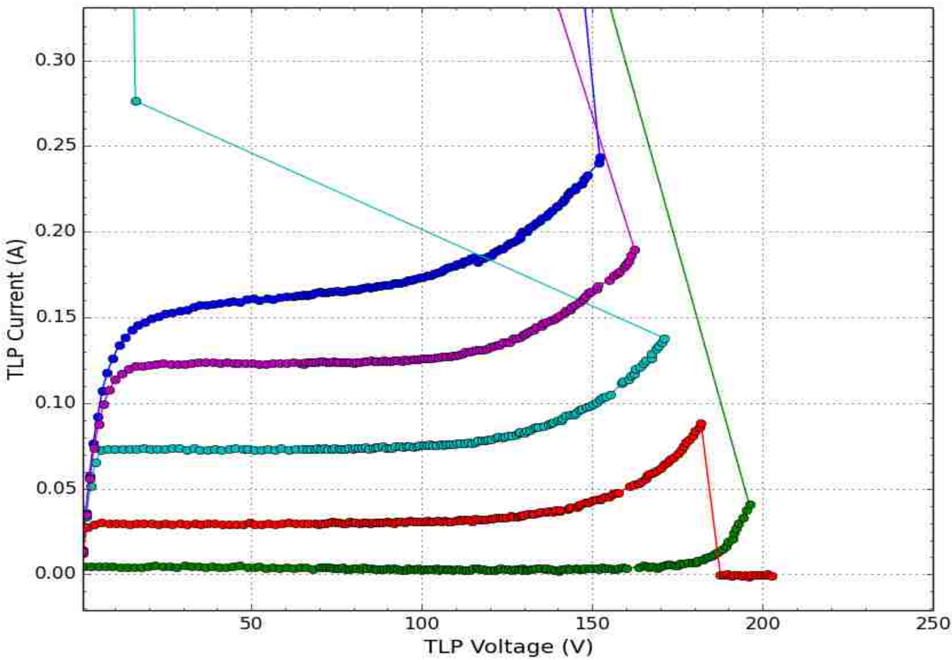


Figure 4-6 TLP quasi-static I-V characteristics of a 125V LDMOS, thermal failure before snapback

Note that for the conditions which failure happens at snapback or before snapback, the failure mechanism is also thermal failure at the junction. The failure points may depend on bias conditions, while the voltage-defined SOA boundary is a special case which is shown in Figure 4-2. The modeling approach is valid for all short pulsing stresses, no matter the failure happens before or after the snapback. As an example, a 125V LDMOS transistor is stressed by 100ns TLP pulses, in which the failure happens before the snapback point, shown in Figure 4-6. The failure points of the 125V LDMOS transistor are strongly depends on bias conditions, which will be discussed and modeled in next section. While for long duration stresses, the thermal failure is caused by the MOS surface current, which will not be discussed in this chapter. As shown in Figure 4-7, thermal failure happens in the MOS operating region without any junction breakdown current.

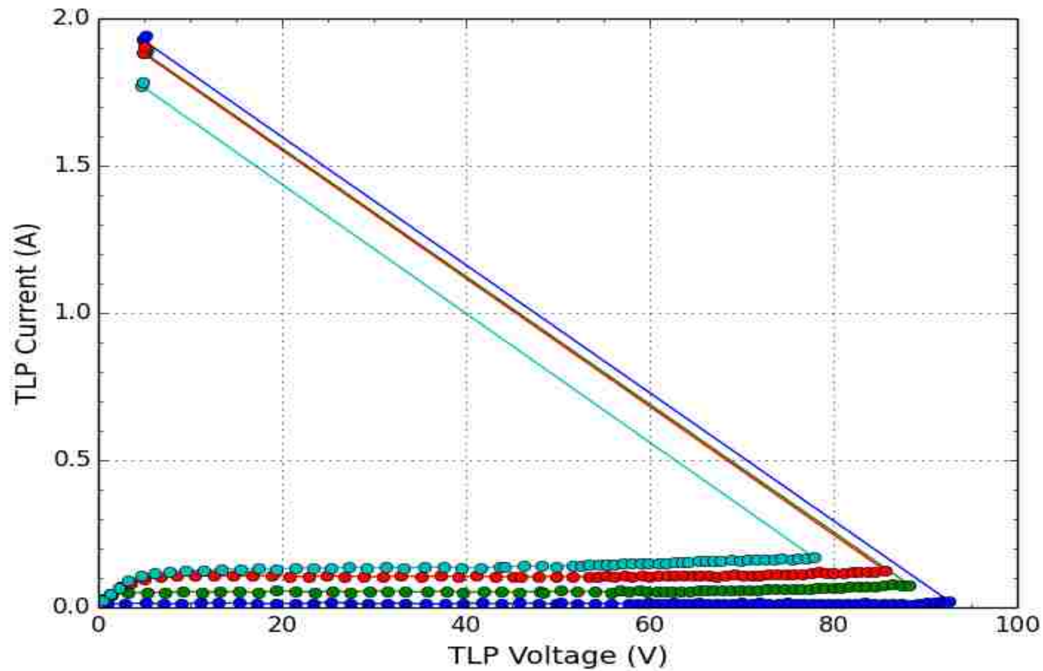
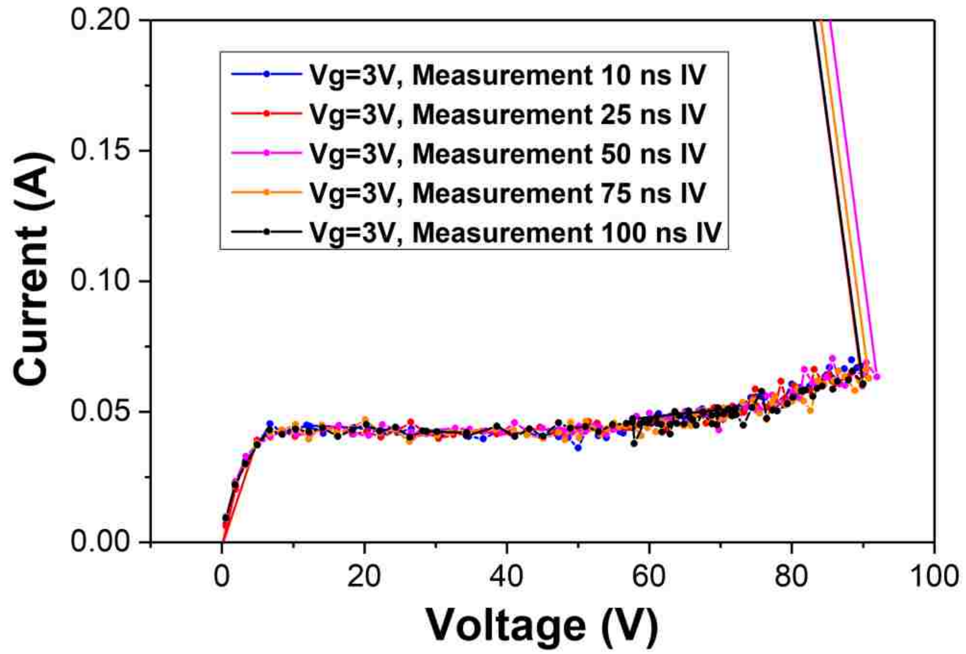
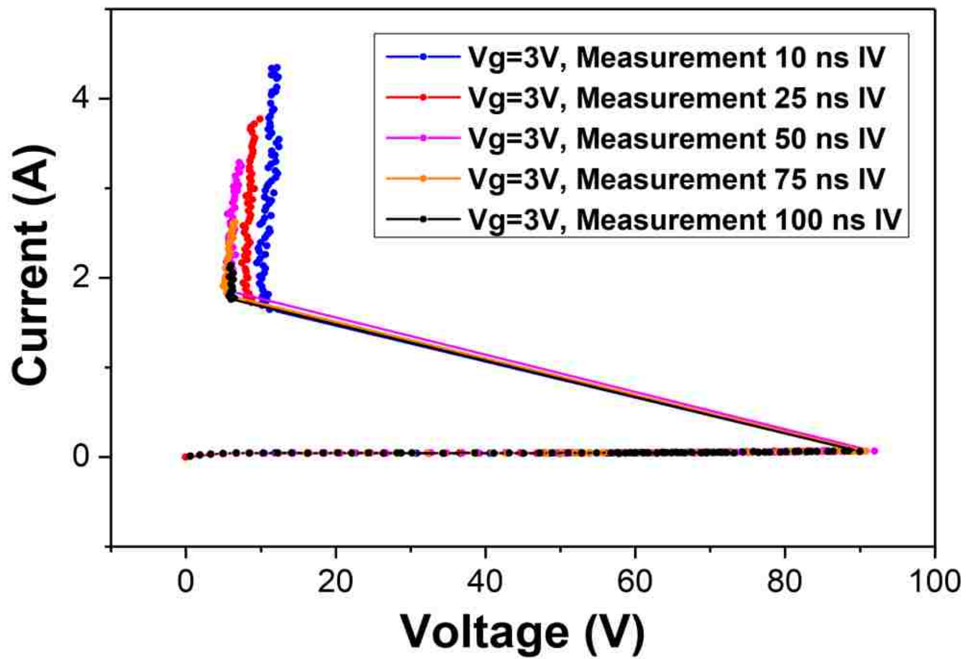


Figure 4-7 TLP quasi-static I-V characteristics for long pulse (1500ns)



(a)



(b)

Figure 4-8 TLP quasi-static I-V characteristics of a LDMOS device with 3V gate bias for different pulse widths (a) before snapback, (b) snapback included

In addition, in order to characterize the pulse width dependence of the analyzed LDMOS device, TLP testing techniques with pulse widths of 10ns, 25ns, 50ns, 75ns and 100ns are used to measure the 60V LDMOS device. The device is biased at 3V, and results are shown in Figure 4-8.

Note that the I-V characteristics and trigger voltage are independent of pulse width, which can also prove the fact that thee LDMOS can snap back without damages, and the gate bias condition independence is consistent with the convention electrical SOA (ESOA) theory. After snapback, the thermal failure is governed by Wunsch-Bell curve [18], namely, the shorter the pulse width the higher the power-to-failure, and it is discussed in detail in Chapter 2. Therefore, the boundary of transient SOA after snapback is determined by the pulse widths. Moreover, it can also be observed that the holding voltages for short pulse stresses are lower than those for long pulses. This is because the pulses of 10ns and 25ns are too short to reach complete conductivity modulation in LDMOS due to the existence of low doped N- drift region.

4.3 Snapback and Thermal Failure Modeling

4.3.1 Normal Operation and Snapback Modeling

The proposed LDMOS compact model is shown in Figure 4-9. The LDMOS transistor is modeled using an industry-standard high voltage MOS model. The BJT, on the other hand, is modeled using an advanced proprietary model similar to Mextram, which is also based on an industry available BJT model. The initial breakdown before snapback is represented by the diode D1. This avoids the inclusion of an explicit external current or voltage source and as a result will overcome simulation engine convergence and computational issues [71].

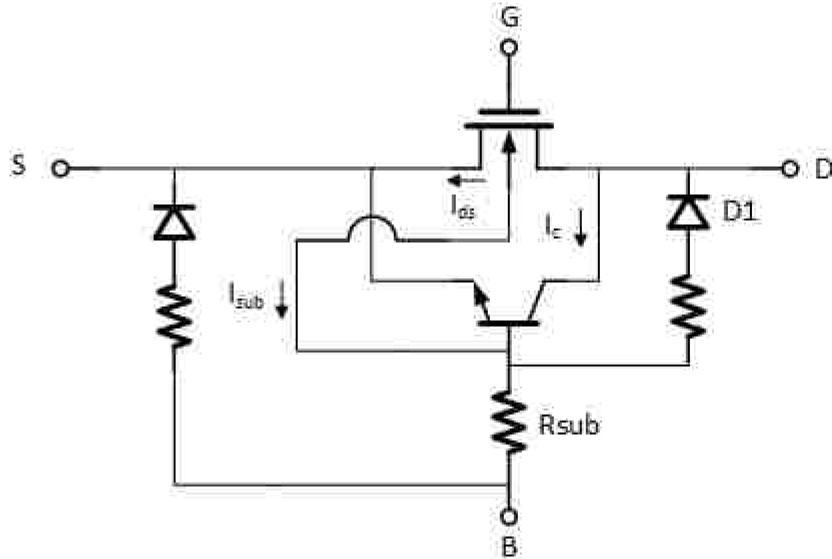


Figure 4-9 Equivalent schematic of LDMOS model

As discussed above, the LDMOS device have an asymmetric structure due to the existence of the drift region which is formed by lightly doped N-Well and deep N-Well. In the LDMOS device, the breakdown starts in the deep N-Well/P-Well depletion region [72]. As the drain-source voltage keeps increasing, the depletion region can expand to the highly doped N+ region. As a result, conductivity modulation happens in the N-Well region and the ionization region is at the N+/N-Well interface [73]. The most important factor that leads to snapback is the voltage drop across the base-emitter junction of the parasitic BJT element, which is the voltage drop across the back-gate resistance. The total substrate current is modeled by the impact ionization current in MOS element and the avalanche current in parasitic BJT element [74]. In existing snapback models, a current source I_{gen} is introduced to model the MOS impact ionization current and/or BJT avalanche current, which can be expressed as [22],

$$I_{gen} = (M - 1) \cdot (I_{ds} + I_c) \tag{4.1}$$

Where M is the multiplication factor, I_{ds} is the MOS surface current and I_c is the collector current of parasitic BJT. Previously, the multiplication factor is expressed by a so-called "Miller formula" [23],

$$M = \frac{1}{1 - K1 \cdot \exp\left(-\frac{K2}{V_d - V_{dsat}}\right)} \tag{4.2}$$

M expressed by equation (4.2) may have the discontinued issue, which will cause convergence problems if the equation is used in simulators. To overcome the discontinued problem, the multiplication factor M is always expressed as [24],

$$M = exp[k1(V_d - V_{dsat} - d1)] + exp[k2(V_d - V_{dsat} - d2)] \tag{4.3}$$

Where k1, k2, d1 and d2 are fitting parameters.

However, there might be some troublesome if explicit current sources are used to model the impact ionization and/or avalanche effect for snapback. Since extensive optimization is required to combine the current sources with multiple other physical effects involved in the device operation. Otherwise, the snapback models may have severe convergence and computational issues. Due to the complexity of the explicit current source, the existing snapback models are not accessible for ESD engineering [68].

In this chapter, an NPN component for the parasitic bipolar transistor and a back-gate resistor are added into the macro model, shown in Figure 4-9. Note that all model elements are standard industry available SPICE device models and there are no explicit current sources in the proposed model. The MOS substrate current can be expressed as [75],

$$I_{sub} = \left(\alpha 1 + \frac{\alpha 0}{L_{eff}}\right) \cdot \left(V_{ds} - V_{dseff}\right) \cdot e^{\left(-\frac{\beta 0}{V_{ds} - V_{dseff}}\right)} I_{dsa} \tag{4.4}$$

Where I_{dsa} is the drain current without impact ionization, L_{eff} is the effective channel length, in saturation region, V_{dseff} equals to V_{dsat}; $\alpha 1$, $\alpha 2$, and $\beta 0$ are fitting parameters.

While the avalanche current in parasitic BJT element is represented by an exponential function given as [76],

$$I_{avl} = I_c \frac{KAVL(VJC - Vbci)}{1 - MJC} e^{-AVL(VJC - Vbci)^{(MJC-1)}} \tag{4.5}$$

Where Ic is the collector current without avalanche, VJC is the junction build-in potential, MJC is the junction grading coefficient, Vbci is the voltage drop over the junction, KAVL and AVL are fitting parameters.

With the modeling approach discussed above, both the MOS substrate current part and the BJT avalanche current part can be treated as two current sources between the drain and source of the LDMOS. The method can avoid using external current sources, and exponential expressions always have computational advance. In conclusion, the model proposed can overcome the discontinuity problem and improve the stability.

4.3.2 Thermal Failure Modeling

As discussed above, the thermal failure is governed by the Wunsch-Bell curve, which means the shorter the pulse width the higher the power-to-failure (P_f) [18]. As described in Chapter 2, Failure is identified as the current (It_2) and voltage (Vt_2) where the leakage current increases by order of magnitude. The product of failure voltage and failure current values are used to determine the power to failure [54],

$$P_f = It_2 \times Vt_2 \tag{4.6}$$

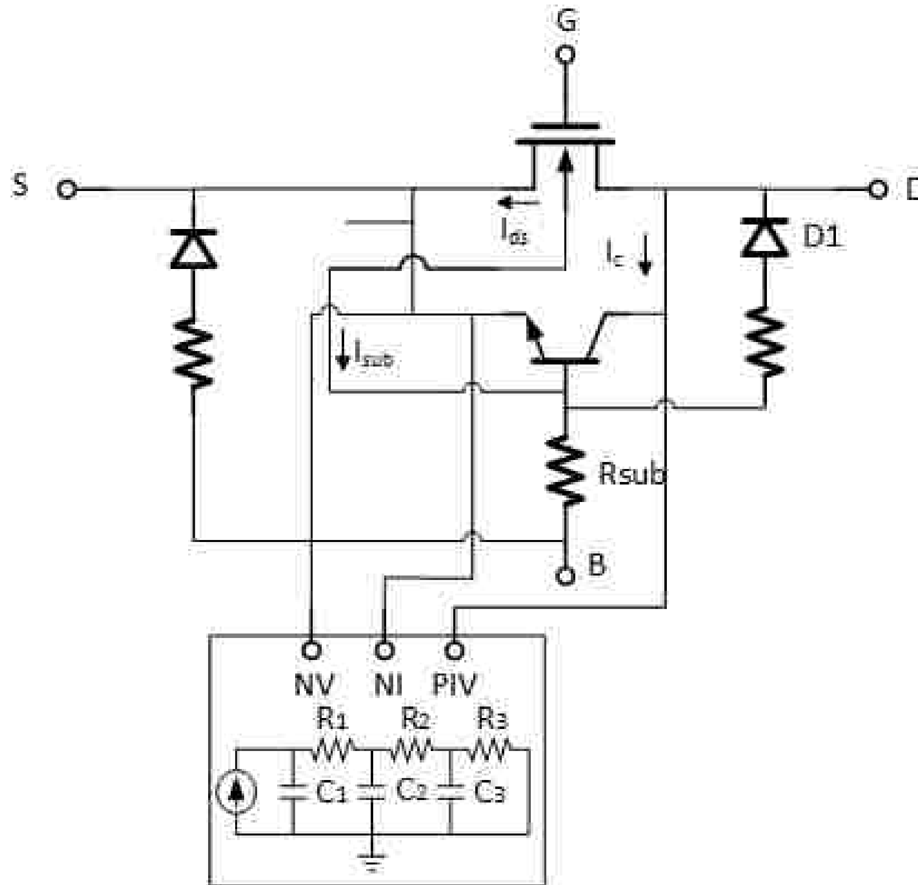


Figure 4-10 Equivalent circuit for LDMOS model, thermal failure monitor connects to BJT

The thermal failure monitor model is similar as the thermal network described in Chapter 2. However, the tricky technique is the location where the thermal network should plug in. The developed model methodology should be valid for any short pulse stresses, no matter the failure happens after, before or at the snapback trigger point. This is because for short pulses, electrical breakdown of the reversed bias drain/bulk junction could be reached. After the junction electrical breakdown, the drain/body junction breakdown current increases to a significant level, and the junction thermal failure is mainly caused by the junction breakdown current. Under this condition, the thermal failure monitor should be connected on the two terminals of the parasitic BJT, and

sense the voltage across the BJT and current flowing through the BJT, shown in Figure 4-10. On the other hand, for long pulse stresses, the thermal failure happens before junction breakdown and is caused by the MOS surface current. Therefore, the thermal failure monitor should be put at the drain and source terminal of the MOSFET, shown in Figure 4-11.

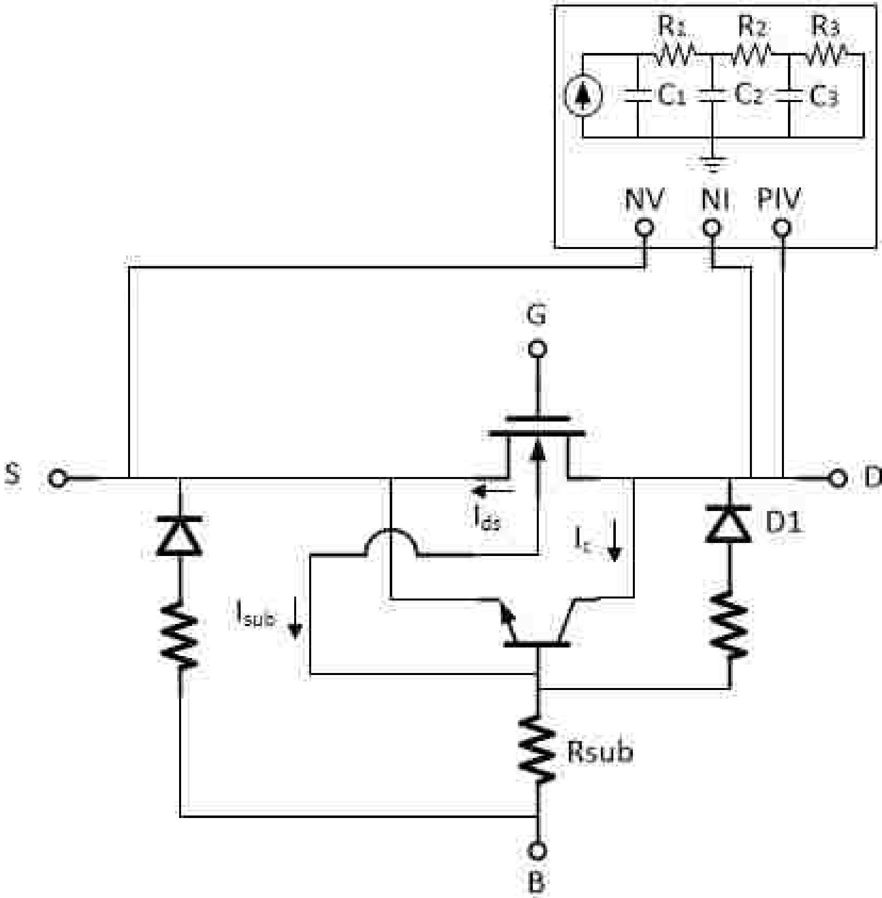


Figure 4-11 Equivalent circuit for LDMOS model, thermal failure monitor connects to MOSFET

As an example, the 60V LDMOS devices studied is stressed by the TLP testing technique with pulse widths of 10ns, 25ns, 50ns, 75ns and 100ns. Snapback can be observed in the 60V LDMOS transistors. Table 4-1 lists the extracted P_f values for different pulse widths.

Table 4-1 Measured power to failure for 60V LDMOS.

P_f vs. Pulse Width	10ns	25ns	50ns	75ns	100ns
3V	52.98	33.20	24.39	17.14	12.82
5V	49.19	33.85	24.41	19.39	12.61

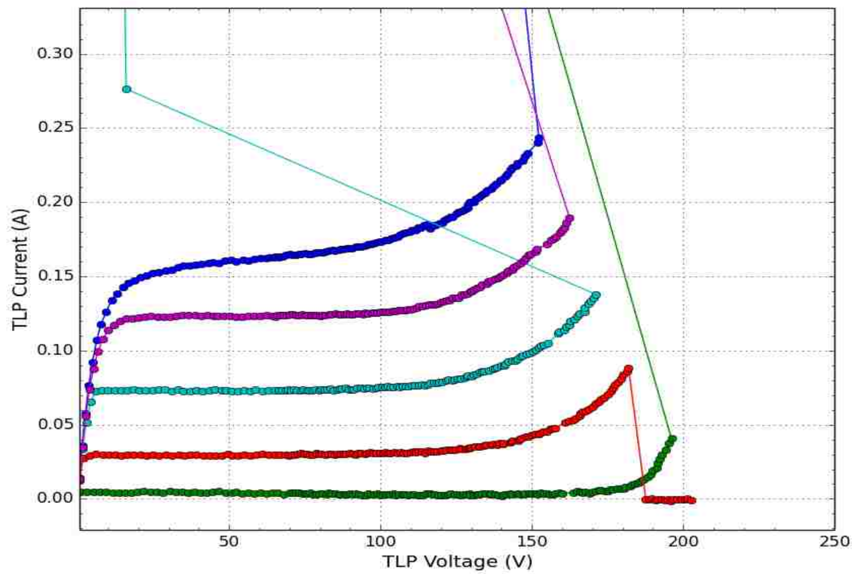


Figure 4-12 TLP quasi-static I-V characteristics of 125V LDMOS transistor

Table 4-2 Measured power to failure for 125V LDMOS.

P_f vs. Gate Bias	1V	2V	3V	4V	5V
100ns	10.39	10.37	10.90	10.56	10.20

In another case, thermal failure happens before the trigger point of 125V LDMOS transistors, shown in Figure 4-12. It can be observed that the thermal failure point is dependent on the gate bias conditions. This is because the boundary of LDMOS transient SOA is actually power-

defined instead of voltage-defined. However, the power should be calculated by the current flowing through the BJT and the voltage across the BJT, which is obtained by the method that failure current minus the MOSFET normal operating saturation current. The calculated power to failure from measurement is listed in Table 4-2. Note that the power-to-failure is independent of gate bias conditions. Therefore, the power-to-failure can be used as the failure judgement criteria. The voltage-defined SOA boundary is actually one of the special cases. And the fact is that the voltage-defined SOA boundary is also power-defined if the MOSFET saturation current is deducted from the total current. Therefore, the methodology proposed is valid for any power-defined SOA boundary conditions.

Similar like the thermal network studied in Chapter 2, a 3-stage thermal network is used for the thermal failure monitor. Similar to the thermal network adopted in Chapter 2 and 3, the silicon region in the LDMOS can be partitioned into three different thermal regions. The capacitors represent different silicon regions that can store thermal energy. And between two thermal capacitors there is a thermal resistor which is equivalent to the heat dissipation efficiency between two adjacent silicon regions. The monitor has 3 terminals: PIV, NV and NI. PIV and NI sense the total current flow into the LDMOS; whereas PIV and NV sense the voltage across the device. The voltage and current are used to calculate power dissipation for the failure monitor. The output of the monitor is a normalized temperature rise to indicate device failure. In this chapter, the temperature is normalized, and failure is indicated when the normalized temperature reaches 1. With the boundary conditions of input power and pulse widths, the values of Rs and Cs were obtained by using an optimization-based parameter extraction methodology to fit the end pulse temperature on C_1 to correspond to the preset normalized failure temperature.

4.4 Model Validation

The measured and simulated I-V characteristics for a 60V LDMOS biased at 1V, 3V and 5V before snapback are shown in Figure 4-13. Note that the simulation is able to reproduce the measurement well, including the trigger voltage dependence on gate biases.

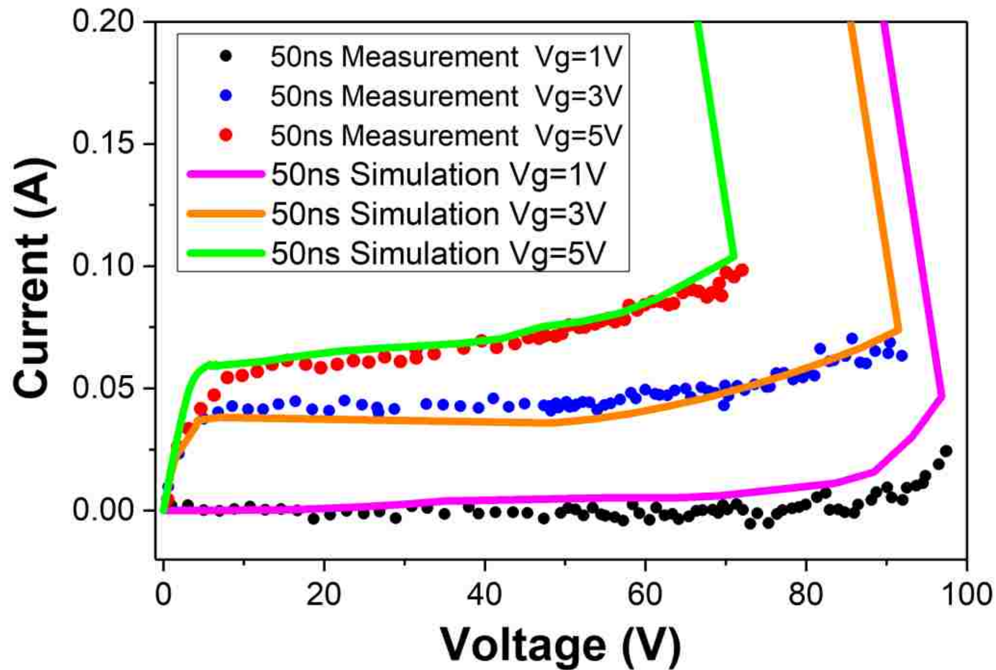
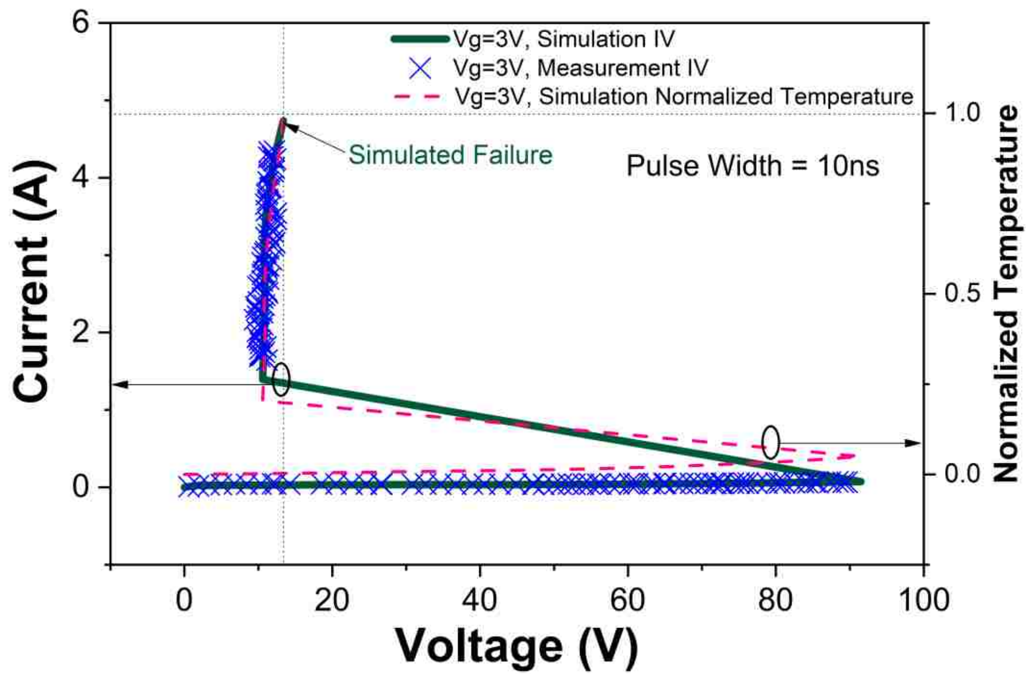


Figure 4-13 TLP quasi-static I-V characteristics of an LDMOS device with different gate bias for a 50ns TLP measurement

Figure 4-14 shows the quasi-static I-V characteristics for the device biased at 3V for different pulse widths. From the simulated and measured results, the simulation is able to reproduce the measurement in normal operating region and negative resistance region post snapback. The normalized failure temperature is preset to "1". When the normalized temperature reaches 1, flag will rise to indicate thermal failure. As shown in Figure 4-14, the simulated failure points are labeled in the plots. The thermal failure voltage is determined by extracting the voltage value at which the normalized temperature reaches the value of "1", marked by the dot lines.



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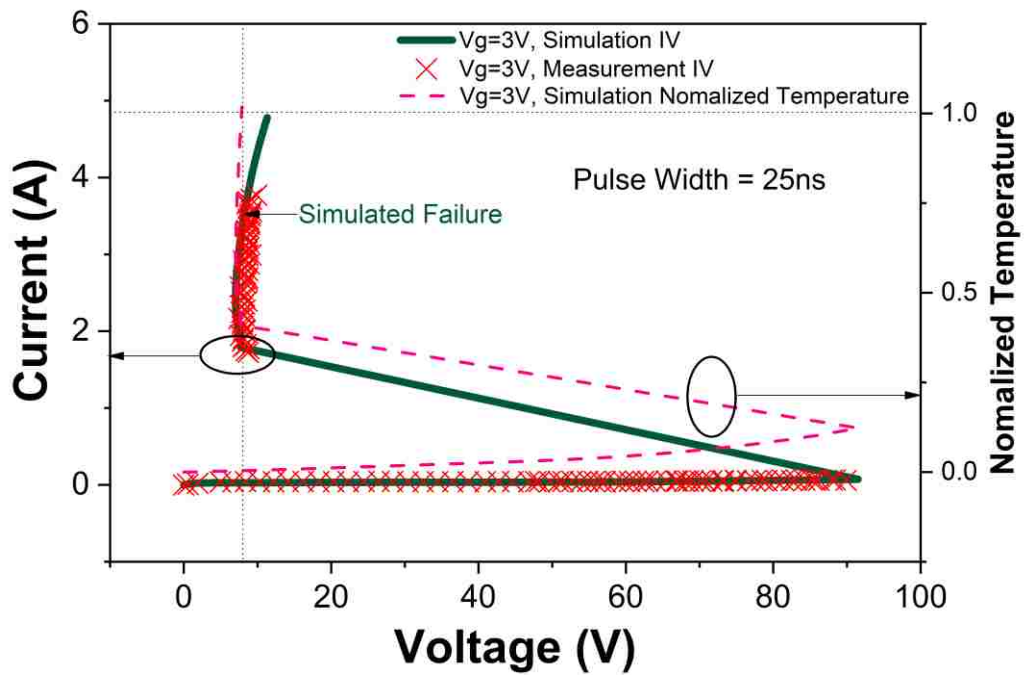

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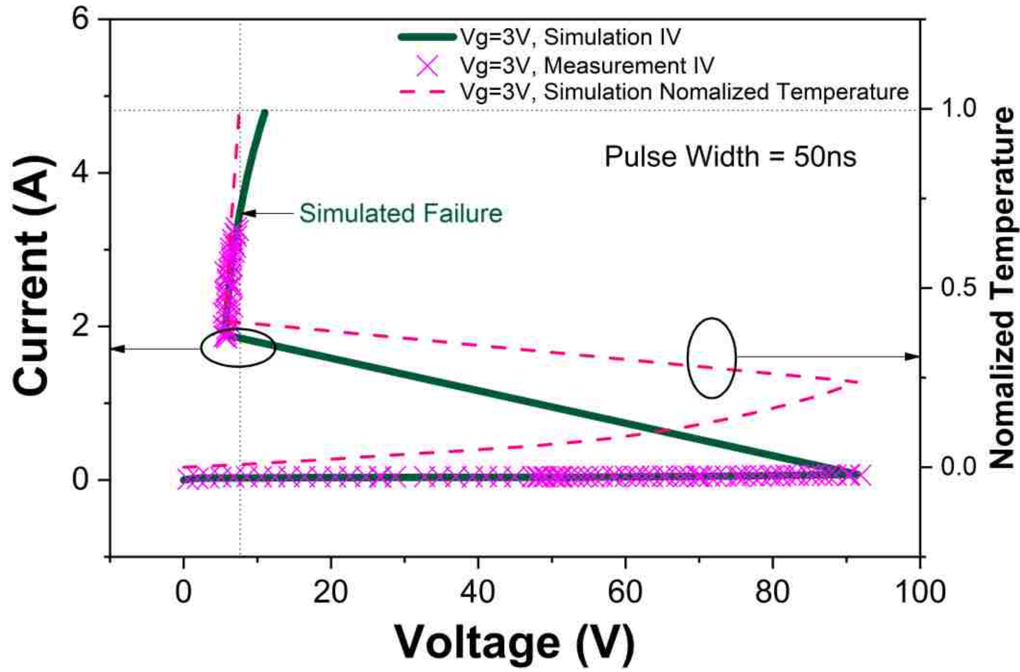

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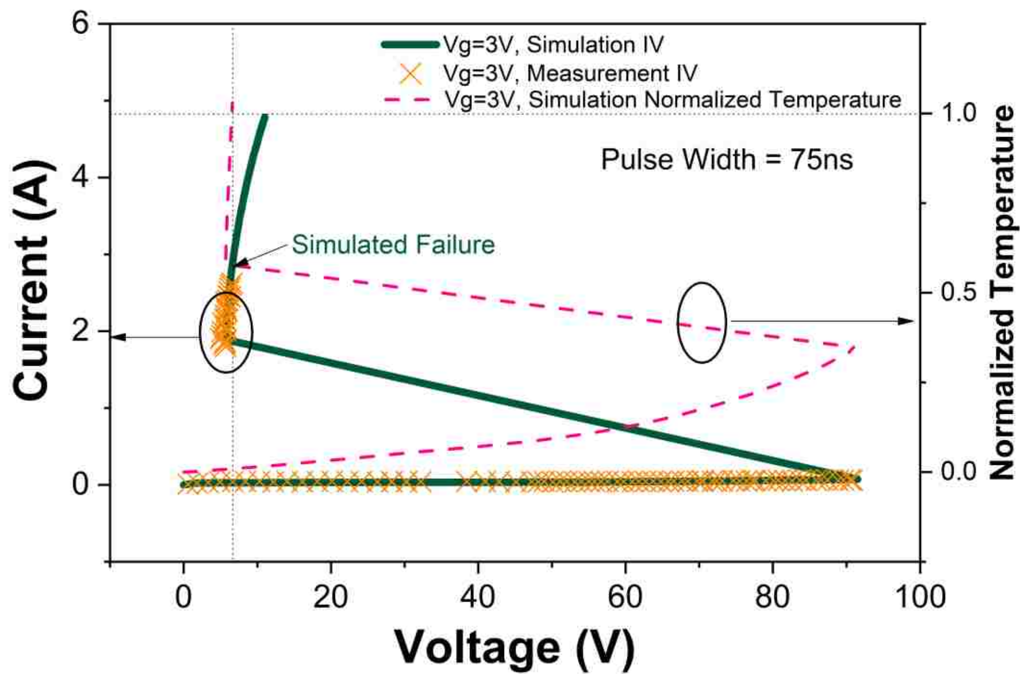
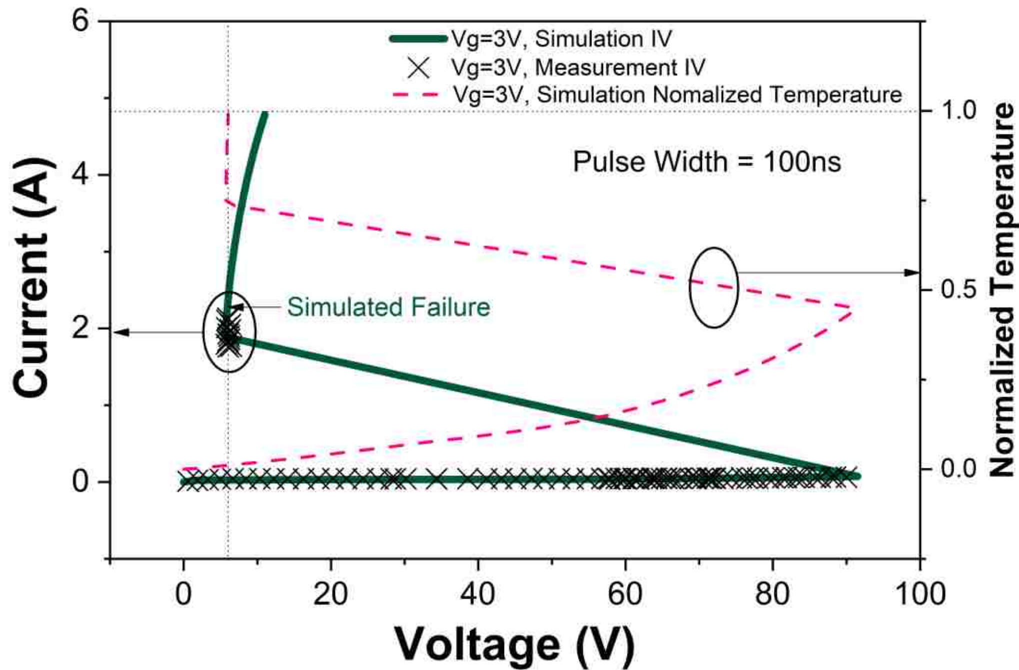


(d)



(e)

Figure 4-14 Measured and simulated quasi-static I-V characteristics of a LDMOS device with 3V gate bias for pulse widths of (a) 10ns, (b) 25ns, (c) 50ns, (d) 75ns, (e) 100ns. The simulated failure points are labeled in the plots. Failure points are extracted by locating the voltages when the normalized temperature rise reaches “1”.

The model is targeted on transient waveforms, the corresponding quasi-static I-V curves are obtained by averaging the voltage and current transient waveforms in the region close to the end of the transient waveforms, usually at 60%-80%. It can be observed that the holding voltage for short pulses (10ns, 25ns) is slightly higher than longer pulses (75ns, 100ns), this is because a longer time is necessary to initiate conductivity modulation in LDMOS devices due to the existence of lightly doped drift region. Figure 4-15 shows a transient voltage waveform of pulse duration of 10ns. The ramp-down after overshoot is obvious, which can prove the fact that 10ns is not enough for the LDMOS transistor to complete the conductivity modulation.

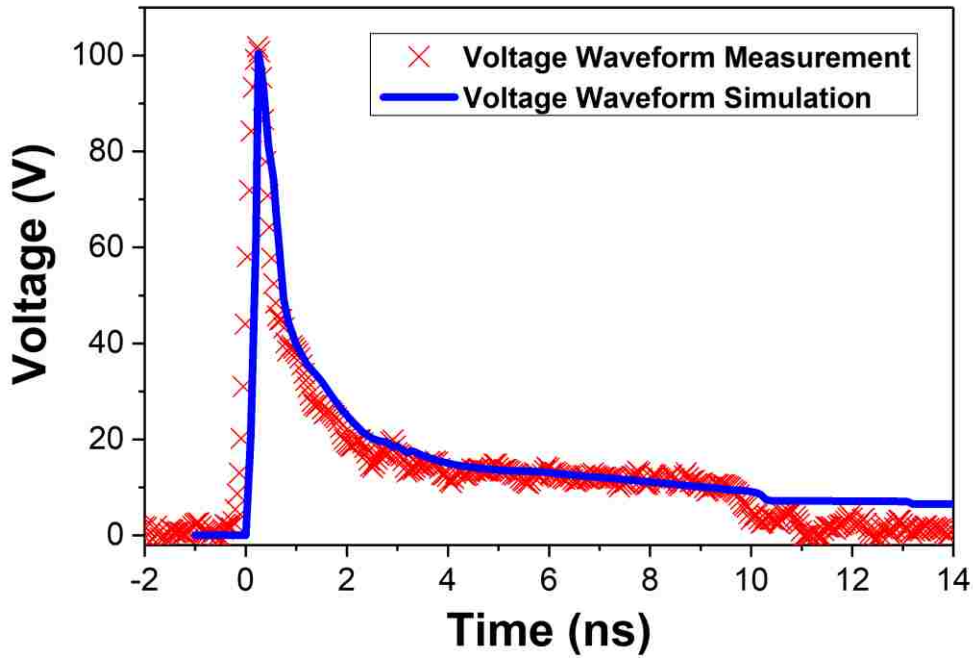


Figure 4-15 Measured and simulated voltage waveform as a function of time for a 10ns TLP measurement

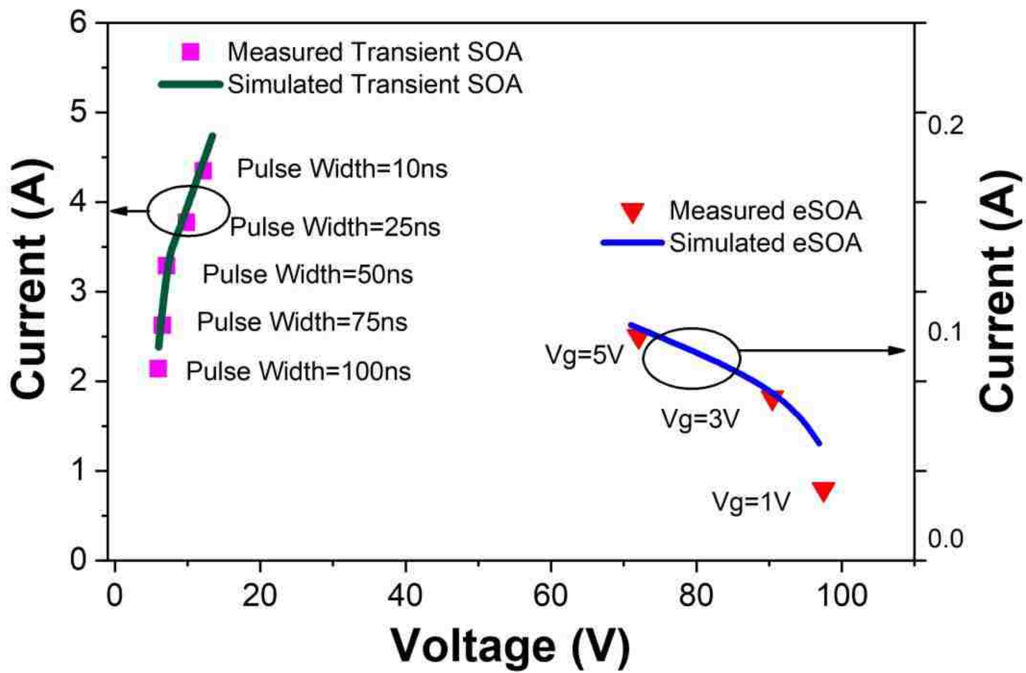


Figure 4-16 Measured and Simulated conventional ESOA and short-pulse transient SOA of 60V LDMOS transistor

The measured and simulated boundaries of conventional ESOA and transient SOA for short pulses of the 60V LDMOS are shown in Figure 4-16. The boundary of conventional ESOA is governed by the electrical breakdown at the drain/bulk junction and depends on gate bias conditions. While the boundary of transient SOA after snapback is determined by the pulse widths.

4.5 Conclusion

As described in this chapter, safe operating area (SOA) is one of the most important factors to evaluate the performance of high-voltage LDMOS transistors. It has been observed that the voltage-defined boundary of SOA is a special case, on the other hand, the boundary of transient SOA is power-defined, generally.

Moreover, modeling of high voltage LDMOS transistors using a macro model approach was presented in this chapter. The proposed model is constructed with several industry available electrical elements, including industry high-voltage MOSFET and BJT similar to Maxtram. To verify the model approach, a 60V LDMOS with snapback and a 125V LDMOS failing before the snapback trigger point are measured and analyzed. By adding the thermal failure monitor model, the boundaries of transient SOA can be determined from the simulation. The proposed model methodology is valid for any short pulsing stresses. Since the thermal failure monitor is connected on the parasitic BJT, the model is valid for any conditions when devices fail after drain/bulk junction breakdown occurs. The proposed model cannot only reproduce the I-V characteristics before and after snapback, but also can predict the boundary of transient SOA for any short pulse stresses.

CHAPTER 5 CHARACTERIZATION OF DIELECTRIC BREAKDOWN AND LIFETIME ANALYSIS FOR SILICON NITRIDE MIM CAPACITORS UNDER ESD CONDITIONS

5.1 Introduction

Silicon Nitride (SiN) metal-insulator-metal capacitor (MIMCAP) is one the most popular components using in GaAs and GaN IC and integrated passive devices (IPD). MIMCAP is used for circuit application because it can provide reliable capacitor characteristics. And it is one of the most important factors to determine the performance of RF integrated circuit. SiN MIM structure is able to provide a wide range of capacitance, and it can be used for DC blocking and bypassing. For DC blocking capacitors, they are more vulnerable to ESD events due to the fact that they are generally located directly at the circuit inputs or outputs, making them the first components along the ESD transit path [78], [79]. Deep understanding on the mechanisms of degradation and breakdown and the lifetime (TDDB) of SiN MIM structures under ESD conditions are necessary.

In this chapter, the different dielectric breakdown mechanisms are analyzed and the time to breakdown (lifetime) is predicted under ESD conditions. A number of MIMCAP samples with different area and thickness are stressed by the TLP techniques across the two capacitor plates. Various ambient temperatures under ESD conditions are also investigated. Measurements are conducted using the Barth 4002 TLP system and Signatone S1060 heating module. The TLP curves of MIMCAP samples are captured by a back-ended oscilloscope, and the breakdown voltages are extracted by the quasi-static I-V characteristics.

The breakdown voltages with respect to various dimensions are analyzed, and the dielectric thickness dependency and area independency cannot be explained by the conventional percolation

model. A new model named constant ΔE model is introduced to explain the dimension dependency for SiN MIM structures with thicker dielectric films. Also, the temperature independence of breakdown voltages is observed, which is because that the displacement current is dominant instead of the Frenkel-Poole conduction current under pulsing stress conditions for thick dielectric films. In addition, by using and extrapolating the transformative version of power law, the pulsed stress periods can be converted into a constant voltage stress (CVS). By using the transformative of the power law, the total stress time and time dependent dielectric breakdown (TDDB) of SiN MIM structure can be evaluated.

5.2 Measurements and Experiments

The SiN MIMCAP samples studied in this chapter are fabricated with SiN films between copper electrodes. The thickness of SiN films varies of 100nm, 200nm and 400nm. The area of MIMCAPs is 60µm × 60 µm, 80µm × 80 µm, and 120µm × 120 µm, and the area is determined by the top electrode area. The Copper layers are electroplated, and the SiN films are deposited using plasma-enhanced chemical vapor deposition (PECVD). The cross section of the MIMCAPs is shown in Figure 5-1.

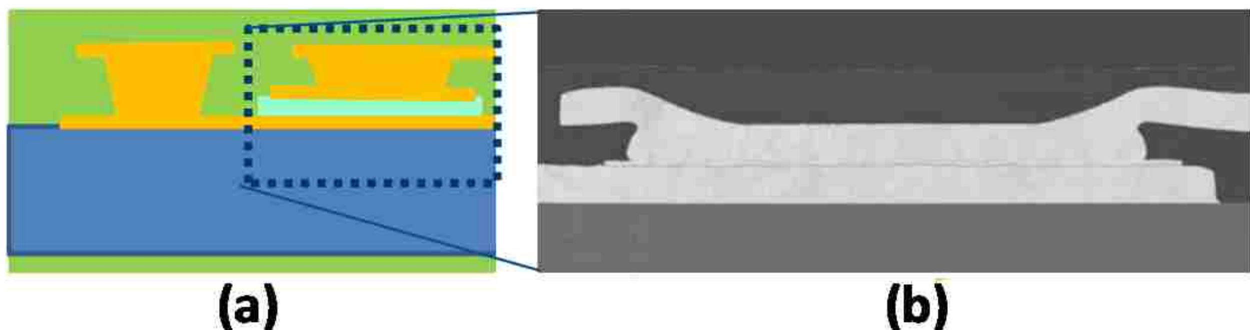
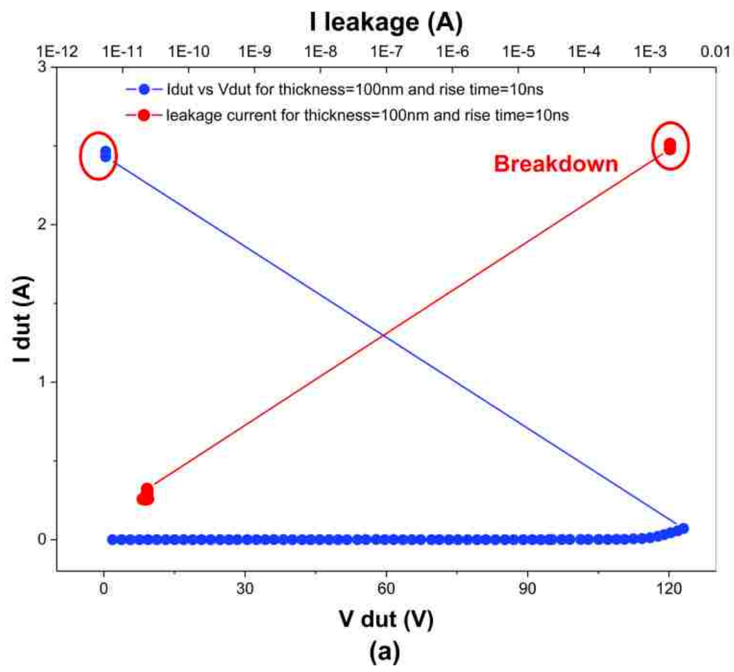


Figure 5-1 Cross-sectional view of the SiN MIM capacitors. (a) Cu/SiN/Cu MIM test structure in this study. (b) SEM cross-section

The measurements are targeted for the human body model (HBM) and are conducted using the Barth 4002 TLP system. The testing procedure includes the charging of a transmission line by a high voltage source, which discharges the calibrated transmission line to stress the device under test, while voltage and current probes measure the device response. The voltage and current transient waveforms are recorded, and after each pulse a DC leakage current stress is performed [80]. The TLP IV characteristics are generated by averaging the voltage and current transient waveforms in the quasi-static region, always between 60% and 80% of the pulse durations. In this chapter, the capacitors are stressed with a pulse width of 100ns and rise times of 200ps, 2ns and 10ns. The Signatone S1060 heating module is used to generate the different ambient temperatures of 25 ^{o}C, 85 ^{o}C and 150 ^{o}C. Based on the power law theory, to eliminate and minimize the impact of initial stress voltage and voltage step during stressing, both of the initial stress voltage and voltage step are set as 1V for each measurement. Since for different initial stress voltage and voltage step, the accumulation effect will be different. And due to the fact that the thermal effect induced by the pulses, the breakdown voltages will be impacted.

Dielectric breakdown is observed at the subsequent pulse that damage the silicon nitride films. It is detected by looking at the point where the DC leakage current increases by orders of magnitude. Figure 5-2 shows three examples of TLP I-V characteristics with pulse width of 100ns, and the breakdown is detected for different dielectric film thicknesses and rise times. The thickness of SiN dielectric film affects the breakdown voltage based on the I-V curves shown in Figure 5-2, making the breakdown voltages approximately 123.23V for 100nm and 225.62V for 200nm at the temperature of 25 ^{o}C and rise time of 10ns.



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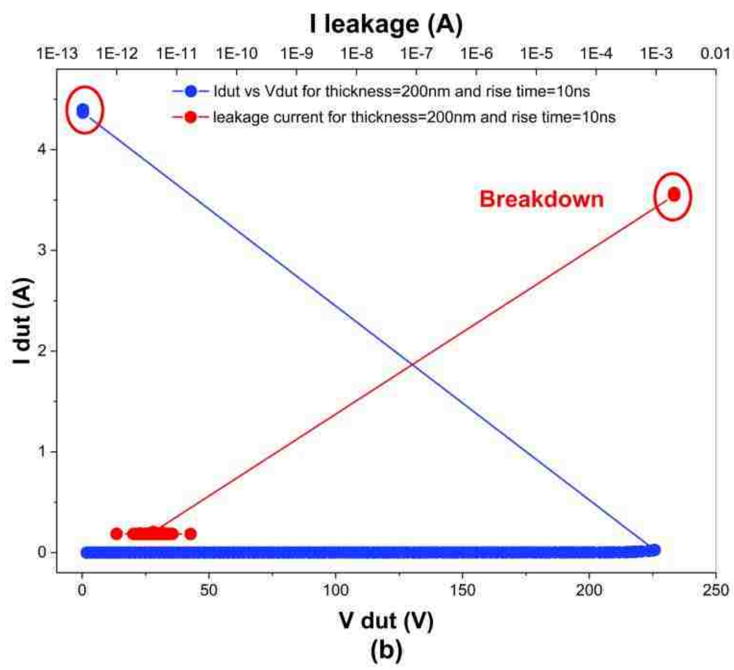

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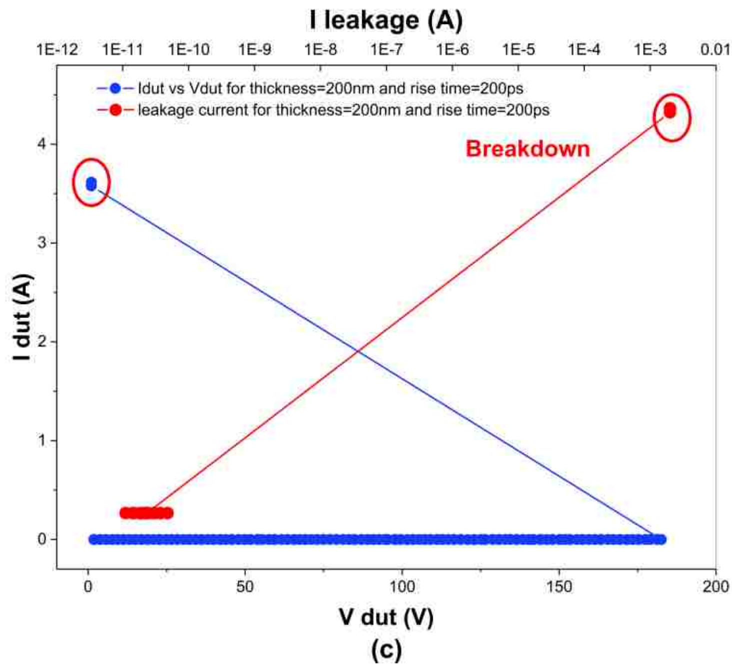
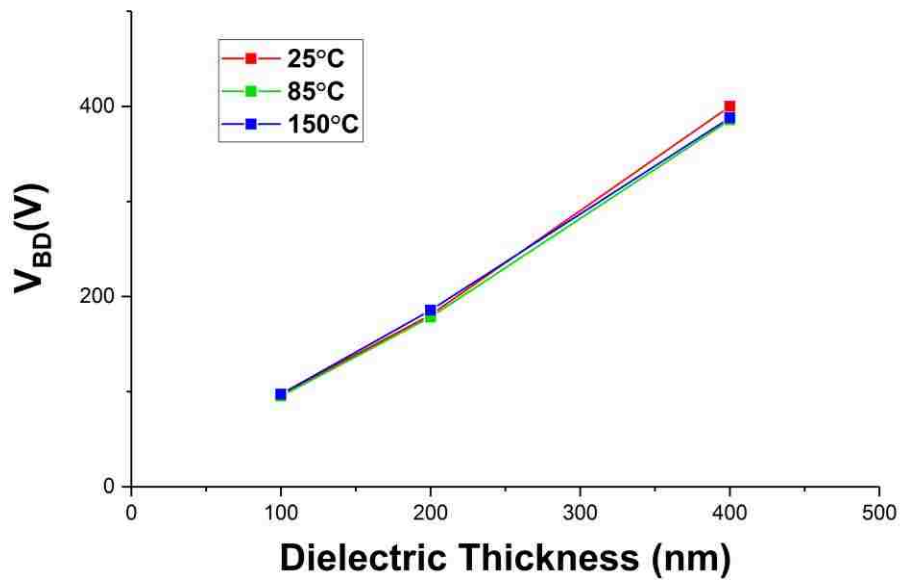


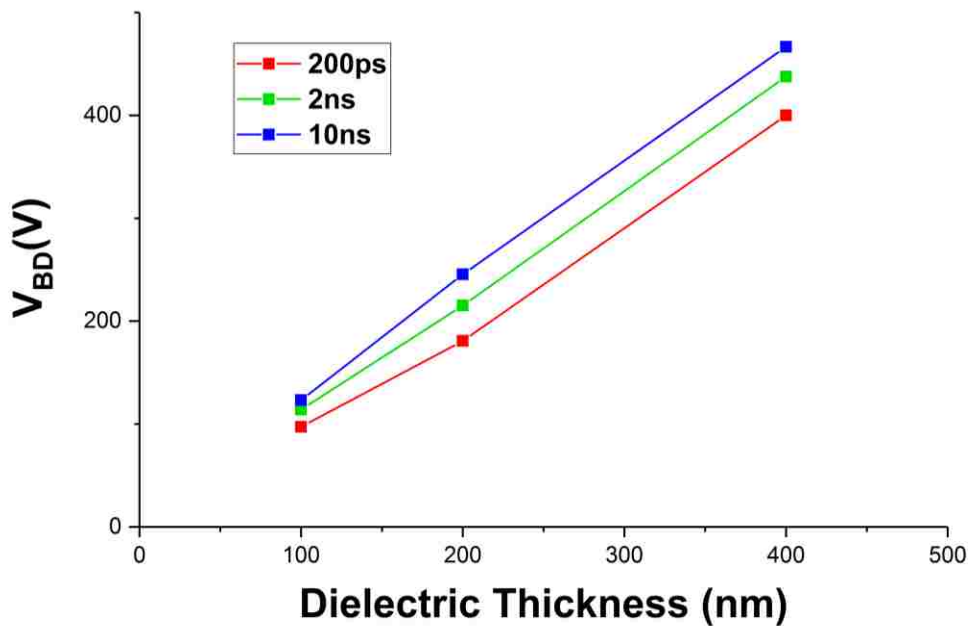
Figure 5-2 I-V characteristics for SiN MIMCAPs at 25 oC temperature and 100ns TLP pulses (a) thickness=100nm, rise time=10ns, (b) thickness=200nm, rise time=10ns, (c) thickness=200nm, rise time=200ps.

5.3 Breakdown Analysis and Lifetime Prediction

Dielectric breakdown is a stochastic process which requires to be investigated with statistical methods. To obtain the statistical data of voltage to breakdown and time to breakdown, fifty MIMCAP samples are measured for each capacitor dimension and each stressing condition. And the breakdown voltages are determined by extracting the voltage level when 63% of MIMCAPs fails based on the Weibull distribution. Figure 5-3 (a) and (b) show the dielectric thickness dependence of breakdown voltages for SiN MIMCAPs with different ambient temperatures and different rise times, respectively. The capacitors are stressed by TLP pulses with duration of 100ns and rise times of 200ps, 2ns and 10ns.



(a)



(b)

Figure 5-3 Dielectric thickness dependence of the breakdown voltages (a)at different ambient temperatures for 200 ps pulse rise time; (b)at different rise times for 25 °C ambient temperature.

The measurement results indicate that the breakdown voltages of SiN MIMCAPs increase with increasing dielectric thickness which agrees well with the expectation and the conventional theory. However, the conventional percolation model is still not able to explain the dielectric thickness dependence for thick films. The basic concept of the percolation model is that traps having fixed radius are generated under the electrical stresses randomly in a dielectric film and the breakdown occurs when a conduction path connecting cathode and anode [81]. The percolation model can be expressed by the following equation [82],

$$N_{BD} = \frac{T_{ox}}{a_0^3} exp[-\frac{1}{\beta} ln\left(\frac{A_{ox}}{a_0^2}\right)] \quad (5.1)$$

Where β is the Weibull slope, T_{ox} is the dielectric thickness, a_0 is the trap diameter, A_{ox} is the area, and N_{BD} is the number of traps needed to induce breakdown.

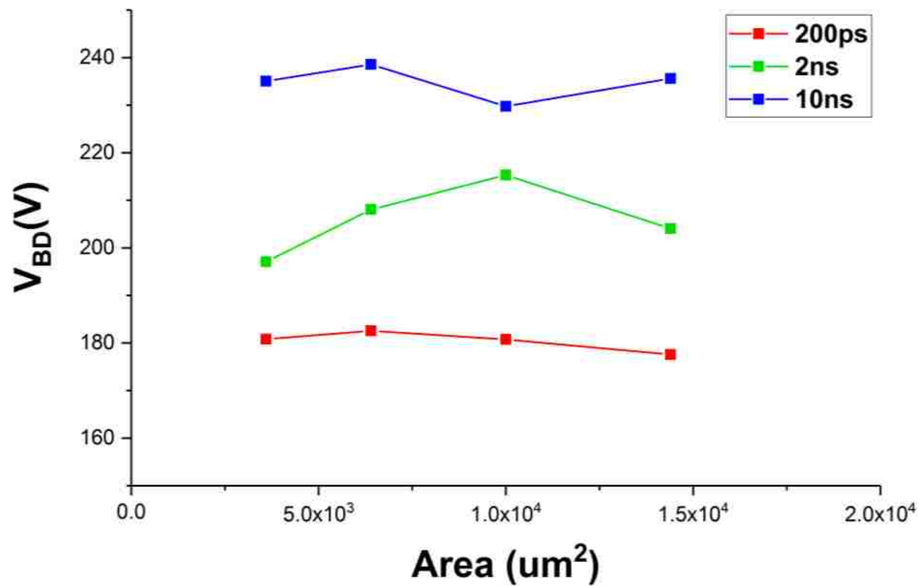


Figure 5-4 Area dependence of the breakdown voltages at different rise times for 200nm dielectric thickness and 25 ºC ambient temperature.

Based on the conventional percolation model described in equation 5.1, the number of traps needed to induce breakdown depends on the area. However, as shown in Figure 5-4, the breakdown voltages are independent of area, which does not consist with the conventional percolation model. In order to explain the thickness dependency and area independency of breakdown voltages, a new model named constant ΔE model is introduced for thick SiN films. Different with E model and Square root E model in previous research, the constant ΔE model considers that electric field shift at cathode and anode interfaces is the dominating factor for the dielectric breakdown [81].

The constant ΔE model considers that the dielectric breakdown of silicon nitride MIMCAPs occurs when the electrical field shift ΔE at the anode or both sides under stresses reaches a threshold field value. A universal relationship between the initial electrical field and the breakdown electrical field is observed regardless of the deposition condition and the film thickness. The threshold field is independent of thickness, stress condition, deposition condition and temperature, while the changing rate of ΔE depends on these above parameters [83]. Therefore, under a same voltage stress, the changing rate of ΔE is lower for thicker dielectric thickness.

In addition, Figure 5-3 (a) also shows that the breakdown voltages of SiN MIMCAPs with thick dielectric films are independent of the ambient temperatures. This is because the displacement current will be dominant instead of the Frenkel-Poole conduction mechanism under pulsing stresses. The Frenkel-Poole current occurs when the charge carriers in the insulator move from trap site to trap site under the influence of the applied electric field. Although the leakage electrical current will increase with increasing temperature [84], the charge accumulation is not remarkable due to the pulsing stresses. Moreover, by the fact that the faster rise times induce lower

breakdown voltages as shown in Figure 5-3 (b), it can be also proved that displacement current is the dominant conduction mechanism. The displacement current can be calculated by [85],

$$I_{disp} = C \cdot \frac{dV(t)}{dt} \quad (5.2)$$

In this study, the range of displacement current is from 0.1mA to several amperes calculated by equation 5.2, considering different device dimensions and different stressing conditions. Compared with the displacement current, the leakage electrical current can be ignored.

The MIMCAPs' lifetime (TDDB) needs to be analyzed with statistical methods, and the time dependent dielectric breakdown TDDB can be described by the Weibull distribution [86],

$$F = 1 - e^{-\left(\frac{T_{BD}}{T_{63\%}}\right)^{\beta}} \quad (5.3)$$

Where F is the cumulative failure probability, $T_{63\%}$ is the time when 63% of the samples fail, and β is the slope of the Weibull distribution.

$$Weibit = ln[- ln(1 - F)] = \beta l\, n\left(\frac{T_{BD}}{T_{63\%}}\right) \quad (5.4)$$

It has been proved that the power law is capable to predict the lifetime (TDDB) accurately, however, power law is used for CVS conditions. There is no power law for pulsing conditions. Under CVS conditions, the power can be described as,

$$t_{BD} = aV_G^{-n} \quad (5.5)$$

Where a and n are the power law constant, and V_G is the applied voltage.

There are five oxide testing methodologies considered in this chapter. The first one is constant voltage stress CVS; the second one is repetitive constant voltage stress (RCVS), and the TDDB is defined as the number of pulses, multiplied by the pulse width; the third one is ramped voltage stress (RVS), in which the voltage increases for each pulse; the fourth one is ramped

voltage stress, which is implemented by constant current source; the last one is stressing the oxide with one specific pulse.

TLP stress is commonly referred to as ramped voltage stress, where the voltage increases for each pulse. It is difficult to define the time to breakdown under TLP stresses, since the stressing pulses at low voltage region do not have the same effect as the ones at high voltage region. In previous research work, the time to breakdown is interpreted by adding all the pulsing times together. However, this method does not give the later pulses more importance. In this work, the TLP stress is transformed into constant voltage stress (CVS) by using the transformative version of power law [87], [88],

$$t_{bd2} = t_{bd1}\left(\frac{V_2}{V_1}\right)^{-n} \tag{5.6}$$

Where t_{bd1} is the time to breakdown for a CVS stress at V_1; similarly, t_{bd2} is the time to breakdown for V_2. n is the power law constant. For the pulses prior to failure, t_{bd1} and V_1 can be represented by the total pulse duration and the average of pulse voltage. However, for the final pulse in which the dielectric fails, t_{bd1} is defined as the time duration from the beginning of the stresses, which means the time when the initial rise-time is completed, to the time when failure occurs. And V_1 is determined by averaging the ten corresponding voltage data points just before the failure time point [87]. Two TLP pulses at the voltage levels at which the dielectric fails with different pulse widths are stressed on the capacitors under test, then the parameter n can be derived from equation 5.6. And in this study, n=13. A voltage stress can be considered as being composed of an infinite number of infinitesimal stresses. A derivation of the transformative version of power law is proposed to transform any arbitrary transient waveforms into an equivalent CVS stress [89],

$$t_{eff} = \int_{t_1}^{t_2} (\frac{V_{ref}}{V(t)})^{-n}\, dt \tag{5.7}$$

Where t_1 and t_2 are the starting and ending times for the voltage waveforms, t_{eff} is the effective stress time for the pre-chosen DC breakdown voltage V_{ref}.

By using the transformative version of power law discussed above, each pulse stress can be transformed into a DC stressing voltage with a specific stressing time which can represents the voltage stress importance. By adding all the transformed times together, the total stressing time for converted CVS can be determined. In this chapter, the equivalent DC stressing voltage is set as 100V, namely V_2 is set as a constant of 100V [90]. The DC equivalent stressing voltage can be set as any constant value, the stressing time is different to indicate the importance of voltage values.

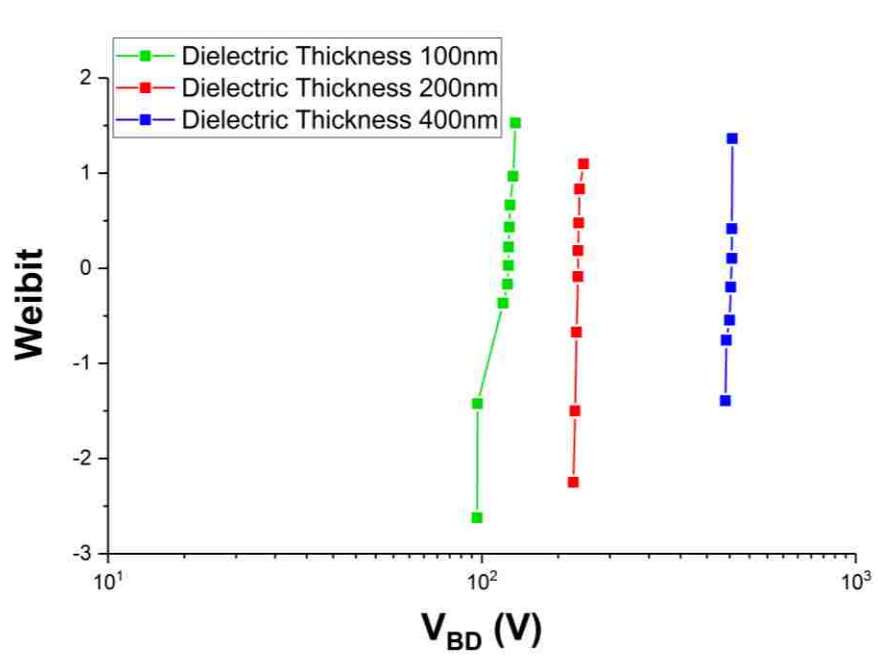


Figure 5-5 Weibull graph of breakdown voltages for TLP stressing at duration of 100ns, rise time of 200ps and temperature of 25 °C.

Figure 5-5 shows the Weibull distribution graph of breakdown voltages for SiN MIMCAPs with different thick dielectric thicknesses (100nm, 200nm, and 400nm). The capacitors are stressed by TLP pulses with duration of 100ns and rise time of 200ps. Using the transformative version of power law, the TLP stress is converted into CVS stress with the constant voltage of 100V. The generated TDDB Weibull distribution graph is shown in Figure 5-6. It can be seen that the Weibull Slope β is independent of the dielectric thickness, which can also prove that the conventional percolation model is invalid for the silicon nitride structure breakdown with thicker dielectric films.

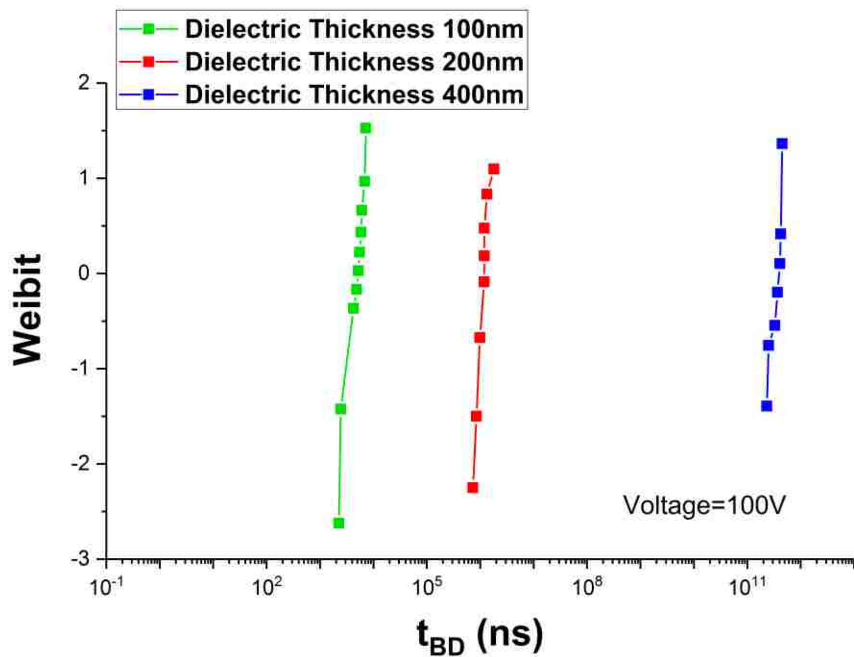


Figure 5-6 TDDB Weibull graph for transformed CVS stressing at voltage of 100V and temperature of 25 ºC

5.4 Conclusion

Characteristics of SiN MIMCAPs under ESD stresses are investigated in this study. It has been demonstrated that the conventional percolation model is not valid for thick silicon nitride films, and the constant ΔE model is introduced to explain the dimension dependence of breakdown voltages. Because the displacement current is the dominant conduction mechanism, the breakdown voltages are independent of temperature, while the breakdown voltages are lower for faster rise times. Furthermore, using the transformative version of power law, TLP stresses are converted into CVS stresses and the lifetime (TDDB) of MIMCAPs is predicted.

CHAPTER 6 SUMMARY AND OUTLOOK

As described in the dissertation, electrostatic discharge (ESD) caused device failure is one of the most important issue during IC design and fabrication. And ESD protection design is becoming more and more challenging due to the fact that the dimension of device keeps shrinking with advanced technology process. It is necessary to develop device models which are industry available and valid under ESD stress conditions. Even though SPICE model is available in most circuit design cases, however, it is difficult to develop good models for ESD conditions. The model for ESD stress conditions needs to address the unique ESD characteristics, including high-voltage, high-current operating region, side effects under high current or high temperature, geometry sensitivity, and electro-thermal coupling effect.

Moreover, it is difficult to evaluate the failure points during simulation, since the failure judgement criteria is difficult to confirm. This is because that the thermal failure may happen earlier than the silicon or metaling melting temperature. The large number of carriers may be induced by ionization impact or high intrinsic ionization at high temperature. The large amount of carriers my change the doping profile inside the junction area, making the junction malfunctional. Under this condition, the failure temperature is much lower than the melting temperature.

In the dissertation, a compact thermal failure model is developed and validated. Instead of analyzing the detailed failure mechanisms, a fixed failure temperature is introduced as the criteria to indicate thermal failure. A 3-stage thermal network is employed to act as the thermal failure monitor model, the multiple stage structure can be used to address the geometry dependence. The corresponding parameters are extracted with an optimization-based extraction methodology with specific boundary conditions. The proposed compact thermal failure model is compatible with

SPICE model and is available for SPICE simulators. Moreover, the model is valid for any ESD transient stresses in the whole ESD timeframe, including HBM, CDM and HMM.

Thereafter, a compressive diode model is proposed. The developed model cannot only fit the I-V characteristics, but also can predict the thermal failure for the whole ESD timeframe. When a diode is operating under high-current high-voltage regions, the on-resistance can increase dramatically. The on-resistance variation can be explained by self-heating effect and velocity saturation. Both of self-heating effect and velocity saturation are modeled with a non-linear resistor model, which is built on the top the CMC-R3 model. In addition to the TLP I-V characteristics, it is important to simulate the actual transient voltage and current response, especially for the stresses with fast rise time. The voltage overshoot is caused by the diode forward turn-on delay, and it is one of the most important factors to evaluate the device ESD protection performance. Since the core circuit may be damaged by the overshoot peak if the ESD protection cannot be turned on quickly enough. By adding a thermal failure monitor model, the proposed diode model is able to predict thermal failure for any type of ESD stresses. The developed model is targeted on transient waveforms and is able to address all the physical mechanisms under ESD stress conditions, including on-resistance variation, voltage overshoot and thermal failure. To validate the proposed model, an STI diode is measured with HPPI and simulated by a SPICE simulator. The simulated and measured results reveal that the model is able to reproduce the transient waveforms, I-V characteristics and predict thermal failure for the whole ESD timeframe.

Moreover, the characterization and modeling of the LDMOS safe operating area is discussed in this dissertation. To evaluate the performance and develop a high-voltage LDMOS, safe operating area (SOA) is one of the most important criteria, besides breakdown voltage and

on-resistance. Previously, it was reported that the boundary of SOA is voltage-defined, which means that the devices fail at the same voltage. In addition, the snapback of LDMOS will cause irresistible damages, which means that snapback phenomenon cannot be observed in a LDMOS device. However, when a LDMOS transistor is stressed with short pulse TLP techniques (<100ns), the device can snap back and enter the region of negative resistance without damages. It is widely accepted that there are two mechanisms causing device failure, one is electro-thermal instability, and the other is thermal-electro instability. However, the junction failure mechanism is thermal failure in reality no matter thermal-electro instability or electro-thermal instability is dominant. In the proposed model, the boundary of transient SOA is predicted by adding the thermal failure monitor model. Since for short pulses, electrical breakdown can happen at the drain/bulk junction, the thermal failure is caused by the junction breakdown current. However, for long pulse stresses, the thermal failure is caused by the MOS surface current. In the proposed model, the thermal failure monitor is placed across the parasitic BJT, making it valid for all short pulse stresses. A 60V LDMOS and a 125V LDMOS are used to validate the model. Based on the simulated and measured results, the model can fit the measured results well and predict the boundary of transient SOA.

In addition, the characterization of breakdown voltages of SiN metal-insulator-metal capacitors is investigated and analyzed. It has been observed that the SiN MIMCAP's breakdown voltages are dependent on the thickness and independent of area. Even though the breakdown voltage thickness dependency is consistent of the conventional oxide breakdown theory, it cannot be explained by the conventional percolation model. A new model named constant ΔE model is introduced to explain the breakdown voltage dependency for SiN MIMCAPs with thick dielectric films. The constant ΔE model considers that the threshold electrical field is the key factor to judge

the capacitor breakdown. By employing the transformative version of the power law, each pulsing stress can be converted into a CVS for a specific duration. And the importance of later pulses before breakdown can be considered by this transforming methodology. With the conversion, the lifetime (time dependent dielectric breakdown, TDDB) of SiN MIMCAPs can be predicted and analyzed.

What's more, there are still several imperfections in the proposed model, and there will be more work to be done to make the proposed models better. First of all, the scalability of the developed model has not been discussed, and only the modeling methodology is released. More work is expected to extend the model scalability. In addition, the thermal failure model is only valid for the junction thermal failure. However, metal or interconnection melting may happen before junction thermal failure, and the characteristics will appear to be an open circuit. Another failure flag is needed to indicate this kind of failure. Moreover, the long pulse stress conditions for LDMOS are not analyzed due to the fact that the failure is caused by different current source.

As a summary, several research jobs which are focusing on device modeling methodologies are introduced in this dissertation, including thermal failure, diode comprehensive behavior and LDMOS transient SOA. This dissertation can act as a reference for the modeling engineering to some degree and present the importance of modeling work for ESD conditions.

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