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Advanced topologies of high-voltage-gain DC-DC boost converters for renewable energy applications

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ADVANCED TOPOLOGIES OF HIGH-VOLTAGE-GAIN DC-DC BOOST CONVERTERS FOR RENEWABLE ENERGY APPLICATIONS

by

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ABSTRACT

This dissertation proposes several advanced power electronic converters that are suitable for integrating low-voltage dc input sources, such as photovoltaic (PV) solar panels, to a high voltage dc bus in a $200 - 960\ V$ dc distribution system. The proposed converters operate in the continuous conduction mode (CCM) and offer desirable features such as low-voltage stresses on components, continuous input currents, and the ability to integrate several independent dc input sources. First, a family of scalable interleaved boost converters with voltage multiplier cells (VMC) is introduced. Several possible combinations of Dickson and Cockcroft-Walton VMCs are demonstrated and compared in terms of the voltage gain, number of components, and input current sharing. This dissertation also presents a novel VMC structure called Bi-fold Dickson. The novel VMC offers equal current sharing between phases regardless of the number of stages, voltage ripple cancellation at each stage, and does not require an output diode. A family of high-voltage-gain multilevel boost converters is presented, with detailed example of the hybrid flyback and three-level boost converter. In this family, the effective frequency seen by the magnetic element is multiple times the switching frequency, and therefore smaller magnetic devices can be used. Theory of operations, steady-state analysis, component selections, simulation, and efficiency analysis are included for each proposed converter. The operation of the proposed converters was further verified with $80 - 200\ W$ hardware prototypes.

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1. INTRODUCTION

1.1. OVERVIEW

The use of high-voltage-gain power converters was limited in the past to a few applications such as supplying power to plasma display panels and integrating batteries to an uninterruptible power supply [1, 2]. Today, high-voltage-gain converters are being used in a wide variety of applications such as radar systems, dc distribution systems, renewable energy harvesting, and data centers. Integrating renewable energy into the electric power grid encourages the use of high-voltage-gain converters to boost the voltage of the renewable energy sources to be suitable for integration to a 400 V dc distribution system. The use of dc distribution has several advantages over the use of an ac distribution system regarding the number of conversion units, price, and power quality. Therefore, using a high-voltage-gain dc-dc converter, one can convert the unregulated low-output voltage of a solar panel to a regulated high-voltage output. Also, the high-voltage-gain converter can extract the maximum power. Several topologies can be used as a high-voltage-gain converter system. However, there is not yet a preferred step-up topology for all applications.

The design goals of power electronic converters vary from application to application, but the most common goals are maximum performance, high power density, or minimum cost. To achieve better performance of the converter, one needs to operate the converter at a suitable frequency, where the switching and core losses are lowest. Also, the passive components should be large enough to reduce the voltage and current ripples. However, decreasing the switching frequency limits the bandwidth of the controller and increases the size of the passive components. High power density of the converter can be achieved

Table 1.1. Common design goals in dc-dc converters

Design goal	**Techniques used**	**Challenges**
Maximum performance	- Low switching frequency to reduce the switching loss - Sizable passive component to reduce the voltage and current ripples	- Low bandwidth for control - Low power density
Maximum power density	- High switching frequency - Topologies with small magnetic elements or switched capacitor techniques	- Thermal constraints - Electromagnetic interference
Minimum cost	- Low cost components, usually old and Less-efficient components - Simplest topologies	- Performance - Efficiency

by either increasing the switching frequency so that passive components are minimized, or finding topologies that require no or very little magnetic storage, such as switched capacitors or resonant switched capacitors. The heat dissipation in the semiconductors and electromagnetic interference are the main hurdles in designing a converter with a very high power density. The total cost of a power converter can be reduced simply by using low-cost components or by designing topologies that require a low count of components. However, obtaining good performance and high efficiency with spending less money is very difficult to achieve. Table 1.1 summarizes the techniques used for the common goal and challenges associated with it.

The common design goals can be even more difficult to achieve in designing high-voltage-gain step-up converters because of the drawbacks of the existing topologies, such as the high voltage stress across components and insufficient voltage gain. Topologies with high voltage stress across components require components with a high voltage rating, which have higher conduction and switching losses. The ideal topology for a high-voltage-gain conversion system would be a topology with a low number of components, high efficiency, low cost, high voltage gain, low weight, small size, high power density, easy integration capability, and high reliability. Practically, the ideal topology is not possible nowadays for several reasons, such as the limitation of operating frequency due to the

losses incurred in the magnetic cores [3, 4] and the high cost of the efficient components and new technologies [5, 6]. In renewable energy applications, the dc-dc topologies need to have specific features, such as drawing continuous and smooth input current and the ability to integrate several different types of power sources. Interleaved high-voltage-gain converters can be fed by several independent voltage sources and have high ac components due to interleaving on the input current, which makes them filtered out easily, and obtain an accurate measurement of the input current to perform maximum power point tracking.

1.2. LITERATURE REVIEW

1.2.1. Conventional Boost Converter. The conventional boost converter is the simplest step-up dc-dc topology. It has only four power-stage elements: an inductor, a low-side MOSFET, a diode, and an output capacitor, as shown in Figure 1.1 [7–9]. The ideal voltage gain of the converter is given by

$$\frac{V_o}{V_{in}} = \frac{1}{1-d} \tag{1.1}$$

where d is the duty cycle, which is the percent of ON time to the switching time period. The conventional boost converter, in theory, can provide a high voltage gain at an extremely high duty cycle, but practically speaking, it cannot be used as a high-voltage-gain converter because of several reasons. First, working with extremely high duty cycles compromises the efficiency and increases the voltage stress across components. Figure 1.2 shows that voltage gain and efficiency versus the duty cycles considering only the conduction loss of the inductor, which is normalized to the output power. The high voltage gain is limited to duties higher than 0.9 and with low efficiency. Considering other conduction losses of the switches, the voltage gain is significantly reduced and the efficiency is severely compromised. The output diode has to block the output voltage, and in high power applications, it may suffer

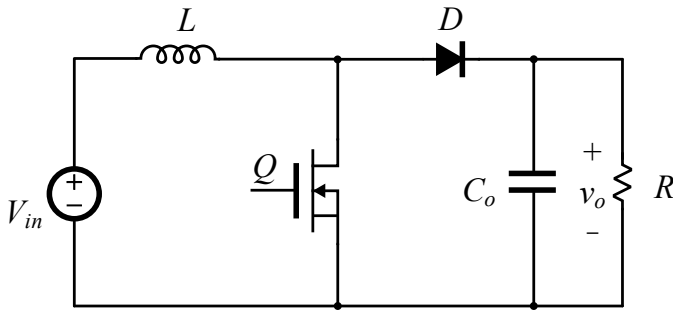

Figure 1.1. The conventional boost converter

from the reverse recovery phenomena. Another disadvantage is that the magnetic element that ensures continuous conduction mode would be massive, which increases the weight of the converter and decreases the power density. [7]

1.2.2. Cascaded and Stacked Boost Converters. Cascading two or more conventional boost converters increases the voltage gain without operation at extremely high duty cycle [10, 11]. Figure 1.3(a) shows a two-stage cascaded boost converter, which is a quadratic boost converter with voltage gain given by

$$Gain_{ideal} = \frac{V_o}{V_{in}} = \frac{1}{(1-d)^2} \tag{1.2}$$

The efficiency of a converter with two cascaded boost converters is given by

$$\eta_{overall_2} = \eta_1 \eta_2 \tag{1.3}$$

More conventional boost converter can be cascaded [12], as shown in Figure 1.3(b), and the voltage gain of the cascaded converter is given by

$$Gain_{ideal} = \frac{V_o}{V_{in}} = \frac{1}{(1-d)^m} \tag{1.4}$$

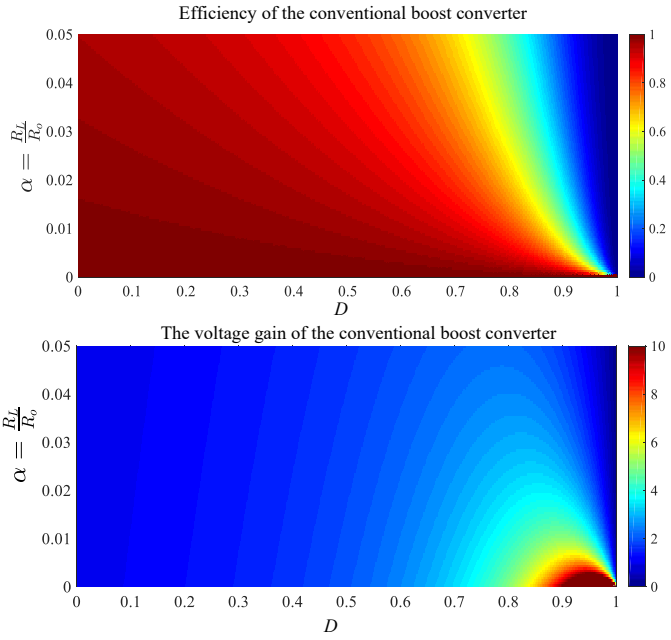

Figure 1.2. The efficiency and gain of the conventional boost converter considering the conduction loss of the inductor.

where m is the number of the cascaded converters. The overall efficiency of m stages can be given by

$$\eta_{overall_m} = \prod_{n=1}^{m} \eta_n \tag{1.5}$$

The drawback of cascading two or more boost converters is that the power is being processed twice, which might compromise the overall efficiency. Another disadvantage is the voltage stress across the active switch and diode of the output stage, which is still as high as the ones in the conventional boost converter. Single-switch cascaded converter has the same gain as the cascaded boost converter but with a reduced number of active switches, as shown in Figure 1.4. Using single switch leads to fewer gate driver circuitry components and lower overall cost. However, the stages cannot be independently controlled as in the cascaded boost converter [2, 13–15].

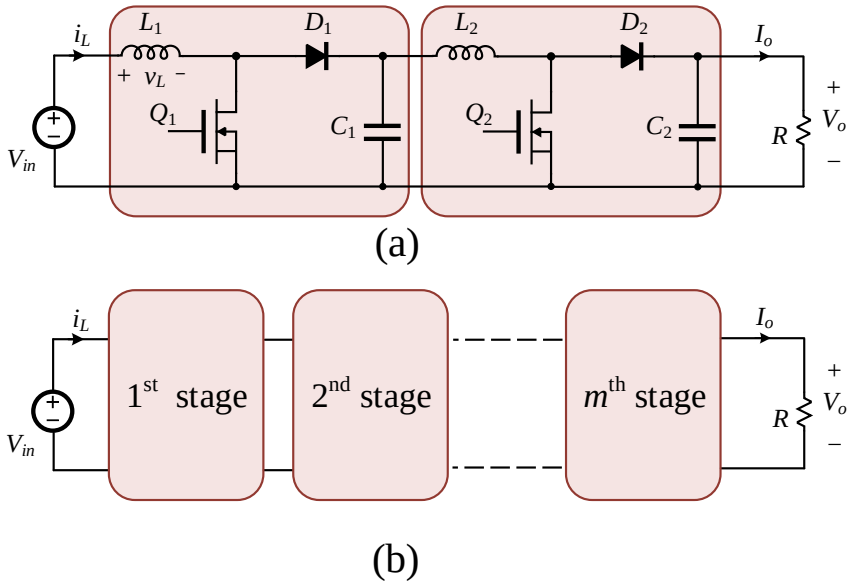

Figure 1.3. Cascaded conventional boost converter (a) two stage (b) *m* stages

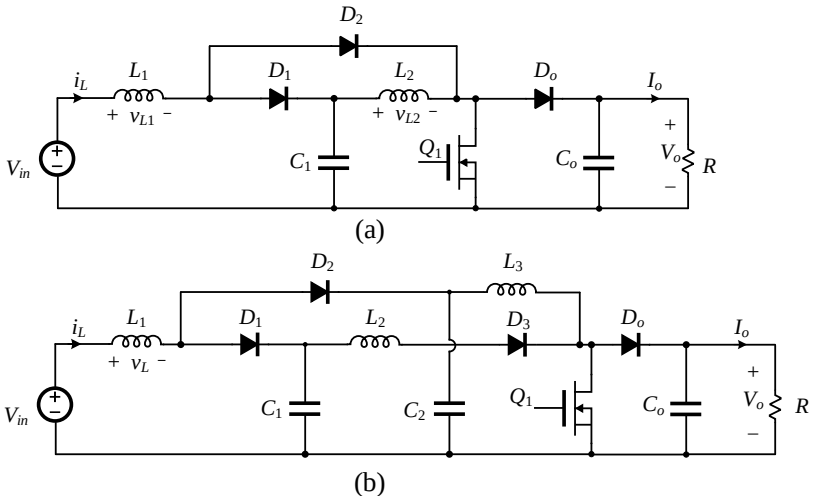

Figure 1.4. Single-switch multistage boost converter (a) two stages (b) three stages

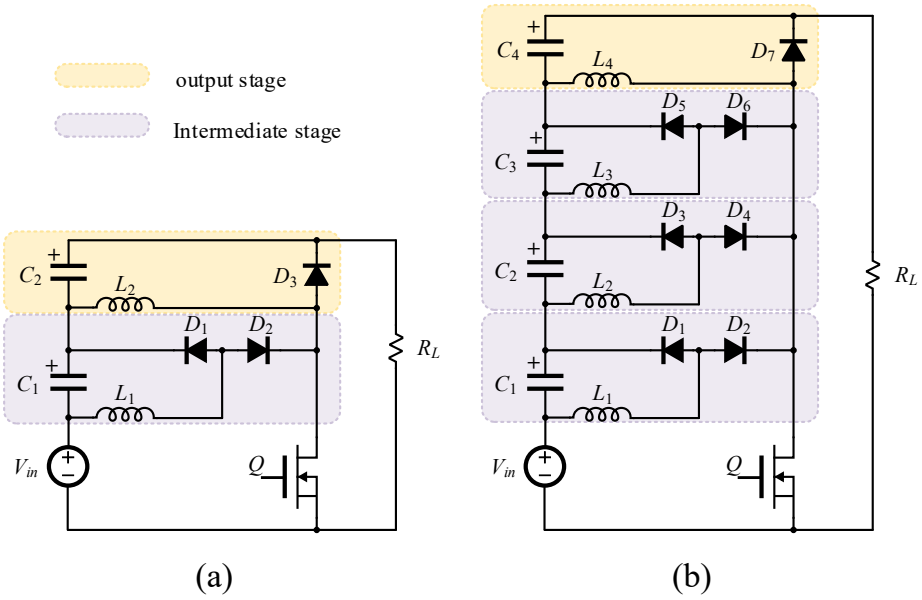

Figure 1.5. Stacked boost converter a) Quadratic b) Quartic

Stacking two or more converters means that the output voltage equals the sum of converters output. Several stacked converters are introduced in the literature to increase the voltage gain [16–19]. Figure 1.5 shows an example of a stacked converter [20]. The example converter has gain of

$$\frac{V_o}{V_{in}} = \frac{1}{(1-d)^n} \tag{1.6}$$

where n is the number of series capacitors. The drawbacks of this type of converter is the voltage balance across the output capacitors if they have large numbers.

1.2.3. Three-level Boost Converter. Three-level boost was first introduced to mitigate the voltage stress across the output diode of the conventional boost converter and reduce the size of magnetic elements by increasing the effective frequency [21]. The three-level boost converter consists of an inductor, two active switches, two diodes, two output capacitors and a floating output, as shown in Figure 1.6(a). The converter has three modes of operation as shown in Figure 1.6(b-d), and their sequence control depends on the voltage balance between the output capacitors [22–25]. By defining the duty cycle with respect

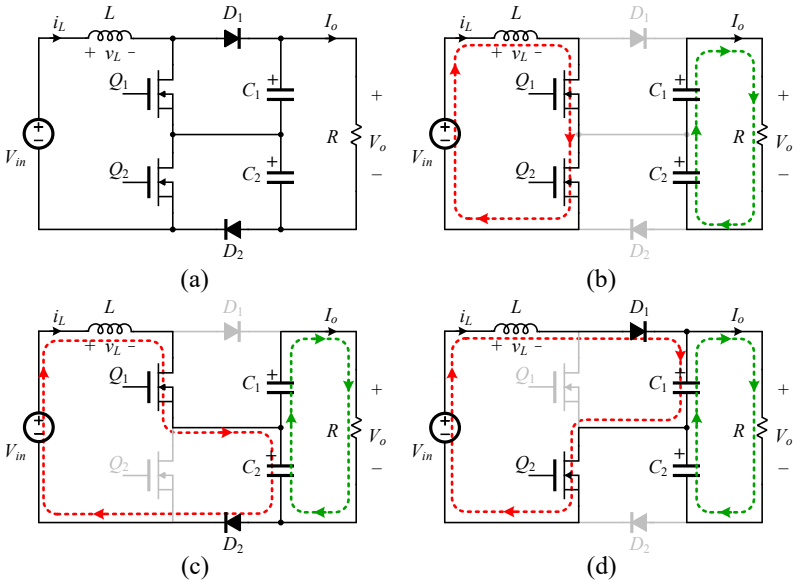

Figure 1.6. Three level boost converter a) schematic b) equivalent circuit to mode 1 where both active switches are ON c) equivalent circuit to mode 2 d) equivalent circuit to mode 3

to the switching frequency, the voltage gain of this converter is the same as the one of the conventional boost converter. Still this converter is impracticable to use for applications that necessitate high-voltage-gain converters because of the insufficient voltage gain.

1.2.4. Isolated Converters. Isolated converters can be used to increase the voltage by increasing the turns ratio of the transformer or the coupled inductor [26–28]. Isolated converters can be categorized based on the symmetry of the magnetic cycle of isolation device in the B-H loop [28]. Converters with an asymmetrical magnetic cycle, such as flyback and forward converters, where the magnetic operating point of the isolation device remains in the same quadrant. Converters with symmetrical magnetic cycles include the half-bridge converter, dual active bridge converter, full-bridge converter, and push-pull converter. Figure 1.7 shows the circuit diagram of some conventional isolated converters, which can be found in the literature [7, 8]. Isolated converters are required in applications where safety is crucial, such as medical devices. However, in other applications, non-isolated dc-dc topologies are more suitable because non-isolated converters have higher power density,

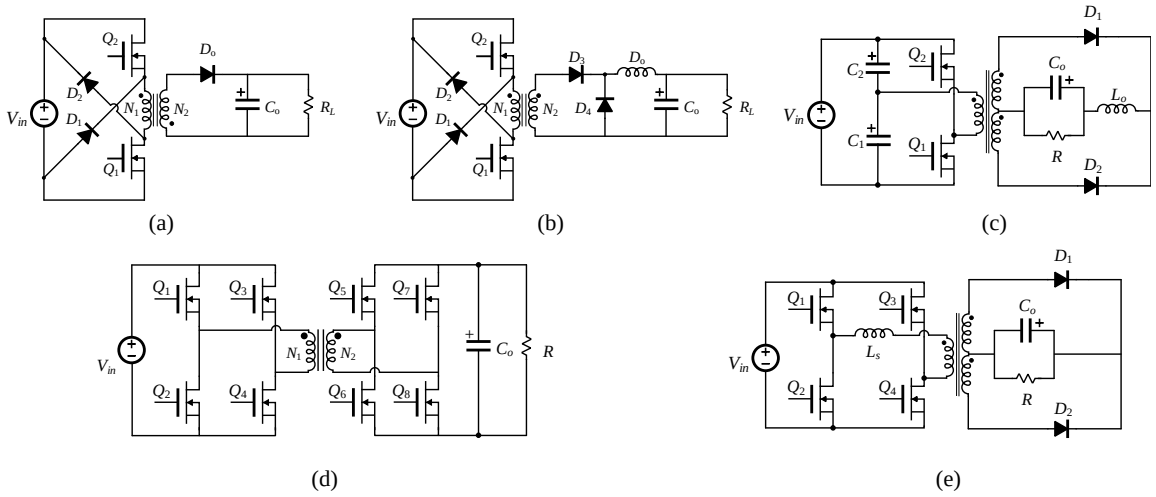

Figure 1.7. Examples of isolated Dc-dc topologies converter a) two-switch flyback converter b) two-switch forward converter c) Voltage-fed half-bridge converter d) dual active bridge converter e) Full-bridge converter

smaller size, and lower weight than the isolated ones. The voltage stress across switches in the isolated converters due to the spikes instigated by the leakage inductance. Therefore, energy circulation circuits are necessary.

1.2.5. Switched Capacitors and Hybrid Boost Converters. Switched capacitors (SCs) mainly consist of active switches and capacitors, and they can boost the voltage by charging and discharging capacitors. SC circuits do not use magnetic storage elements to transfer energy and therefore would significantly increase the power density and reduce the size and weight of the converter. Moreover, the SC circuit can be fabricated into an integrated chip (IC) and used in portable low-power electronics. Figure 1.8 shows examples of the most common SC circuits [29–32]. The disadvantage of using SC circuits is the regulation and the inherent losses. This type of circuit suffers from the discontinuity of the input currents and usually has a fixed output without the ability to increase the voltage using the pulse width modulation signal. Although several papers presented SC converters to have a variable output voltage, such as in [33, 34], the resolution of the conversion ratio is still limited.

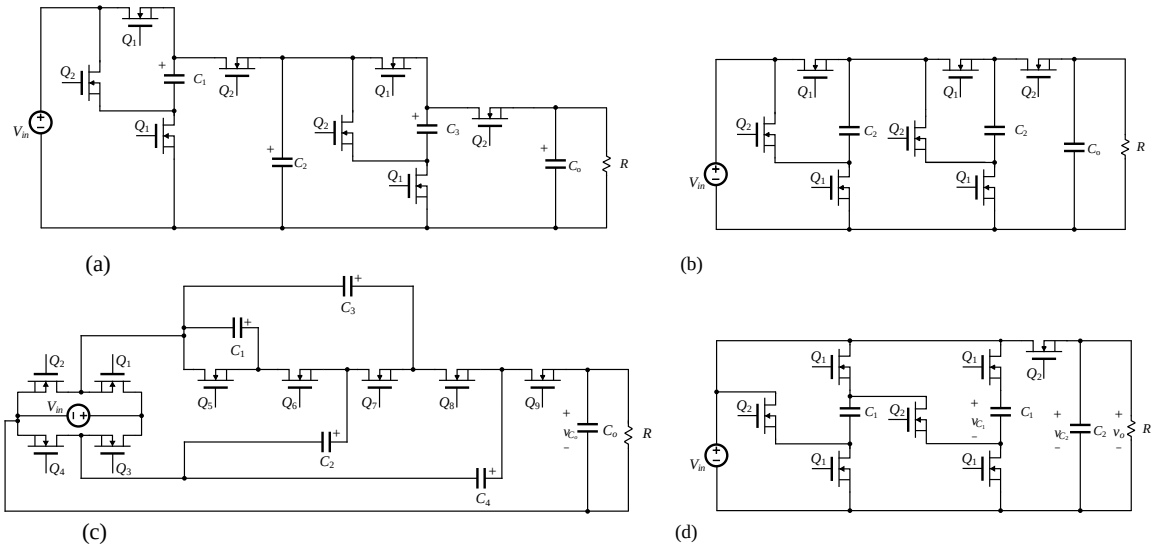

Figure 1.8. Example of common switched capacitor circuits a) Cascaded voltage doubler b) Fibonacci SC c) Dickson SC d) Series parallel SC

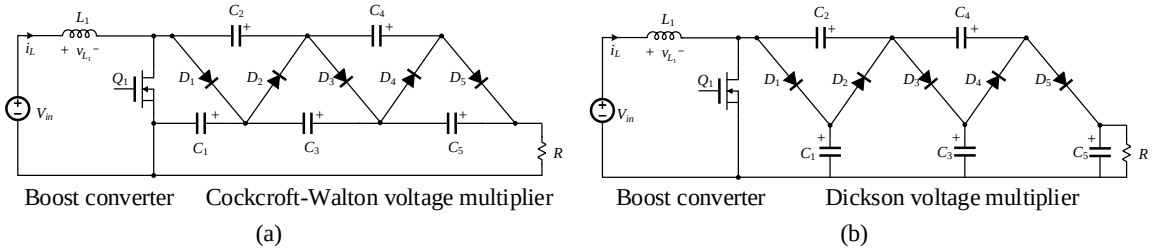

Figure 1.9. Hybrid boost converter with a) Cockcroft-walton VMC b) Dickson VMC

Hybrid boost converters combine the switched capacitor or voltage multiplier cell with the CBC to increase the overall voltage gain, reduce the voltage stress across the switches, and reduce the critical inductance. A typical configuration of hybrid boost converters is shown in Figure 1.9, where the CBC is attached to Cockcroft-Walton or Dickson VMC. Although the voltage gain of the converter is high, the efficiency of such converter is compromised by the conduction losses in the high-current loop, which is the loop that contains the inductor and the active switch.

1.2.6. Interleaved Boost Converters. The interleaving technique connects two or more conventional boost converters on parallel, and switches them with a phase shift between phases [35, 35–37]. The current will be shared among phases, and therefore the current

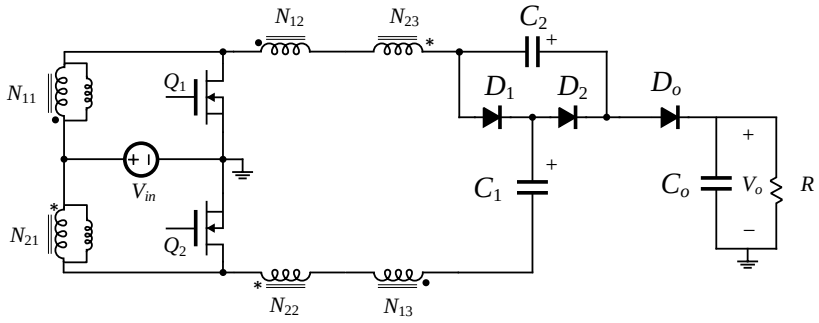

Figure 1.10. Interleaved boost converter with coupled inductors and voltage multipliers

stress is reduced as well as the conduction losses in the active switches and the magnetic elements. Interleaving two conventional boost converters increases the frequency of the input current and makes it easier to be filtered [38]. The voltage stress across the output diode, however, is still the same as in the conventional boost converter [39]. The voltage gain of the interleaved boost converter can be increased using VMC, coupled inductors, or both, such as in [40–42]. Figure 1.10 shows a two-phase interleaved boost converter with coupled inductors and VMCs. Using both VMC and coupled inductors, the voltage gain becomes a function of the turns ratio, VMC stages, and the duty cycles, which makes the converter scalable and has a wide range of output voltage. However, using coupled inductors might require energy circulation circuits and snubbers to reduce the voltage spikes across the switches.

The research in this dissertation is motivated by the drawbacks of the aforementioned topologies. Therefore, several topologies are presented to improve the existing topologies and attain desirable features, such as low voltage stresses and low voltage and current ripples.

1.3. RESEARCH CONTRIBUTION

This dissertation presents several novel DC-DC converter topologies suitable for renewable energy applications.

Paper I introduces a family of an interleaved high-voltage-gain boost converters with extended voltage multiplier cells. This group of converters has the capability of converting low input voltages ($12 - 48\ V$) to high output voltages, such as $380/400\ V$ DC bus. The general structure of the family consists of two stages: an interleaved boost stage and voltage multiplier cells. Either a single or multiple independent voltage sources can feed the interleaved boost stage, and each source can be controlled independently. The presented converters are compared, and the way of extending the voltage multiplier cells is illustrated. An example converter is provided, and its theory of operation and steady-state analysis is included. Then, the analysis results are verified by simulation and experimental results.

Paper II introduces an interleaved voltage multiplier with bi-fold Dickson voltage multiplier cells. The proposed converter in this paper also consists of two stages. However, the proposed topology has an enhanced VMC, which has two diodes and two capacitors per stage. The implementation bi-fold Dickson VMC and its derivation from original Dickson VMCs are illustrated, and their applicable use in various topologies are explained. The main advantage of the converter is the low voltage stress on all components; even the output capacitors share the output voltage equally. Another advantage is that the input current is shared between inductors equally regardless of the number of stages. Modes of operation and steady-state analysis are illustrated. The converter analysis is verified by simulation and A $200 - W$ hardware prototype.

Paper III Introduces a hybrid flyback and multilevel boost converters to be used as a high voltage gain DC-DC converter. The proposed converter has advantages of vertical interleaving, which can multiply the effective frequency seen by the magnetic element and therefore reduce the size and magnetic storage requirement. The converter uses a flyback transformer to increase the voltage gain by increasing the transformer turns ratio. The

converter has improvements over the conventional boost converter regarding the voltage stress across active switches and the effective frequency across the magnetic element. The proposed converter is an enhancement over the three-level boost converter for the voltage gain and over the fly-boost converter in terms of the required magnetic storage to operate in the continuous conduction mode.

Paper IV presents an interleaved switched-inductor boost converter with VMC. The proposed converter utilizes the self-lift cells to increase the voltage gain and reduce the inductors' currents so that the size of the inductors are reduced and the conduction power loss is also reduced. Few self-lift cells, both extended and basic, and some VMC can be used with the proposed converter. An example converter is illustrated with two basic self-lift cells with Cockcroft-Walton VMC cells.

PAPER

I. A FAMILY OF NON-ISOLATED INTERLEAVED BOOST CONVERTERS WITH VOLTAGE MULTIPLIER CELLS

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ABSTRACT

In this paper, a family of non-isolated interleaved high-voltage-gain DC-DC converters is presented. This family can be used in a wide variety of applications, such as in a photovoltaic systems interface to a high voltage DC distribution bus in a microgrid and an X-ray system power supply. The general structure of this family is illustrated and consists of two stages: an interleaved boost stage and a voltage multiplier stage. The interleaved boost stage is a two-phase boost converter, and it converts the input DC voltage to an AC square waveform. Moreover, using the interleaved boost stage increases the frequency of the AC components so that it can be easily filtered with smaller capacitors and, therefore, makes the input current smoother than the one from the conventional boost converter. The voltage multiplier cell (VMC) can be a Dickson cell, Cockcroft-Walton (CW), or a combination of the two. The VMC stage rectifies the square-shaped voltage waveform coming from the interleaved boost stage and converts it to a high DC voltage. Several combinations of VMCs and how they can be extended are illustrated, and the difference between them is

summarized so that designers can be able to select the appropriate topology for their applications. An example of this converter family is illustrated with detailed modes of operation, a steady-state analysis, and an efficiency analysis. The example converter was simulated to convert 20 V_{DC} to 400 V_{DC}, and a 200 W hardware prototype was implemented to verify the analysis and simulation. The results show that the example has a peak efficiency of 97% of this family of converters and can be very suitable for interfacing renewable energy sources to a 400 V_{DC} DC distribution system.

Keywords: Interleaved, boost, Step-up, High-gain, DC-DC, Renewable, Microgrid, PV, DC distribution, VMC, Modular

1. INTRODUCTION

The total power generation from renewable energy sources has been increasing rapidly and is predicted to increase threefold in the near future [1, 2]. The transition from using conventional and depletable energy sources in electricity generation to renewable and sustainable sources requires adaptable power infrastructure and high-efficiency power electronic converters. The power electronics play an indispensable role in renewable energy sources' integration to the main electric grid. Using highly efficient power converters could help customers save energy and therefore increase the economic benefits [3, 4]. The renewable energy market necessitates not only efficient, but also versatile and multipurpose, converters. Recently, the idea of integrating a low voltage PV panel to a 400 V DC distribution bus became a research interest due to the advantage of the DC distribution bus over AC. The DC distribution system has less conversion units and better efficiency, power quality, and performance than the AC distribution systems [5–9]. Integration of a single PV panel to a 400 V DC distribution system requires a high-gain DC-DC converter [10].

Several topologies found in the literature can be used as high-gain DC-DC converters [11–22]. However, there is no superior solution for all applications. The most common topology used to step up the input voltage is the conventional boost converter, which is the

most straightforward step-up converter [23]. However, the conventional boost converter would not have enough voltage gain for integrating renewable energy sources to a 400 V, but if it were to have enough voltage gain, it would be only when operating at a higher duty cycle, which might lead to the appearance of reverse recovery phenomena and low overall efficiency, especially if the inductor DC equivalent resistance is high. Moreover, the required inductance to stay in the continuous conduction mode is very large, and therefore, the converter requires large and bulky magnetics [24, 25].

Cascaded boost converters were introduced to replace the conventional boost converter. Such solutions increase the overall voltage gain and allow each converter to operate at a lower duty cycle [26]. However, cascading two or more converters at least doubles the power being processed, and that might compromise the efficiency as well. Moreover, controlling cascaded converters requires that the output impedance of a converter be lower than the input impedance of the following converter to ensure stability [27]. That might lead to complications in the design and control. Stacking two or more converters helps by sharing the power among different converters and allows the use of lower current rating devices [28]. However, the overall voltage gain is still the same as the voltage gain of the conventional boost converter.

Several converters can achieve higher voltage by incorporating either coupled inductors or transformers [29, 30]. Such topologies increase the voltage gain by increasing the turn ratio. However, several issues can arise. First, the leakage inductance can cause some voltage spikes across switching devices, and that might require some voltage clamp circuits. Second, incorporating such devices reduces the power density of the converter and increases the weight. Furthermore, the semiconductor materials will improve rapidly, while magnetic materials will not. Therefore, with the increase of switching frequency, the magnetic-based components might become the most significant culprits for power loss inside the converter. Thus, this paper introduces a family of converters that can have a high-voltage-gain ratio, continuous current, low stress across both active and passive de-

vices, and high power density. The proposed family consists of two stages: an interleaved boost stage and voltage multiplier cells. The interleaved boost stage reduces the variation of the input current so that it is easy to obtain more accurate measurements of the PV current to track the maximum power. The voltage multiplier cells increase the voltage gain and reduce the voltage stresses across switching devices. Moreover, the converter can achieve a high-voltage-gain ratio while operating at a lower duty cycle. The proposed family requires the lower value of critical inductance to keep the converter operating in the continuous conduction mode (CCM). The rest of the paper is structured as follows: Section 2 provides the theory of operation and the general structure of the proposed family. Section 3 presents different variations of the converter belonging to the proposed family. In Section 4, an example of the proposed converter is given and analyzed. In Section 5 and 6, the simulation and experimental results of the example converter are provided, respectively. Finally, conclusions and future work are described in Section 7.

2. THEORY OF OPERATION AND GENERAL STRUCTURE OF THE PROPOSED FAMILY

The general structure of the proposed family is shown in Figure 1, which consists of an interleaved boost stage followed by a voltage multiplier cell, and then it is either filtered using an output diode and capacitor capacitor as in Figure 1(a) or using an LC filter as shown in Figure 1(b). By using an output diode and a capacitor filter, the output of VMC is further increased by $\frac{1}{1-d}$ but the output current is discontinuous. On the contrary, when using an LC filter, the output voltage of the VMC is not increased, but the output current is continuous if the inductor is large enough to operate in the CCM mode. Several papers present members belonging to the proposed family [31–37]. However, no information about extending the VMC cells or the interleaved boost phases has been reported. The following sections present details about each stage of the proposed family.

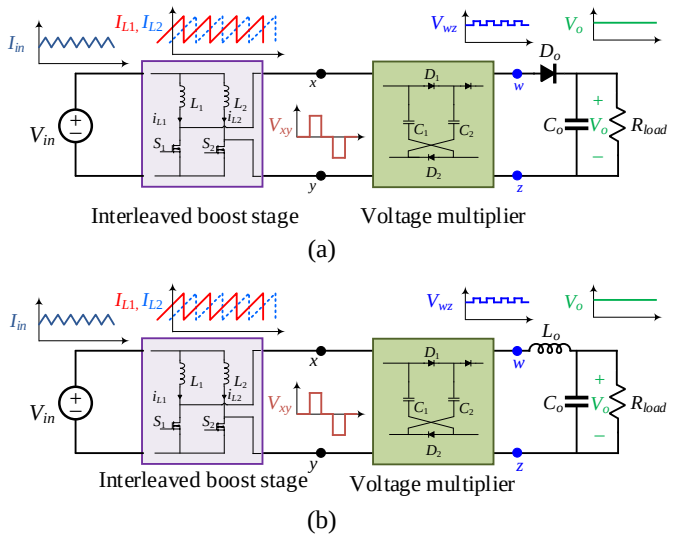

Figure 1. General structure of the proposed family: (a) with output diode and capacitor (b) with LC filter output

2.1. INTERLEAVED BOOST STAGE

The IBC stage consists of two or more phases. Each phase consists of an inductor and a low-side active switch. Since the IBC stage is a current source, the active switches can be closed simultaneously with no need for a dead time insertion circuit as in the voltage-fed converters. A phase shift between the active switches is vital to reduce the current ripples from the input current and therefore reduce the size of the input filter. A recommended phase shift between active switches can be given by

$$Shift = \frac{360^\circ}{\phi} \tag{1}$$

where ϕ is the number of interleaved phases, which is a positive integer greater than or equal to two. To ensure the continuity of the input current and to prevent a voltage-second imbalance in the inductors, the minimum duty cycle is given by

$$D \geq \frac{\phi - 1}{\phi}. \tag{2}$$

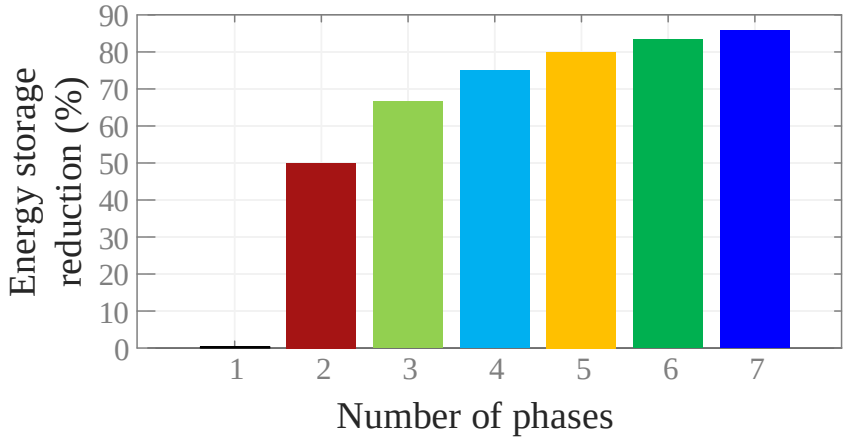

Figure 2. Reduction of energy storage at multiple phases. In case of two phases, the required energy storage is reduced by 50%.

Besides reducing the current ripples, the interleaved boost stage reduces the magnetic storage. In the case of two-phase, and assuming the inductors share the input current equally, the reduction in the magnetic element is half as follows:

$$\frac{E_2}{E_1} = \frac{\frac{1}{2}L\left(\frac{I}{2}\right)^2 + \frac{1}{2}L\left(\frac{I}{2}\right)^2}{\frac{1}{2}LI^2} \times 100 = 50\%. \tag{3}$$

The reduction for E_ϕ is given by κ as

$$\kappa(\%) = (1 - \frac{1}{\phi}) \times 100. \tag{4}$$

Figure 2 shows the percentage of the reduction of a different number of phases. The reduction becomes insignificant as the number of phases increases. The reduction of the magnetic volume ζ does not follow (4) as illustrated in [38]. Instead, one should compare the volume reduction as follows:

$$\zeta = \frac{Volume_{n=1} - \phi Volume_{n=\phi}}{Volume_{n=1}} \times 100 \tag{5}$$

where $Volume_{n=1}$ is the volume of the magnetic element in a single phase converter and $Volume_{n=\phi}$ is the volume of the magnetic element of a multiphase converter with ϕ phases. Another advantage of interleaving is that the total conduction loss in the inductors and the active switching devices is reduced if the current is shared equally between the phases as follows:

$$P_{L_{total}} = \frac{I_L^2 \times R_{DC}}{\phi}, \tag{6}$$

$$P_{S,cond_{total}} = \frac{I_{S,rms}^2 \times R_{ON}}{\phi}. \tag{7}$$

The input current ripples depend on the number of interleaved phases and the duty cycle. Figure 3 shows the relationship between the number of stages and the normalized input ripples. Increasing the number of phases reduces the ripples and allows ripple cancellation to occur at multiple duty cycle values. Two phases can have one point of ripple cancellation at the 0.5 duty cycle; while in three phases the ripple cancellation occurs at two points: the 0.25 and 0.75 duty cycles. For more phases, the duty cycle values where ripple cancellation can occur are given by

$$d_{\Delta v=0} = [\frac{1}{\phi}, \frac{2}{\phi}, ..., \frac{\phi - 1}{\phi}] \tag{8}$$

Figures 4(a) and (b) show the schematic and output waveforms of the interleaved boost stage for two and three phases, respectively. The switching waveforms and modes of operations are shown in Figure 5 for two phases and Figure 6 for three phases. More phases can be used, such as in [39], but three or more phases will not have a uniform pattern of connections to the VMC, and the permutation of variation of the topologies is large. Therefore, the number of phases is limited to two in this paper.

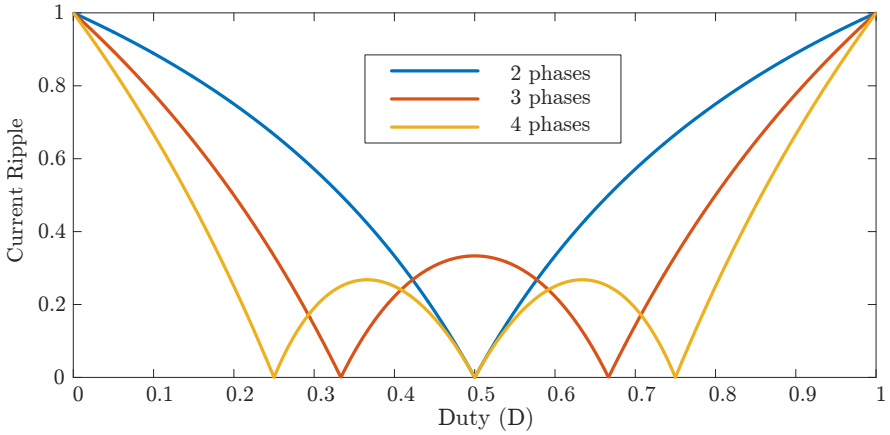

Figure 3. The normalized current ripples with respect to a single phase boost converter.

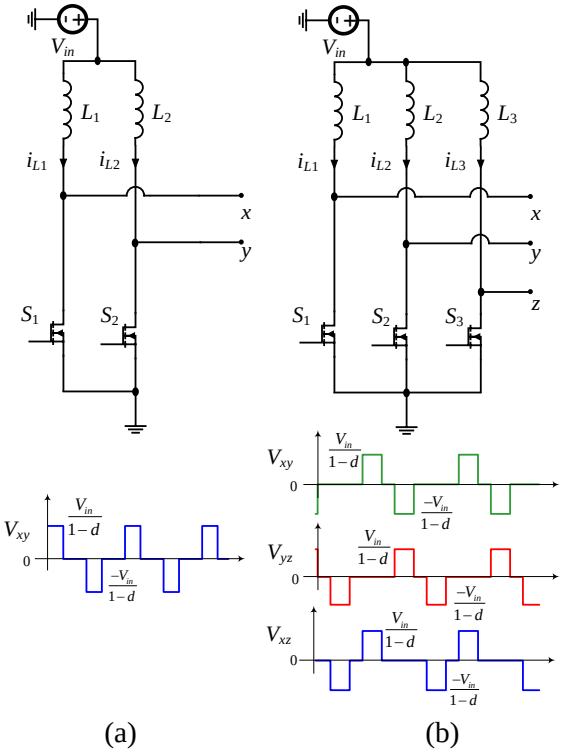

Figure 4. Interleaved boost stage with output waveforms: (a) two phases (b) three phases.

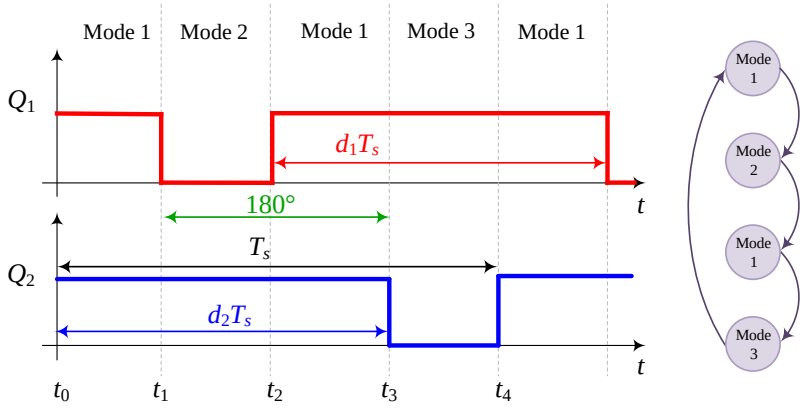

Figure 5. The switching pattern for the two-phase interleaved boost converter. The active switches are driven by two out of phase signals, and the converter operates in three modes of operation in the CCM.

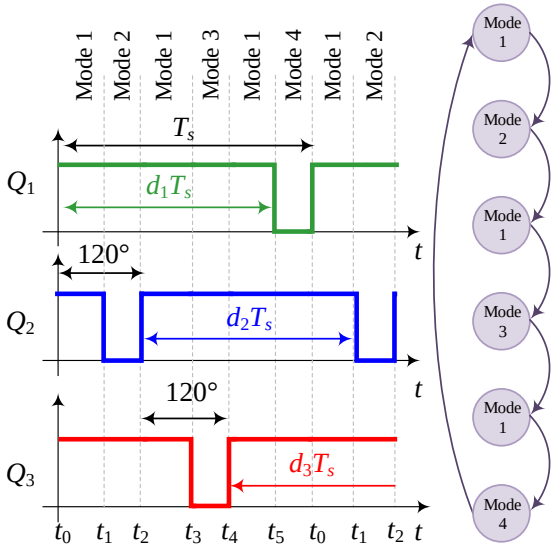

Figure 6. The switching pattern for a three-phase interleaved boost converter. The converter is driven by three signals with a phase shift of 120°, and the converter operates at four modes of operation in the CCM.

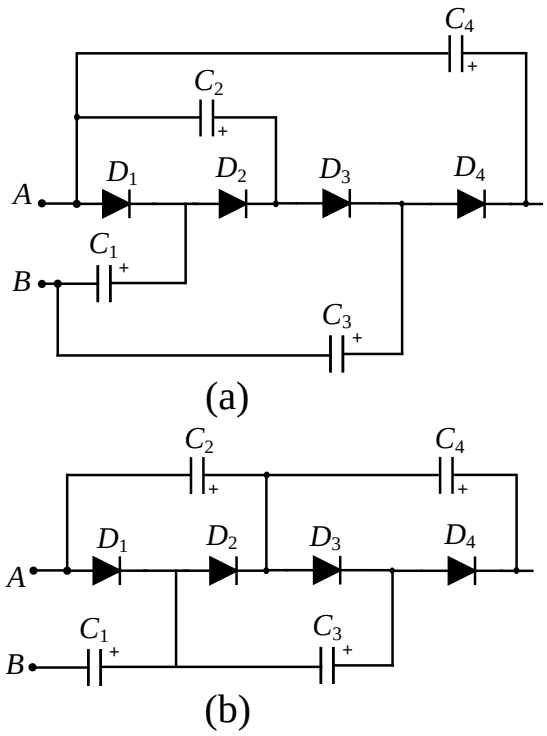

Figure 7. Two main voltage multiplier cells: (a) Dickson VMC (b) Cockcroft-Walton VMC.

2.2. VOLTAGE MULTIPLIER STAGE

The voltage multiplier stage rectifies the modified squared waveform that comes from the interleaved boost stage and boosts the voltage to a higher level. The VMC stage consists of capacitors and diodes. The two main extendable VMCs are the Dickson VMC and Cockcroft-Walton VMC, as shown in Figure 7. The main difference between these VMCs is the way capacitors are connected. In the Dickson VMC, all negative sides of the even capacitors are connected to phase a, and all negative sides of the odd capacitors are connected to phase b. In the Cockcroft-Walton VMC, each negative side of the odd capacitor is connected to the positive side of the previous odd capacitor, and each negative side of the even capacitor is connected to the positive side of the previous even capacitor. Various combinations are derived out of these two VMCs, as in [40–45] .

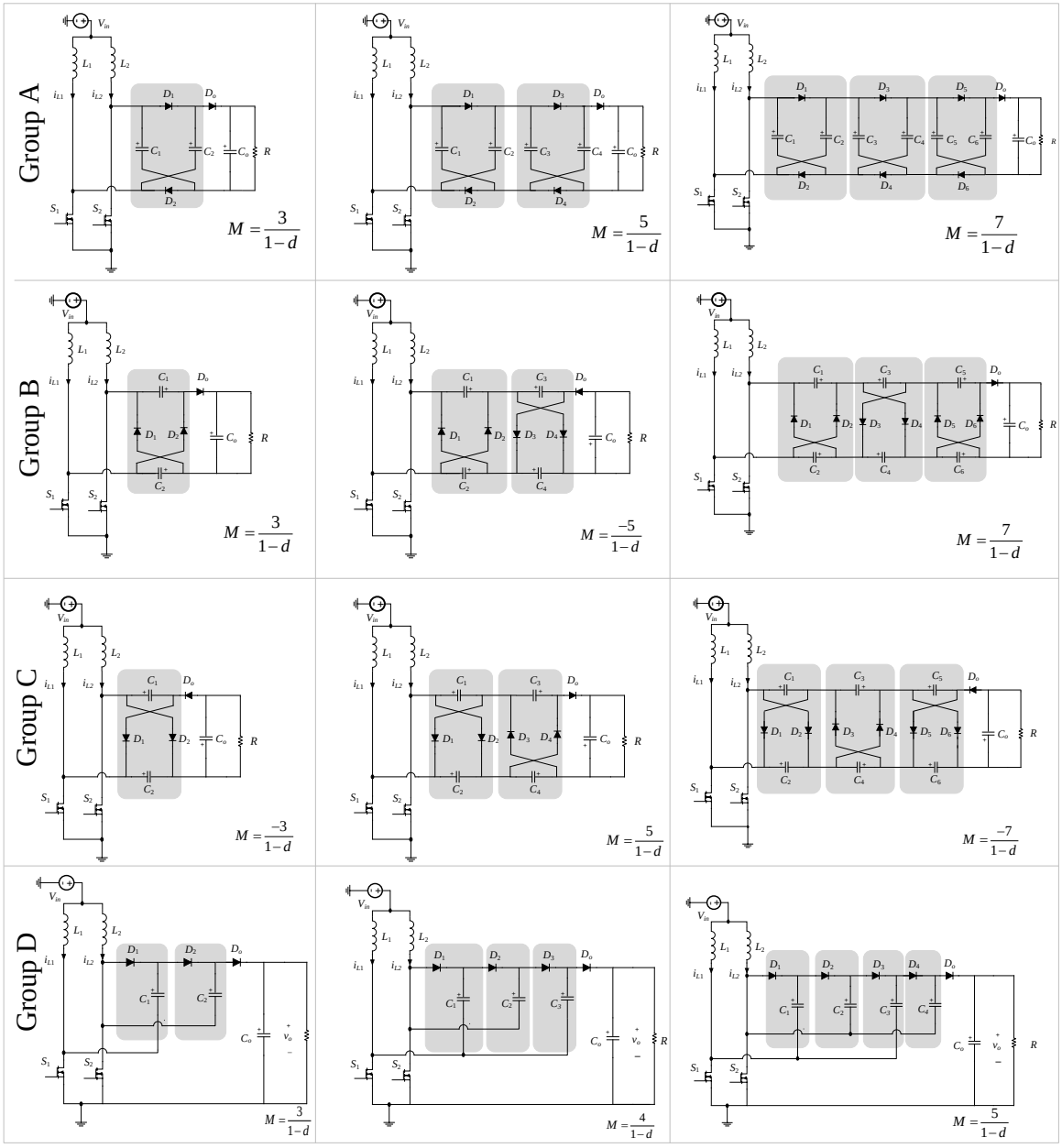

Figure 8. Various topologies belong to the interleaved boost converter with voltage multiplier cells (group A-D). The output is filtered using an output diode and a capacitor filter.

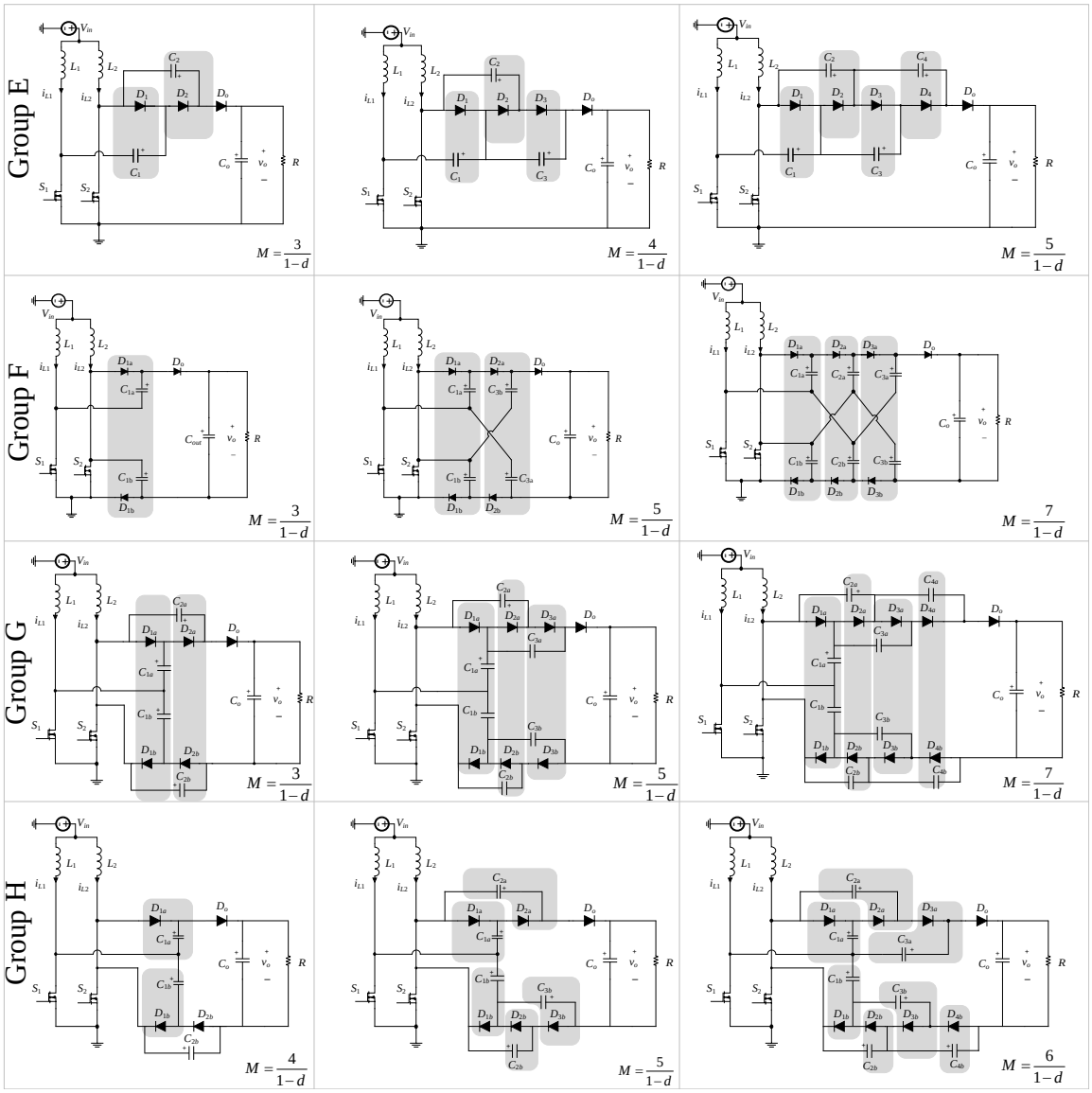

Figure 9. Various topologies belong to the interleaved boost converter with voltage multiplier cells (group E-H): with an output diode and a capacitor filter.

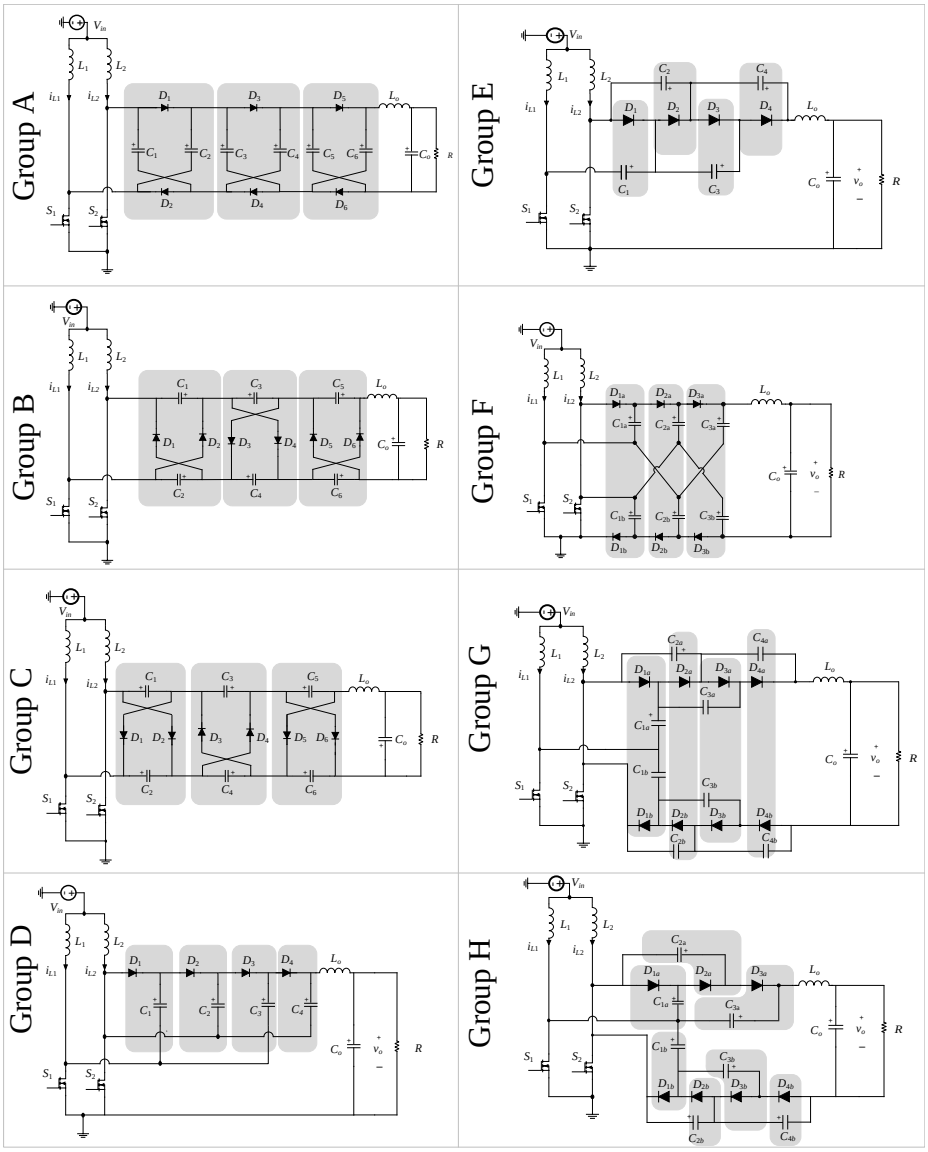

Figure 10. Using an output LC filter instead of a diode-capacitor for the same groups aforementioned.

2.3. TOPOLOGIES OF A TWO-PHASE INTERLEAVED BOOST CONVERTER WITH VMCS

Figures 8 and 9 show different interleaved boost converters with different VMCs and a diode capacitor filter. Figure 10 shows the same groups, but with an LC output filter instead of a diode-capacitor filter. Group A uses cross capacitor VMC cells. This group is analyzed in [46]. Group B and C have cross diode VMC cells, and similar work is presented in [47]. The cells can start in the inverting cells, as in group B, or non-inverting VMC stage, as in group C. To extend the VMC in these two groups, each cell must be followed by a cell with the opposite polarity. For example, the first stage in group B is positive (the diodes are upward), so it must be followed by a negative cell (diodes are downward), and vice versa. The polarity of the output voltage depends on the polarity of the last cell. Group D has Dickson VMC [10], and group E consists of Cockcroft-Walton [48]. Group F contains the example converter and will be analyzed in this paper. Group G has two CW chains, and it can have either the same or a different number of cells on each chain. Finally, Group H uses Dickson cells on one phase and Cockcroft-walton VMC on the other phase with either the same or a different number VMC stages. Several interleaved boost converters with VMCs belonging to this family can be found in the literature such as [49], where the Dickson VMC is modified to have lower voltage stress across capacitors without changing the overall voltage gain.

The main difference between these groups is how internal capacitors are charged and discharged. Some other differences including the load connection type (floating, inverted, or grounded), the stress on the capacitors and diodes, and the number of components in each VMC stage. The VMC structure affects the sharing of the input current between phases in the interleaved boost stage. That is, in converters that have an output diode, if there is a single diode in each stage, then the current sharing can be equal if the number of stages is even. However, if there is an output diode and each stage of the VMC has two diodes, then

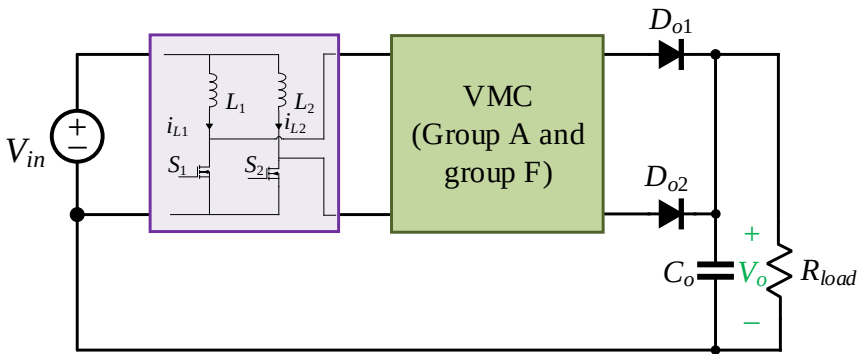

Figure 11. Modification to convert a floating output converter to a grounded output converter.

there will never be equal current sharing between the inductors. In converters where an LC filter is used, there will not be equal current sharing between phases. Table 1 summarizes the differences between the VMCs and illustrates this.

2.4. POSSIBLE MODIFICATIONS TO THE TOPOLOGIES

The presented family can be modified to obtain specific features such as isolation, where a transformer can be inserted between the interleaved boost stage and the VMC stage, or to convert a topology with a floating output to a grounded output.

2.4.1. Convert a Floating Output Converter to Grounded Output. Groups A and F have a floating output, where the output has a different reference point than the input. In voltage control mode, a differential sensor is required for the feedback loop. Designers can convert floating outputs to grounded outputs by adding a diode to the VMC, and connecting the output to the ground, as shown in Figure 11. Although the voltage stress across the components in the grounded output converter are still the same as the ones in the floating output converter, the voltage gain is significantly reduced. Figure 12 shows group A and F with the grounded output.

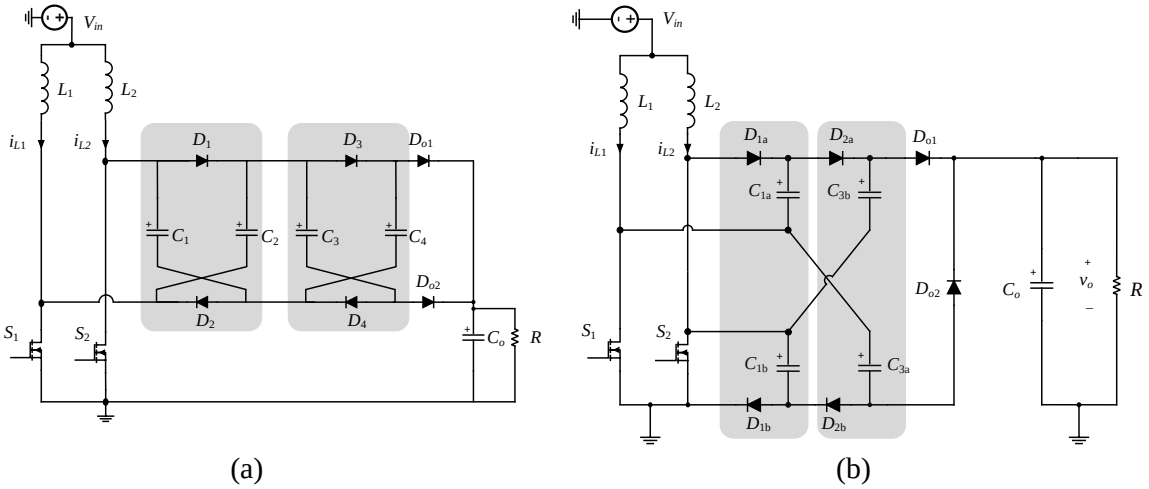

Figure 12. Group A and F can be converted to have a grounded output. Both have an ideal voltage gain of $M = \frac{N+1}{1-d}$, which is $\frac{N}{1-d}$ less than the ones with floating outputs.

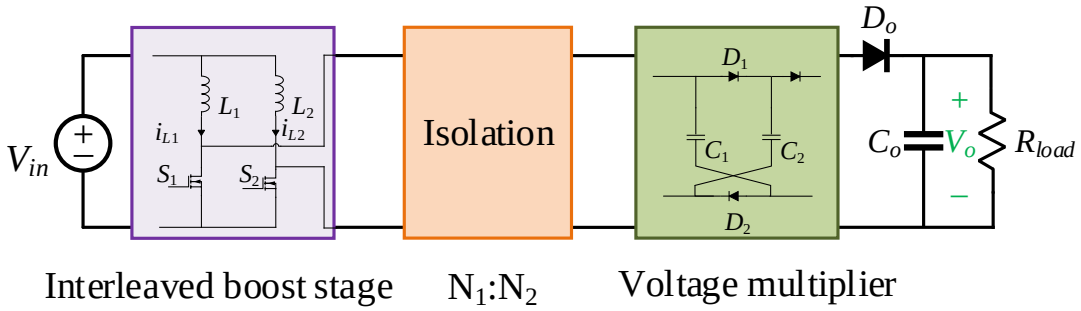

Figure 13. The presented family can be modified by adding an isolation device to meet the isolation requirement and improve the voltage gain.

2.4.2. Modification to Make the Converter Isolated. This family can easily be a family of isolated converters by adding a transformer or coupled inductors between the interleaved boost stage and the VMC stage, as shown in Figure 13. After adding the isolation device with an $N_1 : N_2$ turns ratio, the voltage gain can be calculated as

$$M_{isolated} = M_{nonisolated} \times \frac{N_2}{N_1} \tag{9}$$

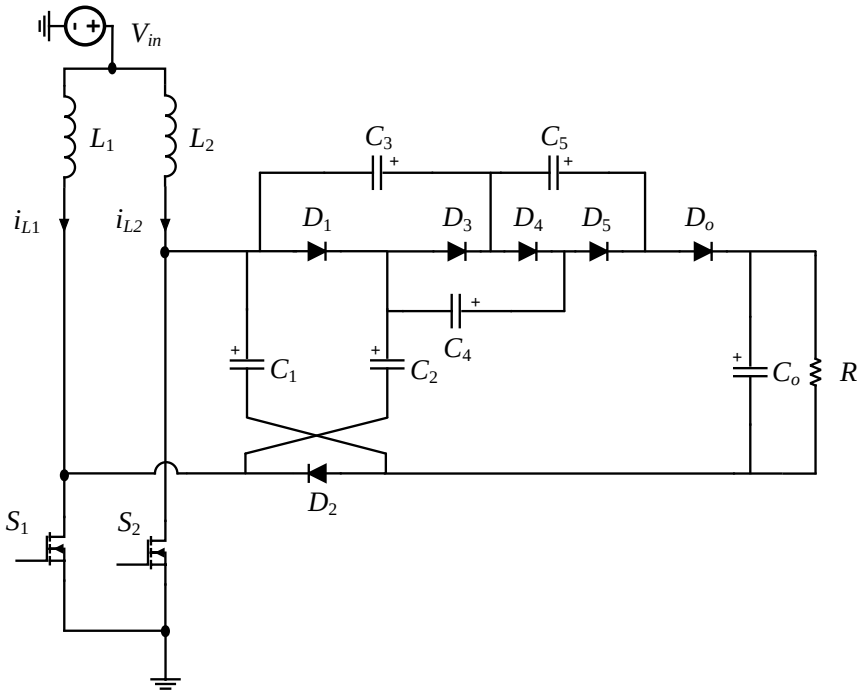

Figure 14. Example of nonuniform topologies. The converter features two different types of VMCs, a cell from group F and Cockcroft-Walton VMC.

2.4.3. Connecting Two Different VMCs to Obtain the Overall Nonuniform Converter. Extra possible combinations of different voltage multiplier cells can be derived, e.g., but will be unable to expand one or both VMCs. The analysis of nonuniform converters is performed on a case by case basis. Figure 14 shows an example of nonuniform combinations. The converter consists of one cell from group F followed by Cockcroft-Walton cells.

3. MODES OF OPERATION AND STEADY-STATE ANALYSIS OF AN EXAMPLE CONVERTER

This section presents a detailed analysis of the circuit, shown in Figure 15. The converter is driven by two 180° out phase signals, as shown in Figure 6. The equivalent circuit of the three modes is shown in Figure 16 (a-c). The analysis was performed with several assumptions: 1) All components are ideal; 2) The capacitors are large enough that

Table 1. Comparison of different interleaved DC-DC converters

				With output diode and capacitor filter (Figures. 8 and 9)		With *LC* filter (Figure 10)	
Group	Output	Diodes/stage	Caps/stage	Ideal voltage gain	$\frac{\langle I_{L_1}\rangle}{\langle I_{L_2}\rangle}$	Ideal voltage gain	$\frac{\langle I_{L_1}\rangle}{\langle I_{L_2}\rangle}$
A	Floating	2	2	$\frac{2N+1}{1-d}$	$\frac{N}{N+1}$	$\frac{2N}{1-d}$	$\begin{cases} \frac{N-1+d}{N+1-d} & N \text{ even} \\ \frac{N-d}{N+d} & N \text{ odd} \end{cases}$
B	Floating/ inverting	2	2	$\begin{cases} \frac{-(2N+1)}{1-d} & N \text{ even} \\ \frac{2N+1}{1-d} & N \text{ odd} \end{cases}$	$\frac{N+1}{N}$	$\begin{cases} \frac{-(2N)}{1-d} & N \text{ even} \\ \frac{2N}{1-d} & N \text{ odd} \end{cases}$	$\begin{cases} \frac{N+1-d}{N-1+d} & N \text{ even} \\ \frac{N+d}{N-d} & N \text{ odd} \end{cases}$
C	Floating/ inverting	2	2	$\begin{cases} \frac{-(2N+1)}{1-d} & N \text{ odd} \\ \frac{2N+1}{1-d} & N \text{ even} \end{cases}$	$\frac{N}{N+1}$	$\begin{cases} \frac{-(2N)}{1-d} & N \text{ odd} \\ \frac{2N}{1-d} & N \text{ even} \end{cases}$	$\begin{cases} \frac{N-d}{N+d} & N \text{ odd} \\ \frac{N+d-1}{N+1-d} & N \text{ even} \end{cases}$
D	Grounded	1	1	$\frac{N+1}{1-d}$	$\begin{cases} \frac{N}{N+2} & N \text{ even} \\ 1 & N \text{ odd} \end{cases}$	$\frac{N+1-d}{1-d}$	$\begin{cases} \frac{N+1-2d}{N+1} & N \text{ odd} \\ \frac{N}{N+2(1-d)} & N \text{ even} \end{cases}$
E	Grounded	1	1	$\frac{N+1}{1-d}$	$\begin{cases} \frac{N}{N+2} & N \text{ even} \\ 1 & N \text{ odd} \end{cases}$	$\frac{N+1-d}{1-d}$	$\begin{cases} \frac{N+1-2d}{N+1} & N \text{ odd} \\ \frac{N}{N+2(1-d)} & N \text{ even} \end{cases}$
F	Floating	2	2	$\frac{2N+1}{1-d}$	$\frac{N}{N+1}$	$\frac{2N}{1-d}$	$\frac{N+d}{N-d}$
G	Floating	2	2	$\frac{2N+1}{1-d}$	$\frac{N}{N+1}$	$\frac{2N}{1-d}$	$\frac{N+d}{N-d}$
H	Floating	$1/VMC_{dn}$ $1/VMC_{dn}$	$1/VMC_{dn}$ $1/VMC_{dn}$	$\begin{cases} \frac{2\ max(N_{up},N_{dn})}{1-d} & N_{up}+N_{dn} \text{ odd} \\ \frac{N_{up}+N_{dn}}{1-d} & N_{up}+N_{dn} \text{ even} \end{cases}$	1	$\frac{N_{up}+N_{dn}}{1-d}$	$\begin{cases} 1 & N_{up}+N_{dn} \text{ even} \\ \begin{cases} \frac{N_{up}-(1-d)}{N_{dn}+(1-d)} & N_{up} > N_{dn} \\ \frac{N_{up}+(1-d)}{N_{dn}-(1-d)} & N_{up} < N_{dn} \end{cases} & N_{up}+N_{dn} \text{ odd} \end{cases}$

ripples can be neglected; 3) The converter is operating in the steady-state condition; 4) The duty cycles of the active switches are symmetrical; and 5) The converter is fed by a single voltage source.

3.1. MODE 1: BOTH MOSFETS ARE ON

In this mode, both inductors draw energy from the source, and all diodes are in reverse biased mode. The output load is fed by the output capacitor. The voltage across the inductors is given by

$$v_{L_1} = v_{L_2} = V_{in}. \tag{10}$$

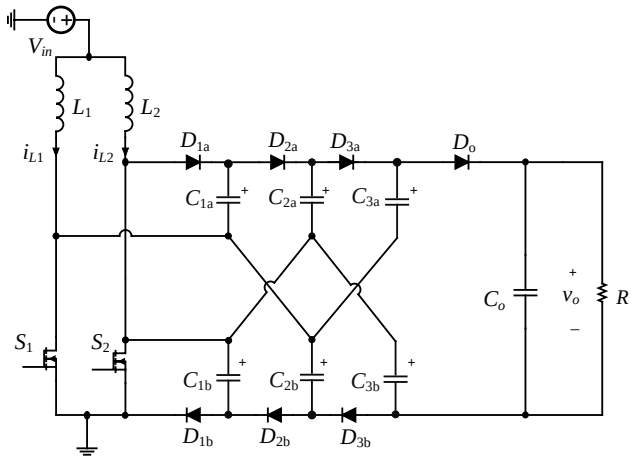

Figure 15. Example converter; an interleaved boost stage with a 3 level VMC

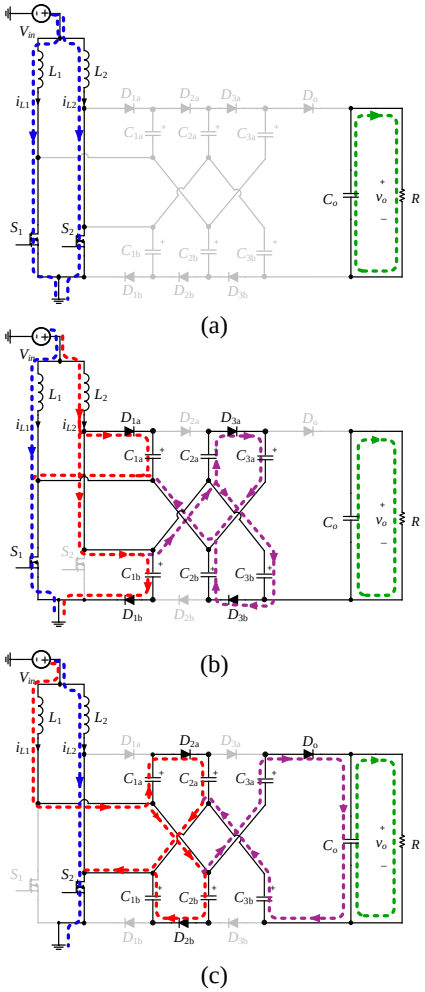

Figure 16. Modes of operation of the example converter; (a) mode 1 (b) mode 2 (c) mode 3

3.2. MODE 2: S_1 IS ON AND S_2 IS OFF

In this mode L_1 still draws energy from the source, L_2 discharges into the VMC capacitors, and all diodes are in reverse biased mode. The voltage across the inductors is given by

$$v_{L_1} = V_{in}, \tag{11}$$

$$v_{L_2} = V_{in} - V_{C_{1a}} = V_{in} - V_{C_{1b}} = V_{in} + V_{C_{2a}} - V_{C_{3a}} = V_{in} + V_{C_{2b}} - V_{C_{3b}}. \tag{12}$$

3.3. MODE 3: S_1 IS OFF AND S_2 IS ON

In this mode L_1 discharges into the VMC capacitors, L_2 draws energy from the source, and all diodes are in reverse biased mode. The voltage across the inductors is given by

$$v_{L_1} = V_{in} + V_{C_{1a}} - V_{C_{2a}} = V_{in} + V_{C_{1b}} - V_{C_{2b}} = V_{in} + V_{C_{3a}} + V_{C_{3b}} - V_o, \tag{13}$$

$$v_{L_2} = V_{in}. \tag{14}$$

3.4. STEADY-STATE VOLTAGE GAIN

Steady state equations can be derived from the state equations by a voltage-second balance on the inductors. The average voltage across the inductors is given by

$$\left\langle v_{L_1} \right\rangle = \left\langle v_{L_2} \right\rangle = 0 \tag{15}$$

The voltage across each first-stage capacitor is given by

$$V_{C_{1a}} = V_{C_{1b}} = \frac{V_{in}}{1 - D}. \tag{16}$$

The voltage of each second-stage capacitor is given by

$$V_{C_{2a}} = V_{C_{2b}} = \frac{2V_{in}}{1-D}. \tag{17}$$

Each third-stage capacitor's voltage is given by

$$V_{C_{3a}} = V_{C_{3b}} = \frac{3V_{in}}{1-D}. \tag{18}$$

Therefore, the output voltage transfer function is given by

$$M = \frac{V_o}{V_{in}} = \frac{7}{1-D}. \tag{19}$$

For N number of VMC stages, the transfer function is given by

$$M = \frac{2N+1}{1-D}. \tag{20}$$

The previous analysis was for a converter that is being fed by a single source, and equal duty cycles were assumed. The proposed converter is capable of being fed by two independent voltage sources, e.g., different PV panels, as shown in Figure 17. Also, it can operate at different duty ratios, which is suitable for tracking the maximum power point for each PV panel. The Table 2 summarizes the voltage gain in cases with two different sources and asymmetrical duty cycles.

4. COMPONENT SELECTIONS AND EFFICIENCY ANALYSIS

This section presents details about the design and component selections of the example converter.

Table 2. Output voltage at different cases of the input current and duty cycles

Case	the output voltage
$d_1 \neq d_2$ and $V_{in_1} \neq V_{in_2}$	$\frac{NV_{in_1}}{1-d_1} + \frac{(N+1)V_{in_2}}{1-d_2}$
$d_1 \neq d_2$ and $V_{in_1} = V_{in_2}$	$V_{in}(\frac{N}{1-d_1} + \frac{(N+1)}{1-d_2})$
$d_1 = d_2$ and $V_{in_1} \neq V_{in_2}$	$\frac{1}{1-d}(NV_{in_1} + (N+1)V_{in_2})$
$d_1 = d_2$ and $V_{in_1} = V_{in_2}$	$\frac{(2N+1)V_{in}}{1-d}$

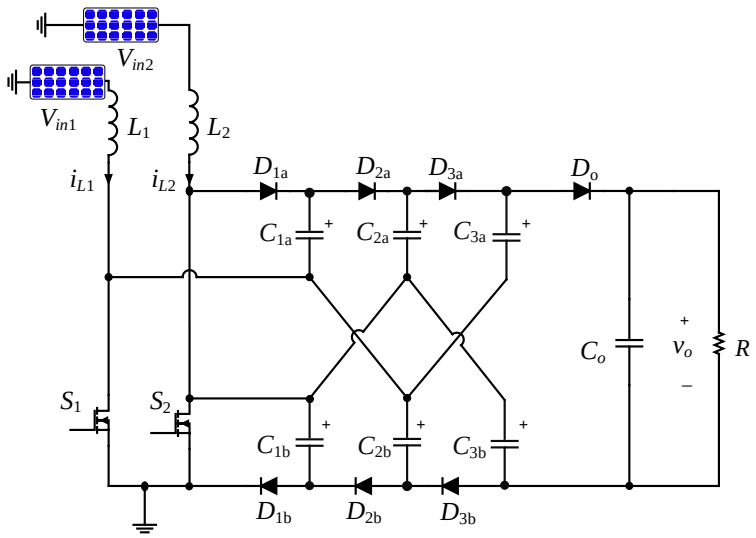

Figure 17. The example converter can convert the voltage from two independent power sources.

4.1. INDUCTOR SELECTION

The critical inductance that ensures CCM operation is given by

$$L_{1_{crit}} = \frac{Rd(1-d)^2}{N(2N+1)f_s}, \tag{21}$$

$$L_{2_{crit}} = \frac{Rd(1-d)^2}{(N+1)(2N+1)f_s}. \tag{22}$$

However, to select an inductor based on the percentage of the ripple, one should follow

$$L_1 = \frac{V_{in}d}{\Delta i_{L_1} f_s}, \tag{23}$$

$$L_2 = \frac{V_{in}d}{\Delta i_{L_2} f_s}. \tag{24}$$

The average current passing through inductors L_1 and L_2 is as follows:

$$I_{L_{1,avg}} = \frac{V_o}{R}\frac{N}{(1-d)}, \tag{25}$$

$$I_{L_{2,avg}} = \frac{V_o}{R}\frac{N+1}{(1-d)}. \tag{26}$$

The peak currents can be calculated as follows:

$$I_{L_{1,pk}} = \frac{V_o}{R}\frac{N}{(1-d)} + \frac{dV_{in}}{Lf_s}, \tag{27}$$

$$I_{L_{2,pk}} = \frac{V_o}{R}\frac{N+1}{(1-d)} + \frac{dV_{in}}{Lf_s}. \tag{28}$$

The RMS currents are given by

$$I_{L_{1,rms}} = \sqrt{\left(\frac{V_o N}{R(1-d)}\right)^2 + \left(\frac{dV_{in}}{2\sqrt{3}Lf_s}\right)^2}, \tag{29}$$

$$I_{L_{2,rms}} = \sqrt{\left(\frac{V_o(N+1)}{R(1-d)}\right)^2 + \left(\frac{dV_{in}}{2\sqrt{3}Lf_s}\right)^2}. \tag{30}$$

4.2. ACTIVE SWITCHES SELECTION

The voltage stress across MOSFETs can be calculated by

$$V_{S_1} = V_{S_2} = \frac{V_{in}}{1-d} \tag{31}$$

and the average current passing through the MOSFETs is given by

$$I_{S_{1,avg}} = \frac{V_o}{R}\left(\frac{dN}{1-d} + N + 1\right), \tag{32}$$

$$I_{S_{2,avg}} = \frac{V_o}{R}\left(\frac{d(N+1)}{1-d} + N\right). \tag{33}$$

The root mean square value of the switch current is given by

$$I_{S_{1_{rms}}} = \sqrt{\left(\frac{V_o}{R}\left(\frac{dN}{1-d} + N + 1\right)\right)^2 + \left(\frac{(2N+1)V_{in}(2d-1)}{2Lf_s}\right)^2}, \tag{34}$$

$$I_{S_{2,rms}} = \sqrt{\left(\frac{V_o}{R}\left(\frac{d(N+1)}{1-d} + N\right)\right)^2 + \left(\frac{(2N+1)V_{in}(2d-1)}{2Lf_s}\right)^2}. \tag{35}$$

4.3. DIODE SELECTION

The voltage stress across the diodes is a function of the number of stages. The voltage stress is reduced as the number of stages increases, and that comes at the cost of efficiency. The voltage stress is given by

$$V_D = \frac{2V_o}{(2N+1)}. \tag{36}$$

The average current passing through each diode can be calculated by

$$I_{D_N,avg} = I_o \tag{37}$$

and the RMS value of the diodes can be calculated as

$$I_{D,rms} = I_o\sqrt{\frac{1}{1-d}}. \tag{38}$$

4.4. CAPACITOR SELECTION

The capacitor is selected based on the tolerated voltage ripple, and it can be calculated using the following equation

$$C = \frac{I_o(1-d)}{f\Delta v}. \tag{39}$$

The RMS value of the current passing through the output capacitor is given by

$$I_{C_o,rms} = I_o\sqrt{\frac{d}{(1-d)}} \tag{40}$$

and the RMS current of the other capacitors can be calculated by

$$I_{C_n,rms} = I_o(1+\sqrt{\frac{d}{(1-d)}}) \tag{41}$$

5. POWER LOSSES AND EFFICIENCY ANALYSIS

The power losses in the inductors are given by

$$P_L = I^2_{L_{1,rms}} DCR_1 + I^2_{L_{2,rms}} DCR_2 \tag{42}$$

where DCR_1 and DCR_2 are the DC resistance. The power losses in the active switches can be divided into two parts: switching loss and conduction loss. The switching loss can be calculated using the following equation:

$$\begin{aligned} P_{SW} &= 2(\frac{1}{2} \times I_{L,avg} \times V_S \times (t_{OFF} + t_{ON}) f_s \\ &\quad + \frac{1}{2} \times f_s \times C_{oss} \times V_S^2). \end{aligned} \tag{43}$$

The conduction loss part is given by

$$P_{S,conduction} = I_{s_{1,rms}}^2 R_1(on) + I_{S_{2,rms}}^2 R_2(on) \tag{44}$$

where $R_1(on)$ and $R_2(on)$ are the drain-source resistance of S_1 and S_2. The power loss in the diodes can be calculated by

$$P_D = \sum_{i=1}^{N} I_{D_{avg}} \times V_F + \sum_{i=1}^{N} I_{D_{rms}} \times r_f \tag{45}$$

where V_F is the forward voltage of the diode, and r_f is the bulk resisor. The power loss in the capacitors due to the equivalent series resistance (ESR) is given by

$$P_{C,total} = N I_{C_{n,rms}}^2 ESR_n + I_{C_{o,rms}}^2 ESR_o. \tag{46}$$

The total loss is given by

$$P_{loss} = P_{D,total} + P_{C,total} + P_{S,conduction} + P_{SW} + P_L \tag{47}$$

The overall efficiency of the converter is given by

$$\eta\% = \frac{P_o}{P_{loss} + P_o} \times 100. \tag{48}$$

6. SIMULATION

The example converter was simulated in PLECS/MATLAB, with a maximum time step of 10^{-7} s and tolerance of 10^{-3}. The parameters used in the simulation are listed in Table 3. The major waveforms are plotted in Figure 18. The voltage stress across the active switches is 57 V. The average current on L_1 and L_2 is 4.28 A and 5.7 A, respectively. The maximum voltage across the diodes is 114 V. The average and effective values of the current passing through each diode are 0.5 A and 0.84 A. The voltage across the capacitors is shown in Figure 19. The currents passing through the diodes and capacitors are shown in Figure 20 and Figure 21, respectively. The first-stage capacitors $C_{1_A}$and C_{1_B} have a voltage of 57 V, the second-stage capacitors have a voltage of 114 V, and the third-stage capacitors have a voltage of 171 V. The RMS current of the output capacitor is 0.68 A, while the other capacitors have an RMS current of 1.18 A. The efficiency analysis was performed using the loss equations of the components and the rating from the datasheets of the components used for implementing the hardware prototype. The approximate loss breakdown and breakdown percentage as a function of the output load is depicted in Figure 22. The total loss at 200 W is about 4.98 W. The major source of loss is the conduction loss in the diodes, which counts for about 68%. The conduction loss in the MOSFETs is about 13%, and the switching loss is about 7% of the total loss. The conduction loss in the inductors counts for about 11%, and the total loss caused by the ESR of the capacitors is less than 1%.

7. EXPERIMENTAL IMPLEMENTATION AND RESULTS

A 200 W hardware prototype was implemented and tested to further verify the operation of the example converter. The components used to construct the hardware prototype are listed in Table 4, and the experimental setup is shown in Figure 23. The converter was designed for a nominal duty cycle of 0.65 and increased to roughly 0.657 to compensate for the gain reduction caused by the diodes' forward voltage and losses in

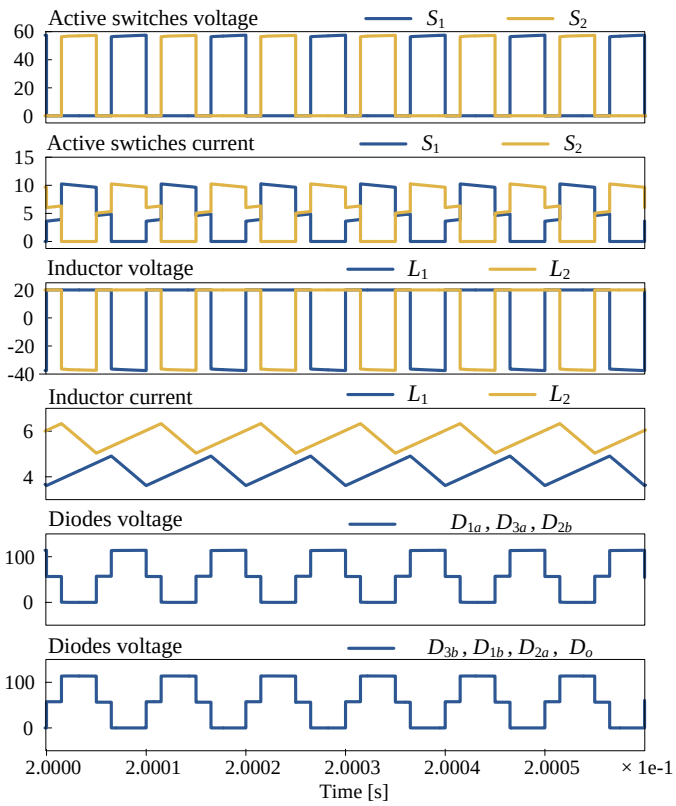

Figure 18. Simulation waveforms of voltages and currents across semiconductor switches and inductors

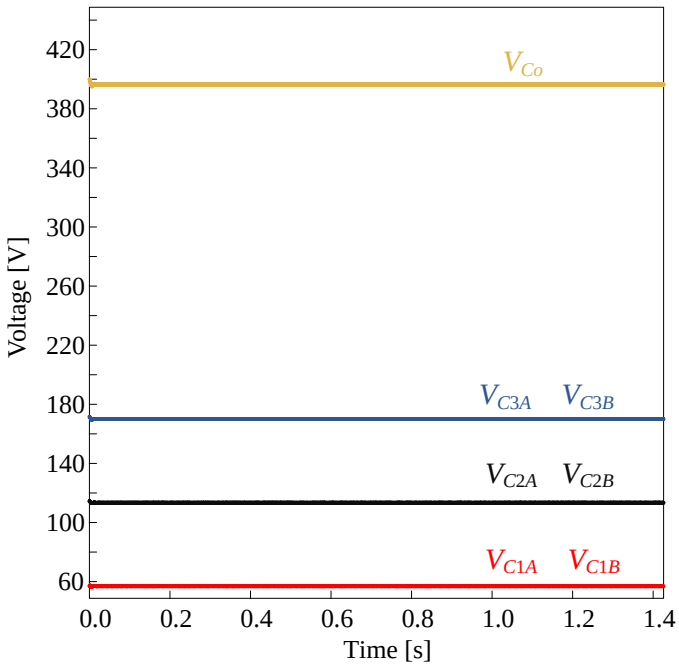

Figure 19. Simulation waveforms of the capacitors' voltage and the output voltage in the steady-state

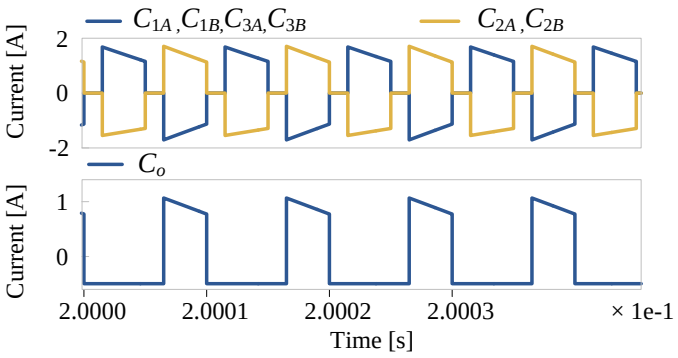

Figure 20. Simulation of the capacitors' currents

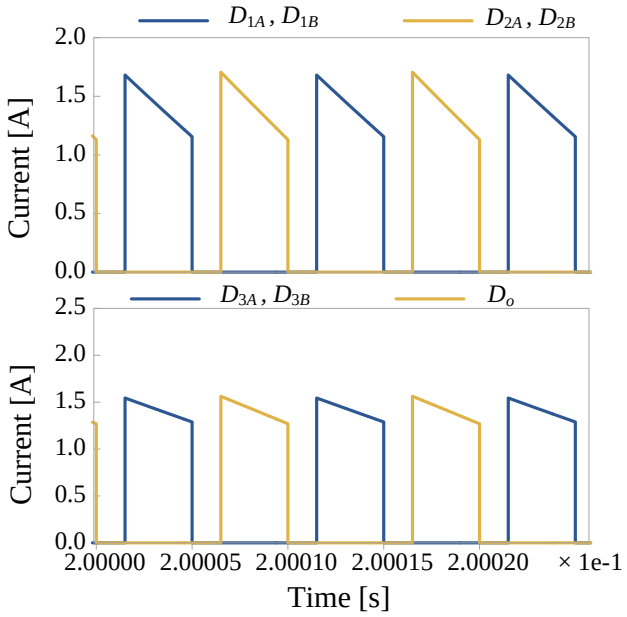

Figure 21. Simulation waveforms of the diodes' currents

Table 3. List of Parameters used in simulation

Parameter	Value
Input voltage	20 V
Output voltage	400 V
Load resistance	800 Ω
Ideal duty cycle	0.65
Switching frequency	100 kHz
Inductors	100 μH
Capacitors	10 μF

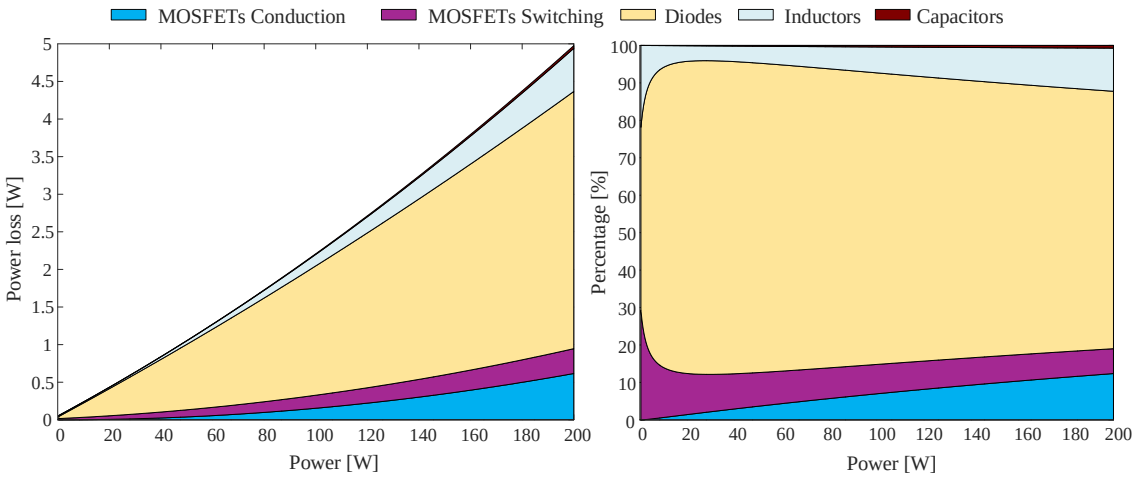

Figure 22. Efficiency analysis of the example converter; the actual losses (left) and the loss breakdown (right)

wires. The $AFG3052C$ signal generator was used to generate gate signals with a switching frequency of 50 kHz. The converter is fed by 20 V, where $N5700$ power supply is used, and the output load is implemented using ceramic resistors with various values. The voltage stress across the active switches and diodes are shown in Figure 24, which supports the simulation results as the voltage across the active switches equals 57 V, and the maximum voltage stress across the diodes equals 124 V. The voltage across the capacitors is shown in Figure 25. The voltage across each capacitor in the first stage equals 57 V, in the second stage equals 133 V, and in the third stage equals 200 V. The output voltage equals 400 V. The current waveforms of inductors, switches, and capacitors were acquired at $\approx$ 100 W, as shown in Figure 26 and 27. The peak efficiency of the converter is about 97% at 160 W and about 96.3% at 200 W.

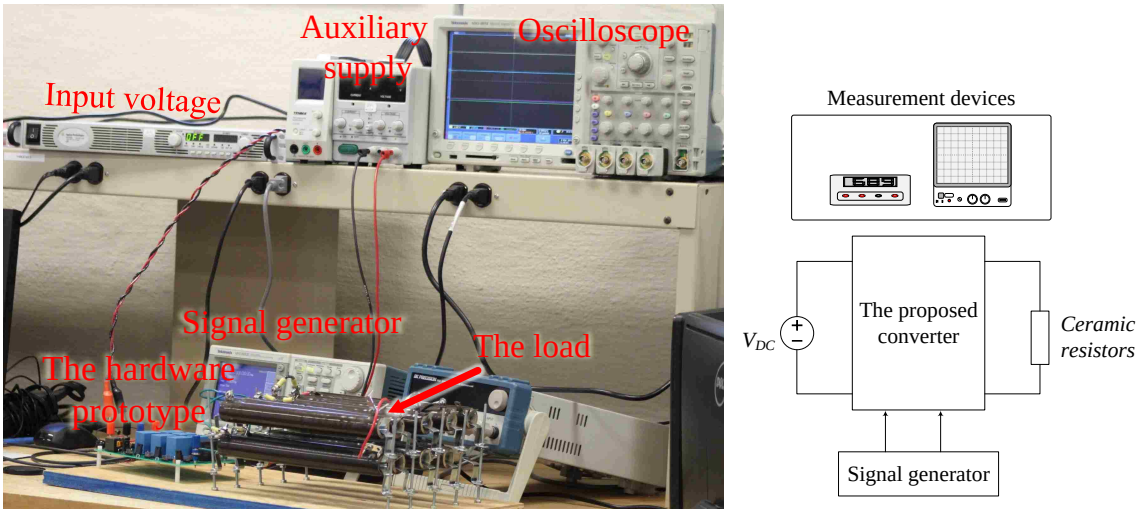

Figure 23. The hardware prototype and the experimental setup

Table 4. List of Components used for the hardware prototype

Item	Designation	Rating	Part No.
Inductor	L_1, L_2	100 μH, DCR = 25 $m\Omega$,	60B104C
Capacitor	C_{1A}, C_{2A} $C_{1B}C_{2B}$ $C_{3A}C_{3B}$	10 μF	B32674D3106K
Capacitor	C_o	22 μF	B32774D4226K000
MOSFET	Q_1, Q_2	150 V, 37 A $R_{ds(on)}$ = 10.525 $m\Omega$	IPA105N15N3
Diode	D_{1A}, D_{2A} D_{1B}, D_{2B}	250V, 40A V_F = 0.86 V, t_{rr} = 35 ns	MBR40250G
load	R_{load}	multiple values	L100J100E, L225J50RE L225J250E,L225J500E

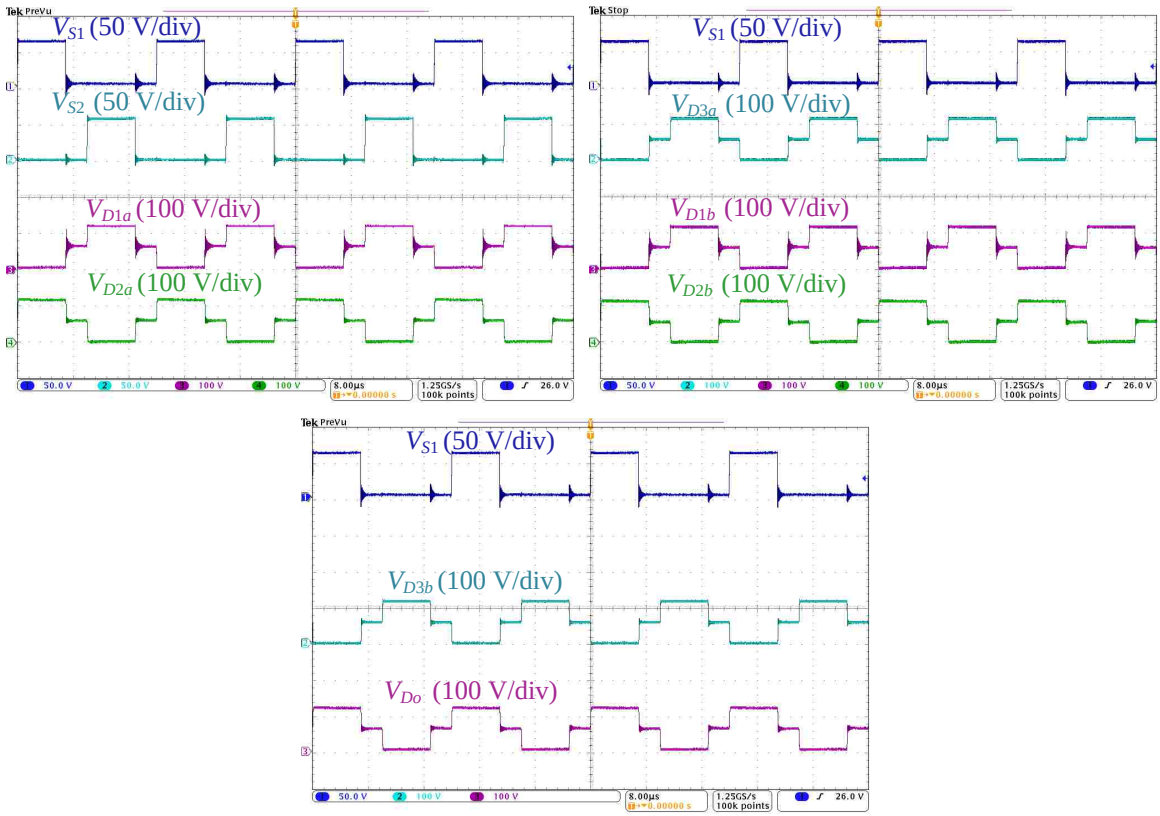

Figure 24. Experimental results of the voltage across the active switches and the diodes

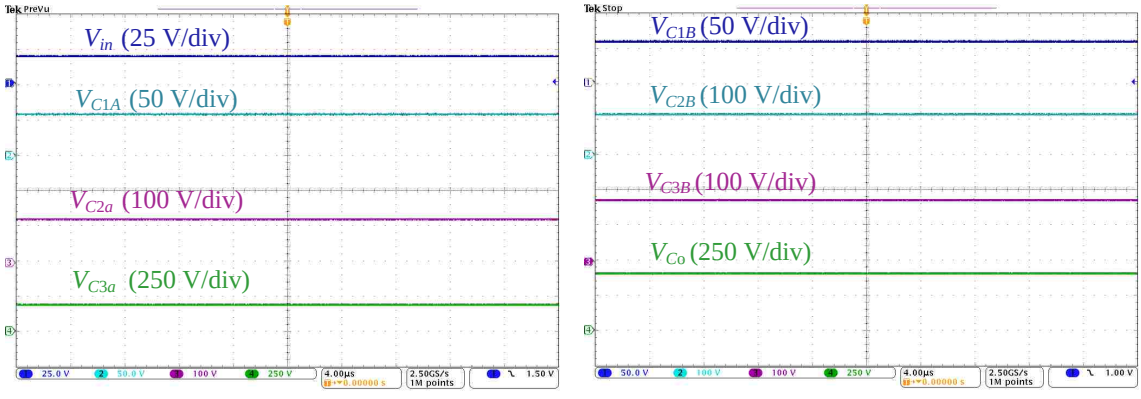

Figure 25. Experimental results of the voltage across the capacitors

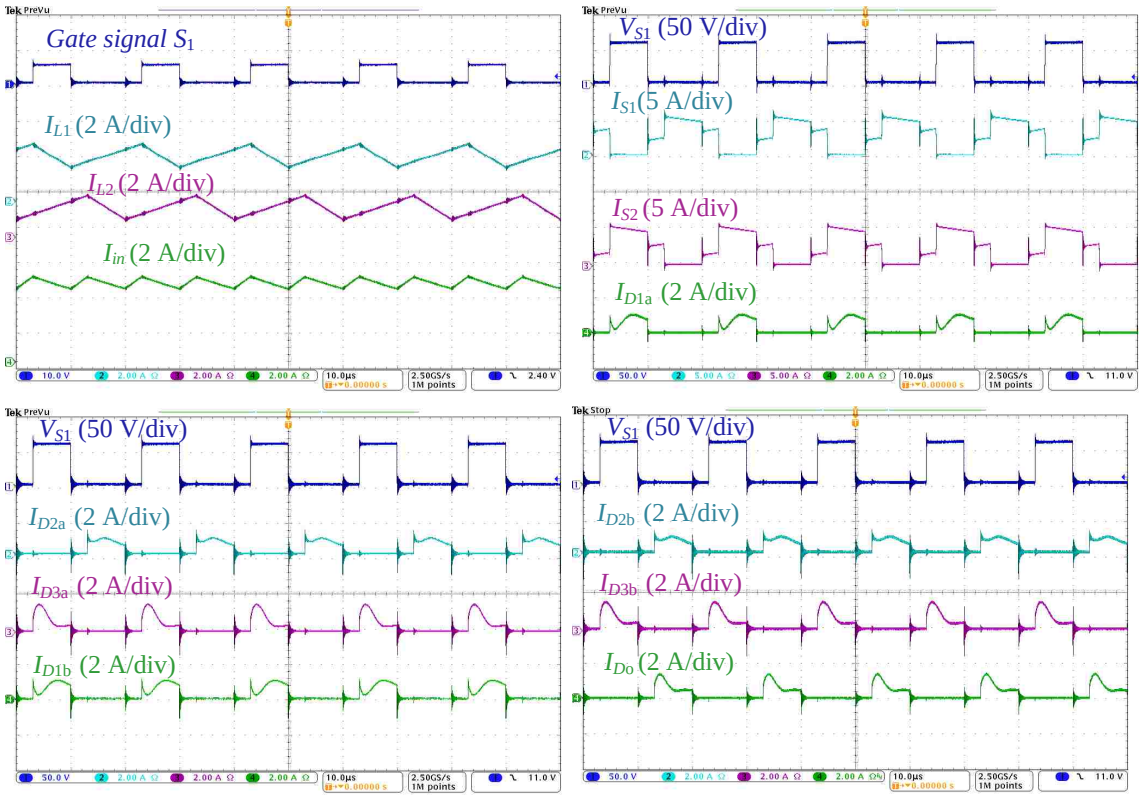

Figure 26. Experimental results of the input current, inductor currents, active switches and diode currents

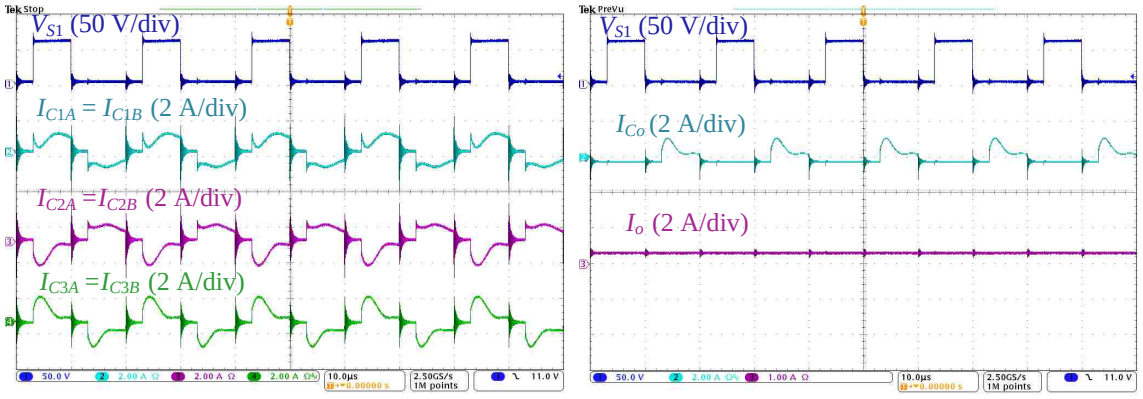

Figure 27. Experimental results of the capacitors' currents and the output current

8. CONCLUSION

In this paper, the family of an interleaved boost converter with voltage multiplier cells was presented. The general structure of the family consists of two sections: an interleaved boost stage and voltage multiplier cells. The structure comes in two configurations. Configuration 1's output is filtered using an output diode and a capacitor filter, where configuration 2's output is filtered using an LC filter. The difference between the two configurations was explained, and a comparison between the various family members was presented. An example of this family was given with a detailed steady-state analysis and component selection, which was evinced by simulation. A 200-W hardware prototype was implemented to further verify the analysis and the simulation. The converter is capable of drawing power from both a single or dual independent input voltage and with the same or different duty cycles of the active switches. These cases were summarized and compared. The family has good features besides the high-voltage gain. The input current ripple has twice frequency of the one in the conventional boost converter, which reduces the filter requirements and increases the accuracy of the current sensing for better tracking of MPPT. Although the converter is efficient, the efficiency can be further increased by either replacing the diodes with better ones or with active switches, with a trade-off of the complexity.

REFERENCES

[1] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid converters for photovoltaic and wind power systems*. John Wiley & Sons, 2011, vol. 29.

[2] F. Blaabjerg, Y. Yang, and K. Ma, "Power electronics - key technology for renewable energy systems - status and future," in *2013 3rd International Conference on Electric Power and Energy Conversion Systems*, Oct 2013, pp. 1–6.

[3] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstübner, "Performance trends and limitations of power electronic systems," in *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*. IEEE, 2010, pp. 1–20.

[4] J. D. van Wyk and F. C. Lee, "On a future for power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59–72, 2013.

[5] V. A. K. Prabhala, B. P. Baddipadiga, and M. Ferdowsi, "Dc distribution systems; an overview," in *2014 International Conference on Renewable Energy Research and Application (ICRERA)*, Oct 2014, pp. 307–312.

[6] A. Pratt, P. Kumar, and T. V. Aldridge, "Evaluation of 400v dc distribution in telco and data centers to improve energy efficiency," in *INTELEC 07 - 29th International Telecommunications Energy Conference*, Sept 2007, pp. 32–39.

[7] P. T. Krein, "Data center challenges and their power electronics," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 1, pp. 39–46, 2017.

[8] D. J. Hammerstrom, "Ac versus dc distribution systemsdid we get it right?" in *2007 IEEE Power Engineering Society General Meeting*, June 2007, pp. 1–5.

[9] A. Mohamed and O. Mohammed, "Connectivity of dc microgrids involving sustainable energy sources," in *2011 IEEE Industry Applications Society Annual Meeting*, Oct 2011, pp. 1–8.

[10] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi, "A dc–dc converter with high voltage gain and two input boost stages," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4206–4215, 2016.

[11] R.-J. Wai, C.-Y. Lin, R.-Y. Duan, and Y.-R. Chang, "High-efficiency dc-dc converter with high voltage gain and reduced switch stress," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 354–364, 2007.

[12] L.-S. Yang, T.-J. Liang, and J.-F. Chen, "Transformerless dc–dc converters with high step-up voltage gain," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 3144–3152, 2009.

[13] Q. Zhao and F. C. Lee, "High-efficiency, high step-up dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 65–73, 2003.

[14] S.-M. Chen, T.-J. Liang, L.-S. Yang, and J.-F. Chen, "A cascaded high step-up dc–dc converter with single switch for microsource applications," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1146–1153, 2011.

[15] N. Denniston, A. M. Massoud, S. Ahmed, and P. N. Enjeti, "Multiple-module high-gain high-voltage dc–dc transformers for offshore wind energy systems," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 5, pp. 1877–1886, 2011.

[16] Z. Liang, R. Guo, J. Li, and A. Q. Huang, "A high-efficiency pv module-integrated dc/dc converter for pv energy harvest in freedm systems," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 897–909, 2011.

[17] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Transformerless dc-dc converters with a very high dc line-to-load voltage ratio," in *Circuits and Systems, 2003. ISCAS'03. Proceedings of the 2003 International Symposium on*, vol. 3. IEEE, 2003, pp. III–III.

[18] S. Dwari and L. Parsa, "An efficient high-step-up interleaved dc–dc converter with a common active clamp," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 66–78, 2011.

[19] T.-F. Wu, Y.-C. Chen, J.-G. Yang, and C.-L. Kuo, "Isolated bidirectional full-bridge dc–dc converter with a flyback snubber," *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1915–1922, 2010.

[20] F. S. Silva, A. A. Freitas, S. Daher, S. C. Ximenes, S. K. Sousa, M. Edilson, F. L. Antunes, and C. M. Cruz, "High gain dc-dc boost converter with a coupling inductor," in *Power Electronics Conference, 2009. COBEP'09. Brazilian*. IEEE, 2009, pp. 486–492.

[21] V. Yaramasu and B. Wu, "Three-level boost converter based medium voltage megawatt pmsg wind energy conversion systems," in *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*. IEEE, 2011, pp. 561–567.

[22] J.-M. Kwon, B.-H. Kwon, and K.-H. Nam, "Three-phase photovoltaic system with three-level boosting mppt control," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2319–2327, 2008.

[23] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

[24] F. L. Tofoli, D. de Souza Oliveira, R. P. Torrico-Bascopé, and Y. J. A. Alcazar, "Novel nonisolated high-voltage gain dc-dc converters based on 3ssc and vmc," *IEEE Transactions on Power Electronics*, vol. 27, no. 9, pp. 3897–3907, Sept 2012.

[25] F. L. Tofoli, D. d. C. Pereira, W. J. de Paula, and D. d. S. Oliveira Júnior, "Survey on non-isolated high-voltage step-up dc-dc topologies based on the boost converter," *IET Power Electronics*, vol. 8, no. 10, pp. 2044–2057, 2015.

[26] R. Haroun, A. E. Aroudi, A. Cid-Pastor, G. Garcia, C. Olalla, and L. Martínez-Salamero, "Impedance matching in photovoltaic systems using cascaded boost converters and sliding-mode control," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3185–3199, June 2015.

[27] M. Veerachary and S. B. Sudhakar, "Stability analysis of cascaded dc-dc power electronic system," in *2007 7th International Conference on Power Electronics and Drive Systems*, Nov 2007, pp. 1422–1426.

[28] M. T. V. and I. Barbi, "Nonisolated high step-up stacked dc-dc converter based on boost converter elements for high power application," in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, May 2011, pp. 249–252.

[29] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up dc-dc converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143–9178, Dec 2017.

[30] B. P. R. Baddipadiga, V. A. Prabhala, and M. Ferdowsi, "A family of high-voltage-gain dc-dc converters based on a generalized structure," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2017.

[31] R. Gules, L. L. Pfitscher, and L. C. Franco, "An interleaved boost dc-dc converter with large conversion ratio," in *2003 IEEE International Symposium on Industrial Electronics (Cat. No.03TH8692)*, vol. 1, June 2003, pp. 411–416 vol. 1.

[32] C.-M. Lai, Y.-C. Lin, and D. Lee, "Study and implementation of a two-phase interleaved bidirectional dc/dc converter for vehicle and dc-microgrid systems," *Energies*, vol. 8, no. 9, pp. 9969–9991, 2015.

[33] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 871–887, March 2008.

[34] W. Li, Y. Zhao, Y. Deng, and X. He, "Interleaved converter with voltage multiplier cell for high step-up and high-efficiency conversion," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2397–2408, 2010.

[35] P. Kim, S. Lee, J. Park, and S. Choi, "High step-up interleaved boost converters using voltage multiplier cells," in *Power Electronics and ECCE Asia (ICPE and ECCE), 2011 IEEE 8th International Conference on*. IEEE, 2011, pp. 2844–2851.

[36] W. Li and X. He, "Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1239–1250, April 2011.

[37] L. Zhou, B. Zhu, Q. Luo, and S. Chen, "Interleaved non-isolated high step-up dc/dc converter based on the diode-capacitor multiplier," *IET Power Electronics*, vol. 7, no. 2, pp. 390–397, February 2014.

[38] M. O'Loughlin, "An interleaving pfc pre-regulator for high-power converters," *Texas Instruments*, pp. 1–14, 2006.

[39] J. Roy and R. Ayyanar, "Sensor-less current sharing over wide operating range for extended-duty-ratio boost converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8763–8777, Nov 2017.

[40] T. Nouri, S. H. Hosseini, E. Babaei, and J. Ebrahimi, "Generalised transformerless ultra step-up dc–dc converter with reduced voltage stress on semiconductors," *IET Power Electronics*, vol. 7, no. 11, pp. 2791–2805, 2014.

[41] E. H. Ismail, M. A. Al-Saffar, and A. J. Sabzali, "High conversion ratio dc–dc converters with reduced switch stress," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 7, pp. 2139–2151, Aug 2008.

[42] J. C. Rosas-Caro, J. C. Mayo-Maldonado, R. Salas-Cabrera, A. Gonzalez-Rodriguez, E. N. Salas-Cabrera, and R. Castillo-Ibarra, "A family of dc-dc multiplier converters," *Engineering Letters*, vol. 19, no. 1, pp. 57–67, 2011.

[43] Y. J. A. Alcazar, D. de Souza Oliveira, F. L. Tofoli, and R. P. Torrico-Bascopé, "Dc–dc nonisolated boost converter based on the three-state switching cell and voltage multiplier cells," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4438–4449, Oct 2013.

[44] M. A. Al-Saffar and E. H. Ismail, "A high voltage ratio and low stress dc–dc converter with reduced input current ripple for fuel cell source," *Renewable Energy*, vol. 82, pp. 35–43, 2015.

[45] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, "Bidirectional converter for high-efficiency fuel cell powertrain," *Journal of Power Sources*, vol. 249, pp. 470–482, 2014.

[46] A. Alzahrani, P. Shamsi, and M. Ferdowsi, "A novel non-isolated high-gain dc-dc boost converter," in *2017 North American Power Symposium (NAPS)*, Sept 2017, pp. 1–6.

[47] A. Alzahrani, P. Shamsi, and M. Ferdowsi, "An interleaved non-isolated dc-dc boost converter with diode-capacitor cells," in *2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA)*, Nov 2017, pp. 216–221.

[48] L. Müller and J. W. Kimball, "High gain dc–dc converter based on the cockcroft–walton multiplier," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6405–6415, 2016.

[49] B. P. Baddipadiga and M. Ferdowsi, "A high-voltage-gain dc-dc converter based on modified dickson charge pump voltage multiplier," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7707–7715, Oct 2017.

II. HIGH-VOLTAGE-GAIN DC-DC STEP-UP CONVERTER WITH BI-FOLD DICKSON VOLTAGE MULTIPLIER CELLS

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ABSTRACT

This paper presents an interleaved boost converter with a bi-fold Dickson voltage multiplier suitable for interfacing low-voltage renewable energy sources to high-voltage distribution buses and other applications that require a high-voltage-gain conversion ratio. The proposed converter was constructed from two stages: an interleaved boost stage, which contains two inductors operated by two low-side active switches, and a voltage multiplier cell (VMC) stage, which mainly consists of diodes and capacitors to increase the overall voltage gain. The proposed converter offers a high-voltage-gain ratio with low voltage stress on the semiconductor switches as well as the passive components. This allows the selection of efficient and compact components. Moreover, the required inductance that ensures operation in the continuous conduction mode (CCM) is lower than the one in the conventional interleaved boost converter. The distinction of the proposed converter is that the inductors' currents are equal, regardless of the number of VMCs. Equal sharing of interleaved boost-stage currents reduces the conduction loss in the active switches as well as the inductors and thus improves the overall efficiency, as the conduction power loss is a quadratic function. In this paper, the theory of operation and steady-state analysis of the proposed converter are illustrated and verified by simulation results. A 200 W hardware prototype was implemented to convert a 20 V to a 400 V DC load and validate both the theory and the simulation.

Keywords: High-Gain, bi-fold Dickson, DC-DC, VMC, Renewable, PV, Solar, MPPT

1. INTRODUCTION

Step-up DC-DC converters with high-voltage-gain ratios were only used in a limited number of applications, such as radar and X-ray systems. Currently, they are being used in a wide variety of applications such as photovoltaic (PV) panels' interface to a microgrid or a DC distribution bus, as shown in Figure 1(a), or power distribution unit (PDU) to power data centers and supercomputers [1], as shown in Figure 1(b). Both applications deploy a 400 V_{DC} distribution system due to its advantage over an AC distribution system in terms of the number of conversion units, size, cost, and immunity against load disturbances and ground faults [2–6]. Most PV panels have an output voltage range between 15 and 45 V [7], which is very low. Integrating a PV panel to a 400 V_{DC} is a challenging task and necessitates a high-voltage-gain step-up converter.

The conventional boost converter (CBC) requires operation at very high duty cycles to obtain a high-voltage-gain ratio. In practice, the gain of the CBC is limited by the conduction losses, and obtaining a high-voltage-gain ratio is not feasible. Not only that, but the CBC also suffers from the voltage stress and reverse recovery phenomenon at high voltages [8] and requires a large inductor to operate in the CCM. Derived topologies from the CBC, such as cascaded boost converters, can achieve a higher voltage and operate at low duty cycles [9, 10]. However, they suffer from low efficiency due to the power being processed multiple times and require complicated control and extra effort to ensure stability [11, 12]. The three-level boost converter is derived from the series-input series-output multiphase boost converter. The stress on the switches and inductance requirement is reduced. However, it still has the same gain as the CBC [13–15]. The single-switch quadratic boost converter has a simple structure and does not suffer from instability like the cascaded boost converter. However, the voltage and current stress across the switches are high, and the inductor that ensures the CCM operation is large. Using isolated topologies such as

forward, flyback, or full-bridge converters, the high-voltage-gain ratio at can be achieved lower duty cycles by increasing the turns ratio of the transformer [16–18]. However, such devices suffer from parasitic leakage inductance, which significantly increases the voltage stress on the active switches and can cause damage unless additional auxiliary is used [19]. Isolated converters generally have low power density, higher cost, and lower efficiency than non-isolated converters [20–22].

Using VMC with the CBC increases the voltage gain and improves the performance, as the total indirect power is reduced [23, 24]. Nevertheless, the inductor size is still relatively substantial to obtain a smooth input current. Therefore, topologies such as those found in [25, 26] use VMCs with an interleaved boost stage to reduce the magnetic storage requirement and obtain a smoother input current. The stress on the internal components depends on the VMC connections and the number of cells (e.g., the modified Dickson cell has lower voltage stress across the components than the original Dickson cell). This paper presents a high-gain interleaved DC-DC converter that is an improved version of [25, 26]. The features of the proposed converter can be summarized as follows: 1- The converter has a high-voltage-gain ratio that is sufficient for the integration of renewable energy sources to a high voltage DC bus. 2- The voltage stresses across active switches, diodes, and passive components are low, and that allows the selection of components whose cost, efficiency, and compactness are balanced. 3- The input current is shared equally between the two phases, regardless of the number of VMC stages. Therefore, the conduction loss of the interleaved boost stage and the thermal dissipation requirement are reduced. 4- The converter has two capacitors at each stage, in which voltage ripple cancellation is achieved. 5- The input current is continuous and has low ripple due to the interleaving. Hence, continuity of the input current reduces the filter requirement and allows accurate current measurement for maximum power point tracking (MPPT). 6- The converter does not need an output diode or an LC filter to rectify or regulate the output voltage such as in [25, 26]. Each stage can produce a constant DC voltage.

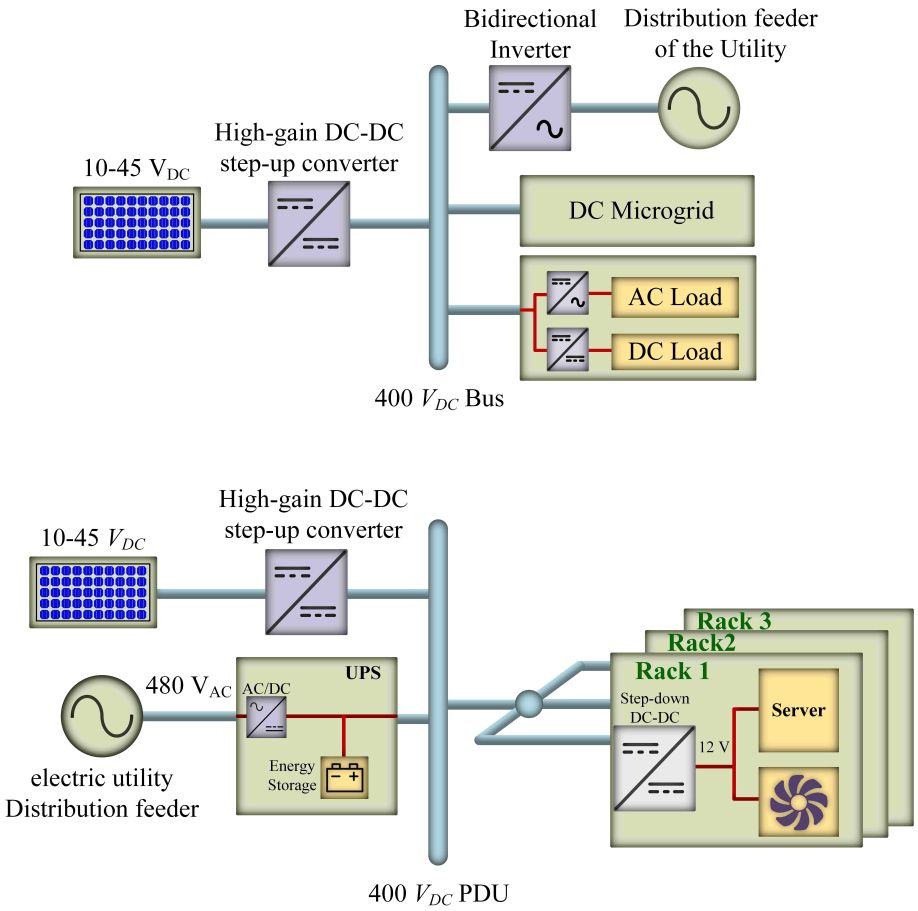

Figure 1. Application of a high-gain DC-DC converter

The rest of this paper is structured as follows. First, the construction of the bi-fold Dickson cell and the Dickson voltage multiplier is presented and explained in Section 2. The theory of operation and a comparison to similar converters is illustrated in Section 3. The analysis of CCM modes and steady-state voltage gain formulas are derived in Section 4. Section 5 presents the operation of the converter in the discontinuous conduction mode and the boundary conduction mode The component selections and their power loss models are derived in Section 6, and the simulation results are presented in Section 7. The implementation of the hardware prototype and the experimental results are explained in Section 8. Finally, conclusions and future work are presented in Section 9.

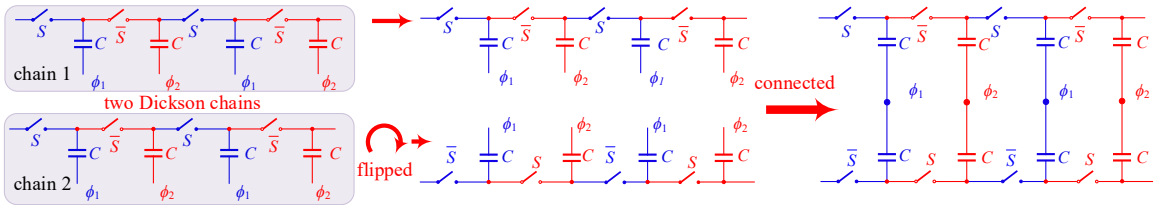

Figure 2. The construction of a bi-fold Dickson cell. The BD cell is constructed using two conventional Dickson cells, and one of the cells is rotated by 180°. Then, they are connected so that a single VMC stage consists of two complementary switches and two capacitors.

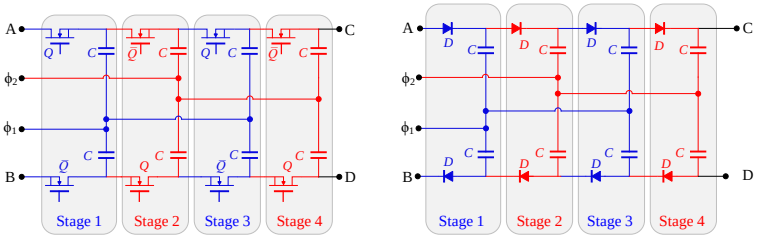

Figure 3. Implementation of a bi-fold Dickson switched capacitor (left) and a bi-fold voltage multiplier cell (right) with $N = 4$.

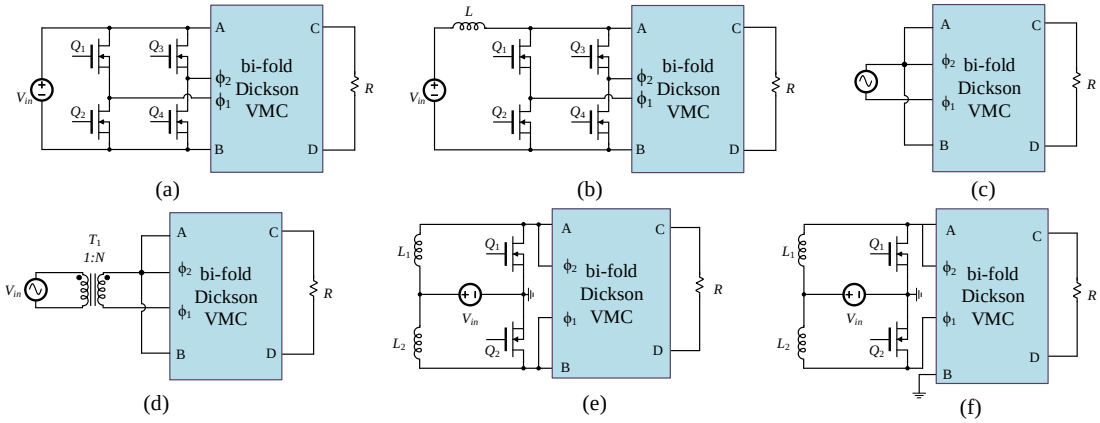

Figure 4. Several examples of using bi-fold Dickson VMC in various power electronics topologies. The VMC can be used in (a) a voltage-fed circuit, (b) a current fed circuit, (c-d) AC rectification circuits, and (d-e) interleaved high-voltage-gain DC-DC circuits.

2. CONSTRUCTION OF BI-FOLD DICKSON SC/VMCS

The conventional Dickson charge pump or voltage multiplier is shown in Figure 2. The circuit takes a DC input voltage and converts it to high-level voltage by charging and discharging internal capacitors. It has been utilized in a variety of applications, including nonvolatile memories, RF antenna switched controllers [27], and recently it was used for ultra step-up voltage ratio converters [26]. The challenge with a Dickson voltage multiplier is that the stress across the capacitors increases as the number of stages increases. Although multiple capacitors can be connected in a series to satisfy the voltage rating, voltage mismatches between capacitors might appear. One way to remove the mismatches is by connecting a resistance in parallel with the capacitors. That makes the resistance dissipate the excessive power. However, this method might not work in high power applications because of the high power dissipation and thermal limitations. Therefore, this paper introduces a bi-fold Dickson voltage multiplier to reduce the voltage stresses on both semiconductors and capacitors. The construction of the bi-fold Dickson cell is shown in Figure 2. The cell is constructed by using two traditional Dickson cells and rotating one by 180°. Then, the capacitors of the upper cell are connected to the capacitors of the lower cell. That is, phase ϕ_1 of the upper cell is connected to ϕ_1 in the lower cell, and likewise for the capacitors connected to phase ϕ_2. The proposed cell consists of multiple stages; each stage has two complementary switches and two capacitors. Either active switches or diodes can be used to implement the switches in the proposed cell, as shown in Figure 3. This can be seen as a trade-off between efficiency, cost, and control complexity. If the switches were implemented using diodes, the forward voltage of the diodes would compromise the overall efficiency. However, with using diodes, the converter has spontaneous split-phase control [28]. The diodes remain reverse-biased until the voltage mismatches between the capacitors are gone. Therefore, no current spikes are present. Alternately, if the switches are implemented using active switches, the efficiency can be significantly improved, but complex control is needed. That is, the switches must be delayed to prevent temporary

KVL violations that cause current spikes. In addition to the control, the circuit requires a large number of gate-driving circuits with level shifting and isolation components to drive the floating switches. In this paper, the proposed converter is implemented using only diodes. Figure 4 shows the use of the cell in different power circuits. The cell can be used in a voltage-fed DC-DC converter [29] or current-fed DC-DC converter [30], as shown in Figure 4(a,b), respectively. Also, it can be used in AC rectification circuits as in a typical 60 Hz AC source, in both isolated and non-isolated topologies as shown in Figure 4(c,d), or a high-frequency AC system (e.g., the 20 kHz Space Station power distribution system proposed by NASA) [31]. In this paper, the cell is used with an interleaved boost stage, as shown in Figure 4(e,f), to convert low-voltage DC sources to higher DC voltages.

3. THE PROPOSED TOPOLOGY INTRODUCTION AND THEORY OF OPERATION

The proposed converter consists of an interleaved boost stage and a bi-fold Dickson multiplier cell stage. The interleaved stage consists of two inductors connected to the input source and switched by two low-side active switches. The function of the interleaved boost stage is to store energy and release it to the bi-fold Dickson VMC capacitors. Figures 5(a), (b), and (d) show the interleaved boost converter with a different number of bi-fold Dickson VMCs. Note that the proposed converter with $N = 2$, shown in Figure 5(b), is similar to the interleaved boost converter with the Greinacher VMC that was proposed in [32], shown in Figure 5(c). The only difference is that the Greinacher cell is not extensible. Each stage contains two diodes and two capacitors, as shown in Figure 5(d). The proposed converter has three modes of operations: mode 1, where both switches are ON; mode 2, where switch 1 is ON and switch 2 is OFF; and mode 3, where switch 1 is OFF and switch 2 is ON. The switching patterns can be seen in Figure 6. There is a 180° phase shift between the active switches' gate signals. This topology, unlike [25], can work with both active switches open and without violating voltage second balance across input inductors. However, opening both

active switches creates several drawbacks to the interleaved topology, such as a reduction in the voltage gain and an imbalance between capacitor voltage. Therefore, it is not beneficial to use this topology for a duty cycle less than 50%. To conduct the analysis, a few assumptions are considered: 1) All components of the proposed converter are ideal; 2) The capacitors are large enough that the voltage ripples can be neglected; 3) The converter operates in the steady state; 4) The duty cycles are symmetrical and greater than 50%, and the converter is fed by a single voltage source. Nonetheless, the voltage gain ratio of the proposed converter will be summarized for cases where the duty cycles are asymmetrical and for cases where the converter is fed by two independent voltage sources.

4. MODE ANALYSIS AND STEADY STATE VOLTAGE GAIN

4.1. MODE 1 ($T_0 - T_1$) AND ($T_2 - T_3$) : BOTH Q_1 AND Q_2 ARE ON

In this mode, both active switches are conducting and allowing the source to transfer energy to both inductors. All diodes are reverse-biased, and they are OFF. The equivalent circuit of this mode is shown in Figure 7(a). The last-stage capacitors, C_{3A} and C_{3B} keep the energy level to the output load. The state equations of this mode are given by

$$L_1 \frac{di_{L_1}}{dt} = v_{L_1} = V_{in} \tag{1}$$

$$L_2 \frac{di_{L_2}}{dt} = v_{L_2} = V_{in} \tag{2}$$

4.2. MODE 2 ($T_1 - T_2$): Q_1 IS ON AND Q_2 IS OFF

In this mode, Q_1 is still ON, and L_1 keeps drawing energy from the source. Alternately, Q_2 is turned OFF, and the energy in L_2 is released to the VMC stage. Diodes D_{1_B}, D_{2_A}, and D_{3_B} are forward-biased and ON, while diodes D_{1_A},D_{2_B}, and D_{3_A} are reverse-biased

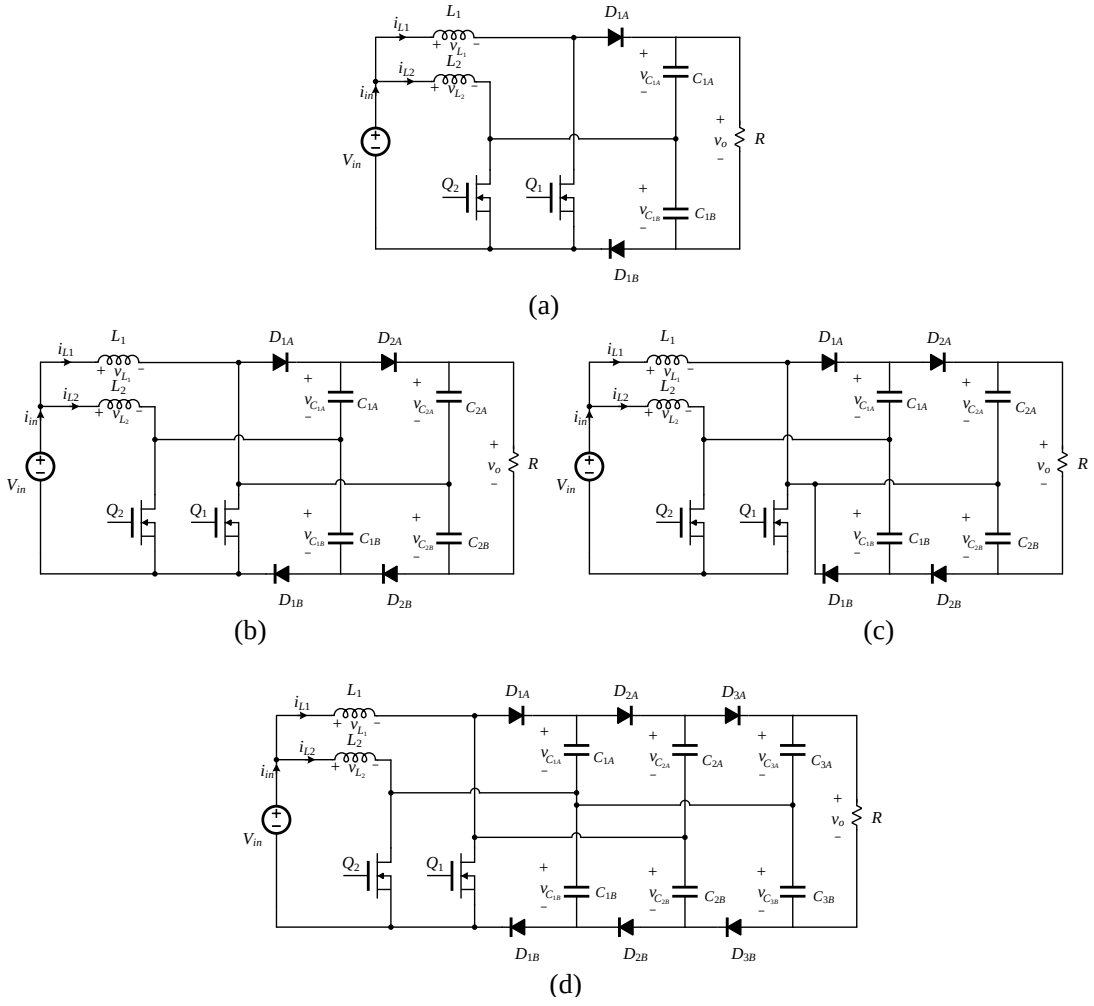

Figure 5. Interleaved boost converter with Dickson voltage multiplier a) $N = 1$ and $\frac{V_o}{V_{in}} = \frac{2}{1-d}$ b) $N = 2$ and $\frac{V_o}{V_{in}} = \frac{4}{1-d}$ c) Interleaved boost converter with a Greinacher VMC, which has the same gain as (b). d) The proposed converter with $N = 3$ and a gain of $\frac{V_o}{V_{in}} = \frac{6}{1-d}$. The analysis, simualtion, and experiment are based on this topology.

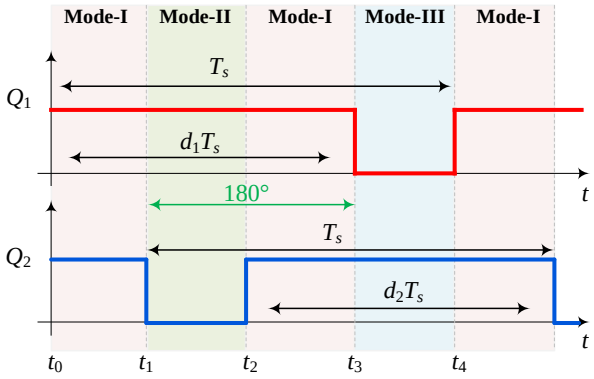

Figure 6. Switching pattern of two-phase boost converter. The phase shift between the active switches' duty cycles yields three modes of operation.

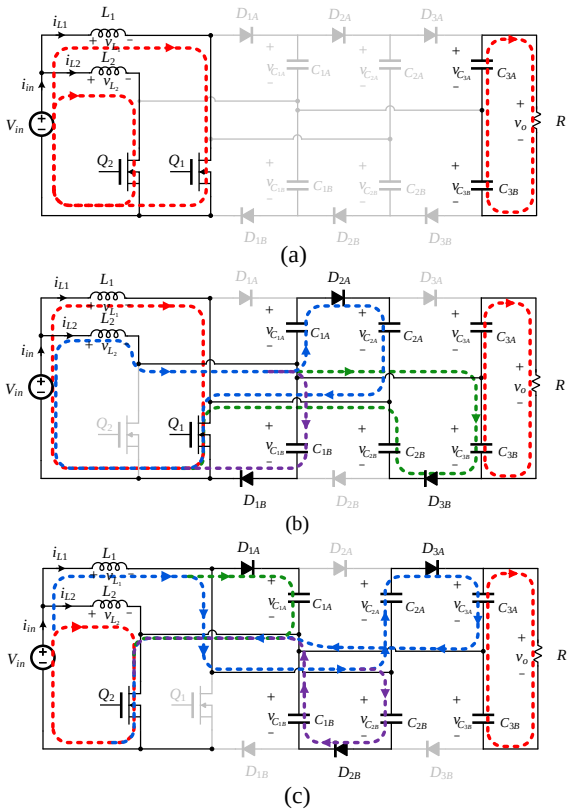

Figure 7. Modes of operation: (a) Mode 1, both Q_1 and Q_2 are ON; (b) Mode 2: Q_1 is ON and Q_2 is OFF; (c) Mode 3: Q_1 is OFF and Q_2 is ON;

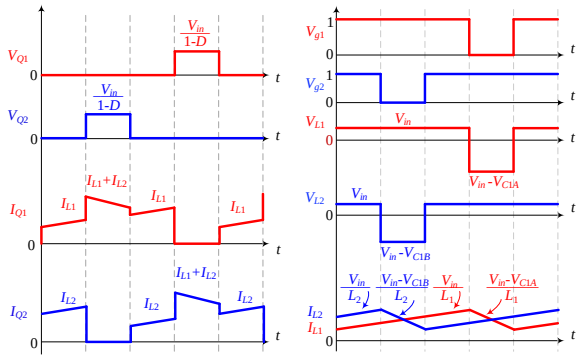

Figure 8. Interleaved boost stage waveforms. Voltage and currents of the active switches (left) and voltage and currents of the inductors (right)

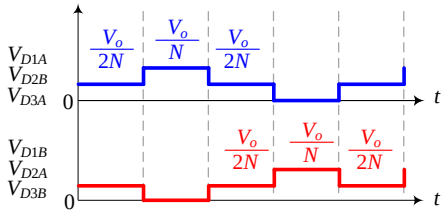

Figure 9. Voltage stress on the diodes

and do not conduct. Inductor L_1 is still being charged by the input voltage. Inductor L_2 and the input voltage charge capacitors C_{1_B}, C_{2_A}, and C_{3_B}. The equivalent circuit of this mode is shown in Figure 7(b), and the inductor voltages and capacitor currents are governed by

$$L_1 \frac{di_{L_1}}{dt} = v_{L_1} = V_{in} \tag{3}$$

$$L_2 \frac{di_{L_2}}{dt} = v_{L_2} = V_{in} - V_{c_{1B}} = V_{in} + V_{c_{2B}} - V_{c_{3B}} = V_{in} + V_{c_{1A}} - V_{c_{2A}} \tag{4}$$

4.3. MODE 3 ($T_3 - T_4$) : Q_1 IS OFF AND Q_2 IS ON

After mode 2, the converter operates in mode 1, and then it switches to mode 3. Mode 3 is the opposite of mode 2. In this mode, switch Q_1 is turned OFF, and switch Q_2 is still ON. The equivalent circuit is shown in Figure 7(c). Diodes D_{1_A},D_{2_B}, and D_{3_A}

are forward-biased. Diodes D_{1_B}, D_{2_A}, and D_{3_B} are reverse-biased, and they are OFF. The inductor L_1 transfers its energy to the VMC stage, while L_2 starts drawing power from the source. The state equations are given by

$$L_1 \frac{di_{L_1}}{dt} = v_{L_1} = V_{in} - V_{c_{1A}} = V_{in} + V_{c_{2A}} - V_{c_{3A}} = V_{in} + V_{c_{1B}} - V_{c_{2B}} \tag{5}$$

To find the voltage transfer function, one can apply the voltage second balance to the inductor voltages. So, the average value of the voltage across the inductors L_1 and L_2 are given by

$$\langle v_{L_1} \rangle = \int_0^{dT} V_{in} dt + \int_{dT}^{T} (V_{in} - V_{C_{1_A}}) dt = 0 \tag{6}$$

$$\langle v_{L_2} \rangle = \int_0^{dT} V_{in} dt + \int_{dT}^{T} (V_{in} - V_{C_{1_B}}) dt = 0 \tag{7}$$

From previous equations, the capacitor voltage can be obtained. The first-stage capacitor voltage is given by

$$V_{C_{1_A}} = V_{C_{1_B}} = \frac{V_{in}}{1-d} \tag{8}$$

The relationship between the second-stage capacitor voltage and the first-stage capacitor voltage can be given by

$$V_{C_{2A}} = V_{C_{2B}} = V_{c_{1A}} + V_{c_{1B}} = \frac{2V_{in}}{1-d} \tag{9}$$

The third-stage capacitor voltage is given by

$$V_{c_{3A}} = V_{c_{3B}} = V_{c_{2A}} + V_{c_{2B}} - V_{c_{1B}} = \frac{3V_{in}}{1-d} \tag{10}$$

The output voltage is the sum of the voltages across the last-stage capacitors. Therefore, the voltage gain ratio for the proposed converter with a three-stage VMC is given by

$$\frac{V_o}{V_{in}} = \frac{6}{1-d} \tag{11}$$

One can generalize the equations for the N^{th} stage converter. The capacitor voltages in each stage are given by

$$V_{c_{NA}} = V_{c_{NB}} = \frac{NV_{in}}{1-d} \tag{12}$$

The output voltage for the N^{th} stage converter is given by

$$V_o = V_{c_{NA}} + V_{c_{NB}} = \frac{2NV_{in}}{1-d} \tag{13}$$

Therefore, the voltage gain ratio is given by

$$\frac{V_o}{V_{in}} = \frac{2N}{1-d} \tag{14}$$

Equation 14 is an ideal gain at $d_1 = d_2$ and a single input V_{in}. However, the converter can work with asymmetrical duty cycle ratios and also with two independent power sources. Table 1 summarizes the output voltage gain at different duties as well as with two different independent input voltage sources.

Table 1. Output voltage at different cases

Case	the output voltage
$d_1 \neq d_2$ and $V_{in_1} \neq V_{in_2}$	$N(\frac{V_{in_1}}{1-d_1} + \frac{V_{in_2}}{1-d_2})$
$d_1 \neq d_2$ and $V_{in_1} = V_{in_2}$	$NV_{in}(\frac{1}{1-d_1} + \frac{1}{1-d_2})$
$d_1 = d_2$ and $V_{in_1} \neq V_{in_2}$	$\frac{N}{1-d}(V_{in_1} + V_{in_2})$
$d_1 = d_2$ and $V_{in_1} = V_{in_2}$	$\frac{2NV_{in}}{1-d}$

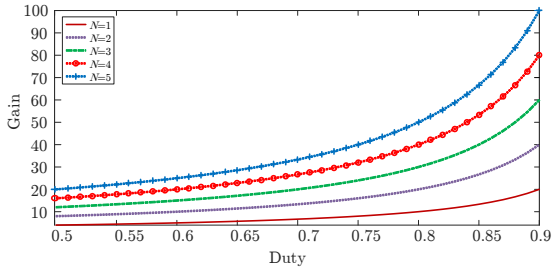

Figure 10. Voltage gain vs. the duty cycle at different numbers of VMC stages.

Increasing the number of VMC stages increases the voltage-gain ratio, as shown in Figure 10. However, practical voltage gain might be reduced due to the nonidealities. The proposed converter can be compared to various interleaved topologies, such as the interleaved boost converter with a Dickson voltage multiplier that was proposed in [26]. The circuit in [26] suffers from high voltage stress on its capacitors as the number of stages increases, and that might be challenging in high power applications. The modified Dickson voltage multiplier that was proposed in [25] is an improved version of the converter in [26]. The circuit connects the output ground to the first stage of the Dickson VMC, and therefore some of the internal capacitors have reduced voltage stress. However, the output capacitor still has high voltage stress. Another drawback of the aforementioned converters is that there is an uneven current share between the inductors when the converter has an even number of VMC stages. Table 2 shows a comparison summary of the proposed converter with the converters presented in [26] and [25]. The proposed converter has the lowest maximum stress and the highest voltage-gain ratio. The active switch voltage stress is also the lowest. The voltage stress across diodes is equal to the converter proposed in [25]. Both the converter presented in [25] and the proposed converter have a floating output feature, which requires a differential voltage sensor for voltage feedback. Nevertheless, the grounded output load is not necessary to interface the PV panels, where the control circuit goal is to extract the maximum power.

Table 2. Comparison between Different Topologies

Topology	Interleaved with the conventional Dickson [26]	Interleaved with the modified Dickson [25]	Proposed Converter
Static Gain	$\frac{N+1}{1-D}$	$\frac{N+1}{1-D}$	$\frac{2N}{1-D}$
Maximum stress on Switches	$\frac{V_o}{N}$	$\frac{V_o}{2}$	$\frac{V_o}{2N}$
Maximum stress on Diodes	$\frac{2V_o}{N+1}$	$\frac{V_o}{N}$	$\frac{V_o}{N}$
Maximum stress on Capacitors	V_o	V_o	$\frac{V_o}{2}$
Equal inductors current sharing	Only with odd number of stages	Only with odd number of stages	Equal regardless of number of stages
Output connection	grounded	floating	floating

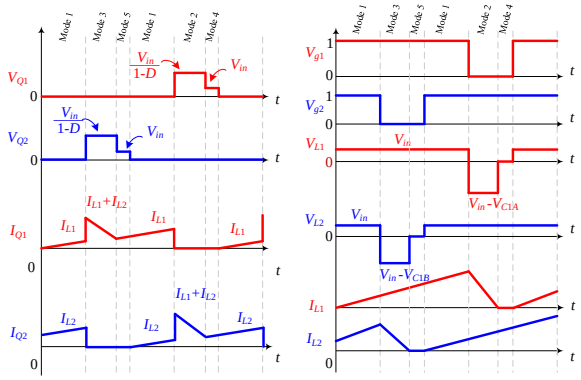

Figure 11. Waveforms of the DCM mode of operation

5. DISCONTINOUS CONDUCTION MODE AND BOUNDARY CONDUCTION MODE

5.1. DCM OPERATION

In DCM mode, the converter has five modes of operation. Three of these modes are similar to the one for a converter operating in CCM mode. The other two are mode 4 and mode 5. Mode 4 occurs after mode 2, where I_{L_1} is zero, and mode 5 occurs after mode 3, where I_{L_2} is zero. The sequence of the modes is mode 1, mode 2, mode 4, mode 1, mode 3, mode 5, and then it repeats. The waveforms of the interleaved boost stage operating in DCM mode are shown in Figure 11

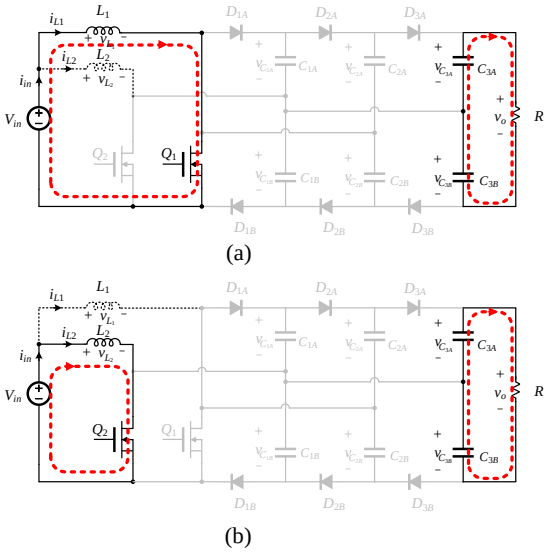

Figure 12. DCM modes: a) mode 4, when i_{L_2} hits the zero b) mode 5, when i_{L_1} hits the zero

5.1.1. Mode 1. same as mode 1 in CCM

5.1.2. Mode 2. same as mode 2 in CCM

5.1.3. Mode 3. same as mode 3 in CCM.

5.1.4. Mode 4. During this mode, Q_1 is OFF and Q_2 is ON. The inductor L_2 is still being charged from the input source. The inductor L_1 discharged all of its stored energy to the VMC stages, and the current is zero. The zero current is not enough to force the diodes to become forward-biased. Therefore all diodes are reversed-biased. The equivalent circuit of this mode is shown in Figure 12(a).

5.1.5. Mode 5. In this mode, Q_1 is ON and Q_2 is OFF. The input source is charging L_1. The L_2 discharged its energy to the VMC stage, and the I_{L_2} is zero. All diodes are reversed=biased, and the output is fed by the last stage capacitors. The equivalent circuit of this mode is shown in Figure 12(b).

5.1.6. Steady-state Analysis. . The voltage gain and voltage across capacitors can be obtained by applying the voltage second balance across the inductors. The voltage of the first capacitors is calculated by

$$V_{1a} = V_{1b} = \frac{1}{2}\left(1 + \sqrt{1 + \frac{d^2}{9\tau}}\right) \times V_{in} \tag{15}$$

where $\tau = \frac{L \times f_s}{R}$ The output of the second and third stage output capacitors are given by

$$V_{C_{2a}} = V_{C_{2b}} = \left(1 + \sqrt{1 + \frac{d^2}{9\tau}}\right) \times V_{in} \tag{16}$$

$$V_{C_{3a}} = V_{C_{3b}} = \frac{3}{2}\left(1 + \sqrt{1 + \frac{d^2}{9\tau}}\right) \times V_{in} \tag{17}$$

The output voltage equals the sum of the voltage across the last stage's capacitors, which can be calculated by

$$V_o = 3\left(1 + \sqrt{1 + \frac{d^2}{9\tau}}\right) \times V_{in} \tag{18}$$

Previous equations can be generalized for a converter with N number of stages. The n^{th} stage capacitor voltage is given by

$$V_{C_{na}} = V_{C_{nb}} = \frac{n}{2}\left(1 + \sqrt{1 + \frac{4d^2}{\tau \times (2N)^2}}\right) \times V_{in} \tag{19}$$

where n is a positive integer. The voltage gain is given by

$$V_o = N\left(1 + \sqrt{1 + \frac{4d^2}{\tau \times (2N)^2}}\right) \times V_{in} \tag{20}$$

Figure 13 shows the voltage gain of the proposed converter in the DCM mode at $\tau = 1.25 \times 10^{-3}$. The voltage gain in DCM is higher than in CCM. However, that comes at the cost of increasing the current ripples across the components.

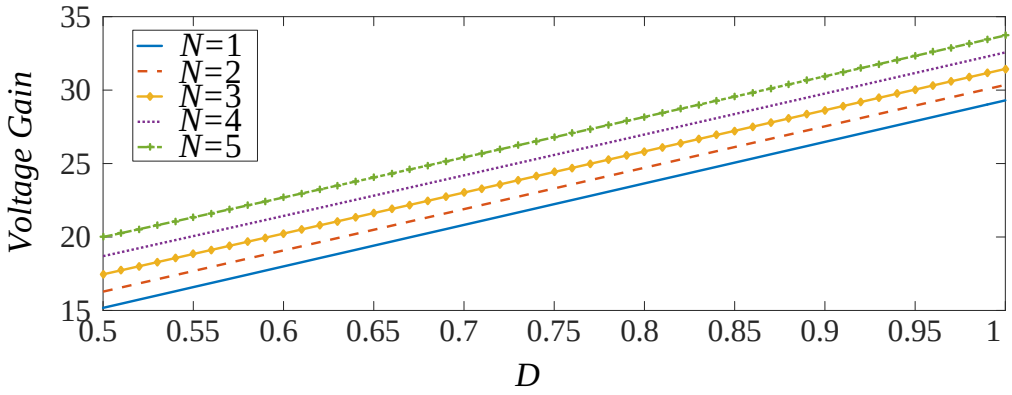

Figure 13. The gain of the converter at $\tau = 1.25 \times 10^{-3}$

5.2. BOUNDARY CONDUCTION MODE (BCM)

The converter is operating in BCM if the average value of the inductor current is equal to the inductor current ripple. In BCM, one can obtain the τ_{BCM} by equating the voltage gain of the CCM to the voltage gain of the DCM, as follows

$$\frac{2N}{1-d} = N\left(1 + \sqrt{1 + \frac{4d^2}{\tau \times (2N)^2}}\right) \tag{21}$$

The time constant of the inductor is calculated by

$$\tau_{BCM} = \frac{d(1-d)^2}{4N^2} \tag{22}$$

The time constant is plotted versus the duty cycle at different numbers of VMC stages, as shown in Figure 14. CCM mode occurs when τ is more than τ_{BCM}.

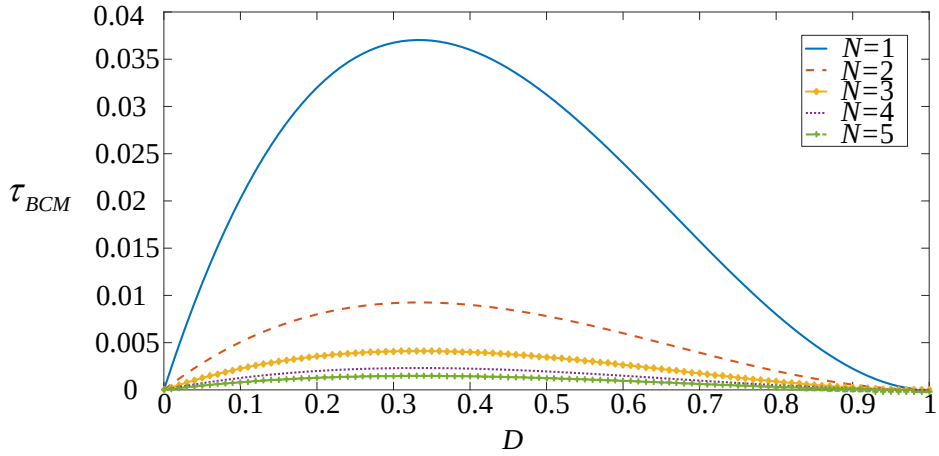

Figure 14. The boundary between CCM and DCM τ_{BCM} at different numbers of bi-fold VMC cells.

6. COMPONENTS SELECTION AND EFFICIENCY CALCULATIONS

6.1. INDUCTOR SELECTION

The average value of inductor currents is dependent on the load current and the number of VMC stages. The average value of the input current can be found with the following equation:

$$I_{in} = \frac{2NI_o}{1-d} \tag{23}$$

The input current is equally shared between inductors and can be calculated by

$$I_{L_1,avg} = I_{L_2,avg} = \frac{I_{in}}{2} = \frac{NI_o}{1-d} \tag{24}$$

The critical inductance that is required to ensure the converter operates in CCM mode is calculated by

$$L_{1,crit} = L_{2,crit} = \frac{V_{in}d(1-d)}{2NI_o f_s} \tag{25}$$

Inductors are normally designed based on the desired value of the inductor current ripple. The equations for L_1 and L_2 selection are

$$L_1 = \frac{V_{in}d}{\Delta i_{L_1} f_s} \tag{26}$$

$$L_2 = \frac{V_{in}d}{\Delta i_{L_2} f_s} \tag{27}$$

The peak value of the inductor current is obtained by

$$I_{L_1,pk} = \frac{NI_o}{1-d} + \frac{V_{in}d}{2L_1 f_s} \tag{28}$$

$$I_{L_2,pk} = \frac{NI_o}{1-d} + \frac{V_{in}d}{2L_2 f_s} \tag{29}$$

The RMS current of the inductors is given by

$$I_{L_1,RMS} = \sqrt{\left(\frac{NI_o}{1-d}\right)^2 + \left(\frac{V_{in}d}{2\sqrt{3}L_1 f_s}\right)^2} \tag{30}$$

$$I_{L_2,RMS} = \sqrt{\left(\frac{NI_o}{1-d}\right)^2 + \left(\frac{V_{in}d}{2\sqrt{3}L_2 f_s}\right)^2} \tag{31}$$

6.2. ACTIVE SWITCH SELECTION

The active switches are implemented using MOSFETs due to their ability to operate at high switching frequencies. To select MOSFETs for this topology, the maximum stresses on the switches need to be calculated. The voltage stress on the MOSFETs depends on the number of stages. The stresses on the active switches are given by

$$V_{Q_1} = V_{Q_2} = \frac{V_o}{2N} = \frac{V_{in}}{1-d} \tag{32}$$

The maximum current that passes through the switches is given by

$$I_{S,pk} = \frac{2NI_o}{1-D} + \frac{V_{in}d}{2Lf_s} \tag{33}$$

The average currents passing through the active switches are given by

$$I_{Q_{1,pk}} = I_{Q_{2,pk}} = \frac{2NI_o}{1-d} + \frac{V_{in}d}{2Lf_s} \tag{34}$$

$$I_{Q_{1,avg}} = I_{Q_{2,avg}} = \frac{NI_o}{1-d} \tag{35}$$

The RMS value is approximated by the following equation:

$$I_{Q_{1,rms}} = I_{Q_{2,rms}} = \frac{NI_o d}{\sqrt{(1-d)^3}} \tag{36}$$

6.3. DIODE SELECTION

One of the advantages of this topology is that the voltage stresses across the diode also depend on the number of stages. The more stages, the less voltage stress on the diodes. The maximum voltage that the diodes have to block is calculated by

$$V_{D_{N_{max}}} = \frac{V_o}{N} \tag{37}$$

The total average currents of the diode are given by

$$I_{D_{N_A}} = I_{D_{N_B}} = \frac{V_o}{R} \tag{38}$$

The RMS current is given by

$$I_{D_{N_A},rms} = I_{D_{N_B},rms} = \frac{V_o}{R}\sqrt{\frac{1}{1-d}} \tag{39}$$

6.4. CAPACITORS SELECTION

The capacitors selection is determined by the maximum current and voltage rating. The maximum voltage stress across the capacitors is already calculated in. Equally important, the maximum allowed voltage ripple and frequency determine the minimum required capacitance. Both capacitors in each VMC stage have to be equal to ensure equal current sharing operation [33]. The output capacitor selection depends on the allowed voltage ripples. Both output capacitors have to be equal, and they are selected based on the following equation:

$$C = \frac{I_o(1-D)T_s}{\Delta V_{C_1}} \tag{40}$$

The RMS current of the capacitors can be given by

$$I_{C_{3A,rms}} = I_{C_{3B,rms}} = I_o\sqrt{\frac{d}{1-d}} \tag{41}$$

$$I_{C_{1A,rms}} = I_{C_{1B,rms}} = I_o\left(1+\sqrt{\frac{d}{1-d}}\right) \tag{42}$$

$$I_{C_{2A,rms}} = I_{C_{2B,rms}} = I_o\left(1+\sqrt{\frac{d}{1-d}}\right) \tag{43}$$

6.5. EFFICIENCY ANALYSIS

The conduction loss in the DC resistance of the inductor (R_L) is given by

$$P_L = \sum_{i=1}^{\phi} I_{L_{i,rms}}^2 \times R_{L_i} \tag{44}$$

In cases of $\phi = 2$, $L_1 = L_2$, and $R_{L_1} = R_{L_2}$, the conduction power loss in the inductors can be given by

$$P_{L_tot} = 2R_L[\frac{N^2}{(1-d)^2}\frac{V_o^2}{R^2} + \frac{d^2V_{in}^2}{(2\sqrt{3}Lf_s)^2}] \tag{45}$$

The total switching loss in both MOSFETs is calculated by

$$P_{Q_{1_{SW}}} = P_{Q_{2_{SW}}} = \frac{f\ V_{in}}{2(1-d)^2}(NI_o(T_{on} + T_{off}) + C_{oss}V_{in}) \tag{46}$$

where C_{oss} is the output capacitance of the MOSFETs, and T_{on} and T_{off} are the turn on and turn off times [34]. The conduction loss in the MOSFET is given by

$$P_{Q_{1_{con}}} + P_{Q_{2_{con}}} = I_{Q_{1,rms}}R_{ON_1} + I_{Q_{2,rms}}R_{ON_2} \tag{47}$$

The conduction power loss of the diode can be calculated by

$$P_D = \sum_{i=1}^{N} I_{D_{avg}} \times V_F + \sum_{i=1}^{N} I_{D_{rms}} \times r_f \tag{48}$$

The power loss through a capacitor is given by

$$P_C = I_{C_{rms}}^2 ESR \tag{49}$$

The total power loss is given by

$$\begin{aligned} P_{Loss} \quad = \quad & P_{L_{tot}} + \sum_{i=1}^{\phi} P_{Q_{i,SW}} + \sum_{i=1}^{\phi} P_{Q_{i,cond}} \\ & + \sum_{n=1}^{2N} P_{D_n} + \sum_{n=1}^{2N} P_{C_n} \end{aligned} \tag{50}$$

The efficiency of the converter is given by

$$\eta\,(\%) = \frac{1}{1+\frac{P_{L_{tot}}+\sum_{i=1}^{\phi} P_{Q_{i,SW}}+\sum_{i=1}^{\phi} P_{Q_{i,cond}}+\sum_{n=1}^{2N} P_{D_n}+\sum_{n=1}^{2N} P_{C_n}}{V_{in}\times I_{in}}} \times 100 \tag{51}$$

More detailed information about the efficiency of the proposed converter is presented in Section 7.

7. SIMULATION

The proposed converter was simulated using the PLECS block set in the MATLAB/SIMULINK software, with the variable-step continuous solver (ode23), a maximum time step of 10^{-7} s, and a tolerance of 10^{-5}. The component parameters used in this simulation are listed in Table 2. To avoid singular loops and errors, small parasitic elements are included in the simulation. The voltage and current waveforms of the switches and the inductors are shown in Figure 15. The maximum stress on active switches Q_1 and Q_2 is 66.6 V, and the average and peak values of the switch currents are 5 A and 6.3 A, respectively. Similarly, the average current of each inductor is 5 A, and the RMS current is $\simeq$ 5.1 A. The inductor currents are interleaved, and that can increase the frequency of the input current ripple currents so that these ripples can be easily filtered out with smaller capacitors than the CBC. Figure 16 shows the diodes' voltage and current waveforms. The maximum voltage stress on the diodes is 133.3 V, the average current is 0.5 A, and the RMS current is 0.91 A. Figure 17 shows the waveforms of the voltage and the current of the capacitors. The voltage across each of the output capacitors is $\simeq$ 200 V, and the RMS current is 1.26 A. The second stage capacitors have 133 V, and the RMS current is 0.76 A. The first-stage capacitors have 57 V, and the RMS current is 0.76 A. The figure also shows the capacitors' voltage ripple cancellation at each stage.

Table 3. List of parameters used in the simulation

Parameter	Value
Input voltage	20 V
Output voltage	400 V
Load resistance	800 Ω
Ideal duty cycle	0.7
Switching frequency	100 kHz
Inductors	100 μH
Capacitors	10 μF

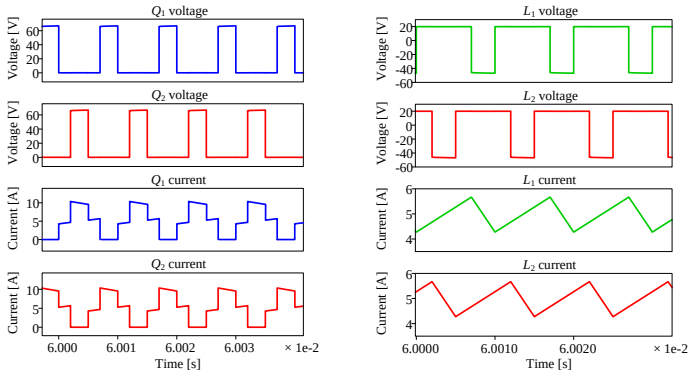

Figure 15. Voltages and currents of active switches (left) and inductors (right)

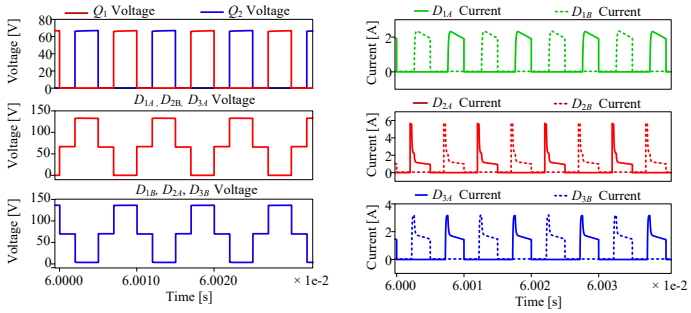

Figure 16. Voltage and current stress through diodes

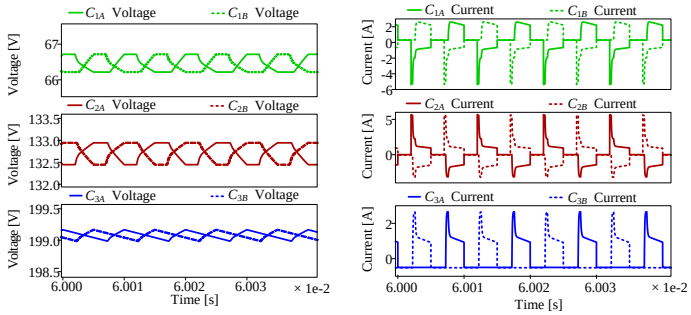

Figure 17. Voltage and current stress on capacitors. The voltage ripples are partially canceled.

Table 4. Component Listing for the Hardware Prototype

Item	Designation	Rating	Part No.
Inductor	L_1, L_2	100 μH, DCR = 25 $m\Omega$,	60B104C
Capacitor	C_{1A}, C_{2A} $C_{1B}C_{2B}$ C_{3A}, C_{3B}	10 μF	EXH2E106HRPT
MOSFET	Q_1, Q_2	150 V, 37 A $R_{ds(on)}$ = 10.525 $m\Omega$	IPA105N15N3
Diode	D_{1A}, D_{2A} D_{1B}, D_{2B}	250V, 40A V_F = 0.86 V, t_{rr} = 35 ns	MBR40250G
load	R_{load}	multiple values	L100J100E, L225J50RE L225J250E,L225J500E

8. EXPERIMENTAL IMPLEMENTATION AND RESULTS

A 200 W hardware prototype was implemented experimentally to verify the analysis and simulation presented in the previous sections. Figure 18 shows the annotated prototype board of the proposed converter. The converter was designed for a nominal converter ratio $\frac{400}{20}$ = 20 and a duty cycle of 0.7. The switching frequency was 50 kHz. The components used to implement the prototype are listed in Table 4. The active switches were implemented using MOSFETs IPA105N15N3 for their low on-resistance, low gate capacitance, and low switching power loss. Schottky diodes MBR40250G were selected to implement the blocking diodes of the VMC because of their fast recovery time as well as their relatively low forward voltage. Film capacitors were selected to implement the blocking and output capacitors, which have a low equivalent series resistance and a high voltage rating. The converter was fed by the N5766A DC power supply to power a 200 W load, which was implemented using a combination of ceramic resistors. Figure 18 shows the thermal image of the converter operating at 100 W, and it shows that the active switches are the only part that is heating up. Figure 19 shows the inductors and active switch currents at 80 W. Each inductor current has an average value of 2 A and a peak current of $\simeq$ 2.1 A. They are shifted 180°, and that doubles the input current ripple frequency as shown. Figure 20 shows the voltage stress across Q_1 and Q_2, as well as the diodes; the stresses across the active switches are 66 V, and the maximum voltage on the diodes is 133 V.

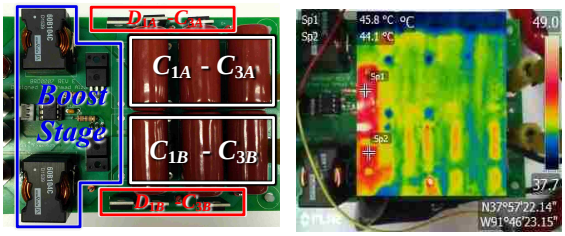

Figure 18. The hardware prototype of the proposed converter (left) and the thermal image of the proposed converter operating at 100 W (right)

The capacitor voltages, stage voltage, and voltage ripples are shown in Figure 21. The stage 1 capacitor voltage is 66.67 V each. The stage 2 capacitor voltage is 133.34 V each. The output stage capacitors have 200 V of stress each, and the output voltage is 400 V.

Figure 22 shows the breakdown of the component loss, excluding the inductor core loss. The breakdown percentage of the losses at 100 W is as follows: the first major loss source are the diodes with about 57% of the total loss; the second major loss source are the active switches. They are the culprit for 30.5% of the total loss due to the conduction and switching loss. The capacitors and inductors conduction losses account of 0.6% and 11.3%, respectively. The loss breakdown assumed the conduction patterns of the diodes are equal, which in practice can be slightly different. Therefore, the diodes' conduction loss is overestimated, and it is lower in experimentation. The overall efficiency is shown in Figure 24. The converter has a dimension of 3.98" $L \times$ 3.35" W, with a height of 1.38 in. The power density of the converter is roughly 21.7 W/in^3. The inductors and film capacitor take dominant real estate of the PCB. The power density could be more than 45 W/in^3 if multilayer ceramic capacitors were used instead of film capacitors, with, of course, a significant increase in the total cost.

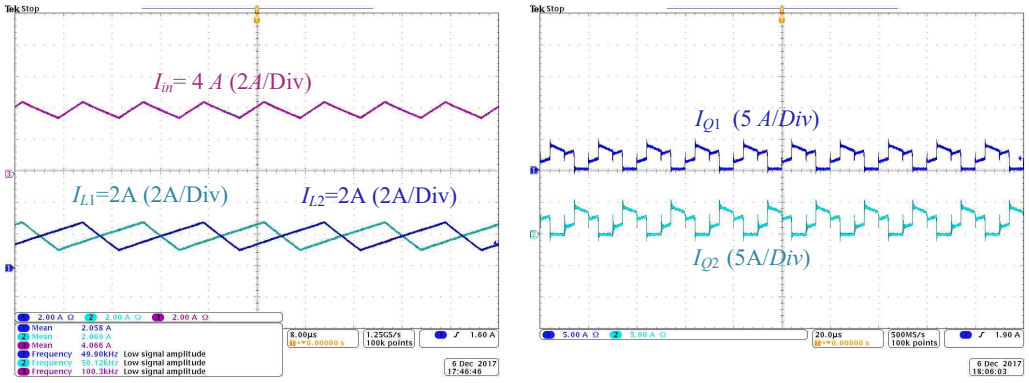

Figure 19. Inductor currents and smooth pre-filtered input current (left) and active switches currents (right)

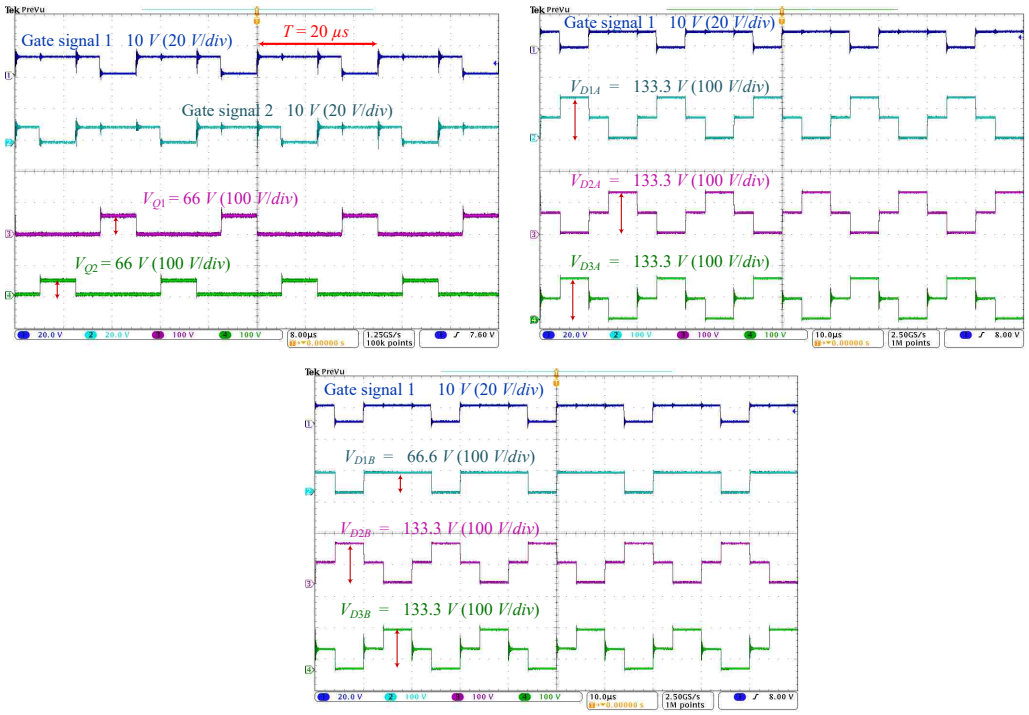

Figure 20. Voltage stress across active switches and diodes

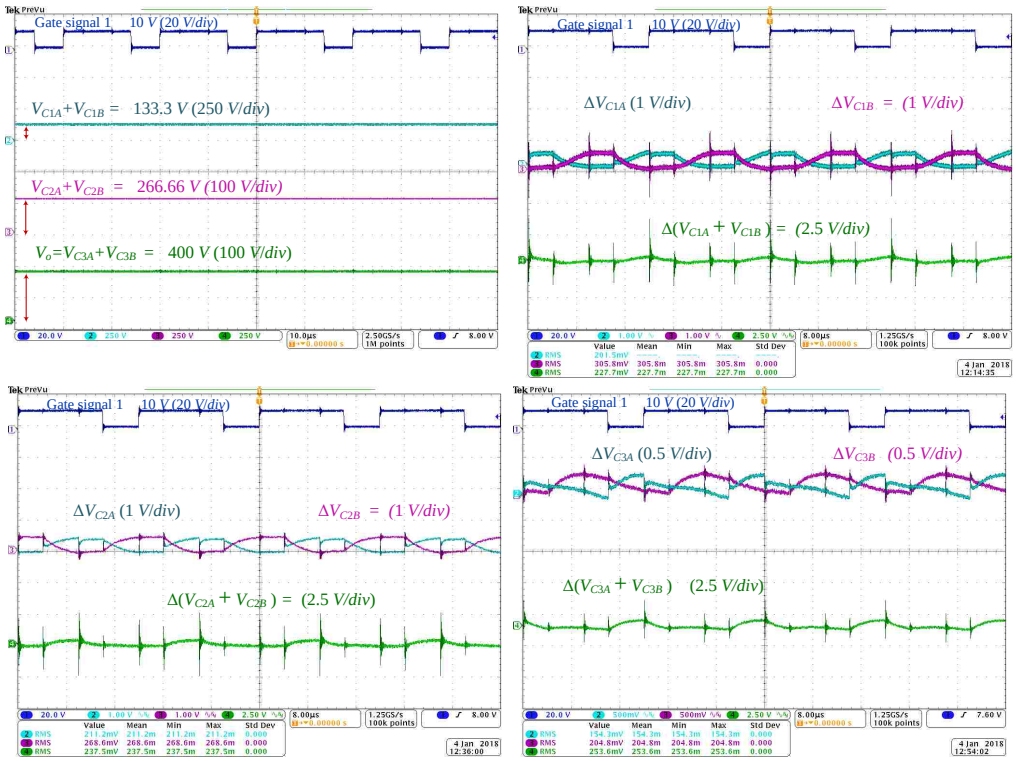

Figure 21. Capacitor voltages and AC voltage ripples

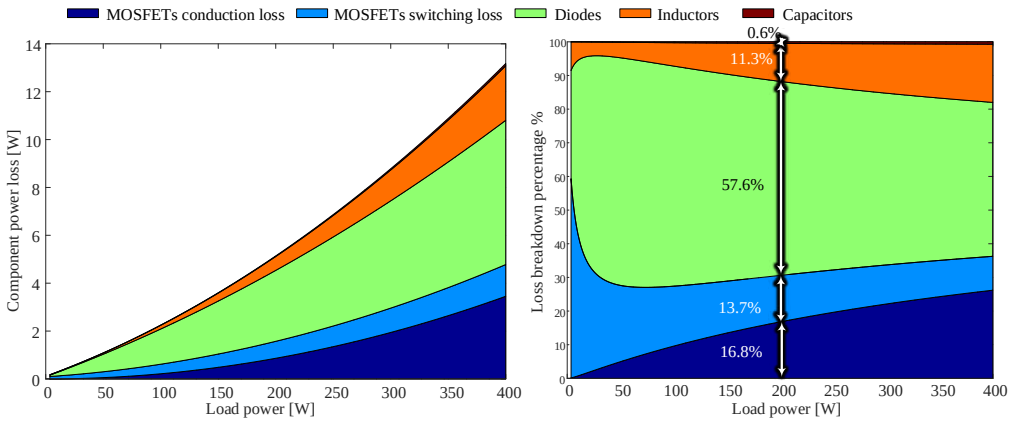

Figure 22. Loss (left) and loss distribution (right) of the converter as a function of the load.

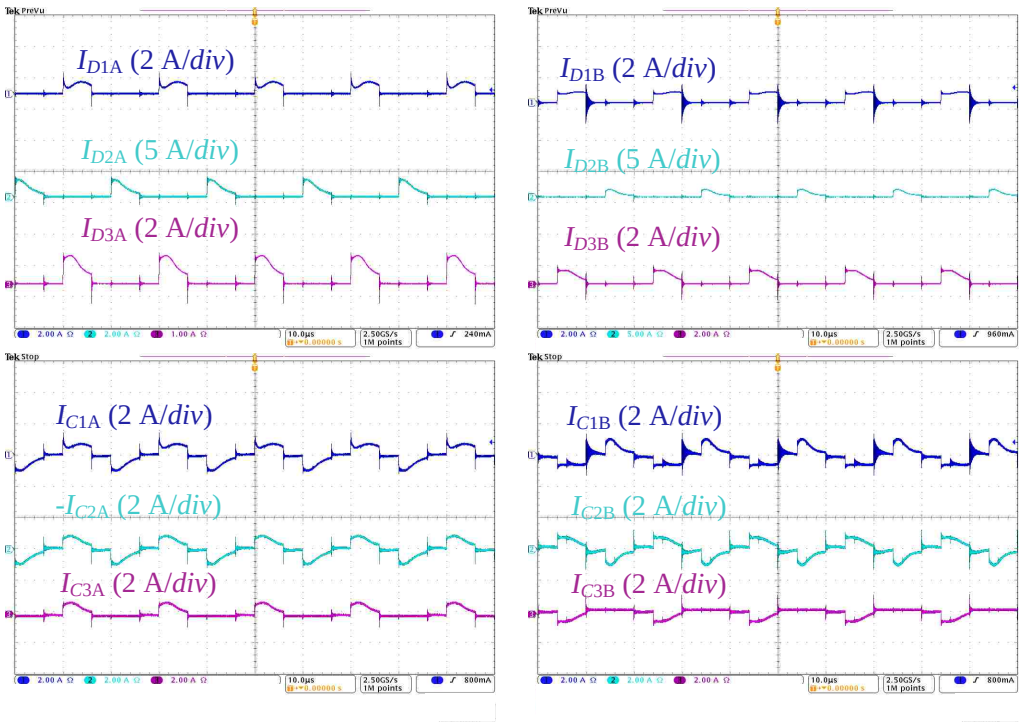

Figure 23. Diode currents (upper waveforms) and capacitor currents (lower waveforms)

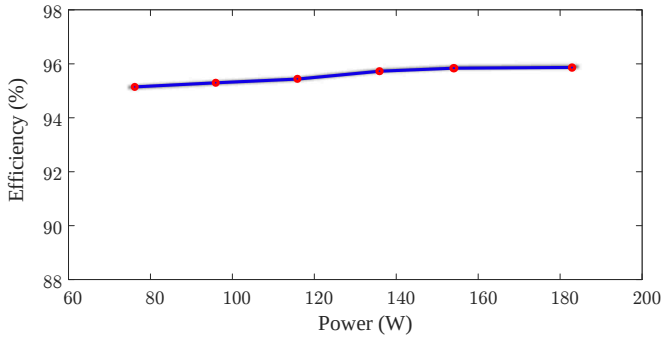

Figure 24. Efficiency of the converter at different loads

9. CONCLUSION

This paper has presented a high-voltage-gain DC-DC step-up converter to interface renewable energy sources to a higher voltage DC bus, such as a 20 V input source to a 400 V_{DC}. The converter employs a bi-fold Dickson VMC with an interleaved boost stage to obtain a high voltage gain. Several features make the converter desirable, such as low voltage stress across components, modularity, and the continuity of the input current. The converter balances the capacitor voltages and features equal current sharing among phases, which improves the conduction losses on both inductors and MOSFETs. Additionally, the proposed converter is capable of converting power from either a single or two independent PV panels. An analysis of the converter and the selection of the components are discussed in detail and supported by the simulation results. A 200-W hardware prototype was implemented to validate the analysis and the simulation.

REFERENCES

[1] "New hikari supercomputer starts solar hvdc," https://www.tacc.utexas.edu/-/new-hikari-supercomputer-starts-solar-hvdc, (Accessed on 02/12/2018).

[2] M. E. Baran and N. R. Mahajan, "Dc distribution for industrial systems: opportunities and challenges," *IEEE Transactions on Industry Applications*, vol. 39, no. 6, pp. 1596–1601, Nov 2003.

[3] J. G. Ciezki and R. W. Ashton, "Selection and stability issues associated with a navy shipboard dc zonal electric distribution system," *IEEE Transactions on Power Delivery*, vol. 15, no. 2, pp. 665–669, Apr 2000.

[4] A. Stupar, T. Friedli, J. Minibock, and J. W. Kolar, "Towards a 99% efficient three-phase buck-type pfc rectifier for 400-v dc distribution systems," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 1732–1744, April 2012.

[5] Y. Sato, Y. Tanaka, A. Fukui, M. Yamasaki, and H. Ohashi, "Sic-sit circuit breakers with controllable interruption voltage for 400-v dc distribution systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2597–2605, May 2014.

[6] P. T. Krein, "Data center challenges and their power electronics," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 1, pp. 39–46, 2017.

[7] M. Kasper, D. Bortis, T. Friedli, and J. W. Kolar, "Classification and comparative evaluation of pv panel integrated dc-dc converter concepts," in *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, Sept 2012, pp. LS1e.4–1–LS1e.4–8.

[8] F. L. Tofoli, D. d. C. Pereira, W. J. de Paula, and D. d. S. Oliveira Júnior, "Survey on non-isolated high-voltage step-up dc-dc topologies based on the boost converter," *IET Power Electronics*, vol. 8, no. 10, pp. 2044–2057, 2015.

[9] B. C. Barry, J. G. Hayes, and M. S. Ryłko, "Ccm and dcm operation of the interleaved two-phase boost converter with discrete and coupled inductors," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6551–6567, Dec 2015.

[10] R. N. A. L. e Silva Aquino, F. L. Tofoli, P. P. Praca, D. d. S. Oliveira, and L. H. S. C. Barreto, "Soft switching high-voltage gain dc-dc interleaved boost converter," *IET Power Electronics*, vol. 8, no. 1, pp. 120–129, 2015.

[11] L. Huber and M. M. Jovanovic, "A design approach for server power supplies for networking applications," in *APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.00CH37058)*, vol. 2, 2000, pp. 1163–1169 vol.2.

[12] Y. Gu, D. Zhang, X. Wu, and X. Zhang, "Research on stability improvement of the cascaded dc-dc converters based on ac signal sampling control method," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4547–4559, May 2018.

[13] M. T. Zhang, Y. Jiang, F. C. Lee, and M. M. Jovanovic, "Single-phase three-level boost power factor correction converter," in *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual*, no. 0, Mar 1995, pp. 434–439 vol.1.

[14] H. C. Chen and W. J. Lin, "Mppt and voltage balancing control with sensing only inductor current for photovoltaic-fed, three-level, boost-type converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 29–35, Jan 2014.

[15] Y. Zhang, J. T. Sun, and Y. F. Wang, "Hybrid boost three-level dc-dc converter with high voltage gain for photovoltaic generation systems," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3659–3664, Aug 2013.

[16] Q. M. Li and F. C. Lee, "Design consideration of the active-clamp forward converter with current mode control during large-signal transient," *IEEE Transactions on Power Electronics*, vol. 18, no. 4, pp. 958–965, July 2003.

[17] R. Ayyanar and N. Mohan, "Novel soft-switching dc-dc converter with full zvs-range and reduced filter requirement. i. regulated-output applications," *IEEE Transactions on Power Electronics*, vol. 16, no. 2, pp. 184–192, Mar 2001.

[18] K. C. Tseng and C. C. Huang, "High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 3, pp. 1311–1319, March 2014.

[19] A. Abramovitz, T. Cheng, and K. Smedley, "Analysis and design of forward converter with energy regenerative snubber," *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 667–676, March 2010.

[20] G. Spiazzi, P. Mattavelli, and A. Costabeber, "High step-up ratio flyback converter with active clamp and voltage multiplier," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3205–3214, Nov 2011.

[21] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc-dc pwm converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 2, pp. 687–696, March 2008.

[22] Y. J. A. Alcazar, D. de Souza Oliveira, F. L. Tofoli, and R. P. Torrico-Bascopé, "Dc-dc nonisolated boost converter based on the three-state switching cell and voltage multiplier cells," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 10, pp. 4438–4449, Oct 2013.

[23] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, "A dc-dc multilevel boost converter," *IET Power Electronics*, vol. 3, no. 1, pp. 129–137, January 2010.

[24] B. Wu, S. Li, Y. Liu, and K. M. Smedley, "A new hybrid boosting converter for renewable energy applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 2, pp. 1203–1215, Feb 2016.

[25] B. Baddipadiga and M. Ferdowsi, "A high-voltage-gain dc-dc converter based on modified Dickson charge pump voltage multiplier," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[26] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi, "A dc-dc converter with high voltage gain and two input boost stages," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4206–4215, June 2016.

[27] G. Palumbo and D. Pappalardo, "Charge pump circuits: An overview on design strategies and topologies," *IEEE Circuits and Systems Magazine*, vol. 10, no. 1, pp. 31–45, First 2010.

[28] Y. Lei, R. May, and R. Pilawa-Podgurski, "Split-phase control: Achieving complete soft-charging operation of a dickson switched-capacitor converter," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 770–782, Jan 2016.

[29] A. Alzahrani, P. Shamsi, and M. Ferdowsi, "Analysis and design of bipolar dickson dc-dc converter," in *2017 IEEE Power and Energy Conference at Illinois (PECI)*, Feb 2017, pp. 1–6.

[30] ——, "Boost converter with bipolar dickson voltage multiplier cells," in *2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA)*, Nov 2017, pp. 228–233.

[31] I. G. Hansen and G. R. Sundberg, "Space station 20 – khz power management and distribution system," in *1986 17th Annual IEEE Power Electronics Specialists Conference*, June 1986, pp. 676–683.

[32] A. Alzahrani, P. Shamsi, and M. Ferdowsi, "A novel interleaved non-isolated high-gain dc-dc boost converter with Greinacher voltage multiplier cells," in *2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA)*, Nov 2017, pp. 222–227.

[33] C. T. Pan, C. F. Chuang, and C. C. Chu, "A novel transformer-less adaptable voltage quadrupler dc converter with low switch voltage stress," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4787–4796, Sept 2014.

[34] Y. Xiong, S. Sun, H. Jia, P. Shea, and Z. J. Shen, "New physical insights on power mosfet switching losses," *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 525–531, Feb 2009.

III. A FAMILY OF HIGH-VOLTAGE-GAIN MULTILEVEL BOOST CONVERTERS

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ABSTRACT

This paper presents various topologies based on multilevel boost converters, with a focus on those derived from three-level boost converters (TLB). The TLB is a common dc-dc step-up topology and is widely used in various applications, such as power factor correction (PFC) and voltage regulation. Using such topology in applications that require high voltage gain is a challenge because of the insufficient voltage gain. The proposed family utilizes several different techniques to increase the voltage gain of the TLB. These techniques include using coupled inductors, switched inductor cells, or a flyback transformer. An example converter of TLB with a flyback transformer is fully illustrated with modes of operation, a steady-state analysis and component selection. The converter simulated to proof the theory and analysis , which is used to convert a 20 V to 200 V. The converter was also simulated to extract power from three PVL-136 photovoltaic (PV) panels using an MPPT algorithm. An 80 W hardware prototype was implemented in the lab to validate the simulation and the analysis.

Keywords: High-Gain, three-Level, dc-dc, boost, self-left, coupled inductor, flyback, MPPT, solar, PV

1. INTRODUCTION

Power electronics converters have an indispensable role in integrating renewable energy sources to the electric power grid. As more renewable energy sources are used, more efficient components and converters are desirable. Renewable energy sources, in general, suffer from low voltage output and high dependence on weather conditions. Photovoltaics energy also has one more issue, which is shading. Shading can reduce the output power of the solar panel and possibly even create hot spots, which might lead to damage in the solar cell itself. The stochastic nature of the PV output leads to a variable maximum power point and variable input voltage, which necessitates a maximum power point tracker (MPPT) [1–3]. Connecting several panels in series increases the overall voltage and power. However, voltage mismatches between cells leads to a reduction of efficiency and output power. Connecting solar panels in parallel increases the total current, but the voltage is still as that of a single cell [4–6].

In this case, a step up converter with a high-voltage-gain ratio is needed. The CBC can achieve high gain at high duty cycles, in theory. In reality, achieving high gain with the CBC is impracticable because of the conduction losses and the nonidealities [7, 8]. Also using the CBC to operate in the continuous conduction mode (CCM) requires bulky magnetics and high rating switching devices [9–11]. The voltage gain can be increased by cascading several CBCs. Each stage operates at a lower value duty ratio, and the overall voltage gain is high. However, cascading two or more CBCs means processing the power two times or more, which might reduce the performance of the converter and complicate the control design [12, 13]. Similarly, stacking several CBCs can share the power and reduce the current rating, but there is no improvement in the voltage gain. A hybrid flyback-boost converter utilizes the flyback transformer to increase the voltage gain of the CBC [13]. The voltage gain of the converter is a function of the transformer turns ratio. However, using a transformer would increase the weight and volume of the converter and decrease the power density. The TLB converter was introduced to reduce the voltage stress of the

semiconductors, and reduce the size of the magnetic elements by increasing the effective frequency. The drawback of the TLB converter is the low voltage gain, which is not sufficient for renewable energy sources that have low voltage. The conventional isolated converters such as flyback, forward and push-pull draw a discontinuous current from the input source, which make them not suitable for use in renewable energy applications [14, 15].

Flying capacitor voltage multiplying converters can achieve high gain with low voltage stress across the components and operate in the CCM with minimal inductance due to the high effective frequency. The effective frequency value is a multiple of the switching frequency, which is based on the number of stages [16–18]. However, the minimum duty cycle and the phase shift is a function of the stages. That is, the greater the FCML level, the higher the duty cycle that is required, and that limits the range of the operating duty cycle. The narrow range of the duty cycle can be a disadvantage in cases with MPPT control and load matching.

The voltage gain can be increased by using a transformer or a coupled inductor, either an isolated or integrated one [19–21]. Therefore, the voltage gain becomes a function of the turns ratio, and as gain requirement increased, so does the turns ratio requirement. However, the leakage inductance causes voltage spikes on the active switches and requires clamping circuits. Furthermore, employing magnetic elements with a higher turns ratio increases the weight of the converter and reduces the power density, especially at a low frequency. Recently, several papers introduce interleaved boost converters with switched-capacitor circuits [22, 23]. The switched-capacitor circuit has a high power density, and the interleaved part can minimize the magnetic storage requirement. However, using switched-capacitor requires very complicated driving circuitry, and complicated control to remove the mismatches between the capacitors.

This paper presents a family a high-voltage-gain step-up dc-dc converter based on multilevel boost converter to integrate solar panels with low output voltage, typically $12 - 45\ V_{dc}$, to a dc distribution bus in a dc microgrid ($200 - 960\ V_{dc}$). To implement a

converter with a high-gain conversion ratio, coupled-inductors and voltage multiplier cells were incorporated to increase the voltage gain of the converter. The proposed converter is better than paralleling or cascading boost converters in terms of efficiency and voltage stress across components. The main advantage is that the effective frequency is seen by the magnetic is higher than the switching frequency, which allow reduction in the magnetic size.

The rest of the paper is structured as follows: Section 2 presents different variations of converters belonging to the proposed family with an explanation of the technique used to enhance the voltage gain. In Section 3, an example of the proposed converter is given and analyzed. The component selections and efficiency analysis is presented in Section 4. In Section 5 and 6, simulation and experimental results of the example converter are provided, respectively. Finally, conclusions and future work are described in Section 7.

2. PROPOSED FAMILY OF MULTILEVEL BOOST CONVERTER WITH HIGH GAIN

2.1. INTERLEAVING

Although the interleaving techniques increase the frequency of the AC components of the input current, the frequency of the AC components of the inductor current is still the same as the switching frequency, which might not be a good trade-off for increasing the number of elements. Topologies, such as flying capacitor multilevel converters (FCMC) and multilevel converter families, tend to increase the effective frequency of the inductor voltage using vertical interleaving. That is, the effective frequency usually equals the switching frequency multiplied by the number of levels. Increasing the effective frequency that is seen by the inductors reduces the critical inductances that ensure the continuous flow of the inductor current and allow designers to select magnetic components with a smaller volume and build high power density converters. At high power, the advantage of vertical

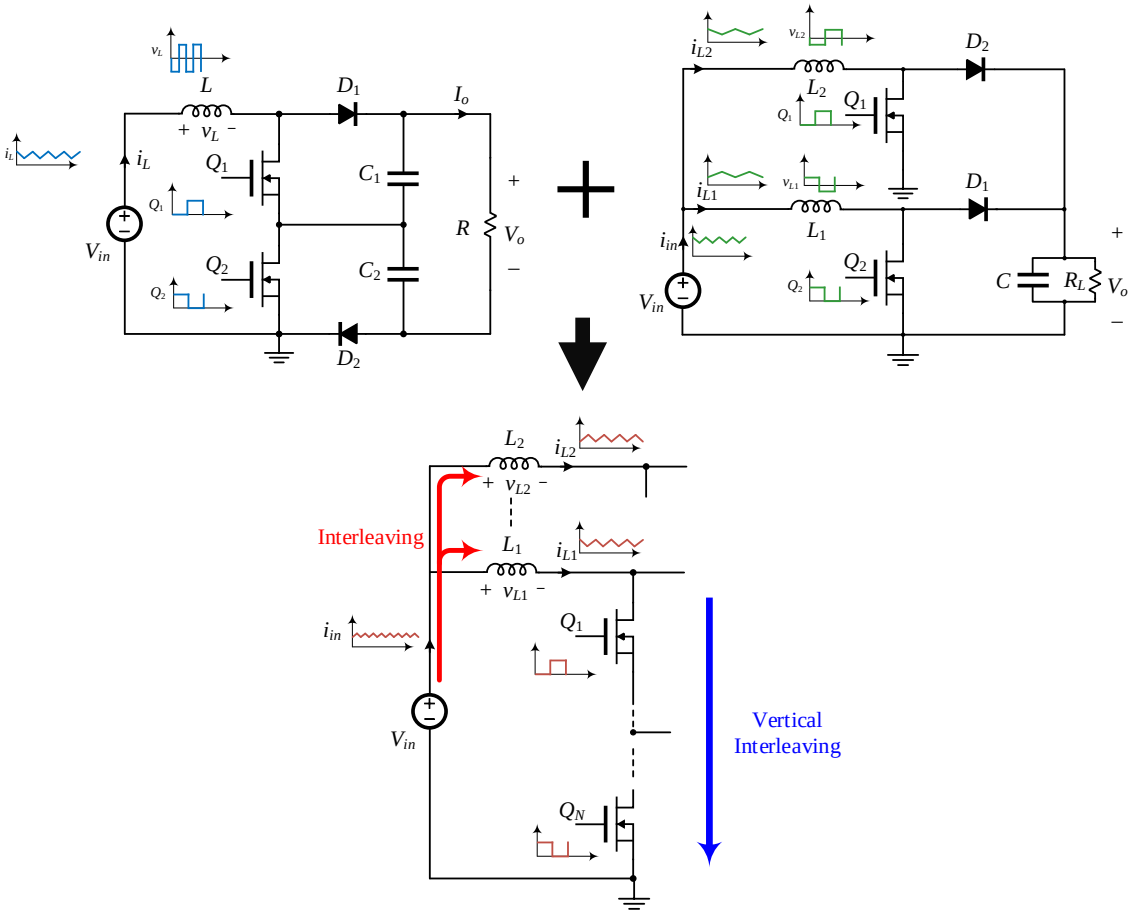

Figure 1. Interleaving types: a) is vertical interleaving using three or multilevel structures, b) interleaving by paralleling two converters and c) mixing both techniques to increase the effective frequency of the magnetic element and reduce the conduction power loss of the inductor

interleaving might not be useful because the magnetic element has to process is a huge amount of energy, and it is difficult to design a small and efficient magnetic element. If that is the case, one can combine both the vertical interleaving and the conventional interleaving to increase the performance of the converter, as shown in Figure 1. However, this paper only explores converters with vertical interleaving, specifically those based on the TLB converter.

2.2. HIGH GAIN CELLS

Figure 2 shows a family of multilevel boost converters. The number of levels does not improve the voltage gain; it only increases the effective frequency across the magnetic elements and reduces the voltage stress. The voltage gain from the TLB converter is not high enough for boosting low-voltage input sources 10 times or more. Therefore, several techniques can be used to improve the voltage gain. First one is to use the coupled inductors to increase the voltage. The voltage gain becomes a function of the turns ratio, and increasing the turns ratio would increase the voltage gain. Figure 3(a) shows the TLB converter with the coupled inductors, which is fully analyzed in [24]. The coupled inductors can be used with a four-level boost converter, as shown in 3(b). Another way to improve the voltage gain is to use a switched inductor cell [25–28] to replace the input inductor, such as in Figure 4 and 5. The inductors in the switched-inductor cells charge in parallel from the input source and discharge in series. The current rating of the inductors is reduced, and the overall voltage gain of the converter is improved. However, the main disadvantage of previous high gain techniques is that they use the diode in the high current loop, the loop that contains the input source and the active switches. Putting a diode in the high current loop can compromise the efficiency of the converter because of the high conduction loss of the diode. Also, a bigger heat dissipation element is required. The voltage gain can be increased without placing a diode in the high current loop. That is, a flyback transformer can be utilized to increase the voltage gain, as shown in Figure 6. The converter has lower voltage stress and a higher effective frequency across the magnetic element than the integrated flyback-CBC converter [29]. Table 1 shows a comparison between different types of converters.

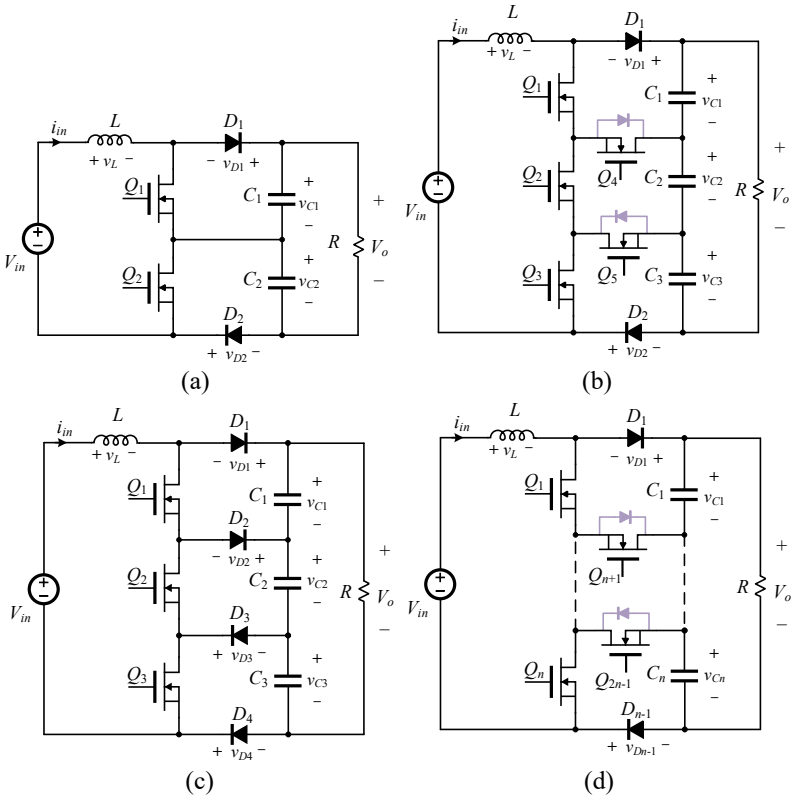

Figure 2. Multilevel boost converter topologies: (a) TLB (b) Four-level boost converter, (c) Floating interleaved TLB, (d) Interleaved TLB and (e) Interleaved four level boost converter.

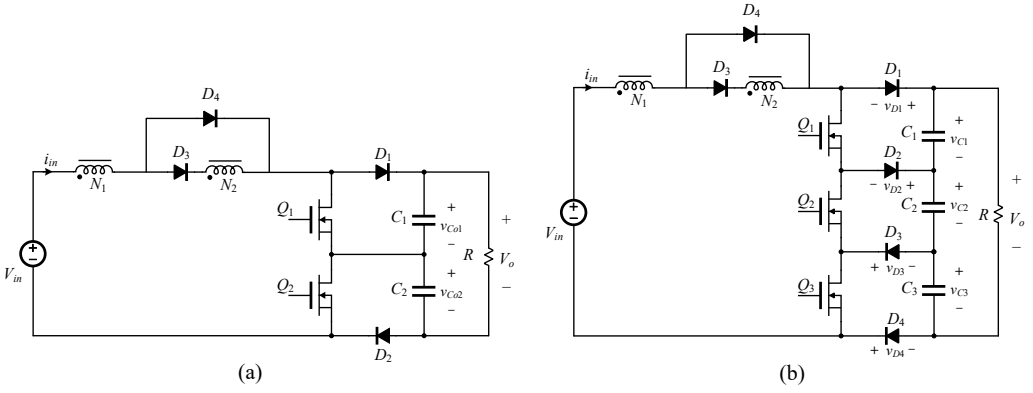

Figure 3. Multilevel boost converter topologies with high coupled inductors cell: (a) TLB with coupled inductors and (b) Four-level boost converter with coupled inductors

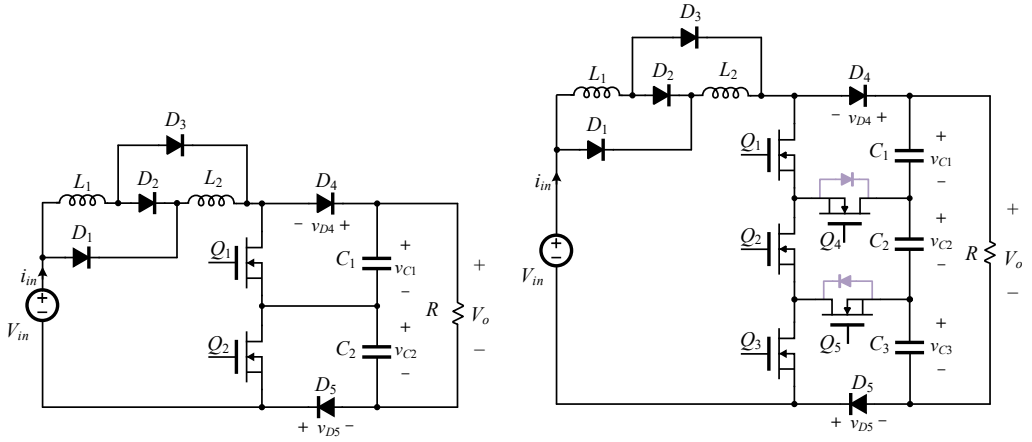

Figure 4. Multilevel boost converter topologies with high switched-inductor cell: (a) TLB with switched-inductor cell and (b) Four-level boost converter with switched-inductor cell

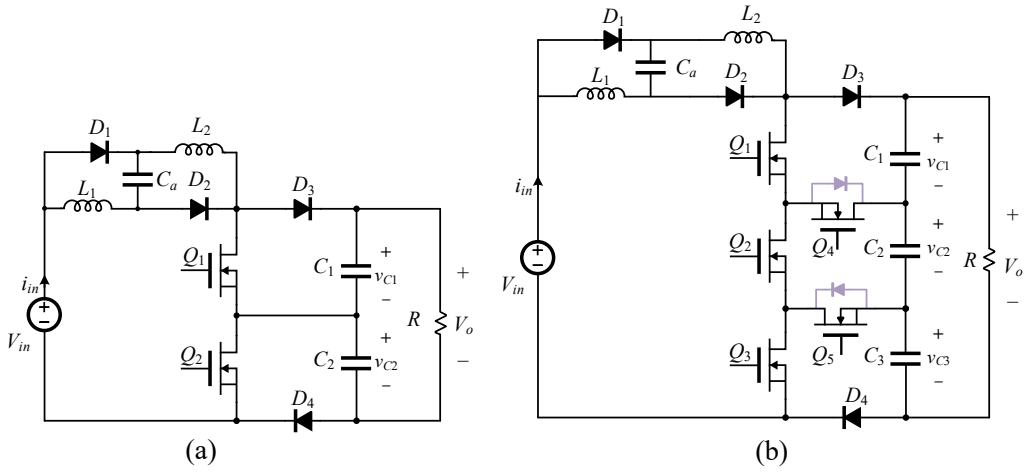

Figure 5. Multilevel boost converter topologies with high switched-inductor cell: (a) TLB with switched-inductor cell and (b) Four-level boost converter with switched-inductor cell

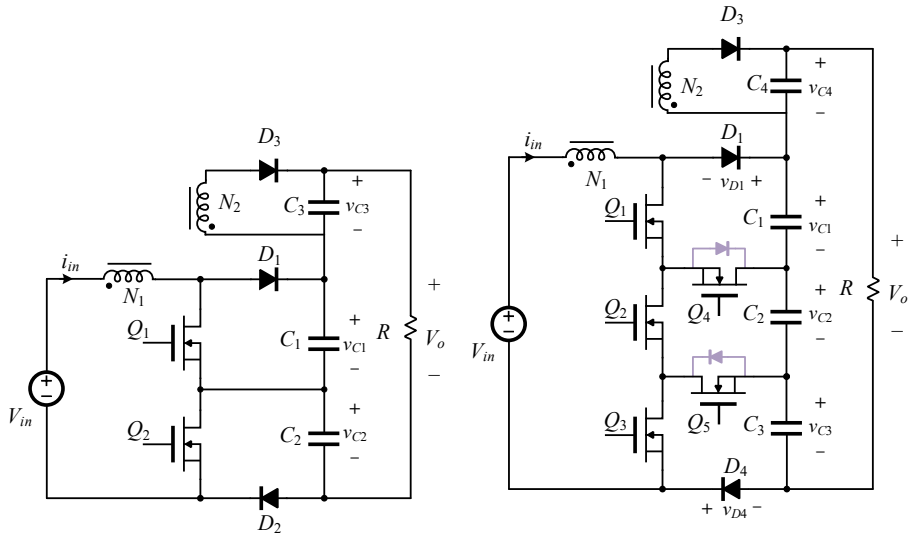

Figure 6. Hybrid multilevel with flyback converter: (a) Hybrid TLB with flyback, (b) Hybrid interleaved TLB with flyback and (c) hybrid four-level boost with flyback

Table 1. Comparison between different converters

Converter	Figure 2(a)	Figure 6(a)	Figure 4(a)	Figure 5(a)	Figure 3(a)
Voltage gain	$\frac{1}{1-d}$	$\frac{\frac{N_2}{N_1}(2d-1)+2}{2(1-d)}$	$\frac{2d}{1-d}$	$\frac{2}{1-d}$	$\frac{N_2}{N_1}\frac{1}{1-d}$
Number of capacitors	2	3	2	3	2
Number of diodes	2	3	5	4	4
number of inductors	1	–	2	2	–
number of Coupled inductors	–	1	–	–	1

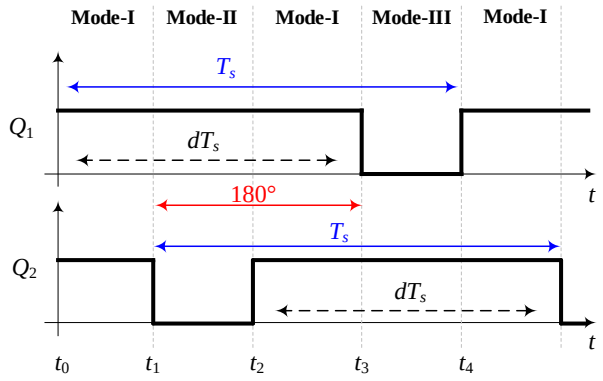

Figure 7. The switching pattern of the example converter. The two active switches have the same duty cycle, and they are 180^o out of phase.

3. EXAMPLE CONVERTER

3.1. THEORY OF OPERATION

This section presents an example of the high-voltage-gain TLB. The converter utilizes the flyback transformer to increase the voltage gain of TLB. The output voltage equals the sum of the voltage across C_1,C_2, and C_3. The converter is switched by an isolated half-bridge. The switches of the half-bridge are not complementary, but rather they are 180^o out of phase, as shown in Figure 7. The analysis of this converter is made with a few assumptions: 1) The converter operates in the steady-state, and the voltage is shared equally between C_1 and C_2; 2) All capacitors are big and the voltage ripples are neglected; 3) All components are ideals.

With respect to these assumptions, the converter has three modes of operation, as shown in Figure 8. During mode 1, both active switches are ON, and all the diodes are reverse-biased and they are OFF. The magnetizing inductor is charged by the input source. All capacitor are discharging to the output load. The equivalent circuit in this mode is

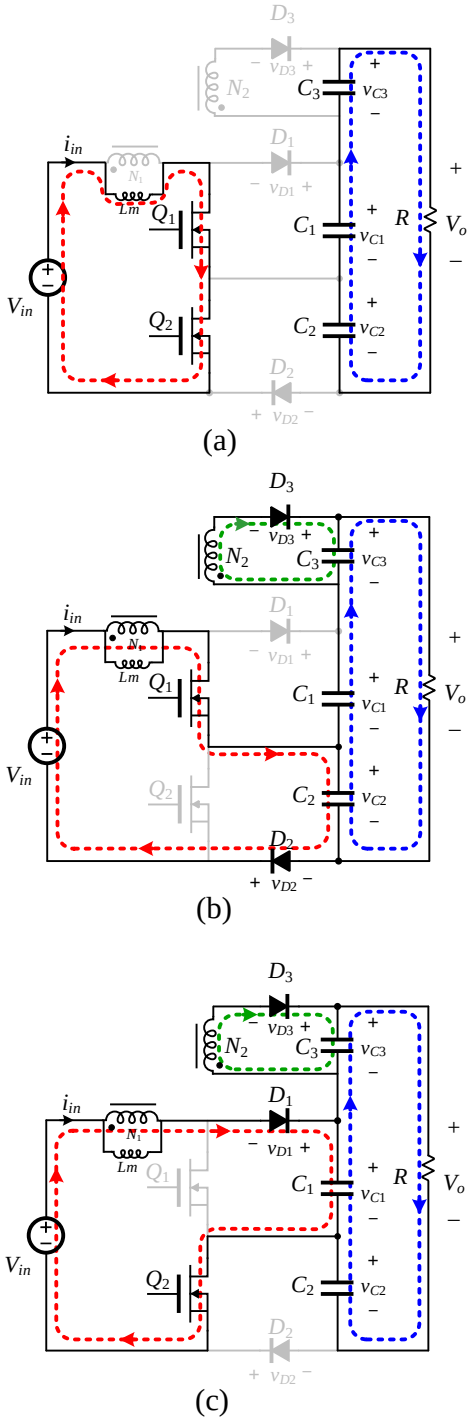

Figure 8. Modes of operation: a) mode 1: Q_1 and Q_2 are ON, b) mode 2: Q_1 is ON and Q_2 is OFF and c) mode 3: Q_1 is OFF and Q_2 is ON

shown in Figure 8 (a). The state equations are given by

$$V_{Lm} = V_{in} \tag{1}$$

$$V_o = V_{C_1} + V_{C_2} + V_{C_3} \tag{2}$$

$$I_{C_1} = I_{C_2} = I_{C_3} = -\frac{V_o}{R} \tag{3}$$

In mode 2, switch Q_1 is ON and Q_2 is OFF. Diodes D_2 and D_3 are forward-biased and conducting. Diode D_1 is reverse-biased and blocking. The equivalent circuit of this mode is shown in Figure 8 (b), and it is represented by the following equations.

$$V_{Lm} = V_{in} - V_{C_2} = \frac{V_{in} + V_{C_1} - V_o}{\left(1 + \frac{N_2}{N_1}\right)} \tag{4}$$

$$I_{C_1} = -\frac{V_o}{R} \tag{5}$$

$$I_{C_2} = I_{Q_1} - \frac{V_o}{R} \tag{6}$$

$$I_{Q_1} = I_{in} - \left(\frac{N_2}{N_1}\right) I_S \tag{7}$$

$$I_{C_3} = I_S - \frac{V_o}{R} \tag{8}$$

In mode 3, switch Q_1 is OFF and Q_2 is ON. The diode D_2 is reverse-biased and blocking. The other diodes are forward-biased and conducting. Figure 8 (c) shows the equivalent circuit of this mode. The state equations of this mode are given by

$$V_{Lm} = V_{in} - V_{C_1} = \frac{V_{in} + V_{C_2} - V_o}{\left(1 + \frac{N_2}{N_1}\right)} \tag{9}$$

$$I_{C_1} = I_{Q_2} - \frac{V_o}{R} \tag{10}$$

$$I_{Q_2} = I_{in} - \left(\frac{N_2}{N_1}\right) I_S \tag{11}$$

$$I_{C_2} = -\frac{V_o}{R} \tag{12}$$

$$I_{C_3} = I_S - \frac{V_o}{R} \tag{13}$$

By applying volt-second balance, one can obtain the steady state equations across the output capacitors, as follows:

$$V_{C_1} = V_{C_2} = \frac{0.5\ V_{in}}{1 - d} \tag{14}$$

$$V_{C_3} = \frac{\frac{N_2}{N_1}(2d - 1)}{2(1 - d)} \times V_{in} \tag{15}$$

The ideal voltage gain of the proposed converter is given by

$$M = \frac{V_o}{V_{in}} = \frac{\frac{N_2}{N_1}(2d - 1) + 2}{2(1 - d)} \tag{16}$$

The gain is a function of the duty and turns ratio. Figure 9 shows the gain of the proposed converter. Also, the gain is compared to the converter listed in Table 1, as shown in Figure 10

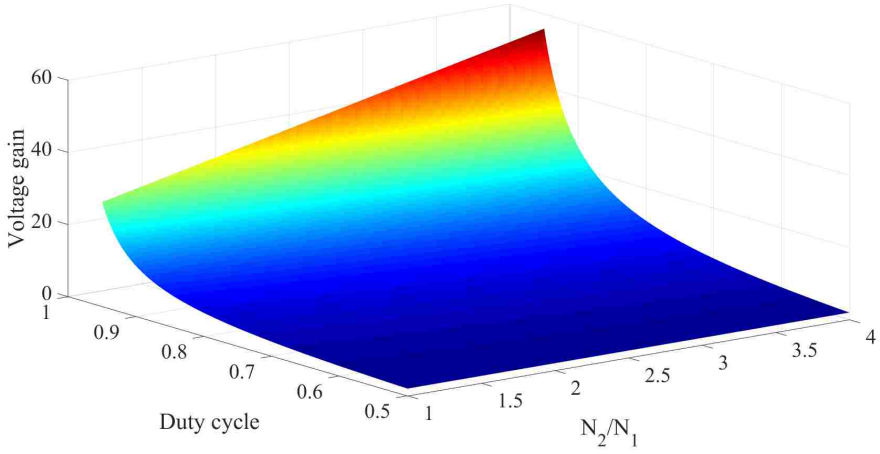

Figure 9. Gain of the converter

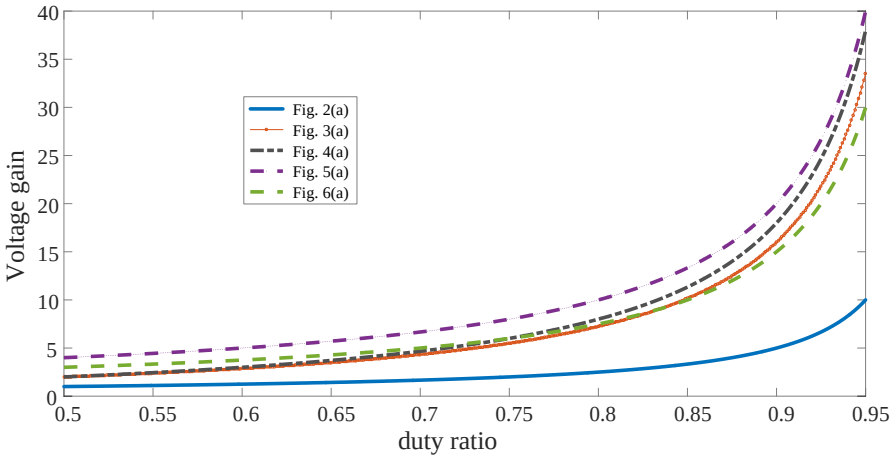

Figure 10. Voltage gain of the converters listed in Table. 1

4. COMPONENT SELECTIONS AND EFFICIENCY ANALYSIS

This section present design information of the example converter and component selections.

4.1. ACTIVE SWITCHES

The voltage stress across the active switches is the same as that of the TLB converter, which is half of the CBC. The voltage stress can be calculated by

$$V_{Q_1} = V_{Q_2} = \frac{0.5V_{in}}{1-d} \tag{17}$$

The average current of the MOSFETs is given by

$$I_{Q_{1,avg}} = I_{Q_{2,avg}} = I_{in} \times \frac{\frac{N_2}{N_1}(2d-1)+2d}{\frac{N_2}{N_1}(2d-1)+2} \tag{18}$$

where I_in can be obtained using the following equation

$$I_{in,avg} = I_o \times \frac{\frac{N_2}{N_1}(2d-1)+2}{2(1-d)} \tag{19}$$

The peak values of the active switches and the peak value of the input current are the same, and they are equal to

$$I_{in,pk} = I_{Q_{1,pk}} = I_{Q_{2,pk}} = I_{in,avg} + \frac{V_{in}(2d-1)}{2f_sL_m} \tag{20}$$

The rms current is approximated by

$$I_{Q_{1,rms}} = \sqrt{(I_o \frac{\frac{N_2}{N_1}(2d-1)+2d}{\frac{N_2}{N_1}(2d-1)+2} \frac{\frac{N_2}{N_1}(2d-1)+2}{2(1-d)})^2 + I_o \frac{\frac{N_2}{N_1}(2d-1)+2}{2(1-d)} \frac{V_{in}(2d-1)}{f_sL_m} + (\frac{V_{in}(2d-1)}{\sqrt{3}f_sL_m})^2} \tag{21}$$

and $I_{Q_{1,rms}} = I_{Q_{2,rms}}$ if the voltage across C_2 and C_1 is equal.

4.2. DIODES

The voltage stress of the diodes D_1 and D_2 can be calculated using

$$V_{D_1} = V_{D_2} = \frac{0.5V_{in}}{1-d} \tag{22}$$

the stress on the output diode D_3 is given by

$$V_{D_3} = \frac{0.5\frac{N_2}{N_1}V_{in}}{1-d} \tag{23}$$

The average current for all the diodes is equal and given by

$$I_{D_{1,avg}} = I_{D_{2,avg}} = I_{D_{3,avg}} = I_o \tag{24}$$

However, the RMS current values are different for D_3 than they are for D_1 and D_2. The RMS current is approximated by

$$I_{D_{1,rms}} = I_{D_{2,rms}} = \frac{I_o}{\sqrt{1-d}} \tag{25}$$

$$I_{D_{3,rms}} = \frac{I_o}{\sqrt{2(1-d)}} \tag{26}$$

4.3. CAPACITORS

The capacitors' voltages were already mentioned in the steady-state section, and, based on that, the voltage rating of the capacitors is selected. The capacitance is selected based on the tolerated voltage ripple of the output voltage. The capacitance can be calculated by

$$C = I_o\frac{d}{\Delta v \times f_s} \tag{27}$$

Note that the frequency seen by C_3 is twice that of the switching frequency. Hence, the required capacitance is reduced to half. The effective values of the capacitor currents are approximated by

$$I_{C_1,rms} = I_{C_2,rms} = I_o\sqrt{\frac{d}{1-d}} \tag{28}$$

$$I_{C_3,rms} = I_o\sqrt{\frac{2d-1}{2(1-d)}} \tag{29}$$

4.4. COUPLED INDUCTORS

The turns ratio of the coupled inductors can be calculated using

$$\frac{N_2}{N_1} = 2 \times \frac{\frac{V_o}{V_{in}}(1-d)-1}{2d-1} \tag{30}$$

Note that d is higher than 0.5. The magnetizing inductance can be designed based on the tolerated current ripple which is given by

$$L_m = \frac{V_{in}(2d-1)}{2\Delta_i f_s} \tag{31}$$

where Δ_i is the tolerated current ripple, which is usually $20-30\%$ of the average current.

4.5. THE LOSS ANALYSIS

The losses of the converter can be divided by the losses in each component. The losses in the coupled inductor are given by

$$P_L = \underbrace{I_{in,rms}^2 \times R_{dc}}_{copper\ loss} + \underbrace{K_{Fe}\left(\frac{dV_{in}}{2f_s N_1 A_c}\right)^{\beta}(core\ volume)}_{core\ loss} \tag{32}$$

where R_{dc} is the dc resistance of the copper wire. The parameters K_{Fe} and β are related to the core loss and determined from the manufacturer's datasheet [30]. N_1 is the number of primary turns, and A_c is the cross section area of the core. The loss in both MOSFETs is given by

$$P_{Q,total} = 2\ \underbrace{(I_{Q,rms}^2 R_{on})}_{\text{conduction loss}} + \underbrace{I_{Q,avg} V_Q (t_{off} + t_{on}) f_s}_{\text{overlap loss}} + \underbrace{C_{oss} V_Q{}^2 f_s}_{\substack{\text{loss caused by} \\ C_{oss} \text{ discharge}}} \tag{33}$$

where $R_{ds}(on)$ is the on-state resistance of the MOSFET, t_{on} and t_{off} are the turn-ON and turn-OFF times, respectively, and the C_{oss} is the output capacitance of the MOSFET. Diode conduction loss is given by

$$P_D = \underbrace{V_F \times I_o}_{\text{conduction}} + \underbrace{Q_R \times V_r \times f_s}_{\text{reverse recovery loss}} \tag{34}$$

where V_F is the forward voltage of the diode, Q_R is the reverse recovery charge, and V_r is the maximum reverse voltage. The losses caused by the capacitors' equivalent series resistance (ESR) is not significant compared to the aforementioned losses. The losses caused by ESR are given by

$$P_C = I_{C,rms}^2 ESR \tag{35}$$

The loss distribution and efficiency analysis are given in the next sections.

5. SIMULATION

The proposed converter was simulated using Simulink with PLECS blockset. The parameters used in the simulation are listed in Table 2, and small parasitic elements were included to help the solver avoid singular loops. The voltages and currents for the switches are shown in Figure 11. The maximum voltage stress across the active switches is 56 V, and that is also the maximum voltage across diodes D_1 and D_2. However, diode D_3 has to

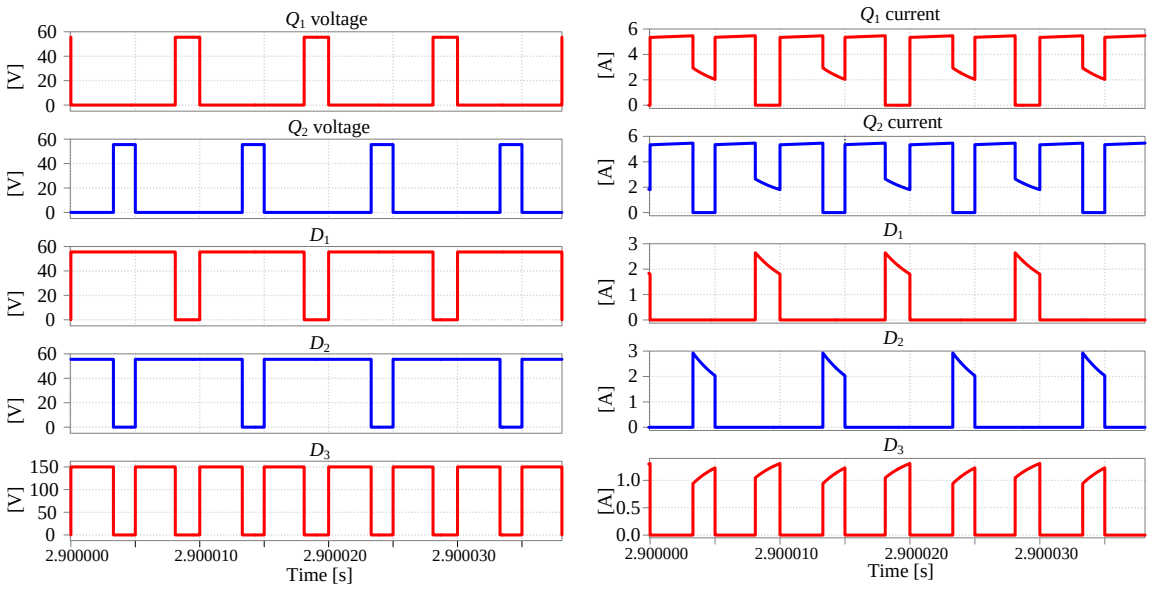

Figure 11. Voltage stress across switched (left) and current passing through switches (right)

block approximately 150 V. The average and rms values of each MOSFET current is 3.87 A and $\simeq$ 4.43 A, respectively The average and rms values of diodes D_1 and D_2's current is 0.41 A and $\simeq$ 0.98 A, respectively, and the average and rms values of the D_3 is 0.41 A and $\simeq$ 0.69 A.

Figure 12 shows the voltage and current of the input source, capacitors and output load. The voltage across capacitors C_1,C_2 and C_3 are $\simeq$ 55 V, $\simeq$ 55 V, and $\simeq$ 95 V, respectively. The output voltage is about 206 V. The effective value of the current is roughly 0.89 A for I_{C_1} and I_{C_2}. The effective value of I_{C_3} is 0.5543 A. The loss breakdown at 80 W is depicted in Figure 13, where the major loss comes from the diodes at about 46%. The active switches, coupled inductors, and capacitors account for about 29%, 24%, and 1%, respectively. The converter efficiency can be improved by selecting diodes with fast reverse recovery and low forward voltage and coupled inductors with dc resistance.

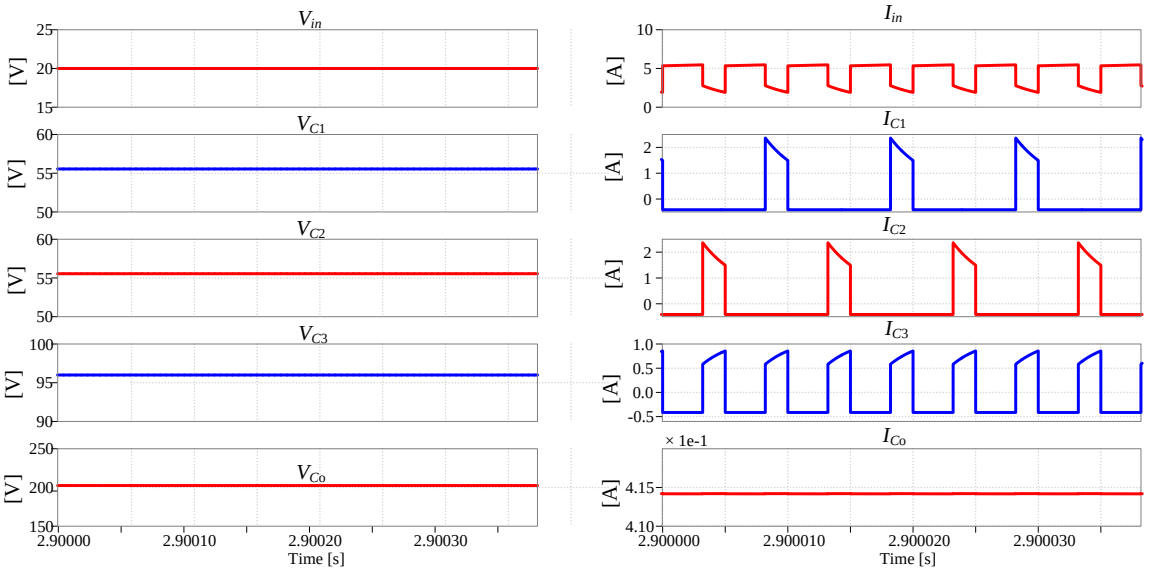

Figure 12. Input, output and capacitors waveforms. The voltage waveforms (left) and current waveforms (right)

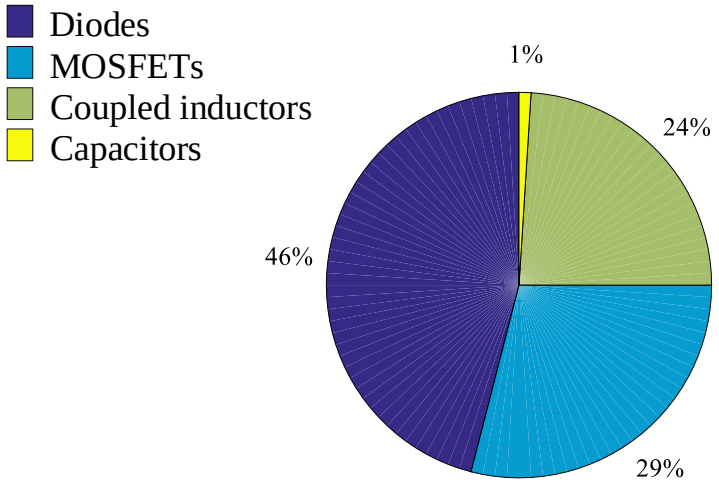

Figure 13. Simulated loss breakdown at 80 *W*

Table 2. List of parameters used in the simulation

Parameter	Value
Turns ratio	2.7
L_m	500 μH
V_{in}	20 V
V_o	200 V
Load R	500 Ω
Duty cycle	0.82
f_s	100 kHz
Capacitors	30 μF

5.1. PHOTOVOLTAIC SOURCE SIMULATION

The PV module (Uni-solar PVL-136) used in this simulation is made of a triple-junction amorphous silicon ($3 - a - Si$) material. The nominal efficiency of the module is roughly 6.26 %, and the area of the module is about 2.16 m^2. The electrical characteristics of the PV panel are given in Table 3 [31]. The simulation of a PV panel requires the identification of several PV parameters, such as the series resistance R_s, parallel resistance R_{sh}, ideality factor n, saturation current I_s and photocurrent I_{ph}. One can extract the parameters of a single diode model using different methods, such as in [32]. Table. 4 lists the extracted parameters using various approaches. The IV and PV characteristic curves at the 1000 W/m^2 and 25°C are shown in Figure 14. The fill factor of the module is 0.574. Plotting the I-V and P-V curves at different temperature values and irradiance levels illustrates how the output power of the PV panel is affected. Figure 15 shows the effect of the temperature on the output power. The PV panel has a lower open circuit Voc at a higher temperature. The output power is also reduced as the temperature is increased. Figure 16 illustrates the correlation between the irradiance and the output power. The output power of the PV increases as the solar irradiance increases [35].

Table 3. Characteristics of PVL-136 solar panel

Parameter	Value	Parameter	Value
V_{oc}	46.2	$Temp_v$ %/C	−0.38
I_{sc}	5.1	$Temp_i$ %/C	0.100
V_{mpp}	33.0	$Temp_v$ %/C	−0.309
I_{mpp}	4.1	$Temp_i$ %/C	0.100
$Maximum\ power$	135.312	$Temp_p$ %/C	−0.209
N_s	22	Fill factor	0.574

Table 4. The parameter extraction of $PVL - 136$

	Conventional [33]	[32]	NREL [34]
I_s	2.076	1.447	2.2377
I_{ph}	5.1	5.66	5.2256
R_s	1.7277	1.8493	1.9114
R_{sh}	60.1	inf	48.34
n	3.737	3.893	3.45

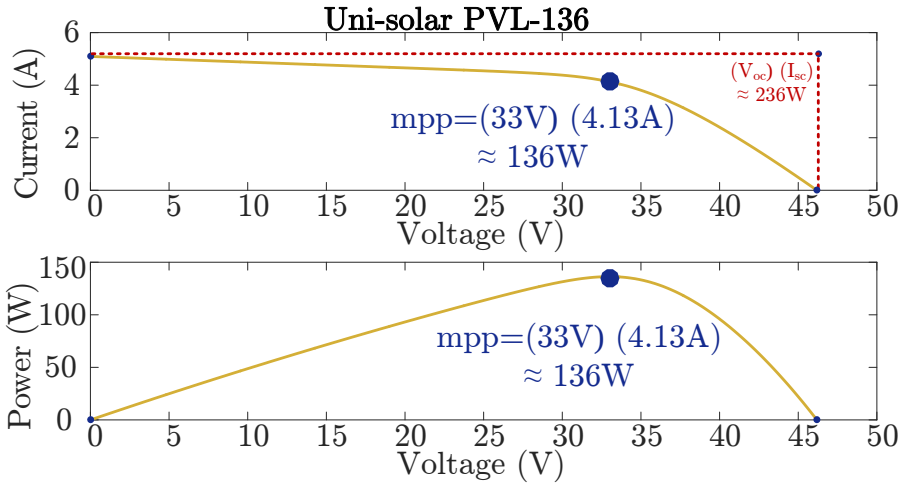

Figure 14. The I-V curve (top) and P-V curve (bottom) at the standard conditions. The maximum power point is about $136W$, and the fill factor is about 0.574.

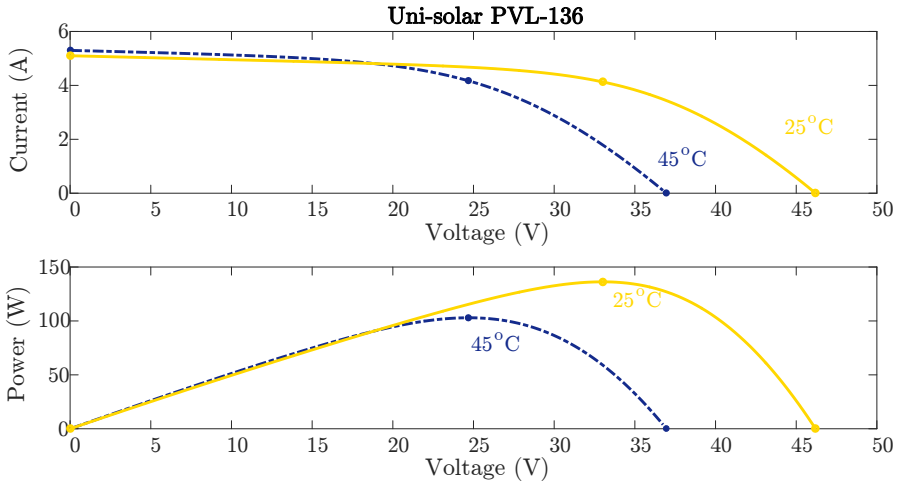

Figure 15. Temperature's effect on the I-V and P-V curves. As the temperature increases, the output power of the PV is reduced.

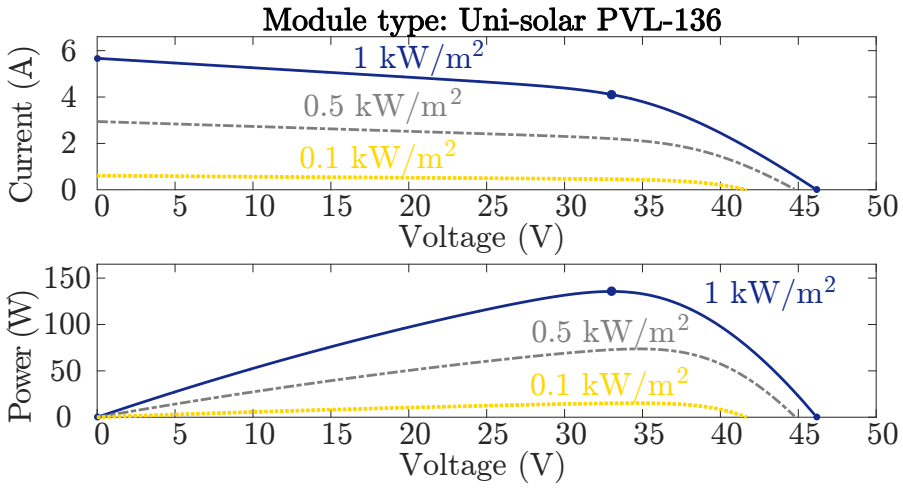

Figure 16. Irradiance's effect on the output of the PV panel. The figure shows that there is a strong correlation between the current of the PV panel and the irradiance level.

5.2. MPPT CONTROL

The PV panel operates at the maximum power (MPP) if the load resistance matches the PV resistance of the maximum power point (R_{mpp}). Often the load resistance does not match the PV, and that results in a power decrease. Therefore, a maximum power point tracker (MPPT) is needed to ensure that the PV panel produces the maximum point at any solar irradiance level. Although there are plenty of MPPT algorithms and techniques [36–40], perturb and observe (P&O) is the simplest and most widely used. The flow chart of P&O is shown in Figure 17. The challenge with such an algorithm is the size of the step of the duty. A large step size can reach the vicinity of MPP faster but mightcause the tracker to zigzag, resulting in an inablity to reach the true MPP. Small step sizes can reacher closer operation points near the true MPP but take more time to reach the MPP, and in the case of local and global maxima, the converter might get stuck in a local maxima. Several solutions suggest the adaptive or variable step size [41], in which the step size can be large if the converter operates far from the MPP and small once it operates near the MPP. However, in rapid changes of the solar irradiance level, the controller might not perform correctly. Figure 18 shows the effect of the step size on the algorithm performance. The converter was simulated to interface three parallel-connected solar panels. The simulation results are shown in Figure 19. The controller can extract the maximum power output of the PV system and perform well in cases where there is a huge dip in the solar irradiance.

6. EXPERIMENTAL

This section presents the implementation of the hardware prototype and the experimental results of the example converter. An 80 W hardware prototype, shown in Figure 20, was implemented to verify the analysis and simulation. The components used to implement the hardware are listed in Table 5. The voltage stress across components, capacitor voltages, and output voltages are depicted in Figures. 21, 22, and 22, respectively. The output voltage

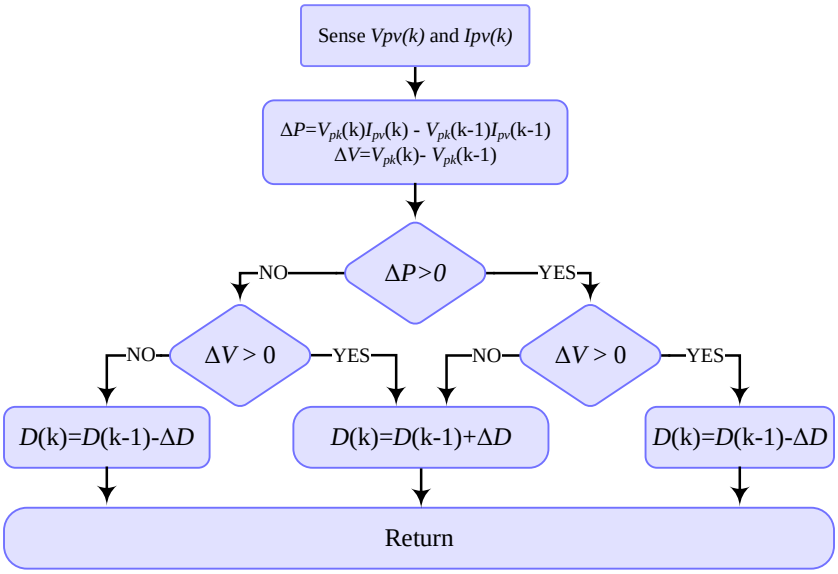

Figure 17. MPPT algorithm used to control the proposed converter

is about 200 V. The voltage stress across the active switches is low although it is slightly different from the analysis. The difference is caused by the voltage balance across the output capacitors. This is inherited from the TLB topology, and several successful attempts to remove the imbalance between capacitors have been published, such as in [42, 43]. The output voltage is not effected by the imbalance across the output capacitors. The output voltage and its ac components are shown in Figure 23, and the currents passing through the switching devices are shown in Figure 24. The efficiency of the hardware prototype is compared to the the simulation, as shown in Figure 25. The peak efficiency of the converter is around 95%.

7. CONCLUSIONS

A family of high-voltage-gain multilevel boost converter was presented. The main advantage of the proposed family is the higher effective frequency across the magnetic elements, without increasing the switching frequency, which leads to a weight and size

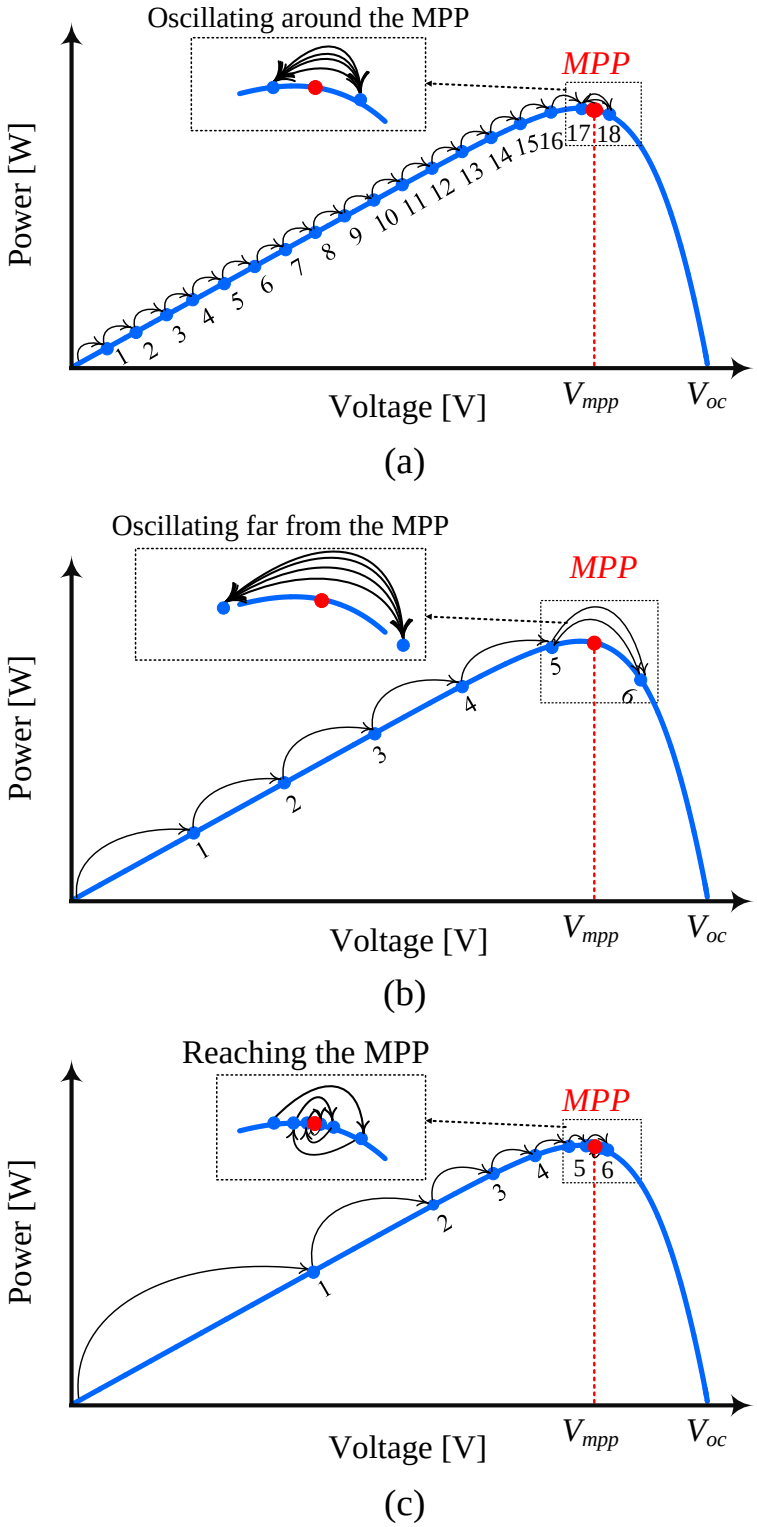

Figure 18. Effect of step size on the performance of the algorithm a) small step size b) large step size c) adaptive with $\frac{\Delta D}{i}$

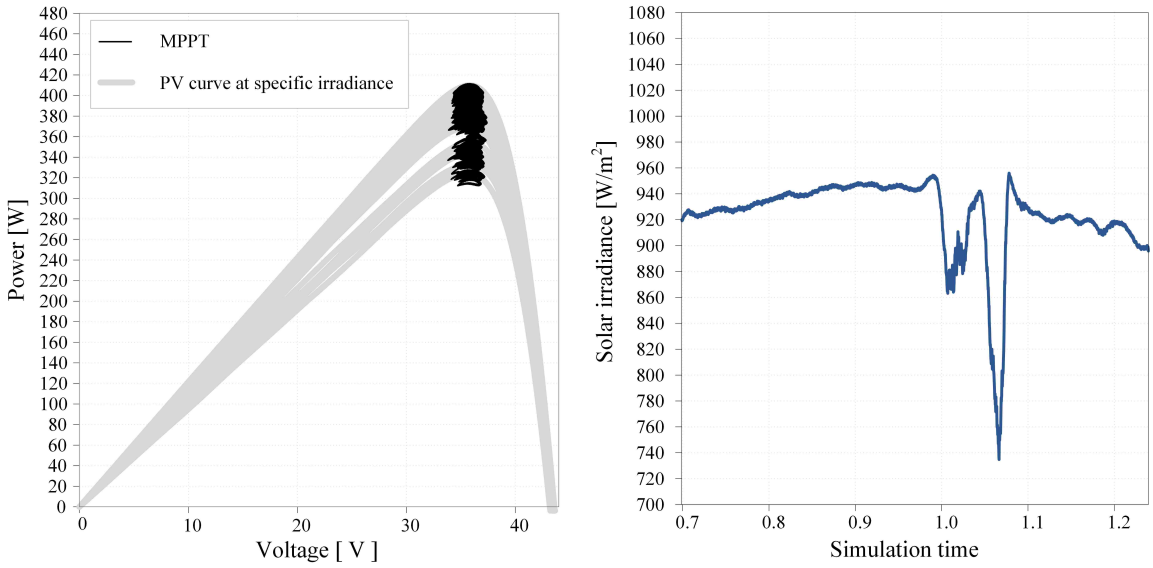

Figure 19. The simulated results of the converter with MPPT: a) Performance of the controller b) Solar irradiance

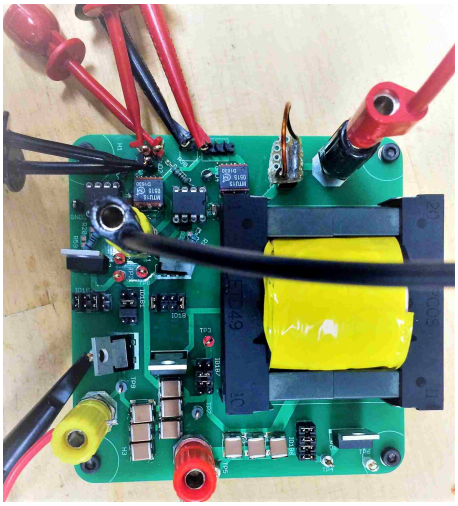

Figure 20. Hardware prototype

Table 5. Component Listing for the Hardware Prototype

Item	Designation	Rating	Part No.
Coupled inductors	$\frac{N_2}{N_1} = 2.7$	200 μH,	ETD 49, turns ratio= 2.7
Capacitor	C_1, C_2 C_3	10 μF	B32674D3106K
MOSFET	Q_1, Q_2	150 V, 37 A $R_{ds(on)} = 10.525\ m\Omega$	IPA105N15N3
Diode	D_1, D_2 D_3	250V, 40A $V_F = 0.86\ V, t_{rr} = 35\ ns$	MBR40250G

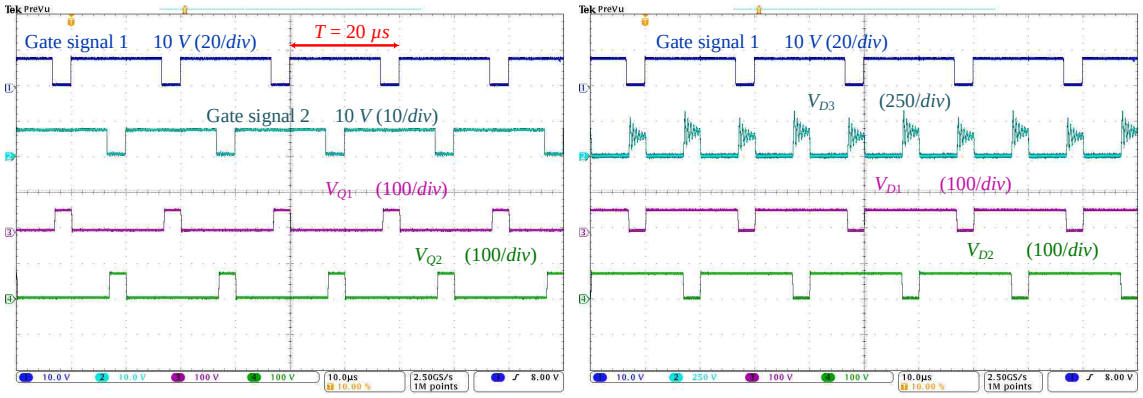

Figure 21. The voltage stress across the active switches (left) and the voltage stress across the diodes (right)

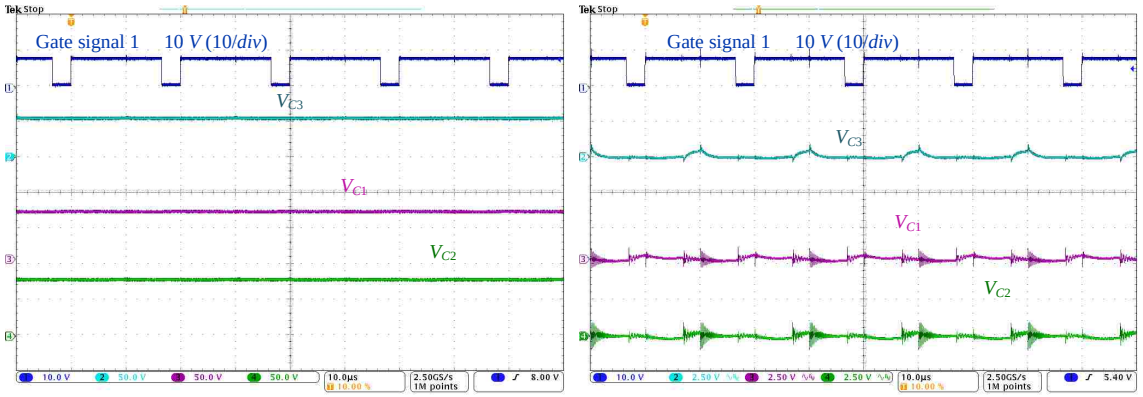

Figure 22. The voltage across the capacitors (left) and the ac components across the capacitors voltage (right)

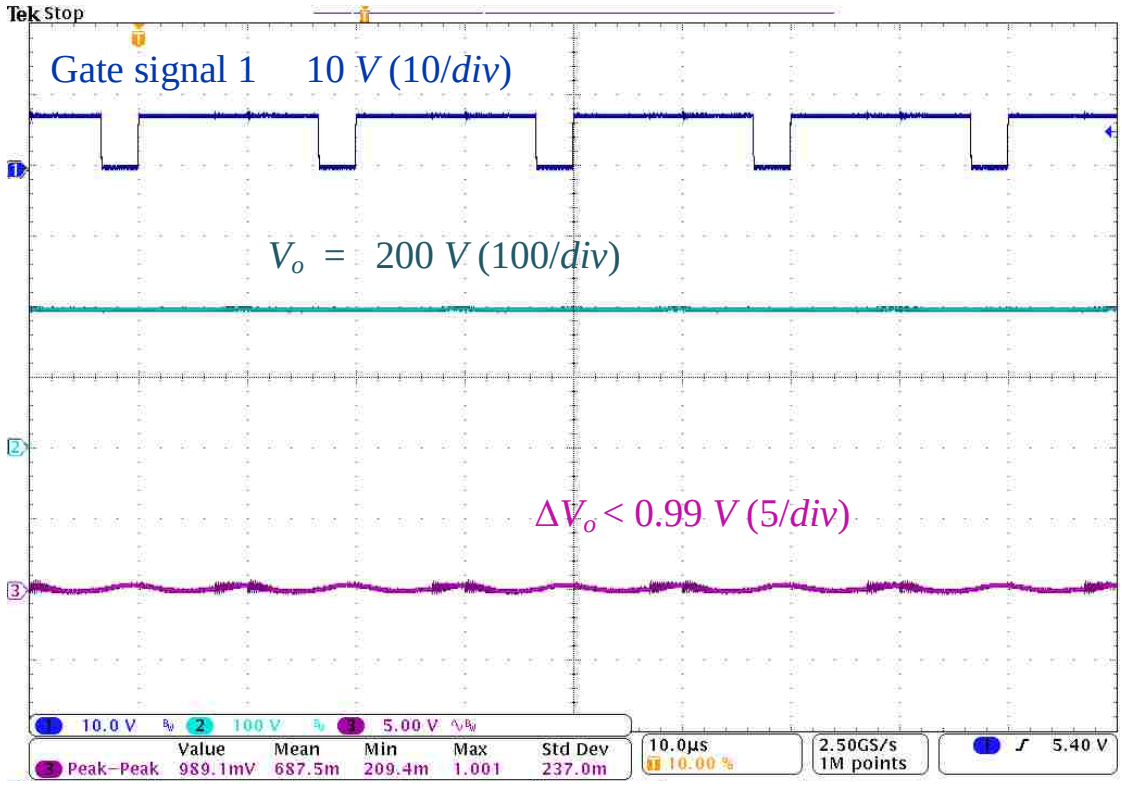

Figure 23. Experimental results of the output voltage and the voltage ripple across the output voltage

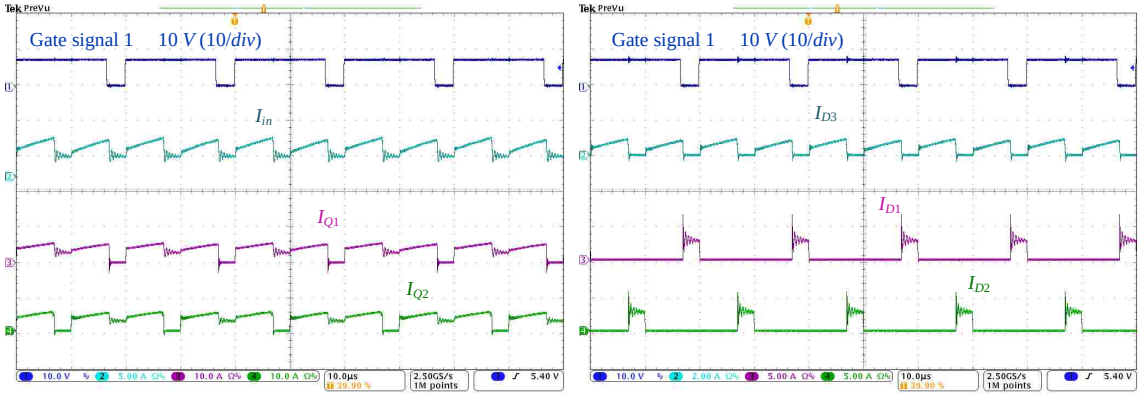

Figure 24. Input current and active switch currents (left) and diodes currents (right)

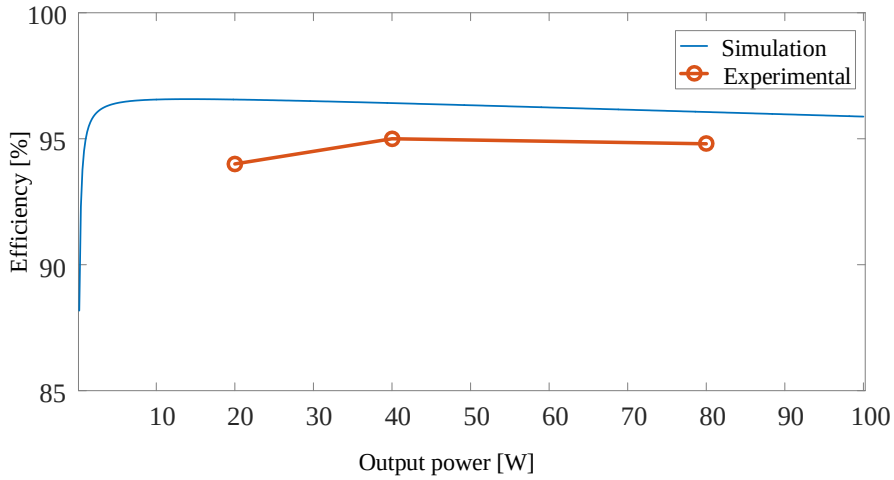

Figure 25. Efficiency of the proposed converter. Comparison between simulated and experimental efficiency

reduction of the magnetic elements. Although the input current is not a triangular waveform in this family, it is not discontinuous and has high-frequency ac components that can be easily filtered. An example converter of TLB with a flyback transformer was analyzed, designed and simulated. The converter was simulated to interface three parallel-connected solar panels, and details about MPPT control were presented. An 80 *W* hardware prototype was implemented to validate the design and simulation.

REFERENCES

[1] B. Xiao, L. Hang, J. Mei, C. Riley, L. M. Tolbert, and B. Ozpineci, "Modular cascaded h-bridge multilevel pv inverter with distributed mppt for grid-connected applications," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1722–1731, March 2015.

[2] E. Koutroulis, K. Kalaitzakis, and N. C. Voulgaris, "Development of a microcontroller-based, photovoltaic maximum power point tracking control system," *IEEE Transactions on Power Electronics*, vol. 16, no. 1, pp. 46–54, Jan 2001.

[3] B. Subudhi and R. Pradhan, "A comparative study on maximum power point tracking techniques for photovoltaic power systems," *IEEE Transactions on Sustainable Energy*, vol. 4, no. 1, pp. 89–98, Jan 2013.

[4] G. R. Walker and P. C. Sernia, "Cascaded dc-dc converter connection of photovoltaic modules," *IEEE transactions on power electronics*, vol. 19, no. 4, pp. 1130–1139, 2004.

[5] G. M. Masters, *Renewable and efficient electric power systems*. John Wiley & Sons, 2013.

[6] J.-M. Kwon, K.-H. Nam, and B.-H. Kwon, "Photovoltaic power conditioning system with line connection," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1048–1054, 2006.

[7] F. L. Tofoli, D. de Castro Pereira, W. J. de Paula, and D. d. S. O. Júnior, "Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter," *IET power Electronics*, vol. 8, no. 10, pp. 2044–2057, 2015.

[8] S.-M. Chen, T.-J. Liang, L.-S. Yang, and J.-F. Chen, "A cascaded high step-up dc–dc converter with single switch for microsource applications," *IEEE Transactions on Power Electronics*, vol. 26, no. 4, pp. 1146–1153, 2011.

[9] C. Carvalho, J. P. Oliveira, and N. Paulino, "Survey and analysis of the design issues of a low cost micro power dc-dc step up converter for indoor light energy harvesting applications," in *Proceedings of the 19th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES 2012*, May 2012, pp. 455–460.

[10] H. C. Sartori, F. Beltrame, M. L. Martins, J. E. Baggio, and J. R. Pinheiro, "Evaluation of an optimal design for a single-phase boost pfc converter (ccm) considering different magnetic materials core," in *Power Electronics Conference (COBEP), 2013 Brazilian*. IEEE, 2013, pp. 1304–1310.

[11] F. Z. Peng, M. L. Gebben, and B. Ge, "A compact nx dc-dc converter for photovoltaic power systems," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*. IEEE, 2013, pp. 4780–4784.

[12] J. Leyva-Ramos, M. Ortiz-Lopez, L. Diaz-Saldierna, and M. Martinez-Cruz, "Average current controlled switching regulators with cascade boost converters," *IET power electronics*, vol. 4, no. 1, pp. 1–10, 2011.

[13] A. A. A. Freitas, F. L. Tofoli, E. M. S. Júnior, S. Daher, and F. L. M. Antunes, "High-voltage gain dc–dc boost converter with coupled inductors for photovoltaic systems," *IET Power Electronics*, vol. 8, no. 10, pp. 1885–1892, 2015.

[14] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters: principles and practice*. John Wiley & Sons, 2003, vol. 18.

[15] M. K. Kazimierczuk, *Pulse-width modulated DC-DC power converters*. John Wiley & Sons, 2015.

[16] Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao *et al.*, "A 2-kw single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, 2017.

[17] Z. Liao, Y. Lei, and R. C. Pilawa-Podgurski, "A gan-based flying-capacitor multilevel boost converter for high step-up conversion," in *Energy Conversion Congress and Exposition (ECCE), 2016 IEEE*. IEEE, 2016, pp. 1–7.

[18] A. B. Ponniran, K. Orikawa, and J. Itoh, "Minimum flying capacitor forn-level capacitor dc/dc boost converter," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3255–3266, July 2016.

[19] A. Chub, D. Vinnikov, F. Blaabjerg, and F. Z. Peng, "A review of galvanically isolated impedance-source dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2808–2828, April 2016.

[20] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up dc-dc converters: A comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143–9178, Dec 2017.

[21] W. Li and X. He, "A family of isolated interleaved boost and buck converters with winding-cross-coupled inductors," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, pp. 3164–3173, 2008.

[22] Y. Park and S. Choi, "Soft-switched interleaved boost converters for high step-up and high power applications," in *The 2010 International Power Electronics Conference - ECCE ASIA -*, June 2010, pp. 987–994.

[23] G. Yao, A. Chen, and X. He, "Soft switching circuit for interleaved boost converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 80–86, Jan 2007.

[24] L.-S. Yang, T.-J. Liang, H.-C. Lee, and J.-F. Chen, "Novel high step-up dc–dc converter with coupled-inductor and voltage-doubler circuits," *iEEE Transactions on industrial Electronics*, vol. 58, no. 9, pp. 4196–4206, 2011.

[25] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc–dc pwm converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 2, pp. 687–696, 2008.

[26] K. I. Hwu, C. F. Chuang, and W. C. Tu, "High voltage-boosting converters based on bootstrap capacitors and boost inductors," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 6, pp. 2178–2193, June 2013.

[27] Y. Jiao, F. L. Luo, and M. Zhu, "Voltage-lift-type switched-inductor cells for enhancing dc-dc boost ability: Principles and integrations in luo converter," *IET Power Electronics*, vol. 4, no. 1, pp. 131–142, January 2011.

[28] Y. Tang, D. Fu, T. Wang, and Z. Xu, "Hybrid switched-inductor converters for high step-up conversion." *IEEE Trans. Industrial Electronics*, vol. 62, no. 3, pp. 1480–1490, 2015.

[29] T. J. Liang and K. C. Tseng, "Analysis of integrated boost-flyback step-up converter," *IEE Proceedings - Electric Power Applications*, vol. 152, no. 2, pp. 217–225, March 2005.

[30] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

[31] S. Pacca, D. Sivaraman, and G. A. Keoleian, "Parameters affecting the life cycle performance of pv technologies and systems," *Energy Policy*, vol. 35, no. 6, pp. 3316–3326, 2007.

[32] G. Petrone and G. Spagnuolo, "Parameters identification of the single-diode model for amorphous photovoltaic panels," in *2015 International Conference on Clean Electrical Power (ICCEP)*, June 2015, pp. 105–109.

[33] J. Merten, J. Asensi, C. Voz, A. Shah, R. Platz, and J. Andreu, "Improved equivalent circuit and analytical model for amorphous silicon solar cells and modules," *IEEE Transactions on electron devices*, vol. 45, no. 2, pp. 423–429, 1998.

[34] N. Blair, A. P. Dobos, J. Freeman, T. Neises, M. Wagner, T. Ferguson, P. Gilman, and S. Janzou, "System advisor model, sam 2014.1. 14: General description," 2014.

[35] H. Patel and V. Agarwal, "Matlab-based modeling to study the effects of partial shading on pv array characteristics," 2008.

[36] N. Kumar, I. Hussain, B. Singh, and B. K. Panigrahi, "Normal harmonic search algorithm based mppt for solar pv system and integrated with grid using reduced sensor approach and pnklms algorithm," *IEEE Transactions on Industry Applications*, pp. 1–1, 2018.

[37] T. Esram, J. W. Kimball, P. T. Krein, P. L. Chapman, and P. Midya, "Dynamic maximum power point tracking of photovoltaic arrays using ripple correlation control," *IEEE Transactions on power electronics*, vol. 21, no. 5, pp. 1282–1291, 2006.

[38] M. Metry, M. B. Shadmand, R. S. Balog, and H. Abu-Rub, "Mppt of photovoltaic systems using sensorless current-based model predictive control," *IEEE Transactions on Industry Applications*, vol. 53, no. 2, pp. 1157–1167, March 2017.

[39] M. Das and V. Agarwal, "Novel high-performance stand-alone solar pv system with high-gain high-efficiency dc–dc converter power stages," *IEEE Transactions on Industry Applications*, vol. 51, no. 6, pp. 4718–4728, Nov 2015.

[40] T. Esram and P. L. Chapman, "Comparison of photovoltaic array maximum power point tracking techniques," *IEEE Transactions on energy conversion*, vol. 22, no. 2, pp. 439–449, 2007.

[41] F. Liu, S. Duan, F. Liu, B. Liu, and Y. Kang, "A variable step size inc mppt method for pv systems," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp. 2622–2628, July 2008.

[42] L. A. Vitoi, R. Krishna, D. E. Soman, M. Leijon, and S. K. Kottayil, "Control and implementation of three level boost converter for load voltage regulation," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, Nov 2013, pp. 561–565.

[43] J. Chen, S. Hou, T. Sun, F. Deng, and Z. Chen, "A new interleaved double-input three-level boost converter," *Journal of Power Electronics*, vol. 16, no. 3, pp. 925–935, 2016.

IV. A FAMILY OF INTERLEAVED STEP-UP TOPOLOGIES USING SINGLE-SWITCH MULTISTAGE BOOST CONVERTERS AND VOLTAGE MULTIPLIER CELLS

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ABSTRACT

This paper presents an interleaved step-up dc-dc converter with single-switch multistage boost converters and voltage multiplier cells (VMC) to convert input sources that have low output voltage, such as renewable energy sources, to a high-voltage dc bus. The proposed converter features low voltage stress across the components, equal current sharing among all phases, and a smooth input current. Moreover, the proposed converter has a modular structure in both the VMC and the boost stage. That is, the VMC can have N number of cells, and the boost stage can have k number of stages. The k can be different in each phase, which allows the designers to integrate two independent renewable energy sources that have different output voltages. The converter was analyzed, and details about the design are included. An 80 W hardware prototype was implemented to validate the theory of operation and analysis.

Keywords: DC-DC, Interleaved, High-Gain, Multilevel, Quadratic, PV, Renewable, Power electronics, Voltage multiplier cells

1. INTRODUCTION

The high-voltage-gain dc-dc step-up converters have become more popular in recent years due to the progress in power and energy fields and the emergence and development of technologies and applications, such as dc microgrids and dc distribution systems [1–5]. The dc distribution system was found to be an enhanced alternative to the ac distribution system due to the low number of conversions, protections against grounding faults, high power quality, and cost. More importantly, the dc distribution is suitable for integrating renewable energy sources [6–12]. However, most of the renewable energy sources have low output voltage, which needs to be boosted by about $15 - 25$ times. The most common topology used for stepping up the voltage is the conventional boost converter, which has a simple structure and a low number of components. However, the voltage gain of the conventional boost converter can only be high at extreme duty cycles [13, 14]. Operating at extremely high duty cycles increases the voltage stress across the components and requires a large inductance in order to make the converter draw a continuous input current. With consideration of the conduction and the switching loss, the voltage gain is significantly reduced. Such drawbacks sparked the research for a topology with high-voltage-gain conversion ratio.

One way to increase the voltage gain is by cascading multiple conventional boost converters, where the output voltage is increased exponentially. Cascading two conventional boost converters allows both stages to operate at a low duty cycle [15–17]. Therefore, the voltage stress on the first stage components is low. However, the stress on the second stage output diode still has to block the output voltage. The quadratic converter can be simplified by using only a single active switch. The output diode of such a converter suffers from high voltage stress, and the input current has high current ripples [18–20]. The voltage stress across the components is reduced in the three-level boost converter, and the size of the converter is decreased due to the increase of the effective frequency across the inductor. The three-level boost has the same gain as the boost converter, which is not sufficient

for renewable energy applications [21, 22]. Switched capacitor circuits are capable of increasing the voltage gain by increasing the number of switching cells. Several advantages can be obtained: high power density, low EMI, the capability of being fabricated into IC chips. The drawbacks are the inherent losses, a high number of active switches that require isolation circuitry and gate drivers. Moreover, the output voltage is fixed and cannot be regulated. Several topologies utilize the transformer or a coupled inductor's turns ratio to increase the voltage gain as in [23–27]. Utilizing the transformer can meet the requirement of isolation and safety and can provide multiple outputs. However, the power density is significantly reduced, and the weight of the converter is increased. Also, the stress on the active switches caused by the parasitic leakage inductance can cause damage to the switches unless an extra auxiliary circuit is implemented to recycle the energy. Similar to using a transformer, using an integrated coupled inductor improves the voltage gain but without providing isolation, such as a hybrid flyback-boost, interleaved with coupled inductors, or quadratic boost converter with coupled inductors. Such topologies suffer from leakage inductance as well and require extra circuits for circulating the energy and reducing the voltage stress across the switches [28–30].

This paper introduces an interleaved single-switch multistage boost converter with voltage multiplier cells. The converter features low voltage stress on components and high voltage gain, allows the user to get the most ripple cancellation that interleaving offers, has the capability to integrate different voltage sources, and can match a wide range of loads. Each phase of the interleaved multistage can have either the same or a different number of boost stages than the other phases. This can be very useful for integrating sources with a significant difference in their output voltage. The VMC stage uses a bi-fold Dickson that has a symmetrical structure and low voltage stress across the components. Incorporating two symmetrical phases with the same duty cycle yields equal current sharing between the phases and a very smooth input current.

The rest of this paper is structured as follows. First, the theory of operation and steady-state

analysis of each mode is presented in Section 2. The components selection and design procedure are presented in Section 3, and the implementation of the hardware prototype and experimental results are explained in Section 4. Finally, conclusions and future work are presented in Section 5.

2. THEORY OF OPERATION AND STEADY-STATE ANALYSIS

The general structure of the proposed converter is shown in Figure 1. The converter consists of two single-switched multistage boost converter cells. These cells are 180° out of phase, and they are independent of each other, which means each cell can have a different number of the boost stages, as shown in Figure 1 (b) and (d). Two independent voltage sources can feed the proposed converter instead of one, which is an essential quality to interface multiple renewable energy sources. The single switch multistage boost converter allows the converter to achieve higher converter gain with no need to add extra active switches and can come in different topologies, as shown in Figure 2. The second stage of the converter consists of voltage multiplier cells to increase the voltage and reduce the voltage stress across the diodes. Numerous VMCs can be used with this converter as in [31–33]. Example converters of the proposed family are shown in Figure 3. In this paper, Bi-fold Dickson VMC is used for the proposed converter, which features lower stress across the diodes and capacitors. Therefore, the voltage gain can be increased in three ways: by increasing the number of VMC cells, by increasing the duty cycle, or by increasing the number of boost stages. The Figure 4 shows the proposed converter with k boost stages and N number of VMC cells. The converter can replace all diodes with active switches to improve the efficiency in case of very high power applications, as shown in Figure 5. The following analysis and experimentation are based on the converter with $k = 2$ and $N = 2$, as shown in Figure 6. The analysis of the proposed converter was performed on several assumptions: 1) All components are ideal 2) All capacitors are large so that the voltage is constant 3) The duty cycles are symmetrical 4) The converter operates in the steady state.

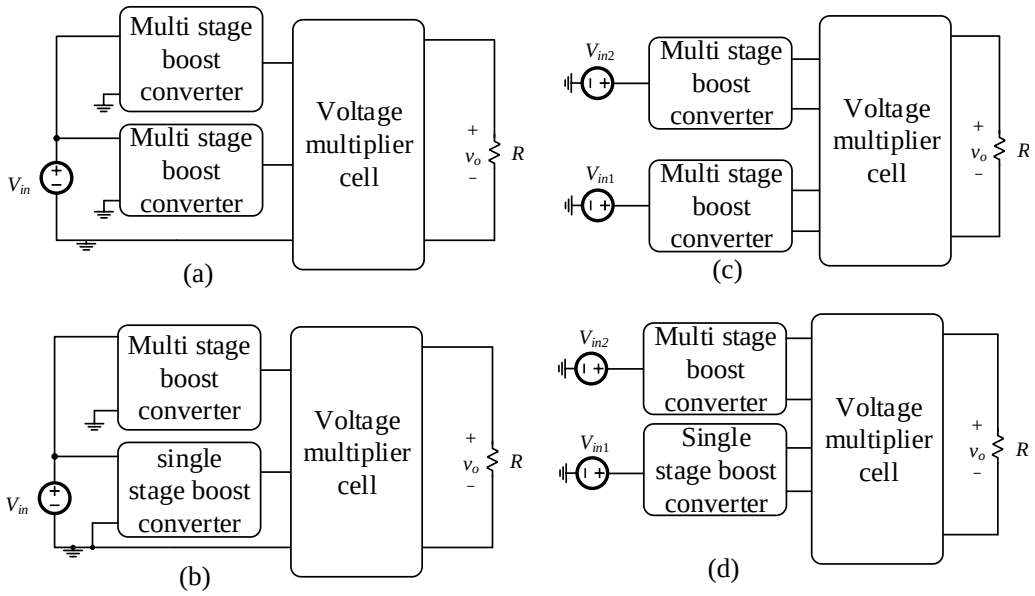

Figure 1. The general structure of the proposed converter a) both phases have a multistage boost converter and fed by a single source b) phases have different numbers of stages and are fed by a single source c) both phases have the same number of cascaded boost stages but they are fed by two independent sources d) each phase has different number of stages and they are fed by two independent voltage sources.)

The switching pattern of the proposed converter can be seen in Figure 7. The converter has three modes of operations and the sequence of the mode is that the mode 1 always comes between mode 2 and 3.

2.1. MODE 1: BOTH ACTIVE SWITCHES ARE ON

In this mode, diodes D_{a1} and D_{a3} are forward-biased, and they are ON, which allows the voltage source to charge the inductors L_1 and L_3, respectively. Diodes D_{a2} and D_{a4} are reversed biased, and they are OFF. Inductors L_2 and L_4 are being charged by capacitors C_{a1} and C_{a2}, respectively. All diodes in the VMC stage are reversed biased, and they are OFF. The load is separated from the source, and it is fed by capacitors C_{2A} and C_{2B}. the equivalent circuit for this mode is illustrated in Figure 7 (a). The inductor voltages are given by

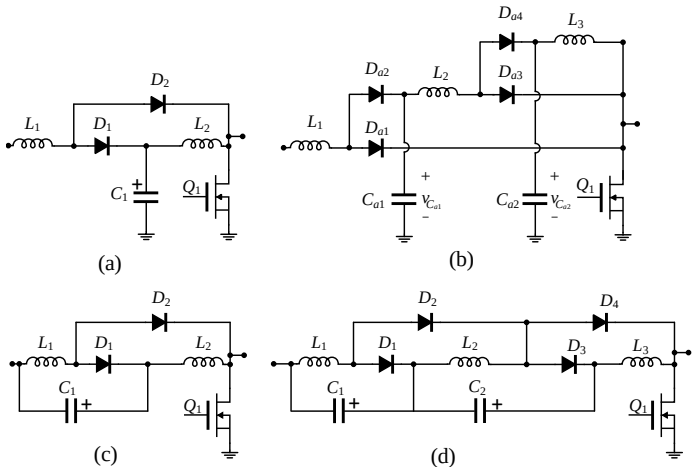

Figure 2. Multistage boost converters a) Quadratic cell with grounded capacitor, b) Cubic cell with grounded capacitors, c) Quadratic cell with floating capacitor, and d) Cubic cell with floating capacitors

$$L_1 \frac{di_{L_1}}{dt} = V_{in} \tag{1}$$

$$L_2 \frac{di_{L_2}}{dt} = V_{C_{a1}} \tag{2}$$

$$L_3 \frac{di_{L_3}}{dt} = V_{in} \tag{3}$$

$$L_4 \frac{di_{L_4}}{dt} = V_{C_{a2}} \tag{4}$$

and the output voltage is given by

$$V_o = V_{C_{2A}} + V_{C_{2B}} \tag{5}$$

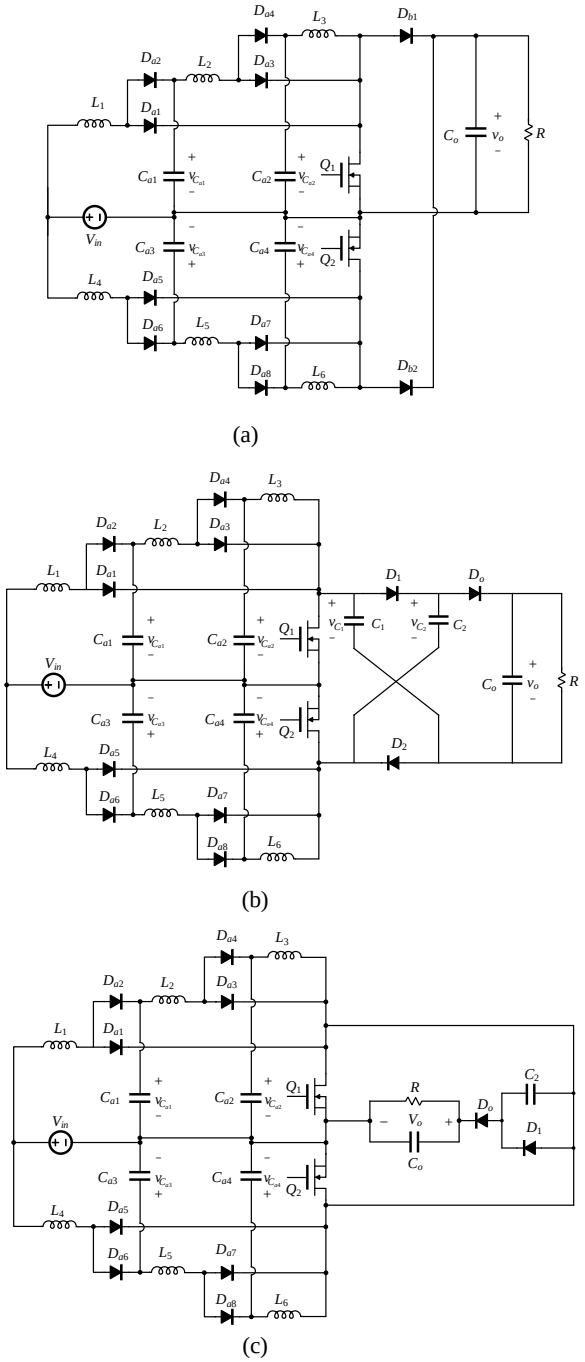

Figure 3. Different variations of the proposed converter (a) Schematic of the proposed converter with 3 stages (cubic) and no VMC, (b) another interleaved cubic boost converter with one stage of cross capacitor VMC, and (c) interleaved cubic boost converter with one Cockcroft-Walton cell.

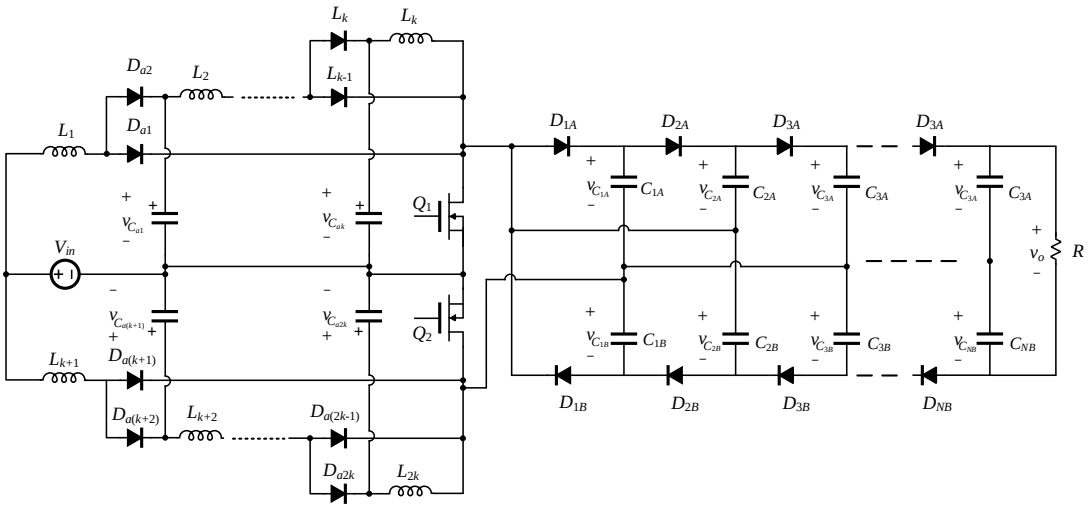

Figure 4. Schematic of the proposed converter with k boost stages and N voltage mutliplier cells. The voltage gain is $\frac{2N}{(1-d)^k}$

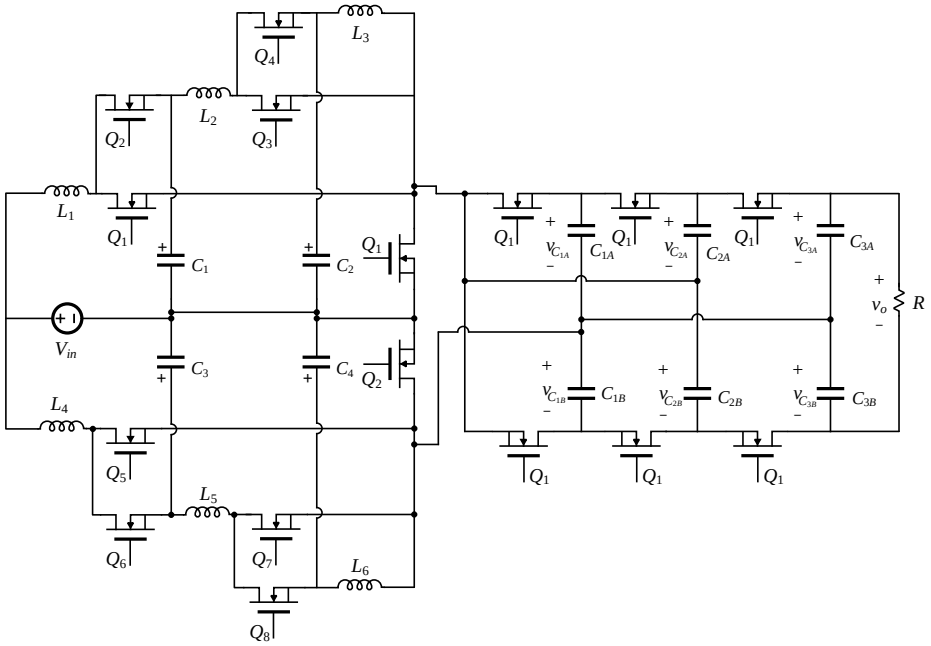

Figure 5. Schematic of the proposed converter with 3 stages (cubic) and 3 voltage mutliplier cells (tripler) and implemented using MOSFETs instead of diodes to reduce the conduction loss.

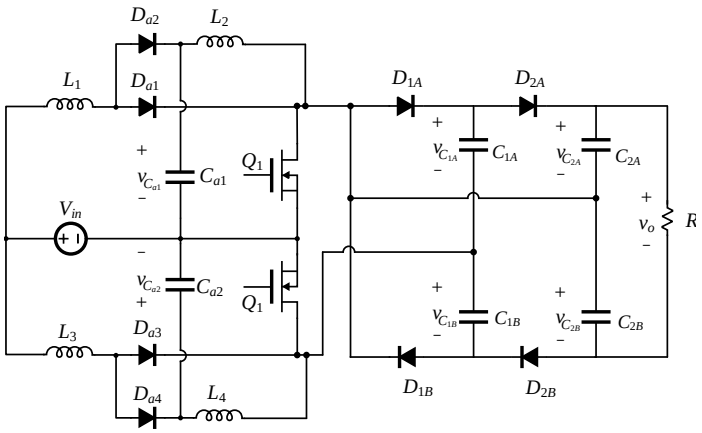

Figure 6. Schematic of the proposed converter with $k = 2$ and $N = 2$

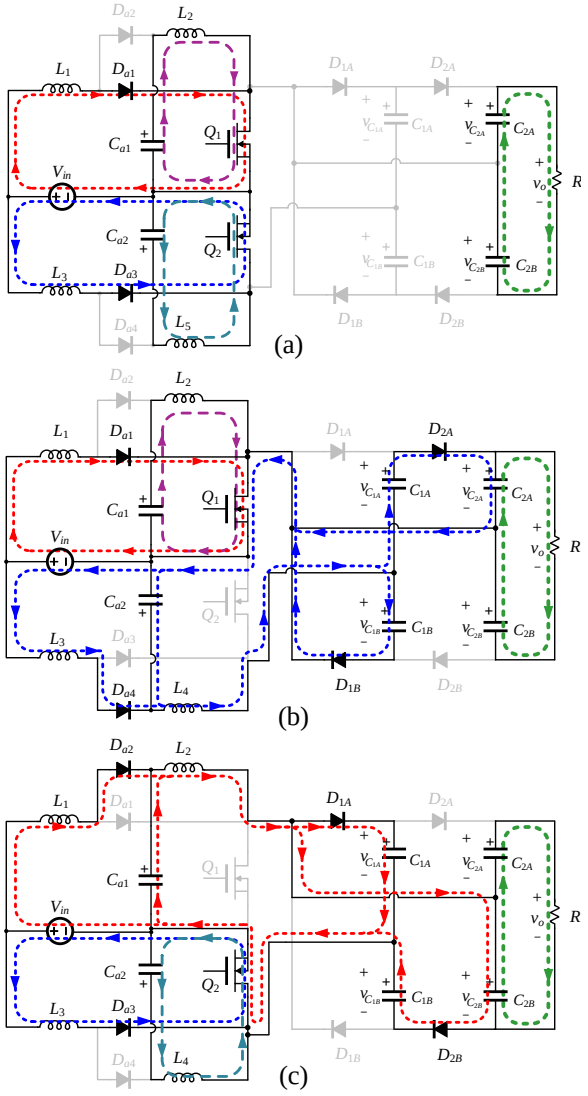

Figure 7. Equivalent circuits to a) mode 1: both active switches are ON, b) mode 2: Q_1 is ON and Q_2 is OFF, and c) mode 3: Q_1 is OFF and Q_2 is ON

2.2. MODE 2: Q_1 IS ON AND Q_2 IS OFF

In this mode, inductor L_1 is still being charged by the input source, while L_2 is being charged by C_{a1}. Inductors L_3 and L_4 are discharging to the VMC stage. Diodes D_{1A} and D_{2B} are reversed biased, and diodes D_{1B} and D_{2A} are forward biased. The energy in capacitors C_{1A} and C_{2B} is being discharged, and capacitors C_{1B} and C_{2A} are being charged. The equivalent circuit of this mode is shown in Figure 7 (b). The state equations are given by

$$L_1 \frac{di_{L_1}}{dt} = V_{in} \tag{6}$$

$$L_2 \frac{di_{L_2}}{dt} = V_{C_{a1}} \tag{7}$$

$$L_3 \frac{di_{L_3}}{dt} = V_{in} - V_{C_{a2}} \tag{8}$$

$$L_4 \frac{di_{L_4}}{dt} = V_{C_{a2}} - V_{C_{1B}} = V_{C_{a2}} + V_{C_{1A}} - V_{C_{2A}} \tag{9}$$

2.3. MODE 3: Q_1 IS OFF AND Q_2 IS ON

In this mode, L_1 and L_2 are being discharged to the VMC stage. Diodes D_{1B} and D_{2A} are reversed biased. Diodes D_{1A} and D_{2B} are also reversed biased, and they are OFF. Opposite from mode 2, capacitors C_{1B} and C_{2A} are being discharged, while C_{1B} and C_{2B} are being charged. The equivalent circuit to this mode is shown in Figure 7(c). The voltage across the inductors is given by

$$L_1 \frac{di_{L_1}}{dt} = V_{in} - V_{C_{1a}} \tag{10}$$

$$L_2 \frac{di_{L_2}}{dt} = V_{C_{a1}} - V_{C_{1A}} = V_{C_{a1}} + V_{C_{1B}} - V_{C_{2B}} \tag{11}$$

$$L_3 \frac{di_{L_3}}{dt} = V_{in} \tag{12}$$

$$L_4 \frac{di_{L_4}}{dt} = V_{C_{a2}} \tag{13}$$

2.4. STEADY-STATE ANALYSIS AND STATIC VOLTAGE GAIN

By applying voltage-second balance to the inductors, the voltage across the capacitors and the output voltage, as well as the voltage gain of the converter, can be obtained. The capacitor voltages are given by

$$V_{C_{a1}} = V_{C_{a1}} = \frac{V_{in}}{1-d} \tag{14}$$

$$V_{C_{1A}} = V_{C_{1B}} = \frac{V_{in}}{(1-d)^2} \tag{15}$$

$$V_{C_{2A}} = V_{C_{2B}} = \frac{2V_{in}}{(1-d)^2} \tag{16}$$

And the output voltage gain is given by

$$V_o = \frac{4V_{in}}{(1-d)^2} \tag{17}$$

The output voltage gain of the proposed converter with k boost converter stages and N VMC cells is given by

$$M = \frac{2N}{(1-d)^k} \tag{18}$$

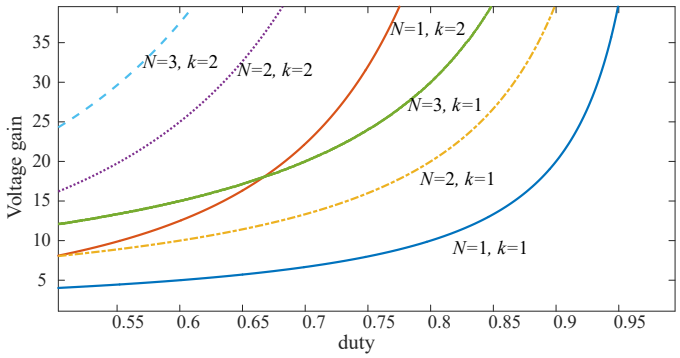

Figure 8. The voltage gain of the proposed converter with different numbers of boost stages k and voltage multiplier cells N

The converter can be fed by two independent voltage sources, and each phase can operate at a different duty cycle. Table 1 shows the output voltage for these cases.

Table 1. Output voltage at different cases when the number of stages are even

Case	the output voltage
$d_1 \neq d_2$ and $V_{in_1} \neq V_{in_2}$	$\frac{N}{(1-d_1)^2}V_{in_1} + \frac{N}{(1-d_2)^2}V_{in_2}$
$d_1 \neq d_2$ and $V_{in_1} = V_{in_2}$	$NV_{in}(\frac{1}{(1-d_1)^2} + \frac{1}{(1-d_2)^2})$
$d_1 = d_2$ and $V_{in_1} \neq V_{in_2}$	$\frac{N}{(1-d)^2}(V_{in_1} + V_{in_2})$
$d_1 = d_2$ and $V_{in_1} = V_{in_2}$	$\frac{2N}{(1-d)^2}V_{in}$

The converter is compared to other topologies in terms of the voltage gain and number of components, as shown in Table 2

Table 2. Comparison between different topologies

Topology	Quadratic cascaded boost converter [34]	Cascaded three-level boost converter (two stages) [35]	Interleaved boost with the Dickson VMC with $N = 5$ [32]	Interleaved quadratic boost converter [36]	Proposed Converter with $N = 2, k = 2$
Static voltage gain	$\frac{1}{(1-d)^2}$	$\frac{1}{(1-d)^2}$	$\frac{6}{1-D}$	$\frac{1}{(1-D)^2}$	$\frac{4}{(1-D)^2}$
Maximum stress on switches or diodes	V_o	$\frac{V_o}{2}$	$\frac{V_o}{N}$	V_o	$\frac{V_o}{2}$
Maximum voltage on capacitors	V_o	$\frac{V_o}{2}$	V_o	V_o	$\frac{V_o}{2}$
Number of capacitors	2	4	6	3	6
Number of diodes	2	4	6	6	8
Number of inductors	1	2	2	4	4
Number of floating active switches	–	2	–	–	–
Number of grounded active switches	2	2	2	2	2

3. COMPONENTS SELECTION AND EFFICIENCY ANALYSIS

3.1. ACTIVE SWITCHES

The voltage stress across the MOSFETs are given by

$$V_{Q_1} = V_{Q_2} = V_{in}\frac{1}{(1-d)^2} = \frac{V_o}{2N} \tag{19}$$

and the maximum current passing through the active switches is given by

$$I_{S_1,pk} = \frac{NV_o}{R}\frac{3-2d}{(1-d)^2} - \frac{V_{in}}{2f_s}\left(\frac{1-d}{L_1} + \frac{1}{L_2} - \frac{d}{(1-d)L_4}\right) \tag{20}$$

$$I_{S_2,pk} = \frac{NV_o}{R}\frac{3-2d}{(1-d)^2} - \frac{V_{in}}{2f_s}\left(\frac{1-d}{L_3} + \frac{1}{L_4} - \frac{d}{(1-d)L_2}\right) \tag{21}$$

The rms currents can be approximated using the following equation

$$I_{S_1,rms} = I_{S_2,rms} = \frac{NV_o}{R}\sqrt{\frac{4}{(1-d)^2} + \frac{1}{(1-d)^4}} \tag{22}$$

Table 3. Diode average and RMS currents

Current	Average	RMS
$I_{D_{1A}}, I_{D_{1B}}, I_{D_{2A}}, I_{D_{2B}}$	$\frac{V_o}{R}$	$\frac{V_o}{R}\sqrt{\frac{1}{1-d}}$
$I_{D_{a_1}}, I_{D_{a_3}}$	$\frac{V_o}{R}\frac{dN}{(1-d)^2}$	$\frac{V_o}{R}\frac{N}{(1-d)^2}\sqrt{d}$
$I_{D_{a_2}}, I_{D_{a_4}}$	$\frac{V_o}{R}\frac{(N)}{(1-d)}$	$\frac{V_o}{R}\frac{N}{(1-d)^2}\sqrt{1-d}$

3.2. DIODES

The maximum voltage stress across the diodes is given by

$$V_{D_{a1}} = V_{D_{a3}} = V_{in}\frac{d}{(1-d)^2} \tag{23}$$

$$V_{D_{a2}} = V_{D_{a4}} = V_{in}\frac{1}{1-d} \tag{24}$$

$$V_{D_{1A}} = V_{D_{2A}} = V_{D_{1B}} = V_{D_{2B}} = 2V_{in}\frac{1}{(1-d)^2} \tag{25}$$

The average current and the RMS current passing through the diodes are shown in Table. 3.

3.3. INDUCTORS

The input current is given by

$$I_{in} = \frac{V_o}{R}\frac{2N}{(1-d)^2} \tag{26}$$

the average current passing through inductors L_1 and L_3 is given by

$$I_{L_1} = I_{L_3} = \frac{V_o}{R}\frac{N}{(1-d)^2} \tag{27}$$

Table 4. Inductor peak and RMS currents

Current	Peak	RMS
I_{L_1}	$\frac{V_o}{R}\frac{N}{(1-d)^2} + \frac{V_{in}d}{2L_1 f_s}$	$\sqrt{\left(\frac{V_o}{R}\frac{N}{(1-d)^2}\right)^2 + \left(\frac{V_{in}d}{2\sqrt{3}L_1 f_s}\right)^2}$
I_{L_2}	$\frac{V_o}{R}\frac{N}{1-d} + \frac{V_{in}d}{2(1-d)L_2 f_s}$	$\sqrt{\left(\frac{V_o}{R}\frac{N}{(1-d)}\right)^2 + \left(\frac{V_{in}d}{2\sqrt{3}(1-d)L_2 f_s}\right)^2}$
I_{L_3}	$\frac{V_o}{R}\frac{N}{(1-d)^2} + \frac{V_{in}d}{2L_3 f_s}$	$\sqrt{\left(\frac{V_o}{R}\frac{N}{(1-d)^2}\right)^2 + \left(\frac{V_{in}d}{2\sqrt{3}L_3 f_s}\right)^2}$
I_{L_4}	$\frac{V_o}{R}\frac{N}{1-d} + \frac{V_{in}d}{2(1-d)L_4 f_s}$	$\sqrt{\left(\frac{V_o}{R}\frac{N}{(1-d)}\right)^2 + \left(\frac{V_{in}d}{2\sqrt{3}(1-d)L_4 f_s}\right)^2}$

the average current passing through inductors L_2 and L_4 is given by

$$I_{L_2} = I_{L_4} = \frac{V_o}{R}\frac{N}{(1-d)} \tag{28}$$

The operation of the proposed converter in the CCM requires minimum inductance. The minimum inductance for L_1 and L_3 can be calculated using

$$L_{1,crit} = L_{3,crit} = \frac{V_{in}d(1-d)^2}{2NI_o f_s} \tag{29}$$

the critical inductance for L_2 and L_4

$$L_{2,crit} = L_{4,crit} = \frac{V_{in}d(1-d)}{2NI_o f_s} \tag{30}$$

The peak and rms values of inductor currents are listed in Table 4

3.4. CAPACITORS

The voltage across the capacitors is already calculated in. The capacitor values are chosen based on the allowed ripples on the voltage. The output capacitance can be caluclaced by

$$C = \frac{V_o}{R}\frac{(1-d)T_s}{\Delta V_C} \tag{31}$$

The RMS current of the output, and the first stage capacitors are given, respectively, by

$$I_{C_{2A,rms}} = I_{C_{2B,rms}} = I_o\sqrt{\frac{d}{1-d}} \tag{32}$$

$$I_{C_{1A,rms}} = I_{C_{1B,rms}} = I_o\left(1+\sqrt{\frac{d}{1-d}}\right) \tag{33}$$

3.5. EFFICIENCY ANALYSIS

The efficiency of the proposed converter is mainly affected by the diodes, inductors and active switches. Table 5 lists all the equations used for calculating the losses of the converter. The simulated efficiency is compared to the experimental in Section 4.

Table 5. Efficiency analysis for components

Components	Equation	Variables
Inductors conduction loss	$I^2_{L_{rms}} \times R_L$	R_L is the dc resistance of the inductor
Inductors core loss	$a(\Delta B)^b f_s^c$	a, b, and c obtained using curve fitting from material datasheet
MOSFETs switching loss	$\frac{f_s}{2} C_{\text{oss}} \times V_S^2 +$ $\frac{f_s}{2} \times \frac{NV_oV_s}{R(1-d)^2} \times (t_{\text{OFF}} + t_{\text{ON}})$	C_{oss} is mosfet output capacitor f_s is switching frequency T_{on} and T_{on} are the on and off time of the mosfet
MOSFETs conduction loss	$I^2_{S_{rms}} \times R_{on}$	R_{on} is the conduction resistance of the MOSFET
Diode conduction loss	$V_f * I_{D_{avg}}$	V_f is the forward voltage of the diode
Capacitor ESR loss	$I^2_{C_{rms}} \times ESR$	ESR is the equivalent series resistance of the capacitor

Table 6. Component Listing for the Hardware Prototype

Item	Designation	Rating	Part No.
Inductor	$L_1 - L_4$	100 μH, DCR = 25 $m\Omega$,	60B104C
Capacitor	C_{1A}, C_{2A} $C_{1B} C_{2B}$	10 μF	EXH2E106HRPT
Capacitor	C_{a1}, C_{a2}	10 μF	B32674D3106K
MOSFET	Q_1, Q_2	150 V, 37 A $R_{ds(on)}$ = 10.525 $m\Omega$	IPA105N15N3
Diode	D_{1A}, D_{2A} D_{1B}, D_{2B}	250V, 40A V_F = 0.86 V, t_{rr} = 35 ns	MBR40250G

4. EXPERIMENTAL IMPLEMENTATION AND RESULTS

An 80 W hardware prototype was implemented and tested in the laboratory to verify the operation and the analysis of the converter. Figure 9 shows the hardware prototype, which was implemented using the components listed in Table. 6. The $N5700$ was used to supply power at 10 V to the prototype, and the output load was implemented using a mix of ceramic resistors. The duty cycle was set to be around 0.6, and that made the output equal to 250 V. The measurements and waveforms were taken at 80 V. Figure 10 shows the voltage waveforms across the switches. The active switches have a maximum voltage stress of 62 V. The maximum voltage stress across the diodes in the interleaved single-switch multistage is about 38 V for D_{a1} and D_{a3} and about 63 V for D_{a2} and D_{a4}. The maximum voltage stress across the VMC diodes is 125 V. The voltage across the capacitors, depicted in Figure 11, is 25 V for C_1 and C_2, 63 V for C_{1A} and C_{1B} and 125 V for C_{2A} and C_{2B}. The output voltage is about 250 V with ac components of less than 2%. Other waveforms such as the current of the switches and passive components are shown in Figure 12 and Figure 13. The efficiency of the converter was simulated and experimentally measured, as shown in Figure 14. As mentioned before, the efficiency can be further increased by selecting efficient diodes with low forward voltage for the interleaved boost stage or by replacing the diodes with efficient ones or MOSFETs.

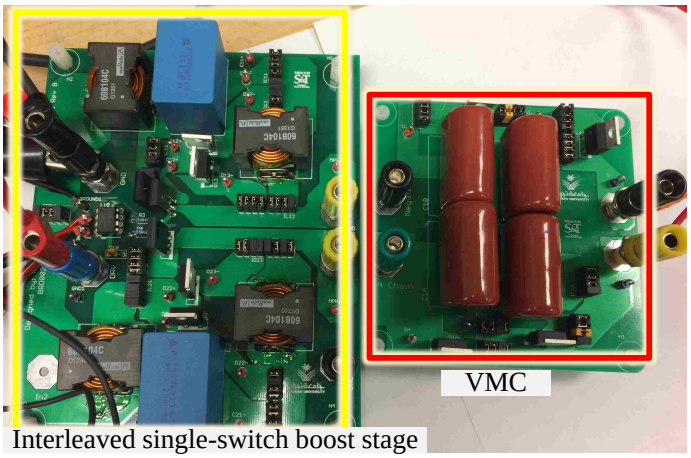

Figure 9. Hardware prototype

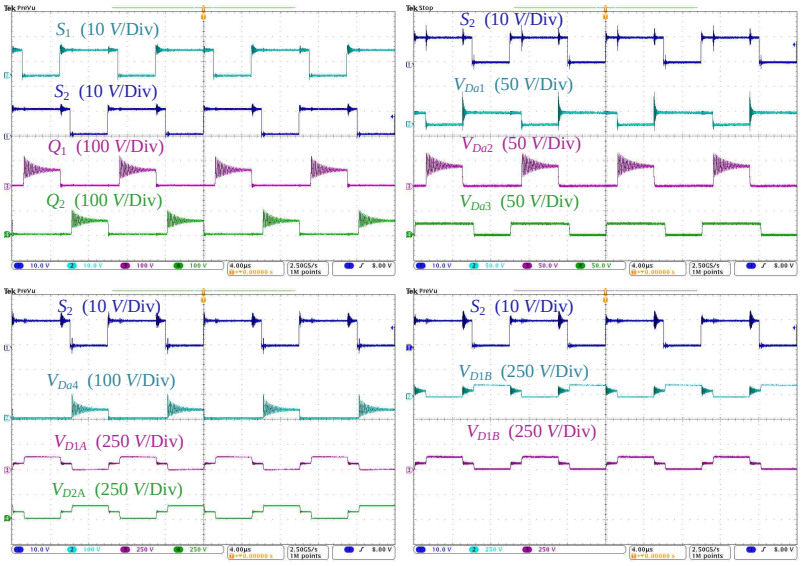

Figure 10. Voltage waveforms of the active switches and the diodes.

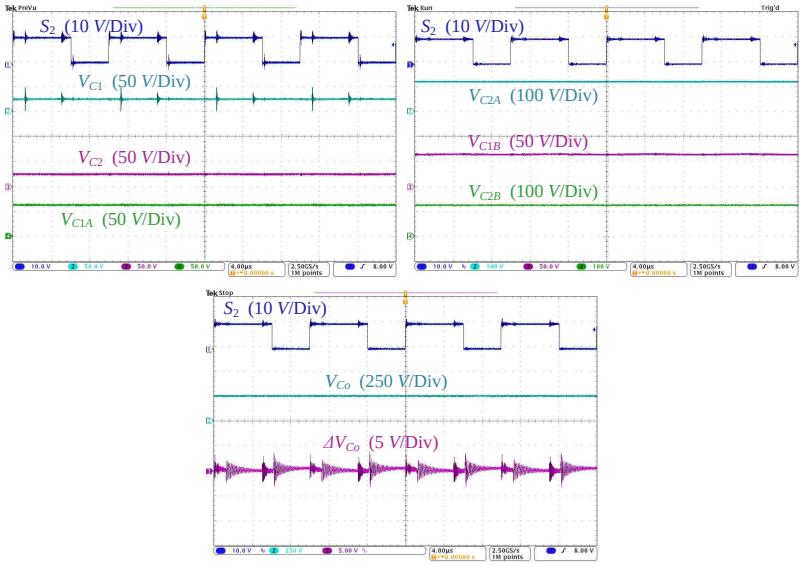

Figure 11. Voltage waveforms of the capacitors, the output load and the ac components of the output voltage.

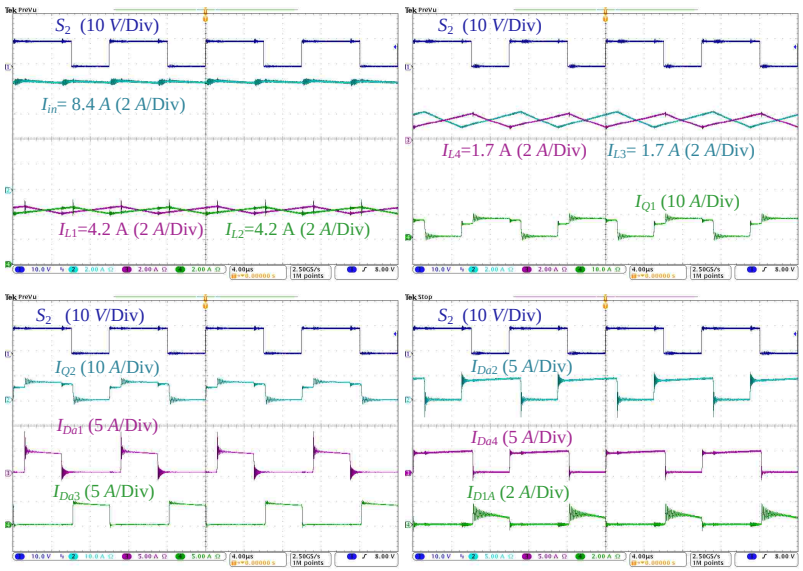

Figure 12. Current passing through the active switches, inductors and diodes D_{11}-D_{23}

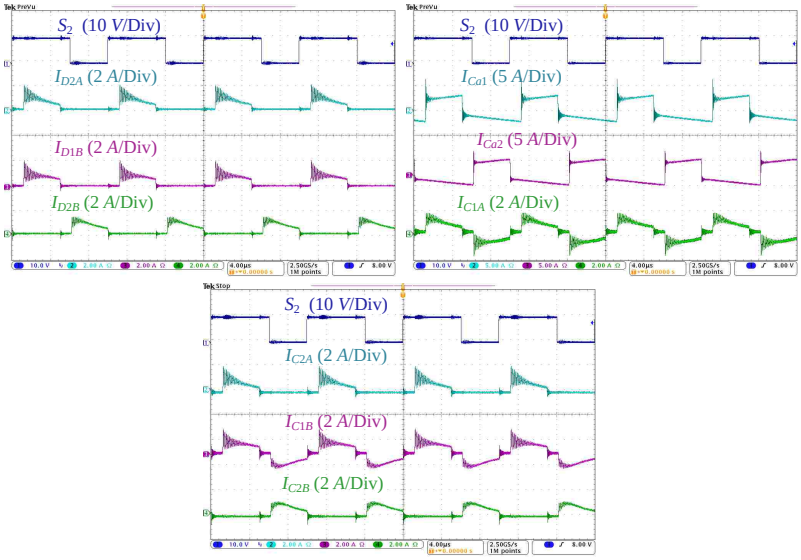

Figure 13. Currents waveforms of the VMC diodes, VMC capacitors and C_{a1} and C_{a2}

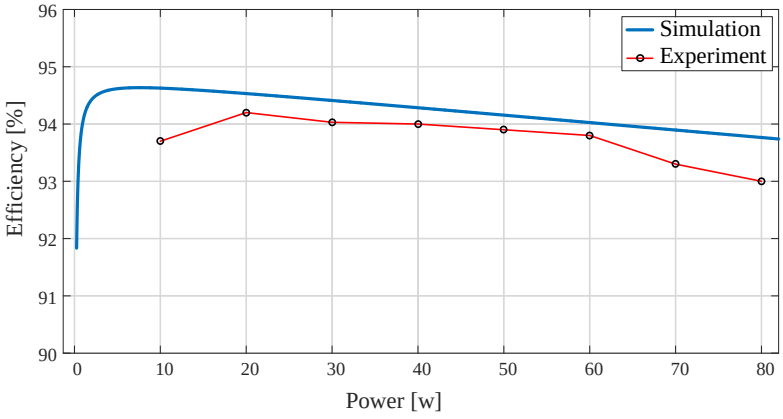

Figure 14. The efficiency of the hardware prototype and the simulated efficiency

5. CONCLUSIONS

This paper presents a non-isolated interleaved multistage boost converter with VMC. The converter has a high voltage and low voltage stresses across the components. Converting a $10V$ to a 250 V can be achieved by the quadratic boost stage and a 2-cell VMC when operating at a 0.6 duty ratio. The converter is capable of converting power from a single source or two independent sources. The input is shared among the two phases equally, and since the converter operates at 0.6 the current ripple cancellation is higher than the other interleaved boost converters. The analysis of this converter was explained and validated by simulation and experimental prototype. The converter is very suitable for integrating PV panels to higher voltage DC buses.

REFERENCES

[1] R. Wai, C. Lin, R. Duan, and Y. Chang, "High-efficiency dc-dc converter with high voltage gain and reduced switch stress," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 1, pp. 354–364, Feb 2007.

[2] O. Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 8, pp. 1098–1102, Aug 2003.

[3] G. A. Henn, R. Silva, P. P. Praca, L. Barreto, and D. S. Oliveira Jr, "Interleaved-boost converter with high voltage gain," *IEEE transactions on power electronics*, vol. 25, no. 11, pp. 2753–2761, 2010.

[4] M. Lakshmi and S. Hemamalini, "Nonisolated high gain dc–dc converter for dc microgrids," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1205–1212, Feb 2018.

[5] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. PortilloGuisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 4, pp. 1002–1016, June 2006.

[6] B. Nordman and K. Christensen, "Dc local power distribution: Technology, deployment, and pathways to success," *IEEE Electrification Magazine*, vol. 4, no. 2, pp. 29–36, June 2016.

[7] C. Xu and K. Cheng, "A survey of distributed power system—ac versus dc distributed power system," in *Power Electronics Systems and Applications (PESA), 2011 4th International Conference on*. IEEE, 2011, pp. 1–12.

[8] E. Planas, J. Andreu, J. I. Gárate, I. M. de Alegría, and E. Ibarra, "Ac and dc technology in microgrids: A review," *Renewable and Sustainable Energy Reviews*, vol. 43, pp. 726–749, 2015.

[9] S. Whaite, B. Grainger, and A. Kwasinski, "Power quality in dc power distribution systems and microgrids," *Energies*, vol. 8, no. 5, pp. 4378–4399, 2015.

[10] M. Monadi, M. A. Zamani, J. I. Candela, A. Luna, and P. Rodriguez, "Protection of ac and dc distribution systems embedding distributed energy resources: A comparative review and analysis," *Renewable and sustainable energy reviews*, vol. 51, pp. 1578–1593, 2015.

[11] B. S. Revathi and M. Prabhakar, "Non isolated high gain dc-dc converter topologies for pv applications–a comprehensive review," *Renewable and Sustainable Energy Reviews*, vol. 66, pp. 920–933, 2016.

[12] M. Nasir, H. A. Khan, A. Hussain, L. Mateen, and N. A. Zaffar, "Solar pv-based scalable dc microgrid for rural electrification in developing regions," *IEEE Transactions on Sustainable Energy*, vol. 9, no. 1, pp. 390–399, Jan 2018.

[13] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

[14] S. D. Johnson, A. F. Witulski, and R. W. Erickson, "Comparison of resonant topologies in high-voltage dc applications," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 24, no. 3, pp. 263–274, May 1988.

[15] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, "A dc-dc multilevel boost converter," *IET Power Electronics*, vol. 3, no. 1, pp. 129–137, January 2010.

[16] G. R. Walker and P. C. Sernia, "Cascaded dc-dc converter connection of photovoltaic modules," *IEEE transactions on power electronics*, vol. 19, no. 4, pp. 1130–1139, 2004.

[17] J. Leyva-Ramos, M. Ortiz-Lopez, L. Diaz-Saldierna, and J. Morales-Saldana, "Switching regulator using a quadratic boost converter for wide dc conversion ratios," *IET Power Electronics*, vol. 2, no. 5, pp. 605–613, 2009.

[18] R. Kadri, J. Gaubert, G. Champenois, and M. Mostefaï, "Performance analysis of transformless single switch quadratic boost converter for grid connected photovoltaic systems," in *The XIX International Conference on Electrical Machines - ICEM 2010*, Sept 2010, pp. 1–7.

[19] E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun, "A family of single-switch pwm converters with high step-up conversion ratio," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 4, pp. 1159–1171, May 2008.

[20] F. L. Luo and H. Ye, *Advanced dc/dc converters*. crc Press, 2016.

[21] J.-M. Kwon, B.-H. Kwon, and K.-H. Nam, "Three-phase photovoltaic system with three-level boosting mppt control," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2319–2327, 2008.

[22] V. Yaramasu, B. Wu, S. Alepuz, and S. Kouro, "Predictive control for low-voltage ride-through enhancement of three-level-boost and npc-converter-based pmsg wind turbine," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 12, pp. 6832–6843, 2014.

[23] A. Chub, D. Vinnikov, F. Blaabjerg, and F. Z. Peng, "A review of galvanically isolated impedance-source dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2808–2828, April 2016.

[24] I. Barbi and R. Gules, "Isolated dc-dc converters with high-output voltage for twta telecommunication satellite applications," *IEEE Transactions on Power Electronics*, vol. 18, no. 4, pp. 975–984, 2003.

[25] M.-K. Nguyen, Y.-C. Lim, J.-H. Choi, and G.-B. Cho, "Isolated high step-up dc-dc converter based on quasi-switched-boost network." *IEEE Trans. Industrial Electronics*, vol. 63, no. 12, pp. 7553–7562, 2016.

[26] J. Duarte, L. Lima, L. Oliveira, M. Mezaroba, L. Michels, and C. Rech, "Modeling and digital control of a single-stage step-up/down isolated pfc rectifier," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 1017–1028, 2013.

[27] F. Evran and M. T. Aydemir, "Isolated high step-up dc–dc converter with low voltage stress," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3591–3603, 2014.

[28] F. L. Tofoli, D. d. C. Pereira, W. J. de Paula, and D. d. S. Oliveira Júnior, "Survey on non-isolated high-voltage step-up dc-dc topologies based on the boost converter," *IET Power Electronics*, vol. 8, no. 10, pp. 2044–2057, 2015.

[29] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman, "Step-up dc–dc converters: a comprehensive review of voltage-boosting techniques, topologies, and applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143–9178, 2017.

[30] W. Li and X. He, "Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1239–1250, April 2011.

[31] A. Alzahrani, P. Shamsi, and M. Ferdowsi, "Boost converter with bipolar dickson voltage multiplier cells," in *Renewable Energy Research and Applications (ICRERA), 2017 IEEE 6th International Conference on*. IEEE, 2017, pp. 228–233.

[32] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi, "A dc–dc converter with high voltage gain and two input boost stages," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4206–4215, June 2016.

[33] M. Fu, C. Zhao, J. Song, and C. Ma, "A low-cost voltage equalizer based on wireless power transfer and a voltage multiplier," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 7, pp. 5487–5496, July 2018.

[34] O. López-Santos, L. Martínez-Salamero, G. García, H. Valderrama-Blavi, and T. Sierra-Polanco, "Comparison of quadratic boost topologies operating under sliding-mode control," in *Power Electronics Conference (COBEP)*, 2013, pp. 66–71.

[35] W. Li, X. Lv, Y. Deng, J. Liu, and X. He, "A review of non-isolated high step-up dc/dc converters in renewable energy applications," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Feb 2009, pp. 364–369.

[36] S. Balci, N. Altin, H. Komurcugil, and I. Sefa, "Performance analysis of interleaved quadratic boost converter with coupled inductor for fuel cell applications," in *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Oct 2016, pp. 3541–3546.

SECTION

2. SUMMARY AND CONCLUSIONS

This dissertation has presented several advanced high-voltage-gain dc-dc step-up topologies suitable for renewable energy sources integration to a high voltage dc distribution bus. First, a family of interleaved boost converters with VMCs was presented. The family consists of two stages: an interleaved boost stage and a VMC stage, which mainly consist of diodes and capacitors and are expendable. The output of the VMC can be filtered by an output diode and output capacitors or by an LC filter. Many group combinations are presented and compared in terms of the voltage gain, output-input connection, input current sharing among inductors, and the number of capacitors and diodes per stage. An example converter to efficiently convert a 20 V to a 400 V was designed and verified by simulation and experimental results. The second paper has presented a novel VMC and connected it to an interleaved boost converter with no need of an output diode or LC filter. Therefore, the output is fed by two capacitors and the voltage is rectified at each VMC stage. The proposed converter features a have high voltage gain, equal current sharing, low voltage stress across components, and better ripple cancellation across capacitors. The proposed converter was analyzed, and the design process was explained. A 200 W hardware prototype was implemented to convert 20 V input to 400 V output. The converter has a peak efficiency of 96% and maximum voltage stress across components less than 135 V. The third paper presents a hybrid fly-multilevel boost converter. The converter utilizes the multilevel structure to increase the effective frequency across the magnetic device, which is a flyback transformer. The proposed hybrid multilevel boost converters have most required features for renewable energy applications, such as low stress across components, high voltage gain, drawing continuous current, and small magnetic elements. The converter modes

of operation and steady-state analysis are presented and verified by simulation. Further verification was ensured by implementing a hardware prototype of an example converter to convert 20 V to 200 V for 100 W output load power. Paper four presents an interleaved multistage boost converter with VMC. In this topology, each phase of the interleaved stage can have the same or a different number of boost stages, and all phases share the VMC. The theory of operation, the steady-state analysis is presented for example converter, which has an interleaved quadratic boost stage with two-stage VMC. The converter was analyzed and verified by simulation results. A hardware prototype was implemented to convert 10 V to 250 V and 200 W to prove the operation and further verify the simulation results. Future work includes experimentation of large PV side surfaced and more panels to demonstrate the benefit of the proposed structures over the flat regular solar PV panels and closed-loop analysis and control of the proposed converters. Different control schemes have to be further studied, and further details about MPPT extraction algorithms under different weather conditions are required to reveal the operation of the proposed converters further.

REFERENCES

[1] B. P. Baddipadiga and M. Ferdowsi. A high-voltage-gain dc-dc converter based on modified dickson charge pump voltage multiplier. *IEEE Transactions on Power Electronics*, 32(10):7707–7715, Oct 2017. ISSN 0885-8993. doi: 10.1109/TPEL.2016.2594016.

[2] Mojtaba Forouzesh, Yam P Siwakoti, Saman A Gorji, Frede Blaabjerg, and Brad Lehman. Step-up dc–dc converters: a comprehensive review of voltage-boosting techniques, topologies, and applications. *IEEE Transactions on Power Electronics*, 32(12):9143–9178, 2017.

[3] Johann W. Kolar. Future challenges for research and teaching in power electronics, 2014. International Conference on Optimization of Electrical and Electronic Equipment, OPTIM 2014; Conference Location: Brasov, Rumania; Conference Date: May 22-24, 2014; Conference lecture on 23 May 2014.

[4] R. Hans, A. Manfred, P. Janina, and S. Alexander. Improved characterization of the magnetic properties of hexagonally packed wires. In *Proceedings of the 2011 14th European Conference on Power Electronics and Applications*, pages 1–9, Aug 2011.

[5] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. PortilloGuisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso. Power-electronic systems for the grid integration of renewable energy sources: A survey. *IEEE Transactions on Industrial Electronics*, 53(4):1002–1016, June 2006. ISSN 0278-0046. doi: 10.1109/TIE.2006.878356.

[6] Bin Lu, Edwin L Piner, and Tomás Palacios. Schottky-drain technology for algan/gan high-electron mobility transistors. *IEEE Electron Device Letters*, 31(4):302–304, 2010.

[7] Robert W Erickson and Dragan Maksimovic. *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

[8] Marian K Kazimierczuk. *Pulse-width modulated DC-DC power converters*. John Wiley & Sons, 2015.

[9] F. L. Tofoli, D. d. C. Pereira, W. Josias de Paula, and D. d. S. Oliveira Júnior. Survey on non-isolated high-voltage step-up dc-dc topologies based on the boost converter. *IET Power Electronics*, 8(10):2044–2057, 2015. ISSN 1755-4535. doi: 10.1049/iet-pel.2014.0605.

[10] L. Huber and M. M. Jovanovic. A design approach for server power supplies for networking applications. In *APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.00CH37058)*, volume 2, pages 1163–1169 vol.2, Feb 2000. doi: 10.1109/APEC.2000.822834.

[11] Tsai-Fu Wu and Te-Hung Yu. Unified approach to developing single-stage power converters. *IEEE Transactions on Aerospace and Electronic Systems*, 34(1):211–223, Jan 1998. ISSN 0018-9251. doi: 10.1109/7.640279.

[12] J. Leyva-Ramos, M. G. Ortiz-Lopez, L. H. Diaz-Saldierna, and J. A. Morales-Saldana. Switching regulator using a quadratic boost converter for wide dc conversion ratios. *IET Power Electronics*, 2(5):605–613, Sept 2009. ISSN 1755-4535. doi: 10.1049/iet-pel.2008.0169.

[13] Fang Lin Luo and Hong Ye. *Advanced dc/dc converters*. crc Press, 2016.

[14] Fang Lin Luo and Hong Ye. Positive output cascade boost converters. *IEE Proceedings-Electric Power Applications*, 151(5):590–606, 2004.

[15] M. G. Ortiz-Lopez, J. Leyva-Ramos, E. E. Carbajal-Gutierrez, and J. A. Morales-Saldana. Modelling and analysis of switch-mode cascade converters with a single active switch. *IET Power Electronics*, 1(4):478–487, December 2008. ISSN 1755-4535. doi: 10.1049/iet-pel:20070379.

[16] J-Y Lee and S-N Hwang. Non-isolated high-gain boost converter using voltage-stacking cell. *Electronics Letters*, 44(10):644–646, 2008.

[17] K. B. Park, G. W. Moon, and M. J. Youn. Nonisolated high step-up stacked converter based on boost-integrated isolated converter. *IEEE Transactions on Power Electronics*, 26(2):577–587, Feb 2011. ISSN 0885-8993. doi: 10.1109/TPEL.2010.2066578.

[18] M. Tanca V. and I. Barbi. Nonisolated high step-up stacked dc-dc converter based on boost converter elements for high power application. In *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, pages 249–252, May 2011. doi: 10.1109/ISCAS.2011.5937548.

[19] S. K. Changchien, T. J. Liang, J. F. Chen, and L. S. Yang. Novel high step-up dc-dc converter for fuel cell energy conversion system. *IEEE Transactions on Industrial Electronics*, 57(6):2007–2017, June 2010. ISSN 0278-0046. doi: 10.1109/TIE.2009.2026364.

[20] Jesus Valdez-Resendiz, Julio Rosas-caro, Jonathan C Mayo-Maldonado, and Armando Llamas-Terres. Quadratic boost converter based on stackable switching stages. *IET Power Electronics*, 2018.

[21] M. T. Zhang, Yimin Jiang, F. C. Lee, and M. M. Jovanovic. Single-phase three-level boost power factor correction converter. In *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual*, number 0, pages 434–439 vol.1, Mar 1995. doi: 10.1109/APEC.1995.468984.

[22] Jung-Min Kwon, Bong-Hwan Kwon, and Kwang-Hee Nam. Three-phase photovoltaic system with three-level boosting mppt control. *IEEE Transactions on Power Electronics*, 23(5):2319–2327, 2008.

[23] Ahmed Shahin, Melika Hinaje, Jean-Philippe Martin, Serge Pierfederici, Stéphane Raël, and Bernard Davat. High voltage ratio dc–dc converter for fuel-cell applications. *IEEE Transactions on Industrial Electronics*, 57(12):3944–3955, 2010.

[24] João Paulo M Figueiredo, Fernando L Tofoli, and Bruno Leonardo A Silva. A review of single-phase pfc topologies based on the boost converter. In *Industry Applications (INDUSCON), 2010 9th IEEE/IAS International Conference on*, pages 1–6. IEEE, 2010.

[25] Venkata Yaramasu and Bin Wu. Predictive control of a three-level boost converter and an npc inverter for high-power pmsg-based medium voltage wind energy conversion systems. *IEEE Trans. Power Electron*, 29(10):5308–5322, 2014.

[26] Ned Mohan and Tore M Undeland. *Power electronics: converters, applications, and design*. John Wiley & Sons, 2007.

[27] R. P. Severus. A new current-fed converter topology. In *1979 IEEE Power Electronics Specialists Conference*, pages 277–283, June 1979. doi: 10.1109/PESC.1979.7081036.

[28] L Wuidart. Topologies for switched mode power supplies. *Application Note AN*, 513:0393, 1999.

[29] Michael Douglas Seeman. *A design methodology for switched-capacitor DC-DC converters*. University of California, Berkeley, 2009.

[30] M. D. Seeman and S. R. Sanders. Analysis and optimization of switched-capacitor dc-dc converters. *IEEE Transactions on Power Electronics*, 23(2):841–851, March 2008. ISSN 0885-8993. doi: 10.1109/TPEL.2007.915182.

[31] G. Palumbo and D. Pappalardo. Charge pump circuits: An overview on design strategies and topologies. *IEEE Circuits and Systems Magazine*, 10(1):31–45, First 2010. ISSN 1531-636X. doi: 10.1109/MCAS.2009.935695.

[32] M. S. Makowski. Realizability conditions and bounds on synthesis of switched-capacitor dc-dc voltage multiplier circuits. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, 44(8):684–691, Aug 1997. ISSN 1057-7122. doi: 10.1109/81.611263.

[33] J. W. Kimball. Performance analysis of generalized algebraic switched capacitor converters. In *2013 IEEE Energy Conversion Congress and Exposition*, pages 1808–1813, Sept 2013. doi: 10.1109/ECCE.2013.6646927.

[34] A. Kushnerov and S. Ben-yaakov. Unified algebraic synthesis of generalised fibonacci switched capacitor converters. *IET Power Electronics*, 7(3):540–544, March 2014. ISSN 1755-4535. doi: 10.1049/iet-pel.2013.0197.

[35] L. Balogh and R. Redl. Power-factor correction with interleaved boost converters in continuous-inductor-current mode. In *Proceedings Eighth Annual Applied Power Electronics Conference and Exposition,*, pages 168–174, March 1993. doi: 10.1109/APEC.1993.290634.

[36] Dean R Garth, WJ Muldoon, GC Benson, and EN Costague. Multi-phase, 2-kilowatt, high-voltage, regulated power supply. In *Power Electronics Specialists Conference, 1971 IEEE*, pages 110–116. IEEE, 1971.

[37] B. A. Miwa, D. M. Otten, and M. E. Schlecht. High efficiency power factor correction using interleaving techniques. In *[Proceedings] APEC '92 Seventh Annual Applied Power Electronics Conference and Exposition*, pages 557–568, Feb 1992. doi: 10.1109/APEC.1992.228361.

[38] R. Giral, L. Martinez-Salamero, and S. Singer. Interleaved converters operation based on cmc. *IEEE Transactions on Power Electronics*, 14(4):643–652, July 1999. ISSN 0885-8993. doi: 10.1109/63.774201.

[39] Michael O'Loughlin. An interleaving pfc pre-regulator for high-power converters. *Texas Instruments*, pages 1–14, 2006.

[40] R. Gules, L. L. Pfitscher, and L. C. Franco. An interleaved boost dc-dc converter with large conversion ratio. In *2003 IEEE International Symposium on Industrial Electronics (Cat. No.03TH8692)*, volume 1, pages 411–416 vol. 1, June 2003. doi: 10.1109/ISIE.2003.1267284.

[41] Wuhua Li, Yi Zhao, Yan Deng, and Xiangning He. Interleaved converter with voltage multiplier cell for high step-up and high-efficiency conversion. *IEEE Transactions on Power Electronics*, 25(9):2397–2408, 2010.

[42] M. M. Jovanovic. A technique for reducing rectifier reverse-recovery-related losses in high-power boost converters. *IEEE Transactions on Power Electronics*, 13(5): 932–941, Sep 1998. ISSN 0885-8993. doi: 10.1109/63.712314.

[43] Remus Teodorescu, Marco Liserre, and Pedro Rodriguez. *Grid converters for photovoltaic and wind power systems*, volume 29. John Wiley & Sons, 2011.

[44] F. Blaabjerg, Y. Yang, and K. Ma. Power electronics - key technology for renewable energy systems - status and future. In *2013 3rd International Conference on Electric Power and Energy Conversion Systems*, pages 1–6, Oct 2013. doi: 10.1109/EPECS.2013.6712980.

[45] Johann W Kolar, Jürgen Biela, Stefan Waffler, Thomas Friedli, and Uwe Badstübner. Performance trends and limitations of power electronic systems. In *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*, pages 1–20. IEEE, 2010.

[46] Jacobus Daniel van Wyk and Fred C Lee. On a future for power electronics. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 1(2):59–72, 2013.

[47] V. A. K. Prabhala, B. P. Baddipadiga, and M. Ferdowsi. Dc distribution systems; an overview. In *2014 International Conference on Renewable Energy Research and Application (ICRERA)*, pages 307–312, Oct 2014. doi: 10.1109/ICRERA.2014.7016575.

[48] A. Pratt, P. Kumar, and T. V. Aldridge. Evaluation of 400v dc distribution in telco and data centers to improve energy efficiency. In *INTELEC 07 - 29th International Telecommunications Energy Conference*, pages 32–39, Sept 2007. doi: 10.1109/INTLEC.2007.4448733.

[49] P. T. Krein. Data center challenges and their power electronics. *CPSS Transactions on Power Electronics and Applications*, 2(1):39–46, 2017. ISSN 2475-742X. doi: 10.24295/CPSSTPEA.2017.00005.

[50] D. J. Hammerstrom. Ac versus dc distribution systemsdid we get it right? In *2007 IEEE Power Engineering Society General Meeting*, pages 1–5, June 2007. doi: 10.1109/PES.2007.386130.

[51] A. Mohamed and O. Mohammed. Connectivity of dc microgrids involving sustainable energy sources. In *2011 IEEE Industry Applications Society Annual Meeting*, pages 1–8, Oct 2011. doi: 10.1109/IAS.2011.6074338.

[52] Venkata Anand Kishore Prabhala, Poria Fajri, Venkat Sai Prasad Gouribhatla, Bhanu Prashant Baddipadiga, and Mehdi Ferdowsi. A dc–dc converter with high voltage gain and two input boost stages. *IEEE Transactions on Power Electronics*, 31(6):4206–4215, 2016.

[53] Rong-Jong Wai, Chung-You Lin, Rou-Yong Duan, and Yung-Ruei Chang. High-efficiency dc-dc converter with high voltage gain and reduced switch stress. *IEEE Transactions on Industrial Electronics*, 54(1):354–364, 2007.

[54] Lung-Sheng Yang, Tsorng-Juu Liang, and Jiann-Fuh Chen. Transformerless dc–dc converters with high step-up voltage gain. *IEEE Transactions on Industrial Electronics*, 56(8):3144–3152, 2009.

[55] Qun Zhao and Fred C Lee. High-efficiency, high step-up dc-dc converters. *IEEE Transactions on Power Electronics*, 18(1):65–73, 2003.

[56] Shih-Ming Chen, Tsorng-Juu Liang, Lung-Sheng Yang, and Jiann-Fuh Chen. A cascaded high step-up dc–dc converter with single switch for microsource applications. *IEEE Transactions on Power Electronics*, 26(4):1146–1153, 2011.

[57] Nicholas Denniston, Ahmed M Massoud, Shehab Ahmed, and Prasad N Enjeti. Multiple-module high-gain high-voltage dc–dc transformers for offshore wind energy systems. *IEEE Transactions on Industrial Electronics*, 58(5):1877–1886, 2011.

[58] Zhigang Liang, Rong Guo, Jun Li, and Alex Q Huang. A high-efficiency pv module-integrated dc/dc converter for pv energy harvest in freedm systems. *IEEE Transactions on Power Electronics*, 26(3):897–909, 2011.

[59] Boris Axelrod, Yefim Berkovich, and Adrian Ioinovici. Transformerless dc-dc converters with a very high dc line-to-load voltage ratio. In *Circuits and Systems, 2003. ISCAS'03. Proceedings of the 2003 International Symposium on*, volume 3, pages III–III. IEEE, 2003.

[60] Suman Dwari and Leila Parsa. An efficient high-step-up interleaved dc–dc converter with a common active clamp. *IEEE Transactions on Power Electronics*, 26(1):66–78, 2011.

[61] Tsai-Fu Wu, Yung-Chu Chen, Jeng-Gung Yang, and Chia-Ling Kuo. Isolated bidirectional full-bridge dc–dc converter with a flyback snubber. *IEEE Transactions on Power Electronics*, 25(7):1915–1922, 2010.

[62] Felinto SF Silva, Antônio AA Freitas, Sérgio Daher, Saulo C Ximenes, Sarah KA Sousa, MS Edilson, Fernando LM Antunes, and Cícero MT Cruz. High gain dc-dc boost converter with a coupling inductor. In *Power Electronics Conference, 2009. COBEP'09. Brazilian*, pages 486–492. IEEE, 2009.

[63] Venkata Yaramasu and Bin Wu. Three-level boost converter based medium voltage megawatt pmsg wind energy conversion systems. In *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, pages 561–567. IEEE, 2011.

[64] Robert W Erickson and Dragan Maksimovic. *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

[65] F. L. Tofoli, D. de Souza Oliveira, R. P. Torrico-Bascopé, and Y. J. A. Alcazar. Novel nonisolated high-voltage gain dc-dc converters based on 3ssc and vmc. *IEEE Transactions on Power Electronics*, 27(9):3897–3907, Sept 2012. ISSN 0885-8993. doi: 10.1109/TPEL.2012.2190943.

[66] F. L. Tofoli, D. d. C. Pereira, W. Josias de Paula, and D. d. S. Oliveira Júnior. Survey on non-isolated high-voltage step-up dc-dc topologies based on the boost converter. *IET Power Electronics*, 8(10):2044–2057, 2015. ISSN 1755-4535. doi: 10.1049/iet-pel.2014.0605.

[67] R. Haroun, A. E. Aroudi, A. Cid-Pastor, G. Garcia, C. Olalla, and L. Martínez-Salamero. Impedance matching in photovoltaic systems using cascaded boost converters and sliding-mode control. *IEEE Transactions on Power Electronics*, 30(6): 3185–3199, June 2015. ISSN 0885-8993. doi: 10.1109/TPEL.2014.2339134.

[68] M. Veerachary and S. B. Sudhakar. Stability analysis of cascaded dc-dc power electronic system. In *2007 7th International Conference on Power Electronics and Drive Systems*, pages 1422–1426, Nov 2007. doi: 10.1109/PEDS.2007.4487890.

[69] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg, and B. Lehman. Step-up dc-dc converters: A comprehensive review of voltage-boosting techniques, topologies, and applications. *IEEE Transactions on Power Electronics*, 32(12):9143–9178, Dec 2017. ISSN 0885-8993. doi: 10.1109/TPEL.2017.2652318.

[70] B. P. R. Baddipadiga, V. A. Prabhala, and M. Ferdowsi. A family of high-voltage-gain dc-dc converters based on a generalized structure. *IEEE Transactions on Power Electronics*, PP(99):1–1, 2017. ISSN 0885-8993. doi: 10.1109/TPEL.2017.2777451.

[71] R. Gules, L. L. Pfitscher, and L. C. Franco. An interleaved boost dc-dc converter with large conversion ratio. In *2003 IEEE International Symposium on Industrial Electronics (Cat. No.03TH8692)*, volume 1, pages 411–416 vol. 1, June 2003. doi: 10.1109/ISIE.2003.1267284.

[72] Ching-Ming Lai, Yuan-Chih Lin, and Dasheng Lee. Study and implementation of a two-phase interleaved bidirectional dc/dc converter for vehicle and dc-microgrid systems. *Energies*, 8(9):9969–9991, 2015.

[73] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules. Voltage multiplier cells applied to non-isolated dc–dc converters. *IEEE Transactions on Power Electronics*, 23(2):871–887, March 2008. ISSN 0885-8993. doi: 10.1109/TPEL.2007.915762.

[74] Pyosoo Kim, Sanghyuk Lee, Junsung Park, and Sewan Choi. High step-up interleaved boost converters using voltage multiplier cells. In *Power Electronics and ECCE Asia (ICPE and ECCE), 2011 IEEE 8th International Conference on*, pages 2844–2851. IEEE, 2011.

[75] W. Li and X. He. Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications. *IEEE Transactions on Industrial Electronics*, 58(4): 1239–1250, April 2011. ISSN 0278-0046. doi: 10.1109/TIE.2010.2049715.

[76] L. Zhou, B. Zhu, Q. Luo, and S. Chen. Interleaved non-isolated high step-up dc/dc converter based on the diode-capacitor multiplier. *IET Power Electronics*, 7(2): 390–397, February 2014. ISSN 1755-4535. doi: 10.1049/iet-pel.2013.0124.

[77] Michael O'Loughlin. An interleaving pfc pre-regulator for high-power converters. *Texas Instruments*, pages 1–14, 2006.

[78] J. Roy and R. Ayyanar. Sensor-less current sharing over wide operating range for extended-duty-ratio boost converter. *IEEE Transactions on Power Electronics*, 32 (11):8763–8777, Nov 2017. ISSN 0885-8993. doi: 10.1109/TPEL.2016.2640319.

[79] T. Nouri, S. H. Hosseini, E. Babaei, and J. Ebrahimi. Generalised transformerless ultra step-up dc–dc converter with reduced voltage stress on semiconductors. *IET Power Electronics*, 7(11):2791–2805, 2014. ISSN 1755-4535. doi: 10.1049/iet-pel.2013.0933.

[80] E. H. Ismail, M. A. Al-Saffar, and A. J. Sabzali. High conversion ratio dc–dc converters with reduced switch stress. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 55(7):2139–2151, Aug 2008. ISSN 1549-8328. doi: 10.1109/TCSI.2008.918195.

[81] Julio Cesar Rosas-Caro, Jonathan Carlos Mayo-Maldonado, Ruben Salas-Cabrera, Aaron Gonzalez-Rodriguez, Eduardo Nacu Salas-Cabrera, and Rodolfo Castillo-Ibarra. A family of dc-dc multiplier converters. *Engineering Letters*, 19(1):57–67, 2011.

[82] Y. J. A. Alcazar, D. de Souza Oliveira, F. L. Tofoli, and R. P. Torrico-Bascopé. Dc–dc nonisolated boost converter based on the three-state switching cell and voltage multiplier cells. *IEEE Transactions on Industrial Electronics*, 60(10):4438–4449, Oct 2013. ISSN 0278-0046. doi: 10.1109/TIE.2012.2213555.

[83] Mustafa A Al-Saffar and Esam H Ismail. A high voltage ratio and low stress dc–dc converter with reduced input current ripple for fuel cell source. *Renewable Energy*, 82:35–43, 2015.

[84] Abbas A Fardoun, Esam H Ismail, Ahmad J Sabzali, and Mustafa A Al-Saffar. Bidirectional converter for high-efficiency fuel cell powertrain. *Journal of Power Sources*, 249:470–482, 2014.

[85] A. Alzahrani, P. Shamsi, and M. Ferdowsi. A novel non-isolated high-gain dc-dc boost converter. In *2017 North American Power Symposium (NAPS)*, pages 1–6, Sept 2017. doi: 10.1109/NAPS.2017.8107216.

[86] A. Alzahrani, P. Shamsi, and M. Ferdowsi. An interleaved non-isolated dc-dc boost converter with diode-capacitor cells. In *2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA)*, pages 216–221, Nov 2017. doi: 10.1109/ICRERA.2017.8191269.

[87] Lukas Müller and Jonathan W Kimball. High gain dc–dc converter based on the cockcroft–walton multiplier. *IEEE Transactions on Power Electronics*, 31(9):6405–6415, 2016.

[88] B. P. Baddipadiga and M. Ferdowsi. A high-voltage-gain dc-dc converter based on modified dickson charge pump voltage multiplier. *IEEE Transactions on Power Electronics*, 32(10):7707–7715, Oct 2017. ISSN 0885-8993. doi: 10.1109/TPEL.2016.2594016.

[89] New hikari supercomputer starts solar hvdc. `https://www.tacc.utexas.edu`. (Accessed on 02/12/2018).

[90] M. E. Baran and N. R. Mahajan. Dc distribution for industrial systems: opportunities and challenges. *IEEE Transactions on Industry Applications*, 39(6):1596–1601, Nov 2003. ISSN 0093-9994. doi: 10.1109/TIA.2003.818969.

[91] J. G. Ciezki and R. W. Ashton. Selection and stability issues associated with a navy shipboard dc zonal electric distribution system. *IEEE Transactions on Power Delivery*, 15(2):665–669, Apr 2000. ISSN 0885-8977. doi: 10.1109/61.853002.

[92] A. Stupar, T. Friedli, J. Minibock, and J. W. Kolar. Towards a 99% efficient three-phase buck-type pfc rectifier for 400-v dc distribution systems. *IEEE Transactions on Power Electronics*, 27(4):1732–1744, April 2012. ISSN 0885-8993. doi: 10.1109/TPEL.2011.2166406.

[93] Y. Sato, Y. Tanaka, A. Fukui, M. Yamasaki, and H. Ohashi. Sic-sit circuit breakers with controllable interruption voltage for 400-v dc distribution systems. *IEEE Transactions on Power Electronics*, 29(5):2597–2605, May 2014. ISSN 0885-8993. doi: 10.1109/TPEL.2013.2274464.

[94] M. Kasper, D. Bortis, T. Friedli, and J. W. Kolar. Classification and comparative evaluation of pv panel integrated dc-dc converter concepts. In *Power Electronics and Motion Control Conference (EPE/PEMC), 2012 15th International*, pages LS1e.4–1–LS1e.4–8, Sept 2012. doi: 10.1109/EPEPEMC.2012.6397403.

[95] F. L. Tofoli, D. d. C. Pereira, W. Josias de Paula, and D. d. S. Oliveira Júnior. Survey on non-isolated high-voltage step-up dc-dc topologies based on the boost converter. *IET Power Electronics*, 8(10):2044–2057, 2015. ISSN 1755-4535. doi: 10.1049/iet-pel.2014.0605.

[96] B. C. Barry, J. G. Hayes, and M. S. Ryłko. Ccm and dcm operation of the interleaved two-phase boost converter with discrete and coupled inductors. *IEEE Transactions on Power Electronics*, 30(12):6551–6567, Dec 2015. ISSN 0885-8993. doi: 10.1109/TPEL.2014.2386778.

[97] R. N. A. L. e Silva Aquino, F. L. Tofoli, P. P. Praca, D. d. S. Oliveira, and L. H. S. C. Barreto. Soft switching high-voltage gain dc-dc interleaved boost converter. *IET Power Electronics*, 8(1):120–129, 2015. ISSN 1755-4535. doi: 10.1049/iet-pel.2014.0275.

[98] L. Huber and M. M. Jovanovic. A design approach for server power supplies for networking applications. In *APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.00CH37058)*, volume 2, pages 1163–1169 vol.2, 2000. doi: 10.1109/APEC.2000.822834.

[99] Y. Gu, D. Zhang, X. Wu, and X. Zhang. Research on stability improvement of the cascaded dc-dc converters based on ac signal sampling control method. *IEEE Transactions on Power Electronics*, 33(5):4547–4559, May 2018. ISSN 0885-8993. doi: 10.1109/TPEL.2017.2724580.

[100] M. T. Zhang, Yimin Jiang, F. C. Lee, and M. M. Jovanovic. Single-phase three-level boost power factor correction converter. In *Applied Power Electronics Conference and Exposition, 1995. APEC '95. Conference Proceedings 1995., Tenth Annual*, number 0, pages 434–439 vol.1, Mar 1995. doi: 10.1109/APEC.1995.468984.

[101] H. C. Chen and W. J. Lin. Mppt and voltage balancing control with sensing only inductor current for photovoltaic-fed, three-level, boost-type converters. *IEEE Transactions on Power Electronics*, 29(1):29–35, Jan 2014. ISSN 0885-8993. doi: 10.1109/TPEL.2013.2262056.

[102] Y. Zhang, J. T. Sun, and Y. F. Wang. Hybrid boost three-level dc-dc converter with high voltage gain for photovoltaic generation systems. *IEEE Transactions on Power Electronics*, 28(8):3659–3664, Aug 2013. ISSN 0885-8993. doi: 10.1109/TPEL.2012.2229720.

[103] Q. M. Li and F. C. Lee. Design consideration of the active-clamp forward converter with current mode control during large-signal transient. *IEEE Transactions on Power Electronics*, 18(4):958–965, July 2003. ISSN 0885-8993. doi: 10.1109/TPEL.2003.813760.

[104] R. Ayyanar and N. Mohan. Novel soft-switching dc-dc converter with full zvs-range and reduced filter requirement. i. regulated-output applications. *IEEE Transactions on Power Electronics*, 16(2):184–192, Mar 2001. ISSN 0885-8993. doi: 10.1109/63.911142.

[105] K. C. Tseng and C. C. Huang. High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system. *IEEE Transactions on Industrial Electronics*, 61(3):1311–1319, March 2014. ISSN 0278-0046. doi: 10.1109/TIE.2013.2261036.

[106] A. Abramovitz, T. Cheng, and K. Smedley. Analysis and design of forward converter with energy regenerative snubber. *IEEE Transactions on Power Electronics*, 25(3): 667–676, March 2010. ISSN 0885-8993. doi: 10.1109/TPEL.2009.2033275.

[107] G. Spiazzi, P. Mattavelli, and A. Costabeber. High step-up ratio flyback converter with active clamp and voltage multiplier. *IEEE Transactions on Power Electronics*, 26(11):3205–3214, Nov 2011. ISSN 0885-8993. doi: 10.1109/TPEL.2011.2134871.

[108] B. Axelrod, Y. Berkovich, and A. Ioinovici. Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc-dc pwm converters. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 55(2):687–696, March 2008. ISSN 1549-8328. doi: 10.1109/TCSI.2008.916403.

[109] Y. J. A. Alcazar, D. de Souza Oliveira, F. L. Tofoli, and R. P. Torrico-Bascopé. Dc-dc nonisolated boost converter based on the three-state switching cell and voltage multiplier cells. *IEEE Transactions on Industrial Electronics*, 60(10):4438–4449, Oct 2013. ISSN 0278-0046. doi: 10.1109/TIE.2012.2213555.

[110] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano. A dc-dc multilevel boost converter. *IET Power Electronics*, 3(1):129–137, January 2010. ISSN 1755-4535. doi: 10.1049/iet-pel.2008.0253.

[111] B. Wu, S. Li, Y. Liu, and K. Ma Smedley. A new hybrid boosting converter for renewable energy applications. *IEEE Transactions on Power Electronics*, 31(2): 1203–1215, Feb 2016. ISSN 0885-8993. doi: 10.1109/TPEL.2015.2420994.

[112] B. Baddipadiga and M. Ferdowsi. A high-voltage-gain dc-dc converter based on modified dickson charge pump voltage multiplier. *IEEE Transactions on Power Electronics*, PP(99):1–1, 2016. ISSN 0885-8993. doi: 10.1109/TPEL.2016.2594016.

[113] V. A. K. Prabhala, P. Fajri, V. S. P. Gouribhatla, B. P. Baddipadiga, and M. Ferdowsi. A dc-dc converter with high voltage gain and two input boost stages. *IEEE Transactions on Power Electronics*, 31(6):4206–4215, June 2016. ISSN 0885-8993. doi: 10.1109/TPEL.2015.2476377.

[114] G. Palumbo and D. Pappalardo. Charge pump circuits: An overview on design strategies and topologies. *IEEE Circuits and Systems Magazine*, 10(1):31–45, First 2010. ISSN 1531-636X. doi: 10.1109/MCAS.2009.935695.

[115] Y. Lei, R. May, and R. Pilawa-Podgurski. Split-phase control: Achieving complete soft-charging operation of a dickson switched-capacitor converter. *IEEE Transactions on Power Electronics*, 31(1):770–782, Jan 2016. ISSN 0885-8993. doi: 10.1109/TPEL.2015.2403715.

[116] A. Alzahrani, P. Shamsi, and M. Ferdowsi. Analysis and design of bipolar dickson dc-dc converter. In *2017 IEEE Power and Energy Conference at Illinois (PECI)*, pages 1–6, Feb 2017. doi: 10.1109/PECI.2017.7935733.

[117] A. Alzahrani, P. Shamsi, and M. Ferdowsi. Boost converter with bipolar dickson voltage multiplier cells. In *2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA)*, pages 228–233, Nov 2017. doi: 10.1109/ICRERA.2017.8191271.

[118] I. G. Hansen and G. R. Sundberg. Space station $20 - khz$ power management and distribution system. In *1986 17th Annual IEEE Power Electronics Specialists Conference*, pages 676–683, June 1986. doi: 10.1109/PESC.1986.7415623.

[119] A. Alzahrani, P. Shamsi, and M. Ferdowsi. A novel interleaved non-isolated high-gain dc-dc boost converter with greinacher voltage multiplier cells. In *2017 IEEE 6th International Conference on Renewable Energy Research and Applications (ICRERA)*, pages 222–227, Nov 2017. doi: 10.1109/ICRERA.2017.8191270.

[120] C. T. Pan, C. F. Chuang, and C. C. Chu. A novel transformer-less adaptable voltage quadrupler dc converter with low switch voltage stress. *IEEE Transactions on Power Electronics*, 29(9):4787–4796, Sept 2014. ISSN 0885-8993. doi: 10.1109/TPEL.2013.2287020.

[121] Y. Xiong, S. Sun, H. Jia, P. Shea, and Z. John Shen. New physical insights on power mosfet switching losses. *IEEE Transactions on Power Electronics*, 24(2):525–531, Feb 2009. ISSN 0885-8993. doi: 10.1109/TPEL.2008.2006567.

[122] S. D. Johnson, A. F. Witulski, and R. W. Erickson. Comparison of resonant topologies in high-voltage dc applications. *IEEE Transactions on Aerospace and Electronic Systems*, 24(3):263–274, May 1988. ISSN 0018-9251. doi: 10.1109/7.192094.

[123] A. Chub, D. Vinnikov, F. Blaabjerg, and F. Z. Peng. A review of galvanically isolated impedance-source dc-dc converters. *IEEE Transactions on Power Electronics*, 31 (4):2808–2828, April 2016. ISSN 0885-8993. doi: 10.1109/TPEL.2015.2453128.

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